A Dual-Polarization Receiver for Multi-Beam Interferometry

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Did You Have Fun?

Andrew Munro
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Abstract

Superconductor/Insulator/Superconductor (SIS) mixers are today the best heterodyne receivers for detecting astronomical signals in the range from 100 GHz to 1 THz. Existing receivers have noise performance approaching the fundamental quantum limit, but large format arrays have not yet been realised. Developing large format arrays is, therefore, the most efficient method for increasing the observational speed.

In this thesis, we describe the development of a planar dual-polarisation SIS receiver. The integration of the receiver circuit on the chip with the SIS mixers for both polarisations simplifies the receiver architecture. Upon this more compact receiver design, extending to a large focal plane array with a high pixel count is simplified. The cost of this simplified receiver is the need for the development of more complicated on-chip circuits. We demonstrate this technology development in the frequency band of the wideband Submillimetre Array (wSMA) low band from 190 GHz to 290 GHz. The dual-polarisation receiver chip with a size of 4.0 mm by 4.1 mm comprises a polarisation splitting 4-probe orthomode transducer (OMT) and the mixers for each polarisation. All planar circuits are fabricated on the same quartz chip alongside some auxiliary circuits needed to connect the OMT with the mixers. We use the twin junction tuning scheme because it offers a compact and robust way of matching the highly capacitive SIS junctions.

As part of this development, we investigate the twin-junction tuning to improve the matching to the feeding RF circuit during the design phase. Furthermore, we extended existing techniques of embedding impedance recovery to apply to twin junction mixers to have a reliable tool to test our integrated receiver experimentally.

Based on these ideas, we designed an on-chip dual polarisation receiver, deployed it in a test setup and finally characterised the receiver. We describe in detail the test setup, including the 40 mm by 40 mm mixer block, which reserves margins on the size for the IF board and the magnetic bias options, and allows the extension into a 2×2-pixel 70 mm by 70 mm array. The preliminary experimental results we obtained with a single receiver chip demonstrate that sufficient local oscillator (LO)

power can be coupled on the receiver chip, and it lines out a procedure for testing and characterising the receiver.

In addition, we present the design of a two-pixel balanced dual-polarisation receiver with an on-chip LO distribution. The design uses the same method we employed for the receiver chip described above but has the capability of rejecting LO noise. This design allows the construction of large format SIS receiver arrays with an improved noise temperature performance.

Declaration statement

The work presented in this thesis has been conducted by myself between October 2019 and October 2023 under the supervision of Boon Kok Tan and Ghassan Yassin unless otherwise stated. Faouzi Boussaha and Christine Chaumont fabricated the SIS devices at the Observatoire de Paris. The personal pronoun 'we' is used instead of 'I' as the academic writing standard.

This document has been compiled from documents, presentations and publications we prepared during this period. A time-ordered overview of publicly accessible documents is:

1. J. Wenninger, F. Boussaha, C. Chaumont, B. K. Tan, and G. Yassin, "Design of a 240 GHz On-Chip Dual-Polarization Receiver for SIS Mixer Arrays," *Superconductor Science and Technology*, 2023
2. J. Wenninger, G. Yassin, and B. K. Tan, "Analytical expressions for the design of twin junction tuning in SIS mixers," *Engineering Research Express*, 2023
3. J. Wenninger, F. Boussaha, C. Chaumont, B. K. Tan, and G. Yassin, "Preliminary Characterisation of a Compact 240 GHz SIS Dual-Polarisation Receiver for Large Array Applications," in *32nd IEEE International Symposium on Space Terahertz Technology*, 2022
4. J. Wenninger, C. Chaumont, F. Boussaha, and B.-K. Tan, "Design of an on-chip integrated 230 GHz dual-polarization balanced SIS receiver for multi-pixel array applications," in *Millimeter, Submillimeter, and Far-Infrared Detectors and Instrumentation for Astronomy XI*, vol. 12190, pp. 1190–1202, SPIE, 2022
5. J. Wenninger, F. Boussaha, B.-K. Tan, and G. Yassin, "Development of a Compact 240 GHz Dual-Polarisation SIS Receiver for Large Focal Plane Array Applications ." Presentation at The Future of Airborne Infrared/Submm Astronomy: Instrument Solutions Workshop, 2021
6. B. K. Tan, J. Wenninger, P. Kittara, P. Noptosporn, P. Jaroenjittichai, D. Singwong, I. G. Bernete, C. Chaumont, and F. Boussaha, "Design of a 350 GHz Circular Waveguide Superconductor-Insulator-Superconductor Mixer for Array Applica-

tions," in *32nd IEEE International Symposium on Space Terahertz Technology*, 2022

These research outputs have been included in this thesis:

Chapter 1 is an extended summary of all introductions we used in papers and yearly reports in the department. Specifically, the thesis outline section largely reproduces abstracts of papers.

Chapter 2 reiterates mostly Tucker's theory, which can be found in many theses on SIS receivers. We wrote this chapter independently in my own words. However, it occurred later that similar wording can be found in existing theses, as there are limited ways of explaining such a complex theory.

Chapter 3 is peer-reviewed, published in IOP Engineering Research Express, and extended by some equations to clarify derivations.

Chapter 4 is in preparation to enter the peer-review process.

Chapter 5 is peer-reviewed and published in IOP Superconductor Science and Technology with minimal changes in the wording.

Chapter 6 contains the receiver block and multi-pixel extension, published in IOP Superconductor Science and Technology and the IEEE International Symposium on Space Terahertz Technology (ISSTT) 2022 conference proceedings and discussed in the second-year report. The receiver preparation is also part of submissions to the ISSTT 2022 conference.

Chapter 7 is largely published in the IEEE ISSTT 2022 conference proceedings and extended by detailed DC characterisation results.

Chapter 8 is published in the SPIE Astronomical Telescopes and Instrumentation conference proceedings paper.

Chapter 9 largely reuses parts of the individual papers.

COVID-19 Pandemic

The project progress has been severely affected by UK governmental lockdowns, departmental restrictions and other pandemic-related measures even after lifting these constraints due to backlogs:

- Lab access was limited;
- Electrical and mechanical workshop and supporting facilities were closed;
- Extended lead times on commercial products and supply shortages;
- Fabrication facilities in France had the same difficulties as listed above;

Nitrogen and Helium supplies were interrupted for four academic terms when lab access and experiments were possible.

The steps mitigating the impact on the progress were a shift towards extensive HFSS simulations during the pandemic and a six-month extension to the maximum submission date, which is four years for DPhil students at the University of Oxford.

Jakob Wenninger
(*October 2023*)

Acknowledgements

I am grateful to my two supervisors, Professor Ghassan Yassin and Dr. Boon Kok Tan, for providing me with guidance, support and valuable feedback. The combination of theoretical and practical approaches made my degree a unique experience. Further, I am very grateful for the sustained mixer fabrication efforts of Faouzi Boussaha and Christine Chaumont. Similarly, big thanks to Rik Elliot for the help in the lab, from building electronics to any of my ideas and to Paul Pattinson for all the different trainings. From within the research group, I owe a lot to Joseph Longden and Javier Navarro for fostering the PhD process in the daily Balliol lunch discussions.

I thank David Smith for designing the bias circuit, Mark Merritt for thinning my quartz dices at RAL and Daniel Gardener for machining the mixer block. Not to forget Ashling Gordon and Leanne O'Donnell for protecting me from behind the scenes from too much administration; thank you. I am also grateful to Andrey Baryshev and Dimitra Rigopoulou for examining me at the end of my postgrad and Christian Holler for sending me off on this academic journey during my undergrad.

Likewise, I want to thank Michael Schöwel for sparking my interest in engineering and the introduction to mechanical engineering; judge it on my mixer block designs. I also thank my office mates, in particular Tobias Geron, who finally met a bear. I am very grateful for all the time and adventures with Risto Martin, through whom I got to know many friends, in particular Haydn Ingram, who will become Bar Billiard champion not only due to demographics, and Hasan Muhammed, through whom I know Léa Schwartz; Thank you for all these good feelings.

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Lastly, I thank my family for all the support over the last eight years of studying, without which this would have been impossible. Thank you – I am back home now!

Contents

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Abbreviations

2SB	Sideband Separating
AC	Alternating Current
ALMA	Atacama Large Millimetre/submillimetre Array
BPF	Bandpass Filter
CHAI	CCAT-Prime Heterodyne Instrument
CPW	Coplanar Waveguide
DAQ	Data Acquisition
DC	Direct Current
DSB	Double Sideband
FEM	Finite-Element Method
FOV	Field of View
HERA	HEterodyne Receiver Array
HPI	Hybrid Planar Integration
JCMT	James Clerk Maxwell Telescope
IF	Intermediate Frequency
IC	Integrated Circuit
KAPPa	Kilopixel Array Pathfinder Project
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Lowpass Filter
LSB	Lower Sideband
NI	Natoinal Instruments
NOEMA	Northern Extended Millimeter Array
OMT	Orthomode Transducer
Pol.	Polarisation
RF	Radio Frequency
RIE	Reactive Ion Etching
S	Scattering
SIS	Superconductor/Insulator/Superconductor
SoI	Silicon-on-Insulator
SSB	Single Sideband
USB	Upper Sideband
VNA	Vector Spectrum Analyser
wSMA	wideband Submillimetre Array

Chapter 1

Introduction

The goal of this DPhil project is to develop an on-chip dual-polarisation Superconductor-Insulator-Superconductor (SIS) receiver for sub-/millimetre (mm)-wave astronomy that is simple to extend to a high-pixel-count focal-plane array and scale to higher operational frequencies. The science community requires large pixel count SIS receivers to increase the observational speed and the field of view (FOV) in order to map large-scale structures at a high spectral resolution.

This chapter first briefly introduces sub-/mm astronomy in the context of incoherent and coherent detectors before describing receiver noise. After introducing the basic frequency conversion in SIS mixers, we then describe SIS receivers. Here, the first part focuses mainly on the extensions required for detecting two polarisations, and the second part describes the extension of SIS receivers into focal plane receiver arrays. Both extensions introduce additional complexity that can be simplified or even made obsolete with superconducting planar circuit technology to replace the 3D waveguide components commonly used. We briefly describe our goals and requirements for an on-chip dual-polarisation receiver solution in Section 1.5. This last section also outlines the chapters of this thesis and the steps undertaken towards achieving a receiver design that allows to accommodate more pixels and, therefore, speeds up sub-/mm-wave observations.

1.1 Sub-/Millimetre Astronomy

Stars are born from accreting interstellar medium, in particular hydrogen gas. When giant stars explode into supernovae, the material fused during the star's lifetime, including all atoms and molecules found on Earth, feedback into the interstellar medium in the form of gas and dust clouds. However, only the emission of the outermost parts

of these processes are observable with visible light since the gas and dust clouds absorb radiation at these frequencies. Consequently, the physics within the lifecycle of the interstellar medium needs to be studied with longer wavelengths in the far-infrared spectrum. Not only can this sub-/mm wavelength radiate through the dust and gas, but it also features unique fingerprints to each atom and molecule, called spectral lines, containing information about the abundance, kinematics and dynamics of atoms and molecules. Hence, the sub-/mm radiation carries vital information for studying the interstellar medium, the cradle and grave of a star.

Incoherent detectors such as transition edge sensors only preserve the amplitude information of the signal without the phase information. Several independent detectors are required for spectrum sampling with incoherent detectors, and incoherent detectors are generally unsuitable for interferometer applications in sub-/mm wavelength.

SIS receivers are coherent detectors, which preserve the amplitude and phase information of the incoming signal, enabling the measurement of spectrum of the incoming signal. The spectral lines in this measurement allow to identify the abundance of specific atoms and molecules and their respective kinematics through spectroscopy, which is vital to the investigation of the interstellar medium mentioned above [7–13]. The amplitude and phase information also facilitates the employment of the interferometry technique to achieve high spatial resolution observations. The advancement of our knowledge in the past few decades with regards to the far infrared spectroscopic Universe in the 100 GHz to 1 THz range, including the direct imaging of the black holes [14, 15], would not be possible without the SIS mixer technology. Modern SIS receivers operating below 1 THz provide near quantum-limited sensitivity, hence approaching fundamental limits in sensitivity and minimising the receiver noise.

The major limiting factor for sub-/mm observations is the relatively small FOV. The FOV of an interferometer is determined by the antenna's primary beam width at half maximum, which is $\propto \lambda/D$, where λ is the wavelength and D is the antenna diameter [13, 16]. Therefore, sub-/mm telescopes have a FOV in the order of 10" in a single pointing. Observations of astronomical targets exceeding this FOV require several pointings combined to the full image with mosaicing techniques. The full image allows for studying the underlying physical processes in the interstellar medium and star formation. However, because observation time is highly competitive and limited, larger survey observation proposals require very strong scientific cases to be carried out. Focal-plane arrays can improve the observational speed because the individual receivers making up the array record a pointing each simultaneously. Hence,

a focal-plane array increases the FOV and speeds up the mosaicing process, which, in turn, allows for carrying out programs to image large-scale structures in the Universe. The caveat to focal-plane arrays, however, is that the individual receivers of the array must have a competitive performance compared to their established single-pixel counterpart.

1.2 Receiver Noise

The sensitivity of coherent detectors is limited by quantum noise due to the Heisenberg principle compared to incoherent detectors, which are background-noise-limited devices [17]. Sub-/mm receiver technology uses the same terminology as radio technology: The noise power P per bandwidth Δf is expressed in terms of equivalent temperature T that causes electrical noise in a conductor. This Johnson-Nyquist noise is

$$\frac{P}{\Delta f} = k_{\mathrm{B}} T \ , \tag{1.1}$$

where k_{B} is Boltzman's constant [18–21]. The detection of amplitude and phase introduces a minimum noise of

$$T_{\mathrm{N}} \geq \frac{hf}{2k_{\mathrm{B}}} = T_{\mathrm{Q}} \ , \tag{1.2}$$

where Planck's constant h, Boltzman's constant k_{B} and the signal frequency f define the noise quantum T_{Q} for detecting a single RF frequency f.

A receiver system is built from a chain of signal-processing components. A typical setup shown in Figure 1.1 comprises telescope optics followed by an antenna, a mixer and a low-noise amplifier (LNA). If each i^{th} component has a noise temperature T_i and a gain G_i associated, as illustrated in Figure 1.2 according to Friis's formulation [22], then the system temperature of the whole receiver is given by

$$T_{\mathrm{sys}} = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + \frac{T_4}{G_1 G_2 G_3} + \frac{T_5}{G_1 G_2 G_3 G_4} + \sum_{i=5}^{n} \frac{T_{i+1}}{\prod_1^i G_i} \ . \tag{1.3}$$

The gain of well-engineered passive components is $G \lessapprox 1$, amplifying the noise contributions of subsequent components. In contrast, the LNA gain is very large $G \gg 1$, which makes noise contributions of subsequent components negligible. For this reason, radio frequency receivers have an LNA connected directly to the antenna. Unfortunately, no sub-/mm LNAs are available, making a low-noise mixing circuit indispensable.

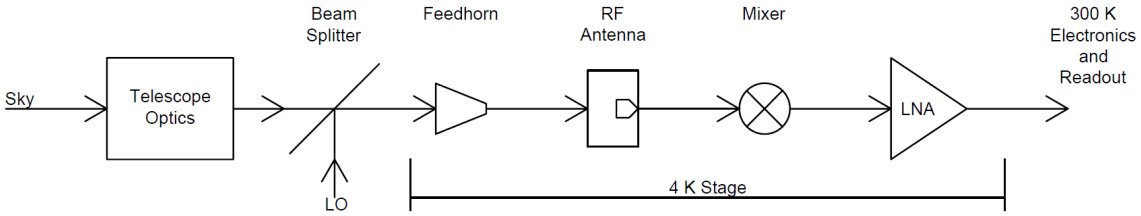


Figure 1.1: An SIS receiver has several components in addition to the SIS junction. First, the telescope optics collimate the sky signal, after which the local oscillator (LO) signal is inserted via a beamsplitter. The feedhorn confines the signal into a waveguide, which contains an antenna that guides the signal onto planar circuits. These transmission lines route the signal to the SIS junction, where the sky and LO signals are mixed and downconverted to the intermediate frequency (IF) range. Finally, a low noise amplifier (LNA) amplifies the IF signal before the signal is routed to the readout electronics at room temperature.

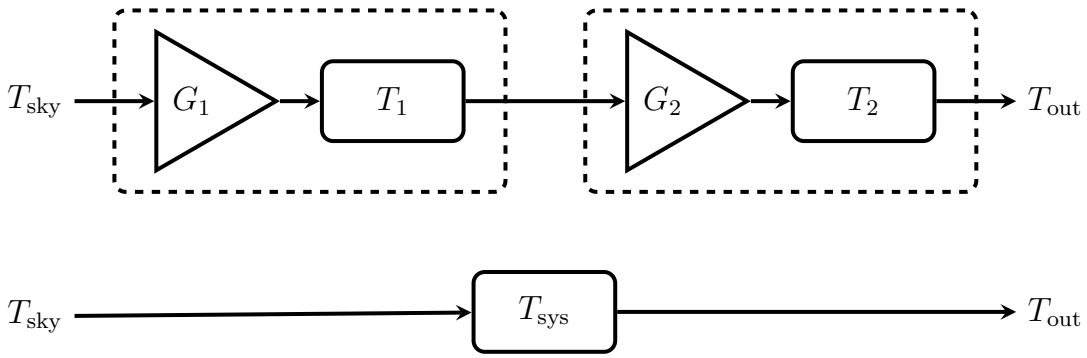


Figure 1.2: The system temperature T_{sys} is an equivalent representing the individual components of the receiver which each has a gain G_i associated and adds a noise equivalent temperature T_i to the signal from the sky T_{sky}.

Considering the faintness of the astronomical spectral features, very sensitive receivers performing the downconversion are required. In fact, state-of-the-art sub-/mm receiver sensitivities have already approached the quantum limit [23–25]. Nonetheless, depending on the apparent brightness of the signal, these receivers still require hours of integration time to recover spectral-line information from a target. The Dicke radiometer equation defines the temperature equivalent signal power per bandwidth Δf of a source that needs to be exceeded to be detectable

$$T_{\mathrm{det}} = \frac{T_{\mathrm{sys}}}{\sqrt{\tau \Delta f}} \tag{1.4}$$

in an integration time τ with a given receiver system temperature T_{sys} [21]. Consequently, observations of extended large-scale structures in the Universe become very time-consuming and costly, requiring resources that could be formidable for an observatory to accept the observation proposal.

1.3 Frequency Conversion

Detecting the spectral-line information in the far-infrared regime builds upon a technique called frequency mixing, downconverting a high-frequency signal into lower frequencies that can be amplified and processed by standard electronics. This frequency conversion is necessary because no electronic readout devices operate at such high frequencies. For example, a 300 GHz signal is mixed with a sinusoidal signal to downconvert it to a 5 GHz signal, where common electronics can digitise and manipulate the signal while preserving the characteristics of the signal, including both amplitude and phase information.

A frequency mixer is a non-linear device that multiplies two signals. The known and controlled signal is a strong sinusoidal, called local oscillator (LO), with which other frequencies get multiplied. The frequency multiplication creates many orders of harmonics, including very high frequencies. Our interest is, in particular, the downconversion of the signal from the sky, called the radio frequency (RF) signal, to the intermediate frequency (IF). These two frequency ranges are represented in Figure 1.3 by a bandpass filter (BPF) defining the RF range and a lowpass filter (LPF) defining the IF range. Thus, the frequency ranges at each connection to the mixer are well-defined without leaving ambiguity where signals propagate or the existence of higher harmonics. The RF and LO signals are mixed within the SIS junction through a non-linear process producing the IF, following the relation

$$f_{\mathrm{IF}} = |f_{\mathrm{RF}} - f_{\mathrm{LO}}| \ , \tag{1.5}$$

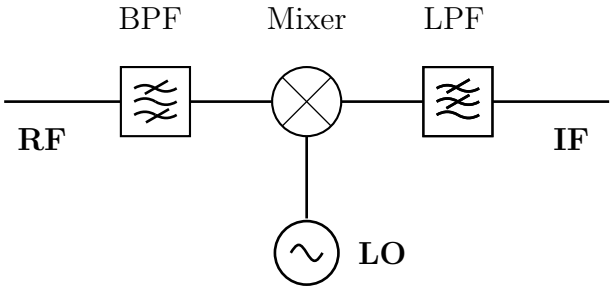


Figure 1.3: The signals of a basic mixer circuit. The RF signal is fed into the mixer via a BPF, which is typically realised in the form of an antenna. The IF signal connects via an LPF to choke RF signals. The LO facilitates the frequency conversion between RF and IF and can also be injected together with the RF through the BPF.

where f denotes the frequency of the signal labelled in the index [26]. The IF signal contains the amplitude and phase information of the RF signal relative to the LO frequency.

Technically, the RF signal above the LO frequency $f_{\mathrm{RF}} > f_{\mathrm{LO}}$ is denoted as the upper sideband (USB), and the RF signal below the LO frequency $f_{\mathrm{RF}} < f_{\mathrm{LO}}$ is denoted as the lower sideband (LSB), as shown in Figure 1.4. In a double sideband (DSB) receiver, both the USB and LSB will be superimposed in the IF band. There are several techniques to separate USB and LSB signals at the IF region [27]: Tunable bandpass or bandstop filters in the RF circuit can reject an unwanted sideband, allowing for single sideband (SSB) detection. Separating and instantaneous detection of both sidebands in sideband separating (2SB) receivers utilises superposition of phase-shifted signals, which cancel either the LSB or USB at one of the two circuit outputs. The phase-shifting of signals, however, adds complexity, which would complicate the description below.

In a similar way, one can further improve the receiver sensitivity by almost eliminating the LO noise via the balanced mode operation [28]. For balanced operation, two separate mixers embedded within a large waveguide network are required instead of a single mixer, as well as a sophisticated LO injection scheme. The resulting IF signals in the two mixers contain downconverted LO noise, which can be separated from the downconverted RF signal. This scheme, however, further adds to the complexity of the mechanical construction, even for a single-pixel receiver.

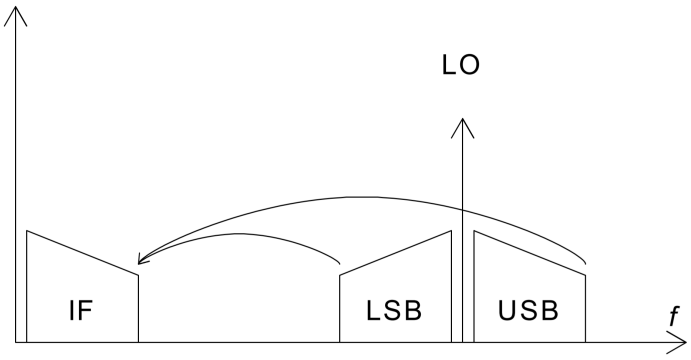


Figure 1.4: The non-linear mixing process downconverts the radio frequency (RF) signal and the local oscillator (LO) into the intermediate frequency (IF) signal. The lower sideband (LSB) represents the RF frequency at lower frequencies than the LO frequency, and the upper sideband (USB) represents the RF signal at higher frequencies than the LO.

1.4 SIS Receivers

A typical single-polarisation SIS receiver is shown in Figure 1.1. The RF signal is collimated by the telescope optics and combined with an LO signal via a beamsplitter. A feedhorn feeds the combined signal into a circular waveguide, and a planar antenna guides the signal from the waveguide onto the chip with the SIS junction. The RF and LO signals are generally in the region of a few hundred gigahertz, while the IF is typically in the microwave region up to 20 GHz, intending to reduce T_{det} according to Equation 1.4 [29–31].

1.4.1 Classical Dual-Polarisation Receiver

The energy and polarisation information of an electromagnetic wave is encoded in the electric and magnetic fields of the wave, which are orthogonal to each other. In order to obtain the full signal power, one needs to detect both polarisations. In addition, the polarisation information is useful in many fields of physics, most famously the detection of B-mode signals in the cosmic microwave background. Therefore, we need to detect both of these polarised fields to retrieve the full energy and the polarisation information of the signal. However, a traditional planar antenna used in an SIS receiver can only detect one polarisation axis. Hence, to construct a dual-polarisation receiver, one requires two identical receivers with the antenna oriented orthogonal to each other.

Most of the SIS receivers deployed at existing sub-/mm observatories are primarily constructed from a stack of two single-polarisation receivers mounted together

to form a single-pixel dual-polarisation SIS receiver. In such a receiver, the two polarisation states are traditionally split with a wire grid or a waveguide orthomode transducer (OMT) [32–39]. The two polarisation states are then fed into the two single-polarisation receivers to recover the polarisation information and the full strength of the astronomical signal. The Atacama Large Millimetre/submillimetre Array (ALMA) observatory has ten receivers for different frequency bands per antenna but only one pixel per receiver. Each receiver acquires the polarisation information of the RF signal by using either wire grids or waveguide OMTs, depending on the frequency band within the receiver cabin [16]. The utilisation of single-polarisation receivers results in a bulky and complex solution which limits the number of pixels within the receiver cartridge and makes it difficult to scale to large focal-plane arrays.

1.4.2 Array Extensions

Multi-pixel array receivers are desired in the astronomy community because the observation time decreases linearly with the number of utilised pixels. For example, doubling the number of pixels could half the observation time. The low pixel count of SIS receivers limits their observational speed and, therefore, the ability to map large-scale structures at the highest spectral resolutions. However, the construction of a large focal-plane multi-pixel SIS array is technically very challenging due to the power consumption and the limited cryogenic cooling power, as well as spatial constraints in the receiver cryostat.

Far-infrared heterodyne receivers typically have a very low pixel count due to the complexity of the cryogenic receiver that requires the integration of many components, resulting in bulky and complicated mechanical and electrical components. Ideally, the receiver architecture of the array should be compact and small in size without compromising the quantum-limited performance of the receiver.

The major drawback of SIS receivers is the method of separating the polarisation information with a wire grid or a waveguide OMT and feeding the two polarisation signals into separate SIS mixer receivers, causing a bulky two-polarisation receiver setup, which can be extended only to a few pixels. Consequently, a single-polarisation detecting focal-plane array is easier to construct, avoiding the complexity of the polarisation splitting capabilities. Several multi-pixel focal-plane SIS arrays that detect only a single-polarisation state of the incoming RF wave at a time have been developed [40–44]. The largest focal plane array deployed in a telescope is SuperCam, with 64 single-polarisation detectors [45]. The only other same-sized array is the CCAT-prime Heterodyne instrument (CHAI), which is currently being developed [46, 47].

The detection of a single polarisation in a single observation results not only in the loss of the polarisation information but also in detecting only half of the incident signal power. Consequently, these arrays require special observation techniques, such as imaging the same astronomical target twice with the receiver rotated by 90° to recover the polarisation information, which is also not applicable to all science problems. As a whole, single-polarisation focal-plane arrays are a step towards identifying key developments necessary and understanding certain difficulties. However, these arrays are not applicable for general-purpose observatories like ALMA with dual-polarisation receivers that detect the total incident signal power of both polarisations and the power of each polarisation instantaneously. Thus, for instance, changing conditions between two observations, like weather changes, have no impact.

A handful of dual-polarisation array concepts exist [36, 42]. The HEterodyne Receiver Array (HERA), for example, uses two 3×3 single-polarisation receivers and a wire grid to form a dual-polarisation receiver and similar is planned for its successor [37, 48, 49]. However, extensions of these concepts to even larger arrays prove difficult since their layout typically occupies space on all sides, making array extensions complicated. Hence, it is vital to locate all accesses at the front and the rear face of the pixel, leaving the four adjacent sides unobscured to attach additional pixels, as illustrated in Figure 1.5. Although it is challenging to connect all quantities for the mixer operation via two surfaces, similar to the Kilopixel Array Pathfinder Project (KAPPa) [50], the utilisation of pixel units following this concept enables a straightforward extension of a single-pixel receiver into a multi-pixel array. In fact, KAPPa addresses many challenges associated with focal plane array extensions, but it is, again, a single polarisation receiver.

1.4.3 Existing On-Chip Dual-Polarisation Receiver

The closest design to the receiver developed in this thesis is the 2×2 pixel array shown in Figure 1.6, developed by the National Astronomical Observatory of Japan [51–57]. Each pixel has a separate receiver chip. The receiver chip contains a polarisation splitting OMT and the mixers to downconvert the two polarisations, where the mixers for each polarisation are arranged in a balanced mixer setup, rejecting the LO noise. This balanced setup requires an LO injection scheme, which is realised with an LO antenna connected to the balanced mixer circuit. The two LO antennas of each receiver chip connect to an LO distribution network, which is milled in the block

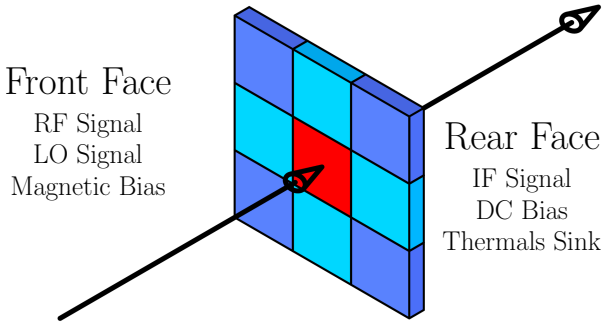


Figure 1.5: An array block configured from nine pixels, which are depicted as coloured boxes. The only available accesses to the central red pixel are the front and rear faces of the array.

housing the four receiver chips. The rectangular waveguides are fabricated in split-block technology, where half of a rectangular waveguide is milled in the lower split-block and the other half in the upper split-block. The whole receiver split block comprises three pieces, with the LO distribution network machined between the top and middle block, and the lowest split block holding the receiver chips. The LO is routed through holes with a rectangular footprint in the middle split block. The RF signal is similarly coupled from the feedhorns to the on-chip OMT via holes in the top and middle split block with a square footprint.

Although the receiver has a good performance in the designed frequency range between 125 GHz and 163 GHz design, we identify the following issues with this high-standard receiver:

1. Holes with a rectangular or square footprint act as waveguides. The scaling of rectangular and square waveguides to higher frequencies imposes very high requirements on machining the three-layer receiver block.
2. The LO distribution network, realised with split-block rectangular waveguides, is difficult to scale not only to a higher frequency but also to a higher pixel count.
3. The on-chip circuit is very sophisticated, employing silicon-on-insulator technology and tunnel junctions to form an on-chip power combiner, although the receiver is designed for relatively low frequencies. This degrades the fabrication yield, especially when scaling to higher frequencies.
4. The IF connections and LO injection to the two-by-two pixel demonstrator are along two sides instead of the array's rear. Accordingly, the array can only be extended to an array of two pixels next to each other.

1.5 Thesis Goals and Outline

This DPhil project aims to develop a pathway and the technologies for a compact dual-polarisation SIS multi-pixel array for heterodyne sub-/mm wave astronomy. We aim to build upon previous projects and improve upon those learnings. We identified the following features specific to achieving a multi-pixel array applicable in telescopes, and we ensure to adhere to those principles in our receiver development:

Simplicity is key to avoiding limitations in the fabrication of the receiver. Our proof of concept is designed for a thinned quartz substrate and fabrication with a standard high-yield photolithography fabrication process. The block housing the receiver chip is machined only by milling and drilling techniques. Restricting the block to two parts is the simplest solution to be able to mount the receiver chip inside. Consequently, split-block waveguides are not possible. Instead, drilled circular waveguides and feedhorns link the receiver chip and the focal plane of the telescope. This feature is also vital to scale to higher frequencies. We identify problematic components and technologies to improve and simplify those for future design refinements or high-frequency adaptions.

Integration of the dual-polarisation receiver RF circuit on a single chip increases the compactness, which in turn provides an opportunity for extending to a focal plane array. The RF circuit comprises the OMT and the mixers to downconvert the RF signal of both polarisations. This on-chip integration considerably reduces the footprint required to detect both polarisations, enabling the population of the focal plane with an SIS receiver array in the future. The integration of the LO coupling network is the subsequent step after integrating the RF circuit on the chip.

Arrayability allows for an easy extension into a focal plane array. There is the possibility to form an array from individual receiver chips or to integrate several receivers on a single chip. The receiver chips sit within the mixer block with blank sides, making the extension to an array straightforward, following the conceptual drawing in Figure 1.5. Any additions required for the receiver operation, such as the magnetic bias, need to fit the footprint of the receiver. Consequently, a large focal-plane array can be populated after refining a prototype design.

There are three major milestones in achieving the above-mentioned goals: First, the design of a dual-polarisation chip demonstrates a workflow for the development of

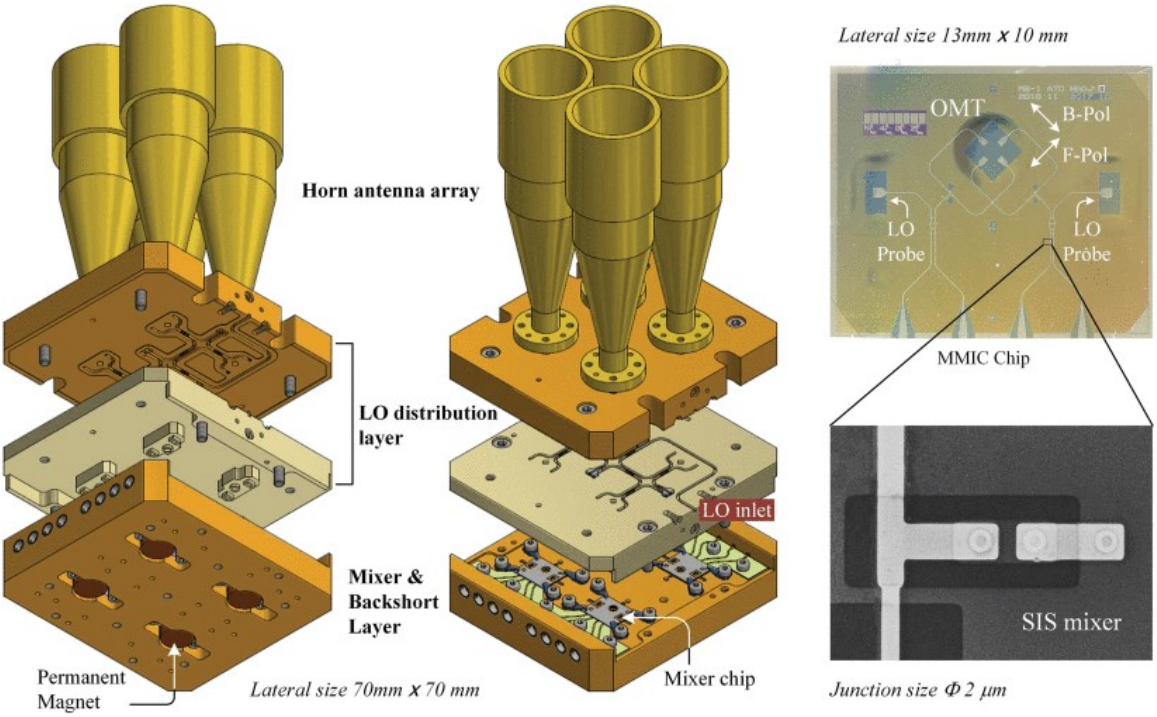


Figure 1.6: The 2×2 pixel array of the National Astronomical Observatory of Japan with an RF bandwidth from 125 GHz to 163 GHz. The receiver is formed from four receiver chips in a three-part split-block. The receiver chip sits in the bottom split block and contains a network to separate the two RF polarisations, the mixers for the two polarisations and the network to inject the LO in an LO-noise-rejecting balanced mixer scheme. The LO signal is distributed to the mixers of each polarisation of each pixel via a split-block rectangular waveguide network milled in the top and middle blocks. The LO-distribution network has six six-branch line couplers and eight waveguide terminations to distribute the LO power evenly between the individual mixers. Original image published by W. Shan, S. Ezaki, H. Kang, A. Gonzalez, T. Kojima, and Y. Uzawa, "A compact superconducting heterodyne focal plane array implemented with HPI (Hybrid Planar Integration) scheme," *IEEE Transactions on Terahertz Science and Technology*, 2020.

the underlying superconducting circuit technology required to develop a state-of-the-art dual-polarisation mixer. Second, the fabrication and test of these receiver chips mounted on a single-pixel mixer block show the feasibility and unforeseen difficulties with the on-chip circuit. Finally, these single-pixel mixer chips will be populated into a 4-pixel dual-polarisation array block to demonstrate a 4-pixel array setup.

We chose to demonstrate the feasibility of the dual-polarisation receiver in the frequency range of 190 GHz to 290 GHz, the low band of the wideband Submillimetre Array (wSMA) with an IF bandwidth from 4 GHz to 20 GHz and an LO range from 210 GHz to 270 GHz [58–60], which also coincides with many other receiver bands of other telescopes such as Band 6 of ALMA [23], Band 3 of the Northern Extended Millimeter Array (NOEMA) [33] and the Receiver A (RxA) of the James Clerk Maxwell Telescope (JCMT) [61].

The following list outlines the content of the individual chapters and their contribution to achieving the goals of this thesis:

Chapter 2, Mixer Theory We introduce SIS junctions, photon-assisted tunnelling and a brief introduction to SIS mixer theory. We first introduce superconductivity and then the SIS junction as a thin insulator barrier sandwiched between two superconductors. The description of the SIS junction is split into a graphical description with the semiconductor picture, illustrating the different tunnelling mechanisms, and a theoretical description, giving a brief summary of Tucker's theory required in later chapters.

Chapter 3, Reflection Coefficient Analysis of Twin Junction Tuning We derive general analytical expressions for matching the complex impedance of the feeding RF circuit to a twin junction device in SIS mixers. A unique feature of our analysis is that it allows for junctions of different admittance and an RF circuit with complex admittance. This provides important design flexibility and accommodates device fabrication tolerances. We then focus on special cases of identical junctions, in particular those cases that yield simple expressions for matching the twin junction to a real impedance. Finally, we derive design curves that allow the determination of the twin junction parameters for a given complex impedance of the feeding circuit. These curves allow the designer to choose different solutions than the commonly used quarter-wavelength transmission line separating the two SIS junctions, which our analysis shows is not always the optimal solution. Moreover, even when commercial software is used for designing the circuits, our analytical equations will act as an

important guide to understanding the physics and guide the designer to the optimal solution.

Chapter 4, Embedding Impedance Recovery The embedding impedance recovery is vital to compare the measured mixer performance with simulations. Although the twin-junction tuning technique is common, twin-junctions lack a method to recover the embedding impedance for a performance check. We first reiterate the established single junction case, detailing four distinct methods and discussing differences between these methods and common features and weaknesses. Upon this basis, we derive and adapt the equation set to the twin junction tuning circuit. We then describe special cases with the aim of justifying our derivations and also linking to Chapter 3. We then introduce some simplifications and assumptions with respect to the fabricated device. We present the impedance recovery of a real twin-junction receiver in the same structure as the single-junction introduction to this chapter, first, with the simplification of neglecting the IF circuit and, then with accounting for the IF circuit. Finally, we apply our embedding impedance recovery technique on another twin-junction mixer operating at higher frequencies.

Chapter 5, Single-Pixel On-Chip Dual-Polarization Receiver Design We present the design of a compact dual-polarisation on-chip SIS receiver covering the wSMA low band from 190 GHz to 290 GHz. After an introductory receiver overview, we introduce the five circuit elements, which have the following functions in the receiver:

1. A polarisation splitting 4-probe OMT that couples the RF and LO signal from free space to the chip via a drilled feedhorn;
2. Two hybrids that recombine the power of each polarisation from the two sets of orthogonal OMT probes;
3. A crossover that crosses transmission lines carrying different RF polarisations to connect the OMT probes with the hybrids;
4. Four BPFs that isolate the hybrids and mixer circuits where only RF, and also IF and DC signals are present, respectively; and
5. Four twin-junction $Nb/AlO_x/Nb$ mixers with LPF that downconvert the recombined signals to the IF and isolate the IF circuit from the RF signal.

In the two-part design process, the single circuit components are designed individually in the first step and then interconnected in the second step. This second step first interconnects two subsystems, the polarised signal coupling network, comprising

OMT, crossover and two hybrids, and the mixer circuit, comprising BPF, mixer and LPF. These two subsystems are then connected to form the full on-chip receiver chip, for which we also present predictions on the heterodyne performance.

Chapter 6, Experimental Setup We present the experimental setup, which is, first and foremost, the mixer block design. As all of the RF components required to form the receiver are formed using planar circuit technology and fabricated on a single quartz chip, our design significantly simplifies the design of the receiver block. The mixer chip can be housed in a simple split block without any waveguide structure, apart from the feedhorn drilled directly into the copper block using the smooth-walled horn technology. The receiver chip, only 4.0 mm by 4.1 mm in size, is mounted in a simple split block where the feedhorn and the magnetic biasing are located on the front side, and the IF and DC biasing connectors are on the rear side. Therefore, the four adjacent sides of the block are left unobscured for a 2-dimensional extension into a multi-pixel array, for which we present the detailed 4-pixel demonstrator as an example in the second section. The following preparation of the receiver, the mounting of the receiver chip in the block, is the same procedure for the single-pixel and 4-pixel blocks. The fourth section is a detailed design description of the cryostat setup. We then give an overview of the experimental system separated into five subsystems:

1. Quasi-optical feeding system, which are RF components accessible during the experiment;
2. Cryogenic test system, which has several features and connections to room temperature;
3. DC readout, which is important for the characterisation of the SIS junctions;
4. IF readout, which is the signal used in astronomical applications;
5. Data acquisition, which records the experimental data;

Finally, we briefly describe the procedure required to carry out an experiment.

Chapter 7, Experimental Results We summarise the preliminary results obtained from testing the compact dual-polarisation receiver. We first present the DC characterisation, which revealed issues in the fabrication of the devices. The fix to this problem is an increased junction area, which affects the receiver performance. The following section then covers the characterisation of the optical coupling on the second-best device available before experiments were halted. These measurements include coupling an arbitrarily polarised LO signal and an LO signal polarised with

a wire grid. We assess the findings of the RF testing and proceed with identifying causes for the observations in the final section.

Chapter 8, 2-Pixel On-Chip Dual-Polarization Balanced Receiver Design We report the design of a balanced dual-polarisation SIS receiver that is based on the design presented in Chapter 5 and can still be easily extended for large array applications. We achieve this by integrating all of the required RF and LO components on-chip using planar superconducting circuit technology, therefore simplifying the architecture of the receiver block substantially. We first describe the concept of the receiver array before discussing the schematic layout of a 2-pixel demonstrator and the balanced operation terminating LO noise. One major feature of our design is the planar LO injection scheme, which couples the LO with a single on-chip antenna and distributes the LO power via a series of microstrip couplers to the balanced mixers of each polarisation of each pixel. We first describe in detail the design and layout of the additional planar circuit components before combining them into one of the three subsystems:

1. LO distribution network, which is the novel component of this receiver;
2. Polarised signal coupling network, which is largely similar to the previously presented design except for replacing the hybrid with a planar power combiner;
3. Mixer circuit, which is identical to the previously presented design but laid out differently;

We then conclude the chapter with the design of a 2-pixel array demonstrator, illustrating how the balanced SIS mixer and the LO distribution network can be extended to form an even larger array.

Chapter 9, Conclusion The conclusion chapter summarises novel features of this thesis and identifies potential future research.

Chapter 2

SIS Mixer Theory

The heterodyne receivers in astronomy from 100 GHz to 1 THz rely on SIS tunnel junctions that employ quantum-tunnelling effects between two superconductors. Quantum detection occurs via an $\approx 1\,\mathrm{nm}$ thin insulating barrier separating two superconductor electrodes. In this chapter, we describe the theoretical background required to understand the design and characterisation process used in this thesis. First, superconductivity and its effects are introduced before we discuss SIS mixers and describe the associated physics involved in quantum-limited detection at sub-/mm wavelength. First, we present tunnelling with the semiconductor pictures before we continue with the key equations of quantum mixer theory for the DC, large and small signal cases.

2.1 Superconductivity

Superconductors are typically metals or alloys and show characteristics of classical conductors or even insulators above their critical temperature T_c [62, 63]. Once cooled below T_c, the material undergoes a phase transition and its behaviour changes abruptly: No DC resistivity and no magnetic fields are measurable within the superconductor [64–66]. The material-dependent, exponential decay length of external magnetic fields into the superconductors is described as London penetration depth [67]. A comprehensive microscopic theoretical frame of superconductivity that explains all experimental findings of low-temperature superconductivity has been developed by Bardeen, Cooper and Schrieffer to the well-known BCS theory [68].

Below T_c, electrons are paired with opposite spin and equal momentum to form a Cooper pair. The electrons of a Cooper pair bind via lattice interactions that are bigger than the Colomb force that repels two negatively charged electrons. The interaction with the lattice gives the Cooper pair a net binding energy 2Δ, where Δ is

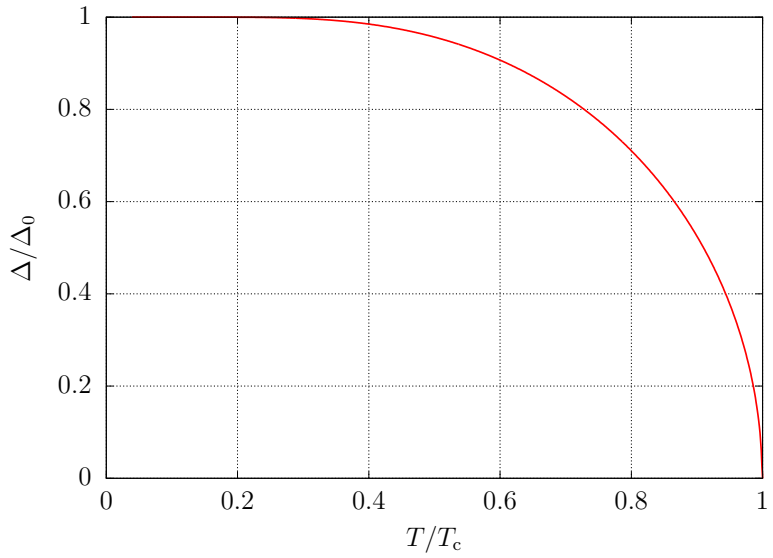


Figure 2.1: The temperature dependence of the Cooper pair binding energy.

the binding energy per electron. Δ is material-dependent since the phonon-mediated attraction depends on the lattice structure.

At zero-temperature $T = 0\,\mathrm{K}$, the binding energy is related to the critical temperature by

$$2\Delta_0 = 3.5 k_\mathrm{B} T_\mathrm{c} \ , \tag{2.1}$$

where k_B is the Boltzmann constant. In many applications, the zero-temperature binding energy is used as an approximation $\Delta(T) \approx \Delta_0$ for temperatures $T < T_\mathrm{c}/2$. Δ_0 and the temperature-dependent value of Δ are obtained from solving the implicit equation

$$\frac{1}{V_\mathrm{eq} N_\mathrm{N}\left(\xi = 0\,\mathrm{eV}\right)} = \int_0^{\hbar\omega_\mathrm{D}} \frac{\tanh\left(\frac{\sqrt{\xi^2+\Delta^2}}{2k_\mathrm{B}T}\right)}{\sqrt{\xi^2+\Delta^2}} \mathrm{d}\xi \ , \tag{2.2}$$

where $\hbar$ is Planck's constant, and are shown in Figure 2.1. The electron-phonon coupling strength is the product of the electron-phonon interaction V_eq and the density of normal states N_N. The integration of the energy relative to the Fermi surface ξ from the Fermi surface to the Debey frequency ω_D sums over all possible phonon energies.

Cooper-pairs can be excited to two quasiparticles by absorbing an energy $E \geq 2\Delta$. Quasiparticles are normal electrons but with a Δ energy gap in their density of states. The energy required to break a Cooper pair into quasiparticles is

$$E^2 = \Delta^2 + \xi^2 \tag{2.3}$$

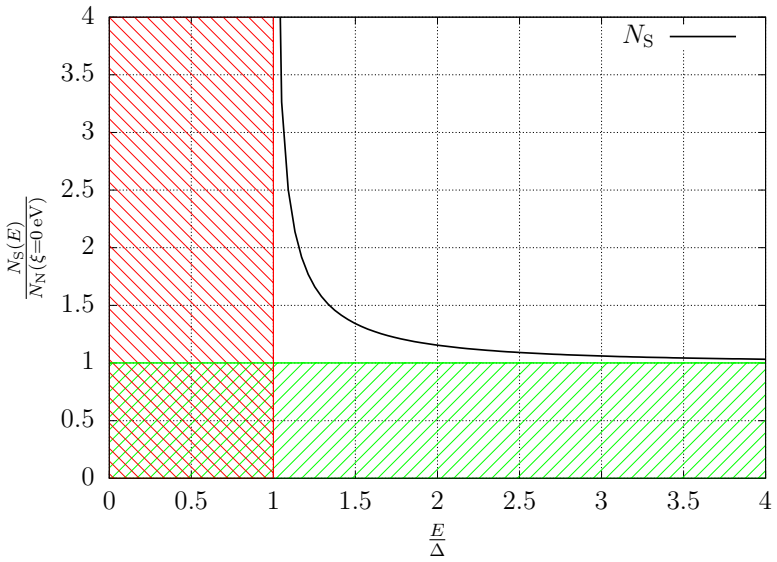


Figure 2.2: The ratio of superconducting over normal state densities depending on the excitation energy. The area hashed green highlights the density of normal states, which would be available without superconductivity. The area hashed red highlights the Cooper pair binding energy, in which no superconducting energy states exist. The Fermi level $\xi = 0\,\mathrm{eV}$ is at $\frac{E}{\Delta} = 0$.

per quasiparticle. Because no quasiparticles are excited for $E < \Delta$, the energy states centred around the Fermi surface are not filled in the 2Δ energy gap of superconductors. For $E \geq \Delta$, the ratio of quasiparticle states per normal states at the Fermi surface is

$$\frac{N_\mathrm{S}(E)}{N_\mathrm{N}(\xi = 0\,\mathrm{eV})} = \frac{E}{\xi} \ , \tag{2.4}$$

as shown in Figure 2.2. The likelihood that one of these energy states is occupied is given by the Fermi-Dirac distribution

$$f(E) = \frac{1}{\mathrm{e}^{\frac{E}{k_\mathrm{B}T}} + 1} \tag{2.5}$$

similar to electrons in a normal material.

The conductivity of superconductors illuminated by an RF signal is a complex quantity, which may be written as

$$\sigma = \sigma_1 - i\sigma_2 \ , \tag{2.6}$$

where σ_1 and σ_2 depend on the angular frequency ω of the signal. The Mattis-Bardeen formulation for conductivity follows from the BCS theory [69]. In this formulation, the conductivity is expressed in terms of normal state conductivity σ_n, where the real

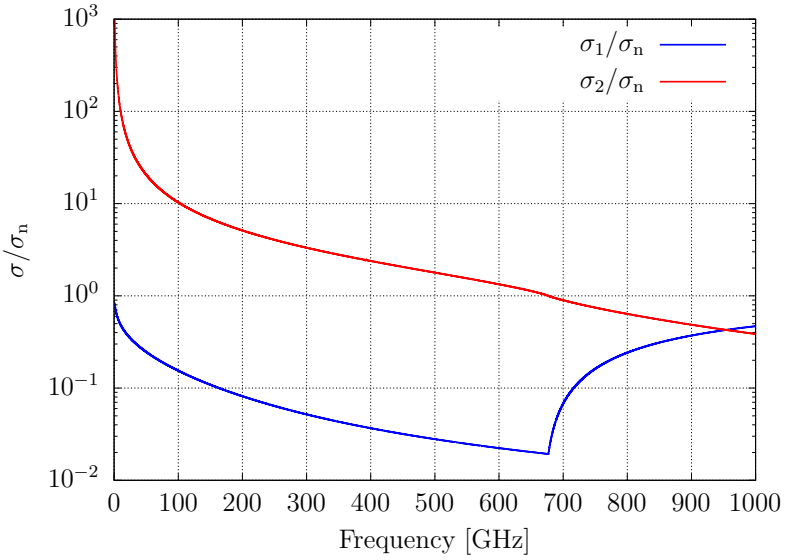


Figure 2.3: The complex conductivity of niobium with $\frac{\Delta}{e} = 2.8\,\mathrm{mV}$ at $T = 4.2\,\mathrm{K}$.

part is

$$\begin{aligned}\frac{\sigma_1}{\sigma_n} =& \frac{2}{\hbar\omega}\int_{\Delta}^{\infty}(f(E)-f(E+\hbar\omega))\,\frac{E^2+\Delta^2+\hbar\omega E}{\sqrt{E^2-\Delta^2}\sqrt{(E+\hbar\omega)^2-\Delta^2}}\mathrm{d}E \\ &+\frac{1}{\hbar\omega}\int_{\Delta-\hbar\omega}^{-\Delta}(1-2f(E+\hbar\omega))\,\frac{E^2+\Delta^2+\hbar\omega E}{\sqrt{E^2-\Delta^2}\sqrt{(E+\hbar\omega)^2-\Delta^2}}\mathrm{d}E\ ,\end{aligned} \tag{2.7}$$

and the imaginary part is given by

$$\frac{\sigma_2}{\sigma_n} = \frac{1}{\hbar\omega}\int_{\Delta-\hbar\omega\ ,\ -\Delta}^{\Delta}(1-2f(E+\hbar\omega))\,\frac{E^2+\Delta^2+\hbar\omega E}{\sqrt{\Delta^2-E^2}\sqrt{(E+\hbar\omega)^2-\Delta^2}}\mathrm{d}E\ . \tag{2.8}$$

In the latter equation, the lower integration boundary is $\Delta - \hbar\omega$ in case $2\Delta \geq \hbar\omega$, and $-\Delta$ otherwise. This change in the integration boundaries accounts for the fact that high-frequency photons have sufficient energy to break a Cooper pair. Figure 2.3 clearly shows the change of σ for Nb at 677 GHz: At higher frequencies, σ_1 and σ_2 are similar, while at lower frequencies, σ_2 is at least one order of magnitude larger than σ_1. All receivers developed in this thesis are operated below 300 GHz, unaffected by the transition at 677 GHz.

2.2 Quasiparticle Tunnelling in the Semiconductor Picture

An SIS junction is a sandwich of two superconductors separated by a 10 nm insulator of $\approx 1\mu m^2$ area. The mixer operation is based on the tunnelling of quasiparticles between two superconductors. The insulator layer of the SIS junction is thin enough to allow for a large probability that a quasiparticle on either side of the insulator layer is allowed to tunnel to the other side [70–72]. Cooper pair tunnelling is the mechanism in Josephson junctions, a generally undesired process for mixer operation and suppressed with an external magnetic field applied across the SIS junction [8, 73–75]. Quasiparticles are the tunnelling charges in SIS junctions. The tunnelling process needs to conserve energy and satisfy the Pauli exclusion principle in both superconductors of the SIS junction.

Figure 2.4 shows the semiconductor picture of an SIS junction where the energy potential of the two superconductors and, therefore, their Fermi levels are displaced by eV_0, where e is the electron charge and V_0 is the DC voltage between the two superconductors. The filled states of one superconductor are at the same energy level as the empty states of the other due to the shown displacement of $eV_0 > 2\Delta$. Tunnelling is possible when the filled states of one superconductor are on the same energy level as empty states in the other superconductor. Consequently, a net current of quasiparticles will flow from the filled to the empty states. We emphasise that it is a net current because tunnelling occurs in both directions.

The density of normal states in Figure 2.4 at $eV_0 > 2\Delta$ is similar to the superconducting states, as can be seen by referencing to the green hashed area in Figure 2.2. Therefore, the DC response of SIS junctions is similar to that of a normal resistor R_N at $eV_0 > 2\Delta$. For $eV_0 < 2\Delta$ shown in the semiconductor picture in Figure 2.5, the filled states in one superconductor encounter the energy band gap region in the opposing superconductor, hence, no tunnelling can occur through the superconductor. Only a $eV_0 = 2\Delta$ potential displacement of the superconductors causes a strong tunnelling current due to the large density of superconducting states at $E = \Delta$, shown in Figure 2.2. The displacement energy equivalent bias voltage at the gap is

$$V_g = \frac{2\Delta}{e} , \tag{2.9}$$

which is an important characteristic of superconductors.

Figure 2.6 shows an idealised SIS junction response:

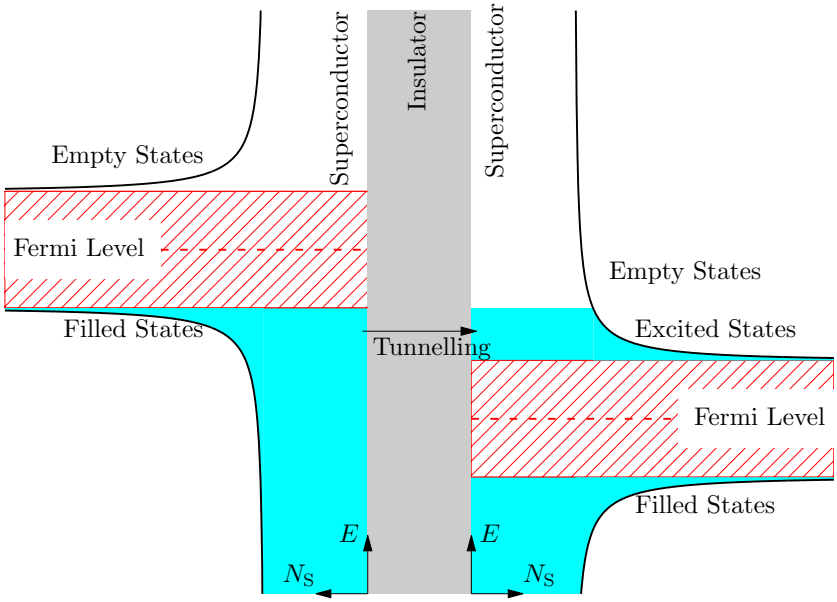


Figure 2.4: The semiconductor picture of tunnelling between superconductors with the potential energy of the two electrodes displaced by more than the superconducting gap energy $eV_0 > 2\Delta$. The superconducting gap energy 2Δ is hashed in red and centred at the Fermi Level $\xi = 0\,\mathrm{eV}$.

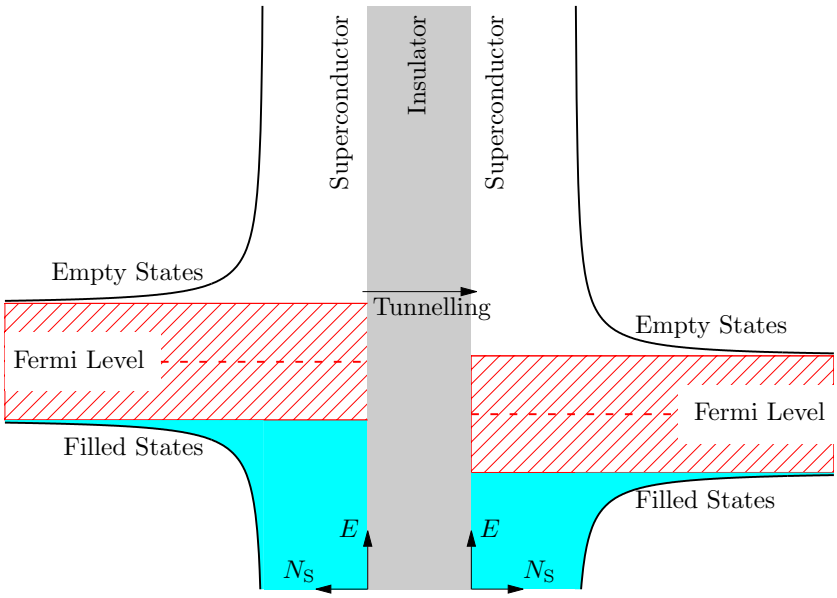


Figure 2.5: The semiconductor picture of tunnelling between superconductors with the potential energy of two electrodes displaced by less than the superconducting gap energy $eV_0 < 2\Delta$. The superconducting gap energy 2Δ is hashed in red and centred at the Fermi Level $\xi = 0\,\mathrm{eV}$. The indicated tunnelling is due to thermally excited quasiparticles above the superconducting gap energy.

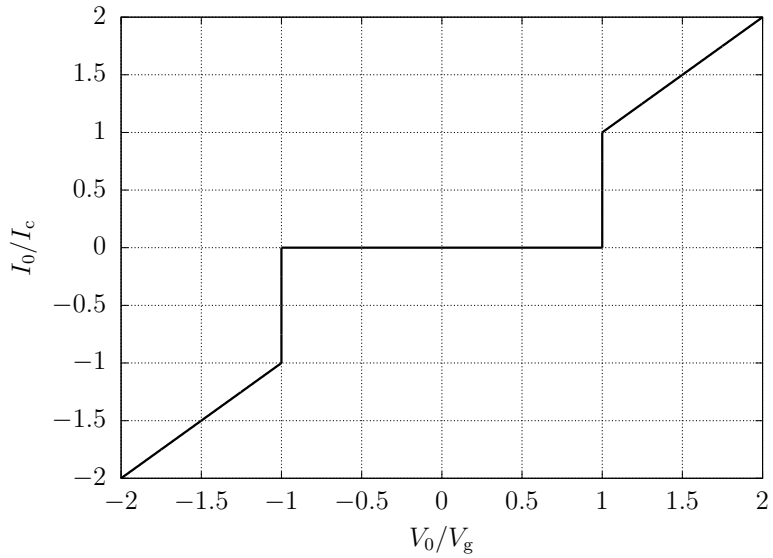


Figure 2.6: An idealised IV curve: No current for $|V_0| < V_g$, a normal resistance region for $|V_0| > V_g$, and an infinitely sharp current onset at $|V_0| = V_g$.

1. At $|V_0| < V_g$, no DC current flows because no energy states are available in the energy gap;
2. At $|V_0| = V_g$ is a sharp DC current onset due to an excess of available quasiparticle energy states;
3. At $|V_0| > V_g$ is a linear DC current behaviour because the density of states approaches that of a normal metal;

The sign of V_0 depends on the definition and on which superconductor is on the higher energy. Generally, the currents for negative V_0 are the same but in the opposite direction to the ones for positive V_0, as can be seen from the semiconductor pictures.

The ideal behaviour description in Figure 2.6 is valid for $T = 0\,\mathrm{K}$. Thermal excitations of quasiparticles caused at $T > 0\,\mathrm{K}$ modify this ideal DC distribution and cause a non-zero leakage current below V_g. The expression for the semiconductor picture, depending on the Fermi-Dirac distribution $f(E)$, for the DC through an SIS junction is

$$I\left(V_0\right) = \frac{1}{eR_N}\int_{-\infty}^{\infty} N_S(E)N_S(E+eV_0)\left(f\left(E+eV_0\right) - f\left(E\right)\right)\mathrm{d}E\ , \tag{2.10}$$

following [72], where R_N is the normal resistance observed at $|V_0| > V_g$.

Subgap tunnelling currents below V_g originate from thermally excited quasiparticle states, which fill the empty states above the energy gap in the semiconductor picture in Figure 2.5. These thermally excited quasiparticles encounter empty states

above the energy band gap of the opposing superconductor. The net tunnelling current originates from the fact that the states just above the energy band gap of the superconductor at the lower potential encounter the band gap of the opposing superconductor. As a result, there is a favourable direction of tunnelling. However, the tunnelling current at $|V_0| < V_g$ is small because the number of thermally excited quasiparticles is much smaller than those filled below the energy gap. Zero net tunnelling current occurs then only at $V_0 = 0\,\mathrm{mV}$ because if both superconductors are on the same energy potential, the thermally excited quasiparticles have no favourable direction of tunnelling; Hence, the currents cancel each other.

2.2.1 Photon-assisted quasiparticle tunnelling

The quasiparticles that encounter the energy gap of the opposing superconductor can tunnel if they overcome the potential barrier across the two superconductors, the energy missing to the quasiparticle states above the gap energy [76, 77]. Photons with an energy $\hbar\omega$ can provide the energy required to overcome this potential difference, as depicted in the semiconductor picture in Figure 2.7. Photo-assisted quasiparticle tunnelling occurs if the energy provided by photons $n\hbar\omega$ is larger than the energy difference between the filled and empty quasiparticle states $(V_g - V_0)\,e$. n photons, where n is an integer, can be absorbed at a time, but it is clear that it is more likely to absorb one photon than two photons at once. Thus, the quasiparticle tunnelling probability depends on the displacement of the Fermi levels of the two superconductors and the frequency of the signal. The condition for photon-assisted tunnelling is, therefore,

$$eV_0 \geq eV_g - n\hbar\omega \ . \tag{2.11}$$

The n dependency causes a step like DC response, the so-called photon steps. The width of these photon steps is related to the photon energy and the frequency of the signal

$$V_{\mathrm{Ph}} = \frac{\hbar\omega}{e} \ . \tag{2.12}$$

The number of photon steps observable depends on the number of incident photons or the strength of the 'pumping' signal illuminating the SIS junction. If more photons are incident, more quasiparticles will absorb the necessary energy to tunnel. The number of incident photons is measured as AC voltage V_{D}, known as the pumping level. The pumping level is characterised by the pumping parameter

$$\alpha_{\mathrm{D}} = \frac{V_{\mathrm{D}}}{V_{\mathrm{Ph}}} \ , \tag{2.13}$$

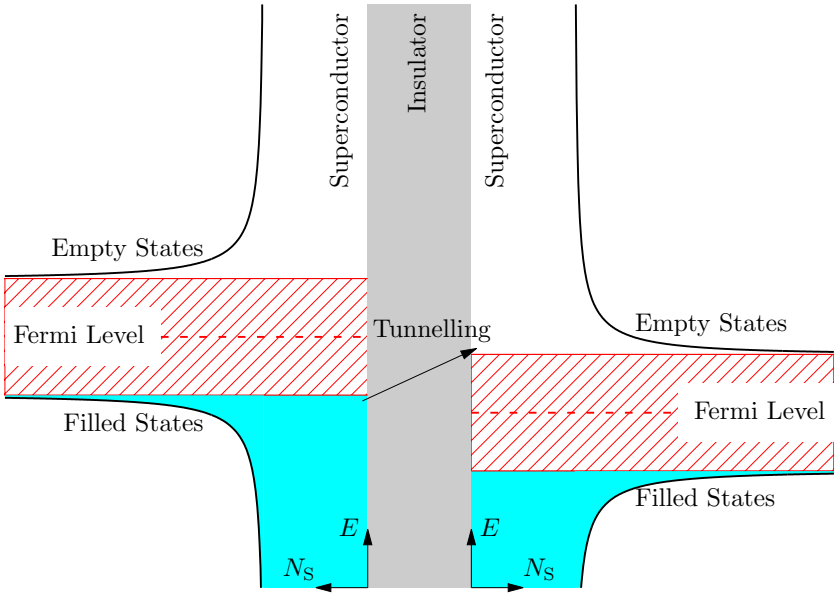


Figure 2.7: The semiconductor picture of photon-assisted tunnelling between superconductors with the potential energy of two electrodes displaced by less than the superconducting gap energy $eV_0 < 2\Delta$. The vertical component of the tunnelling arrow is the energy that should be provided by photons for photon-assisted tunnelling to occur. The superconducting gap energy 2Δ is hashed in red and centred at the Fermi Level $\xi = 0\,\mathrm{eV}$.

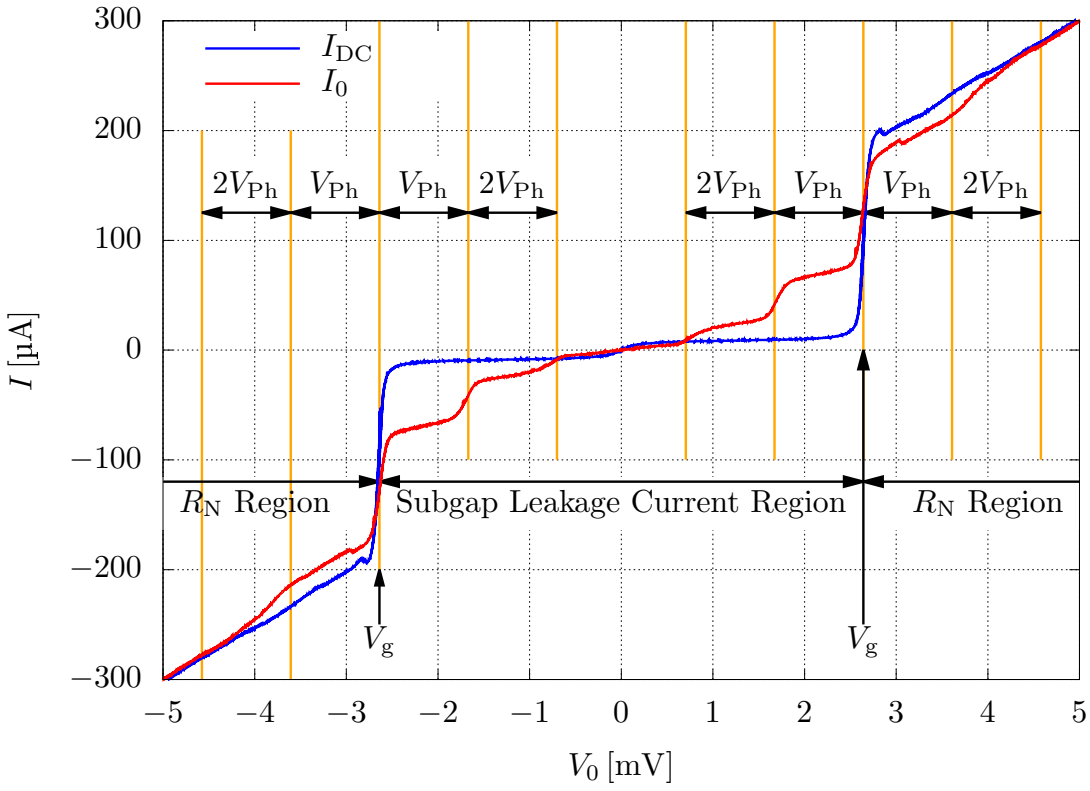


Figure 2.8: Measured $I_{DC}(V_0)$ and $I_0(V_0)$ pumped at 234 GHz.

which is a normalised quantity to measure the strength of the signal. As we shall show in the following section, the pumping level parameter α relates the unpumped and pumped IV curves, $I_{DC}(V_0)$ and $I_0(V_0)$ by

$$I_0(V_0, V_{LO}) = \sum_{n=-\infty}^{\infty} J_n^2(\alpha_D) I_{DC}(V_0 + nV_{Ph}) \ , \tag{2.14}$$

where J is the Bessel function of the first kind of n^{th} order.

Measured $I_{DC}(V_0)$ and $I_0(V_0)$ are shown in Figure 2.8. $I_{DC}(V_0)$ has a non-negligible but small leakage current in the subgap region $|V_0| < V_g$ and a linear R_N region for $|V_0| > V_g$. The current onset at $|V_0| = V_g$ is sharp. The transitions between the individual regions have several features outside the scope of this thesis of integrating a dual-polarisation receiver on-chip. We chose to display I_0 for a high α_D so that two photon steps are visible. The currents are symmetric to the 0 mV bias, as expected from the semiconductor picture explanation.

2.3 Quantum Mixer Theory

The quantum mixer theory was first reported by Tucker in [78] and a full account of this theory was reported by Tucker and Feldman in [79]. In this section, only a brief account of this theory will be given, aiming to outline the expressions for the tunnelling currents used in future chapters. The impedance recovery chapter builds on the equations of the large-signal analysis, and the predictions of receiver performances with the Supermix package use the small-signal analysis.

The time-dependent phase factor of the wave function is $\tau(t)$, and the Fourier transform of τ is defined by Tucker as [79]

$$W(\omega) = \int_{-\infty}^{\infty} \tau(t)\, \mathrm{e}^{-i\omega t} \mathrm{d}t \tag{2.15}$$

This Fourier transform can be substituted into the Werthamer expression to calculate the averaged quasiparticle tunnelling current, which is according to Tucker [79, 80]

$$\langle I(t) \rangle = \mathfrak{Im} \left\{ \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} W(\omega')\, W^*(\omega'')\, \mathrm{e}^{-i(\omega' - \omega'')t} I_{\mathrm{R}} \left(V_0 + \frac{\hbar \omega'}{e} \right) \mathrm{d}\omega' \mathrm{d}\omega'' \right\} \ , \tag{2.16}$$

where I_{R} is the complex response function that completely characterises the SIS junction.

In the DC case, without a time-dependent voltage applied, the response function is defined by Tucker as [79]

$$I_{\mathrm{R}}(V_0) = i I_{\mathrm{DC}}(V_0) + I_{\mathrm{KK}}(V_0) \ . \tag{2.17}$$

The imaginary part of the response function is the measurable unpumped current I_{DC} through the SIS junction. The real part of the response function is the reactive part of the tunnelling current as the Kramers-Kronig transformation of I_{DC}

$$I_{\mathrm{KK}}(V_0) = \frac{P}{\pi} \int_{-\infty}^{\infty} \frac{I_{\mathrm{DC}}(V) - \frac{V}{R_{\mathrm{N}}}}{V - V_0} \mathrm{d}V \ , \tag{2.18}$$

following Tuckers description, where R_{N} is the normal resistance of the SIS response, and P is the Cauchy principal value [79, 81, 82]. I_{KK} expresses the sharpness of the current onset at V_{g} of I_{DC}, as shown in Figure 2.9. The reactive term introduced by I_{KK} is necessary to account for non-classical reactances, for instance, those other than the geometric capacitance, and a physically consistent description of the tunnelling process [79, 83].

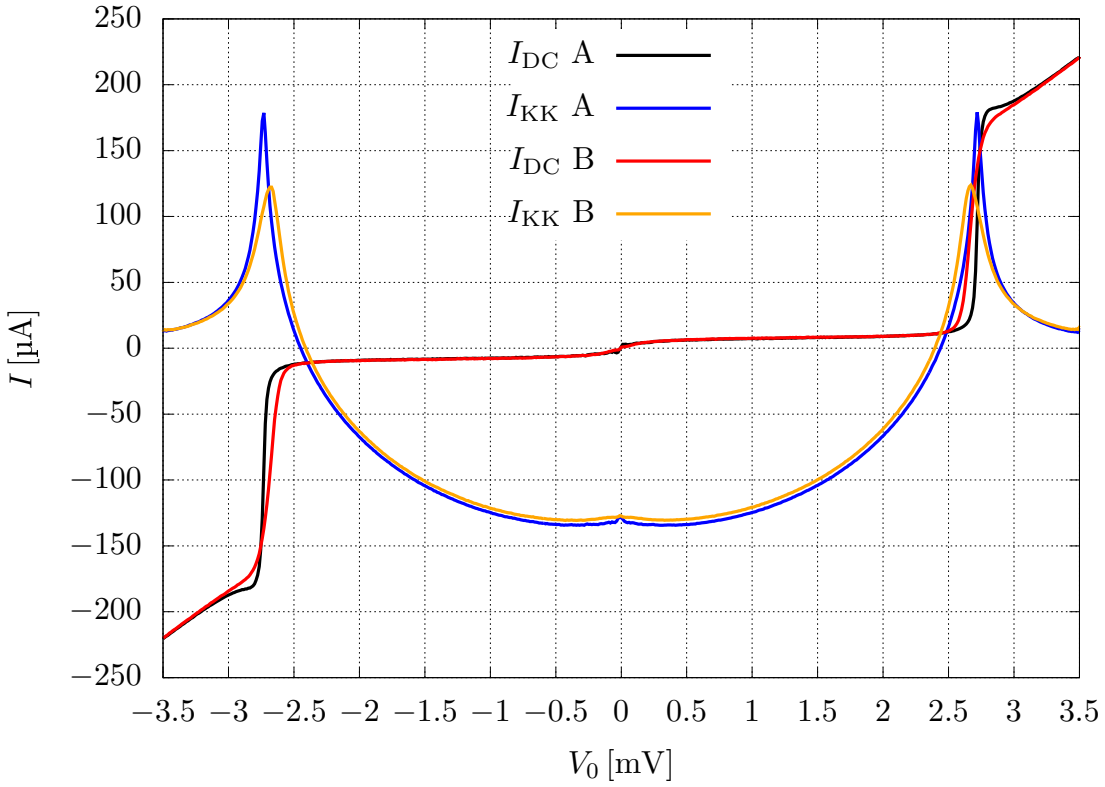


Figure 2.9: I_{DC} and I_{KK} for different magnetic biases. The larger magnetic bias in case B smears out I_{DC} at V_{g} compared to case A. I_{KK} measures the sharpness of I_{DC}.

2.3.1 Large-Signal Analysis

Applying a time-dependent voltage across the SIS device as described in Tucker [79] of the form

$$V(t) = V_0 + V_\mathrm{D}\cos(\omega t) \tag{2.19}$$

modifies the energy of the time-dependent phase factor τ. The phase factor τ is now

$$\begin{aligned}\tau = \mathrm{e}^{-i\frac{Et}{\hbar}} =& \mathrm{e}^{-i\frac{eV_0 t}{\hbar}}\mathrm{e}^{-i\frac{e\int V_\mathrm{D}\cos(\omega t)\mathrm{d}t}{\hbar}} \\ =& \mathrm{e}^{-i\frac{eV_0 t}{\hbar}}\mathrm{e}^{-i\frac{eV_\mathrm{D}\sin(\omega t)}{\hbar\omega}} \\ =& \mathrm{e}^{-i\frac{eV_0 t}{\hbar}}\sum_{n=-\infty}^{\infty} J_n\left(\frac{eV_\mathrm{D}}{\hbar\omega}\right)\mathrm{e}^{-in\omega t}\end{aligned} \tag{2.20}$$

using the Jacobi-Anger expansion, detailing here Tuckers derivation [79]. Following further Tucker [79], the Fourier transform in Equation 2.15 of τ is

$$W(\omega') = \sum_{n=-\infty}^{\infty} J_n\left(\frac{eV_\mathrm{D}}{\hbar\omega}\right)\delta(\omega' - n\omega) \ , \tag{2.21}$$

where δ is the Kronecker Delta function.

Substitution of Equation 2.21 into Equation 2.16 yields

$$I_\mathrm{D}(t) = \mathfrak{Im}\left\{\sum_{n=-\infty}^{\infty}\sum_{m=-\infty}^{\infty} J_n\left(\frac{eV_\mathrm{D}}{\hbar\omega}\right)J_{n+m}\left(\frac{eV_\mathrm{D}}{\hbar\omega}\right)\mathrm{e}^{im\omega t}I_\mathrm{R}\left(V_0 + n\frac{\hbar\omega}{e}\right)\right\} \ , \tag{2.22}$$

which Tucker expressed as Fourier series [79]

$$I_\mathrm{D}(t) = a_0 + \sum_{m=1}^{\infty} a_m\cos(m\omega t) + b_m\sin(m\omega t) \ . \tag{2.23}$$

The coefficients of the Fourier series are according to Tucker [79]

$$a_m = \sum_{n=-\infty}^{\infty} J_n(\alpha_\mathrm{D})\left(J_{n+m}(\alpha_\mathrm{D}) + J_{n-m}(\alpha_\mathrm{D})\right)I_\mathrm{DC}(V_0 + nV_\mathrm{Ph}) \tag{2.24}$$

and

$$b_m = \sum_{n=-\infty}^{\infty} J_n(\alpha_\mathrm{D})\left(J_{n+m}(\alpha_\mathrm{D}) - J_{n-m}(\alpha_\mathrm{D})\right)I_\mathrm{KK}(V_0 + nV_\mathrm{Ph}) \ . \tag{2.25}$$

In practice, second- and higher-order harmonics are assumed to be shorted by the capacitance of the SIS junction. As Tucker shows, $m = 1$ returns the AC tunnelling current

$$\begin{aligned}I_\mathrm{D}(V_0, \alpha_\mathrm{D}) = \sum_{n=-\infty}^{\infty} & J_n(\alpha_\mathrm{D})\left[J_{n-1}(\alpha_\mathrm{D}) + J_{n+1}(\alpha_\mathrm{D})\right] \\ & \left[I_\mathrm{DC}(V_0 - nV_\mathrm{Ph}) + iI_\mathrm{KK}(V_0 - nV_\mathrm{Ph})\right] \ ,\end{aligned} \tag{2.26}$$

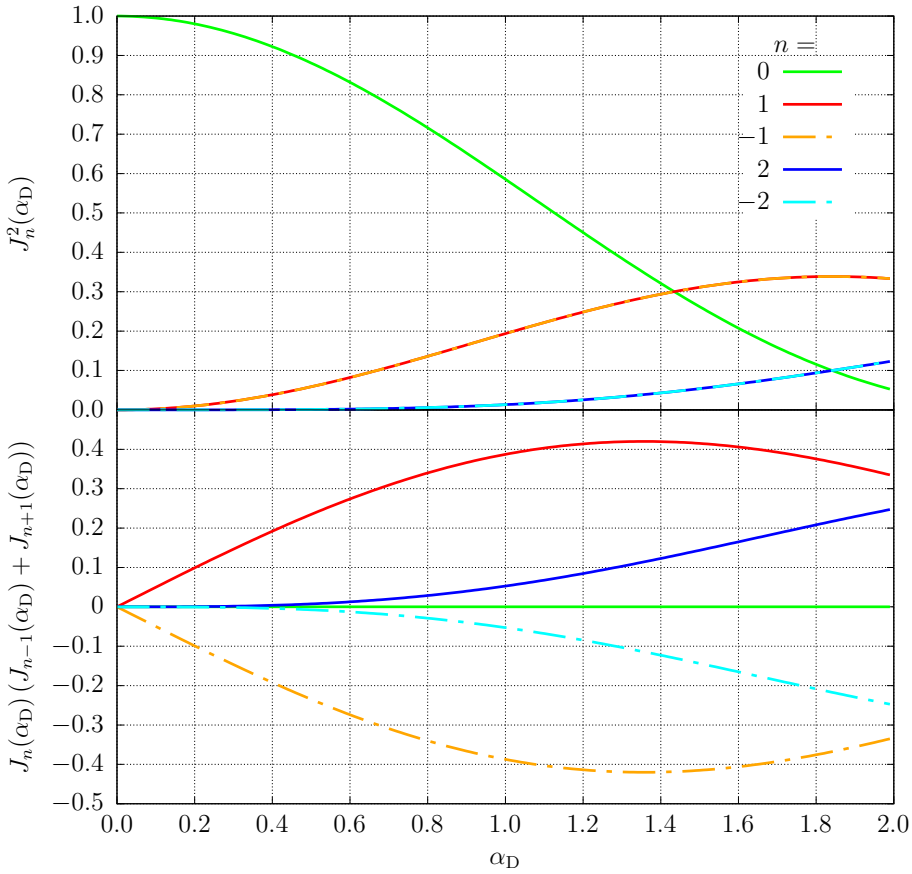


Figure 2.10: The Bessel function expressions used in Equations 2.26 and 2.27 at different orders n.

and $m = 0$ returns the DC tunnelling current

$$I_0(V_0, \alpha_D) = \sum_{n=-\infty}^{\infty} J_n^2(\alpha_D) I_{DC}\left(V_0 - nV_{Ph}\right) \ . \tag{2.27}$$

The right-hand side of Equation 2.27 may be interpreted as the summation of the probability of tunnelling $J_n^2(\alpha_D)$ multiplied with DC tunnelling current at a bias voltage $V_0 - nV_{Ph}$. The tunnelling probability is significantly stronger for $n = -1$, 0, 1 at reasonable pumping levels ($\alpha_D \approx 1$), as shown in Figure 2.10. As each quasiparticle at a given bias voltage V_0 of the unpumped IV curve has a displacement energy equivalent to $V_0 - nV_{Ph}$, a high-frequency signal causes the largest photon step currents next to the gap voltage V_g in the range from $V_g - V_{Ph}$ to $V_g + V_{Ph}$, e.g. for $n = -1$ and 1. This forms the first photon step.

2.3.2 Small-Signal Analysis

In addition to the non-linear response of the SIS tunnel device on a large signal V_{D}, it has a linear response on a small signal $v(t)$, which is responsible for the mixing processes. The small signal $v(t)$ modifies the definition of $V(t)$ in Equation 2.19, causing an additional term $i(t)$ in $\langle I(t) \rangle$ in Equation 2.16. The strong LO pumping of the tunnel junction generates the harmonic frequencies

$$\omega_m = |m\omega + \omega_{\mathrm{IF}}| \text{ with } m = 0, \pm 1, \pm 2, \ldots , \tag{2.28}$$

where ω is the LO angular frequency, and ω_{IF} is the IF angular frequency. As we argued above, the capacitance of the SIS junction shorts higher harmonics, thus, we only consider $m = -1, 0, 1$. In particular, $m = 1$ is the USB, $m = -1$ is the LSB, and $m = 0$ is the low-frequency IF signal. An incoming signal at $\omega_1 = |\omega + \omega_{\mathrm{IF}}|$ or $\omega_{-1} = |-\omega + \omega_{\mathrm{IF}}|$ is converted into the ω_{IF} signal.

Figure 2.11 shows a Norton equivalent circuit representation of the SIS mixer device for the small-signal analysis in the limits of $m = -1, 0, 1$. The large signal on the left facilitates the mixing process and sets the operating point but has no further implications for the small signals. The LSB and USB are shown with a current source I_m and corresponding internal source admittance Y_m, representing the RF signals to be downconverted and ideally matched to the IF load Y_0.

Tucker's derivation follows the same sequence as the large-signal analysis above, however, with the addition of the small-signal terms [79]

$$v(t) = \mathfrak{Re}\left\{ \sum_m v_m \mathrm{e}^{-i\omega_m t} \right\} . \tag{2.29}$$

The individual small-signal currents i_m and voltages v_m applied to the SIS mixer device are linked via a linear admittance matrix

$$i_m = \sum_{m'} Y_{mm'} v_{m'} , \tag{2.30}$$

where only I_{DC}, I_{KK} and α_{D} are required to obtain the elements of $Y_{mm'} = G_{mm'} + iB_{mm'}$ [79]. The individual terms are

$$G_{mm'} = \frac{e}{2\hbar\omega_{m'}} \sum_{n=-\infty}^{\infty} \sum_{n'=-\infty}^{\infty} \left\{ \begin{bmatrix} J_n(\alpha) J_{n'}(\alpha) \delta(m - m') \delta(n' - n) \\ I_{\mathrm{DC}}\left(V_0 + n'\frac{\hbar\omega}{e} + \frac{\hbar\omega_{\mathrm{m}'}}{e}\right) - I_{\mathrm{DC}}\left(V_0 + n'\frac{\hbar\omega}{e}\right) \\ + I_{\mathrm{DC}}\left(V_0 + n\frac{\hbar\omega}{e}\right) - I_{\mathrm{DC}}\left(V_0 + n\frac{\hbar\omega}{e} - + \frac{\hbar\omega_{\mathrm{m}'}}{e}\right) \end{bmatrix} \right\} \tag{2.31}$$

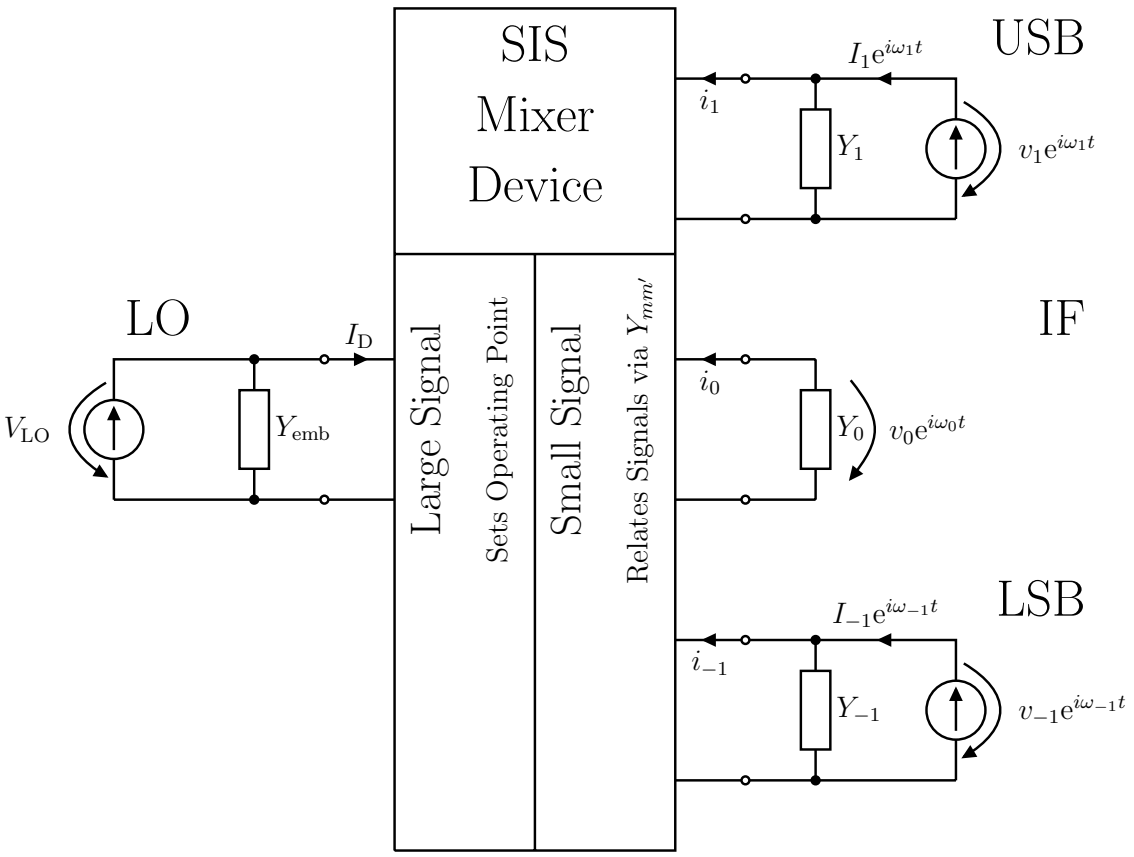


Figure 2.11: The Norton equivalent circuit small-signal representation of the SIS device assuming second- and higher-order harmonics shorted. The LO on the left sets the operating point at which the harmonics of the small signals on the right relate linearly.

and

$$B_{mm'} = \frac{e}{2\hbar\omega_{m'}} \sum_{n=-\infty}^{\infty} \sum_{n'=-\infty}^{\infty} \left\{ \begin{array}{c} J_n(\alpha) J_{n'}(\alpha) \delta(m-m') \delta(n'-n) \\ \left[\begin{array}{c} I_{\mathrm{KK}}\left(V_0 + n'\frac{\hbar\omega}{e} + \frac{\hbar\omega_{\mathrm{m}'}}{e}\right) - I_{\mathrm{KK}}\left(V_0 + n'\frac{\hbar\omega}{e}\right) \\ + I_{\mathrm{KK}}\left(V_0 + n\frac{\hbar\omega}{e}\right) - I_{\mathrm{KK}}\left(V_0 + n\frac{\hbar\omega}{e} - + \frac{\hbar\omega_{\mathrm{m}'}}{e}\right) \end{array} \right] \end{array} \right\} . \tag{2.32}$$

Again, I_{DC} and I_{KK} are SIS junction intrinsic characteristics, and α_{D} is the operation point set by the LO signal. We abstain from more detail on this derivation as this thesis focuses on integrating a dual-polarisation receiver on-chip.

The link between the small-signal voltages and currents can be used to determine the conversion gain. Now, circuit Equation 2.30 considers the current sources and source admittances Y_m at ω_m in Figure 2.11 in addition to the $Y_{mm'}$ terms [79]

$$\begin{pmatrix} I_1 \\ 0 \\ I_{-1} \end{pmatrix} = \begin{pmatrix} Y_{1\,1} + Y_1 & Y_{1\,0} & Y_{1\,-1} \\ Y_{0\,1} & Y_{0\,0} + Y_0 & Y_{0\,-1} \\ Y_{-1\,1} & Y_{-1\,0} & Y_{-1\,-1} + Y_{-1} \end{pmatrix} \begin{pmatrix} v_1 \\ v_0 \\ v_{-1} \end{pmatrix} . \tag{2.33}$$

For the DSB conversion gain, the sum of the available power at the LSB and USB

$$P_{\mathrm{in}} = \frac{|I_{-1}|^2}{8G_{-1}} + \frac{|I_1|^2}{8G_1} \tag{2.34}$$

is compared with the power at the IF load

$$P_{\mathrm{out}} = \frac{G_0 |v_0|^2}{2} . \tag{2.35}$$

Tucker takes the reciprocal of the admittance matrix to obtain the impedance matrix $Z_{mm'} = Y_{mm'}^{-1}$ to find [79]

$$v_0 = Z_{0,1} I_1 + Z_{0,-1} I_{-1} . \tag{2.36}$$

We substitute this result into P_{out} to get an expression for the conversion efficiency

$$\frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = 4G_0 \frac{|Z_{0,1} I_1 + Z_{0,-1} I_{-1}|^2}{\frac{|I_{-1}|^2}{G_{-1}} + \frac{|I_1|^2}{G_1}} . \tag{2.37}$$

Under the assumption that the two sidebands have an identical source circuit $I_1 = I_{-1}$ and $G_1 = G_{-1}$, which is reasonable for closely located RF frequencies, the equation reduces to

$$\frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = 2G_0 G_1 |Z_{0,1} + Z_{0,-1}|^2 . \tag{2.38}$$

Furthermore, $Z_{0,1} = Z_{0,-1}$ is reasonable for closely located RF frequencies yielding the DSB gain expression

$$\frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = 8G_0 G_1 |Z_{0,1}|^2 . \tag{2.39}$$

2.4 Summary

In this chapter, we introduced some aspects of the SIS mixer theory. We started by discussing aspects of superconductivity relevant to this thesis. In the next step, we discussed quasiparticle tunnelling through an insulator barrier sandwiched by two superconductors using the semiconductor picture. We presented the key equations describing quasiparticle tunnelling currents in the quantum mixer theory section, in which we first introduced the Werthammer expression and the DC case, then the large-signal analysis, and finally the small-signal analysis.

We will use the large signal together with the impedance recovery in Chapter 4 and the small-signal analysis during performance predictions within Supermix in Chapter 5, which is described in more detail in Appendix A.

Chapter 3

Reflection Coefficient Analysis of Twin Junction Tuning

Chapter published slightly shortened: J. Wenninger, G. Yassin, and B. K. Tan, "Analytical expressions for the design of twin junction tuning in SIS mixers," *Engineering Research Express*, 2023.

Previous publications gave only tentative descriptions of the twin junction design, focusing mainly on the performance of the SIS mixer [84–86]. It is also evident that in recent years, SIS mixer designers use commercial electromagnetic software packages, such as Ansys HFSS described in Appendix A, to optimise the mixer design. In those packages, the SIS tunnel junction is modelled as a lumped element circuit of a capacitance connected in parallel to a resistance, while the rest of the mixer circuits are rigorously modelled as planar superconducting transmission lines [87]. While this method is effective and can lead to accurate modelling of the mixer performance, it has the disadvantage that it obscures the intuitive understanding of the design, which may, in fact, lead to missing out effective designs. For example, we will later show that a quarter-wavelength transmission line separating the two junctions is not the only solution for good matching and, indeed, may not be the best solution for particular values of the line characteristic impedance dictated by the limitation of fabrication. In fact, we will show that other length choices may provide more flexibility in choosing the impedance of the transmission line separating the two junctions or other output impedance values of the feeding RF circuit.

Another assumption that previous publications made is that the two junctions are identical [84, 88]. While this assumption is quite reasonable considering that

the two junctions are closely located on the mixer chip, it would be interesting to investigate the effect of possible differences in admittance due to fabrication tolerances of the two junctions on the tuning and, indeed, if there are any advantages of using a twin junction device with different junction admittances. Also, common mixer designs aim at having a real input impedance of the twin junction device by mutual cancellation of the reactance of two identical junctions [89, 90]. This, however, may not be sufficient for an optimum mixer design and, in fact, may not even be the best choice for designing an SIS mixer with large RF bandwidth that, in general, has complex input impedance. For example, mixers that use complex RF circuits, such as an integrated local oscillator feed by using the harmonic of an SIS device, have complex output impedance [91]. Therefore, an additional circuit may be needed to match it to the twin junction device. A real input impedance of the twin junction device, in this case, may not constitute a significant advantage.

3.1 Reflection Coefficient between the RF circuit and twin junction circuit

In Figure 3.1, we show the Norton equivalent circuit model of a typical SIS mixer chip using twin junction tuning, such as the mixer shown in Figure 3.2. As usual, the SIS tunnel junction is modelled as a lumped element, which has been shown by both experimental and simulation results to be an excellent approximation, assuming the dimensions of the device are small relative to the length of transmission lines [92]. The reflection coefficient between the twin junction circuit of admittance $Y_{\rm in}$ and the feeding RF circuit of admittance $Y_{\rm RF}$ is defined as [26]

$$\Gamma = \frac{Y_{\rm RF} - Y_{\rm in}}{Y_{\rm RF} + Y_{\rm in}} \ , \tag{3.1}$$

where

$$Y_{\rm in} = Y_1 + Y_0 \frac{Y_2 + iY_0 \tan(\beta l)}{Y_0 + iY_2 \tan(\beta l)} \ . \tag{3.2}$$

In these equations, Y_1 and Y_2 are the complex admittances of the junctions, and l, β, and Y_0 are, respectively, the length, propagation constant and characteristic admittance of the transmission line connecting the two junctions, assumed lossless. Substituting and separating the real and imaginary parts yields

$$\Gamma = \frac{Y_0 (Y_{\rm in} - Y_1 - Y_2) + i (Y_{\rm in}Y_2 - Y_1Y_2 - Y_0^2) \tan(\beta l)}{Y_0 (Y_{\rm in} + Y_1 + Y_2) + i (Y_{\rm in}Y_2 + Y_1Y_2 + Y_0^2) \tan(\beta l)} \ . \tag{3.3}$$

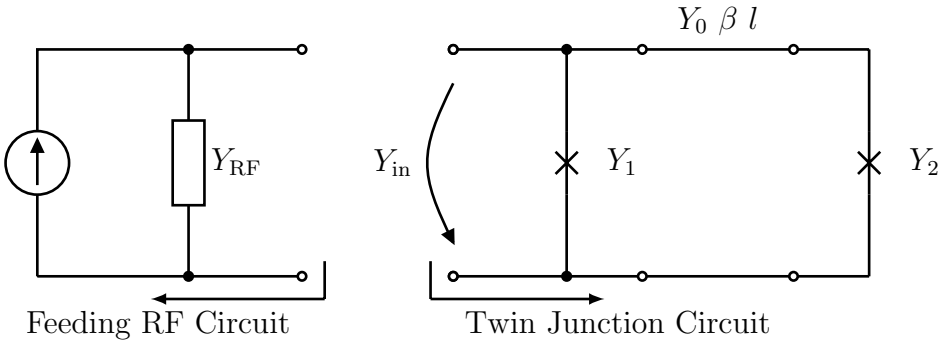


Figure 3.1: The Norton equivalent circuit model of a twin junction mixer with an RF circuit represented by admittance $Y_{\rm RF}$ and a twin junction circuit with input admittance $Y_{\rm in}$. The two SIS junctions in the twin junction device have admittances Y_1 and Y_2 and are connected by a lossless transmission line of characteristic admittance Y_0, propagation constant β and length l.

We request that $\Gamma = 0$, implying $Y_{\rm RF} = Y_{\rm in}$, to ensure maximum power coupling from the RF feeding circuit to the twin junction circuit. Therefore, the real and imaginary parts of the numerator in Equation 3.3 are both set to 0.

Expressing the admittances as $Y = G + iB$, where G is the conductance and B is the susceptance, then in the matched case $\Gamma = 0$, we obtain the solution

$$G_{\rm in} = \frac{Y_0^2\left(G_1+G_2\right) - 2Y_0G_1B_2T + \left(G_1\left(G_2^2+B_2^2\right)+Y_0^2G_2\right)T^2}{Y_0^2 - 2Y_0B_2T + \left(G_2^2+B_2^2\right)T^2} \tag{3.4}$$

and

$$B_{\rm in} = \frac{Y_0^2\left(B_1+B_2\right) + Y_0\left(Y_0^2 - G_2^2 - B_2^2 - 2B_1B_2\right)T + \left(B_1\left(G_2^2+B_2^2\right) - Y_0^2B_2\right)T^2}{Y_0^2 - 2Y_0B_2T + \left(G_2^2+B_2^2\right)T^2}\ , \tag{3.5}$$

where we defined $T = \tan\left(\beta l\right)$.

The above expressions give the admittance that the designer may use for adjusting the output admittance of the feeding RF circuit in order to maximise the coupling to the twin junction device. In what follows, we shall consider the special case of two identical junctions with $Y_1 = Y_2 = Y$. In this case, the reflection coefficient in Equation 3.3 simplifies to

$$\Gamma = \frac{Y_0\left(Y_{\rm in} - 2Y\right) + i\left(Y_{\rm in}Y - Y^2 - Y_0^2\right)\tan\left(\beta l\right)}{Y_0\left(Y_{\rm in} + 2Y\right) + i\left(Y_{\rm in}Y + Y^2 + Y_0^2\right)\tan\left(\beta l\right)}\ . \tag{3.6}$$

and the admittance for the matched case $\Gamma = 0$ can be expressed as

$$G_{\rm in} = G\left(1 + \frac{Y_0^2\left(1+T^2\right)}{Y_0^2 - 2Y_0BT + \left(G^2+B^2\right)T^2}\right) \tag{3.7}$$

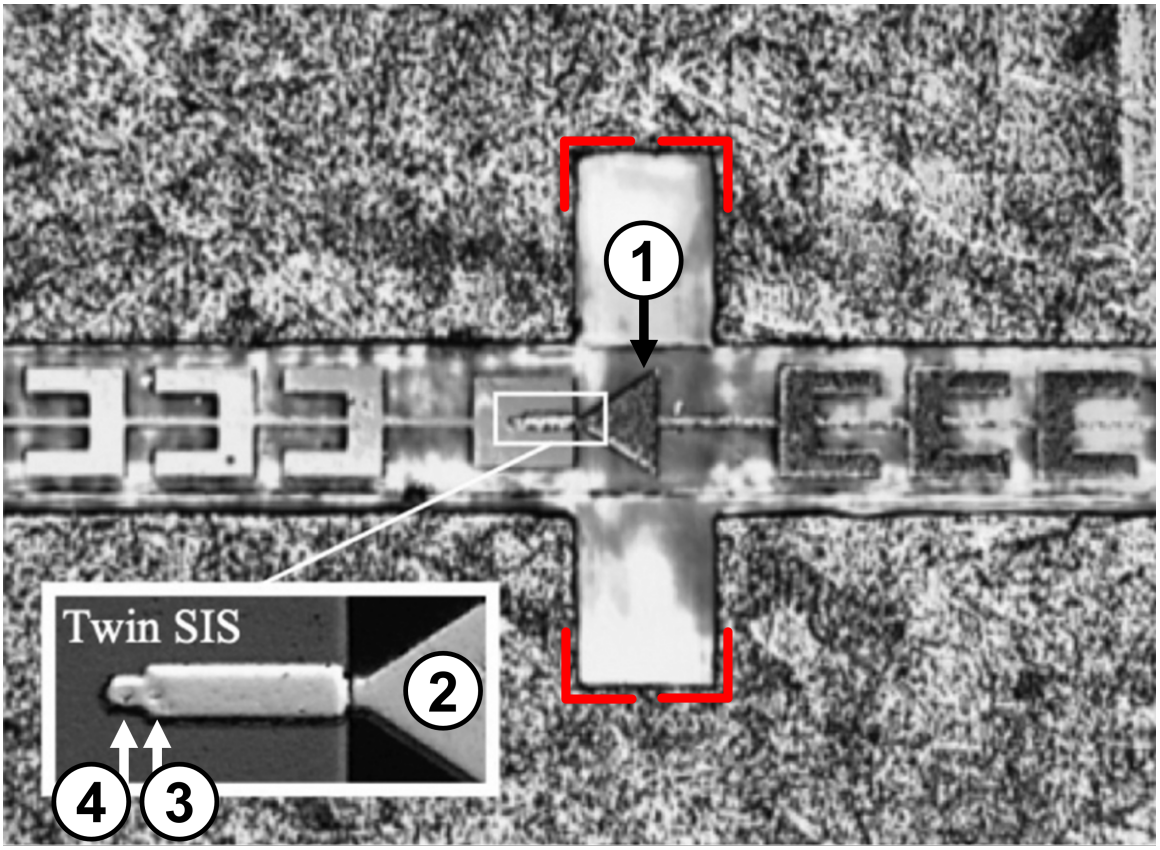


Figure 3.2: A fabricated 790 GHz to 950 GHz twin junction SIS mixer in a 300 µm by 75 µm rectangular waveguide highlighted with red. The signal is coupled to the mixer chip with the triangular antenna (1). The triangular antenna, shown in the inset as (2), couples the signal to the twin junction, where (3) and (4) indicate the first and second SIS junction under the microstrip. The junctions appear as craters or doughnut shapes. Modified image, original version published by A. Khudchenko, A. M. Baryshev, K. I. Rudakov, P. M. Dmitriev, R. Hesper, L. De Jong, and V. P. Koshelets, "High-Gap Nb-AlN-NbN SIS Junctions for Frequency Band 790-950 GHz," *IEEE Transactions on Terahertz Science and Technology*, 2016.

and

$$B_{\text{in}} = B + Y_0 \frac{Y_0 B\left(1 - T^2\right) + \left(Y_0^2 - G^2 - B^2\right) T}{Y_0^2 - 2Y_0 BT + \left(G^2 + B^2\right) T^2} \ . \tag{3.8}$$

We shall now discuss the following two options: Matching to 1) a real input impedance and 2) a complex impedance;

3.1.1 Matching to a real input impedance

Matching to a real input impedance is the commonly used case in which the reactance of the tunnel junctions is cancelled, and the input impedance of the twin junction device viewed from the RF side becomes real. This case may also be applied when the RF circuit has complex output impedance, but with an intermediate circuit between the RF circuit and the junction circuit, such that the impedance seen by the twin junction device is real. In either case, it is interesting to consider the following cases that yield simple analytical expressions that can easily be analysed:

1. The half-wavelength multiples case where $T = 0$:
   It corresponds to a transmission line satisfying $\beta l = n\pi$ where n is an integer. The tangent terms vanish in Equations 3.2 and 3.6, so that

   $$\Gamma\left(T = 0\right) = \frac{Y_{\text{in}} - 2Y}{Y_{\text{in}} + 2Y} \ . \tag{3.9}$$

   where the twin junction admittance is then given by

   $$Y_{\text{in}}\left(T = 0\right) = Y_1 + Y_2 = 2\left(G + iB\right) \ . \tag{3.10}$$

   This is simply a parallel circuit of shunt admittances which is not influenced by the characteristic admittance of the transmission line Y_0. The special case $\beta l = 0$ can be interpreted as doubling the junction area. However, it is clear from the equation above that the imaginary part of Y_{in} is $B_{\text{in}} \neq 0$, hence it is impossible to match the twin junction device to a real impedance of the RF feeding circuit.
2. The quarter-wavelength multiples case where $T = \infty$:
   The commonly used design choice corresponds to a transmission line length $\beta l = \left(1/2 + n\right)\pi$ in which the tangent terms dominate Equation 3.6

   $$\Gamma\left(T = \infty\right) = \frac{Y_{\text{in}} Y - Y^2 - Y_0^2}{Y_{\text{in}} Y + Y^2 + Y_0^2} \ . \tag{3.11}$$

   Applying the substitution $Y = G + iB$ and separation of real and imaginary parts yields

   $$\Gamma\left(T = \infty\right) = \frac{Y_{\text{in}} G - G^2 + B^2 - Y_0^2 + i\left(Y_{\text{in}} B - 2GB\right)}{Y_{\text{in}} G + G^2 - B^2 + Y_0^2 + i\left(Y_{\text{in}} B + 2GB\right)} \ . \tag{3.12}$$

In the matched case $\Gamma = 0$, the imaginary part is

$$(Y_{\text{in}} - 2G)\, B = 0 \ . \tag{3.13}$$

This results in $Y_{\text{in}} = 2G$, which is independent of the junction susceptance B. Substitution in the real part yields

$$G^2 + B^2 - Y_0^2 = 0 \ . \tag{3.14}$$

Therefore, the twin junction can be matched to a real RF circuit admittance ($B_{\text{in}} = 0$) by choosing

$$Y_0^2 = G^2 + B^2 \text{ with } G_{\text{in}} = 2G \ . \tag{3.15}$$

The same solution can be derive from setting the input susceptance Equation 3.8 to 0

$$B_{\text{in}}\,(T = \infty) = B\left(1 - \frac{Y_0^2}{G^2 + B^2}\right) = 0 \ , \tag{3.16}$$

and using the resulting Y_0 in Equation 3.7

$$G_{\text{in}}\,(T = \infty) = G\left(1 + \frac{Y_0^2}{G^2 + B^2}\right) \ . \tag{3.17}$$

3. The intermediate cases where $T = \pm 1$:
   The intermediate cases of transmission line lengths $\beta l = (1 + 2n)\,/4\pi$ flip only the sign of the imaginary component of Equation 3.6

$$\Gamma\,(T = \pm 1) = \frac{Y_0\,(Y_{\text{in}} - 2Y) \pm i\,(Y_{\text{in}}Y - Y^2 - Y_0^2)}{Y_0\,(Y_{\text{in}} + 2Y) \pm i\,(Y_{\text{in}}Y + Y^2 + Y_0^2)} \ . \tag{3.18}$$

   The positive sign $T = +1$ corresponds to a transmission line length satisfying $\beta l = (1/4 + n)\,\pi$. This gives

$$G_{\text{in}}\,(T = +1) = G\left(1 + \frac{2Y_0^2}{Y_0^2 - 2Y_0B + G^2 + B^2}\right) \tag{3.19}$$

   and

$$B_{\text{in}}\,(T = +1) = B + Y_0\frac{Y_0^2 - G^2 - B^2}{Y_0^2 - 2Y_0B + G^2 + B^2} \ . \tag{3.20}$$

   We set $B_{\text{in}} = 0$

$$0 = Y_0^3 + Y_0^2B - Y_0\left(3B^2 + G^2\right) + G^2B + B^3 \tag{3.21}$$

to find solutions with real input admittance. There are two physical solutions (positive values of Y_0), namely

$$Y_0 = B \text{ with } G_{\text{in}} = G\left(1 + 2\frac{B^2}{G^2}\right) \tag{3.22}$$

and

$$Y_0 = -B + \sqrt{2B^2 + G^2} \text{ with } G_{\text{in}} = 2G\ , \tag{3.23}$$

while the third solution has a negative characteristic admittance

$$Y_0 = -B - \sqrt{2B^2 + G^2} < 0. \tag{3.24}$$

Finally, the case $T = -1$ corresponding to $\beta l = (3/4 + n)\,\pi$. Only a sign flip in comparison to the $T = +1$ case is needed to give

$$G_{\text{in}}\,(T = -1) = G\left(1 + \frac{2Y_0^2}{Y_0^2 + 2Y_0B + G^2 + B^2}\right) \tag{3.25}$$

and

$$B_{\text{in}}\,(T = -1) = B + Y_0\frac{G^2 + B^2 - Y_0^2}{Y_0^2 + 2Y_0B + G^2 + B^2}\ . \tag{3.26}$$

We again set $B_{\text{in}} = 0$

$$0 = -Y_0^3 + Y_0^2B + Y_0G^2 + 3Y_0B^2 + G^2B + B^3 \tag{3.27}$$

to find solutions with real input admittance. There is only one physical solution for the cubic equation, namely

$$Y_0 = B + \sqrt{2B^2 + G^2} \text{ with } G_{\text{in}} = 2G\ . \tag{3.28}$$

The remaining two solutions have negative characteristic admittances

$$Y_0 = B - \sqrt{2B^2 + G^2} < 0 \tag{3.29}$$

and

$$Y_0 = -B < 0\ , \tag{3.30}$$

noting that the susceptance of our capacitive SIS junctions is positive $B > 0$.

The behaviour of the input impedance of a twin junction as a function of the characteristic impedance $Z_0 = 1/Y_0$ at 230 GHz is shown in Figure 3.3 for the special cases described above. We have chosen an SIS junction with junction capacitance of 75 fF and normal resistance of $R_{\text{N}} = 20\,\Omega$, which are typical values for a $1.0\,\mu\text{m}^2$ $\text{Nb/AlO}_\text{x}\text{/Nb}$ tunnel junction used in SIS mixers at mm/sub-mm wavelengths. Such

a junction will have an input impedance $Z_{\text{in}} = (R_{\text{in}}, X_{\text{in}}) = (0.18R_{\text{N}}, -0.38R_{\text{N}})$ when the junction is modelled as a lumped element.

A twin junction with the two SIS junctions separated by half a wavelength ($T = 0$) halves the required RF circuit admittance independent of Z_0, which is disadvantageous since the RF circuit impedance needs to have low resistance in a highly capacitive circuit. In fact, it can be seen from Figure 3.3 that when the length of the transmission line is half a wavelength, the input impedance of the twin junction cannot possibly be made real and hence cannot be matched to a real value. In contrast, a twin junction circuit with a transmission line separation satisfying the conditions given in cases 2 ($T = \infty$) or 3 ($T = \pm 1$) can be made to transform the large capacitance of the tunnel junctions into a pure resistance by carefully choosing βl and Z_0.

For a quarter-wavelength multiples transmission line $\beta l = (1/2+n)\pi$, R_{in} is almost three times that of a single SIS junction at $Z_0 \approx 8.4\,\Omega$, where the reactance crosses through $0\,\Omega$. At large values of Z_0, the input impedance approaches the impedance of the first junction, as can easily be seen from Equation 3.2.

As we have indicated previously, the quarter-wavelength multiples transmission line defined by $\beta l = (1/2+n)\pi$ (or $T = \infty$) is not always the best choice for matching the twin junction device. From Figure 3.3 we can see that the slope of the $T = \infty$ reactance curve at the characteristic impedance where $X_{\text{in}} = 0\,\Omega$ is much sharper than that for the curve corresponding to $T = 1$. This makes it much less tolerant to the choice of Z_0 and hence to tolerances in the device fabrication. Moreover, for $Z_0 > 10\,\Omega$, the reactance for the $T = \infty$ case becomes highly capacitive, while it remains close to zero for $T = 1$ for all impedance values in the range from $0\,\Omega$ to $22\,\Omega$. It is, however, evident from Figure 3.3 that the input resistance values for the $T = 1$ line are too low for $Z_0 < 15\,\Omega$. Hence, the final choice will depend on the preferred Z_0 value.

3.1.2 Matching to a complex impedance

This is the general case where we would match the complex impedance of the twin junction directly to the impedance of the RF circuit, which is, in general, complex. Given tunnel junction parameters and known admittance of the input RF feeding circuit G_{RF} and B_{RF}, Equation 3.1 and 3.2 can be solved for Y_0 and βl of the transmission line connecting the two tunnel junctions.

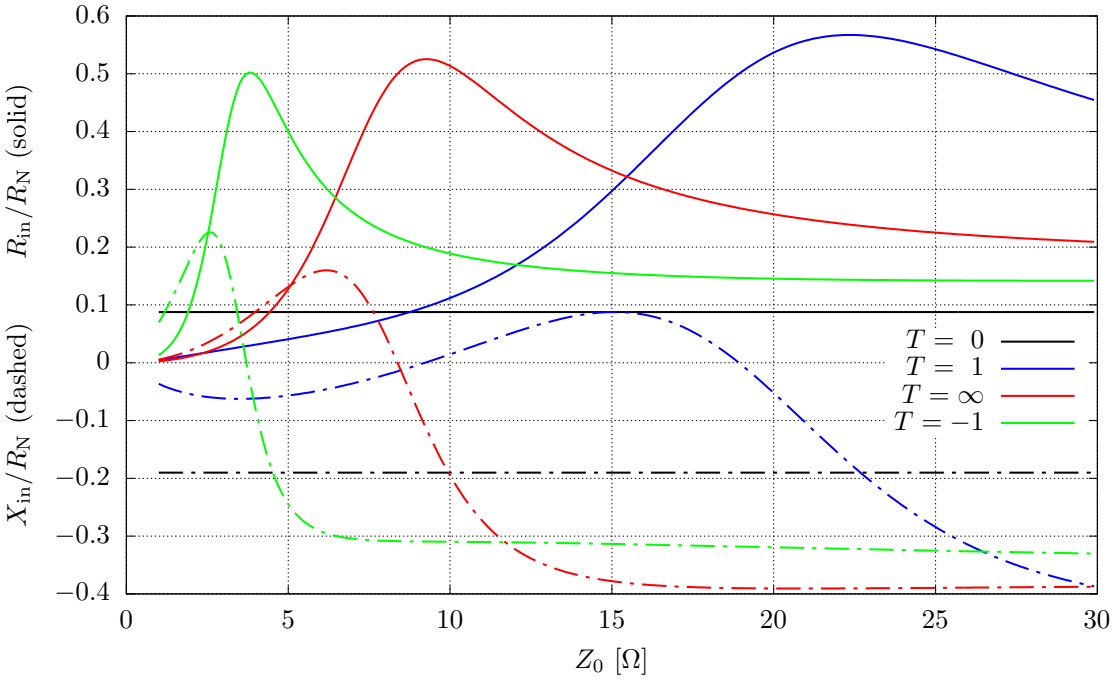


Figure 3.3: Computed curves showing the input impedance of the twin junction as a function of characteristic impedance Z_0 for the discussed lengths T of the transmission lines connecting the junctions, where R_{in} is the input resistance and X_{in} is the input reactance of the twin junction. The y-axis is normalised to the normal resistance of the SIS junction R_{N}, and R_{in} and X_{in} are shown as solid and dashed lines, respectively. The curves were computed from Equations 3.4 and 3.5 assuming identical junctions.

Setting $\Gamma = 0$ in Equation 3.3 yields

$$0 = Y_0 \left(B_{\text{in}} - B_1 - B_2\right) + \left(G_{\text{in}}G_2 - B_{\text{in}}B_2 - G_1G_2 + B_1B_2 - Y_0^2\right) \tan\left(\beta l\right) \tag{3.31}$$

for the imaginary part, and

$$0 = Y_0 \left(G_{\text{in}} - G_1 - G_2\right) + \left(-G_{\text{in}}B_2 - B_{\text{in}}G_2 + G_1B_2 + B_1G_2\right) \tan\left(\beta l\right) \tag{3.32}$$

for the real part. The real part relates Y_0 and βl linearly with

$$Y_0 = \frac{G_2 \left(B_{\text{in}} - B_1\right) + B_2 \left(G_{\text{in}} - G_1\right)}{G_{\text{in}} - G_1 - G_2} \tan\left(\beta l\right) \ , \tag{3.33}$$

which then can be used to obtain the design expressions. Substituting the Y_0 of Equation 3.33 in Equation 3.31 yields

$$\tan^2 \beta l = \frac{\left\{\left(G_{\text{RF}} - G_1\right)\left[G_2(G_{\text{RF}} - G_1 - G_2) - B_2^2\right] + G_2 \left(B_{\text{RF}} - B_1\right)^2\right\} \left(G_{\text{RF}} - G_1 - G_2\right)}{\left[G_2 \left(B_1 - B_{\text{RF}}\right) + B_2 \left(G_1 - G_{\text{RF}}\right)\right]^2} \ , \tag{3.34}$$

and substituting $\tan\left(\beta l\right)$ of Equation 3.33 in Equation 3.31 yields

$$Y_0^2 = \left(G_{\text{RF}} - G_1\right) G_2 + \frac{\left(G_1 - G_{\text{RF}}\right) B_2^2 + G_2 \left(B_{\text{RF}} - B_1\right)^2}{G_{\text{RF}} - G_1 - G_2} \ . \tag{3.35}$$

The expression above becomes singular for $G_{\text{RF}} = G_1 + G_2$, however, expressions for this case have already been derived and analysed in the previous section. The analytical solution above is given graphically as design curves in Figure 3.4. The curves are plotted for junction admittances used in the previous section and typical characteristic impedance values employed in SIS mixer circuits. These plots allow the designer to match the twin junction device to both real and complex impedances.

For example, assume that the output impedance of the RF circuit is given by $Z_{\text{RF}} = (11 - 4i)\,\Omega$. The designer will therefore notice from Figure 3.4 that the matched twin junction would be given by points on the blue curves corresponding to $\beta l = 3\pi/8$ and, therefore, to a transmission line of length $l = 3/16\lambda$ and characteristic impedance $Z_0 = 15\,\Omega$.

3.2 Influence of the IF circuit

In some twin-junction receivers, the IF circuit is connected at the second SIS junction, as shown in the Norton equivalent circuit in Figure 3.5. This IF circuit, of which the first element is typically an LPF, has an input admittance Y_{IF} associated. Y_{IF} has

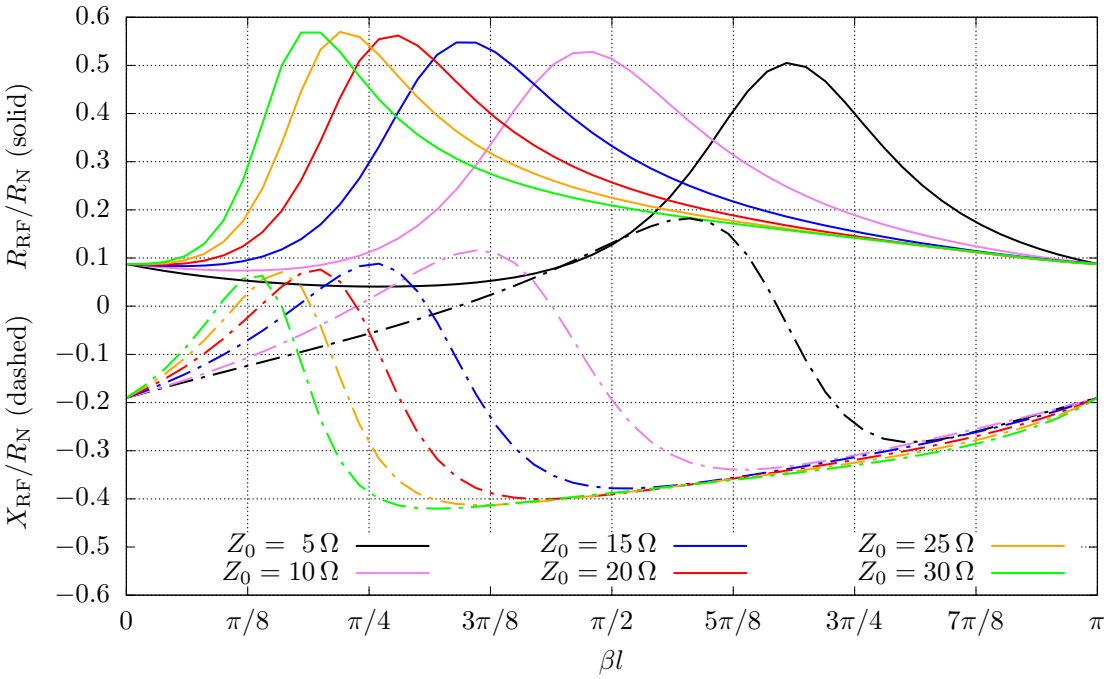


Figure 3.4: Design curves showing the matching impedance of the RF circuit as a function of the transmission line length for various values of characteristic impedances of the transmission line connecting the two junctions. The y-axis is normalised to the normal resistance of the SIS junction R_{N}, and R_{RF} and X_{RF} are shown as solid and dashed lines, respectively.

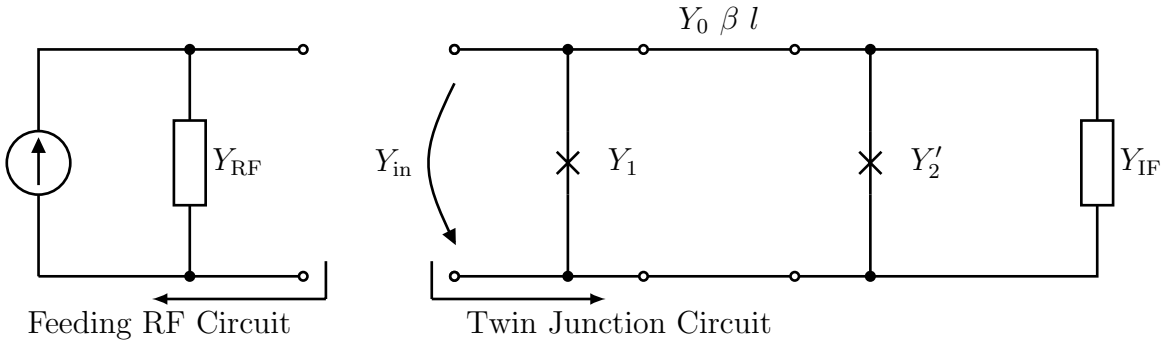


Figure 3.5: The Norton equivalent circuit model of a twin junction mixer with the admittance of the IF circuit $Y_{\rm IF}$ separated from the admittance of the second SIS junction Y_2'.

to be included in the admittance of the second SIS junction Y_2 with the equation set above. Alternatively, the IF circuit admittance can be treated separately by substituting

$$Y_2 = Y_2' + Y_{\rm IF} \ , \tag{3.36}$$

where Y_2' is the admittance of only the second SIS junction without the IF circuit input admittance $Y_{\rm IF}$. Equation 3.2 is, in this case,

$$Y_{\rm in} = Y_1 + Y_0 \frac{Y_2' + Y_{\rm IF} + iY_0 \tan(\beta l)}{Y_0 + i\,(Y_2' + Y_{\rm IF}) \tan(\beta l)} \ . \tag{3.37}$$

The reflection coefficient expression in Equation 3.3 expands to

$$\Gamma = \frac{Y_0\,(Y_{\rm in} - Y_1 - Y_2' - Y_{\rm IF}) + i\,(Y_{\rm in}Y_2' - Y_1Y_2' + Y_{\rm in}Y_{\rm IF} - Y_1Y_{\rm IF} - Y_0^2)\tan(\beta l)}{Y_0\,(Y_{\rm in} + Y_1 + Y_2' + Y_{\rm IF}) + i\,(Y_{\rm in}Y_2' + Y_1Y_2' + Y_{\rm in}Y_{\rm IF} + Y_1Y_{\rm IF} + Y_0^2)\tan(\beta l)} \ . \tag{3.38}$$

The real and imaginary parts in Equation 3.36 can be separated

$$G_2 + iB_2 = G_2' + G_{\rm IF} + i\,(B_2' + B_{\rm IF}) \ , \tag{3.39}$$

and G_2 and B_2 can be substituted in Equation 3.4 to obtain

$$G_{\rm in} = G_1 + Y_0^2 \frac{(G_2' + G_{\rm IF})\,(1 + T^2)}{[Y_0 - (B_2' + B_{\rm IF})\,T]^2 + (G_2' + G_{\rm IF})^2\,T^2} \tag{3.40}$$

and in Equation 3.5 to obtain

$$B_{\rm in} = B_1 + Y_0 \frac{Y_0\,(B_2' + B_{\rm IF})\,(1 - T^2) + [Y_0^2 - (G_2' + G_{\rm IF}) - (B_2' + B_{\rm IF})]\,T}{[Y_0 - (B_2' + B_{\rm IF})\,T]^2 + (G_2' + G_{\rm IF})^2\,T^2} \ . \tag{3.41}$$

As previously, we again consider the special case of two identical junctions with $Y_1 = Y_2' = Y$. In this case, the reflection coefficient in Equation 3.38 simplifies to

$$\Gamma = \frac{Y_0\left(Y_{\text{in}} - 2Y - Y_{\text{IF}}\right) + i\left(Y_{\text{in}}Y - Y^2 + Y_{\text{in}}Y_{\text{IF}} - YY_{\text{IF}} - Y_0^2\right)\tan\left(\beta l\right)}{Y_0\left(Y_{\text{in}} + 2Y + Y_{\text{IF}}\right) + i\left(Y_{\text{in}}Y' + Y^2 + Y_{\text{in}}Y_{\text{IF}} + YY_{\text{IF}} + Y_0^2\right)\tan\left(\beta l\right)} \,. \tag{3.42}$$

The admittance for the matched case $\Gamma = 0$ can be expressed as

$$G_{\text{in}} = G + Y_0^2 \frac{\left(G + G_{\text{IF}}\right)\left(1 + T^2\right)}{\left[Y_0 - \left(B + B_{\text{IF}}\right)T\right]^2 + \left(G + G_{\text{IF}}\right)^2 T^2} \tag{3.43}$$

and

$$B_{\text{in}} = B + Y_0 \frac{Y_0\left(B + B_{\text{IF}}\right)\left(1 - T^2\right) + \left[Y_0^2 - \left(G + G_{\text{IF}}\right) - \left(B + B_{\text{IF}}\right)\right]T}{\left[Y_0 - \left(B + B_{\text{IF}}\right)T\right]^2 + \left(G + G_{\text{IF}}\right)^2 T^2} \,. \tag{3.44}$$

The IF circuit admittance complicates the previously more simple expressions in Equations 3.7 and 3.8, preventing a simple and insightful discussion of the special cases. However, Equations 3.43 and 3.44 can guide the design process of a twin junction circuit taking the IF circuit into account while working with the identical junction simplification.

3.3 Conclusion

We have derived analytical expressions for the design of the twin junction mixer, for both identical and non-identical tunnel junctions. We have shown that the commonly employed quarter-wavelength transmission line length that connects the junctions is not always the ideal choice, even if matching to a real RF circuit impedance is sought. Other solutions may be more suitable depending on the parameters of the junction. In fact, tuning out the junction's capacitance may not be the ideal design procedure for mixers that employ complex RF circuit impedance. The analysis given, therefore, contributes to additional miniaturising of the mixer circuits and hence allows the integration of important receiver circuits, such as the on-chip integration of the dual-polarisation receiver presented later in this thesis. Notice that our mathematical derivations are based on modelling the mixer using lossless transmission lines with the SIS devices as a lumped element. This method has shown to work very well in SIS mixers operating below the superconducting gap (700 GHz for niobium) and using small SIS devices ($\approx 1\,\mu\text{m}^2$), which are necessary for large RF bandwidth.

Chapter 4

Embedding Impedance Recovery

Chapter in preparation for publication: J. Wenninger, G. Yassin, and B. K. Tan, "Determining embedding circuit parameters from DC measurements on twin junction mixers," *In preparation for publication in IEEE Transactions on Terahertz Science and Technology*, 2024.

In the previous sections, we presented a method to optimise the coupling between the mixer RF circuit and the twin junction device. It is, however, useful for the designer to actually verify the effectiveness of this matching since the accuracy of the design can be degraded by fabricating tolerances and circuit parasitics. This can be achieved by experimentally measuring the impedance of the embedding circuit using the measured pumped and unpumped IV curves of the mixer. The recovery of the embedding impedance of a single junction mixer has already been reported, and several computational techniques have been used [94–96].

In the following, we first introduce the embedding impedance recovery of a single junction mixer circuit to reiterate the established equation set, the recovery methods and several associated aspects. In the second section of this chapter, we expand the equation set and methods for a single junction mixer circuit to apply them to a twin junction mixer.

4.1 Single Junction Impedance Recovery

The measurable set of unpumped and pumped IV curves contain the information of the SIS junction as well as the circuit around it, in particular, the admittance of the mixer circuit which embeds the SIS junction. According to Thévenin's theorem, the

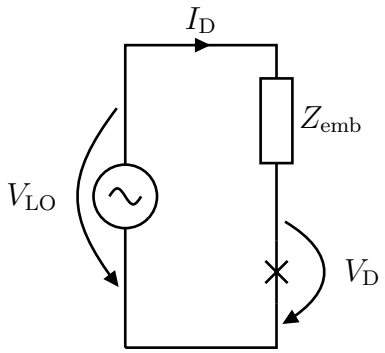


Figure 4.1: The Thévenin equivalent circuit representations of a single junction mixer circuit.

components connecting the SIS junction can be represented by a single voltage source with an impedance embedding the SIS junction Z_{emb} in a serial circuit [97, 98]. The theorem is, however, valid for linear components only, which is the case for passive components, in our case, with the SIS junction linearised at its operational point. This approximation has been shown to apply to SIS mixer receivers. The Thévenin equivalent circuit of the mixer is shown in Figure 4.1, and the circuit equation can be written as

$$V_{\mathrm{LO}} = V_{\mathrm{D}} + Z_{\mathrm{emb}} I_{\mathrm{D}} \ , \tag{4.1}$$

where V_{LO} is the source voltage, V_{D} is the voltage across the SIS junction device, and $Z_{\mathrm{emb}} I_{\mathrm{D}}$ is the product of the embedding impedance and the current through the SIS junction device.

The pumping level is the strength of the AC signal voltage across the junction normalised to the photon energy equivalent voltage V_{Ph}

$$\alpha_{\mathrm{D}} = \frac{e}{h f_{\mathrm{LO}}} \left| V_{\mathrm{D}} \right| = \frac{\left| V_{\mathrm{D}} \right|}{V_{\mathrm{Ph}}} \ , \tag{4.2}$$

where f_{LO} is the source frequency, h is Planck's constant, and e is the electron charge. The pumping level and the unpumped IV curve determine the AC through the SIS device following the relation [79]

$$\begin{aligned} I_{\mathrm{D}}(V_0, \alpha_{\mathrm{D}}) = \sum_{n=-\infty}^{\infty} & J_n(\alpha_{\mathrm{D}}) \left[J_{n-1}(\alpha_{\mathrm{D}}) + J_{n+1}(\alpha_{\mathrm{D}}) \right] \\ & \left[I_{\mathrm{DC}} \left(V_0 - n V_{\mathrm{Ph}} \right) + i I_{\mathrm{KK}} \left(V_0 - n V_{\mathrm{Ph}} \right) \right] \ , \end{aligned} \tag{4.3}$$

which is the current of the first harmonic $m = 1$, assuming second- and higher-order harmonics are shorted by the capacitance of the SIS junction. I_{D} is complex due to the Fourier components, where the reactive term depends on the Kramers-Kronig

transformation I_{KK} of the measurable unpumped IV curve I_{DC} [79]. The embedding impedance $Z_{\mathrm{emb}} = R_{\mathrm{emb}} + iX_{\mathrm{emb}}$ is, in general, complex with the real embedding resistance R_{emb} and imaginary embedding reactance X_{emb}. We have, therefore, the choice to set the phase of either V_{LO} or V_{D} in Equation 4.1 to zero. α_{D} also links the unpumped and pumped IV curves by

$$I_0(V_0, \alpha_{\mathrm{D}}) = \sum_{n=-\infty}^{\infty} J_n^2(\alpha_{\mathrm{D}}) I_{\mathrm{DC}}\left(V_0 - nV_{\mathrm{Ph}}\right) \tag{4.4}$$

via the tunnelling probability $J_n^2(\alpha_{\mathrm{D}})$, where J is the Bessel function of the first kind of n^{th} order.

4.1.1 Impedance Recovery Methods

Equation 4.1, representing the circuit in Figure 4.1, needs to be satisfied for all V_0 of V_{D}, while Z_{emb} and V_{LO} are independent of V_0. Thus, the unknowns Z_{emb} and V_{LO} can be determined by satisfying Equation 4.1 for different V_0. The complex phase of V_{LO} is irrelevant for the impedance recovery, hence, only the magnitude of the source voltage is used $|V_{\mathrm{LO}}|$. We are, therefore, at liberty to assume that V_{D} is real. In practice, the bias voltages V_0 of the first photon step are used because they show the largest DC response and, therefore, a well-defined α_{D} in Equation 4.4.

In what follows, we shall describe four methods of finding Z_{emb} and $|V_{\mathrm{LO}}|$:

1. **Eyeball Method:** The eyeball method is the simplest method, initially presented by Skalare with a Norton equivalent circuit [94]. The Norton and Thévenin equivalent circuits are interchangeable, and within this chapter, we only use the Thévenin representation.

   Following the flowchart in Figure 4.2, one guesses the values of Z_{emb} and $|V_{\mathrm{LO}}|$ and evaluates the circuit Equation 4.1 to obtain $V_{\mathrm{D}}(V_0)$. The circuit equation is solved implicitly at each bias voltage by minimising

   $$\epsilon^{\mathrm{Circ}} = |V_{\mathrm{LO}}|^2 - |V_{\mathrm{D}} + Z_{\mathrm{emb}} I_{\mathrm{D}}|^2 \tag{4.5}$$

   because of the V_{D} dependency of I_{D}. The obtained $V_{\mathrm{D}}(V_0)$ for an Z_{emb} and $|V_{\mathrm{LO}}|$ guess is then used in Equation 4.4 to obtain a simulated pumped IV curve I_0^{Sim}, which is compared to the measured pumped IV curve I_0^{Meas} by eye, judging the overlap subjectively and giving this method its name, or by introducing an error surface function ϵ. The error to be minimised for the Eyeball method is

   $$\epsilon^{\mathrm{Eye}} = \sum_{v_0} \left[\left| I_0^{\mathrm{Meas}}(V_0 = v_0) \right| - \left| I_0^{\mathrm{Sim}}(V_0 = v_0) \right| \right]^2 \ . \tag{4.6}$$

The three parameters minimised for are $Z_{\rm emb} = R_{\rm emb} + iX_{\rm emb}$ and $|V_{\rm LO}|$. For each set of $R_{\rm emb}$, $X_{\rm emb}$ and $|V_{\rm LO}|$, circuit Equation 4.1 is satisfied to get $V_{\rm D}(V_0)$, and then Equation 4.4 is applied to get $I_0^{\rm Sim}$.

We will now implement the method on a 230 GHz SIS mixer at 260 GHz. The measured $I_{\rm DC}$ and I_0 of this mixer are shown in Figure 4.3. The positive slope of the photon step indicates capacitive tuning, which is reasonable considering the fact that the mixer is pumped on its upper-frequency band end. Minimising the error surface in the voltage range from 1.8 mV to 2.45 mV yields $Z_{\rm emb} = (2.47 - i12.95)\ \Omega$ and $|V_{\rm LO}| = 1.21$ mV. We show the fitted IV response in Figure 4.4 alongside other IV responses for different $|V_{\rm LO}|$ values. The larger the $|V_{\rm LO}|$, the stronger the pumping and the higher the photon step current I_0. Similarly, we show the effect of varying $Z_{\rm emb}$ in Figure 4.5. A flat photon step results from little reactive components, while a positive IV slope results from a capacitive $Z_{\rm emb}$, and a negative IV slope indicates an inductive $Z_{\rm emb}$. $I_0^{\rm Meas}$ has a positive slope, and therefore, $Z_{\rm emb}$ is very capacitive.

2. **RF Voltage Match Method:** The last steps of the Eyeball method in Figure 4.2 are redundant since $\alpha_{\rm D}$ can be determined from the measured $I_{\rm DC}$ and I_0 from Equation 4.4. Thus, a more efficient way is to compute $\alpha_{\rm D}^{\rm Meas}$ from the measured $I_{\rm DC}$ and I_0 and compare $\alpha_{\rm D}^{\rm Meas}$ with the simulated $\alpha_{\rm D}^{\rm Sim}$, which is obtained from a set of $R_{\rm emb}$, $X_{\rm emb}$ and $|V_{\rm LO}|$ and Equation 4.1 as in the Eyeball method.

   The error surface in this method is

$$\epsilon^{\rm RF} = \sum_{v_0} \left[\left|\alpha_{\rm D}^{\rm Meas}(V_0 = v_0)\right| - \left|\alpha_{\rm D}^{\rm Sim}(V_0 = v_0)\right| \right]^2 , \tag{4.7}$$

   which follows directly on determining $V_{\rm D}$ with $\epsilon^{\rm Circ}$ and Equation 4.5 in Figure 4.2. Equation 4.1 is solved for a guessed set of $R_{\rm emb}$, $X_{\rm emb}$ and $|V_{\rm LO}|$ to obtain $\alpha_{\rm D}^{\rm Sim}$, which is then used to minimise the error surface. Although this method is faster than the Eyeball Method, it is still slow since three free parameters are fitted, and Equation 4.1 is still implicitly solved for $\alpha_{\rm D}^{\rm Sim}$ because of $I_{\rm D}(\alpha_{\rm D}^{\rm Sim})$.

   Minimising the error in the voltage range of the first photon step from 1.8 mV to 2.45 mV yields $Z_{\rm emb} = (2.29 - i13.44)\ \Omega$ and $|V_{\rm LO}| = 1.23$ mV, which is similar to the Eyeball method result. Figure 4.6 shows the fit between $\alpha_{\rm D}^{\rm Meas}$ and $\alpha_{\rm D}^{\rm Sim}$ and the resulting match between the $I_0^{\rm Meas}$ and $I_0^{\rm Sim}$. Furthermore, the noisy response of $\alpha_{\rm D}^{\rm Meas}$ for $V_0 < 1.5$ mV illustrates the reason for fitting only on the first photon step.

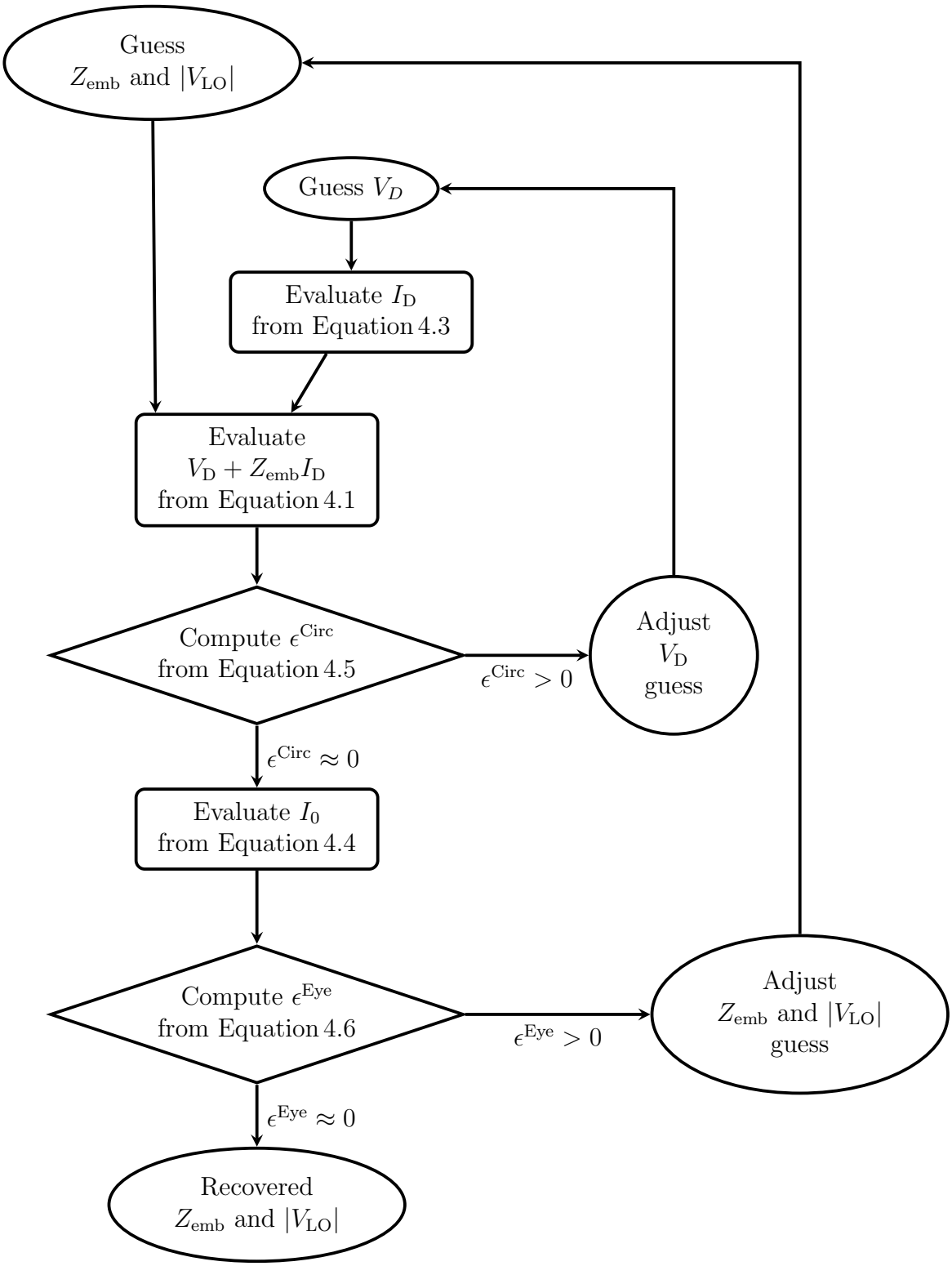


Figure 4.2: Flowchart for the Eyeball method. Equation 4.2 is used to relate $\alpha_{\text{D}} \propto |V_{\text{D}}|$.

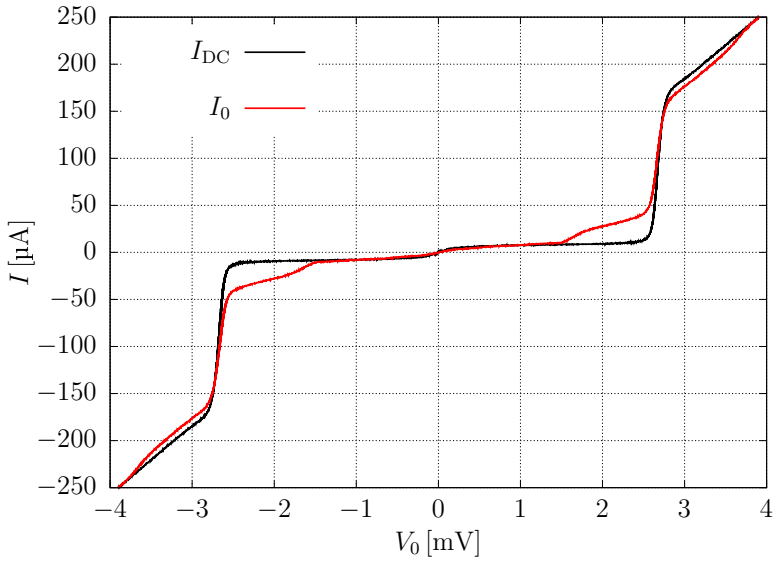


Figure 4.3: The measured I_{DC} and I_0. Both datasets are only corrected for the voltage offsets and sorted by increasing V_0.

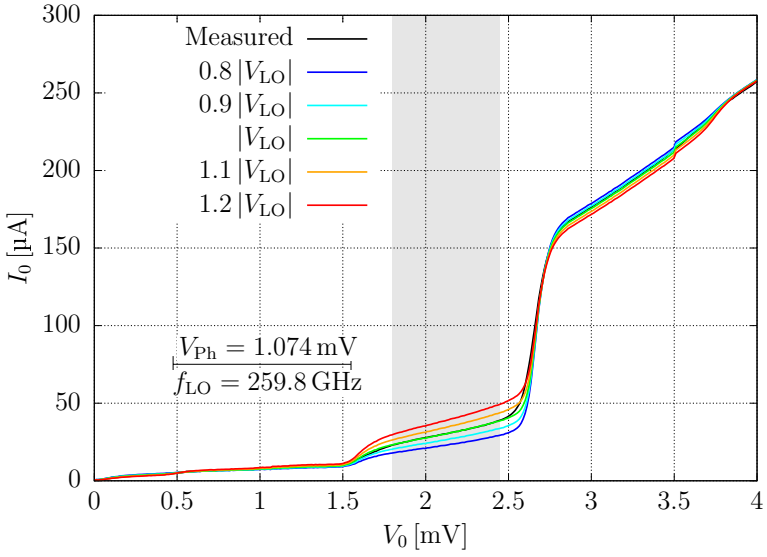


Figure 4.4: The IV responses for different values of $|V_{\mathrm{LO}}|$ in terms of the recovered $|V_{\mathrm{LO}}| = 1.21\,\mathrm{mV}$ and $Z_{\mathrm{emb}} = (2.47 - i12.95)\ \Omega$ obtained with the Eyeball method. The fitting range from 1.8 mV to 2.45 mV is shaded grey.

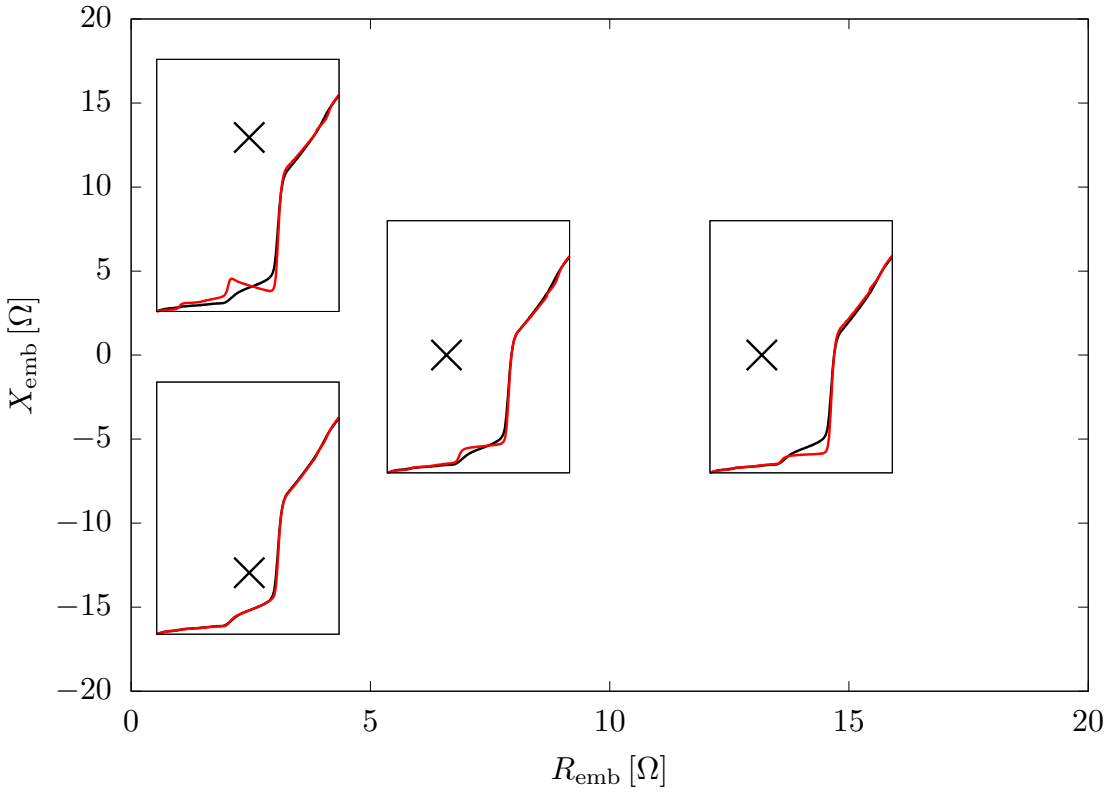


Figure 4.5: The IV responses for different values of Z_{emb} for $|V_{\mathrm{LO}}| = 1.21\,\mathrm{mV}$. $\times$ indicates Z_{emb} of each inset. The black line of the insets is I_0^{Meas}, and the red lines are the I_0^{Sim} for the respective Z_{emb} value. The insets have a voltage range from 0.0 mV to 4.0 mV on the x-axis and a current range from 0 µA to 300 µA.

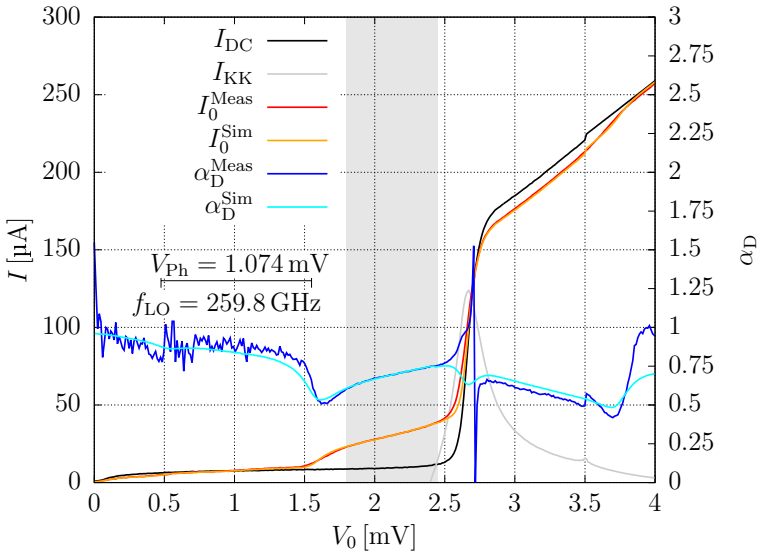


Figure 4.6: In the RF voltage match method, the pumping levels $\alpha_{\mathrm{D}}^{\mathrm{Meas}}$ and $\alpha_{\mathrm{D}}^{\mathrm{Sim}}$ are compared in the grey-shaded fitting range from 1.8 mV to 2.45 mV to find the recovered pumped IV curve measured.

3. **Voltage Divider Method:** The Thévenin equivalent circuit implies that the voltage across the junction is given by

$$V_{\mathrm{D}}(V_0) = |V_{\mathrm{LO}}(V_0)| \, \frac{Z_{\mathrm{D}}(V_0, V_{\mathrm{D}})}{Z_{\mathrm{emb}} + Z_{\mathrm{D}}(V_0, V_{\mathrm{D}})} \tag{4.8}$$

with the SIS device equivalent impedance defined as

$$Z_{\mathrm{D}}(V_0) = \frac{V_{\mathrm{D}}(V_0)}{I_{\mathrm{D}}(V_0, \alpha_{\mathrm{D}})} \; . \tag{4.9}$$

However, Z_{D} can be computed from $\alpha_{\mathrm{D}}^{\mathrm{Meas}}$, which is obtained from the I_{DC} and I_0 with Equation 4.4. Thus, the simulated voltage across the SIS device can be computed directly from a guessed set of R_{emb}, X_{emb} and $|V_{\mathrm{LO}}|$ and Equation 4.8 without having implicit equations that require iterations to solve. Consequently, the error surface

$$\epsilon^{\mathrm{Div}} = \sum_{v_0} \left[\left| V_{\mathrm{D}}^{\mathrm{Meas}}(V_0 = v_0) \right| - \left| V_{\mathrm{LO}} \frac{Z_{\mathrm{D}}(V_0 = v_0)}{Z_{\mathrm{emb}} + Z_{\mathrm{D}}(V_0 = v_0)} \right| \right]^2 \tag{4.10}$$

can be minimised relatively quickly.

Minimising the error in the voltage range of the first photon step from 1.8 mV to 2.45 mV yields $Z_{\mathrm{emb}} = (2.23 - i13.88)\ \Omega$ and $|V_{\mathrm{LO}}| = 1.24\,\mathrm{mV}$. We show the error surface across the different dimensions at the optimum value for the respective third parameter in Figure 4.7.

4. **Voltage Divider Derivative Method:** Withington et al. introduced a powerful improvement to this method by reducing the number of variables [95]: The error surface minimum can be determined only with $Z_{\mathrm{emb}} = R_{\mathrm{emb}} + iX_{\mathrm{emb}}$. $|V_{\mathrm{LO}}|$ is eliminated by noting that the derivative of the error surface ϵ^{Div} needs to be 0 at the minimum. We take the partial derivative by applying the chain rule following Withington et al. [95] and obtain

$$\begin{aligned}
\frac{\partial \epsilon^{\mathrm{Div}}}{\partial |V_{\mathrm{LO}}|} &= \frac{\partial \left[\sum_{v_0} \left(\left| V_{\mathrm{D}}^{\mathrm{Meas}}(V_0 = v_0) \right| - \left| V_{\mathrm{LO}} \frac{Z_{\mathrm{D}}(V_0 = v_0)}{Z_{\mathrm{emb}} + Z_{\mathrm{D}}(V_0 = v_0)} \right| \right)^2 \right]}{\partial |V_{\mathrm{LO}}|} \\
&= -\sum_{v_0} 2 \begin{bmatrix} \left| V_{\mathrm{D}}^{\mathrm{Meas}}(V_0 = v_0) \right| \\ - \left| V_{\mathrm{LO}} \frac{Z_{\mathrm{D}}(V_0 = v_0)}{Z_{\mathrm{emb}} + Z_{\mathrm{D}}(V_0 = v_0)} \right| \end{bmatrix} \left[\left| \frac{Z_{\mathrm{D}}(V_0 = v_0)}{Z_{\mathrm{emb}} + Z_{\mathrm{D}}(V_0 = v_0)} \right| \right] \\
&= -\sum_{v_0} 2 \begin{bmatrix} \left| V_{\mathrm{D}}^{\mathrm{Meas}}(V_0 = v_0) \frac{Z_{\mathrm{D}}(V_0 = v_0)}{Z_{\mathrm{emb}} + Z_{\mathrm{D}}(V_0 = v_0)} \right| \\ - \left| V_{\mathrm{LO}} \left(\frac{Z_{\mathrm{D}}(V_0 = v_0)}{Z_{\mathrm{emb}} + Z_{\mathrm{D}}(V_0 = v_0)} \right)^2 \right| \end{bmatrix} \; .
\end{aligned} \tag{4.11}$$

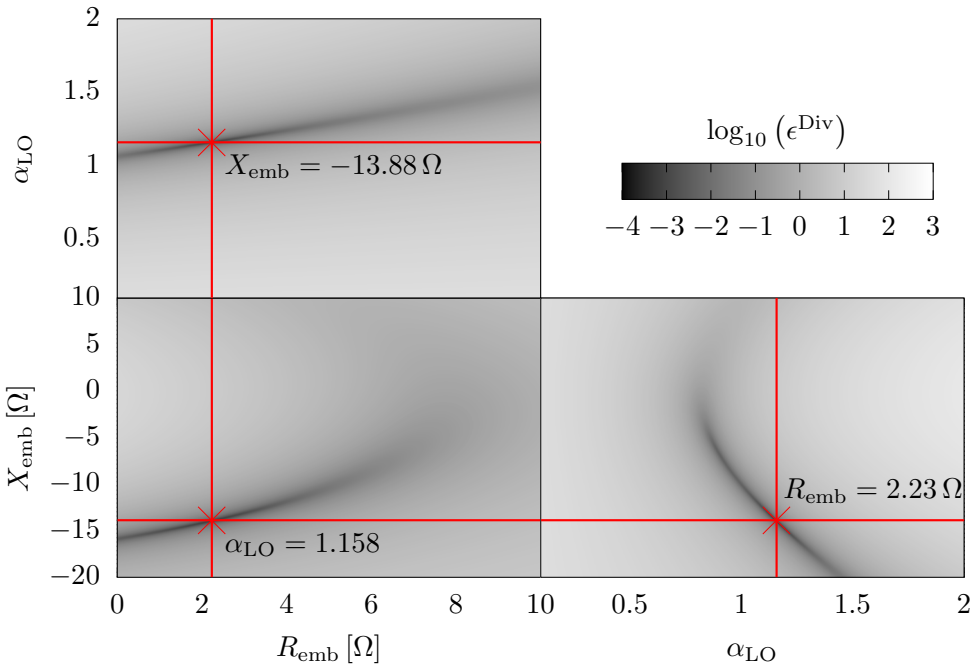


Figure 4.7: The error surfaces of the voltage divider method.

The sum of this result is separated into two terms. Then, the result is set to 0 and solved for the source voltage

$$|V_{\mathrm{LO}}| = \frac{\sum_{v_0} \left| V_{\mathrm{D}}^{\mathrm{Meas}}(V_0 = v_0) \frac{Z_{\mathrm{D}}(V_0=v_0)}{Z_{\mathrm{emb}}+Z_{\mathrm{D}}(V_0=v_0)} \right|}{\sum_{v_0} \left| \left[\frac{Z_{\mathrm{D}}(V_0=v_0)}{Z_{\mathrm{emb}}+Z_{\mathrm{D}}(V_0=v_0)} \right]^2 \right|} \,. \tag{4.12}$$

Substituting this back into Equation 4.10 and solving the binomial formula returns a new error surface

$$\epsilon^{\mathrm{Der}} = \left[\sum_{v_0} \left| V_{\mathrm{D}}^{\mathrm{Meas}}(V_0 = v_0) \right|^2 \right] - \frac{\left[\sum_{v_0} \left| V_{\mathrm{D}}^{\mathrm{Meas}}(V_0 = v_0) \frac{Z_{\mathrm{D}}(V_0=v_0)}{Z_{\mathrm{emb}}+Z_{\mathrm{D}}(V_0=v_0)} \right| \right]^2}{\sum_{v_0} \left| \left[\frac{Z_{\mathrm{D}}(V_0=v_0)}{Z_{\mathrm{emb}}+Z_{\mathrm{D}}(V_0=v_0)} \right]^2 \right|} \,, \tag{4.13}$$

with only $Z_{\mathrm{emb}} = R_{\mathrm{emb}} + iX_{\mathrm{emb}}$ as unknowns.
Therefore, the error surface can be directly calculated for a pair of R_{emb} and X_{emb}, and the minimum is determined in the voltage range of the first photon step from 1.8 mV to 2.45 mV, as shown in Figure 4.8. In a subsequent step, $|V_{\mathrm{LO}}| = 1.23\,\mathrm{mV}$ is determined by solving Equation 4.12 at the error surface minimum $Z_{\mathrm{emb}} = (2.30 - i13.42)\ \Omega$.

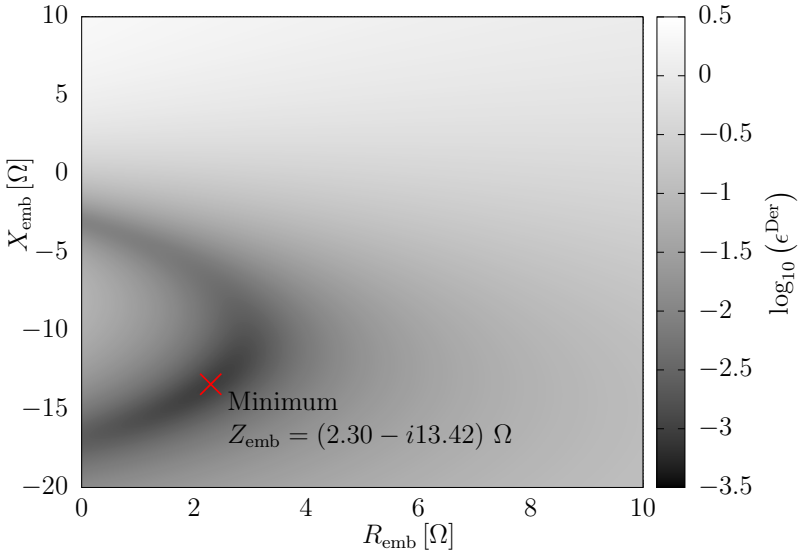


Figure 4.8: The error surface of the voltage divider with the derivative method that eliminates $|V_{\mathrm{LO}}|$.

4.1.2 Discussion of the Impedance Recovery Methods

All presented methods yield very similar, almost identical, $I_{\mathrm{dc}}^{\mathrm{Sim}}$, as shown in Figure 4.9, and the Z_{emb} and $|V_{\mathrm{LO}}|$ values are reasonably similar. The error surfaces in Figures 4.7 and 4.8 show that the error surface is very low over a wide parameter space. Thus, the location of the minimum might vary.

In fact, the impedance recovery method is very sensitive to small changes, e.g. measurement noise, and therefore the recovered parameters should be treated as a guidance value. We binned the measured data into equispaced voltage bins of $0.011 V_{\mathrm{Ph}}$ with a bin for 0 mV to match the currents of I_{DC} and I_0. Changing the bin size or having the bin boundary at 0 mV affects the result. Moreover, the results differ for impedance recoveries performed at different fitting intervals or using only the negative or positive voltage interval. Table 4.1 summarises the deviations caused by these systematic variations. The table also shows the effect of halving the magnetic field and a shift of 5 GHz to 255 GHz LO frequency to set the deviations due to systematic variation in relation to real deviations.

Finally, we would like to highlight that the sums in Equations 4.3 and 4.4 have been taken between $n = \pm 15$. The choice for this range is motivated by sufficiently representing small contributions for larger ns in our application ($\alpha < 3$) without adding negligible terms to the computation. The measured unpumped IV response is extended to larger voltages with linear regression of the normal resistance R_{N} region

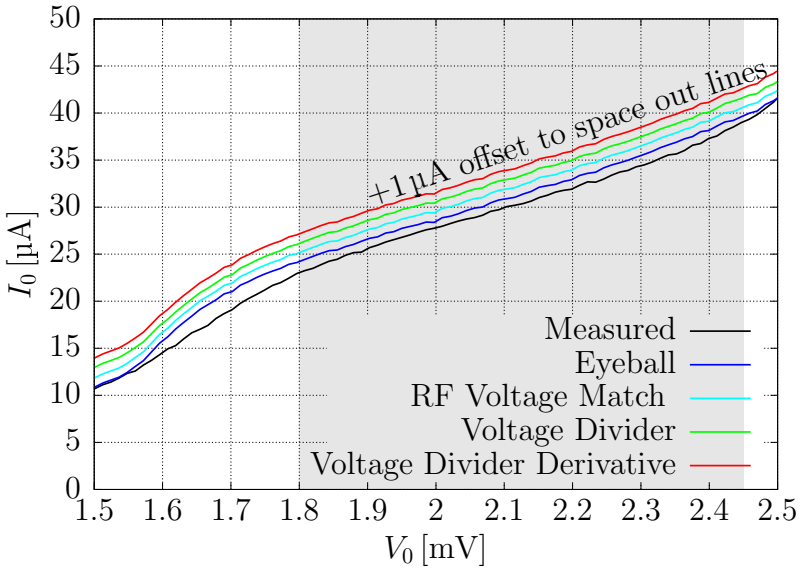


Figure 4.9: A comparison of the recovered pumped IV curves with the four methods presented and the measured pumped IV curve. An 1 µA offset is introduced to distinguish the individual traces. The fitting range from 1.8 mV to 2.45 mV is shaded grey.

to evaluate I_{DC} and I_{KK} at $V_0 + nV_{\mathrm{Ph}}$ for large ns.

4.1.3 Power

The results above allow us to calculate the power available to the circuit and the power absorbed by the SIS device. The power absorbed by the SIS device is

$$P_{\mathrm{D}} = \frac{|V_{\mathrm{D}}|\,\mathfrak{Re}\{I_{\mathrm{D}}\}}{2}\ , \tag{4.14}$$

using quantities required for the impedance recovery. The 1/2 results from the root mean square of a sinusoidal signal accounting for time averaging. The absolute value of V_{D} is used because I_{D} is calculated from $\alpha_{\mathrm{D}} = |V_{\mathrm{D}}|/V_{\mathrm{Ph}}$, and using only the real term of I_{D} allows us to calculate the true power without the reactive terms.

Similarly, the maximum power available from the Thévenin circuit is

$$P_{\mathrm{av}} = \frac{|V_{\mathrm{emb}}|^2}{2R_{\mathrm{emb}}} = \frac{|V_{\mathrm{LO}}|^2}{8R_{\mathrm{emb}}} = \frac{|V_{\mathrm{D}} + Z_{\mathrm{emb}}I_{\mathrm{D}}|^2}{8R_{\mathrm{emb}}} \tag{4.15}$$

using the quantities recovered above. V_{emb} is the voltage across the embedding impedance Z_{emb} in Figure 4.1. Again the true power is calculated from real R_{emb} and the voltage across the circuit. Factor 8 comprises the time averaging of the voltage $\sqrt{(2)^2} = 2$ and the voltage at the Thévenin circuit $V_{\mathrm{LO}} = 2V_{\mathrm{emb}}$ at maximum power transfer occurring for $Z_{\mathrm{emb}} = Z_{\mathrm{D}}$, where Z_{D} is the impedance of the SIS device.

	$\lvert V_{\mathrm{LO}}\rvert$ [mV]	R_{emb} [Ω]	X_{emb} [Ω]
Voltage Divider Derivative Method	**1.23**	**2.30**	**-13.42**
Voltage Divider Method	1.24	2.23	-13.88
RF Voltage Match Method	1.23	2.29	-13.44
Eyeball Method	1.21	2.47	-12.95
With 0 mV voltage bin	1.28	2.63	-13.94
positive fitting range only	1.25	3.00	-12.87
negative fitting range only	1.27	2.56	-13.90
averaging two fitting range only	1.26	2.78	-13.38
0.02 mV voltage bins	1.23	2.16	-13.62
Different fitting interval	1.27	2.54	-14.06
Half coil current	1.26	2.78	-13.42
Lower frequency	1.76	3.71	-10.32

Table 4.1: Different results obtained using different methods and settings. The different settings are applied to the voltage divider derivative method.

The analysis of the power shown in Figure 4.10 has two interesting features. First, the power absorbed by the SIS device compared to the maximum power available by the source indicates the matching. The ratio shown on the right y-axis shows that less than 40% of the available power is absorbed by the SIS device. Second, the latter two terms in Equation 4.15 are constant and bias-voltage dependent. Hence, one can use them to validate the impedance recovery. The good matching between the dark blue trace $P_{\mathrm{av}}(V_0)$ in Figure 4.10 and the light blue trace representing the constant $P_{\mathrm{av}}^{V_{\mathrm{LO}}} = \frac{|V_{\mathrm{LO}}|^2}{8R_{\mathrm{emb}}}$ shows that our impedance recovery is valid.

4.2 Twin Junction Impedance Recovery

The impedance recovery of a single SIS junction mixer incorporates the tuning circuit in Z_{emb}. Twin junction mixers are represented differently because the SIS device response is distributed between two SIS junctions. The interconnection of these two SIS junctions is maintained by a transmission line shown in Figure 4.11a, and the distributed circuit response of the transmission line has to be accounted for in the calculations. Nonetheless, the twin junction arrangement can be simplified to the circuit shown in Figure 4.11b, which resembles the Thévenin equivalent circuit of a single junction mixer.

In what follows, therefore, we will essentially use the same impedance recovery

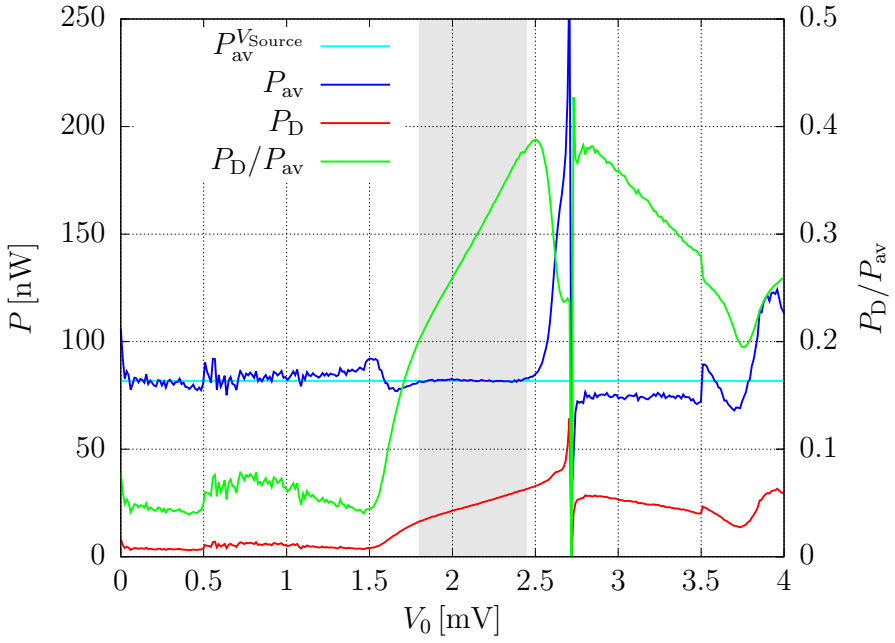
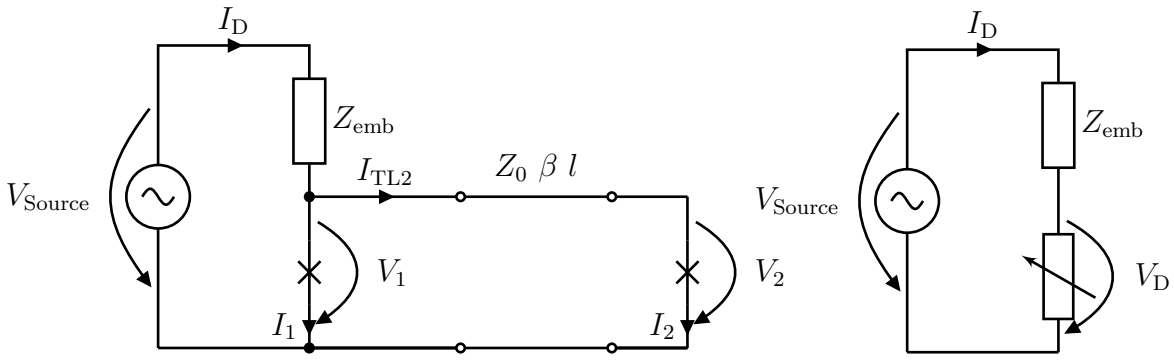


Figure 4.10: The power absorbed by the SIS junction device P_{D} and the maximum power available from the Thévenin circuit P_{av}. Both methods to compute P_{av} presented in Equation 4.15 are shown. The green curve shows the ratio of $P_{\mathrm{D}}/P_{\mathrm{av}}$. The fitting range from 1.8 mV to 2.45 mV is shaded grey.



(a) Barrier representation; (b) Device representation;

Figure 4.11: The Thévenin equivalent circuit representations of a twin junction mixer circuit.

technique as discussed previously, but the single junction will now be replaced by a lumped element component Z_{D} representing the twin junction device. The two junctions of the twin junction device will, in general, have different pumping levels even when the junctions are assumed to be identical. As a result, the impedance recovery requires additional steps to link the two SIS junctions.

4.2.1 Twin-Junction Equations

The Thévenin equivalent circuit in Figure 4.11b has the same circuit equation as the single junction equivalent circuit

$$V_{\mathrm{Source}} = V_{\mathrm{D}} + Z_{\mathrm{emb}} I_{\mathrm{D}} \ . \tag{4.16}$$

However, the device voltage V_{D} is now across the twin junction circuit, which is also the voltage of the first SIS junction $V_{\mathrm{D}} = V_1$ due to the circuit configuration.

The following analysis of the voltages and currents requires the barrier representation with the transmission line in Figure 4.11a. The voltage at the SIS junctions and the current into the transmission line connecting the second SIS junction are given by the ABCD matrix relations of two-port circuits

$$\begin{aligned} \begin{pmatrix} V_1 \\ I_{\mathrm{TL2}} \end{pmatrix} &= \begin{pmatrix} \cos(\beta l) & iZ_0 \sin(\beta l) \\ \frac{i\sin(\beta l)}{Z_0} & \cos(\beta l) \end{pmatrix} \begin{pmatrix} 1 & 0 \\ Y_2 & 1 \end{pmatrix} \begin{pmatrix} V_2 \\ 0 \end{pmatrix} \\ &= \begin{pmatrix} V_2 \left[\cos(\beta l) + iY_2 Z_0 \sin(\beta l)\right] \\ V_2 \left[Y_2 \cos(\beta l) + \frac{i\sin(\beta l)}{Z_0}\right] \end{pmatrix} . \end{aligned} \tag{4.17}$$

More detail on the ABCD matrix can be found in Appendix A.1. Y_1 and Y_2 are the admittances of the first and second SIS junction, respectively, and the transmission line connecting the two junctions has a length l, propagation constant β and characteristic impedance Z_0. The voltage across the first junction V_1 is, therefore, related to the voltage and current through the second junction, V_2 and I_2, respectively, by the relation

$$\begin{aligned} V_1(V_0) &= V_2(V_0)\left[\cos(\beta l) + iY_2(V_0) Z_0 \sin(\beta l)\right] \\ &= V_2(V_0)\cos(\beta l) + iI_2(V_0, |V_2|) Z_0 \sin(\beta l) \ , \end{aligned} \tag{4.18}$$

and the current through the transmission line is

$$\begin{aligned} I_{\mathrm{TL2}} &= V_2 \left[Y_2 \cos(\beta l) + i\frac{\sin(\beta l)}{Z_0}\right] \\ &= I_2 \cos(\beta l) + i\frac{V_2 \sin(\beta l)}{Z_0} \ . \end{aligned} \tag{4.19}$$

Consequently, the current from the source in Figure 4.11 sums up to

$$\begin{aligned} I_{\mathrm{D}} =& I_1 + I_{\mathrm{TL2}} \\ =& I_1(V_0, |V_1|) + I_2(V_0, |V_2|)\cos(\beta l) + i\frac{V_2(V_0)\sin(\beta l)}{Z_0} \ . \end{aligned} \tag{4.20}$$

The tunnelling current through the k^{th} SIS junction is

$$\begin{aligned} I_k(V_0, V_k) = \sum_{n=-\infty}^{\infty} & J_n(\alpha_k)\left[J_{n-1}(\alpha_k) + J_{n+1}(\alpha_k)\right] \\ & \left[I_{DC,k}\left(V_0 - nV_{\mathrm{Ph}}\right) + iI_{\mathrm{KK},k}\left(V_0 - nV_{\mathrm{Ph}}\right)\right] e^{i\phi_k} \ , \end{aligned} \tag{4.21}$$

similar to the single junction, but with the addition of a phase factor

$$\phi_k = \arctan^{-1}\left(\frac{\mathfrak{Im}\left\{V_k\right\}}{\mathfrak{Re}\left\{V_k\right\}}\right) \ . \tag{4.22}$$

The two SIS junctions are distinguished by the integer k, and only one junction can be chosen to have a real V_k, which is the case for a single junction circuit. The junctions have individual pumping levels

$$\alpha_k(V_0, V_k) = |V_k(V_0)|\,\frac{e}{hf_{\mathrm{LO}}} = \frac{|V_k(V_0)|}{V_{\mathrm{Ph}}} \tag{4.23}$$

and unpumped DC $I_{\mathrm{DC,k}}$ with the corresponding Kramers-Kronig transformation $I_{\mathrm{KK,k}}$.

Consequently, the pumped DC response of the k^{th} junction is

$$I_{0,k}(V_0, \alpha_k) = \sum_{n=-\infty}^{\infty} J_n^2(\alpha_k) I_{\mathrm{DC},k}\left(V_0 - nV_{\mathrm{Ph}}\right) \ . \tag{4.24}$$

Both SIS junctions connect to the same microstrip and a common ground plane in a traditional twin junction receiver so that the two top and the two ground plane electrodes are shorted together. Hence, the measured DC is the sum of both junctions

$$I_0(V_0, \alpha_1, \alpha_2) = \sum_{n=-\infty}^{\infty} J_n^2(\alpha_1) I_{\mathrm{DC},1}(V_0 + nV_{\mathrm{Ph}}) + J_n^2(\alpha_2) I_{\mathrm{DC},2}(V_0 + nV_{\mathrm{Ph}}) \tag{4.25}$$

and

$$I_{\mathrm{DC}}(V_0) = I_{\mathrm{DC},1}(V_0) + I_{\mathrm{DC},2}(V_0) \ . \tag{4.26}$$

4.2.2 Special Cases

There are four interesting special cases which we would like to highlight:

Open Transmission Line Case $Z_0 = \infty$

If no transmission line connects the SIS junctions $Z_0 = \infty$, the result depends on βl and is obviously hypothetical. For $\sin(\beta l) = 1$, it is clear that $I_\mathrm{D} = I_1$, and the choice of V_2 does not affect V_1. For $\sin(\beta l) = 0$, $I_\mathrm{D} = I_1 + I_2$, and Equation 4.18 goes to infinity. However, as soon as $\sin(\beta l) > 0$, we find that $V_1 \gg V_2$. Hence, only the first SIS junction is pumped.

Single Junction Case $\beta l = 2n\pi$

If both junctions are at the same position $\beta l = 0$, or more general $\beta l = 2n\pi$, where n is an integer, the equation set introduced above reduces to the established formulation of a single SIS junction. In this case, both junctions are pumped identically $V_1 = V_2$ in Equation 4.18, and the device current in Equation 4.20 is $I_\mathrm{D} = I_1 + I_2$. Because of $V_1 = V_2$, the DC Equation 4.25 simplifies so that Equation 4.26 can be substituted to obtain the single junction expression. The same simplification can be applied to the AC in Equation 4.21 so that I_D is identical to the single junction case.

Half-Wavelength Transmission Line $\beta l = (2n+1)\pi$

This case causes $V_1 = -V_2$ in Equation 4.18. The definition in Equation 4.23, however, implies that $\alpha_1 = \alpha_2$ and $I_1 = -I_2$, where $e^{i\phi_k} = -1$ in Equation 4.21 for the V_k following the chosen (positive) V_k. The sign in Equation 4.20 flips twice, once because of the cosine and once because of the phase factor, resulting in an addition of the currents $I_\mathrm{D} = \pm(I_1 + I_2)$. Altogether, the end results for the $\beta l = 2n\pi$ and $\beta l = (2n+1)\pi$ are identical, and the intermediate results reflect only the 180° phase shift between the SIS junctions.

Quarter-Wavelength Transmission Line $\beta l = (2n+1)\pi/2$

The quarter wavelength case $\beta l = (2n+1)\pi/2$ reduces Equation 4.20 to

$$I_\mathrm{D} = I_1(V_0, |V_1|) \pm i\frac{V_2(V_0)}{Z_0} \tag{4.27}$$

and Equation 4.18 to

$$V_1(V_0) = \pm i Z_0 I_2(V_0, |V_2|)\ . \tag{4.28}$$

Substituting these results into the circuit Equation 4.16 yields

$$V_\mathrm{Source} = Z_\mathrm{emb} I_1(V_0, |V_1|) \pm i\left[\frac{Z_\mathrm{emb}}{Z_0} V_2(V_0) + Z_0 I_2(V_0, |V_2|)\right]\ . \tag{4.29}$$

4.2.3 Simplifications and Assumptions

Although the theoretical derivations we have given in this chapter are general, we decided to introduce several simplifications and assumptions to the coming simulations with the twin-junction equations. The motivation is to give a good introduction to the impedance recovery method, simplifying factors complicating the recovery process without requiring modifications to circuits. Hence, the simplifications and assumptions should make the recovery method easily applicable, giving a sufficient approximation to the true result.

4.2.3.1 Junction Size

Defining the SIS junction area in the fabrication process is a critical step carried out by specialists with years of experience, for which we give only a brief account in Appendix A.4. An optimised photolithography process is required to yield well-defined SIS junction areas without any remnants or defects at the SIS junctions preventing a connection to the SIS electrodes or causing shorts. Typically, the optimised process, especially the liftoff, is for a particular SIS junction area on a particular device layout. Consequently, differently sized SIS junctions in a twin junction add difficulty to the fabrication. We understand this is the reason for the lack of further investigations into employing differently sized SIS junctions in a twin-junction circuit.

Because, in practice, identically sized SIS junctions are employed, we will assume two identical SIS junctions for the simplicity of our calculations. Then, the measured unpumped DC splits evenly between the SIS junctions

$$I_{\mathrm{DC},1}(V_0) = I_{\mathrm{DC},2}(V_0) = I_{\mathrm{DC}}(V_0)/2 \ , \tag{4.30}$$

and Equation 4.25 simplifies to

$$I_0(V_0, \alpha_1, \alpha_2) = \sum_{n=-\infty}^{\infty} \frac{J_n^2(\alpha_1) + J_n^2(\alpha_2)}{2} I_{\mathrm{DC}}(V_0 + nV_{\mathrm{Ph}}) \ . \tag{4.31}$$

As a further simplification, the calculations involving DC are carried out for both SIS junctions with the same IV response, half of the measured DC. Alternatively, a ratio factor a could be introduced relating, for instance, $I_{\mathrm{DC},1} = aI_{\mathrm{DC}}$ and $I_{\mathrm{DC},2} = (1-a)\, I_{\mathrm{DC}}$, accounting for junction size differences.

4.2.3.2 Transmission Line Parameters Z_0, β, and l

We further assume the transmission line parameters Z_0, β, and l to be known, using the design parameters obtained from BCS theory with transmission line theory. In principle, Z_0, β, and l could be recovered alongside Z_{emb} and V_{Source} because they are all constants. However, this extension would open the parameter space to four variables from two unknowns (βl is a single parameter). In practice, Z_0, β, and l will be similar to the design values, and consequently, we use the design values for our calculations.

4.2.3.3 IF Circuit

The classical single junction mixer circuit has a transmission line from the RF side leading to the IF circuit with the SIS junction connected to the ground. The RF and IF circuits are directly connected so that they can be condensed into Z_{emb}.

The twin-junction circuit has several possibilities to connect the IF circuit. If the RF and IF circuit connect both to the first SIS junction, such as in Figure 3.2 or [99–101], the ABCD matrix in Equation 4.17 and Figure 4.11 represent the true circuit. However, in the design described in Chapter 5, the RF circuit connects to the first SIS junction, and the IF circuit connects to the second SIS junction. Consequently, the output vector is (V_2, I_{IF}) instead of $(V_2, 0)$ in Equation 4.17, which is then terminated by the IF circuit impedance $Z_{\mathrm{IF}} = V_2/I_{\mathrm{IF}}$. The voltage relation Equation 4.18 is then

$$V_1(V_0) = V_2(V_0)\cos(\beta l) + i\left[I_2(V_0, |V_2|) + \frac{V_2(V_0)}{Z_{\mathrm{IF}}}\right] Z_0 \sin(\beta l)\ , \tag{4.32}$$

and Equation 4.19 is expanded so that I_{TL2} in the device current in Equation 4.20 is

$$I_{\mathrm{D}} = I_1(V_0, |V_1|) + \left[I_2(V_0, |V_2|) + \frac{V_2(V_0)}{Z_{\mathrm{IF}}}\right]\cos(\beta l) + i\frac{V_2(V_0)\sin(\beta l)}{Z_0}\ . \tag{4.33}$$

In principle, Z_{IF} can be recovered together with Z_{emb} and V_{Source}, but again, this would add an additional parameter to be fitted. The additional terms are negligible for large Z_{IF}. In real mixer circuits, the RF circuit will feature a BPF, while the IF circuit features an LPF, maximising the power converted by the mixer. The LPF in the IF circuit will present a high impedance (neglecting distributed circuit effects), which allows for our assumption of neglecting Z_{IF}. This simplification then reduces the number of parameters to be optimised.

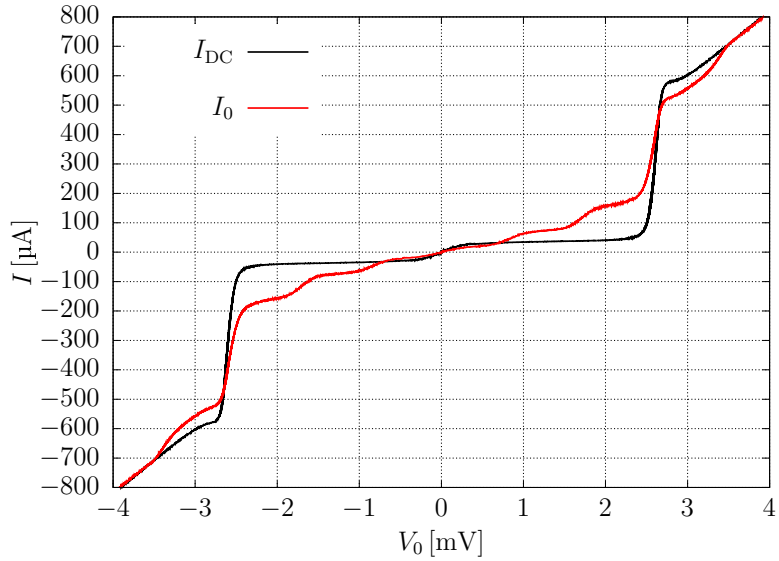


Figure 4.12: The measured I_{DC} and I_0. Both datasets are only corrected for the voltage offsets and sorted by increasing V_0.

4.2.4 Impedance Recovery Simulations

An important strength of our theoretical method is that the impedance recovery methods remain essentially the same as for a single junction, except for introducing an additional computational step to evaluate Equation 4.18. We shall, therefore, repeat the same procedure employed previously for the impedance recovery of the twin junction device. We use the IV curve shown in Figure 4.12, pumped at 214 GHz of our 240 GHz receiver, discussed later in this thesis.

4.2.4.1 Eyeball Method

The eyeball method starts with guessed Z_{emb} and V_{Source} to satisfy the circuit Equation 4.16. This calculation is an iterative process as I_D from Equation 4.20 depends on the AC voltage similar to the single-junction Eyeball method, but now with the additional step of relating V_1 and V_2. The iterations are based on V_2 guesses, which are used to compute I_2 and V_1, from which then I_1 follows so that the circuit equation can be evaluated. The resulting V_1 and V_2 are then used in Equation 4.31 to compute I_0^{Sim}, which is then compared to the measured response I_0^{Meas}.

We apply the new equation set for twin junctions to the DC data and minimise the same error surface as in the single junction case to obtain $Z_{emb} = (1.14 - i5.89)\ \Omega$ and $V_{Source} = 1.66\,\text{mV}$. Figure 4.13 shows the measured and recovered DC currents. I_0^{Sim} agrees very well with I_0^{Meas} in the voltage range of the first photon step from 1.85 mV

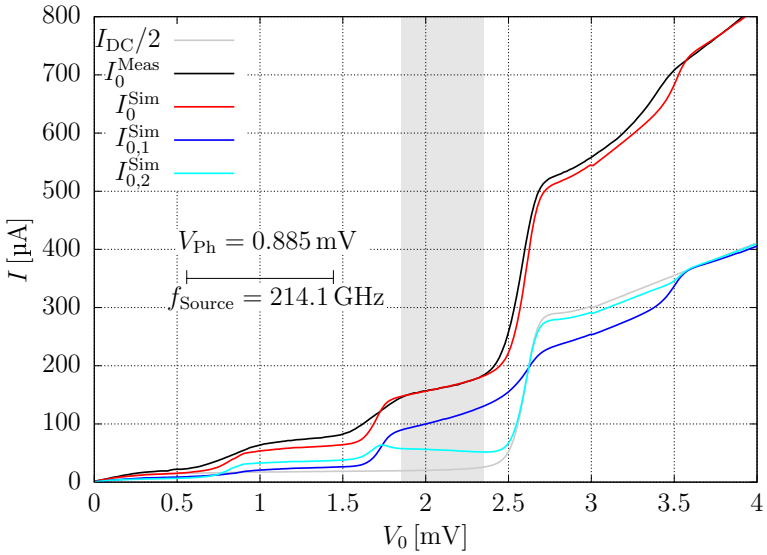


Figure 4.13: The DC recovered with the Eyeball method for $Z_{emb} = (1.14 - i5.89)\ \Omega$ and $V_{Source} = 1.66\,mV$. The fitting range from 1.85 mV to 2.35 mV is shaded grey.

to 2.35 mV. Notice that the contribution of the two junctions is very different. $I_{0,1}^{Sim}$ is very strongly pumped, especially compared with $I_0/2$.

We plot the same quantities for different Z_{emb} in Figure 4.14 at $V_{Source} = 1.66\,mV$. The slope of I_0 depends on X_{emb}, similar to the single junction case. The contributions of the individual junctions vary, and as in the shown cases, $I_{0,2}$ has negative slopes for all X_{emb}.

We use the Eyeball method to analyse the effect of changing the transmission line parameter βl in Figure 4.15a, keeping the recovered quantities constant. In the previously discussed special cases $\beta l = n\pi$, we find $I_{0,1} = I_{0,2}$ due to $\alpha_1 = \alpha_2$, as shown in Figures 4.15b and 4.15j. $I_{0,1}$ shows a steep positive photon step current slope for a rather small βl in Figures 4.15c and 4.15d, while $I_{0,2}$ has a much smaller but flat or slightly negative photon step current response. The slope of $I_{0,2}$ slightly increases while the slope of $I_{0,1}$ decreases with increasing βl in Figures 4.15e to 4.15g. At $\beta l \approx 0.8\pi$ in Figures 4.15h and 4.15i, $I_{0,1}$ and $I_{0,2}$ show a small positive photon step response. The sum of these currents I_0 has, however, still a positive photon step slope, indicating still capacitive tuning. This behaviour is not unexpected as $Z_{emb} = (1.14 - i5.89)\ \Omega$ is very capacitive, and therefore it would require a very special combination of Z_0 and βl to match this tuning.

One notices from Figure 4.15a that $I_{0,1} > I_{0,2}$ for most βl, which is again due to the tuning choices. We show the effect of changing Z_0 in Figure 4.16a in a similar manner as above, but now keeping $\beta l = 91/480\pi$. $I_{0,2} > I_{0,1}$ for small Z_0 in a highly

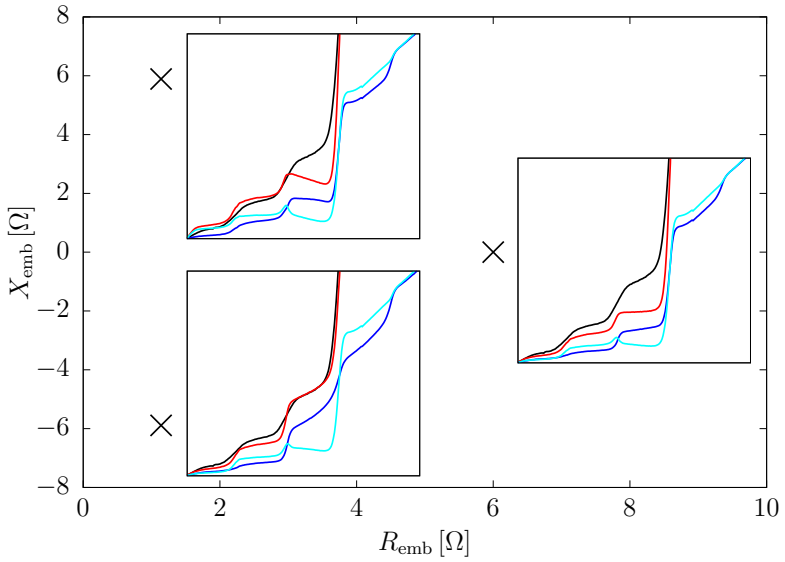


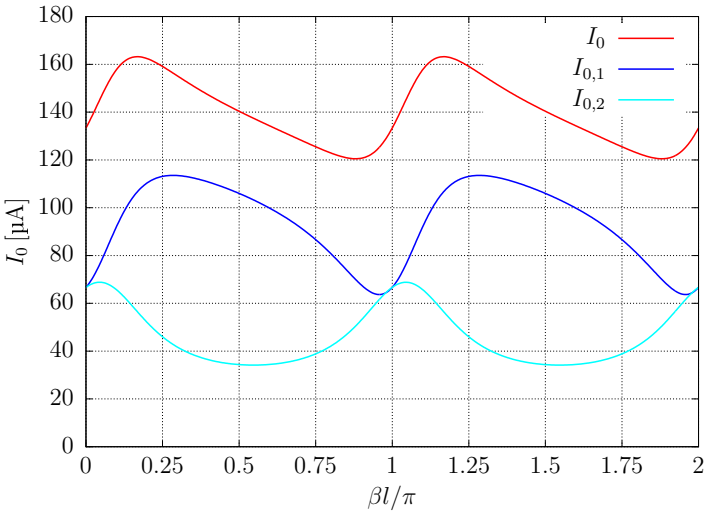
Figure 4.14: The IV responses for different values of Z_{emb} for $V_{\mathrm{Source}} = 1.66\,\mathrm{mV}$. × indicates Z_{emb} of each inset. The black line of the insets is I_0^{Meas}, and the red lines are I_0^{Sim}, with the contributions of $I_{0,1}^{\mathrm{Sim}}$ and $I_{0,2}^{\mathrm{Sim}}$ in dark and light blue, respectively. The insets have a voltage range from 0.0 mV to 4.0 mV on the x-axis and a current range from 0 µA to 400 µA on the y-axis.

capacitive tuning, as can be seen from the positive photon step current slopes in Figures 4.16b and 4.16c. $I_{0,2}$ decreases with increasing Z_0, while also the photon step current slope decreases for $Z_0 > 7.5\,\Omega$. This partially cancels the capacitance of the first junction and flattens the photon step of I_0 in Figures 4.16d to 4.16g. Altogether, this analysis shows that the magnitude of $I_{0,1}$ and $I_{0,2}$ depends on Z_0 in addition to βl. Furthermore, Figures 4.16c to 4.16e show that the crossover of $I_{0,1}$ and $I_{0,2}$ depends strongly on the choice of V_0, which needs to be considered in addition to Figure 4.16a. Despite this V_0 dependence at the $I_{0,1}$ and $I_{0,2}$ crossover, we can extrapolate from Figures 4.16a and 4.16g to confirm the special case of an open transmission line $Z_0 = \infty$, where $I_{0,1} \gg I_{0,2}$.

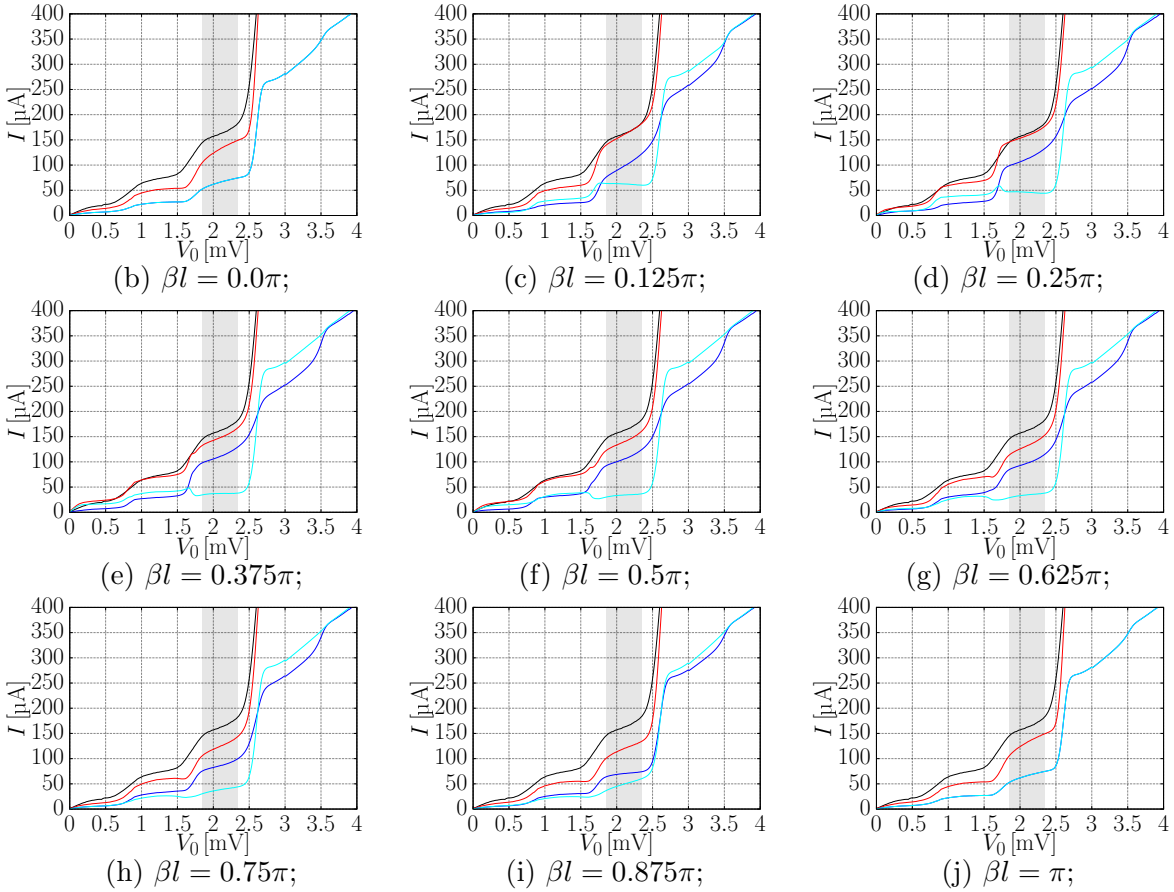
4.2.4.2 RF Voltage Match Method

Z_{emb} and V_{Source} can be determined by comparing $\alpha_{\mathrm{D}}^{\mathrm{Meas}}$ and $\alpha_{\mathrm{D}}^{\mathrm{Sim}}$ similar to the single junction. $\alpha_{\mathrm{D}}^{\mathrm{Meas}}$ follows from the DC relationship between I_0 and I_{DC} in Equation 4.31. However, now Equation 4.18 is required to relate α_2^{Meas} and $\alpha_1^{\mathrm{Meas}} = \alpha_{\mathrm{D}}^{\mathrm{Meas}}$ in this computation. $\alpha_{\mathrm{D}}^{\mathrm{Sim}}$ is computed from guessed Z_{emb} and V_{Source} values and Equations 4.16, 4.18 and 4.20, similar to the Eyeball method.

Minimising the error surface in the voltage range of the first photon step from



(a) The simulated DC at $V_0 = 2.10\,\mathrm{mV}$ for different transmission line lengths βl.

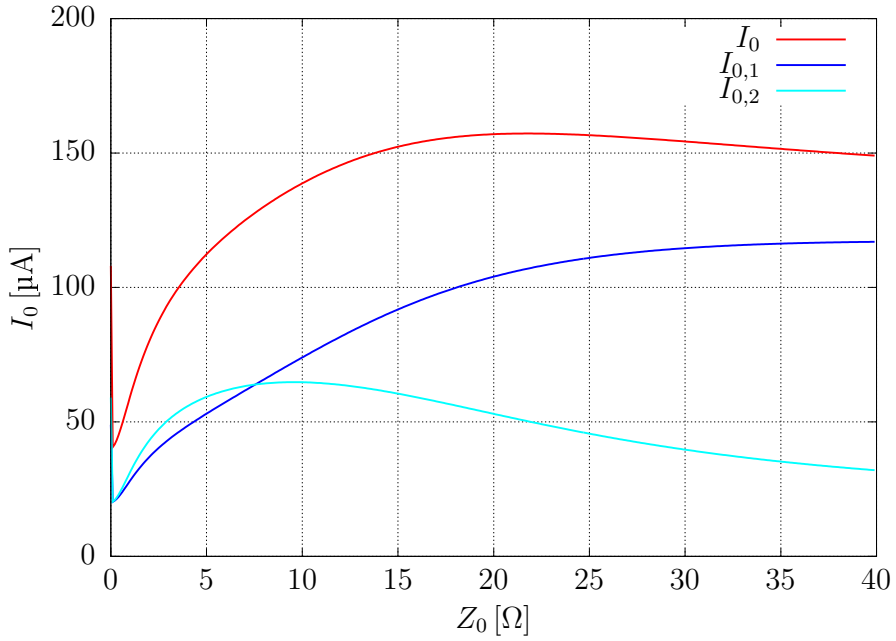


(b) $\beta l = 0.0\pi$; (c) $\beta l = 0.125\pi$; (d) $\beta l = 0.25\pi$;

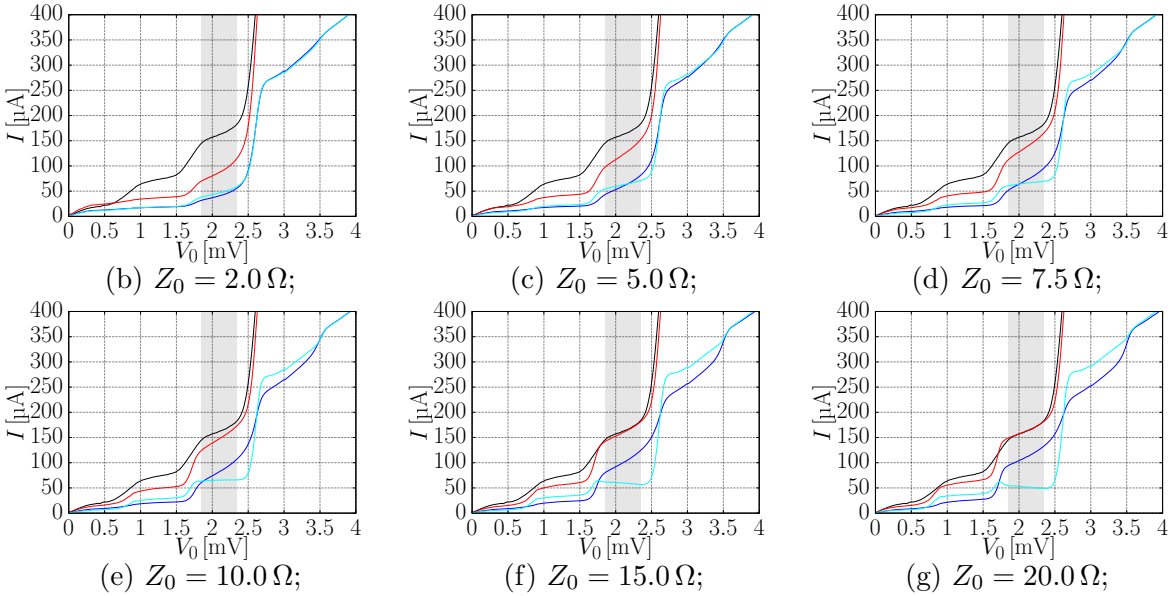
(e) $\beta l = 0.375\pi$; (f) $\beta l = 0.5\pi$; (g) $\beta l = 0.625\pi$;

(h) $\beta l = 0.75\pi$; (i) $\beta l = 0.875\pi$; (j) $\beta l = \pi$;

Figure 4.15: The behaviour of the simulated DC depending on different transmission line lengths βl at $Z_0 = 18\,\Omega$, $Z_{\mathrm{emb}} = (1.14 - i5.89)\ \Omega$ and $V_{\mathrm{Source}} = 1.66\,\mathrm{mV}$. I_0^{Meas} is shown in black, and the remaining colour code from Figure (a) applies to Figures (b) to (j).



(a) I_0 at $V_0 = 2.10\,\mathrm{mV}$ for different characteristic impedances Z_0.



(b) $Z_0 = 2.0\,\Omega$; (c) $Z_0 = 5.0\,\Omega$; (d) $Z_0 = 7.5\,\Omega$;

(e) $Z_0 = 10.0\,\Omega$; (f) $Z_0 = 15.0\,\Omega$; (g) $Z_0 = 20.0\,\Omega$;

Figure 4.16: The behaviour of the simulated DC depending on different characteristic impedances at $\beta l = 91\pi/480$, $Z_{\mathrm{emb}} = (1.14 - i5.89)\ \Omega$ and $V_{\mathrm{Source}} = 1.66\,\mathrm{mV}$. I_0^{Meas} is shown in black, and the remaining colour code from Figure (a) applies to Figures (b) to (j).

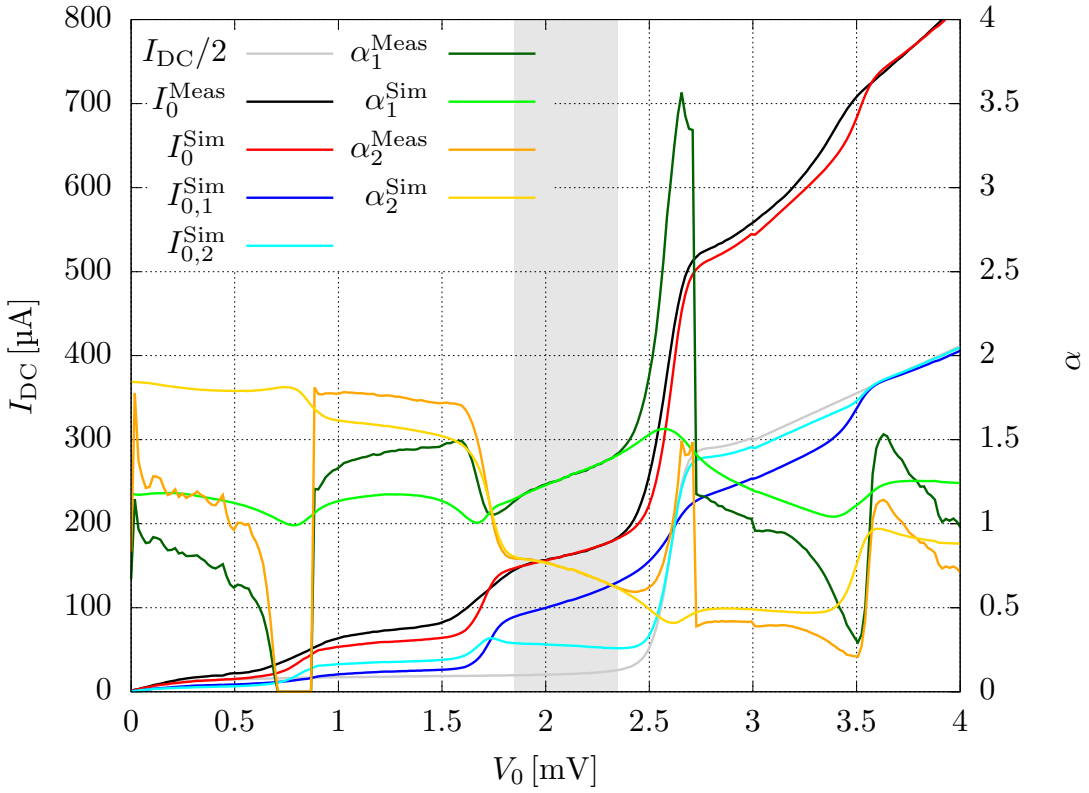


Figure 4.17: The simulated and measured DC and pumping levels used and obtained with the RF voltage match method for $Z_{emb} = (1.13 - i5.78)\ \Omega$ and $V_{Source} = 1.64\,\text{mV}$. The fitting range from 1.85 mV to 2.35 mV is shaded grey.

1.85 mV to 2.35 mV yields $Z_{emb} = (1.13 - i5.78)\ \Omega$ and $V_{Source} = 1.64\,\text{mV}$, which is very close to the values recovered with the previous method. The recovered response is compared to the measured response in Figure 4.17. α_k^{Meas} and α_k^{Sim} for the two SIS junctions $k = 1, 2$ agree well in the grey-shaded fitting interval so that I_0^{Sim} follows I_0^{Meas}. Although $I_{0,k}^{Meas}$ are not shown to prevent overcrowding Figure 4.17, it is clear that $I_{0,k}^{Meas}$ are known from α_k^{Meas}. Thus, the overall measured response I_0 is obtained in the RF voltage match method by fitting the individual responses of the k^{th} junction. The required iterative process starts again with $k = 2$ to obtain I_2, V_1 and I_2 from a guessed V_2 for the same practical reasons as in the Eyeball method.

A careful examination of α_k^{Meas} shows, however, poles in the responses, which do not appear in α_k^{Sim}. We show the error surface for the difference between I_0^{Meas} and $I_0(\alpha_2^{Meas})$ in Figure 4.18, which is used to determine α_2^{Meas}. α_2^{Meas} is uniquely defined in the voltage range of the first and second photon steps from 1 mV to 2.5 mV. However, α_2^{Meas} has two possible values outside this interval, one below and one above 1.5. We suspect that the Bessel functions in Equation 4.25 introduce the additional possibility

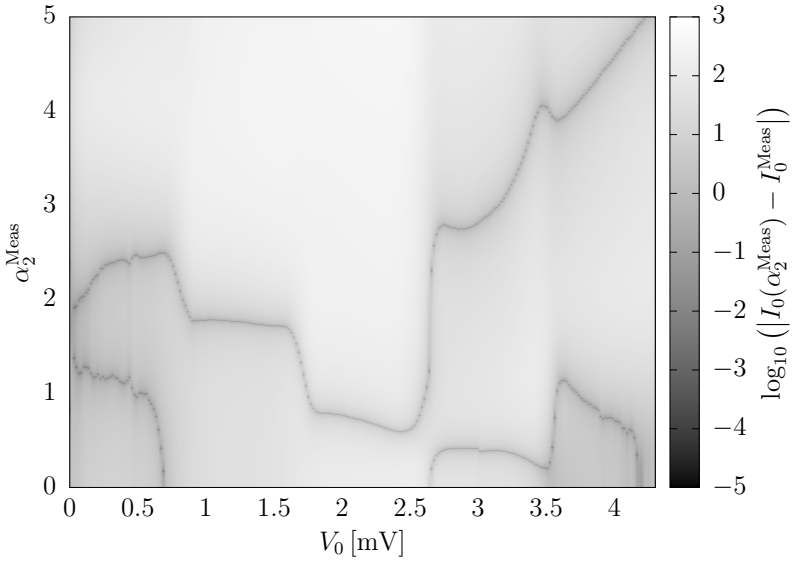


Figure 4.18: The error surface for calculating α_2 from the measured DC with Equations 4.18 and 4.25.

due to the increasing significance of higher ns at high pumping levels, as discussed in the single junction case. In particular, the discontinuities of α_2^{Meas} in Figure 4.17, and as a result of those also of α_1^{Meas}, are introduced by the initial guess $\alpha_2^{\mathrm{Meas}} = 0.8$ in the minimisation function determining α_2^{Meas}.

4.2.4.3 Voltage Divider Method

The twin-junction circuit of the Thévenin equivalent circuit in Figure 4.11a can be represented by a single device impedance Z_{D}, as shown in Figure 4.11b, that was previously a single junction device. The voltage divider representation used for the single junction impedance recovery applies to this circuit. However, now the device impedance is

$$Z_{\mathrm{D}}(V_0, \alpha_1, \alpha_2) = \frac{V_{\mathrm{D}}(V_0)}{I_{\mathrm{D}}(V_0, \alpha_{\mathrm{D}})} = \frac{V_1(V_0)}{I_1(V_0, |V_1|) + I_2(V_0, |V_2|)\cos(\beta l) + i\frac{V_2(V_0)\sin(\beta l)}{Z_0}} \,, \tag{4.34}$$

determined by the device parameters. Alternatively, the admittances of the individual junctions

$$Z_k^{-1} = Y_k = \frac{I_k(V_0, \alpha_k)}{V_k(V_0)} \tag{4.35}$$

can be applied similarly to the analysis in the preceding chapter to determine the device impedance

$$Z_{\mathrm{D}}^{-1} = Y_{\mathrm{D}} = Y_1 + Y_0 \frac{Y_2 + iY_0 \tan(\beta l)}{Y_0 + iY_2 \tan(\beta l)} \,. \tag{4.36}$$

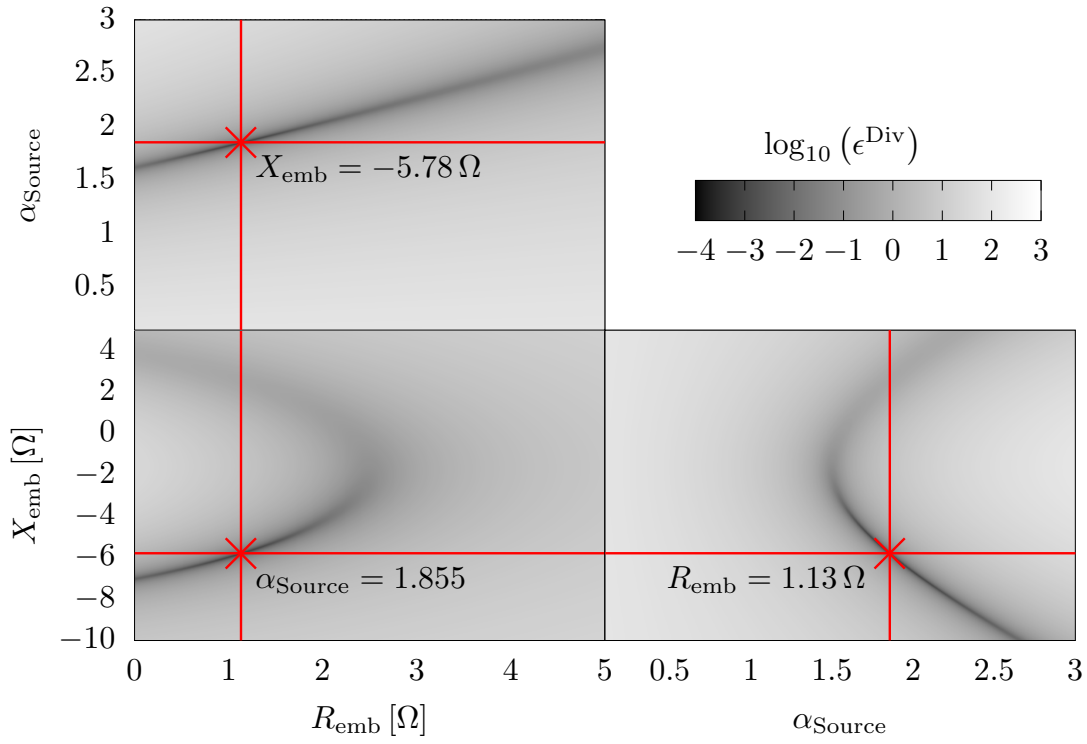
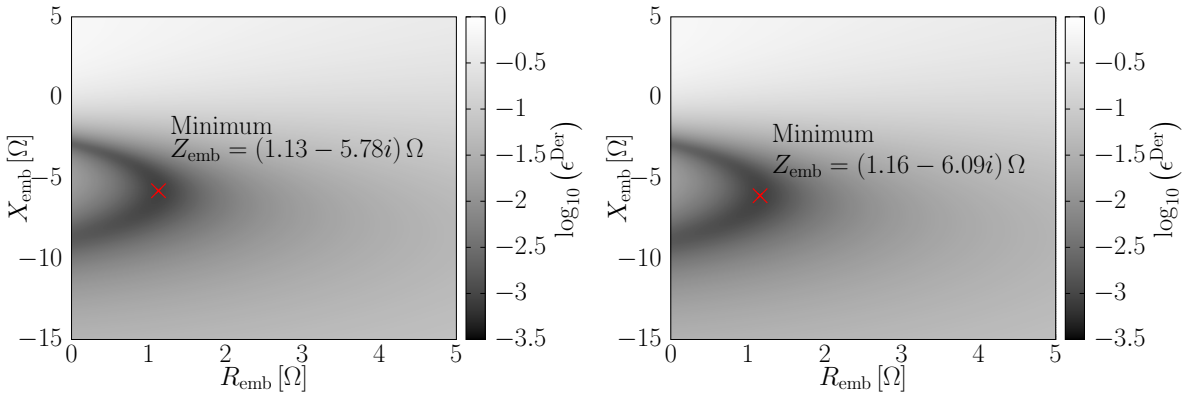


Figure 4.19: The error surfaces of the voltage divider method.

Z_{D} can be computed with V_1^{Meas} and V_2^{Meas} that are determined as in the RF voltage match method from Equations 4.31 and 4.18 from a guessed V_2. Then, the voltage divider can be evaluated for different Z_{emb} and V_{Source} without solving any further implicit relations.

We recover $Z_{\text{emb}} = (1.13 - i5.78)\ \Omega$ and $V_{\text{Source}} = 1.64\,\text{mV}$ with the Z_{D} definition in Equation 4.34 using V_{D} and I_{D} and the same result with the Z_{D} definition in Equation 4.36 using the impedances of the individual junctions. Indeed, the error surfaces around the respective optimum in Figure 4.19 are identical for the two methods. Although this conclusion sounds trivial, as Equations 4.34 and 4.36 describe the same circuit, we still can confirm that the introduction of the $e^{i\phi_k}$ term in Equation 4.21 is necessary: While Equation 4.34 can only be correctly calculated if accounting for the phase factor ϕ_k of V_k, Equations 4.35 and 4.36 can be computed with $V_k = \alpha_k$ if I_k in Equation 4.21 is calculated with $e^{i\phi_k} = 1$. We conclude, therefore, that the $e^{i\phi_k}$ term in Equation 4.21 has been correctly introduced because two different methods return the same results.



(a) $Z_{\text{D}}(V_0, \alpha_1, \alpha_2) = \frac{V_{\text{D}}(V_0)}{I_{\text{D}}(V_0, \alpha_{\text{D}})}$; (b) $Z_{\text{D}}^{-1} = Y_{\text{D}} = Y_1 + Y_0 \frac{Y_2 + iY_0 \tan(\beta l)}{Y_0 + iY_2 \tan(\beta l)}$;

Figure 4.20: The error surface of the voltage divider derivative method computed from different definitions of Z_{D}.

4.2.4.4 Voltage Divider Derivative Method

The voltage divider derivative method remains unchanged because Z_{D} is treated as constant, not affected by the elimination of V_{Source} in the voltage divider equation. Again, both methods of calculating Z_{D} introduced with the voltage divider method above are applicable to this method.

We recover $Z_{\text{emb}} = (1.13 - i5.78)\ \Omega$ and $V_{\text{Source}} = 1.64\,\text{mV}$ in Figure 4.20a with the Z_{D} definition in Equation 4.34 using V_{D} and I_{D}, and $Z_{\text{emb}} = (1.16 - i6.09)\ \Omega$ and $V_{\text{Source}} = 1.69\,\text{mV}$ in Figure 4.20b with the Z_{D} definition in Equation 4.36 using the impedances of the individual junctions. The difference between the two results shows that the two ways of calculating Z_{D} are different, although these might be only rounding issues. These small differences change the determined minima in Figure 4.20, especially since the minima valleys are distributed over a large R_{emb} and X_{emb} space. These minima valleys look for both methods of calculating Z_{D} identically, comparing Figures 4.20a and 4.20b.

4.2.4.5 IF Circuit Inclusion

The methods above have been presented with several simplifications and assumptions described in Section 4.2.3. One assumption is to exclude the effect of the IF circuit attached to the second SIS junction, and we would like to relax this assumption.

The receiver presented above has $A = 3\,\mu\text{m}^2$ SIS junctions with $C = 75\,\text{fF}/\mu\text{m}^2$ and an LPF attached to the second SIS junction. From simulations described in more detail in Chapters 5 and 7, we expect an input impedance of $Z_{\text{LPF}} = (0.13 + i30.54)\ \Omega$

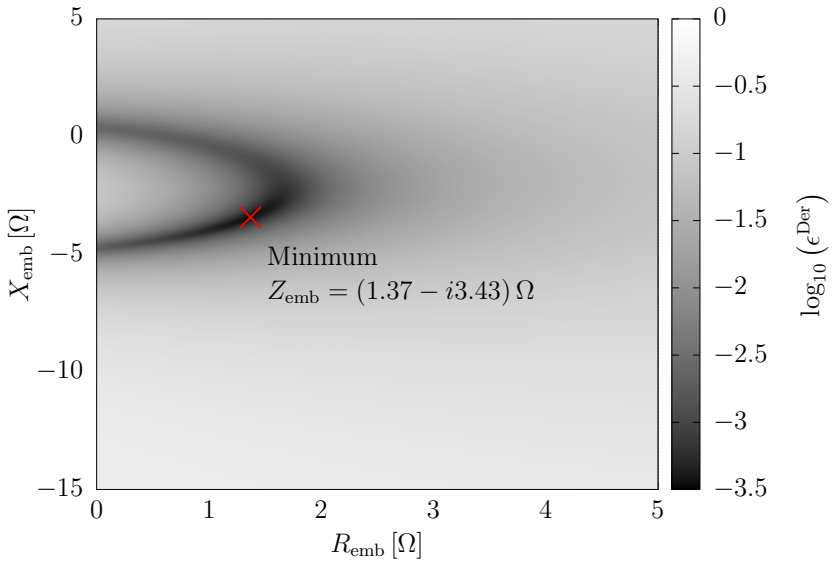


Figure 4.21: The error surface of the voltage divider derivative method accounting for the IF circuit impedance $Z_{\mathrm{IF}} = (0.0018 - i3.7074)$.

into this LPF. This, together with the junction capacitance, gives

$$Z_{\mathrm{IF}} = \left(\frac{1}{Z_{\mathrm{LPF}}} + i2\pi f C A\right)^{-1} = (0.0018 - i3.7074)\ \Omega \tag{4.37}$$

at frequency $f = 214.1\,\mathrm{GHz}$. We use this impedance in Equations 4.32 and 4.33 in the voltage divider derivative method to achieve the error surface shown in Figure 4.21. The result for Z_{emb} differs from the result without including the IF circuit: R_{emb} is larger, and X_{emb} is significantly smaller. One also notices that the minima valley in the plot is shifted to coincide with $Z_{\mathrm{emb}} = (0 + i0)\ \Omega$.

Figure 4.22 shows a very good agreement between measured and recovered pumped IV curves I_0^{Meas} and I_0^{Sim}. The good agreement extends to lower voltages than the first photon step, which is not the case when neglecting Z_{IF}, as done in the previous simplification. Moreover, the pumping levels α agree much better when accounting for Z_{IF}, as a comparison of Figures 4.22 and 4.17 shows. Again, the effects below 1 mV discussed with Figure 4.18 appear in the measured pumping levels α_1^{Meas} and α_2^{Meas}.

From our simulations in Chapter 7, we expect to recover an embedding impedance of $(1.75 - i2.76)\,\Omega$ with a $3\,\mu\mathrm{m}^2$ first SIS junction. The recovered embedding impedance with the inclusion of the effect of the IF circuit is much closer to this expected value than the result obtained without accounting for Z_{IF}. We interpret the good agreement between the data in Figure 4.22 and the simulations in Chapter 7 as an indication that the inclusion of Z_{IF} is important to recover Z_{emb} correctly.

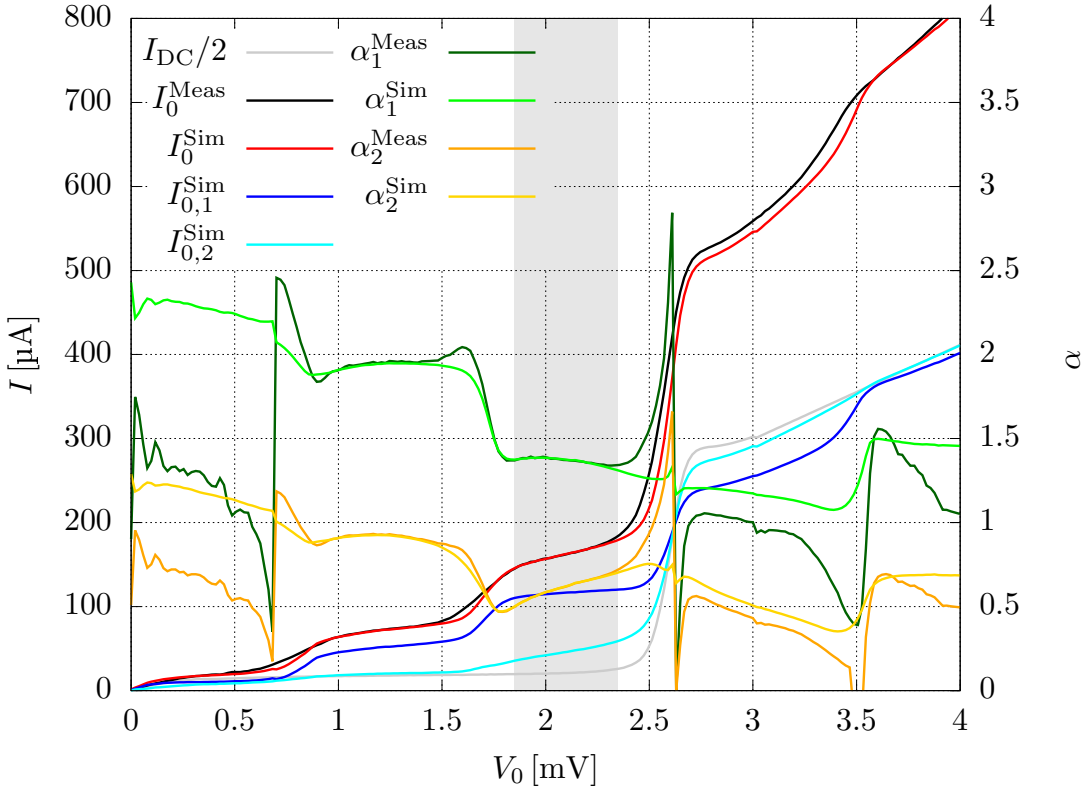


Figure 4.22: The simulated and measured DC and pumping levels used and obtained with an IF circuit impedance $Z_{\mathrm{IF}} = (0.0018 - i3.7074)$ for $Z_{\mathrm{emb}} = (1.37 - i3.43)\ \Omega$ and $V_{\mathrm{Source}} = 1.33\,\mathrm{mV}$.

4.2.4.6 Application on a THz Receiver

We also recorded the data for a THz receiver and performed the impedance recovery on this device to show the capabilities of this method. The twin-junction mixer is shown in Figure 3.2, where the two 0.5 µm^2 Nb/AlN/NbN SIS junctions are connected with a 6.5 µm long, 4.5 µm wide microstrip [86]. The microstrip is formed from a 300 nm thick NbTiN ground plane, a 250 nm SiO_2 dielectric and a 500 nm thick Al strip. We estimate the characteristic impedance for the transmission line between the SIS junctions to be 9.2 Ω and an electrical length of 13° at 840 GHz. The SIS junction capacitance is 80 fF/µm^2.

The Nb/AlN/NbN hybrid junctions are expected to have a Cooper pair binding energy $\Delta_{\mathrm{Nb}} + \Delta_{\mathrm{NbN}} = 3.3\,\mathrm{meV}$, which is slightly lower due to fabrication [86]. The measured gap voltage $V_{\mathrm{g}} = 3.2\,\mathrm{mV}$ implies that the SIS junction is operated above the gap voltage equivalent frequency of $\approx 780\,\mathrm{GHz}$. Hence, an Al strip is used to connect the SIS junction. Another effect at these frequencies is that the LO power heats the SIS tunnel junction and consequently reduces V_{g} when illuminating the SIS junction. This LO power heating has practical implications for the embedding impedance recovery. To allow for comparison and circumvent issues due to LO heating, a topic beyond the scope of this thesis, we use in the following existing 840 GHz data, the same data as in [102]. I_{DC} is recorded at 4.99 K and, therefore, at a higher temperature than I_0, which is heated by the 840 GHz LO power. Consequently, $V_{\mathrm{g}} = 2.9\,\mathrm{mV}$ in both dataset, matching I_{DC} and I_0.

We applied our twin-junction impedance recovery method with an IF circuit impedance of $Z_{\mathrm{IF}} = (0.0001 - i4.7368)\ \Omega$, accounting for the geometric capacitance of the second SIS junction and assuming negligible contributions from the RF choke structure in the ground layer. Figure 4.23 shows good agreement between measured and recovered currents within the fitting range. At lower voltages $V_0 < 1.0\,\mathrm{mV}$, we find some disagreement between the measured and simulated currents, where our simulated current drops quickly at $V_0 \approx 0.6\,\mathrm{mV}$. The reasoning remains under investigation, but a similar behaviour can be found in the classical single-junction impedance recovery in the LO heating publication [102].

We recover $Z_{\mathrm{emb}} = (0.36 + i0.30)\ \Omega$ and $\alpha_{\mathrm{LO}} = 0.399$, and subtracting the capacitance of the first SIS junction yields $(0.37 + i0.35)\ \Omega$ for the circuit feeding the twin junction. A comparison with simulations of the initial design is not possible because some dimensions on the rectangular waveguide and the planar antenna are missing. We, however, compare this result with the result obtained with our single junction impedance recovery. This is especially interesting since $\beta l = 13°$ at 840 GHz and,

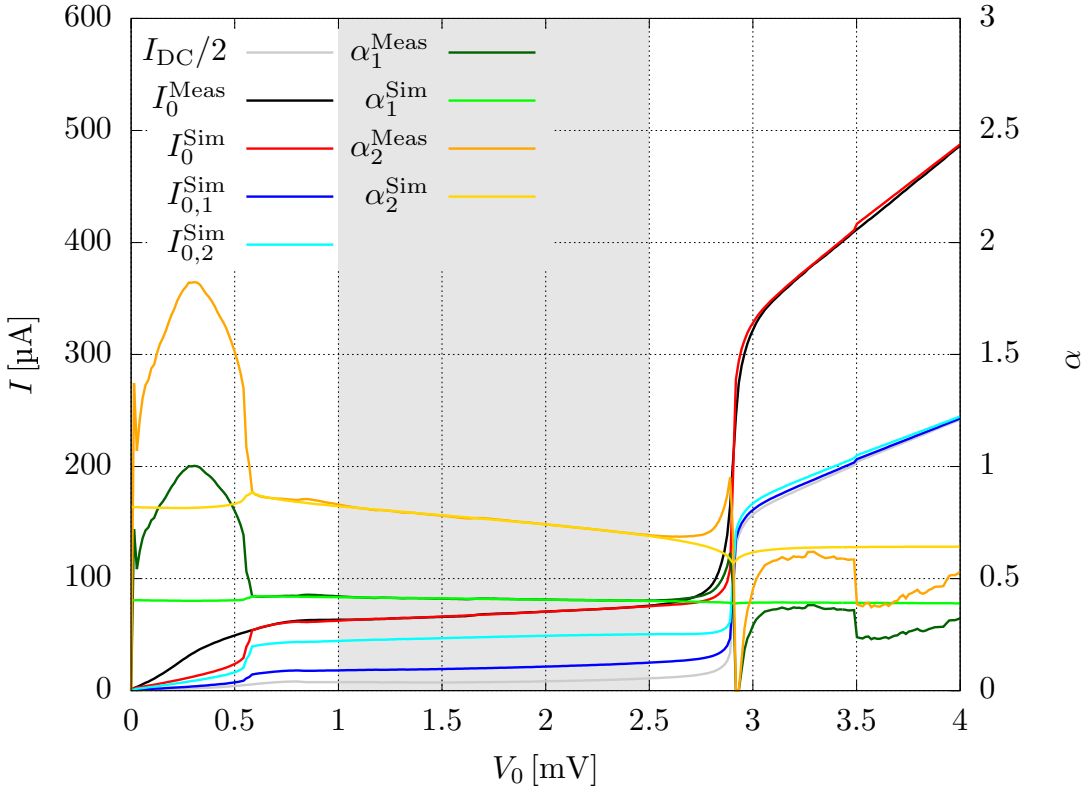
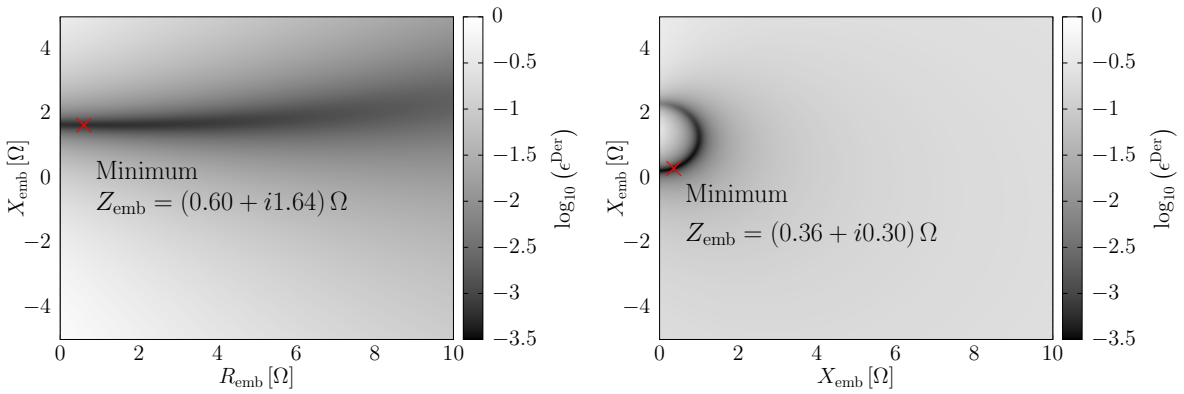


Figure 4.23: The simulated and measured DC and pumping levels used and obtained with an IF circuit impedance $Z_{IF} = (0.0001 - i4.7368)$ of the THz mixer at 840 GHz for $Z_{emb} = (0.36 + i0.30)\ \Omega$ and $V_{Source} = 1.39\,\text{mV}$.



(a) Single Junction Impedance Recovery; (b) Twin Junction Impedance Recovery;

Figure 4.24: A comparison of the error surfaces of the single and twin junction method on 840 GHz data.

therefore, a value close to the single junction special case $\cos(\beta l) \approx 1$. The recovered pumped current is indistinguishable from the pumped current recovered with the twin junction impedance recovery method. However, the single junction impedance recovery yields $Z_{\mathrm{emb}} = (0.60 + i1.64)\ \Omega$ and $\alpha_{\mathrm{LO}} = 0.620$. Even after accounting for the geometric capacitance of the SIS junction, the Z_{emb} obtained with the single junction method is significantly more inductive than the value obtained with our twin junction. Furthermore, we find that the error surfaces between the single junction and twin junction impedance recovery differ significantly, as shown in Figure 4.24.

4.2.5 Conclusion

We have reviewed the established embedding impedance recovery, including four established recovery methods. In the second section, we applied this method for the first time to perform embedding impedance recoveries on twin junction mixer circuits. Therefore, we first introduced the new circuit equation, the link between the voltages at the two SIS junctions and minor changes to the established equation set. This general equation set is then used to describe special cases before introducing simplifications and reasonable assumptions. We introduce the four recovery methods with the twin junction equations using the same structure as in the single junction section. We refer to special cases and use different approaches yielding the same results to verify our twin junction recovery method whenever appropriate. An important conclusion is that even for identical junctions, the pumping of the two SIS junctions is different. The recovered information is important to understand discrepancies between receiver designs and the fabricated samples in the experiment.

Chapter 5

Single-Pixel On-Chip Dual-Polarization Receiver Design

Chapter published: J. Wenninger, F. Boussaha, C. Chaumont, B. K. Tan, and G. Yassin, "Design of a 240 GHz On-Chip Dual-Polarization Receiver for SIS Mixer Arrays," *Superconductor Science and Technology*, 2023.

In this chapter, we present the design of an on-chip dual-polarisation receiver centred at 240 GHz with 100 GHz RF bandwidth, covering the wideband Submillimeter Array (wSMA) low band [58]. This chapter first gives an overview of the receiver design. We then describe the individual on-chip circuit elements used to form the full chip and follow that with the performance estimation of the full receiver chip assembled from these circuit elements.

5.1 Receiver Overview

The receiver, shown as a schematic in Figure 5.1, has the entire RF signal processing circuit fabricated on the chip shown in Figure 5.2. A feedhorn and a circular waveguide couple the LO signal and the two free-space RF polarisations, Pol. 1 and Pol. 2, to the on-chip OMT, which separates the two orthogonal polarisations with two sets of opposing probes. The two signals from each pair of opposing probes are recombined with 90° hybrids. This routing inevitably leads to the crossover of two transmission lines, which must be carefully designed considering the potential crosstalk between the polarisations. The signals of each polarisation recombine at the Σ port of the

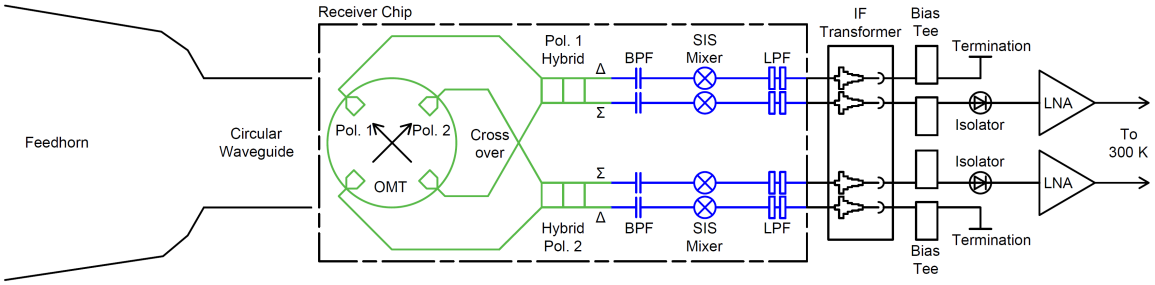


Figure 5.1: The schematic of the dual-polarisation SIS receiver. Components fabricated on the receiver chip are shown within the dashed rectangle, with the polarised signal coupling network coloured in green and the mixers circuits in blue. The two RF polarisations are incident at the feedhorn on the left of the schematic. The circuit and connections for the downconverted IF signals are on the right side of the schematic.

hybrid, leaving the Δ port isolated. Nonetheless, both ports are connected to two identical mixer circuits, which comprise a BPF, an SIS mixer, and an LPF.

The IF output signal of the receiver chip is wire-bonded to an IF transformer, which matches the impedance of the IF circuit to $50\,\Omega$ and accommodates the connectors towards the bottom of the pixel. The following bias tees inject the DC bias for the mixer operation and connect to either a termination or room temperature electronics via an isolator and an LNA depending on the preceding hybrid port, Δ or Σ, respectively, as shown in Figure 5.1.

5.2 Design of the Individual Circuit Elements

All the individual circuit elements on-chip were designed with Ansys HFSS for an established chip topology and fabrication process presented in Appendix A.4. HFSS is a commercial finite-element method (FEM) software to solve Maxwell's equations in an arbitrary-defined 3D simulation space and is described in detail in Appendix A.2. In the following sections, we describe the design of each circuit component following the RF signal path of the receiver chip shown in Figure 5.1.

5.2.1 Orthomode Transducer (OMT)

We use a planar OMT to couple the RF and LO signals into microstrips on the receiver chip while separating the two polarisations, similar to bolometric detectors of cosmic microwave background experiments [103–108]. For this setup, the free-space signals couple via a feedhorn into two perpendicular TE_{11} modes in the $\varnothing 1.0\,\mathrm{mm}$ circular waveguide. These two modes are then guided onto the planar circuit with

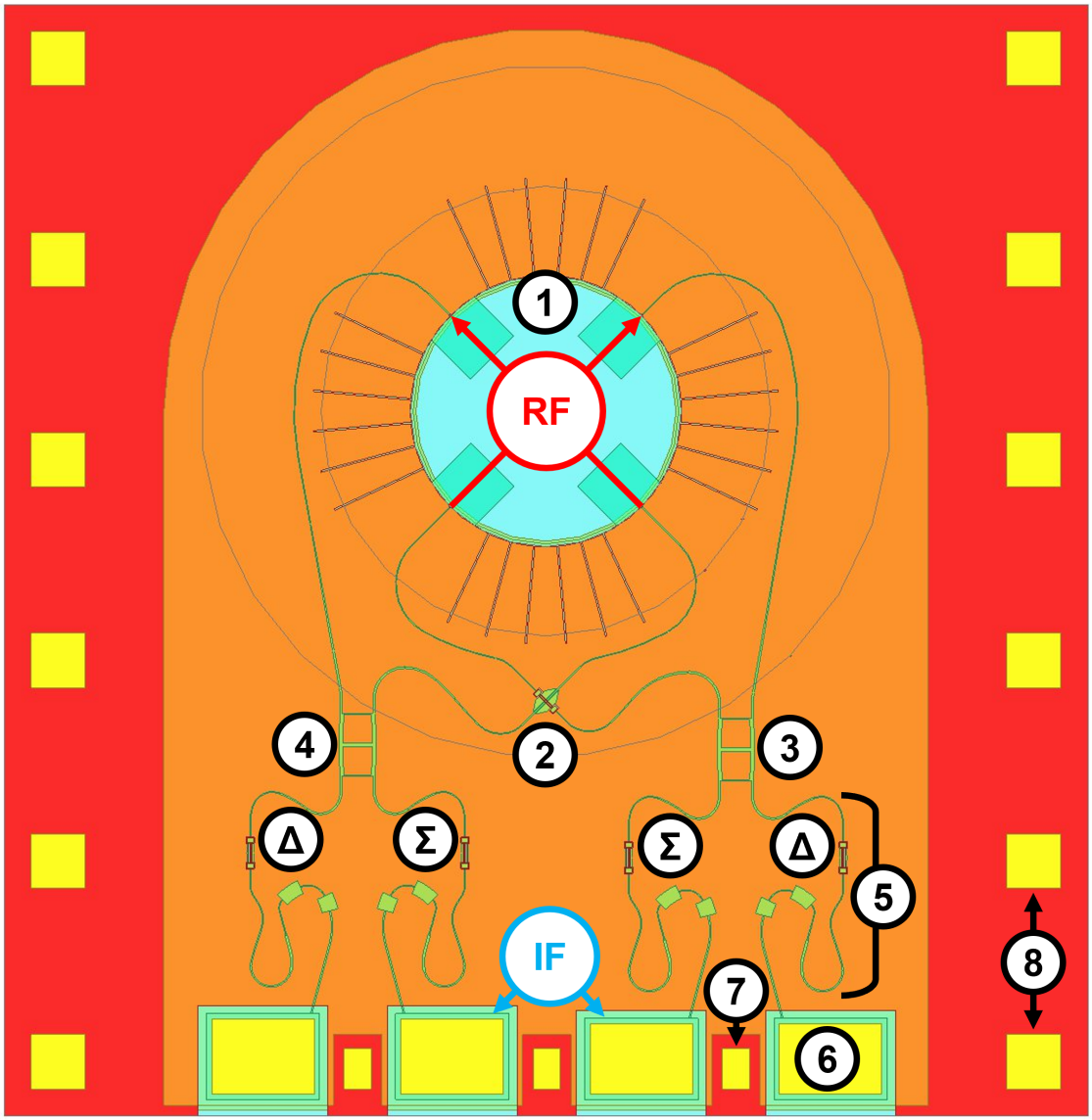


Figure 5.2: The actual layout of the dual-polarisation receiver chip, 4.0 mm horizontally by 4.1 mm vertically in size. The polarised signal coupling network couples both RF polarisations on-chip with the OMT (1) and connects them via the crossover (2) to the hybrids for Pol. 1 (3) and Pol. 2 (4). All hybrid outputs, the Σ port with the superimposed signal of a polarisation and the Δ port, which is ideally isolated, connect to identical mixer circuits (5) comprising the BPF, the SIS mixer and the LPF. The outputs of the mixer circuits lead to bonding pads, approximately 400 µm by 300 µm in size (6), for the IF signal connection. Between these bonding pads leading to the individual mixer circuits are 100 µm by 150 µm ground bonding pads (7), and further 200 µm by 200 µm ground bonding pads are along the sides of the chip (8).

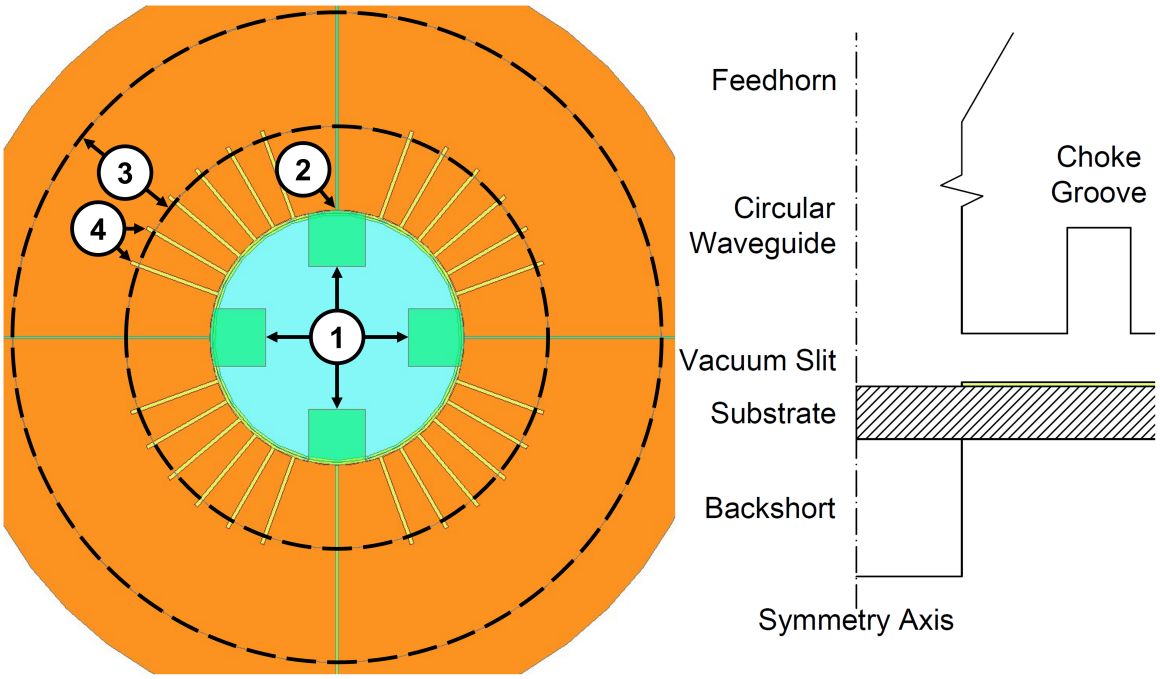


Figure 5.3: The top view of the OMT on the left and the not-to-scale side view on the right. The OMT probes (1) transform into microstrips at the radius of the circular waveguide (2). The radii defining the choke groove are indicated by (3), and (4) shows the serrations in the ground-plane layer. The width of the microstrips and the serrations are widened for clarity.

two sets of opposing probes forming the OMT shown in Figure 5.3. We employ a probe set per polarisation so that each probe receives half of the incident signal power of one polarisation with 180° phase difference between the opposing probes due to the symmetry of the TE_{11} field distribution.

The OMT probes are designed to couple maximum power from the circular waveguide with an impedance of a couple of hundred ohms to the 19 Ω microstrips. The backshort extension of the circular waveguide further enhances the coupling into the probes and, thus, the microstrips.

The presence of the quartz substrate causes reflections of the signal at the interfaces and induces unwanted losses. Although thinning the substrate to 50 µm (which is the practical limit considering the brittleness of quartz) mitigates these effects, the losses are still noticeable. These losses could potentially be minimised using silicon-on-insulator (SoI) technology, but this is still under development in our fabrication facilities.

In addition to losses through the substrate, losses also occur in the vacuum slit above the substrate. The slit needs to exceed a minimum height to avoid interference

with the on-chip circuit and to accommodate fabrication tolerances, such as the substrate thickness and the machining of the block housing the receiver chip. Balancing the OMT performance with the losses and the uncertainties in the fabrication results in a 50 µm slit.

The losses through this slit are reduced by a quarter-wavelength deep choke groove, machined concentrically at a quarter-wavelength distance from the circular waveguide. This causes the electromagnetic wave in the circular waveguide to encounter an electric short, which prevents a significant fraction of signal power from leaking into the vacuum slit.

Both of the losses discussed above propagate as independent parallel-plate waveguide TEM modes in the substrate and the vacuum slit since these two volumes are separated by the ground-plane layer of the microstrip. The choke groove forms a vacuum-filled parallel-plate ring between the circular waveguide and the choke groove. This ring resonates when an integer number of wavelengths fit into the ring circumference, preventing those signals from coupling into the OMT probes. Adjusting the radius of the circular waveguide and the choke groove changes the ring circumference and therefore offers a method of shifting the resonance to frequencies outside the receiver bandwidth. However, as the resonance is shifted away from the operation band, another order resonance will shift towards the operation band from the other frequency end. Thus, this solution of varying waveguide and groove radii only suppresses the resonance up to a certain fractional bandwidth. The wSMA specifications of 42% fractional bandwidth exceed this fractional bandwidth.

To circumvent this problem, Mauskopf et al. [109] increased the circumference length of the parallel-plate ring by cutting radial slots between the circular waveguide and the choke groove at a 45° angle to the OMT probes, removing the resonance from the frequency band. However, this solution complicates the machining process of the block. We, therefore, disturb the parallel-plate waveguide with radial serrations in the ground-plane layer, shifting the resonance to a frequency outside the band. With this method, we successfully limit the losses through the vacuum slit with a choke groove and suppress the emerging resonances by serrating the ground-plane layer. The achieved fractional bandwidth of 50% exceeds the requirement and allows operating the OMT with optimal coupling throughout the frequency band.

Figure 5.4 shows the simulated response of the OMT. The coupling to the individual probes is essentially identical, leading to a uniform coupling for both polarisations on the chip. This is crucial in order to avoid receiver biases towards one polarisation. In addition, the cross-coupling generated by the OMT is less than −30 dB. The return

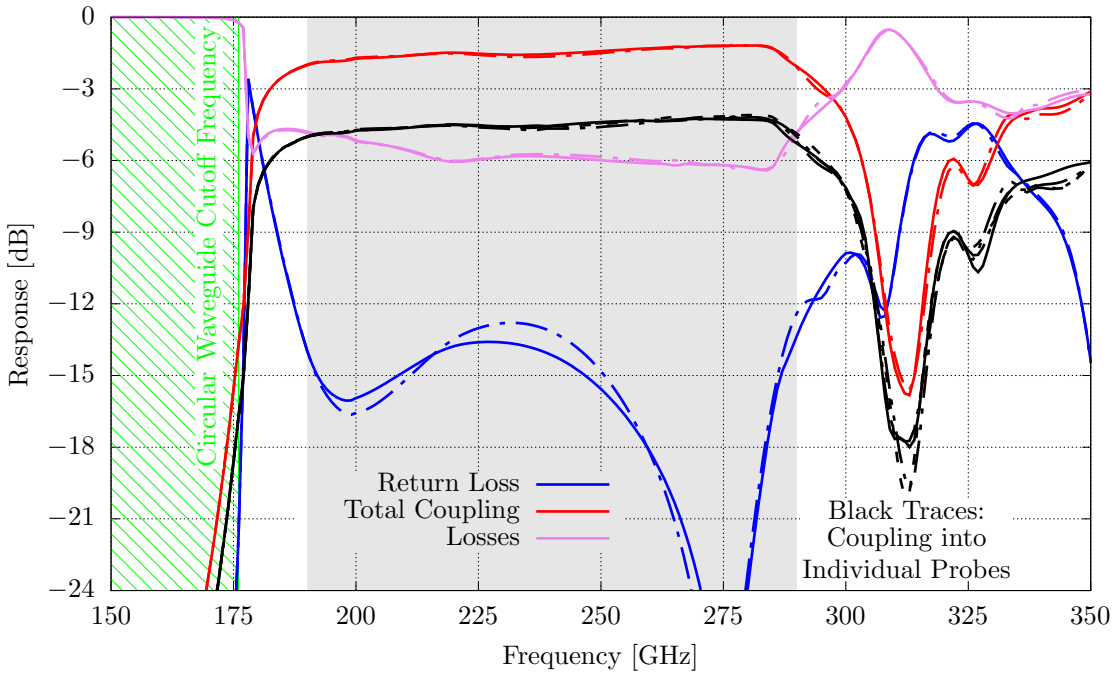


Figure 5.4: The simulated OMT performance with Pol. 1 responses as solid lines and Pol. 2 as dash-dotted lines. Total Coupling denotes the sum over a probe set, and Losses encapsulate the difference between the input and output power measured on all ports.

loss is reasonable at less than −10 dB, and the total coupling of each polarisation into the designated microstrip pair is better than −2 dB in the fitting range from 190 GHz to 290 GHz, shaded gray in Figure 5.4. This not-optimal coupling is a consequence of the unavoidable −6 dB loss due to the relatively thick substrate, which can be improved with SoI technology in the near future.

5.2.2 Crossover

Routing the full signal power of each polarisation from the OMT to the hybrids inevitably leads to a crossing of two transmission lines carrying different polarisations due to the OMT geometry, which couples the polarisations into the microstrips connected to opposing probes. Therefore, the crossover must be designed to minimise crosstalk between the two crossing transmission lines.

Our planar broadside coupler solution, shown as an inset in Figure 5.5, is largely similar to the design reported in [107, 110] but now at a much higher centre frequency and with lower characteristic impedances. The microstrips are transformed into two coplanar waveguide (CPW) structures in the two conductor layers of the microstrip,

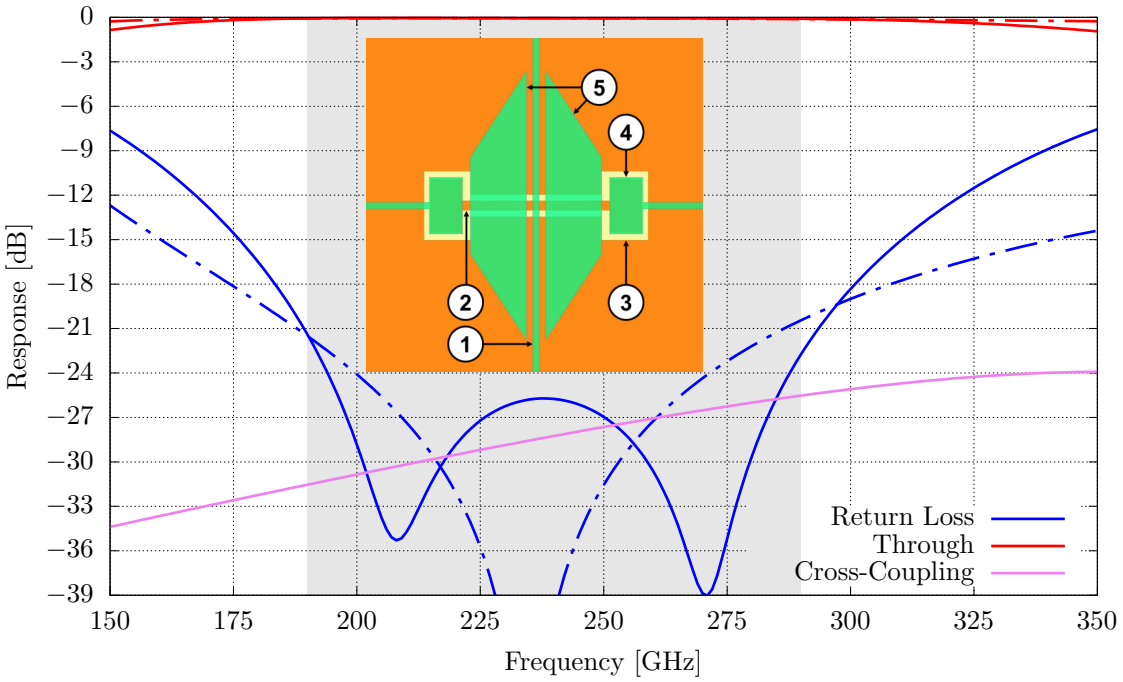


Figure 5.5: The simulated performance and layout of the crossover. The vertical CPW (1) is routed in the wiring layer, while the horizontal CPW (2) is routed within a gap in the ground-plane layer (3), which connects to the feeding microstrip with a set of broadside couplers (4). Brackets (5) form the quasi-ground of the wiring-layer CPW, whose response is shown with dash-dotted lines, and solid lines show the ground-plane layer CPW response.

namely the wiring layer and the ground-plane layer, as shown in Figure 5.6. In the wiring layer, the CPW is formed from two conductor patches bracketing the 3 µm wide microstrip feed with 3 µm wide gaps over a length of 125 µm, and the ground-plane layer has an opening to deposit the 4.4 µm wide centre strip between the 3 µm wide gaps of the 69 µm long ground-plane CPW. This CPW is capacitively connected to the feeding microstrip via two 25 µm by 15 µm broadside coupler sets. These DC-isolated conductor rectangles in the ground-plane layer and the wiring layer allow for a closed dielectric layer throughout the chip and comply with our 5-step fabrication process. In addition to carefully selecting the broadside coupler dimensions, the performance is enhanced by providing an additional load to the broadside couplers in the wiring layer with the patches bracketing the wiring-layer CPW.

The central conductors for the CPWs overlap less than 15 µm^2, leading to the excellent cross-coupling isolation shown in Figure 5.5, which does not exceed –25 dB. The broad bandwidth design with return losses well below –20 dB was obtained by carefully selecting the planar circuit dimensions. The return loss poles at 270 GHz

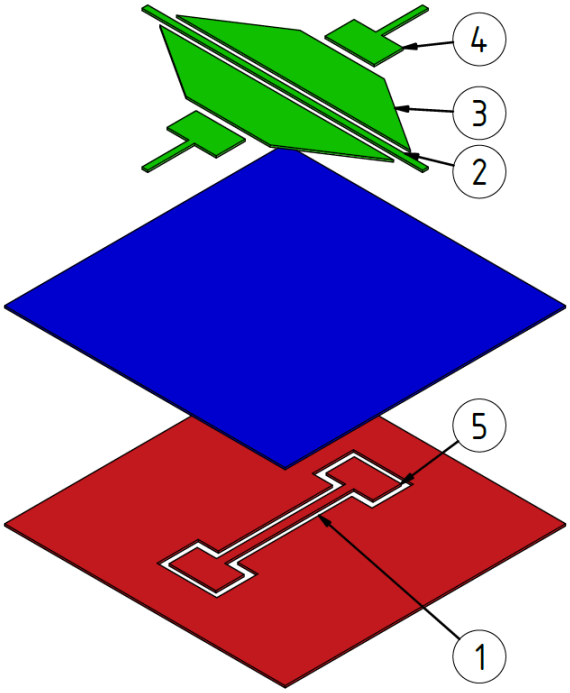


Figure 5.6: An explosion view of the microstrip layers at the crossover. The ground plane is shown in red, the dielectric layer in blue and the wiring layer in green. Pol. 1 is routed in a CPW in the ground plane (1) underneath the Pol. 2 microstrip (2), which is bracketed to form a CPW in the wiring layer with two conductor patches (3). The Pol. 1 signal is connected via broadside couplers in the wiring layer (4) and the ground plane (5).

and 240 GHz originate from the CPW lengths of approximately a quarter-wavelength at the respective frequencies, and the pole at 210 GHz originates from the broadside couplers. This low cross-coupling and return loss yield a high transmission using this compact and easy-to-fabricate crossover design for routing the OMT outputs to the hybrids for recombination.

5.2.3 Hybrid

Once the two microstrips from an OMT probe set are routed to the same chip location, a circuit element is required to recombine those to feed the mixer with the maximum power available. We abstained from employing a 3-port circuit solution due to the difficulty of implementing power-dissipating circuit elements with our superconducting thin-film deposition process and fundamental impedance mismatches arising from non-dissipative 3-port circuits. Instead, we used the two-section 90° branch-line hybrid shown in Figure 5.7 to recombine the signal since all four ports of this reciprocal circuit can be matched simultaneously [26, 111, 112].

The hybrid branches are approximately quarter-wavelength long microstrips with carefully selected characteristic impedances, with the narrowest 19 Ω microstrips connecting adjacent ports, 5 Ω microstrips leading from the ports to the centre and a 6 Ω microstrip in the centre between the two hybrid sections. The branches are arranged symmetrically in two squares, where the additional section widens the frequency bandwidth, as shown in Figure 5.7.

An input signal at the Σ port couples at −3 dB to the Through and Coupled port with a 90° phase difference while leaving the Δ port isolated over the 42% fractional bandwidth. The coupling to the isolated port and the return loss remain well below –15 dB, and the hybrid design has similarly negligible ±2° phase difference variations. As the branch-line hybrid is reciprocal, two identical signals with 90° phase difference applied at the Through and Coupled port consequently superimpose on the Σ port constructively while superimposing deconstructively on the Δ port. Hence, the hybrid is suitable for recombining the signals splitting between an OMT probe set.

5.2.4 Bandpass Filter (BPF)

Each hybrid output connects to the SIS mixer via a BPF, preventing IF signals from leaking into the RF circuit while maximising the IF power output. Furthermore, the BPF isolates the DC bias of the individual SIS mixers while passing the RF signal

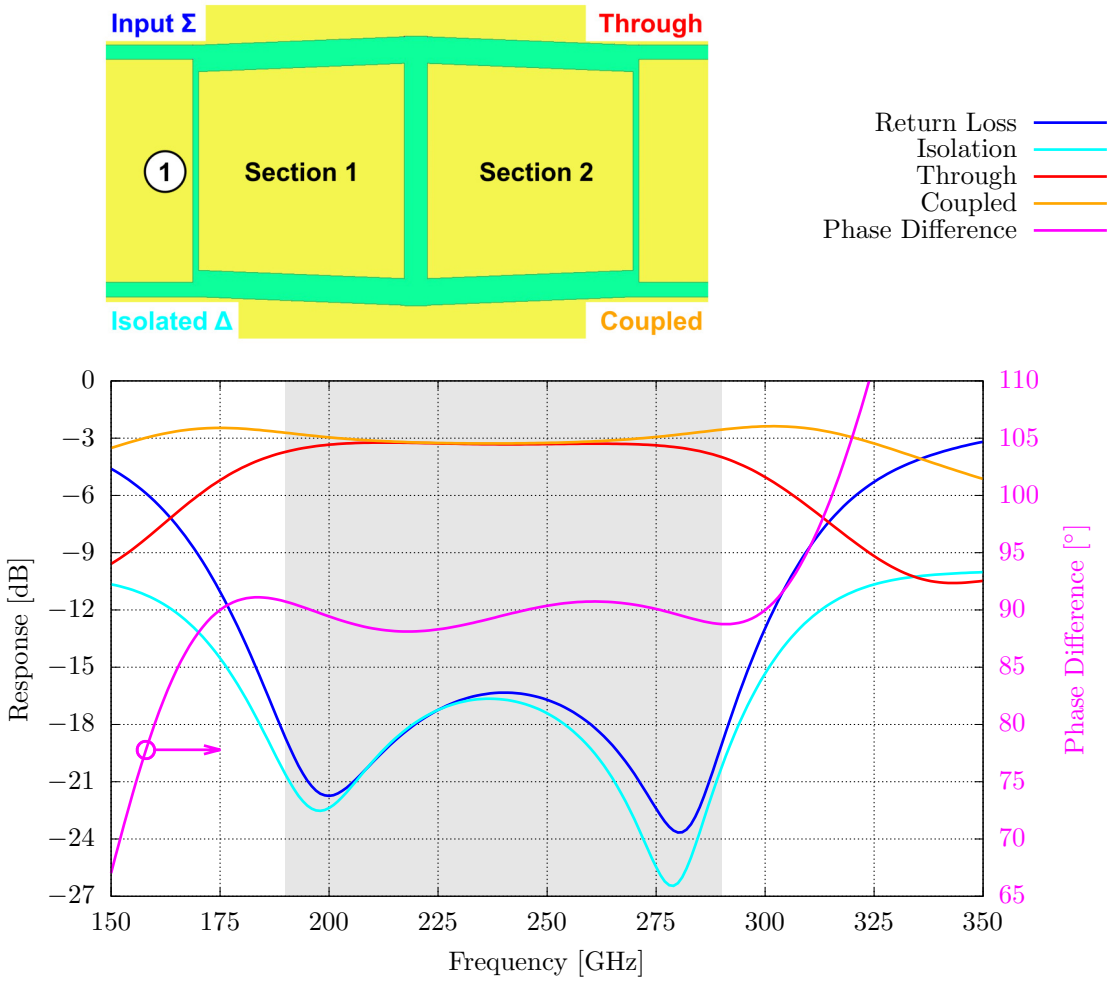


Figure 5.7: The simulated performance and layout of the two-section hybrid. The performance is shown for an input signal applied on the Σ port. The highest characteristic impedance microstrip (1) is between adjacent ports of a section.

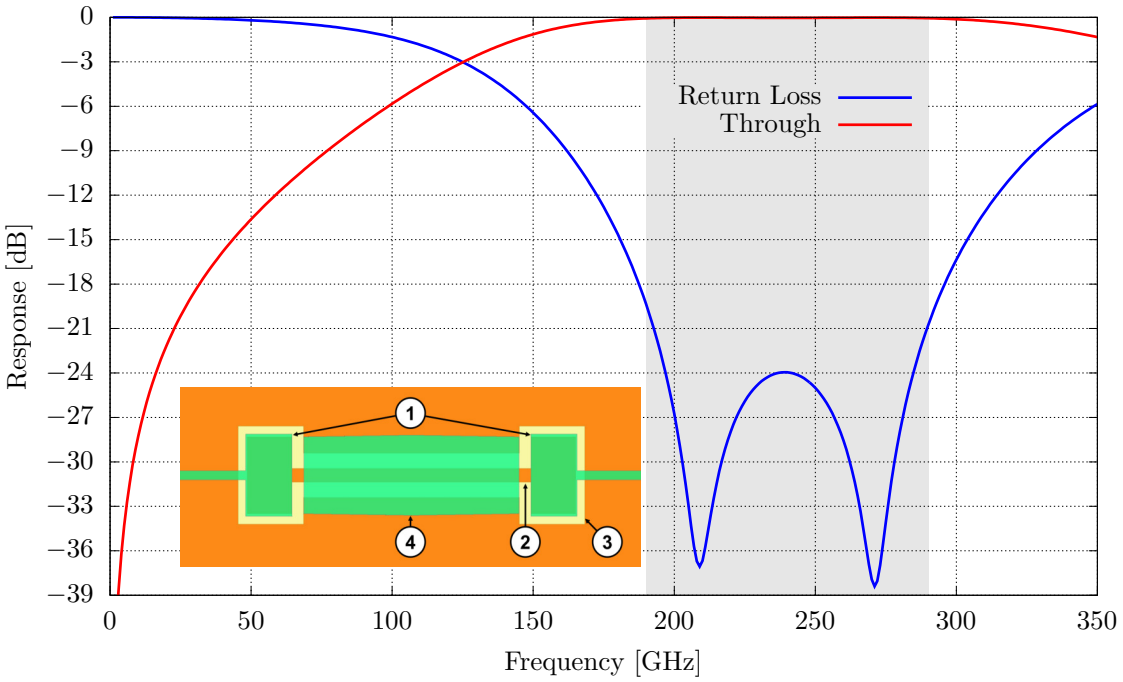


Figure 5.8: The simulated performance and layout of the BPF. Broadside couplers (1) link the feeding microstrip and the CPW (2), deposited within an opening in the ground-plane layer (3) and covered by a conductor patch in the wiring layer (4).

from the hybrid output to the SIS mixer. In this way, we can DC bias each SIS mixer independently.

The BPF design, shown in Figure 5.8, utilizes a set of broadside couplers to route the signal from the 3 µm wide microstrip into an 80 µm long CPW deposited within an opening in the ground-plane layer, leaving 5 µm wide gaps, similar to the crossover. Again, a 72 µm by 25 µm conductor patch on top of the CPW is deposited to improve the coupling of the broadside couplers. Consequently, the RF couples efficiently from the hybrid to the following SIS mixer with close to 0 dB coupling and without DC and IF leakage from the SIS mixer into the hybrid due to a through coupling well below –20 dB up to 20 GHz.

5.2.5 SIS Mixer and Lowpass Filter (LPF)

We opted for a twin-junction tuning circuit, as shown in Figure 5.9, although a single junction's impedance can be tuned with a series of stubs. Additionally, a 139 µm long and 9 µm wide series microstrip transformer is added in front of the twin-junction circuit to improve the impedance matching to the circuit prior to this SIS mixer circuit over the full bandwidth. The tuning circuit shown in Figure 5.9 comprises two

circular 1.5 µm^2 SIS junctions with 13.3 Ω dynamic resistance and 120 fF geometric capacitance separated by a 46 µm long 18 Ω microstrip section.

The downconverted IF signal is routed to the bonding pad via a microstrip connected to the second SIS junction. This microstrip would also pass considerable RF power to the bonding pads, reducing the power available for downconversion at the SIS junctions. Therefore, the second SIS junction is connected directly to an LPF, which consists of alternating high- and low-impedance, 3 µm and more than 50 µm wide microstrip sections to choke RF signals while passing IF signals. The LPF reflects the RF signal power so that more than −0.4 dB of the incoming RF power couples into the two SIS junctions and less than −30 dB couples through the LPF. This circuit, feeding the IF to the bonding pad, has an associated input impedance, which alters the RF tuning of the twin-junction circuit. We optimised the entire mixer circuit, including the LPF components, to ensure maximum power coupling to the junctions. Both SIS junctions couple close to −3 dB of the input power at the centre frequency, while on each end of the band, the signal couples to one of the junctions predominantly.

5.3 Layout of the Receiver Chip

The chip, shown in Figure 5.2, is too large to simulate as a single circuit in HFSS, especially since the waveguide and planar circuit components differ substantially in dimensions. Therefore, we split the receiver into two sub-circuits similar to traditional receivers: First, the polarised signal coupling network shown in Figure 5.10, routing signals from the OMT to the hybrids for each polarisation via the crossover; and second, the mixer circuit shown in Figure 5.11, comprising the BPF, the SIS mixer and the LPF. The mixer circuits connect to all four hybrid outputs of the polarised signal coupling network, similar to mixer blocks attached to waveguide OMTs in traditional receivers.

We first lay out these sub-circuits within HFSS and then interconnect these structures with Ansys Circuit, a software that applies transmission line theory to the scattering parameters generated by the HFSS models, also described in Appendix A. Thus, a single FEM analysis of the mixer circuit is sufficient in lieu of incorporating four identical mixer circuits as a large model. In the final step, we apply Tucker's theory to predict the receiver gain and noise temperature using the SuperMix library and the same circuit representation as in Ansys Circuit, which is described in Appendix A.3.

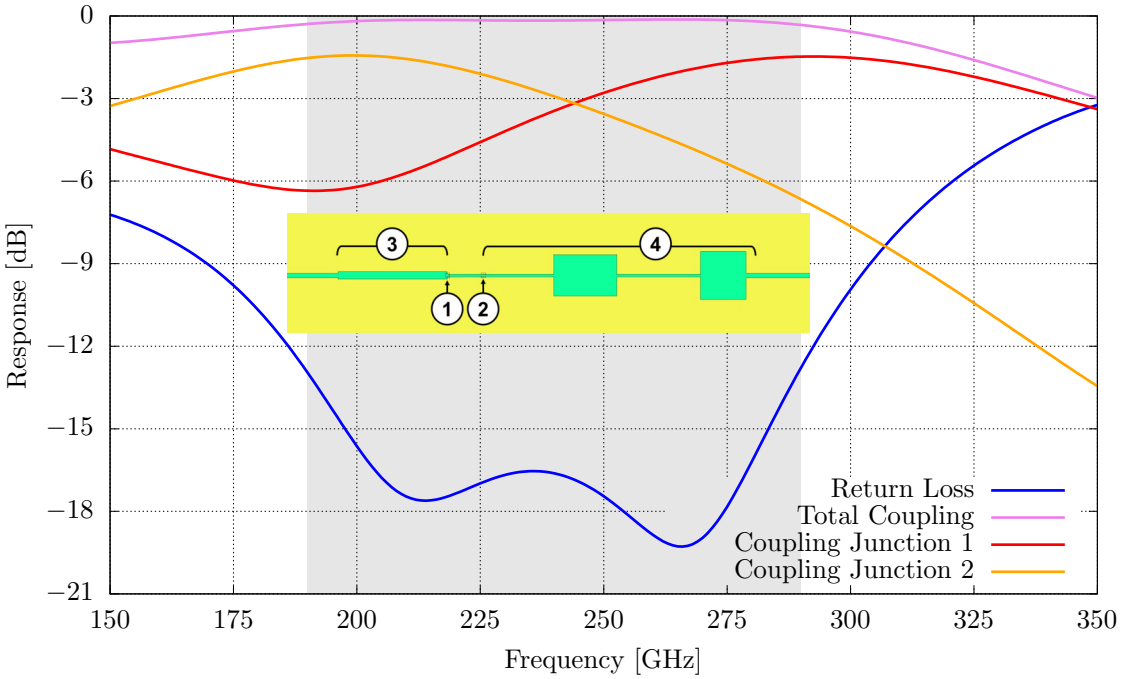


Figure 5.9: The simulated performance and layout of the SIS mixer and LPF. The SIS mixer consists of a twin-junction circuit, with the first SIS junction (1) closer to the RF circuit and the second SIS junction (2) after an intermediate microstrip. The RF circuit is connected to the twin-junction circuit via a serial impedance transformer (3) and the IF circuit via the LPF (4). Total Coupling denotes the sum over both junctions.

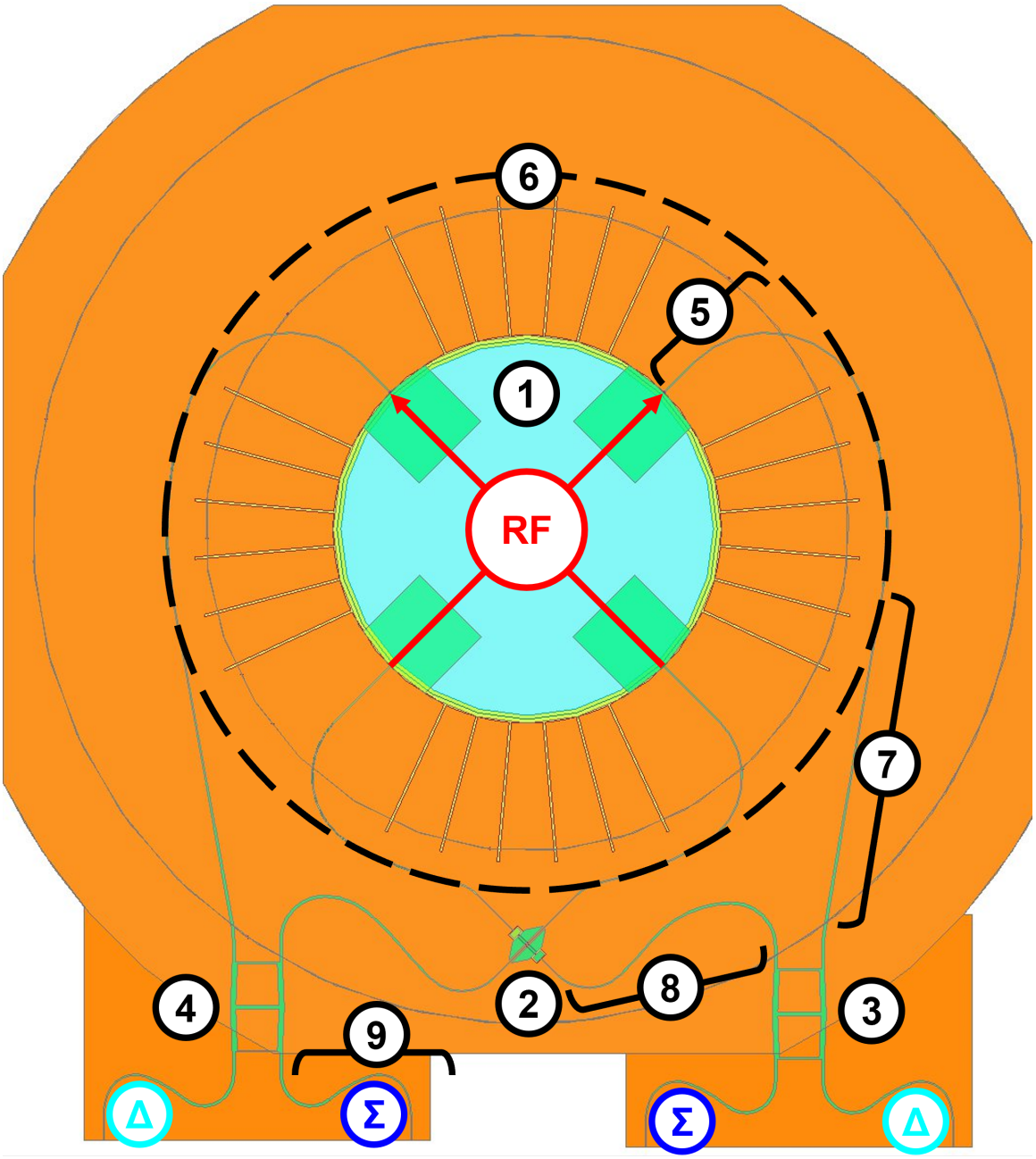


Figure 5.10: The polarised signal coupling network contains the OMT (1), the crossover (2) and two hybrids, which connect to the ground-plane-layer CPW of the crossover for Pol. 1 (3) and the wiring-layer CPW for Pol. 2 (4). Each OMT probe connects via a straight and an arced microstrip section (5) to the routing concentric to the OMT on the dashed line (6). From this concentric routing, the non-crossing microstrips, connecting the upper two probes, lead via a straight section and a curved section into the straight feeds of the hybrids (7). The crossing microstrips, connecting the lower two probes, lead from the concentric circle via an arc section to the straight feeds of the crossovers and afterwards via seven arcs to the hybrids (8). The hybrid outputs are curved to space out the following mixer circuits (9).

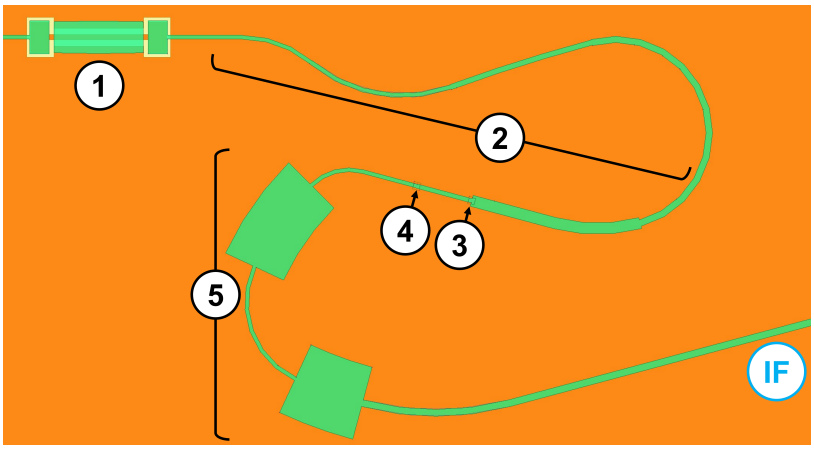


Figure 5.11: The layout of the mixer circuit. In the mixer circuit, the BPF (1) connects to the SIS mixer via a 3-section impedance transformer (2). The first (3) and second (4) junctions are followed by the LPF (5), which leads to the IF output.

5.3.1 Polarised Signal Coupling Network

The polarised signal coupling network, shown in Figure 5.10, contains the OMT, crossover, and two hybrids. The crucial parameter in this circuit is the microstrip length between the OMT probes and the hybrid input ports. To ensure that the full signal power of one polarisation recombines at the Σ port of the hybrid, the microstrip lengths adjust the 180° phase difference between a set of opposing OMT probes to the 90° phase difference at the inputs of a hybrid by having a length difference equivalent to a quarter-wavelength at the centre frequency.

Moreover, the routing of the two polarisations is symmetric to avoid undesired biases towards one polarisation due to loss differences introduced by, for example, the dielectric. Therefore, the crossover is placed at the centre between OMT probes, and the hybrids are located symmetrically with respect to the centre line formed by the OMT and crossover. Furthermore, the hybrids are arranged in parallel to this centre line so that their outputs lead to the same chip edge at which all mixers can be connected to the IF transformer, keeping the receiver compact.

We designed the transmission lines connecting the OMT to the hybrid with straight and curved microstrip lines to avoid corner discontinuities and to reduce the total microstrip lengths. To make the optimisation of the design feasible, we first chose a suitable geometry with which all microstrips could be restricted except the straight sections connecting to OMT probes and the following arc, which leads into a concentric circle centred at the OMT, as shown in Figure 5.10. We then achieved the required 90° phase difference between the hybrid inputs by varying the length of the

Polarisation	Pol. 1		Pol. 2	
Microstrip	Uncrossed	Crossed	Uncrossed	Crossed
Length	2128 µm	1884 µm	2115 µm	1871 µm
Crossover Length	N.A.	100 µm	N.A.	125 µm
Total Length	2128 µm	1984 µm	2115 µm	1996 µm
Difference	144 µm		119 µm	

Table 5.1: The microstrip lengths connecting the OMT and the hybrids.

straight microstrip sections connecting the OMT probes and the radius of the following curved section, keeping the radius of the OMT-concentric circle, the position of the crossover, and hybrid fixed.

Table 5.1 summarizes the physical lengths of the microstrips connecting the OMT probes and the hybrids in Figure 5.10, which are routed at the crossover in the ground-plane-layer CPW for Pol. 1 and the wiring-layer CPW for Pol. 2. The length of the microstrips routed via the crossover is approximately a quarter-wavelength shorter than that of the uncrossed microstrips; thus, the Σ ports of the hybrids are closer to the OMT-crossover centre line.

In addition to adjusting the phase difference at the hybrid inputs, all circuit elements are impedance matched to avoid reflections, maximising the signal power coupling to the mixer. Both the OMT and the crossover connect to 19 Ω microstrips, requiring no intermediate impedance transformer, whereas 9 Ω microstrips connect the hybrid as described in Section 5.2.3. Consequently, the microstrips connecting the OMT and crossover to the hybrids are designed as 5-section binominal impedance transformers [26]. Similarly, the hybrid outputs are constructed from 3-section binominal impedance transformers to match the BPF in the mixer circuit, which again is fed by a 19 Ω microstrip.

The simulation in Figure 5.12 shows that both polarisations couple almost identically with approximately −2 dB to their designated Σ ports. In fact, the cross-coupling between the two Σ ports, corresponding to contamination of the two polarisations, is less than −30 dB. Furthermore, the low coupling level into the Δ ports suggests that the circuit is indeed tuned to a 90° phase difference at the hybrid inputs. Similarly, the general behaviour of the OMT remains unchanged apart from the expected addition of return loss poles and a slightly higher return loss level, which can be attributed to the addition of impedance transformers and circuit elements such as the hybrid. In summary, the polarised signal coupling network reliably separates the

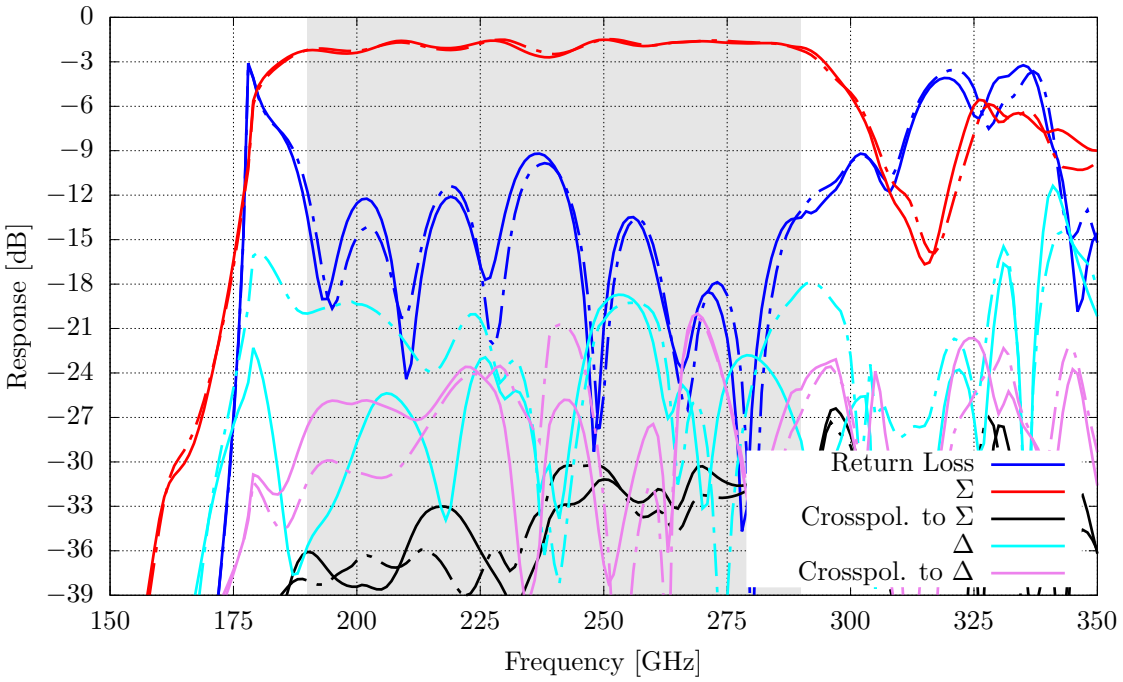


Figure 5.12: The simulated performance of the polarised signal coupling network with the Pol. 1 responses as solid lines and Pol. 2 responses as dash-dotted lines. Σ and Δ denote the coupling to the respective hybrid ports.

polarisations and recombines the signal power into a single microstrip throughout the desired frequency band.

5.3.2 Mixer Circuit

The polarised signal coupling network outputs connect to the mixer circuit, comprising the BPF, the SIS mixer and the LPF. We employ these filters so that the RF signals can propagate via the BPF to the SIS mixer for downconversion but not through the LPF, and the downconverted IF signal can only propagate through the LPF.

Figure 5.11 shows that the BPF connects to the RF input of the SIS mixer via a 3-section impedance transformer to match the 19 Ω output of the BPF to the 12.5 Ω input of the SIS mixer circuit. The impedance transformer and the LPF are meandered to decrease the footprint of the mixer circuit, while the twin-junction circuit of the SIS mixer is on a straight microstrip section. This layout can be fitted to the polarised signal coupling network while maintaining compactness and symmetry. Likewise, the LPF output is angled compared to the feeding microstrip to achieve even spacing between the bonding pads in the layout of the whole receiver chip.

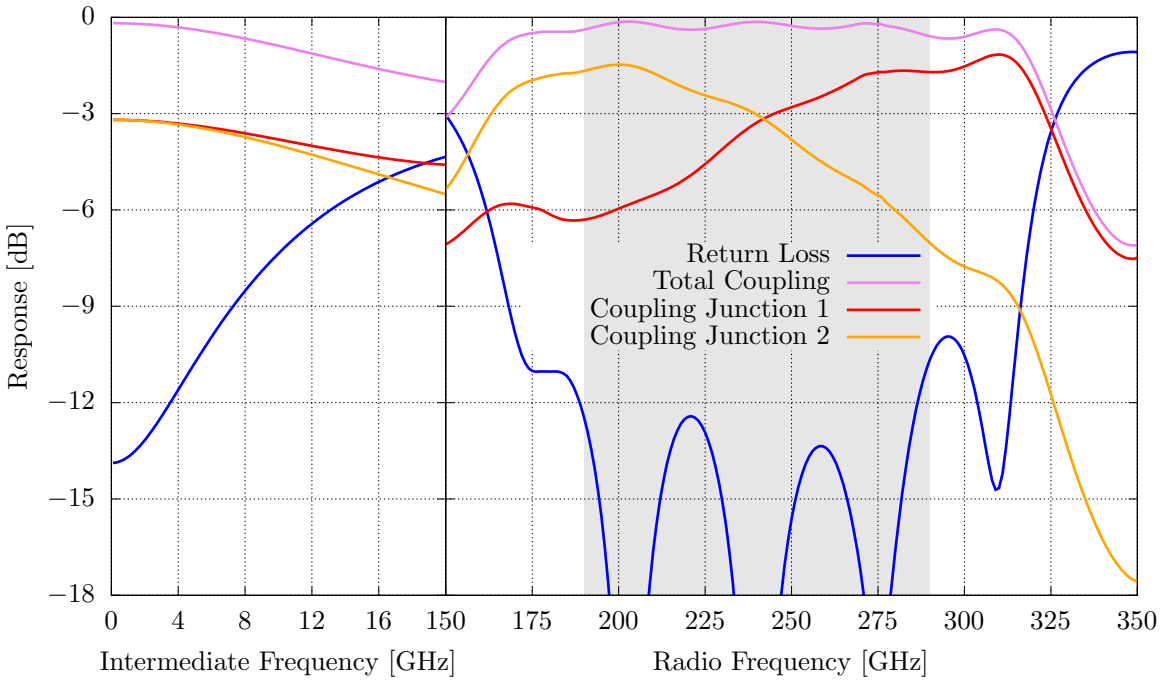


Figure 5.13: The simulated performance of the mixer circuit. At IF, the parameters, such as the return loss, are referred to the IF port of the circuit, and at RF, the parameters are referred to the RF port. Total Coupling denotes the sum over the individual junctions.

Figure 5.13 shows the power coupling from the junctions to the IF and RF ports as a function of frequency. Adding the BPF to the SIS mixer and LPF introduces poles in the return loss, but none of these poles peaks above −12 dB within the operation band. The general behaviour of the coupling curves into the individual junctions remains largely similar to the previous mixer circuit simulations, which not include the BPF. In fact, the addition of the BPF reduces the total coupling by less than −0.2 dB while introducing a −30 dB isolation between the RF and IF port throughout the shown IF and RF range. The IF results have to be interpreted with the caveat that the solution setup is the same for IF and RF, using the port parameters for the RF. The port impedance is larger at IF than at RF by a factor that depends on Tucker's theory and the pumping level. Thus, the shown the total coupling summed over both junctions only drops below −3 dB above 30 GHz in Figure 5.13, but accounting for the higher IF port impedance results in a −3 dB drop at approximately 6 GHz.

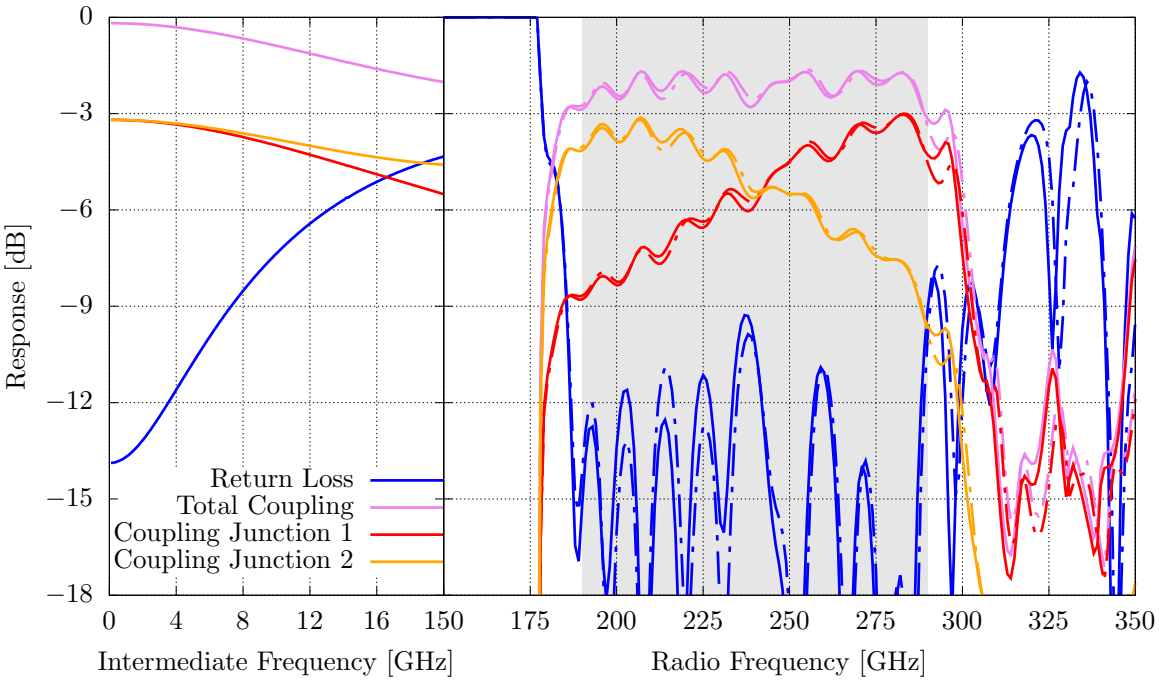


Figure 5.14: The simulated overall performance of the polarised signal coupling network connected to four mixer circuits, representing the full on-chip receiver. At IF, the parameters are referred to the four IF ports for which the performance is identical. At RF, the parameters are referred to the circular waveguide port with Pol. 1 as solid lines and Pol. 2 as dash-dotted lines. Total Coupling denotes the sum over the individual junctions.

5.3.3 Simulated Performance of the Full Receiver Chip

The performance of the entire receiver chip, shown in Figure 5.14, is simulated by connecting the polarised signal coupling network to four mixer circuits in Ansys Circuit. The IF response is identical for all four mixer circuits, and the polarised signal coupling network does not affect the IF behaviour, indicating a well-functioning BPF. At RF, both polarisations continue to behave similarly, without any bias towards a particular polarisation. In fact, adding the mixer circuits introduces only extra return loss poles without overly increasing the return loss level and increases the coupling into the Δ mixer circuit by less than 2 dB. The coupling level from the circular waveguide to the designated Σ mixers is around -2 dB, dominated by the OMT losses, as explained earlier. The cross-coupling level between the two polarisations remains below -30 dB, mirroring the behaviour of the polarised signal coupling network.

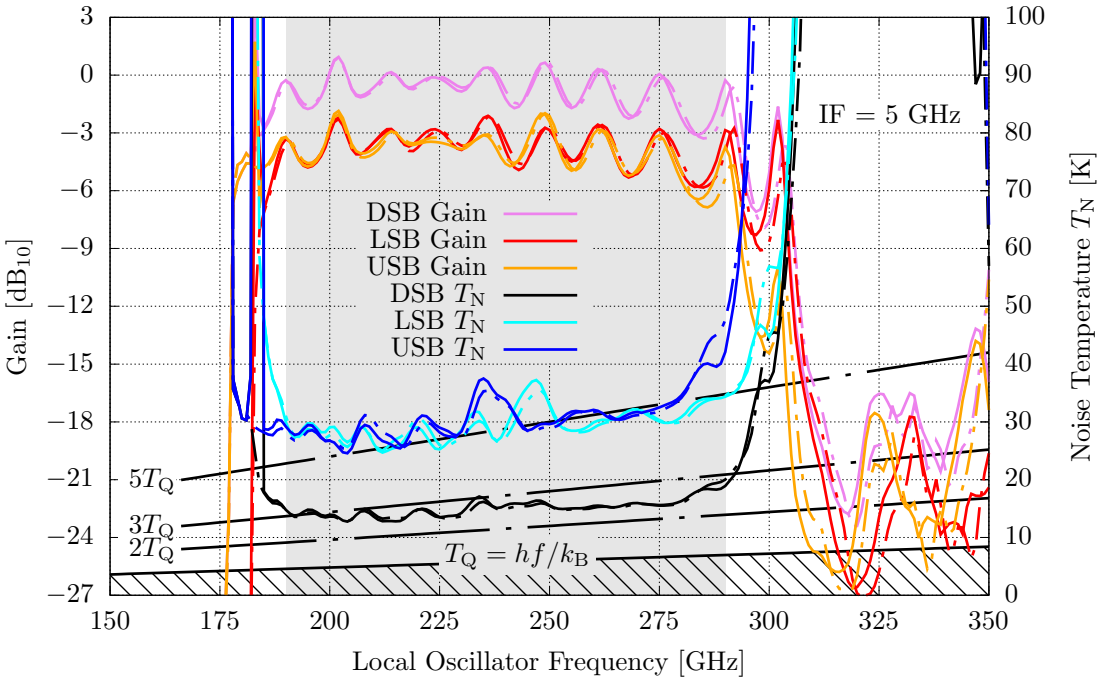


Figure 5.15: The simulated DSB mixer gain and noise temperature over LO frequency with Pol. 1 responses as solid lines and Pol. 2 as dash-dotted lines at 5 GHz IF.

5.3.4 Gain and Noise Temperature Analysis

We analyse the mixer gain and noise temperature T_N of our receiver using a circuit model similar to the Ansys Circuit setup with a C++ script based on the SuperMix library, which is described in more detail in Appendix A.3 [113, 114]. The circular waveguide has a frequency-dependent port impedance following HFSS simulations, but now we also employ a standard impedance matching circuit to match the on-chip circuit to 50 Ω. We carefully chose the LO power and DC bias in order to maximise the double-sideband (DSB) mixer gain at 5 GHz IF. Figure 5.15 shows the optimised DSB mixer gain, the sum of lower-sideband (LSB) and upper-sideband (USB) gain, and preliminary predictions for the noise temperature T_N. Again, both polarisation states have an almost identical response. The DSB gain approaches 0 dB, and the DSB noise temperature $T_{N,DSB}$ is between two and three times the quantum limit T_Q. We want to emphasise that the noise temperature values shown in Figure 5.15 are much lower than expected in the real experiment since the model does not include losses of several receiver components, such as optics, but only the chip itself.

5.4 Conclusion

This chapter presents the design of a planar-circuit dual-polarisation receiver with 240 GHz centre frequency and 100 GHz bandwidth. First, we gave an overview of the receiver layout and the required circuit components. Then, we presented the designs of these critical components in detail before combining them to form the on-chip receiver. We explain the careful steps required to be taken into account to connect these components to form the receiver circuit, such as the careful adjustment of the length of the microstrip to ensure proper operation of the hybrid and how the layout is planned to ensure a symmetric and compact layout that is easy to scale and fabricate. The final simulation of the receiver chip shows that we successfully separate the two polarisations with less than −30 dB cross-coupling and feed approximately −2 dB RF power into the SIS mixer for downconversion. The associated losses in the coupling are dominated primarily by the OMT fabricated on the available quartz substrate.

The size and complexity of the integrated receiver prevents a detailed tolerance analysis within this thesis. However, we identified some critical circuit features from designing the individual circuit elements, presented in Section 5.2 in addition to those relating to the SIS junction as described, for instance, in [115]. First, the alignment of the ground layer and wiring layer are important at the broadside couplers of the crossover and the BPFs. Inaccuracies in fabrication can impact the performance substantially. Second, the OMT has several features, such as the thickness of the quartz substrate or the machining of the receiver block, which are not part of the cleanroom fabrication process described in Appendix A.4. Furthermore, variations in the electrical length of the microstrips between the individual circuit elements, as it could be caused by a different ϵ_r of the SiO dielectric, can cause issues with the phase difference at the hybrid inputs or even resonances. As this short outline shows, the scope a full and structured tolerance analysis of this receiver chip is beyond the scope of thesis.

Chapter 6

Experimental Investigation Setup

Chapter parts published:

- J. Wenninger, F. Boussaha, C. Chaumont, B. K. Tan, and G. Yassin, "Design of a 240 GHz On-Chip Dual-Polarization Receiver for SIS Mixer Arrays," *Superconductor Science and Technology*, 2023, and
- J. Wenninger, F. Boussaha, C. Chaumont, B. K. Tan, and G. Yassin, "Preliminary Characterisation of a Compact 240 GHz SIS Dual-Polarisation Receiver for Large Array Applications," in *32nd IEEE International Symposium on Space Terahertz Technology*, 2022.

The receiver chip presented in the last chapter, Chapter 5, comprises most of the RF circuit logic, but as illustrated in Figure 5.1, a few additional components are required to make the receiver, such as the feedhorn and IF components. The design and setup of these components are important to allow for extending into a large format array. Furthermore, a whole experimental system is required to characterise our receiver.

In this chapter, we present the design for the experimental characterisation setup of the on-chip receiver. We first introduce the compact pixel design, which is extendable into a multi-pixel array. In the second section, a 4-pixel array is presented as a minimalistic demonstrator, highlighting that our design concept makes larger arrays feasible. We then describe the preparation of the receiver and the method used to mount the receiver chip in the block. In the fourth section, we look at the cryostat design, and finally, we present the whole laboratory setup for the experimental investigation of the receiver and highlight some details and possible configurations.

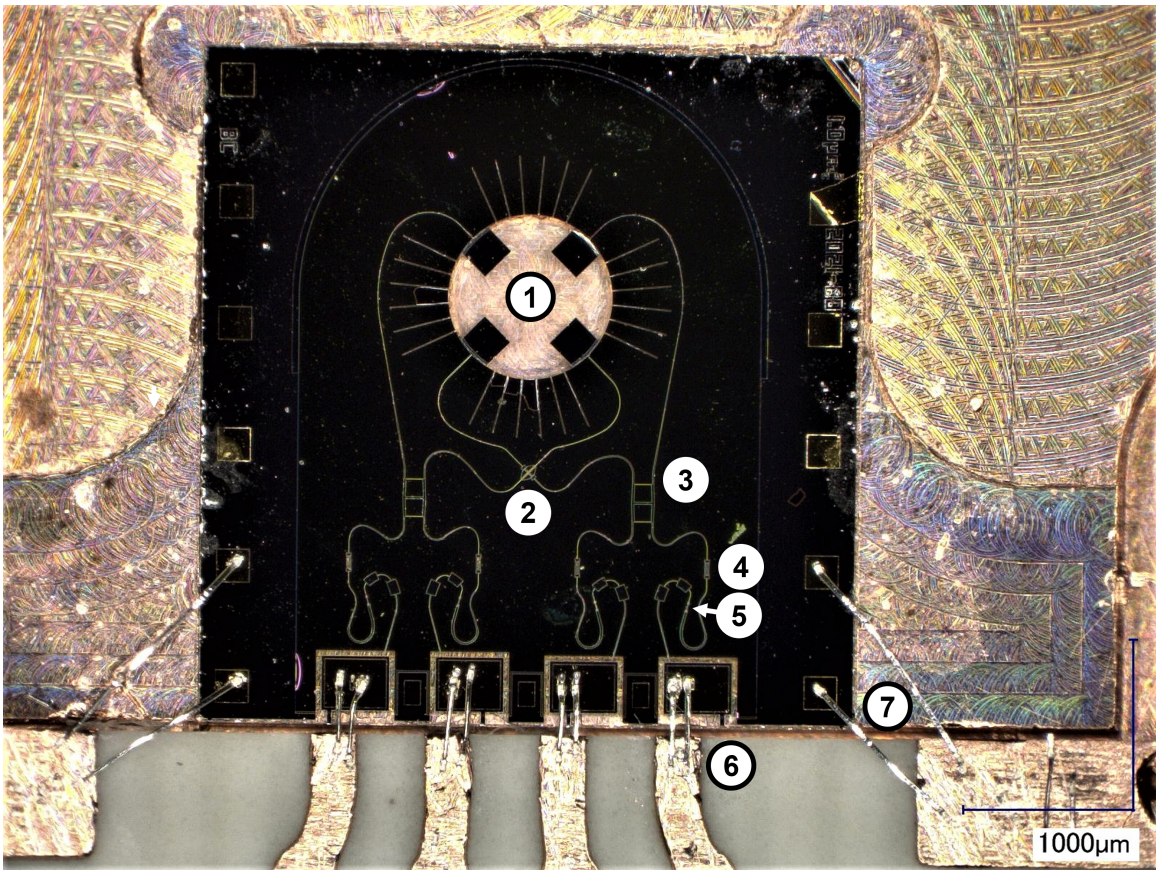


Figure 6.1: The thinned receiver chip mounted in the bottom block and bonded to the IF transformer. The chip consists of the OMT (1), the crossover (2) and two hybrids, where the hybrid for Pol. 1 is marked with (3). All hybrid outputs connect via a BPF (4) to a twin junction SIS mixer (5). The twin junction SIS mixer connects via the LPF and bond wires to the IF transformer (6). The ground is connected at (7).

6.1 Design of the Mixer Block for a Single Pixel

Figure 6.1 shows the receiver chip presented in Chapter 5 fabricated using the cleanroom facilities at the Observatoire de Paris. The entire receiver is fabricated onto a 4.0 mm by 4.1 mm quartz substrate, hence, the design of our split block is substantially simplified. As shown in Figures 6.2 and 6.3, the mixer block is made up of two separate parts using split block technology without the need for any complicated mechanical waveguide structure. The top block comprises a compact three-section flare-angle smooth-walled horn and openings for the magnetic circuit assembly, and the bottom block has a large area milled out for hosting the mixer chip, magnetic shoes, and IF transformer with holes for the IF and DC connectors. The entire mixer block is only 40 mm by 40 mm, the size determined primarily by the size of the IF SMP connectors and the IF transformer.

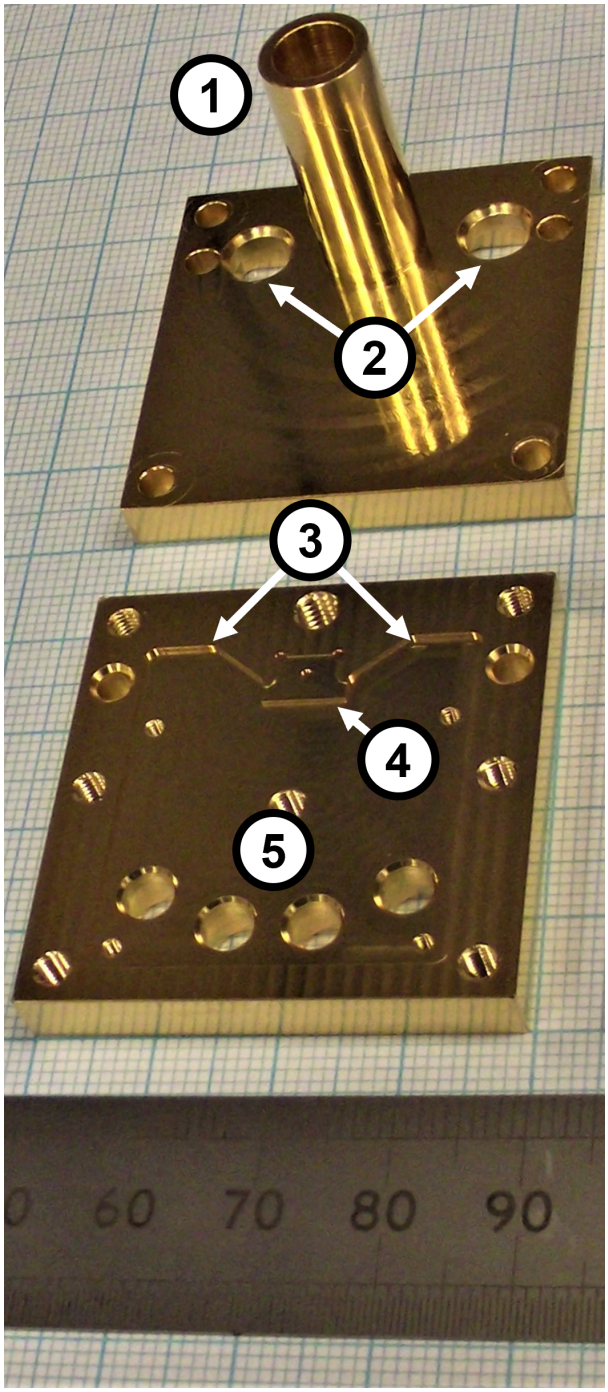


Figure 6.2: The split block image shows the feedhorn (1) and the holes for magnetic biasing (2) drilled into the top block. The bottom block is milled out to accommodate the magnetic shoes (3) and the IF transformer, which is bonded to the mixer chip sitting in the bottom block on a pedestal with the backshort section (4). The DC and IF signals are connected via panel-mount SMP connectors fed through holes (5).

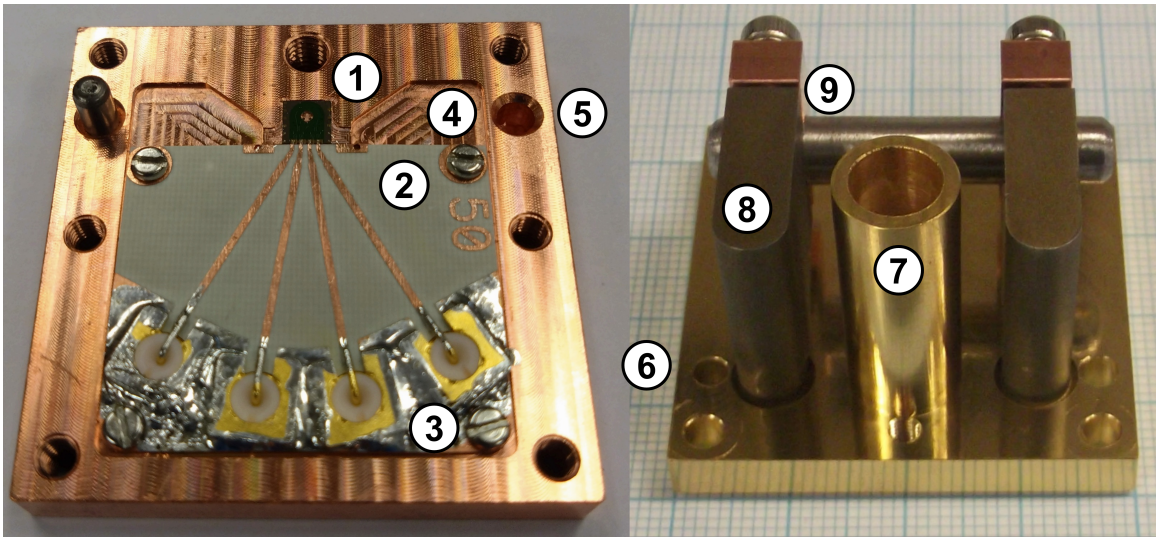


Figure 6.3: The receiver is made from the bottom block on the left, the top block on the right, and the receiver chip on a pedestal in the bottom block (1). The receiver chip is wire-bonded to the IF transformer (2), which ends in SMP connectors (3) to the rear of the receiver. The bottom block has a recess for the IF transformer and coil shoes (4). An identically shaped but deeper counterpart is in the top block. Dowel holes in the bottom (5) and top (6) block align the feedhorn (7) with the receiver chip and the backshort section, which is milled into the bottom block. The magnetic assembly consists of a feed (8) connecting the shoes next to the receiver chip with the coil, which sits on a rod clamped on the feed (9).

Figure 6.4 (a) shows the interior of our pixel in the explosion view. The receiver chip sits on a pedestal in the bottom block, where the bonding pads are adjacent to the IF transformer, which are also shown in detail in Figure 6.1. The IF signals are connected from the chip to the IF transformer via bond wires and then directed to the bottom of the pixel via panel-mount SMP connectors, as shown in Figure 6.3. For practicality, the IF transformer size has plenty of margins to accommodate different circuit designs. We can further reduce the IF transformer and, consequently, the pixel size in a future design refinement once the IF transformer design is finalised.

The bottom block is milled into three levels, as shown in Figure 6.2 and the explosion view in Figure 6.4 (a). The lowest level for the 290 µm thick IF transformer allows for same-level wire bonding to the surface of the receiver chip, which sits on a pedestal forming the middle level, shown in Figure 6.1. The top level is the interface to the top block defining the height of the receiver chip substrate and vacuum slit above this region. This prevents fabrication tolerances from adding up, as would be the case with a non-flat top block surface.

The interior of the top block has only two levels, namely, one interfacing with the bottom block and a lower level to accommodate the vacuum above the IF transformer and the magnetic shoes. These magnetic shoes are either permanent magnets with a threaded bush counterpart or, as in the design option shown in Figures 6.3 and 6.4 (a – c), iron cores fed by a coil at the top of the pixel.

The main feature of the top block is the three-section flare-angle smooth-walled feedhorn required to couple the RF and LO signals from free space to the planar OMT on the receiver chip. This horn type has the properties of a corrugated horn, but it is easier to fabricate [116–118]. The horn is fabricated by first drilling a pilot hole and then opening this hole to the three-section flare-angle hole with a special drilling tool. The used dimensions and drilling tool are reported by Leech [119, 120], together with the predicted and measured performance. The only difference in our receiver is that the pilot hole, and, therefore, the smallest radius, is 0.5 mm instead of 0.62 mm in the publication. We adjusted the length of the first flare to achieve the same opening angle of the section and reuse the drill. Our simulations show negligible effects of this change except for an increased return loss at the low-frequency end due to the higher cutoff frequency with a smaller waveguide radius.

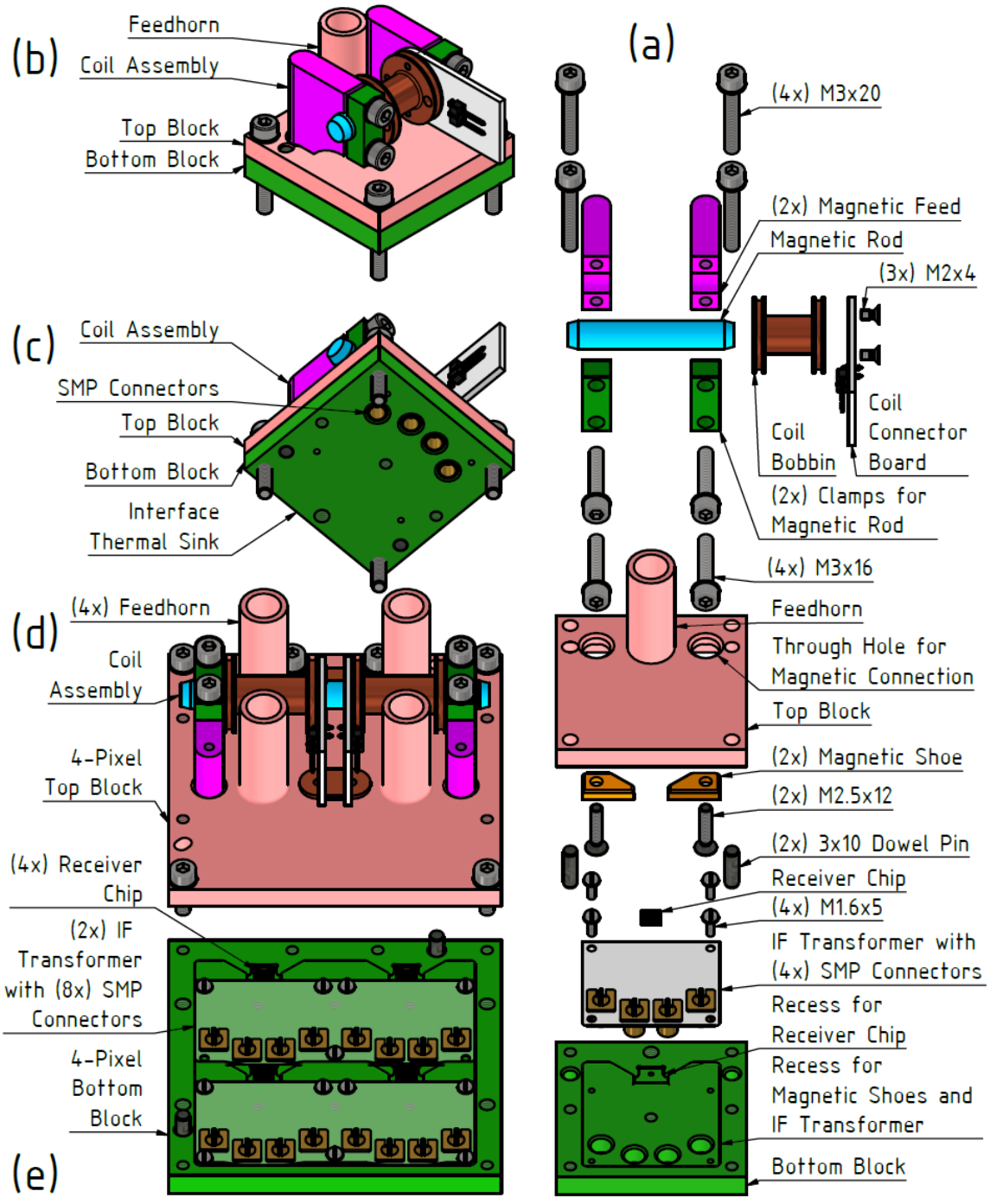


Figure 6.4: The explosion view of the pixel (a) and the assembled pixel viewed from the front (b) and the rear (c). The 4-pixel array extension is separated in the (d) top and (e) bottom block assemblies.

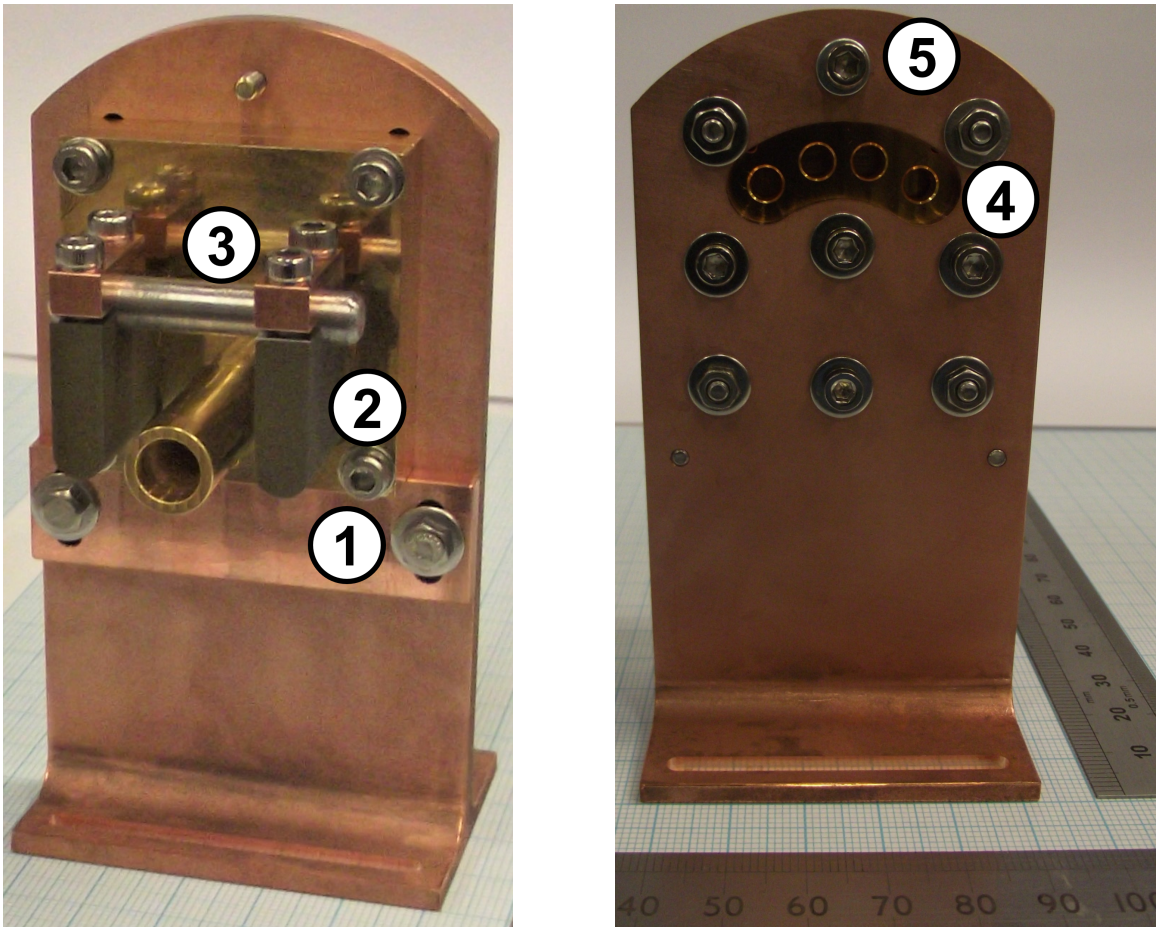
6.2 Extension into a Multi-Pixel Array Block

One important aspect of the simple mixer block design is that all the required accesses are provided via the front and the rear faces of the block, as shown in Figures 6.4 (b, c) and 6.5. The top surface of the pixel shown in Figure 6.4 (b) is mainly occupied by the mentioned coil assembly, fitted within the footprint of the pixel, and the drilled three-section flare-angle smooth-walled feedhorn to inject the RF and the LO to the chip [117, 119]. In contrast, the bottom surface of the pixel shown in Figures 6.4 (c) and 6.5 features only the SMP connectors to connect the IF and DC signals alongside its flat surface, on which the thermal sink is flanged.

Therefore, all four adjacent sides of the pixel are left available for array extensions. This allows a straightforward extension of the 40 mm by 40 mm single-pixel design into a multi-pixel array with a 40 mm pitch between the pixels. Some features of the single-pixel design are only required on the outermost edges, such as the dowel pins. Therefore, removing those parts yields a pixel pitch of 30 mm with similar generous margins for the IF transformer, as shown in Figures 6.4 (d, e) and 6.6. This 4-pixel design, 70 mm by 70 mm in size, is fed by a single magnetic circuit with the possibility to mount four independent coil assemblies for each pixel or permanent magnets, similar to the single-pixel design. Importantly, this 4-pixel design again has unobscured adjacent sides and thus can be extended to an even larger array. For practicality in the lab, we set the number of pixels to four. The existing cryostat window setup allows only for illuminating one pixel. Thus, the characterisation of the 4-pixel design requires adjustments in the cryostat, as shown in Figure 6.7. However, Figure 6.7 shows that this design can be easily extended to a larger pixel count array because the sides of the array are unobscured. For the most part, the 4-pixel dual-polarisation receiver is ready to be populated with devices and characterised once the single-pixel tests are finalised satisfactorily.

6.3 Receiver Chip Preparation

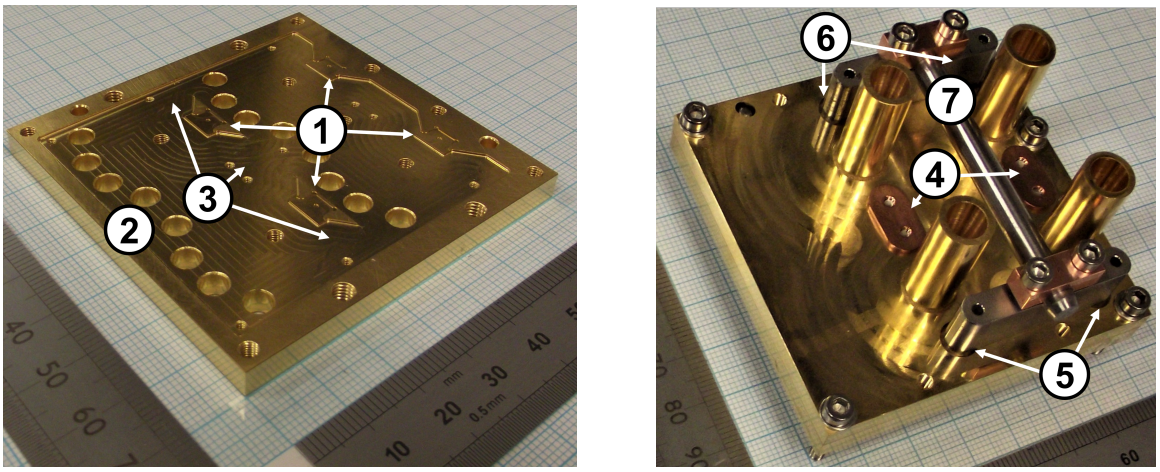
After Faouzi Boussaha and Christine Chaumont at the Obervatoire de Paris fabricated the devices, we selected devices for thinning to the designed quartz thickness of 50 µm based on the fabrication yield measured by sampling devices across the wafer. The devices were thinned with a dicing saw by Mark Merritt at the Rutherford Appleton Laboratory. We mounted the thinned devices with a brush to their position in the bottom block and affixed them with Agar Scientific Crystalbond 555, a low



(a) Front view;

(b) Rear view;

Figure 6.5: The front and rear faces of the receiver block on the bracket for the cryostat test setup. The assembled receiver block is 40 mm by 40 mm by 10.5 mm in size. A stopper (1) on the front of the bracket allows for adjusting the feedhorn position relative to the cryostat window. The magnetic feed (2) connects to the magnetic shoes in the block next to the receiver chip and to a rod (3) on which a coil is mounted. At the rear of the bracket is an opening to access the SMP connectors for the DC and IF connections (4). The thermometer for the receiver is mounted at the top of the bracket (5).



(a) The bottom block; (b) The assembled block;

Figure 6.6: The 4-pixel receiver array block, 70 mm by 70 mm by 10.5 mm in size. Four individual receiver chips are mounted on pedestals (1), and the DC and IF signals are connected to the receiver chips with panel-mount SMP connectors (2) via IF transformers. The magnetic shoes are located in recesses (3), where the middle shoe is fixed with a bushing (4) in the shown configuration. In the block are two magnetic circuit arms in parallel connected at (5) and (6) and fed from a single coil assembly on a rod (7).

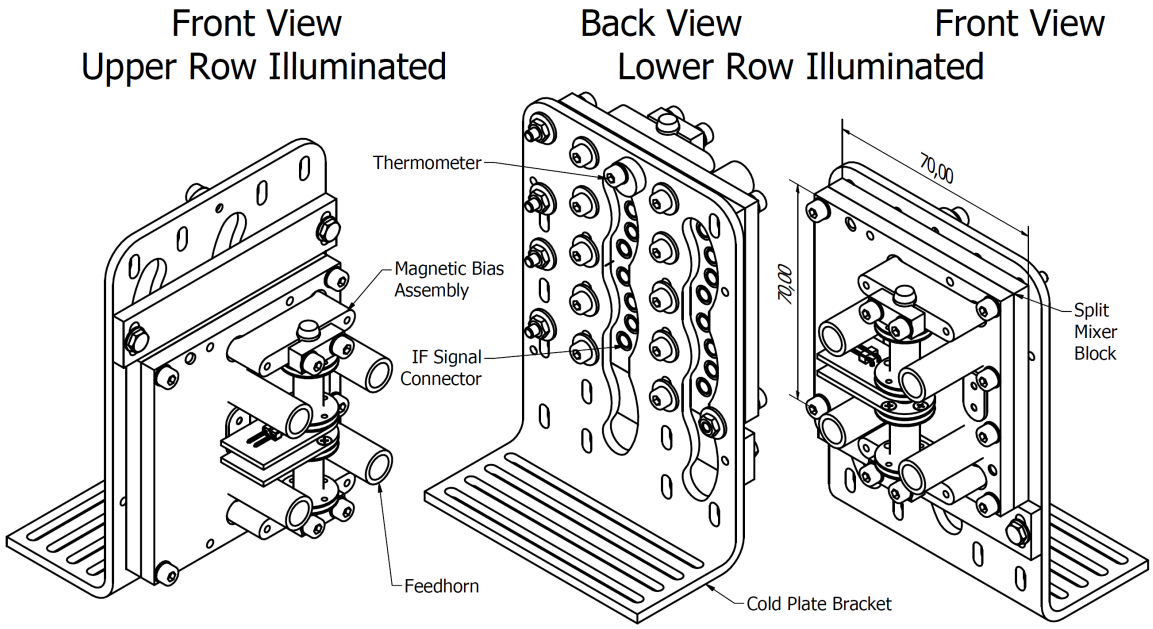


Figure 6.7: The 4-pixel mixer block has four feedhorns located in a 30 mm by 30 mm square, with the entire block 70 mm by 70 mm in size. The drawing shows the magnetic bias assembly consisting of a single circuit driven by two coils and splitting into a parallel circuit within the mixer block.

melting point (54 °C) adhesive. Crystal bond is more versatile than the commonly used superglue since it can be applied without time restrictions and re-liquefied for adjustments.

A frequent source of difficulty was applying pressure on the receiver chip to remove excess adhesive between the chip and the bottom block. The excess adhesive would elevate the chip and consequently cause the chip to touch the top block, potentially destroying the receiver chip once assembling the receiver. In case the receiver chip protruded from the bottom block, we liquefied the crystal bond and adjusted the chip position. We followed the same procedure when we could identify an imperfect alignment of the backshort section underneath the optically transparent OMT.

An effective tool for positioning the receiver chip and applying pressure is the chip mount rig shown in Figure 6.8. The 3D-printed rig consists of a platform, which flanges on the bottom block with the IF transformer board. Three 3D-printed arms, spring-loaded on screws, press the chip down after a first adjustment. The employment of springs allows moving the arms and adjusting the chip with sharp wooden sticks without damaging the receiver chip. Furthermore, the arms are positioned and kept short enough to prevent them from touching microstrip structures as long as the receiver chip is approximately in its final location.

Once we satisfactorily mounted the receiver chip in the bottom block, we wire-bonded the receiver chip to the IF transformer in Oxford Physics cleanroom facilities, and then mounted the top block on the bottom block, forming the receiver. This receiver was mounted in the cryostat for RF characterisation.

6.4 Design of the Cryogenic Receiver

The assembled receiver mounted in a liquid helium cryostat and connected to the signal processing chain is shown as a technical drawing in Figure 6.9 and a photograph in Figure 6.10 with the DC wiring. The pixel is fastened to the cold plate via a bracket with an access hole to the SMP connectors, shown in detail in Figure 6.5. SMP connectors are used due to the smaller footprint of the push-pull mechanism in comparison to the hex nut of SMA connectors, which would need additional space for a spanner, keeping the receiver compact. The four mixer circuits on the receiver chip connect via adaptor coaxial cables from the SMP connectors to the SMA connectors of the AEROFLEX bias tees rated up to 26 GHz. These bias tees are clamped between two brackets for structural integrity and thermalising the assembly. The two bias tees connected to the Δ mixer circuits have terminated AC ports, while the two bias tees

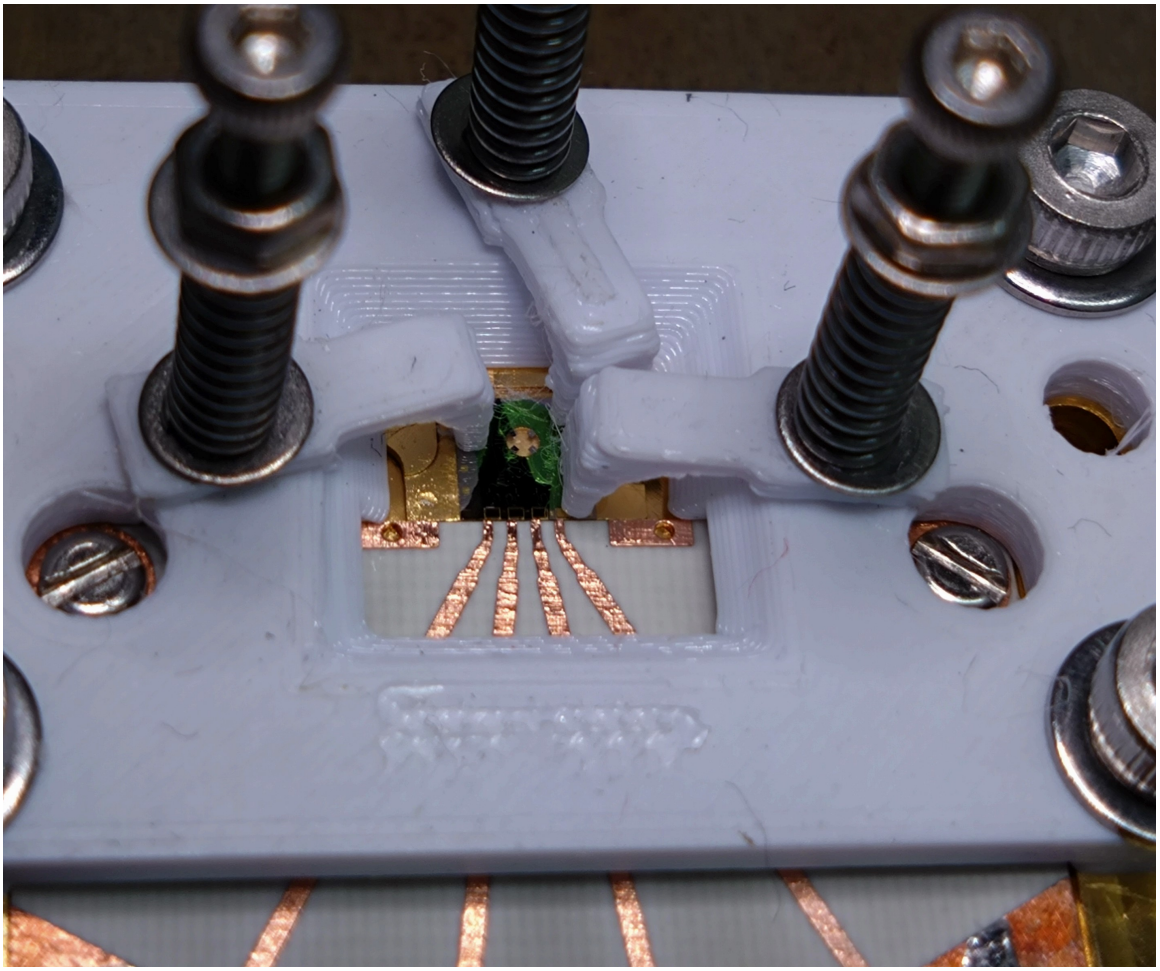


Figure 6.8: The 3D-printed chip mounting rig. Three spring-loaded arms apply pressure on the receiver chip while the crystal bond dries. The arrangement prevents physical contact of the arms with on-chip circuitry and allows for positioning the on-chip OMT over the backshort section in the bottom block.

connected to the Σ mixer circuits connect to QUINSTAR circulators and CITCRYO 4 GHz to 12 GHz LNAs with more than 35 dB gain. Following such high amplification, the IF signal is then fed via stainless steel cables to the room temperature detector system. The LNAs are clamped on brackets to dissipate the generated heat. The DC ports of the four bias tees connect independently to room-temperature four-way bias modules and a data acquisition (DAQ) unit. Thus, the DC signal of all four mixers can be swept and read simultaneously. The linear arrangement of the signal processing chain behind and within the footprint of the receiver can be extended to an array in an ALMA-style cartridge.

6.5 Experimental System Overview

The characterisation in the lab has several setup options. The following system overview highlights connections and user interfaces. The whole system is split into the five subsystems shown in Figure 6.11:

Quasi-Optical Feeding System The LO source is placed on an optical table with various additional components. The LO source is a Linwave Gunn diode in a cavity emitting from 71 GHz to 86 GHz via a WR12 waveguide. The precise frequency is manually adjusted via a micrometre, and an additional power micrometre is used to optimise the emitted LO power. The frequency of the generated signal is measured via a Radiometer Physics waveguide coupler connected to a frequency counter. A Radiometer Physics W band (75 GHz to 110 GHz) isolator protects this assembly from reflections at the tunable waveguide attenuator and the following frequency tripler, shown in Figure 6.12. The Radiometer Physics attenuator is controlled via one micrometre, and the input and output couplings of the Radiometer Physics frequency tripler are controlled with two micrometres. The output waveguide connects via a rectangular to circular waveguide adaptor to a multi-flare angle feedhorn, emitting the signal between 213 GHz and 258 GHz.

There are two distinct setups of the feeding quasi-optical system:

1. The quasi-optical setup shown schematically in Figure 6.13 makes no use of any beam-focusing elements. The LO feedhorn points directly into the vacuum window of the cryostat and the detector behind it, as shown in Figure 6.12. Optionally, a polarising wire grid can be placed between the LO and the vacuum window to sweep the polarisation of the signal, as shown in Figure 6.14.

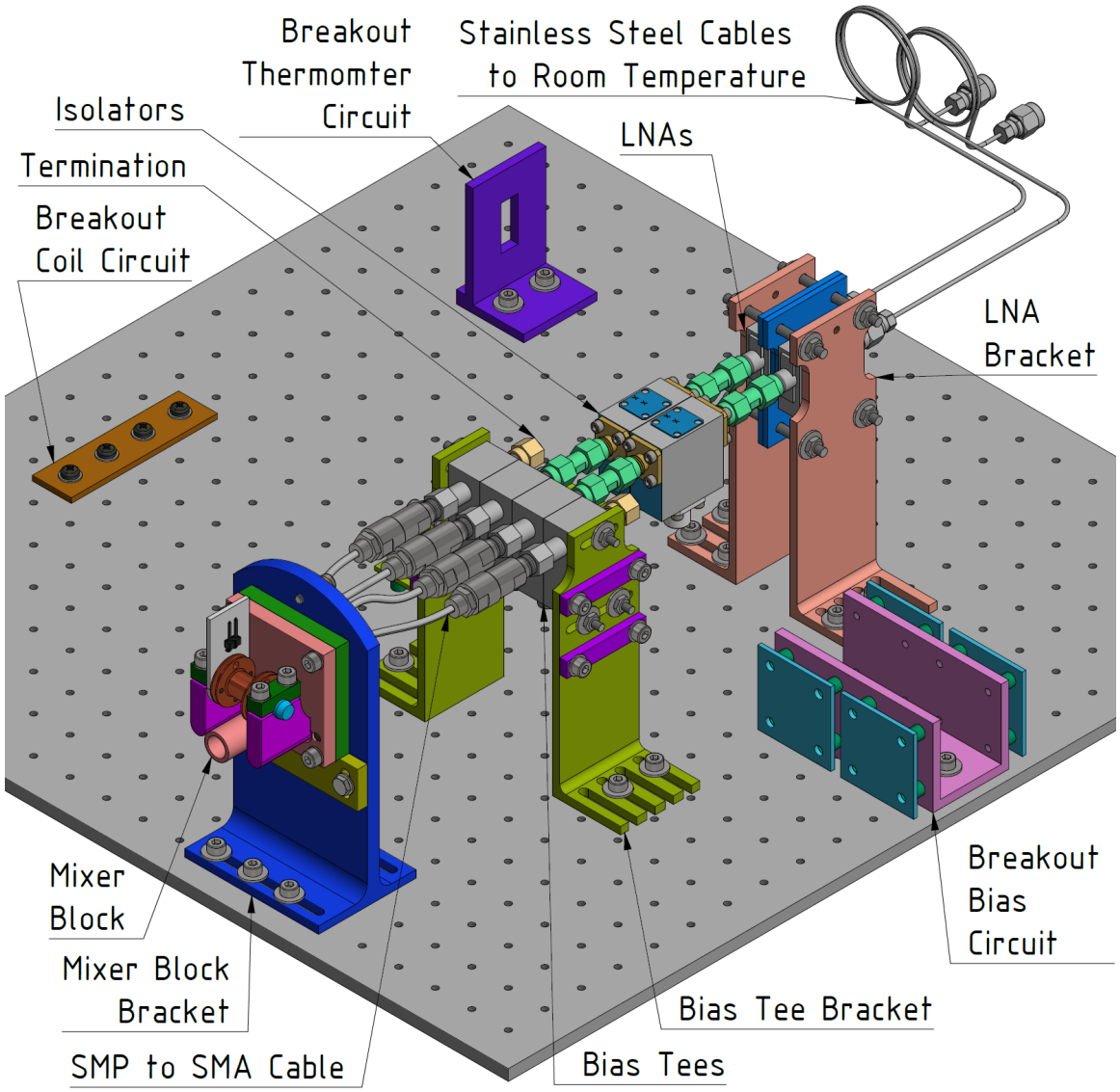


Figure 6.9: The cryogenic receiver test system setup comprises the mixer block and the IF chain, which includes bias tees, isolators and LNAs. The bias tees provide the DC bias for the SIS junctions, and the LNAs amplify the IF signal connecting to room-temperature electronics. The isolators between the bias tees and the LNAs absorb reflected power and avoid the generation of standing waves, which may deteriorate the performance of the receiver.

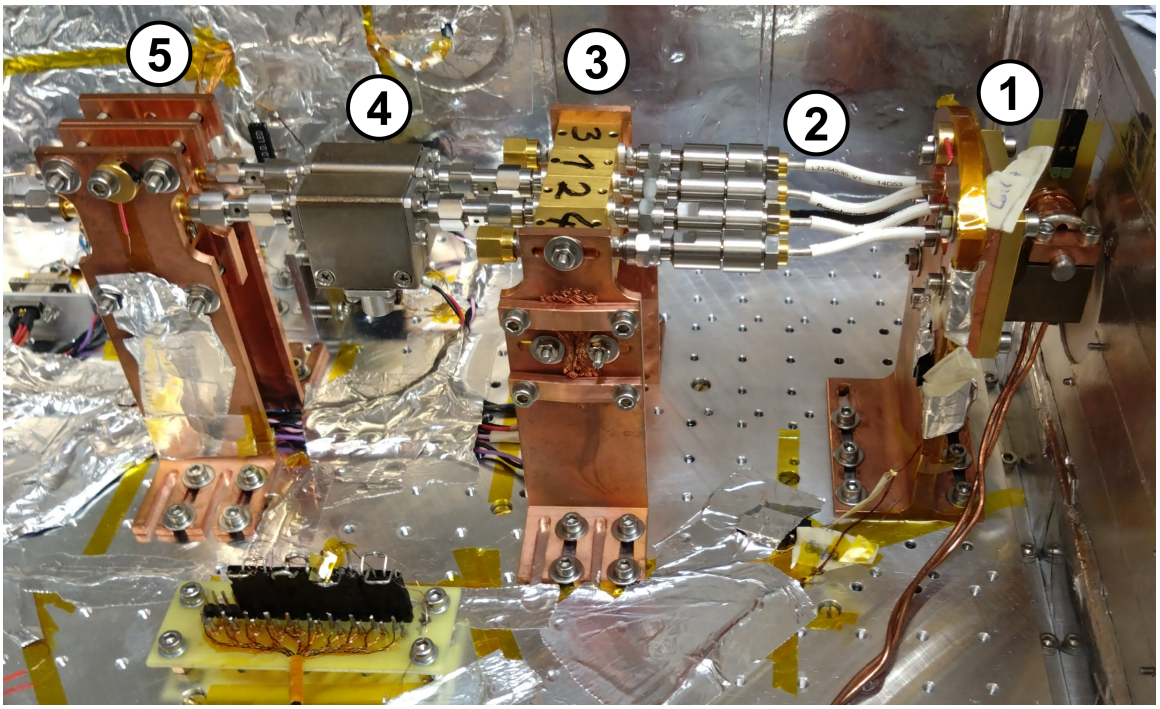


Figure 6.10: The cryogenic receiver test system setup. The receiver (1) is connected via four SMP-to-SMA cables (2) to four bias tees (3). The outer two bias tees are terminated as they connect to Δ twin junctions, and the inner two bias tees connect via two isolators (4) and LNAs (5) to room temperature.

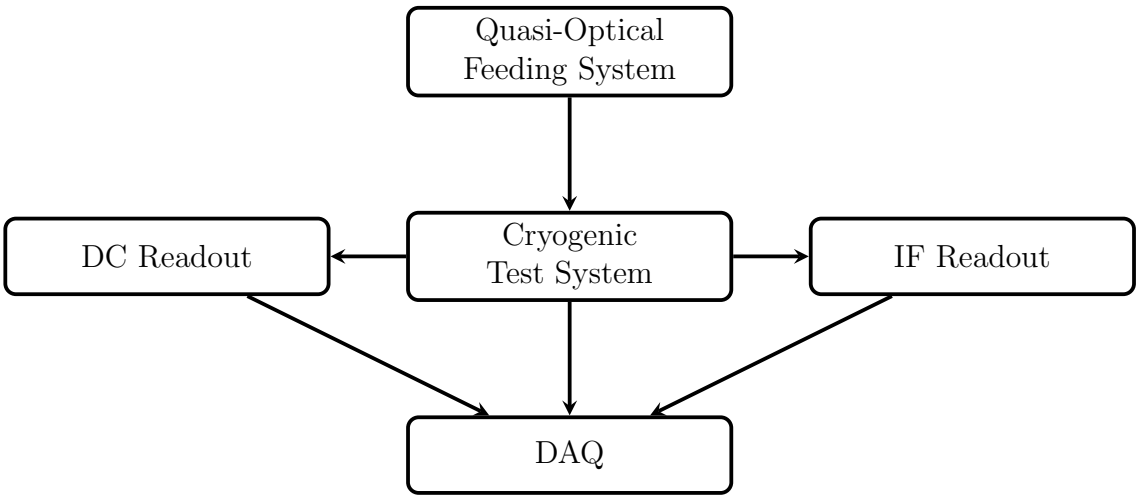


Figure 6.11: An overview of the experimental system.

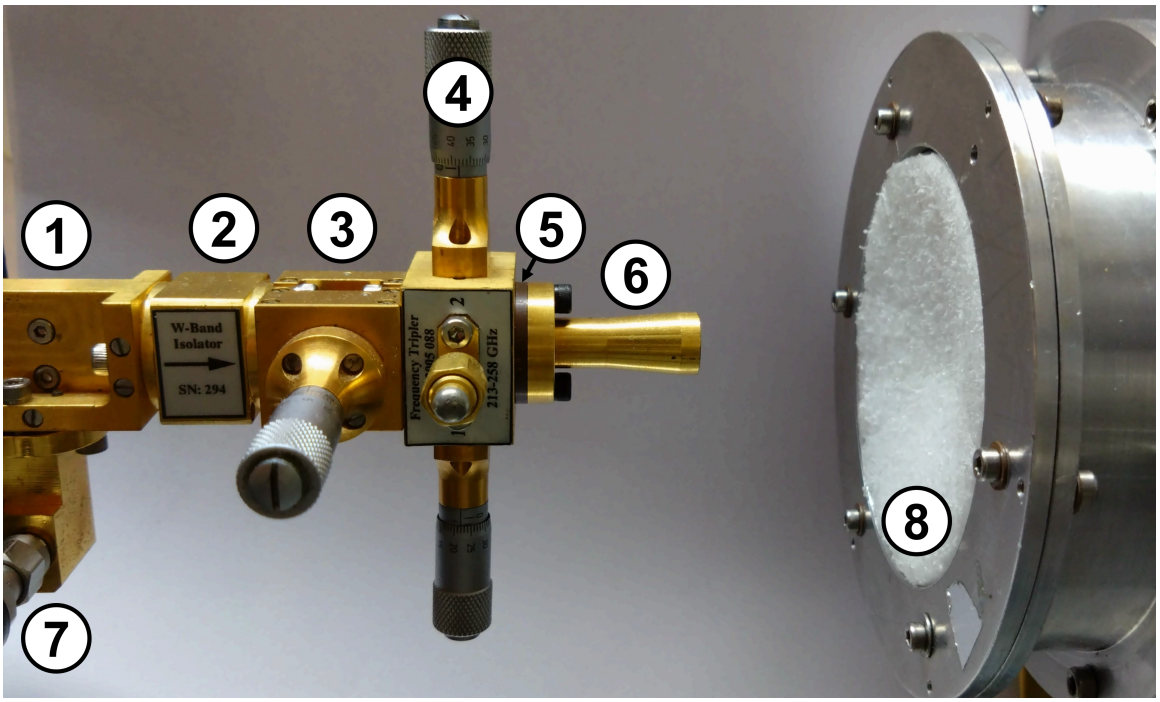


Figure 6.12: The LO consists of a Gunn diode connected to a waveguide coupler (1), an isolator (2), an attenuator (3), a frequency tripler (4), an adaptor from a rectangular-to-circular waveguide (5) and a feedhorn (6). The frequency emitted at the not-shown Gunn diode is manually adjusted, and the actual frequency is measured through the waveguide coupler connection (7) and a frequency counter. The LO faces the cryostat window (8).

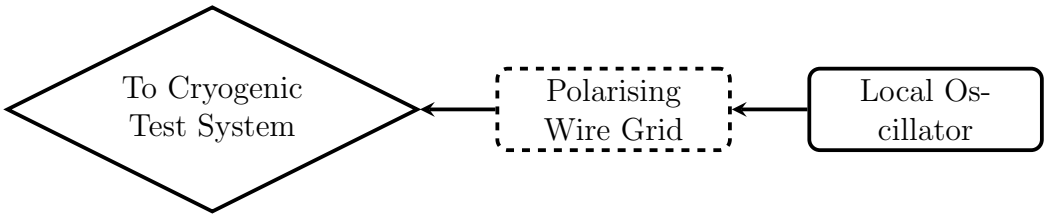


Figure 6.13: The setup schematic for direct LO illumination of the receiver. The polarising wire grid is optional.

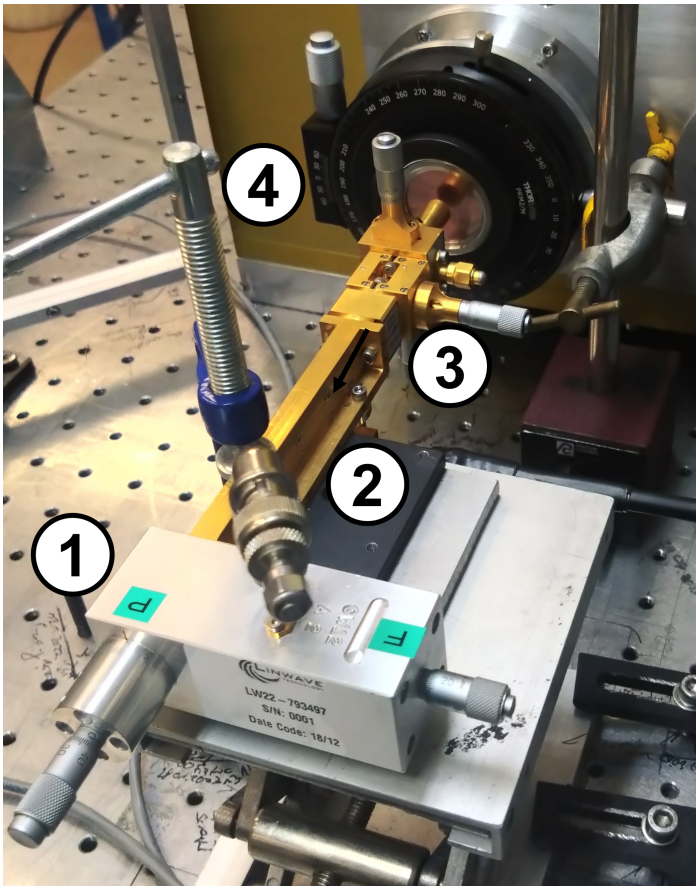


Figure 6.14: The quasi-optical setup directly illuminating the receiver with a polarised LO signal. The Gunn diode cavity (1) connects directly to the waveguide coupler (2), connected to the LO assembly (3), as shown in detail in Figure 6.12. The polarising wire grid (4) is mounted in a manual rotary mount.

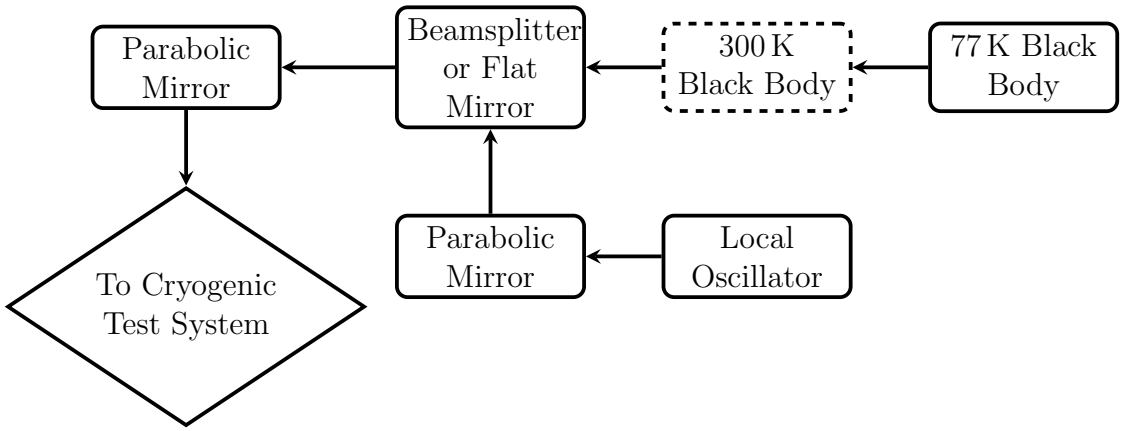


Figure 6.15: Schematic of the beam-focusing quasi-optical setup. The 300 K black body in the dashed box is used as an option to block the 77 K black body radiation.

2. The focusing quasi-optical setup shown schematically in Figure 6.15 consists of two focusing mirrors. In addition, a flat mirror is used to allow for a compact setup. Black-body radiation from an Eccosorb JCS-9 flexible absorber silicone rubber sheet in liquid nitrogen at 77 K or room temperature at 293 K can be introduced by replacing the flat mirror with a Mylar beamsplitter, as shown in Figure 6.16. The mirrors are mounted on micrometre-controlled rotation stages, and all optical components are controlled manually. The DAQ unit senses if a 77 K or 293 K Eccosorb sheet faces the Mylar beamsplitter with a switch.

Cryogenic Test System: The cryogenic test system is shown schematically in Figure 6.17, containing several auxiliary components to operate the cryogenic receiver discussed in Section 6.4. The signal from the quasi-optical system at room temperature is fed into the cryostat via a window in the vacuum chamber and an infrared filter at the 77 K radiation shield of the cryostat. Several components and connections are in the cryostat in addition to the previously described IF circuit elements:

1. The temperatures in the cryostat are monitored with four thermometers on the 77 K radiation shield, the 4 K cold plate, the mixer block and the LNA bracket. The diode thermometers connect in a 4-wire measurement configuration to a Lake Shore Cryogenics temperature monitor. The Lake Shore Cryogenics temperature monitor has the calibration files for the individual thermometers and converts the measured voltage into the displayed temperature.
2. The coil on the receiver block connects to room temperature and a constant current source. This current is controlled and monitored manually.

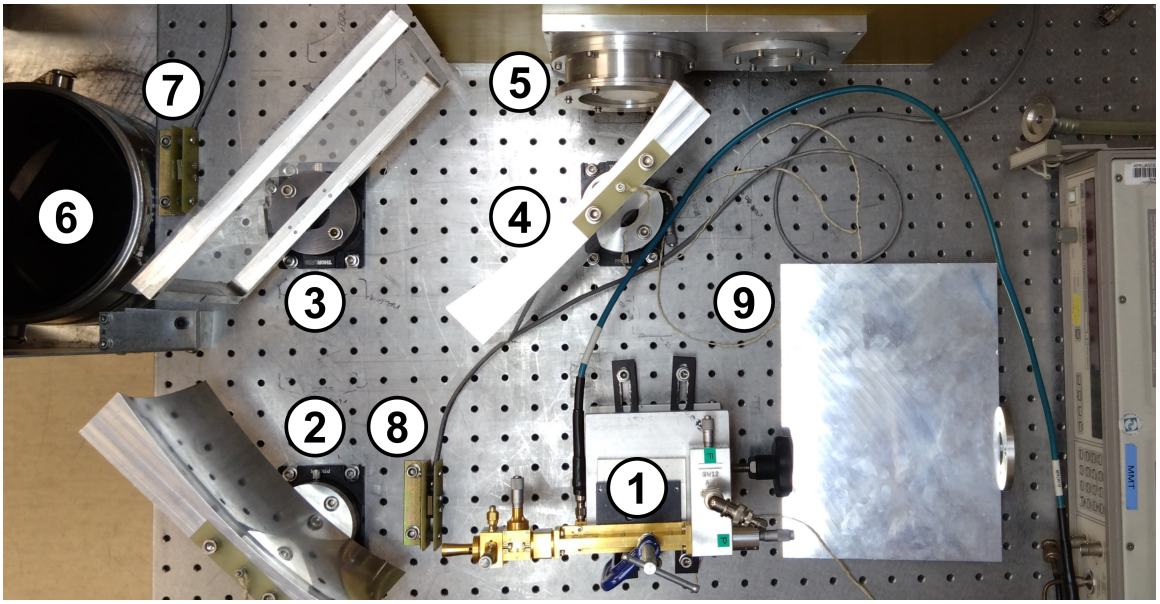


Figure 6.16: The beam-focusing quasi-optical setup. The beam from the LO source (1) is focused on the first mirror (2) and is reflected from the beamsplitter (3) to the second mirror (4), which focuses the beam to the receiver within the cryostat (5). The beamsplitter is used to couple thermal black body radiation from Eccosorb in a nitrogen bath (6) or from Eccosorb at 300 K slotted into a first switch (7). A second switch (8) is used to sense if the LO source is blocked by the flat mirror (9). Alternatively, the flat mirror can replace the beamsplitter.

3. The CITCRYO LNAs connect similarly to a manual supply unit at room temperature. The parameters for each LNA are manually adjusted according to the datasheet and not altered.
4. The DC connections of the bias tees lead to a breakout board at the 4 K stage, at which a voltage-divider setup reduces the drive voltage to the voltage at the SIS junctions and a 4-wire measurement connection that leads to room temperature.

DC Readout The DC readout at room temperature is shown schematically in Figure 6.18. The 4-wires determining the voltage and current at each bias tee in the cryostat are preamplified directly at the cryostat. The preamplifier allows for a manual offset correction for each measurement. The pre-amplified signals are then connected to a 4-channel bias module with the corresponding drive unit. The measured voltage and current of each channel are again amplified and fed via BNC cables into a DAQ module interfacing the computer. The drive voltage of each channel is either an independently set constant voltage or follows a common sweep signal controlled by the computer, generated by the DAQ unit and fed into the 4-channel bias module. The drive voltage sent into the cryogenic test system is larger than at the SIS junction because a voltage divider connects the SIS junction in the cryostat.

IF Readout The IF signals of two channels are amplified with the LNAs in the cryostat and then connected to hermetic connectors on the vacuum chamber via stainless steel coaxial cables to limit the thermal load on the 4 K stage. The signal is then connected to one of two identical IF units, shown in Figure 6.19, each comprising two LNAs, a zero-bias diode and the required auxiliary DC electronics. The IF unit is modular so that the inputs and outputs of the LNAs and zero-bias Schottky detector diode are accessible via SMA connectors on the outside of the unit. Thus, the IF unit can be used for two distinct measurements, shown schematically in Figure 6.20:

1. The IF spectrum is recorded by bridging the output of the first to the input of the second LNA and by connecting the output of the second LNA to an Anritsu 9 kHz to 21.2 GHz spectrum analyser. The spectrum analyser is connected to the computer via a GPIB to USB cable and controlled with a Python script.
2. The absolute power can be measured by connecting the output of the second LNA to the Atlantic Microwave zero-bias Schottky detector diode input. As the zero-bias Schottky detector diode converts the incident power within its specified frequency range from 10 MHz to 12.4 GHz to a voltage, this setup

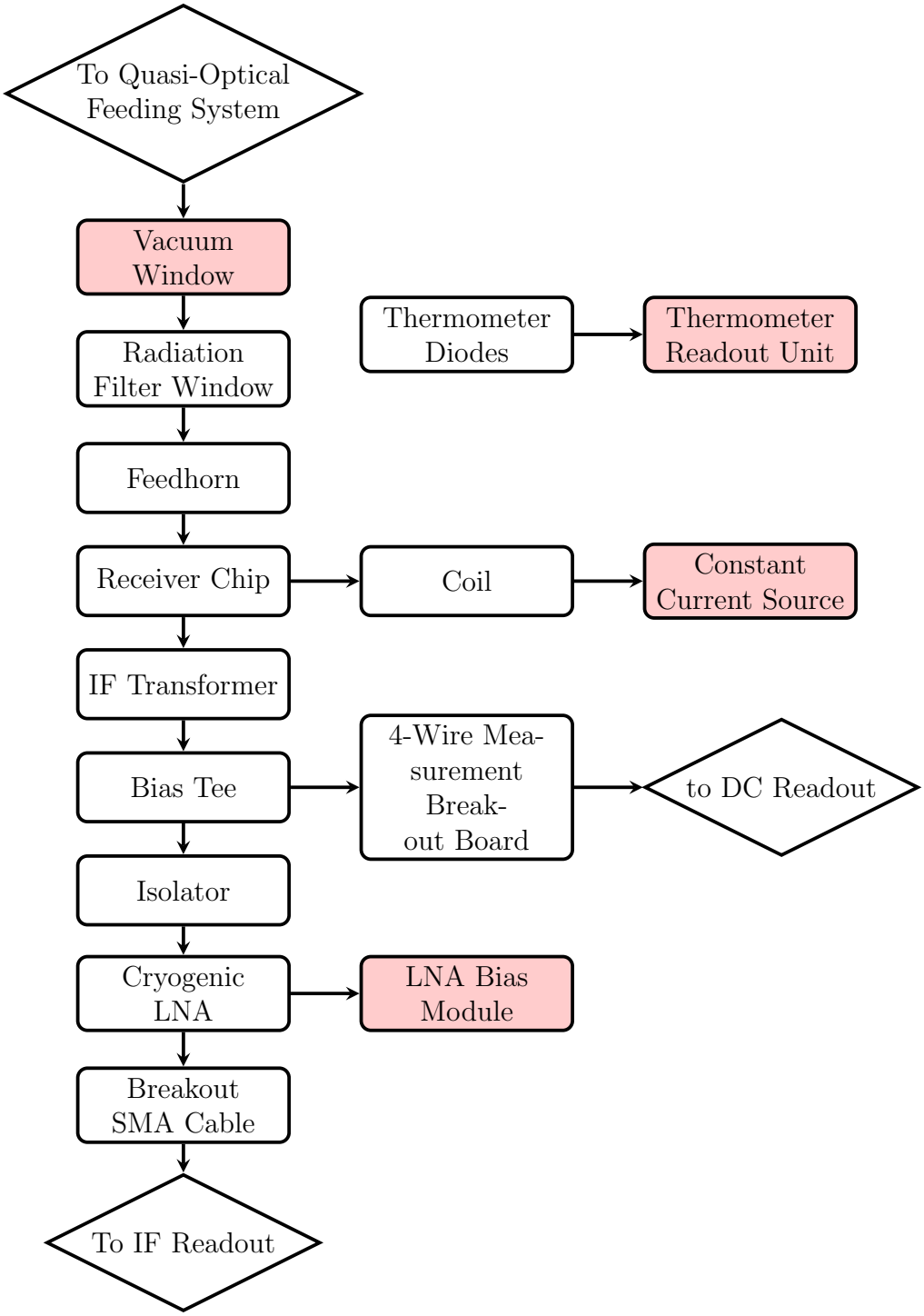


Figure 6.17: A schematic of the cryogenic test system. The components in red are at room temperature and are left in this schematic for convenience.

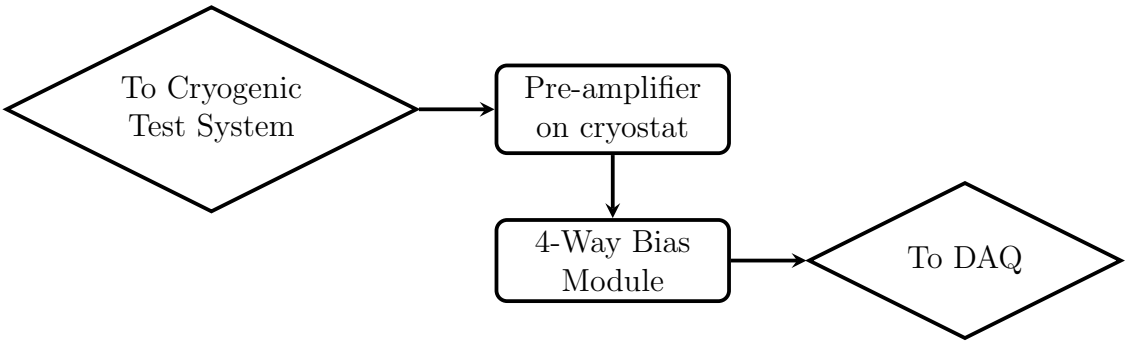


Figure 6.18: Schematic of the DC readout.

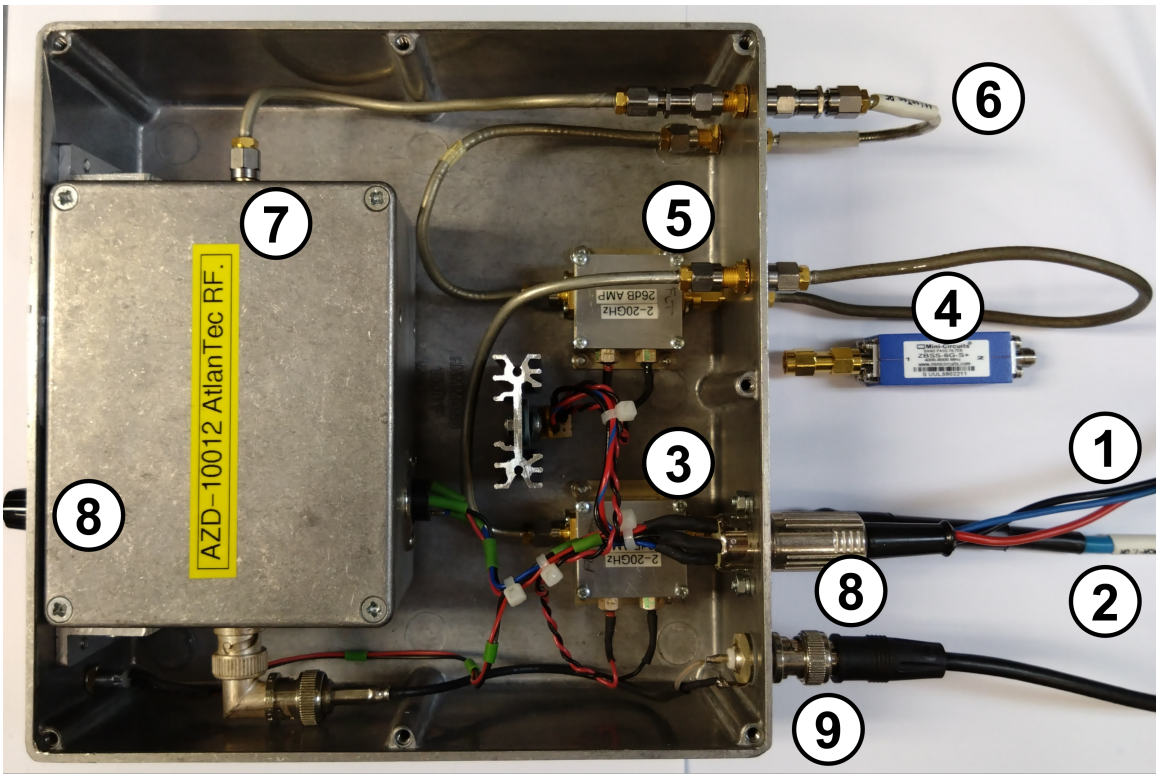


Figure 6.19: The IF readout unit. Underneath the DC power supply for the unit (1) is the IF signal connection (2), which directly connects to the first LNA (3). The IF signal is then fed to the jumper SMA outside the unit (4), where the shown BPF can be connected, before feeding the IF signal in the second LNA (5). The amplified signal is then connected to the outside of the IF unit (6), which is bridged to the input of the zero-bias diode (7) in the shown configuration. The operational amplifier in the enclosed zero-bias diode can be offset-controlled via the potentiometer on the front panel (8), and the amplified IF-power equivalent voltage can be connected at a BNC connector (9).

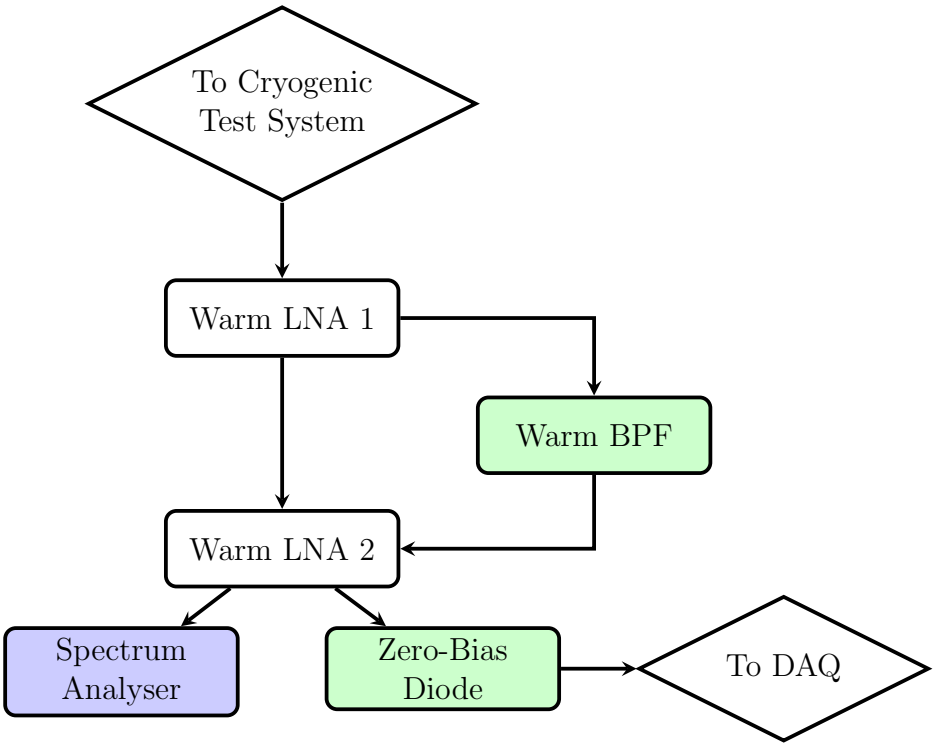


Figure 6.20: Schematic of the IF readout. The two options are colour-coded in green and blue.

typically uses a 4 GHz to 6 GHz or 8 GHz BPF between the output of the first and input of the second LNA to define the detector bandwidth. The output of the zero-bias Schottky detector diode is connected via an operational amplifier to a BNC socket that connects to the ADC unit. A helipot potentiometer allows correcting for voltage offsets.

Data Acquisition (DAQ) The National Instruments (NI) BNC-2090A breakout unit is connected via a SCSI connection to the NI DAQ device slotted in the motherboard of the computer. A Labview program controls the breakout unit that uses eleven BNC connectors for the current and voltage measurement inputs of the four channels, two inputs from the zero-bias diodes and one output generating the bias sweep, as shown in Figure 6.21. The DAQ unit uses two digital inputs to sense blocked quasi-optical paths, e.g. a thermal load at room temperature in front of the thermal load in the nitrogen bath. Another six digital inputs are connected to lever switches, easing the experiment, e.g. by initiating the recording of a dataset.

The Lake Shore Cryogenics unit monitors the four thermometers on the 77 K radiation shield, the 4 K cold plate, the mixer block and the LNA bracket. A Python

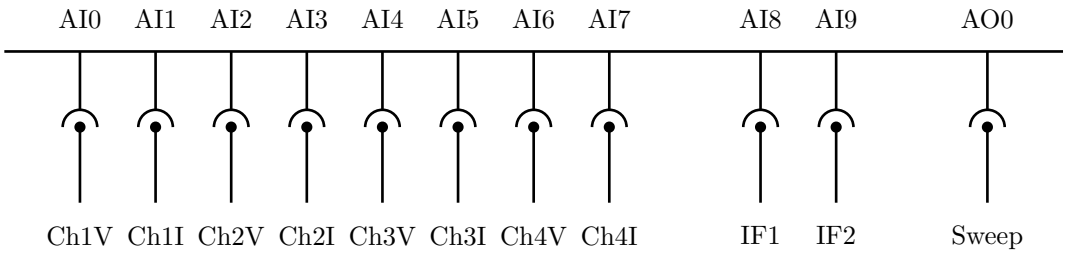


Figure 6.21: The analogue inputs of the DAQ. 'AI' and 'AO' are the analogue input and output of the DAQ unit. 'Ch' stands for channel, followed by the channel number, and 'V' or 'I' represents voltage and current. IF1 and IF2 are connected to the zero-bias diode output. 'Sweep' is the drive voltage connected to the 4-way bias module.

script records the temperatures via an RS232 connection to the control computer.

6.6 Experimental Sequence

The usage of a system relying on liquid cryogenics requires a well-prepared experiment plan for each cooldown due to the limited time at 4 K. We abstained from topping up the helium during a cooldown due to the hazard of introducing gasses that could clog the helium exhaust line. Instead, all wires have been thoroughly heat-sunked with aluminium tape on the 77 K and 4 K stages with a generous length between the heat sinks, reducing the thermal gradient. Thus, we could reduce the thermal load at the 4 K stage to a level at which the time at 4 K exceeded 6 hours.

These 6 hours of experiment time are part of an experimental sequence taking at least two days for which the temperatures of the individual thermometer readings in the cryostat are shown in Figure 6.22: First, the vacuum chamber is evacuated with a rotary and turbo-molecular pump below 1 mPa. Then, the N_2 tank in the cryostat connected to the radiation shield is filled with liquid N_2. Subsequently, the cryostat tank connected to the 4 K cold plate with the cryogenic receiver is filled with liquid N_2. This pre-cooling typically requires several hours and a refill of both tanks at the end of the day. The refill lasts until the morning of the second day, when the outer tank is refilled with liquid N_2. The liquid N_2 in the inner tank connected to the cryogenic receiver is removed by pressurising the tank with N_2 gas and decanting the liquid through a transfer line. Then, liquid He is decanted from a dewar into the inner tank, where the excess pressure in the dewar is created from evaporating liquid He. The decanting process typically takes around 2 hours, within which the experiment is prepared and the vacuum pump is removed from the cryostat. Once

the helium dewar is disconnected from the cryostat, the experiments are carried out until the temperature at the cold plate rises.

6.7 Summary

In this chapter, we described the design of the receiver block and the receiver test system. First, we described the design of a single pixel and then its extension into a 4-pixel receiver. We describe in detail the procedure of preparing the receiver, e.g. the mounting of the receiver chip in the receiver block. In the fourth section, we present the design of the linear arrangement of the IF signal processing components in the cryostat behind the receiver that allows for extensions into a focal plane array. We then give an overview of the experimental system separated into five subsystems: the quasi-optical feeding system, the cryogenic test system, the DC readout, the IF readout and the DAQ system. In the final section, we briefly describe the sequence of tasks required for an experiment.

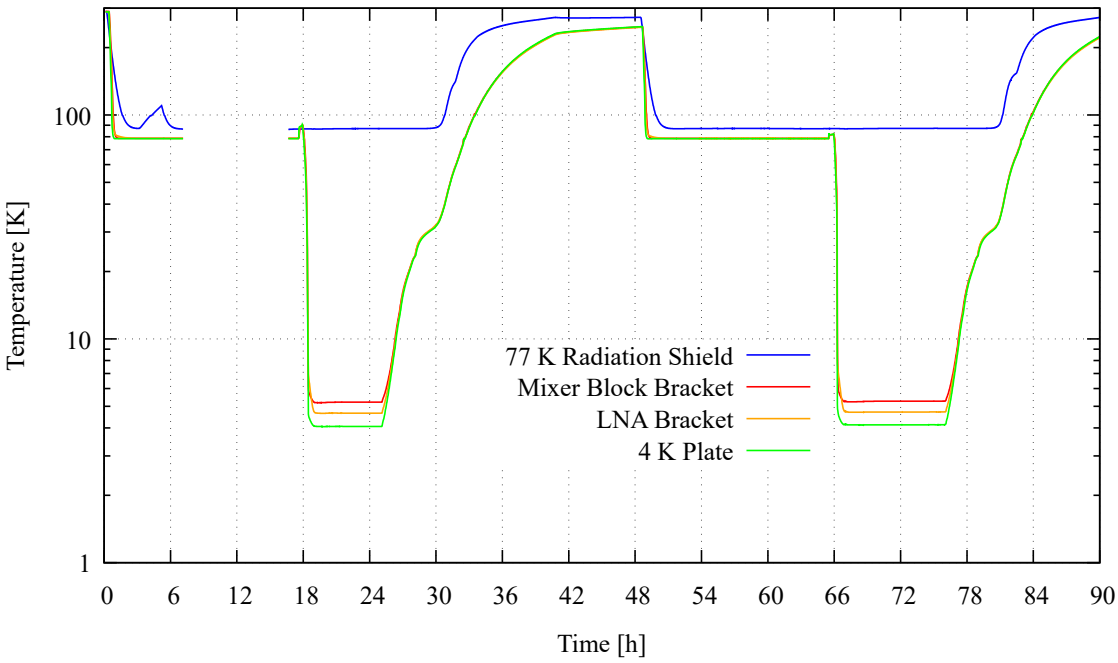


Figure 6.22: The temperatures in the cryostat for two consecutive cooldowns. The recording starts with the pre-cooling of both stages. The temperature on the 77 K stage after 4 h increases because the liquid N_2 evaporated off, and it was not refilled for approximately 1.5 h. At 18 h, the temperature of the 4 K stage first increases due to the removal of liquid N_2 from the inner tank. The empty tank was then filled with liquid He, which caused the temperature to drop to 4 K. After approximately 6 hours of experiments, the temperature increased as the liquid He evaporated. A second pre-cooling phase starts at 48 h, and the second experiment starts at 66 h.

Chapter 7

Experimental Investigation

Chapter published shortened: J. Wenninger, F. Boussaha, C. Chaumont, B. K. Tan, and G. Yassin, "Preliminary Characterisation of a Compact 240 GHz SIS Dual-Polarisation Receiver for Large Array Applications," in *32nd IEEE International Symposium on Space Terahertz Technology*, 2022.

The setup for the experimental investigation described in the previous section is used to test the fabricated receiver chips. Faouzi Boussaha and Christine Chaumont fabricated the devices in the cleanroom facilities at the Observatoire de Paris, and we performed DC screening tests before employing samples in the described setup.

In this chapter, we describe the experimental tests performed on the receiver. As we shall see, the performance of the receiver was degraded by fabrication difficulties of the mixer chip. We first describe in detail the DC characterisation and the modifications to the fabrication and design to improve the fabrication yield. The following optical coupling characterisation shows power measurements of coupling the LO signal to the SIS junctions. We also investigate the response when polarising the LO signal. Finally, we present our thorough investigation of the causes of the observed weak coupling observed.

7.1 DC Characterisation

After dicing the wafer and before thinning the receiver substrate to the thickness required for RF testing, we conducted DC screening tests. The DC characterisation aims to test the SIS junction immediately after fabrication, in particular, the fabrication yield, gap voltage, critical current and normal resistance. As this test involves

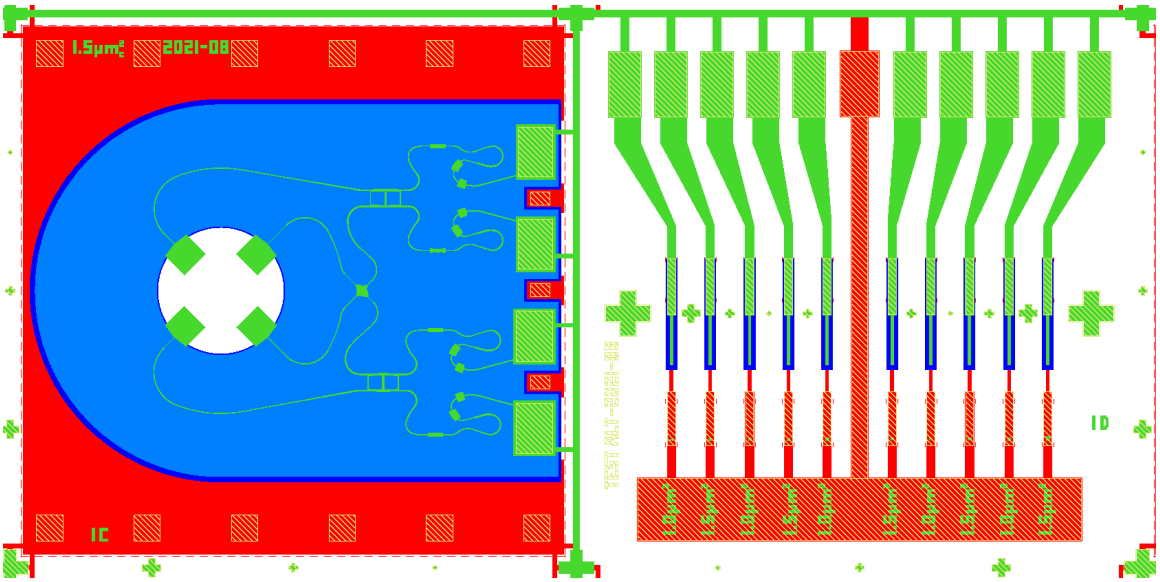


Figure 7.1: The mask set of a receiver device on the left and a test device on the right. The first mask for the trilayer is in red, and the second mask for etching the trilayer and depositing the first SiO layer is in dark blue. The second SiO layer is deposited with the light blue mask. The wiring layer is shown in green, and the gold finish is shown in hashed yellow.

only DC resistance measurements at 300 K and 4 K, the devices are not thinned at this step and are only superglued and bonded to an FR-4 PCB. This PCB is dipped into liquid He to obtain the 4 K data. Although the PCB is connected via 20 independent DC connections to the readout system, only a single chip with either four or ten SIS circuits is tested at a time to minimise the risk of device destruction due to ESD. Only receiver chips of batch 8 were characterised with two receivers on a single sample holder.

A subset of thinned devices underwent another iteration of DC characterisation to rule out performance degradation of the SIS junctions due to the thinning process. The response of the devices remained unchanged, and only data of the devices before thinning is included in the following DC characterisation data.

The mask set contains four receiver variations with either 1.0 µm^2 or 1.5 µm^2 twin junction devices and four test structures with ten circuits of alternating 1.0 µm^2 and 1.5 µm^2 SIS junctions connected to a common ground. The test structures accelerate the DC characterisation and allow to test individual junctions instead of twin junction circuits. Both the mask sets for a receiver and a test device are shown in Figure 7.1.

7.1.1 Original Receiver Mask Set

Figure 7.2 summarises all batches of receiver devices of the original mask set for which all fabrication steps were successfully completed. The 300 K resistance is in Ω due to the high resistance of the superconductor wiring connecting the junction. From the data available, we find that circuits with a 300 K resistance between 40 Ω and 160 Ω typically show gap voltage characteristics at 4 K. This resistance range is rather wide due to the different on-chip Nb wiring: The test structures in Figure 7.1 have much wider traces, not narrower than 20 µm and partially covered with gold while the twin junctions on the receiver devices are connected via a 5 µm wide and 600 µm long microstrip. Once superconducting, the measured resistance is normalised by the total junction area because the resistance of the wiring connection is negligible compared to the normal resistance of the SIS junction. The total junction area in the circuit is used for the area normalisations, or in other words, twice the junction area in receiver devices with twin junction circuits, to allow for comparison with the test devices. We find gap voltage characteristics with an area normalised 4 K resistance between 20 Ωµm^2 and 50 Ωµm^2, depending on the circuit configuration.

As the histogram of the 4 K resistance on the right in Figure 7.2 shows, a significant number of circuits turn open when cooled. Furthermore, we observed that the 300 K resistance changed for several samples with thermal cycling. The 300 K resistances of batches 1 and 5 show a reasonable spread in the histogram at the top of Figure 7.2, peaking between 100 Ω and 200 Ω for batch 1 and between 50 Ω and 100 Ω for batch 5. The resistances at 4 K spread over several orders of magnitude. The batch 1 devices with 4 K resistances between 10 Ωµm^2 and 30 Ωµm^2 show gap voltage characteristics typical to an SIS junction. However, the yield of devices is not sufficient, and the variation between the DC responses exceeds acceptable tolerances. The batch 5 devices show characteristics of superconductors but no gap voltage characteristic.

7.1.2 Test Device Mask Set

Our fabrication directly follows a recipe parametrisation for another project. This preceding parametrisation has a mask set with 16 test devices and 10 individual circuits. These ten circuits on a device either contain identically sized junctions or two times five junctions of the sizes: 1.0 µm^2, 1.5 µm^2, 3.0 µm^2, 5.0 µm^2 or 10.0 µm^2.

We returned three times to the mask set with 16 sectors used in the fabrication parametrisation preceding our fabrication to rule out unnoticed changes in the fabrication setup, especially because of observed photoresist burning. The results of these

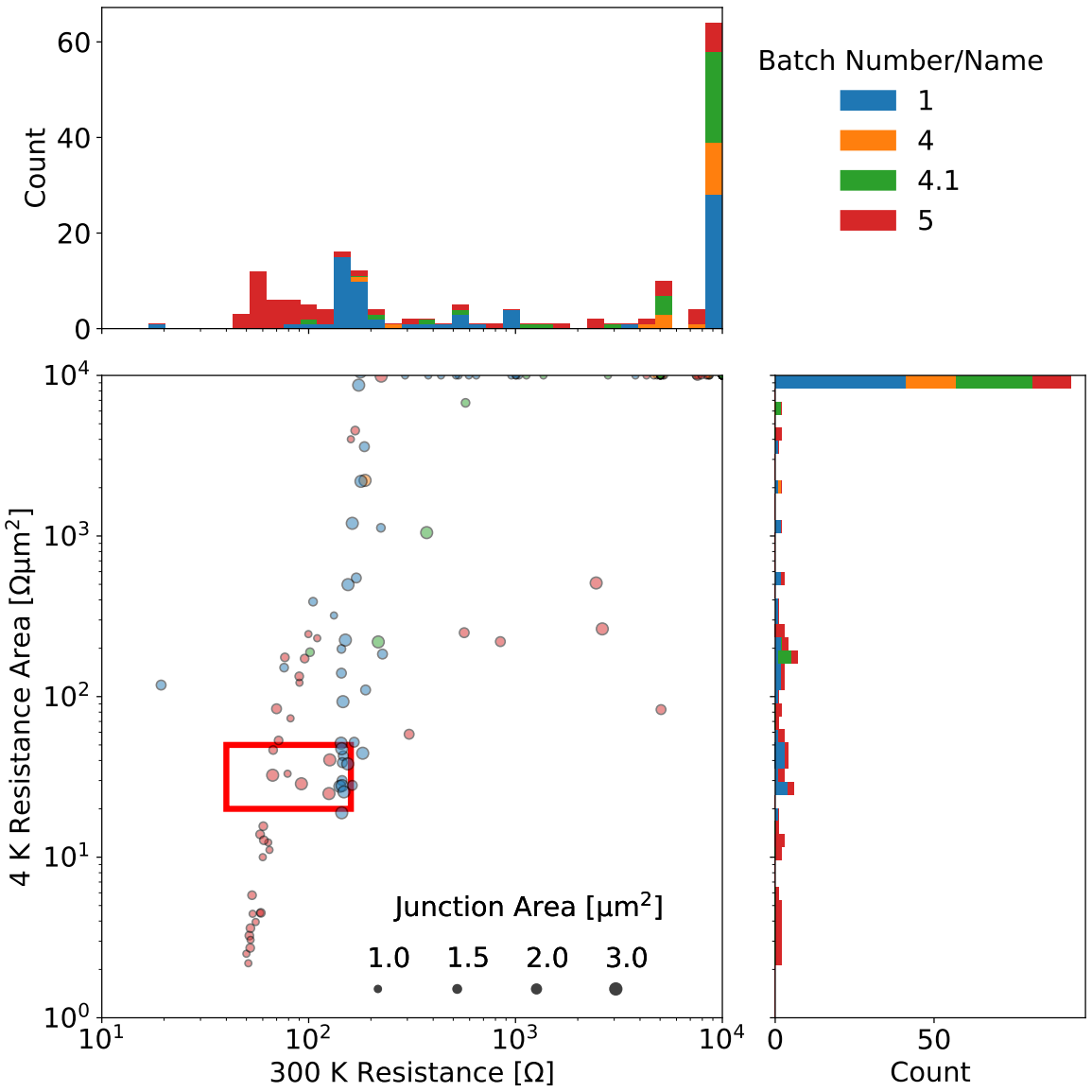


Figure 7.2: DC characterisation results for dual-polarisation receiver devices fabricated with the original mask set. The main panel shows the 300 K resistance and 4 K resistance area for the tested devices, where the point size represents the junction area and the colour represents the batch number/name. Circuits in the red rectangle typically show gap voltage characteristics. Above the main panel is a histogram for the 300 K resistance, and on the right is a histogram for the 4 K resistance area. Open circuits are included in the $10^4\,\Omega$ and $10^4\,\Omega\mu m^2$ bins. The junction area is doubled to calculate the resistance area in twin junction circuits.

batches shown in Figure 7.3 are more concise than with the receiver mask set, and the yield is significantly better. The deviation from the desired DC performance is observed increasingly with decreasing junction area. The samples with 300 K resistances between 40 Ω and 100 Ω have consistent 4 K resistances between 20 Ωμm^2 and 40 Ωμm^2.

7.1.3 Fabrication and Design Modifications

The DC screening results of the first fabricated batches with the original receiver mask set showed a low fabrication yield, which is too small for our devices, requiring eight functioning SIS junctions for each mixer chip. Consequently, we reviewed the recipe by fabricating the separate test device batches with 1.0 μm^2 to 10 μm^2 SIS junctions, and we found evidence that the large ground layer of our receiver causes issues during the reactive ion etching (RIE) process. The fabrication recipe and processes are summarised in Appendix A.4. We suspect that the SF_6 etching of the trilayer might have polluted the photoresist defining the SIS junction area, preventing a clean lift-off. In the deposition of the wiring layer, these photoresist remnants were then sandwiched between the SIS top electrode and the wiring layer, causing a resistive response.

Accordingly, we modified the fabrication process described in Appendix A.4 by 1) increasing the SIS junction area and 2) reducing the area etched to define the SIS junctions. The mask of the second fabrication step now defines larger SIS junction areas, 2.0 μm^2, 3.0 μm^2, 4.0 μm^2 or 5.0 μm^2, but only exposes the trilayer at a 10 μm^2 square around the SIS junctions to the RIE and subsequent SiO deposition, as shown in Figure 7.4. Hence, the ground layer at most of the receiver chip consists of the trilayer, which is covered with 200 nm SiO and a 6 μm^2 square around the SIS junctions in the third fabrication step. An additional fabrication step, Step 3.5, is inserted before the fourth step of Table 7.1 to deposit another 200 nm SiO with a 14 μm^2 square around the SIS junctions to achieve 400 nm SiO on most of the chip and, therefore, the desired characteristic impedances. With these modifications, the fabrication yield improved significantly.

Two batches were fabricated with the recipe modifications. Figure 7.5 shows that batch 7 has mostly open circuits due to an issue with the vacuum pump during the RIE. Batch 8 has a yield of 40% with little scatter. The distinct peaks of the 300 K resistance histogram at 40 Ω correspond to test devices and at 100 Ω with receiver devices due to the different wiring connections of the warm superconductor. The two peaks in the 300 K resistance histogram fall both into the 30 Ωμm^2 bin of the 4 K resistance area histogram because we account for the total junction area of a circuit

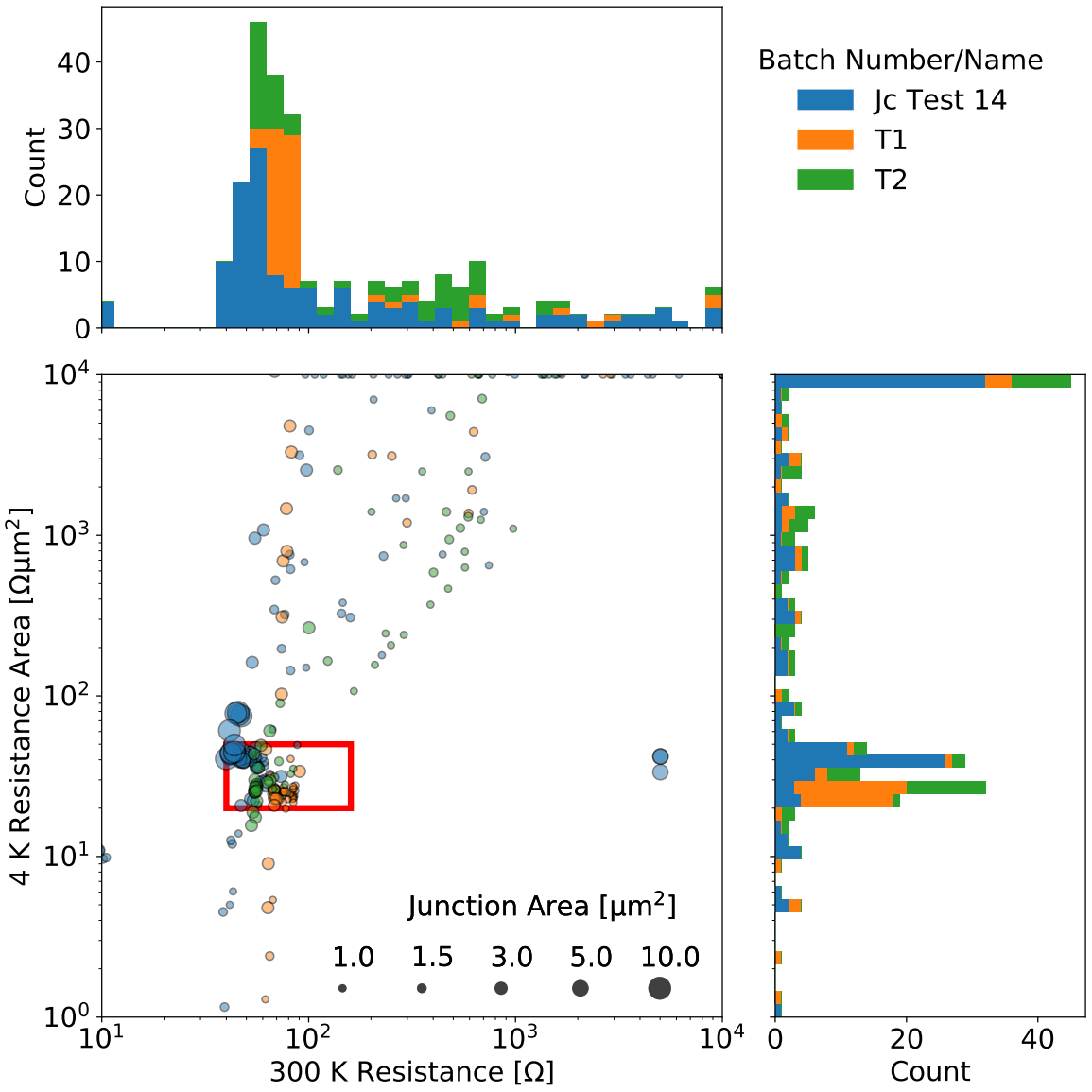


Figure 7.3: DC characterisation results for test mask devices fabricated during dual-polarisation receiver tests. The main panel shows the 300 K resistance and 4 K resistance area for the tested devices, where the point size represents the junction area and the colour represents the batch number/name. Circuits in the red rectangle typically show gap voltage characteristics. Above the main panel is a histogram for the 300 K resistance, and on the right is a histogram for the 4 K resistance area. Open circuits are included in the $10^4\,\Omega$ and $10^4\,\Omega\mu m^2$ bins.

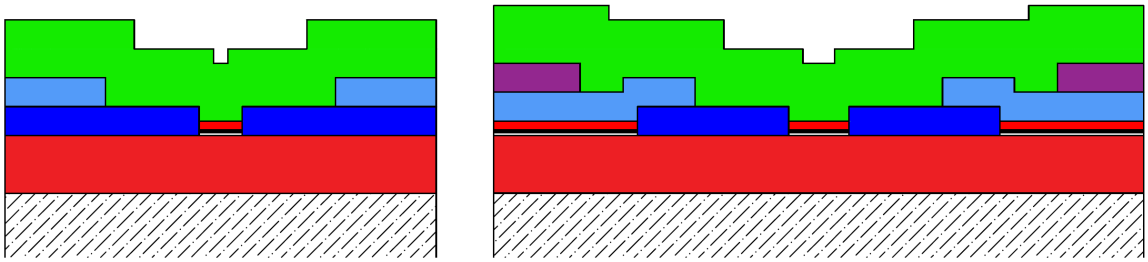


Figure 7.4: Side views of the film topology obtained with the original mask set on the left and the revised mask set on the right with larger SIS junctions and an additional SiO layer. The quartz substrate is shown hashed. The Nb of the trilayer is shown in red, which sandwiches the passivated Al in white and black. The first SiO layer is deposited where the trilayer has been removed, shown as dark blue. The second SiO layer is pale blue, and the third SiO layer is purple. The wiring layer Nb is shown in green.

Step	Description	Material	Thickness
1	Deposition trilayer	$Nb/AlO_x/Nb$	400/1/200 nm
2	Etching junctions from trilayer	Nb Remains	400 nm
	Deposition of first dielectric	SiO	200 nm
3	Deposition of second dielectric	SiO	200 nm
3.5	Deposition of third dielectric	SiO	200 nm
4	Deposition of wiring layer	Nb	400 nm
5	Deposition of bonding pads	Ti/Au	10/150 nm

Table 7.1: The modified 5-step planar-circuit thin-film deposition process.

for the normalisation. Thus, we can use the 300 K as a first selection criterion to identify devices for further tests and thinning.

The increased junction size inevitably affected the performance of the receiver, which was designed for much smaller 1.0 µm^2 junctions. As shown in Figure 7.6, the return loss of a signal incident at the circular waveguide is very high, but the ripples reach below –10 dB up to 240 GHz, offering us a chance to characterise the on-chip integrated circuit albeit at a reduced frequency range. In the initial design, most of the incident signal couples in the second SIS junction. Our simulation showed that the increased junction area causes the incident signal to couple mostly into the first SIS junction of the twin junction, leaving the second SIS junction with very little coupling. Although the increased junction area completely altered the tuning of the SIS junctions, the coupling of the first SIS junction offers a possibility of characterising the optical coupling of the receiver, especially at low RF frequencies. However, the simulations predict coupling undulations of 3 dB with return loss poles every 12 GHz, causing strongly varying responses in the optical coupling measurements.

7.2 Optical Coupling Characterisation

The optical coupling to the receiver was tested using the twin junction mixers as direct detectors, with an LO source directly illuminating the receiver in the cryostat behind a Zotefoam vacuum window and a Zitex infrared filter. The photon-step responses of the four twin junctions enabled us to infer the coupling efficiency of the circuit, in particular, the coupling from the circular waveguide to the microstrips at the OMT and the power-combining capabilities of the hybrid.

The first thinned device we characterised has 3 µm^2 SIS junctions and has not been screened before thinning. The corresponding IV responses and parameters are shown in Figure 7.7. The 300 K resistance test showed that the warm resistance of the Pol. 1 Δ twin junction has a resistance of 124 Ω, indicating that the twin junction device is faulty. The faulty response can be seen from the unpumped response with very low tunnelling current at the gap voltage, potentially caused by a defective SIS junction and a series resistance.

7.2.1 Power Measurement

The pumped IV responses in Figure 7.7 show the highest photon step current we could achieve at 230.4 GHz when the Gunn LO source was directly illuminating the horn. Hence, the LO should have been strong enough to saturate the IV response. We,

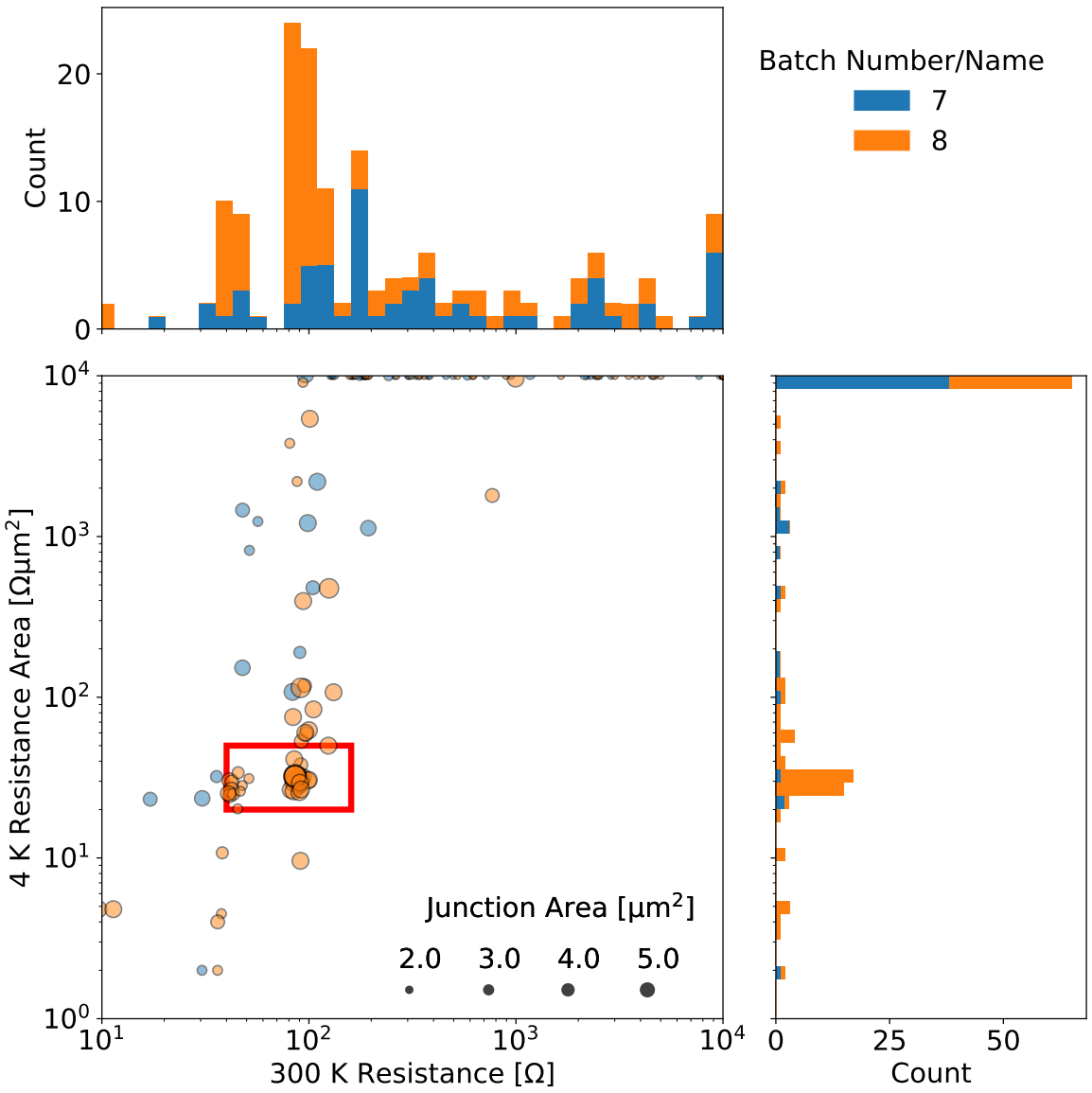


Figure 7.5: DC characterisation results for dual-polarisation receiver devices fabricated with the mask set defining larger junction areas. The main panel shows the 300 K resistance and 4 K resistance area for the tested devices, where the point size represents the junction area and the colour represents the batch number/name. Circuits in the red rectangle typically show gap voltage characteristics. Above the main panel is a histogram for the 300 K resistance, and on the right is a histogram for the 4 K resistance area. Open circuits are included in the $10^4\,\Omega$ and $10^4\,\Omega\mu m^2$ bins. The junction area is doubled to calculate the resistance area in twin junction circuits.

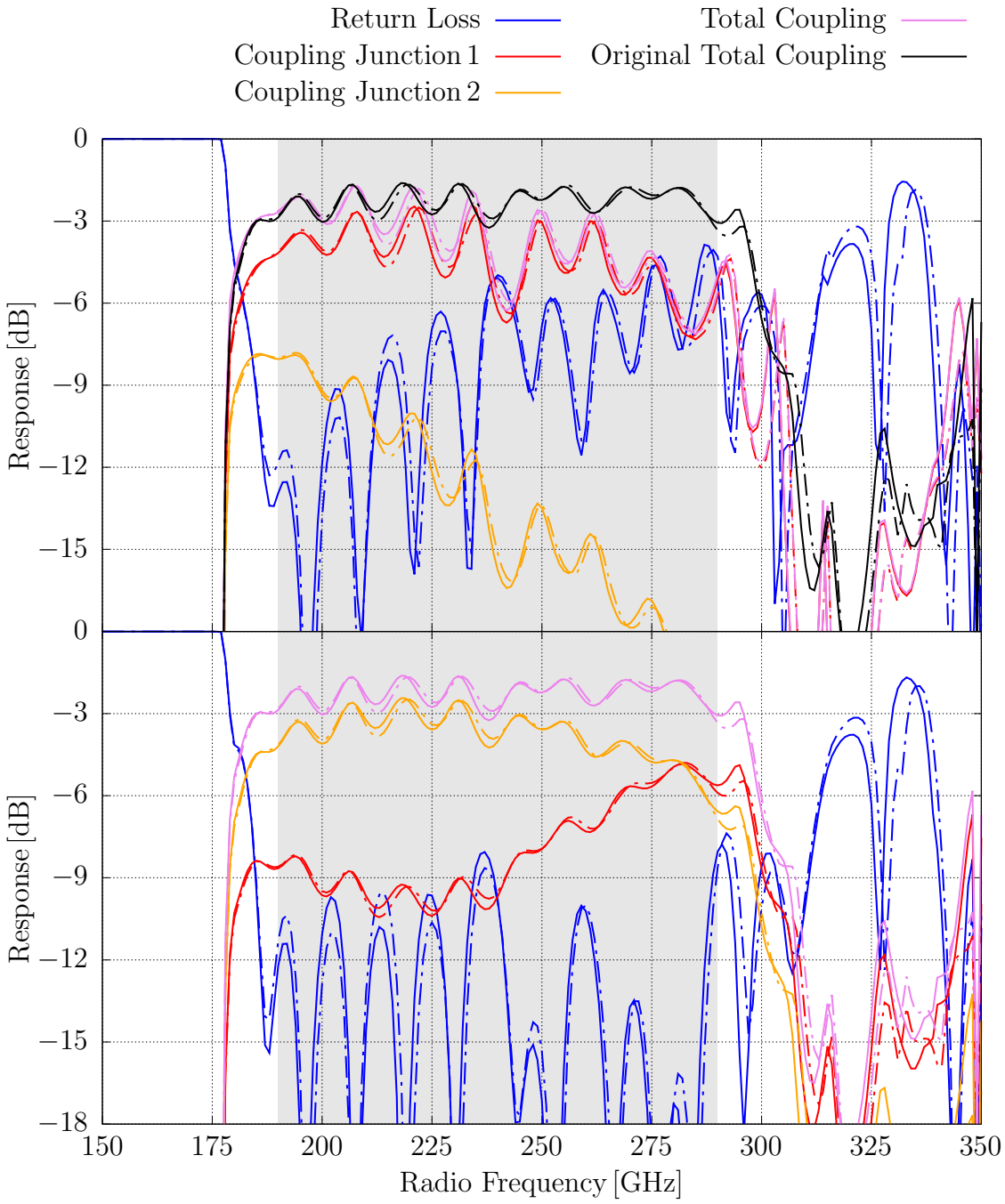


Figure 7.6: The simulated performance of the receiver chip fabricated with the revised mask set and 3.0 µm^2 SIS junctions in the upper panel and the original design in the lower panel. The Pol. 1 responses incident at the circular waveguide of the model are shown as solid lines, and Pol. 2 responses as dash-dotted lines. Total coupling denotes the sum over the two SIS junctions of a twin junction circuit, and it is also shown for the original design in the upper panel for comparison.

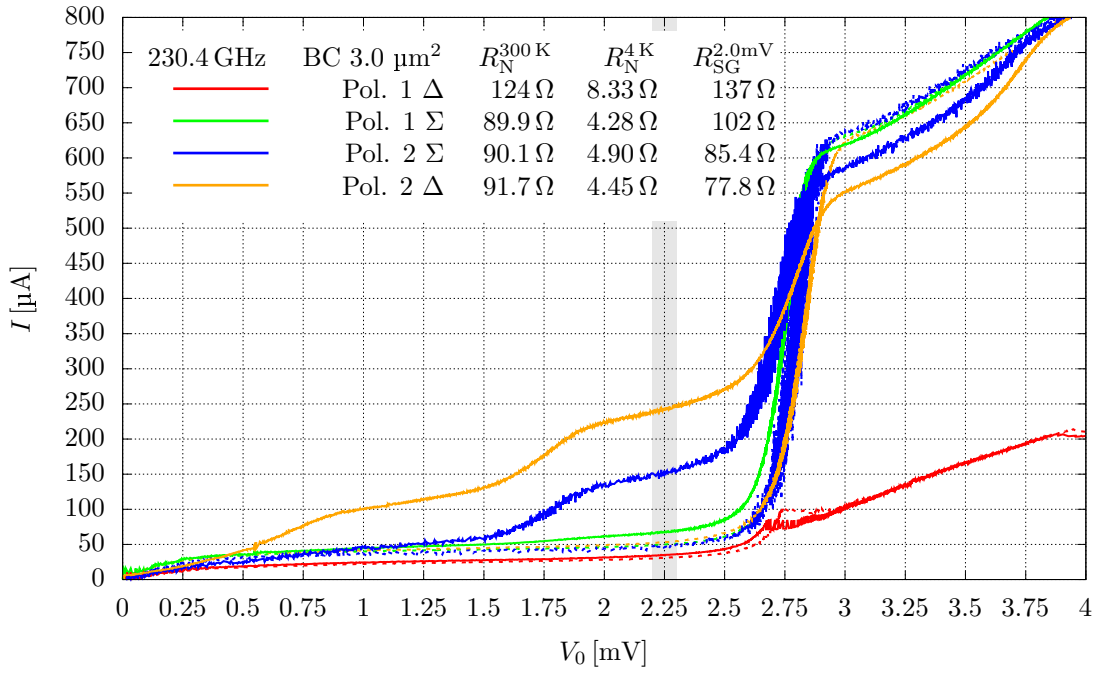


Figure 7.7: The pumped IV curves and the unpumped IV curves of the four twin junction circuits. The unpumped currents are shown as dotted lines. The legend summarises the 300 K resistance $R_N^{300\,K}$, the normal resistance at 4 K R_N^{4K} and the subgap resistance measured at 2.0 mV $R_{SG}^{2.0mV}$. The grey shaded area is the (2.25 ± 0.05) mV interval used to gauge the direct detector response to the LO signal.

therefore, conclude that the coupling of the SIS junctions to the LO source is poor, either due to faulty subcircuits or excessive losses. Furthermore, the LO couples to both twin junctions connected to the Pol. 2 hybrid, but more LO signal couples to the Δ twin junction than the Σ twin junction at 230.4 GHz, although the Δ twin junction was designed to be isolated. In contrast, both twin junctions connected to the Pol. 1 hybrid are not at all responding to the LO. Following the design, a photon step should appear in the Pol. 1 Σ twin junction, considering that it has a good unpumped IV response. However, as the Δ twin junction is defective, we can not extract information to learn if any LO signal is incident at the Pol. 1 hybrid.

Figure 7.8 shows the photon step current at a bias voltage centred at 2.25 mV as a function of LO frequencies. The data comprises two different cooldowns, a preliminary test and one cooldown designated for this frequency sweep, where most data points were recorded by sweeping the LO frequency. Due to the described fabrication difficulties, the size of the SIS junction is much larger than designed, significantly impacting the coupling to the junctions, as shown in Figure 7.6. Furthermore, photon steps appear in both twin junctions connected to the Pol. 2 hybrid at all frequencies. Since the power in the Δ and Σ ports are approximately equal, the observed behaviour resembles a single input signal into the hybrid, splitting with –3 dB and 90° phase difference between the outputs.

7.2.2 Polarisation Measurement

In order to confirm that the photon step responses in the Σ and Δ twin junction of the Pol. 2 hybrid originate from the same signal polarisation, we varied the LO polarisation. Instead of rotating the LO source, we placed a wire grid between the LO source and the vacuum window. This reduces uncertainties and difficulties associated with the optical alignment as the LO source and wire grid are positioned only once. However, this method inevitably introduces losses due to the addition of the wire grid in the optical path.

The photon step currents centred at 2.25 mV are shown in Figure 7.9 as a function of the wire grid orientation. We again recorded different LO powers for each data point and stepped the wire grid orientation by 20° to interleave the data of a full rotation to the shown 10° resolution.

Both twin junctions attached to the Pol. 2 hybrid show photon-step currents varying sinusoidally with the wire grid angle and peaking together. This observation implies that the Σ and Δ twin junction responses originate from the same LO polarisation. Furthermore, since the power in the Δ and Σ ports is almost equal, it

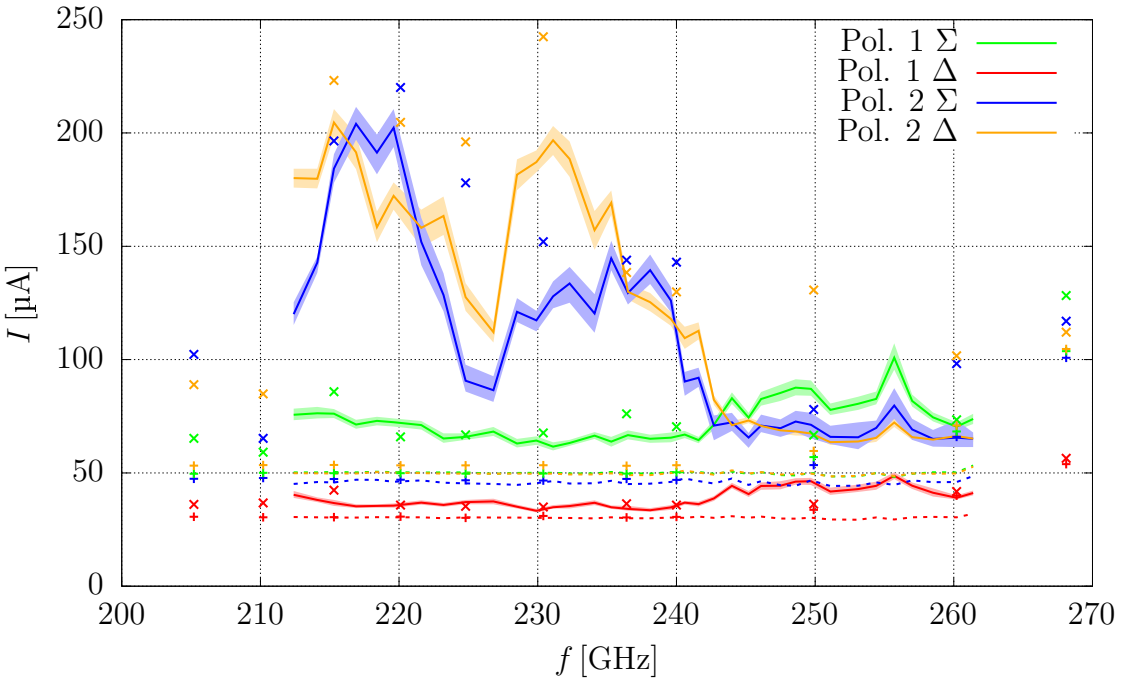


Figure 7.8: The current of the pumped IV curve at a bias voltage of $(2.25 \pm 0.05)\,\mathrm{mV}$ at various LO frequencies. The unpumped currents are shown as dotted lines. $\times$ and $+$ show the pumped and unpumped data of the same experiment taken in a preliminary test.

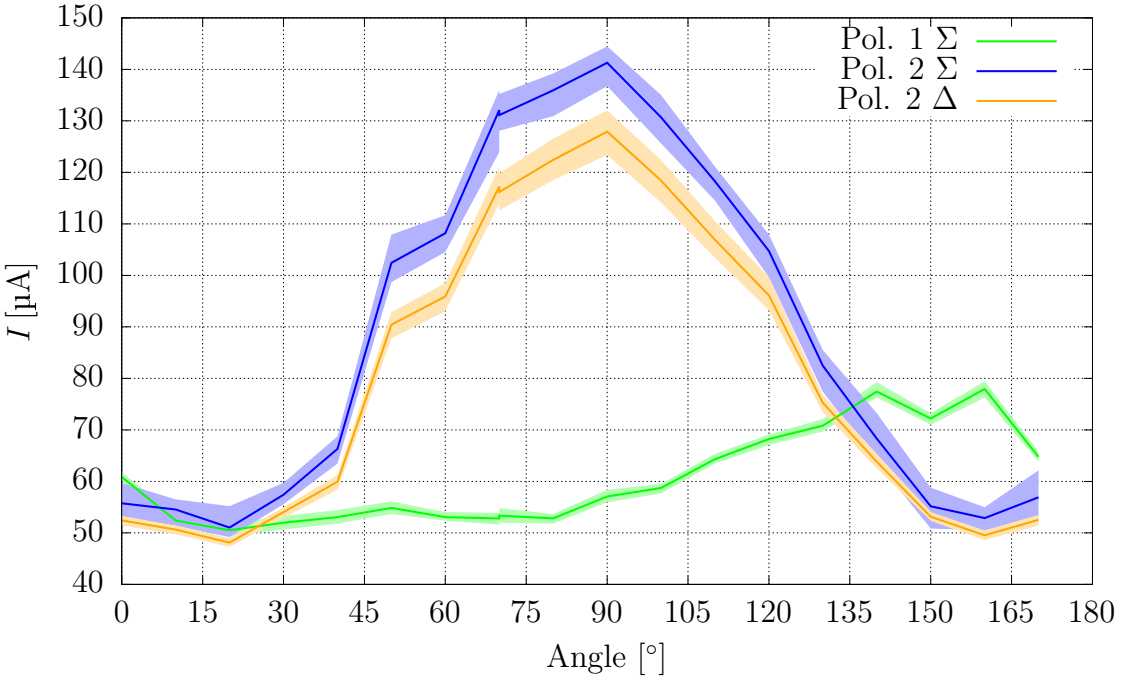


Figure 7.9: The current of the pumped IV curve at a bias voltage of $(2.25 \pm 0.05)\,\mathrm{mV}$ at different orientations of the wire grid at 216.8 GHz.

raises the possibility that the LO power is injected at only one hybrid input. In this scenario, the fabricated hybrid responds similarly to the designed performance shown in Figure 5.7, where a single input signal is applied and splits with $\approx -3\,\mathrm{dB}$ between the two opposing ports.

The current into the twin junction attached to the Pol. 1 hybrid Σ port is $25\,\mu\mathrm{A}$ less at the peak of the Pol. 2 photon step response compared to its maximum current in Figure 7.9. The peak of the Pol. 1 Σ twin junction occurs at a wire grid angle of 150°, providing evidence that the OMT, indeed, splits the two polarisations. However, the wire grid angles corresponding to the two polarisation peaks differ by only approximately 60°. This angle was, of course, designed to be 90°, indicating some issues with the polarisation splitting capabilities of the OMT. Again, this observation is with the caveat of a defective Pol. 1 Δ twin junction.

We repeated this experiment for a set of LO frequencies shown in Figure 7.10. Throughout, we observe that the photon steps of Pol. 1 and Pol. 2 peak at wire grid angle differences well below 90°. In spite of this discrepancy, the photon step currents of the two Pol. 2 twin junctions peaked at the same grid angle at all frequencies. An interesting observation is that the photon step currents peaked at different angles depending on the LO frequency. A reaffirming observation is that the photon step response varies sinusoidally with a period of 180°, indicating that the experimental setup is fine.

7.2.3 Summary of RF Testing

We can summarise the RF testing in the previous section as follows: We have had difficulties pumping the twin junctions and were unable to saturate them at any frequency, although the Gunn LO has been facing the receiver directly. The characterisation of Pol. 1 has been compromised by the defective twin junction attached to the Pol. 1 Δ hybrid output. The Pol. 1 Δ twin junction response has been negligible throughout, and the Pol. 1 Σ twin junction response has shown rather small photon steps. In contrast, both twin junctions attached to the Pol. 2 hybrid showed clear photon steps. For Pol. 2, it depends on the LO frequency, which twin junction circuit, Σ or Δ, shows the larger photon step current. We confirmed that the responses of the twin junction circuits attached to the Pol. 2 hybrid originate from the same polarisation by rotating a wire grid inserted between the LO source and the cryostat vacuum window.

The optical coupling characterisation reveals two issues with the device:

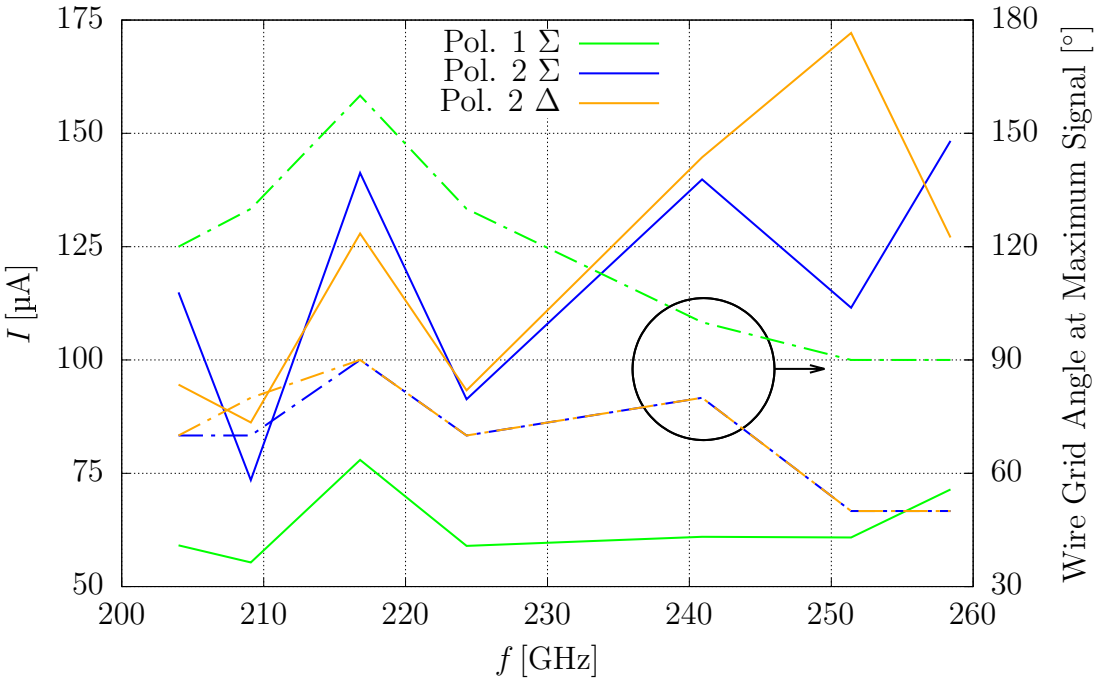


Figure 7.10: The maximum current of the pumped IV curve at a bias voltage of $(2.25 \pm 0.05)\,\mathrm{mV}$ on the left y-axis in solid lines and the corresponding wire grid orientations on the right y-axis in dash-dotted lines at various LO frequencies.

1. The coupling of LO power from the Gunn LO source to the twin junctions is weak.
2. Both twin junctions attached to the Pol. 2 hybrid respond similarly to the LO with frequency dependence.

7.3 Investigation of the Causes of Weak Coupling

The weak coupling of the LO power of the receiver could be caused by several factors, including:

1. Misalignment in assembling the top and bottom split blocks, where the feedhorn and OMT were aligned. This causes the waveguide containing the four OMT probes in the bottom block to be displaced with respect to the feeding circular waveguide in the top block. To investigate the influence of the displacement on the coupling, we simulated the behaviour with Ansys HFSS. The results are shown in Figure 7.11, where we assumed a misalignment of 10% of the waveguide diameter along the axis of a particular polarisation. The OMT probe shifting away from the circular waveguide couples significantly less than the opposing OMT probe, which shifts towards the centre of the circular waveguide.

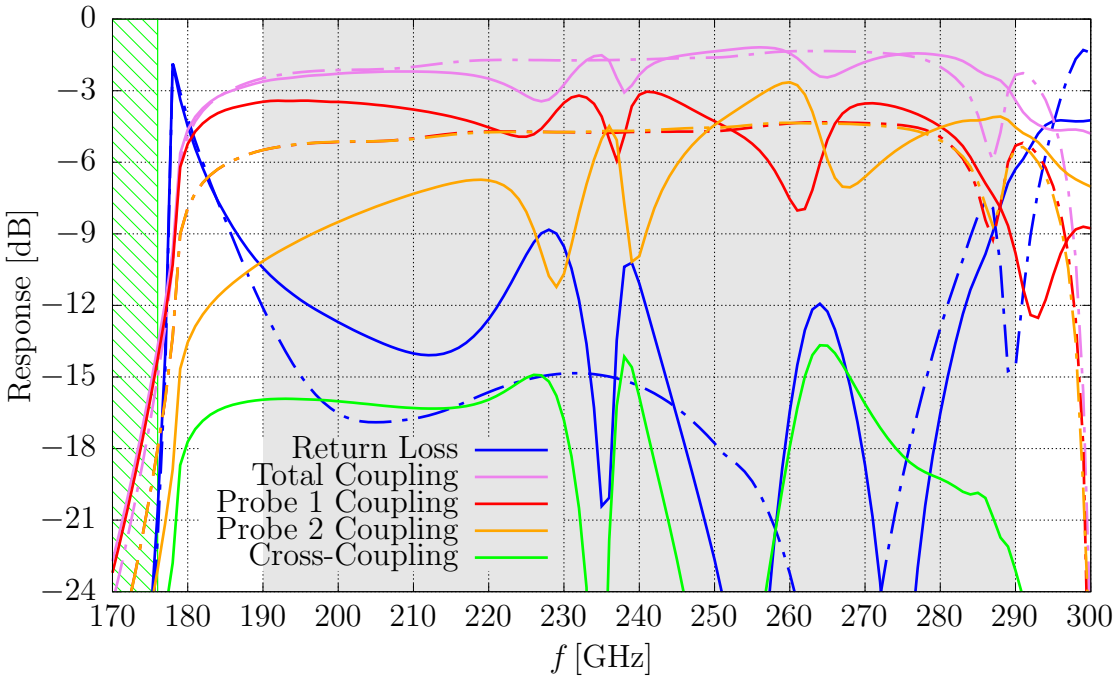


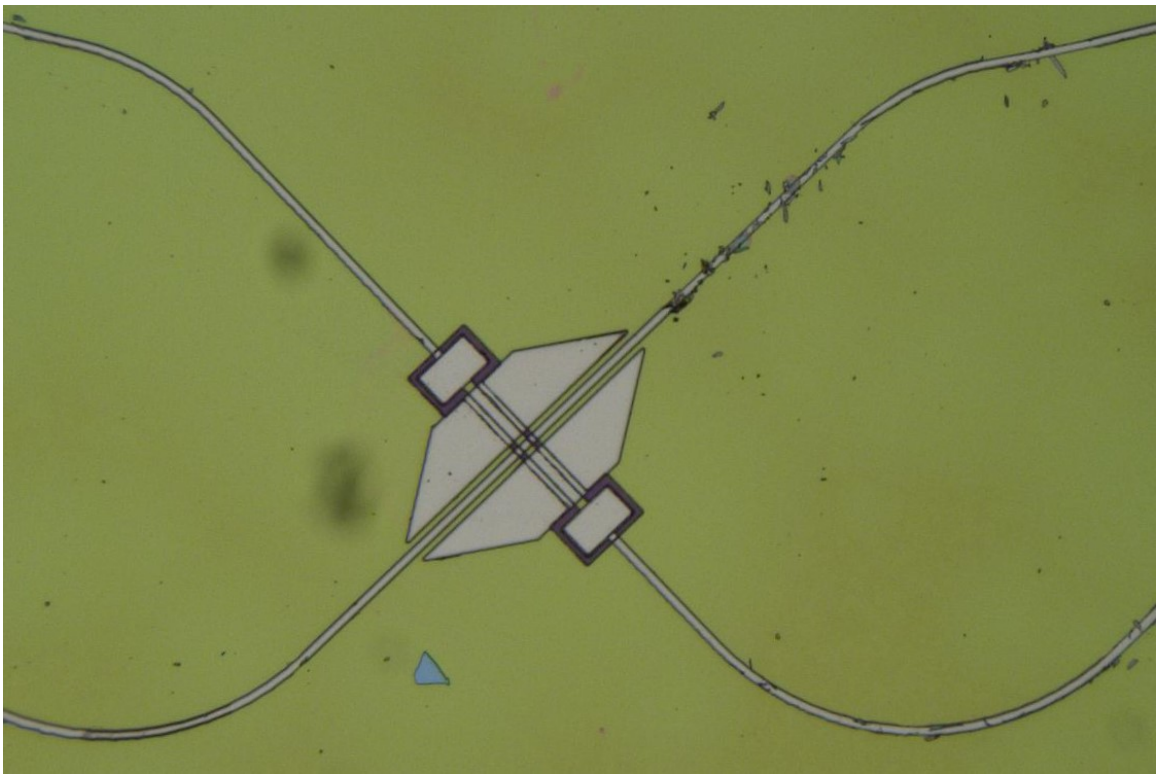
Figure 7.11: The simulated OMT performance with the circular waveguide offset by 100 µm towards Probe 2 of the polarisation, which responses are shown as solid lines. The orthogonal polarisation, shown dash-dotted, shows largely similar responses to the designed performance, especially below 270 GHz, except for the excess cross-coupling in green.

We also observe some cross-coupling into the OMT probes of the orthogonal polarisation. However, the coupling to this polarisation is affected very little by this misalignment. These simulations demonstrate that a displacement of the two circular waveguides could account for the coupling in both twin junctions attached to the Pol. 2 hybrid because one input is significantly stronger.

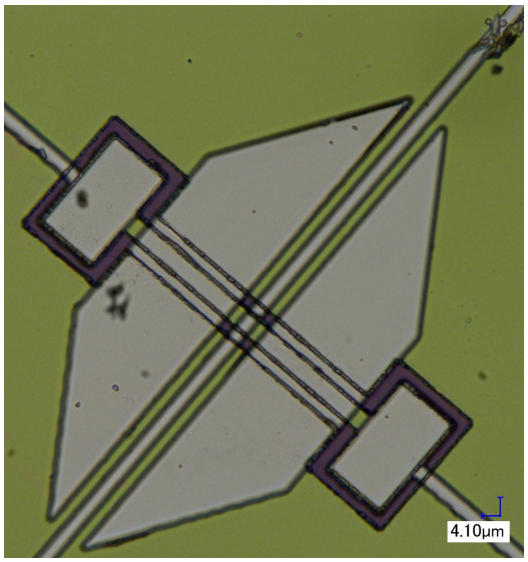
2. Fabrication defects of the receiver components on the chip. The on-chip receiver contains several components that require skilful fabrication to operate as designed. We, therefore, inspected the receiver chip under the microscope and found the following:

   The crossover: The visual inspection showed that the transmission lines comprising the crossover are clean, and, therefore, assuming that no short to the ground plane exists, we do not expect the weak coupling to be caused by the crossover component. A selection of microscope images of the crossover is shown in Figure 7.12.

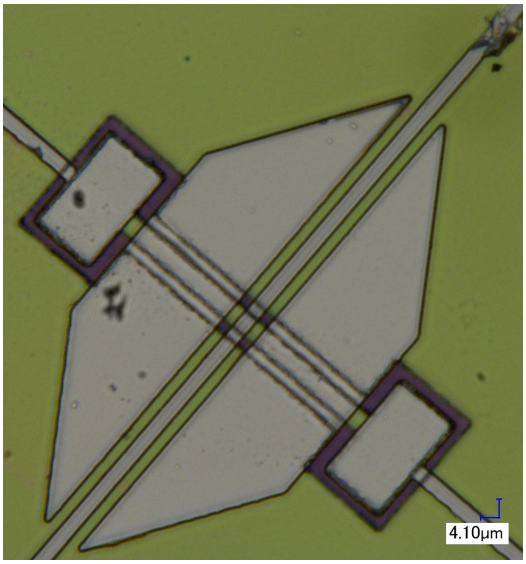
   The hybrid: The transmission lines comprising the hybrids looked to be in good shape, as shown in Figure 7.13. It is interesting, however, to emphasise



(a) Magnification ×500;

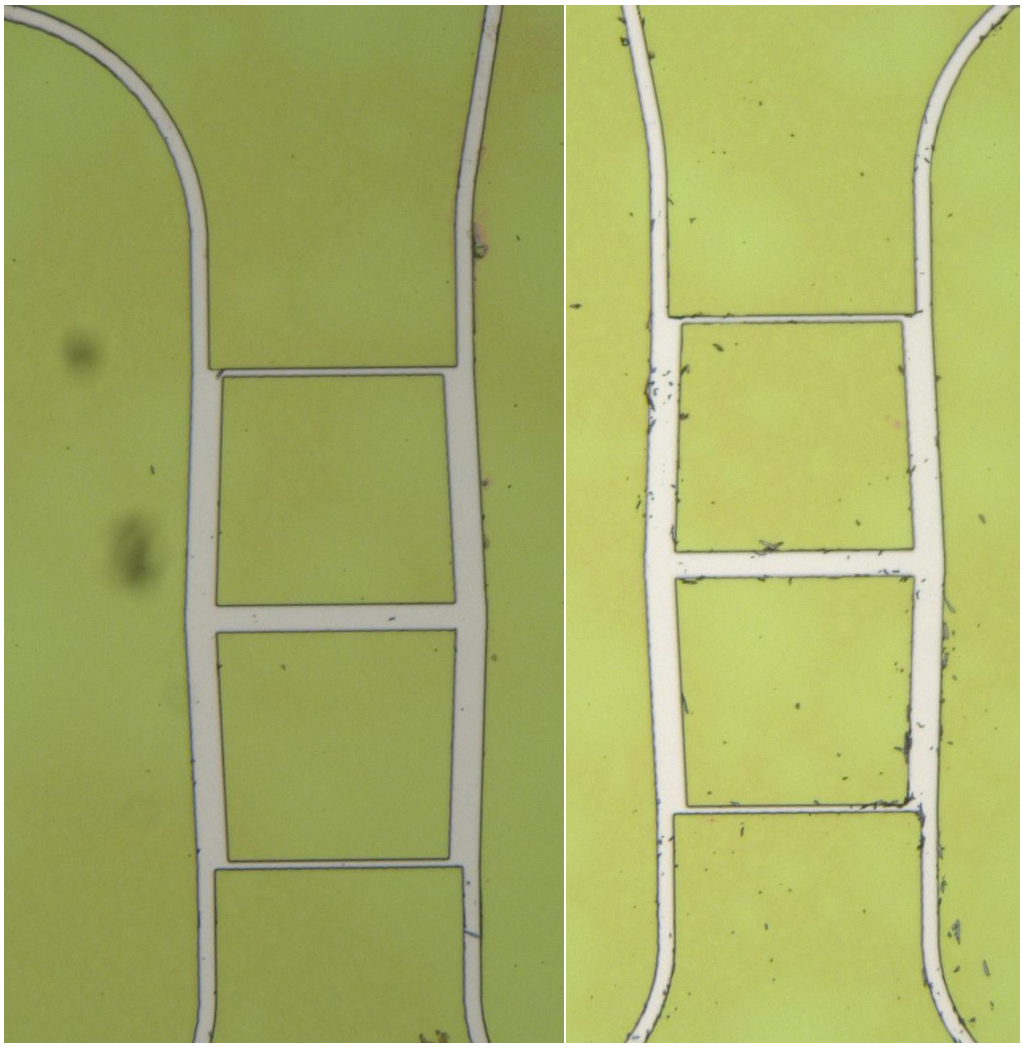


(b) Magnification ×2000 and low focus;



(c) Magnification ×2000 and high focus;

Figure 7.12: Microscope images of the crossover.



(a) Pol. 1 hybrid; (b) Pol. 2 hybrid;

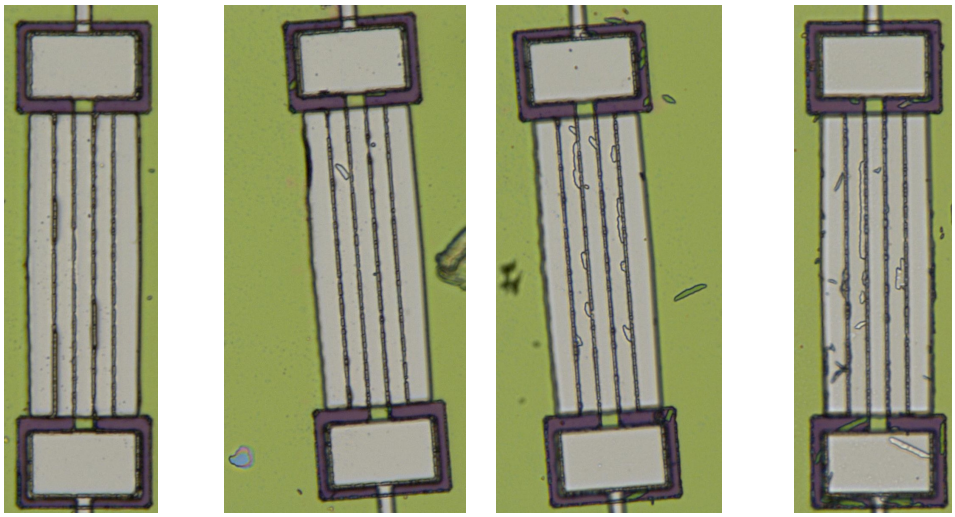
Figure 7.13: Microscope images of the hybrids at $\times 500$ magnification.

that the Σ and Δ ports of Pol. 2 received the same amount of power as our test in the previous section demonstrated.

The BPF: Inspection of the BPF under the microscope does show small defects in fabrication that could cause shorts to ground in both mixer circuits attached to the Pol. 2 hybrid, which could explain the weak coupling. The microscope pictures in Figure 5 show these defects next to the broad-side couplers in green. The Pol. 1 Δ BPF in Figure 7.14a has no defects.

7.4 Conclusion

We describe the DC characterisation performed alongside the fabrication. We changed



(a) Pol. 1 Δ BPF; (b) Pol. 1 Σ BPF; (c) Pol. 2 Σ BPF; (d) Pol. 2 Δ BPF;

Figure 7.14: Microscope images of the BPFs at ×2000 magnification.

the fabrication process and increased the SIS junction area to yield receiver chips with the necessary number of functioning SIS junctions. This modification, however, negatively impacts the predicted RF performance.

With the enlarged SIS junction, we have investigated the performance of an on-chip compact dual-polarisation receiver using SIS tunnel junctions in the frequency range of 200 GHz to 270 GHz. Our experimental test showed weak coupling to the SIS junctions, and we experimentally investigated the polarisation behaviour of the receiver. There is an indication that the OMT and the feeding waveguide in the bottom and top block are not aligned, which causes the signal to couple predominately into one OMT probe. We have performed a thorough analysis of the experimental results to learn about the modifications needed on the chip design and the receiver block to obtain a high-quality on-chip receiver.

Altogether, the on-chip receiver requires significant effort in adjusting the fabrication recipe to achieve high-quality SIS junctions. Furthermore, issues in the RF performance proof difficult to be narrowed down due to the number of integrated circuits. We discuss likely causes for the weak coupling that, however, require future research, such as by modifying the design, to determine the precise reasoning. Thus, the experiments conducted shall be used as a starting point for future projects.

Chapter 8

2-Pixel On-Chip Dual-Polarization Balanced Receiver Design

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In this chapter, we aim to substantially simplify the architecture of an mm-wave dual-polarisation balanced SIS receiver so that it can be easily extended to form a large array. The receiver sensitivity is improved by eliminating the LO noise via the balanced mode operation [28]. For balanced operation, two separate mixers are required for each polarisation, as well as a sophisticated LO injection scheme. Similar to our earlier approach in Chapter 5, we replaced all of the mechanical waveguide structures of the receiver with planar circuit components to relax the requirements and reduce the complexity of the receiver block design. One major difference compared to the design presented in Chapter 5 is that in this advanced design, we utilise the on-chip LO coupling technique to remove the requirement of an LO-injecting beamsplitter array in front of the mixer array. This further simplifies the construction of such receiver array and reduces the optical loss and requirement for large cooling power to cool the beamsplitter array. This is important as conventional beamsplitters such as mylar sheets sag at cryogenic temperatures, affecting the beam coupling to the SIS mixer. Although this can be solved by thermal cycling and tightening of the mylar sheet, it weakens the strength of the material and may cause physical damage.

Therefore, we choose to couple the LO power directly to the mixer via a planar circuit coupler. In the following, we shall describe in detail the electromagnetic designs of some of the additional components not reported in Chapter 5 and the integration of these and the circuit components presented earlier into an array receiver chip.

8.1 Array Receiver Concept

Before we discuss the designs of the individual circuit components, we first present an overview concept of our balanced dual-polarisation array receiver in this section. Figure 8.1 shows an idealised schematic of a 16-pixel balanced dual-polarisation array, employing a single planar 4-probe antenna for coupling the LO power into the array. The same 4-probe antenna will also be deployed for each RF pixel, acting as the planar OMT to split the polarisation states of the incoming signal, similar to the design presented in Chapter 5. Each of these 4-probe antennas, including the LO antenna, will be connected directly to the output of a drilled feedhorn, removing the need for a rectangular-to-circular waveguide transition that is difficult to machine at high frequency. This, therefore, allows for the design of a very simple array block requiring only backshorts and drilled feedhorns, as shown in Figure 8.2, repeated throughout the array.

The array chip is configured to be symmetric for each quadrant, with the LO antenna at the centre and the RF pixels extended radially outward. Each of the LO antenna probes couples a quarter of the incident LO power to each quadrant. In this example, we have four RF pixels in each quadrant, hence the LO power from each LO probe is further distributed to these four pixels via a series of microstrip couplers, coupling a small portion of the LO power to 'pump' the SIS mixers. This radial arrangement around the central LO antenna also allows for even spacing between the RF pixels and provides enough margins to route the IF signal to the edge of the receiver chip for wire bonding. It is worthwhile noting that this particular array arrangement is facilitated by the availability of substrate technology accessible to us, which in our case would be a thinned quartz wafer. Therefore, such an array design can be further simplified and improved, allowing for a more compact and arbitrary pixel arrangement, using a more versatile substrate such as the SoI substrate technology.

It is obvious that the construction of such a 16-pixel array is ambitious at this stage and beyond the scope of this thesis. Therefore, we should only describe the concept here using a 2-pixel demonstrator for clarity and ease of explanation. In the following

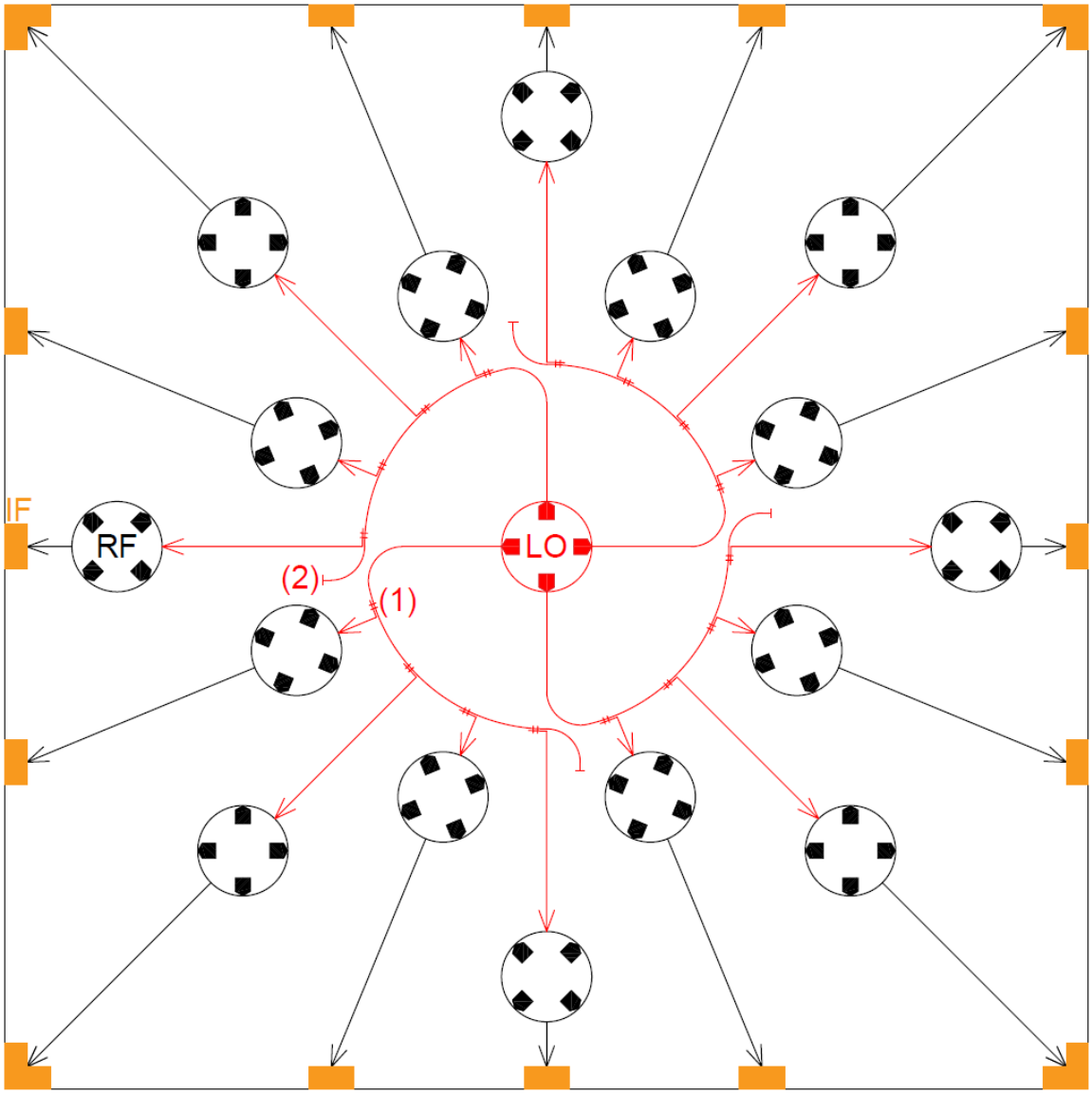


Figure 8.1: Illustration of the 16-pixel dual-polarisation on-chip receiver concept. The LO is coupled into the on-chip LO distribution network via a 4-probe antenna (red) and distributed to the individual RF pixels (black) with microstrip couplers (1) before it is terminated (2). The downconverted IF signals from both polarisations are guided to the IF transformer at the IF bonding pads near the edge of the receiver chip (orange).

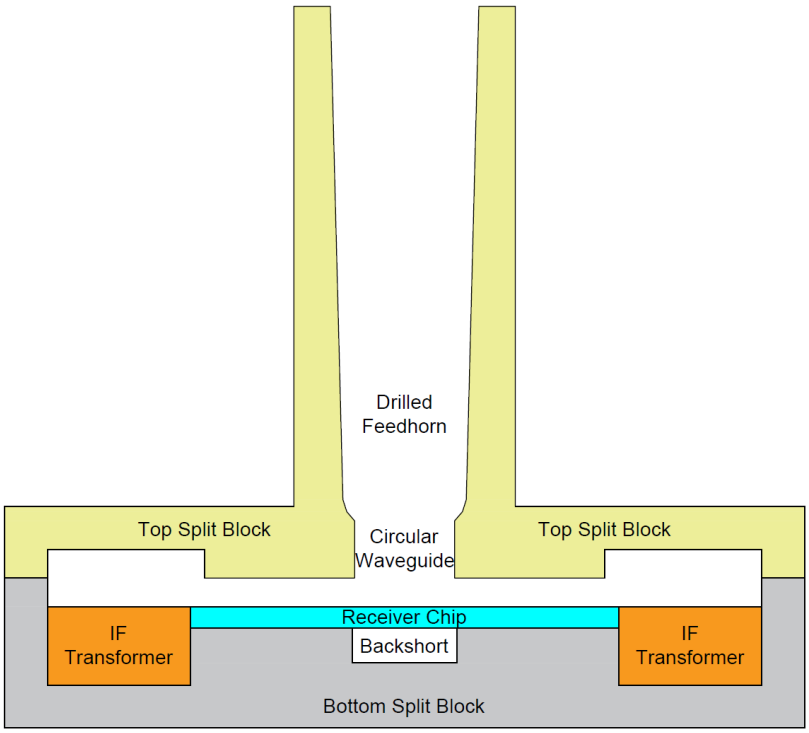


Figure 8.2: Cross-section drawing of the 2-part split-block for the 16-pixel dual-polarisation on-chip receiver concept.

sections, we focus on the schematic layout of the 2-pixel demonstrator and describe in detail the LO distribution mechanism, the separation of the RF polarisations, the mixer circuit, and the overall balanced dual-polarisation receiver circuitry. Finally, we conclude this chapter by presenting the full 2-pixel balanced dual-polarisation receiver design along with the predicted performance and the accommodating receiver block design.

8.2 Schematic of the Balanced 2-Pixel Array Demonstrator

Figure 8.3 shows the schematic of the 2-pixel demonstrator array. The LO power is coupled from a two-probe antenna and is distributed to each polarisation branch of each pixel with a set of two microstrip couplers. The RF signal of each pixel is coupled on-chip via a 4-probe OMT, where each polarisation state is fed from a set of opposing probes similar to the design introduced in previous chapters. As shown in Figure 8.3, the layout of both RF pixels and all the polarisation branches are identical from there onwards.

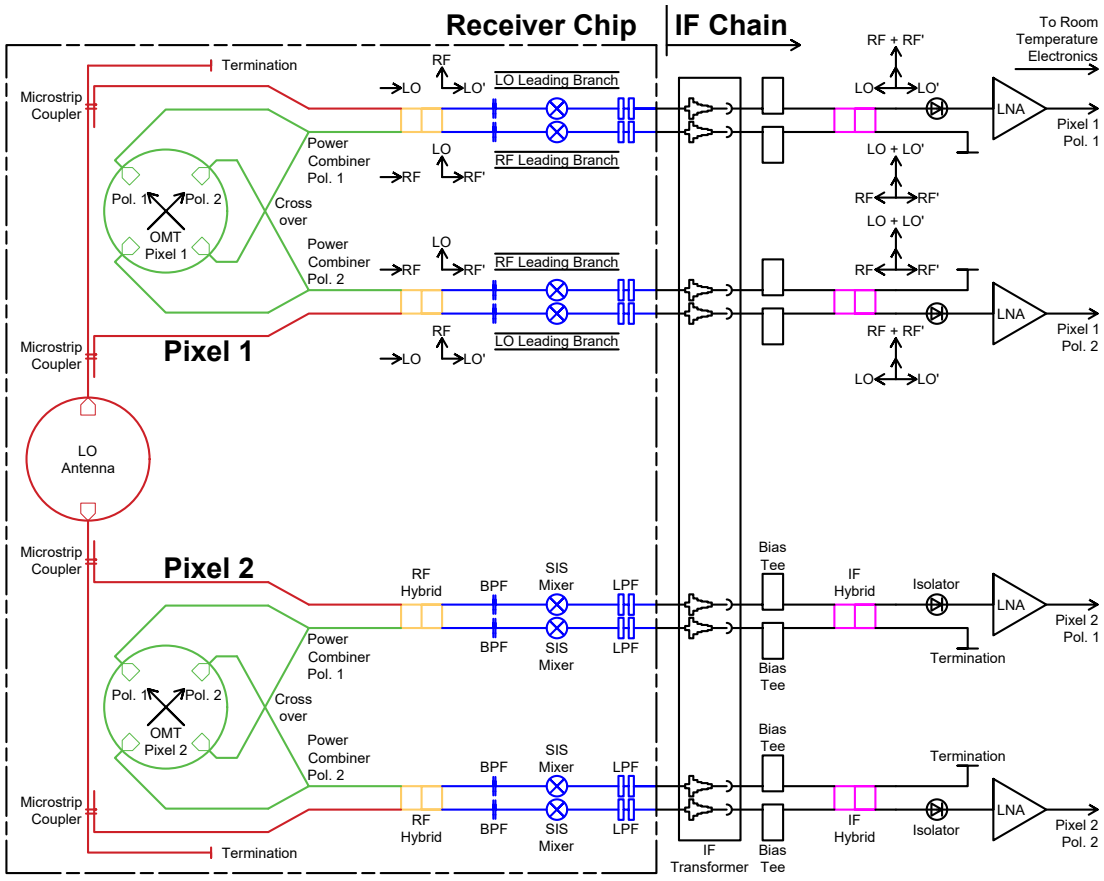


Figure 8.3: The schematic diagram of the 2-pixel balanced SIS receiver. Components on the receiver chip are shown within the dashed rectangle, including the LO distribution network shown in red and the dual-polarisation RF receiver network of each pixel shown in green. The RF hybrids, coloured orange, combine the RF and LO signals before feeding them to the mixer circuits shown in blue. The RF hybrid introduces a 90° phase difference between the RF and the LO signals, indicated by the vector diagram shown in Pixel 1 branches. The IF hybrid, coloured pink, introduces a similar 90° phase difference to separate out the downconverted IF and the LO noise component into two separate ports, hence the balanced operation mode.

Focusing on the Pol. 1 branch of Pixel 1: The signals of the OMT probe sets are routed via a crossover to the planar power combiner, where the output powers from both probes are recombined. The combined RF and the LO power from the top microstrip coupler are then fed into an RF quadrature hybrid. This hybrid splits the power of both, the RF and the LO signals, equally between its outputs. The output ports are connected to two identical mixer circuits comprising a BPF, an SIS mixer circuit and a LPF, similar to the mixer circuits used in the receiver design discussed in previous chapters. The downconverted IF outputs from these mixers are then fed to an IF quadrature hybrid via a series of IF transformers for impedance matching and bias tees for DC-biasing the mixers. The output ports of the IF hybrids that contain the IF signal are then connected to the IF amplification chains for further processing.

8.2.1 Balanced Operation

One notes immediately that this configuration of feeding the RF and LO power to the two mixer branches via a set of RF and IF quadrature hybrid is, in effect, a balanced scheme. Similarly, focusing on the Pol. 1 branch of Pixel 1, the RF hybrid introduces a 90° phase shift between the RF and the LO tones, including the LO noise. As a result, the hybrid output for the top mixer branch indicated as 'LO Leading Branch' in Figure 8.3 contains an RF/LO signal pair where the LO is leading the RF tone by 90°, as shown in the vector diagram in the figure. Likewise, the 'RF Leading Branch' has an RF/LO pair where the RF is leading the LO by 90°. This phase difference between the RF and LO tones remains unchanged during the mixing process. Once processed by the SIS mixers, the downconverted IF signals are fed via the IF transformers and bias tees to an IF quadrature hybrid. Following the vector diagram of the IF hybrid, we see now that the top IF branch contains both the RF signals, which are in-phase, while the LO pair is 180° out-of-phase, hence cancelling out each other. Similarly, the LO pairs recombined in-phase at the bottom IF branch, which now contains all the LO noise contribution, can be terminated with a matched load, allowing for an LO-noise-free operation of the receiver.

In this 2-pixel example, the remaining LO power from the 2-probe antenna is terminated with an RF load. As the LO power needed to 'pump' an SIS mixer is relatively low, this terminated port, in fact, still contains quite a lot of LO power. This microstrip branch can, therefore, be used to 'pump' a subsequent array of SIS pixels, all with the same layout as the configuration of the diagram shown earlier

except for a minor alteration to the microstrip couplers (see later Section 8.3.1.2), hence the flexibility of this scheme to form a large array.

8.3 Design of the Front-End Receiver Chip

Figure 8.3 shows the full receiver circuit diagram of the entire 2-pixel demonstrator, including both the front-end receiver chip, which contains all the high-frequency components, as well as the back-end IF signal chain. Since the microwave components required to form the IF chain can be purchased commercially, we shall focus only on the design of the front-end receiver chip.

We chose to demonstrate the feasibility of the array chip in the same frequency range from 190 GHz to 290 GHz as the design introduced in the previous chapters. The same film parameters, topology and design methods, summarised in Appendix A, are used to exploit and re-optimise the models from the initially presented design in Chapter 5. Again, it is not feasible to model the entire receiver chip in HFSS due to its large electrical size, spanning several tens of wavelengths across the entire chip with features several microns in size. From the discussion above and Figure 8.3, it is clear that the circuit of the receiver chip can be grouped into three major parts: 1) The LO distribution network, 2) the polarised signal coupling network, and 3) the mixer circuit. Therefore, we split the 3D model of the receiver chip into three parts accordingly to speed up the simulations and better understand the behaviour of individual components without adding too much complexity. The overall performance of the full chip is then simulated by connecting these three main parts following the circuit depicted in Figure 8.3 using Ansys Circuit, in the same way as we concatenated the polarised signal coupling network and mixer circuits in the previously discussed design.

8.3.1 LO Distribution Network

The most novel feature of our array chip design is the on-chip LO distribution network, feeding the LO from the planar 2-probe antenna to each polarisation branch of all RF pixels of the array. This allows for a compact and easy-to-control LO power distribution design using planar circuit technology, replacing the complicated waveguide or mylar beamsplitter structures and thus simplifying the receiver design. Our LO distribution network comprises two main components: the 2-probe antenna and the microstrip couplers, interconnected with microstrip lines.

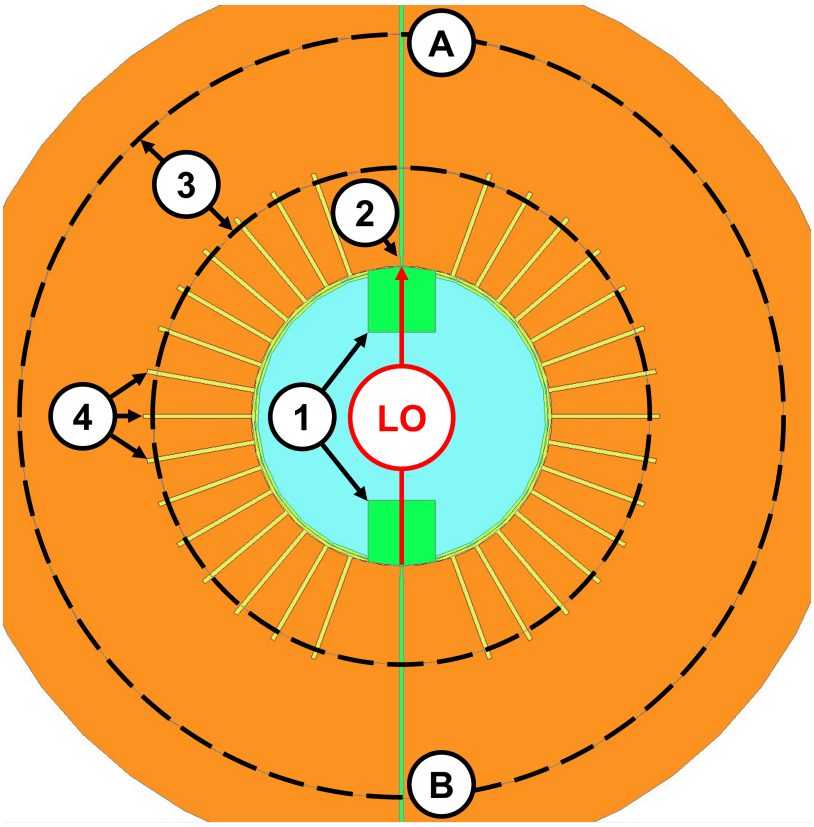


Figure 8.4: The layout of the two-probe LO antenna. The probes (1) couple the TE_{11} mode from the circular waveguide via an intermediate microstrip impedance transformer (2) into microstrips (A) and (B). Losses through the vacuum slit above the chip are reduced by the choke groove shown with dashed lines (3), and the serrations in the ground plane (4) to prevent parallel-plate waveguide resonances in the 'ring' area between the choke groove and the circular waveguide. The width of the microstrips and the serrations are artificially widened for clarity.

8.3.1.1 Two-Probe Antenna

The 2-probe antenna shown in Figure 8.4 is basically one of the polarisation probe-sets of the 4-probe OMT used in the RF pixels. The 2-probe antenna is mounted directly underneath a drilled three-section flare-angle smooth-walled feedhorn [116, 118] that couples the free-space signal into the TE_{11} mode of the circular waveguide hosting the antenna, similar to the presented 4-probe OMT design. By aligning the probe set along the E-field direction of the TE_{11} mode, each of the probes picks up half of the incident LO power and splits it evenly between the two output microstrips.

The coupling from the circular waveguide into microstrips is improved in comparison to our 4-probe OMT design by introducing a single-section impedance transformer between the probe and the output microstrip. This microstrip transformer has the

narrowest width possible with the established fabrication process and connects to a lower characteristic impedance, matching the following microstrip coupler.

We were able to improve the performance further by optimising the LO antenna only within the frequency range from 210 GHz to 270 GHz in comparison to the 4-probe OMT. The low- and high-frequency end of the RF bandwidth will be down-converted as LSB and USB, respectively. We optimistically aim for a 20 GHz IF bandwidth so that, for example, a 190 GHz RF signal is converted to a 20 GHz IF signal with a 210 GHz LO. Thus, the required LO bandwidth can be reduced at the benefit of improving the coupling in the narrower bandwidth.

As shown in Figure 8.5, we managed to improve the total coupling from the circular waveguide to the set of microstrips to approximately –1.3 dB. The return loss is better than –18 dB across the entire designated bandwidth. More importantly, the power coupling between the two probes is identical and flat across the entire band, ensuring that the LO power is distributed evenly between the two RF pixels. It can be noted from the plot that the loss through the substrate and the vacuum slit is still rather high at –6 dB. As mentioned before, it is possible to improve the performance using SoI membrane technology to thin down the substrate further, but unfortunately, this technology is unavailable to us at the moment. Hence, we believe that the current performance is the best one could achieve using the standard quartz substrate technology.

8.3.1.2 Microstrip Coupler

As only a small portion of the LO power coupled from the 2-probe antenna needs to be injected into the SIS mixers, we utilise a series of planar microstrip couplers to route approximately –10 dB of the LO power to each polarisation branch of each pixel. As shown in Figure 8.6, our microstrip coupler is similar to the conventional design, where two adjacent microstrips are fabricated close to each other to allow for the fringing field lines to cross over between the two microstrips, with the fourth unused port terminated with a quarter-wavelength radial stub. However, as the field lines in a microstrip are strongly confined between the wiring and the ground plane, it is not feasible to increase the coupling level without too narrow a gap between the two microstrips or to transition into another type of transmission line topology. Following the design presented by Tan et al. [121], we employ a pair of slot openings in the ground plane underneath the microstrip pair to promote the field line crossover and therefore increase the coupling. This feature is important as the coupling level can be controlled precisely by altering the length and width of the slot openings. In

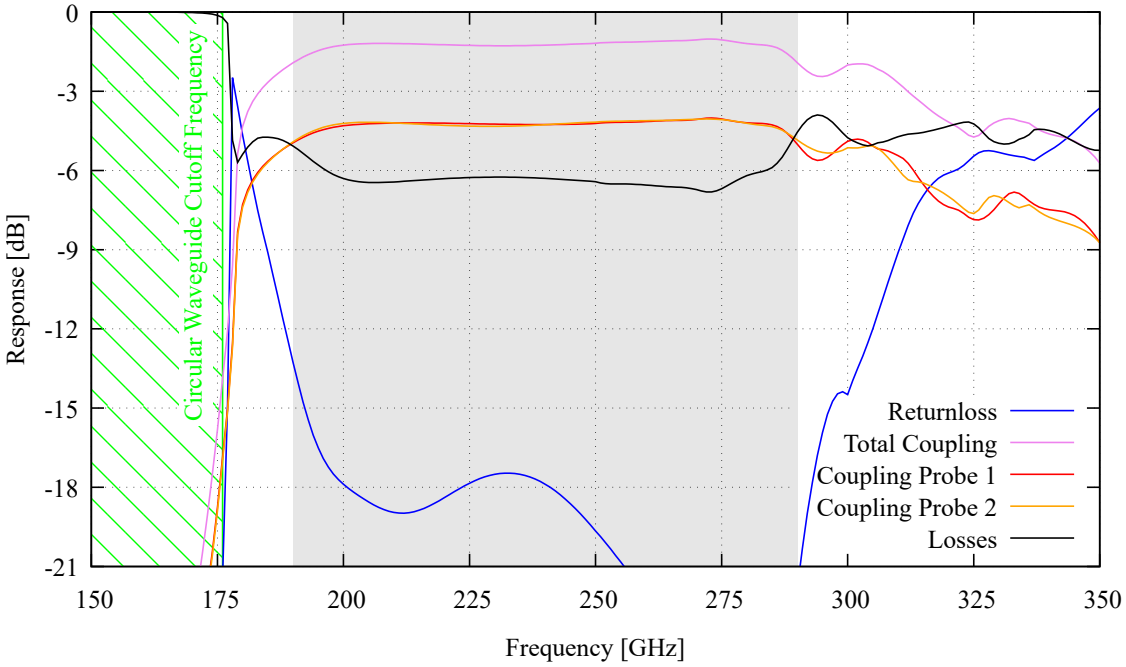


Figure 8.5: The predicted performance of the two-probe antenna. Total Coupling denotes the sum over a probe set, and Losses encapsulate the difference between the input and output power measured on all ports.

our case, after the first coupler, the width of these slots in the subsequent coupler is widened accordingly to achieve the same power coupling as the first coupler, ensuring all the mixer branches are 'pumped' at a similar level. This simple design also allows us to employ the same coupler layout for a larger array since they can be cascaded in series easily and yield the same LO coupling for all pixels by simply controlling the slot dimensions.

Using HFSS to optimise the performance of the microstrip coupler in the designated frequency range from 210 GHz to 270 GHz, we successfully achieve an identical power coupling between –12 dB to –8 dB from the output of the probe to both polarisation branches of one of the RF pixels of our 2-pixel demonstrator, as shown in Figure 8.7. Again, the return loss performance is better than –18 dB across the band, and the coupling difference between the two couplers is less than 0.3 dB throughout. Although the coupling level is lower at the lower frequency ends, due to the nature of the fringing fields being less tightly confined in the dielectric layer at shorter wavelength, this effect has less impact on our application since the LO power can be adjusted while tuning the LO frequency during actual observations. Therefore, the mixer can still be 'pumped' at a similar level over the full frequency bandwidth.

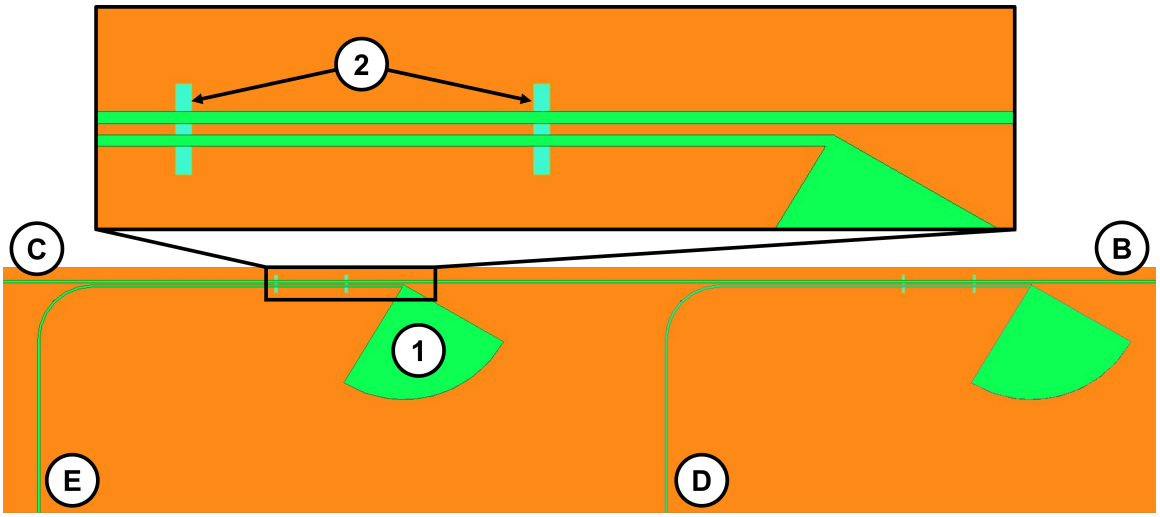


Figure 8.6: The layout of the microstrip coupler, showing the main microstrip line, fed from the LO antenna (B) to (C), where more microstrip couplers can be incorporated. The LO power from (B) is coupled to (D) and (E) for subsequent connection to the two polarisation branches of an RF pixel. The fourth port is terminated with a radial stub (1). The slot openings in the microstrip ground plane (2) improve the LO power coupling from (B) into each branch (D) and (E).

As explained earlier, even after a set of microstrip couplers, more than –3 dB of LO power remains in the main line. Thus, additional microstrip couplers can be cascaded to 'pump' subsequent pixels in a larger array.

8.3.2 Polarised Signal Coupling Network

The RF power coupling path of our receiver chip, comprising mainly a 4-probe OMT antenna, a crossover and two power combiners, is shown in Figure 8.8. The main objective of this network is to couple the polarised signal from the circular waveguide and split the two orthogonal states before feeding them separately into two individual branches for subsequent connection. The 4-probe OMT and crossover design have been described in detail in Chapter 5. Hence, in the following, we shall focus mainly on the design of the power combiner.

The OMT couples the two TE_{11} polarisation states from the circular waveguide into microstrips via two pairs of opposing probe sets in the same way as the previously introduced receiver chip. The incident power of a polarisation state splits evenly between the opposing probes, hence needs to be routed to the same location on the chip for recombination. This routing, however, leads unavoidably to the need for a crossover still in the same way as the previously introduced receiver chip.

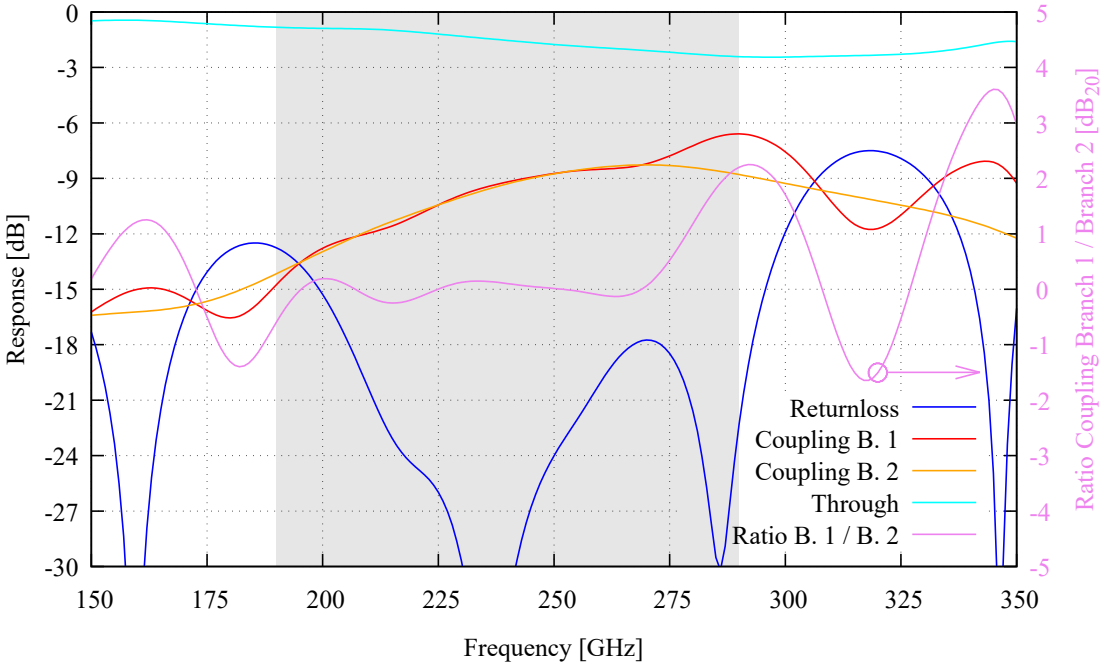


Figure 8.7: The predicted performance of the –10 dB microstrip coupler.

After routing the output power from the probe set to the proximate locations on the chip, the RF power from each probe set is recombined using the planar power combiner shown in Figure 8.9. The design of a planar power combiner is challenging with the standard photolithography fabrication process we utilised here, as it is difficult to fabricate a planar power absorbing component to replace the resistor in a conventional Wilkinson power combiner without complicating the fabrication process [122]. It is possible to terminate this power absorbing port by transforming a 4-port Wilkinson power combiner into a 3-port device, but it is well known that it is not possible to match the impedance of all ports in a lossless 3-port device [26, 123]. In this case, we opt to match only the power combining output port with an equal –3 dB in-phase coupling from the two input ports while leaving the return losses and the coupling between the two input ports fixed at approximately –6 dB.

For the termination of the power absorbing port, we introduce a back-to-back radial stub structure with a microstrip connecting the two input ports. These radial stubs act, in effect, as a quasi-lossy component to radiate away the power imbalance between the two input ports, hence improving the combiner's performance. As shown in Figure 8.10, with this method, we successfully achieve a uniform –3 dB coupling from the two input ports to the combined output port across the required band, with the phase difference close to 0° throughout the band. The return loss performance of

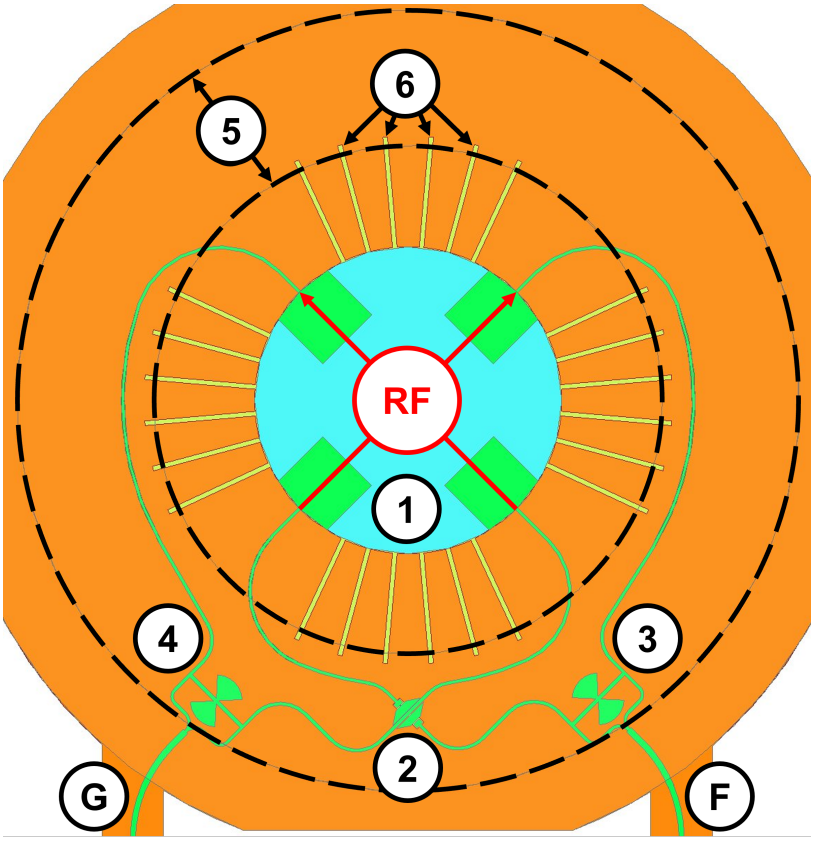


Figure 8.8: The layout of the OMT-to-power-combiner circuit. The four-probe OMT (1) couples both polarisation states from the circular waveguide with two sets of opposing probes. The signal of a probe set is then routed via the crossover (2) to the power combiners (3) and (4) for Pol. 1 and Pol. 2 states respectively. The recombined signal power at (F) and (G) is fed to the subsequent mixer circuits. Similar to the LO antenna, the OMT features a choke groove (5) and serrations in the ground plane (6). The width of the microstrips and the serrations are artificially widened for clarity.

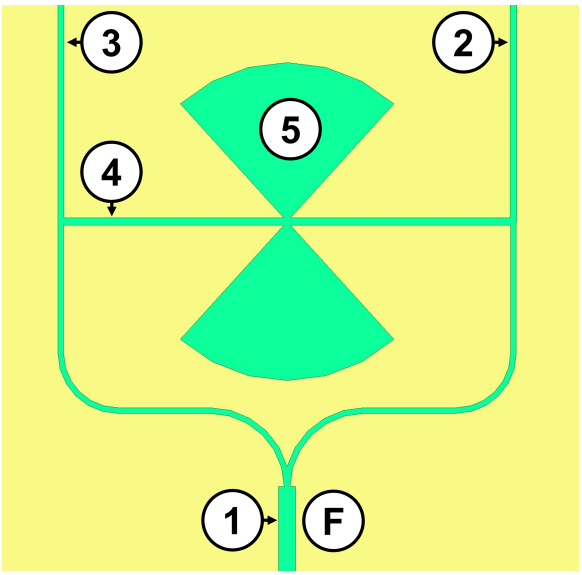


Figure 8.9: The layout of the planar power combiner. The matched combined port (1) is fed by two branches (2) and (3), which are interconnected with a microstrip (4) and two radial stubs (5).

the combined port is well below –20 dB as well. The only downside here is the –6 dB return loss of the input ports and the power coupling between these two ports at a similar level. However, it is worth noting that this combiner is very simple to design and does ease the fabrication process significantly, as the structure can be fabricated using the same material as the other circuit components, using just the microstrip topology.

8.3.2.1 Performance of the Integrated Polarised Signal Coupling Network

Once the individual circuit components are optimised, we integrate them within the HFSS environment to form the entire RF signal coupling network. This network guides each polarised RF signal to be combined with the LO power from the LO distribution network before feeding to the subsequent mixer circuits. As the planar power combiner we utilised here is an in-phase power combiner, while the phase difference between the two probes from the probe-set of each polarisation branch is 180° out of phase, we need to ensure that the lengths of the two microstrip lines that connect the outputs of the probes to the inputs of the combiner are differed by 180° to compensate for the 180° phase difference. In our design, those microstrips guided through the crossover are a half-wavelength shorter than their counterpart without the crossover. These microstrips also feature several sections of quarter-wavelength

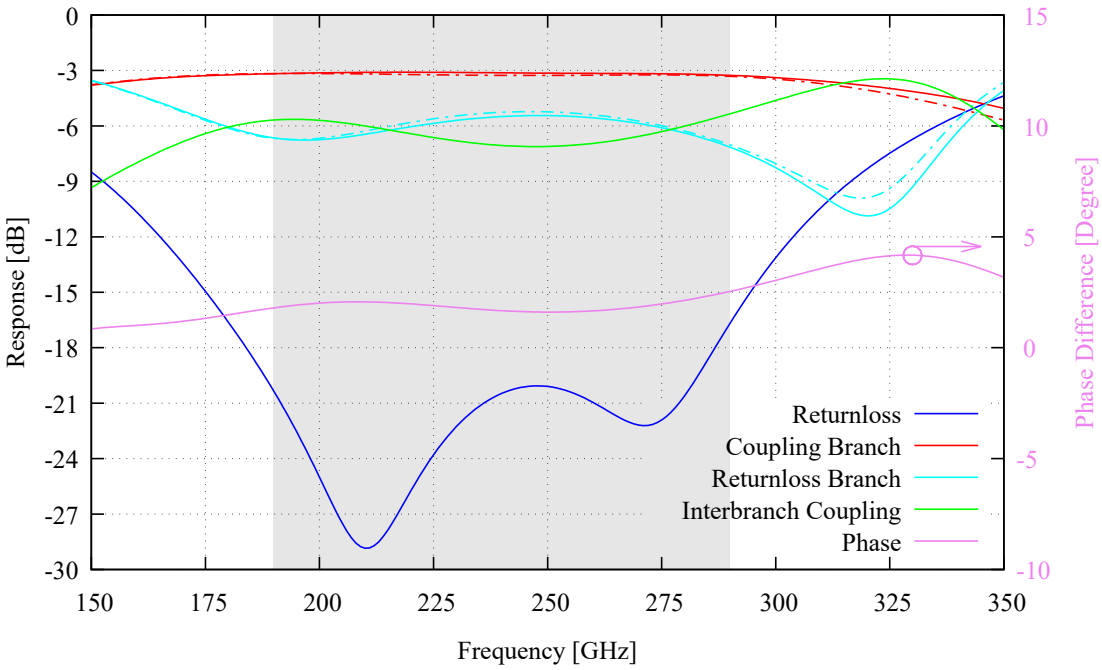


Figure 8.10: The predicted performance of the power combiner. The responses of the individual branches are shown as solid and dash-dotted lines.

impedance transformers to match the output impedance of the probes to the input impedance of the power combiner.

We should emphasise that the simplest way to combine a 180° out-of-phase signal pair is, in fact, to use a 180° hybrid, where the two signals combine at the Δ port. However, this would require an efficient way to terminate the Σ port of the hybrid, such as the use of another mixer circuit biased above the gap voltage acting as a matched load or again with power absorbing-material [115,124]. It is obvious that this method complicates the array chip design substantially, requiring six mixer branches now instead of four and consequently making the chip unnecessarily larger due to the additional bonding pads for biasing these 'terminating' junction loads.

Figure 8.11 shows the simulated responses of the RF signal coupling network, and we see that the overall performance of the network is good. The power coupling from the OMT to the output of the power combiner stays near the –1.8 dB level. The return loss of the entire network remains below –10 dB across the band for both polarisation states, except for the very high-frequency end of the band for Pol. 1. The total loss in the network is about –5 dB, again dominated mainly by the energy loss of the OMT antenna through the quartz substrate and the vacuum slit. More importantly, we see that the behaviour for both polarisation branches remains largely identical

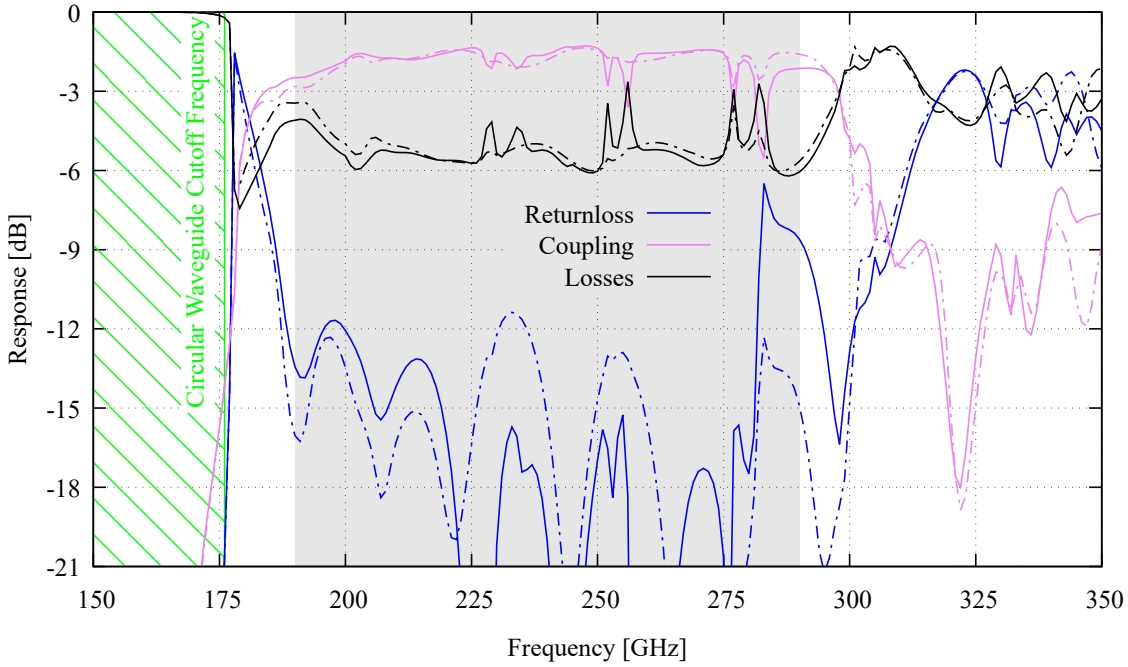


Figure 8.11: The predicted performance of the OMT-to-power-combiner circuit. The response of Pol. 1 is shown with solid lines and Pol. 2 with dash-dotted lines.

throughout the band, preventing any bias during observations with the receiver.

However, it is evident from the plot that there are unexpected resonance features within the network. Curiously, Pol. 1 appears to have more repeated resonance structures than Pol. 2. The causes of this, together with the unexpectedly slightly higher return loss for Pol. 1 at the high-frequency end, are still under investigation. We suspect that this could be due to the high return losses from the input ports of the power combiner, reflecting –6 dB of power back to the OMT probes, which subsequently coupled via the OMT to the other branches and set up unwanted standing waves within the system. It could also be caused by the imperfect impedance matching between the individual components, particularly at the broadside couplers of the crossover. However, we do not rule out that the issue could simply be caused by the irregular meshing by HFSS due to the large electrical model of the network. Therefore, further investigations are required to identify the root cause of these unexpected effects by carefully tracing the energy flows between all the components forming the RF signal coupling network.

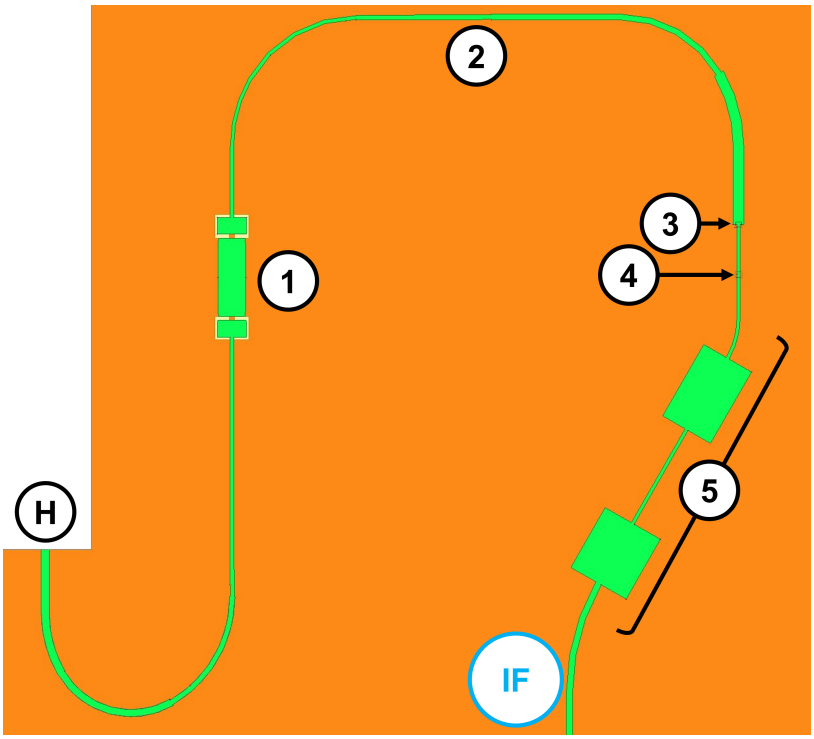


Figure 8.12: (a) The layout of the mixer circuit. The RF and LO signals fed from (H) couple through the BPF (1) and an impedance transformer (2) to the twin-junction mixer, comprising a first (3) SIS junction, a short intermediate microstrip and a second (4) SIS junction. The twin-junction is followed by a LPF (5) to prevent RF power leakage into the IF circuit.

8.3.3 Mixer Circuit

The final major component of the array chip is the mixer circuit shown in Figure 8.12, comprising the DC and IF blocking BPF, the SIS tuner circuit and the RF chokes acting as LPF for the IF chain. The SIS tuner circuit is again a twin junction circuit with a series microstrip transformer. The design of this mixer circuit is largely similar to the one reported earlier but laid out differently to space out the bonding pads in the final receiver assembly.

As shown in Figure 8.13, we successfully achieve a total coupling from the input port of the mixer circuit to the twin junctions better than –0.4 dB throughout the designated bandwidth, with a return loss of less than –15 dB across the bandwidth. This simulated return loss performance is 3 dB better than the simulated performance of the receiver circuit designed and presented initially because of the different, more generous layout and minimal adjustments.

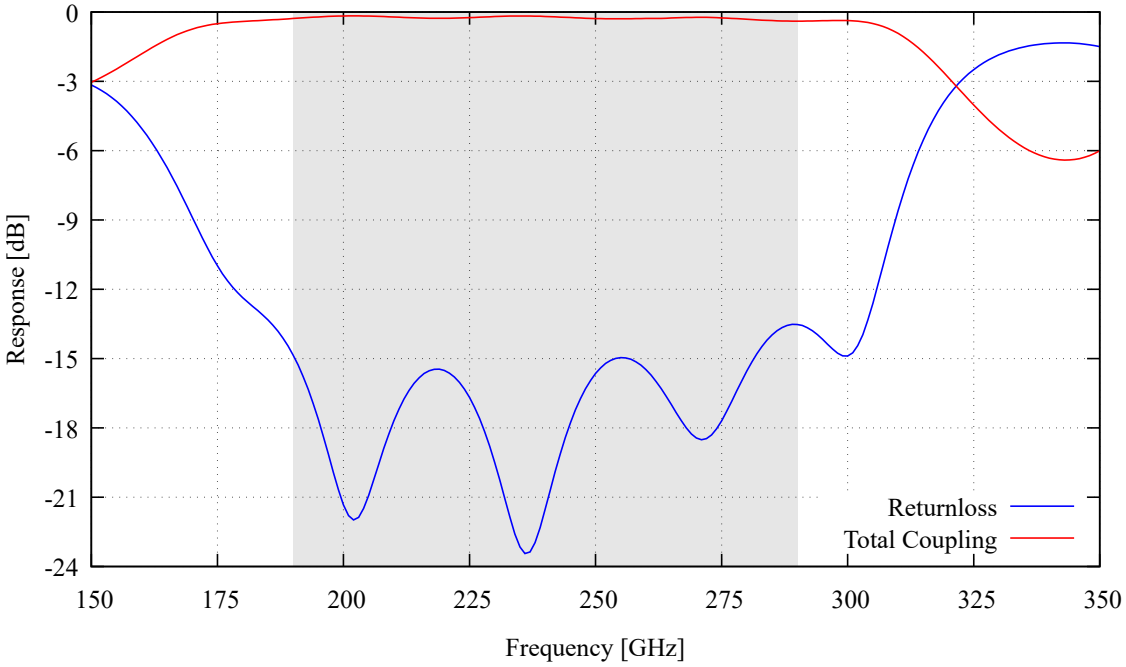


Figure 8.13: The simulated performance of the mixer circuit. Total Coupling denotes the sum over both junctions.

8.4 Design of the Integrated 2-Pixel Array Chip

As shown in Figure 8.3, the three main sub-circuits, the LO distribution network, the RF signal coupling network and the mixer circuits, are integrated via a series of quadrature hybrids to form the entire 2-pixel array receiver chip. The design of the hybrid is pretty straightforward, and has been described in detail in Chapter 5, where we cascade two conventionally used branch-line quadrature hybrids in series to broaden the operational bandwidth as shown in Figure 8.14.

As the layout of the integrated LO-RF-mixer circuit is identical for both pixels and both polarisation branches, we shall focus only on Pol. 1 of Pixel 1. The two input ports of the RF hybrid are connected to the LO distribution network and the RF coupling network, resulting in an equal distribution of RF and LO power to the two output ports, which are subsequently connected to two identical mixer circuit branches. In our design, the LO and RF signals are applied to the Σ and Δ ports of the hybrid shown in Figure 8.14. The simulated performance of our RF hybrid is shown in Figure 8.15, with minor improvements to the performance of the hybrid presented with the design introduced in previous chapters after further optimisation. As expected, we achieve equal and flat –3 dB coupling from the input ports to the 'through' and 'coupled' output ports. The return losses for both input ports and the

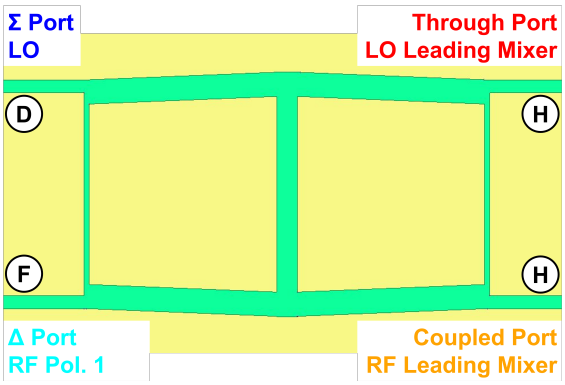


Figure 8.14: The naming scheme of the two-section branch-line 90° hybrid. The labels in the figure show the conventionally used port names of hybrids, as well as the connection reference to other subcircuits with reference to Pol. 1 branch of Pixel 1.

isolation between the two input ports are well below –15 dB across the band. The phase difference between the two output ports remains close to 90° throughout the band, with a ±3° variation. However, it is well-acknowledged that the performance of a balanced SIS mixer is relatively tolerant to the phase difference variation [115, 125]. Therefore, we expect a good performance of the array chip design presented here.

Figure 8.16 shows the full array receiver chip layout, mapping the design schematic shown in Figure 8.3. The size of the chip is measured at 13.8×19.6×0.05 mm, primarily constrained by the size of the feedhorns' aperture. Although the entire RF circuit network for a single pixel, including the mixer circuits, fit within an area of 4.6 mm by 3.8 mm, we need to separate the two RF OMTs by about 10 mm to accommodate the feedhorn aperture with a diameter of ⌀7.3 mm [119, 120]. The LO antenna is centred 15 mm away from the RF pixels to allow for additional optical components to guide the LO power to the mixer block.

Nevertheless, this relatively small receiver chip allows us to design a compact receiver block, measuring only 64.0×55.0×34.4 mm in size, as shown in Figure 8.17(a). This receiver block can be easily machined using two-part split-block technology, along with the assembly to apply a magnetic field across the SIS junctions, the IF transformers, and IF connectors for connections to the bias tees and the IF hybrids. As can be seen from the exploded view shown in Figure 8.17(b), this split block design simplifies dramatically the fabrication of the array block. It requires only milled recesses for the RF chip and IF board, and holes for various connectors, in comparison to traditional array designs that are often populated with a large waveguide network throughout the block.

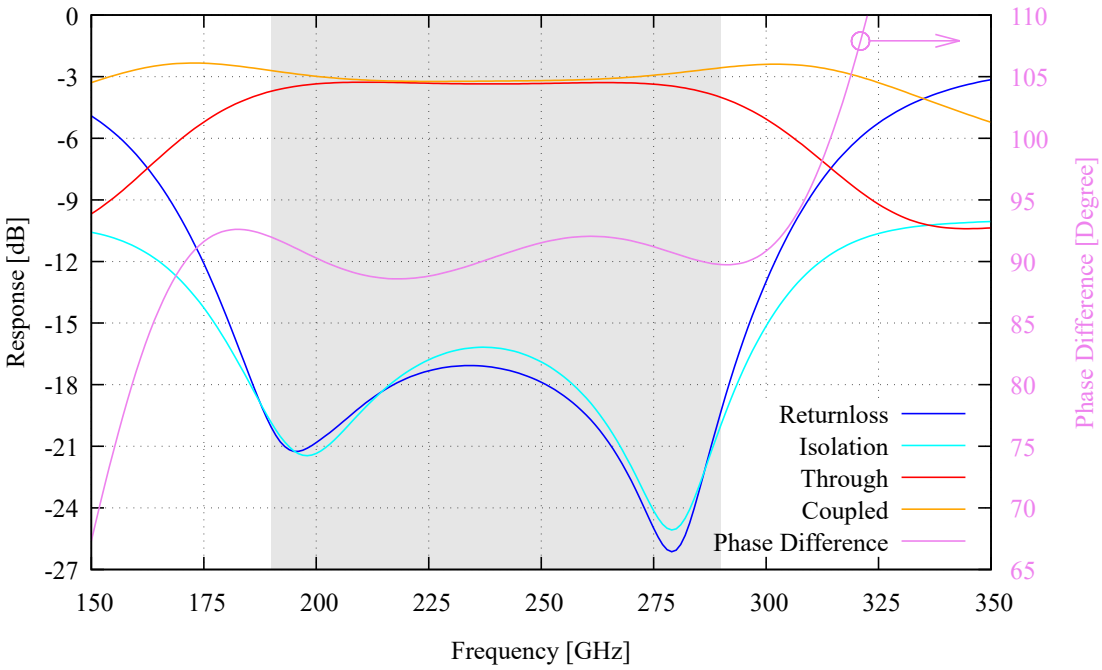


Figure 8.15: The simulated performance of the quadrature hybrid. The performance is shown for an input signal applied on the Σ port.

As explained earlier, the overall performance of our full receiver array chip is simulated by concatenating the scattering parameters of the three main sub-circuits together with the RF hybrids using Ansys Circuit. Figure 8.18 shows the RF and the LO coupling responses for one of the pixels (the responses are identical for both pixels). It is clear that the simulated performances are very similar for the two polarisation branches. The RF signal couples on average –2.5 dB from the circular waveguide into the SIS junctions with approximately –19 dB to –13 dB of LO power across the band, sufficient to pump the mixer array with our existing LO source [44]. If the LO coupling level is too low, we can easily alter the design of the microstrip coupler to improve the coupling, e.g., increasing the coupling level of the microstrip coupler by 4 dB to increase the overall LO power coupling from the waveguide to the mixer to a level between –15 dB and –9 dB. This modification requires only a replacement of the ground plane photolithography mask.

Another potential improvement upon the current design is the flattening of the standing wave structure shown in the performance of our array receiver chip. This can be seen clearly in Figure 8.18, where both the LO and RF power coupling levels, as well as the return losses, are undulating at about ± 1 dB level. The root cause for the existence of the standing wave is unclear and requires further investigation. We

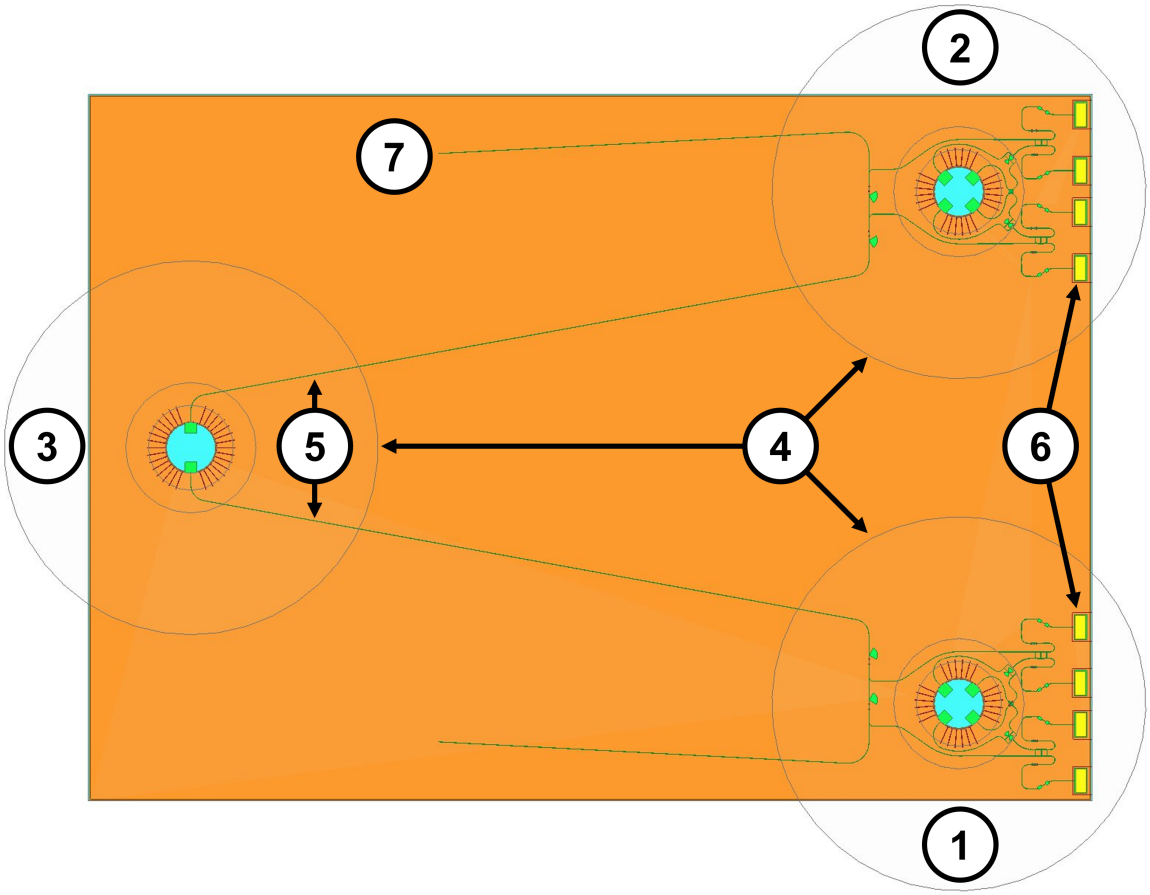
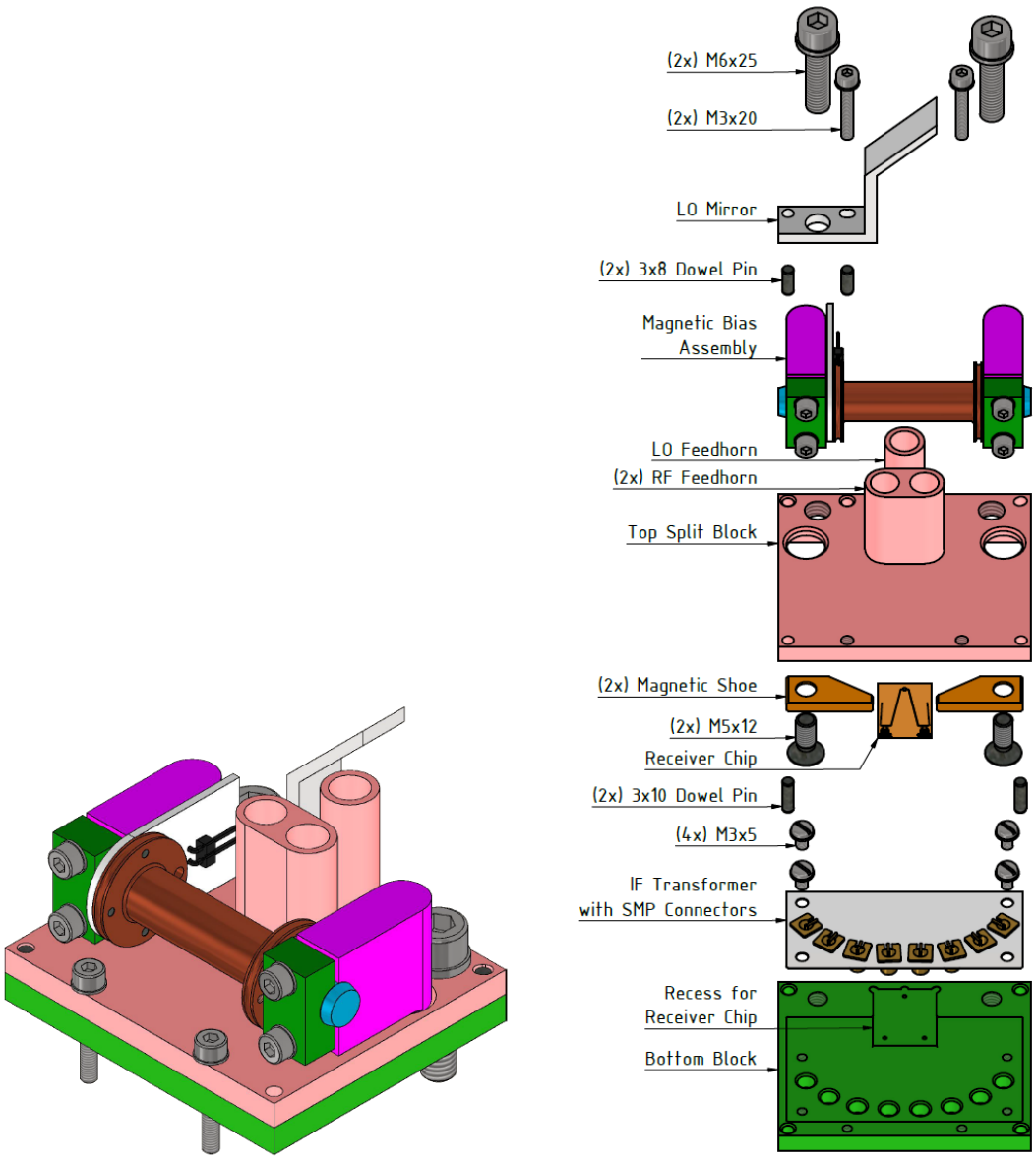


Figure 8.16: The layout of the full receiver chip. Pixel 1 (1) and Pixel 2 (2) are identical, comprising the polarised signal coupling network, the hybrids and mixer circuits for each polarisation. The microstrip couplers are placed to the left of the OMTs of the RF pixels to couple the LO power from the LO antenna (3). The spacing between the LO antenna and the RF pixels is mainly dictated by the aperture of the feedhorns (4), resulting in long microstrips (5) connecting the LO antenna and the microstrip couplers. The IF bonding pads (6) are at the right-side edge of the chip. The location of the bonding pads for the ground and the termination of the remaining LO power (7) is yet to be finalised.



(a) (b)

Figure 8.17: The (a) assembled receiver block and (b) exploded view with all required components.

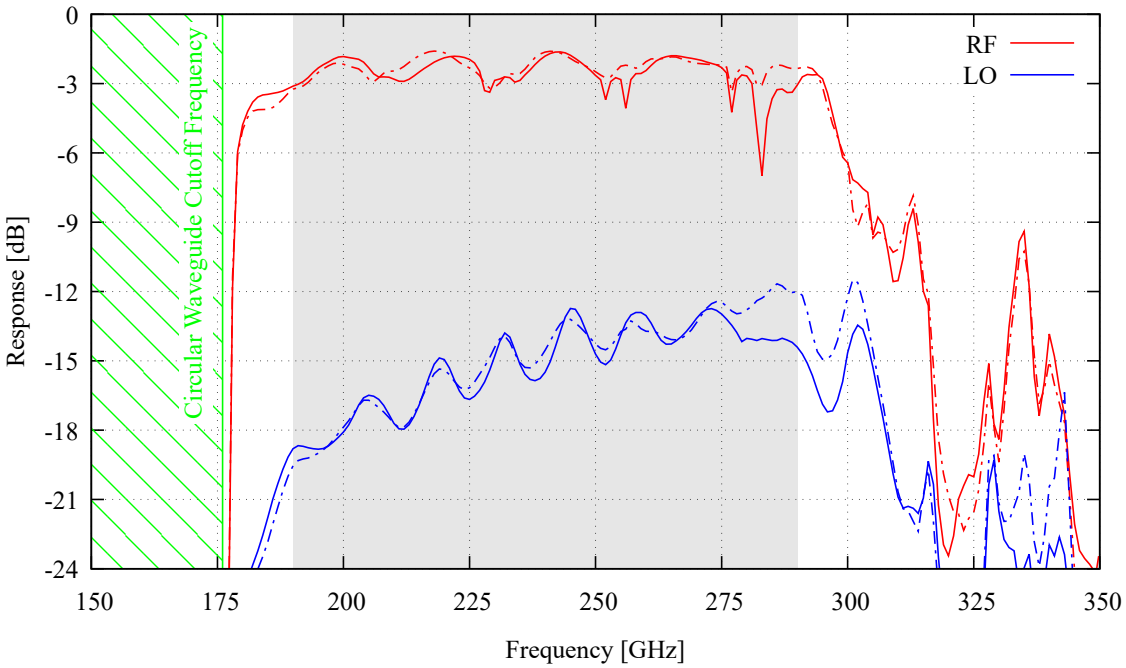


Figure 8.18: The predicted performance of the full 2-pixel array chip, showing the total RF and LO power coupling from the circular waveguides to the SIS mixers of Pixel 1. The responses of both pixels are identical, where Pol. 1 performance is shown with solid lines, and Pol. 2 with dash-dotted lines.

suspect that the standing waves are caused by the imperfect impedance matching between the different circuit components and/or by the –6 dB return loss and coupling between the branches of the power combiner. The prior issue could be resolved by re-optimising the impedance transformers deployed at different stages. The performance of the power combiner can be improved using a different methodology to reduce the return loss of the input ports. A more detailed description of the power combiner is given in Appendix C. However, it is worth noting that because we cascade these sub-circuits to form the full-chip model, a small artificial impedance miscalculation in HFSS could also cause these coupling level undulations. This is because an accurately calculated port impedance of the sub-circuits requires a high number of meshing passes in HFSS, which inevitably increases the model size and results in an impractically long simulation run. For this reason and to incorporate learnings from the experiments with the first receiver design, the performance was not further optimised as the current results are sufficient to show the principle of integrating a balanced dual-polarisation receiver upon our first design.

8.5 Conclusion

We have described the design of a 2-pixel 240 GHz dual-polarisation balanced SIS mixer array. The main difference between this design and the design presented in Chapter 5 is the use of a planar LO injection scheme that enables the construction of a balanced mixer array, further improving the receiver performance by removing unwanted LO noise. We described in detail the electromagnetic design of the additional components required to form the balanced receiver chip, as well as presented their predicted performance. Finally, we integrated all these optimised circuit components to form the full-chip model and discussed the overall performance of the 2-pixel receiver array. We showed that we could achieve good and uniform coupling for both pixels in both polarisation states, demonstrating the feasibility of constructing such a 2-pixel array with planar on-chip technology. Thus, we demonstrated that our approach of extending the array size via planar on-chip technologies is achievable without sacrificing the bandwidth performance of the array. Although our design couples more than –3 dB RF power from the circular waveguide to the SIS junctions, there is still potential for improvements, such as improving the return loss performance of the power combiner and minimising the coupling undulations of the receiver chip. Some work towards achieving these improvements is summarised in Appendix C. An im-

plementation of these finding in this receiver design requires further work beyond the time scale of this thesis.

Chapter 9

Conclusion

The sub-/mm heterodyne astronomy community has outstanding observatories with receivers operating near the quantum limit. However, most of these instruments employ single-pixel dual-polarisation receivers, such as ALMA, which limits the observational speed. Consequently, mapping large-scale structures in the Universe using heterodyne receivers, such as SIS mixers, requires long observation times due to the low pixel count in most instruments. Increasing the number of pixels while keeping the sensitivity of the individual pixels at a similar level allows to reduce the required observation time.

In this thesis, we developed a single-pixel on-chip dual-polarisation receiver that can be easily deployed in focal plane arrays. Our work demonstrates this concept at 240 GHz centre frequency with 100 GHz RF bandwidth, a fractional bandwidth of 42%. The entirety of our receiver circuit is integrated into a single chip with a tiny footprint of 4.0 mm by 4.1 mm by 0.05 mm. In particular, the chip separates the two polarisation states of the signal and feeds them into two independent mixers on the same chip, which traditionally requires the use of two receivers to recover the signal information.

The detector block required to accommodate the chip has been made relatively simple to fabricate, featuring mainly drilled holes without the need for complicated 3D structures. The simplicity of the block featuring only circular waveguides and no rectangular waveguides is the main difference to the only similar on-chip receiver, amongst the higher operation frequency. These features allowed us to easily extend the operation of our device to higher operational frequencies and into a 4-pixel array, paving the way for much larger pixel count applications in large format arrays.

Our work towards achieving this work can be summarised on a chapter-by-chapter basis as follows:

Chapter 1, Introduction We introduce sub-/mm heterodyne astronomy and summarise the background.

Chapter 2, SIS Mixer Theory We introduce the fundamental theory of SIS mixers, which is essential for this thesis. The large signal analysis is used in Chapter 4, and the small signal analysis is used within the Supermix in Chapter 5.

Chapter 3, Reflection Coefficient Analysis of Twin Junction Tuning We analyse the impedance matching of twin-junction mixers. The reflection coefficient between a feeding RF circuit and the twin-junction circuit is analysed for different circuit arrangements to guide the design of the dual-polarisation receiver. A novel feature of this work is the derivation of analytical expressions for the reflection coefficient. We also show more comprehensive and additional methods for designing the twin-junction to the conventional quarter-wavelength transmission line. The work in this chapter is useful for designing and understanding the twin-junction mixer used in Chapter 5 and future twin-junction mixer designs. The development of an application for a systematic analysis for the response over frequency would benefit the practical application of the equation set in future projects.

Chapter 4, Embedding Impedance Recovery We derive equations and extend the established embedding impedance recovery methods for single junction mixers to recover the embedding impedance of twin junction mixers. This new equation set to recover the embedding impedance is important to characterise the fabricated dual-polarisation receiver experimentally. In addition, we include the influence of the IF circuit impedance on the recovered embedding impedance. The data of a THz receiver is analysed to emphasise the strength of this method on a well-functioning receiver. The project is currently summarised in a publication but a consequent implementation as software tool, such as Supermix or QMix [44], would make this work more user-friendly applicable to the community.

Chapter 5, Single-Pixel On-Chip Dual-Polarization Receiver Design We present the on-chip dual-polarisation receiver design. We use a 4-probe OMT to couple the RF and LO and to split the incoming signal into two RF polarisation states before they are routed to the twin junction $Nb/AlO_x/Nb$ mixers via a planar crossover, branch-line hybrids and bandpass filters. The design procedure is structured similarly to the text structure, where circuit elements are first designed individually and

then combined to form two subsystems that form the full receiver chip. We show the receiver layout and extensive performance predictions. The chapter not only presents a receiver design but also illustrates the required workflow to achieve such a receiver design. Independent of our experimental results, this workflow is generally applicable and can be used in future projects.

Chapter 6, Setup for Experimental Investigation We summarise the experimental setup used to test the receiver. We start by presenting the design of the block housing the receiver chip and then show the simplicity of extending it to a focal-plane array block. We describe in detail the preparation of the receiver and its deployment in the cryostat. Upon describing these components, we give an overview of the whole experimental setup, dividing it into subsystems and summarising the sequence required to conduct an experiment. The improved modular setup and software package upgrades accelerate and improve current experiments and ease future adjustments.

Chapter 7, Experimental Results We summarise the experimental results, interpretations and consequences of these findings. A major consequence of our findings is the modification of the photolithography mask set to fabricate SIS junctions with larger areas. We show the effect on the simulated performance, the results of coupling the LO signal into the receiver, and the effects of polarising the LO signal. The required future work includes a refinement of the fabrication process to achieve and compare to the designed performance, or an adoption of the receiver design to the current fabrication process. Very likely, both adjustments are needed to achieve a competitive SIS receiver. The already available receiver chips can be used to improve the fault finding process and identify weaknesses, accelerating the next design iteration.

Chapter 8, 2-Pixel On-Chip Dual-Polarization Balanced Receiver Design We present the design of a balanced dual-polarisation receiver with on-chip LO distribution. The design is a 2-pixel demonstrator for a potential 16-pixel receiver. The design is an extension and modification of the receiver design in Chapter 5, with three additional circuit elements required for the LO injection scheme to ensure that all mixers receive the same LO power. The LO power coupled on the chip and reserved for the future 16-pixel extension has no termination mechanism designed yet. The termination can be done with RF power-absorbing materials, resistors, or patch

antennas in future design refinements. The work in this chapter shows some possibilities that can be implemented upon achieving a good single pixel receiver design.

As a whole, the work of this thesis is a step towards realising on-chip integrated SIS receivers. However, as our investigation shows, the resulting circuit is very complex and, therefore, delicate and difficult to test. The challenges solved in fabrication by increasing the junction size are not the only difficulties to overcome before achieving a state of the art receiver. In particular, the high integration level of the superconducting circuit prevents effective experimental verification and optimisation. As a solution, we suggest to focus on simple designs in the future, for instance by attaching the 4-probe OMT to four SIS mixers, as described in Appendix B.1. This design can act as a simple dual-polarisation receiver, or as a test setup for the OMT circuit element.

We want to stress that the on-chip receiver integration is also an opportunity. Instead of transforming existing receiver architectures into planar circuits, on-chip circuits offer advantages that cause difficulties when realised with optical or waveguide components in classic receiver setups. An example for an advantage is the OMT, where the power of a polarisation splits evenly between a set of opposing probes with 180° phase difference. As we show in more detail in Appendix B.2, a design using this phase difference to form a balanced receiver setup is a much more compact concept than existing receivers, which have first a polarisation splitting circuit element, then an antenna coupling the signal of each polarisation on the chip and finally split this signal with a phase-difference to achieve with LO injection balanced mixer operation. Thus, the next on-chip integrated dual-polarisation receiver should exploit the advantageous opportunities of the planar integration, while having a very simple design and making the extension to a focal plane array feasible.

Appendix A

General Design Techniques

In this appendix, we define some basics we used for the design of SIS mixer receivers. The motivation is to avoid repetition and understand, for example, the implications of the fabrication process on the design process. We also use this appendix to highlight some key items with regard to the extensive simulations performed during the design process and basic circuit theory.

A.1 RF Network Analysis and Transmission Line Theory

The electromagnetic wave identity of the signal is the main difference between DC and RF electronics. In DC electronics, circuit elements are lumped and connected without losses, such as setting two resistors in parallel with a lossless wire. In RF engineering, however, the length of this lossless wire plays an important role as it introduces a phase shift to the signal.

Wires in RF engineering are typically distributed elements called transmission lines [26]. The voltage and current of a wave travelling along the line are related by the characteristic impedance Z_0 and propagation constant γ at each point of this transmission line. In the lossless limit, Z_0 is real, and $\gamma = i\beta$ is imaginary, where β is the phase constant.

In analogy to optics, a signal gets reflected if the medium changes, e.g. if a transmission line is connected to a load with a different impedance. The impedance mismatch causes signal reflections back into the transmission line, not propagating into the load impedance Z_L, as shown in Figure A.1. The reflection coefficient, the ratio of reflected and incident voltage, depends on the impedances connected by [26]

$$\Gamma = \frac{Z_\mathrm{L} - Z_0}{Z_\mathrm{L} + Z_0} \ . \tag{A.1}$$

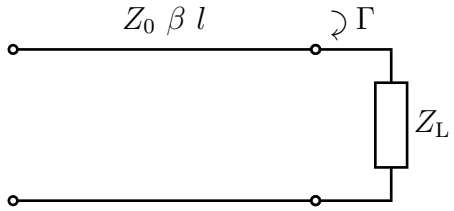


Figure A.1: A terminated transmission line. The load impedance Z_L terminates the transmission line with a characteristic impedance Z_0, propagation constant β and length l. An impedance mismatch between these components causes signal reflections at their interface, characterised by Γ.

Networks are typically treated as black boxes with n accesses named ports. The energy entering and especially exiting the black box is measured at the ports. The scattering (S) parameter matrix relates the incident voltage amplitude at port a with the exiting voltage amplitude at port b of this black box [126, 127]. The coupling from port a to b is represented by the parameter S_{ba}. Our example in Figure A.1 has $\mathrm{S}_{11} = \Gamma$ defined above. If $Z_\mathrm{L} = Z_0$, $\mathrm{S}_{11} = \Gamma = 0$, and the incident voltage amplitude propagates into the load impedance without any reflections at the interface.

In case $\mathrm{S}_{11} = \Gamma \neq 0$ and the reflections are too large, an impedance transformer can be designed, which steps the load impedance to the desired Z_0 with smaller reflections. Impedance transformers are 2-port networks. The S-parameters of a 2-port network are

$$\begin{pmatrix} V_1^- \\ V_2^- \end{pmatrix} = \begin{pmatrix} \mathrm{S}_{11} & \mathrm{S}_{12} \\ \mathrm{S}_{21} & \mathrm{S}_{22} \end{pmatrix} \begin{pmatrix} V_1^+ \\ V_2^+ \end{pmatrix} , \tag{A.2}$$

where V_n^- is the voltage exiting the n^{th} port, and V_n^+ is the voltage amplitude incident at the n^{th} port.

Common setups, including impedance transformers, cascade several 2-port networks, which is not straightforward with S-parameter matrices. Instead, the S-parameters of each 2-port network are converted into an ABCD matrix. These ABCD matrices are multiplied to a single 2-port network, which then can be converted back into an S-parameter matrix [26].

The ABCD matrix relates the voltage V_1 and current I_1 at port 1 with the voltage V_2 and current I_2 at port 2 by

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} \mathrm{A} & \mathrm{B} \\ \mathrm{C} & \mathrm{D} \end{pmatrix} \begin{pmatrix} V_2 \\ I_2 \end{pmatrix} . \tag{A.3}$$

The serial impedance transformer consists of a transmission line with characteristic impedance Z_0, propagation constant β and length l. Their ABCD matrix is given

by [26]

$$\begin{pmatrix} \mathrm{A} & \mathrm{B} \\ \mathrm{C} & \mathrm{D} \end{pmatrix}_{\text{Transmission Line}} = \begin{pmatrix} \cos(\beta l) & iZ_0 \sin(\beta l) \\ i\frac{\sin(\beta l)}{Z_0} & \cos(\beta l) \end{pmatrix} . \tag{A.4}$$

Several impedance transformer sections can be cascaded by multiplying their ABCD matrices. The load impedance Z_L in Figure A.1 can be represented by a shunt admittance ABCD matrix by

$$\begin{pmatrix} \mathrm{A} & \mathrm{B} \\ \mathrm{C} & \mathrm{D} \end{pmatrix}_{\text{Shunt Admittance}} = \begin{pmatrix} 1 & 0 \\ Y_\mathrm{L} & 1 \end{pmatrix} \tag{A.5}$$

and $I_2 = 0\,\mathrm{A}$ because the shunt admittance $Y_\mathrm{L} = Z_\mathrm{L}^{-1}$ terminates the network. A single-section impedance transformer with this load admittance in ABCD matrix representation is

$$\begin{aligned} \begin{pmatrix} V_1 \\ I_1 \end{pmatrix} &= \begin{pmatrix} \cos(\beta l) & iZ_0 \sin(\beta l) \\ i\frac{\sin(\beta l)}{Z_0} & \cos(\beta l) \end{pmatrix} \begin{pmatrix} 1 & 0 \\ Y_\mathrm{L} & 1 \end{pmatrix} \begin{pmatrix} V_2 \\ 0 \end{pmatrix} \\ &= \begin{pmatrix} \cos(\beta l) + iY_\mathrm{L} Z_0 \sin(\beta l) & iZ_0 \sin(\beta l) \\ Y_\mathrm{L} \cos(\beta l) + i\frac{\sin(\beta l)}{Z_0} & \cos(\beta l) \end{pmatrix} \begin{pmatrix} V_2 \\ 0 \end{pmatrix} \\ &= V_2 \begin{pmatrix} \cos(\beta l) + iY_\mathrm{L} Z_0 \sin(\beta l) \\ Y_\mathrm{L} \cos(\beta l) + i\frac{\sin(\beta l)}{Z_0} \end{pmatrix} . \end{aligned} \tag{A.6}$$

The matrix in the second line could be converted into a 2-port S-parameter matrix. Furthermore, the last line can be used to calculate the input impedance into the 1-port network

$$Z_\mathrm{in} = \frac{V_1}{I_1} = Z_0 \frac{Z_\mathrm{L} + iZ_0 \tan(\beta l)}{Z_0 + iZ_\mathrm{L} \tan(\beta l)} , \tag{A.7}$$

where we applied $Z_\mathrm{L} = \frac{1}{Y_\mathrm{L}}$ and $\tan x = \frac{\cos x}{\sin x}$ to obtain the standard terminated transmission line expression.

We will predominantly use the ABCD matrix for analytical solutions to a problem and S-parameters with FEM and network simulations. We want to stress that these matrices are interchangeable for 2-port networks.

A.2 Finite-Element Method Simulations

This thesis heavily relies on FEM simulations. In particular, Ansys HFSS has been used to design the receiver. HFSS is a full-wave FEM that utilises adaptive meshing to solve Maxwell's equations in a simulation space with arbitrary-defined 3D structures.

The user defines geometric structures, their materials, and boundary conditions. Boundary conditions can be of various forms, such as surfaces in the simulation space

radiating away energy, surface impedances, and excitations to the simulation space, referred to as ports. The S-parameters of the solved model can be therefore used to represent it as an n-port network. The user also defines the simulation setup, such as the frequency/ies to be solved for meshing, the conditions for stopping the adaptive meshing process, and the frequency range of interest.

The user-defined geometry is used to generate a first initial mesh forming tetrahedrons. Subsequently, this initial mesh is refined to tetrahedrons that are smaller than the solved wavelength. The Maxwell equations are then solved for all finite element tetrahedrons of the model. HFSS determines the tetrahedrons with the largest errors, refines the mesh and solves the electromagnetic fields again. This adaptive meshing process is repeated until the stopping criterion is fulfilled, yielding a mesh like the one shown in Figure A.2.

The stopping criterion is determined by the maximum change of the scattering parameter magnitude between the last and previous solution. The standard value for this Maximum Delta S criteria is typically 2%. Increasing Maximum Delta S to 5% requires fewer iterations to obtain a solution and computational resources, however, with the caveat of the increased inaccuracy in the solution. We show the solved against the possible S-parameter values in Figure A.3. All simulations shown in this thesis have been computed with a 2% Maximum Delta S, which allows little deviation between solved and possible S-parameter down to –20 dB.

A.2.1 Surface Impedance

Although HFSS materials can be assigned to a frequency-dependent complex bulk conductivity, the technical notes documentation recommends that the surface impedance boundary condition is advantageous for metal traces with finite thickness. The advantages are to avoid solving within conducting objects, ensuring causality, and, therefore, achieving correct impedance values.

The surface impedance is complex and can be written as

$$Z_{\mathrm{S}} = R_{\mathrm{S}} + iX_{\mathrm{S}} \ , \tag{A.8}$$

where R_{S} is the surface resistance, and X_{S} is the surface reactance. The surface impedance of a conductor with finite thickness t is given by [128]

$$Z_{\mathrm{S}} = \frac{k}{\sigma} \frac{e^{kt} + \frac{\sigma Z_\eta - k}{\sigma Z_\eta + k} e^{-kt}}{e^{kt} - \frac{\sigma Z_\eta - k}{\sigma Z_\eta + k} e^{-kt}} \ , \tag{A.9}$$

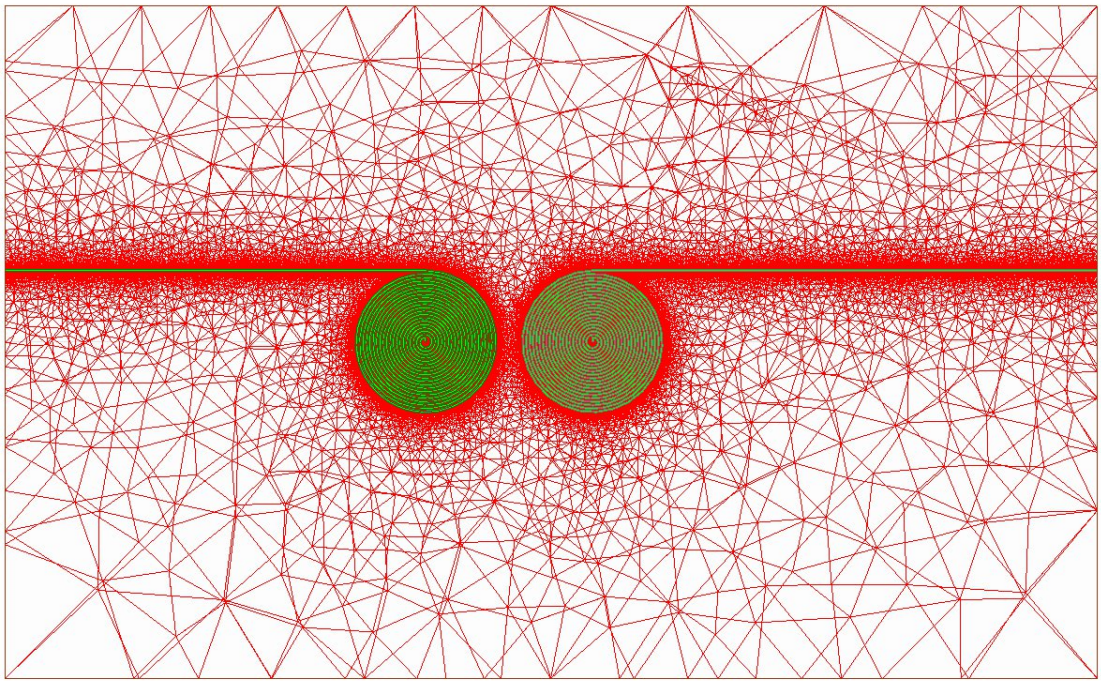


Figure A.2: The mesh of tetrahedrons of a model with two coil spirals for a planar solution for suppressing Cooper pair tunnelling in SIS junctions. The tetrahedrons are only shown on the surface underneath the green coil traces. Due to the proximity to the excited structure, the number of tetrahedrons near the green wire is much higher than at the boundary of the model.

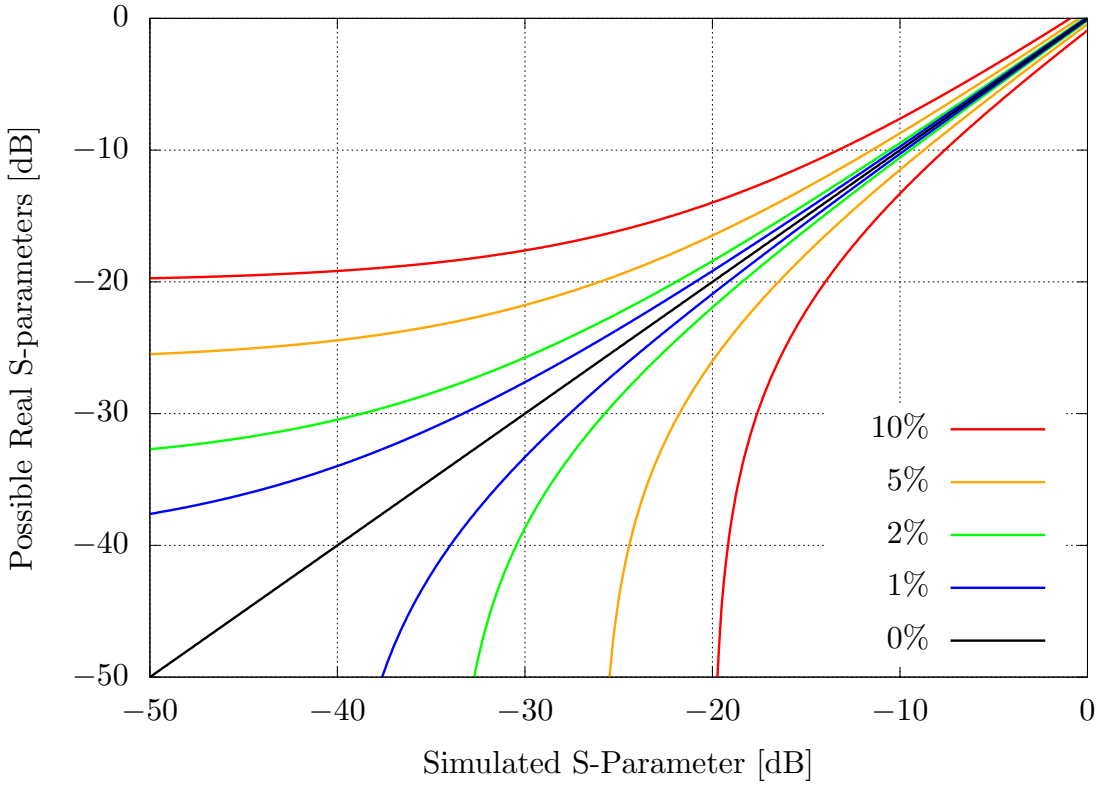


Figure A.3: The S-parameter FEM solution against the possible real S-parameter values for different Maximum Delta S criteria. 0% indicates an ideal match between simulation and real value. The solution possibilities are around this optimum to the limits indicated for a finite Maximum Delta S.

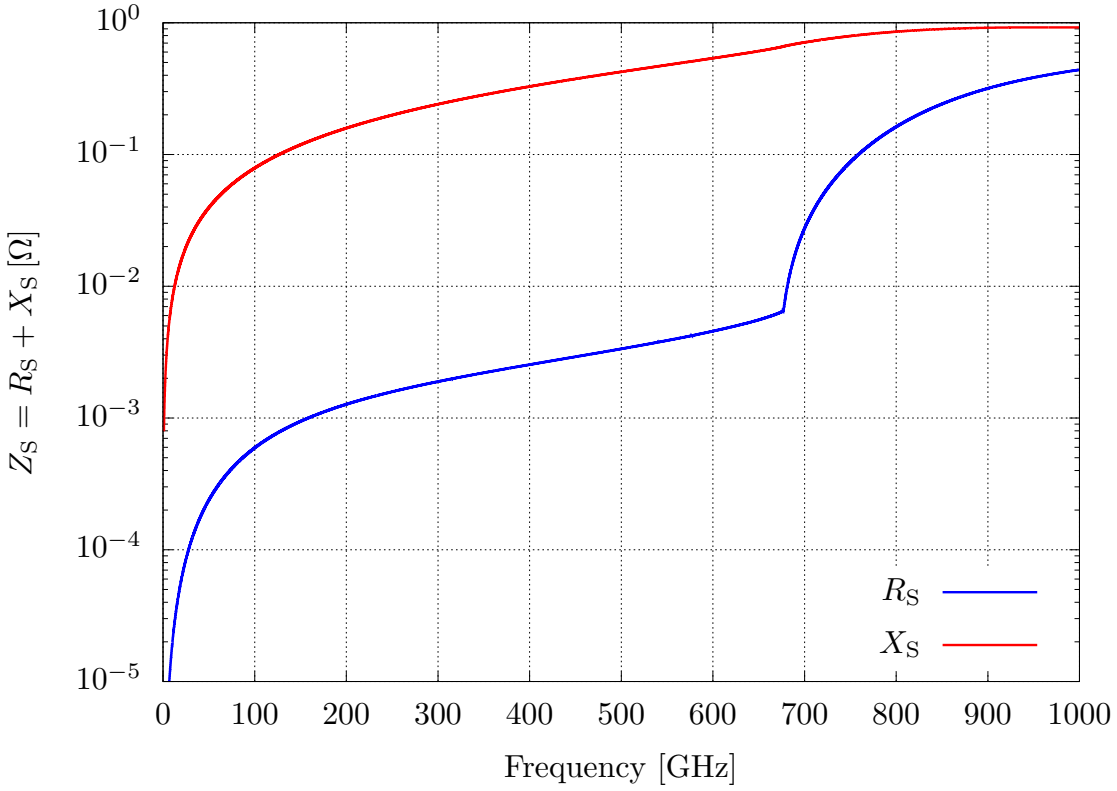


Figure A.4: The simulated surface impedance of a 400 nm thick niobium sheet with $\sigma_n = 1.23\,10^7\,\frac{1}{\Omega m}$ and $\frac{\Delta}{e} = 2.8\,\mathrm{mV}$ at $T = 4.2\,\mathrm{K}$.

where $Z_\eta = \sqrt{\frac{\mu_0}{\epsilon_0}}$ is the free-space impedance, $k = (1+i)\sqrt{\frac{\omega\sigma\mu}{2}}$, and σ is the complex conductivity, which depends on the angular frequency ω.

A common technique for implementing the surface impedance in HFSS is fitting the real and imaginary surface impedance component with a polynomial over frequency. This polynomial fit can, however, introduce errors if they are used from very low to higher frequencies which is the case for the RF and IF signal, for instance. Certainly, the discontinuity at the frequency of the Cooper pair binding energy ($\hbar\omega = 2\Delta$) can be poorly fitted with a polynomial. In particular, in such cases, inputting the surface impedance for every frequency over the desired frequency range is beneficial. HFSS's piecewise linear input function assumes a linear change of the surface impedance between two adjacent frequency data points. The dataset shown in Figure A.4 is used in our simulations and has a 1 GHz resolution.

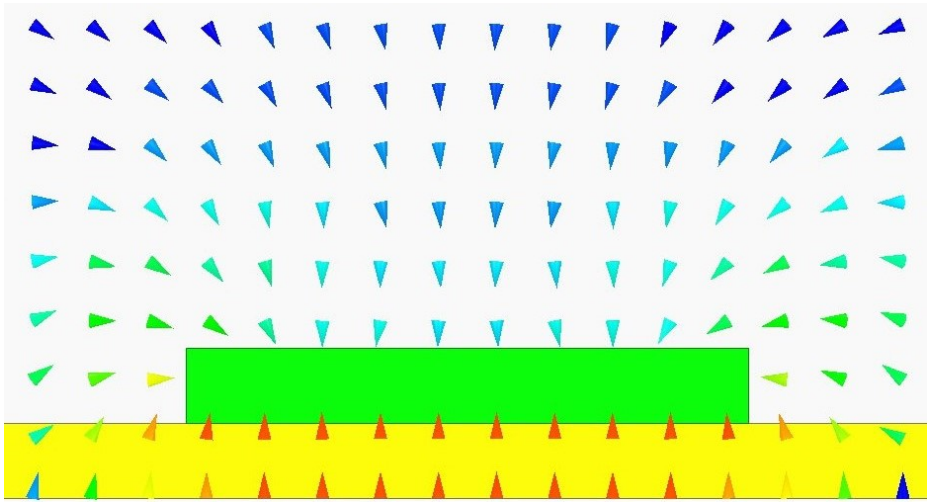


Figure A.5: The electric field vectors for the cross-section of a microstrip. The microstrip line is green, and the dielectric is yellow. The ground layer is underneath the dielectric, and vacuum is above the dielectric. The field strength is colour-coded to the vectors, with blue indicating a small and red a large electric field.

A.2.2 Superconducting Microstrips

The designs presented in this thesis use microstrip transmission lines for propagating the RF signal through the mixer components. We show in Figure A.5 a specimen of a microstrip cross-section: A trace of width w sits on top of a dielectric layer with a thickness t that covers the ground plane. The space above the dielectric is typically filled with vacuum with $\epsilon_\mathrm{r} = 1$.

The ϵ_r difference between the vacuum and dielectric prevents pure TEM modes from propagating due to the different phase velocities in the materials [26]. However, most of the field lines shown in Figure A.5 are tightly confided between the trace and ground plane in the dielectric due to $w = 7.5t$ in the shown example. In practice, a quasi-TEM mode propagates because the dielectric thickness is much smaller than the wavelength of the signal. Moreover, the small portion of the electric field leading through the vacuum is accounted for by introducing the effective permeability approximation

$$\epsilon_\mathrm{e} = \frac{\epsilon_\mathrm{r} + 1}{2} + \frac{\epsilon_\mathrm{r} - 1}{2} \frac{1}{\sqrt{1 + 12\frac{t}{w}}} \,, \tag{A.10}$$

where ϵ_r is the dielectric constant of the dielectric layer between the trace and ground plane. In the description of Schneider [1969], the factor 12 is 10, which is insignificant for our cases where $\frac{t}{w} \ll 1$.

We are interested in properly representing superconducting materials within our

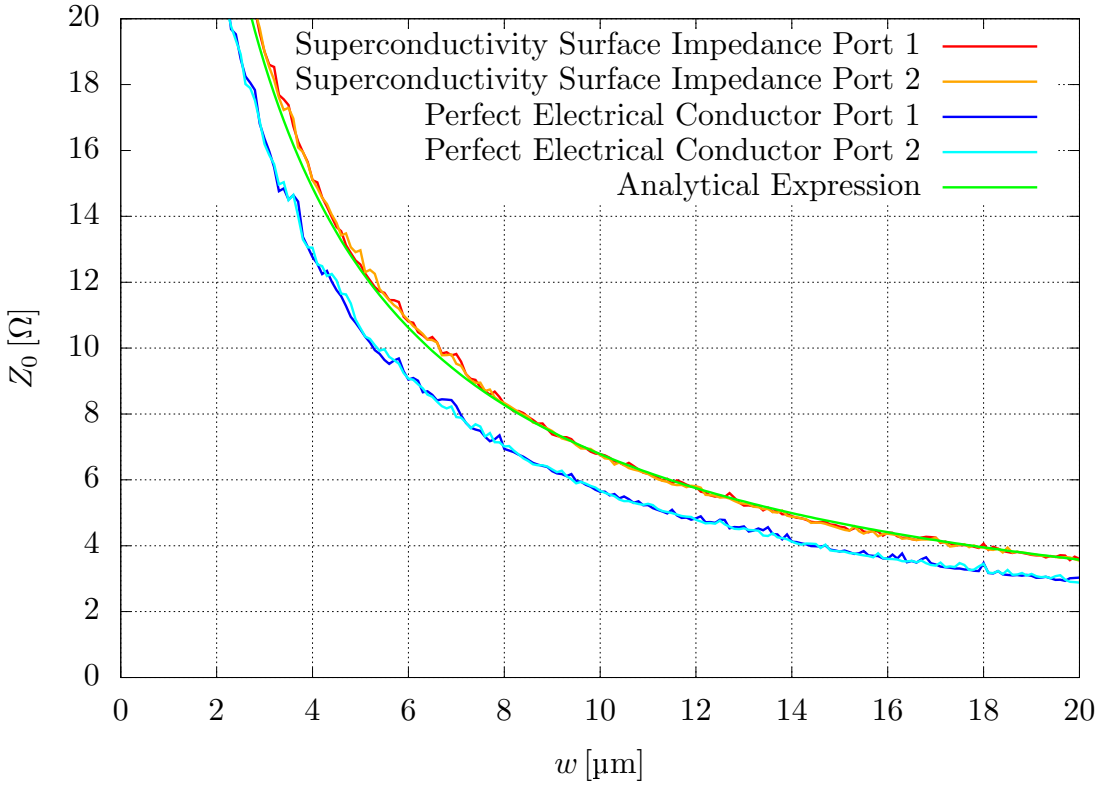


Figure A.6: A comparison of characteristic impedances of microstrips with different trace widths. The HFSS simulations with a surface impedance assignment representing superconductivity agree well with the analytical expression. The simulated response of a perfect electrical conductor without surface impedance assignment illustrates the effect of superconductivity on Z_0.

HFSS simulations. Yassin and Withington presented a full theoretical description of superconducting microstrip lines [129]. This paper was especially important before the advent of FEM simulation software packages, but it is still an important metric for the validation step of the simulation process. Figure A.6 shows the characteristic impedances of superconducting microstrips as a function of the trace width w calculated from the theoretical expressions and using HFSS. The agreement of the curves confirms that the surface impedance assignment reflects superconductivity appropriately. Furthermore, the small variations between the solutions for the two ports connected to the same microstrip show the errors introduced by the FEM. We also show the characteristic impedances calculated for a perfect electrical conductor without surface impedance assignment to illustrate the effect of superconductivity on the simulations.

A.3 Network Simulations

The propagation of high-frequency electromagnetic waves in a superconducting transmission line with complex geometry is difficult to analyse rigorously. Our simulation tool is Ansys Electronics Desktop, a commercial software solution for RF and integrated circuit (IC) design, which also features multi-physics extensions for magnetic, mechanical and thermal analysis. Our interest is in the FEM application, discussed in Section A.2, and the schematic editor. The schematic editor, called Ansys Circuit, allows the analysis of graphically interconnected parametrised models of a standard library. One standard component is the S-parameter n-port network, which can be dynamically linked to the corresponding FEM model and its parameters. The graphical representation of components as symbols and interconnections as wires allows for a well-structured electric circuit schematic.

Although Ansys Circuit is capable of including commercially available mixers in a circuit schematic and analysing these circuits, the software has no obvious way of including Tucker's theory, presented in Chapter 2. Therefore, we utilise the Supermix C++ library [113, 114]. Supermix has been developed to model SIS mixers and to apply Tucker's theory when developing superconducting heterodyne receivers. The SIS receiver model can be formed from various lumped and distributed circuit components or again from an n-port network S-parameter representation. The components are identically interconnected as with Ansys Circuit described above, but now, with C++ functions, objects and methods instead of the user-friendly wires interconnecting boxes on a graphical user interface.

Generally, the Supermix analysis is more complex than the analysis with Ansys Circuit: RF, IF and DC circuit objects must be initialised separately because the RF port differs from the IF port. Furthermore, the individual circuits are only allowed to have one port for excitation. The remaining ports have to be terminated. For instance, in our dual-polarisation receiver, only one RF polarisation can be excited while the other RF polarisation has to be terminated. Consequently, the simulation is executed twice to get the information for both polarisations. Another complication is that the excited and terminated RF ports require additional perfect impedance transformers in Supermix to transform the frequency-dependent wave impedance of the hollow waveguide to a constant characteristic impedance matching the network impedance. Ansys Circuit includes this impedance transformer in the port definition and dynamically imports the impedance matrix from the FEM model.

The SIS junction is the only other port besides the excitation port. A model can have more than one SIS junction. SIS junctions in Supermix are characterised by their operational temperature, gap voltage and normal resistance. The geometric capacitance can be assigned to the Supermix SIS junction object or accounted for by the circuit, such as within the n-port network black box.

Supermix, in principle, solves the Tucker expressions introduced in Chapter 2. We take three harmonics into account for our simulations and follow the description in the source code examples. However, we use a different solution setup to the classical calculation of mixer gain and noise temperature T_{N}. The mixer gain and T_{N} are calculated classically for user-defined constant LO power P_{LO} and DC bias voltage V_0 of the SIS junction at a certain IF f_{IF} while sweeping the LO frequency f_{LO} across the spectrum. This method, however, reflects not real experiments because an experimentalist would adjust P_{LO} and V_0 to obtain the best T_{N} at a given f_{LO}. The more realistic software solution sweeps across a reasonable range for P_{LO} and V_0 for each f_{LO}, and either the best T_{N} or best mixer gain is recorded in the dataset, depending on the design philosophy followed. We prefer to maximise the mixer gain as, from Friss law, this reduces the contribution of subsequent non-simulated IF components to the total system noise temperature T_{sys} discussed in the introduction Equation 1.3 [130]. Figure A.7 shows that P_{LO} and V_0 vary with f_{LO}. The comparison to the result for constant $P_{\mathrm{LO}} = 90\,\mathrm{nW}$ and $V_0 = 2.6\,\mathrm{mV}$ shows the possible improvement which can be achieved using this method. We used a single-polarisation finline antenna receiver and the existing FEM model to generate this comparison because the model is less complex than the dual-polarisation receiver allowing for a simpler Supermix setup.

A.4 Fabrication and Receiver Chip Topology

The fabrication procedure and receiver chip topology inherently depend on each other. Our group has collaborated with Faouzi Boussaha's group with specialised fabrication facilities in the Observatiore de Paris for several years [131]. The dual-polarisation receiver designs in this thesis build upon these successes by using the same fabrication process. As a consequence, the topology of the individual layers on the receiver chip is already predefined. The fabrication processes can be split into three categories:

1. **Photolithography:** The substrate is uniformly covered with a photoresist and then exposed to ultraviolet light through a mask. Either the exposed or unexposed photoresist becomes soluble in the developer solution, depending on the type of photoresist. After the photoresist is developed, the wafer is

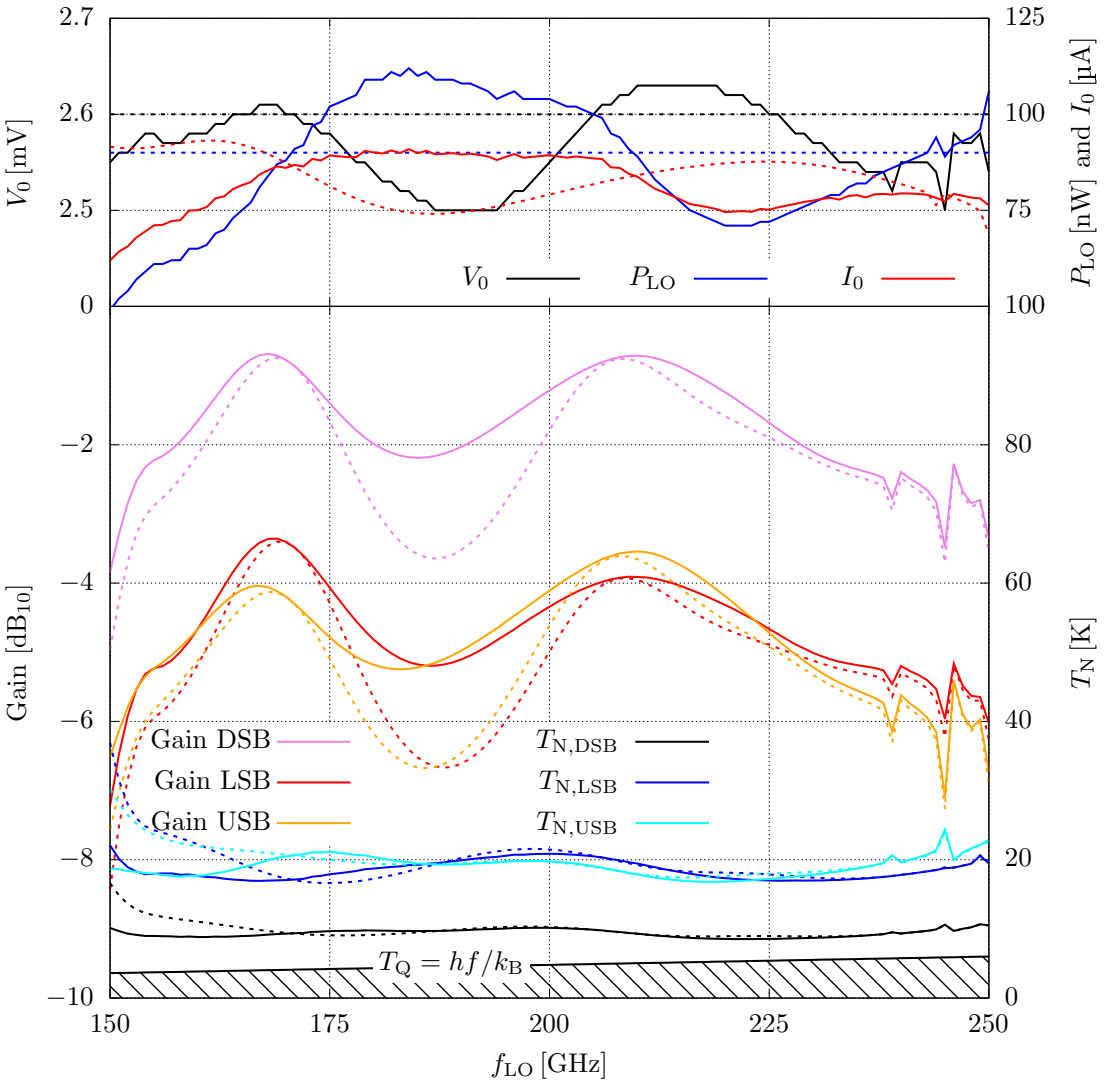


Figure A.7: Supermix gain and noise temperature T_N predictions optimised by varying the bias voltage V_0 and LO power P_{LO}. The resulting gain and T_N are shown in the lower panel at $f_{IF} = 5\,\text{GHz}$. The upper panel shows the varying bias voltage DC bias voltage V_0 and current I_0, which follows from V_0, and local oscillator power P_{LO}. The dotted lines correspond with constant values for $P_{LO} = 90\,\text{nW}$ and $V_0 = 2.6\,\text{mV}$.

treated with deposition or etching processes, and subsequently, the developed photoresist is removed with acetone in a process called liftoff. We refer to each iteration of this photoresist process as a fabrication step because each step has its photolithography mask. The masks are prepared from 2D AutoCAD and KLayout drawings, which are exported slices for each layer of the HFSS 3D model. The masks contain several copies and design variations to maximise the number of chips fabricated on a 2 inch wafer in one fabrication batch.

2. **Deposition:** Thin films are uniformly deposited on the whole wafer, and shapes are defined by dissolving the photoresist underneath some parts of this film during the liftoff. As the name suggests, the films on top of the dissolving photoresist lift off the wafer into the acetone bath. There are two main ways of thin-film deposition: Sputter deposition and evaporation, a physical and thermal vapour deposition process, respectively. In evaporation, the material in the evaporator vacuum chamber is heated until it evaporates and then deposits on the wafer (and everywhere else in the vacuum chamber). The sputtering process generates a plasma from the noble gas Ar and accelerates the Ar ions from the plasma to hit a target of the material to be deposited. The incident, relatively heavy Ar ions sputter or eject target material, which then deposits on the wafer and forms a film. SiO, which forms the dielectric material for the microstrip, Au, used to improve the adhesion of the bond wire, and Ti, used to improve the adhesion of Au on Nb, are evaporated. Nb, which forms the superconducting material for the SIS tunnel junctions and on-chip transmission lines, and Al, used as the base layer for the SIS junction isolator, are sputtered. AlO_x is formed by passivating the Al with O_2 and air.
3. **Etching:** Some applications require the removal of thin films from the wafer. We use reactive ion etching (RIE) to remove thin-film material from our wafer. A plasma is generated by applying AC on the electrodes in the vacuum chamber. In contrast to the noble gas in sputtering, RIE uses highly reactive radicals, in particular, O and F. O^+ reacts with C-chains in the photoresist, and F^+ reacts with the thin film metals, such as Nb and Al. RIE is used to define the SIS junction area.

Our receiver chips are fully planar, formed mainly from microstrip transmission lines. The common microstrip topology eases the design and connection of on-chip circuit elements without transitions to other transmission line topologies while providing a common ground throughout the chip. The circuit is fabricated on a quartz substrate with a relative permittivity $\epsilon_r = 3.78$ in a 5-step process, summarised in

Step	Description	Material	Thickness
1	Deposition trilayer	$Nb/AlO_x/Nb$	400/1/200 nm
2	Etching junctions from trilayer	Nb Remains	400 nm
	Deposition of first dielectric	SiO	200 nm
3	Deposition of second dielectric	SiO	200 nm
4	Deposition of wiring layer	Nb	400 nm
5	Deposition of bonding pads	Ti/Au	10/150 nm

Table A.1: The 5-step planar-circuit thin-film deposition process.

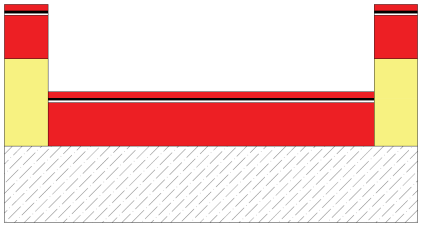
Table A.1. In the first step, the 14 kA/cm^2 $Nb/AlO_x/Nb$ trilayer is deposited on all areas covered with the ground conductor, the whole chip except for areas at the OMT, the IF bonding pads and CPW features of the crossover and BPF, as shown in Figures A.8a and A.8b. In the second step, the trilayer is etched to the 1.5 µm^2 SIS junctions, leaving the bottom layer on the remaining areas to form the 400 nm thick Nb ground-plane layer, as shown in Figure A.8c. After etching, a first SiO layer is deposited in the same fabrication step so that the SIS junctions are self-aligned with the SiO layer and the entire ground-plane layer is covered, as shown in Figures A.8d and A.8e. In the third step, a second SiO layer is deposited, as shown in Figures A.8f and A.8g, forming a 200 nm deep 6 µm by 6 µm well where the SIS junctions are exposed to the 400 nm thick wiring layer, which is deposited in the fourth step shown in Figure A.8h. In the final step, the bonding pads are coated with a 10 nm Ti linking layer and 150 nm Au for reliable wire bonding to the chip. After completion of the deposition, the quartz substrate is diced and thinned to 50 µm.

Except for the SIS junctions, all circuit features are designed to be larger than 3 µm to ensure a reliable photolithography process. This, together with the 400 nm thick SiO ($\epsilon_r = 5.7$) layer, defines a reliably fabricated characteristic impedance of 19 Ω for the microstrips.

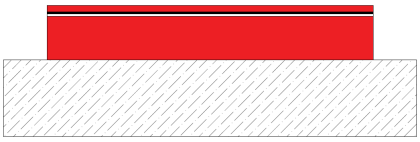
A.5 Tuning of the SIS Junction Capacitance

The on-chip circuits are required to feed the RF and LO signal into the SIS junction for mixing and downconversion. SIS junctions are very capacitive due to their geometry with a $d \approx 1$ nm thick AlO_x insulator with $\epsilon_r \approx 10$. This means that the geometric capacitance, which is defined as

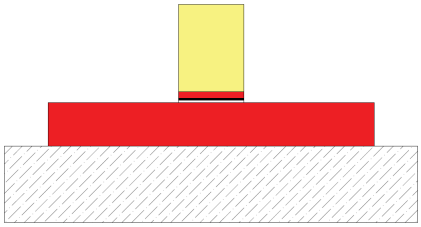
$$C = \epsilon_0 \epsilon_r \frac{A}{d} \ , \tag{A.11}$$



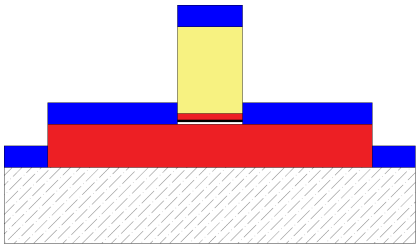
(a) Trilayer deposition;



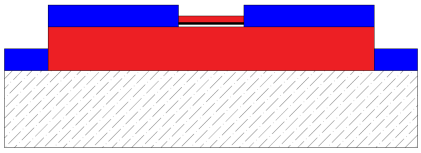
(b) Liftoff after trilayer deposition;



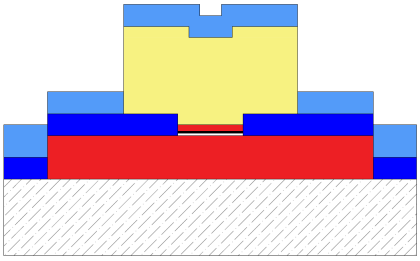
(c) After etching trilayer;



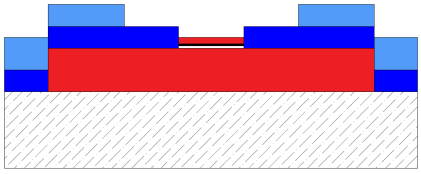
(d) First SiO deposition after trilayer etching;



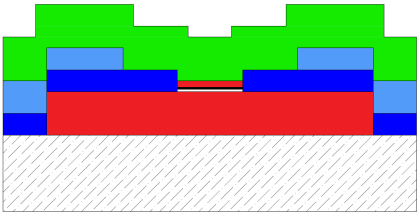
(e) Liftoff after first SiO deposition;



(f) Second SiO deposition;



(g) Liftoff after second SiO deposition;



(h) Wiring layer deposition;

Figure A.8: The thin-film topology on the wafer at different steps of the fabrication process. The quartz substrate is shown dashed. The Nb of the trilayer is shown in red, which sandwiches the passivated Al in white and black. The first SiO layer is dark blue, the second SiO layer is pale blue, and the wiring layer Nb is green. The photoresist is shown in yellow.

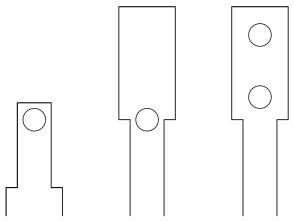


Figure A.9: The three main methods of tuning the junction's capacitance are end-loaded tuning (left), end-stub tuning (middle), and twin junction tuning (right). Circles represent the SIS junctions. The lines define the microstrip trace.

of a $A \approx 1\,\mu m^2$ SIS junction is 75 fF and that the reactance at 240 GHz is $\approx 10\,\Omega$. An important step in designing SIS mixers is the cancellation of the junction's capacitance which would otherwise short high-frequency signals, and to maximise the coupling of the feeding RF circuit to the SIS mixer.

Figure A.9 shows the three methods to tune out the SIS junction's capacitance. All three methods are based on the terminated transmission line equation

$$Z_{\mathrm{in}} = Z_0 \frac{Z_{\mathrm{L}} + iZ_0 \tan(\beta l)}{Z_0 + iZ_{\mathrm{L}} \tan(\beta l)} \,, \tag{A.12}$$

where Z_{in} is the input impedance into the transmission line terminated by the load impedance Z_{L}, and Z_0, β and l are the characteristic impedance, propagation constant and length of the transmission line, respectively. An end-loaded tuner has the impedance of the SIS junction as load, which is transformed to a resistive input impedance. Similarly, the end-stub tuner is a transmission line which transforms the open circuit at its end ($Z_{\mathrm{L}} = \infty$) into an inductance, which cancels the capacitance of the SIS junction. A third approach, called twin junction tuning, is to connect two identical SIS junctions via a transmission line to mutually tune out the junctions capacitance. Thus, a real input impedance is achieved that can be matched to the RF circuit. The performance and bandwidth of the tuning can be broadened by modifying and combining these methods, as shown in the example in Figure A.10, where end-loaded tuning is combined with end-stub tuning. The end-stub is part of the LPF, which is used to connect the IF to the SIS junction.

A commonly used method to achieve this tuning is by using a $\approx \lambda/4$ transmission line terminated by a stub, which is an end-stub type tuning, where λ is the guided wavelength of the signal [132, 133]. While this method serves the purpose in many working receivers, it implies that the bandwidth of the mixer will not only be limited by the RF transmission line but also by the stub bandwidth [134]. Moreover, the large capacitance of the stub can severely limit the downconverted IF bandwidth,

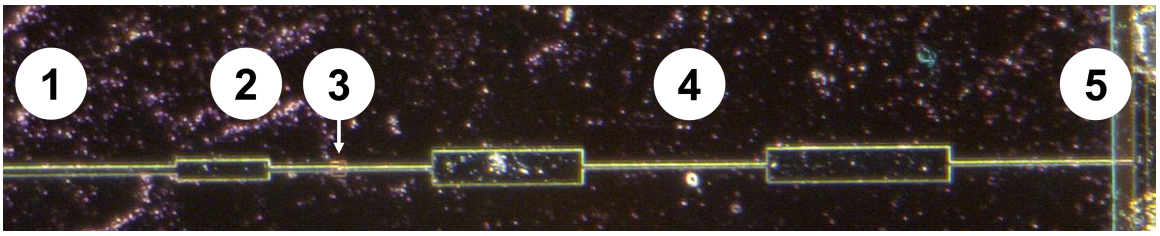


Figure A.10: Example of real mixer tuning. The RF and LO signal incident at (1) connect via an end-loaded tuning (2) to the SIS junction (3). The LPF (4) connecting the IF signal output (5) acts as end-stub tuning.

especially in mixers that aim to operate at high IF bandwidths [135]. Preliminary investigations show that solutions with end-loaded and end-stub tuning are either too narrow RF bandwidth or too complex to achieve the required performance for the work in this thesis.

A more elegant tuning mechanism that has been proposed by Belitsky et al. [136] is the twin junction tuning method which has been successfully employed in SIS mixers at several frequency bands [88, 137]. It consists of two parallel SIS tunnel junctions connected by a transmission line, typically a microstrip line. The principle of operation is based on the fact that when a transmission line with a carefully selected electrical length and characteristic impedance separating the two SIS junctions is used, the reactances of the two junctions can be made to cancel each other, and the input impedance of the device becomes real, hence can easily be matched to the feeding RF circuit. A strong feature of this design is its fabrication simplicity which enables the mixer to achieve sufficient RF bandwidth for a typical astronomical heterodyne receiver without the addition of complex tuning circuits on the mixer chip.

We use twin junction mixers in our receiver design. In Chapter 3, we give an analytical approach to designing twin junction mixers in order to understand the principle of operation in more detail. This analysis feeds into the HFSS simulations presented with the receiver design in Chapter 5. Furthermore, we developed a method for analysing the fabricated RF circuit in the lab in Chapter 4. Techniques exist for single junction mixers, but the DC through the additional SIS junction require expanding the existing techniques.

Appendix B

Minimalistic Receiver Design

The implementation of the receiver in Chapter 5 is in preparation for the balanced receiver adaption in Chapter 8. The descriptions and explanations in the chapters show the complexity of integrating a traditional dual-polarisation on a single chip. A major source of complexity is that the circuit can be tested only as a whole and that the individual components are not accessible for testing, which is the case for a classical waveguide OMT. In this appendix, we present an alternative on-chip receiver design before discussing its deployment as a balanced receiver. In this second part, we first present the planar beamsplitter circuit element to realise the LO injection and then the layout of the RF and LO coupling network without the mixer circuit.

B.1 OMT-Probe Dual-Polarisation Receiver

Figure B.1 schematically shows an alternative design concept, where the RF polarisations are separated on the chip with the planar OMT. Half of the RF power of a polarisation, which falls on each OMT probe, is fed directly into the SIS mixer without any further circuits complicating the signal path. The two IF signals of one polarisation are then combined with commercially available components, such as a hybrid or Wilkinson combiner, which requires a crossover of the IF transmission line. This crossover can be realised with coaxial cables needed for connecting IF circuit components, making the on-chip crossover of previous approaches redundant.

The OMT-probe receiver chip design shown in Figure B.2 is not only a stand-alone receiver, but also a minimalistic setup to test the OMT, which has been adopted from the receiver design in Chapter 5. The OMT-probe receiver circuit in Figure B.3 is identical for all four OMT probes. The OMT probe connects via a two-section impedance transformer to the twin junction and LPF circuit. The impedance transformer connection of the OMT probe improves the coupling of the OMT, similar to the

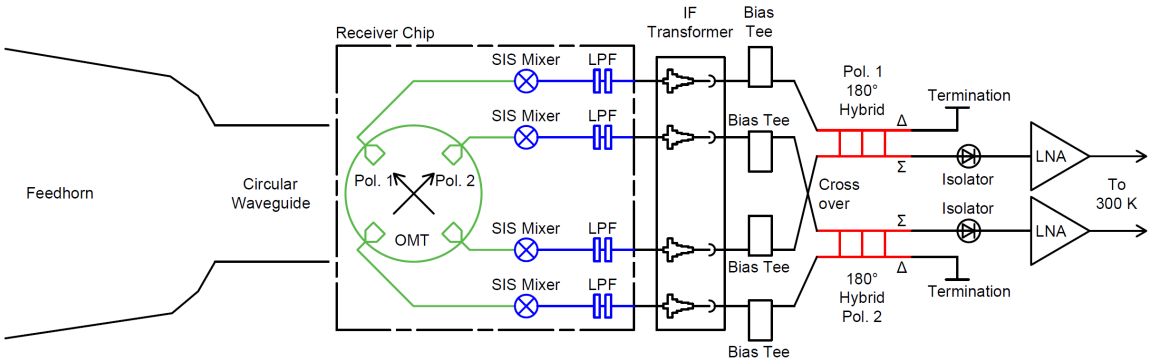


Figure B.1: The schematic of the OMT-probe dual-polarisation SIS receiver that downconverts each polarisation with two individual mixers. Components fabricated on the receiver chip are shown within the dashed rectangle, with the OMT coloured in green and the mixers circuits in blue. The 180° IF hybrid recombines the signal of one polarisation splitting between a set of opposing OMT probes. The two RF polarisations are incident at the feedhorn on the left of the schematic. The circuit and connections for the downconverted IF signals are on the right side of the schematic.

impedance transformer in the two-probe antenna of the LO distribution network in Chapter 8. Here, the serial impedance transformer, described as part of the SIS mixer circuit in Chapter 5, has been modified to be a two-section impedance transformer.

Figure B.4 shows the –2 dB coupling of the RF signal into the twin junctions. The return loss has only two poles, similar to the stand-alone OMT circuit. We designed the return loss to remain below –12 dB in the lower half of the RF bandwidth and at approximately –10 dB at frequencies above 240 GHz. The coupling to the individual SIS junctions is slightly different to the previous response, with equal coupling into the first and second SIS junctions above 250 GHz instead of at 240 GHz due to the modified impedance transformer. Importantly, the cross-coupling between the polarisations is less than –40 dB. This improvement of –10 dB to the design presented in Chapters 5 and 8 is caused by discarding the crossover and introducing the two-section impedance transformer. Similarly, the simulations show an isolation between RF and IF circuits exceeding –40 dB. The IF response is not optimised and is slightly worse than in the receiver designs in Chapter 5, which is again a consequence of the altered mixer circuit.

B.1.1 Design of the Mixer Block

The concept of extending to a multi-pixel receiver remains unchanged from the previous receivers and applies to this receiver as well. The main difference is that the

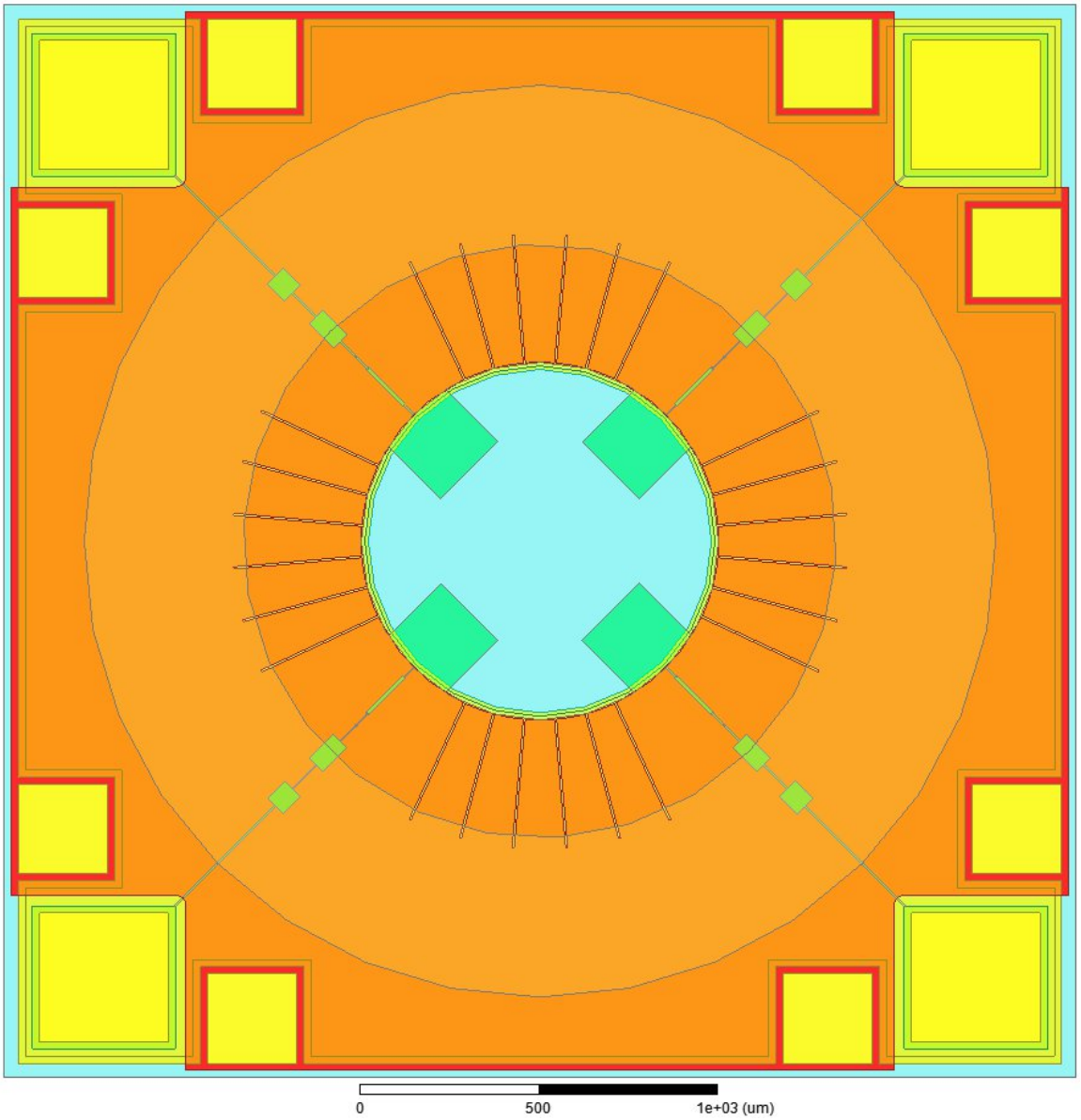


Figure B.2: The OMT-probe dual-polarisation receiver chip design on a 3 mm by 3 mm quartz dice. Each OMT probe connects to a twin junction and an LPF, which is shown in more detail in Figure B.3. The downconverted IF signal connects to the IF bonding pads at the corners of the chip. The wiring layer is shown in green, the dielectric layer is orange, and the ground plane is in red. On each side of the IF bonding pads are two bonding pads for ground connections, shown in yellow.

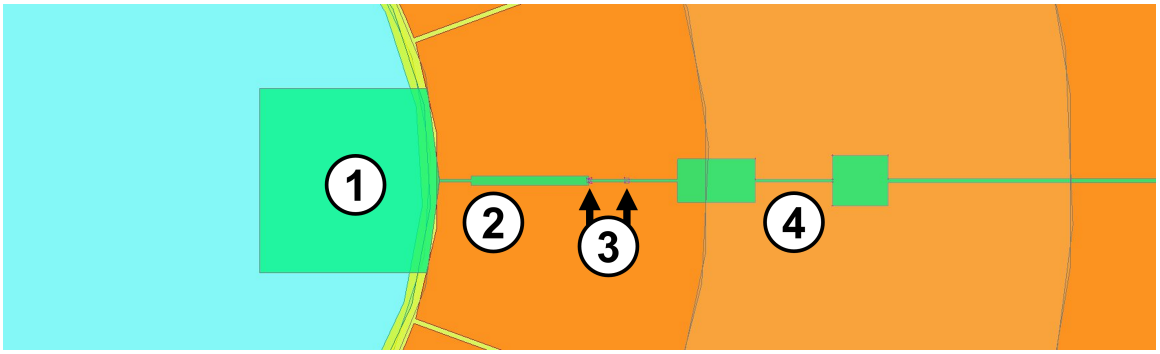


Figure B.3: The OMT-probe receiver circuit. The OMT probe (1) connects via a two-section impedance transformer (2) to the twin junction SIS mixer (3) and an LPF (4).

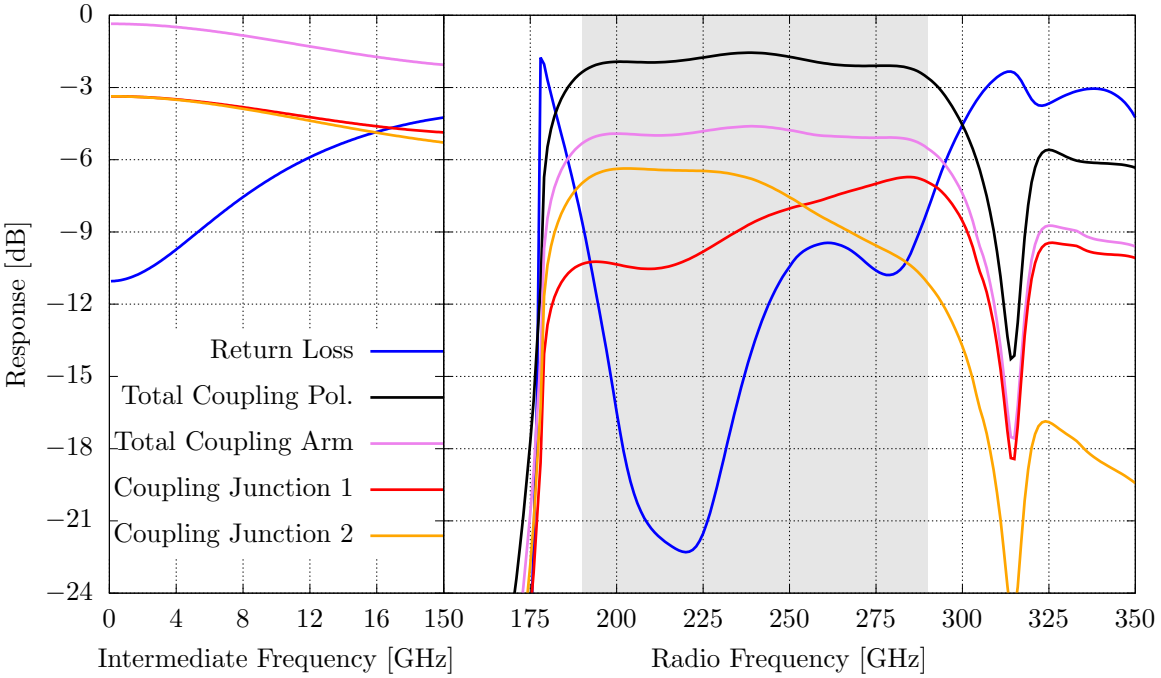


Figure B.4: The simulated performance of the OMT-probe dual-polarisation receiver. The performance is identical for both polarisations and all four OMT-probe arms. At IF, the parameters are referred to the corresponding IF port. At RF, the parameters are referred to the circular waveguide port. Total Coupling Arm denotes the sum over the individual junctions in one OMT-probe arm, and Total Coupling Pol. is the sum over a pair of opposing OMT-probe arms.

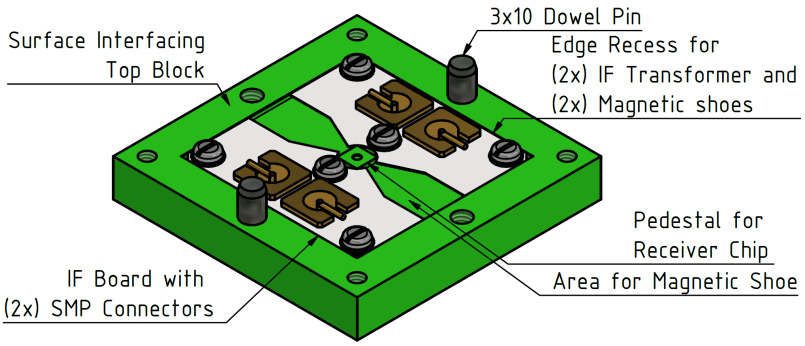


Figure B.5: The bottom block for the OMT-probe dual-polarisation receiver. The receiver chip sits on the central pedestal. There are two IF transformer boards with two SMP connectors for the IF signal of different RF polarisations separated by an area left for the magnetic shoes, which are part of the magnetic bias assembly in the top block.

bonding pads are now on the corners of a 3 mm by 3 mm quartz dice, shown in Figure B.2, instead of a single edge of the chip. This layout is motivated by keeping the circuit symmetric so that the signals of the same polarisation can be recombined in the IF circuit following the receiver. The chip layout, together with the block layout in Figure B.5, allows for meandering the microstrip on the IF transformer to the SMP connectors, thereby obtaining additional transformer length. Thus, a compact receiver layout is achieved with just a 35 mm by 35 mm footprint.

Despite this small footprint, magnetic shoes with a cross-section similar to those used in the other designs fit in the receiver block. Again, the magnetic bias assembly is next to the feedhorn and has the same options as previous designs. The design in Figure B.6 utilises two coils to ensure a sufficiently strong magnetic field at the SIS junctions. An experimental test would reveal if the second coil is redundant and if the design can be trimmed to a single coil.

As with our previous designs, the IF signals are connected via panel mount SMP connectors, which are accessible through two holes in the bracket to the cold plate. The coaxial cables connecting to the SMP connectors can be crossed and connected to the circuit, combining the IF power of the same polarisation, such as an standard Wilkinson power combiner. These standard components can be selected to fit behind and within the footprint of the receiver block. As a whole, this receiver assembly has all accesses on the front and the rear to enable simplistic extension to focal plane arrays, such as a four-by-four pixel array.

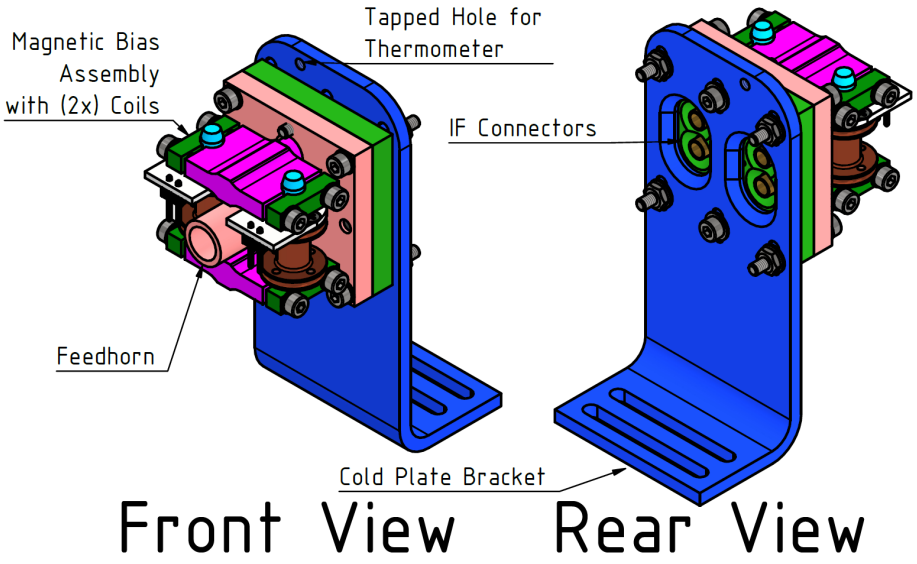


Figure B.6: The front and rear faces of the receiver block on the bracket for the cryostat.

B.2 Balanced Receiver Extension

We are able to incorporate the OMT-probe dual-polarisation receiver above in a balanced receiver scheme. However, the difficulty is in realising an efficient LO injection separate from the RF injection to achieve a relative phase difference between RF and LO, as discussed in Section 8.2.1. As this SIS receiver is very compact, the possibilities to inject the LO into the individual mixers are very limited. Figure B.7 shows a schematic of two potential locations for injecting the LO signal that are considered: Option A between the OMT probe and SIS mixer or Option B between the SIS mixer and LPF.

As per Chapter 8, an LO distribution network with an LO antenna is utilised. However, the microstrips connecting the OMT probes lead to the bonding pads on four corners of the dice or, alternatively, to two edges of the chip. Even if all four IF bonding pads were located on and the microstrip routed to one chip edge, a crossover would be required to separately connect each mixer with the LO signal within this planar circuit. Therefore, the microstrip coupler design presented in Section 8.3.1.2 is impractical as it requires additional crossovers to access all mixers.

B.2.1 Planar Beamsplitter

The solution to the LO distribution network for this receiver is a planar beamsplitter that has been proposed and demonstrated to function well at lower frequencies [138].

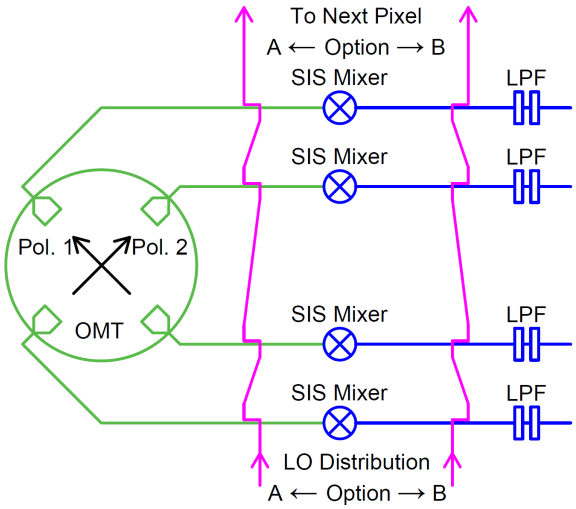


Figure B.7: The schematic of the LO injection for a balanced OMT-probe dual-polarisation SIS receiver. Only a single RF pixel is shown, and the LO antenna is omitted. The OMT is coloured in green, and the mixers circuits in blue. The LO distribution network is shown in magenta for two options: Option A couples the LO between the OMT and the SIS mixers, and Option B couples the LO between the SIS mixer and the LPF.

The circuit design resembles the crossover presented in Section 5.2.2 and is shown in Figure B.8. The purpose of the crossover is to minimise the contamination of one RF polarisation with the other presented in Chapter 5, but as described, the cross-coupling is a feature to be managed. In the LO distribution, we utilise a crossover as a planar beamsplitter that controls the amount of cross-coupling by controlling the overlap between the bottom and top layer CPW. A longer overlap allows for more cross-coupling. Furthermore, the meander of the top layer CPW introduces directivity to the coupling. The directivity allows the injection of LO power into the direction of the mixer in the RF path and, therefore, prevents the loss of available LO power. Consequently, the circuit functions as a beamsplitter: Most of the power passes through, and only a small fraction is cross-coupled into a specific direction of the other transmission line.

Figure B.9 shows the response of a planar beamsplitter designed to couple –10 dB. The isolation is better than –20 dB, and the remaining power is through-coupled with minimal reflections. The return loss of the microstrip routed through the top layer CPW has a smaller bandwidth than the microstrip routed via broadside couplers through the ground layer CPW. Figure B.9 also shows that the coupling varies by -10 ± 0.5 dB for altering the overlap length 5 ± 1 µm. The LO power injected into the individual SIS mixers can, therefore, be adjusted by changing the corresponding

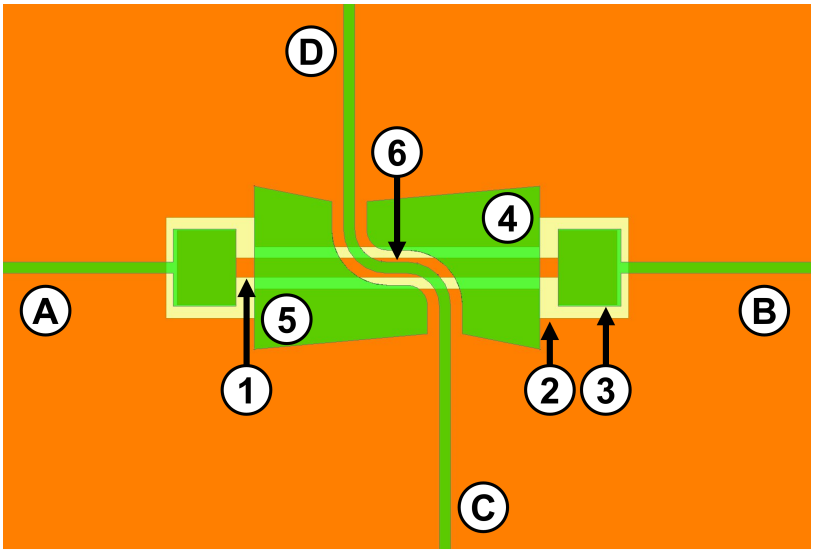


Figure B.8: The layout of the planar beamsplitter. As in the crossover, the signal is routed from the microstrip ports A to B via a CPW (1) in a gap in the ground layer (2) using broadside couplers (3). The microstrip connecting ports C and D is routed between brackets in the wiring layer (4 and 5), forming a quasi-ground for the wiring-layer CPW. The difference to the crossover is the parallel section of the ground-layer and wiring-layer CPWs (6), which results in the following beamsplitter performance: The signal incident at port A couples to port D, leaving port C isolated. Similarly, the signal incident at port C couples to port B, leaving port A isolated. The length of the parallel CPW section (6) controls the strength of the coupling from port A to D and port C to B.

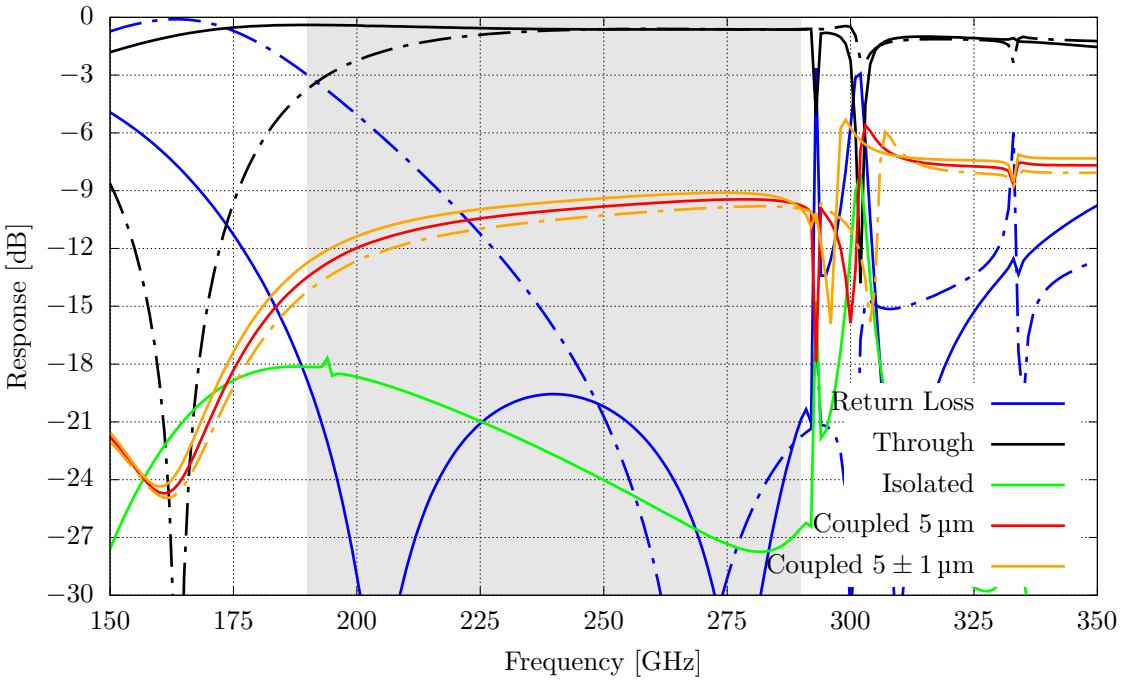


Figure B.9: The simulated performance of the planar beamsplitter. The return loss and through coupling for the signal routed in the ground-plane layer CPW connecting A and B in Figure B.8 are shown as solid lines. The return loss and through coupling for the signal routed in the wiring layer CPW connecting C and D in Figure B.8 are shown as dash-dotted lines. The return losses are minimally directional and only shown for one direction. The orange Coupled ±1 µm traces are solid for 6 µm and dash-dotted for 4 µm long overlapping parallel CPW sections highlighted with (6) in Figure B.8.

overlap in the planar beamsplitter.

By placing the planar beamsplitter, as shown in Figure B.7, either between the OMT probe and the SIS mixer or between the SIS mixer and the LPF, we can control the amount of LO power coupling into the SIS mixer. As the following designs, illustrating the layout of the RF and LO coupling network for balanced operation, are yet to be finalised, a 5 µm overlap is utilised for all planar beamsplitters. For the same reason, we abstain from showing the LO coupling into the mixers, although we ensure that the coupling is good enough to fine-tune the design in future.

B.2.2 Layout of the RF and LO Coupling Network for Balanced Operation

In principle, the orientation and location of the planar beamsplitter have no further implications so long as LO power can be injected into the SIS junction. However, as

the return loss of the planar beamsplitter in Figure B.9 has a larger bandwidth for the transmission line routed through the ground layer CPW, it is intuitive to use this path for the RF signal from the OMT probe to the mixer. From this design decision follows that the SIS mixers connect to a broadside coupler of the planar beamsplitter. To ensure DC bias for the SIS junctions without the need for additional circuit elements, it is only possible to place the planar beamsplitter between the OMT probe and the SIS mixer. Therefore, the balanced receiver can be designed with the OMT and LO injection first, as shown in Figure B.10, before adding the mixer circuits.

Another consideration is the layout of the LO distribution. In Chapter 8, we had one LO microstrip serving both polarisations of several pixels. We can apply the same concept here and loop the LO microstrip around the OMT, as shown in Figure B.10. The phase difference between the LO in SIS mixers connected to opposing OMT probes can be adjusted by lengthening or shortening this microstrip. In the shown example, the injected LO phase into opposing mixer arms varies every 34 GHz by 360°. Therefore, the physical transmission line length will limit the receiver bandwidth because of the 180° phase difference required for the separation of the RF signal and LO noise in the IF signal for the balanced operation.

Another disadvantage of this concept is that the planar beamsplitter not only injects LO into the RF mixer circuit but, in the same ratio, injects some RF power in the LO microstrip. The small amount of RF power coupling through the LO distributing network should be rejected in the IF hybrid due to the signal phase. However, reflections introduced with each planar beamsplitter cause the OMT-to-mixer coupling to undulate increasingly down the LO distribution microstrip, as shown in Figure B.11 for the circuit shown in Figure B.10. The coupling at the first probe of each polarisation is still very flat, while the coupling at the second probe already undulates. Besides this issue, the return loss remains below –10 dB, and the overall coupling of each polarisation is approximately –2 dB.

The solution to the challenges of narrowband operation due to the LO phase and the coupling undulations is shown in Figure B.12, wherein two separate LO microstrips are routed through two OMT probes only. The coupling from the circular waveguide to the port for the mixer is much flatter than previously, as shown in Figure B.13. Furthermore, the LO phase difference between two opposing OMT probes varies only by the microstrip length required to connect two adjacent planar beamsplitters. The signal phase difference changes 360° over 70 GHz.

We would like to highlight that the balanced receiver mode is reportedly tolerant to deviations from the required phase differences [125]. A DC applied to the LO

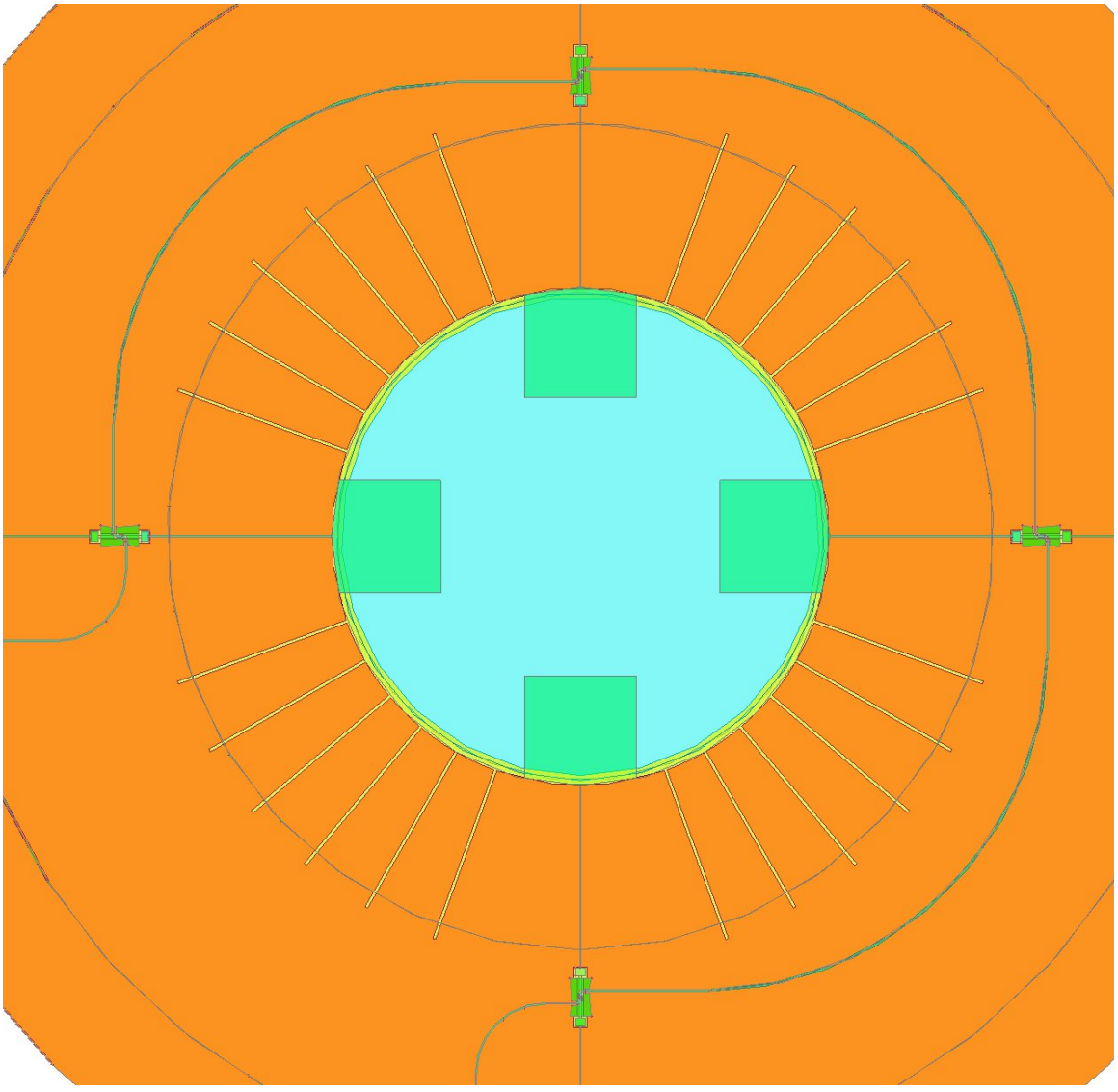


Figure B.10: The layout of the RF and LO coupling network with a single LO distribution microstrip for a balanced OMT-probe dual-polarisation SIS receiver.

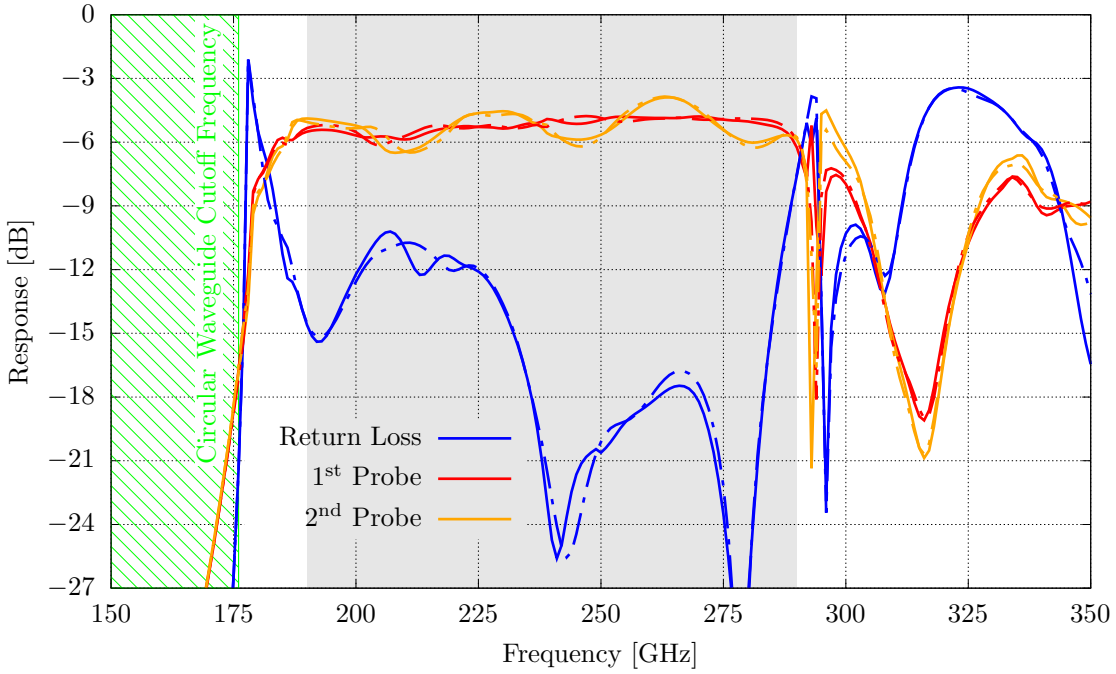


Figure B.11: The simulated RF performance of the RF and LO coupling network with a single LO distribution microstrip for a balanced OMT-probe dual-polarisation SIS receiver. The solid line is for Pol. 1 and dash-dotted for Pol. 2. The LO distribution first injects LO into the arm attached to the 1st OMT Probe of Pol. 1 and last to the 2nd OMT probe of Pol. 2.

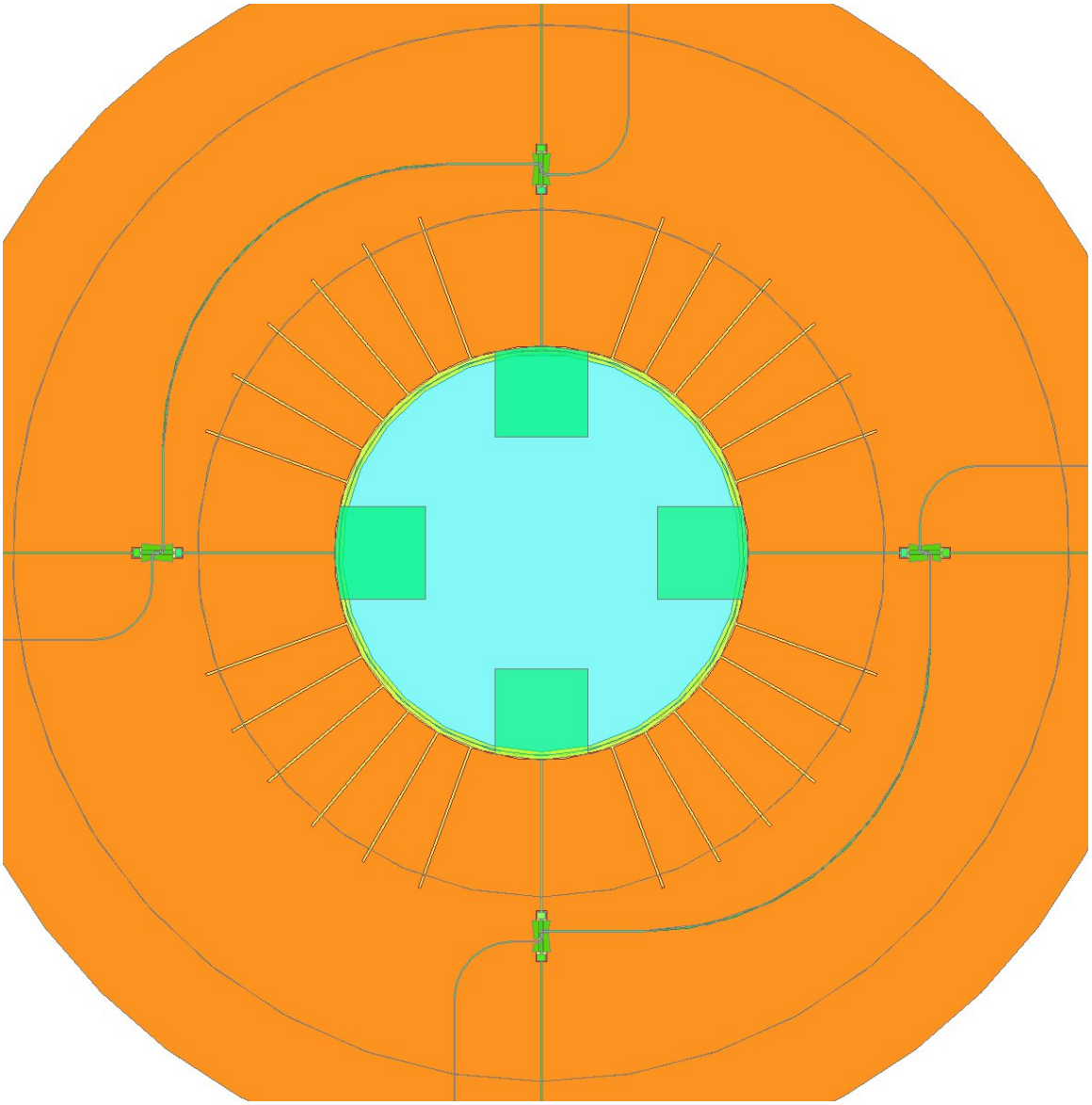


Figure B.12: The layout of the RF and LO coupling network with two LO distribution microstrips for a balanced OMT-probe dual-polarisation SIS receiver.

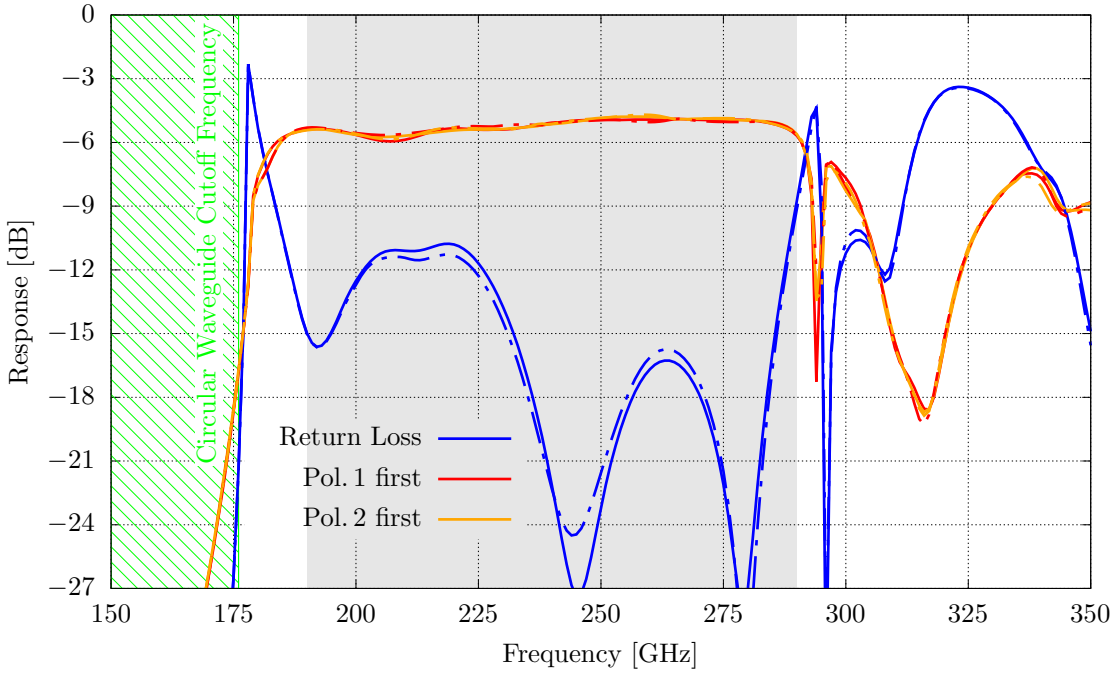


Figure B.13: The simulated RF performance of the RF and LO coupling network with two LO distribution microstrips for a balanced OMT-probe dual-polarisation SIS receiver. The solid line is for Pol. 1 and dash-dotted for Pol. 2. The key indicates whether the LO distribution injects the LO signal first in the Pol. 1 or Pol. 2 arm.

microstrip can also change the electrical length of the superconducting transmission line. Consequently, one can adjust the LO phase between mixers attached to opposing OMT probes. Furthermore, as this design is inherently more applicable to smaller RF bandwidth applications, it is worthwhile considering redesigning the OMT. As discussed in Section 5.2.1, the design with the serrations in the ground plane is needed to suppress resonances and achieve the 100 GHz bandwidth at 240 GHz centre frequency. For a more narrow band design, the OMT bandwidth could be optimised for operation without the ground plane serrations, which also allows for significantly shortening the microstrip connecting adjacent planar beamsplitters. Then, an optimum design could be found, optimising the RF bandwidth and balanced mixing. At this stage, further considerations such as arrayability can be taken into account: The design in Figure B.12 can be only scaled along one axis into an array, while the design in Figure B.10 allows for an arbitrary arrangement of the pixels on a focal plane without the need of additional components. Therefore, the layout decision for the balanced mixer depends strongly on the scientific goal targeted with such a receiver.

Appendix C

Planar Power Combiner

Simultaneous matching all ports of a non-power-dissipating 3-port circuit is impossible. The advantage of a superconducting circuit, however, is that the losses are minimal. Furthermore, the fabrication of resistors in superconducting high-frequency on-chip integrated circuits is difficult. These power-dissipating resistors, however, would be necessary to introduce the losses.

A suitable power combiner should be matched at the combined port, called port 1 and the two arms, ports 2 and 3, should couple with –3 dB to this combined port [123]. Assuming that the circuit is reciprocal, these requirements largely dictate the S-parameter matrix

$$\begin{pmatrix} |S_{11}|^2 & |S_{12}|^2 & |S_{13}|^2 \\ |S_{21}|^2 & |S_{22}|^2 & |S_{23}|^2 \\ |S_{31}|^2 & |S_{32}|^2 & |S_{33}|^2 \end{pmatrix} = \begin{pmatrix} 0 & 0.5 & 0.5 \\ 0.5 & |S_{22}|^2 & |S_{23}|^2 \\ 0.5 & |S_{32}|^2 & |S_{33}|^2 \end{pmatrix} . \tag{C.1}$$

Due to the no-loss condition, the sum of each row and column equals 1. The simplest tradeoff choice would be $|S_{22}|^2 = |S_{33}|^2 = |S_{32}|^2 = |S_{23}|^2 = 0.25$. Again, $S_{22} = S_{33} = 0$ is impossible from the way the reflection coefficient is calculated in Equation A.1 with the load impedance following from the remaining two port impedances of the 3-port circuit [26]. In this appendix, we discuss two power combiner solutions employable in superconducting circuits.

C.1 T-Junction Power Combiner with Stubs

In this section, we discuss the capabilities of a non-power-dissipating 3-port circuit, which we used previously in Chapter 8 and has been employed in other receiver designs [115]. We aim for superconducting transmission lines, including microstrips, because resistive films require additional fabrication effort, and the deployment of lumped

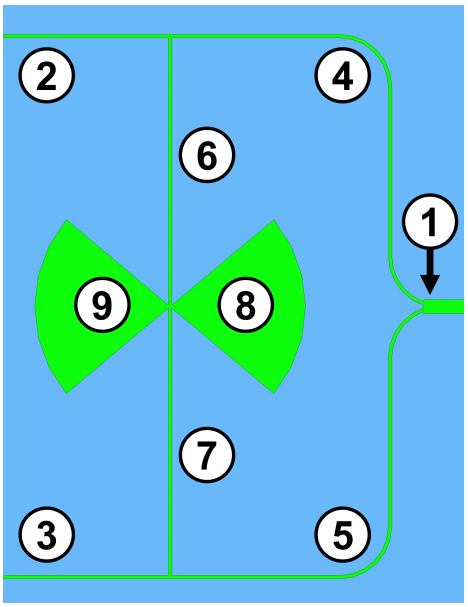


Figure C.1: The layout of the planar T-junction power combiner with stubs. The matched combined port (1) with an admittance $2Y_{\mathrm{F}}$ connects to the branch ports (2) and (3) with an admittance Y_{L} each via two branches (4) and (5) with a characteristic admittance Y_{B} and an electrical length βl_{B}. The branches are interconnected at the ports with the two stubs (6) and (7). At the interconnection of these two stubs are two radial stubs (8) and (9).

elements is impractical due to the short wavelength at the frequencies of our receivers. In the following, we first apply transmission line theory to describe our 3-port device, which we then use to describe several special cases.

C.1.1 Analytical Description of Power Combiner

The simplest planar power combiner is the T-junction variant, which comprises a junction of three transmission lines: one low-impedance input splitting into two high-impedance outputs. We expand this simple structure by adding stub structures between the two high-impedance transmission lines to mimic a structure similar to that of a branch-line hybrid, as shown in Figure C.1. The following five-step analysis resembles largely the analysis of a hybrid [26].

Circuit Reduction The circuit layout in Figure C.1 can be represented by the schematic shown in Figure C.2. The first step in our analysis is reducing the 3-port circuit shown in Figure C.2 into a 2-port circuit shown in Figure C.3 by symmetry. The reduced circuit has two modes depending on the phase difference between the signals on port 2 relative to port 3 of the real circuit. If these two ports are in phase,

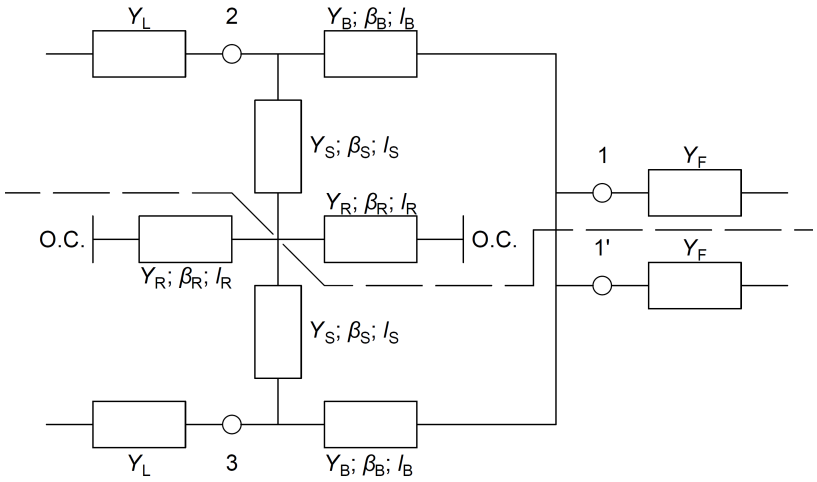


Figure C.2: Schematic representation of the planar T-junction power combiner with stubs. The ports 1 and 2 have an admittance Y_F and Y_L, respectively. The remaining circuit components are characterised by a characteristic admittance Y, propagation constant β and physical length l. The actual port 1 admittance is $2Y_\mathrm{F}$ in the layout, as the admittance is split in the analysis for easier calculation.

the even mode applies, and if the two ports are 180° out of phase, the odd mode applies. The modes are represented in the 2-port circuit with admittances where the symmetric reduction was applied: $Y_\mathrm{E/O}^\mathrm{Even} = 0$ for even modes and $Y_\mathrm{E/O}^\mathrm{Odd} = \infty$ for odd modes. Consequently, the circuit is reduced from a 3-port circuit into a 2-port circuit with two cases, the even- and odd-mode. All variables for the following discussion are defined in Figures C.1, C.2 and C.3.

Simplification of the Stub Structure The additional stub structures between the two high-impedance transmission lines provide additional tuning in contrast to a simple intersection of three transmission lines. The input admittance into this stub structure is

$$Y_\mathrm{in,S}^\mathrm{Even} = Y_\mathrm{S} \frac{Y_\mathrm{in,R} + iY_\mathrm{S} \tan(\beta l_\mathrm{S})}{Y_\mathrm{S} + iY_\mathrm{in,R} \tan(\beta l_\mathrm{S})} \tag{C.2}$$

for even modes and

$$Y_\mathrm{in,S}^\mathrm{Odd} = -i \frac{Y_\mathrm{S}}{\tan(\beta l_\mathrm{S})} \tag{C.3}$$

for odd modes, where we represent the input admittance into the radial stub with $Y_\mathrm{in,R}$. In the case of a simple transmission line stub instead of a radial stub, the admittance is

$$Y_\mathrm{in,R} = iY_\mathrm{R} \tan(\beta l_\mathrm{R}) \ . \tag{C.4}$$

Equations for radial stubs have been described in the literature [139–141].

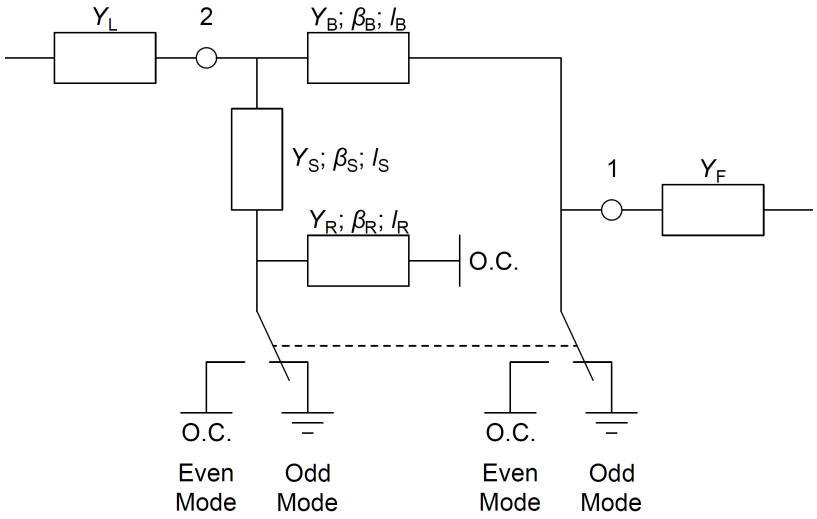


Figure C.3: 2-port even-odd mode reduction of the planar T-junction power combiner with stubs. The two switches connect depending on the mode, even or odd, to an open circuit (O.C.) or ground, respectively.

ABCD Matrix Representation The 2-port reduction of the power combiner and the simplification of the stub structure allow an easy ABCD representation:

- $\mathrm{ABCD_{E/O}}$ represents the even-/odd-mode shunt admittance next to port 1,
- $\mathrm{ABCD_B}$ represents the transmission line between ports 1 and 2, and
- $\mathrm{ABCD_{in,S}}$ represents the shunt admittance of the stub structure.

From port 1, the ABCD matrix is

$$\mathrm{ABCD_1} = \mathrm{ABCD_{E/O}} \cdot \mathrm{ABCD_B} \cdot \mathrm{ABCD_{in,S}} \ , \tag{C.5}$$

with the matrix elements

$$\begin{aligned}
\mathrm{A_1} &= \cos\left(\beta l_\mathrm{B}\right) + i\frac{Y_\mathrm{in,S}}{Y_\mathrm{B}}\sin\left(\beta l_\mathrm{B}\right) \\
\mathrm{B_1} &= iY_\mathrm{B}^{-1}\sin\left(\beta l_\mathrm{B}\right) \\
\mathrm{C_1} &= \left(Y_\mathrm{E/O} + Y_\mathrm{in,S}\right)\cos\left(\beta l_\mathrm{B}\right) + i\left(Y_\mathrm{B} + \frac{Y_\mathrm{in,S}Y_\mathrm{E/O}}{Y_\mathrm{B}}\right)\sin\left(\beta l_\mathrm{B}\right) \\
\mathrm{D_1} &= \cos\left(\beta l_\mathrm{B}\right) + i\frac{Y_\mathrm{E/O}}{Y_\mathrm{B}}\sin\left(\beta l_\mathrm{B}\right) \ .
\end{aligned} \tag{C.6}$$

The ABCD matrix from port 2 $\mathrm{ABCD_2}$ is derived likewise or results from the reciprocity theorem [26].

Reflection and Transmission Coefficient The textbook [26] expressions for reflection Γ and transmission T coefficient using the ABCD matrix representation above

are

$$\begin{aligned}\Gamma^{\text{Port}} =& \frac{\text{A}Y_{\text{Load}}^{-1} + \text{B} - \text{C}Y_{\text{Port}}^{-1}Y_{\text{Load}}^{-1} - \text{D}Y_{\text{Port}}^{-1}}{\text{A}Y_{\text{Load}}^{-1} + \text{B} + \text{C}Y_{\text{Port}}^{-1}Y_{\text{Load}}^{-1} + \text{D}Y_{\text{Port}}^{-1}} \\ T^{\text{Port}} =& \frac{2\sqrt{Y_{\text{Port}}^{-1}Y_{\text{Load}}^{-1}}\,(\text{AD} - \text{BC})}{\text{A}Y_{\text{Load}}^{-1} + \text{B} + \text{C}Y_{\text{Port}}^{-1}Y_{\text{Load}}^{-1} + \text{D}Y_{\text{Port}}^{-1}} \ ,\end{aligned} \tag{C.7}$$

where Y_{Port} is the admittance at the port at which the coefficients are calculated, and Y_{Load} is the admittance terminating the other port.

Scattering Parameters The scattering parameters follow simply from the reflection and transmission coefficients. For port 1,

$$\text{S}_{11} = \Gamma_{\text{Even}}^{\text{Port 1}} = \frac{Y_{\text{B}}\left(Y_{\text{F}} - Y_{\text{L}} - Y_{\text{in,S}}\right) + i\left(Y_{\text{F}}Y_{\text{L}} + Y_{\text{F}}Y_{\text{in,S}} - Y_{\text{B}}^2\right)\tan\left(\beta l_{\text{B}}\right)}{Y_{\text{B}}\left(Y_{\text{F}} + Y_{\text{L}} + Y_{\text{in,S}}\right) + i\left(Y_{\text{F}}Y_{\text{L}} + Y_{\text{F}}Y_{\text{in,S}} + Y_{\text{B}}^2\right)\tan\left(\beta l_{\text{B}}\right)} \tag{C.8}$$

and

$$\begin{aligned}\text{S}_{21} = \text{S}_{31} =& \frac{T_{\text{Even}}^{\text{Port 1}}}{\sqrt{2}} \\ =& \frac{Y_{\text{B}}\sqrt{2Y_{\text{F}}Y_{\text{L}}}}{Y_{\text{B}}\left(Y_{\text{L}} + Y_{\text{F}} + Y_{\text{in,S}}\right)\cos\left(\beta l_{\text{B}}\right) + i\left(Y_{\text{L}}Y_{\text{F}} + Y_{\text{in,S}}Y_{\text{F}} + Y_{\text{B}}^2\right)\sin\left(\beta l_{\text{B}}\right)} \ .\end{aligned} \tag{C.9}$$

For ports 2 and 3,

$$\begin{aligned}\text{S}_{22} = \text{S}_{33} =& \frac{\Gamma_{\text{Even}}^{\text{Port 2}} + \Gamma_{\text{Odd}}^{\text{Port 2}}}{2} \\ =& 0.5\frac{Y_{\text{B}}\left(Y_{\text{L}} - Y_{\text{F}} - Y_{\text{in,S}}\right) + i\left(Y_{\text{L}}Y_{\text{F}} - Y_{\text{in,S}}Y_{\text{F}} - Y_{\text{B}}^2\right)\tan\left(\beta l_{\text{B}}\right)}{Y_{\text{B}}\left(Y_{\text{L}} + Y_{\text{F}} + Y_{\text{in,S}}\right) + i\left(Y_{\text{L}}Y_{\text{F}} + Y_{\text{in,S}}Y_{\text{F}} + Y_{\text{B}}^2\right)\tan\left(\beta l_{\text{B}}\right)} \\ &+ 0.5\frac{-Y_{\text{B}} + i\left(Y_{\text{L}} - Y_{\text{in,S}}\right)\tan\left(\beta l_{\text{B}}\right)}{Y_{\text{B}} + i\left(Y_{\text{L}} + Y_{\text{in,S}}\right)\tan\left(\beta l_{\text{B}}\right)}\end{aligned} \tag{C.10}$$

and

$$\begin{aligned}\text{S}_{32} =& \frac{\Gamma_{\text{Even}}^{\text{Port 2}} - \Gamma_{\text{Odd}}^{\text{Port 2}}}{2} \\ =& 0.5\frac{Y_{\text{B}}\left(Y_{\text{L}} - Y_{\text{F}} - Y_{\text{in,S}}\right) + i\left(Y_{\text{L}}Y_{\text{F}} - Y_{\text{in,S}}Y_{\text{F}} - Y_{\text{B}}^2\right)\tan\left(\beta l_{\text{B}}\right)}{Y_{\text{B}}\left(Y_{\text{L}} + Y_{\text{F}} + Y_{\text{in,S}}\right) + i\left(Y_{\text{L}}Y_{\text{F}} + Y_{\text{in,S}}Y_{\text{F}} + Y_{\text{B}}^2\right)\tan\left(\beta l_{\text{B}}\right)} \\ &- 0.5\frac{-Y_{\text{B}} + i\left(Y_{\text{L}} - Y_{\text{in,S}}\right)\tan\left(\beta l_{\text{B}}\right)}{Y_{\text{B}} + i\left(Y_{\text{L}} + Y_{\text{in,S}}\right)\tan\left(\beta l_{\text{B}}\right)} \ .\end{aligned} \tag{C.11}$$

Once again, the circuit is reciprocal and lossless because one can show that $|\text{S}_{11}|^2 + |\text{S}_{21}|^2 + |\text{S}_{31}|^2 = 1$ and $|\text{S}_{12}|^2 + |\text{S}_{22}|^2 + |\text{S}_{32}|^2 = 1$.

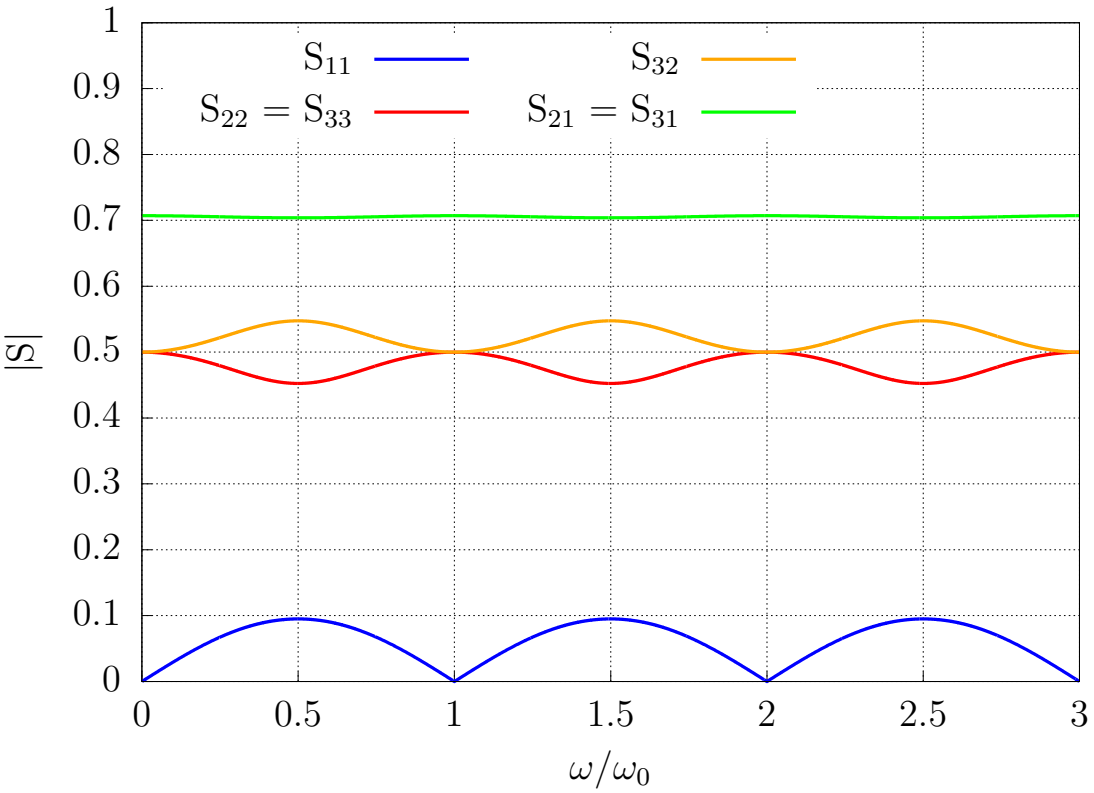


Figure C.4: No stub structure $Y_{\mathrm{in,S}} = 0$ with $Y_{\mathrm{F}} = Y_{\mathrm{L}} = 1$ and $Y_{\mathrm{B}} = 1.1$

C.1.2 Different Designs

The analytical expressions above allow for the design and optimisation of a power combiner for a specific problem. Although a thorough description of the effects of the individual parameters extends beyond the scope of this appendix, but in the following, we discuss several special cases in the following.

C.1.2.1 No Stub Structure, T-Junction Power Combiner

In the simplest case, wherein no stub structure $Y_{\mathrm{in,S}} = 0$ connects the two high-impedance transmission lines, the branch impedance is that of the load, and the low-impedance transmission line is matched $\mathrm{S}_{11} = 0$, which is $Y_{\mathrm{F}} = Y_{\mathrm{L}} = Y_{\mathrm{B}}$. The obtained response is frequency-independent with $\mathrm{S}_{21} = \mathrm{S}_{31} = -3\,\mathrm{dB}$ and $\mathrm{S}_{22} = \mathrm{S}_{33} = \mathrm{S}_{32} = -6\,\mathrm{dB}$.

The next more advanced T-junction case has $Y_{\mathrm{L}} \neq Y_{\mathrm{B}}$, making βl_{B} meaningful. For $Y_{\mathrm{F}} = Y_{\mathrm{L}}$, port 1 is matched $\mathrm{S}_{11} = 0$ if $\beta l_{\mathrm{B}} = n\pi$ with the integer n. Consequently, Figure C.4 shows frequency ω/ω_0 dependence. Note that $\beta \propto \omega$ and that we normalised by ω_0.

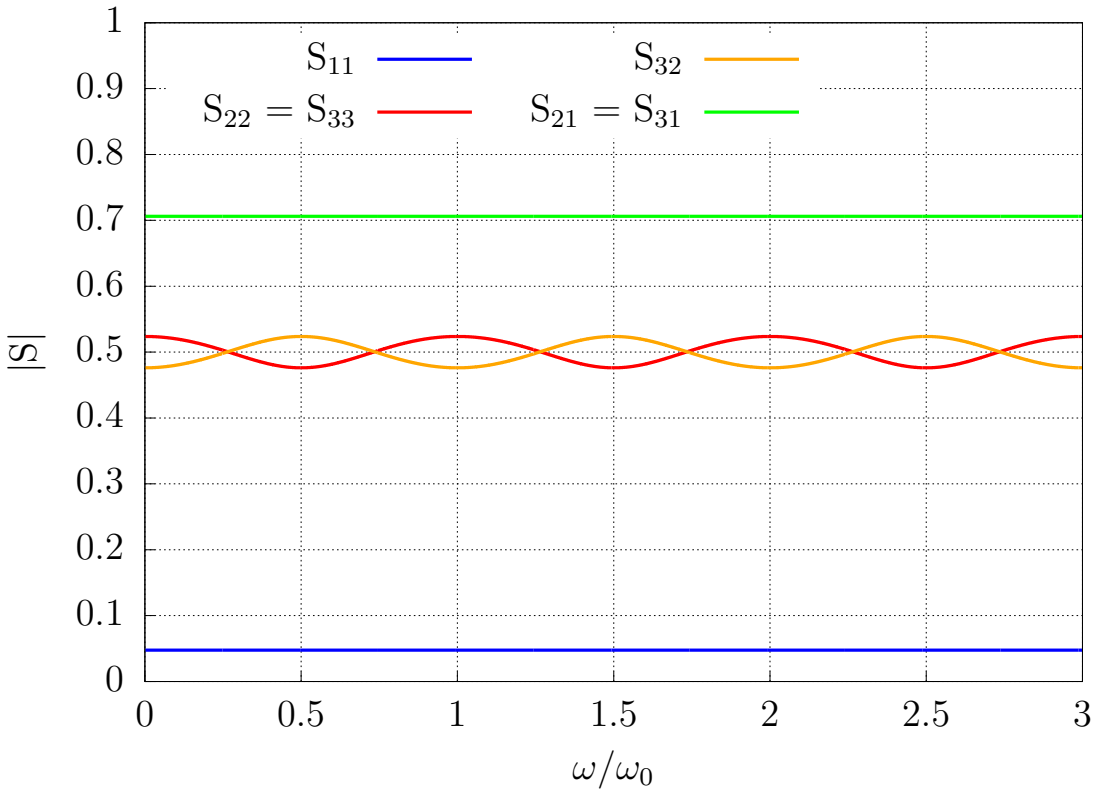


Figure C.5: No stub structure $Y_{\mathrm{in,S}} = 0$ with $Y_{\mathrm{L}} = 1$ and $Y_{\mathrm{F}} = Y_{\mathrm{B}} = 1.1$.

Finally, we discuss the case matching the branch to the combined port. Y_{L} is different from Y_{B}, which connects to the combined port with $Y_{\mathrm{F}} = Y_{\mathrm{B}}$. As shown in Figure C.5, $\mathrm{S}_{11} \neq 0$ and S_{21} and S_{22} undulate symmetrically around –6 dB. In fact, $|\mathrm{S}_{21}|^2 + |\mathrm{S}_{22}|^2 + |\mathrm{S}_{32}|^2 = 1$ holds, and because $\mathrm{S}_{12} \approx -3\,\mathrm{dB}$, $|\mathrm{S}_{22}|^2 + |\mathrm{S}_{32}|^2 \approx -3\,\mathrm{dB}$ or –6 dB each. The main difference to Figure C.4 is that the changed parameter set shifted the average $|\mathrm{S}_{32}|$ to a lower level and $|\mathrm{S}_{22}|$ to a higher level so that both are averaging around –6 dB in Figure C.5.

In summary, the simple intersection of three transmission lines shows already bandstop behaviour once a change in admittance (here Y_{B}) is introduced.

C.1.2.2 Simple Stub Interconnecting the Two Branches

In the next step, we introduce a stub interconnecting the two high-impedance transmission line branches, which is Equation C.2 with $Y_{\mathrm{in,R}} = 0$ and Equation C.3. Consequently, an additional pair of parameters affect the tuning, Y_{S} and βl_{S}.

Returning to the frequency-independent case with port 1 matched $Y_{\mathrm{F}} = Y_{\mathrm{L}} = Y_{\mathrm{B}} = Y$ described with no stub structure, the position of the stub interconnection

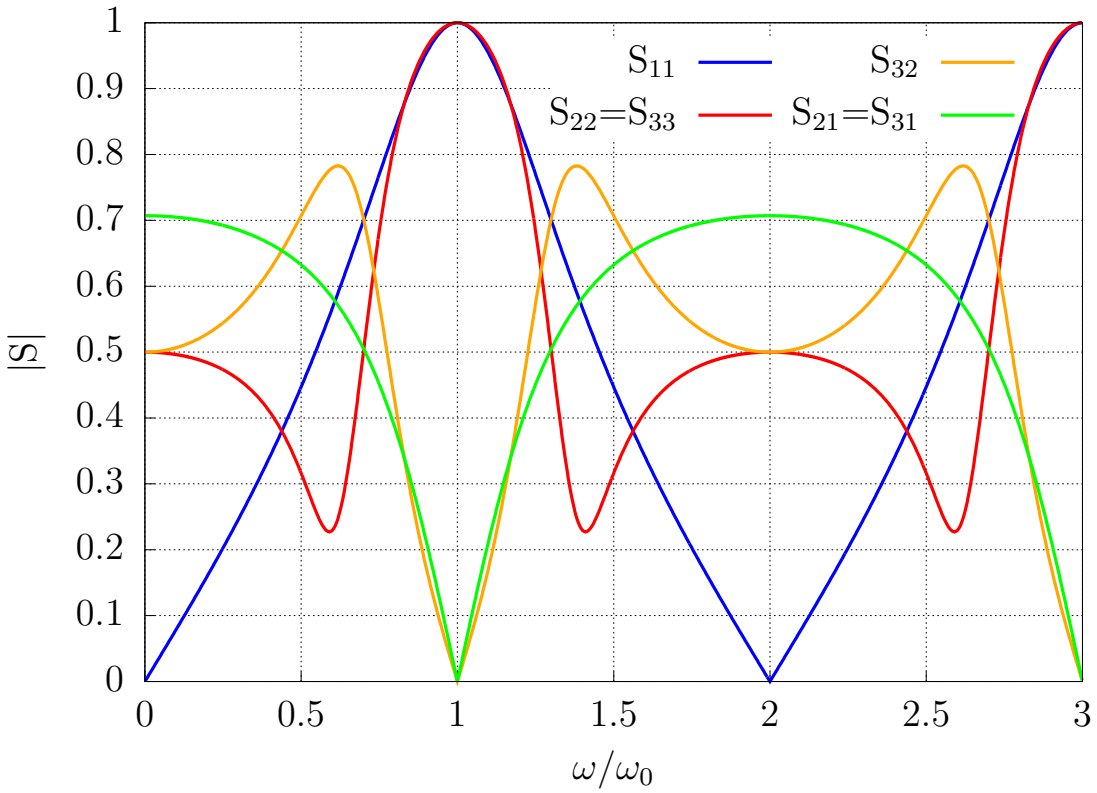


Figure C.6: Simple stub interconnecting the two branches with identical admittances $Y_\mathrm{F} = Y_\mathrm{L} = Y_\mathrm{B} = Y_\mathrm{S}$, and $\beta l_\mathrm{B} = 1$ and $\beta l_\mathrm{S} = 0.5$.

also defines βl_B. Hence, this case has three additional parameters: Y_S, βl_S and βl_B. The return loss at port 1 is now

$$\mathrm{S}_{11} = \frac{-Y_\mathrm{S} \tan(\beta l_\mathrm{S}) (\tan(\beta l_\mathrm{B}) + i)}{2Y - Y_\mathrm{S} \tan(\beta l_\mathrm{S}) \tan(\beta l_\mathrm{B}) + i (2Y \tan(\beta l_\mathrm{B}) + Y_\mathrm{S} \tan(\beta l_\mathrm{S}))} , \tag{C.12}$$

which allows for $\mathrm{S}_{11} = 0$ only with $\beta l_\mathrm{S} = n\pi$. βl_B controls the complex phase, and Y_S with βl_S controls the magnitude of the changes of S_{11}. βl_B has only an effect on the amplitudes of $|\mathrm{S}_{22}|$ and $|\mathrm{S}_{32}|$ but not on $|\mathrm{S}_{11}|$ and $|\mathrm{S}_{21}|$. An example is shown in Figure C.6 for $\beta l_\mathrm{B} = 1$ and $\beta l_\mathrm{S} = 0.5$.

The second case with a simple stub interconnecting two high-impedance branches restricts only $Y_\mathrm{F} = Y_\mathrm{L}$. The special case with $Y_\mathrm{B} = Y_\mathrm{S}$ is most similar to a ring hybrid structure, also known as a rat race hybrid. The return loss behaves as a band stop and pass filter, where $\omega = \omega_0$ is the stop band frequency, as shown in Figure C.7. A comparison with Figure C.6 shows that the S_{32} pass band in Figure C.7 becomes flatter with the changed parameter set.

The behaviour described with no stub structure in Section C.1.2.1 also applies to the circuit with interconnecting stub. S_{22} and S_{32} can be engineered to overlap

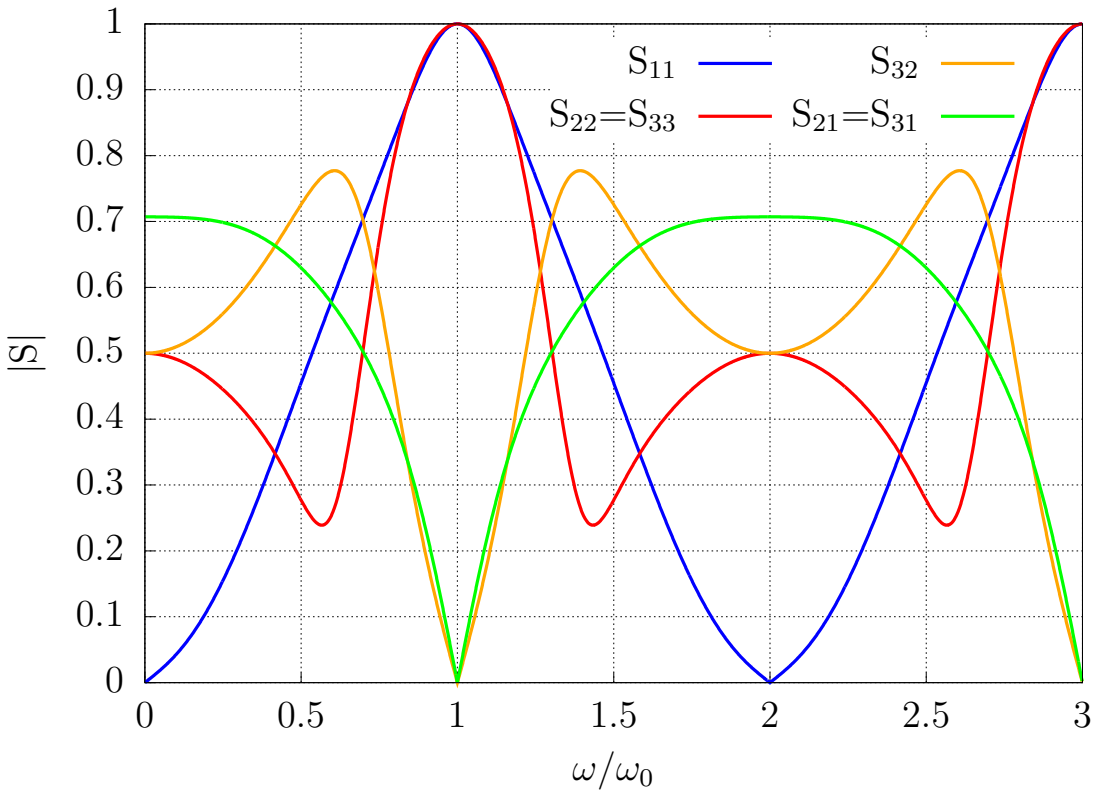


Figure C.7: Simple stub interconnecting the two branches with lower admittance than the port admittances $Y_{\mathrm{F}} = Y_{\mathrm{L}} = 1$, $Y_{\mathrm{B}} = Y_{\mathrm{S}} = 0.9$, $\beta l_{\mathrm{B}} = 1$ and $\beta l_{\mathrm{S}} = 0.5$

instead of S_{32} above –6 dB and S_{22} below –6 dB. Either way, they average –6 dB or less in the bandstop region.

C.1.2.3 Interconnecting Stub with Stub in the Middle

The examples above show increased complexity due to the stub interconnecting the two branches. A simple stub, or even a radial stub in the design in Chapter 8, will make the equation set even more complex. Therefore, we leave it with the discussed examples. Altogether, the additional stubs do not change the fact that it is $|S_{12}|^2 + |S_{22}|^2 + |S_{32}|^2 = 1$ or, in other words, that the reflection at each branch and the cross-coupling between the two branches average –6 dB.

C.2 Hybrid with Patch Antenna Power Combiner

Throughout this thesis and discussion, we tackle the same fundamental limit: 3-port power combiner solutions, such as the Wilkinson power combiner, prove difficult to implement at high frequencies and within superconducting circuits because all ports of a non-power-dissipating 3-port circuit are impossible to match simultaneously. Consequently, we employ complicated solutions in our on-chip sub-/mm receivers for astronomy. In Chapter 5, we employ a mixer circuit for terminating the isolated port of a branch-line hybrid. The same power-combining technique would have required eight mixer circuits for the balanced scheme in Chapter 8 and further circuit elements to inject the LO. Therefore, we used the circuit element described above and managed the issues from the –6 dB interbranch coupling and return loss at each branch. Other methods found in the literature are not applicable to our fabrication requirements [51, 142].

In this section, we present a novel quasi-lossless, easy-to-fabricate 3-port power combiner solution suitable for high frequencies and lossless circuits based on a branch line hybrid and a patch antenna terminating one hybrid branch. Therefore, we avoid any resistive power dissipation, which would be difficult to fabricate for SIS receivers. We first describe the design and then the predicted and measured performance of a scale model at 5 GHz centre frequency and 2 GHz bandwidth, achieving 40% fractional bandwidth.

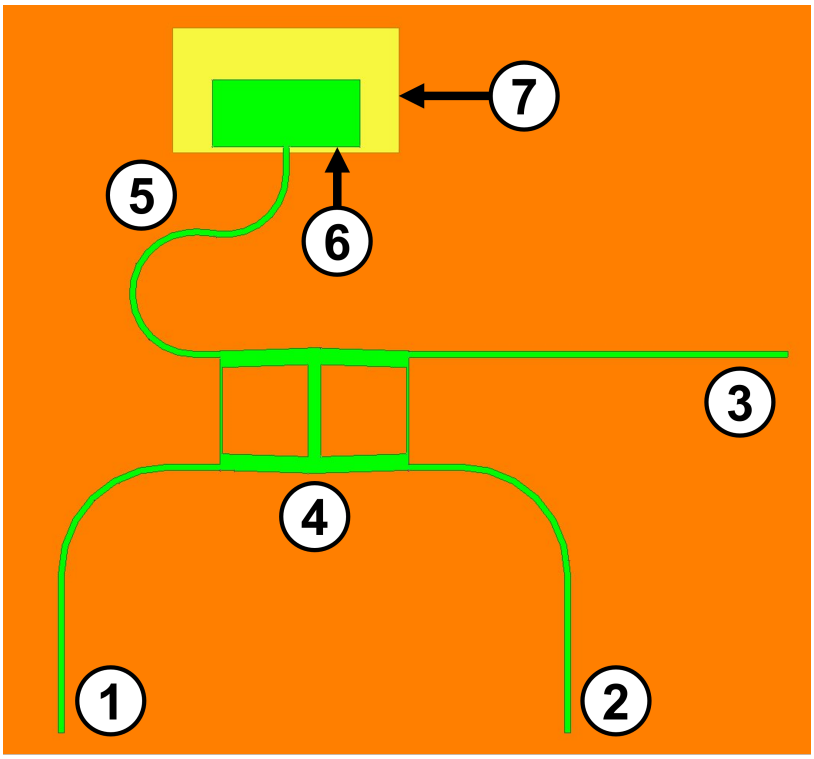


Figure C.8: Design of the hybrid with patch antenna power combiner. The combined Σ port (1) is fed from the Through port (2) and the Coupled port (3) via the hybrid (4). The Isolated hybrid port connects to the patch antenna (5), which consists of a metal patch connecting to the microstrip (6) and a cutout in the ground plane (7).

C.2.1 Design of the Hybrid with Patch Antenna Power Combiner

We design the power combiner in two steps using Ansys HFSS. First, we design the hybrid and the patch antenna individually before combining them into the design shown in Figure C.8 in the second step. An input signal at the hybrid Σ port couples with –3 dB and 90° phase difference to the Through and Coupled ports. The remaining isolated hybrid port connects to the patch antenna. In this configuration, all the ports can be matched, and so the return loss and isolation are generally low. Consequently, minimal power radiates at the patch antenna.

We performed simulations on the behaviour of the patch antenna in different surroundings. These simulations are important to avoid resonances appearing when the circuit is placed within a cavity, such as the mixer block. The simulations for different cavity dimensions show negligible effects until the cavity walls are unnecessarily close to the patch antenna.

Although the design is to be employed in a superconducting circuit at 240 GHz,

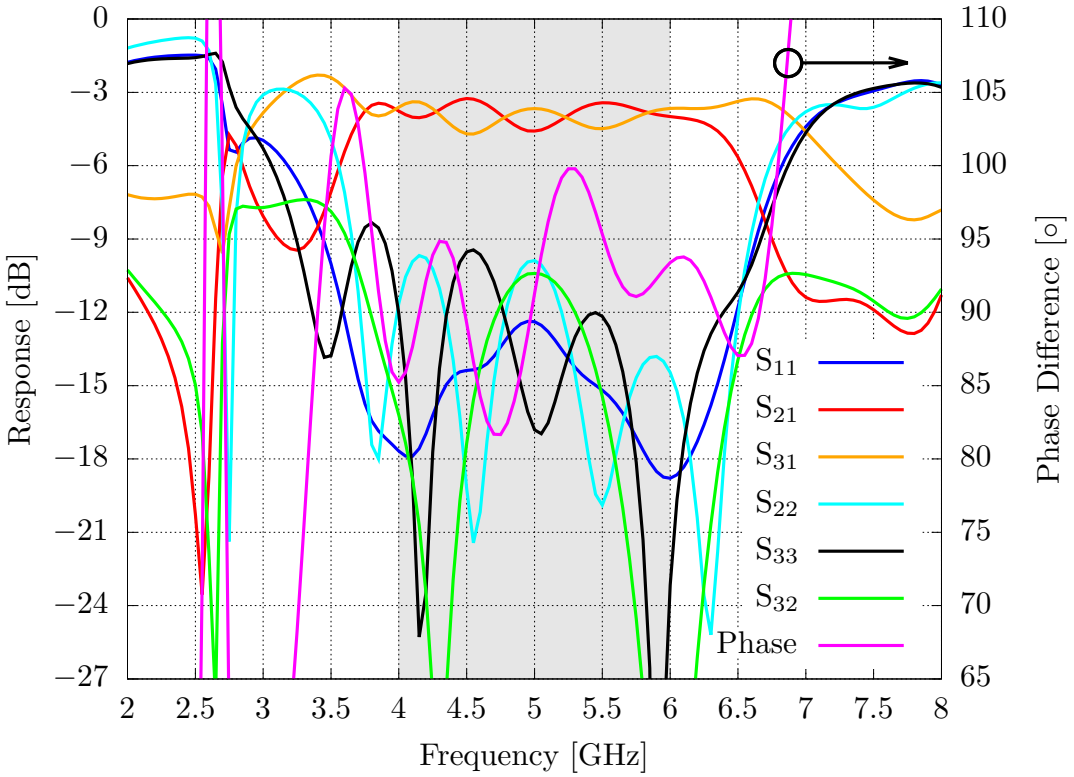


Figure C.9: The simulated performance of the hybrid with patch antenna power combiner. The port numbering follows that of Figure C.8. The circuit is reciprocal.

we verify the power combiner at 5 GHz with 40% fractional bandwidth to test with the vector spectrum analyser (VNA). The conductor of this scale model is 17.5 µm thick copper, sandwiching 250 µm thick Rogers RO4350 dielectric with an $\epsilon_R = 3.66$. For the simulation, we assumed vacuum with a radiating boundary condition above and underneath this setup. In the high-frequency application, the circuit would be supported with quartz from underneath, but we want to avoid the complication of adding a glass plate with our scale model measurements. Furthermore, the feeding microstrips are designed to a characteristic impedance of 50 Ω for use with commercial 50 Ω end-launch connectors and the standard calibration procedure of the VNA.

The predicted performance in Figure C.9 shows that we can achieve a power division with –4 dB to the two arms with a phase difference of $(90 \pm 10)^\circ$. The return loss in the combined arm S_{11} is below –12 dB, and the other two arms have return losses S_{22} and S_{33} and interbranch coupling S_{32} of less than –10 dB for 40% fractional bandwidth. This return loss and interbranch coupling is an improvement of more than –3 dB to the –6 dB of classical lossless 3-port power combiners.

In Figure C.10, we show the fabricated design with connectors attached. The

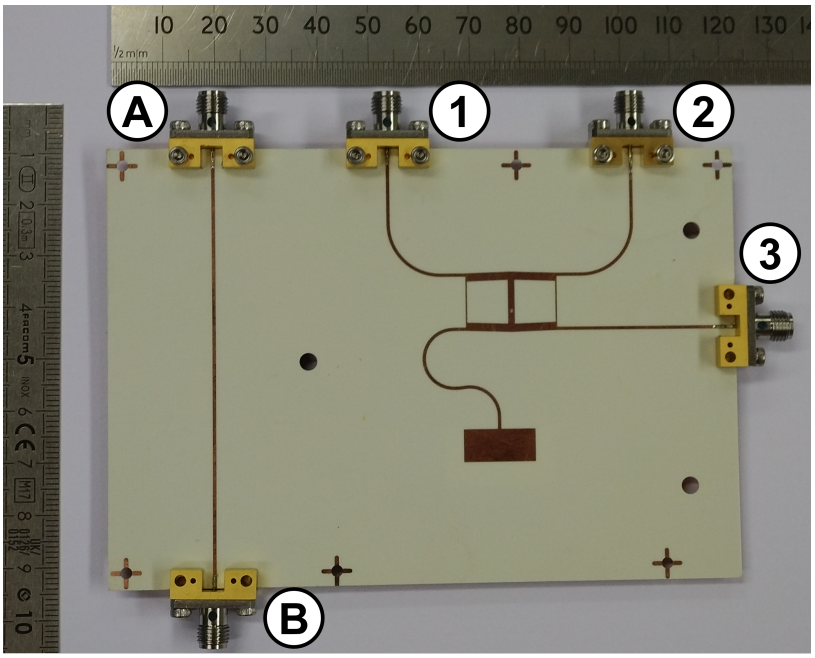


Figure C.10: The PCB with the hybrid with patch antenna power combiner connected at ports 1, 2 and 3, and a reference 50 Ω line connected at ports A and B.

measurements with the VNA shown in Figure C.11 are not optimal with regard to non-overlapping S_{12} and S_{13}. Instead, S_{12} is always slightly lower than S_{13}. However, the return losses are all below –10 dB in the frequency range from 4 GHz to 6 GHz. Similarly, low is the interbranch coupling S_{23}, which is below –12 dB. Furthermore, the phase difference remains mainly in the range $95 \pm 5°$, close to the expected value. Overall, despite non-optimal S_{12} and S_{13} performance, we could form a 3-port power combiner that has no resistive power dissipation and is still matched on all three ports.

In addition, we tested the sensitivity of the circuit on a metallic sheet placed above and underneath the patch antenna. The effects were negligible until the metal was close to touching the circuit. This data was been recorded systematically, as the S_{12} and S_{13} were not optimal, and the circuit design would require another design iteration. However, from the observations with this scale model circuit, we conclude that it is a viable option to use a hybrid with a patch antenna on a receiver chip to combine the RF power splitting between an OMT probe set because all three ports can be matched to a -10 dB level simultaneously. The circuit is independent of power-dissipating components and fits the fabrication procedure for superconducting SIS mixer circuits.

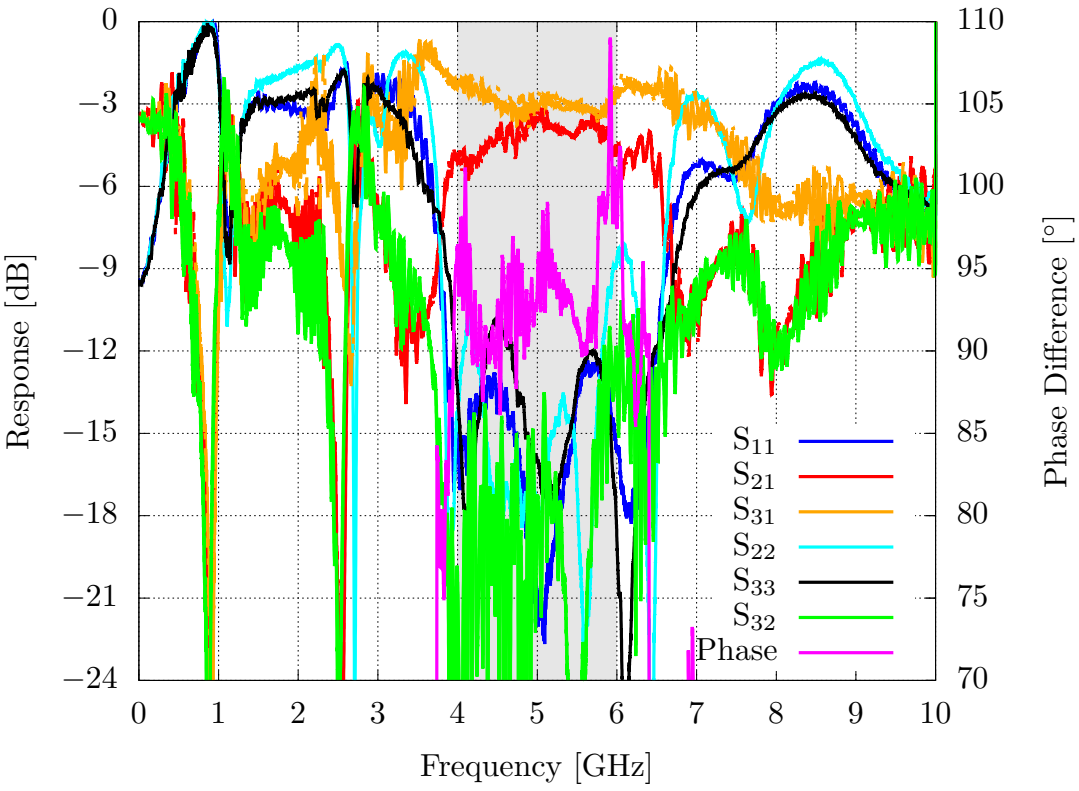


Figure C.11: The measured performance of the hybrid with patch antenna power combiner. The port numbering follows Figure C.10, and the reciprocal scattering parameters are shown dash-dotted in the same colour.

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