Digital Active Gate Drives to Increase Power Semiconductor Performance



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A thesis submitted for the degree of

Doctor of Philosophy

Hilary Term 2021

Abstract

Active Gate Drives (AGDs) tailor the signal applied to the gates of power metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs) to improve the switching behaviour of these power semiconductor devices. The AGDs can slow down the transition when switching between the OFF and ON states (and vice-versa) to reduce peak transient voltages and electromagnetic interference (EMI). However, the longer duration of the switching transition can lead to a higher energy loss in the power devices.

In the hard-switched bridge-leg studied in this thesis, it is found that the synchronous switching device experiences high transient voltage stresses as it undergoes its reverse-recovery, due to the parasitic inductance of the circuit as explained in Chapter 1. Using the pre-existing arbitrary waveform gate driver developed in [63], a method of driving the control IGBT of the bridge-leg is proposed, which can adapt the switching behaviour of the IGBT to keep this peak transient voltage below a specified limit. The AGD operates in three modes of differing complexity. The potential of each mode to reduce the peak transient voltage is assessed using an experimental method where a variety of control waveforms are in turn applied to the IGBT, and the peak voltage and switching energy loss associated with each control input is measured and recorded. The results reveal that the AGD is capable of suppressing the transient peak voltage across the diode by sharing the inductive voltage spike between the IGBT and the diode. This enables the voltage stress of the diode to be reduced with a small increase in total switching energy loss.

The implications of this increased energy loss on the power-processing capacity

of the IGBT are investigated. By reducing the peak transient voltage resulting from switching, AGD enables operation of the IGBT at higher dc bus voltages. However the larger switching loss means that a reduction in the conducted current is necessary to avoid exceeding the maximum allowable device junction temperature. A method is developed which experimentally quantifies the trade-off between these two factors, the results of which indicate that a small increase in IGBT power capacity can be obtained by use of an appropriate AGD.

In addition, an investigation is conducted into the role of the gate drive in obtaining the lowest possible switching loss of a silicon carbide (SiC) MOSFET, when circuit parasitic inductance does not limit the maximum speed of the switching transition. Use of an integrated circuit (LMG5200) containing two gallium nitride (GaN) FETs as a low-impedance gate drive is found to enable a high slew-rate of the MOSFET drain-source voltage, which is further increased by raising the voltage at the MOSFET gate. The results suggest that the full potential of these wide-bandgap devices is yet to be realised, that conventional gate drives currently limit the switching speed of SiC MOSFETs, and that switching performance may be enhanced by new gate drive designs.

Acknowledgements

This research was funded by an EPSRC doctoral training studentship and project EP/L019469/1. I would like to thank Dan Rogers and Boris Murmann for developing the gate driver hardware which formed the foundation of this work, and for the early work on gate waveform shaping of IGBTs [63] which inspired the research in this thesis.

This work was also enabled by Andrew Lui at Oxford University's Department of Materials, who willingly assisted by taking the x-ray CT scans of the IGBT device; and also by Jeff Fullerton who repeatedly drilled the IGBT package with such precision.

The research in this thesis is based on peer-reviewed publications, listed below with a description of my contribution to them.

> Gwilym Jones and Daniel Rogers. "Investigation of IGBT switching energy loss and peak overvoltage using digital active gate drives". In: 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics, COMPEL 2017. Stanford, CA: IEEE, July 2017, pp. 1–8. ISBN: 9781509053261. DOI: 10.1109/COMPEL.2017.8013407

I developed the software running the experiment to perform automated testing of gate drive waveforms, which resulted in the discovery of the voltage-sharing behaviour between control and synchronous devices. Rogers provided the gate drive and the IGBT circuit-board hardware.

> G. T. Jones, Y. P. Siwakoti, and D. J. Rogers. "Active Gate Drive to Increase the Power Capacity of Hard-Switched IGBTs". In: IEEE Jour-

nal of Emerging and Selected Topics in Power Electronics (2020). DOI: 10.1109/JESTPE.2020.2986097

I designed and built the half-bridge power circuit, and developed the experimental method for evaluating the IGBT power capacity. Rogers provided the problem motivation and proposed that we consider IGBT power capacity as the metric to be maximised. Siwakoti provided advice on how to best convey the method and results in the paper.

Moreover I would like to personally thank Dan Rogers for supporting and mentoring me over the course of my studies, from undergraduate through to doctorate. Thank you for taking the time to share your knowledge and experience in the lab, for your insightful guidance, and for trusting me to explore my own ideas.

Thank you to my colleagues and friends in the Power Electronics Group, and Energy and Power Group, for creating a friendly and inspiring working environment, and for the many lively discussions at the Gardener's Arms. Thank you Tim Erskine for the solid bedrock of friendship.

I am deeply grateful to my sister, Eleanor, for her sage advice, and to my parents Huw and Candice for their love and support. Also to Jiemin, your love and endless encouragement has got me through the ups and downs of finishing this research in the time of coronavirus.

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Abbreviations

ADC	Analogue to digital converter
AGD	Active gate drive
BJT	Bipolar junction transistor
DAC	Digital to analogue converter
DR-AGD	Double-ramp AGD
EMI	Electromagnetic interference
FGD	Fast gate drive
FPGA	Field-programmable gate array
GaN	Gallium Nitride
GTO	Gate turn-off (transistor)
IGBT	Insulated-gate bipolar transistor
LUT	Look-up table
MOSFET	Metal-oxide-semiconductor field-effect transistor
PCB	Printed circuit board
PP-AGD	Push-pull AGD
RAM	Random-access memory
Si	Silicon
SiC	Silicon carbide
SCR	Silicon controlled rectifier
SPICE	Simulation Programme with Integrated Circuit Emphasis
VDMOS	Vertical double-diffused MOSFET
VR-AGD	Variable-ramp active gate drive
WBG	Wide band-gap

1 Introduction

This thesis investigates how the application of tailored voltage waveforms to the gates of power transistors can be used to control their switching behaviour and obtain improved performance from the devices. The concept of the Active Gate Drive (AGD) is explored with the purpose of determining the extent to which such technology can expand the useful operating environment of power transistors.

This chapter begins by briefly outlining the historical development of power electronic switches in order to highlight how the rapid increase in the use of power electronics has been facilitated both by the invention of new power semiconductor devices and by the development of driving techniques to operate the devices effectively. The operating principles of the two most common power transistor architectures, the MOSFET and the IGBT, are presented, and the conventional gate drive technique is discussed.

The particular characteristics of *hard-switching* are outlined for a bridge-leg of two transistors. By considering the internal capacitances of the transistor, the sources of switching energy loss are explained and the influence of the gate drive on switching loss is considered. Following this, the causes and effects of power-loop parasitic inductance and diode reverse-recovery behaviour are examined. The chapter concludes with an outline of the structure and research contributions of the thesis.

1.1 The evolution of power switches and their drives

Power electronics is ubiquitous in the modern world [1]. With at least 50 % of electricity estimated to be controlled by power electronics [2], and the electricity generated from renewable sources predicted to increase by 60 % over the next decade [3], the prevalence of power electronics in all sectors is set to continue.

The growth in the application of power electronics has closely followed the development of power switch technology. Figure 1.1 outlines some of the key developments in power switch technology over the last century. Early power electronics, using electron tubes as switches [4], gave way to solid-state technology with the advent of the first bipolar junction transistor (BJT) in 1947 [5]. The invention of the thyristor (SCR) in 1956 provided a means to conduct high current and block high voltage [6], however the lack of turn-off capability limits the thyristor to line-commutated applications (typically switching at 50 Hz or 60 Hz). The gate-turn-off (GTO) transistor was developed soon afterwards, further expanding the areas of application [6]. However, the cumbersome drive and protection requirements of the GTO resulted in large and expensive equipment [2].

The arrival of the metal-oxide-semiconductor field-effect transistor (MOSFET), in particular the vertical double-diffused MOSFET (VDMOS) in 1978, marked the beginning of a new generation of easy to drive, voltage-controlled power semiconductor devices [7, 8]. The subsequent development of the insulated-gate bipolar transistor (IGBT) in the early 1980s extended the power handling capability of the voltage-controlled devices, and MOSFETs and IGBTs continue to be the most commonly used switching technology today [2]. Fig. 1.2 indicates where these types of power devices are commonly applied. Together the MOSFET and IGBT occupy a wide range of application areas, from the 1 W, 1 MHz MOSFETs used in portable electronics, through to the 1 MW, 1 kHz IGBTs found in utility grid scale power converters.

The most recent step-change in power electronic switch technology has been the adoption of wide band-gap (WBG) semiconductor materials. These materials,

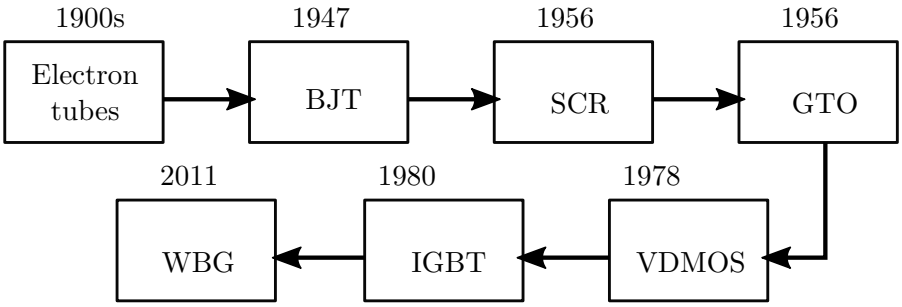


Figure 1.1: Breakthroughs in power semiconductor device technology. BJT: Bipolar Junction Transistor. SCR: Silicon Controlled Rectifier (Thyristor). GTO: Gate Turn-Off Thyristor. VDMOS: Vertical Double-diffused MOSFET. IGBT: Insulated Gate Bipolar Transistor. WBG: Wide Band-gap devices.

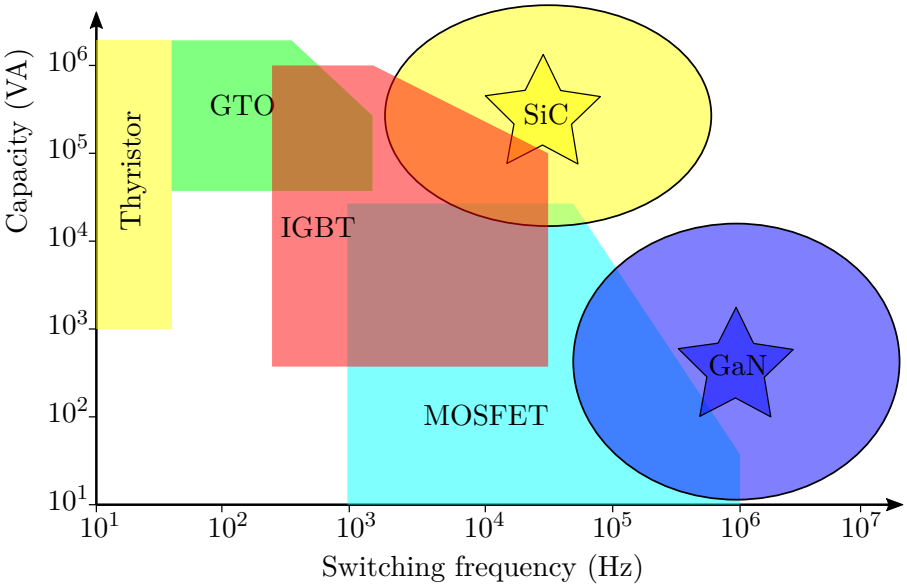


Figure 1.2: Typical range of switching frequency and power capacity for the major silicon semiconductor device families (polygons), and areas of opportunity for WBG devices (ellipses) (adapted from [9] and [10]).

principally silicon carbide (SiC) and gallium nitride (GaN), are used to fabricate devices with superior switching characteristics, blocking voltage capability, and conductivity. These two WBG materials are expanding the power capacity and the range of switching frequencies at which modern power electronic switches can operate, as shown by the ellipses in Fig. 1.2. For the reasons behind the superior performance of devices fabricated from these WBG materials, related to the critical electric field and the carrier effective mass, see [11].

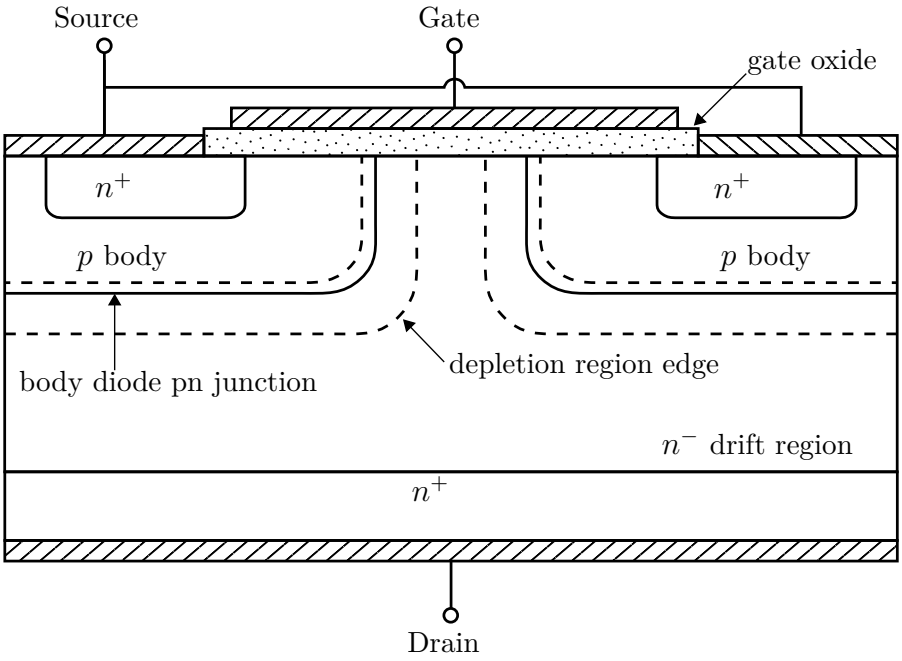


Figure 1.3: Structure of an n-channel vertical double-diffused MOSFET (VDMOS), the most common MOSFET used in power electronics. (Not to scale.)

1.2 The MOSFET and IGBT

Figure 1.3 shows a cross-section through an n-channel vertical double-diffused MOSFET (VDMOS), the most commonly used MOSFET in power electronics. Three terminals for connecting to the device are shown: *drain* and *source* terminals directly contact the semiconductor surface, while the *gate* terminal is separated from the semiconductor by an insulating oxide layer. Sequential diffusion processes create a p-doped well, known as the *body*, in the n-type substrate and a highly-doped n^+ well within the body, to which the aluminium source contact is connected. The lightly-doped *drift region* between the drain contact and the body forms a pn junction known as the *body diode* that can conduct current from source to drain (known as MOSFET *reverse-conduction*) but blocks current from drain to source (*forward-conduction*) [7].

Forward-conduction only becomes possible when the voltage between the gate and body region is sufficiently large to 'invert' the body region and attract electrons to the underside of the oxide, as illustrated in Fig. 1.4. A conductive channel is then formed between the n^+ source region and the edge of the body-diode

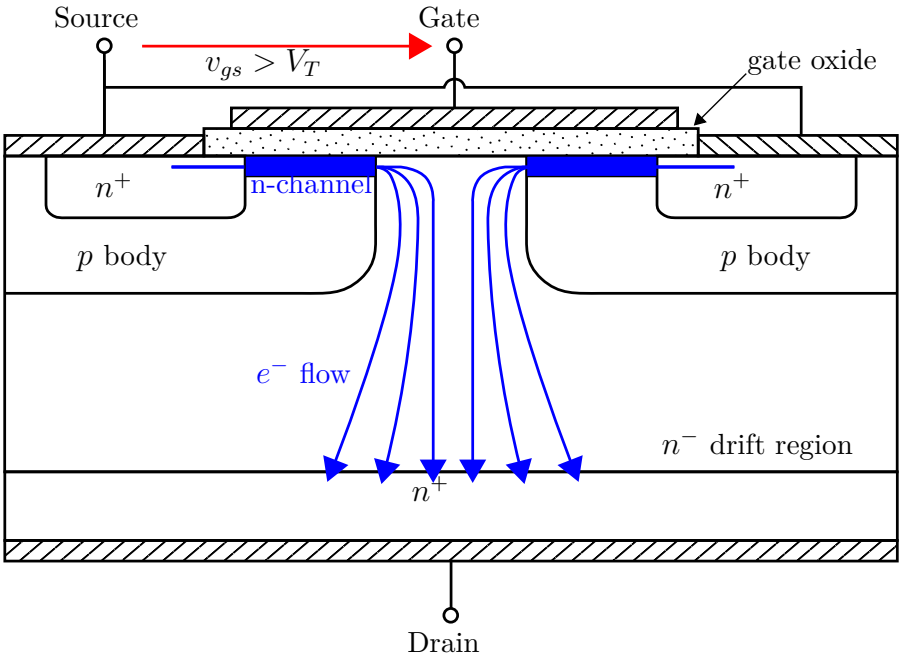


Figure 1.4: Electrons can drift from source to drain once a channel of inversion charge is formed.

depletion region. Under an applied drain-source voltage, electrons can drift from source to drain through the channel.

Dopant concentration, device geometry, and material properties can be carefully controlled to create devices where the body region has low electron concentration at thermal equilibrium (no voltage applied to the terminals) but becomes inverted upon application of a relatively small gate-body *threshold voltage* (V_T). These devices are called *enhancement-mode* or *normally off* devices. The body region is connected to the source terminal so that the channel is created when the applied gate-source voltage v_{gs} is greater than V_T. *P*-channel devices can also be created if the p-type and n-type doping in the structure of Fig. 1.3 is reversed, however these devices have lower channel conductivity per unit area compared to *n*-channel devices, due to the lower mobility of holes compared to electrons, and therefore *p*-channel power devices are rarely used in power electronics. The *n*-channel enhancement-mode MOSFET is the only type considered in this work.

The MOSFET has three modes of operation depending on the applied gate-source voltage v_{gs} and drain-source voltage v_{ds}: cut-off, linear (ohmic) conduction, and saturation. It is useful to express the drain current i_d in terms of v_{gs} and v_{ds}

for each mode. The derivation of such relations is provided in many sources, for example [7, 11, 12]. The relations are briefly stated here.

The cut-off (also known as sub-threshold) mode occurs when v_{gs} is below the threshold voltage V_T. The channel is not inverted, therefore no significant current can flow from drain to source:

$$i_d \approx 0 \tag{1.1a}$$

when

$$v_{gs} \leq V_T \,. \tag{1.1b}$$

When v_{gs} is greater than V_T and v_{ds} is small, the drain current is approximately proportional to v_{ds}, and the MOSFET behaves simply as a resistor, hence this is called the 'linear' or 'ohmic' mode:

$$i_d = \frac{W\mu_n C_{\text{ox}}}{L}\left[(v_{gs} - V_T)v_{ds} - \frac{v_{ds}^2}{2}\right] \tag{1.2a}$$

when

$$v_{ds} \leq v_{gs} - V_T \tag{1.2b}$$
$$v_{gs} > V_T \,. \tag{1.2c}$$

The MOSFET is said to have 'saturated' when the drain-source voltage exceeds the gate-source voltage. Then the MOSFET drain current becomes independent of the drain-source voltage:

$$i_d = \frac{W\mu_n C_{\text{ox}}}{2L}(v_{gs} - V_T)^2 \tag{1.3a}$$

when

$$v_{ds} > v_{gs} - V_T \tag{1.3b}$$
$$v_{gs} > V_T \,. \tag{1.3c}$$

The i_d-v_{ds} characteristic is illustrated in Fig. 1.5 for several values of v_{gs}, where the transition from ohmic to saturated-regions is indicated.

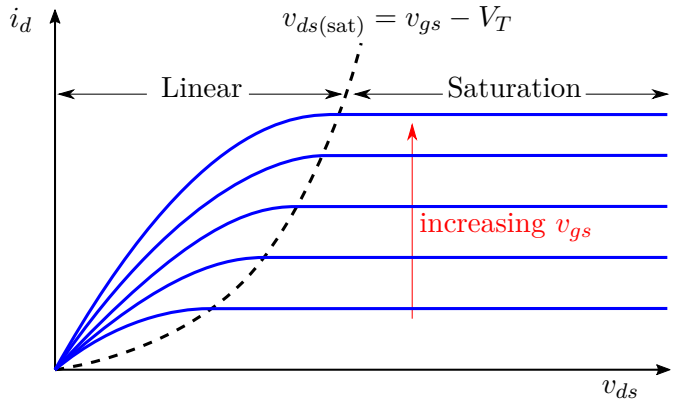


Figure 1.5: Drain current plotted against drain-source voltage as a function of gate-source voltage, for an n-channel enhancement mode MOSFET. The dashed line indicates the critical value of v_{ds} above which the MOSFET saturates and i_d becomes independent of v_{ds}.

The on-state resistance R_{on} is the reciprocal of the gradient of the i_d-v_{ds} curve in the ohmic region. When expressed per unit die area it is called the specific on-state resistance $R_{on,sp}$, and is used to compare device technologies.

The specific on-state resistance of MOSFETs increases as their blocking-voltage capability increases, because when blocking positive v_{ds} the pn-junction depletion region expands into the drift region which imposes a minimum thickness on the drift region. By assuming a uniformly-doped, one-sided junction, the specific on-state resistance of a MOSFET can be expressed as a function of rated blocking voltage V_{bv} [13]

$$R_{on,sp} = \frac{4V_{bv}^2}{\mu_n \epsilon E_{\text{crit}}^3}, \tag{1.4}$$

where E_{crit} (the critical electric field strength at the onset of impact-ionisation i.e. avalanche breakdown), μ_n (electron mobility), and ϵ (permittivity) are properties of the semiconductor material.

The specific on-state resistance is proportional to the square of the blocking voltage. Since the conduction loss is proportional to the square of the conducted current, for a given processed power the conduction loss is independent of the blocking voltage (since current decreases as voltage increases such that the IV product is constant). However, often the objective of operating at higher voltages is to increase the power capacity (i.e. maintaining the same levels of current as

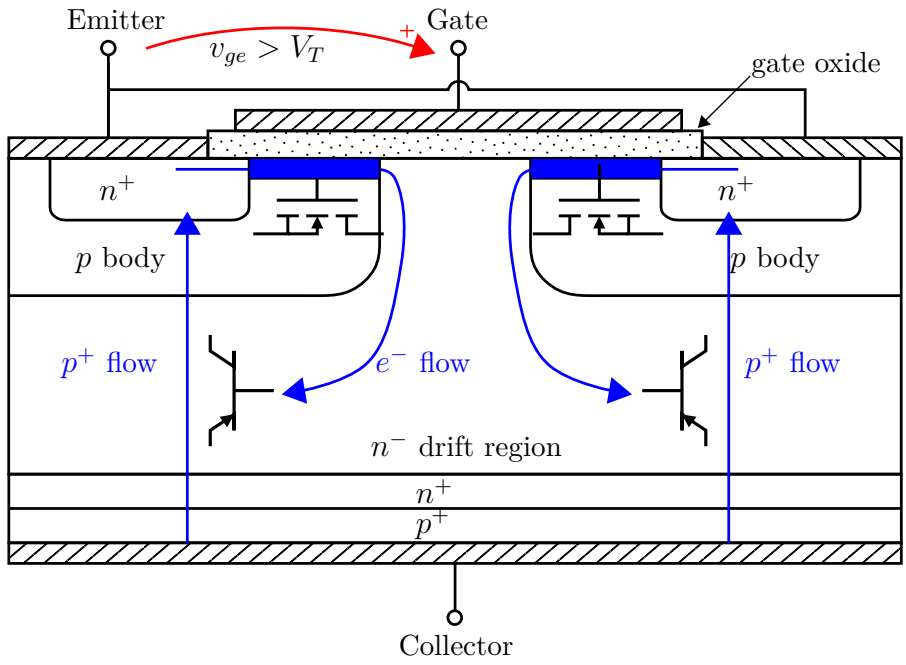


Figure 1.6: The IGBT structure. On-state electron and hole current flows are illustrated. The conduction mechanism is an n-channel MOSFET supplying base current to a *pnp* BJT, as indicated by the circuit symbols.

voltage increases), and in this case Equation (1.4) puts a practical limit on the current-density, hence rated-power, of high voltage MOSFETs [14]. (Note however that this simple prediction is based on analysis in one-dimension and superjunction MOSFETs exceed this limit by using two-dimensional geometric features [15].)

The IGBT was invented to overcome the large on-state resistance of high-voltage devices. The structure is similar to the MOSFET structure but with the addition of a highly p-doped region at the drain. The action of this layer, illustrated in Fig. 1.6, is to inject holes into the drift region during conduction. This *conductivity modulation* reduces the resistivity of the drift layer [16]. The IGBT can be thought of as the coupling of a MOSFET and a *pnp* BJT in a Darlington pair: the MOSFET supplies electron current to the base of the BJT, and the BJT provides current amplification due to the hole flux from the p^+ layer to the p-body region. This allows the IGBT to surpass the unipolar limit (1.4) of MOSFETs and provide both low on-state voltage drop and high blocking voltage capability.

It is conventional to label the two power terminals of the IGBT as for an *npn* BJT: i.e. what would be called the drain and source of a MOSFET are termed

the *collector* and *emitter* for an IGBT. In this thesis the MOSFET terminology is used when the discussion applies equally to MOSFETs and IGBTs. Note that the term 'saturation' means different things when applied to MOSFETs and BJTs, and in this work the MOSFET definition of saturation given above is used when discussing IGBTs (i.e. that $v_{ge} - V_T > v_{ce}$).

1.3 The switching leg

The operating principle of a hard-switched bridge-leg is outlined in this section. The bridge-leg is a common configuration where two transistors are connected in series between a dc voltage source, and the mid-point between the transistors is connected to an inductive load, as shown in Fig. 1.7. In switched-mode operation each transistor spends most of its time in either the cut-off region ($v_{gs} < V_T$) or the low-resistance linear region ($v_{gs} - V_T >> v_{ds}$). These two states are referred to as 'OFF' and 'ON', respectively, and the transistors operated in this way are called 'switches'. The switch states are complementary so that when one is ON the other is OFF and vice-versa. In this way, the voltage at the mid-point between the transistors can be pulled to either the dc supply voltage V_{dc} (when S1 is ON and S2 is OFF) or to 0 V (when S1 is OFF and S2 is ON). The sum of S1 and S2 drain-source voltages equals the dc bus voltage:

$$v_{ds1} + v_{ds2} = V_{dc}\,. \tag{1.5}$$

The conductive path for the current I_L changes with the switch state. With S1 ON and S2 OFF, I_L flows through the dc supply taking the path labelled (1) in Fig. 1.7 (power is delivered from source to load), and with S1 OFF and S2 ON I_L circulates ('*freewheels*') through S2 on the path labelled (2). Kirchoff's current law dictates that:

$$i_{d1} - i_{d2} = I_L\,. \tag{1.6}$$

The brief interval when the switches change state is known as the *switching transition*. During this transition, I_L *commutates* from one path to the other. The

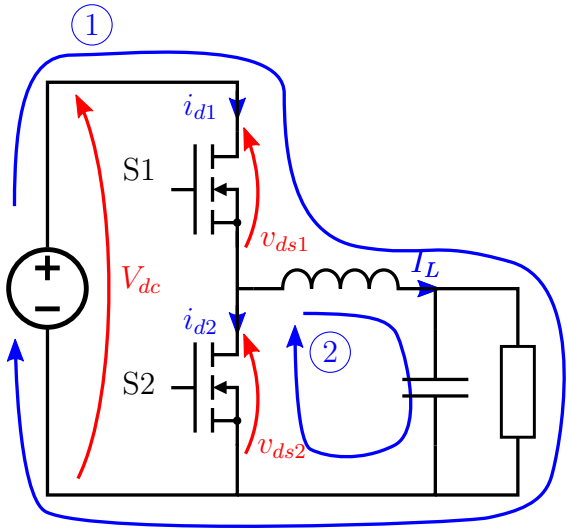


Figure 1.7: A bridge-leg formed by two MOSFETs connected in series between a dc voltage source. Load current I_L takes two distinct paths (1 or 2) depending on the switch state.

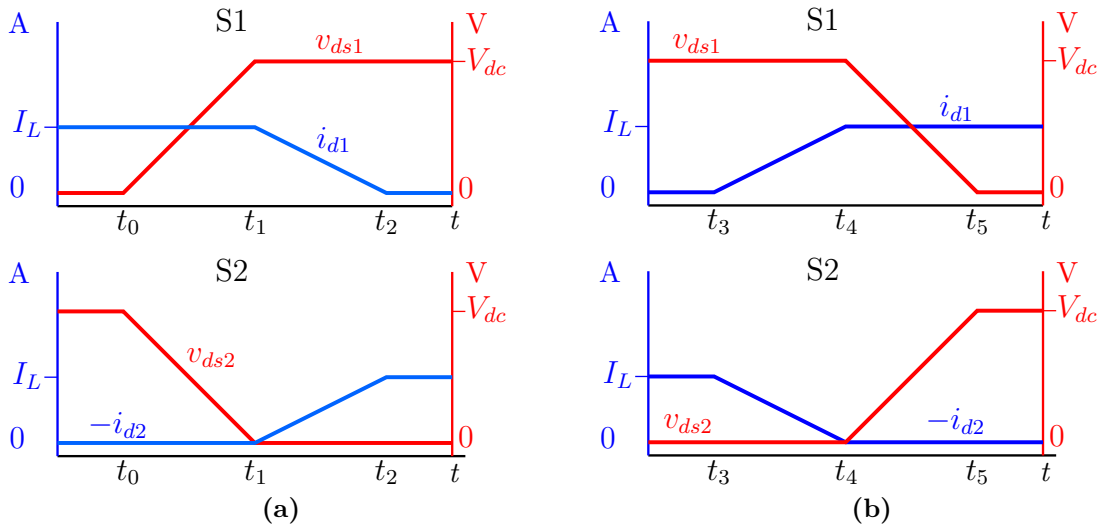


Figure 1.8: Piece-wise linear approximation of the switching transition waveforms for (a) S1 turning OFF and S2 turning ON, and (b) S1 turning ON and S2 turning OFF, for the circuit show in Fig. 1.7.

magnitude of I_L remains approximately constant during the switching transition because the time constant associated with charging/discharging the load inductance is much longer than the time required for the current to commutate between the two paths. To avoid the channels of both switches conducting simultaneously (an energy-dissipating event known as cross-conduction or shoot-through), a *dead-time* period is introduced between the ON switch turning OFF and the OFF switch turning ON. During the dead-time, the current flows through the body-diode of S2 on the path marked (2).

A piecewise-linear approximation of each switch's drain-source voltage and drain current during the switching transition is shown in Fig. 1.8a for S1 turning OFF and S2 turning ON, and in Fig. 1.8b for S1 turning ON and S2 turning OFF [17]. In both cases a separation exists between the voltage rise/fall and the current commutation, because the diode of S2 needs to be forward biased for S2 to conduct.

When S1 turns OFF, the load current I_L charges the output capacitance of S1 and discharges the output capacitance of S2. S1's drain-source voltage v_{ds1} rises to v_{dc} (between times t_0 and t_1 in Fig. 1.8a) until the body-diode of S2 can enter forward bias. Once this happens, the current I_L commutates from path (1) to path (2) and the drain current of S1 falls to zero (between t_1 and t_2).

When S1 turns ON, the voltage of the mid-point is clamped by the body-diode of S2 to 0 V until all the current has commutated from path (2) to path (1) (between t_3 to t_4 in Fig. 1.8b), after which v_{ds1} falls to its low on-state value (between t_4 to t_5). The voltage and current waveforms for S2 are dictated by (1.5) and (1.6).

It is evident from Fig. 1.8 that switch S1 operates in the saturation mode during both switching transitions. Significant power dissipation occurs in the switch during this interval as both v_{ds1} and i_{d1} are non-zero. S1 is sometimes called the 'active' switch since it determines the commutation of I_L and the change in drain-source voltage during the switching transition. On the other hand, in this ideal case S2 experiences no overlap of v_{ds2} and i_{d2}. In S2 the current direction is always from source to drain, meaning that either the channel or body diode can conduct the current. MOSFET S2 can in fact be replaced by a diode, however in practice a

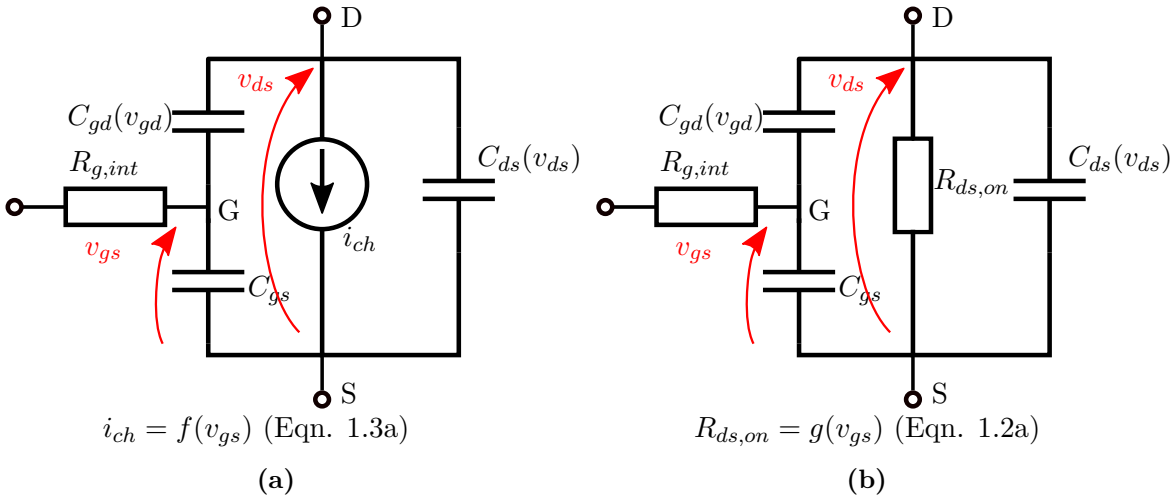


Figure 1.9: Equivalent circuits of MOSFET in (a) saturation, and (b) linear mode.

MOSFET is often used to reduce conduction loss because the voltage drop across the conducting channel can be lower than the p-n junction drop of the diode. The body diode of S2 conducts during the dead-time before the channel of S2 conducts. Known as the *synchronous switch*, S2 behaves simply as a diode during the commutation of I_L and the gating of S2 does not govern the switching transition behaviour.

1.4 Equivalent-circuit model of MOSFET

A common equivalent circuit representation of the MOSFET (Fig. 1.9) models the channel as a voltage-dependent current source or resistance, and considers the internal capacitances between the device terminals. The channel current i_{ch} of the saturated MOSFET (Fig. 1.9a) is a function of v_{gs} (i.e. Eqn. (1.3a)), and the channel resistance of the ohmic MOSFET (Fig. 1.9b) is also a function of v_{gs} (i.e. Eqn. (1.2a)).

The three capacitors C_{ds}, C_{gs}, and C_{gd} in the equivalent circuit are the drain-source, gate-source, and gate-drain capacitances respectively. C_{ds} arises from the pn junction between the n^- drift region and the p body region. The gate is capacitively coupled across the gate oxide to several regions. Coupling between gate and source metallizations, and between the gate and p body leads to a net gate-source capacitance C_{gs}, while coupling between the gate and the n drift region

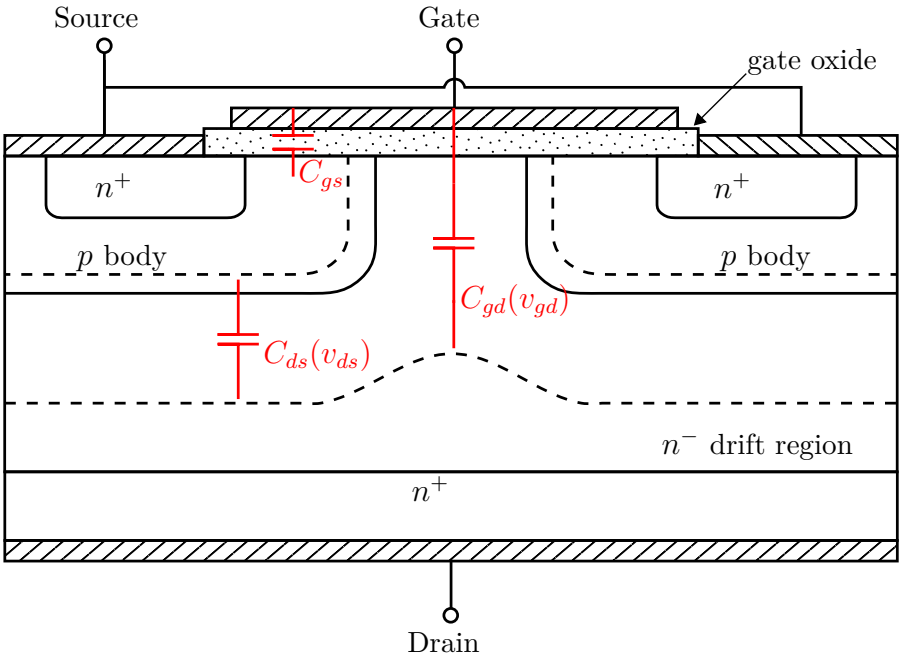


Figure 1.10: The MOSFET lumped internal capacitances C_{gs}, C_{ds}, and C_{gd}.

results in a gate-drain capacitance C_{gd}. These capacitances are illustrated in the cross-section of Fig. 1.10. It is important to note that the strength of the capacitive coupling to the n-drift region depends on the depletion state of the region, a function of drain-source voltage. Therefore the value of the gate-drain and drain-source capacitance is a strong function of drain-source voltage, whereas the gate-source capacitance is relatively independent of bias condition.

1.5 Conventional gate driving

The conventional way to switch a power device is to amplify and level-shift the control pulse-width-modulation signal so that a step voltage is applied to the device gate. An external resistance $R_{g,ext}$ is normally added between the gate drive and the MOSFET to control the charging rate of the device input capacitance. The effective gate charging resistance is the sum of the internal and external resistances:

$$R_g = R_{g,ext} + R_{g,int}\,. \tag{1.7}$$

A parallel resistive path with a series diode can be added between gate drive and MOSFET to provide different $R_{g,ext}$ for turn-ON and turn-OFF. The high and low

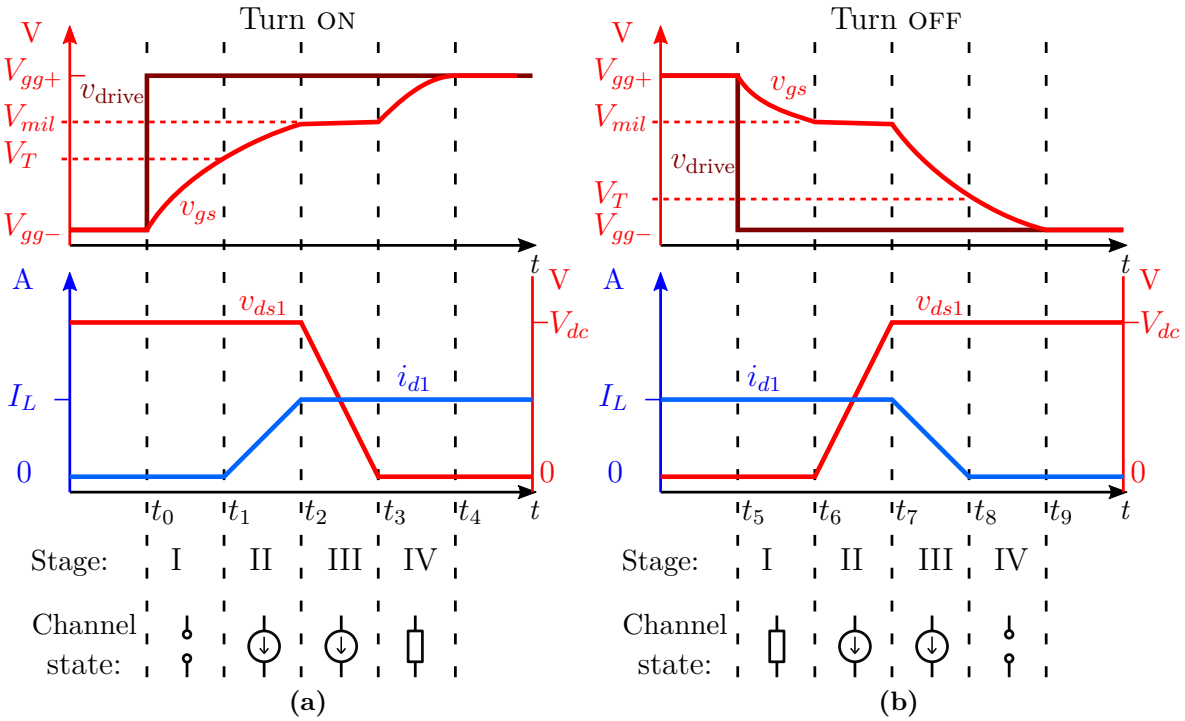


Figure 1.11: Stylised plots of MOSFET switching behaviour showing four distinct periods when driven conventionally (i.e. by a step-input to the gate). (a) Turn-ON, and (b) turn-OFF.

voltage levels that the gate drive output steps between are denoted V_{gg+} and V_{gg-} respectively. The low drive level V_{gg-} is often 0 V, but sometimes is a negative voltage to provide increased immunity against spurious turn-ON of the power device.

An understanding of the switching duration and voltage/current slew-rates is obtained by combining the equivalent-circuit model of the MOSFET with the inductive switching behaviour of the bridge-leg. The transition is normally split into four distinct periods, here denoted I to IV and illustrated in Fig. 1.11. The MOSFET turn-ON waveforms of Fig. 1.11a resemble those of Fig. 1.8, but the gate-source voltage is plotted here which is key to determining the switching speed. The channel condition is also illustrated in Fig. 1.11 to make clear which equivalent circuit model (linear or saturated) is applicable during each period.

Period I begins when the gate drive applies a step input from the hold-off level V_{gg-} to the hold-on level V_{gg+}, and ends when v_{gs} reaches the threshold voltage V_T. The channel is not conductive during this period. A simple exponential curve

describes the voltage rise as the capacitive gate is charged through the series gate resistance during this period:

$$v_{gs}(t) = V_{gg-} + (V_{gg+} - V_{gg-}) \left(1 - e^{\frac{-t}{C_{iss}R_g}}\right) , \tag{1.8}$$

where the input capacitance C_{iss} is the sum of C_{gs} and C_{gd}.

The gate-source voltage continues its exponential rise during period II, and now the drain current rises with it according to (1.3a) as the channel begins to conduct. The rate of rise of drain current is determined by the rate that the channel is opened - i.e. the gate charging time-constant $C_{iss}R_g$ [18]:

$$\frac{\mathrm{d}i_d(t)}{\mathrm{d}t} = \frac{g_m \left(V_{gg+} - v_{gs}(t)\right)}{R_g C_{iss}} , \tag{1.9}$$

where g_m is the transconductance of the MOSFET.

In practice during this period a significant voltage drop often occurs across parasitic inductance common to both the gate and power circuits (the common-emitter inductance L_e), and (1.9) is modified to account for this [18]:

$$\frac{\mathrm{d}i_d(t)}{\mathrm{d}t} = \frac{\left(V_{gg+} - v_{gs}(t)\right)}{L_e + \frac{R_g C_{iss}}{g_m}} . \tag{1.10}$$

Period III begins once the device is conducting the full load current and the opposing device is able to begin blocking voltage. The drain-source voltage falls according to [19]

$$\frac{\mathrm{d}v_{ds}(t)}{\mathrm{d}t} = \frac{I_L - g_m \left(V_{gg+} - V_T\right)}{C_{ds} + C_m + C_{gd} \left(1 + g_m R_g\right)} , \tag{1.11}$$

where C_m is the additional capacitance of switched node (including C_{ds} of opposing device but excluding the MOSFET's own C_{ds}).

During Period III the gate charging current flows predominantly into C_{gd} as v_{dg} falls, the well-known Miller effect. Therefore v_{gs} is approximately constant at the Miller voltage plateau V_{mil}:

$$V_{mil} = V_T + \frac{I_L}{g_m} . \tag{1.12}$$

Period IV commences once the drain-source voltage reaches the steady-state on value and the feedback of $\frac{\mathrm{d}v_{ds}}{\mathrm{d}t}$ to the gate through C_{gd} ceases. The gate-source voltage rises to the hold-on voltage V_{gg+}.

Similar analysis leads to equivalent expressions for the four periods of the turn-OFF transient. The piecewise-linear analysis here assumes that transconductance g_m and capacitances C_{ds} and C_{gd} are constant throughout the switching transition. The change in C_{ds} and C_{gd} with v_{ds} is sometimes (see [17]) partially accounted for by splitting the voltage fall period into two sub-periods, and using a different value for C_{ds} and C_{gd} in each sub-period. Reverse-recovery of the opposing device and parasitic inductance in the power loop also cause switching behaviour to deviate from these simplistic expressions, however the expressions provide insight into the role of R_g and $V_{gg\pm}$ in the switching behaviour. This understanding is used in Chapter 5 to obtain high v_{ds} slew-rates.

It is evident from (1.10) and (1.11) that both the rate-of-change of current during Period II and the rate-of-change of voltage during Period III are functions of R_g and V_{gg+}. It is not straightforward to obtain independent control of these two rates of change through selection of R_g and V_{gg+}. Equation (1.11) also reveals that the rate-of-change of voltage is a function of the load current: at higher load currents the Miller plateau of v_{gs} occurs at higher voltages, meaning that there is a smaller voltage drop across resistance R_g and therefore a lower gate current to discharge C_{dg}. This means that even careful selection of R_g will not result in a constant v_{ds} slew-rate if the load current changes. This becomes particularly apparent for SiC MOSFETs because they have a low transconductance (relative to Si MOSFETs) which means the v_{ds} slew-rate is more strongly a function of load current. Overcoming this limitation of conventional gate driving to obtain independent control of voltage and current slew-rates is one of the motivations behind the Active Gate Drives discussed in Chapter 2.

1.6 The effect of parasitic inductance in the power loop

The discussion of the switching transition of the bridge-leg has so far assumed that the components are connected together by 'ideal' wires which have zero impedance to current flow. In reality, because large currents commutate between different paths in the circuit, the magnetic fields associated with each current path and the effect of these fields on the switching behaviour should be considered. The magnetic fields create an impedance to changes in current flow known as inductance. The relationship (Faraday's law of induction) between the voltage v across an inductor and the current i flowing through it is [20]

$$v = L\frac{\mathrm{d}i}{\mathrm{d}t}\,, \tag{1.13}$$

where the inductance L is the amount of magnetic flux linked by the current path per unit current flow (units Wb/A or equivalently H).

A conductive path can be divided into segments, each of which contributes a certain parasitic inductance. For the bridge-leg considered here, contributions to parasitic inductance come from the dc link capacitors, PCB traces, semiconductor package leads and bond-wires (Fig. 1.12a). For analysing the switching transition, all such inductances can be summed to give a single equivalent inductance, because all undergo the same $\frac{\mathrm{d}i}{\mathrm{d}t}$ (Fig. 1.12b).

During switching, the commutation of the load current through this parasitic inductance L_p results in different voltage waveforms for the active switch than shown in the idealised (zero-inductance) plots of Section 1.5. From Fig. 1.12b, we see that

$$v_{ds1} + v_{Lp} + v_{ds2} = V_{dc}\,, \tag{1.14}$$

where

$$v_{Lp} = L_p\frac{\mathrm{d}i_{d1}}{\mathrm{d}t}\,, \tag{1.15}$$

so that

$$v_{ds1} = V_{dc} - L_p\frac{\mathrm{d}i_{d1}}{\mathrm{d}t} - v_{ds2}\,. \tag{1.16}$$

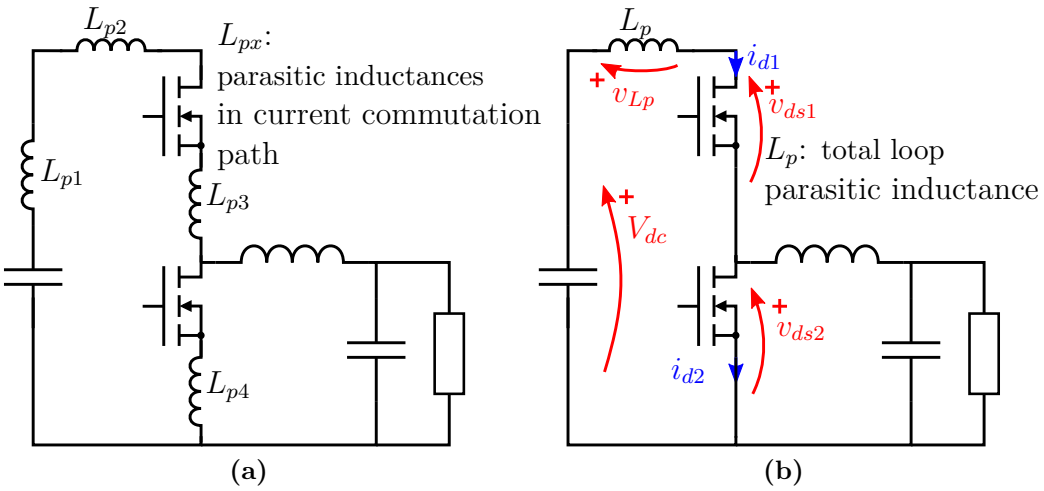


Figure 1.12: The distributed parasitic inductance present in the current commutation path (a) can be lumped into a single inductance (b) for the purpose of analysing switching behaviour.

During the current commutation period (Period II of turn-ON and Period III of turn-OFF), the voltage drop across S2 is the diode forward voltage and is negligible:

$$v_{ds2} \approx 0\,, \tag{1.17}$$

so that

$$v_{ds1} \approx V_{dc} - L_p \frac{\mathrm{d}i_{d1}}{\mathrm{d}t}\,. \tag{1.18}$$

Fig. 1.13 shows piecewise-linear approximations of the voltage considering the effect of L_p. During turn-ON (Fig. 1.13a) $\frac{\mathrm{d}i_{d1}}{\mathrm{d}t}$ is positive and the voltage across the switch is suppressed below V_{dc}, whereas during turn-OFF (Fig. 1.13b) the negative $\frac{\mathrm{d}i_{d1}}{\mathrm{d}t}$ forces the switch voltage above V_{dc}.

1.7 Switching energy loss

The energy dissipated in the switch during the switching transition is called the switching loss. The instantaneous power dissipation in the switch is the product of the voltage across the switch and the conducted current. Integration of the instantaneous power over the switching transition results in the energy lost during the transition [21]

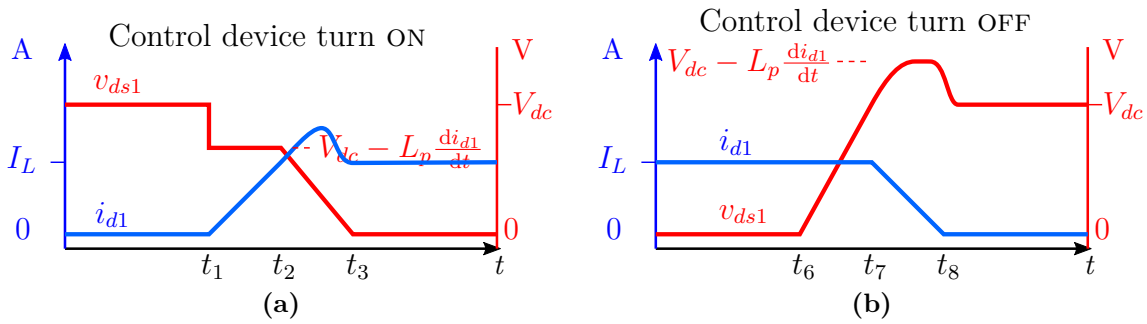


Figure 1.13: Modified piecewise-linear waveforms of bridge-leg switching showing the approximate effect of parasitic inductance. MOSFET voltage is reduced during (a) turn-ON, but increased during (b) turn-OFF.

$$\begin{aligned} E_{\text{sw}} &= E_{\text{on}} + E_{\text{off}} \\ &= \int_{t_0}^{t_4} \left(v_{ds} i_d + v_{gs} i_g\right) .\mathrm{d}t + \int_{t_5}^{t_9} \left(v_{ds} i_d + v_{gs} i_g\right) .\mathrm{d}t \,, \end{aligned} \tag{1.19}$$

where t_0, t_4 and t_5, t_9 are respectively the start and end times of the turn-on and turn-off switching event. The power dissipation from the gate current i_g is often an insignificant fraction of the total dissipation and is ignored.

Simple expressions for switching energy loss ignoring parasitic inductance are obtained by applying (1.19) to the piecewise-linear waveforms presented in Section 1.5. For turn-ON

$$E_{\text{on}} = \frac{1}{2} V_{dc} I_L \left(\tau_{cr} + \tau_{vf}\right) \,, \tag{1.20}$$

where τ_{cr} is the duration of the current rise interval (Period II in Fig. 1.11a - i.e. $(t_2 - t_1)$) and τ_{vf} is the duration of the voltage fall interval (Period III in Fig. 1.11a - i.e. $(t_3 - t_2)$).

Similarly for turn-OFF

$$E_{\text{off}} = \frac{1}{2} V_{dc} I_L \left(\tau_{vr} + \tau_{cf}\right) \,, \tag{1.21}$$

where τ_{vr} is the duration of the voltage rise interval (Period II in Fig. 1.11b - i.e. $(t_7 - t_6)$) and τ_{cf} is the duration of the current fall interval (Period III in Fig. 1.11b - i.e. $(t_8 - t_7)$).

Evaluating (1.19) using the waveforms accounting for parasitic inductance (Fig. 1.13) yields

$$E_{\text{on}} = \frac{1}{2} V_{dc} I_L \left(\tau_{cr} + \tau_{vf}\right) - \frac{1}{2} L_p I_L^2 \left(1 + \frac{\tau_{vf}}{\tau_{cr}}\right) , \tag{1.22}$$

$$E_{\text{off}} = \frac{1}{2} V_{dc} I_L \left(\tau_{vr} + \tau_{cf}\right) + \frac{1}{2} L_p I_L^2 . \tag{1.23}$$

The effect of the parasitic inductance is to reduce the turn-ON loss and increase the turn-OFF loss and the total switching loss is approximately unchanged.

1.8 Output capacitance losses

This analysis of switching loss based on piece-wise linear voltage and current waveforms suggests that the loss tends towards zero as the voltage and current transitions become sharper. However a lower bound on loss exists for hard-switching due to capacitive charging/discharging during the switching cycle. To determine the value of the lower bound on switching loss, assume that the parasitic inductance in the commutation loop is negligible and that the active switch channel can transition from conducting to blocking instantaneously (implying instantaneous charging of the active switch's gate). Under these conditions the load current commutates instantaneously, therefore the only non-zero loss components in (1.20) and (1.21) are during the voltage rise and fall intervals. As the switch voltages change, energy is added or removed from the switch drain-source capacitances C_{ds} (often called the output capacitance C_{oss}).

When S1 is OFF and S2 is ON, the energy stored in the output capacitance of S1 is

$$E_{c1} = \frac{1}{2} V_{dc}^2 C_{oss1} , \tag{1.24}$$

where C_{oss1} is the energy-equivalent capacitance of S1 (different from the charge-equivalent capacitance of S1 because C_{ds1} is non-linear with respect to v_{ds1} [22]). No energy is stored in the output capacitance of S2 since its drain-source voltage is approximately zero:

$$E_{c2} = 0 . \tag{1.25}$$

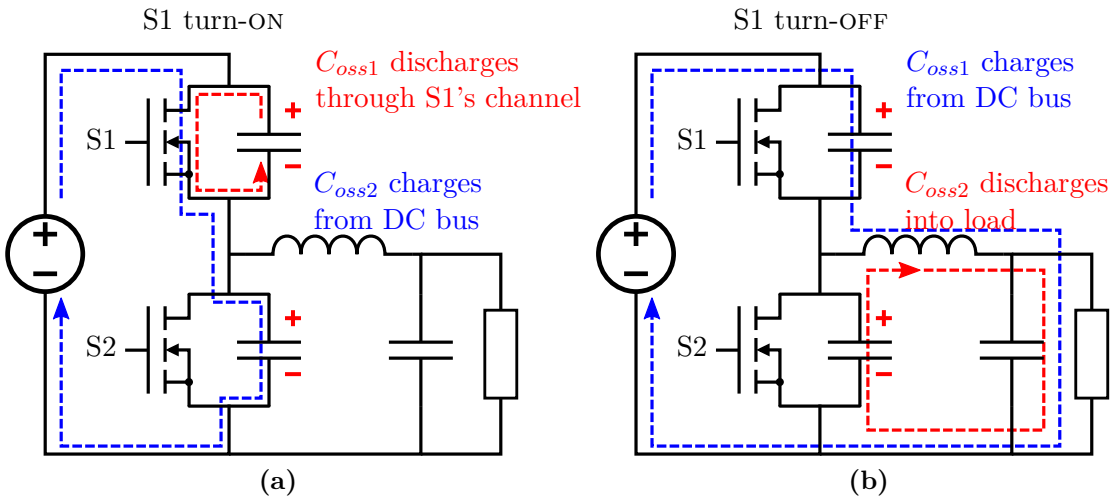


Figure 1.14: Capacitive charging/discharging currents associated with (a) S1 turn-ON, and (b) S1 turn-OFF.

Fig. 1.14a illustrates the capacitive currents during the transition when S1 turns-ON. The energy in S1's output capacitance is dissipated internally in S1. Simultaneously the output capacitance of S2 is charged from the dc-bus. An energy of $V_{dc}^2 C_{oss2}$ is supplied by the dc-bus, half of which is dissipated in S1, and the other half is stored in C_{oss2}. Therefore at the end of the transition,

$$E_{c1} = 0 \tag{1.26}$$

$$E_{c2} = \frac{1}{2} V_{dc}^2 C_{oss2}\,. \tag{1.27}$$

Fig. 1.14b illustrates the capacitive currents during the subsequent transition when S1 is turning OFF. This transition is driven by the load current flowing in the output inductor and the rate of change of voltage is determined by the magnitude of the load current. The dc-bus delivers $\frac{1}{2} V_{dc}^2 C_{oss1}$ to S1 as its output capacitance is charged. The energy stored in C_{oss2} is delivered into the load rather than being dissipated.

Over the entire switching cycle, energy stored in the output capacitances of S1 and S2 is only dissipated during the transition when S1 turns ON (Fig. 1.14a), with the total dissipation being

$$E_{c,\text{loss}} = \frac{1}{2} V_{dc}^2 \left(C_{oss1} + C_{oss2}\right)\,. \tag{1.28}$$

This lower bound on loss for hard-switching is useful to keep in mind when considering the extent to which losses can be reduced by the gate drive (the topic explored in Chapter 5), and is especially relevant at very low load currents when the actual switching loss approaches the limit.

1.9 Reverse-recovery

The behaviour of a *pn* junction as it changes from forward-conducting to reverse-blocking state is known as the *reverse-recovery* of the junction. Excess minority carriers which are stored during forward-conduction of the junction recombine or are swept away from the junction. The reverse-recovery of diodes contributes to the switching loss of the power converters.

This effect is particularly prominent in *pin* devices, which have an intrinsic or lightly doped n-type drift region in order to obtain a high reverse breakdown voltage (Fig. 1.15a). During steady-state conduction, the distribution of the excess minority carriers (holes) in the drift region is determined by the flux of holes injected across the forward-biased junctions, and the recombination of the holes within the drift region. Since the lifetime of these carriers (mean time before they are recombined) can be hundreds of nanoseconds or longer, this means that when the polarity of the applied voltage is reversed, a negative current (from cathode to anode) can flow for a short time as the excess minority charge is removed.

The particular manner in which the excess charge is removed from the freewheeling diode determines the profile of the diode terminal voltage and current over time, and therefore affects the switching behaviour of the bridge-leg. The reverse-recovery behaviour of high-voltage *pin* diodes has been extensively investigated [16, 23, 25, 26] and found to depend both on parameters internal to the diode (such as minority carrier lifetime, doping profile, and length of drift region) and external factors (such as circuit parasitic inductance, forward current, and junction temperature) [27].

In general, the negative terminal current simultaneously removes excess charge from the n^- drift region and charges the depletion capacitances of the two junctions. Fig. 1.15b shows a stylised plot of how the stored charge in the drift region can

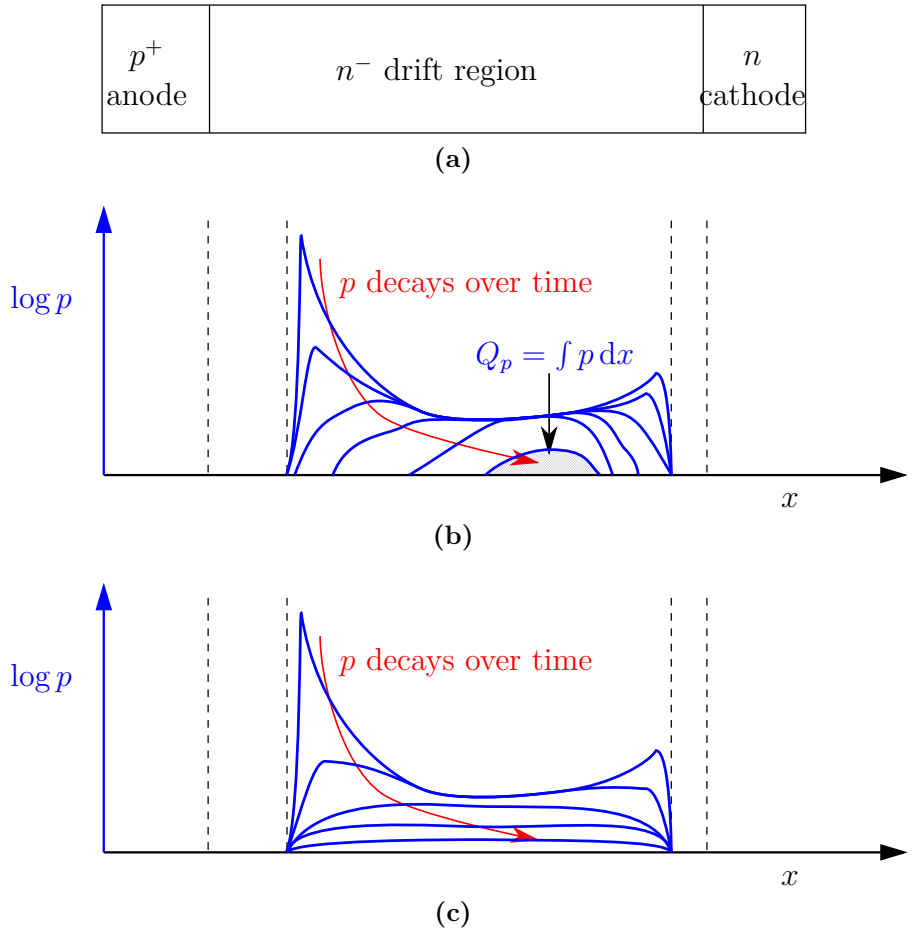


Figure 1.15: (a) Schematic of a *pin* diode's structure, illustrating the lightly-doped or intrinsic drift region which stores charge during conduction. (b) Stylised plot of how the stored charge decays during reverse-recovery (adapted from the numerical simulation results in [23]). (c) A special case where all the stored charge is removed or recombined before the depletion capacitances are charged (adapted from the stylised plot in [24]).

decay over time during reverse-recovery. The dashed lines show the positions of the depletion layer edges at steady-state before the reverse current is applied. The depletion layers are able to grow once the excess charge has fallen to zero at the edges of the drift region (but excess charge may still exist in the interior of the drift region during this time, as illustrated). As the depletion capacitances are charged, the terminal voltage across the diode can rise appreciably, while the reverse current is still removing the excess charge from the interior of the drift region. Modelling the reverse current and the simultaneous rise in terminal voltage requires solving the ambipolar diffusion equation for the stored charge in the n^- drift region, with appropriate boundary conditions that account for the expanding

depletion regions (see for example [25]).

A specific reverse-recovery behaviour occurs when the excess charge is completely removed from the drift region before the depletion capacitances are charged. Fig. 1.15c schematically illustrates the excess charge profile across the drift region in this case. This is the behaviour modelled by the standard Berkeley SPICE circuit simulation tool, which assumes that the diode excess charge Q_p is a function of the junction voltage $V_j(t)$, with no explicit dependence on time other than through V_j (the *quasi-static* description of the excess charge) [24, 28]:

$$Q_p = \tau_p I_{ss} \left(e^{\frac{V_j}{V_{th}}} - 1 \right) , \tag{1.29}$$

where τ_p is the excess charge lifetime, I_{ss} is the reverse saturation current, and V_{th} is the thermal voltage.

This means that all the reverse current which removes Q_p occurs while V_j is a small forward-biasing potential, and that Q_p has necessarily fallen to zero by the time that the junction enters reverse-bias. Once Q_p has fallen to zero the impressed reverse current rapidly charges the depletion capacitance. This leads to an abrupt rise of the reverse voltage while the reverse current 'snaps off' [27]. Energy stored in the circuit parasitic inductance oscillates between the circuit inductance and the diode depletion capacitance.

Fig. 1.16a shows example waveforms of this behaviour obtained by SPICE simulation. Once the diode junction becomes reverse-biased, the terminal voltage is forced well above the dc-bus voltage by the ringing. This is referred to as 'snappy' reverse-recovery in this thesis. (Note that sometimes the term 'snappy' is used to refer specifically to the phenomenon where, under sufficiently high reverse bias, the depletion layers at either side of the drift region meet leading to a dramatic drop in diode capacitance and particularly large-amplitude high-frequency ringing [23].)

A widely-adopted modification to the standard SPICE diode model is to add a term to (1.29) to make Q_p dependent on its own rate of change [24]:

$$Q_p = \tau_p \left[I_{ss} \left(e^{\frac{V_j}{V_{th}}} - 1 \right) - v_p \frac{\mathrm{d}Q_p}{\mathrm{d}t} \right] . \tag{1.30}$$

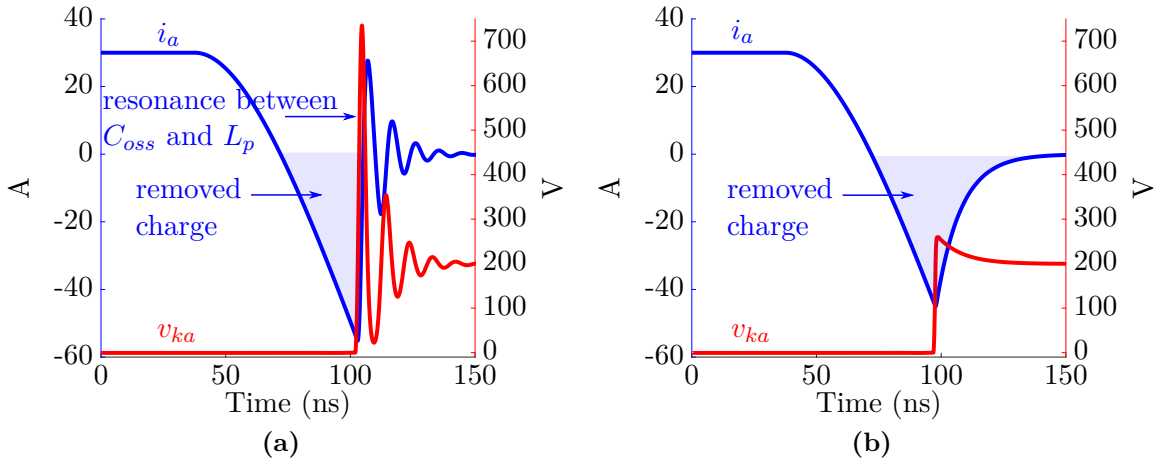


Figure 1.16: Diode reverse recovery waveforms from SPICE simulation for (a) 'snappy' recovery and (b) 'soft' recovery. SPICE diode parameters: $I_s = 2\,\text{nA}$, $C_{jo} = 2\,\text{nF}$, $TT = 50\,\text{ns}$. Circuit $L_p = 15\,\text{nH}$. In (b) damping term $v_p = 0.3$ (see Eq. 1.30).

This acts as a damping term and results in a more gradual decay in the reverse-current, as shown in Fig. 1.16b. The lower current slew-rate induces a smaller voltage peak across the diode than in the snappy recovery case. This behaviour better models the reverse-current waveforms of soft-recovery diodes (although the modification lacks a physical basis and the rise in diode voltage is not properly modelled).

This theory describing the reverse-recovery behaviour of *pin* diodes is returned to in Chapter 3 where it is used to derive analytical expressions relating the switching energy loss to the peak voltage across the diode.

1.10 Structure of this thesis

This introductory chapter has outlined the operating principles of the inductive-switched bridge-leg, the effect of the conventional gate drive on the MOSFET/IGBT switching behaviour, and other background theory pertinent to understanding this thesis. Parasitic inductance in the current commutation loop was shown to induce peak transient voltages in excess of the dc bus voltage across the power semiconductor devices, with higher peak voltages occurring for higher rates-of-change of current. At the same time, a simple calculation of switching energy loss showed that the losses are reduced by increasing the rate-of-change of current commutation.

The remainder of the thesis is structured as follows. Chapter 2 introduces the concept of an Active Gate Drive (AGD) and reviews the AGDs proposed in the literature. Particular attention is paid to the AGDs which actively manage the trade-off between switching energy loss and peak transient voltage across the semiconductors. In Chapter 3, one of these pre-existing gate drivers is used to explore the extent to which the the switching energy loss and the peak transient voltage can be traded between. This is built upon in Chapter 4 where the practical benefits of being able to tune this trade-off dynamically (during converter operation) is investigated in terms of the achievable increase in power processing capability of the power semiconductor device. Chapter 5 explores how careful design of the power loop can solve the problem of transient voltage overshoot, and how the high switching speeds possible when using wide band-gap semiconductors can be obtained. The contributions made in the thesis are summarised in Chapter 6 along with suggestions of promising future avenues of enquiry.

2

Active gate driving in the literature

In recent years there has been considerable interest in using the gate drive not only to take the power device from the cut-off to the ohmic regime, but also to control the trajectory that the device takes when switching between these regimes. This chapter reviews the approaches that have been published to date for power devices that are hard-switched.

Table 2.1 provides a summary of selected active gate drives that have been proposed since 1996. The 'Type' classification indicates the sort of control approach is used. OL is open loop, where the switching control strategy is not informed by feedback of behaviour during operation. CL is conventional closed loop control, where feedback of a signal is compared against a reference, and the control actuation is based on the error between the two signals. IT is iterative control, where the control actuation is adapted based on feedback of device behaviour, but only between (not during) switching transients. SD stands for stage-detection, where the switching transition is divided into stages (for example the stages outlined in Section 1.5) based on some measurement of the switching behaviour, and the control actuation changes depending on the switching stage. The examples that follow will illustrate the distinctions between these types.

First Author(s)	Year	Power device	Type	Control reference	Controlled quantity	Comments
Gerster [29]	1996	Si IGBT	CL	$\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}$ & $\frac{\mathrm{d}i_c}{\mathrm{d}t}$	Voltage balancing of series IGBTs	
Hofer-Noser [30] [31]	1996, 1999	Si IGBT	IT	Emitter current.	v_{ge} rise/fall delay (transient balancing), v_{ge} magnitude (static balancing)	Current balancing of paralleled modules
Park [32, 33]	2001, 2003	Si IGBT	CL	$\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}$ & $\frac{\mathrm{d}i_c}{\mathrm{d}t}$		
Bortis [34]	2008	Si IGBT	IT	Emitter current.	v_{ge} rise/fall delay (transient balancing), v_{ge} magnitude (static balancing)	Current balancing of transformer-coupled modules.
Alvarez [35]	2010	Si IGBT	CL	Current balancing of paralleled modules		
Palmer [36] Wang [37] Bryant [38] Lim [39]	2004, 2006, 2007, 2013	Si IGBT	CL & IT	v_{ce} profile (varying dv/dt)	v_{ge} - P compensator	Voltage balancing of series IGBTs
Fink [40]	2013	Si IGBT	CL	$\frac{\mathrm{d}i_c}{\mathrm{d}t}$		
Dang [41]	2013	Si IGBT	IT, SD			
Oswald [42] [43]	2012, 2014	Si IGBT	OL	-	3-stage PWL v_{ge}	Reducing high frequency spectral content in i_c and v_{ce}
Dymond [44] [45]	2017, 2018	GaN FET [45], SiC MOSFET [44]	OL	-	R pull-up/down, updatable at 150ps resolution.	

First Author(s)	Year	Power device	Type	Control reference	Controlled quantity	Comments
Tripathi [46]	2016	SiC MOSFET	OL	-	Rg selectable between two values for turn-on	
Zeng [47]	2018	SiC MOSFET	OL	-	R_g, external added C_{gs}, gate drive voltage levels	Switching rates of change, time delays, overshoots investigated as function of gate drive parameters.
Zhang [48]	2017	SiC MOSFET	OL	-	Duration of v_{gs} levels.	Slew rates, cross-talk suppression, investigated with multi-level gate drive.
Camacho [49]	2017	SiC MOSFET	OL	-	R_g selectable between two levels for turn-on and turn-off	R_g switched by comparator with feedback of v_{gs}
Nayak [50] [51]	2017, 2018	SiC MOSFET	SD	Gate drive voltage level, gate resistance	Stage detect based on v_{ds} and i_d	
Zhang [52]	2017	Si IGBT	IT, SD	Duration of dv/dt di/dt stages	Gate drive current, active duration of gate drive current source	Voltage balancing of series IGBTs
Velander [53] [54]	2015, 2018	SiC MOSFET [54], Si IGBT [53]	OL (LUT)	-	Gate drive current	Goal is to reduce dV/dt of opposing diode
Lobsiger [55] [56] [57] [58]	2012-2015	Si IGBT	CL	$\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}$ & $\frac{\mathrm{d}i_c}{\mathrm{d}t}$	v_{ge} & i_g	
Shu [59]	2017	Si IGBT	CL	$\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}$ & $\frac{\mathrm{d}i_c}{\mathrm{d}t}$	i_g	

First Author(s)	Year	Power device	Type	Control reference	Controlled quantity	Comments
Chen [60]	2009	Si IGBT	CL	$\frac{\mathrm{d}i_c}{\mathrm{d}t}$	i_g	
Riazmontazer [19] [61]	2015	SiC MOSFET	CL	$\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}$ & $\frac{\mathrm{d}i_c}{\mathrm{d}t}$	i_g	Laser driver for optically triggered driver FETs
Wang [18]	2014	Si IGBT	SD	i_g	i_g boost provided during delay stage of switching	
Blank [62]	2015	Si MOSFET	IT	i_g		
Rogers [63]	2016	Si IGBT	IT	v_{ge}		Output update rate is 7 ns. Output amplifier large-signal bandwidth is 40 MHz.
Gluck [64]	2018	Si MOSFET	IT	$\frac{\mathrm{d}v_{ds}}{\mathrm{d}t}$ & $\frac{\mathrm{d}i_d}{\mathrm{d}t}$	i_g	
Pan [65]	2018	Si IGBT	SD	R_g		
Yang [66]	2019	SiC MOSFET	SD	Gate drive voltage level	Similar multi-level drive as in [48], with addition of feedback for stage detection	
Obara [67] Miyazaki [68, 69] Cheng [70–72] Yamaguchi [73]	2016-2019	Si IGBT, SiC MOSFET	OL (LUT)			

Table 2.1: A review of selected active gate driving publications from 1996-2020. Abbreviations: OL - Open Loop; LUT - Look-up Table; CL - Closed Loop; IT - Iterative; SD - Stage Detection. The gate driver used in this thesis is taken from the work highlighted in blue.

2.1 Common objectives of AGD

The objectives of AGD which are stated in the publications are diverse. A common objective of AGD is to control the slew-rate of current conducted through the device, and/or the slew-rate of voltage across the device. Controlling these slew-rates was first investigated with the purpose of obtaining equal voltage sharing of series-connected devices [29, 36–39, 52, 74–76], or equal current sharing of parallel-connected devices [30, 31, 34, 35]. Series-connecting devices to increase the blocking voltage capability is a particular challenge for devices whose resistance/voltage-drop increases with temperature (MOSFETs and many IGBTs) since any voltage imbalance is amplified by the positive feedback introduced by self-heating. Conversely, the increase in resistance/voltage-drop with self-heating serves to equalise current-sharing between these devices when they are paralleled: AGDs may not be required to obtain current-sharing of these positive temperature-coefficient devices but they can assist in achieving balancing if the current slew-rates of all devices are controlled to be equal [34].

Control of voltage and current slew-rates using AGD has gained attention not only for voltage/current sharing between devices, but also as a means to influence the trade-off between switching energy loss, electromagnetic interference (EMI), and semiconductor peak voltage stress. The link between voltage and current slew-rate and switching loss is clear for hard-switching, as described in Chapter 1. Device turn-off transient voltage overshoot is also well understood to be a function of the slew-rate of the falling current. For other switching features however, the slew-rates of voltage and current are a somewhat indirect control input for modifying the feature of interest.

An example is switching EMI: many AGDs are proposed to influence conducted or radiated EMI in some way. However the direct relationship between switching slew-rate and the EMI criterion of interest is difficult to model precisely, because it depends on the environment surrounding the bridge-leg - for example filters, shielding, and grounding layouts. One approach, taken in [42–45], is to compare the spectral content of the voltage and current waveforms inside the converter, for

different gate driving strategies, and make a judgement about the implications of different spectra on the EMI outside the converter. Since the EMI implications of particular voltage/current spectra are highly application-specific, it is not immediately apparent to what extent the switching edges should be slowed down, incurring additional switching energy loss, in order to obtain a reduction in high-frequency spectral content of the voltage/current waveforms. However these publications provide a means for the EMI and switching loss to be traded between, which can be made use of when choosing between the two in a particular application. An extreme application might be the driving of an electrical machine directly from a bridge-leg without a low-pass filter between the two (as in [53]), in which case the output (switched-node) voltage rate-of-change may be constrained by the insulation degradation properties of the machine windings.

2.2 Strategies for adaptive AGD

The diverse motivations for using AGD are reflected in the correspondingly wide range of ways the AGDs are implemented. An overview of the types of control implemented in the AGDs of Table 2.1 is presented in Fig. 2.1. Here the major classifications are Open Loop, Iterative, Stage-Detection, and Closed Loop control.

2.2.1 Open loop control

Several AGD proposals demonstrate sophisticated tailoring of the gate voltage/current to achieve a particular aim, but the gate actuation does not adapt based on measurements of switching behaviour. These are therefore classified as open-loop methods, although many are suitable for extension to a iterative control (see Section 2.2.3). The technique in [44, 45] is a good example of this, where a gate drive with finely adjustable output current and a 150 ps update rate is applied to reduce ringing and EMI for GaN power switches. This update rate is the highest achieved for a gate drive to date, and is especially promising for controlling the switching trajectory of the fast-switching GaN devices. The adjustable output current is achieved by selecting the number of parallel driver MOSFETs which

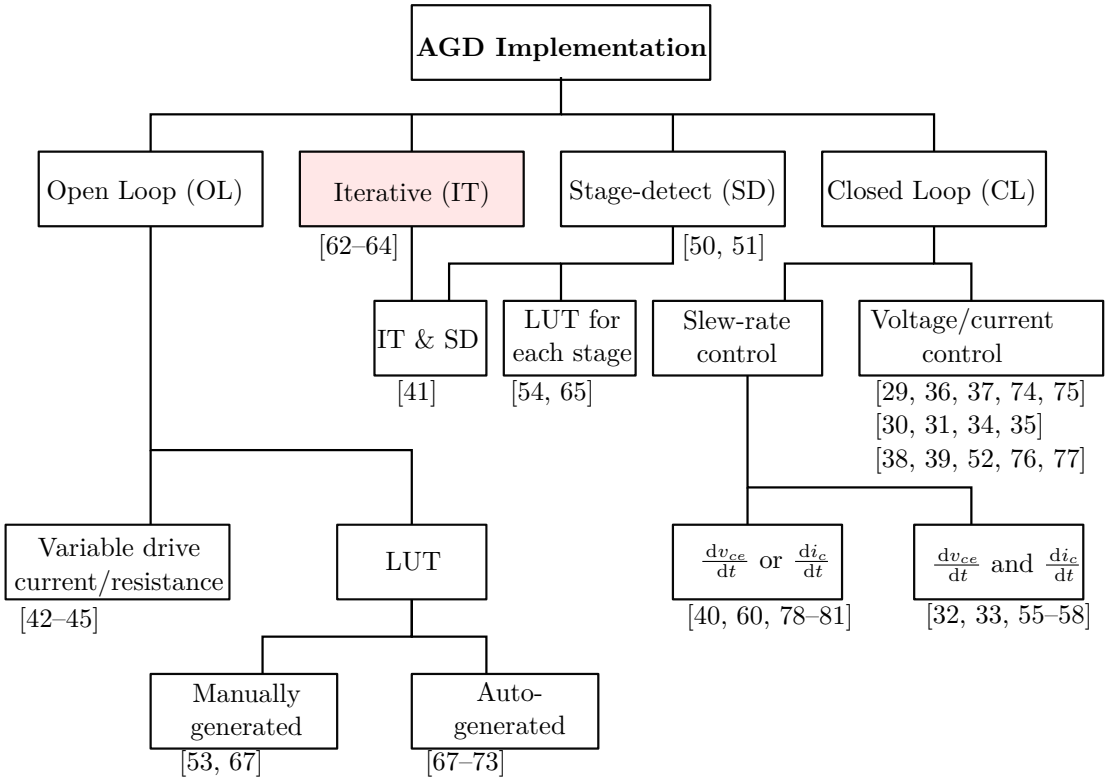


Figure 2.1: AGDs classified by how they are implemented. The implementation category explored in this thesis, iterative control, is highlighted.

each source/sink an approximately constant current in their saturation mode. The gate drive current profile is manually selected in the laboratory setting, but could be extended to iteratively adapt 'online'.

An extension of the open loop approach is to combine it with a 'look-up table' (LUT), i.e. a database containing a number of different gate actuations, each associated with a particular operating condition. During online operation the operating condition is monitored and the relevant gate actuation strategy is looked-up in the table and used. For example in [53] the gate drive current for an IGBT is selected from a LUT based on the load current and the device temperature (i.e. a two-dimensional LUT) with the objective of obtaining a constant switched-node voltage slew-rate (which would normally be a function of load current and temperature). The advantage of the LUT scheme is that no specialised measurements need to be taken during operation - in this case only the load current and device

temperature are required (both relatively low-bandwidth signals that are often already measured for other purposes).

A drawback of the LUT approach is the work required to gather the data to populate the table. If the desired gate actuation depends on several variables, or if the actuation itself has many degrees of freedom, it can quickly become impractical to manually create the table. Optimisation routines can be used to automatically populate gate-drive LUTs. Algorithms such as 'simulated annealing' [69] and 'particle swarm optimisation' [70] are reported to take between 15-60 minutes to create a LUT containing gate drive current profiles for a range of load currents. However because the LUTs are generated 'offline' prior to converter operation, when the gate actuation is based solely on a LUT then the switching behaviour is susceptible to disturbances from sources that were unforeseen or not included in the LUT.

2.2.2 Closed-loop control

Closed-loop control provides a method for compensating for disturbances during converter operation by using feedback of the switching behaviour. One reason for the popularity of slew-rate control (despite the often indirect connection between voltage/current slew-rate and the switching feature of interest) is that slew-rates are relatively straightforward to measure and control in a closed-loop manner. Feedback of collector-emitter voltage slew-rate is obtained in [29] by measuring the current through a capacitor connected between collector and emitter. Similarly, collector current rate of change can be measured by the voltage drop across the common emitter inductance (the inductance between the 'kelvin emitter' to which the gate drive is referenced and the emitter power terminal) [29]. These slew-rate signals can be used as feedback for closed-loop control of the voltage and current rates of change using analogue electronics. This is demonstrated for $\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}$ control during turn-OFF and $\frac{\mathrm{d}i_c}{\mathrm{d}t}$ control during turn-ON in [29], for $\frac{\mathrm{d}i_c}{\mathrm{d}t}$ control during both turn-ON and turn-OFF in [60, 78, 80, 81], for $\frac{\mathrm{d}i_c}{\mathrm{d}t}$ control during turn-ON in [40], and for control of both $\frac{\mathrm{d}i_c}{\mathrm{d}t}$ and $\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}$ during both turn-ON and turn-OFF in [32, 33].

A drawback of controlling both $\frac{\mathrm{d}i_c}{\mathrm{d}t}$ and $\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}$ for turn-ON and turn-OFF is the complexity of combining all the separate control circuits and switching between them. This is mitigated to some extent in [55–58] where a single analogue circuit implements PI control for $\frac{\mathrm{d}i_c}{\mathrm{d}t}$ and $\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}$ by exploiting the natural separation between current and voltage slopes during hard-switching.

Closed-loop control is not limited to obtaining linear rises/falls in the current and voltage waveforms. It is shown in [82] that shaping the switching edges to follow a Gaussian (infinitely differentiable) profile is optimal for reducing the high-frequency spectral content of the signal for a given switching duration. However this is not experimentally realised: implementing complicated reference shapes becomes increasingly difficult with an approach based purely on analogue electronics.

Implementing AGD using digital logic is attractive as it provides greater flexibility in choosing the control objective, allows adaptation to changes in circuit parameters and operating point, and provides the possibility to optimise certain aspects of the switching behaviour 'online' [41]. However obtaining high control-loop bandwidth is a particular challenge for digital implementations, because latency in analogue to digital converters (ADCs) and digital to analogue converters (DACs) combines to introduce input-output delays of more than 30 ns into the control loop (even when using fast ∼1 GS/s ADCs and DACs) [63]. This limits the bandwidth (slew-rates) of the voltage and current signals that can be controlled in closed-loop. Digital closed-loop control of $\frac{\mathrm{d}v_{ce}}{\mathrm{d}t}$ is implemented on an FPGA in [79], however the highest slew-rate obtained is only 2 V/ns. With the key to lower switching energy loss being higher slew-rates, the relatively low bandwidth of a closed-loop digital controller is a significant constraint. Even as the speed of digital logic has increased, so too have the switching slew-rates of the power electronics, so this constraint remains an issue.

2.2.3 Iterative control

Iterative control is a popular way of accommodating the latencies in the digital control loop. With iterative control, rather than adapting the gate actuation based on feedback *within* a switching transition (e.g. with a 1 ns update time), the update

is made *between* switching transitions. This provides an entire switching period (e.g. 10 µs for 100 kHz switching) for processing the data acquired during the previous switching transition and calculating the next control output (typically the gate voltage/current profile to be applied at the next switching transition).

Iterative control has advantages beyond accommodating latencies in the digital control loop: it enables information about the whole switching transition (e.g. switching loss, obtained by post-processing data acquired during the transition) to be used to inform the control action on the next transition. Conventional closed-loop control cannot accomplish this, as it is limited to instantaneous measurements.

An example is [63] where switching energy loss is minimised subject to a constraint on maximum switch voltage. Current and voltage waveforms are captured during the switching transition, from which switching energy loss and peak voltage stress are obtained in post-processing. The gate-control (a piecewise-linear voltage reference) is automatically optimized based on the extracted data (using the Patternsearch routine [83]). This approach showcases the potential of iterative control because it controls behaviours which have a direct impact on the converter performance (the semiconductor voltage rating must not be exceeded, and switching loss is undesirable for reasons of efficiency and power density), in contrast to approaches that control behaviours (e.g. voltage/current slew-rates) which are only indirectly related to converter performance.

A similar trade-off between switching energy loss and peak transient voltage is explored in [68, 69], however here the peak transient voltage is treated not as a constraint (as in [63]) but as a factor in the objective function to be minimised, for instance

$$f_{\mathrm{OBJ}} = \sqrt{E_{\mathrm{loss}}^2 + V_{\mathrm{overshoot}}^2} \tag{2.1}$$

where f_{OBJ} is the objective function, and E_{loss} and $V_{\mathrm{overshoot}}$ are normalised values of the energy loss and peak voltage, respectively. The value of this approach is unclear, since it is not explained how to choose the relative weighting between energy loss and peak voltage in the objective function, and given that the semiconductor

switches have a rated maximum voltage, it would seem more natural to treat peak voltage as a constraint.

2.2.4 Stage-detection

Yet another control approach is to divide the switching transient into different time periods (often based on the switching stages outlined in Section 1.5) and use feedback to detect the transitions from one stage to the next. Different control strategies can be implemented during each stage. For example in [51] a different gate drive resistance is used for each of four stages of MOSFET switching; the transition between stages is detected based on drain current and drain-source voltage. A low gate resistance is used in the first stage to reduce turn-ON/OFF delay, with a higher gate resistance used in later stages to limit current/voltage slew-rate.

The stage-detection technique can be combined with the look-up tables method described above. This is done in [54] to obtain a desired drain-source voltage slew-rate under varying temperature, load current, and dc-bus voltage. A different look-up table is used for each switching stage. Stage-detection can also be combined with iterative control, for instance in [41] the gate currents for each switching stage are independently controlled iteratively, the stages being detected by thresholds in gate-emitter voltage and collector current.

2.3 Relation of this thesis to existing AGD work

This thesis explores the use of AGD to dynamically adjust the trade-off between energy loss and peak transient voltage when switching. It builds upon the work of Rogers and Murmann by using the same gate driver hardware, and developing the iterative control method presented in [63]. As outlined above, the iterative method allows the switching energy loss to be directly measured and used as a control objective, rather than using an indirect indicator of switching loss such as voltage or current slew-rates. In this sense the approach taken is similar to that in [68, 69], however in this work the switches' rated maximum voltage is treated as a constraint that must not be violated, rather than a variable to be minimised

as part of an objective function. Therefore unlike in previous work, the approach does not penalize switching behaviour with peak voltages that are close to, but still below, the voltage limit. Indeed, from the point of view of minimising losses, it is desirable to operate with peak voltage approaching the switches' rated limit, given the inherent trade-off between the switching energy loss and peak transient voltage.

Furthermore, this thesis extends the existing work on the trade-off between switching loss and peak voltage, by considering how to obtain a practical benefit from managing this trade-off. The prior literature makes it clear that peak voltages can be reduced if switching loss increases, and vice-versa, however the use-cases for this are not fully developed. For instance, should one use AGD to reduce peak transient voltages so that a converter can operate at higher voltages, for a given device rating? This particular question is the subject of Chapter 4.

3

Managing semiconductor voltage stress using the gate drive

This chapter proposes a simple model of bridge-leg switching, including diode snappy reverse-recovery. Closed-form expressions are obtained which relate the switching loss to the worst-case peak transient voltage. Experimental measurements confirm the model's prediction that reverse-recovery behaviour of the diode is the cause of the highest peak transient voltages when switching. An active gate drive which can modify the switching behaviour [63] is used to experimentally investigate the trade-off between peak transient voltage and switching loss as a function of the gate drive input. Three AGD modes are compared. The simplest AGD mode is able to reduce the peak transient voltages occurring in the circuit, but at the expense of increased switching energy loss, while the most sophisticated AGD mode obtains the same peak voltage reduction with a smaller increase in switching energy loss. This chapter is largely based on the author's publication [84].

3.1 Modelling peak transient voltage and switching energy loss

Chapter 1 introduced the basic theory describing the switching behaviour of the bridge-leg. This theory is extended here to obtain a relationship between the

peak transient voltage across the semiconductor switches and the energy dissipated during the switching transition. The model is based on the linear rise/fall of the commutating current and switched-node voltage. Both the peak transient voltage and switching energy loss are expressed in terms of the rates-of-change of current/voltage, so that the potential for managing the trade-off between these two quantities by altering the rates-of-change can be evaluated. The bridge-leg modelled is that shown in Fig. 1.7, where the active switch is labelled S1 and the synchronous switch is labelled S2.

3.1.1 Active switch turn-on

When the active switch S1 turns ON, the reverse-recovery behaviour of the freewheeling diode (S2) has a major influence on the peak transient voltage. The 'snappy' recovery of S2's diode, as described in Section 1.9, is modelled here, because under this condition the peak voltage can be approximated by a simple closed-form expression. Snappy recovery also leads to higher peak transient voltages than soft recovery, making it the worst case to be modelled.

Based on the background in Section 1.9, the switching transient occurs in two distinct phases: Phase I, when the current commutates and the stored charge is removed from S2's (the synchronous device's) diode; and Phase II, when S2's diode becomes reverse-biased and the voltage across it rises. Figure 3.1a shows the current and voltage of S2 through both phases of the switching transient. In Phase I, the rate of current commutation is determined by the speed that S1's channel opens (which is itself influenced by both the gate driver and the characteristics of the power device). Throughout this phase the diode remains forward-biased. Excess stored charge is swept out of the device when the diode current becomes negative.

Phase II begins at the point when all excess charge has been removed or recombined, such that the junction can enter reverse-bias state. In this phase the depletion capacitance of the diode, C_{oss2}, in series with the parasitic power loop inductance L_p and the loop resistance R, forms a series LCR oscillator (Fig. 3.1b). If the values of L_p, R, and C_{oss2} are constant, then the LCR oscillator is a linear

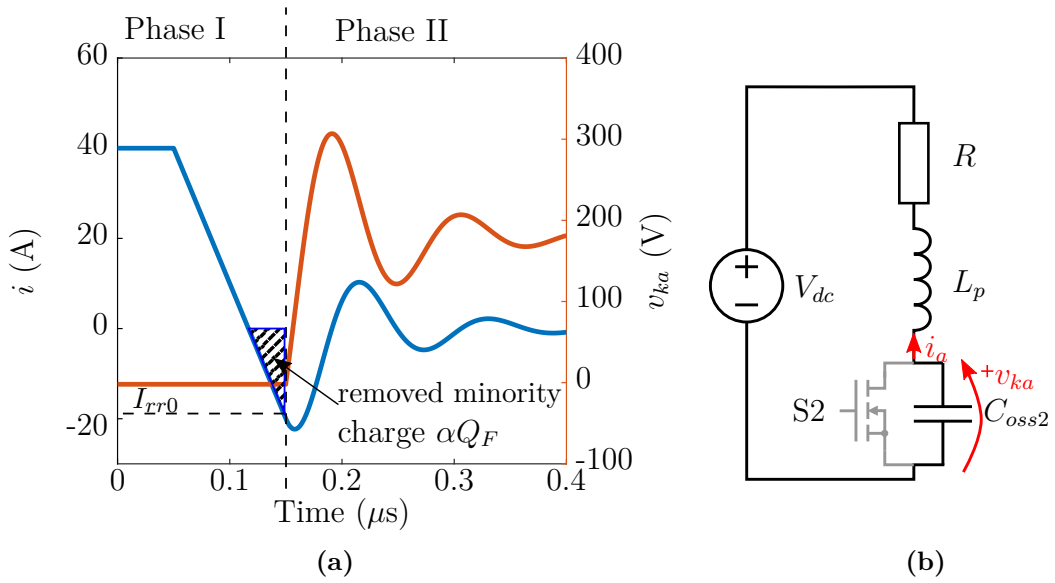


Figure 3.1: (a) Snappy turn-OFF of the synchronous device's body diode occurs in two phases: first all stored charge is removed in Phase I, then the depletion capacitance of the device forms an LCR circuit in Phase II. (b) The equivalent LCR circuit for Phase II (a temporary subset of the full circuit shown in Fig. 1.7).

time-invariant system, and the voltage $v_{ka}(t)$ and current $i_a(t)$ can be expressed in terms of their initial state at the onset of Phase II.

In reality, the diode output capacitance C_{oss2} changes greatly during the switching transient as the bias voltage changes. The assumption of a constant capacitance is a fundamental limitation of this model. Likewise, in reality the value of the damping resistance R changes during Phase II as the channel of S1 continues to open, and could be frequency-dependent due to the skin-effect [85]. The ringing in the later stages of Phase II will be particularly influenced by the damping resistance; however, since the feature of interest is the peak of v_{ka}, an accurate model of the later stages of Phase II is unnecessary. In general, this simple model is useful for identifying trends but not for making accurate quantitative predictions.

By definition the diode voltage v_{ka} is zero at the onset of Phase II. The reverse-current at the start of Phase II, I_{rr0}, is expressed in terms of the diode stored charge and the commutating current rate-of-change $\frac{\mathrm{d}i}{\mathrm{d}t}$. The diode has some stored charge Q_F from forward conduction before the switching transient. Denoting the charge swept out by the reverse current as αQ_F (the charge that recombines inside the

diode is $(1-\alpha)Q_F$ for $0 \leq \alpha \leq 1$), the integral of the negative current equals the removed charge (the hatched area in Fig. 3.1a), giving [16]

$$I_{rr0} = \sqrt{2\frac{\mathrm{d}i}{\mathrm{d}t}\alpha Q_F}\,. \tag{3.1}$$

With this initial current, an expression for the voltage v_{ka} across the diode capacitance in Fig. 3.1a follows from this

$$\begin{aligned} v_{ka}(t) = e^{-\sigma t}\Big[&\left(I_{rr0}L_p\omega + \frac{R\sigma I_{rr0}}{2\omega} - \frac{V_{dc}\sigma}{\omega}\right)\sin(\omega t) \\ &- \left(I_{rr0}L_p\sigma - \frac{RI_{rr0}}{2} + V_{dc}\right)\cos(\omega t)\Big] \\ &+ I_{rr0}L_p\sigma - \frac{RI_{rr0}}{2} + V_{dc}\,, \end{aligned} \tag{3.2}$$

where

$$\sigma = \frac{R}{2L_p} \tag{3.3a}$$

$$\omega = \sqrt{\frac{1}{L_pC_{oss2}} - \sigma^2}\,. \tag{3.3b}$$

The maximum voltage across S2 occurs at time t^*.

$$\max(v_{ka}(t)) = v_{ka}(t^*)\,, \tag{3.4}$$

where

$$t^* = \frac{1}{\omega}\left(\arctan\left(\frac{1}{\omega L_p}\left(\frac{V_{dc}}{I_{rr0}} - \frac{R}{2}\right)\right) + \frac{\pi}{2}\right)\,. \tag{3.5}$$

This means that for a given rate-of-change of current, stored charge, and circuit parameters, the worst-case peak transient voltage across the diode can be directly estimated.

For this simple model, all switching loss occurs in the active switch S1. No energy is dissipated in the diode since it has negligible voltage drop across it throughout Phase I and behaves as an ideal capacitor in Phase II. The Phase I energy loss E_{on1} is as given in Section 1.7, but with an additional loss component from the diode reverse recovery charge αQ_F which the switch must conduct while blocking voltage.

$$E_{\mathrm{on1}} = \left(\frac{I_L^2}{2\frac{\mathrm{d}i}{\mathrm{d}t}} + \alpha Q_F\right)\left(V_{dc} - L_p\frac{\mathrm{d}i}{\mathrm{d}t}\right) \tag{3.6}$$

The loss during the ringing of Phase II is determined using the principle of energy conservation. Taking the difference between the energy stored in the bridge-leg at the start (E_a) and at the end (E_b) of Phase II, and adding the input energy (E_c) gives the energy dissipated during Phase II (E_{on2})

$$E_{\text{on2}} = E_a - E_b + E_c \,. \tag{3.7}$$

At the start of Phase II, the bridge-leg energy is stored in the parasitic inductance L_p and the output capacitance of S1 ($E_a = \frac{1}{2}L_p I_{rr0}^2 + \frac{1}{2}C_{oss1}V_{dc}^2$). At the end of Phase II when steady-state is reached, energy is stored in the diode capacitance C_{oss2} ($E_b = \frac{1}{2}C_{oss2}V_{dc}^2$). Charge amounting to $C_{oss2}V_{dc}$ has been delivered from the dc bus, with an energy of $E_c = C_{oss2}V_{dc}^2$. Inserting these quantities into (3.7) gives the Phase II loss as

$$E_{\text{on2}} = \frac{1}{2}L_p I_{rr0}^2 + \frac{1}{2}\left(C_{oss1} + C_{oss2}\right)V_{dc}^2 \,. \tag{3.8}$$

The total switching loss when the active switch S1 turns ON is

$$E_{\text{on}} = E_{\text{on1}} + E_{\text{on2}} \,. \tag{3.9}$$

3.1.2 Active switch turn-off

The peak transient voltage across S1 as it turns OFF is a function of $\frac{\mathrm{d}i}{\mathrm{d}t}$ as given by (1.18). Taking the expression for turn-OFF switching loss (1.21) and expressing the voltage rise duration τ_{vr} and current fall duration τ_{cf} in terms of the voltage and current rates-of-change gives

$$E_{\text{off}} = \frac{V_{dc}^2 I_L}{2\frac{\mathrm{d}v}{\mathrm{d}t}} + \frac{V_{dc}I_L^2}{2\frac{\mathrm{d}i}{\mathrm{d}t}} \,. \tag{3.10}$$

Accounting for the effect of parasitic inductance (the energy stored in the power loop parasitic inductance is lost), gives the calculated energy loss of S1 turn-OFF as

$$E_{\text{off}} = \frac{V_{dc}^2 I_L}{2\frac{\mathrm{d}v}{\mathrm{d}t}} + \frac{V_{dc}I_L^2}{2\frac{\mathrm{d}i}{\mathrm{d}t}} + \frac{1}{2}L_p I_L^2 \,. \tag{3.11}$$

Parameter	Value
V_{dc}	180 V
I_L	40 A
L_p	160 nH
C_{oss2}	2 nF
αQ_F	3 µC

Table 3.1: Parameters used for model example

3.1.3 Model predictions over range of $\frac{\mathrm{d}i}{\mathrm{d}t}$

The model-predicted switching energy losses and peak transient voltages are shown in Fig. 3.2 for various rates-of-change of current. The model parameters (listed in Table 3.1) approximately correspond to the experimental setup discussed later in this chapter.

For turn-ON of S1, the peak transient voltage increases while the total turn-ON switching loss decreases for increasing $\frac{\mathrm{d}i}{\mathrm{d}t}$ (Fig. 3.2a). The loss component from the phase when the switch current rises (E_{on1}) decreases with increasing $\frac{\mathrm{d}i}{\mathrm{d}t}$ as the duration of the phase is shortened and more voltage is dropped across the parasitic inductance instead of across the switch. The loss component from the ringing phase (E_{on2}) increases with $\frac{\mathrm{d}i}{\mathrm{d}t}$ as more energy is stored in the parasitic inductance at the onset of the ringing phase. The predicted peak transient voltages increase almost linearly with $\frac{\mathrm{d}i}{\mathrm{d}t}$ and are extremely high for large $\frac{\mathrm{d}i}{\mathrm{d}t}$ (>300% of the dc bus).

The diode current and voltage waveforms are plotted in Fig. 3.3 for S1 turn-ON under two rates of current commutation: 200 A/µs (Fig. 3.3a) and 600 A/µs (Fig. 3.3b). The impact of the current commutation rate on the peak reverse current and subsequent ringing is clear. The period of Phase II up to the first peak in v_{ka} is highlighted in red: beyond this point the model is not considered accurate due to the damping resistance, discussed above.

The switching loss and peak voltage for S1 turn-OFF (Fig. 3.2b) follow the same trends for changing $\frac{\mathrm{d}i}{\mathrm{d}t}$ as turn-ON. The predicted peak transient voltage during turn-OFF is much lower than turn-ON, indicating that the turn-ON transient is the critical event (in terms of device voltage stress) when there is snappy reverse-recovery of the diode.

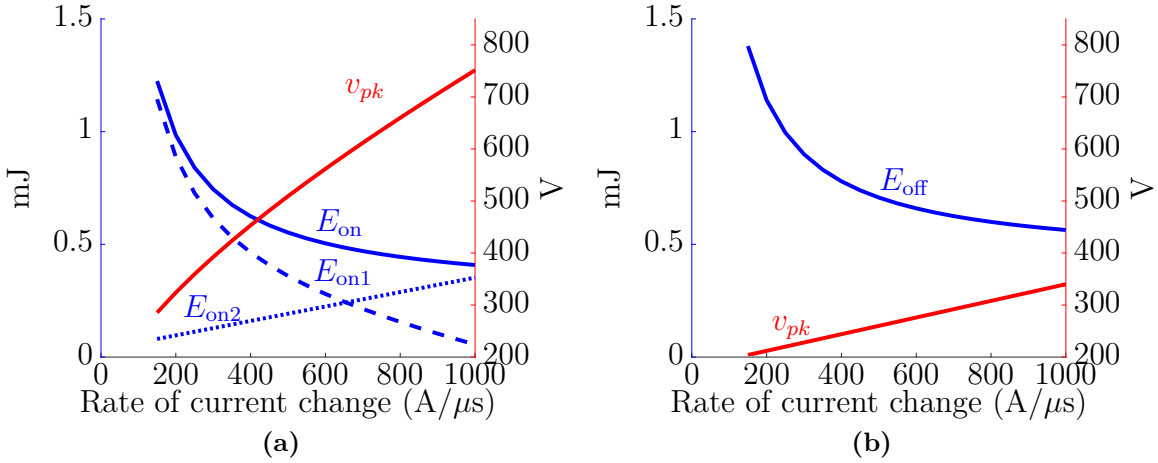


Figure 3.2: Energy loss and peak transient voltage as a function of $\frac{\mathrm{d}i}{\mathrm{d}t}$ for (a) S1 turn-ON and (b) S1 turn-OFF (plotted for $\frac{\mathrm{d}v}{\mathrm{d}t}$ =2 V/ns). Snappy diode recovery in (a) creates the highest peak voltages. The circuit diagram pertaining to this is shown in Fig. 3.1b.

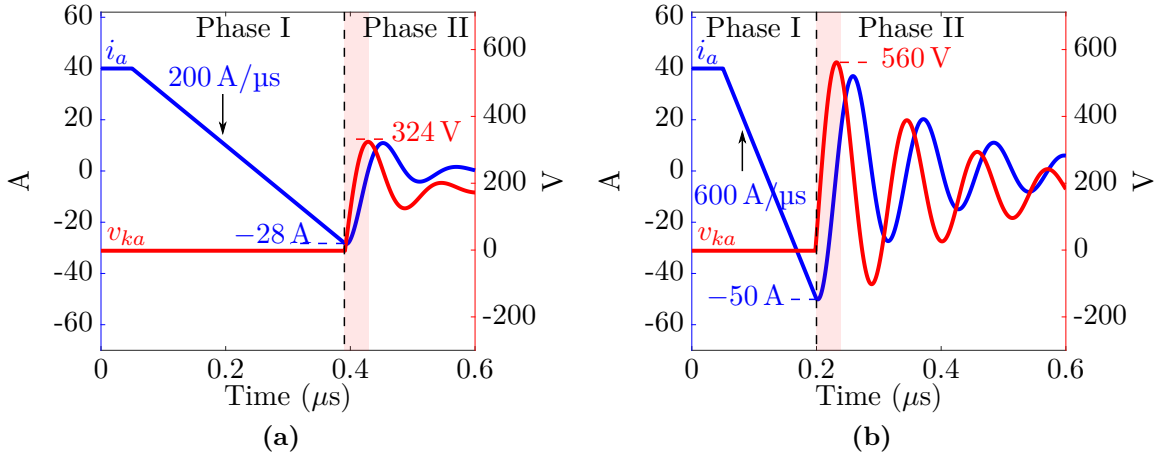


Figure 3.3: Diode cathode-anode voltage v_{ka} and current i_a waveforms from the model for (a) 200 A/µs current commutation-rate, and (b) 600 A/µs current commutation-rate. The red window highlights the region of Phase II where the model is relevant (up to the first peak in v_{ka}). The circuit diagram pertaining to this is shown in Fig. 3.1b.

The implication of snappy diode reverse-recovery is clear: to avoid high voltage stress across the freewheeling diode / synchronous switch (S2), the load current must commutate slowly at the expense of increased switching loss.

3.2 Experimental investigation of peak voltage and switching energy loss in a bridge-leg with active gate driving

While the model provides insight into the causes of the trade-off between switching energy loss and peak voltage stress, the strong assumptions that underpin its simplicity (in particular the assumption of 'snappy' diode recovery, and constant R and C_{oss2} in Phase II of turn-ON) mean that it should not be expected to provide accurate predictions of practical circuit behaviour.

An experimental approach, outlined in this section, is used to investigate more realistic values of the peak transient voltage and switching energy loss.

3.2.1 The power circuit

The switching behaviour of the bridge-leg of Fig. 3.4 is measured. The bridge-leg hardware is taken from [63]. This circuit is equivalent to the buck converter considered previously (e.g. Fig. 1.8), with the difference that the load is connected on the 'high side' - i.e. between the positive rail of the dc bus and the mid-point of the bridge-leg, rather than between the negative rail of the dc bus and the mid-point of the bridge-leg. This means that the bottom switch becomes the 'active' switch that is gated on and off, while the top switch becomes the synchronous switch or - as in this case - simply the antiparallel diode. For consistency with the previous discussion, we label the active switch S1 and the synchronous switch S2. This configuration with the load on the high-side has the advantage of not requiring a high-side (not ground-referenced) gate drive: the gate and emitter of S2 are shorted together so that IGBT S2 is held OFF.

The half-bridge power module Fuji 2MBI300U4N-120-50 contains the upper and lower silicon IGBTs and antiparallel silicon *pin* diodes. Collector-emitter voltage v_{ce} is measured for both switches using two 100:1 25 MHz differential probes (Testec TT-SI9001) and collector current i_c is measured using two 100 MHz clip-on current probes (Keysight N2783A). Gate-emitter voltage v_{ge} of S1 is measured with a 10:1

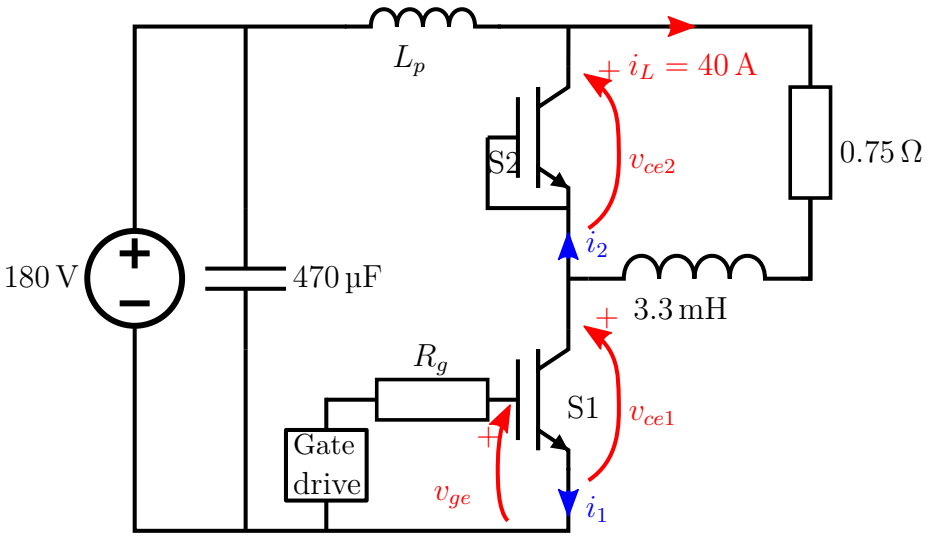


Figure 3.4: The bridge-leg used for experimental measurements of switching behaviour.

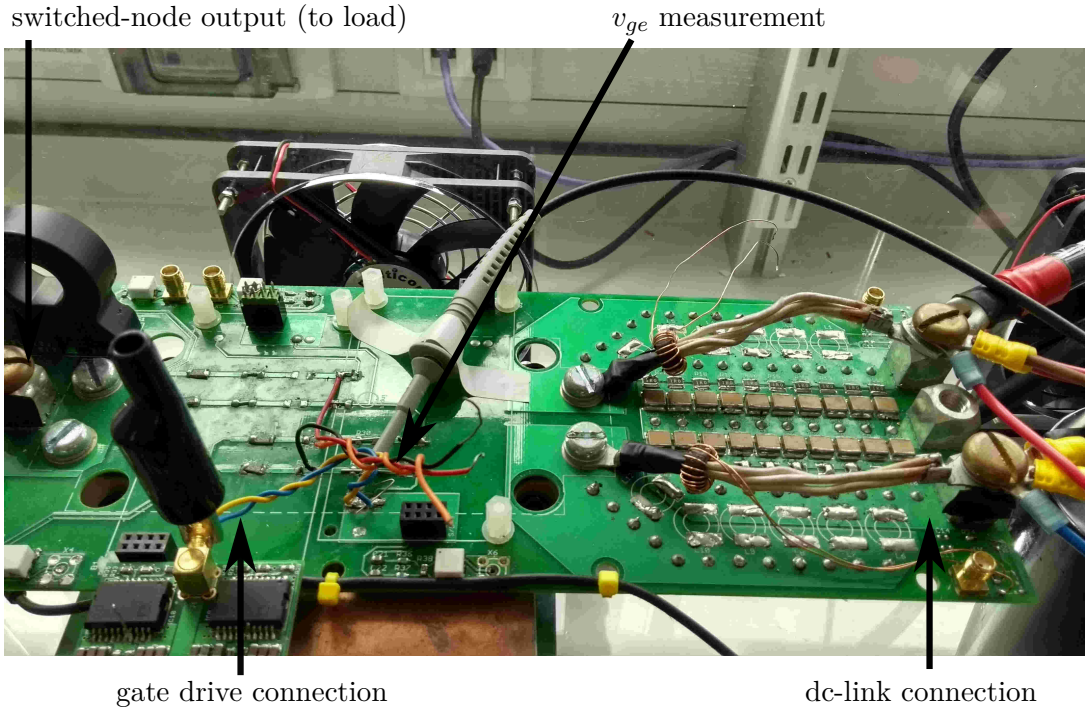


Figure 3.5: The half-bridge power board [63]. Power module 2MBI300U4N-120-50 is on board underside.

350 MHz passive probe. All five signals are sampled at 300 MSPS by oscilloscope (250 MHz Picoscope 6402C for v_{ce} and i_c and 200 MHz Keysight DSOX2024A for v_{ge}).

The IGBT S1 is switched at 20 kHz with a duty cycle chosen to set the load current at 40 A. A photograph of the bridge-leg power board is shown in Fig. 3.5.

3.2.2 Switching energy loss measurement

The switching energy loss is obtained from the current and voltage waveforms using (1.19). The integration is performed numerically on the sample points using a trapezoidal integration scheme. Errors in the current and voltage measurements will propagate through to the switching energy loss result. Here the effect of the finite oscilloscope sample-rate and quantisation are assessed by comparing the energy loss calculated from exact reference waveforms to that calculated from distorted waveforms representing oscilloscope data.

Voltage and current waveforms produced by the model (the ringing waveforms of Phase II in Fig. 3.3b) are used in (1.19) to obtain the reference switching energy loss. Since the waveforms $v(t)$ and $i(t)$ are analytically defined, the integration of the instantaneous power loss can be calculated exactly:

$$E_{\text{sw,exact}} = \int_{t_1}^{t_2} v(t)i(t)\,\mathrm{d}t\,, \tag{3.12a}$$

$$= \int_{t_1}^{t_2} p(t)\,\mathrm{d}t\,, \tag{3.12b}$$

$$= 29.67\,\mu\mathrm{J}\,,$$

where t_1 and t_2 are the start and end times of the waveform segments and $p(t)$ is the exact instantaneous power loss.

The voltage and current waveforms are quantised to emulate the 8-bit digitisation that takes place in the oscilloscope. The vertical resolutions for the voltage and current waveforms are

$$\Delta v = \frac{1500\,\mathrm{V}}{2^8} = 5.86\,\mathrm{V}\,, \tag{3.13a}$$

$$\Delta i = \frac{150\,\mathrm{A}}{2^8} = 0.586\,\mathrm{A}\,, \tag{3.13b}$$

where the oscilloscope full-range voltage/current is taken to be approximately four times the waveform peak.

The quantised voltage and current waveforms are

$$v^*(t) = \left\lfloor \frac{v(t)}{\Delta v} + \frac{1}{2} \right\rfloor \Delta v \,, \tag{3.14a}$$

$$i^*(t) = \left\lfloor \frac{i(t)}{\Delta i} + \frac{1}{2} \right\rfloor \Delta i \,, \tag{3.14b}$$

where $\lfloor\,\rfloor$ is the floor function.

The quantised waveforms are sampled in time at the oscilloscope sampling frequency f_{samp}:

$$v_k^* = v^* \left(\frac{k}{f_{\text{samp}}} \right) , \tag{3.15a}$$

$$i_k^* = i^* \left(\frac{k}{f_{\text{samp}}} \right) , \tag{3.15b}$$

$$\text{where} \quad k \in \{1, 2 \dots\} \,.$$

The resulting quantised, sampled power loss p_k^* is

$$p_k^* = v_k^* i_k^* \,, \tag{3.16}$$

and the integration (1.19) becomes the discrete sum to give the 'measured' switching energy loss as

$$E_{\text{sw,meas}} = \frac{1}{f_{\text{samp}}} \sum_k p_k^* \,. \tag{3.17}$$

Fig. 3.6a shows the exact current and voltage waveforms $i(t)$ and $v(t)$ (solid lines) and the quantised and sampled waveforms i_k^* and v_k^* (dot markers). The waveforms are well resolved in time and voltage/current, although the quantisation steps are visible. Fig. 3.6b shows the corresponding waveforms for the instantaneous power losses $p(t)$ (solid line) and p_k^* (marker dots), and the exact (solid line) and trapezoidal-integrated (dot markers) switching energy losses. Fig. 3.6c plots the difference between the exact and the trapezoidal-integrated energies in absolute and percentage errors. Despite the sampled-quantised power p_k^* appearing to closely match the exact power $p(t)$, the difference in the integration products varies with a peak relative difference of ∼1.8 %. The ringing waveforms analysed here are particularly prone to high relative error because the energy loss overall is small. For

higher losses we expect the error in the measured switching energy loss to be of the order of 1 %. The probes are de-skewed (relative delay between probes compensated for) and any zero-offset is removed before the experiment. The same probes are used for all tests, therefore gain error from the probes will affect all measurements equally.

3.2.3 The gate drive

Switch S1 is driven by an AGD, which is used to vary the switching behaviour of the bridge-leg. The gate drive is composed of two systems: the 'Gate Waveform Constructor' and the 'Signal Generator'.

The Signal Generator presented in [63] is used in this experiment (Fig. 3.7). It consists of an FPGA, a DAC, and an analogue amplifier. It produces a voltage signal v_{gg} based on a sequence of data-points stored in the FPGA RAM. This voltage is applied to the gate of S1. When S1 is held OFF, v_{gg} equals V_{gg-}, the hold-off gate voltage level. When S1 is held ON, v_{gg} equals V_{gg+}, the hold-on gate voltage level.

During the switching transition period, v_{gg} is determined by the data points stored in RAM. The FPGA clocks the sequence of data points out from the RAM into the 14-bit DAC. The DAC converts the digital data to an analogue signal which is level-shifted, amplified, and buffered up to a maximum current of 4 A. This signal is applied to the power device gate through a resistance R_g and a 50 mm twisted-pair cable. A split supply of $V_{ge}^{+} = 22\,\mathrm{V}$ and $V_{ge}^{-} = -13\,\mathrm{V}$ (referenced to the IGBT emitter potential) powers the analogue circuitry, giving the gate-emitter voltage of S1, v_{ge}, a potential range of $-11\,\mathrm{V}$ to $20\,\mathrm{V}$.

The Signal Generator provides great flexibility in choosing the gate signal of S1 (since there are 2^{14M} possible combinations of M input points to the 14-bit DAC). To reduce this large number of possible gate drive signals, a parametrization is chosen which maps a small number of physically meaningful variables to the sequence of M 14-bit numbers that go to the DAC. This parametrization is the function of the Gate Waveform Constructor.

The Gate Waveform Constructor creates the gate reference voltage waveform $v_{g,\mathrm{ref}}$ and passes it to the Signal Generator. The Gate Waveform Constructor runs

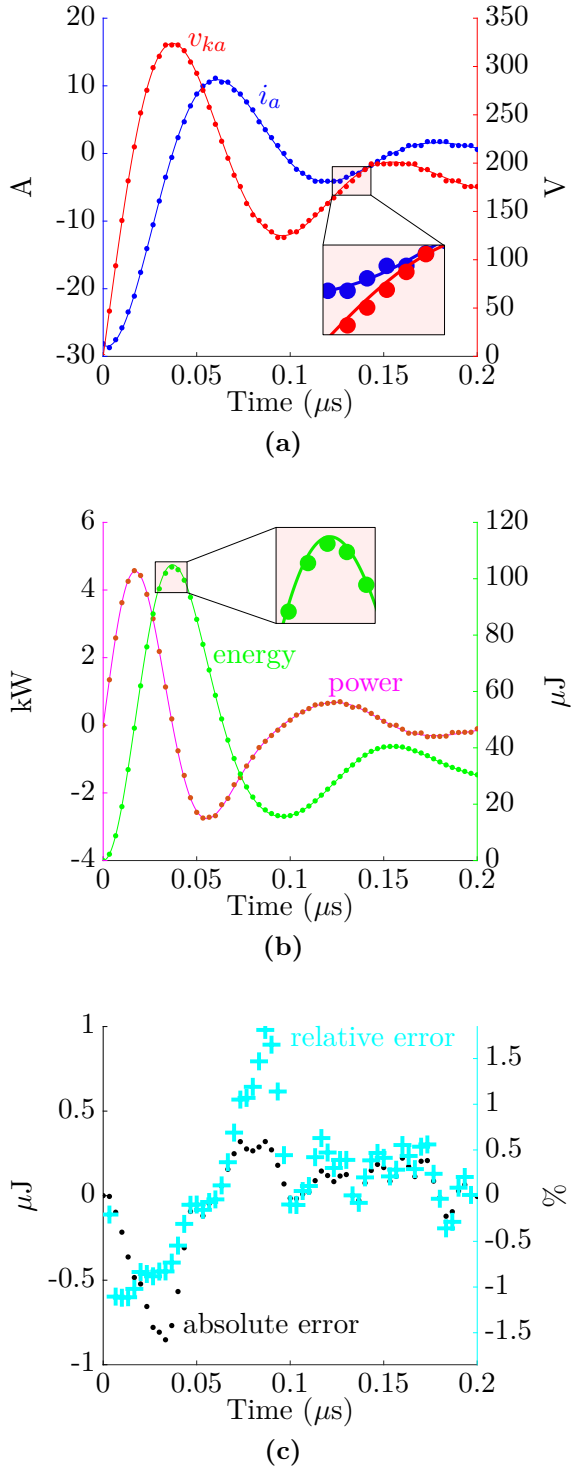


Figure 3.6: The effect of sampling and quantising the voltage and current waveforms on the measured switching energy loss. (a) Exact waveforms (solid lines) and sampled-quantised data-points (markers) of voltage and current. (b) Exact (solid line) and sampled-quantised (markers) power loss and switching energy loss. (c) Absolute and relative error between the exact loss and the sampled-quantised loss.

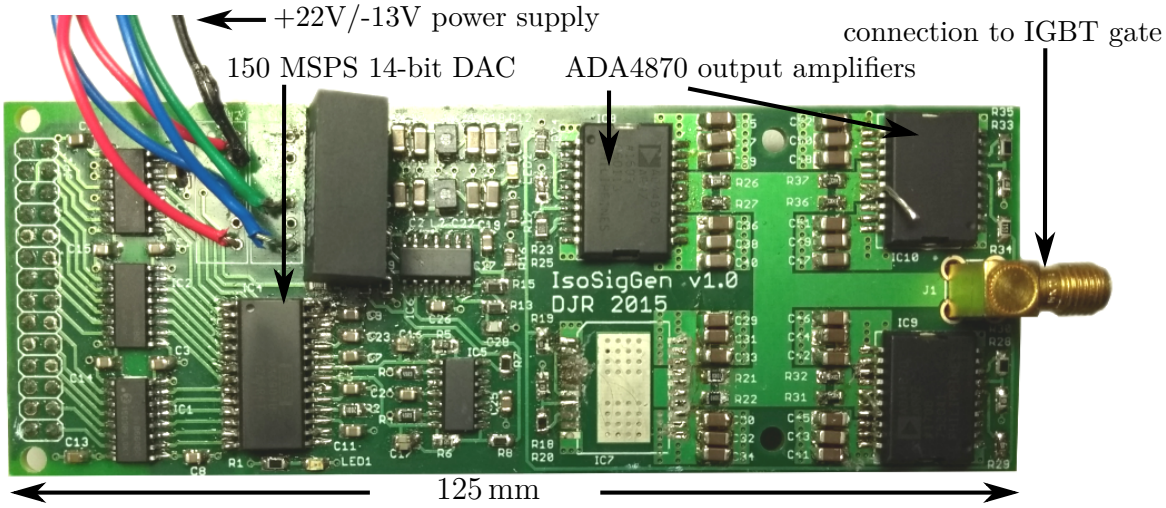


Figure 3.7: Gate drive printed circuit board providing digital to analogue conversion and amplification. (This is developed in [63] - the design and build of this board is not the author's work.)

in MATLAB on a desktop PC, and operates in either 'fast switching' mode or 'AGD mode' (active gate drive mode). For 'fast switching', the reference $v_{g,\text{ref}}$ is simply a step from V_{gg-} to V_{gg+} for turn-ON or from V_{gg+} to V_{gg-} for turn-OFF. For 'AGD mode', $v_{g,\text{ref}}$ is parametrised based on an input vector $\mathbf{x}$ (as illustrated in Fig. 3.8).

To make the IGBT sensitive to the upcoming AGD voltage profile, the gate is first brought to a pre-charge level $V_{\text{pre}}^{\text{on/off}}$ which is close to the threshold voltage. Then, there is an 'active period', the duration of which is given by the first element in the input vector, i.e. x_1. This period is split into N sections of equal duration, where the voltages at the $N-1$ points between the sections are given by the remaining elements in $\mathbf{x}$, i.e. $x_2, x_3 \ldots$. The gate reference voltage between these points is found by linear interpolation. The length N of the input vector $\mathbf{x}$ determines the number of piecewise-linear segments that constitute the voltage reference. The AGD with $N \in \{1, 2, 3\}$ is investigated, and these three cases are given the descriptive names listed in Table 3.2. When $N = 1$, the gate drive is called the *Variable-Ramp active gate drive (VR-AGD)* because the degree of freedom is in the gradient of the gate-voltage ramp. The $N = 2$ case is called the *Double-Ramp active gate drive (DR-AGD)* since the gate-voltage ramp is split into two piecewise-linear segments. The $N = 3$ case is called the *Push-Pull active gate drive (PP-AGD)* because it

Table 3.2: The three AGD cases which are investigated.

N	Name	
1	Variable-ramp AGD	(VR-AGD)
2	Double-ramp AGD	(DR-AGD)
3	Push-pull AGD	(PP-AGD)

can both inject and remove charge from the gate during the switching transient. More elements in $\mathbf{x}$ potentially improve switching performance by allowing a greater range of gate waveforms to be created, but also increase the dimension of the space to be experimentally characterised.

The shape of the reference waveforms is informed by the previous work using this gate drive, [63]. In particular, the idea of the pre-charge is presented by Rogers and Murmann, and early experiments I performed verified that this indeed increases the effectiveness of the subsequent active period. This appears to be due to the large amount of gate charge that is required to bring the voltage of the gate to the threshold level, relative to the charge required to modify the switching behaviour during the active period. The division of the voltage reference into piecewise-linear segments is also proposed in [63]. The piecewise-linear formulation of the reference voltage is repeated here as it combines conceptual simplicity with the flexibility to synthesise detailed profiles. Note that in [63] the number of linear segments was fixed to two for turn-ON and three for turn-OFF, whereas here the effect of different numbers of segments is investigated. Furthermore, the durations of all the linear segments of a given reference waveform are equal in this work, as opposed to [63] where the duration of one segment was varied but the others were held constant. I found during experiments that varying the duration of all segments together allowed for a greater range of switching behaviour, because the duration of the entire reference waveform could modified without being constrained by the fixed duration of any one segment.

Figs. 3.8a and 3.8b show example gate reference voltage profiles for turn-ON with the Variable-Ramp AGD ($N = 1$) and Push-Pull AGD ($N = 3$), respectively. Figs. 3.8c and 3.8d show corresponding examples for turn-OFF.

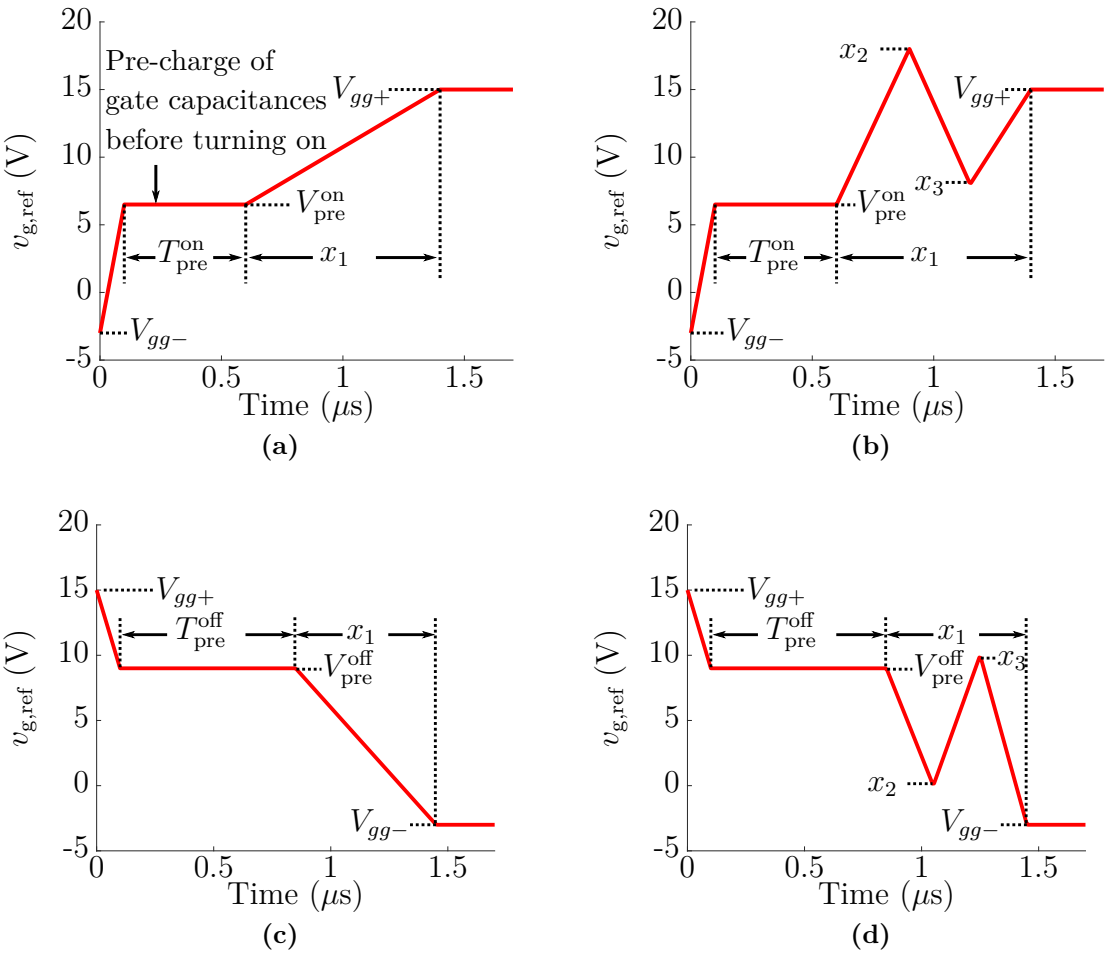


Figure 3.8: Examples of AGD reference waveforms $v_{g,\text{ref}}$, illustrating the function of each element of $\mathbf{x}$ for (a) turn-ON with VR-AGD, (b) turn-ON with PP-AGD, (c) turn-OFF with VR-AGD, and (d) turn-OFF with PP-AGD.

At the end of the active period, the gate is held at some high voltage V_{gg+} (for turn-ON) or some low voltage V_{gg-} (for turn-OFF) to keep the IGBT fully on or off. The values of the parameters which are fixed (those not in the input $\mathbf{x}$) are listed in Table 3.3. The reference voltage $v_{g,ref}$ is downsampled to 256 points and these points are sent from the host PC to the signal generator RAM over USB. The points are clocked into the signal generator DAC at a rate of 100 MSPS, such that the resulting signal from the DAC has a duration of

$$\frac{256}{100 \cdot 10^6} = 2.56\,\mu\text{s}\,. \tag{3.18}$$

Table 3.3: Values of fixed gate waveform parameters

Name	Value
$T_{\text{pre}}^{\text{on}}$	0.50 µs
$T_{\text{pre}}^{\text{off}}$	0.75 µs
$V_{\text{pre}}^{\text{on}}$	6.0 V
$V_{\text{pre}}^{\text{off}}$	9.0 V
V_{gg+}	15.0 V
V_{gg-}	−3.0 V
R_g	1.25 Ω

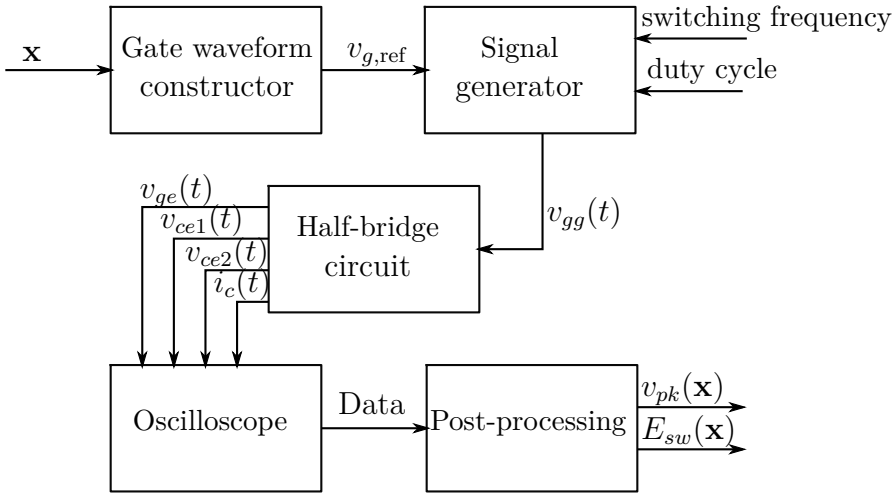


Figure 3.9: Block diagram illustrating experimental process from gate waveform parameters $\mathbf{x}$ to switching energy loss E_{sw} and peak transient voltage v_{pk}.

3.2.4 Procedure

The experimental procedure is summarised in Fig. 3.9. A mesh of all feasible $\mathbf{x}$ is generated, and each $\mathbf{x}$ is applied to the IGBT bridge-leg in turn using the gate driver. The switching voltage and current waveforms are captured by oscilloscope (as described in Section 3.2.1), and the peak voltage and switching energy are extracted from the waveforms in a post-processing step. The peak transient voltage and switching energy loss, expressed as a function of $\mathbf{x}$ (i.e. $v_{pk}(\mathbf{x})$ and $E_{sw}(\mathbf{x})$), are graphically displayed over a range of $\mathbf{x}$. At each $\mathbf{x}$ the mean of several E_{sw} and v_{pk} measurements is taken to reduce measurement noise.

This method is repeated for $N \in \{1, 2, 3\}$ (the three modes of AGD listed in

Table 3.2). Results from each AGD are discussed in turn. To provide a numerical comparison between the AGD cases, the upper limit on the peak voltage is taken as 260 V, and the minimum attainable switching loss under this constraint is the figure of comparison. Since for turn-OFF even a step-input at the gate does not produce a peak voltage above the 260 V constraint, in practice this is only a comparison of the turn-ON behaviour of the AGDs. The performance of the AGDs as the voltage constraint is tightened is discussed in Section 3.2.11. Before the three AGDs are compared, waveforms for two switching cases (fast-switching and slow VR-AGD switching) are presented to illustrate the difference in behaviour.

3.2.5 Fast-switching behaviour

The voltage and current waveforms of S1 (Fig. 3.10a) and S2 (Fig. 3.10b) as S1 turns-ON with a voltage step input at the gate show high rates of change of voltage and current, a large reverse recovery current, and a 384 V peak transient voltage across S2. Most of the dc bus voltage is dropped across the parasitic inductance as i_1 rises, lowering the turn-ON losses of S1 to approximately 0.3 mJ. In contrast the energy dissipated in S2 is much greater than S1 (approximately 1.6 mJ), contrary to the prediction of the simple model of Section 3.1. It is apparent that stored charge is removed from diode S2 even after v_{ce2} rises - i.e. the diode reverse-recovery is not completely snappy - leading to higher energy dissipation and lower peak transient voltage than predicted by the model.

The energy to charge S2's output capacitance is

$$E_{coss2}(180\,\mathrm{V}) \approx \frac{1}{2}(2\,\mathrm{nF})(180\,\mathrm{V}^2) = 32\,\mu\mathrm{J}\,, \tag{3.19}$$

clearly dwarfed by actual reverse-recovery energy.

Turn-OFF behaviour under a step input at S1's gate is shown in Fig. 3.11. The peak transient voltage (250 V observed across S1) is lower than the turn-ON case. Switch S1 experiences a larger turn-OFF loss than S2 (2.1 mJ as opposed to 0.3 mJ) due to the overlapping voltage and current across S1. S2 initially (at 0.4 µs) *supplies* power to the load as its output capacitance discharges, however

the subsequent forward recovery power dissipation (at 0.5 µs) results in a small net dissipation of energy.

3.2.6 Slow-switching behaviour from the Variable-Ramp AGD

Waveforms resulting from a slow ramp of gate voltage delivered by the VR-AGD (Fig. 3.12 for turn-ON and Fig. 3.13 for turn-OFF) illustrate the capability of this gate drive.

The turn-ON rate of S1 current rise (Fig. 3.12a) is markedly lower than for the fast-switching case. The peak reverse recovery current is halved compared to fast-switching (−40 A compared to −80 A) and the decay of reverse current is more gentle, producing a peak transient voltage of only 210 V across S2 (Fig. 3.12b). The distribution of energy loss between S1 and S2 is also reversed, with S1 dissipating more energy than S2 during turn-ON.

The turn-OFF behaviour is almost unchanged for the step input case, except that all the waveforms are shifted in time because of the pre-charge delay period. This suggests that the ramp rate of the gate voltage has influence on turn-ON behaviour but little influence on turn-OFF behaviour. This may indicate that the turn-OFF dynamics are mainly driven by the bipolar behaviour of the IGBT and not by the rate that the MOS channel is closed.

3.2.7 Peak voltages and switching losses of the Variable-Ramp AGD

The relationship between switching loss and peak voltage when using VR-AGD is evident in Fig. 3.14a for S1 turn-ON. The shortest ramp duration that satisfies the 260 V limit is 1.26 µs, with a corresponding turn-ON switching loss of 2.56 mJ. The time domain waveforms for this turn-ON are show in Figs. 3.18a and 3.18b. No control of either switching loss or peak voltage is obtained for turn-OFF of S1 (Fig. 3.14b). The turn-OFF loss is unchanged from the step-input case at approximately 2.30 mJ. The total switching loss for the 260 V limit is $E_{sw} = 4.86$ mJ.

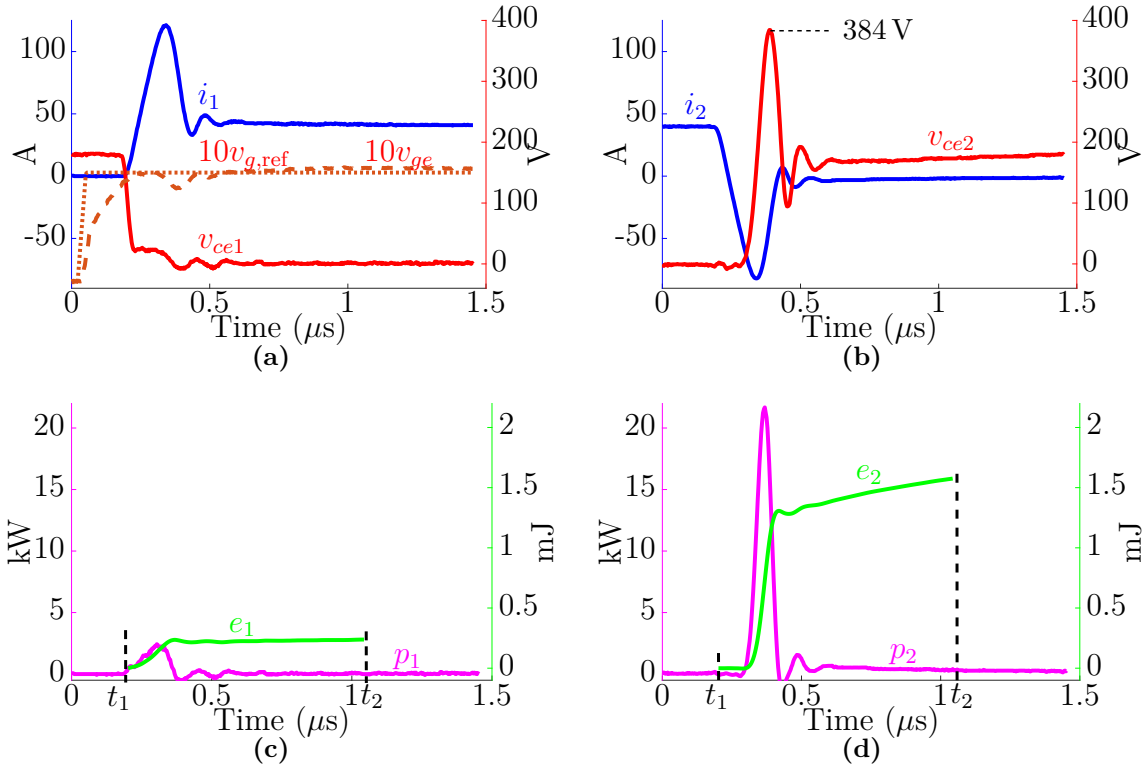


Figure 3.10: Fast-switching waveforms for turn-ON. (a,c) S1, (b,d) S2.

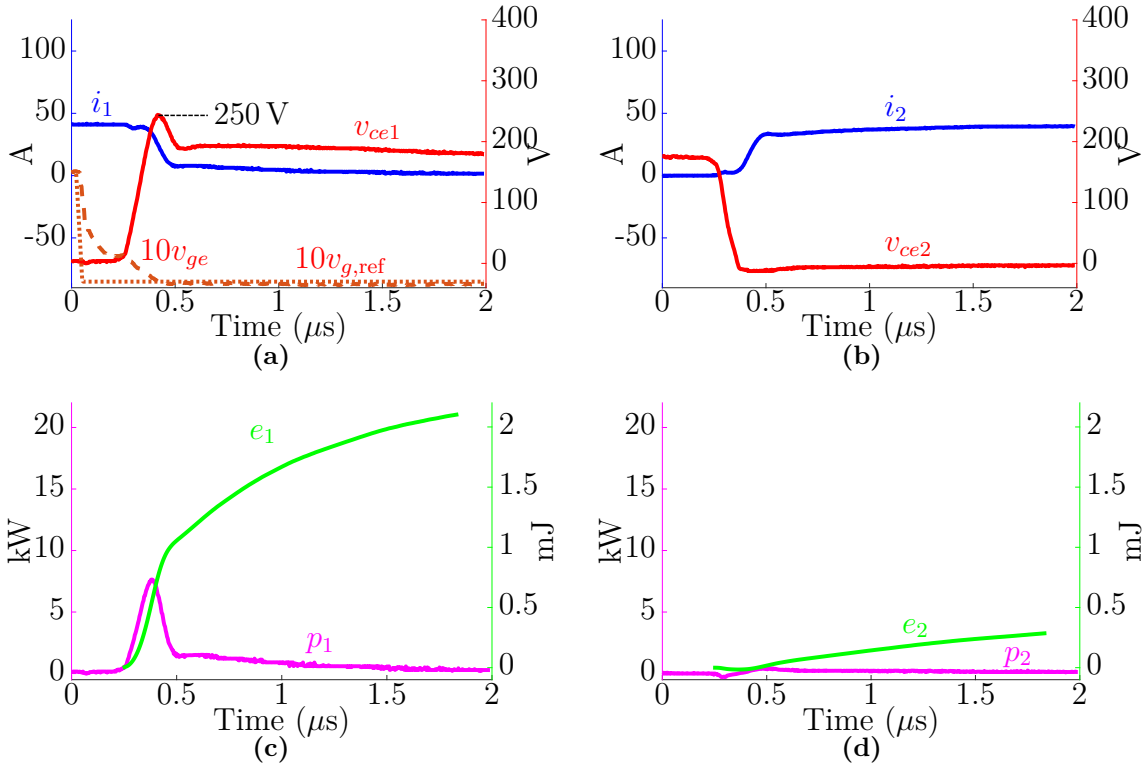


Figure 3.11: Fast-switching waveforms for turn-OFF. (a,c) S1, (b,d) S2.

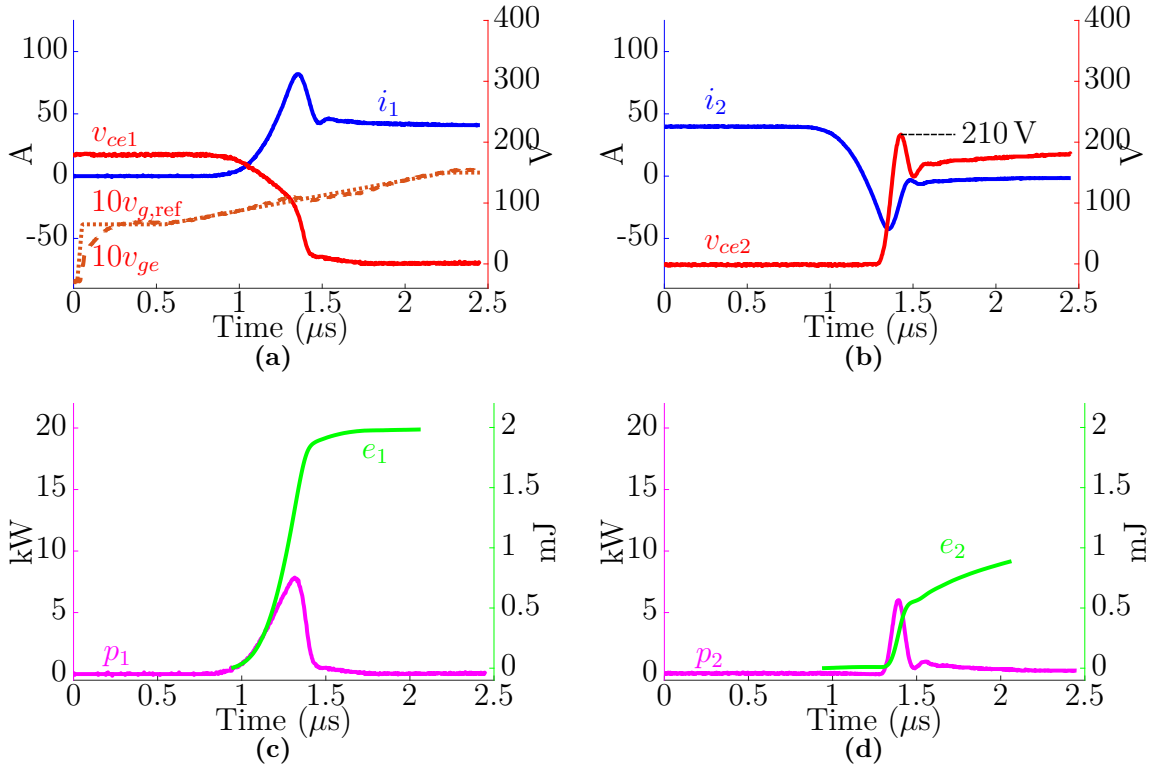


Figure 3.12: VR-AGD slow switching waveforms for turn-ON. (a,c) S1, (b,d) S2.

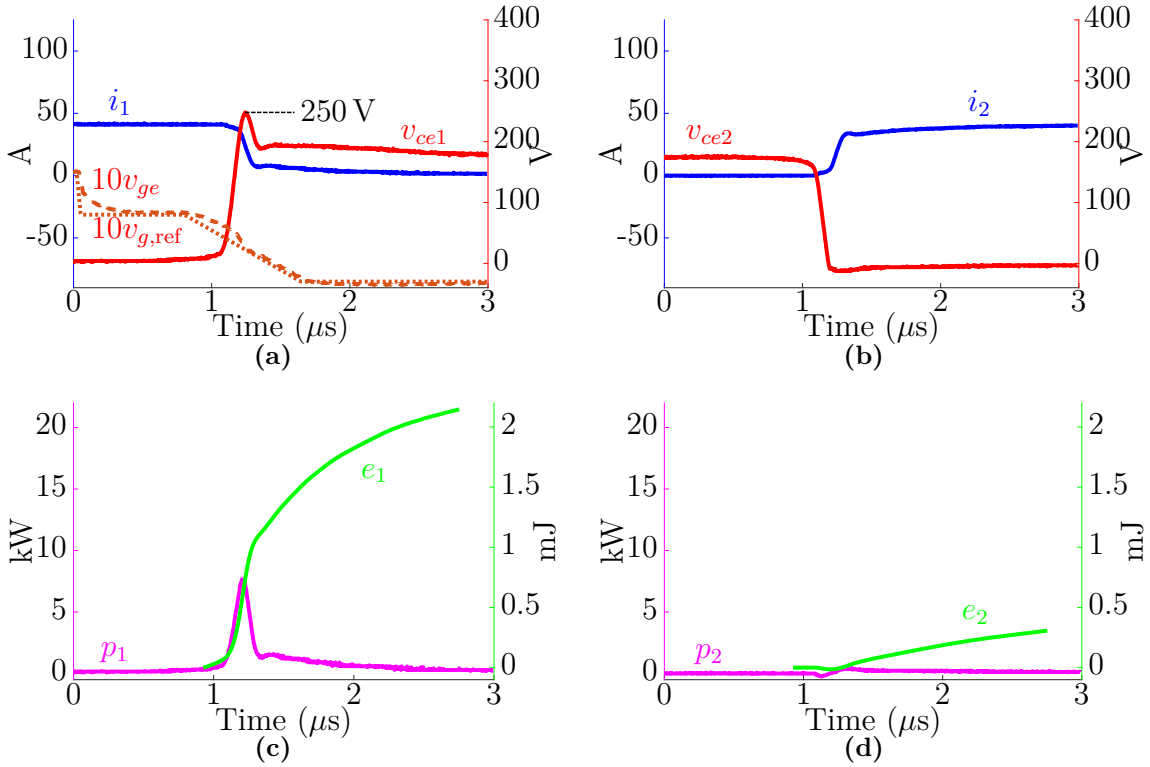


Figure 3.13: VR-AGD slow switching waveforms for turn-OFF. (a,c) S1, (b,d) S2.

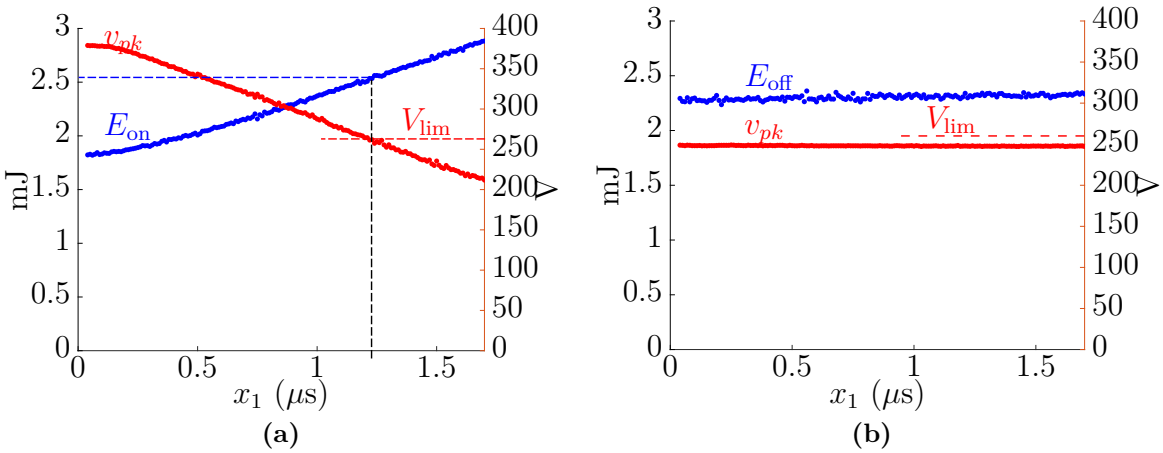


Figure 3.14: Switching loss and peak voltage for (a) S1 turn-ON and (b) S1 turn-OFF, for varying gate ramp duration x_1.

Each turn-ON x_1 duration is plotted against the resultant $\frac{\mathrm{d}i}{\mathrm{d}t}$ in Fig. 3.15a. The one-to-one mapping indicates that the gate ramp duration indeed controls the rate of current commutation for turn-ON. Fig. 3.14a is transformed using this mapping to create Fig. 3.15b, which shows peak voltage and switching energy loss as a function of rate of current commutation. This enables comparison against the predictions made by the model of diode snappy-reverse recovery (Fig. 3.2a). The experimental results confirm the overall trend predicted by the model (switching energy decreases and peak voltage increases as $\frac{\mathrm{d}i}{\mathrm{d}t}$ increases), but the experiment finds greater energy loss and lower voltage overshoot than the model predicts. This suggests that the simple treatment of reverse-recovery behaviour in Section 3.1 is not sufficient to make accurate predictions, and highlights the importance of an experimental approach when investigating switching behaviour.

3.2.8 Peak voltages and switching losses of the Double-Ramp AGD

The turn-ON behaviour as a function of the two inputs x_1 and x_2 of the Double-Ramp AGD is illustrated with iso-lines of peak voltage (Fig. 3.16a) and switching loss (Fig. 3.16b). It is evident that the peak voltage and switching loss are inversely

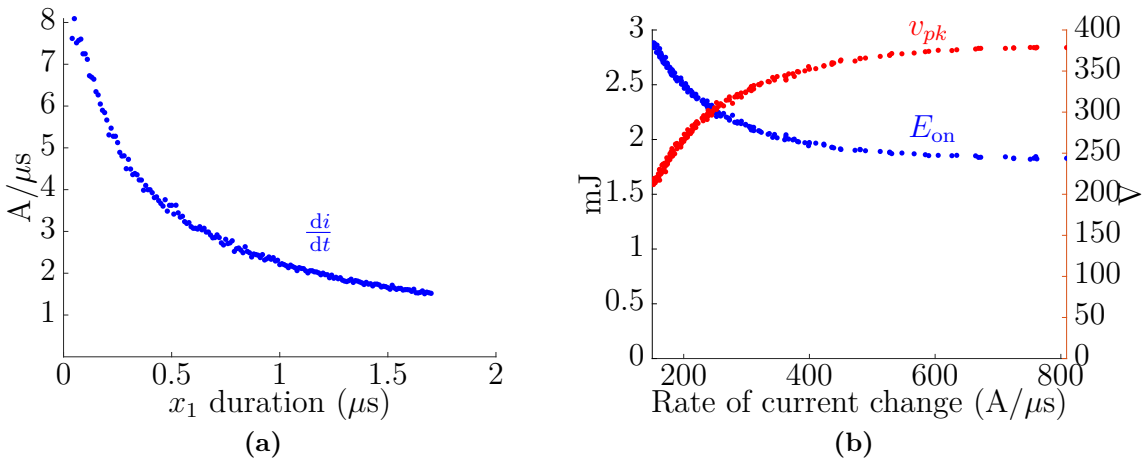


Figure 3.15: Rate of rise of S1 current is inversely related to gate ramp rate. The observed correspondence between current rate of change and x_1 (a) is used to plot switching energy and peak voltage against current rate of change (b).

related: the 'valley' of low peak voltage is coincident with the 'ridge' of high switching loss at large x_1 and $x_2 \approx 10\,\text{V}$.

Blue dots indicate evaluated (x_1, x_2) combinations. An adaptive meshing of x_1 and x_2 is implemented where the whole region is coarsely discretised (x_1 in 0.1 µs steps and x_2 in 1 V steps) to identify regions of interest where the peak voltage is less than 260 V. The mesh is then refined in the regions of interest and further measurements taken on the new mesh points.

The 260 V voltage constraint contour is marked in red on both figures. The (x_1, x_2) point with minimum achievable switching energy within the voltage constraint is marked with a green star on Fig. 3.16b. The switching energy corresponding to this point is 2.50 mJ. The time domain waveforms for turn-ON at this point are shown in Figs. 3.18c and 3.18d.

As with the Variable-Ramp AGD, very little control over turn-OFF behaviour is obtained. The peak voltage and switching loss remain approximately the same as for the fast-switching turn-OFF case.

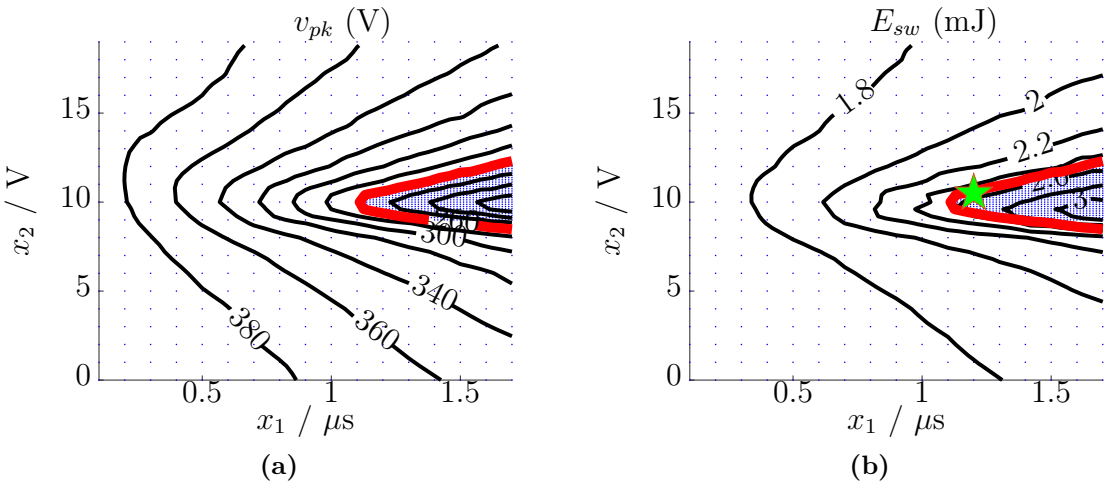


Figure 3.16: Turn-ON of S1 with Double-Ramp AGD: (a) peak transient voltage, and (b) switching energy loss. The green star in (b) marks the point within the 260 V constraint with the smallest switching energy loss.

3.2.9 Peak voltages and switching losses of the Push-Pull AGD

The peak voltage and switching energy are a function of *three* variables for the Push-Pull AGD. A two-dimensional representation of the data is obtained by taking the following approach.

1. Only data points with a peak voltage less than 260 V are plotted.

2. The x_1 dimension is removed to 'squash' the data into two dimensions, by solving the following optimisation problem at each (x_2, x_3) point:

$$x_1^j = \arg\min_{x_1} E_{sw}(x_1, (x_2, x_3)^j) \tag{3.20}$$

   where j is the index of each (x_2, x_3) point.

In other words, the x_1 point which minimises switching loss is chosen for every pair of (x_2, x_3).

The results are shown in Fig. 3.17. The points satisfying the 260 V constraint lie in a narrow band. The mesh is refined in the area where switching energy loss is lowest - evidenced by the increased density of points - so that the resolution is 25 ns in x_1 and 0.25 V in x_2 and x_3. As the first variable-voltage point x_2 increases,

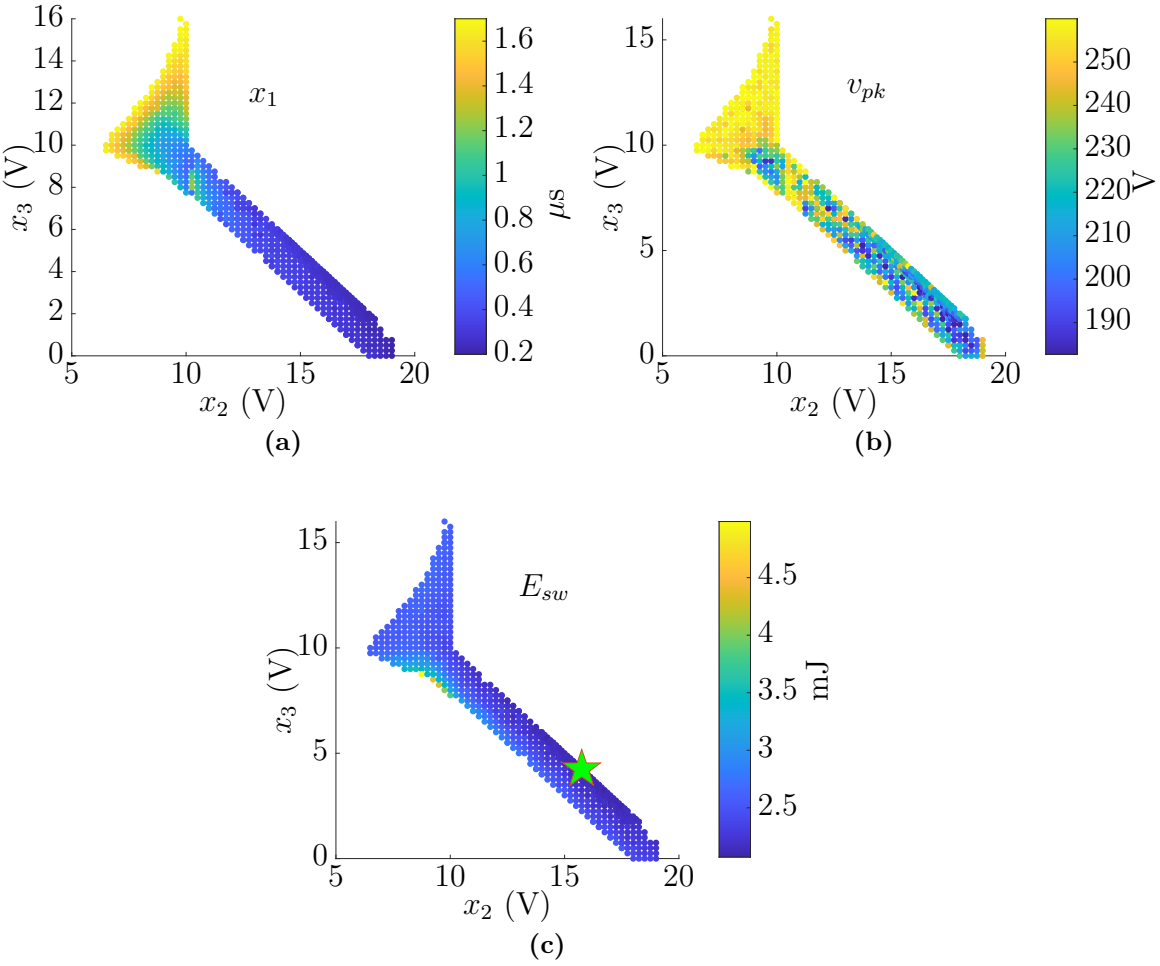


Figure 3.17: Push-Pull AGD turn-ON behaviour: (a) duration x_1 as given by (3.20), (b) peak transient voltage, and (c) switching energy loss with green star marking minimum. Unshaded points violate the 260 V peak voltage constraint.

the second variable-voltage point x_3 must decrease in order for the 260 V constraint to be met. (Measurements are taken across the whole range of $\mathbf{x}$, not just within this band, but only the points satisfying the voltage constraint are shown.)

Active period duration x_1 is long (∼1.6 µs) for x_2:x_3 ratios near unity, and becomes as short as 0.2 µs for large x_2:x_3 ratios (Fig. 3.17a). The switching loss ranges from 2.07 mJ to 4.99 mJ (Fig. 3.17c). A green star on Fig. 3.17c marks the point of minimum switching loss at $(x_1, x_2, x_3) = (0.3\,\mu\text{s}, 15.75\,\text{V}, 4.25\,\text{V})$. The time domain waveforms for turn-ON at this point are shown in Figs. 3.18e and 3.18f.

Table 3.4: The minimum switching energy and corresponding $\mathbf{x}$ for each AGD subject to a peak voltage constraint of 260 V.

	x_1 (μ s)	x_2 (V)	x_3 (V)	$v_{pk}(\mathbf{x})$ (V)	$E_{\text{on}}(\mathbf{x})$ (mJ)
Variable-ramp AGD	1.26	-	-	258	2.56
Double-ramp AGD	1.20	10.5	-	259	2.50
Push-pull AGD	0.3	15.75	4.25	259	2.07
Fast Step GD	-	-	-	384	1.77

3.2.10 Summary and waveforms at 260 V limit

A summary of the minimum attainable switching energies and the $\mathbf{x}$ points at which they occur for the three gate drives is given in Table 3.4. All AGDs can reduce peak voltage to less than the 260 V limit, unlike the fast-switching gate drive which causes a peak voltage of significantly above the limit. All AGDs incur a higher switching loss than the fast-switching case, however the PP-AGD energy loss is only 17 % higher than the fast-switching case, unlike the DR-AGD and VR-AGDs which have switching energy losses of 41 % and 45 % greater than the fast switching case, respectively. In other words, for the same peak voltage, the PP-AGD incurs 17 % less switching loss than the other two AGDs.

The voltage and current waveforms recorded at the minimum switching energy points for each AGD are presented in Fig. 3.18. The VR-AGD (3.18a and 3.18b) and DR-AGD (3.18c and 3.18d) are nearly indistinguishable and produce very similar results. The PP-AGD (3.18a and 3.18b) produces qualitatively different behaviour: by briefly discharging S1's gate during the decay in S2's reverse-recovery current, the voltage across S1 rises for a short time. Thus the voltage peak created by the parasitic inductance is shared between the two semiconductor devices so that the breakdown voltage is not exceeded for either device.

3.2.11 Varying voltage constraint

The results presented above for the 260 V limit make use of the AGDs' ability to reduce turn-ON peak transient voltages, however since the turn-OFF peak voltage remains below 260 V even for step-input switching the AGDs have little effect on turn-OFF.

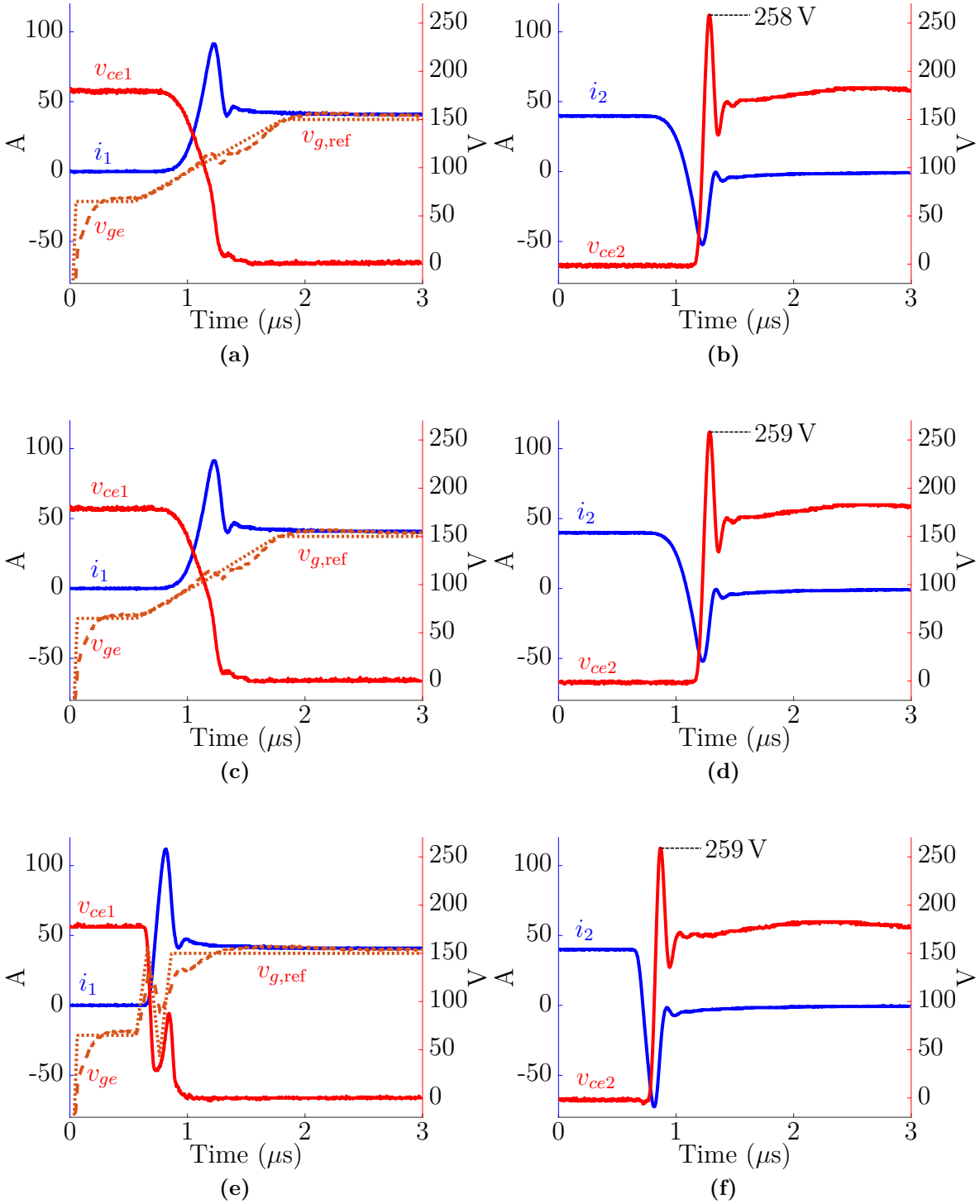


Figure 3.18: Turn-ON voltage and current waveforms for (a)(b) Variable-Ramp AGD (c)(d) Double-Ramp AGD, and (e)(f) Push-Pull AGD. Each AGD is working at the **x** point identified to produce lowest switching loss subject to a 260 V constraint on peak voltage.

The procedure followed above is repeated for different peak voltage limits: for each limit, the lowest attainable turn-ON and turn-OFF switching loss is found for the VR-AGD, DR-AGD, and PP-AGD. The results for the limit ranging from 200 V to 300 V (Fig. 3.19) show all switching energies increasing as the constraint is tightened (voltage limit reduced).

The minimum turn-ON losses (Fig. 3.19a) increase more for the VR-AGD and DR-AGD than for the PP-AGD as the voltage limit is reduced. The extra degree of freedom (gate voltage point) of the DR-AGD only gives a small (∼2%) reduction in turn-ON loss as compared to the VR-AGD. The PP-AGD outperforms both VR- and DR-AGD across the voltage range due to the way in which it enables high rates of change of current while suppressing the peak voltage across any one device.

The turn-OFF losses (Fig. 3.19b) are truncated at peak voltage limits below ∼250 V for the VR- and DR-AGD since these AGDs cannot reduce the peak transient voltage below this limit (no feasible points exist). The PP-AGD can reduce the peak transient voltage as low as 216 V but at the cost of relatively high turn-OFF loss. Above a limit of ∼250 V all three AGDs switch S1 off as fast as possible, resulting in constant turn-OFF loss with respect to voltage limit in this range.

Some artefacts resulting from the discretization of measurement points in $\mathbf{x}$ are visible in Fig. 3.19: the apparent discontinuities in the switching energy loss above ∼270 V are attributed to the relatively coarse mesh at the corresponding region in the $\mathbf{x}$-space. (Measuring on a fine mesh across the whole of the $\mathbf{x}$ space is expensive in time due to the large number of measurements that must be taken.) The difference in turn-OFF losses between the AGDs above a limit of ∼250 V is similarly a result of insufficient data in this area - all AGDs are ideally expected to produce the low turn-OFF losses of the step-input gate-drive of Fig. 3.11.

3.3 Conclusions

This chapter demonstrated how IGBT switching behaviour can be altered by AGDs in order to control switching energy loss and peak transient voltage. Analysis suggests that diode snappy reverse-recovery is the cause of the highest transient

voltages in the silicon IGBT bridge-leg considered. This was observed in practice when fast-switching driven by a step input to the gate of the control device: a peak voltage 213 % of the dc bus (384 V peak for a bus voltage of 180 V) appeared across the freewheeling diode during its reverse-recovery. This peak transient voltage was reduced by all three AGDs considered, with the penalty of increased switching energy loss. A procedure was introduced for finding the lowest switching loss obtainable by each AGD for a given limit on peak voltage. It was found that the most sophisticated AGD considered, the PP-AGD, can operate with greatly reduced turn-ON switching loss compared to the simpler VR-AGD and DR-AGD (17 % lower loss when peak voltages are constrained to 260 V). The PP-AGD is unique among the gate drives considered in that it can remove charge from the IGBT gate during the turn-ON transient, which enables the IGBT collector-emitter voltage to briefly rise as the diode recovers, thereby sharing the peak voltage stress between the two semiconductor devices and reducing the stress on any individual device.

The practical implications of these results are investigated in the next chapter. It should be noted that the IGBT bridge-leg tested here is rated to block collector-emitter voltages up to 1200 V, while the data presented in this chapter is from operation at below 400 V due to experimental limitations. This may mean the data are not representative for devices operating near their rated voltage limits. The experiment presented in the next chapter uses 600 V rated devices so that the tested operating conditions are realistic for the device class.

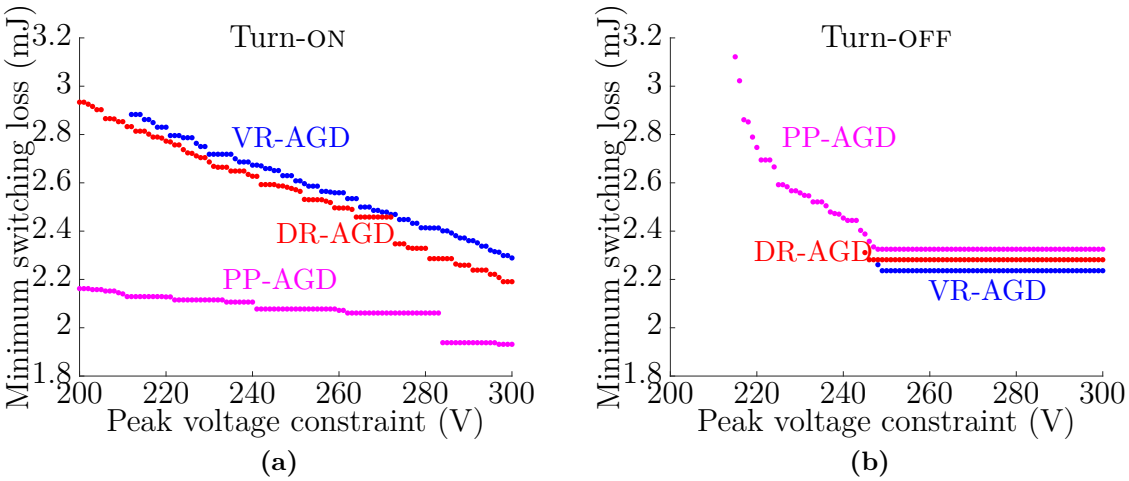


Figure 3.19: Minimum switching loss that each AGD can obtain for different limits on peak transient voltage. (a) Turn-ON, and (b) turn-OFF switching loss.

4

Increasing IGBT power capacity using AGD

This chapter investigates whether the capability of AGD demonstrated in Chapter 3 can be usefully applied to increase the power that is processed by the IGBTs in a converter. The significance of the power-processing capability of the IGBTs in an inverter is explained in Section 4.1. This leads to the definition of the switch's power-processing *capacity*, and a framework is proposed to assess the impact of AGD on switch capacity. An experimental method used to obtain data on the switch power capacity is presented, followed by results showing the maximum IGBT power throughput for three different gate drive strategies. This chapter is based on the journal publication [86]. The gate driver hardware used here is contributed by Rogers and Murmann, as in the preceding chapter, and the goal of maximising the IGBT power capacity was proposed by Rogers. The development of the experimental method, and the design and assembly of the power circuit hardware and associated control software, is my own work.

4.1 Optimal matching of dc bus voltage to device voltage rating

AGDs, by limiting the peak transient voltage stress across the semiconductors, could find use in two different scenarios. In the first, the AGD could increase the range of power semiconductors suitable for operating at a particular dc-bus voltage, by reducing the transient voltage overshoot so that it becomes possible to use lower voltage rated devices. This is applicable to the common design process where the dc-bus voltage is determined before the power semiconductors are selected. For example, a standard dc bus voltage in electric vehicles is 400 V, therefore the IGBTs in the inverter might be rated for 650 V to accommodate transient peak voltages [87]. By reducing the transient peak voltages using AGD, it could become possible to use lower voltage rated devices (e.g. 600 V IGBTs) in the inverter, thereby reducing cost and/or conduction losses. However, selecting the device voltage rating is a relatively coarse decision since commercially available devices only have voltage ratings from a limited discrete set (e.g. {600 V,650 V,1200 V,1700 V...} for IGBTs). Therefore optimally matching device voltage rating to a particular dc bus voltage is limited to the standard voltage classes.

The second scenario is the reverse of the first: the dc bus voltage is selected to be optimal for a particular of semiconductor device. In an application where the dc bus voltage is a continuously-variable design decision, this means the dc voltage can be chosen to fully utilise the rating of the power devices. This is applicable, for example, to power converters that are coupled through transformers. The turns-ratio of the transformer is chosen to optimally match the dc bus voltage of the converter to the external fixed voltage that the converter is interfaced with. For example, in the three-phase grid-tied inverter (Fig. 4.1), the transformer provides a degree of freedom to match the dc bus voltage V_{dc} to grid voltage V_{LL} at the design stage by selecting the appropriate turns ratio n.

The dc bus voltage that is considered 'optimal' here is that which maximises the power throughput of the converter. The power delivered to the grid in the

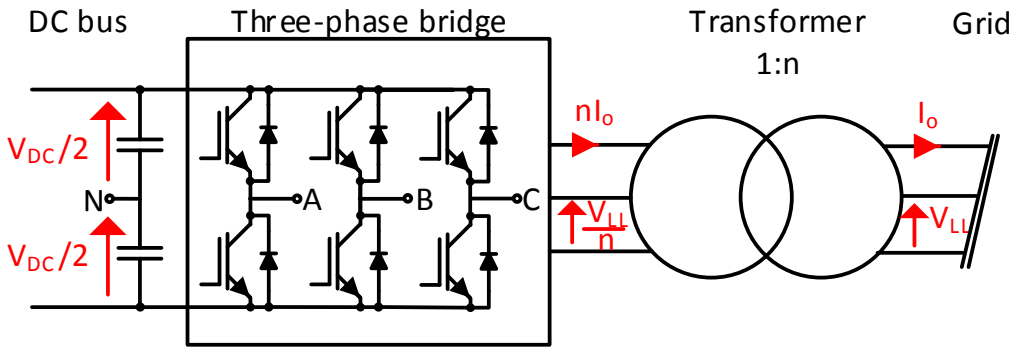


Figure 4.1: An example application where the dc-bus voltage can be optimally matched to the power semiconductor devices. The grid-tied three-phase inverter has an output transformer whose turns ratio n allows matching of the dc-bus voltage to the low or medium voltage 3-phase grid.

example of Fig. 4.1 is

$$P_{\text{out}} = \sqrt{3} V_{\text{LL}} I_L \,, \tag{4.1}$$

where V_{LL} is the line-to-line voltage of the transformer output, and I_L is the transformer line current. Maximum line-to-line voltage is set by the dc bus voltage V_{dc}, therefore the goal of increasing converter output power P_{out} (4.1) is analogous to increasing the $V_{dc} I_L$ product.

4.2 Definition of switch capacity

We consider the case where V_{dc} and I_L are both limited by the power semiconductor devices: the device voltage rating places an upper limit on V_{dc}, and the maximum device temperature places an upper limit on I_L. It is natural to define the $V_{dc} I_L$ product as the *apparent power* S that the semiconductor switch is processing

$$S = V_{\text{dc}} I_{\text{L}} \,. \tag{4.2}$$

The *capacity* of the switch is the maximum apparent power the switch can sustain, and is a measure of its power handling capability:

$$S^{\text{max}} = \max\left(S\right). \tag{4.3}$$

The upper limit on the dc bus voltage is determined by the voltage rating of the switch $V_{\text{CE(max)}}$ and by the magnitude of the transient voltage V_{ov} above

the dc level during switching, i.e. the dc bus voltage plus transient overshoot must be less than the switch rating

$$V_{\mathrm{dc}} + V_{\mathrm{ov}} \leq V_{\mathrm{CE(max)}} \,. \tag{4.4}$$

The upper limit on the conducted current is thermally determined: the power loss of the switch increases as a function of the conducted current, and the maximum power loss is set by the junction temperature limit of the device

$$P_{\mathrm{loss}}^{\mathrm{max}} = \frac{T_j^{\mathrm{limit}} - T_a}{R_{ja}} \,, \tag{4.5}$$

where T_j^{max} is the junction temperature limit, T_a is the ambient temperature, and R_{ja} is the junction-ambient thermal resistance.

Conventionally, the dc bus voltage limit and conducted current limit are treated independently [88]. However the peak transient voltage $V_{\mathrm{dc}} + V_{\mathrm{ov}}$ and the switching energy loss are coupled: both are a function of the gate drive, as demonstrated in Chapter 3. Therefore this coupling must be taken into account when finding the capacity of a switch. For example, the switch could be driven with low gate resistance: the resulting low switching loss would allow the maximum conducted current to be high, but the dc bus voltage would have to be significantly below the switch voltage rating because of the high peak transient voltage. Conversely, if the switch were driven slowly with a high gate resistance, the high switching loss would limit the maximum conducted current, but the dc bus voltage could approach the device voltage rating since transient voltage overshoot would be reduced.

Expressing the voltage constraint on switch capacity (4.4) in terms of the gate drive $\mathbf{x}$, gives

$$V_{\mathrm{dc}} \leq V_{\mathrm{CE(max)}} - V_{\mathrm{ov}}(\mathbf{x}) \tag{4.6}$$

and expressing the power loss constraint (4.5) in terms of a conduction loss and an $\mathbf{x}$-dependent switching loss gives

$$P_{\mathrm{loss}} = D I_{\mathrm{L}} V_{\mathrm{CE(on)}}(T_j, I_{\mathrm{L}}) + f_{\mathrm{sw}} F(\mathbf{x}, I_{\mathrm{L}}, V_{\mathrm{dc}}, T_j, \dots) \leq P_{\mathrm{loss}}^{\mathrm{max}} \,, \tag{4.7}$$

where

$V_{\mathrm{CE(on)}}$ is the on-state collector-emitter voltage of the IGBT,

T_j is the junction temperature of the switch,

D is the duty cycle of the switch,

f_{sw} is the switching frequency,

$F()$ is an unknown function mapping switching energy loss to load current, dc-bus voltage, and other factors such as device physics, circuit layout, gate drive etc.

The form of the function $F()$ is unknown, but the value of $F()$ is the switching energy loss and can be calculated based on experimental measurements using (1.19). The form of $F()$ in (4.7) is presented in this section to highlight the dependence of switching energy loss on load current, dc-bus voltage, and gate drive. Later in the chapter, the form of (1.19) is used when numerical values of E_{sw} are being discussed.

Rearranging (4.6) and (4.7) and substituting into (4.2) gives the maximum switch apparent power as

$$S^{\max} = \frac{(V_{\mathrm{CE(max)}} - V_{\mathrm{ov}}(\mathbf{x}))(P_{\mathrm{loss}}^{\max} - f_{\mathrm{sw}}F(\mathbf{x}, I_L, V_{\mathrm{dc}}, T_j, \dots)}{DV_{(\mathrm{CE,on})}(T_j, I_L)}\,. \tag{4.8}$$

Table 4.1 presents ways in which $S^{\max}$ can be increased, which either enable operation at higher dc bus voltages, or increase the current that the device can conduct. Drawbacks associated with each intervention are also listed. Designers must choose between the conflicting factors based on knowledge of the associated trade-offs. Here, the use of the gate-drive to trade-off switching loss and peak transient voltage is investigated, i.e. effectively increasing the switch capacity, without changing the switching device itself or other characteristics of the power converter.

There are two factors that contribute to the increase of switching loss at higher dc-bus voltages:

1. Simply increasing the dc-bus voltage causes switching losses to increase, since the product of drain current and drain-source voltage at any instant during switching is larger. This is the case even if the gate drive remains unchanged.

Action to increase $S^{\max}$	Advantage	Penalty
Use devices with a higher voltage rating	Allows higher dc-bus voltage	Larger channel resistance or on-state voltage drop (per unit area)
Use devices with a smaller on-state voltage drop $V_{(\mathrm{CE,on})}$	Increases device current carrying capacity	Lowering conduction loss by increasing die area increases device cost and increases capacitive switching losses [89]
Increasing $P_{\mathrm{loss}}^{\max}$ by reducing the junction to ambient thermal resistance R_{ja}	Increases device current carrying capacity	Practical size/weight/cost constraints limit the R_{ja} achievable
Reduce the voltage overshoot $V_{\mathrm{ov}}(\mathbf{x})$ occurring during switching	Allows higher dc-bus voltage	Reducing peak transient voltages by modifying the gate drive parameters $\mathbf{x}$ increases switching loss
Reducing the switching losses (e.g. by reducing the switching frequency f_{sw} or using lower gate resistance)	Increases device current carrying capacity	Increased energy storage requirements of capacitors and inductors in the circuit (increased size/weight/cost); degradation of output waveform quality; increased peak transient voltages

Table 4.1: Interventions to increase a switch's power-handling capacity, from (4.8). The intervention investigated in this chapter is highlighted.

2. If the gate drive is an AGD which slows down the switching as the dc-bus voltage approaches the device voltage limit (in order to reduce the voltage overshoot), then the drain current and drain-source voltage overlap for longer, leading to a further increase in the switching energy loss.

Equation (4.8) shows that an AGD has potential to increase utilization of the switch if it enables an increase in dc-bus voltage great enough to counteract the increase in switching energy loss. In other words, the trade-off between the increased dc-bus voltage and the higher switching loss is investigated in terms of the switch capacity. Since $F()$ is a complicated function dependent on many variables, an experimental approach is used here to investigate the impact of AGD

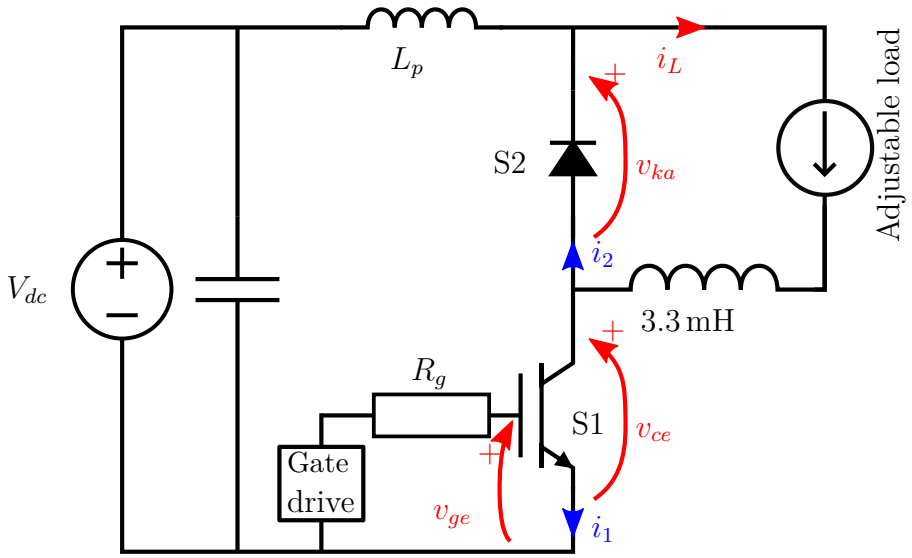


Figure 4.2: Converter used for experiment with independent control of load current and dc-bus voltage.

on switch capacity across a range of switching frequencies. As switching loss is proportional to switching frequency, the hypothesis is that there will be a critical switching frequency below which the AGD will increase the capacity of the switch compared to a conventional gate drive.

4.3 Experimental methodology

4.3.1 Power circuit topology and hardware

Switch capacity is investigated using a diode-clamped IGBT buck converter (Fig. 4.2). Independent control of dc-bus voltage and load current is achieved by using an adjustable power supply to support the dc-bus and an electronic load in constant-current mode as the load. A 600 V, 25 A IGBT (IRG4PC40KDPbF [90]) and freewheeling diode (ISL9R3060G2 [91]) are used for verification. Both are discrete devices in the TO247 package. The converter is run at a constant duty cycle of 0.3 throughout the experiment. The 0.3 ratio is selected because it corresponds to the maximum power capability (3 kW) of the external power supply which is delivering power to the dc-bus, when the converter is operating at the highest voltage (∼400 V) and load current (25 A). In keeping with the previous discussion, the IGBT is named S1 and the diode S2.

The measurement hardware is similar to that in Chapter 3. The signals exhibit shorter rise times here than in Chapter 3 due to the faster switching devices, which means a higher measurement bandwidth is required. Collector-emitter voltage of the IGBT S1, v_{ce}, is measured with a 300 MHz 100:1 passive probe. A second probe (of the same type) measures the voltage between the cathode of S2 and the emitter of S1. The cathode-anode voltage of the diode, v_{ka}, is calculated from this voltage minus v_{ce}. This use of two ground-referenced voltage measurements means that passive probes can be used instead of the lower-bandwidth differential probes used for the experiment in Chapter 3.

A 100 MHz N2783A Keysight current probe measures the IGBT collector current, i_1, and the diode current i_2 is inferred from Kirchoff's current law:

$$i_2(t) = I_L - i_1(t)\,. \tag{4.9}$$

The gate-emitter voltage of S1, v_{ge}, is measured with a 350 MHz 10:1 passive probe. All signals are sampled at 1.25 GS/s using a 250 MHz-bandwidth 8-bit oscilloscope (PicoScope PS6402C). All probes are de-skewed before running the experiment. Switching energy loss is calculated from the voltage and current waveforms using (1.19) The error in switching energy loss measurement is expected to be on the order of 1 %, based on the analysis of Section 3.2.2. Repeated measurement of switching energy loss during steady-state operation of the converter yielded a range in the loss of less than 1 %. The implementation of the converter is shown in Fig. 4.3.

4.3.2 Gate drive methods

The gate drive hardware described in Chapter 3 is used in this experiment. As before, the Gate Waveform Generator operates in several distinct modes for S1 turn-ON. The *Fast Gate Drive (FGD)* (Fig. 4.4a) applies a step input to the gate of S1 to trigger a fast switching transition. The *Variable-Ramp AGD (VR-AGD)* and *Push-Pull AGD (PP-AGD)* take an input vector of parameters $\mathbf{x}$ and output a gate reference voltage waveform based on $\mathbf{x}$ (Figs. 4.4b and 4.4c). The *Double-Ramp AGD* tested in Chapter 3 is not investigated here as the additional degree

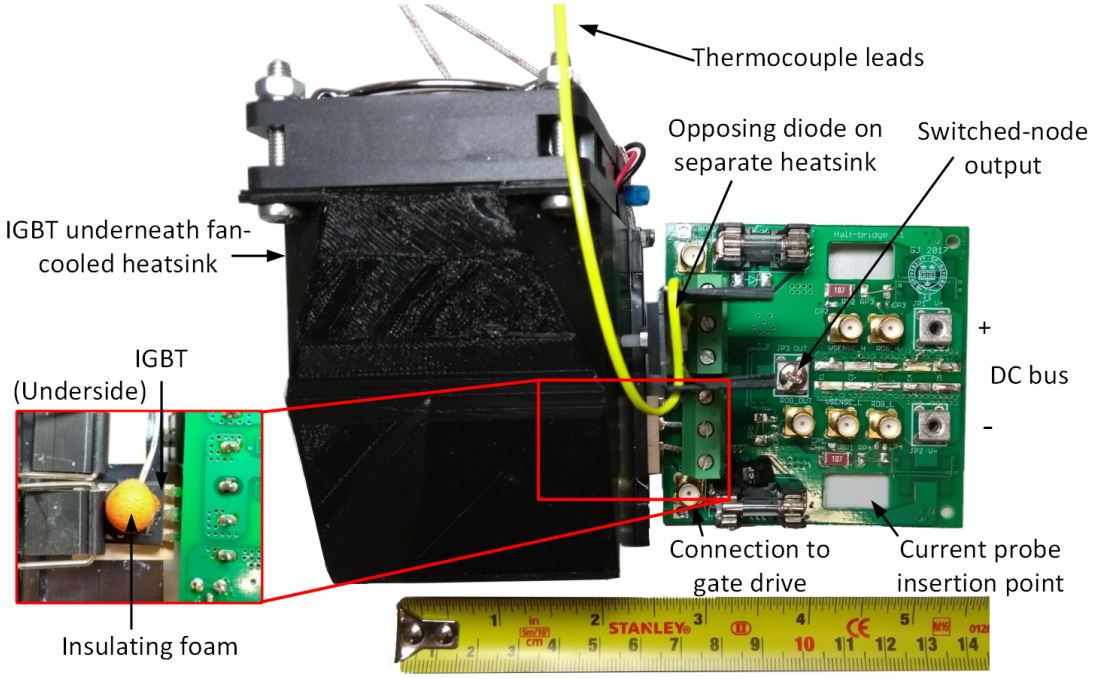


Figure 4.3: Half-bridge circuit board, with separate heat-sinks for IGBT and opposing diode. Inset shows back-view of IGBT with thermocouple and insulating foam (explanation in Section 4.3.4). Not shown are 2x 330 nF polypropylene capacitors on board underside.

of freedom only gained a small improvement in switching behaviour. Note that the PP-AGD is parametrised slightly differently here than for the experiment in Chapter 3: two of the three degrees of freedom define durations and there is only one variable-voltage point. This is because I observed that the voltage of the first variable-point in the PP-AGD waveforms in Chapter 3 did not vary much for the best performing gate waveforms, suggesting that this was a redundant variable in the parameterization. Instead, allocating this degree of freedom to the duration of the linear segment was found to be a more effective.

The peak transient voltage during turn-ON exceeds that during turn-OFF across the range of load currents investigated. In fact, turn-OFF transient voltage reaches no more than 112% of the dc bus voltage during fast switching, compared to turn-ON transient voltages of approximately 130% of the dc bus voltage (Table 4.2). Therefore it is primarily the turn-ON behaviour that limits the magnitude of the dc bus voltage. The VR-AGD but not the PP-AGD is applied to the turn-OFF transition (Fig. 4.4d), since the required reduction in turn-OFF transient voltage is

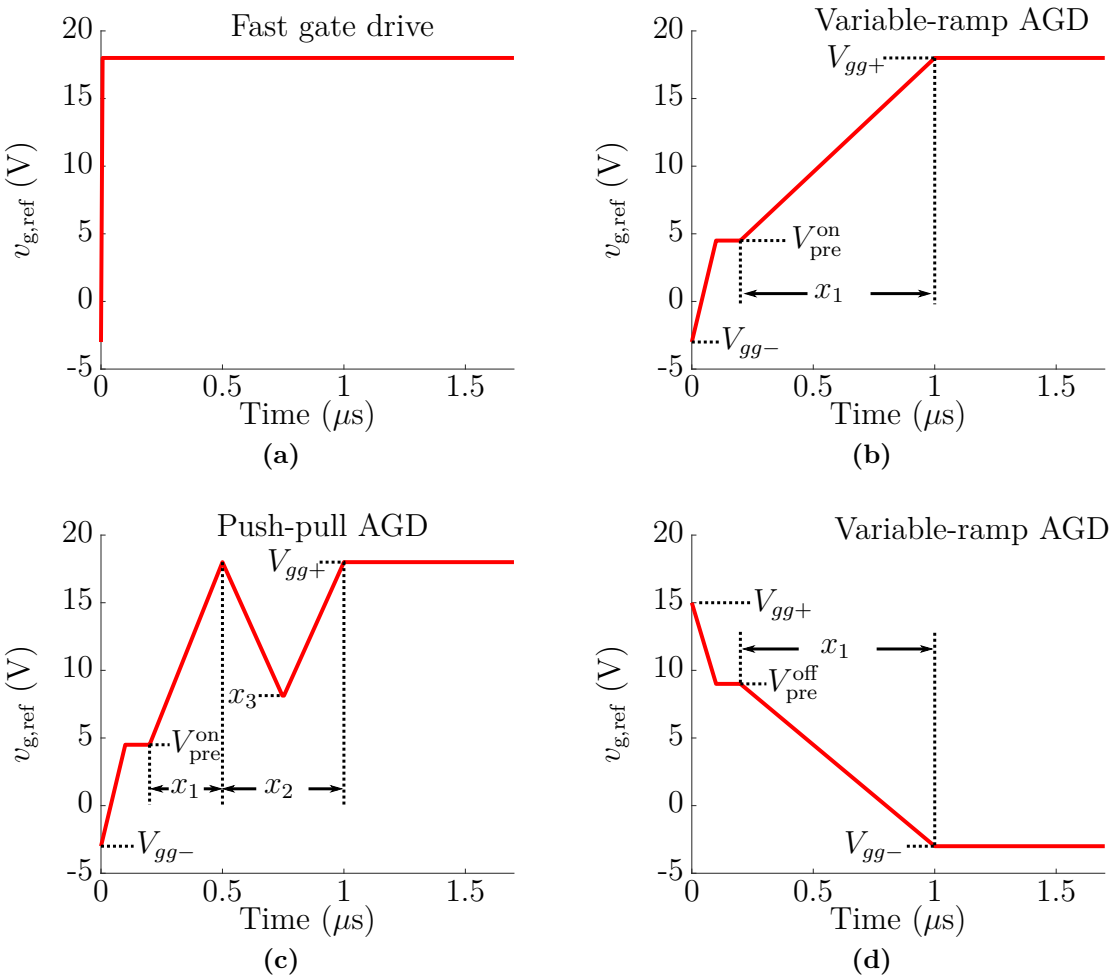


Figure 4.4: Example gate reference waveforms for the gate drive modes used in the experiment: (a) Fast gate drive (FGD) turn-ON, (b) Variable-ramp AGD (VR-AGD) turn-ON, (c) Push-pull AGD (PP-AGD) turn-ON, and (d) Variable-ramp AGD (VR-AGD) turn-OFF.

small and it is simpler to find the optimum parameter vector $\mathbf{x}$ for the VR-AGD.

Table 4.3 lists the fixed parameters used by the gate drive. The maximum swing of the output is from $-10\,\mathrm{V}$ to $18\,\mathrm{V}$.

4.3.3 Overview of the experimental method

Maximum IGBT capacity is found for each type of gate drive (FGD, VR-AGD and PP-AGD) by taking measurements of switching behaviour across a range of load currents and dc-bus voltages. The load currents tested are $18\,\mathrm{A}$, $19\,\mathrm{A}$ ... $25\,\mathrm{A}$, and the dc-bus voltages tested are $300\,\mathrm{V}$, $310\,\mathrm{V}$ ... $400\,\mathrm{V}$. Every combination of load

Table 4.2: Peak transient voltage for turn-ON and turn-OFF with the FGD expressed as a percentage of the dc-bus voltage (400 V). Turn-on overshoot dominates in all cases.

		Junction temperature	
		75 °C	100 °C
Load	18 A	On 136 % Off 110 %	On 132 % Off 106 %
	24 A	On 130 % Off 112 %	On 128 % Off 108 %

Table 4.3: Values of fixed gate waveform parameters

Name	Value
$T_{\text{pre}}^{\text{on}}$	0.1 µs
$T_{\text{pre}}^{\text{off}}$	0.1 µs
$V_{\text{pre}}^{\text{off}}$	4.5 V
$V_{\text{pre}}^{\text{off}}$	9.0 V
V_{gg+}	18.0 V
V_{gg-}	−3.0 V
R_g	1.4 Ω

current and dc-bus voltage within these ranges is tested.

Figure 4.5 illustrates the method for the PP-AGD case. Subscript i refers to the load current, subscript k refers to the dc-bus voltage, and $x_{1,m}$, $x_{2,n}$ and $x_{3,p}$ refer to the gate drive parameters of the PP-AGD. Switching waveforms are captured for every combination of I_i, V_k, $x_{1,m}$, $x_{2,n}$, and $x_{3,p}$, and these waveforms are processed to calculate the switching energy loss and peak voltage, denoted $E(I_i, V_k, x_{1,m}, x_{2,n}, x_{3,p})$ and $\hat{v}(I_i, V_k, x_{1,m}, x_{2,n}, x_{3,p})$ respectively. Switching loss is converted into the resultant steady-state IGBT junction temperature using (4.11) as explained later in Section 4.3.4.

For each load current and dc-bus voltage, the best waveform of the AGD is selected by choosing the gate parameters $x_{1,m}$, $x_{2,n}$, and $x_{3,p}$ that minimise the resultant IGBT temperature while also not causing peak voltages to exceed the device limit, i.e.

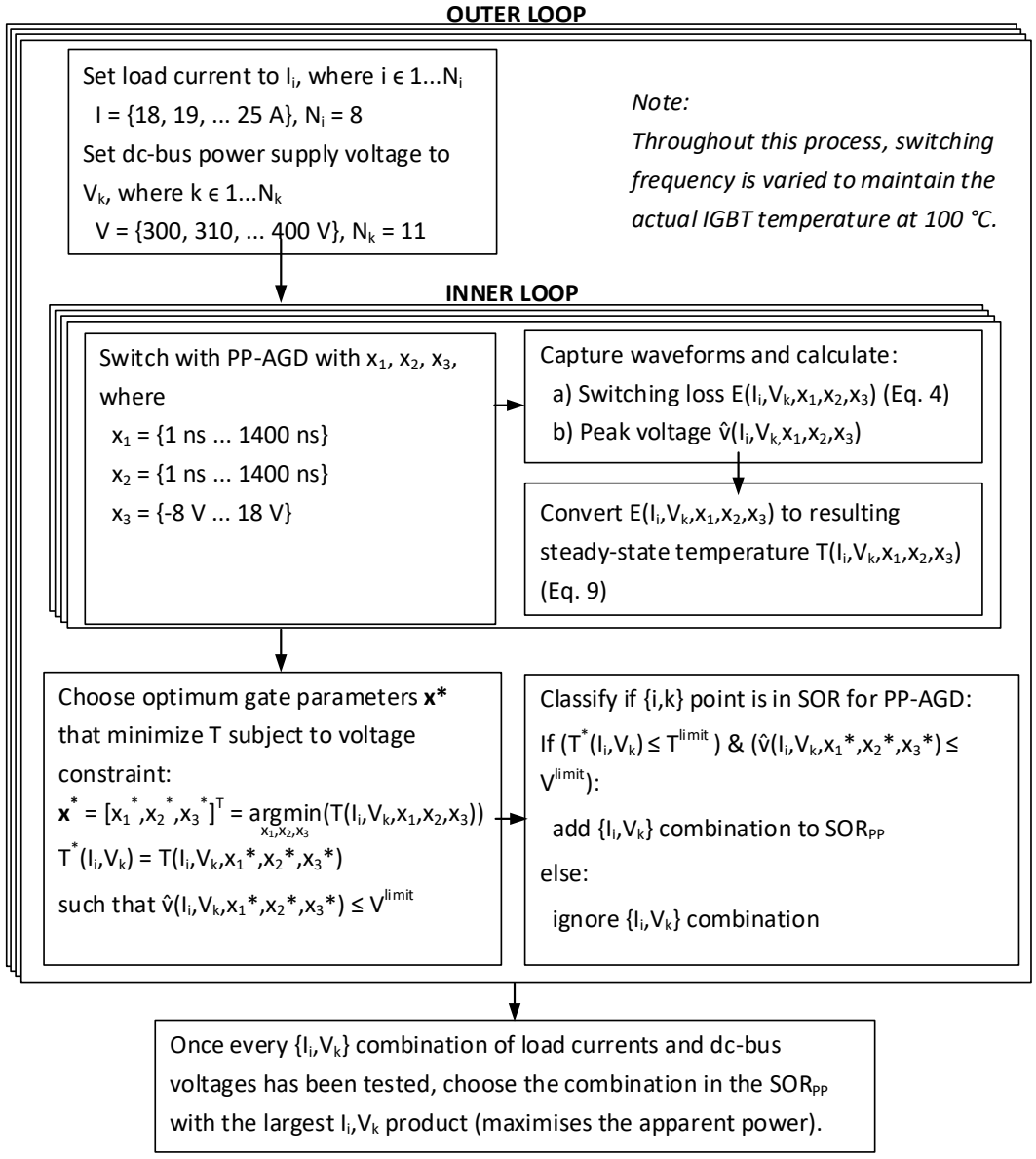


Figure 4.5: The method flow for determining the maximum apparent power obtainable using the PP-AGD. All combinations of load current, dc-bus voltage and gate parameters are tested. The methods for the FGD and VR-AGD are identical, except that the VR-AGD only has one gate parameter, and the FGD has no gate parameters.

$$\begin{aligned}
\mathbf{x}^*(I_i, V_k) &= [x_1^*, x_2^*, x_3^*]^{\mathrm{T}} \\
&= \arg \min_{x_{1,m}, x_{2,n}, x_{3,p}} T(I_i, V_k, x_{1,m}, x_{2,n}, x_{3,p}) && \text{(4.10a)} \\
T^*(I_i, V_k) &= T(I_i, V_k, x_1^*, x_2^*, x_3^*) && \text{(4.10b)} \\
\text{such that} \quad & \hat{v}(I_i, V_k, x_1^*, x_2^*, x_3^*) \leq V^{\text{limit}} && \text{(4.10c)}
\end{aligned}$$

This leaves, for each I_i, V_k combination, only a single temperature $T^*(I_i, V_k)$ which is the lowest feasible IGBT temperature that the gate drive can obtain. If this temperature is less than the device limit, then the I_i, V_k combination of load current and dc-bus voltage is acceptable. Therefore the combination I_i, V_k is added to the set of acceptable operating points, which is called the *safe operating region* or *SOR*. However if $T^*(I_i, V_k)$ is above the device limit this means that the gate drive has been unable to produce acceptable switching behaviour at the load current and dc-bus voltage, therefore the I_i, V_k combination is not added to the SOR.

The maximum apparent power $S^{\max}$ is obtained at the point in the SOR whose product of load current and dc-bus voltage is larger than at any other point in the SOR. $S^{\max}$ and the load current and dc-bus voltage combination at which it occurs is saved for the PP-AGD.

The procedure is analogous for the FGD and the VR-AGD, the only difference being that there is only one gate drive parameter for the VR-AGD, and no gate parameters for the FGD. For the FGD, $T(I_i, V_k) = T^*(I_i, V_k)$, and only I_i, V_k combinations that result in both $T(I_i, V_k) \leq T^{\text{limit}}$ and $\hat{v}(I_i, V_k) \leq V^{\text{limit}}$ get added to the SOR.

At high dc-bus voltages, the SOR is dictated by the devices' rated blocking voltage limit, while at higher load currents the IGBT junction temperature constrains the SOR. The maximum IGBT capacities obtained using the different gate driving methods indicate the potential to increase IGBT capacity by expanding the SOR to higher voltages. It is reasonable to expect that the AGD SOR will be bounded by a higher dc-bus voltage (since AGDs reduce transient voltage overshoot) while the maximum load current boundary will be reduced (since using anything other than the fastest gate drive increases switching energy loss).

The IGBT and diode used in the experiment have a rated blocking voltage of 600 V and maximum rated junction temperature of 150 °C. To allow the SOR to be determined using this procedure, without destroying the devices when the limits are exceeded, the peak diode/IGBT voltage V^{limit} is taken as 430 V and the maximum junction temperature limit T^{limit} as 100 °C (a 75 °C rise above the ambient of 25 °C). Because the switching loss of the IGBT is greater than that of the diode [92], only the thermal constraint on the IGBT is considered in this work.

4.3.4 Electrical measurement of switching loss used as a proxy for junction temperature

Each AGD method requires the evaluation (by switching) of many different gate drive waveform shapes in order to find the optimal $\mathbf{x}^*$, as described above, each of which causes a different switching energy loss. Since the thermal time constant of the system is of the order of tens of seconds and several thousand $\mathbf{x}$ need to be evaluated, it is not feasible to directly measure the resulting steady-state junction temperature of the IGBT by allowing the system to reach thermal steady-state for each $\mathbf{x}$. Therefore, the steady-state junction temperature rise that would result from continuous operation at a given $\mathbf{x}$ is instead calculated from the device power loss and the junction-to-ambient thermal resistance as

$$\Delta T_j = P_{\text{loss}} R_{ja} = (P_c + P_{\text{sw}}) R_{ja} \tag{4.11}$$

where thermal resistance R_{ja} is 3.0 °C/W.

Device conduction loss is calculated (using a similar method as found in [93]) as

$$P_c = D I_L V_{\text{CE(on)}} \,. \tag{4.12}$$

On-state voltage $V_{\text{CE(on)}}$, a function of junction temperature and load current, is found by quadratic interpolation of the data-sheet values. Device switching loss P_{sw} equals $f_{\text{sw}} E_{\text{sw}}$ where the switching energy E_{sw} is calculated using (1.19).

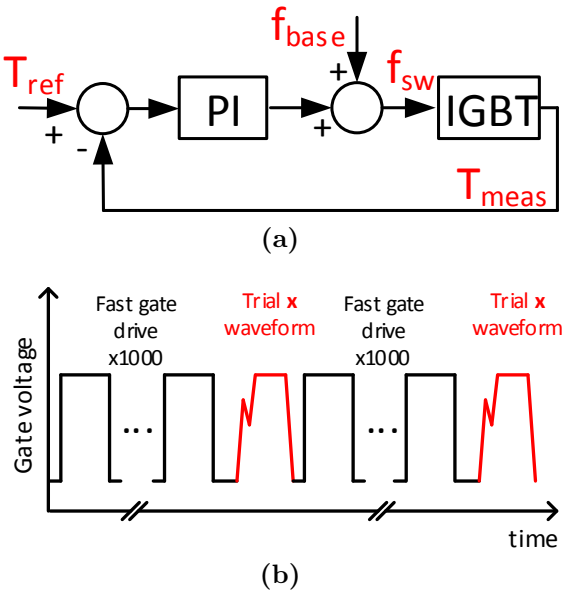


Figure 4.6: IGBT temperature control: (a) closed-loop control maintains IGBT temperature at $T_{\text{ref}} = 100\,°\text{C}$, (b) IGBT gate voltage pulse-train when performing AGD search. Temperature fluctuations are reduced by keeping the majority of switching events constant.

4.3.5 Regulation of IGBT temperature at 100 °C

As switching loss is strongly temperature dependent (increasing with temperature) [90], the IGBT must be kept at 100 °C for all trial $\mathbf{x}$ to allow the boundary of the SOR to be determined. Device power loss varies with V_{dc}, I_L and $\mathbf{x}$, therefore the die temperature is held at 100 °C by varying the switching frequency as illustrated in Fig. 4.6a. A PI controller compensates for changes in temperature that would otherwise occur when V_{dc} or I_L change.

During the AGD grid search of $\mathbf{x}$ at a given V_{dc} and I_L, the average power dissipation is kept almost constant by only having a changing gate parameter vector $\mathbf{x}$ for 1 out of 1000 switching transitions; the remaining switching edges use the constant fast gate drive shape (see Fig. 4.6b). Therefore the actual die temperature is not significantly affected by the rapidly changing trial $\mathbf{x}$, and can be maintained at 100 °C.

To obtain accurate die temperature measurements, a type-T thermocouple is placed 150 µm from the IGBT die (a similar method as used by IGBT manufacturers when thermally characterizing devices in this type of package [94]). The package

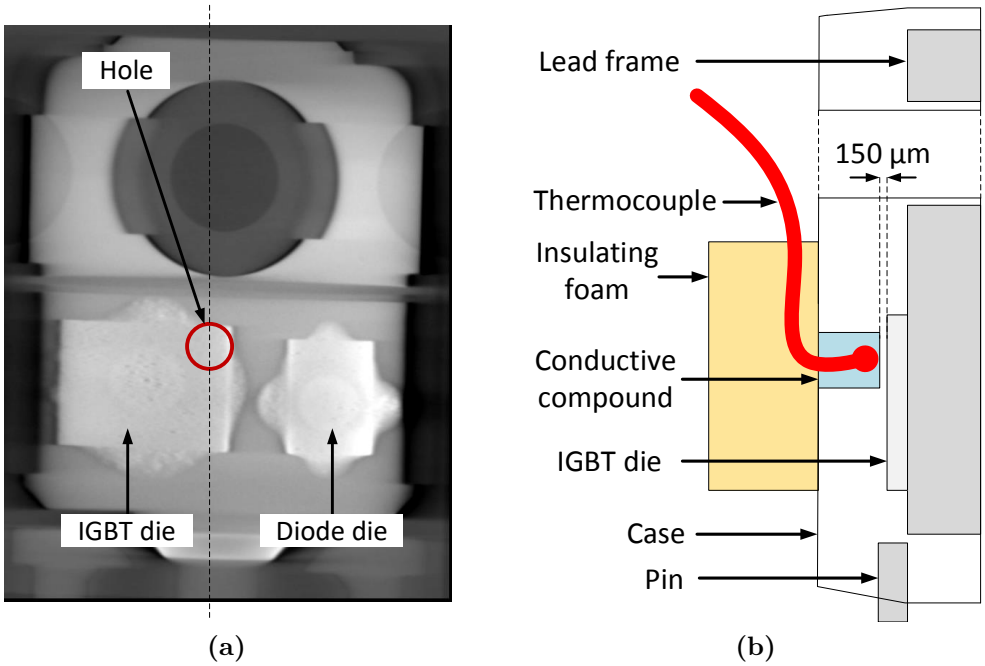


Figure 4.7: (a) Slice from an x-ray tomogram showing the silicon dies and the position of the milled hole. (b) Schematic side-view of TO-247 package showing thermocouple position relative to IGBT die.

has been imaged using x-ray tomography (Fig. 4.7a) to locate the dies and bond-wires, a 2.2 mm deep, 2 mm diameter hole has been milled above the die, and the thermocouple is fixed in this hole with thermally conductive compound (schematically illustrated in Fig. 4.7b). Thermally insulating foam is fixed on the case above and around the hole.

4.4 Results

4.4.1 Safe operating regions at 7 kHz

The IGBT steady-state junction temperature across a range of dc-bus voltages and load currents is presented in this section when using the three gate drive techniques. Temperatures are inferred using the ΔT_j from (4.11) and (1.19) based on a switching frequency of 7 kHz and the ambient temperature of 25 °C. Fig. 4.8 shows the IGBT temperatures plotted against dc-bus voltage, one plot for each type of gate drive. Each load current is plotted as a curve; the temperature limit of 100 °C is marked with a solid red line. Points with peak transient voltage above the limit of 430 V

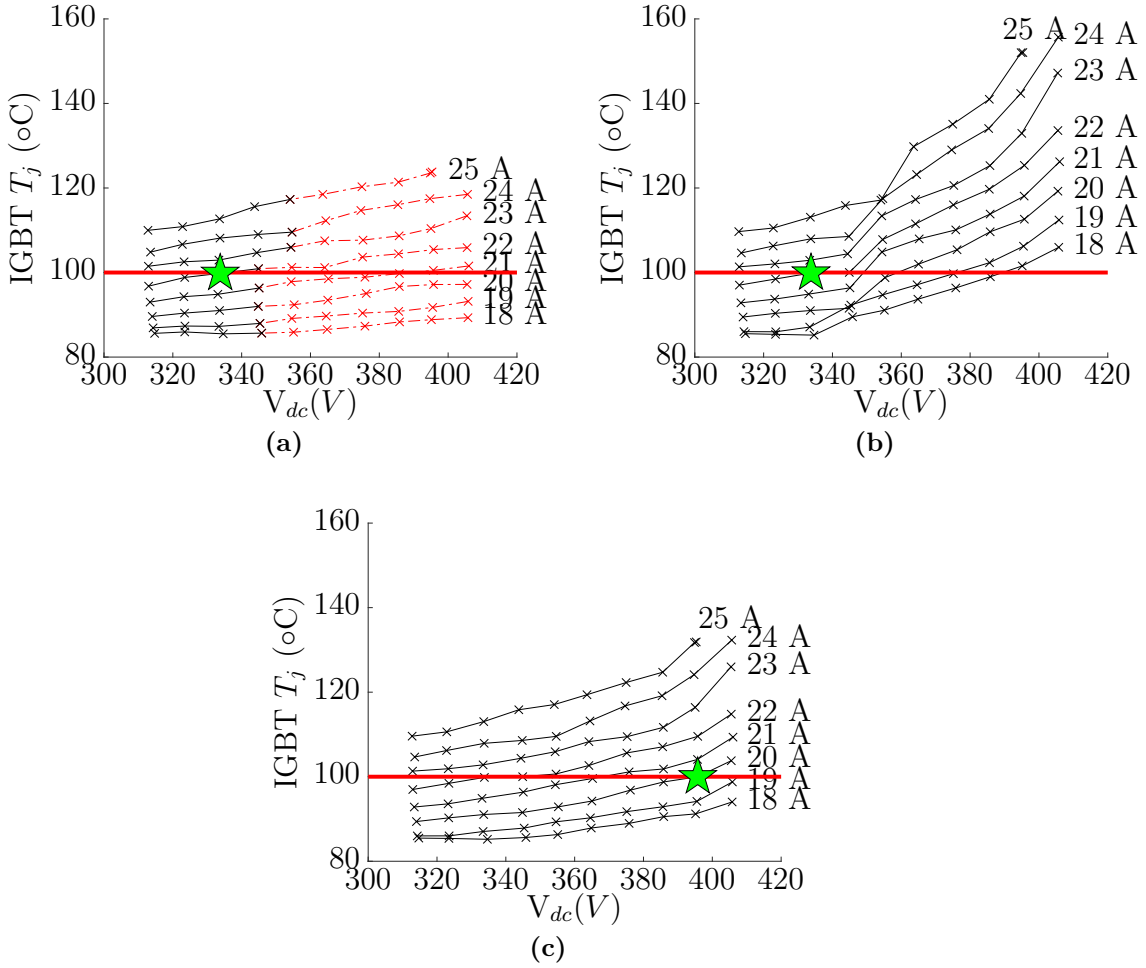


Figure 4.8: IGBT junction temperature rise across operating point range, when switching with (a) FGD, (b) VR-AGD, and (c) PP-AGD. Solid lines join points with peak transient voltage below the limit of 430 V, dashed lines indicate unsafe area with peak voltage above the limit. The green star marks the point in the SOR at which the apparent power is maximised.

are joined with a dashed red line, whereas black solid lines connect points with peak voltage below 430 V. Note that Fig. 4.8 contains information about the IGBT power loss (conduction plus switching loss) but loss measurements are transformed into resulting junction temperatures using (4.11) since it is the maximum temperature that limits the IGBT power capacity. In other words, the red line marking the limit of 100 °C indicates a constant IGBT power loss - in this case

$$\frac{100\,^{\circ}\mathrm{C} - 25\,^{\circ}\mathrm{C}}{3.00\,^{\circ}\mathrm{C/W}} = 25\,\mathrm{W} \tag{4.13}$$

The SOR for the FGD (Fig. 4.8a) is constrained both by the voltage limit and

Table 4.4: Comparison of gate drives at 7 kHz

	FGD & VR-AGD	PP-AGD
E_{on} (mJ)	0.57	0.76
V_{dc} (V)	334	396
I_L (A)	22.3	20.4
P_A (kVA)	100	108
x_1 (ns)	1	61
x_2 (ns)	-	290
x_3 (V)	-	7.4

junction temperature limit. High transient peak voltage limits the dc-bus voltage to 334 V, while the maximum load current is 22.3 A. The switch capacity in this case, obtained by operating at the maximum apparent power point marked by the green star, is $S = V_{dc}I_L = (334\,\text{V})\,(22.3\,\text{A}) = 7.5$ kVA.

For the VR-AGD (Fig. 4.8b) the voltage limit is respected at all points by slowing down the switching events. However, the penalty is larger switching loss leading to higher calculated steady-state junction temperature. As a result, the point of maximum power is the same as for the FGD (i.e. the VR-AGD offers no practical benefit).

The PP-AGD, like the VR-AGD, respects the voltage limit all the way up to a 410 V dc-bus (Fig. 4.8c). However, the PP-AGD does this with less of an increase in switching loss, compared to the VR-AGD. This means the point of maximum apparent power is shifted to 396 V, 20.4 A, giving $S = 8.1$ kVA, an 8% increase in switch capacity compared to the other gate drives. This is due to the shape of the gate control reference allowing relatively fast switching without creating high transient voltages. The comparative performance of the gate drives at 7 kHz and $T_j = 100\,°\text{C}$ is summarised in Table 4.4. The measured switching loss during turn-on is higher for the PP-AGD than for the FGD or VR-AGD since the *total* power loss is the same in all cases (25 W) and the conduction losses are lower for the PP-AGD maximum power point since it is at 20.4 A as opposed to 22.3 A.

4.4.2 Switch capacity at different switching frequencies

The results can be generalised over a range of switching frequencies. At each frequency, the SOR is calculated using (4.11) and (1.19) in the same way as in Section 4.4.1, and the maximum apparent power is found. The switch capacity across a range of frequencies is shown in Fig. 4.9a for the three gate drive cases. The power drops as switching frequency increases due to the IGBT junction temperature limit.

In the 4-8 kHz range, the PP-AGD enables higher power for the reasons discussed above. At higher switching frequencies the increased losses from the AGD become more significant and the apparent powers begin to converge, as predicted by (4.8). The AGDs always perform at least as well as the FGD: at frequencies above 10 kHz the AGD waveforms resemble the FGD waveform, resulting in the same switching behaviour - the AGDs never perform worse than the FGD.

The dc bus voltage and load current of the maximum power point for each switching frequency are shown in Figs. 4.9b and 4.9c respectively. The dc bus voltage remains higher for the PP-AGD than for the FGD and VR-AGD across the range. The load current drops as the switching frequency increases due to increased power loss, which affects the PP-AGD the most due to its higher E_{sw}. The 'steps' in the lines of Fig. 4.9 are a result of the discrete measurement points of dc bus voltage and load current. As the switching frequency increases, when the maximum power point hits the 100 °C limit it jumps to the next best operating point in the set of measurement.

It should be noted that the range of frequencies for which the PP-AGD outperforms the FGD depends on the thermal resistance between device and ambient, since it is the device temperature rise that limits the maximum load current when using PP-AGD at higher switching frequencies. Therefore, with lower thermal resistance the increased loss of the PP-AGD begins to dominate only at higher switching frequencies. For example, if the temperature rises are calculated using (4.11) with a thermal resistance of 2.00 °C/W instead of 3.00 °C/W the PP-AGD and FGD apparent powers converge at a switching frequency of approximately 19 kHz.

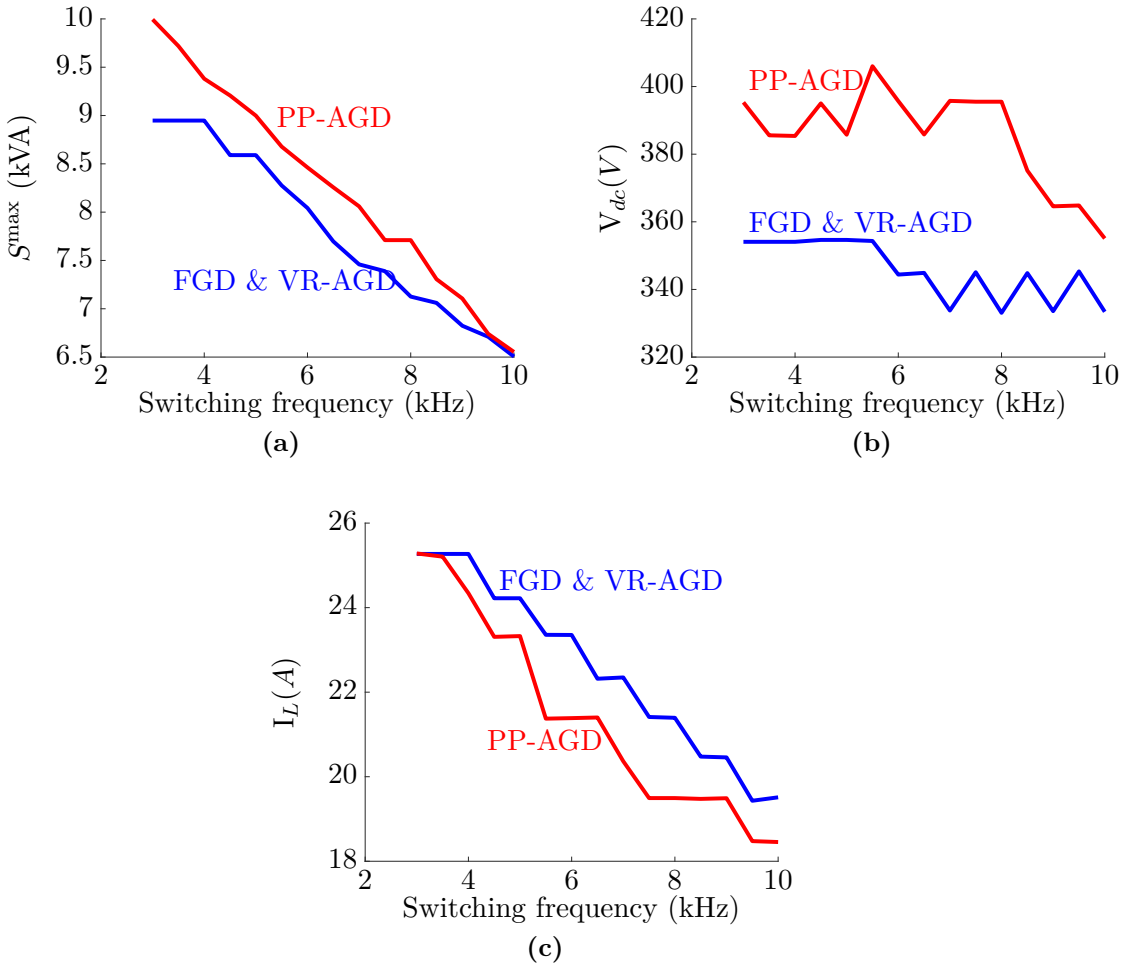


Figure 4.9: (a) Maximum apparent power for the three gate drive cases across a range of frequencies. At each frequency, the combination of dc-bus voltage (b) and load current (c) that leads to the highest apparent power is chosen from the SOR.

There is no switch capacity increase from using the VR-AGD: the peak apparent power from using it is never greater than that of the FGD. This is because, at the maximum-power point, the VR-AGD always ramps the gate reference as rapidly as the FGD, and therefore produces the same switching behaviour as the FGD. In other words, the FGD can be thought of as a special (fastest) case of the VR-AGD.

4.4.3 Switching waveforms

This section presents waveforms captured during switching events to illustrate the action of the three gate drives. Figs. 4.10a and 4.10b show the turn-on waveforms for S1 and S2 respectively when operating with the FGD at the maximum power

point identified from Fig. 4.8a (334 V, 22.3 A). The voltage peak across the diode is within the 430 V limit, since the dc-bus voltage is relatively low.

The corresponding switching waveforms for the VR-AGD at its maximum power operating point are the same as for the FGD, as discussed above, so are not shown. Instead, the VR-AGD turn-on waveforms (Figs. 4.10c and 4.10d) are shown at the maximum power point of the PP-AGD (396 V, 20.4 A), for comparison against the PP-AGD waveforms (Figs. 4.10e and 4.10f). This is *not* the VR-AGD's maximum power operating point: it is outside its SOR. The rate of collector current increase is slower for the VR-AGD than for the PP-AGD. This has a two-fold effect on the switching loss: it takes longer for the diode to become reverse biased and allow the collector-emitter voltage to fall (longer switching time); and the collector-emitter voltage is depressed less by the voltage drop across the parasitic inductance of the commutation path. Both factors lead to 1.5 mJ of switching loss, which causes the unacceptably high calculated junction temperature for the VR-AGD. The PP-AGD, in contrast, reduces voltage overshoot while achieving a lower switching loss of 0.76 mJ. The PP-AGD's extra degrees of freedom allow independent control of the collector current rise and the decay of the diode reverse recovery current. This means that the collector current can increase rapidly at first (reducing switching loss), and the peak $\frac{\mathrm{d}i}{\mathrm{d}t}$ when the reverse recovery current decays can be reduced (creating smaller voltage overshoot).

4.5 Discussion

The AGD techniques investigated here, compared with gate drives that switch as fast as possible, can reduce the peak voltage across the power devices and allow the converter to be operated at higher dc-bus voltages. However, only the more advanced AGD, the PP-AGD, is found to increase the switch power handling capability. On the other hand, the simpler VR-AGD results in higher switching losses which limit the switch power capacity. The VR-AGD is similar to a gate drive where the rate of gate charge/discharge is controlled by a series gate resistance that is varied between, but not during, the switching events. These results indicate that a variable gate

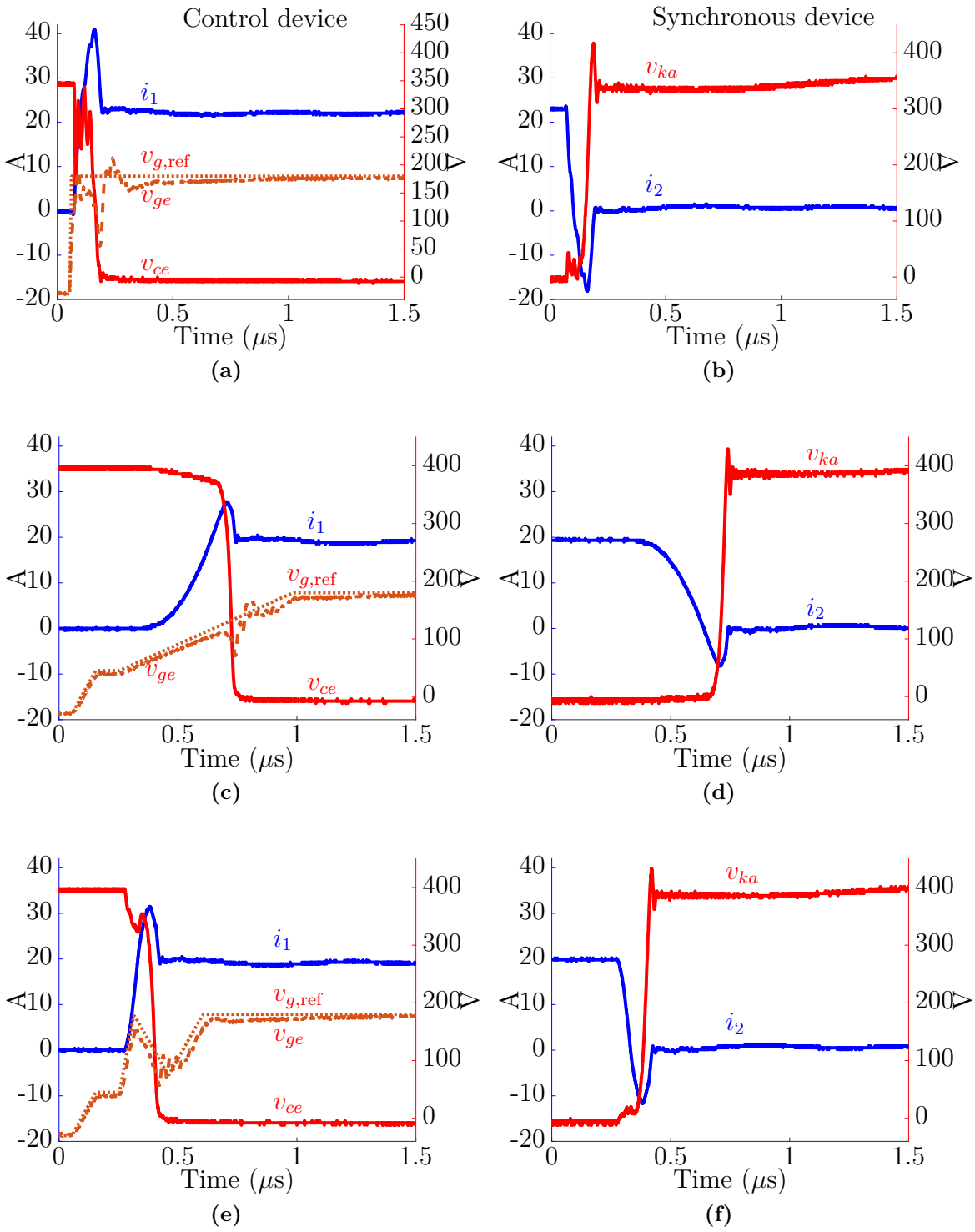


Figure 4.10: Turn-on waveforms when switching with the three gate drives. (a-b) FGD at 334 V 22.3 A, (c-d) VR-AGD at 396 V 20.4 A, and (e-f) PP-AGD at 396 V 20.4 A. The variables plotted here correspond to those shown in the circuit schematic of Figure 4.2. The FGD and PP-AGD plots are from the respective maximum apparent power operating points for those gate drives, and illustrate acceptable switching behaviour. The VR-AGD plots illustrate the VR-AGD keeping voltage overshoot below the 430 V limit but incurring a high switching loss.

resistance alone has limited utility, and cannot increase switch capacity. The better performance of the PP-AGD suggests that there is merit in a more advanced gate drive compared to the simpler option of implementing an adjustable gate resistance.

It should be recognised that the PP-AGD formulation of the gate drive is not necessarily the best possible, and there may be more complex gate waveforms that achieve greater performance improvements. The PP-AGD as presented here was chosen as a good trade-off between complexity (number of parameters to tune, i.e. experiment run-time) and control over switching behaviour. The theory here has been validated for a single device in a particular converter layout. It is expected that the benefits of AGD will be greater for layouts with large parasitic inductance between dc-link capacitors and the power switches. Conversely, careful power circuit layout reduces the problem of peak transient voltage and reduces the need for AGD.

The procedure for finding the best reference waveform during operation is not considered here. The exhaustive search for $\mathbf{x}^*$ conducted here results in switching voltage overshoot that sometimes exceeds the device limit, and it is only the choice of a conservative limit that makes this approach possible. It is necessary in practical systems to search in a way that does not violate the peak voltage constraint.

The exact moment when the load current commutates between the switching devices depends on the variable $\mathbf{x}$. Therefore, for synchronous switching the deadtime between the 'on' PWM signals for two devices in a leg may need to be increased to guarantee the absence of shoot-through for all $\mathbf{x}$. Use of an adaptive deadtime mechanism such as that proposed in [95] could address this. Similarly, the duty cycle of the switched device will vary slightly with $\mathbf{x}$ as the instant of switching changes. However, the effect of this is small: the maximum variation in on-time observed during experiments is less than 1 µs, causing duty cycle to vary by less than 1 % when switching at 10 kHz.

The AGD can be thought of as providing 'free silicon' by increasing the capacity of a given switch, meaning either more power can be processed by the same device, or a smaller device can be chosen to process a particular power level. The better switch utilization may imply higher converter power density if the power semiconductor

devices and their heat-sinks significantly contribute to the overall volume of the converter. This would have to be factored against the additional volume and weight of the AGD hardware compared to a conventional gate drive.

4.6 Conclusion

In this chapter, the first framework for evaluating the impact of an active gate drive on the power processing capability of an IGBT is proposed. The power capacity of the device is experimentally shown to increase by up to 8 % at frequencies between 4 and 8 kHz (Fig. 4.9) when using the PP-AGD in a buck converter. The AGD method enables operation of a given converter at increased dc-link voltages by limiting the voltage overshoot and enlarging the safe operating area of the device (Figs. 4.8 and 4.10). Consequently, the application of AGD may result in increased utilization of the power semiconductor device.

5

Obtaining high switching speeds with SiC MOSFETs

This thesis so far has focused on the problem of transient peak voltage across the power semiconductors due to the parasitic inductance of the power loop. The decay of the reverse-recovery current was shown to be the cause of the highest peak voltages. The low reverse-recovery charge of SiC MOSFETs raises the prospect of negligible transient voltage overshoot during switching, when the commutation current path is designed to have minimal parasitic inductance. The absence of transient voltage overshoot opens the possibility for very fast switching with the goal of reducing the switching energy loss.

This chapter begins by reviewing the switching speeds of SiC MOSFETs published in the literature. The design of a fast-switching bridge-leg is then presented, including the role of the gate drive in facilitating high switching speeds. This is followed by experimental results demonstrating that it is possible to obtain higher switching speeds, and lower switching energy losses, than are currently being obtained in publications of SiC switching behaviour.

5.1 Published switching speeds of SiC MOSFETs

It is commonly accepted that the faster switching speed of wide band-gap (WBG) devices makes it increasingly important to control parasitic inductances and capacitances of the power converter. Indeed, many of the issues reported with WBG devices such as ringing, EMI, and transient voltage stress often arise when WBG devices are inserted in place of slower-switching devices (e.g. Si IGBTs) without making appropriate changes to reduce parasitics in the circuit. It then becomes necessary to mitigate these effects by artificially slowing the switching using a large gate resistor to increase the gate charge/discharge time. Therefore the potential of these devices to reduce switching loss remains unexploited.

Awareness of this has led to attempts to control the converter parasitics, at the level of the device [96, 97], module [98, 99], PCB [100], bus-bar [101], and passive components [102]. For example, careful layout of SiC MOSFET dies and signal routing within a half-bridge power module has reduced the module commutation inductance to <1.4 nH [98]. In [100], four PCB layout options for GaN flip-chip packages are compared and a 30 % reduction in commutation inductance is observed between the worst and best layout.

The result of these efforts to reduce parasitic inductance and capacitance is that higher rates of change of current and voltage are obtainable when switching. The rate of change of MOSFET drain-source voltage is often used as a measure of the MOSFET's switching speed. In the large number of published papers related to SiC MOSFET switching, most demonstrate drain-source voltage slew rates of a few tens of volts per nanosecond. Table 5.2 presents a selection of publications and lists the voltage slew rate obtained in the work. The wide range of slew rates is due to variations between the driven MOSFETs, different gate driving techniques, and different converter operating conditions and layouts. Only one publication demonstrates >100 V/ns switching [93], where a resonant driver is used. Here, current in the gate-loop inductance is built up before turn-ON, and switching is then triggered by directing the current into the gate of the power device [103]. This can rapidly charge the gate capacitances of the SiC MOSFET (eliminating delays

normally introduced by the gate-loop inductance) and obtain fast switching, but adds complexity to the driver and limits the range of duty cycles obtainable.

Non-resonant approaches to rapid charging/discharging of the SiC MOSFET gate are restricted to reducing the gate resistance [93], or increasing the supply voltage, in the case of voltage-source gate drives, or increasing the supply current in the case of current-source drives [104]. A lower limit to the gate resistance is set by the internal gate resistance of the device. This resistance arises from the distribution of the gate signal across the MOSFET die via the aluminium metallization and polycrystalline silicon gate network. The smaller die area of SiC MOSFETs, compared to Si devices of similar rating, increases the internal gate resistance and makes it an important factor limiting the rate of gate charging/discharging. In devices with low die area, the internal gate resistance can be as high as 25 Ω [105]. In this case, reducing the gate resistance outside the device package/die has limited effect on switching speed.

Increasing the turn-ON gate drive voltage, and reducing the turn-OFF voltage, are alternative means to charge/discharge the MOSFET gate more quickly. Multi-level gate drives have been proposed [48, 50] as a way of 'boosting' the gate charging voltage during particular stages of the switching transient, and it is shown to increase the drain-source voltage slew rate. However, the obtained slew rate (∼40 V/ns) is still markedly smaller than that obtained with a resonant gate drive (∼120 V/ns).

The maximum gate-source voltage of a MOSFET is determined by the breakdown strength of the gate oxide layer. SiC MOSFETs tend to have a thinner gate oxide layer than Si MOSFETs, in order to compensate for the lower channel mobility under the SiC MOSFET gate due to interface defects, and obtain comparable transconductance [107]. The thin oxide means the critical electric field strength in the oxide is reached at lower gate-source voltages in SiC MOSFETs than in Si MOSFETs, an issue returned to in Section 5.6.

A concern about the high slew rate of the switched-node voltage is that it can trigger 'false turn-ON', i.e. turn-on of the MOSFET that should be OFF because of the transient current path through the drain-gate capacitance, leading to a shoot-through current and increased switching loss [108–111]. Negative gate-source

Reference	Device	$\frac{\mathrm{d}v_{ds}}{\mathrm{d}t}\|_{\mathrm{on}}$ (V/ns)	$\frac{\mathrm{d}v_{ds}}{\mathrm{d}t}\|_{\mathrm{off}}$ (V/ns)	Comments
Tripathi [46]	10 kV	57		Custom gate drive, R_g =10 Ω
Dymond [44]	C3M0065090J	48		AGD varying R_g
Anthony [93]	CMF10120D	62	57	
		123		Resonant drive
Oswald [43]	CMF20120D	11	19	IXDN609SI driver, R_g =12 Ω
Ji [106]	10kV-20A Cree	82	50	
Zhang [48]	Cree 1200-V/20-A	42	31	Multi-level AGD
Camacho [49]			4.8	
Nayak [50]	1200V 35A SCH2080KE		16	Multi-level AGD

Table 5.2: Selected papers demonstrating switching of SiC MOSFETs at various drain-source voltage slew rates. Specific MOSFET models are given where known, otherwise the device rating is provided. Only the resonant gate drive in [93] obtains a >100 V/ns slew rate.

bias to hold the MOSFET off (increasing margin between hold-off and threshold voltages) ameliorates this, however a low-resistance pull-down path (sometimes called a 'miller clamp') is also essential to suppress false turn-on in [110]. Similar mitigation against negative gate-source voltage spikes is proposed in [112].

5.2 Experimental methodology

The experiment here demonstrates the switching speed possible with current state-of-the-art discrete SiC MOSFETs. The design of the power circuit (Section 5.2.1), gate drive (Section 5.2.2), and measurement method (Section 5.2.3) are detailed with emphasis on the considerations for high switching speed.

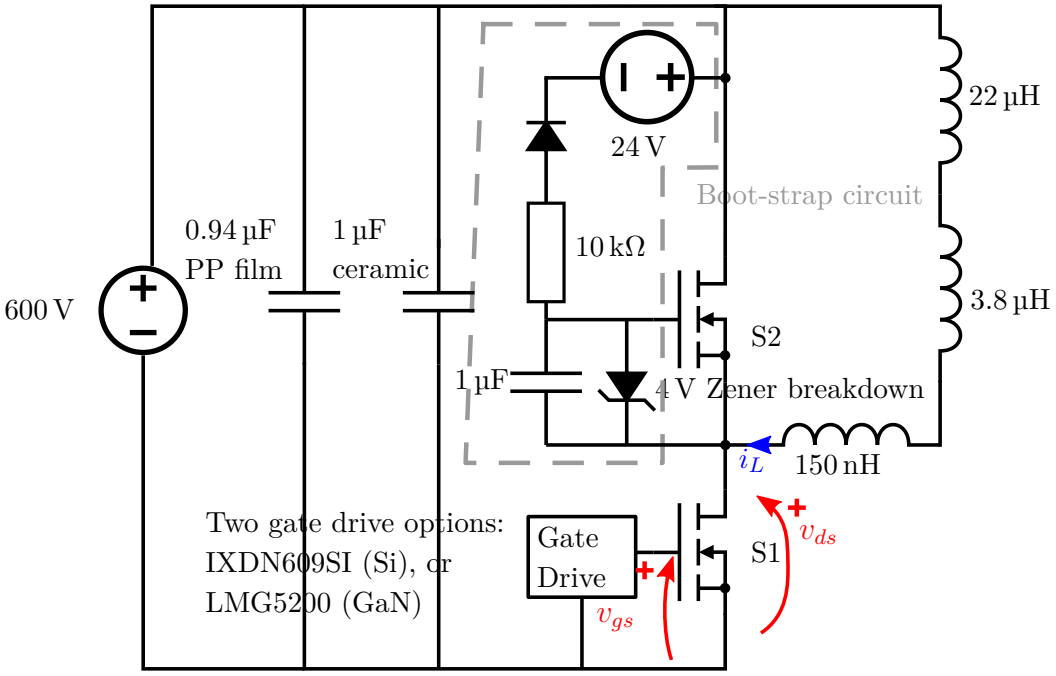


Figure 5.1: Schematic of the double-pulse circuit used in experiment. Switch S2's v_{gs} is held at $-4\,\text{V}$ by the Zener diode and isolated dc-dc converter (boot-strap circuit explanation in Section 5.2.2)

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5.2.1 Power circuit design

The SiC MOSFET switching behaviour is evaluated in a circuit designed to create the fastest switching edges possible. As before, the bridge-leg is the circuit investigated here. The leg is symmetric with identical MOSFETs used for the upper and lower switches. Thus the leg is representative of the general-purpose half-bridge which can both supply and sink current from its switched-node.

The classic double-pulse test is used to characterise the bridge-leg. In this configuration the load is on the high-side so that the lower MOSFET S1 is the actively driven switch and the upper MOSFET S2 is the synchronous switch (Fig. 5.1).

The MOSFETs (Cree C3M0120090J) are 900 V 120 mΩ devices in the TO-263-7 (D2PAK) package. This package offers better transient performance than any other package commercially available for chip-scale SiC MOSFETs (e.g. TO-220, TO-247, TO-247-4) because it provides a dedicated kelvin source pin for the gate drive (reducing coupling between the power circuit and gate circuit) and low power terminal inductances. The wide drain pad avoids the inductance inherent in package

leads, and the paralleling of five source leads reduce the source inductance to $\leq$3 nH (compared to $\geq$10 nH for the TO-220 package) [113].

The power circuit board (Fig. 5.2) is laid out so that the principle of flux cancellation minimises the parasitic inductance of the commutation current loop. The PCB has four layers with 35 µm copper thickness and 220 µm vertical spacing of FR4 between outer layers (i.e. a standard low-cost PCB). Schematics of the top layer (Fig. 5.3a) and Layer 2 (immediately below the top layer, Fig. 5.3b) illustrate the flux cancellation. The load current path when S1 is ON is marked (1) and shown in blue: current is supplied by the dc-link capacitors, flows through the high-side load, into the switched-node, though S1, and returns through Layer 2 to the dc-link capacitors. The path of the freewheeling current, when S1 is OFF, is marked (2) and indicated in green. The solid lines indicate the path section where the current is constant during the switching transition; the dashed lines indicate the path sections that the current commutates between during switching. Only the path marked with the dashed lines contributes to the parasitic inductance since only those sections undergo $\frac{\mathrm{d}i}{\mathrm{d}t}$. Most of the magnetic flux associated with the current in the commutating path is cancelled by the return current flowing in the adjacent layer. Some parasitic flux still exists due to the 220 µm spacing between the opposing currents, the section between the drain pad and source leads of S2 where no opposing current flow exists, and the current concentration though the MOSFETs, vias, and ceramic capacitors.

The capacitance of the switched-node is charged and discharged in the course of every switching cycle, and the rate of charging/discharging determines the slew rate of the switched-node voltage, as described in Chapter 1. The largest contributors to the switched node capacitance are listed in Table 5.3.

The capacitance between the switched-node copper on the top layer and the ground plane underneath can be approximated as

$$C = \frac{A\epsilon_r\epsilon_0}{t} = 28\,\mathrm{pF} \tag{5.1}$$

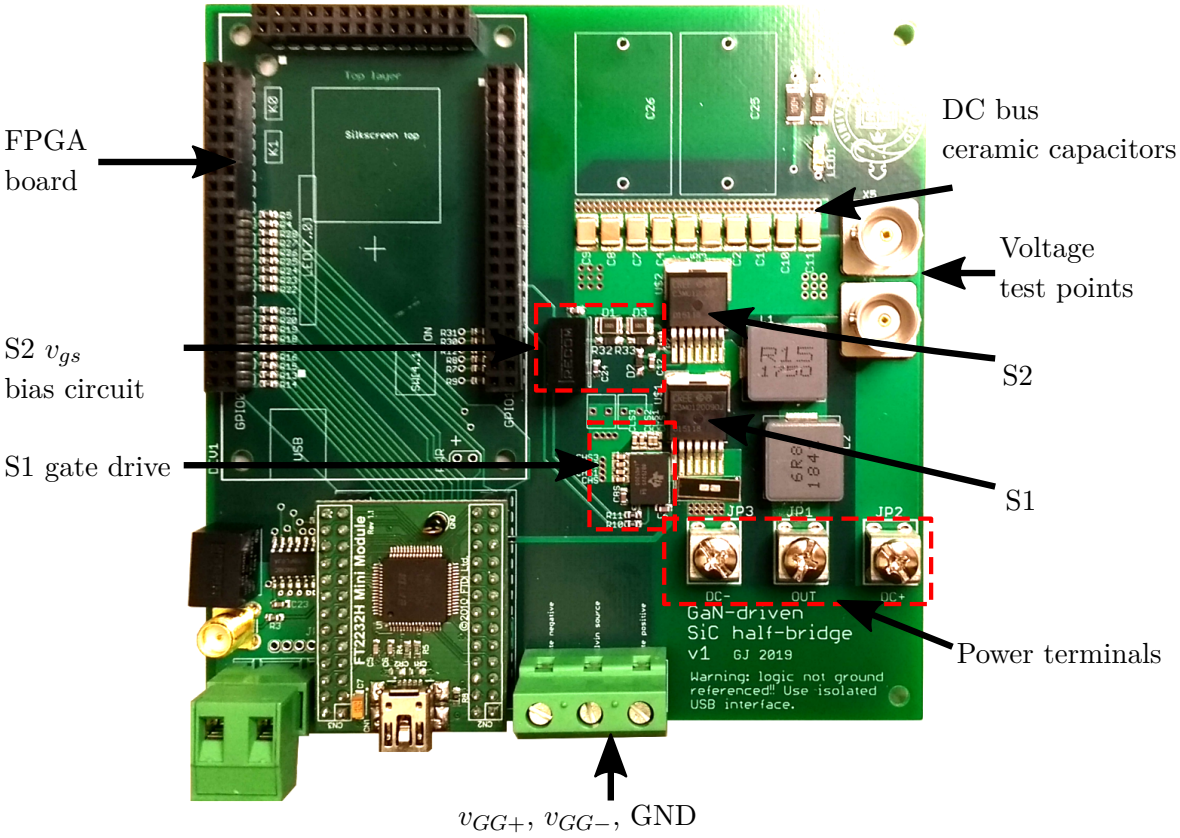


Figure 5.2: The half-bridge showing SiC MOSFETs, gate drive, and output inductors.

Component	Capacitance (pF)	
C_{oss}	55	per MOSFET at $v_{ds} = 300\,\mathrm{V}$
PCB overlap	28	
Voltage probe	6	
Filter inductor	≤ 4	150 nH inductor
Total	148	Both MOSFETs at $v_{ds} = 300\,\mathrm{V}$

Table 5.3: Components contributing to switched-node parasitic capacitance.

where the area A of the switched-node copper is $1.6\,\mathrm{cm}^2$, FR4 relative permittivity ϵ_r is 4.4, and plate spacing t is the layer separation of 220 µm.

An approximate value for the inter-winding parasitic capacitance C_L of the filter inductor is found from the series resonant frequency of the inductor

$$C_L = \frac{1}{(2\pi f_0)^2 L} = 4\,\mathrm{pF} \tag{5.2}$$

where resonant frequency f_0 is 210 MHz and inductance L is 150 nH. Taking this value as the load parasitic capacitance is a worst-case: the 3.8 µH and 22 µH series inductors reduce the equivalent load parasitic capacitance. Nevertheless, the

4 pF capacitance estimated for the single inductor is much smaller than the other components of the switched-node parasitic capacitance.

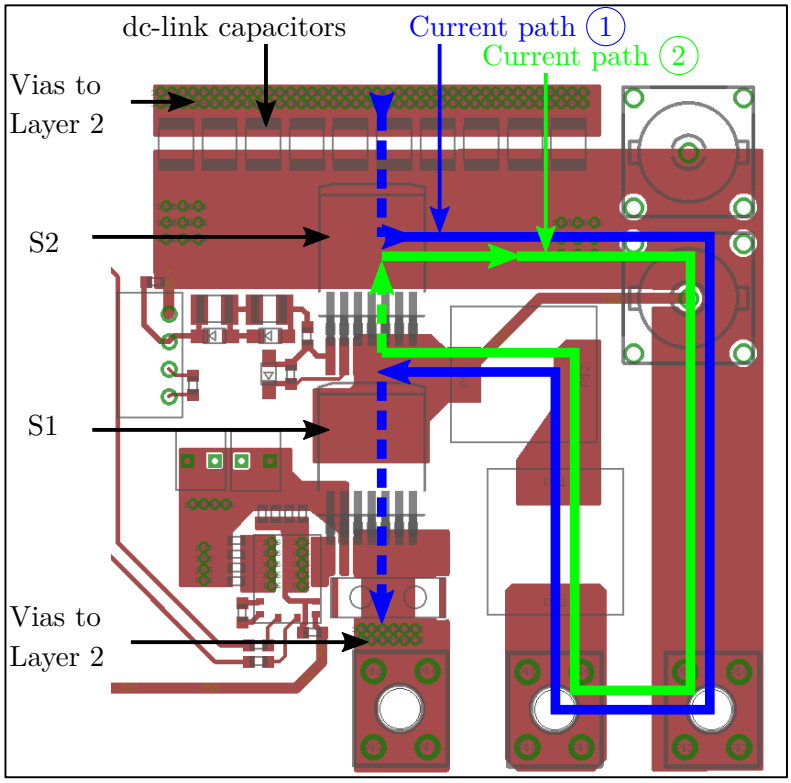
Although MOSFET C_{oss} is the biggest contributor to switched-node capacitance, the PCB inter-layer capacitance comprises 20% of the total capacitance and it is important to keep reasonably small. As evident in Fig. 5.3a, the switched-node area is reduced as much as possible given the clearance required by the device packages, and keeping the current paths wide to reduce parasitic inductance. The filter inductors are also placed close to the MOSFETs to reduce the switched-node capacitance.

5.2.2 Gate drive design

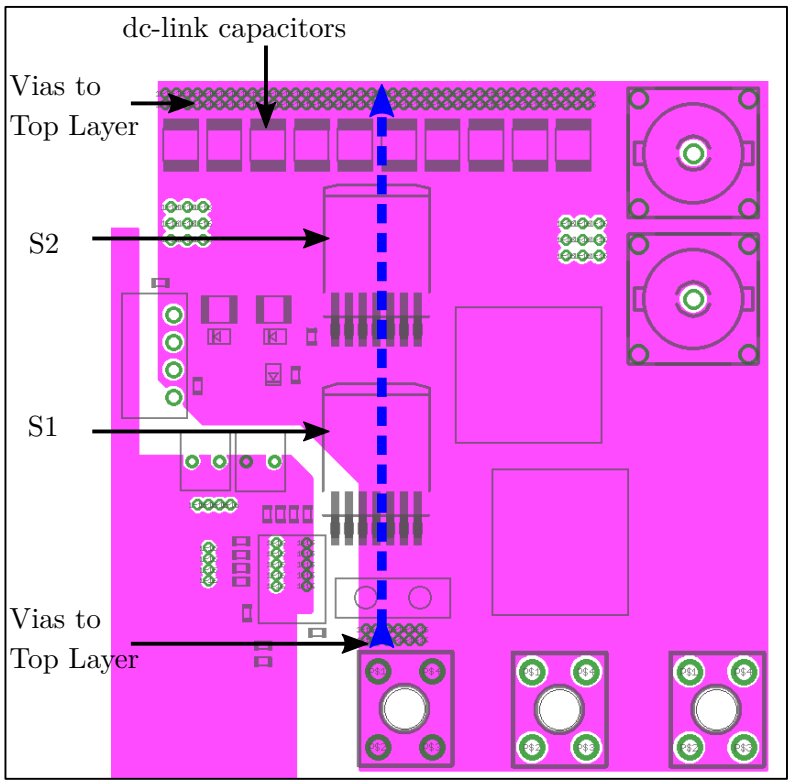
Active switch S1 is driven using a conventional two-level voltage gate drive technique, where the gate drive voltage rails V_{GG+} and V_{GG-} are supplied by an adjustable bench power supply and are referenced to the kelvin source of S1. The effect of the gate drive voltage on the switching is assessed by varying the bench power supply output during switching.

Two gate driver integrated circuits (ICs) are investigated. The first is the IXDN609 from Ixys Corporation. This is a dedicated MOSFET driver and is recommended by Cree Inc. for driving their C3M family of SiC MOSFETs. (The IXDN609 IC is used in Cree's CGD15SG00D2 gate driver board [114, 115].) This is therefore the reference driver. The pull-up resistance is 2 Ω and the pull-down resistance is 1.5 Ω (from the datasheet). The second driver is the LMG5200 from Texas Instruments. This contains two GaN n-type FETs in a half-bridge configuration, with integrated gate drivers for the FETs. The driver FETs are each 15 mΩ, 80 V devices. This driver is expected to provide particularly fast charging/discharging of the SiC MOSFET gate, and hence allow fast switching, due to the low-resistance of the driver FETs and the low output capacitance of the GaN material.

The use of GaN devices to drive SiC MOSFETs has recently been investigated due to their capability for high output voltage slew-rate [116–118], and have been



(a)



(b)

Figure 5.3: Extract from PCB layout highlighting load current paths on (a) top layer and (b) layer 2. Flux associated with the commutation path (dashed lines) is mostly cancelled by the opposing current flowing in the adjacent layer. Solid lines show the steady-state current path (not commutating during switching).

applied at high switching frequencies (10 MHz and 40 MHz in [117] and [118], respectively). These works use discrete GaN devices. The use of integrated GaN-based half-bridges to drive SiC MOSFETs appears to be a novel concept, likely because these GaN half-bridge ICs have only recently become commercially available. The attraction of an IC compared to discrete devices is twofold: the parasitics in the gate path can be minimised by tight integration of the components, and the single IC provides ease of use for converter designers. The LMG5200 investigated here is not ideally suited to this application since it is rated for 80 V, however it is the most suitable component available at the time of writing. A lower rated (e.g. 30 V) half-bridge could obtain a lower pull-up/down resistance for the same output capacitance. The gate drive ICs are positioned close to MOSFET S1 to reduce inductance in the gate loop. Two parallel arrays of ceramic capacitors provide a low-inductance split-supply for the gate drive ICs.

Switch S2 is held-OFF during the switching transient. The high slew-rate of the switched-node voltage raises concerns about parasitic turn-on of S2. To ensure that S2 remains OFF, v_{gs2} is held at -4 V by a low parasitic capacitance bias circuit (Fig. 5.1). This gate bias circuit uses the 4 V breakdown voltage of a Zener diode to clamp v_{gs2}. An external 'bootstrap' 1 µF gate-source capacitor is charged to -4 V by an isolated dc-dc converter when S2's body diode is forward biased and the switched-node voltage is one diode-drop above V_{dc}. When S1 is ON and the switched-node voltage is low, the gate of S2 is de-coupled from the 600 V dc bus by two blocking diodes in series. The two diodes are in series to limit the parasitic capacitance added to the switched-node. They each have a depletion capacitance of less than 1.2 pF when reverse biased by more than 30 V, so in series they add only 0.6 pF of equivalent capacitance to the switched-node for the majority of the switched-node's voltage range. This compares favourably with the lowest achievable isolation capacitances of high-side gate drive transformers [119]. In a converter with bidirectional output current it would be necessary to implement a low-capacitance gate-drive to turn S2 ON, however in this work the focus is on demonstrating fast switching of S1 and the implemented bias circuit for S2 enables this.

5.2.3 Measurement methods

Slew rate of the switched-node voltage (i.e. S1's drain-source voltage v_{ds}) is one metric used to define the switching speed. This is measured with a 300 MHz 100:1 passive probe. Another probe (of same type) measures the dc bus voltage across the bridge-leg, and the drain-source voltage of S2, v_{ds2}, is inferred from the difference between these two signals. The signals are probed at the BNC test points visible in Fig. 5.2. The voltage between the gate and kelvin source pins on S1's package is measured by a 1 GHz 10:1 passive probe directly touching the package pins. All signals are sampled at 3 GSPS by oscilloscope with 1 GHz bandwidth (Tektronix MSO54).

The load current is measured at the output power terminal with a 100 MHz hall-effect probe (Keysight N2783A). The measurement of the MOSFET drain currents requires a high-bandwidth signal path for accurate measurement (at least $\sim$ 300 MHz for the expected $\sim$ 3 ns rise-times of the current signals [85]). Furthermore the parasitic inductance introduced by the measurement circuit to the power loop should be as small as possible to avoid degrading the switching behaviour. Several publications review the techniques available for measuring switching currents in power electronics [85, 120–124]. The cutting-edge in non-invasive current sensing of wide band-gap switches is a 225 MHz bandwidth sensor with 0.2 nH insertion inductance, resembling a planar Rogowski coil, presented in [120]. This 'infinity sensor' is installed adjacent to the source of S1, visible in Fig. 5.2. However the sensor was not used in results that follow, and only the voltage waveforms are presented.

5.3 Switching waveforms

Waveforms illustrating the switching behaviour are shown in this section, where markers on the waveforms indicate the oscilloscope sample points. The magnitude of the positive gate drive voltage V_{GG+} has a strong effect on the turn-ON fall in drain-source voltage. Figs. 5.4a and 5.4c show the gate-source and drain-source voltage of S1 respectively, when switched with the IXDN609 driver with

$V_{GG+} \in \{15\,\text{V}, 16\,\text{V}, 17\,\text{V}, 18\,\text{V}, 19\,\text{V}, 20\,\text{V}, 21\,\text{V}, 22\,\text{V}\}$. Large V_{GG+} (plotted in red) speeds up the fall in v_{ds}, and also brings the onset of the voltage-fall phase earlier, compared to smaller V_{GG+} levels (plotted in blue). The corresponding waveforms for switching with the LMG5200 driver (Figs. 5.4b and 5.4d) show the same trend with rising V_{GG+}. Two phases are visible in the fall of v_{ds}: initially the voltage falls relatively slowly, until reaching a distinct knee-point after which the voltage rapidly falls. The initial drop in voltage is likely due to the load current commutating through the parasitic inductance, with the knee-point indicating when the current commutation has completed.

Figs. 5.4e and 5.4f show a magnified view of the windowed regions of the preceding plots. Waveforms for $V_{GG+} \in \{15\,\text{V}, 22\,\text{V}\}$ are shown for both LMG5200 and IXDN609 drivers. The gate is charged faster and has higher overshoot when driven by the LMG5200 IC compared to the IXDN609 IC. This difference in the gate charging rate between the drivers is apparent in the current-commutation drop of v_{ds}, which is larger and of shorter duration for driving with the LMG5200 than with the IXDN609. This suggests that the shorter rise-time of the LMG5200 driver is causing a faster rise in the drain current. The fall in v_{ds} after the knee-point is similar for both drivers.

Gate-source and drain-source waveforms for turn-ON under a range of load currents ($I_L \in \{5\,\text{A}, 6\,\text{A} \ldots 20\,\text{A}\}$) are shown in Figs. 5.5a and 5.5c for the IXDN609 driver and Figs. 5.5b and 5.5d for the LMG5200 driver, all at a single gate drive supply voltage ($V_{GG+} = 15\,\text{V}$). The knee-point of v_{ds} occurs earlier at lower load currents, corroborating the idea that it represents the point at which the current-commutation has completed. After the knee-point, v_{ds} falls more quickly at low load currents (plotted in blue) than at high load currents (plotted in red). This can be explained by the miller-plateau voltage increasing with switched current, such that there is less voltage drop across the gate resistance to drive current into the gate at high load currents (see Section 1.5 equation (1.11)).

Turn-OFF behaviour is unaffected by changing the driver and the supply voltage V_{GG+}. Turn-OFF with the IXDN609 (Figs. 5.6a and 5.6c) produces the same

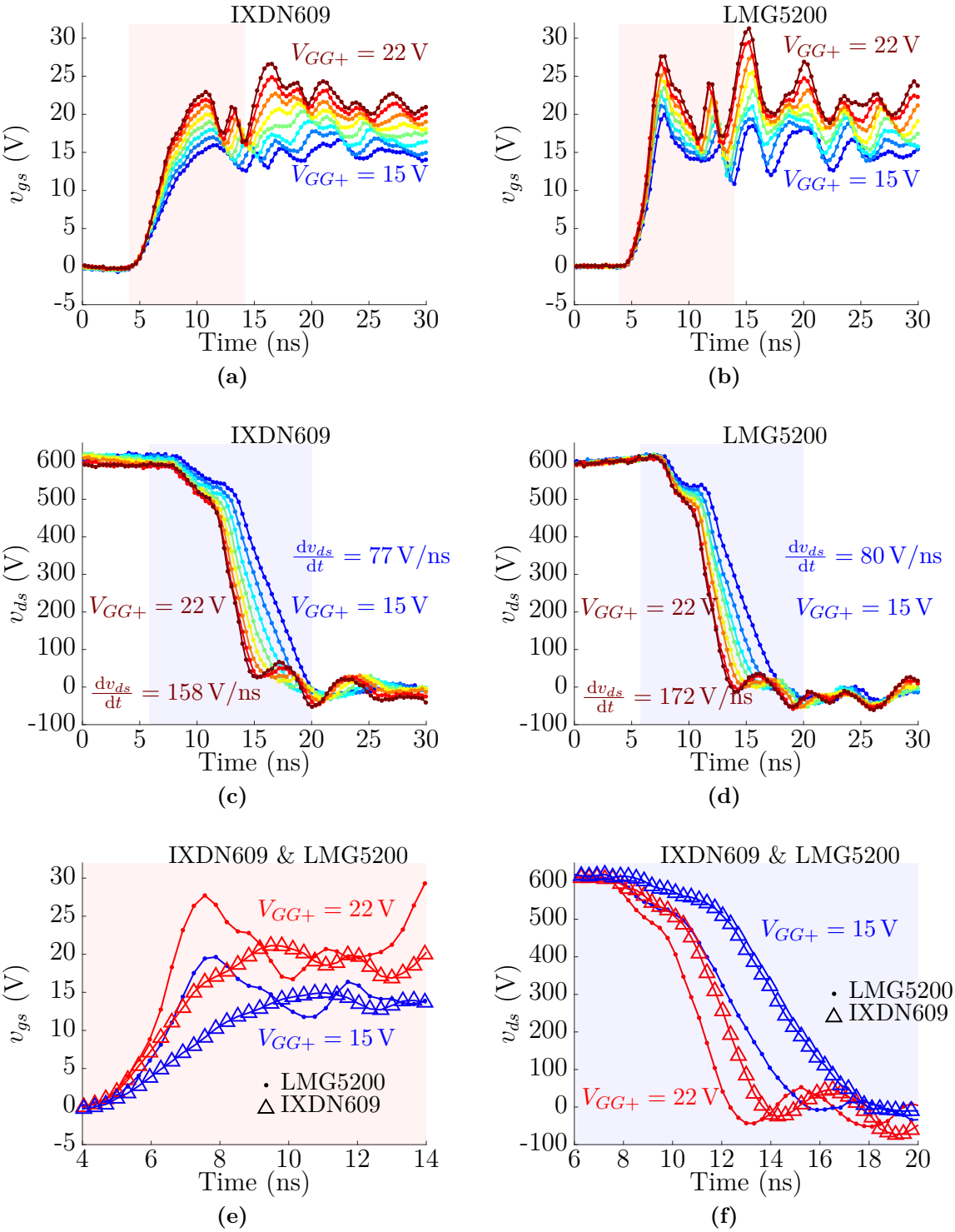


Figure 5.4: Varying gate drive voltage and its affect on turn-ON drain-source voltage. I_L =20 A. (a,c) IXDN609 driver, (b,d) LMG5200 driver. Gate drive on-state voltage V_{GG+} 15 V-22 V. The windowed area of (a) and (b) is expanded in (e) for two V_{GG+} for each driver. Similarly the windowed area of (c) and (d) is expanded in (f).

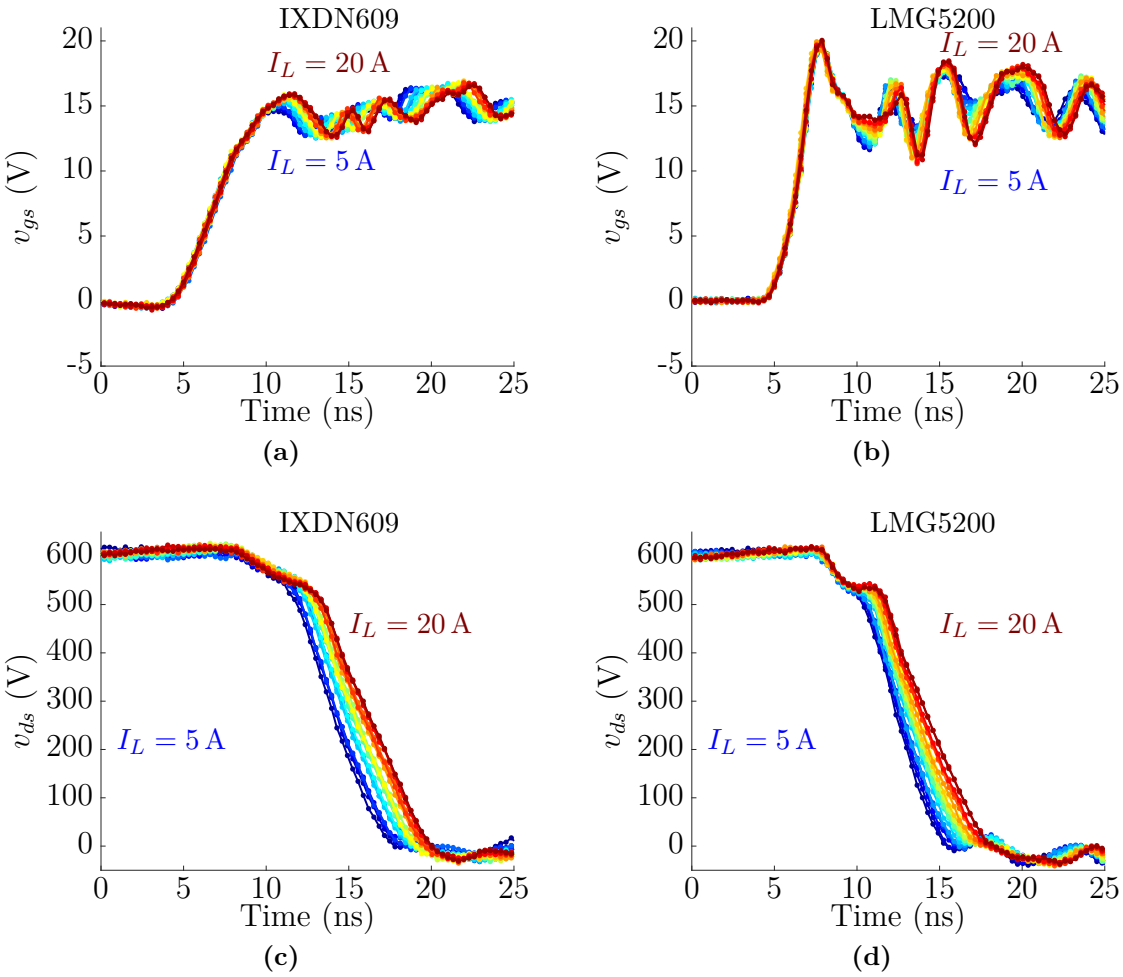


Figure 5.5: Varying load current and its effect on turn-ON behaviour. Gate-source and drain-source voltage when switching with (a,c) IXDN609 driver, and (b,d) LMG5200 driver. Load current varying from 5 A to 20 A. Gate drive on-state voltage V_{GG+} 15 V.

drain-source voltage profile as when switched with the LMG5200 driver (Figs. 5.6b and 5.6d), despite the faster discharge of the gate in the LMG5200 case. The switched current is 20 A in these figures.

Waveforms for turn-OFF under a varying load current are shown in Figs. 5.7a and 5.7c for the IXDN609 driver and Figs. 5.7b and 5.7d for the LMG5200 driver. Slew-rate of the drain-source voltage is determined only by the load current since the switched-node capacitance is charged by this current.

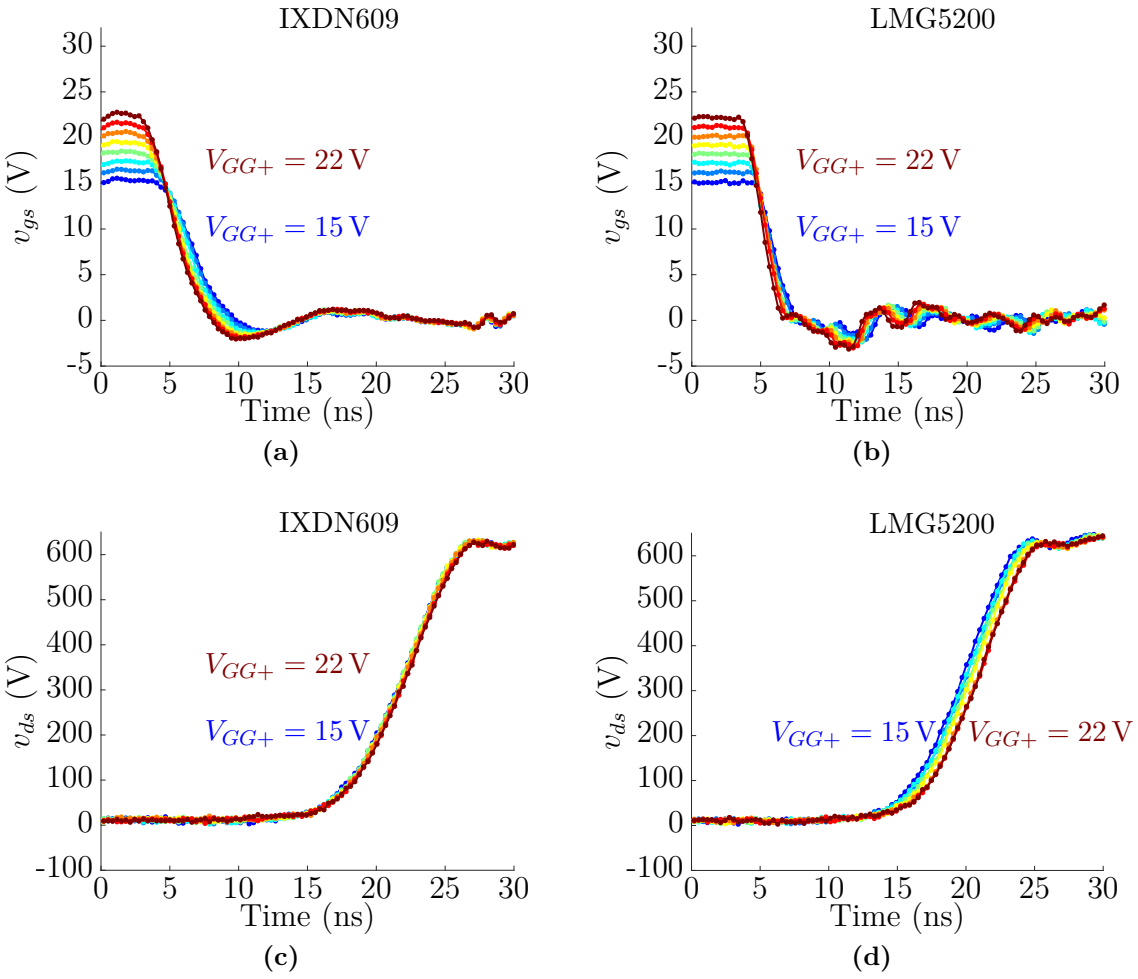


Figure 5.6: Varying gate drive voltage has no effect on the turn-OFF rise of drain-source voltage. I_L =20 A. (a,c) IXDN609 driver, (b,d) LMG5200 driver. Gate drive on-state voltage V_{GG+} 15 V-22 V.

5.4 Measured voltage slew-rate

Voltage slew-rate during turn-ON is calculated for the rapid fall in v_{ds} occurring after the current-commutation knee-point. The slew-rate calculation is performed on the voltage data within the range

$$0.2V_{dc} < v_{ds} < 0.7V_{dc}\,, \tag{5.3}$$

where the 20 % and 70 % thresholds are chosen to exclude voltage ringing at low v_{ds}, and the current-commutation voltage drop at high v_{ds}, respectively.

The magnitude of the voltage slew rate during turn-ON is shown in Fig. 5.8a for the IXDN609 IC and Fig. 5.8b for the LMG5200 IC. Drive voltage levels

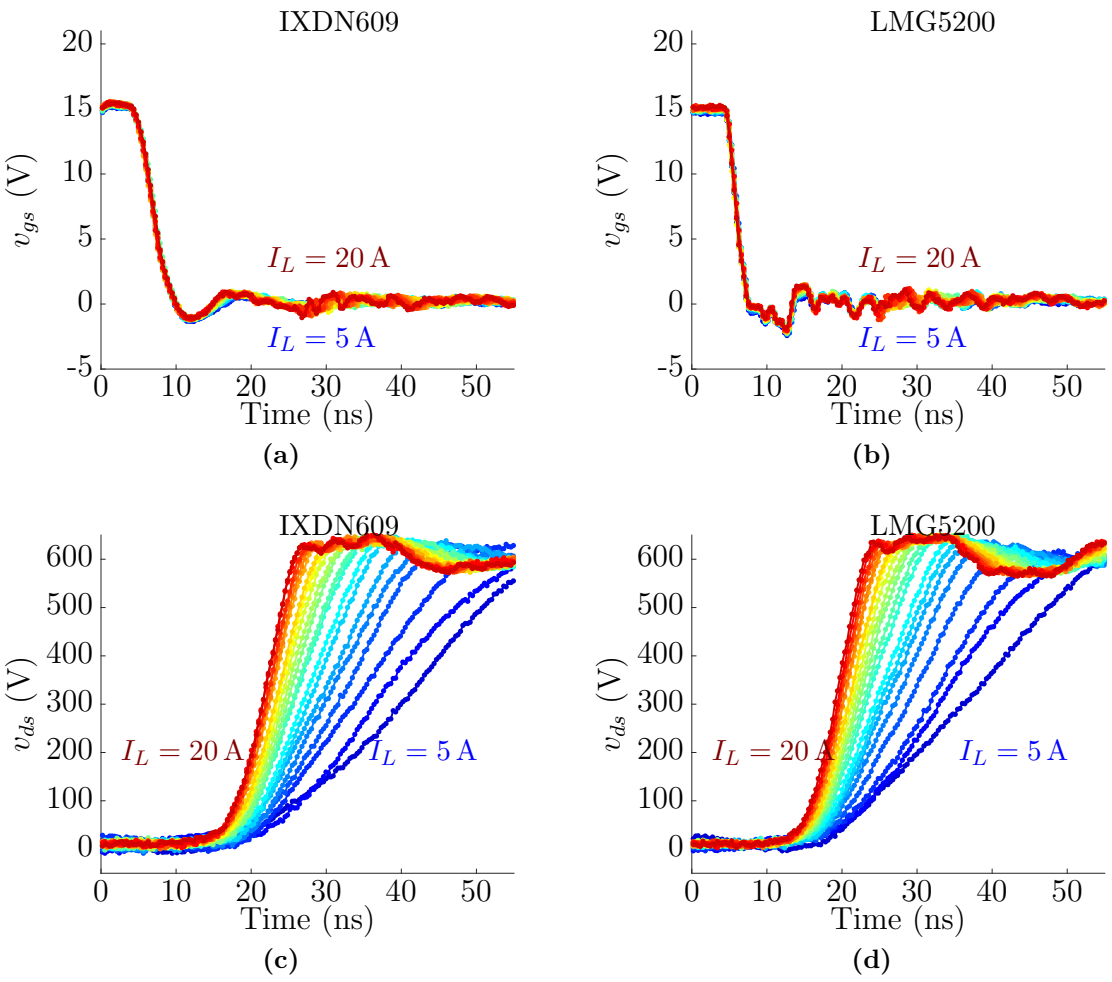


Figure 5.7: Load current is the main influence on turn-OFF drain-source voltage slew-rate. Gate-source and drain-source voltage when switching with (a,c) IXDN609 driver, and (b,d) LMG5200 driver. Load current varying from 5 A to 20 A. Gate drive on-state voltage V_{GG+} 15 V.

$V_{GG+} \in \{15\,\mathrm{V}, 16\,\mathrm{V} \ldots 22\,\mathrm{V}\}$ are plotted in a colour range from blue (15 V) to red (22 V). The dependence of turn-ON v_{ds} slew-rate on drive voltage level is clear, as is the relationship to the switched load current. Fig. 5.8c plots slew-rate for both drivers for selected drive levels ($V_{GG+} \in \{15\,\mathrm{V}, 22\,\mathrm{V}\}$). The LMG5200 IC obtains a small increase in slew-rate above the IXDN609 IC, for both drive levels across the load current range, although this is not obvious from looking at the v_{ds} waveforms for 20 A load current of Fig. 5.4f. By operating at a drive voltage level of 22 V, a v_{ds} slew-rate in excess of 170 V/ns is obtained by the LMG5200 driver across the current range.

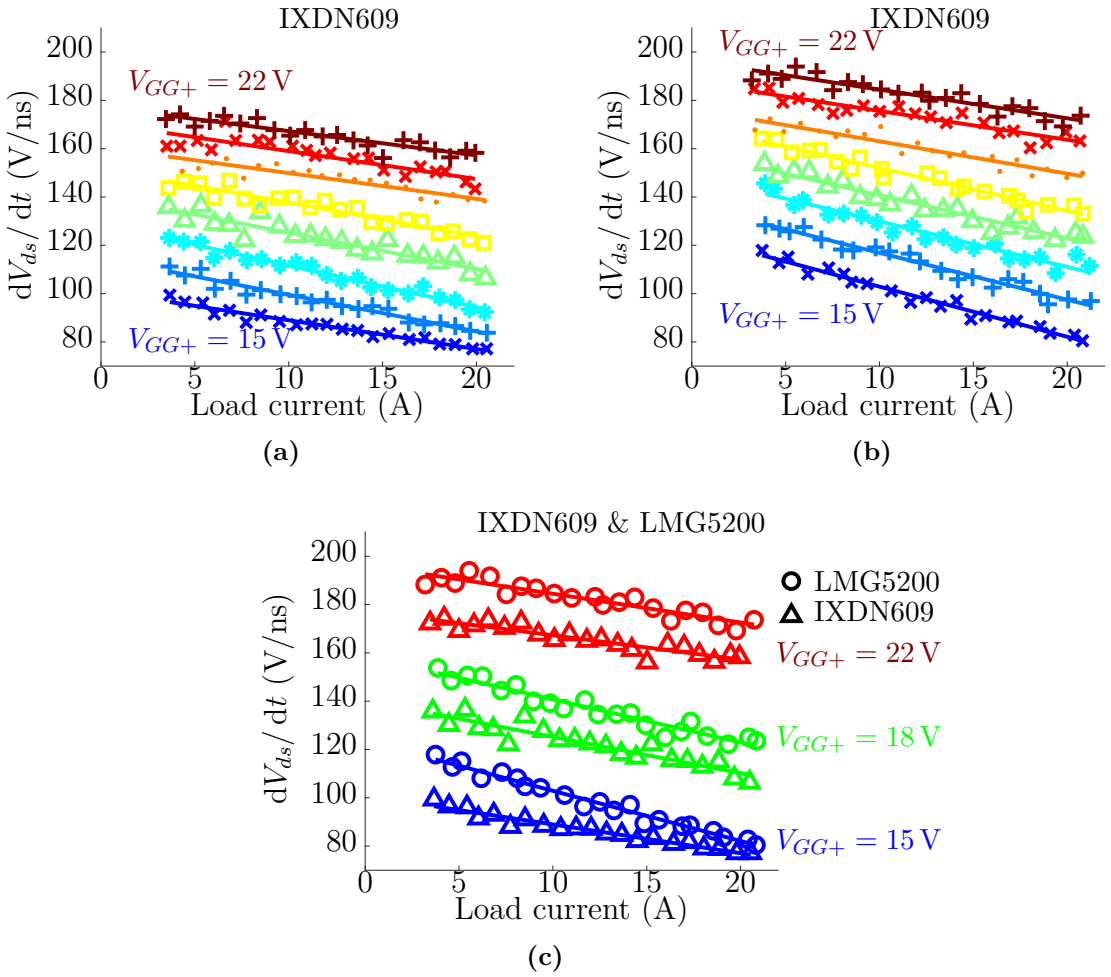


Figure 5.8: Turn-ON drain-source voltage slew rate as a function of load current and gate drive voltage. (a) IXDN609 Si driver IC, and (b) LMG5200 GaN driver IC, for $V_{GG+} \in \{15\,\mathrm{V}, 16\,\mathrm{V} \ldots 22\,\mathrm{V}\}$. (c) Both driver ICs for $V_{GG+} \in \{15\,\mathrm{V}, 22\,\mathrm{V}\}$.

The turn-OFF v_{ds} slew-rate (Fig. 5.9) depends greatly on the load current, and the gate drive has little influence since this transient is driven by the load current charging the switched-node capacitance.

5.5 Estimate of switching loss

The turn-ON switching loss can be estimated by taking the small inductive drop in the v_{ds} waveform as an indication of when the load current begins to commutate. Then, assuming a linear rise in drain current, from (1.20) we have

$$E_{on} = \frac{1}{2} I_L V_{dc} \left(t_2 - t_1\right) , \tag{5.4}$$

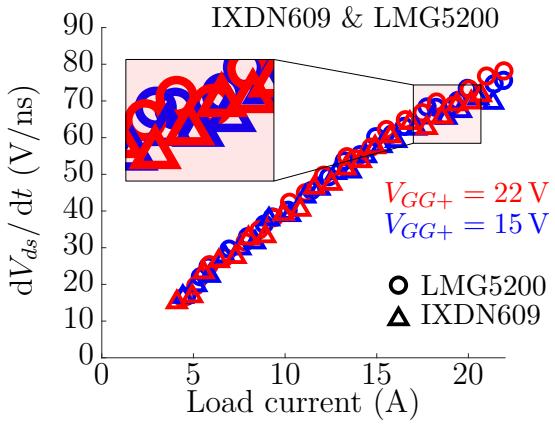


Figure 5.9: Turn-OFF drain-source voltage slew rate is a function of load current, not gate drive.

Driver	V_{GG+} (V)	E_{on} (µJ)	% change
IXDN609	15	61	0
LMG5200	15	56	-8
IXDN609	22	38	-38
LMG5200	22	32	-48

Table 5.4: Comparison of estimated turn-ON switching losses under different drive conditions at a load current of 20 A. Percentage change in loss relative to the IXDN609 driver at $V_{GG+} = 15\,\mathrm{V}$.

where load current I_L is taken from the inductor current waveform immediately before switching, t_1 is the time when v_{ds} starts to drop below the bus voltage V_{dc}, and t_2 is the time when v_{ds} has fallen to approximately 0 V.

The estimated turn-ON loss is shown in Figs. 5.10a and 5.10b for the IXDN609 and LMG5200 drivers, respectively. Larger V_{GG+} (red markers) leads to lower switching loss, as expected given the v_{ds} slew-rate findings. The two driver ICs are directly compared in Fig. 5.10c for drive voltage levels $V_{GG+} \in \{15\,\mathrm{V}, 22\,\mathrm{V}\}$. The increase in drive voltage from 15 V to 22 V reduces the estimated turn-ON energy loss from 56 µJ to 32 µJ for the LMG5200 driver at 20 A load current, a reduction in loss of 43 %. The difference in loss between the two drivers operating at the same voltage level is smaller (e.g. 61 µJ for the IXDN609 IC compared to 56 µJ for the LMG5200 IC at $V_{GG+} = 15\,\mathrm{V}$, an 8 % difference). Table 5.4 compares the estimated losses at 20 A load current.

This estimate is based on the assumption that the drain current of S1 rises

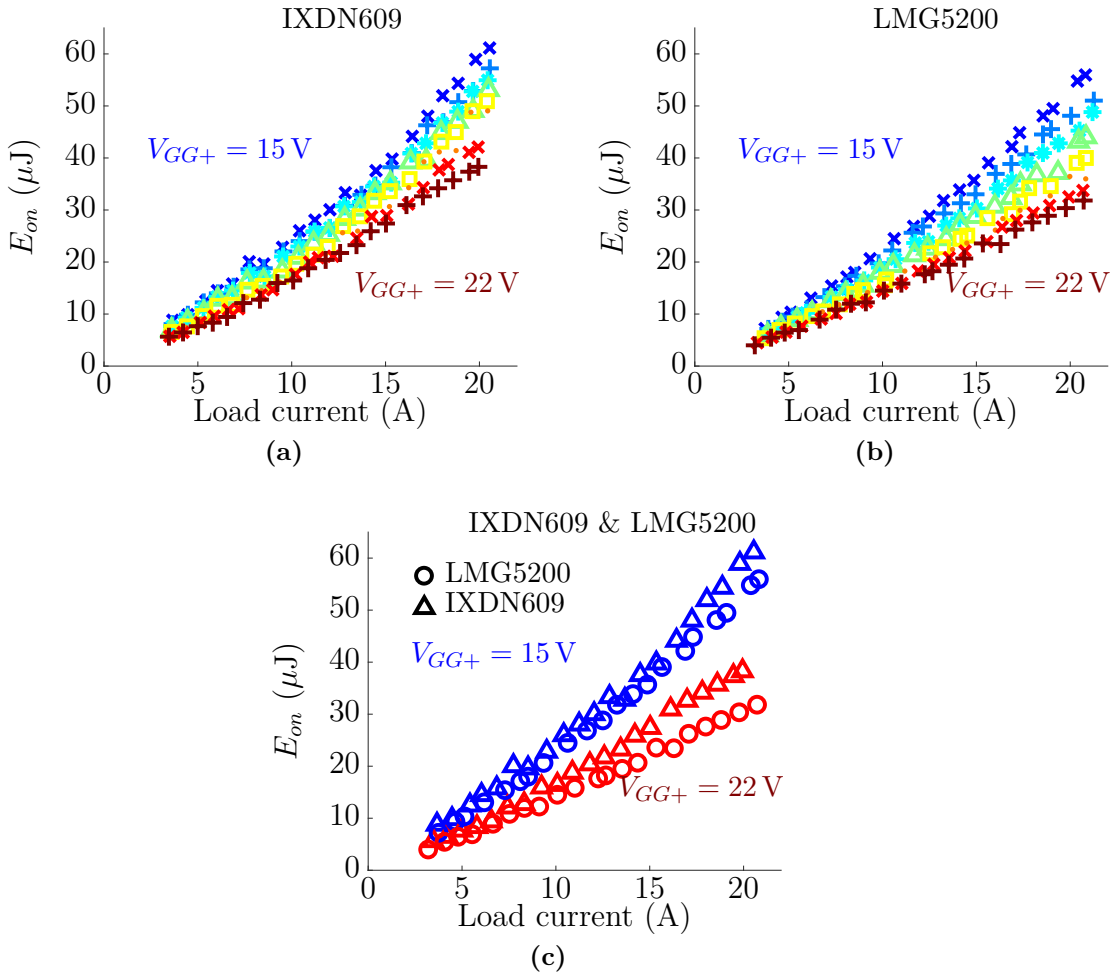


Figure 5.10: Estimated turn-ON switching loss from (5.4), for (a) IXDN609 driver, and (b) LMG5200 driver for $V_{GG+} \in \{15\,\mathrm{V}, 16\,\mathrm{V} \ldots 22\,\mathrm{V}\}$. (c) Both driver ICs for $V_{GG+} \in \{15\,\mathrm{V}, 22\,\mathrm{V}\}$.

linearly. In fact, it is evident from the shape of the inductive drop of v_{ds} that the drain current does not rise linearly (v_{ds} falls with a gradual ramp rather than a step, especially for switching with the IXDN609). Therefore the true switching loss is expected to be somewhat smaller than the approximation indicates.

5.6 Discussion

The findings in this chapter are consistent with the simple theory of MOSFET switching presented in Section 1.5. Specifically, the higher drain-source voltage slew-rate at higher gate drive voltages is qualitatively predicted by (1.11), as is

the observed higher drain current slew-rate and drain-source voltage slew-rate for lower gate drive resistance.

The resistance of the gate network inside the C3M0120090J MOSFET (i.e. the bond-wire and aluminium / polycrystalline silicon mesh distributing the gate signal on-chip) is reported to be 16 Ω [125]. Therefore the total turn-ON gate loop resistance with the LMG5200 IC as a percentage of that with the IXDN609 IC is

$$\frac{16\,\Omega + 0.015\,\Omega}{16\,\Omega + 2\,\Omega} = 90\,\%\,. \tag{5.5}$$

This corresponds to the ∼10 % higher drain-source voltage slew-rate when switching with the LMG5200 compared to the IXDN609 IC. In other words, the switching speed is only a weak function of gate driver resistance when the total gate loop resistance is dominated by the MOSFET internal gate mesh resistance. This poses an upper limit to the switching speed of the SiC MOSFETs with high internal gate resistance. It is not clear why the drain-source voltage slew rates for the two drivers converge at high load currents when the drive voltage is 15 V (as seen in Fig. 5.8c). This is perhaps due to the smaller margin between the drive voltage and the miller-plateau voltage at this combination of high load current and relatively low drive voltage, such that the miller-plateau voltage becomes equal to the drive voltage when v_{ds} is falling rapidly (due to the additional channel current required to discharge the switched-node capacitance).

The remaining mechanism to obtain fast switching is to increase the gate drive voltage. This is shown here to have a strong effect on switching speed (i.e. an approximate doubling in drain-source voltage slew-rate with an increase in drive voltage from 15 V to 22 V). The disadvantage of this approach is the reduction in lifetime due to greater electric field stress across the gate oxide. Making predictions of gate oxide lifetime/reliability is complicated by dependency on temperature, manufacturing processes, and the need to separate the effects of multiple different failure modes [126–129]. A trade-off between reliability and switching loss could be found by using a multi-level gate driver which applies a high (e.g. 22 V) voltage to the gate for a short period during switching to rapidly charge the gate, before

reducing to a steady hold-ON voltage (e.g. 15 V) to eliminate the gate oxide's high electric field stress. For example, the waveforms in Fig. 5.4a suggest that the high gate charging voltage would only need to be applied for 10 ns or less to charge the gate during each turn-ON transient, so that at 100 kHz switching the gate oxide would be exposed to the high electric field for only 0.1 % of the time.

It is also evident from Fig. 5.8 that the gate drive voltage level could be adaptively set to compensate for the variation in drain-source voltage slew-rate as the load current changes. The data suggest that an approximate 2 V increase in gate drive voltage would be required obtain the same v_{ds} slew rate when switching 20 A as when switching 5 A. This could be a useful tool for situations where a constant output voltage slew rate is desirable, such as automotive motor drives where the switched-node is directly connected to the electrical machine and control over voltage slew-rate is necessary to avoid exciting resonances in the machine windings [53].

5.7 Conclusions

The design of a fast-switching SiC bridge-leg was outlined in the chapter. The effect of the gate driver resistance and gate drive voltage level on turn-ON switching speed was investigated. An integrated GaN FET half-bridge driver was proposed to provide fast charging of the SiC MOSFET gate with no added external gate resistance. Waveforms show that this driver charges the gate-source voltage at the MOSFET package leads in approximately half the time than a commercial driver IC.

This reduced charging time of the MOSFET gate corresponds to a ∼10 % increase in drain-source voltage slew-rate. A larger influence on the voltage slew-rate is the gate drive voltage level, with a peak slew-rate of 180 V/ns observed when over-driving the gate with a 22 V supply. No peak transient voltages significantly above the dc bus were observed, despite the high switching speed. This indicates that these high slew-rates might be achievable in practice, raising the possibility of a ∼40 % reduction in switching energy loss.

6 Conclusions and further research

This thesis has explored how effective use of the gate drive can increase transistor power capacity and reduce switching losses. The capability of active gate drives (AGD) to control peak transient voltages when switching was demonstrated, and the practical implications on power processing capability were assessed experimentally. This chapter summarises the contributions of this thesis, and indicates areas where further research is needed.

6.1 Contributions of this thesis

6.1.1 Mapping the voltage-energy trade-off using AGD

It is well established in the literature, reviewed in Chapter 2, that the switching energy loss is inversely correlated to the peak transient voltage when hard-switching IGBT and MOSFET bridge-legs, and that the energy loss can be traded against the peak transient voltage by controlling the switching speed using the gate drive.

Chapter 3 of this thesis identifies that the highest transient voltage in the bridge-leg appears across the terminals of the synchronous device as it turns off (i.e. as the control device turns on). This transient voltage is caused by the rapid decay of the synchronous device's reverse-recovery current in conjunction with the parasitic inductance of the circuit. A simple model is developed to

provide insight into the mechanism by which the speed of current-commutation influences the peak transient voltage. The contribution made here is to introduce an AGD which can operate in several different modes, and to develop a systematic method of assessing the performance of the different modes. Extensive data is gathered to map the peak voltage and switching energy loss as a function of the gate drive waveform parameters.

The AGD modes differ in the number of degrees of freedom that they provide in constructing the IGBT gate waveform. The proposed Variable-ramp AGD (VR-AGD), Double-ramp AGD (DR-AGD), and Push-pull AGD (PP-AGD) modes have one, two, and three degrees of freedom, respectively. Noting that the number of possible gate waveforms increases with each additional degree of freedom, it is important to identify the value added by each degree of freedom.

A key finding of this work is that the PP-AGD, being able to remove as well as provide charge to the control device's (IGBT) gate during turn-ON, can obtain greatly reduced switching loss compared to the simpler VR-AGD and DR-AGD (17 % lower loss when peak voltages are constrained to 260 V). The removal of charge from the IGBT gate allows the control device's collector-emitter voltage to briefly rise as the synchronous device recovers, thereby sharing the peak voltage stress between the two semiconductor devices and reducing the stress on any individual device. This demonstrates the potential utility of such gate drives.

6.1.2 A framework for assessing switch power capacity using AGD

Chapter 4 assesses whether the AGD control of peak voltage and switching loss can increase the power throughput of a converter. Based on the observation that the use of AGD can permit operation at higher dc bus voltages (since AGD reduces peak transient voltage compared to fast-switching) but at reduced output currents (since AGD increases switching loss), a framework is proposed for finding the dc bus voltage and load current which maximises device output power.

This framework is based on measuring switching behaviour over a range of gate drive inputs across a grid of dc bus voltage and load currents. An automated procedure is outlined for this, and the results indicate that a small increase in output power can be achieved when using the PP-AGD compared to fast-switching. The increase in output power demonstrated in these experiments when using PP-AGD is approximately 8 %.

6.1.3 The limitations of simple AGDs

An important finding of this work is that the simpler VR-AGD does not improve on fast-switching because the prohibitively large increase in switching loss from this AGD severely limits the output current. This suggests that implementing a variable gate drive resistance that only varies *between* switching transitions (does not vary during the transition), will not yield any performance improvement in terms of power throughput. This is significant since such a gate drive would only have one variable to optimise over and so would be relatively much more simple to implement than gate drives which present a drive voltage/resistance that varies over the duration of the transient. Unfortunately the results presented here suggest that such a scheme would be of little benefit for increasing device power capacity.

6.1.4 The potential of gate voltage boosting for reduced losses

Chapter 5 considers a SiC MOSFET bridge-leg with minimal parasitic inductance, where the objective of tailoring the gate drive is to obtain high slew-rates and reduce switching loss, rather than mitigate peak transient voltage. A high turn-ON drain-source voltage slew-rate is achieved by careful design of the power and gate circuits.

Furthermore, the resistance of the gate driver circuit and the gate drive supply voltage level were both investigated to assess their influence on the switching speed. It was found that the gate drive resistance has only a small effect on the switching speed of SiC MOSFETs where the dominant resistance in the gate loop is the internal gate resistance of the power device. A novel application of an integrated

GaN FET-based half-bridge IC to drive the SiC MOSFET gate resulted in a faster rise of gate-source voltage (measured on the MOSFET package leads) but only led to a ∼10 % increase in switching speed.

However, an large increase in drain-source voltage slew-rate was demonstrated by increasing the gate drive supply voltage. At the rated load current (22 A) and recommended gate drive voltage (15 V) a drain-source voltage slew-rate of 80 V/ns was observed. This increased to 180 V/ns when driven with a gate voltage of 22 V. The corresponding reduction in turn-ON switching loss is estimated to be 40 %.

As an example of the possible impact of this on overall efficiency, consider an application where the energy efficiency is 95 % when switching with a gate supply voltage of 15 V, the losses being equally divided between switching loss and conduction loss. All other factors being equal, by increasing the gate voltage to 22 V the 40 % reduction in switching loss would correspond to an increase in overall efficiency to 96.5 %. This significant improvement in efficiency indicates the potential of boosting the SiC MOSFET gate voltage.

6.1.5 The importance of layout and minimising parasitics

The problem of transient peak voltage across the synchronous device, which is mitigated using AGD techniques in Chapters 3 and 4, is caused fundamentally by the combination of the abrupt change in the synchronous device's reverse-recovery current and the parasitic inductance of the power-loop layout. The experiments discussed in Chapter 4 were conducted on a bridge-leg with a relatively high parasitic inductance in the commutation current loop of approximately 160 nH. This accentuated the transient voltage overshoot and created the opportunity for AGD to improve performance by controlling the overshoot.

The results of Chapter 5 showcase the advantage of tightly integrating the passive components and the power switches to reduce parasitic inductance in the commutation current path. When optimizing a converter, therefore, the layout should be kept in mind from an early stage. Before the use of AGD is considered, the layout parasitic inductance should be minimised as much as is reasonably practical.

However it is often not possible to achieve such tight integration in practice, for several reasons:

1. Heat removal from the power semiconductor devices may pose a limit to how densely the components can be packed. For example, adding a heat-sink to the lower (control) MOSFET in the experiment of Chapter 5 would require re-routing the return current within the PCB in order for vias to connect the control MOSFET's drain pad to the underside of the PCB. This would reduce flux cancellation and add parasitic inductance, and the heat-sink would add capacitance to the switched-node.

2. Designers might choose to not install dedicated high-frequency-response capacitors close to the power switches for decoupling the switching transients from the dc bus. In this case, the bulk dc-link capacitors (often large film or electrolytic capacitors with high equivalent series inductance) have to supply the pulsed current to the switching leg. These bulk capacitors might be far away from the switching leg due to space constraints or because they support a dc bus that is shared between several physically-separate converters. The decoupling capacitors might be omitted to reduce the bill of materials, to improve reliability by avoiding the use of ceramic capacitors near to the switches (which would experience thermal cycling stress), or to avoid ringing between the bulk and decoupling dc-link capacitors which can lead to self-heating and destruction. I found during experiments that the ringing between bulk and decoupling capacitors destroyed the ceramic decoupling capacitors, a problem mitigated by reducing the distance (therefore inductance) between the bulk and the decoupling capacitors.

3. If a current measurement of the switching leg is needed, the current-shunt or probe insertion loop adds further parasitic inductance.

4. At high power levels, power devices are operated in parallel, often in power modules. The packaging of modules adds parasitic inductance. Despite module

manufacturers focusing on reducing parasitic inductance in the modules, some parasitic inductance remains [99].

It is for reasons such as these that converters often have significant parasitic inductance and experience problems with high peak voltages. In these cases, the results in this thesis suggest that the application of AGDs to manage transient voltages is promising.

However, the demonstrated performance gains are modest for AGD, in terms of increasing IGBT power capacity. The small increase in switch capacity when using AGD does not automatically justify the additional cost and complexity incurred. This in itself is a contribution of this thesis: despite the large reduction in peak transient voltage from using AGD (which is widely reported in the literature), here we show that it is in fact rather challenging to obtain a practical benefit from this effect. One area where AGD might find application is in megawatt-scale wind turbine power converters, where an increase in power capacity of 8 % would correspond to a large additional revenue, and the alternative means of increasing the power capacity (i.e. buying higher-voltage rated devices) is costly.

6.2 Future work

6.2.1 Automated generation of optimised gate waveforms

The procedure for finding the optimal AGD waveforms has not been addressed in this thesis. Rather, in this work the optimal gate waveforms have been selected based on a 'brute-force' approach where waveforms from a large set are exhaustively trialled and finally the best is selected. An intriguing challenge lies in finding the optimal gate waveforms 'online', i.e. during operation of a practical converter.

As the operating conditions change, the gate drive must adapt the gate waveform, so the speed of adaptation must be suitable for tracking the changes in load current. For example, for an inverter switching at 50 kHz and supplying sinusoidal output current at 50 Hz, the load current can change by up to 1.3 % of the peak value

between two switching transitions. Therefore the gate drive algorithm must be able to adapt within a small number of transitions.

A particular challenge when finding the optimal gate waveform is to avoid violating the constraint on peak transient voltage. When operating near the rated maximum voltage of the semiconductors, use of an inappropriate gate waveform could result in a peak transient voltage which causes the power converter to fail. There has been little research attention on this topic to date. Related work [63, 70] assumes a voltage limit somewhat below the device's actual rating to avoid damage during experiments when the peak voltage exceeds the limit. It is crucial that this problem be solved if AGDs are to be implemented as investigated here.

6.2.2 The relevance of AGD to devices with no reverse-recovery

The results demonstrating increased power capacity in this thesis are based on mitigating peak voltage induced across circuit parasitic inductance due to *pin* diode reverse-recovery. The reverse-recovery behaviour is a major disadvantage of these high voltage Si diodes, and is a motivation for the use of SiC Schottky-barrier diodes (SBDs) that do not exhibit noticeable reverse-recovery behaviour [130].

Use of SiC SBDs eliminates the reverse-recovery peak voltage, so that the turn-OFF peak voltage across the control switch becomes the factor limiting the maximum operating voltage. In this case, an AGD which is able to control the turn-OFF transition (not demonstrated here) would be of interest for increasing switch power capacity. The existence of a similar trade-off between turn-OFF peak voltage and switching loss is expected (based on the considerations in Sections 1.6 and 1.7). The framework and methodology presented here for evaluating the impact of AGD on switch power capacity could be adapted to assess the potential for turn-OFF control to increase the power capacity.

This would be a valuable study as SiC SBDs become more widespread. Currently, Si *pin* diodes are still often used due to their low cost, especially in low switching-

frequency applications, and in these applications the AGD control demonstrated here can still help to mitigate the effect of reverse-recovery peak voltage.

6.2.3 Validation of gate voltage-boosting results and reliability implications

The reduction in switching loss by increasing the gate drive voltage level, demonstrated in Chapter 5, was determined using electrical measurements of drain-source voltage and load current. Using a calorimetric method to measure the difference in MOSFET loss at different gate drive voltage levels would provide further evidence about the reduction in energy loss.

Provided this calorimetric method corroborated the results obtained by electrical measurements, the implications of increasing the gate-source voltage on the reliability of the gate oxide should be investigated. Development of a multi-level gate drive to allow a high 'charging' voltage followed by a lower 'hold-on' voltage to be applied to the MOSFET gate would enable extended lifetime tests to be performed under different levels of gate oxide stress.

6.2.4 Gate waveform shaping for rapid charging

A special case of the gate voltage-boosting concept proposed in Chapter 5 would be to generate a shaped waveform to rapidly charge/discharge the MOSFET gate in such a way that the voltage across the gate oxide never exceeds the rated voltage. Detailed knowledge both of the impedance between the gate driver and the SiC die, and of the impedance of the gate mesh network within the die, could be used so that the applied 'excess' voltage (that above the 'hold-on' level) is dropped over the external gate loop impedance instead of across the gate oxide. In this way the impedance between the gate driver and the die could be overcome without the gate oxide being exposed to high electric field stress.

For example, Fig. 6.1a models the path between the gate driver and the SiC die as resistive and inductive (from package pins, PCB traces, and bond-wires), and the gate signal distribution on the die surface as resistive and capacitive. Fig. 6.1b

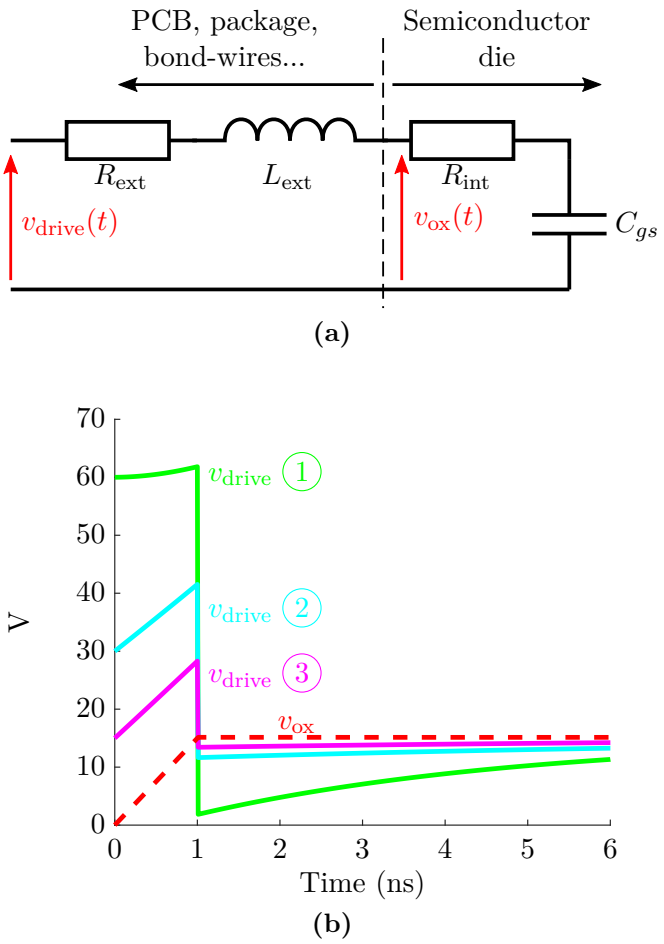


Figure 6.1: Given a model of the gate charging path (a), the drive voltage can be tailored to obtain rapid gate charging without any voltage overshoot across the gate oxide (b). The three inputs of v_{drive} produce the same controlled ramp of oxide voltage v_{ox} for different values of the circuit elements in (a). Values for case (1): $R_{\text{ext}} = 0.03\,\Omega$, $L_{\text{ext}} = 16\,\text{nH}$, $R_{\text{int}} = 4\,\Omega$, $C_{gs} = 1\,\text{nF}$. Values for case (2): $R_{\text{ext}} = 0.03\,\Omega$, $L_{\text{ext}} = 16\,\text{nH}$, $R_{\text{int}} = 8\,\Omega$, $C_{gs} = 1\,\text{nF}$. Values for case (3): $R_{\text{ext}} = 0.03\,\Omega$, $L_{\text{ext}} = 8\,\text{nH}$, $R_{\text{int}} = 8\,\Omega$, $C_{gs} = 1\,\text{nF}$.

shows the drive voltage waveforms $v_{\text{drive}}(t)$ required to raise the gate oxide voltage $v_{\text{ox}}(t)$ to 15 V within 1 ns, for three example scenarios each with different values for the circuit impedances. The three inputs of v_{drive} produce the same controlled ramp of oxide voltage v_{ox} for different values of the circuit elements in Fig. 6.1a.

A challenge in implementing this idea is obtaining an accurate model for the gate circuit, in particular the gate network on the SiC die. The gate network on the die would be better represented by a distributed network of resistive and capacitive elements, rather than the single lumped RC network in the simple example given.

Characterising this network in detail would probably require cooperation from device manufacturers in providing data about the gate layout on the die.

A further challenge is in generating the appropriate gate drive voltage signal. It is possible that an approximation to a profile like v_{drive} (1) in Fig. 6.1b could be generated by a small-valued capacitor, pre-charged to several tens of volts, being discharged into the SiC MOSFET gate.

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