Hole-selective SiN_x and AlO_x Tunnel Nanolayers for Improved Polysilicon Passivating Contacts

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Abstract: A highly efficient hole-selective passivating contact remains the crucial step required to increase the efficiency of polysilicon-based Si solar cells. The future development of solar modules depends on a device structure that can complement the electron-selective Tunnel Oxide Passivating Contact (TOPCon) with an equivalent hole-selective contact. We investigate Plasma Enhanced Chemical Vapour Deposited (PECVD) SiN_x and Atomic Layer Deposited (ALD) AlO_x as alternative nanolayers for the passivation layer in polysilicon tunnel contacts. We have fabricated p^+ poly-Si contacts with resistivities below 100 $m\Omega \cdot cm^2$ using these alternative metal oxide and nitride nanolayers. Initial passivation tests yielded low levels of passivation; however, a detailed understanding of the nanolayers elucidated the strategies to improve passivation significantly, achieving an implied open circuit voltage (iV_{OC}) of 698 mV and dark saturation current density (J_0) of 34 fA/cm^2 for a p^+ poly-Si contact using a PECVD SiN_x interlayer. These are among the best reported for nitride-based nanolayer tunnelling contacts, with research into nitride-based tunnelling contacts being still in its infancy.

Keywords: hole-selective contacts, silicon solar cells, polysilicon contacts, silicon nitride, aluminium oxide, conduction mechanisms, passivation.

1 Introduction

Polysilicon-based contacts have emerged as a revolutionary contact technology unlocking dramatic increases in the efficiency of single-junction silicon solar cells using industrially compatible processes. The TOPCon structure, as it is known in the field, uses a SiO_x nanolayer topped with an n^+ poly-Si as the electron contact with a diffused boron emitter for the hole contact.[1] This structure has achieved high power conversion efficiencies, with efficiencies reaching 26%[2] and it is now replacing the Passivated Emitter and Rear Cell (PERC) architecture in industrial manufacturing lines.[3] Further increases in the efficiency of single junction c-Si devices requires passivation of both the electron and hole contacts, with either both sides contacted[4–6] or an interdigitated back contact (IBC) architecture.[4,6,7] Studies of SiO_x/poly-Si contacts consistently show higher dark saturation current density (J_0) and contact resistivity (ρ_c) for the hole contact compared to the electron contact.[6,8–12] This can be attributed to the properties of the SiO_x and the Si/SiO_x interface. First, the valence band offset (VBO) of the SiO_x to Si is large, limiting the tunnelling current[13]. To obtain low-resistivity contacts, pinholes must be formed by high-temperature anneals. Pinholes are small areas of direct Si-Si interface, which are not passivated. At small pinhole densities, the passivation is not affected but if the pinhole density is above ~10^6 cm^{-2}, the passivation quality of the contact is reduced.[14–16] Second, in p-type poly-Si contacts the boron diffusion through the SiO_x layer

can be excessively deep, increasing Auger recombination.[17] In electron-selective poly-Si contacts, the phosphorus builds up at the poly Si/SiO_x interface,[18] resulting in a shallow diffusion and a strong field effect passivation (FEP) induced by the sharp doping profile.[17] On the other hand, boron has a high solubility in SiO_x[19] so it is not blocked at the SiO_x layer and a deep diffusion can form during the poly-Si anneal. This reduces the beneficial FEP that forms when a sharp dopant profile is present at the surface, as is the case for phosphorous-doped polysilicon. In addition, the boron within the SiO_x forms B-O pairs resulting in a strained Si/SiO_x interface[12,20] and an increase in defect states. The high diffusivity of boron, combined with the requirement to form pinholes via a high annealing temperature, make the optimisation of a hole TOPCon contact significantly more complex than the electron equivalent.

Recently, alternative dielectrics such as aluminium oxide (AlO_x),[21–26] silicon nitride (SiN_x),[22,23,27] and titanium oxide[22,28] and hafnium oxide have been investigated for passivating contact structures. These materials offer potential benefits to SiO_x in hole-selective contacts. First, the dielectrics have a lower VBO, which enables low contact resistivity from purely tunnelling conduction. The large VBO of 4.3 eV for SiO_x,[23] effectively blocks hole tunnelling for thicknesses above 1.2 nm. SiN_x and AlO_x have lower VBO's of 1.4 eV and 3.5 eV, respectively,[23] corresponding to allowable tunnelling thicknesses of 2.0 and 1.4 nm.[13,23] Secondly, SiN_x or SiO_xN_y interlayers have been shown to block boron effectively, and thus may produce improved diffusion profiles compared to SiO_x p^+ poly-Si contacts.[17,29] Finally, SiO_x has a low fixed charge density (Q_f). It relies only on chemical passivation to provide a low surface recombination velocity. Alternative dielectrics can contain high Q_f, which provides FEP in addition to chemical passivation. Simulations investigating the effect of interface charge show a beneficial effect in both the resistivity and passivation of the contacts for negatively charged tunnel layers. The charge can reduce the requirements for doping in the poly-Si as well. AlO_x is well known to form a large negative charge at the Si surface.[23,30–33] even in layers <10 ALD cycles (<1 nm).[23,31] SiN_x is known to have a positive fixed charge,[33] which could be detrimental to the properties of a p-type contact by reducing the passivation, or increasing the contact resistivity[13]. Simulations have shown the highly doped p^+ poly-Si layer compensates for positive charge, mitigating the effect for $Q_f < 10^{12}$ q/cm^2.[13] Initial findings suggest this charge is sufficiently low in ~2 nm films.[23]

Accurately quantifying the charge in the nanolayer dielectrics is difficult using standard techniques (e.g. Ref.34-35[34,35]) due to the highly conductive nature of the films. Previous works[36,37] used corona discharge to neutralise the internal charge in the dielectric. However, leakage current through the dielectric changes the net charge between deposition and measurement, resulting in an overestimation of Q_f. Others used contacted C-V measurements but accounted for the leaky dielectric by incorporating the conduction through the dielectric, as well as the conductivity arising from interface states, into the theoretical models.[35,38,39] Lastly, charge in the dielectrics can be characterised using surface photovoltage (SPV) measurements[40]. In this technique, the samples are not contacted so leakage through the dielectric cannot occur. However, the effect of Q_f and the interface state density (D_{it}) on the measured signal cannot be completely isolated, which limits precision. Developing techniques to determine the fixed charge in nanolayer dielectrics is crucial to maximise the potential of these materials in passivating contact structures.

There have been few studies incorporating dielectrics other than SiO_x into poly-Si contacts. The wealth of studies on SiO_x has enabled optimised processing conditions to be established for SiO_x and hole-selective contacts have been fabricated with J_0 approaching 5 fA/cm^2 for p^+ poly-Si on p-type wafers.[41], while p^+ poly-Si on n-type wafers can generally obtain better passivation[11,20,42], with the lowest reported J_0 being 1.5 fA/cm^{-2}.[43] For non-SiO_x dielectrics with

p^+ poly-Si on p-Si, the best SiN_x contacts have measured an iV_{oc} of 690 mV[22] (approximate J_0 of 73 fA/cm^2 extracted using ref.44[44]) with a ρ_c of 800 mΩ·cm^2,[22] and AlO_x contacts have reported a J_0 of 14 fA/cm^2 with a ρ_c of 300 mΩ·cm^2.[37] An alternative approach is to dope a SiO_x layer with nitrogen using an N_2O plasma[17,45]. This method aims to combine the beneficial boron blocking seen in nitride-based contacts with the chemical passivation of an SiO_x nanolayer. It has proved effective, with a low J_0 of 6 fA/cm^2 measured for p^+poly-Si on n-Si[46].

For a full area passivating contact to have a negligible impact on the series resistance of the cell, the contact resistivity must be below 100 mΩ·cm^2.[47] So far, it has proved challenging for SiN_x and AlO_x contacts to meet this benchmark [22,37] while maintaining high levels of passivation, despite the potential theoretical advantages over SiO_x. However, many aspects of these nanolayers are yet to be fully understood, so there is still scope for significant improvement with optimised processing.

In this study, SiN_x and AlO_x are investigated in hole-selective poly-Si contacts. The resistivity and passivation quality of the nanolayers are compared to UV-O_3 SiO_x reference samples. In addition to measuring the contact properties of the alternative nanolayers, there is a focus on obtaining a detailed understanding of the mechanisms governing the passivation and transport properties of the contacts. This is achieved through temperature-dependent current-voltage measurements (T-JV) to establish the dominant conduction mechanisms, and by developing a capped C-V analysis to determine the relative contribution from chemical and field-effect passivation. Using the understanding gained from these techniques, we processed a new set of samples with improved passivation. They showed a large scope for process optimisation and efficiency improvements when the tunnelling dielectric material is reconsidered in p-TOPCon.

2 Experimental Methodology

2.1 Sample Fabrication

Poly-Si passivating contacts are prepared using the process flow shown in Figure 1a. Float-zone p-type wafers (2 Ω·cm) are cleaned using standard RCA cleaning and dipped in hydrofluoric acid (HF) before dielectric nanolayer deposition of RF Plasma Enhanced Chemical Vapour Deposition (RF PECVD) silicon nitride or Atomic Layer Deposition (ALD) aluminium oxide. In an additional group, the samples undergo a second treatment in RCA2 solution after HF etching, and the resulting silicon oxide layer forms an interlayer between the silicon and deposited dielectric (SiN_x or AlO_x). Silicon nitride is deposited using an Oxford Instruments PECVD at 350 °C. The chamber pressure is held at 650 mTorr while 20 sccm silane, 40 sccm ammonia, and 980 sccm N_2 are admitted into the chamber. A 20 W plasma is initiated for 3 s to deposit an SiN_x layer of ~2 nm. Aluminium oxide is deposited in an Anric thermal ALD at 150 °C. One full AlO_x cycle consists of 3× trimethylaluminium pulse/purge cycles followed by 2× H_2O pulse/purge cycles. 10 deposition cycles (10 c) form a ~1.5 nm AlO_x layer. The reported thicknesses were measured using ellipsometry with a FilmSense FS1 multi-wavelength ellipsometer using a Cauchy fitting for SiN_x and the model of McGraw-Hill for AlO_x.[48]

For fabrication of p+ poly-Si contacts, a boron-doped amorphous silicon (a-Si) layer is deposited on top of the thin passivating dielectric by PECVD in a KAI-M system from Unaxis. The layer stack is then annealed in an Ar atmosphere with a heating rate of 10 °C/min to the set point, immediately followed by a 2 °C/min cooling. Such annealing results in the crystallisation of the a-Si layer into poly-Si, the activation of B dopants in the layer, and shallow

B-diffusion in the Si substrate. Optimisation of the PECVD parameters for a-Si deposition and annealing temperature was carried out in previous work to maximise the surface passivation while minimising the contact resistivity of the resulting p+ poly-Si contact[49]. The poly-Si contact is formed on both sides of the Si substrate for lifetime samples. Then, a double-sided PECVD SiN_x layer of about 80 nm is deposited and fired at 840 °C to provide hydrogenation (Figure 1b). The p^+ poly-Si has previously been shown to achieve a high iV_{OC} in SiO_x poly-Si structures.[49,50] The SiN_x is removed using an 5% HF solution for electrochemical capacitance-voltage (ECV) and resistivity measurements. Due to slight variations in the processing conditions of the dielectrics and poly-Si layers, a SiO_x reference sample is included in each processing batch. The SiOx layer is grown on an HF dipped wafer by exposure to UV light for 2 min (Jelight UVO cleaner 42) to form a 1±0.3 nm layer. Table 1 details the dielectric layers and poly-Si anneal temperature included in each sample set.

The resistivity of the dielectric nanolayers is measured by depositing Al contacts using a thermal evaporator. The poly-Si is etched using reactive ion etching (RIE) to leave an exposed contact stack, preventing current spreading through the highly doped poly-Si. The rear poly-Si is also removed using RIE, and then a rear Al contact is deposited. The contacts are cured on a hotplate at 300 °C for 10 mins. The final structure for resistivity measurements is shown in Figure 1c.

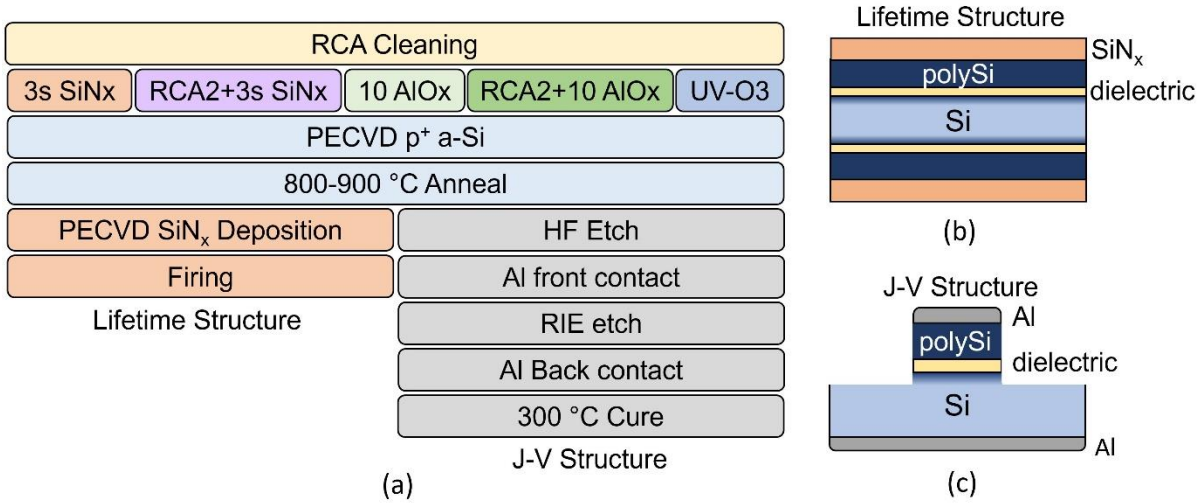

Figure 1: a) Sample preparation process flow. A schematic of the final sample structure for b) lifetime and PL measurements and c) J-V measurements.

Table 1: Dielectric interlayers and poly-Si anneal temperatures for each sample set.

	Dielectric Interlayers	Poly Si Anneal Temperature (°C)
Sample Set A	3 s SiN_x 10 c AlO_x RCA2+3 s SiN_x RCA2+10 c AlO_x UV-O_3	850
Sample Set B	3 s SiN_x UV-O_3	800, 850, 900
Sample Set C	RCA2+3 s SiN_x RCA2+10 c AlO_x UV-O_3	800, 850, 900

2.2 Characterisation

The minority carrier lifetime was measured on symmetrical samples with either a Sinton WCT-100 or WCT-120 instrument. The implied open-circuit voltage (iV_{OC}) was extracted at 1 sun conditions and the J_0 for a single side is extracted using the method described in ref.51[51]. Photoluminescence (PL) images are taken with an in-house built setup. The photocarriers are generated using an 808 nm wavelength laser and a PIXIS camera from Princeton Instruments is used for the imaging. The ECV measurements are performed using an ECV CVP21 tool from WEP. A 0.1 mol/L NH_4F solution is used as the etchant. X-ray photoelectron spectroscopy (XPS) is used for compositional analysis and band alignments of the nanolayer dielectrics to silicon. Full details of the XPS are included in the supporting information.

Current Density-Voltage (J-V) measurements were performed using a Keithley 2611 source meter, with the sample structure shown in Figure 1c. The RIE etch isolates the contact stack to prevent lateral conduction in the poly-Si layer. A straight J-V curve between ±0.1 V indicated ohmic characteristics for all samples. The total resistivity (ρ_{tot}) is extracted from the inverse gradient of the curve between ±0.01 V as:

$$\rho_{tot} = \left[\frac{\Delta J}{\Delta V}\right]^{-1}_{V\approx 0},$$

and the contact resistivity (ρ_c) is determined by removing the spreading resistance of the wafer (R_s), given by,

$$R_s = \frac{\rho}{d\pi} arctan\left(\frac{4t}{d}\right).$$

Where ρ is the wafer base resistivity, d is the contact diameter and t is the wafer thickness. Hence, the contact resistivity is calculated as

$$\rho_c = \rho_{tot} - R_s \cdot A_c.$$

Where A_c is the contact area. Temperature dependent J-V measurements are used to determine the dominant hole transport mechanisms across the dielectric interlayers. The measurements followed the procedure detailed in previous work.[23]

2.2.1 Capped Capacitance-Voltage (C-V)

To determine the interface properties of the highly conductive tunnel dielectrics, a capped C-V method was developed using a low-damage PECVD 100 nm SiO_x layer to prevent conduction through the dielectrics. The SiO_x is deposited using Oxford Instruments PlasmaPro 80. The chamber is held at 800 mTorr with gas flows of 10 sccm silane, 680 sccm N_2O, and 790 sccm N_2. The stage is set to 350 °C and a plasma power of 20 W is used to deposit the SiO_x at a rate of ~1 nm/s. The thick SiO_x is deposited on top of the nanolayer dielectrics to suppress the high conductivity, while the original Si/dielectric interface strongly influences the C-V signal. Silicon oxide prevents a substantial FEP effect, which would affect the measurements. Some hydrogenation may occur during the SiO_x layer deposition and reduce the D_{it}. Indeed, the lifetime of the SiN_x samples increased after SiO_x deposition (from ~40 to ~100 µs). Figure 2a shows the process flow for fabricating the capped C-V test samples.

C-V measurements are performed on 10 Ω·cm, p-type, Cz wafers at 1 MHz using 1 mm circular aluminium contacts. An Agilent E4980A precision LCR meter is used to sweep the voltage from the depletion region to accumulation with a 20 s initialisation delay and a 1 s step delay. The A.C. signal is set to 0.05 V. Theoretical fitting of the C-V curve is used to extract the Q_f and D_{it} of the Si/dielectric interface.[52] The density of interface states as a function of the

band gap energy is modelled as a constant value at the mid gap and an exponentially increasing density towards the band edges.[53] The density of states at the mid gap is used when reporting values of D_{it}.

Figure 2b shows a C-V curve for a 100 nm PECVD SiO_x sample, without a nanolayer dielectric interlayer, and includes the theoretical fit (black line). The sample shows a characteristic 'S shaped' curve, as expected for a Metal-Insulator-Semiconductor (MIS) device. The voltage at which the inflection point occurs indicates the charge present at the Si/Dielectric interface, while the transition between the accumulation and depletion regimes provides information on the density of interface states. The charge and D_{it} indicated in the inset are higher than would be expected for a 100 nm thermal SiO_x. The high D_{it} is as unsurprising for a low-temperature deposition of SiO_x. When measuring the nanolayer dielectrics, the PECVD SiO_x does not directly contact the silicon, so the C-V measurement is not affected by the SiO_x D_{it}. The charge of 7–8×10^{11} q/cm^2 might have a minor influence on the underlying dielectric, resulting in a small systematic error in the absolute value of Q_f extracted. The charge likely forms at the Si/PECVD SiO_x interface, which is not present when PECVD SiO_x is used as a capping layer on another dielectric. Therefore, it cannot be corrected by simply subtracting the charge in the PECVD SiO_x from the value measured in the dielectric/SiO_x stack. The influence of this charge is considered in the discussion of the results. The error is systematic, so it is consistent for all measurements, and therefore, the comparison between samples is unaffected.

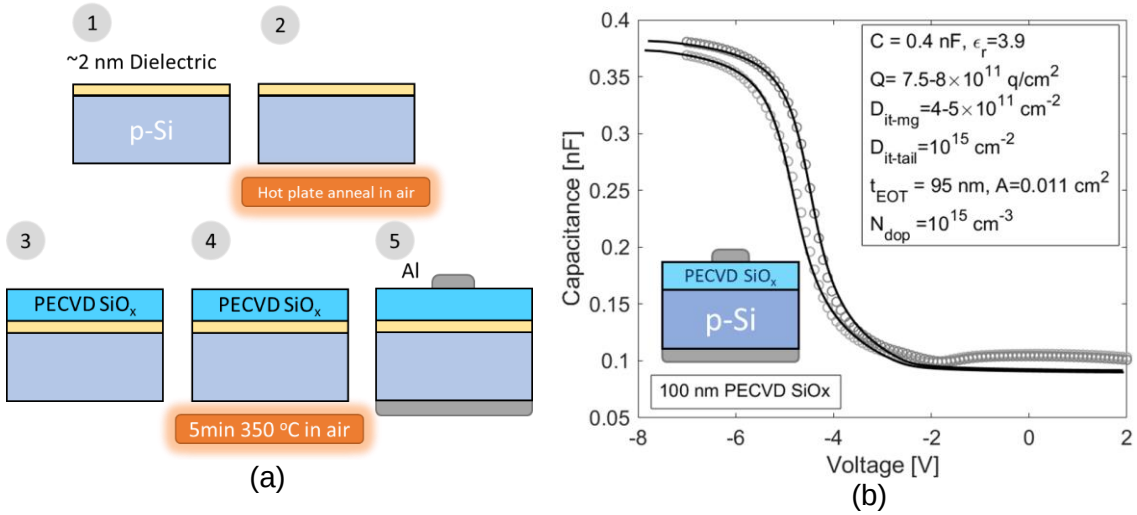

Figure 2: (a) Sample preparation for C-V analysis. 1. Deposition of dielectric, 2. Hot plate anneal (if required), 3. Deposition of PECVD SiOx, 4. 350 °C anneal of PECVD SiO_x 5. Deposited Al contacts on front and rear. (b) C-V curve of 100 nm PECVD SiO_x with no dielectric interlayer (two contacts measured). Insets show sample schematic and theoretical fitting parameters.

3 Results and Discussion

3.1 Resistivity Measurements

Poly-Si contacts with either SiN_x or AlO_x nanolayers were fabricated according to the process in Figure 1a (Sample Set A) and the resistivity was measured as described in Section 2.2. The contact resistivity was measured for UV-O_3 SiO_x, 5 and 10 cycles of ALD AlO_x, 3 s PECVD SiN_x, and RCA2+3 s PECVD SiN_x nanolayers. The poly-Si was annealed at 850 °C for all samples, and the measured contact resistivity is shown in Figure 3a. The samples with 5 cycles of AlO_x or 3 s SiN_x have comparable resistivity to the UV-O3 SiO_x. A slight increase in the resistivity is measured for the 10 cycles of AlO_x and the RCA2+SiN_x stacks but all contacts

stacks have median resistivities below 100 mΩ·cm^2. A contact resistance of 100 mΩ·cm^2 is a useful benchmark for fabricating a solar cell with a full area contact, without a significant reduction in the fill factor (~0.05%$_{abs}$).[47]

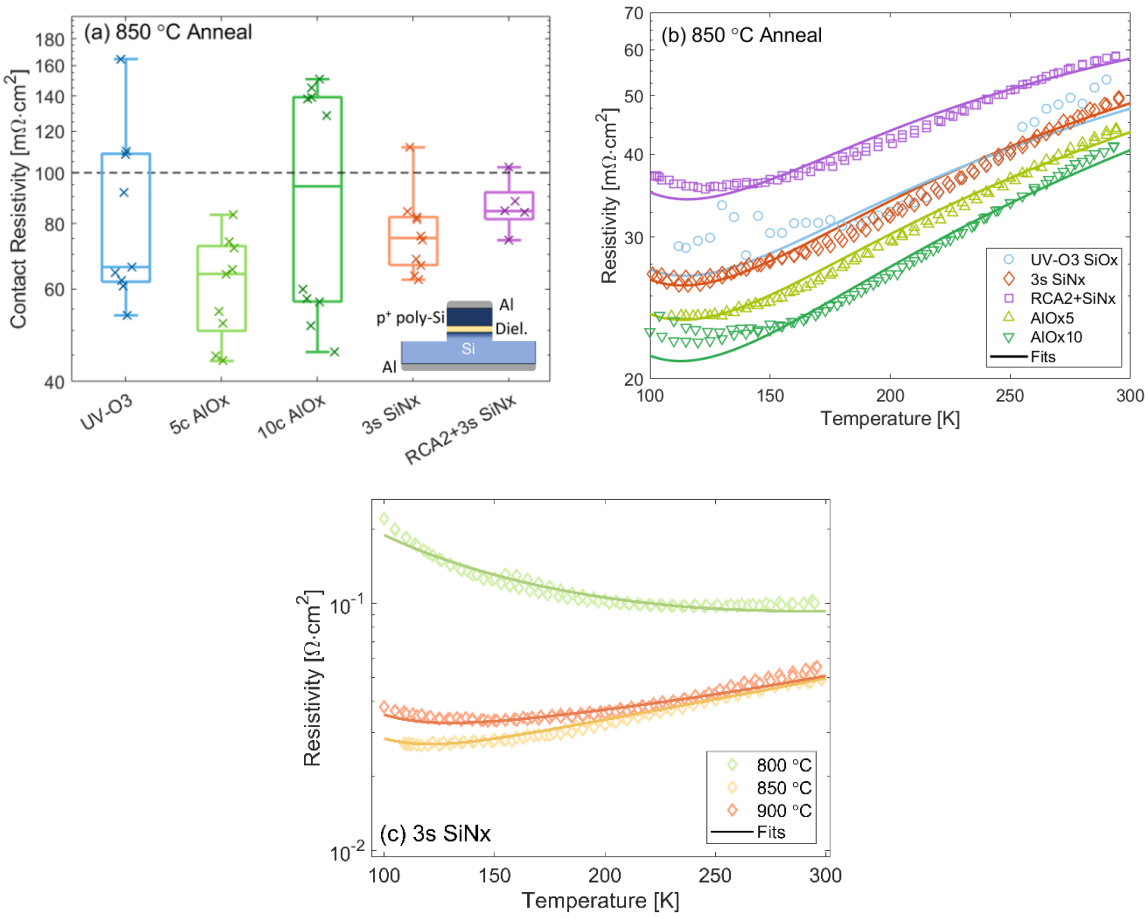

Figure 3: (a) Contact resistivity of Sample Set A: UV-O_3 SiO_x, 5 and 10 cycles of ALD AlO_x, 3 s PECVD SiN_x, and RCA2+3 s PECVD SiN_x nanolayers annealed at 850 °C. The box plots indicate the median, 25th and 75th percentiles, and the maximum and minimum values. A schematic of the samples is shown in the inset. (b) The total resistivity measured between 100-300 K with theoretical fits for Sample Set A. (c) The total resistivity measured between 100-300 K with theoretical fits for Sample Set B for different annealing conditions. A pinhole radius of 0.5 nm is assumed.

Temperature-dependent J-V measurements were also performed for the dielectrics to provide information on the conduction mechanisms present in the samples. Figure 3b shows the total resistivity, ρ_{tot}, measured between 100-300 K. The solid lines are theoretical fits, with the fitting parameters shown in Table 2. The equivalent circuit diagram and an example fitting are shown in Supporting Information Section 1, while a detailed description of the fitting procedure and the experimental determination of the VBO using the XPS based Kraut's method, is described in previous work.[23,54] The instrumental set up is described in Supplementary Section 3. It can be seen in Figure 3b that all dielectrics follow the same trend with temperature. The decrease in resistivity with reducing temperature is indicative of pinhole dominated conduction, and indeed high pinhole concentrations are required to fit the data, as shown in Table 2. A second batch of samples was prepared to study the effect of the annealing temperature on the transport mechanisms (Sample Set B). The 3 s SiN_x/poly-Si samples were annealed at 800, 850 and 900 °C. For the 3 s SiN_x layer after an 800 °C anneal, the T-JV curve shows the opposite behaviour with an increase in the resistivity at low temperature. This is fitted with purely tunnelling conduction, indicating the pinhole density is below the sensitivity of the

technique and that these layers allow substantial tunnelling conduction despite being about 1.9 nm thick. It is noted that the 800 °C sample measures a slightly thicker dielectric. If this discrepancy occurred during SiN_x deposition, the thicker dielectric may have been less susceptible to forming pinholes during anneal, which, in combination with the lower temperature, resulted in the tunnelling behaviour and observed temperature trend. Alternatively, the higher temperature anneals could induce thinning of the SiNx (densification) as well as forming pinholes. We cannot distinguish between these two possibilities, but the primary conclusion still stands. It is possible to fabricate purely tunnelling hole selective poly-Si contacts. This means the high-temperature anneal may to be optimised solely for passivation. In the contacts that formed pinholes, there is a mixed mode of current transport, with contributions from tunnelling and pinholes. This is highlighted in Figure S1, where it is shown that our samples are dominated by tunnelling conduction at room temperature, while at low temperature pinhole conduction dominates. Hence, although pinholes form during the high temperature processing, these pinholes are not required to achieve the low resistivity SiN_x contact. The high pinhole concentration results in a larger area of direct Si-Si contact, which can reduce the contact passivation quality. An increase in J_0 is predicted at pinhole densities $>10^6$ cm^{-2} [14–16,55] – a threshold that is significantly exceeded in these samples.

Table 2: Fitting parameters for T-JV measurements of Sample Set A and B, assuming a pinhole radius of 0.5 nm.

	Dielectric	T [°C]	VBO [eV]	t_{diel} [nm]	Φ_b [eV]	N_{pin} [$\times 10^8$ cm^{-2}]
Set A	UV-O_3 SiO_x	850	4.3	1.2	0	1
	3 s SiN_x	850	1.4	1.9	0	1.1
	RCA2 + 3 s SiN_x	850	1.4	1.92	0	0.6
	5 cycles AlO_x	850	3.5	1.32	0	1.4
	10 cycles AlO_x	850	3.5	1.32	0	2
Set B	3 s SiN_x	800	1.4	1.86	0	0
	3 s SiN_x	850	1.4	1.73	0	1
	3 s SiN_x	900	1.4	1.73	0	0.6

3.2 Passivation

The passivation quality of the poly-Si contacts was initially investigated using QSSPC on symmetrical lifetime samples of Sample Set A. The samples were measured after the 850 °C anneal and again after a PECVD SiN_x hydrogenation layer was deposited on top of the poly-Si and fired at 840 °C. At this stage, the AlO_x samples had a lifetime too low to be measured. The SiN_x samples are compared to the UV-O_3 SiO_x reference via their iV_{OC}, as pictured in Figure 4. The passivation of the SiN_x layers is currently lower than the SiO_x reference, both after annealing and hydrogenation. The RCA2+SiN_x shows the most significant improvement in iV_{OC} after hydrogenation, with one sample reaching an iV_{OC} of 668 mV. We note that for this batch, the iV_{OC} measured on samples featuring the UV-O_3 SiO_x reference was about 15-20 mV lower than usual after annealing and hydrogenation, with optimised UV-O_3 SiO_x poly-Si layers previously reaching iV_{OC} of 720 mV[56] . We attributed the variation to a drift in the PECVD chamber conditioning when depositing the poly-Si layer. This suggests that the iV_{OC} measured on samples featuring thin SiN_x and AlO_x layers may also be higher when combined with optimal poly-Si processing.

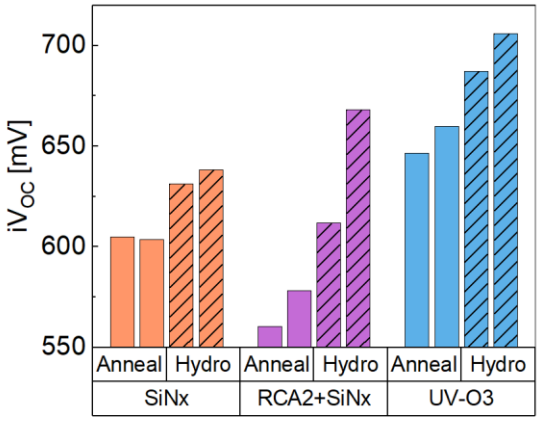

Figure 4: iV_{OC} of Sample Set A, SiN_x nanolayers compared to the UV-O_3 SiO_x control samples. Samples were annealed at 850 °C (shown as Anneal) then hydrogenated (shown as Hydro) using a fired PECVD SiN_x. 2 samples are measured at each processing step.

PL images of the poly-Si samples after hydrogenation provide a spatial map of the passivation quality. Figure 5 shows PL images of a) SiN_x, b) RCA2+SiN_x and c) UV-O_3 SiO_x samples after the hydrogenation treatment. Images of the other samples are shown in Figure S3. The UV-O_3 SiO_x has uniform passivation, while significant inhomogeneities are observed in both SiN_x samples. The SiN_x samples have large areas with poor passivation, which could be due to issues with sample handling or a non-uniform deposition of SiN_x. In the RCA2+SiN_x sample, the regions with the best passivation quality approach that of the SiO_x. The significant spatial variation partially explains the low iV_{OC} observed in the SiN_x samples, as the measured iV_{OC} is an average across the area of the Sinton instrument sensor. Although, the brighter regions in the SiN_x do not quite represent the same iV_{OC} as the control UV/O_3 sample.

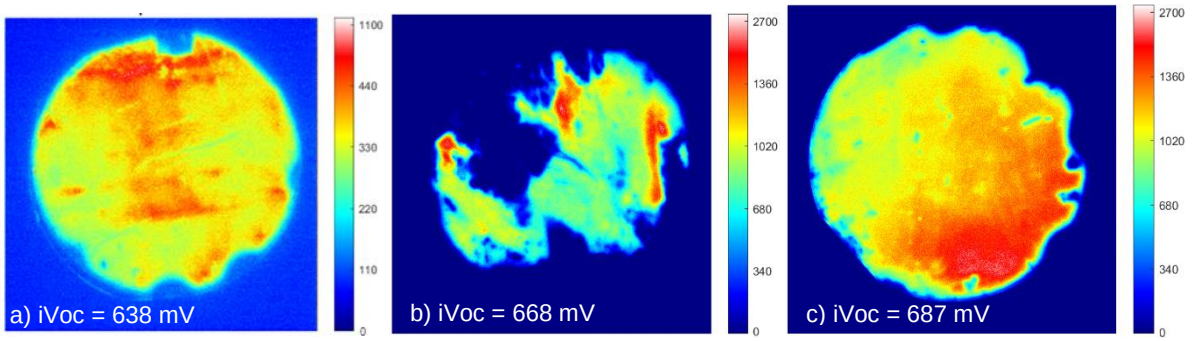

Figure 5: Photoluminescence images of (a) SiN_x, (b) RCA2+SiN_x and (c) UV-O_3 SiO_x after hydrogenation.

3.2.1 D_{it} and Q_f analysis using Capped C-V

The reasons for the poor passivation quality of the AlO_x and SiN_x were investigated further to develop a greater understanding of the differences between these dielectrics and a standard SiO_x layer. One of the key differences is that SiN_x and AlO_x can have high interface charge densities. This is well documented in thick AlO_x and SiN_x layers used for surface passivation.[33] Capacitance-Voltage measurements are often used to extract the interface charge and density of defect states at a semiconductor/dielectric interface.[57,58] However, the high conductivity of the nanolayers used in passivating contacts prevents an accurate capacitance from being measured. To overcome this problem a novel technique was developed, where a thick PECVD SiO_x (~100 nm) was deposited on top of the nanolayer dielectric. This reduces the conductivity while the measurement remains highly sensitive to the Si/nanolayer interface. Figure 6 shows the C-V curves for nanolayer dielectrics capped with 100 nm PECVD SiO_x. SiN_x and AlO_x

layers are compared to an RCA2 silicon oxide. All samples were made before any polysilicon was deposited or fired, and thus are only indicative of the initial condition the interface nanolayers display. The black lines indicate theoretical fits, and the fitting parameters are detailed in Table 3.

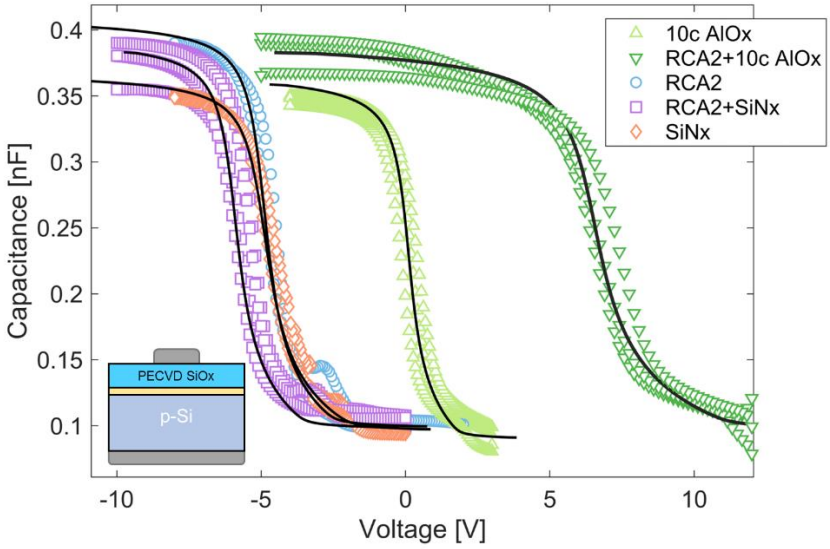

Figure 6: C-V analysis of AlO_x and SiN_x nanolayer stacks. Solid lines indicate the theoretical fitting, with fitting parameters detailed in Table 3. A schematic of the sample structure is shown in the inset.

Table 3: Fitting parameters for capped C-V measurements.

Dielectric	Q_f [10^{12} q/cm^2]	D_{it} [10^{12} cm^{-2}]
RCA2 SiO_x	0.7±0.1	0.5±0.2
3 s SiN_x	0.6±0.05	0.6±0.2
RCA2 + 3 s SiN_x	1±0.1	0.4±0.2
10 c AlO_x	-0.4±0.1	0.4±0.2
RCA2 + 10 c AlO_x	-3.2±0.2	2±0.5

In Figure 6, the SiN_x nanolayer shows a similar behaviour to the RCA2 SiO_x, and Table 3 confirms similar values of both Q_f and D_{it}. A slight increase in positive charge is seen for the RCA2+SiN_x layer. Note that there is a small systematic shift to positive Q_f due to the intrinsic charge in PECVD SiO_x (as discussed in Section 2.2.1 and shown in Figure 2b). Despite this, Q_f below 10^{12} cm^{-2} was observed in all SiN_x layers, and previous simulation work determined that at this charge concentration, there is only a small detrimental effect in p^+ poly-Si contact properties[13]. AlO_x shows a distinct shift to negative charge, increasing significantly with the addition of an RCA2 interlayer. At such high Q_f, the negative charge can contribute to reductions in ρ_c and J_0 of the contact.[13] The higher Q_f observed for the RCA2+AlO_x stack relates to the reactivity of the ALD precursors to the silicon surface. The oxidised surface improves the adsorption of the TMA,[59] resulting in a higher concentration of Al in the film. This is observed via stoichiometry analysis using XPS (Figure S7). The D_{it} increase in the RCA2+AlO_x stack is unexpected and could inhibit higher passivation levels. Further investigation is required to study the cause of the high D_{it} and develop methods to mitigate it. These results agree with previous measurements using SPV,[23] further validating the technique, while this C-V method enables a more precise evaluation of the interface.

3.2.2 Electrochemical capacitance-voltage (ECV)

The doping profiles of SiO_x, SiN_x, and AlO_x poly-Si contacts from Sample Set A were measured using ECV and are shown in Figure 7. SiO_x and AlO_x nanolayers have a diffusion depth between 90 and 120 nm, while the SiN_x has an apparent blocking effect, reducing the in-diffusion to 60 – 80 nm. The deep diffusion of the boron in SiO_x nanolayer samples can be linked to the high diffusivity/solubility of boron in SiO_x[60], while phosphorus has a low diffusivity in the SiO_x[61] and therefore less in-diffusion is observed[17]. The high boron concentration in the SiO_x results in increased strain and reduces the ability to passivate the dangling bonds at the Si surface.[62] The SiN_x has a lower boron solubility and therefore could provide a better chemical passivation, possibly through utilising a higher temperature or longer anneal. In addition, the steeper diffusion profile can increase the field effect passivation across the dielectric and limit the Auger recombination in the device.[63] We observe here that the SiN_x nanolayer brings an additional blocking effect to B diffusion compared to SiO_x and AlO_x. Thus, a SiN_x nanolayer could facilitate the optimisation of p^+ poly-Si contacts towards high surface passivation, high field-effect passivation, and low Auger recombination in the B-diffused region.

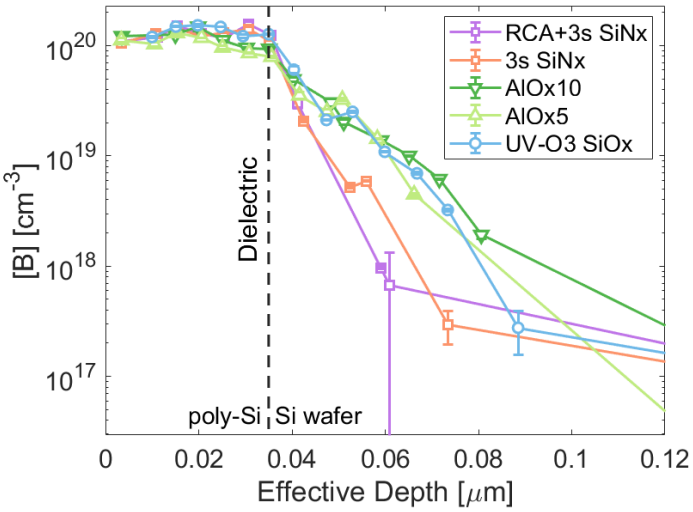

Figure 7: ECV doping profiles of poly-Si samples with SiO_x, SiN_x and AlO_x nanolayers after 850 °C anneal.

3.3 Improved Passivation

The C-V and ECV results elucidated possible paths to improve the passivation quality of the AlO_x and SiN_x contacts. The high charge obtained for the RCA2+AlO_x sample make this an attractive option and a lower anneal temperature may be preferable to prevent the AlO_x breaking up, reducing its pinhole density. The RCA2+SiN_x layer showed some promise in Sample Set A, with a significant enhancement possible if the uniformity was improved. In addition, the ability for SiN_x to block the boron can enable a higher thermal budget to be used. To improve the passivation, a new batch of samples was fabricated and termed Sample Set C. The effect of different poly-Si anneal temperatures was studied, focussing on the most promising nanolayers. In this iteration, handling of the wafers was minimised during RCA2 growth and subsequent depositions to improve passivation uniformity. Figure 8 shows the iV_{OC} for RCA2+SiN_x and RCA2+AlO_x layers at a range of annealing temperatures after

hydrogenation. The iV_{OC} of samples with the dielectric but without a poly-Si layer is included here and referred to as “pre poly-Si”. These samples underwent a hotplate anneal in air before being measured.

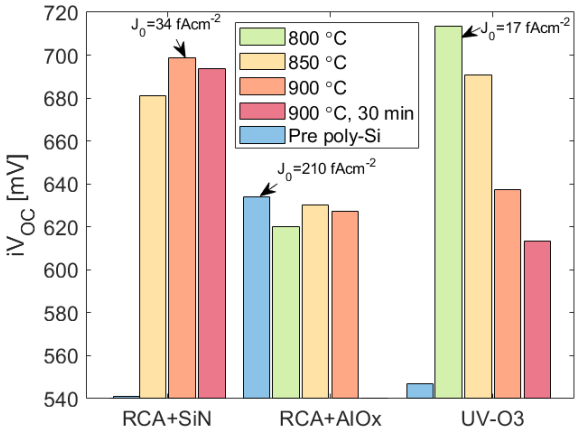

Figure 8: iV_{OC} for symmetrical RCA2+SiN_x and RCA2+AlO_x poly-Si structures with a range of annealing temperatures. The samples are measured after hydrogenation. The ‘pre poly-Si’ measurement indicates the highest lifetime obtained without the poly-Si after a hotplate anneal. The hotplate anneal temperature was 600 °C for the RCA2+SiN_x and UV-O_3 samples and 350 °C for the RCA2+AlO_x sample. The single sided dark saturation current density, J_0, is indicated for the best passivation achieved for each dielectric.

The RCA2+SiN_x sample shows an increase in the passivation quality, with a maximum iV_{OC} of 698 mV after the 900 °C anneal. It also shows excellent thermal stability, with high iV_{OC} maintained across different anneal conditions. The UV-O_3 passivation, on the other hand, drops significantly after 800°C, indicating it is less stable to process variability. Figure 9 shows the corresponding PL image for the optimum anneal condition of each dielectric. A substantial improvement in the homogeneity of the passivation has been achieved for the SiN_x, compared to Figure 5b). This shows that PECVD deposition is a viable method for achieving highly uniform passivation of nanolayer dielectrics across a full wafer. An improvement is also seen in the AlO_x nanolayers compared to Sample Set A, where lifetime was not measurable. However, only moderate iV_{OC} is achieved at present with AlO_x poly-Si contacts. Interestingly, the AlO_x nanolayers perform better than SiN_x and SiO_x before poly-Si deposition, but this does not translate to the final contact structure. This indicates that poly-Si deposition and high-temperature annealing may damage the Si/AlO_x interface. Recent work by Grant et al. [32] shows that at temperatures up to 600 °C the high charge density remains in the nanolayer, however, at temperatures above 500 °C the chemical passivation begins to decrease. This may become more severe at the >800 °C temperatures in poly-Si contacts. We also observed some blistering in the poly-Si of the AlO_x samples, covering <0.5% of the total area (Figure S8). This may contribute to the poor lifetime and increase scatter in the results.

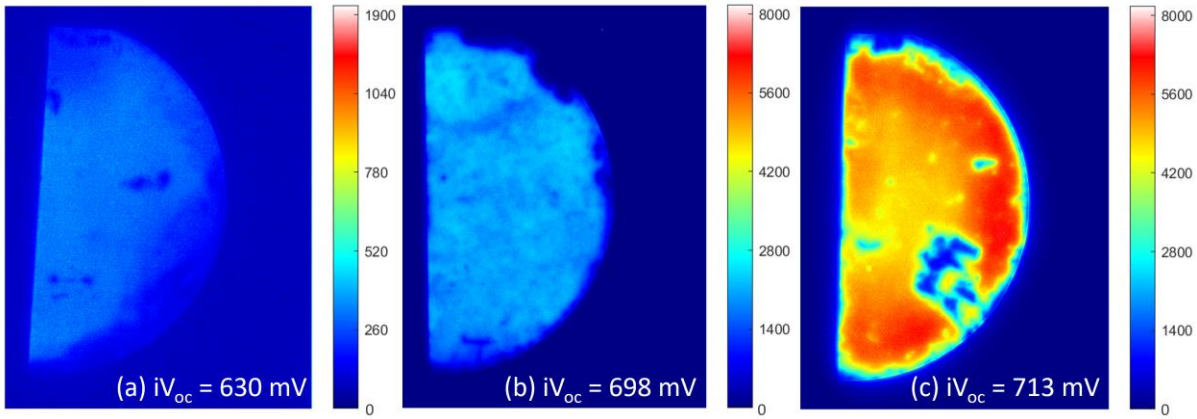

Figure 9: PL images for (a) RCA2+AlO_x layers after 850 °C anneal, (b) RCA2+SiN_x after 900 °C anneal, and (c) UV-O_3 after 800 °C.

The resistivity of the samples from Sample Set C was measured and is included in the supporting information (Figure S2). The contact resistivity was notably higher for the SiN_x and AlO_x samples, while ρ_c for the UV-O_3 samples was consistent compared to the previous results. It is expected this is due to slight variation in the dielectric thickness of the ALD and PECVD layers between batches. Further explanation is included in the supporting information. Optimisation of the processing flow is required to achieve the best passivation at an acceptably low resistivity. This may include a more streamlined process flow to minimise the time between dielectric deposition and a-Si deposition. In the case of the thin SiN_x layers, it may be possible to combine its deposition with the a-Si in a single PECVD chamber. Such prospects will be explored in future work.

3.4 Efficiency Potential of Contacts Integrated into Full Device Structures

SiN_x and AlO_x passivation layers have been implemented into p^+ poly-Si contacts. The RCA2+SiN_x stacks showed the most promise in the poly-Si contact structure with iV_{OC} approaching 700 mV and a single sided J_0 of 34 fA/cm^2. This is among the best passivation achieved for a SiN_x, SiO_xN_y, or SiO_x+SiN_x stacks in p^+ poly-Si contacts, bettering the iV_{OC} of 690 mV achieved by Reichel et al.[22]. Feldmann et al. achieved a similar iV_{OC} of 695 mV for a nitrided plasma oxide.[17] As with SiO_x contacts, n^+ poly-Si contacts using SiN_x nanolayers have achieved higher levels of passivation.[22,64,65] Figure 10 compares the best results from this work to literature values for p^+ poly-Si contacts using SiN_x, AlO_x or SiO_x nanolayers. The contact selectivity indicated by the black dashed lines is a metric devised by Brendel et al.[66] as a figure of merit for passivating contacts. It is noted that the best p^+ poly-Si contacts were fabricated on n-type Si wafers, with an enhanced FEP. Studies using SiO_x far outnumber those using any other passivation layers. Thus, it is unsurprising that the best results are still observed from extensive optimisation of the processing for SiO_x.[49,67,68]

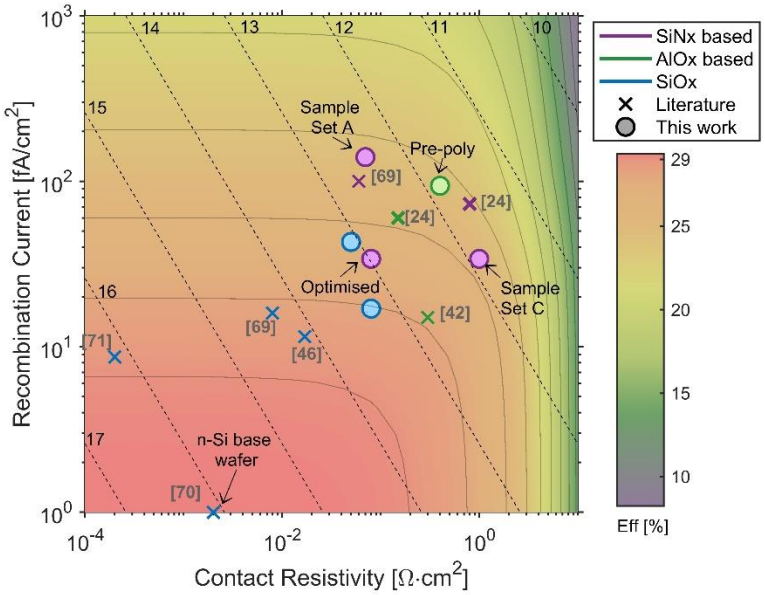

Figure 10: Contact selectivity of p^+ poly-Si passivating contacts in the work compared to literature values.[22,37,43,49,68,69] In instances where only iV_{oc} was reported this was converted to J_0 using ref.4[44]. The selectivity is shown as black dashed lines, while the grey lines indicate efficiency contour lines. The maximum potential efficiency is simulated using PC1D for a 110 µm, 1 Ω·cm p-type wafer with perfect light trapping and electron contact.

The AlO_x structures in this work have so far been less effective as poly-Si contacts despite showing the highest levels of passivation prior to poly-Si deposition. The cause of this passivation loss is suspected to be due to blistering seen after the poly-Si anneal (Figure S8). Blistering is caused by hydrogen outgassing during the high-temperature anneal, which can damage the Si/dielectric interface.[70] Initial tests show some improvement in the passivation when the AlO_x layer undergoes a low-temperature anneal before the poly-Si processing (Figure S8). Optimisation of this step could prevent blistering and enable the full potential of the AlO_x nanolayers to be exploited.

Understanding the nanolayer dielectrics has enabled us to adapt our processes to maximise the capabilities of each dielectric (within only two experimental iterations) and understand where they differ from the ubiquitous SiO_x. The capped C-V method introduced in this paper provides a tool to obtain Q_f and D_{it} to high accuracy and precision in highly conductive nanolayer dielectrics. The PECVD SiO_x capping layer provides an insulating layer to enable good-quality C-V measurements, while the Si/dielectric interface remains the primary influence of the measured capacitance signal. The additional processing of the SiO_x layer could influence the Si/dielectric interface, due to the high concentration of hydrogen in the PECVD SiO_x altering the chemical passivation of the interface, thus leading to an underestimation of the D_{it}. This is not necessarily a problem, as any full contact structure will undergo a hydrogenation step. In fact, with optimisation of the SiO_x anneal, the hydrogenation of the interface could be maximised to give an idea of the minimum D_{it}. The results from the capped C-V show good agreement with the estimated values of D_{it} and Q_f from SPV measurements in previous work.[23] It is noted that the technique cannot be applied to the dielectrics in the full poly-Si structure, however, the information it provides is still valuable.

Significant improvements in the passivation properties were made after only two process iterations (Sample Set A and C), while further optimisation is required to combine this with low contact resistivity. The rapid progress can be partly attributed to the understanding obtained from the capped C-V process in combination with the T-JV and PL images. These results

highlight the importance of developing a complete understanding of the nanolayer dielectric in the poly-Si contact structure. Despite having a thickness of <10 atomic layers, these interlayers govern the contact's resistivity and passivation quality. A deeper understanding of these layers is extremely beneficial to balancing the passivation and transport requirements of the contact. It is vital in the search for ever-higher power conversion efficiencies in solar cells.

4 Conclusion

The development of highly efficient hole contacts is required to complement the already established electron-selective TOPCon structure and further increase the efficiency of poly-Si based Si solar cells. In this work, we investigated SiN_x and AlO_x based stacks as the passivating nanolayer in p^+ poly-Si contacts. The SiN_x and AlO_x offered potential advantages over SiO_x including a lower barrier height for hole tunnelling (SiN_x and AlO_x), an advantageous boron diffusion profile (SiN_x), or an enhanced FEP due to negative charge at the Si surface (AlO_x). We fabricated poly-Si contacts with low contact resistivity for AlO_x and SiN_x layers and, using T-JV, we provide the first demonstration of the conduction mechanisms in hole selective poly-Si contacts using alternative dielectrics. This proved it is possible to fabricate a purely tunnelling SiN_x p^+ poly-Si contact. However, thus far their passivation still does not match the UV-O_3 SiO_x reference. We found the AlO_x samples to have the best passivation prior to poly-Si deposition, partly due to a high charge density of 3×10^{12} q/cm^{-2}. However, the surface passivation did not improve after processing of the p^+ poly-Si layer on top of AlO_x, in contrast to SiN_x and SiO_x. Further analysis is required to determine if the observed blistering is the cause of the limited passivation obtained with AlO_x, and to develop a pathway to increase the passivation in a complete contact structure. Recombination and charge transport measurements helped determine that a high pinhole density and non-uniformity hampered the passivation quality of the RCA2+SiN_x samples, not a high positive charge. With improved processing, we obtained a significant improvement in the passivation quality, obtaining a highly uniform PECVD SiN_x nanolayer with a single-sided J_0 of 34 fA/cm^2. Using direct RF PECVD, we showed the potential of growing tunnelling nanolayers, demonstrating a particularly appealing prospect for streamlined processing of hole-selective polysilicon contacts.

5 Supporting Information.

Additional resistivity measurements including detailed fitting for an example temperature-dependent current-voltage measurement and measurements for Sample Set C. Photoluminescence and minority carrier lifetime measurements for Sample Set A and C, including the fitting for the extraction of J_0. XPS measurements used for stoichiometry analysis of the AlO_x and SiN_x films. Micrograph images of blistering observed in the AlO_x samples from Sample Set C and the improvement in iV_{oc} observed when the AlO_x underwent an additional annealing step before poly-Si deposition.

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7 Data Availability

All data created during this research and published in this article is openly available from the Oxford University Research Archive and can be downloaded free of charge from http://ora.ox.ac.uk.

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