On Wide Dynamic Range Logarithmic CMOS Image Sensors

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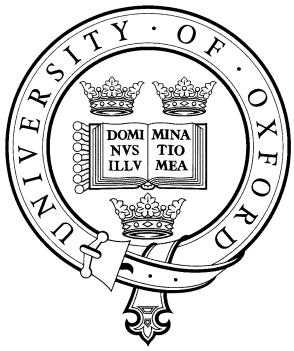

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Abstract

Logarithmic sensors are capable of capturing the wide dynamic range of intensities available in nature with minimum number of bits and post-processing required. A simple circuit able to perform logarithmic capture is one utilising a MOS device in weak inversion. However, the output of this pixel is crippled due to fixed pattern noise. Technique proposed to reduce this noise fail to produce high quality images on account of unaccounted high gain variations in the pixel. An electronic calibration technique is proposed which is capable of reducing both multiplicative as well as additive FPN. Contrast properties matching that of human eye are reported from these sensors.

With reduced FPN, the pixel performance at low intensities becomes concerning. In these regions, the high leakage current of the CMOS process affects the logarithmic pixel. To reduce this current, two different techniques using a modified circuit and another with modified layout are tested. The layout technique is observed to reduce the leakage current. In addition, this layout can be used to linearise the output of logarithmic pixel in low light regions.

The unique linear response at low light and logarithmic pixel at high light is further investigated. A new model based on the device physics is derived to represent this response. The fixed pattern noise profile is also investigated. An intelligent iterative scheme is proposed and verified to extract the photocurrent flowing in the pixel and correct the fixed pattern noise utilising the new model. Future research ideas leading to better designs of logarithmic pixels and post-processing of these signals are proposed at the end of the thesis.

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Dedicated to my elder brother

Shree Shekhar Choubey

Bhaiyajee

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1.1 Digital imaging

Imaging is one of the oldest intellectual endeavours of humankind and is an integral part of our lives. The desire to capture what is observed has motivated human beings towards several technological advancements. The tradition was started by the early man depicting his life experiences on cave walls. With the growth of civilisation, this tradition saw immense technical as well as aesthetical improvements. Men and women have used several mediums to represent nature as well as their lives, including walls, stone, paper, leaves and even body parts. Coloured dyes added a new spectrum to the imaging business. Parallelly, attempts were also made to reduce the required human labour whilst increasing the truthiness of the captured image. Pinhole structures to record images on walls in darkened rooms were one of the first developments in this direction. The discovery of the lens and optical physics added extensively to the arsenal of men in their quest to record life and nature.

Advances in the last century, however, changed the scope of imaging entirely. Cameras

become the present and future of imaging. Using an assembly of lens (or lenses) and a medium to store and reproduce the observed scene, these devices soon became inseparable from modern day man. The first three quarters of the last century saw immense technological as well as commercial growth in film based cameras. These cameras capture a scene on a photo-sensitive film. The film is then developed in a specialist room and the final image may be viewed on the film itself or printed on paper. These reproductions or photographs were a revolution in how we remember our past. The later half of the last century, however, saw another change in the tide of imaging in the form of digital imaging. The film was replaced by semiconductor devices and the picture was stored as a two-dimensional array of binary digits. With this new concept, the picture could be stored and produced infinitely without the fear of degradation over time. This tradition of digital imaging started with the discovery of Charge Coupled Devices (CCD) in 1969 and research since then has expanded the boundaries of imaging to previously unbelievable limits.

The first usage of digital cameras was mainly in scientific imaging. However, commercial general purpose digital cameras were soon populating in the market, the first of these appearing as early as 1973 (Fairchild's CCD camera). Soon, these cameras were recording static as well as video scenes. In recent years, advances in personal computing and the internet have added multiple dimensions to the imaging capabilities. Computer based imaging started with introduction of Apple QuickTake 100 camera in 1994, with a serial interface to the PC. Several similar products followed and these computer cameras not only stored image information, but also changed the way people communicate with one another.

The new digital camera revolution adversely affected the market for film cameras. As of 2006, 82% of cameras sold are digital and film based camera sales are dropping by 20% every year [1]. Since their commercial inception, digital cameras have been embedded in several other systems, including toys, automobiles, security systems and so on. However, the recent integration of digital cameras with mobile devices surpassed all expectations. In fact, the popularity of these camera-phones has been increasing at such a rapid rate that they are soon to become the largest segment in the camera market. As shown in Figure 1.1, about 500 million

camera phones were sold in 2005, which means that about two thirds of all mobile phones purchased had cameras in them and about five out of every six digital cameras sold in 2005 was in a mobile [1].

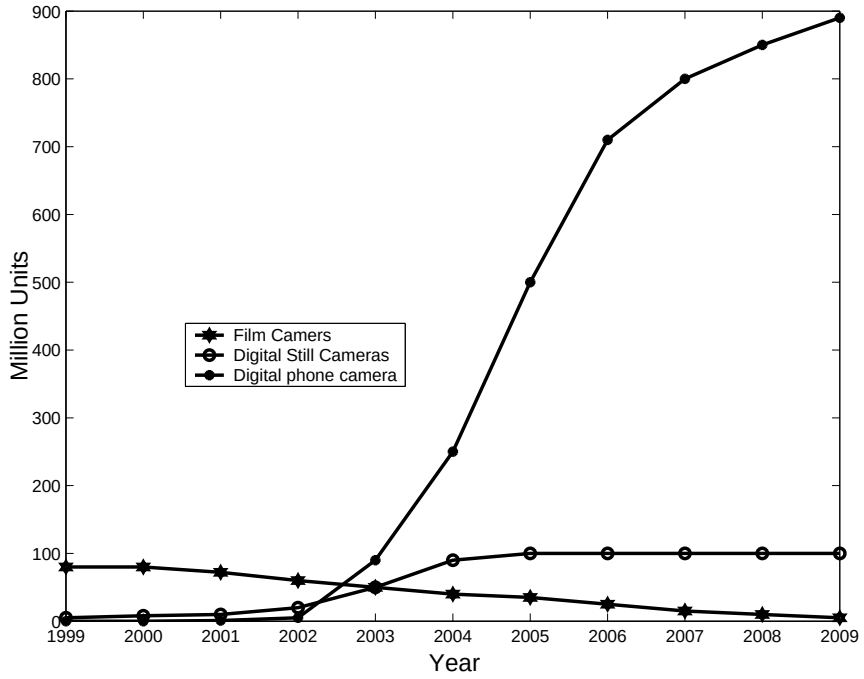

Figure 1.1: Current and projected worldwide sales of cameras

Despite all these technical advances and market popularity, digital cameras are yet to fulfil the ultimate imaging feat - to reproduce a scene as would be visible by the human eye. None of the imaging technologies developed to date have been able to match the performance of the human eye. The performance capabilities of film based as well as digital cameras have been compared to those of the human eye in Table 1.1. The table has been updated from an original table published by Dierickx in 1999 [2]. One may observe that immense improvement is still needed in the artificial imagers in order to match the human eye. In particular, the dynamic range of the image sensor is an area in which imagers still fall behind the human eye. The dynamic range of the imaging system is defined as the range of intensities which it can capture and reproduce faithfully. Current cameras can capture only two to three decades of illumination intensity. This is in contrast to nearly ten orders of intensities available in nature and capturable by the human eye [3]. The natural illuminances vary from as low as 10^{-4} lux in a starlit night

Criterion	Eye	Digital Camera	Film
Spectral response	400 – 700 nm	400 – 1000 nm	300 – 700 nm
Peak quantum efficiency	$<$ 10 %	$>$ 50 %	
Dynamic range	10 decades	2–3 decades	1–4 decades
Dark limit	10^{-3} lux	10^{-4} – 0.1 lux	$\approx$ 0 lux
Noise photons	10	10	100
Integration time	0.3 s	40 ms – 5 mins	Unlimited
Maximum frame rate	$\approx$ 15 Hz	$\gg$ 10 kHz	1 shot only
Number of pixels	12 $\cdot 10^7$ cones	10^7	$> 10^6$
Pixel pitch	2 – 3 μm	5 – 10 μm	10 – 20 μm
Image size	3 cm	1 mm – 11 cm	Film size
Radiation hardness	1 mrad	10 krad – ?	
Operational temperature	309 K	73 – 473 K	273 – 373 K
Power dissipation	$<$ 1 mW	50 mW	None
Colour quality	Ideal	Poor	Poor
Photometry	Impossible	Easy	Possible
Pre-processing	Extensive	Some	None
Access method	Data driven	Serial/random	Optical only
Data path	$5 \cdot 10^6$ nerves	8–16 bits	None
Unit price	Invaluable	5 Pounds	0.1 Pounds
Development cycle	5 $\cdot 10^8$ years	10 years	20 years
Number of fabs	$3 \cdot 10^9$	1000	10

Table 1.1: Comparative chart of performance indicators of the human eye, the best digital cameras in the market and the film. Numbers given are typical values.

to as high as 10^5 lux in bright sunlight. This means that the digital cameras often fail to capture important visual information in several of the captured scenes. The human eye, on the other hand, adjusts its dynamic range by constant adaptation and effective logarithmic compression to map this wide dynamic range and thus retains all needed information from the scene [4]. Even within a scene, the human eye is able to capture about five orders of intensities [5].

Thus, there is a need to investigate ways to improve the dynamic range of the digital image sensors. Several ways have been proposed; however none of these have been able to produce good enough results to match the performance of human eye. This thesis explores ways to capture the wide dynamic range available in nature through digital cameras. The next section of this chapter introduces various technologies used for manufacturing digital cameras. In the third section of the chapter, designs proposed to manufacture wide dynamic range sensors are investigated. The last section of the chapter provides an overview of the thesis and outlines the

goal and methodology of the study.

1.2 Process technologies

Charge Coupled Devices (CCD) and Complementary Metal Oxide Semiconductor (CMOS) based sensors have been the major contending technologies for imaging. CCDs are essentially an array of closely spaced MOS capacitors, in the form of photo-diodes or photo-gates [6]. The photogenerated charge is physically transferred from these capacitors to a common output structure, which converts it into a voltage or current. A typical CCD structure consists of a p-substrate on which an n-type region is formed, as shown in Figure 1.2(a). Overlying this structure is a thin silicon dioxide layer covered by a layer of metal or heavily doped polycrystalline silicon, which forms a gate structure. To capture an image using this device, a four step procedure consisting of charge generation, charge collection, charge transfer and charge detection is utilised.

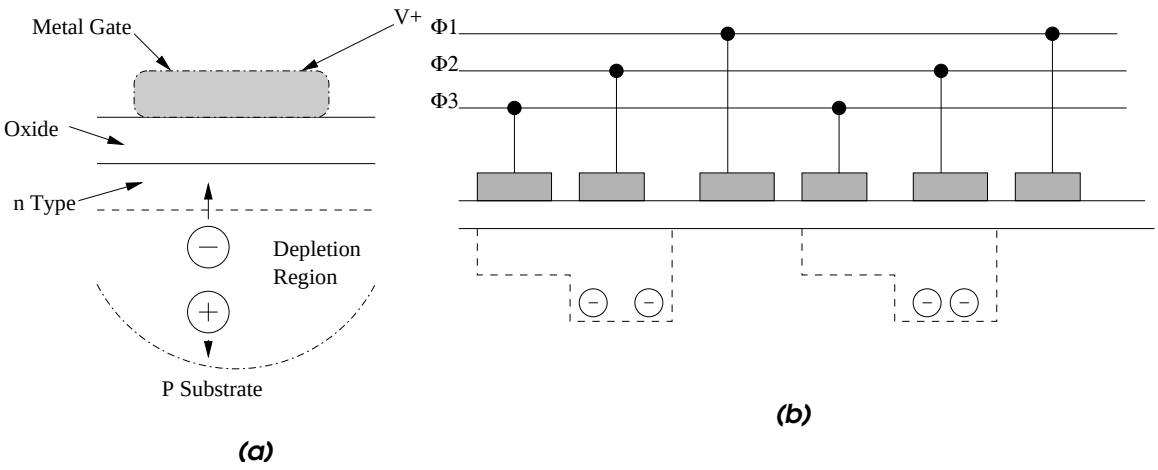

Figure 1.2: (a) A CCD pixel (b) Clocking circuitry and charge transfer in a CCD pixel

When a positive voltage is applied on the gate structure of the CCD, the electric field produces a depletion region by repelling the mobile holes. When light falls on the CCD, the optically generated electrons accumulate in this depletion region, near the $Si - SiO_2$ interface. This collected charge can be transferred to a neighbouring gate by applying a lower potential

at the gate. Thus, charge read in a column can be laterally shifted and serially readout. Finally charge is converted into a voltage and digitally encoded.

The simplest CCD pixel, hence, consists of three polysilicon gates, between two channel stop region, one gate to transmit($\phi 3$), one gate to receive($\phi 2$) and another gate to act as a barrier between two pairs of transmit-receive gates ($\phi 1$) at the time of charge transfer, as shown in Figure 1.2(b). The clocks change their roles in a cyclic fashion. Thus, several clock phases are required for complete data capture. Other formats having one, two or four poly gates in the CCDs have also been used.

Charge coupled devices are manufactured in special purpose process and may also be used in other applications like data storage. However, their success in other products has been limited and hence most CCD foundries are used exclusively for image sensors. CMOS pixels, on the other hand, are made in the standard CMOS processes which are widely used for digital and analogue circuits. A wide variety of circuits capable of converting light into an electrical quantity have been designed in this process. The photodetectors offered in this technology include photodiodes, phototransistors and photogates. In-pixel circuits are often deigned for various signal processing applications including amplification, compression, filtering and digitization.

The simplest CMOS sensor consists of an array of photodetectors connected through a switch. These are referred to as Passive Pixel Sensors (PPS) and have been have been known since 1967, the early days of CCDs [7]. A typical passive pixel sensor has been shown in Figure 1.3. The readout and reset operations in these arrays are performed by a single off-array circuit, thereby having a similar readout structure as that of the CCDs. However, the external circuit and the shift register to scan through the pixels can be designed on the same chip. Similar to the CCDs, these pixels offer a large area for light capture, close to 90% of the total pixel area. The response of pixels in the array is fairly uniform as well. However, the sensor suffers from very low speed owing to high impedances in the readout lines. The photocurrent generated is often very small and hence it requires a long settling time to charge these impedances. These arrays are also very sensitive to interference in the column line, leading to severe degradation in the signal to noise ratio (SNR).

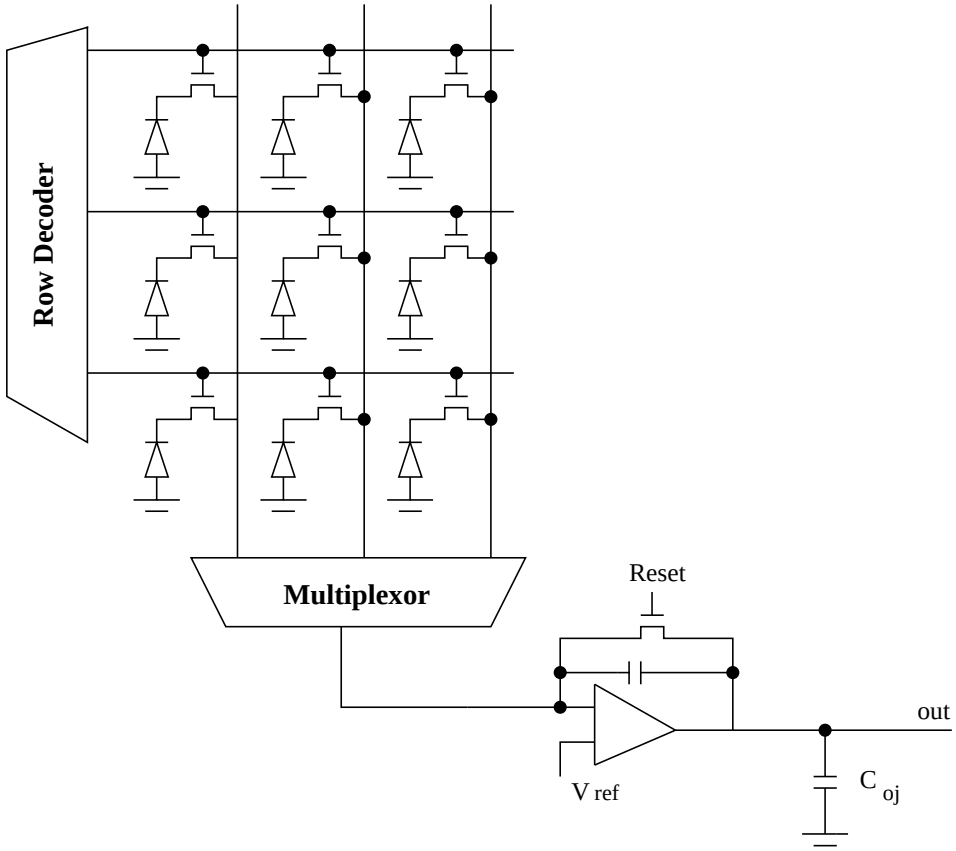

Figure 1.3: A typical passive pixel sensor

Problems with passive pixels led to the development of active pixels, wherein the photosignal is processed in the pixel before transmitting it outside the array. The majority of sensors in the market belong to this type and are referred to as the Active Pixel Sensors (APS) [8]. Of these, most integrate the photogenerated charge on a capacitor, and reset this capacitor to a known value after the readout. A simple active pixel sensor is shown in Figure 1.4. Here, device $M1$ is used to reset the photodiode capacitor to a high value. Device $M2$ acts as a source follower and device $M3$ is used as a switch to select a particular pixel. In a two-dimensional array of these pixels, a second stage of readout structures, preferably made of pMOS type source-follower switch combination, is used in every column of the array.

The pixel operation can be understood with the help of Figure 1.4. By pulling the Rst signal high on the gate of the reset device $M1$, the photodiode node $N1$ is also pulled high. The pixel is then known to have been reset between this time and $t2$. At time $t2$, the reset node

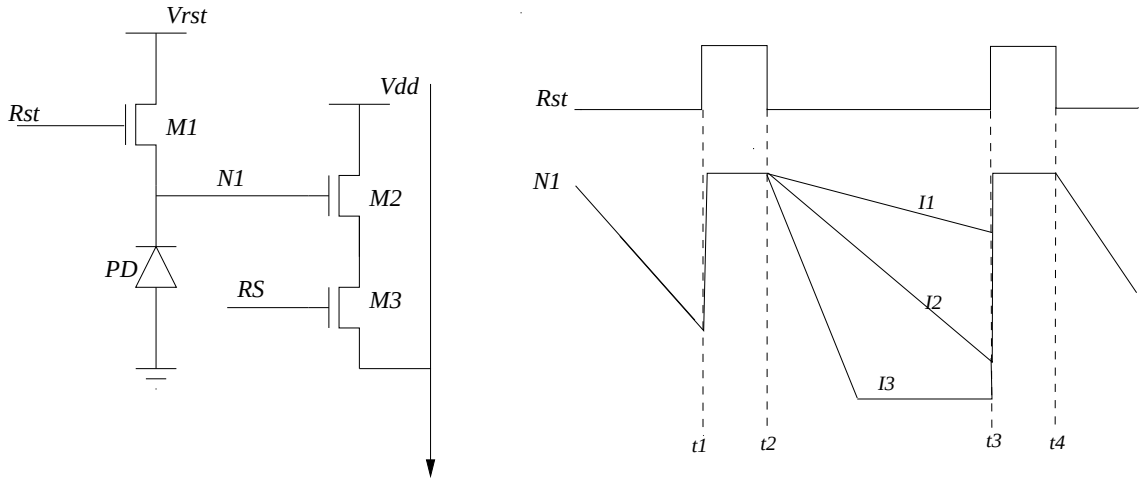

Figure 1.4: A typical active pixel sensor (APS) and signal flows during photocapture

is pulled down disconnecting the node $N1$ from signal, V_{rst}, which is often connected to the power supply. Between times $t2$ and $t3$, the charge generated in the diode due to the incident light integrates on the node $N1$. At $t3$, the node voltage at $N1$ is again pulled high, thereby resetting the pixel. The voltage at node, $N1$ at the end of the integration time is read out as the pixel output. This voltage provides an indicator of input illumination as per the following equation.

$$V_{N1} = V_{reset} - \frac{t_{int} I_{PD}}{C_{PD}} \tag{1.1}$$

Here, V_{reset} is the reset value at $N1$ at time $t2$, t_{int} is the integration time $t3 - t2$, I_{PD} is the photocurrent generated due to incident light and C_{PD} is the capacitance of the photodiode. The pixel output is thus linearly dependent on the input illumination. In Figure 1.4, pixel response to three different photocurrents has been shown. For the lower photocurrent, $I1$, the output voltage is higher than the higher photocurrent $I2$. Further, for currents higher than a particular value (for example $I3$ in the figure) the pixel output saturates to a constant value

Table 1.2 compares the performance of the two technologies. The comparison indicates that pixels in CCD technology have higher fill factor that is more area is devoted to light detection than the CMOS APS. A high fill factor results in high sensitivity. Another advantage of CCDs is the low fixed pattern noise (FPN). This noise arises due to the variations in the devices used in

Criterion	CCD	CMOS APS	Explanation
Cost	High	Low	CMOS process is less costly due to its wide use
Installed base of production	Low	High	Hence increasing production should cut down costs by a higher margin.
Supply Voltage	High	Low	
Power Usage	High	Low	
Integration	Not Possible	Possible	CMOS can thus produce a complete imaging system on a single chip
Downscaling	Poor	Better	Making multi-mega pixel camera is thus easier in CMOS than in CCDs
Image lag	Present	Absent	Incomplete charge transfer in CCD
Market Perspective	Better	Improving	Long existence of CCD
Fixed pattern noise	Low	High	CMOS pixels are more sensitive to mismatch between circuit elements
Temporal noise	Lower	Higher	CCDs do not have the circuit noise of CMOS and remove white noise with an off-chip filter
Fill factor	High	Low	In CMOS, considerable space is used by non-photocircuits
Responsivity	Moderate	Slightly better	
Dark current	Low	High	CCDs have dedicated process
Speed	Low	High	CMOS reduces transmission delays by integration
Uniform Shutter	Fast and common	Poor	CCDs can hence start and stop exposure arbitrarily
Biasing and clocking	Multiple high voltages	Single low voltage	
Windowing	Not Possible	Possible	Parts of array is capturable in CMOS

Table 1.2: Comparison of CCD and CMOS technologies for imaging purposes

the array, thereby leading to a non-uniform ‘salt and pepper’ response to uniform light. Devices in a CMOS process suffer much higher FPN than the CCDs. In addition, CCD processes have been optimized for low dark current and high sensitivity to the input light. These developments made CCD the technology of choice for imaging applications for about two decades. However, having specialized manufacturing process increases the cost of production of the CCDs. CMOS processes are used to manufacture a wide variety of circuits and hence the initial investment needed is evenly spread out thereby reducing the cost of individual chips produced. Further, charge transfer in CCDs requires external biasing and clocking schemes often with high volt-

ages. This increases the net power consumption of a CCD imaging system.

CMOS sensors, on the other hand, have the advantage of being able to integrate clocking circuits on the same substrate and hence are able to work at much lower power. Additional low power gains are expected to be made as the feature size in these process reduces. This reduction in geometry being pushed by the need of high speed digital applications also means that the CMOS image sensors would scale down faster than the CCDs. CMOS is also capable of integrating several other processing elements on the same chip, thereby performing several image processing tasks.

In the past, CMOS sensors had poorer imaging characteristics compared to CCDs, which meant the image sensors manufactured in CMOS process concentrated only in markets requiring lower performance and low cost (such as PC cameras, toys and early mobile phone-cameras). Recent technological developments, however, have improved the optical properties of the CMOS process and it is now making headway in all forms of the digital cameras being produced, including the market that has traditionally been the stronghold of CCDs, the digital still camera. Though CCDs are still the favourite technology to manufacture high end cameras, the market growth of the CMOS cameras has been faster and they have replaced CCDs in the low and medium performance market. In 2004, unit shipments of CMOS image sensors surpassed those of CCDs and the trend is expected to continue in the coming years [9]. It is predicted that CMOS will eventually popularise every spectrum of market, with CCDs maintaining a niche in the production of specific products.

Both technological and commercial perspectives indicate that CMOS will be the future technology of choice for imaging applications. As far as the wide dynamic range imagers are concerned, CMOS provides the added incentives of being able to improve the pixel circuit and the facility of implementing additional modules on the same chip. Thus any post-processing required to increase the dynamic range may be performed with minimum loss in the signal. In the basic structure, CCDs have slightly higher dynamic range (60-70 dB) than CMOS sensors (50-60 dB). However, their dynamic range is limited by the well capacity and hence can not be improved upon, without post-processing using multiple frame capture. Thus, in order to cap-

ture more than 150 dB of the dynamic range available in nature, it is preferable to utilise CMOS sensors. This thesis will, hence, concentrate on designs using CMOS process to improve the dynamic range of the digital cameras.

1.3 Wide dynamic range sensors

Revisiting the CMOS active pixel sensor and its functioning, shown in the Figure 1.4, one may observe that for very high input intensity, $I3$, the readout node saturates to a fixed value. Hence, the pixel is unable to capture photogenerated charge higher than a particular limit. This charge is often referred to as the saturation charge, Q_{sat} or the well capacity of the pixel. The minimum intensity that a pixel can capture is determined by the leakage current flowing in the diode with no incident illumination. In addition, the temporal noise in the pixel and the readout chain also affects the minimum reliable capturable intensity. Thus, the best case dynamic range of the pixel is bounded between the leakage current and a maximum photocurrent determined by the saturation charge.

Typical sensors using the basic architecture have reported dynamic range between 50-60 dB, which corresponds to 2-3 decades of input illumination. Theoretically, the largest imagable photocurrent in an active pixel sensor can be increased by either decreasing the integration time and/or increasing the capacitor of the photodiode. However, this also increases the lowest detectable photocurrent, thereby causing no difference to the net dynamic range of the pixel. There have been several techniques proposed to increase the highest capturable photocurrent without affecting the lowest detectable current.

1.3.1 Well capacity adjustment sensors

One way of increasing the dynamic range of CCDs has been to increase the well capacity by changing the reset signal one or more times during the integration period [10]. In a similar approach, Decker and co-workers have changed the reset signal (referred to as barrier signal by the authors with the reset device acting as an overflow gate) at a rate increasing with time over

the period of integration [11]. This changes the charge barrier at every change of reset voltage thereby resulting in non-linear integration of the pixel charge. Figure 1.5 shows a stepped barrier along with the pixel charge at different light intensities. Similar technique of using variable height multiple reset signals is used by Cypress semiconductors IM-103 image sensor (previously from SMaL Camera Technologies) [12]. A significantly high dynamic range is obtained; however, this increase is at the cost of reducing the signal to noise ratio. The adjustment in the reset signal brings in more temporal as well as fixed pattern noise. The non-linear stepped response of the sensor also makes colour reproduction an involved task.

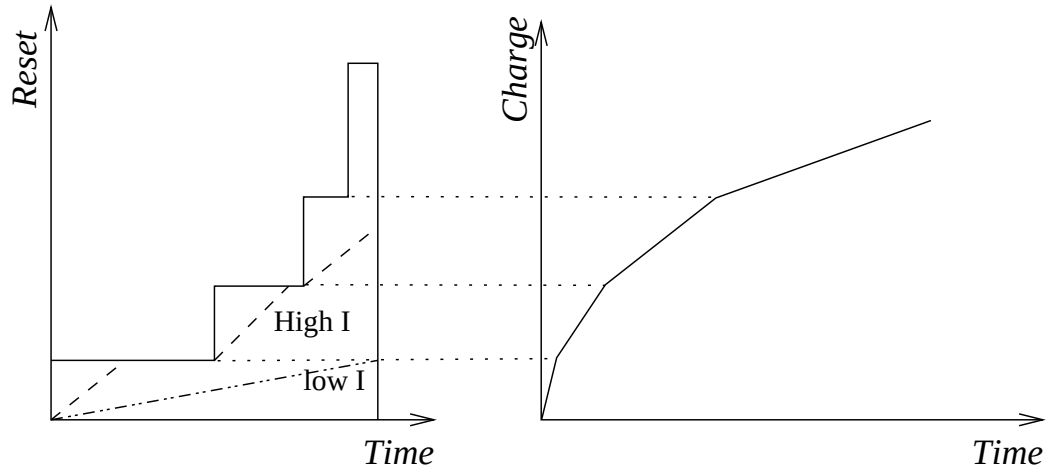

Figure 1.5: A stepped reset signal and corresponding collected charge used to enhance the dynamic range of the sensor

In a similar approach, Guidash has proposed a scheme to utilise the spilled over charge from a saturated pixel [13]. One problem caused by high dynamic range scenes in integrating pixels is over saturation. In an over-saturated pixel, charge may spill over to the neighbouring pixels, the phenomenon being known as blooming. In the proposed system, the charge that blooms from the photodetector is integrated for a period that is controlled independently from the photodetector integration time. This collected blooming charge is added to the photodetector signal charge in the readout of the pixel. Effectively, this scheme increases the well capacity. However, additional noise sources, both temporal as well as fixed pattern, cripple the system. Further, signal reconstruction is also complicated with two different independent integration times.

1.3.2 Dual and multi sampling sensors

Another approach which has been extensively used to increase the dynamic range of the linear active pixel sensor is to capture the same image two or more times with different integration times. The principle is to use a short integration time to capture the high intensity regions of the image and a long integration times for the low intensity regions. Yadid-pecht and Fossum have taken two samples of the same scene with different integration times [14]. Their architecture uses two capacitor banks to store the outputs from two different rows which have undergone integration for different periods. The intra-scene dynamic range of the sensor can be computed from the ratio of the two integration times. The resulting data from samples with different integration time can be fitted into one image by using algorithms from Schery and co-workers [15].

In a multi-sampling approach, Yang and el-Gamal have introduced non-linearity through an in-pixel analogue to digital converter [16]. The researchers refer to their sensor as digital pixel sensor, as an ADC is implemented in every pixel. The pixel response is sampled at exponentially increasing exposure times $T, 2T, ..., 2^kT$ and is digitized in the pixel into m bits of binary data. The total response of the pixel is thus in the form of a floating number with length of $m + k$ bits. Wide dynamic range has been demonstrated using 9 multiple samples of the same image. In a related work, Liu and El Gamal have described a method to estimate the photocurrent in an active pixel sensor by using multiple samples of an image [17]. This can, in turn, be used to improve the dynamic range of the sensor. To improve the performance of multiple sampling techniques, Acosta-Serafini and co-workers have described a predictive algorithm to automatically find an optimal integration time (the longest integration time for which the pixel does not saturate) for a pixel receiving an unknown illumination [18]. They propose the division of the total integration time into slots of different durations and use an iterative procedure to select the longest integration time before the pixel saturates. An on-chip SRAM is used to store the integration information. However, this RAM reduces the effective photosensitive area on the chip.

Dual and multi-sampling approaches improve the dynamic range of the pixel. However, the requirement of several integration frames reduces the frame rate of the pixel, thereby making

it inapplicable in video and other fast capture application. To remove the need of multiple frames, Mase and co-workers have utilised a fast readout circuit to capture pixel output after four different exposure times in the same frame [19]. However, extensive post processing is still needed to estimate the illumination intensity. Colour reproduction and any additional processing are also complicated and not trustworthy in such sensors.

1.3.3 Integration time control sensors

Attempts have also been made to control the integration time of the active pixels to enhance the dynamic range. Sensors with global shutters, wherein the exposure time is changed globally depending on the average intensity of the image, have been proposed as one way to control the integration time [20, 21]. Local adaptation of integration time has also been used to compensate for problems with global integration time. Yadid-pecht has used automatic control of integration time, wherein a non-destructive readout from the photo-pixel is compared to a threshold, the result of which may generate a conditional reset pulse [22]. The camera presented by Scanz and co-workers [23], has the capability of selecting the optimum integration time and gains individually for each pixel through a column switched capacitor amplifier. There are four different integration time and gain factors to select from in their architecture. The response of the pixel array thus contains 10 bits of pixel output, 2 bits of integration time information and 2 bits of gain information, obtaining dynamic range in excess of 100dB with these 14 bits. Another way proposed to improve dynamic range has been to introduce extra pixel reset in order to selectively remove some charge and restart integration [24]. These pixels use a soft reset midway through an integration cycle to remove some of the integrated charge thereby providing the well an ability to integrate additional charge.

The integration time control sensors also suffer extensively from fixed pattern noise problems. These are not only due to mismatch in circuit elements but also due to as integration time mismatch between pixels. Pixels having comparator circuits have added mismatch from comparator performance. In addition, the extra pre and post processing required degrades the applicability of such pixels.

1.3.4 Threshold comparing pixels

In another approach, the photocurrent is integrated only till the output reaches a known threshold value detected by a voltage comparator [25, 26, 27]. Hynecek has proposed a provision for resetting the pixel only when the accumulated charge exceeds a certain threshold voltage and ignore the reset at all other instances [26]. In another approach, Andoh and co-workers count the number of times, a pixel saturates in a given frame as a measurement for higher intensities [28]. In another approach, Stopa and co-workers have used the time taken for the comparator to switch as a measure of the input signal at high intensities. At low intensities, however, the capacitor voltage is used as output [27]. They use two time coding ramps to remove the need of any external memory. As shown in Figure 1.6, one of these ramps covers a 1-V range N times, with an alternately increasing or decreasing linear behaviour, changing its slope at instants $T, 2T, ..., 2^{N-2}T$. The other ramp monotonically decreases in the 1 V range, in voltage steps of $1/N$ V. Thus, the second ramp discriminates between several different time intervals, while the first provides a finer resolution between the two. Dynamic Range in excess of 120 dB has been reported.

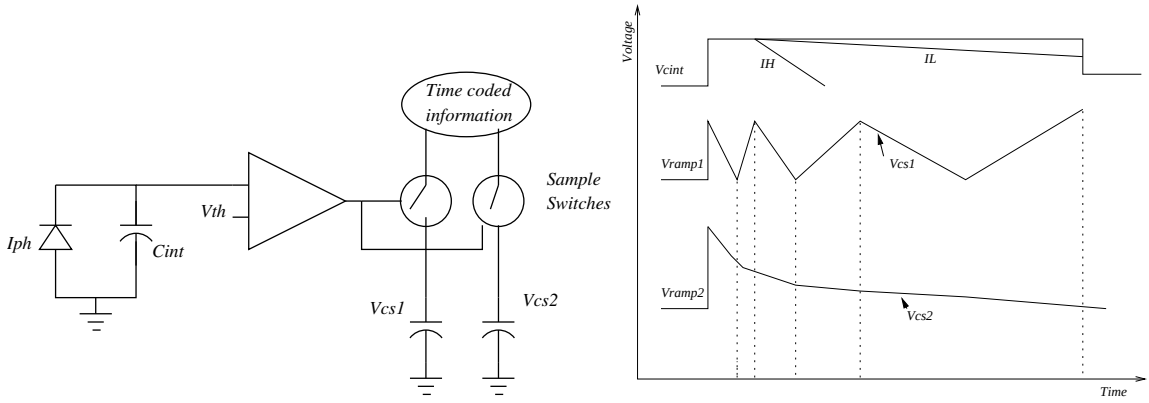

Figure 1.6: Pixel and various ramps in a ramp based piecewise linear mapping high dynamic range sensor proposed by Stopa and co-workers

In a similar approach Anaxagoras and Allinson have proposed an active pixel which resets every time it saturates [29]. A counter is used to measure the number of saturations. This count in combination with the final pixel output is used to extend the dynamic range of the pixel.

These approaches have also been extended to systems utilising readout mechanisms similar to the human visual system. These utilise pixels that produce a spike when their output reaches a threshold [30, 31]. In yet another approach, a high speed clock is used to measure the time to reach a threshold [32].

These approaches are capable of measuring wide dynamic range, however, at a price of large pixels with a small area devoted to light capture. This means that their sensitivity is very low. Use of several devices also raised the issue of uniformity of pixel responses. Post-processing and additional clock signal required are other limitations of these systems. Colour processing is also an involved operation with these pixels. Pixels utilising spiking approach are crippled by the use of two-dimensional readout, as they are unable to distinguish between two pixels firing at the same time.

1.3.5 Frequency based sensors

Some attempts have also been made to use frequency output as a measure of dynamic range [33, 34]. Yang has used an integrate-and-reset circuit, as shown in Figure 1.7 to produce a pulse frequency output over 5-6 decades [33]. However, these pixels suffer from severe fixed pattern noise owing to large number of circuit elements. Further, large pixel sizes, reduce the fill factor thereby reducing the camera resolution. The signal output also requires port-processing for proper display of images.

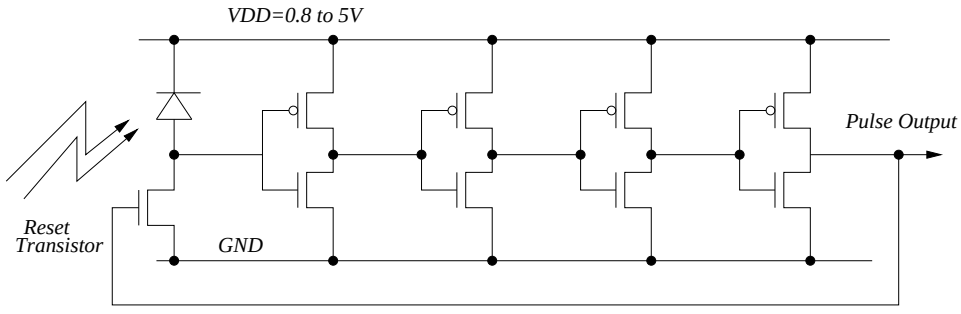

Figure 1.7: A pixel of wide dynamic range sensors having frequency output

1.3.6 Logarithmic Sensors

Approaches described above try to enhance the dynamic range of the linear imager and hence produce a linear relationship between the output and the input intensity. A major disadvantage of these approaches is that the data produced needs to be compressed at a later stage. If not compressed in the analogue domain, a large number of bits are required after digitising the signal in order to represent the wide dynamic range. This disadvantage is solved by pixels which logarithmically compress the signal in the pixel. The most popular way to create a logarithmic output is to utilise a MOS device working in weak inversion, which has a logarithmic relationship between its drain current and gate-source voltage [35, 36, 37]. The simplest logarithmic pixel, shown in Figure 1.8, uses a similar circuit as that of the active pixel sensor except for the gate of the load transistor, which is shorted to the drain. Photogenerated current from diode PD is fed to the subthreshold transistor, $M1$, which then produces a voltage output at node $N1$, which is logarithmically related to the photocurrent.

$$V_{S,M1}(orV_{G,M2}) = V_{G,M1} - V_{T,M1} - \frac{nkT}{q}\log\left(I_{DS,M1}/I_{DSO,M1}\right) \tag{1.2}$$

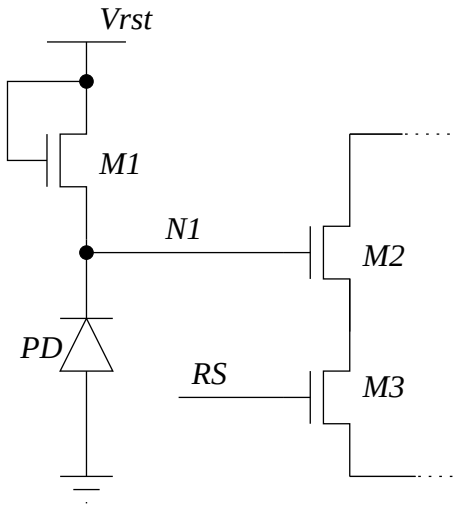

Figure 1.8: A lypical logarithmic pixel using a nMOS in weak inversion

In this expression, $I_{DSO,M1}$ is the current flowing in the device $M1$, when the gate-source voltage of the device equals its threshold voltage and hence the device is making its transition from weak inversion to moderate inversion. k is the Boltzmann constant, T is the absolute

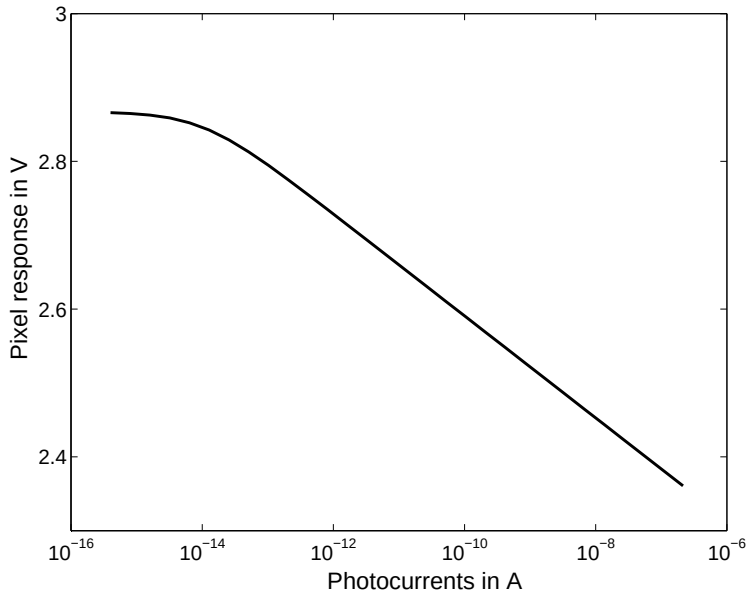

Figure 1.9: A typical response of a logarithmic pixel simulated using cadence with parameters from 0.35μm CMOS technology

temperature, q is the electronic charge constant and n is the subthreshold slope. The readout mechanism is similar to that of active pixel sensors. The response of this pixel has been plotted in Figure 1.9.

Logarithmic pixels are capable of capturing more than 6 decades of light intensities. In addition to requiring less number of bits to represent the wide dynamic range, these pixels offer several other advantages over their linear counterparts. They do not require any additional circuit element in the pixel and hence can achieve fill factors comparable to active pixel sensors. They also provide random addressability as they have continuous operation. Compared with other active pixels, these pixels do not need any clocking circuitry (except the scanning circuitry) and thus minimise any noise associated with the clock jitter and switching noise. Problems associated with saturation, like blooming, are also absent in these pixels. In addition, these pixels have similar logarithmic response as that of human eye and hence neuromorphic signal processing is easy to perform on the output of these sensors.

1.4 Aim and organisation

	Fixed Pattern Noise	Additional Circuits Needed	Additional Clocks Needed	Require Post Processing	Random Addressability	Provide In-pixel Compression
Anti Blooming Sensor	Low	Yes	Yes	Yes	No	No
Multi Sampling	Low	No	Yes	Yes	No	No
Integration Time Control	Low	Yes	Yes	Yes	No	No
Frequency Based	High	Yes	No	Yes	Yes	No
Threshold Based	High	Yes	Yes	Yes	Yes	No
Logarithmic	High	No	No	No	yes	Yes

Table 1.3: Comparison of various wide dynamic range sensors

Table 1.3 compares various approaches described earlier to wide dynamic range imaging based on five first order performance criteria. It may be observed that logarithmic pixel performs better than other approaches on all counts except for the fixed pattern noise. Several commercial products using logarithmic image capture has been introduced in the market, including Fuga from Fill Factory [38], HDRC imager from IMS Chips [39] and Pupilla from Neuricam [40]. However, their success in the market has been limited. One of the principal reasons for this lack of success has been the high level of fixed pattern noise in these cameras. Hence, the first goal of this thesis is to improve the performance of these logarithmic pixels by reducing their fixed pattern noise. These pixels are henceforth referred to as logCMOS pixels for convenience. Fixed pattern noise in pixel arrays owes its origins to the mismatch between devices manufactured in a typical CMOS process. The second chapter of this thesis identifies the devices in a logCMOS pixel that are susceptible to mismatch and studies their role in producing fixed pattern noise in the end image. Various approaches proposed in literature to correct this noise are also reviewed in this chapter.

Chapter 3 of this thesis works towards a simple yet effective technique to reduce the fixed pattern noise. An ideal measure for residual fixed pattern noise is first identified. Mathematical analysis based on this new measure and experiments with typical pixels are performed to identify the causes of failures of the various techniques proposed in literature to reduce FPN.

Alternative readout circuit aimed at improving these techniques are then reported. The primary conclusion from these studies is that one has to correct for the additive as well as multiplicative FPN in order to produce a good quality image. An electronic calibration circuit with these capabilities is then proposed and experimentally verified in chapter 4.

Despite the good results from the calibration process, the logCMOS pixel still suffers from high dark current in a typical CMOS process. These are investigated in Chapter 5 of this thesis. It begins by examining sources of the dark current. Thereafter, it examines various attempts to reduce these dark currents. It is observed that majority of these techniques propose modification of the manufacturing process. However, this is costly. Hence, the chapter works towards circuit and layout based techniques to reduce the effect of dark current. A double current mirror circuit is first tested. It holds the promise of maintaining zero potential across the diode, thereby reducing the effect of the leakage current on the pixel performance.

Layout techniques involving guard ring of polysilicon around the photodiode are also investigated. Significant reduction in the leakage currents is observed. By reusing the guard ring as a reset device, it is observed that the new layout can be used as a pixel having linear response for low intensities and logarithmic response for high intensities.

Chapter 6 is devoted to characterisation of this new response. For convenience, the new response pixels are referred as LLCMOS pixels. The response is first compared to that of typical logarithmic pixel. Various models are then derived and verified to represent this unique response. The penultimate chapter of this thesis, chapter 7 examines the behaviour of LLCMOS pixels with reference to various noise sources, both temporal as well as fixed pattern. Strategies to reduce these noises are proposed and verified. In order to reduce the FPN, the chapter also proposes an intelligent iterative scheme to calculate the photocurrent flowing in the pixel from its output and the complex model derived earlier.

The final chapter of the thesis, Chapter 8, provides the conclusion of the thesis. It summarises the results of the thesis and proposes various directions for possible future research. There are two appendices. The first of these describes the two chips used for various experiments. The second appendix lists various publications from the thesis.

Chapter 2

Fixed Pattern Noise in Logarithmic Sensors

Tis hard to say, if greater Want of Skill
Appear in Writing or in Judging ill,
But, of the two, less dang'rous is th' Offence,
To tire our Patience, than mis-lead our Sense:
Alexander Pope

One of the major constraints in designing pixels in CMOS technology is to design small pixels in order to increase the spatial resolution of the imager. Further, the photodiode area within each pixel has to be maximised to maximise the amount of light capture. This means that the non-photosensitive circuits in the pixel should be accommodated in as small an area as possible, prompting the use of the smallest geometry devices available in the technology. However, small geometries introduce a large amount of variation in device features, leading to output characteristics variations, known as mismatch [41, 42, 43, 44]. This mismatch means every pixel in an array will have a different response to the same input intensity. The equivalent noise due to this non-uniform response is time independent and appears as a fixed pattern on the scenes produced by the array. This fixed pattern noise (FPN) is one of the principal limitations of the current logarithmic sensors. This chapter will investigate the sources of this noise and various approaches to reduce it.

The first section of the chapter will explore various sources of FPN in a typical logCMOS

pixel. As described in the previous chapter, the circuits of the logCMOS and the Active Pixel Sensor (APS) pixel are very similar and hence one way to reduce the FPN in logCMOS pixel would be to modify the FPN strategy used in APS sensors for logCMOS sensors. The second section of this chapter provides a brief overview of the predominant technique used to correct FPN in the active pixel sensors. This will be followed by a review of various methods proposed to use this technique or its variants in logCMOS pixels. However, the residual FPN using these techniques has been found to be too high. The third and the fourth sections of this chapter will therefore review some other techniques proposed to reduce the FPN. Techniques which aim to remove the mismatch from the devices in the pixel are covered in section 3 while the section 4 covers a model based correction technique. The former fails to produce good quality images while the later is too impractical to be used in real time.

2.1 Sources of fixed pattern noise

As described earlier, mismatch between devices leads in FPN in the responses of pixels in an array. The principal sources for mismatch between the transistors in a typical CMOS process are the variations in the effective length and width of the devices, impurities in the oxide layer along with the non-uniform distribution of dopant atoms in the bulk [41, 42, 43, 44]. Variations in the length of MOS transistors, in turn, owe their origin to the lateral diffusion of the source and drain implants, while width variations have their sources in the field oxide encroachment in the MOS channel. The non-uniform distribution of dopant atoms means that the devices in different parts of a chip have different concentration of carriers, leading to a spatial location based nonuniformity in their responses. In addition to these two primary sources, several other factors including local mobility fluctuations, oxide granularity, oxide charge and gate dielectric thickness have also been attributed as sources of mismatch [45, 46, 47, 48]. Device orientation and shape has also been found to affect the amount of mismatch.

The standard models for the mismatch quantify it as variations in the threshold voltage, V_T, and current gain factor, β. It has been shown experimentally that both these variations can be

modelled as a Gaussian distribution random processes with zero mean and a variance, which is dependent on the device area [47].

$$\sigma^2(\Delta V_T) = \frac{A_{V_T}^2}{W_{eff}.L_{eff}} \tag{2.1}$$

$$\frac{\sigma^2(\Delta\beta)}{\beta^2} = \frac{A_\beta^2}{W_{eff}.L_{eff}} \tag{2.2}$$

Here, A_{V_T} and A_β are process dependent terms, while W_{eff} and L_{eff} are the effective width and the length of the channel, respectively. It may be observed here that even though the threshold voltage and the current gain factor have similar origins, their variations have been found to be fairly independent of one another. Additional terms have also been added to these simple models to account for widely spaced devices [49, 47] or when the model has been used over wide range of operating conditions and device sizes [50]. Further, in very low geometries, significant deviations from this basic law have also been reported [41, 51]. However, all these models predict that the smaller geometry devices will have large variations in their threshold voltage and current gain factors. Further, these variations are only made worse by large distance between the devices.

For a first order study, these two variations may be used to identify the devices responsible for FPN in logCMOS pixel. Figure 2.1 shows a typical logCMOS pixel with the readout circuits needed to access every pixel in a two-dimensional array. To identify the sources of fixed pattern noise in this circuit, each of the devices in the schematic should be considered. In this pixel, device $M1$ is operated in weak inversion (subthreshold), with its current-voltage relationship being given by [52]

$$I_{DS,M1} = I_{DSO,M1} \exp\left(\frac{V_{GS,M1} - V_{T,M1}}{nkT/q}\right)\left(1 - \exp\frac{V_{DS,M1}}{kT/q}\right) \tag{2.3}$$

Where terms have their usual meaning. It may be observed that the term involving V_{DS} becomes negligible at values larger than a few hundred millivolts at room temperature. Hence, in general

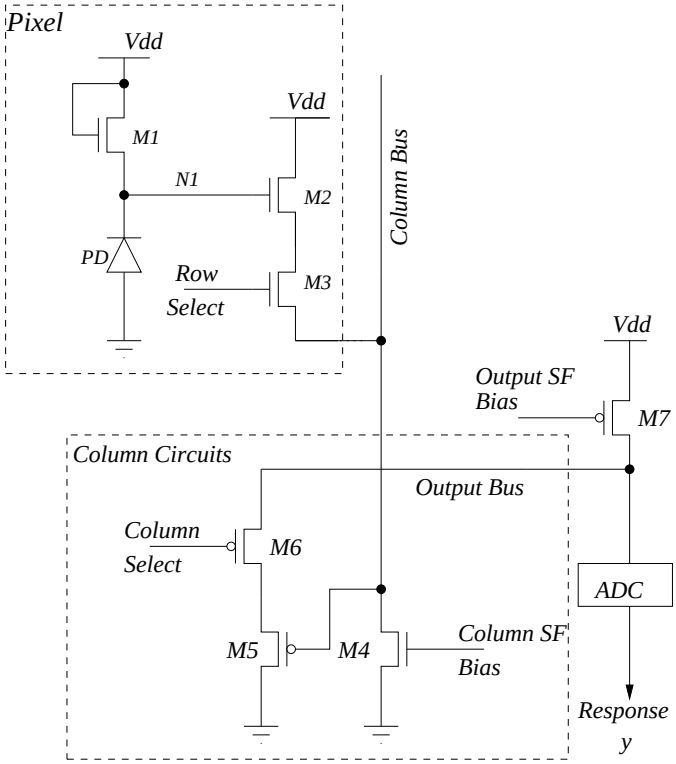

Figure 2.1: Conventional logCMOS pixel with 2 stage source follower readout

operating conditions of the logarithmic pixel, the source or the output voltage may be given by the simple expression

$$V_{S,M1}(or V_{G,M2}) = V_{G,M1} - V_{T,M1} - \frac{nkT}{q}\log\left(I_{DS,M1}/I_{DSO,M1}\right) \tag{2.4}$$

From this equation, it may be concluded that any variations in the threshold voltage of the logarithmic load $M1$, will cause an additive error in the output of these pixels. Assuming no variations in other terms, this error will be a zero mean Gaussian random process with the variance given by the variance of threshold voltage mismatch. The output of the logarithmic load is placed on the column lines using the source follower device, $M2$ and the switch, $M3$. The transfer expression of the source follower may be given as,

$$V_{S,M2} = V_{G,M2} - V_{T,M2} - \sqrt{\frac{2I_{DS,M2}}{\beta_{M2}}} \tag{2.5}$$

It may be observed here that variations in both the threshold voltage and the current gain factor will lead to variations in the output. The third transistor $M3$ of Figure 2.1is a switch used to enable a particular row of pixels to place their output on the column readout line. When on, a similar switch in all other pixels of the same column are off, and the gate voltage, $V_{G,M5}$ of transistor $M5$, equals the source voltage $V_{S,M2}$ of $M2$. Variations in switch resistance may also lead to variations in the output.

The column bus is biased by transistor $M4$ and hence the drain-source currents in $M2$ and $M4$ are same when $M3$ is on. Replacing the current term in equation 2.5 by its equivalent expression in terms of parameters of device $M4$, one may derive the following expression for the output at the end of the column of the array

$$V_{G,M5} = V_{G,M2} - V_{T,M2} - \sqrt{\frac{\beta_{M4}}{\beta_{M2}}}(V_{GS,M4} - V_{TM4}) \tag{2.6}$$

From this equation, it may be deduced that in addition to the FPN caused by mismatch in devices $M1$ and $M2$, threshold voltage variations as well as current gain factor variations from device, $M4$ also lead to FPN. This column current source is the same for every pixel in a column and hence does not cause any variation between the outputs of pixels in one column. However, variations in this device introduce a column to column variation in the output of the array appearing as vertical lines of differing intensities in the output image.

In a two dimensional array, two addressing mechanism are needed to connect a pixel to the single output and hence a second stage of readout circuits needs to be added at the end of every column. In a conventional design, the second stage is designed from pMOS transistors to compensate for the threshold voltage drop in nMOS source follower, $M2$. One such schematic, shown in Figure 2.1 involves transistors $M5$ and $M6$ being present in every column. When transistor $M6$ is switched on, $M5$ is connected to the output bus and the voltage V_{ADC} at the input of the analogue to digital converter. Transistor $M7$ is common to whole array and provides the current bias to the column source followers. Similar to the source follower in pixel, devices in the column source follower also introduce variations in the output due to the variations in

their threshold voltage and current gain factor. The expression for the input at the ADC in the Figure 2.1 may be given as

$$V_{ADC} = V_{G,M5} - V_{T,M5} - \sqrt{\frac{\beta_{M7}}{\beta_{M5}}}(V_{GS,M7} - V_{T,M7}) \tag{2.7}$$

In alternative designs, an ADC is used in every column and the output is digitally multiplexed to increase the speed of operation of the array. This would remove the mismatch due to column readout circuits; however, mismatch in the ADC comparator would become a new source FPN. It should be noted here that the column circuits have lower spatial constraints compared to the pixel circuits and hence it is possible to use large devices to reduce the mismatch. However, at least one dimension of these devices is limited by the pixel pitch and hence will lead to mismatch.

In addition to the response non-uniformity due to transistors characteristics variations, the photodiode may also contribute to the fixed pattern noise in the array. The current produced by the diode, PD, consists of two terms. The first of these is the optical term given by the input intensity multiplied by the quantum efficiency of the diode and various gain terms of the optical assembly. The second is a leakage current produced even in the absence of light and hence is often referred to as the dark current of the pixel.

$$I_{PD} = Q_{PD}G_A A_{PD} G_L L_{opto} + I_{dark} \tag{2.8}$$

Here, Q_{PD} is the quantum efficiency of the material used to make the photodiode, and hence is the intrinsic property of silicon. G_A is the gain factor related to the photodiode area compared to the total area of the pixel, and thus accounts for the amount of light captured by the photodiode or lost due to non-photosensitive parts of the pixel. A_{PD} is the area of the photodiode. G_L is the gain of optical assembly and L_{opto} is the input intensity. G_L and L_{opto} are uniform for all pixels. However, pixel area A_{PD} and area gain G_A, may suffer variations due to changes in geometries of the photodiode.

The dark current term, I_{dark}, has been found to depend on the area and the number of corners in the photodiode [53]. Variations in the photodiode area, hence, introduce another form of fixed pattern noise, predominantly visible in the low intensity regions of a typical world scene. Some camera manufacturers differentiate this nonuniformity from the illumination dependent fixed pattern noise, referring it as the Dark Current Non-Uniformity (DCNU).

From the aforementioned discussion, it is clear that there are several constituents of the logCMOS pixel suffer device mismatch. The standard approach to reduce this mismatch is to use layout techniques like common centroid, finger style interleaved structures, etc [49]. Common centroid layouts help in generating gradual and uniform mismatch over various circuits. It is possible to draw such layouts for few circuits only and hence can not be used for pixel arrays. Further, finger style interleaved structures are suitable for matching small number of transistors only and hence do not offer any solution for a pixel array. Therefore, the only way to reduce the effect of mismatch on pixel performance is to compensate for it through circuit and/or post-processing techniques.

2.2 FPN correction techniques in linear pixels

It is worth recalling here, that the logCMOS pixel has the same readout chain as that of linear Active Pixel Sensor (APS) in the CMOS technology. In addition, the reset switch in the APS also suffers threshold voltage variation, thereby introducing a source of FPN, very similar to the logarithmic load device of logCMOS pixel. Thus, the APS suffers with similar sources of fixed pattern noise. In this context, a good starting point towards reduction of FPN in logCMOS pixel would be to study the techniques used in active pixel sensors to eliminate fixed pattern noise.

Linear pixels operate by integrating the photo generated charge on the diode capacitance. At the beginning of every frame, the voltage on this diode capacitance is reset using a switch. This leads to the following expression for pixel output after the integration time.

$$V_{out} = V_{reset} - G_{pixel} t_{int} I_{PD} \tag{2.9}$$

Here, G_{pixel} is the net gain provided by the photodiode as well as the readout circuit whereas t_{int} is the integration time. Most linear pixels utilise this expression to use some form of double sampling to reduce the fixed pattern noise. The principal assumption in these double sampling techniques is that that the nature of FPN is additive and hence is manifested in the reset value of the pixels read after the readout stages. Thus the simplest way to remove the FPN is to remove the contribution of reset voltage in the output. Two techniques to extract this reset voltage have been used previously. In the first technique, known as differential double sampling (DDS), the output of a row of pixels is read after an integration cycle, and stored on column capacitors. This row is then reset and the reset value is read on another pair of column capacitors. The difference of these two values is computed either using analogue circuits or in the digital domain, leading to FPN free output.

In a modified scheme, an in-pixel memory is used to store the reset value before the integration time. An advantage of using the reset value before the integration time is that that this reset value is noise correlated to the pixel output after integration and hence is capable to reducing the temporal noise along with the fixed pattern noise. This scheme is hence known as correlated double sampling (CDS) [8].

One circuit which is capable of performing CDS is shown in Figure 2.2 with the related signal flow in Figure 2.3. In this circuit, a photogate with transmission switch TX is used as the photo-detector as well as the in-pixel memory. The pixel is reset using the switch $M1$. The transmission switch TX is then closed, and the photo-generated charge is integrated on the capacitance of photogate PG. At the same time, the reset value is held at the node $N1$, using the gate capacitance of device $M2$. At the end of the integration period, a row of pixels is read using the row select switch $M3$ present in every pixel of the row. Initially, the reset value stored on the node $N1$ is transferred to the capacitance CR using the switch SHR. In the next clock cycle, this switch SHR is closed, and sample switch SHS is opened. At the same time, the transmission gate TX is opened. These two switches along with the row select switch transfer the integrated value to the capacitance CS. These sets of capacitances and switches are present in every column. The second stage readout is used to read these values in a way similar to that of

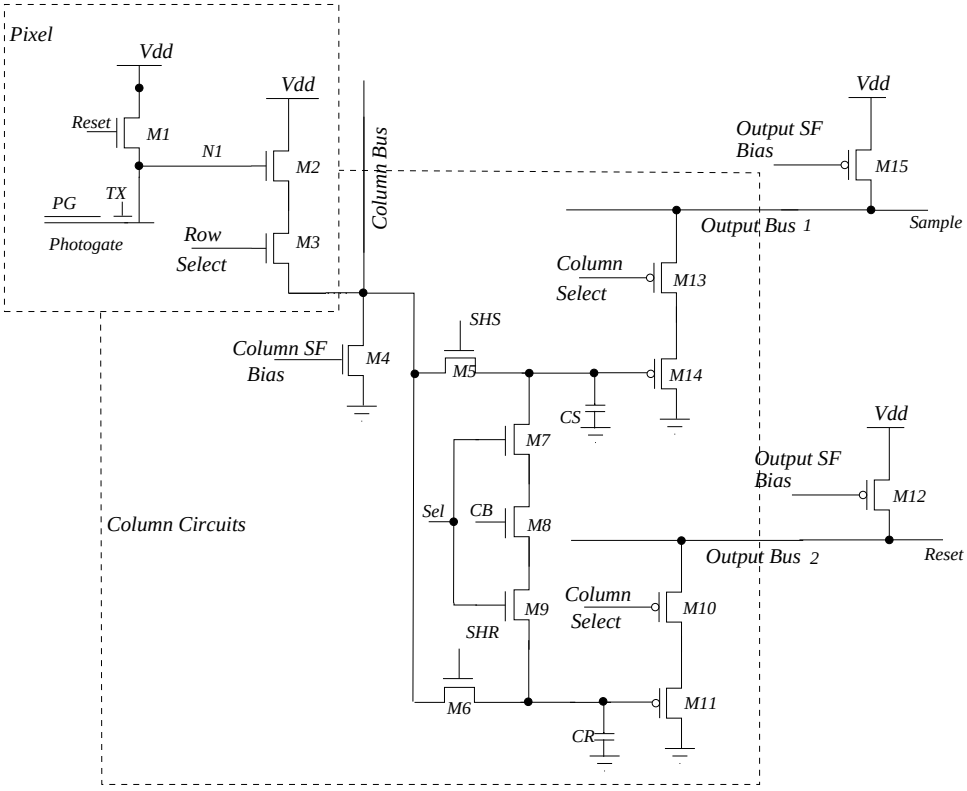

Figure 2.2: An active pixel sensor with readouts to support correlated double sampling

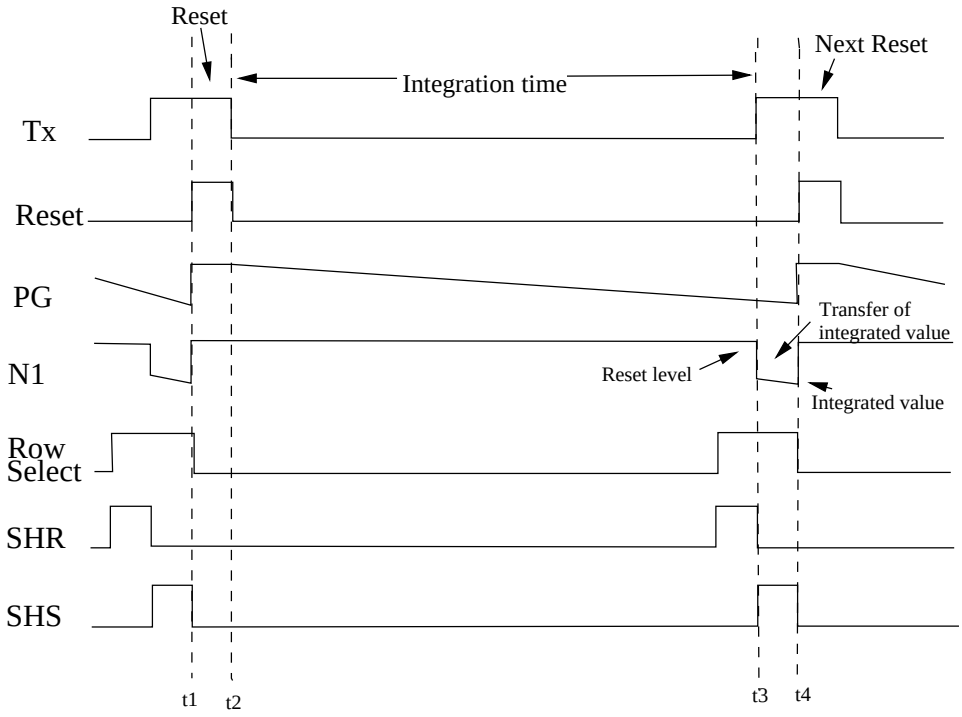

Figure 2.3: Signals flow in a pixel showing correlated double sampling operation

logCMOS pixels. In Figure 2.2, the second stage is designed using column switches, $M10$ and $M13$, pMOS source followers $M11$ and $M14$. In addition to these circuits, transistors $M12$ and $M15$ provide the necessary current to these column current sources. The difference between the reset value and integrated value can be computed either using differential amplifiers or digital subtracters, after digitizing the signal.

The circuit shown in Figure 2.2 also corrects for any possible mismatch between two different readout pathways used by reset and the integrated values. To remove these noises, the crowbar switch $M8$ is used to short the inputs of two different pMOS source followers. The Sel signal is fed by column select lines, thereby selecting a particular column's value on the output bus. With the inputs shorted, the difference between the outputs of the two source followers can be used as a measure of mismatch between the two readout paths. This difference, in turn, can be subtracted from the difference of reset and integrated value to compensate for the fixed pattern noise introduced by the column readout circuits [8].

2.3 Double sampling techniques in logarithmic pixels

The double sampling technique in their simple form can not be used in logarithmic pixel owing to continuous operation of logCMOS pixel and absence of any reference reset value. Researchers have hence tried to modify the pixel to generate a reference value. Kavadias and co-workers have generated a reference output from the pixel by feeding in a high current in the pixel parallel to the photocurrent [54]. This pushes the logarithmic load in moderate inversion and thus provides a reference value from a region outside the normal working regions of the pixel. The difference between these two signals is expected to eliminate all threshold voltage variations. The reported resulting fixed pattern noise was 2.5 % of $V_{sat,rms}$, and the temporal noise obtained was 0.76 % of $V_{sat,rms}$ for pixels of dimension 7.5 μm$\times$10 μm, made in 0.5 μm technology. The residual fixed pattern noise is very high, as with the reported gain, the imager would not be able to differentiate between two points in the image with contrast change of as high as 30%. In addition to this high residual fixed pattern noise, this scheme also suffers from

the serious drawback of transient effects between calibration frame and next readout. This is so because when discharging from a high input current to a low input current, the logarithmic load has a small current to discharge the high voltage difference leading to long settling times. This results in transient noise for all low-intensity regions imaged by the sensor. The variations in this settling time also introduce another source of fixed pattern noise.

Ni and Matou [55] on the other hand generate a dark reference in the pixel, by using a photovoltaic device as the detector as shown in Figure 2.4. Despite the use of dark reference, the settling time effects are still present in the output. The reported residual fixed pattern noise is 6.5mV overall and 2.5mV in a column with the pixel size being 30μm$\times$30μm, (fabricated in 0.8μm technology). In addition to large pixel size, the resultant fixed pattern noise is very high when compared to the small gain of 50mV/decade from these pixels.

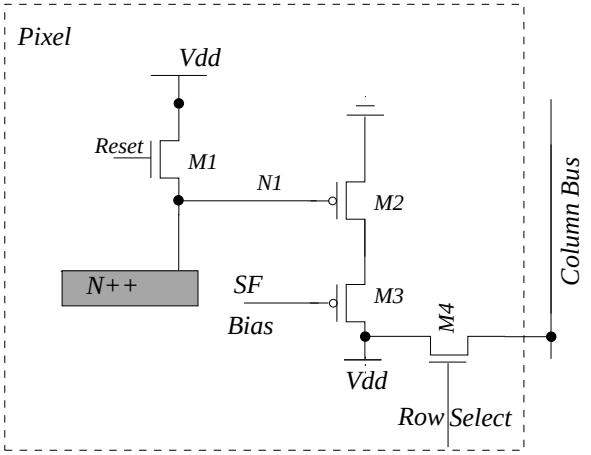

Figure 2.4: A logarithmic pixel using a photovoltaic device as the photosensitive device and having double sampling abilities

In order to remove the settling time effects while using the dark value as the reference value in double sampling, Lai and co-workers have used a lateral PNP BJT structure as the photosensitive element, as shown in Figure 2.5 [56, 57]. They claim to have obtained residual fixed pattern noise of 2.46% $V_{sat,RMS}$, in a pixel with dimensions of 10μm$\times$10μm and a fill factor of 43%. The BJT phototransistor provides a gain to the photocurrent generated. This photoconversion gain is known to have a high variance in BJTs, thereby introducing another source of fixed pattern noise. Further, this gain pushes the logarithmic load in moderate and strong

inversion, whereby it looses its logarithmic characteristics. The residual fixed pattern noise is still very high.

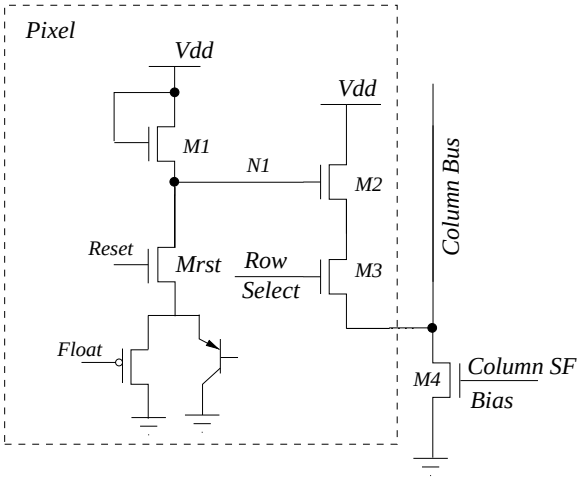

Figure 2.5: A logarithmic pixel using lateral PNP BJT as the photosensitive device and having double sampling abilities

Some off-chip techniques have also tried to use variants of double sampling techniques. Rather than generating a reference at every frame, these techniques store a reference reading from the array illuminated with uniform light in an off-pixel memory [39, 58, 59]. Commercially available logCMOS cameras also calibrate the pixels in a similar way by showing a white paper to the array and storing the response of every pixel in a memory [38, 39]. The pixel output to a scene is subtracted from its white response to produce FPN-free output. The scheme is, however, not automatic and is inconvenient, especially if the camera is remote. Some discrepancies may also result due to uniformity of white paper used, type of light falling on it and angle of paper shown to the pixel array. The residual noise is dependent on the amount of light available during the calibration process.

2.4 Uniform response producing techniques

From the discussions of the previous section, it is clear that the double sampling approaches do not produce good results as far as residual FPN is concerned. In alternative strategies, researchers have tried to remove the source of fixed pattern noise by changing the devices in

the pixel. As discussed earlier, the principal source of FPN is the threshold voltage variations. One way to remove these variations is to use hot carrier degradation, as reported by Ricquer and Dierickx in a 3-transistor logarithmic pixels [60]. However, the reported FPN correction procedure required long stressing times to remove offset variations while using driving signals as high as 16 V. The long time and high power consumption makes this technique difficult to implement and use.

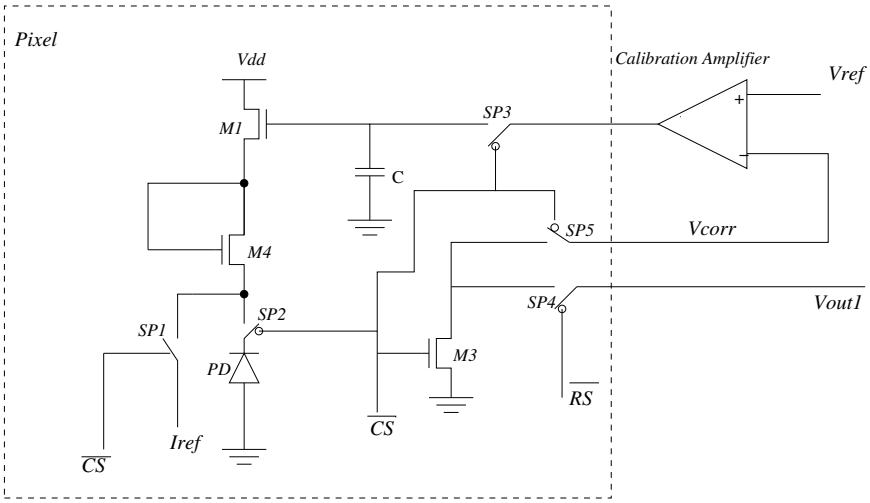

Figure 2.6: In-pixel calibration circuit proposed by Loose and co-workers

In another approach, Loose and co-workers [61] have compensated for threshold voltage variation by using an in-pixel calibration technique. They have described a pixel having two subthreshold loads, the voltage at the gate of one these being adjustable, as shown in Figure 2.6. During calibration, every pixel is stimulated with a reference current using an external current source. The output of these pixels is compared to a reference voltage and gate voltage at the load transistor is adjusted until both the reference and the pixel outputs are same. With a pixel size of 24μm$\times 24\mu$m and a fill factor of 30$\%$ in 0.6μm technology, the reported residual fixed pattern noise is 3.8 $\%$ of a decade(RMS) for the whole array and 2.1 $\%$ per column. This pixel design utilises large pMOS switches and hence has a very small fill factor despite using large pixel size. This means that this pixel will lose most of the input intensity and hence is not a practical design.

2.5 Model based FPN correction

Another approach to reduce FPN has been proposed by Joseph and Collins. They use a three-parameter model to correct the fixed pattern noise in commercial logarithmic cameras [62]. Assuming unity gain of the readout circuit, they have obtained the following form of the response function of the logarithmic pixel.

$$y = a + b\log(x + c) + \epsilon \tag{2.10}$$

In this equation, x represents the photocurrent, which is directly related to the incident light intensity and ϵ is the residual noise in the response. a can be referred to as the offset, b as the gain and c as the bias in the response of the pixel. For the pixel circuit shown in Figure 2.1, these parameters can be expressed in terms on device parameters as follows

$$\begin{aligned} a = F_{ADC} + G_{ADC} \Bigg[& V_{DD} + \frac{n_{M1}kT}{q} \ln\left(\frac{I_{on,M1}}{G_A G_L G_Q A}\right) \\ & - V_{on,M1} - V_{T,M2} - \sqrt{\frac{\beta_{M4}}{\beta_{M2}}}(V_{GS,M4} - V_{T,M4}) \\ & - V_{T,M5} - \sqrt{\frac{\beta_{M7}}{\beta_{M5}}}(V_{GS,M7} - V_{T,M7}) \Bigg] \end{aligned} \tag{2.11}$$

$$b = -G_{ADC}\frac{n_{M1}kT}{q} \tag{2.12}$$

$$c = \frac{I_{dark}}{G_A G_L G_Q A} \tag{2.13}$$

Here, F_{ADC} and G_{ADC} are the offset and gain of the analogue to digital converter, respectively. Other terms have the same meaning as explained earlier. Joseph and Collins further argue that the each of these three terms of offset, gain and bias, contribute towards the fixed pattern noise. They have extracted these parameters from the response of a commercial logarithmic camera to 24 different scenes of uniform intensities. Based on these parameters, they show that offset only correction, as performed by double sampling and threshold voltage correction techniques, are unable to provide high quality images. They hypothesize that this is due to the gain variation of

these pixels being of significant magnitude to be neglected. They further show that correcting for all these parameters reduces the residual fixed pattern noise to levels below that of one LSB in the 8 bit system of the cameras.

Despite the good results obtained by Joseph and Collins, their technique is not very practical. In particular, 24 uniform intensity images are difficult to produce for calibration even in laboratory environment. Further, their scheme can not be used in real time due to requirement of iterative computational techniques.

2.6 Summary

Image sensors suffer from high fixed pattern noise owing to mismatch between the devices used to manufacture these pixels. This mismatch may be modelled as variations in threshold voltage and the current gain factor in the response of the MOS devices. Standard techniques used to reduce the mismatch are unusable in these sensors due to small size constraint and the large format of imagers to be designed.

The similarity between the circuit schematics of linear active pixel sensors and the logarithmic pixels have prompted several researchers to employ the double sampling techniques used in active pixel sensors for FPN correction in logCMOS pixels. However, the residual FPN from these sources is too high to produce good quality image. Other attempts to remove the source of mismatch in the pixels have led to impractical pixel designs while having high residual noise. Model based correction techniques do produce good quality images, however, the iterative and demanding computation required, makes the scheme fairly difficult to apply in real time. Thus, there is a need to further investigate these techniques to produce simple yet effective techniques of reducing FPN in logCMOS sensors.

Chapter 3

FPN Reduction in Logarithmic Sensors

O WHAT has made that sudden noise?
What on the threshold stands?
William Butler Yeats

It has been established in the previous chapter that high fixed pattern noise is one of the major limitations of logCMOS pixels and the techniques proposed in literature to reduce this noise either yield too high residual fixed pattern noise or are too complex to be applicable in real-time cameras. In this chapter, a simple yet effective technique for fixed pattern noise reduction would be devised. Two possible approaches will be investigated. The first of these would be based on the studies of Joseph and Collins which experimentally show that the high residual FPN in offset corrected images is due to the high gain variations in the pixels. The offset only correction techniques would hence be improved by either reducing the gain variations and/or reducing their contributions to the FPN in the end-image. The second approach will be to improve the complexity of multiple parameter correction procedure of Joseph and Collins to produce a good quality image in real-time without using complex computations and need of multiple images. The first approach will be pursued in this chapter and the second in later chapters to identify the best possible technique for FPN correction in logCMOS cameras.

Before any discussion of FPN correction strategy, however, one needs to identify a measure for fixed pattern noise. This is necessitated due to the lack of a standard measure to represent the residual fixed pattern noise, making the task of comparing different techniques and any im-

provements devised, difficult. The first section of this chapter will hence discuss an appropriate measure for fixed pattern noise.

The second section of this chapter will revisit the offset only correction techniques to study the effect of gain variations in the corrected output image. Mathematical analysis of this technique and experiments with an array of logCMOS pixels with the conventional source follower readout circuits will then be presented to identify the sources of gain variation and their effects on the end-image. An improved readout circuit will then be presented to reduce the effects of gain variations on the output image. Experiments performed with an array of these new circuits will also be presented.

3.1 A measure for residual fixed pattern noise

Revisiting the literature review of FPN reduction techniques of section 2.3, one may observe that the residual error, after the correction procedure, has been reported using different measures by different authors. The measures used include $\%$ of the root mean square of the total signal swing as used Kavadias et.al. [54] and Lai et.al [56], mV as used by Ni and Matao [55], $\%$ of a decade as used by Loose et.al. [61], lowest significant bits as used by Joseph and Collins [62], etc. This makes a comparison of these techniques a fairly difficult task.

In order to identify the ideal measure for fixed pattern noise, let us consider the effect of fixed pattern noise on the imaging system. FPN essentially increases the threshold of the minimum intensity level changes, which can be faithfully recorded by the imager. Alternatively, FPN in an image can also be described as an error in the intensity levels as experienced by the end-user. An ideal measure should be able to quantify either or both of these effects. The units used by other researchers measure the output signal level. With no information of the gain of imaging system, it is difficult to predict either the input threshold or the observed output error in the image from these measures alone.

To find a better measure, it is important to understand how the human visual system would perceive the errors due to FPN in an image. The human visual system encodes the contrast of

an image [4], and thus any intensity error in the image is perceived as a contrast error by the viewer. Hence, any measure involving contrast would be able to measure the user-experience due to FPN. One such property of the imaging system is contrast thresholds, which is defined as the smallest input intensity difference, expressed as the percentage of the input intensity, which could be faithfully reproduced by the imager. From this definition, contrast threshold can measure the input differentiability of the image sensor while measuring the end-user experience. Thus, it is a better suited measure for fixed pattern noise.

Further, it is reasonable to argue that any residual FPN more than the contrast performance limit of the human eye would be visible to the end-user. Figure 3.1 shows the contrast performance of the human eye [63]. The human visual system has a best case relative contrast threshold between 1 and 2% and thus a fixed pattern noise reduction strategy will be considered good enough, if it reduces the residual error below this limit. A sensor with this strategy would be able to capture every details of an image visible to the human user. Thus, in addition to being an ideal measure, contrast threshold also provides a benchmark for performance of logarithmic image systems.

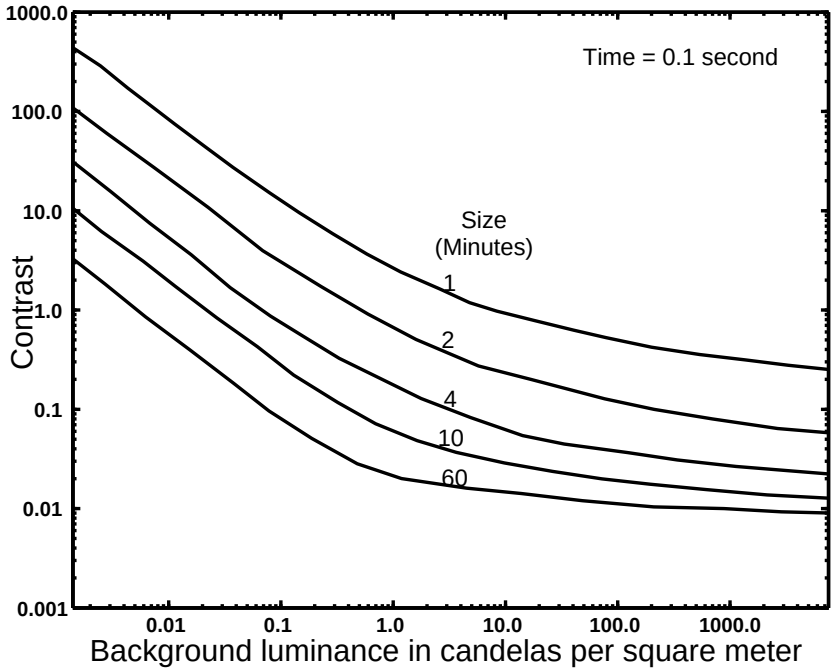

Figure 3.1: The contrast limits of a normal human eye for various sized target

The various measures expressing FPN in terms of output voltage of logCMOS pixels can be related to that of contrast threshold using the response function of logarithmic pixel of equation 2.10. Let us consider a pixel with parameters of offset, gain and bias as a_1, b_1 and c_1. Let us also consider two illuminations x_α and x_β, where the output voltage of the pixel is y_α and y_β, respectively

$$y_\alpha = a_1 + b_1 \log(x_\alpha + c_1) \tag{3.1}$$

$$y_\beta = a_1 + b_1 \log(x_\beta + c_1) \tag{3.2}$$

The contrast, K, of x_α as compared to x_β can be given as

$$K = 1 - \frac{x_\beta}{x_\alpha} \tag{3.3}$$

If the lowest voltage difference which the imager is able to differentiate is that between y_α and y_β, then the contrast given by the aforementioned equation gives the contrast threshold of the imaging system. Using these equations, the double sampling techniques studied earlier will each produce contrast error in excess of 15%. Hence, they are not good enough to produce good quality image.

3.2 The offset-only correction procedures

Joseph and Collins have postulated that the high residual FPN in offset-only correction techniques are caused by the high gain variations in the pixels [62]. A study of the effect of gain variations on the image, with reference to the measure of contrast threshold can be used to investigate this statement. Any offset-only correction technique forces a constant reference current through the load transistor and uses the output at this reference current to correct for the FPN. This reference current takes the form of either a very high current [54] or that of the leakage current with no illumination, I_{dark} (thereby producing the dark response of the pixel) [55, 56]. Let us consider a constant reference current, x_c, through the load transistor of a pixel, which

leads to a response y_c. Subtracting this from the pixel response at an unknown input x_{in} will then lead to a corrected output y_{corr}

$$y_{corr} = y_{in} - y_c = b \log(x_{in}/x_c) \tag{3.4}$$

For mathematical simplicity, the bias term has been assumed to be negligible as compared to x_{in} in the above equation. Neglecting any photodiode variations, the current through all the pixels will be the identical with an input scene of uniform intensity. The corrected output, however, will be identical only if all pixels have the same gain. Unfortunately, variations between the devices within each pixel will lead to gain variations. In order to quantify the effects of gain variations, let us consider a pixel whose gain b differs from the mean pixel gain $\bar{b}$ by Δb. With offset correction only, this gain variation will lead to an error in the corrected output of

$$\Delta y_{corr} = \Delta b \log(x_{in}/x_c) \tag{3.5}$$

The equivalent percentage error, K, in the apparent contrast of this pixel compared to an average pixel is then given by

$$\bar{b} \log\left(1 + \frac{K}{100}\right) = \Delta b \log(x_{in}/x_c) \tag{3.6}$$

For small values of K, the approximation $\log(1 + K) \approx K$ may be used to simplify this expression to

$$K = \frac{100\ \Delta b}{\bar{b}} \log(x_{in}/x_c) \tag{3.7}$$

This equation shows that, since the contrast error depends on the ratio of photocurrent to calibration current, the effects of any gain variations can be limited by using a typical photocurrent as the calibration current. However, changing the reference current depending on the input intensity is difficult to implement and hence most calibration schemes use a typical calibration current to generate the data for fixed pattern noise correction. Since these atypical currents can be as much as six orders of magnitude larger or smaller than a photocurrent these techniques

can only match the contrast sensitivity of the eye if the gain variations between pixels are less than 0.14%.

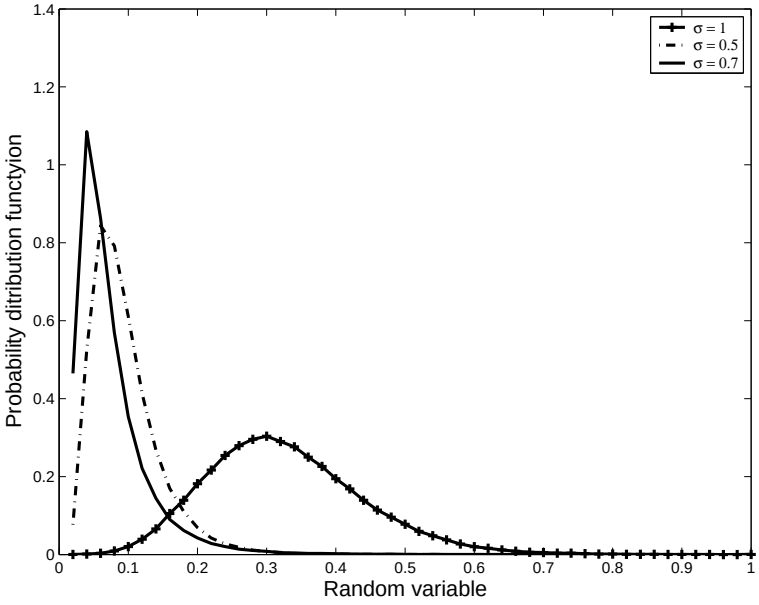

Figure 3.2: Probability density function of a lognormal curve with different variances.

An interesting observation from equation 3.7 is that that the contrast error produced by any double sampling technique is dependent the relative magnitude of the photocurrent with that of the reference current. Hence, the residual FPN is not constant at all photocurrents. This raises a serious problem with researchers citing a constant value of the residual FPN without mentioning the photocurrent flowing through the pixel. There is a possibility that the worst case FPN from these techniques could be far worse than the value quoted. Another interesting observation from equation 3.4 is statistical nature of extracted currents from corrected output. The residual FPN is reported in terms of its first order statistics assuming it to be a Gaussian random process. Now, if $b\log(x_{in}/x_c)$ has to be Gaussian, and b is a constant, x_{in}/x_c becomes a lognormal (or logistic normal) function, whose probability density function is given by

$$f(x;\mu,\sigma) = \frac{1}{x\sigma\sqrt{2\pi}}\exp\left(\frac{-(lnx-\mu)^2}{2\sigma^2}\right) \tag{3.8}$$

where μ andσ are the mean and standard deviation of the variable's (x) logarithm. The expected

value and the variance of the variable, x is given by

$$E(x) = e^{\mu+\sigma^2/2} \quad (3.9)$$

$$var(x) = (e^{\sigma^2}-1)e^{2\mu+\sigma^2} \quad (3.10)$$

Figure 3.2 shows the probability density function of a normalised lognormal function with varying σ. A worrying conclusion from this curve is that the curve could have a long tail for certain σ, thereby leading to high peak errors.

3.3 Conventional source follower readout circuit

3.3.1 Theory

The analysis in the previous section suggests that the gain of the logarithmic pixel is either too low and/or its variability is too high for it to produce good quality images. In equation 2.10, the gain of a logCMOS pixel has been shown to be the subthreshold slope of the load device multiplied by constants. Hence, the gain variations in the pixel outputs should be directly related to the subthreshold slope variations. Studies of mismatch in the subthreshold regime of MOS devices generally ignore these variations, claiming them to be too small compared to variations of other parameters [48, 64].

Variations of low magnitude should lead to good quality images by offset correction only. However, the failure for these schemes suggests that either the subthreshold slope is having large variations and/or there are other sources of gain variations, thereby prompting an inquiry in the model itself. It was assumed in the model derivations, that the readout circuits have a constant unity gain, and hence their contribution on the pixel gain could be ignored. To confirm this assumption, simulations of a typical nMOS source follower readout circuit designed in 0.35μm process were performed using the Spectre simulator of the Cadence tool set. Figure 3.3 shows the simulated source follower output. The gain was observed to be dependent on the bias current; however, it was always less than unity. For typical biasing conditions, it was found to be

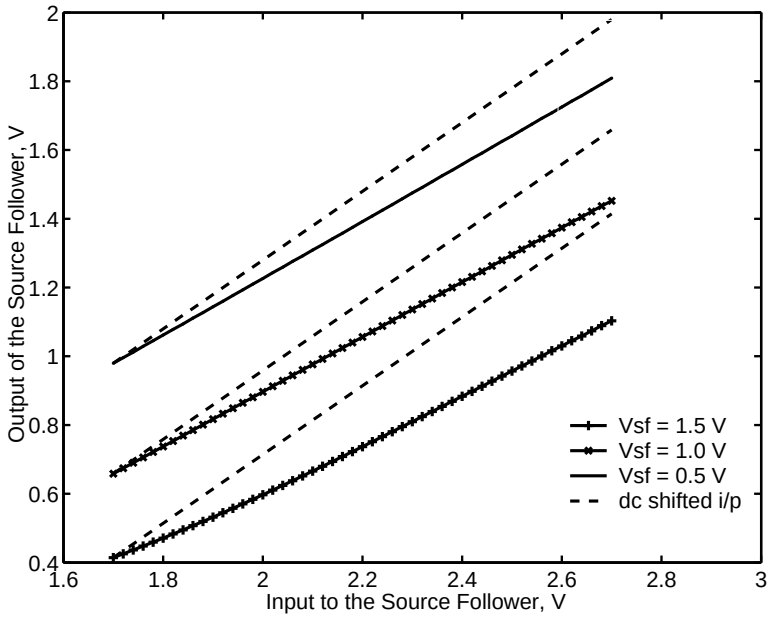

Figure 3.3: Simulation output of a typical source follower output at various biases to the current source

0.784. The principal cause of this reduction was the body effect and channel length modulation, the higher order effects which were neglected while studying the sources in fixed pattern noise in this circuit in section 2.1. This raises the possibility that the source follower gain variations between the pixels could be a source of gain variations in the pixel output. With the stringent requirement of gain variations to be as low as 0.14%, these effects need to be investigated for the possibility of any mismatch.

The conventional source follower circuit of Figure 2.1 has been reproduced as Figure 3.4. One may observe in this figure that in a non-dual well process (such as the n-well 0.35μm AMS process), the source and substrate of devices $M2$ and $M3$ will not be at the same potential. This is due to the common substrate for the whole chip, which is generally connected to the common ground. Even in a dual well process, a designer would be compelled to use single well for all devices in a pixel, due to the space constraints. The floating source of these nMOS devices will lead to a source voltage dependent change in the threshold voltage of the devices (body effect).

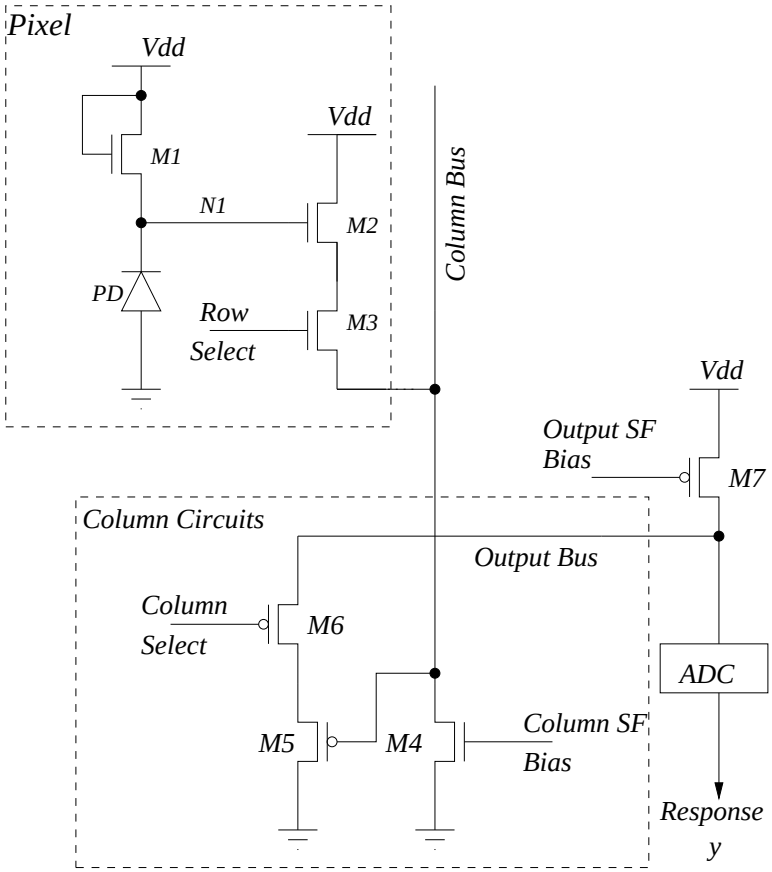

Figure 3.4: Conventional logCMOS pixel with 2 stage source follower readout

A first order expression for body effect may be given as [65]

$$V_T = V_{T0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right) \tag{3.11}$$

where V_{T0} is the threshold voltage with zero source to substrate voltage, ϕ_F is the built in Fermi potential of the material used, and γ is the body effect constant given by

$$\gamma = \frac{\sqrt{2qN_A K_s \epsilon_0}}{C_{ox}} \tag{3.12}$$

Here, ϵ_0 is the permittivity of free space (equal to $8.854 \times 10^{-12} F/m$), K_s is the relative permittivity of silicon (equal to 11.8) and N_A is the doping concentration. Studies of mismatch generally restrict themselves to variations in V_{T0} only. However, presence of the doping concentration dependent term suggests that γ may vary from device to device, as well.

In addition to the body effect, channel length modulation also affects the source follower as well as the current source for the follower. A first order equation of I-V characteristics of a MOS device in saturation involving channel length modulation is given by,

$$I_D = \frac{\beta}{2}\left(V_{GS} - V_T\right)^2 \left[1 + \lambda(V_{DS} - V_{eff})\right] \tag{3.13}$$

Here, λ depends on the length of the channel, the drain-to-source voltage and the Fermi potential.

$$\lambda = \frac{\sqrt{2K_s\epsilon_0/qN_A}}{2L\sqrt{V_{DS} - V_T + \phi_0}} \tag{3.14}$$

$$V_{eff} = V_{GS} - V_T \tag{3.15}$$

Here ϕ_0 is the built-in voltage of a pn junction [65]. The channel length variation among devices is one of the major contributors to mismatch and is expected to cause variations in λ. Further, presence of V_T in these equations will give rise to more variations. Incorporating these two effects and assuming an ideal row select switch, one may write a response expression of the source follower circuit of Figure 3.4 as follows

$$\begin{aligned}
&\beta_{M4}\left(V_{G,M4} - V_{T,M4}\right)^2 \left[1 + \lambda_{M4}\left(V_{G,M5} - V_{G,M4} - V_{T,M4}\right)\right] \\
&\quad = \beta_{M2}\left\{V_{G,M2} - V_{G,M5} - V_{T,M2} - \gamma_{M2}\left(\sqrt{2\phi_F + V_{G,M5}} - \sqrt{2\phi_F}\right)\right\}^2 \\
&\quad \left[1 + \lambda_{M2}\left\{V_{DD} - V_{G,M2} - V_{T,M2} - \gamma_{M2}\left(\sqrt{2\phi_F + V_{G,M5}} - \sqrt{2\phi_F}\right)\right\}\right]
\end{aligned} \tag{3.16}$$

From this complex expression, it is difficult to obtain a simple relationship between the input and the output of the source follower. This also makes the prediction of the amount of gain variation a difficult task. However, this equation does point towards other sources affecting the pixel gain than the ones previously believed. Further, mismatch owing to these higher order effects is not properly modelled by any simulator and hence any simulation will not be able to predict the nature of gain variations in the pixels accurately. This necessitates experiments with arrays of such pixel to determine the gain variation from the responses at different illuminations.

3.3.2 Experimental setup

Experiments were performed on a chip manufactured in a standard 0.35μm technology and containing a small array of typical logarithmic pixels. The array had 1000 pixels arranged in 100 rows and 10 columns. Each pixel had a single nMOS load and one stage of nMOS type source follower readout circuit. All pixels in a column share a common bias circuit of a single transistor voltage controlled current source. The pixel dimensions were 10 μm $\times$ 10 μm and device dimensions of the load transistor was 1 μm/ 0.6μm(W/L). The source follower and the switch had the dimensions of 2 μm/ 0.6μm(W/L). The fill factor of the pixel was 58%. The arrangement was similar to Figure 3.4, except for the absence of the second stage readout circuits. The row select switch of the pixel was connected to an on-chip shift register. This enabled access to every row of the array through minimum number of external signals.

In addition to the array, a large photodiode with dimensions of 100 μm $\times$ 100 μm was also manufactured on the chip. This diode was used to measure the input light intensity on the chip, and thus act as an on-chip photometer. Further, using the area ratios of this large photodiode and the photodiode in each pixel, one can estimate the photocurrent in every pixel from the measured photocurrent of the large diode, provided the chip is uniformly illuminated.

$$I_{PD,pixel} = I_{PD,largediode}\frac{A_{PD,pixel}}{A_{PD,largediode}} \tag{3.17}$$

It is well known that the peripheral columns and rows in an array suffer higher stress during fabrication leading to higher mismatch. Hence, pixels belonging to the 7 inner columns and the 90 inner rows (630 pixels) were used for this study. Absence of a second stage readout circuit meant there were 7 output signals for every clock signal. To record these signals, a computer based data acquisition system using Instrunet 100B analogue/digital I/O unit was used. This interface board has 16 single ended or 8 differential ended analogue inputs, in addition to 8 single ended analogue outputs. These analogue outputs were used to provide various biasing signals, including the bias to the source follower.

The instrunet board used a 14 bits analogue to digital converter to convert the analogue in-

put to TTL signal levels. The analogue outputs are generated using an 8 bit digital to analogue converter. In addition to these analogue signals, the Instrunet board also had 8 bit bidirectional digital lines, along with a 5V digital power supply and several ground ports. These digital lines were used to provide various digital signals including the clocks to the shift register in the chip. In addition, these lines were also used to monitor the output of the shift register. The Agilent Vee programming environment was used to program both the analogue as well as digital interface to the Instrunet board. The same program was also used to interact with a general purpose instrumentation bus controlled semiconductor parameter analyzer (Agilent 4155B). This device was used to measure the low photocurrents generated by the large photodiode on the chip, thereby measuring the input illumination intensity on the chip. A flowchart of the control program is shown in Figure 3.5.

In order to study the fixed pattern noise properties of the array, the pixels need to be stimulated with uniform intensity images. Various kinds of light sources were tested to generate these images. The fluorescent lighting available in the laboratory was the first to be used. However, sinusoidal fluctuations were observed in the response of the pixel with these sources. Fluctuations of similar nature but with smaller amplitudes were also observed in experiments performed with ac powered tungsten lamp. A dc powered lamp, however, removed these flickers. An intense (150W) dc powered quartz tungsten source was, hence used to generate uniform images for all experiments.

In addition to the lamp, the optical assembly included an infra-red reject filter, to cut out high infra-red components of lamp's spectrum. Further, to obtain a lambertian surface, the light beam was passed through an opal glass diffuser. A red-colour pass-filter was then used to remove the effects associated with spectrum sensitive response of the silicon diodes and neutral density filters. A combination of neutral density filters was used to vary the intensity of input light falling on the chip. To reduce optical interference from stray light in laboratory, the optical assembly except the light source and the board under test were housed in a black box. A small opening in the box was used to allow light to enter the test setup.

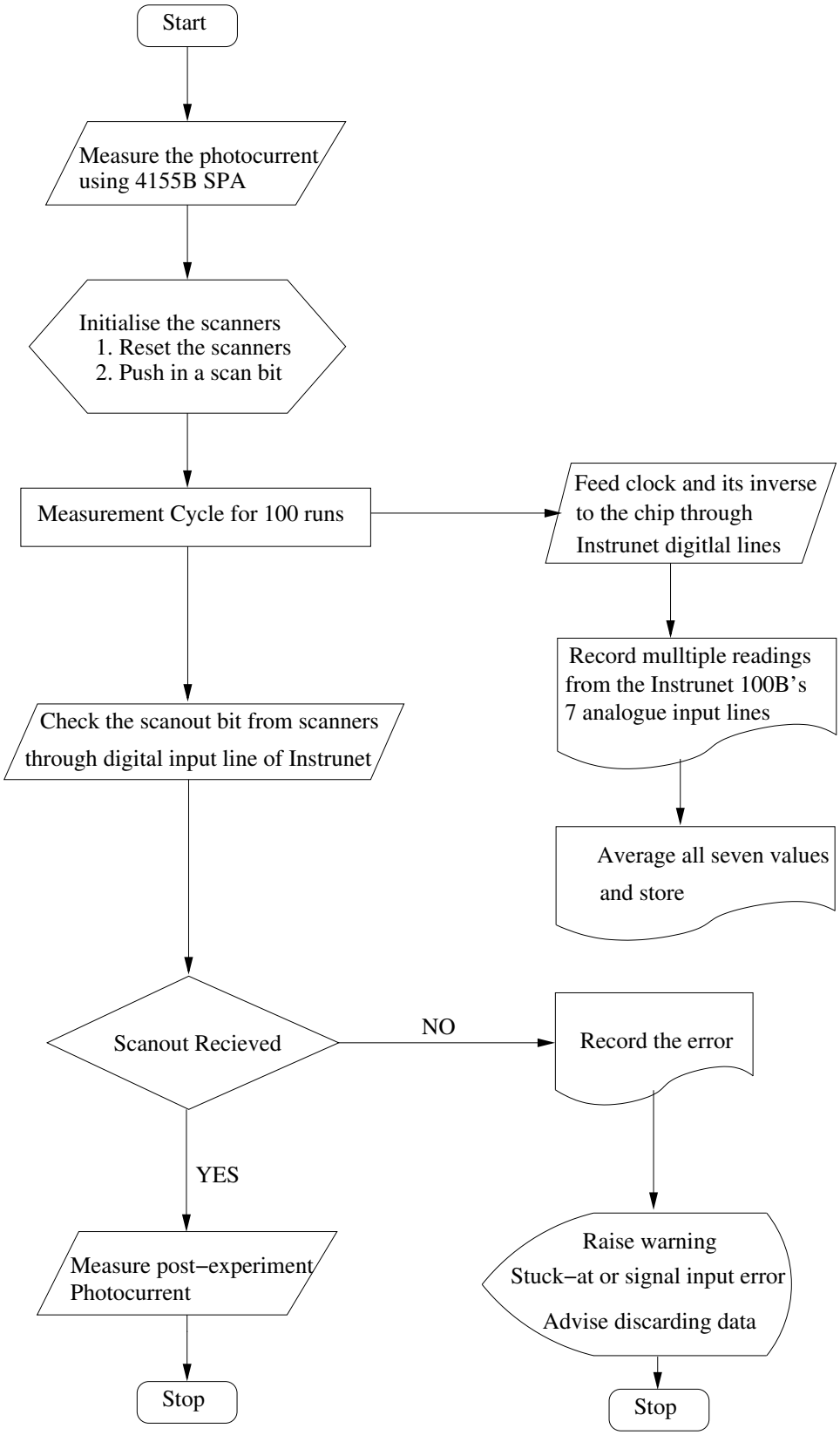

Figure 3.5: Flowchart of the measurement program. The program was designed using Agilent Vee environment

3.3.3 Results

Various noise sources were observed during the experiments. The most prominent of these was random fluctuations while measuring very low photocurrents of the order of less than 100 pA, from the large photodiode. Sources of such fluctuations may have included the power lines and/or the heating units. To minimise these interferences, triaxial cables with a very small unshielded contact was used to measure the photocurrent. The black box, described earlier to house the optical assembly, was further covered with multiple layers of aluminium sheets to minimise any other electromagnetic interferences.

Voltage measurements with the PC based data acquisition boards had transient noise of the order of 8mV peak-to-peak. On the other hand, the same responses when measured through Agilent 4155B semiconductor parameter analyzer had peak to peak temporal noise of 1.5mV. This suggests noise at the data conversion stage in PC based boards. However the measurement speed of 4155B is low compared to the Instrunet board and it has limited memory. Hence, it can not be used to measure response of large number of pixels. To reduce the temporal noise measured through PC based board, several readings of every data point were recorded and averaged.

Using the aforementioned assembly, the pixel outputs at various illuminations as well as the pixel response at no illumination and hence their dark response, were recorded. These readings along with the corresponding measured photocurrent were then input into an iterative routine, similar to the one used by Joseph and Collins to extract the three parameters of each pixel [62]. The statistical behaviour of these parameters is listed in the Table 3.1.

Parameter	Units	Mean	Standard Deviation
Offset	V	0.552	0.017
Gain	mV/decade	-56.9	0.335
Bias	fA	28.2	4.5

Table 3.1: Statistics of the three parameters of logarithmic pixels with a conventional source follower readout circuit (630 pixels)

The gain variations from these results are of the order of 0.6%. This level of gain variations will not be able to produce images with 1-2% contrast threshold over a high dynamic range as argued earlier. These results explain the high residual FPN from all additive fixed pattern noise correction strategies. Another conclusion from these results is that either the subthreshold slope of the nMOS load and/or gain in the readout chain of the pixel have a good amount of variations.

It must be noted here that the array under investigation is a very small array, when compared to any typical image sensor array. Hence, distance dependent mismatch factors are not present in these results. Secondly, a single stage readout circuit has been used and hence column to column fixed pattern noise due to second stage readout circuits is also not included in these results. Thus, in a typical array, the amount of gain variation is expected to be higher than the current value.

3.4 Alternative readout circuit

The theoretical analysis and the experiments with the conventional source follower circuit suggest that in order to improve the offset-only fixed pattern noise correction strategy, the gain of the readout circuits has to be increased and/or their variations have to be decreased. Readout circuits that do not involve source follower may provide a higher gain and/or lower gain variation and hence, need to be investigated. One circuit that may do so is that of differential amplifier readout with feedback also referred to as the active column sensor readout circuit [66, 67, 68, 69].

3.4.1 Theory

A differential amplifier readout circuit with the possibility of providing near unity gain is shown in Figure 3.6. The two pMOS transistors form a current mirror and the transistor $M4$ acts as a current source to bias the differential amplifier. The switch $M3$ will be assumed to be ideal. For the currents in the two sides of the pMOS current mirror to be equal, the gate-source voltages

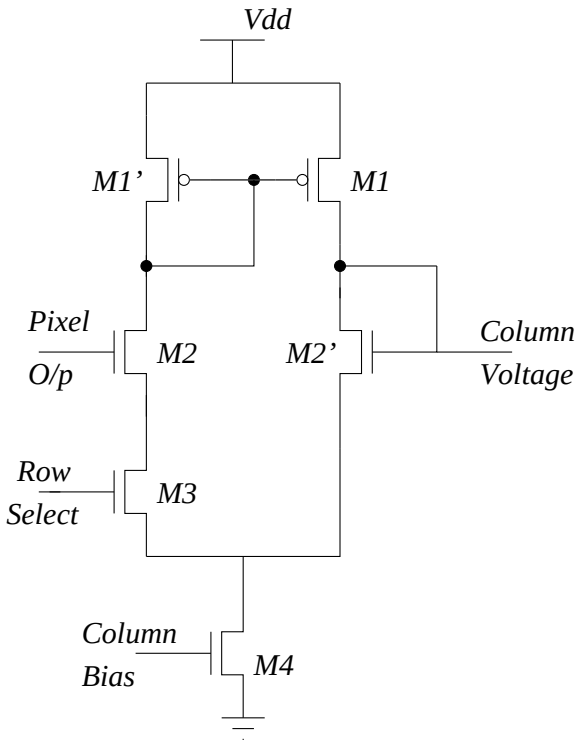

Figure 3.6: A readout circuit with a unity gain differential amplifier. Transistors $M2$ & $M3$ belong to pixel circuit, while others are shared by all pixels in a column.

of $M2$ and $M2'$ should be equal. Since the two transistors have their sources at same potential, their gate potential should be identical and hence the output will be equal to the input voltage. A similar circuit with a folded cascode has been also presented by Snoeij, Theuwissen and Huijsing [67].

Ideally the gain of the circuit should be unity, however, the simulated gain of this readout circuit was found to be 0.922, which is still higher than that of the source follower circuit. It has been claimed by various proposers that this circuit also reduces gain variation while increasing the gain when compared to the conventional source follower readout circuit. However, no quantitative data has been presented on the magnitude of either of these two quantities.

3.4.2 Experiments and results

To test the possibility of a higher gain with lower variation from the differential amplifier readout, arrays of 100×10 pixels of this type were tested, using the same assembly, which was used to test the conventional source follower readout circuits. The transistors M2 and M3 in the Figure 3.6 are present in every pixel. The other transistors of the readout circuit including the current source were shared by every pixel in a column. This means that the new pixel design is similar to the pixel with source follower readout, save for an extra column line. However, it has been layed out so that it has identical fill factor to that of previous pixel. The nMOS transistors (M2 and M2') had dimensions of 2μm$/0.6\mu$m(W/L), where as pMOS transistor(M1 and M1') had a dimension 20μm$/0.6\mu$m(W/L).

The parameters obtained from the responses of this array are shown in Table 3.2. It may be observed that the bias and its variations for these readout circuits are similar to that of source follower readout circuits. Bias has its origin in the photodiode used and with both the pixels using similar photodiodes; similar values for this parameter were expected. The mean offsets are higher in the differential amplifier readout pixels. This is also an expected result as the differential amplifier readout circuit does not include any voltage drop as in the source follower readout circuits. Offset variations in this readout are also very similar to the former. The primary sources of offset variations have been observed to be the threshold voltage variation in the logarithmic load and readout transistors. The differential amplifier readout operates using a current mirror between the nMOS devices $M2$ and $M2'$. However, $M2'$ is placed at the end of every column, and the hence a high amount of mismatch is expected between $M2$ and $M2'$ owing to the spatial distance between the two halves of the mirror. Thus any advantage gained towards mismatch reduction by matching the currents in the two halves of the mirror is lost. Further, both pixels share similar type of logarithmic load and hence similar amount of gain variations from the two circuits is within expectations.

The most important difference in the mean parameter values is an increase in the pixel gain from 56.9 mV/decade with a source follower to 66.7 mV/decade when a differential amplifier readout circuit is used. The latter value is also very close to the gain parameter at the pixel

Parameter	Units	Mean	Standard Deviation
Offset	V	1.743	0.018
Gain	mV/decade	-66.7	0.340
Bias	fA	26.2	6.3

Table 3.2: Statistics of the three parameters of the pixels with the differential amplifier readout circuits (630 pixels)

without a readout circuit as determined by circuit simulation. The larger gain of the differential amplifier readout circuit means that the gain variations in these pixels will give rise to a smaller contribution to fixed pattern noise. Significantly, because only two of the transistors within the differential amplifier circuit are within each pixel, this improvement has been achieved without increasing the area of the pixel.

The variability of the gains of the two types of readout circuits have, however, been found to be comparable. The level of gain variations can be attributed to mismatch between the output side and the input side of the two nMOS current mirrors of the readout circuit. Since, the gain variations are still approximately 0.5% of the mean pixel gain, the discussion in previous section shows that it will be impossible to obtain good quality high dynamic range images without correcting for gain variations.

3.5 Conclusion

LogCMOS sensors suffer from severe fixed pattern noise, which arises from device variations from pixel to pixel. These variations degrade the quality of the image and are the principal demerits preventing logarithmic cameras from becoming commercially popular. Building on the survey of the techniques proposed for reduction of the FPN of the Chapter 2, this chapter has produced techniques to reduce the effect of this noise on the end image.

In the first section of this chapter, contrast threshold was established as an ideal measure for the fixed pattern noise, in terms of imager's differentiability of the input intensity as well as the end-user's experience. In view of this measure, mathematical analysis of the various FPN reducing techniques suggests that these techniques reduce only the offset part of the fixed

pattern noise and place an extreme requirement on gain variation in order to produce high quality images. Further analysis of the pixel circuit suggests that the readout circuit is a major culprit towards the high gain variations. A high gain readout circuit was hence experimented with to reduce the effect of gain variation. Gains, higher than the conventional readout circuit were obtained, however, these were not high enough to counter the effect of their variations, which was found to be similar to that of the conventional readout circuits. This means that one has to correct for offset as well as gain correction in order to produce good quality images from arrays of logarithmic pixel.

Chapter 4

Electronic Calibration of Logarithmic Sensors

I measure every grief I meet
With analytic eyes;
I wonder if it weighs like mine,
Or has an easier size.
Emily Dickinson

The discussion in the Sections 3.3 and 3.4 suggests that despite obtaining higher gains using improved readout circuits, one will have to correct for gain variations in order to obtain a good quality high dynamic range image. The technique used by Joseph and Collins for gain calibration has already been introduced in the earlier chapter. However, this technique is impractical on account of demanding non-real time computation and need of uniform images for calibration. A simple yet effective calibration technique to correct for all parameters is hence required. An electronic calibration scheme along with various optical and electronic assemblies required to verify this scheme will be presented in this chapter.

4.1 Introduction

In order to calibrate a pixel against offset, gain and bias variations, these parameters of all pixels should be stored and used to compute the FPN corrected response of each pixel. The various

parameters in this equation are dependent on the working conditions, mainly temperature, as shown by Joseph [66]. The offset and gain are expected to be either monotonically increasing or decreasing with temperature, depending upon the manufacturing process used. The bias depends on the leakage current. This leakage current doubles for every 10 degrees rise in temperature and the same is expected for the bias. Hence, the camera needs to be calibrated at the time of use.

There are only three unknown parameters in the model and these parameters can therefore be estimated using three data points per pixel. Furthermore, one of the parameters simply determines the minimum illumination at which the pixel gives a logarithmic response. Only two data points per pixel are therefore required to correct for variations in both offset and gain. In particular, if the response of each pixel is measured at two currents that are large enough so that the contribution of bias term to the response of the pixel is negligible, then the gain and offset parameters for the pixel can be calculated using

$$b = \frac{y_1 - y_2}{\ln(x_1/x_2)} \tag{4.1}$$

$$a = y_1 - b\ln(x_1) \tag{4.2}$$

where y_1 is the pixel response at reference current x_1 and y_2 is its response to another current x_2. The last two equations can be solved to find the values of a and b. If required, these two values can then be used with dark response of the pixel to compute the value of bias term c.

$$c = \exp(\frac{y_d - a}{b}) \tag{4.3}$$

Thus, complete characterization of the pixel by all parameters is possible. These equations can also be used to determine the statistics for the variations between pixels for a particular circuit design. Otim and co-workers have studied the performance characterisation using this method and iterative computation used earlier and found them to be comparable over a wide dynamic range [70].

The data from each pixel could be used to correct each image for offset and gain variations.

However, a more direct method of performing offset and gain correction is simply to use the responses of the pixel at the two reference currents. In particular, substituting equations 4.2 and 4.1 into equation 2.10 gives

$$\begin{aligned} y &= y_1 - b\ln(x_1) + \frac{y_1 - y_2}{\ln(x_1/x_2)}\ln x \\ &= y_1 - \frac{y_1 - y_2}{\ln(x_1/x_2)}\ln\frac{x}{x_2} \end{aligned} \tag{4.4}$$

This can be re-arranged to give a corrected output y_{corr}

$$y_{corr} = \ln\frac{x}{x_1} = \frac{y - y_1}{y_1 - y_2}\ln(\frac{x_1}{x_2}) \tag{4.5}$$

which shows that the ratio of the two reference currents is a common multiplication factor, while one of the reference currents becomes the scaling factor for the logarithmic response. The pixel output can therefore be corrected to compensate for offset and gain variations without any knowledge of the actual currents used to obtain the calibration data needed.

4.2 Circuit design

One method to obtain 3 points to perform such a calibration would be to show the camera two bright uniform scenes of different light intensity and then to close the shutter and take the dark reading. But for the end user, providing two differently illuminated, yet uniform scenes and then to close down the shutter will be too cumbersome. It is more convenient to obtain the data electronically. Another advantage of electronic calibration is that the reference currents used to obtain the data can be selected by the circuit designer to ensure the best possible results.

4.2.1 Pixel circuit

The logarithmic pixel, shown in Figure 4.1, has been designed to be calibrated electronically, if necessary. In this circuit transistor $M1$ is the load device that converts the photocurrent to a

voltage. Transistor $M4$ was included in the pixel to limit the voltage across the photodiode while transistor $M5$ acts as a calibration enable switch. This switch can be used during calibration to selectively connect the pixel to the drain of transistor $M6$ which acts as the voltage controlled current source. In order to save area and to ensure uniformity of the current flowing in different pixels, this device is shared by all the pixels in the same column. The differential amplifier readout circuit described in the previous section has been used to provide improved gain in the readout chain. The devices $M1$, $M4$ and $M5$ have the dimension of 1μm/0.6μm (W/L), whereas the devices $M2$ and $M3$ have the dimension of 2μm/0.6μm (W/L).

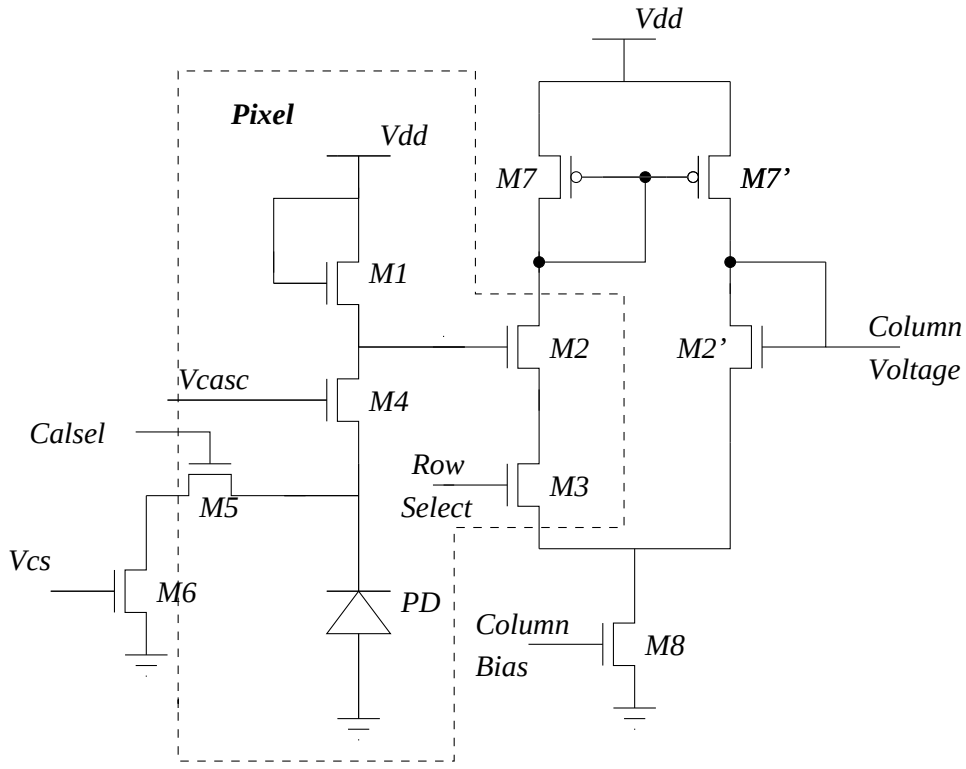

Figure 4.1: A logarithmic pixel with one stage of a differential amplifier readout and circuit for electronic calibration

4.2.2 Calibration circuit

In addition to readout circuits, every pixel in a column shares a common calibration current source. Although FPN correction takes into account variations in the readout circuits, these shared current sources introduce a new source of FPN between different columns of pixels. To

allow the variability of these current sources to be quantified and to allow for correction for this type of FPN if required, the pixel array is designed so that each of these current sources can be selectively connected to a reference pixel circuit. This reference circuit is the same as a logarithmic pixel, except that it does not have a photodiode.

To characterise the variability of the current source, a constant calibration voltage is applied to the gates of all current sources. Each of these current sources is then connected to the reference circuit in turn and the response of this circuit is measured. The response of the reference circuit to the different current sources gives a measure of variability of these sources.

To complete the calibration circuit, the calibration select switch of every pixel is activated by an 'AND' combination of the row select and the calibration signals. The switch to feed the calibration current source to the reference circuit is activated by an 'AND' combination of the column select, calibration enable signals and the row select signal for the last row. This ensures that at any particular time a current source can only supply current to either one pixel in the column or the reference circuit.

4.2.3 Test chip

An integrated circuit has been designed and manufactured that contains an array of 200 $\times$100 electronically calibratable pixels, with the various column circuits as described above. This circuit was fabricated in a 0.35 μm standard CMOS process from Austria Micro Systems. Each pixel has an area of 10 μm by 10 μm with a fill factor of 49$\%$. Figure 4.2 shows a representative schematic of various circuits in the test array. In addition to the pixel, readout and the calibration circuits explained earlier, the array also contained column and row scanners to selectively access every pixel. These scanners were designed using pass transistor logic. The scanners were powered through a separate power line and were spatially protected to minimise the effect of transition feed-through to the analogue circuit. The row scanners produced two outputs for every row of the pixels as shown in Figure 4.2. The first of these was the 'row select' signal which was connected to the readout switch in every pixel (device $M3$ in Figure 4.1). The second signal was the 'calibration enable' signal which was connected to the calibration switch of every

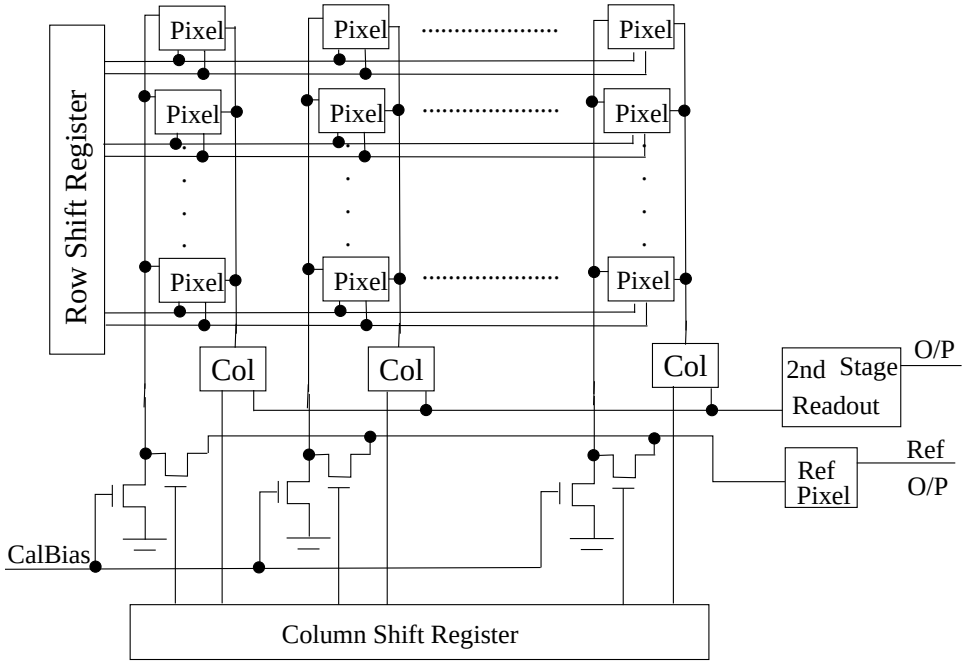

Figure 4.2: Test chip with different stage of readout circuits. The row shift register generates a row select signal to select one row for readout. It also generates pixel calibration enable signal for the calibration frames. The column shift register generates the column select switch and calibration source correction signal. In the figure 'col' stands for column readout circuits.

pixel (device $M5$ in Figure 4.1). Similarly, the column shift register also produced two signals. The first of these was used to connect to the column readout circuits and the second was used to study the variations in the column current sources. The second stage of the readout was similar to the first stage and used a differential amplifier circuit.

4.3 Experimental setup

Initial experiments with the array were limited to the study of one column of 200 pixels only. This was primarily done in order to prove the concept of electronic calibration and avoid column effects as well as analysis of large streams of data. Further, a central column was used to remove the periphery effects. For these experiments, low speed instruments were sufficient and hence the setup involving Instrunet 100B PC based data acquisition board and Agilent 4155B semiconductor parameter analyser, explained earlier, was used. It has been reported earlier that analogue measurements involving the semiconductor parameter analyzer are less noisy than the

ones performed through analogue inputs of the PC based data acquisition board. Hence, the data was acquired through the analogue voltage input facility of semiconductor parameter analyser, while experimenting with a single column.

However, the speed of operation of Instrunet 100B and Agilent 4155B, controlled through a general purpose instrumentation bus, was limited to few Hertzs. Hence, data collection from the whole array using these equipments would be a time consuming process. This would also raise additional constraints on temporal stability of the light output. Owing to these problems, a different clocking and data acquisition strategy was needed while experimenting with the whole array. Clocks and other digital signals, needed to test the pixel arrays, were generated using a Xilinx^{TM}Spartan^{TM}-3 field programmable gate array. The gate array chip was placed on a Digilent S3 board. ISE^{TM}design platform from Xilinx^{TM}was used to program these gate arrays using VHDL (Very High Speed Integrated Circuits Hardware Description Language). The flowchart of the program was similar to the one used for testing smaller arrays with the addition of structures for the column shift registers. These structures, in turn, are similar to the ones used for the row shift registers.

The analogue output voltages from the pixel arrays were digitized using an external 2MSPS 16-bit ADC from Analogue devices. The clocks and other signals required for this ADC were also generated using the Xilinx^{TM}Spartan^{TM}-3 FPGA. The digital output of the ADC was recorded using the PowerDaq digital input data acquisition board. The recorded output was written directly onto the hard disk of a PC using direct memory access to increase the speed of data acquisition. The temporal noise recorded from these measurements had a peak to peak range of 1mV. Hence, to reduce the temporal noise between data points, introduced by the connection between the pixel array output and the ADC, to less than the signal corresponding to the target sensitivity of a 1% change in contrast, each measurement was recorded 8 times and the measurements were averaged to produce the corresponding data point.

Improvements were also carried out to the optical setup. Use of diffusers to obtain lambertian surface results in loss of intensity and therefore, high dynamic range could not be generated with the light sources available. Hence, the diffusers were replaced by an integrating sphere of

diameter 100 mm and an output port of diameter 10 mm. The output port of the integrating sphere was large enough for the chip area to be illuminated.

A DC-powered stable light source working at 12 V and 100 Watts was used with the sphere. As before, the intensity of the resulting uniform output beam was then altered by using neutral density filters and/or by varying the input power of the light source. At different light intensity, the photocurrent flowing in the large photodiode present in the chip was used to determine the photocurrent through a typical pixel. The bias voltage applied to the column current sources could then be used to ensure that two typical currents were used to calibrate the pixel array.

4.4 Experimental results

An added advantage of having a calibration source per column in the array is that, it can be used to generate any current, which can then be fed to a pixel to stimulate an optically generated current. This way, a pixel can be tested electronically without the need of any optical sources. This method also has the advantage of being simple and fast, in addition to the ability of stimulating high intensity scenes, without the need of high intensity light sources and the disposal of the heat associated from these sources. An optical testing is hence required only to study the variations in photodiode responses.

4.4.1 Pixel response

Figure 4.3 compares the simulated and the measured response of the electronically calibrated pixel, when stimulated with the calibration current source. The two curves show good match. Parameters of the pixels in the central column of the array were extracted using the simple parameter extraction procedure, explained earlier. The statistical values of these parameters were found to be similar to the ones reported for the differential amplifier readout pixel. Table 4.1 shows these values.

A few of these pixels were also studied for the temperature dependence of the parameters. However, the limitations of the constant temperature facility available in the lab meant that these

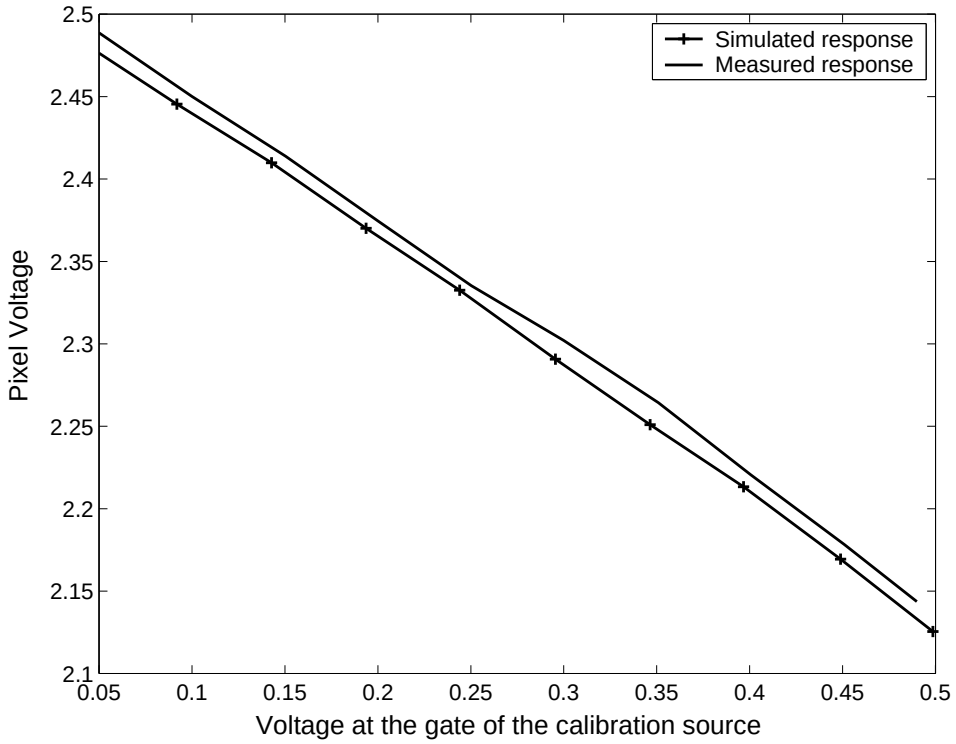

Figure 4.3: Comparison of simulated and experimental results with calibration source as the source of excitation currents.

Parameter	Units	Mean	Standard Deviation
Offset	V	1.743	0.0174
Gain	mV/decade	-66.7	0.360
Bias	fA	26.1	6.1

Table 4.1: Statistics of the three parameters of the electronically calibratable pixels with the differential amplifier readout circuits from the central column of 200 pixels in the array

studies could only be conducted between 40 and 70 degree Celsius. The electronic stimulation method also enables a low cost solution to temperature testing by keeping the test board in a small oven, as temperature stable high intensity light sources are costly and would require a large temperature stable oven. Figure 4.4 shows the typical behaviour of offset, gain and bias parameters against temperature. It is observed that the bias doubles every ten degrees rise in temperature, which is expected, as bias depends on leakage current, which doubles every ten degrees rise in temperature. The offset and gain monotonically decrease with temperature. While the offset decreased by 14 mV per degree rise in temperature, the gain fell by 0.95

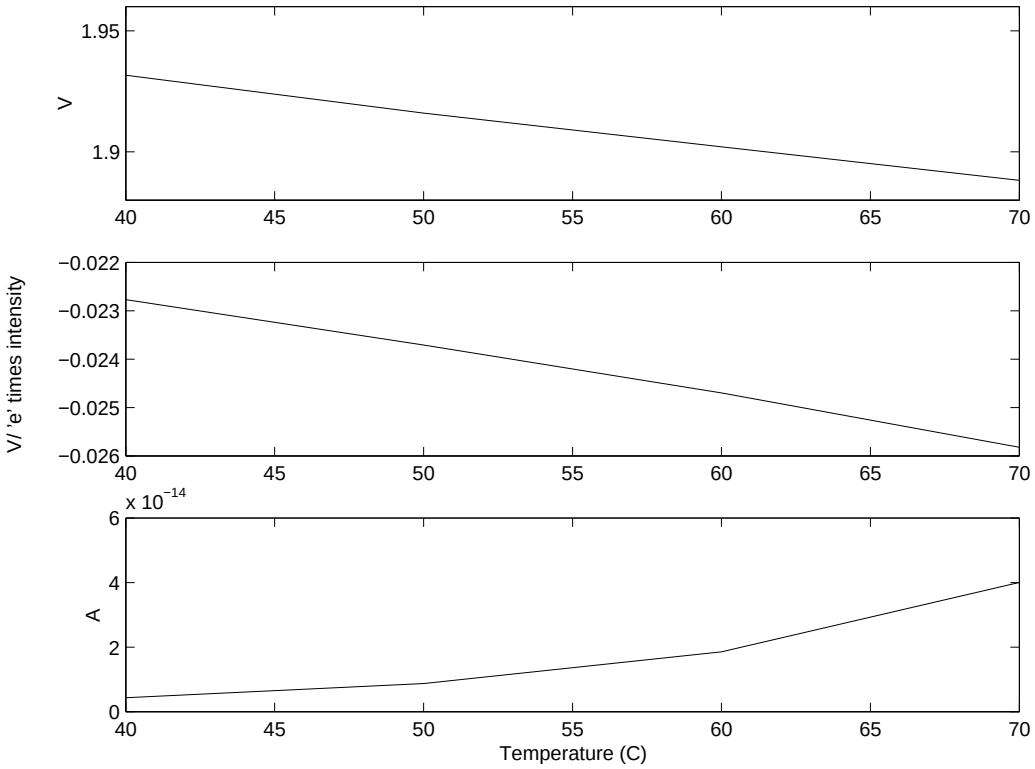

Figure 4.4: Parameter variation with temperature of (a) Offset (b) Gain (c) Bias

mV units (corresponding 2mV/decade) for every 10 degrees rise in temperature. A detailed theoretical study of these results has been carried out by Otim [71].

It must be noted that these results are correct only to the degree of the correctness of the prediction of temperature response of the calibration current source from the simulator. Further, these studies represent temperatures at the extreme end of the commercial temperature range and hence will not be replicated in most usage of a digital camera. However, a quick conclusion from these results is that the pixel parameters are very sensitive to working environment, particularly temperature. Hence, an onsite calibration is required to compensate for various changes in working environment. Further, this procedure should be repeated for every change in the working environment.

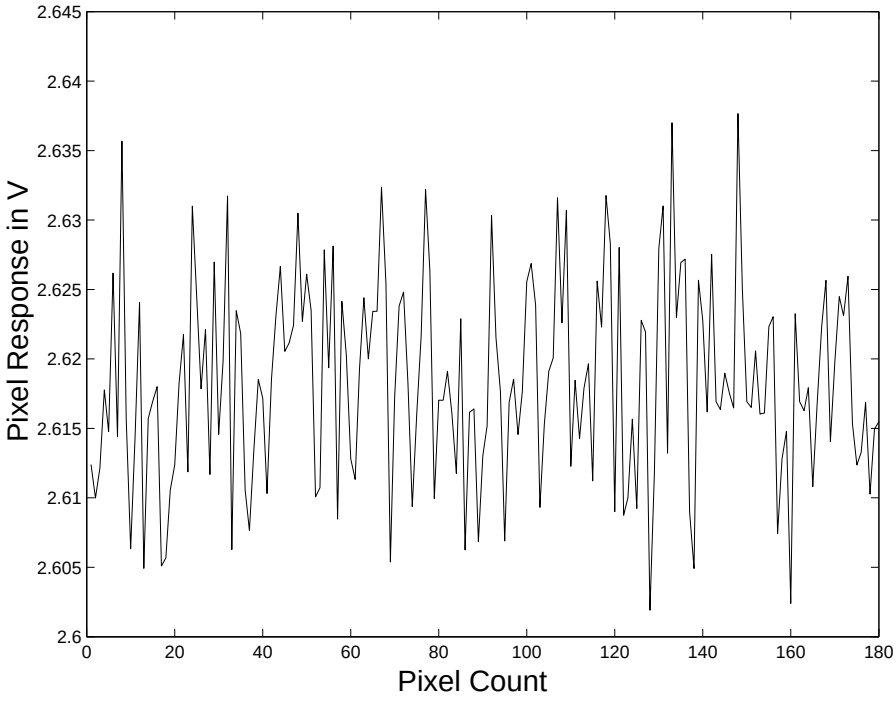

Figure 4.5: Uncorrected response from a column of pixel to a typical uniform scene

4.4.2 FPN correction

Figure 4.5 shows the response of a column of pixels to a typical uniform scene. The peak-to-peak variability in these responses is of the order of 30mV, which corresponds to half a decade of illumination. These variations need to be corrected in order to produce good quality images. To correct images for both offset and gain variations, the response of each pixel to two different input currents needs to be measured. The two currents used to perform fixed pattern noise correction need to be chosen carefully. In particular, the equation 4.1 assumes that the effects of leakage currents are negligible on the pixel response. This means that the smaller of the two calibration currents should be chosen to be significantly larger than the leakage current in a pixel. As described in Section 3.1, the aim of any fixed pattern noise correction algorithm should be to achieve a contrast sensitivity between 1-2$\%$. Hence, the smaller current was set to at least one hundred times the largest expected leakage current. The choice of the second calibration current is more difficult. Since the correction procedure relies upon the difference between the responses of each pixel to the two input currents, it can be expected that the accuracy of

correction will be improved by using two very different input currents. However, the minimum value that can be used is fixed and it has been pointed out using simulation data that the larger of the two currents must be small enough for the load transistor to remain operating in weak inversion, rather than moderate inversion [71]. Even with a pixel model that includes the effects of the load transistor operating in either weak or moderate inversion, it is difficult to predict the nature of residual FPN with any maximum current used to calibrate each pixel [71]. The effect of varying the larger of the two calibration currents has therefore been investigated empirically.

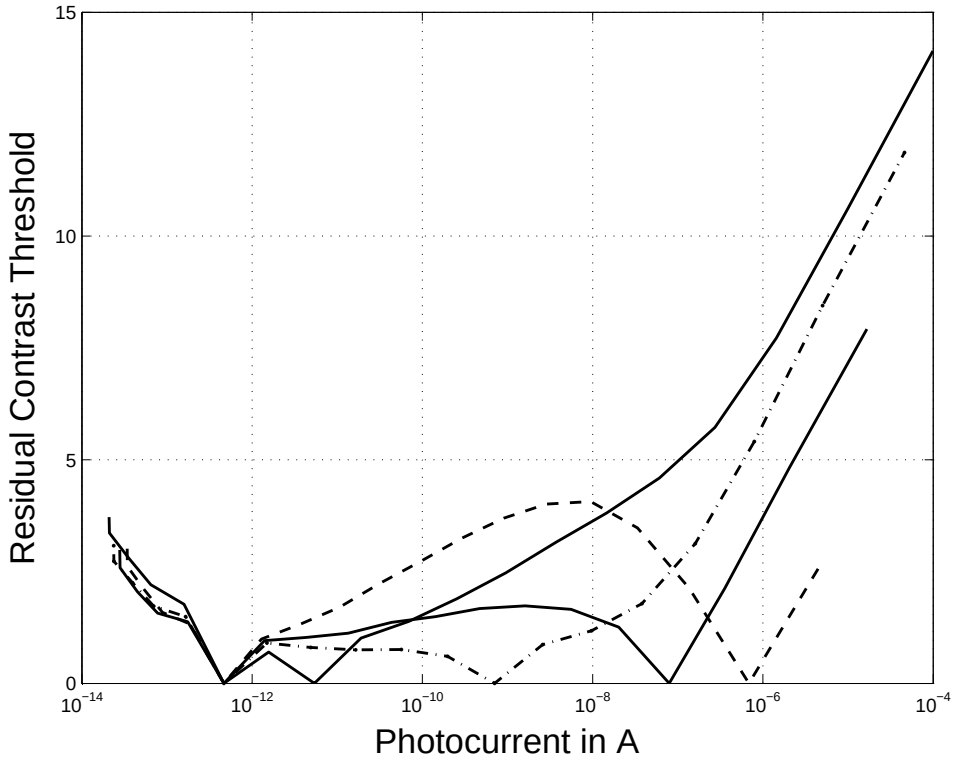

Figure 4.6: Residual fixed pattern noise expressed as contrast threshold % at different photocurrents with one calibration current fixed and a second calibration current that is 1, 3, 5.5 and 6 orders of magnitude larger than the first.

To quantify the effects of different choices of calibration current, the response of 200 pixels in a column was measured over a wide range of different currents generated by the current source at the end of the column. One of these responses, corresponding to a photocurrent significantly above the leakage current was then chosen as one of the calibration points. The impact of various different choices of the second calibration current on the level of fixed pattern

noise is shown in Figure 4.6. These results show that for all combinations of calibration currents the quality of the final image is degraded at low currents, when the leakage current becomes significant, and at high currents, when the load transistor operates in moderate inversion. More importantly, these results show that when appropriate calibration currents are selected, fixed pattern noise is reduced to less than the equivalent of a 2% change in contrast for currents corresponding to six decades of light intensity. Thus, by performing offset and gain correction, it should be possible to create a sensor that matches the dynamic range and contract sensitivity of the human eye. The data of a pixel column shown in Figure 4.5, after correction for offset and gain has more limited variations, as shown in Figure 4.7.

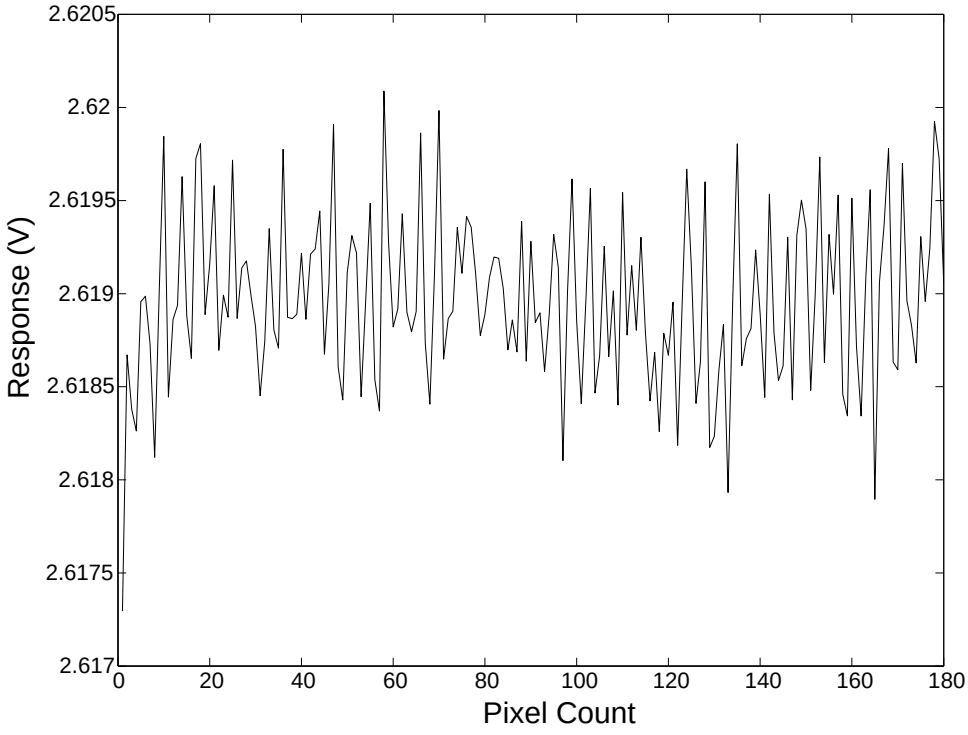

Figure 4.7: Response of a column of pixels after calibration of offset and gain

The experimental data obtained from electronic stimulation of the pixel column can also be used to simulate the double sampling approach of fixed pattern noise correction and compare it to the current procedure. In Figure 4.8, one of these responses has been selected as the reference point for double sampling, and FPN correction has been performed by subtracting this response

from other responses. It may be observed that removal of additive fixed pattern noise by double sampling removes the major source of FPN. However, other sources of FPN become prominent once the additive error has been removed. It should be noted here that the reference frame used in the Figure 4.8 is such that the pixel still operates in the logarithmic region. The reference frame from moderate inversion region, as used by Kavadias and co-workers [54] or the dark current output as used by Lai and co-workers [56] would dramatically increase the residual fixed pattern noise. Another important inference from Figure 4.8 is that the residual FPN in double sampling procedure depends on the input intensity of the scene and increases with the intensity difference from the reference frame increases.

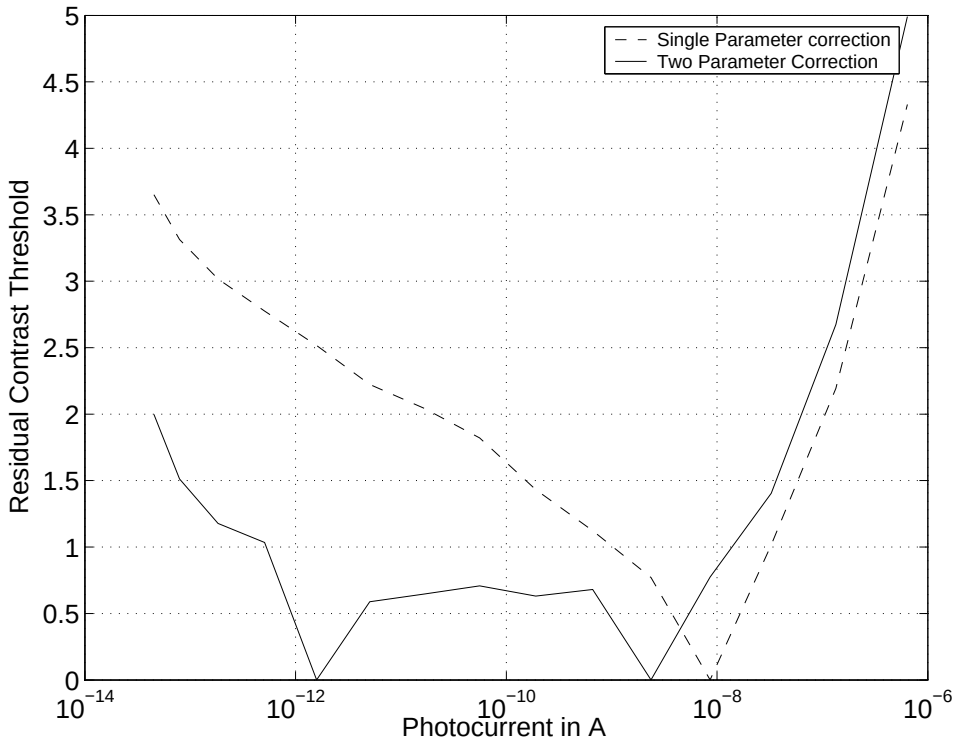

Figure 4.8: Comparison of double sampling and two parameter calibration procedure. The residual FPN with simple double sampling increases as one moves away from the calibration frame.

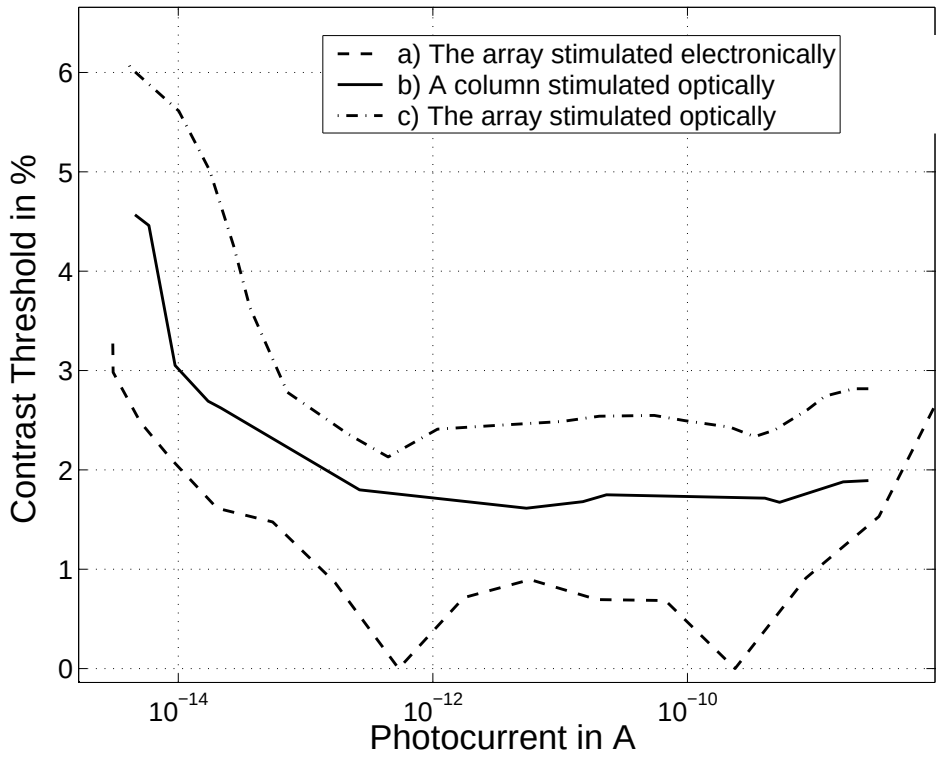

Figure 4.9: Residual fixed pattern noise at different illumination levels. Curve (a) shows the residual fixed pattern noise after electronic calibration in the response of a pixel stimulated electronically. Curve (b) shows the residual FPN after electronic calibration of the response of one column of pixels stimulated optically. It should be noted that these data do not include column current source variations. Curve (c) shows the residual fixed pattern noise in the array of pixels stimulated optically. The responses have been corrected for pixel as well as current source variations.

4.4.3 Optical stimulation

The one source of variability between pixels that will not be corrected using the responses of pixels to currents flowing through the voltage-controlled current sources in each column, is variations in the responses of the photo-diodes. To quantify the impact of these uncorrected variations, the response of a column of 200 pixels to varying levels of uniform illumination was measured. The resulting data was then corrected using the responses of the same pixels to two similar currents flowing through the voltage controlled current sources. The results in Figure 4.9 show that after correction with this data the residual fixed pattern noise corresponds to a contrast change of less than 2%. A comparison with the corresponding results obtained from the responses of the pixel to the same currents flowing through the voltage-controlled

current sources, also shown in Figure 4.9 suggests that variations between the photodiodes are equivalent to a contrast of approximately 1%. Variations between photodiodes are therefore expected to make a significant but not dominant contribution to the residual fixed pattern noise remaining once an image has been corrected to compensate for variations in the gain and offset of pixels.

4.4.4 Uniformity of calibration current sources

Ideally, a single current source would be used to calibrate all the pixels in an array. However, the relatively long time required for the response of each pixel to settle would make this a lengthy process. To reduce the time needed to calibrate the pixels, a voltage-controlled current source has been included at the end of each column. Although this will reduce the time needed to gather the data from each pixel, using different current sources introduces a source of non-uniformity that could cause fixed pattern noise between columns rather than between pixels.

To study the uniformity of the column current sources, a constant gate voltage was applied to the current sources and their outputs were selectively connected to the reference pixel. A marked variation in the reference pixel's response was observed when it was connected to the different column current sources. From the reference pixel's response it was found that the calibration currents generated by these sources had a variation of approximately 8%. This variation is too large to be ignored. Figure 4.10 shows the extracted photocurrents at a typical illumination across a row ignoring these variations, thereby prompting the need of a procedure to compensate for the variations between the calibration currents in each column of pixels.

In order to remove the effects of offset and gain variations, the response of each pixel and the reference pixel must be measured at two input currents. If the response of a particular pixel and the reference pixel at one input current are, y_1 and y_{1r}, whilst their responses at a second current are y_2 and y_{2r}, then a subsequent output from this pixel, y_{out}, can be transformed to the equivalent output from the reference pixel, y_{outr}, using the equation

$$y_{outr} = y_{1r} - \frac{y_{1r} - y_{2r}}{y_1 - y_2}.(y_1 - y_{out}) \tag{4.6}$$

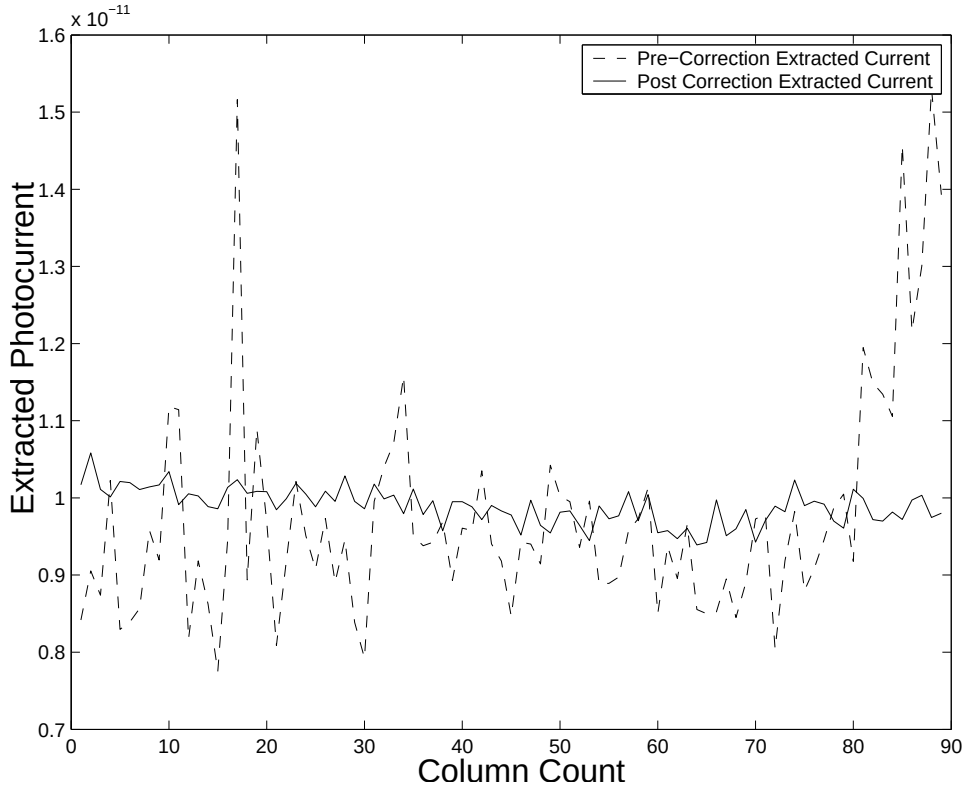

Figure 4.10: Currents extracted from a single row of pixels (spanning across all columns) before and after correction for current sources variability. The second stage correction process removes the residual FPN arising due to variability in calibration sources present in every column.

This expression then generates an image which is equivalent to the one that would be obtained if the reference pixel occupied each position in the two dimensional array. Ideally, this means that there will be no fixed pattern noise in the final output image. After correcting for these column current sources, a worst case contrast threshold of 2.5% was obtained for about five decades of illumination for the complete array after calibration of pixels and correction for calibration sources, as shown in Figure 4.9. The residual fixed pattern noise for the whole array after correction is higher than that of a single column by about 1%. The source of this error lies in the correction procedure for calibration currents, which has an accuracy of approximately 1%. To make the calibration procedure easier and more accurate larger current sources may be used in any future design to minimise the effects of this source of variability.

4.5 Conclusion

An electronic calibration procedure has been proposed in this chapter which is capable of removing the offset as well as gain related fixed pattern noise. This involves use of a voltage controlled current source, present in every column, to produce two reference calibration currents. The output of every pixel at these currents is recorded and used to extract the values of offset and gain parameter of the pixel using a simple parameter extraction procedure. These parameters are then used to estimate the actual photocurrent flowing in every pixel from the output of the pixel.

Mismatch in the calibration current sources, however, forms a new source of fixed pattern noise, across the columns. To correct for this new source, an external pixel which could be selectively connected to each of these sources, was used. The output of this reference pixel to different current sources was used to correct for their variations. This two stage correction procedure led to very low fixed pattern noise from an array of logarithmic pixels, thereby enabling them to produce images with contrast threshold matching that of the human eye. An interesting future activity would be to investigate the exact effect of change in temperature on the calibration process. Two possible approaches may be studied. One is to recalibrate the camera after a certain degree change in temperature. The other could be to calibrate the parameters against change in temperature. Both of these need to be investigated at the full range of commercial temperature range.

Chapter 5

Dark Current Suppression in Logarithmic Pixels

Dark is the past to them, and dark
The future still must be,
Till pitying Saints conduct her bark
Into a safer sea–
William Wordsworth

5.1 Effect of high dark current on logCMOS performance

It has been observed in the previous chapter that high dark current adversely affects the performance of electronic calibration technique in low light regions. The simple two-parameter correction technique yields very high residual fixed pattern noise in low light regions, due to the non-negligible influence of this leakage current (shown in Figure 4.9).

One way to reduce the effect of the dark current on the calibration technique may be to calibrate for the bias parameter along with offset and gain of the pixel. This may be achieved by extracting the bias parameter from the dark response of the pixel, y_d, as follows

$$c = \exp \frac{y_d - a}{b} \tag{5.1}$$

where a and b are the offset and the gain of the pixel respectively. The photocurrent at any

instance may then be calculated according to the following equation

$$x_{ph} = \exp \frac{y_{ph} - a}{b} - c \tag{5.2}$$

However, these two computations have high complexity and are difficult to perform in real time. Further, in the two parameter calibration process, it was proposed to shift the responses of pixels in an array to that of a reference pixel using linear computation to calibrate for the variations in the column readout circuits and the column calibration sources. Involving bias parameter in the calibration process would make this shift non-linear leading to iterative as well as even more demanding computation. Thus, it is safe to conclude that bias calibration is not an efficient method for FPN correction,

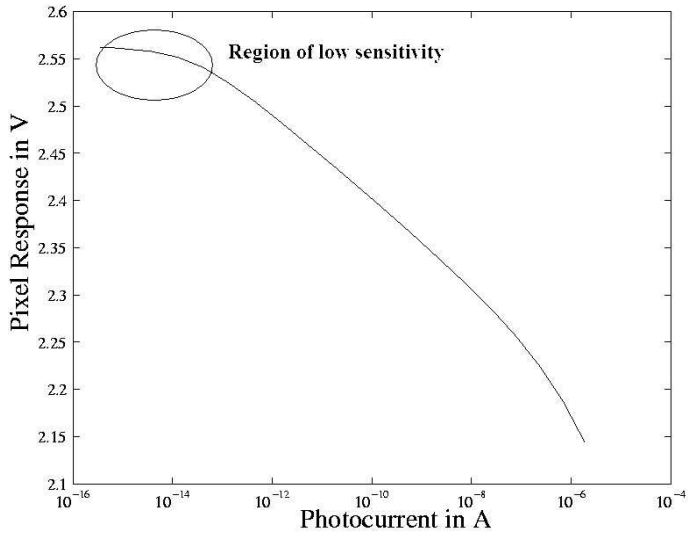

Figure 5.1: Figure showing loss of sensitivity at low photocurrents due to high leakage currents in the response of a logarithmic pixel

Even if one performs the bias calibration to reduce the FPN in low intensity regions, the performance of the logCMOS pixel would still be degraded due to the diminishing sensitivity of the pixel in these regions. Figures 5.1 and 5.2 show that as the photocurrent approaches the dark current, the gain of the pixel reduces to fairly small values. The reason for this reduction is again the bias parameter, which breaks the strict logarithmic relationship between the input photocurrent and the pixel response. Hence the computationally demanding task would of little

use, as the output signal will be lost in temporal noise on account of the low gain. Thus, low dark current in a logCMOS pixel would be highly desirable.

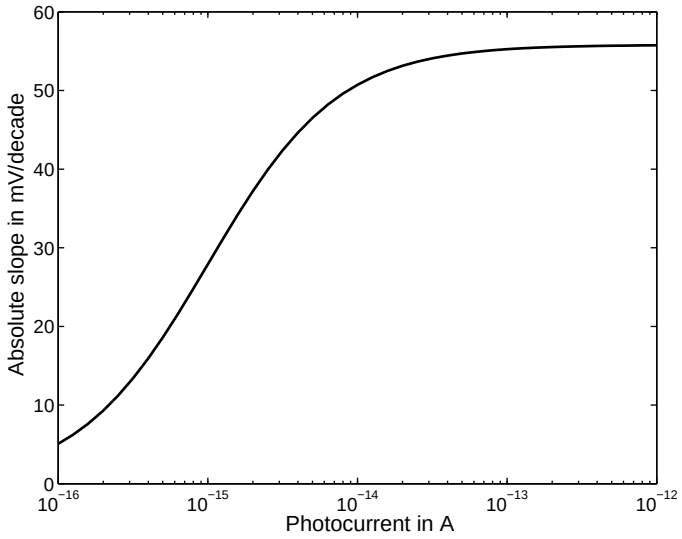

Figure 5.2: Decreasing gain of the logCMOS pixel at low photocurrents

This chapter is devoted to ways leading to the reduction of the effect of the typically high dark currents in a CMOS process. The next section identifies the various sources of the dark current. The ideal approach to reduce the dark current would be to improve the manufacturing process. A review of several modifications proposed in this direction has been provided in the third section of this chapter. However, any process modification is costly to implement, thereby increasing the cost of the image sensor produced. Hence, there is a need to attempt other ways to reduce the leakage currents. Towards this goal, the fourth section of this chapter proposes use of a double current mirror circuit to reduce the effect of high dark current on the performance of the logCMOS pixel. The fifth section of this chapter utilises a layout technique to reduce the leakage current. Experimental results from both these techniques have been provided.

5.2 Sources of dark current

Figure 5.3 shows various sources of dark currents in an n^+/p-sub diode in a typical CMOS process. The dark current in this photodiode can be broadly classified to be composed of two

types of constituents [53]. The ideal or normal leakage currents owe their origins to the thermal generation-recombination process followed by drift phenomena in silicon and the injection-diffusion process. The former is due to thermally generated minority carriers having high enough energy to cross the potential barrier. This phenomenon is controlled by the Shockley-Hall-Read equation for generation-recombination [72] and the drift current is given by [65]

$$J_{dr,gen} = \frac{qn_iW}{\tau_g} \tag{5.3}$$

where q is elementary charge constant, n_i is the intrinsic carrier concentration of silicon, W is the depletion layer width and τ_g is the generation lifetime, which depends on dopant concentration among other factors. Since the depletion layer width is dependent on the applied voltage, the output current also has a dependency on the applied bias voltage. In the logCMOS pixel, this would mean the leakage current is dependent on the pixel output.

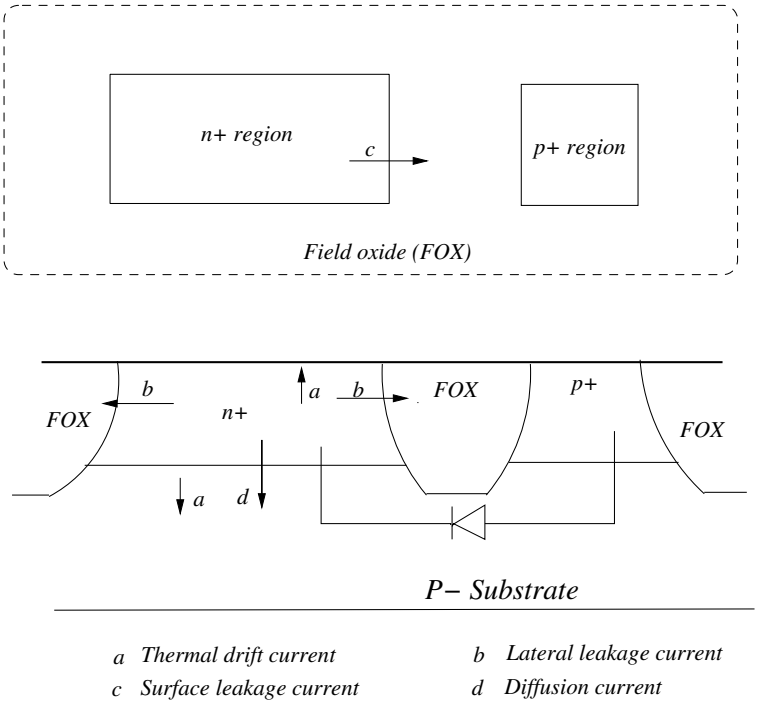

Figure 5.3: Sources of dark current in an n^+/p-sub diode in CMOS technology. The top figure shows the top view of a diode, whereas the lower figure shows the side view of the diode.

The diffusion current, on the other hand, is zero in regions away from junction due to uni-

form distribution and random movement of carriers. However, the carrier concentrations decreases near the depletion region giving rise to a larger diffusion current, which is dependent on the distance from the diffusion edge.

$$J_{dr,dif} = qD_n \frac{dn}{dx} \tag{5.4}$$

At the diffusion edge, this current is given as

$$J_{dr,dif} \cong \frac{qD_n n_i^2}{L_n N_A} \tag{5.5}$$

where D_n is the diffusion coefficient, N_A is the majority carrier concentration, and L_n is the diffusion length. In heavily doped regions, Auger recombination also affects the diffusion current by changing the lifetime and diffusion length of a carrier [65].

The net current, however, is dominated by the thermal-generation current owing to small values of intrinsic concentration in silicon. This net current has also been shown to have temperature dependence as follow [6]

$$I_{dr} = CT^{1.5} e^{-E_g/2kT} \tag{5.6}$$

where C is a constant, T is the absolute temperature, E_g is the bandgap energy, which also has a temperature dependence and k is the Boltzmann's constant. This means that the dark current in the logCMOS pixel will double for approximately every 10 degree Celsius rise in temperature, thereby further degrading the performance of the pixel.

Equations representing the various leakage current, however, are correct only when the reverse biased voltage across the diode exceeds $3kT/q$. As shown in Figure 5.4, for reverse bias voltages lower than this value, the leakage current reduces to zero at zero reverse bias voltage, before exponentially increasing for the forward bias voltages.

In addition to these normal leakage currents, there are parasitic leakage currents in a diode formed in a typical CMOS process. These owe their origins to several sources including the

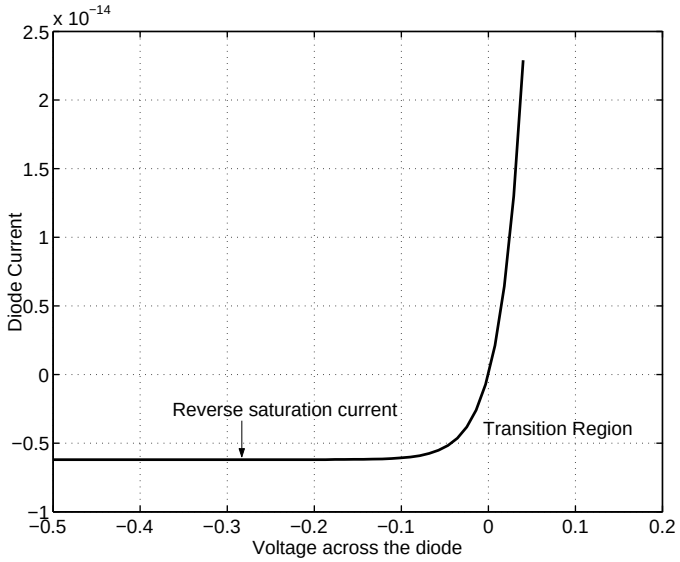

Figure 5.4: I-V characteristics of a typical diode in a typical CMOS process

dislocations near the isolations regions and surface damage [73, 74]. The former is caused by the contamination in the process and the various stresses applied in processing. Local Oxidation of Silicon (LOCOS) and Shallow Trench Isolation (STI) are the prominent ways to introduce isolation between devices in CMOS processes, with the latter being preferred for deepsubmicron processes. Both of these are known to introduce high mechanical stresses on the adjoining regions. Oxide stiffness at the temperatures used in LOCOS process is a prominent source of stress on the silicon wafer [75]. This stress causes local distortions by creating a tensile stress in the LOCOS area and a compressive stress in the active area [73].

STI introduces even more defects owing to the large stresses during trench formation [76, 77]. This stress is due to the visco-elastic stress in the oxide fill material along with the differential oxidation rates between the trench sidewalls and the oxidation surface[78]. Crystal defects, primarily due to ion implantation and thermal annealing also increase the number of defects.

Circuit simulators generally do not model these parasitic leakage currents, and hence fail to predict the dark current. There have been few attempts to model these effects. Shcherback and co-workers have empirically modelled the diode leakage in terms of layout parameters as a function of the pixel area and number of corners to account for the various leakage currents due

to dislocations.

$$I_{dr} = \alpha A + \beta n \tag{5.7}$$

Here α and β are empirical constants, with β having an inverse relationship with the corner angles. A is the area of the diode and n is the number of corners. From their experiments, it may be concluded that corners are responsible for higher leakage current than the edges. This model however, does not attribute any physical explanations to these parameters.

In another model for the dark current in different geometry photodiodes, Loukianova and co-workers have assumed that the dark current has three components [74]. The first is an area dependent term due to processes occurring in the depletion region. The second component is a length dependent leakage current from the p-n junction at the surface (mainly in areas where depletion comes to the surface). The third component needed to model the measured data was a constant term. The resulting equation for the dark current was

$$I_{dr} = J_1 A + J_2 L + I_3 \tag{5.8}$$

where, J_1 is the current density (A/μm^2) generated in bulk, A is the area of the junction in the bulk, J_2 is the current per μm generated in the surface, L is the length of the depletion at the surface and I_3 is a constant current. From the results of this study, it was found that for n$^+$/pwell photodiodes the constant term is negligible and the length dependent term dominates the area dependent term for the size of photodiodes typically used in pixels. Based on the experimental results, they also postulate that in addition to these basic sources, tunnelling plays an important source for the leakage current, particularly in the highly doped junctions with narrow depletion layer. Further, at higher voltages in these junctions, impact ionization was also observed to affect the dark current.

5.3 Process improvements to reduce leakage currents

On account of all leakage phenomena, a photodiode in a normal CMOS process has a high leakage current of the order of $1nA/cm^2$ [79]. This amount of leakage current would lead to about $1fA$ of leakage in a pixel of 10μm pitch. With the optical sensitivity of about $1fA/lux$, this is clearly a leakage current, which will affect the performance of logCMOS pixel in several natural scenes. The ideal way to reduce these currents would be to improve the process. Several ways have been proposed to reduce these leakage currents.

One possible option is to increase the available signal by capturing all incident photons. This will not reduce the dark current; however it will increase the signal to noise ratio. Techniques such as microlenses [80], hole accumulation diode [81] and extended junction geometry to provide multiple interactions with light [82] have been proposed to enhance the electric signal.

The majority of the process modification techniques, however, try to reduce either of the two major sources of parasitic leakage current that is either reduce the surface defects and/or the stresses caused by LOCOS or STI in neighbouring regions. Techniques proposed to reduce the surface defects include deuterium annealing [83, 84] and surface passivation [85]. The stresses caused at the active region to field oxide interface can be reduced by use of high temperatures during LOCOS or STI [73], rounded angles of the diode [86], special angles of field oxide [87], low and/or graded doping concentrations for junctions [88] and silicide exclusion masks for photosensitive area [89, 90]. An alternative approach is to separate the photodiode from the defects and/or stressed areas. Vertical separation can be achieved using pinned photodiodes, similar to structures used in CCD processes [91, 92, 93] or buried photodiodes [73, 24, 94, 95, 96]. Lateral separation can achieved using spacer etching barrier films [97], field stop layers or junction isolation regions (usually made of p+ regions in p-substrate devices in either LOCOS [79, 98, 99, 100, 101, 102] or STI [103, 104, 105]) and use of an isolated trench for the photodiode [106].

Some CMOS foundries are offering processes with additional process steps to fabricate photodiodes with reduced dark currents. Exact details of the fabrication steps being used and/or the

dark current performance from each of these processes are difficult to obtain. However, any process solution is costly to implement on account of extra processing steps required and therefore increases the cost of the image sensor produced. As an example, one process with improved photodiodes, available through the Europractice integrated circuit prototyping service, is 25% more expensive than its standard counterpart [107]. Hence, there is a need to develop ways to reduce the leakage currents on standard processes without involving use of any extra processing step.

5.4 Circuit improvements

Two approaches may be pursued to reduce the leakage current and/or its effect on the logarithmic pixel. The first of these is to change the circuit while the second is to improve the layout of the pixel. The former approach may not be able to reduce the dark current in the photodiode, however, the effect of the dark current on the performance of logCMOS pixel may be improved by proper design of the pixel.

5.4.1 Theory

One approach to do so would be to emulate the signal enhancing process modification techniques. Ward and co-workers have proposed a circuit using a bipolar Darlington circuit to enhance the signal from the photodiode [108]. However, with the logarithmic pixel, any gain provided to the photocurrent will also enhance the dark current and the net effect of any such circuit would be to add an offset. This may be observed by the following derivations, wherein the parameter 'k' represents the gain provided to the photocurrent.

$$y_1 = a + b\log(k(x+c)) \tag{5.9}$$

$$= a + b\log k + b\log(x+c) \tag{5.10}$$

Thus, no improvement in the performance of logCMOS pixel is gained. For devising other strategies, let us revisit the I-V characteristic of a photodiode as shown in Figure 5.4. An interesting feature of the curve is the transition region between the forward and reverse biased regions. The diode current makes a transition from a high positive current to a very low negative current on the two sides of the axes. However, with diode bias voltage at zero, the reverse saturation current is zero and hence the current flowing through the diode consists of the photocurrent only. A pixel capable of maintaining zero potential across the photodiode would hence have zero leakage current. One pixel, which can do so is shown in Figure 5.5

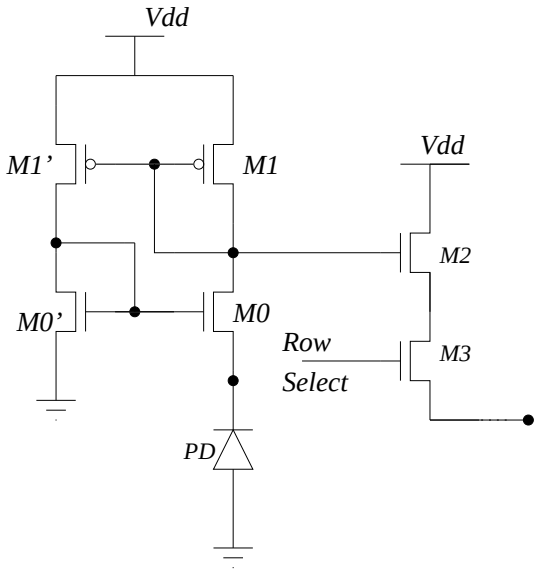

Figure 5.5: A double current mirror pixel to limit the voltage across the photodiode

To maintain near zero bias across the photodiode, the circuit shown in Figure 5.5, uses a double current mirror, with $M0$ and $M0'$ forming an nMOS current mirror while $M1 \& M1'$ form a pMOS current mirror [66]. Both mirrors are expected to work in subthreshold. The pMOS current mirror ensures the currents are identical in the two sides of the mirror. The identical current in the two sides, in turn, forces the gate-source voltage of the two nMOS transistor to be equal. This means that the voltage at the source of $M0$ should be zero, as the source of $M0'$ is grounded. The source voltage of $M0$, being the reverse biased voltage of the photodiode, will ensure that the leakage current of the photodiode remains zero for all pixels. Further since this condition is obtained by negative feedback, it is expected that pixel to pixel

variance will have minimum effect on it. The transistors $M2$ and $M3$ form the first stage of the readout circuit.

5.4.2 Experiments and results

Simulation of the circuit with the Cadence Spectre simulator for a 0.35 μm 3.3V p-substrate 3-metal, 2-poly Austria Micro Systems CSI CMOS process [109] shows a low and fairly constant level of voltage across the photodiode for a wide dynamic range of photocurrent, as shown in Figure 5.6. The logarithmic response of the pixel is also verified by the upper plot. Further the gain of the pixel per decade is appreciably higher than a normal nMOS load pixel. This stems from the fact that the pMOS load provides higher gain.

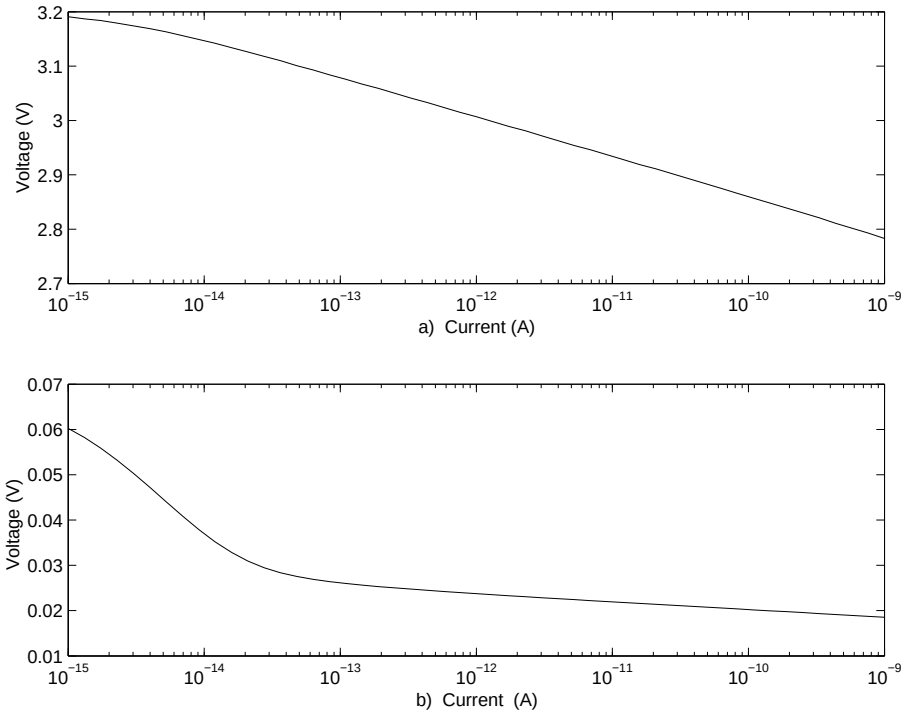

Figure 5.6: Results of simulation of the DCM pixel (a) Pixel output (b) Voltage across the photodiode

A 100×10 array of these pixels, with dimensions of 10μm×10μm, and a differential amplifier readout was used for test purposes. The array and the chip are described in details in the Appendix A.1. The differential amplifier readout circuit had the same dimensions as that

Parameter of the	pixel	DCM Pixel	Conventional Pixel
Offset	Mean	1.787	1.743
(V)	Std. Dev.	0.056	0.017
Gain	Mean	94.0	66.8
(mV/decade)	Std. Dev.	4.40	1.01
Bias	Mean	36.4	26.1
(fA)	Std. Dev.	12.9	6.3

Table 5.1: Statistics of the three parameters of the double current mirror (DCM) and the conventional pixels (630 each)

of the pixel used for calibration in the previous chapter. The transistors $M0$ and $M0'$ of Figure 5.5 had dimension of 1μm$/0.6\mu$m (W/L), while pMOS $M1$ and $M1'$ had dimensions of 10μm$/0.6\mu$m (W/L).

Experiments were performed with this pixel using the assembly used to measure the performance of the readout circuit, as explained in section 3.3.2. The experimental procedure was same as the one used for comparing the two readout circuits. Only the inner 630 pixels were used for comparison, to avoid any effects due to the additional stress on the terminal pixels. Uniform scenes of different light intensities were generated and the pixel responses at these intensities were stored. The pixel response to the input intensity was observed to be logarithmic as expected. Various parameters related to the pixel response were extracted from the responses of the pixels. In order to compare these parameters with that of a conventional pixel, the same experiments were also carried out with a conventional pixel with similar readout.

Table 5.1 compares the statistical values of the various parameters of the two pixel designs. As expected, the gain provided by the DCM pixels, 95 $mV/decade$, is significantly higher than that of the conventional pixels, owing to the use of pMOS loads. Thus, these pixels provide a higher resolution in their outputs. Further, the mean values of the offset parameter in the two types of pixels are comparable, as expected. This is due to the same readout circuit used in the two pixels. The variation of offset in DCM pixels is higher than that of conventional pixels. This can be attributed to pMOS transistors, which are known to have higher mismatch that their nMOS counterparts. The process parameters for Monte Carlo analysis as provided by the manufacturer support this claim [109].

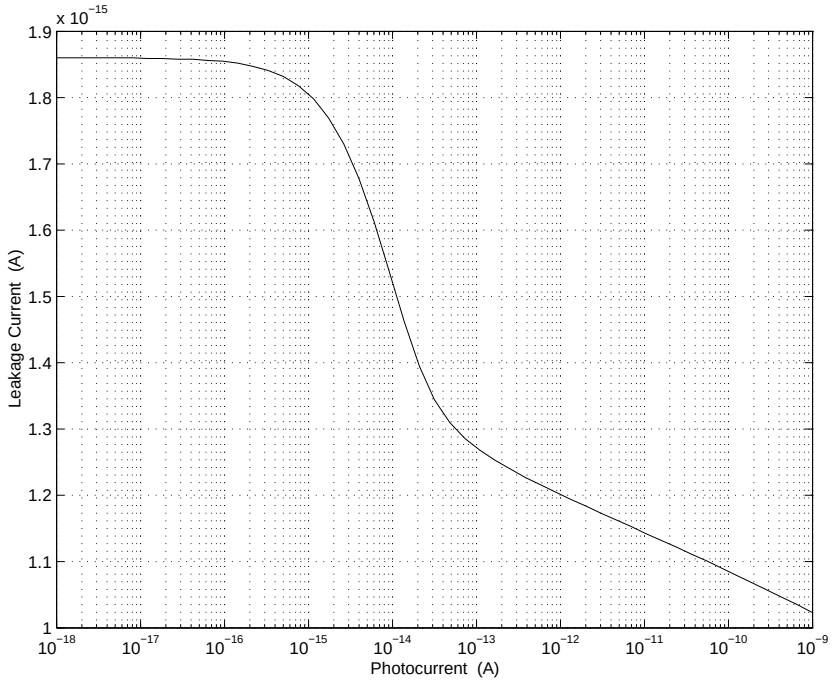

Figure 5.7: Diode leakage currents in the DCM pixel at various levels of photocurrent

The leakage dependent bias parameter and its variation unfortunately are higher than that of a conventional pixel. This means, contrary to our expectation, the DCM pixel has a larger dark current than that of the conventional pixel. It appears that the double current mirror pixel is failing to maintain a small enough bias across the photodiode to reduce its leakage current. One explanation could be failure of the two mirrors to have sufficient matching for the correct operation of the pixel. To minimise the pixel area, only small devices can be used in the current mirror and it appears that the resulting mismatch between devices may mean that the circuit is too far from ideal to be useful. Extended simulations of the circuit using more relaxed parameters show that the voltage across the diode fails to maintain zero levels at low currents. The simulation results, as shown in figure 5.7 and 5.8, do suggest a mismatch in the current mirrors at low currents. From these results, it is apparent that the DCM maintains a fairly low leakage current, when the photocurrent in the diode is high. However, with low photocurrents, the leakage current rises. The voltage across the photodiode also rises at low leakage currents.

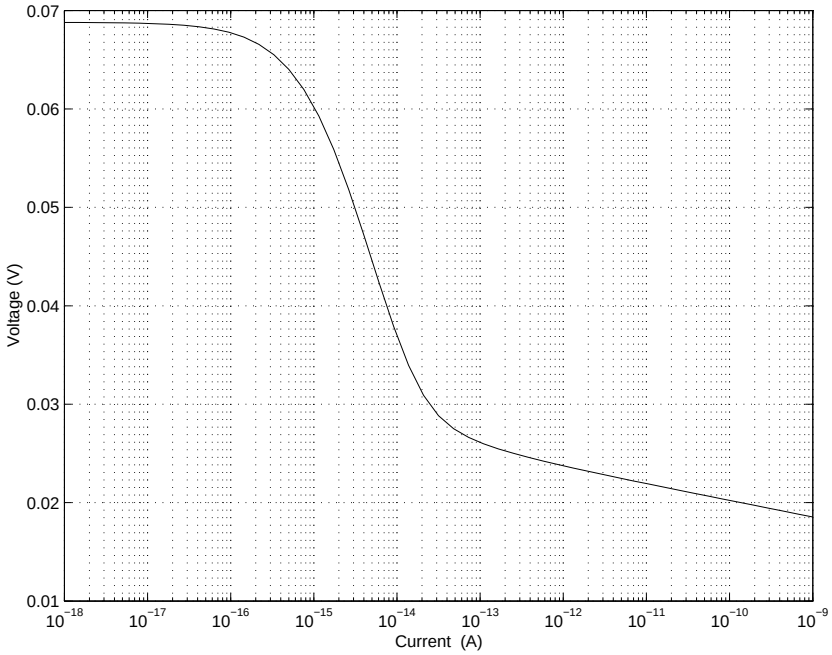

Figure 5.8: Voltage across the diode in the DCM pixel at different levels of photocurrent

5.5 Layout improvements

Failure of the double current mirror prompted an inquiry in potential use of circuit layout techniques to reduce the leakage current. Following the discussions in the Sections 5.2 and 5.3, it is clear that one of the principal components of the dark current has its origins in the diode edge s. This has prompted various researchers to propose solutions to introduce a barrier between these two regions using additional process steps in order to reduce the leakage current as described earlier. However, similar barriers can be introduced by using a suitable layout without the need of any extra process step.

Kopley, Vook and Dungan have proposed a biased guard layer, preferably of a conductive material, to block the doping of the active area diode during fabrication in an active pixel sensor [110]. If the guard layer is biased below the threshold voltage for formation of a channel this structure reduces leakage currents by separating the photodiode from the field oxide. Cheng and King have used a similar structure, but have utilised an n+ reset ring structure to reduce the dark current in active pixel sensor [111]. Thus, a guard ring around the diode should reduce the dark current of a logarithmic pixel.

5.5.1 Theory

In order to test the possibility of reducing leakage current using such a guard ring, simple logarithmic pixels of Figure 1.8, were manufactured with and without guard rings. Figure 5.9 shows the layout of a 10μm$\times$10μm simple logarithmic pixel, with a guard ring designed to be manufactured on an 0.35μm process with a fill factor of 40$\%$. Similarly, Figure 5.10 shows the same pixel without the guard ring structure. In the layout with the guard ring, the photodiode has been encircled by the thinnest possible ring of polysilicon, to separate the diffusion and field oxide region. The layout does not meet the design rule requirement of minimum diffusion spacings on two sides of a polysilicon feature, but this is not a process critical design rule violation [112]. The guard ring needs to be biased at a voltage below the threshold voltage of the technology. In an active pixel sensor, this guard ring can be used as the reset gate of the pixel to reduce its impact on the fill factor. However, in a logarithmic pixel this reset transistor is replaced by the load transistor which operates in subthreshold. To accommodate this transistor, the photodiode is connected to the load device using a metal bridge across the guard ring which is provided with a separate bias connection.

In addition, previous experience of electronic calibration of pixels in this technology has shown that the device leakage currents through nMOS devices with a zero gate-source bias are comparable to the dark current of the photodiodes used. This leakage current however reduces to insignificant values when a negative gate-source voltage in excess of -250mV is used. In this layout the guard ring around the photodiode therefore acts as the gate of an nMOS transistor in which the photodiode acts as the drain and the surrounding region acts as the source. Applying a positive voltage to the bias for the source and a zero voltage to the guard ring will ensure a negative gate-source bias on this guard transistor.

This type of pixel has been fabricated to determine the effectiveness of the guard ring. However, the space between the metal track on the right hand edge of Figure 5.9 and the guard ring is occupied by the left hand side circuit of the adjoining pixel. This means that it is possible to accommodate the guard structure with minimum reduction in fill factor. To study the effectiveness of the guard structure, a small array of 100$\times$ 10 pixels of both types of layout have been

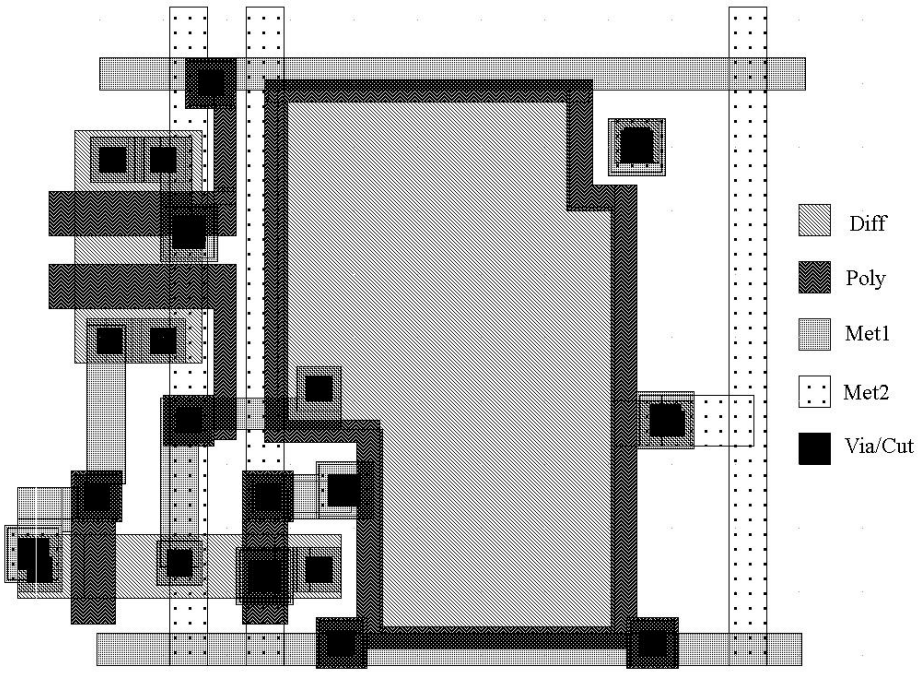

Figure 5.9: Layout of a logarithmic pixel with a guard ring.

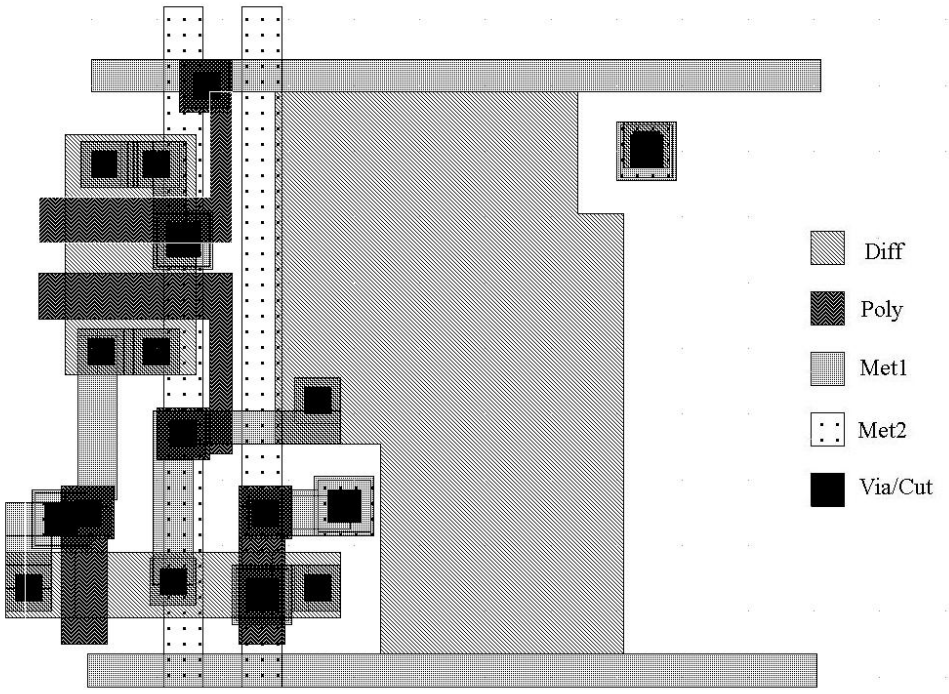

Figure 5.10: Layout of a logarithmic pixel with the guard ring removed.

fabricated on a standard 0.35μm CMOS process from Austria Microsystems.

Comparison of the Figures 5.9 and 5.10 shows that by placing the connection for the source bias of the guard nMOS over the non-photosensitive region of the adjacent pixel from the left hand side, it is possible to accommodate the guard structure with a minimum reduction in fill-factor. To determine the effectiveness of the guard structure, a small array of 100$\times$10 pixels of both layouts, with conventional source follower readout circuit were fabricated on a typical 0.35μm CMOS process from Austria Microsystems (C35). However, due to a change of the typical 0.35μm CMOS process offered by the foundry, the chip could not be manufactured in the same process as that of DCM pixels. The new process provides for four metal and two poly layers.

5.5.2 Experiments and results

Experiments involving these layouts were conducted with uniform scenes generated electronically. The strategy used to determine the effective dark current in each pixel in the array was based upon the technique that has been previously used to characterize the logarithmic pixels. This was possible because the electronic calibration circuit was also manufactured with these arrays. This removed the need to optically generate uniform light scenes to extract parameters. Further, presence of these circuit, helped in extraction of the offset and gain parameter, using the techniques used for electronic calibration. The bias parameter was extracted using the dark response of the pixels, as per the equation 5.1. However, the optical properties of the two arrays were still compared using uniform light scenes to eliminate the possibility of loss of optical performance from the pixels with layouts of guard ring. The three parameters of the two arrays of pixels are summarised in the following table.

The three parameters of the two arrays of pixels as calculated from the experimental are summarised in the Table 5.2. As expected the offset and gain parameters of the two different pixels are very similar. It can also be seen that the mean value of dark current related parameter of the layout with the guard ring is less than half of that of the pixel without the guard ring. In addition, the spread of the dark current related parameter has also been reduced to one third of

Parameters of the pixel		Without guard ring	With guard ring
Offset (in mV)	Mean	680	668
	Std	8.9	9.2
Gain (in mV/decade)	Mean	55.8	56.2
	Std	0.26	0.28
Bias (in fA)	Mean	0.75	0.31
	Std	0.27	0.10

Table 5.2: Statistics of the three parameters of pixels with and without guard ring (630 each)

its original value. This means that the worst case dark current in the pixel array is expected to be reduced by a factor of between two and three by using the guard ring. In fact, results show that in addition to reducing the mean and the standard deviation of the dark current related parameter, the presence of the guard ring also eliminated some particularly high dark currents that occurred near the edge of the array of pixels without a guard ring. In fact, using the guard ring reduced the worst case dark current from $2.8fA$ to less then $0.6fA$. The worst case dark current is therefore reduced by a factor of almost five.

5.6 Linear response from the layout

In addition to reducing the dark current, the new pixel layout has a second possible advantage. In particular the biasing scheme for the guard ring can be changed to increase the sensitivity of the pixel at low photocurrents.

To reduce the dark current, the guard ring is kept at zero bias and the pixel is operated continuously. However, it is also possible to apply a reset pulse on the guard ring. To understand the effect of this, let us consider the equivalent circuit shown in Figure 5.11. The figure shows that if the gate voltage of the reset transistor is held low the pixel will have a logarithmic response. However, if a positive pulse is applied to the gate the internal capacitance can be reset to a voltage above the gate bias for the load transistor. This will turn off the load transistor. The photocurrent will then discharge the pixel capacitance to create a linear response. However, eventually the voltage in the pixel will fall below the gate bias voltage for the load transistor

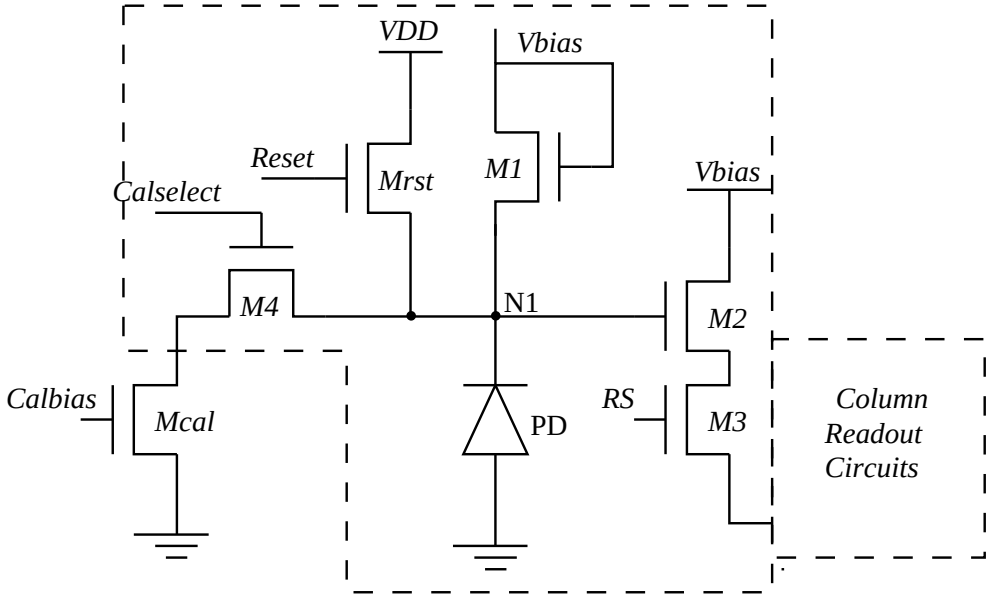

Figure 5.11: Equivalent schematics of the layout with guard ring used as a pixel with combined linear and logarithmic response

which will then supply current and an equilibrium will be achieved when the pixel output voltage is proportional to the logarithm of the photocurrent. If the pixel output voltage is measured at a predetermined time after the reset pulse has gone low the pixel will have a linear response at low light-levels and logarithmic response for high light-levels.

To show this new operating mode a pixel with a guard ring has been tested at various electronically generated currents. Figure 5.12 shows the temporal response of the pixel at three different photocurrents. As expected at low photocurrents, equivalent to low light intensities, the pixel capacitance is simply discharged by the photocurrent until the pixel is reset. In contrast at high photocurrents, an equilibrium is quickly achieved and the pixel voltage is constant. The relationship between this constant voltage and the photocurrent is most easily determined by measuring the pixel output voltage at the end of a constant integration time for different photocurrents. The results in Figure 5.13 show the linear relationship between output voltage and photocurrent at low photocurrents followed by a linear region at higher photocurrents. The pixel response curve undergoes a smooth but quick transition between these two regions of operation. At the extreme right hand side of the data there is also evidence of the beginnings of a

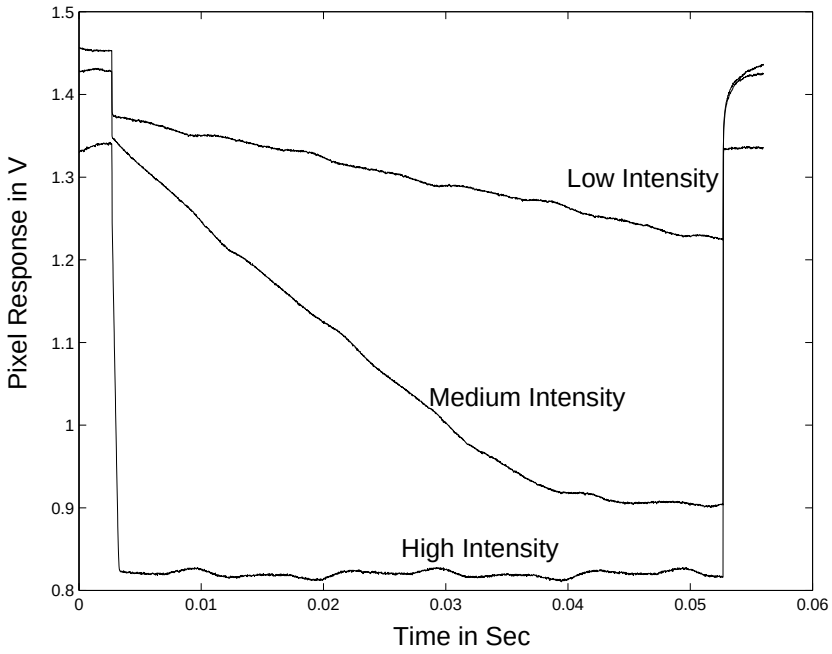

Figure 5.12: Response of the pixel as a function of time. The pixel starts integrating when the voltage at the guard ring is pulled low. The pixel is reset when the guard ring is pulled high again after 50 msec.

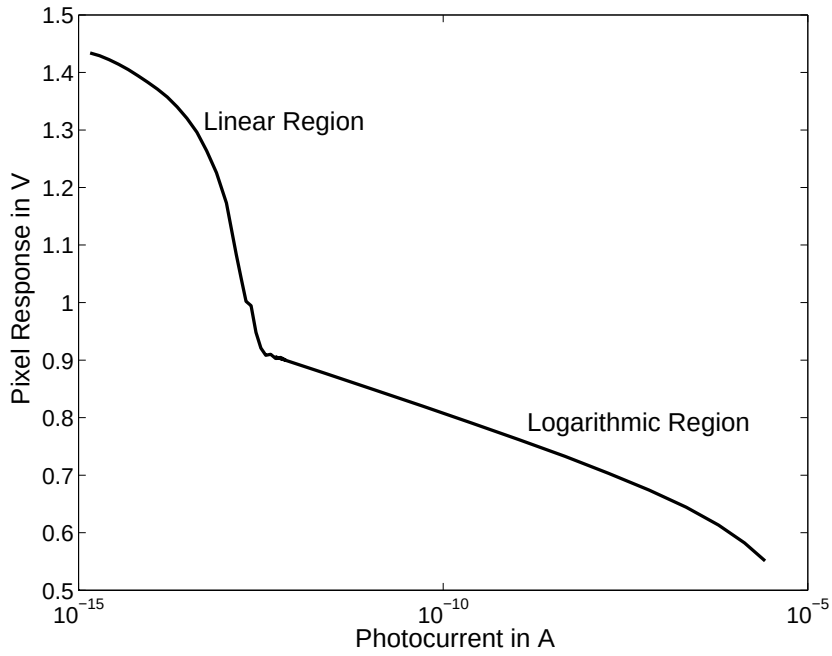

Figure 5.13: Response of the pixel at various photocurrents with fixed integration time. The pixel shows a linear response till a few picoamperes and a logarithmic response at higher photocurrents. At very high photocurrents there is also evidence of the beginnings of a breakdown in the logarithmic response as the load transistor is driven into moderate inversion.

breakdown in the logarithmic response as the load transistor is driven into moderate inversion.

5.7 Conclusion

The logarithmic pixels are not able to compete with their linear counterparts in low light conditions. This is due to high inherent leakage current in the CMOS process. This current not only limits the lowest imagable input intensity but also degrades the sensitivity of the logarithmic pixel for two decades above the lowest intensity. In addition, it also degrades the performance of two parameter calibration process. Since this leakage current flows even in absence of any illumination, it is often referred to as the dark current of the pixel.

The principal sources of this dark current can be broadly classified in two groups. The first group is present in every silicon junctions and owes its origin to thermal generation-recombination and drift phenomena. The second group owes its origin to the defects in CMOS processing. High stresses at the diffusion edges and contamination on the surface gives rise to these defects. Several process modifications have been suggested to reduce the number of defects thereby reducing the dark current. However, these are costly to implement. One low cost solution to remove the influence of dark current on pixel performance is to bias the photodiode at zero volts. At this bias, the only current which flows through the diode consists of the photocurrent. A double current mirror circuit shows the promise to provide such bias. A small array of these pixels was hence tested. However, the circuit failed to provide low enough bias across the diode to reduce the leakage current.

Failure of this circuit prompted an enquiry in the layout of the pixel. A new layout of the pixel with guard ring of polysilicon around the photodiode was investigated. This structure reduced the highest leakage current in the pixel by a factor of five. By reusing the guard ring as a reset device, the pixel can also be made to operate as a linear pixel for low intensities. For high intensities, this pixel continues to operate as a logarithmic pixel. This new response will be further characterised in the later chapters.

Chapter 6

Combined Linear and Logarithmic Response Pixels

The other two, slight air and purging fire,
Are both with thee, wherever I abide;
The first my thought, the other my desire,
These present-absent with swift motion slide.
William Shakespeare

In the previous chapter, it was observed that the layout for reducing the leakage current in the logCMOS pixel, could be operated as a pixel with linear response at low light intensities and a logarithmic response to high illuminations. This response will be further explored in this chapter. To differentiate from the response of logCMOS pixels, these pixels will be referred to as LLCMOS (for linear-logarithmic CMOS) pixel through out the rest of the thesis. In the first section of this chapter, a comparative study of linear-logarithmic response with that of the logarithmic response and the advantages as well as disadvantages of the new response will be investigated. A literature survey of similar responses obtained by other researchers will be presented in the second section. The rest of the chapter will be devoted to characterisation of the response of the LLCMOS pixels. A simple two-expression model would be used initially. However, finding it inadequate for all regions of operation, a unified model will be developed based on the operational physics of the devices used in the pixel. The new model will be verified using simulation as well experimental results.

6.1 Comparison of LLCMOS and logCMOS response

The low light linear response from the LLCMOS pixel provides a much higher gain in low light than that provided by the logCMOS pixels. Two features of the logarithmic pixel contribute to their low gain. First, the gain of the logarithmic pixel is limited by the subthreshold slope of the load device, and hence is limited to 50-65 mV/decade in typical CMOS processes. The gain in the linear pixel, on the other hand, is independent of any subthreshold slope and depends on the diode capacitance and the integration time. Further, as shown by Figure 5.2, the gain in logarithmic pixel reduces at low intensities on account of the dark current. The linear pixel gain is independent of the dark current as well as the photocurrent levels. Thus linearising the pixel output for low intensities significantly improves the pixel gain in low intensity areas of the scene.

In addition to improvement in gain, the reset-charge mechanism at low light also improves the dynamic performance of the logarithmic pixel. It may be recalled that one of the major limitations of double sampling techniques using high reference currents for fixed pattern noise removal in logCMOS pixels, was the inability of the pixel to charge from the reference frame to that of the image frame within the frame time for low intensity region of the scene [54]. This is so because a high reference current produces a low output from the logarithmic pixel. With a low input intensity, the steady state output of the pixel would be a high voltage. However, due to the low intensity, the current available to charge the diode capacitance from the low reference output to high scene output is very low. This means that the pixel would require a long time to settle down. Similar effects are observed when the input scene changes from bright illumination to low illumination. This effect is shown through simulations of a typical pixel using process parameters of a typical CMOS process, in Figure 6.1. It may be observed that when the input current change from low to high, the output waveform has a small discharging time on account of large current, though the vice versa is now true. This differential settling time introduces another source of transient fixed pattern noise not corrected by any of the correction mechanism discussed earlier [66].

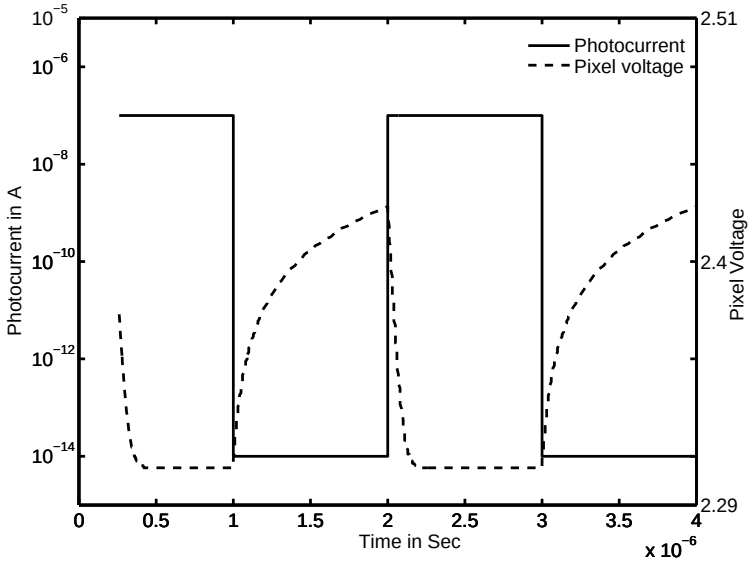

Figure 6.1: Dynamic response of logCMOS pixel with the input photocurrent changing from low intensity to high and vice versa. The pixel has different settling time for the two instances.

LLCMOS pixels, on the other hand, do not suffer from this defect as the pixel is reset at the beginning of every frame and hence the dynamic response is same for all photocurrents. Thus, it may be concluded that the LLCMOS pixel offers significant improvements over the conventional logCMOS pixel. However, the improvement comes at the price of a non-linear and complex relationship between the input intensity and the pixel output. Thus, in order for the pixel to be useful, further analysis of the pixel needs to be carried out.

6.2 Pixels with combined response

Before undertaking characterisation of the response, a literature survey of similar responses is being presented. The simplest approach to produce a pixel with combined response would be to use an active pixel sensor as a linear pixel in one frame and as a logarithmic pixel in second frame. These two outputs can then be merged using a threshold voltage to separate the two response regimes. Hence, in the first frame, integration of the photo-generated charge is used to account for low light intensities. In the second frame, the reset device is used in weak inversion, thereby producing logarithmic output. This accounts for the high illuminations, where the linear pixel saturates. Pixels such as those reported by Tu and co-workers [113],

Tabet and Hornsey [114] and Strom and co-workers [115] have used this strategy to produce the linear-logarithmic response. For example, the pixel as described by Strom and co-workers is shown in figure 6.2. It uses a $Logsel$ switch to change from linear operation to logarithmic pixel. However, any two-frame approach reduces the frame rate, making the pixel unsuitable for many applications. Further, the signal reconstruction also becomes an involved task on account of different FPN source in different frames.

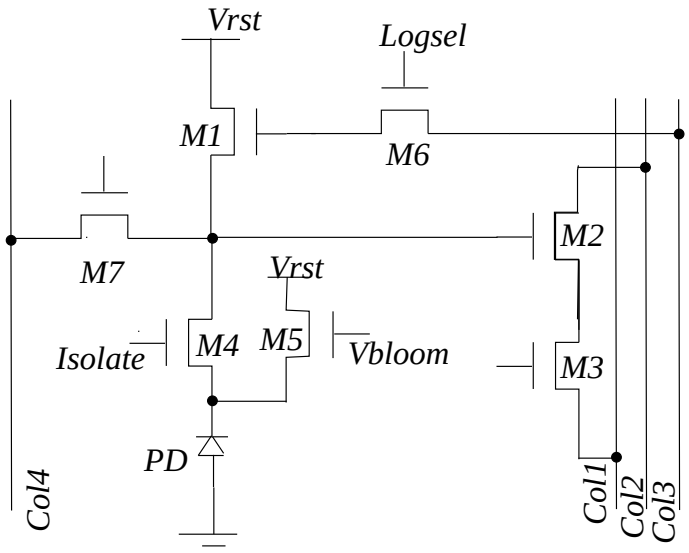

Figure 6.2: A pixel with two-frame readout providing linear-logarithmic response, using a Logsel switch

Approaches similar to the one obtained in the last chapter are capable of producing linear-logarithmic response using a single frame output. Fox, Hynecek and Dykaar have reported a pixel with linear-logarithmic response [116], with the pixel schematic similar to that of Figure 5.11 with the exception of the calibration switch and the current source. Further, their readout circuit is connected to the power supply, as shown in Figure 6.3. The advantage of this connection is that the bias to the logarithmic pixel can be varied to change the voltage at which the pixel switches from its linear operation to logarithmic operation. In a related work, they also report a pixel with two or more logarithmic load to improve the gain in logarithmic region of operation [117]

In a similar pixel, shown in Figure 6.4, Martin has used a switch between the reset device and the logarithmic device to provide for an in-pixel memory [118]. This switch may be used

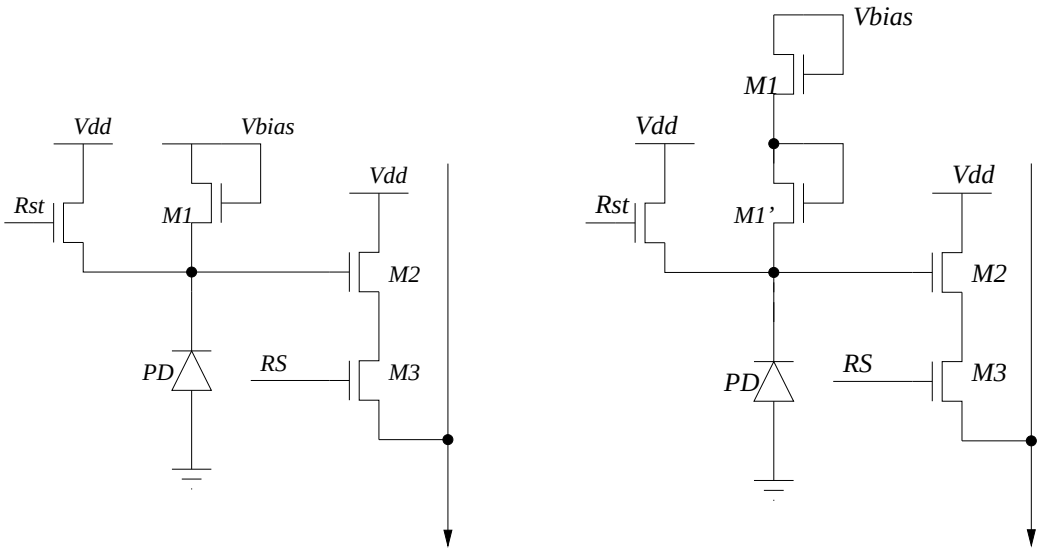

Figure 6.3: a) Pixel with linear-logarithmic response as described by Fox, Hynecek and Dykaar b) Same pixel with two logarithmic loads to improve the logarithmic region gain

to provide global reset and assist in fixed pattern noise correction. The pixel operates by transferring the reset value at the start of integration to the read node. The integration takes place on the photodiode capacitor thereby producing the linear response. Thus, during the readout, both outputs are available assisting in fixed pattern as well temporal noise reduction. However, it may be observed that the time provided to the logarithmic load to reach weak inversion is very small here. This will cause errors in some photocurrents, around the transition region from linear to logarithmic region of operation, as the diode capacitance takes significant time to charge from its reset value to the logarithmic output.

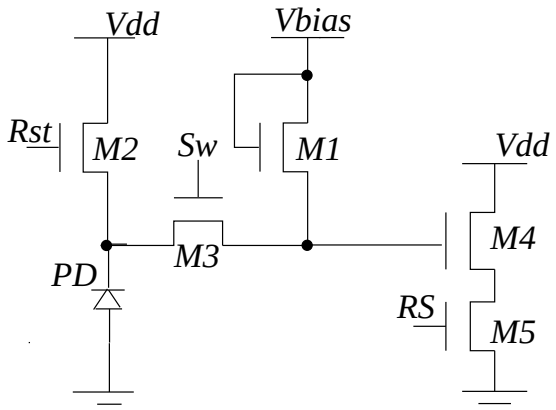

Figure 6.4: A pixel with combined linear and logarithmic response and a transfer switch as proposed by Martin

In another approach, Liu and co-workers have used a feedback loop from the pixel output to control a charge supply mechanism to delay the saturation [119]. As shown in figure 6.5, devices $M6 - M9$ are used in the feedback loop to drive the gate of device $M5$. It may be observed that this pixel operates the device $M5$ in weak inversion leading to logarithmic output at high currents. A higher gain is achieved due to two loads. However, a complex feedback loop is used with small gain in the circuit performance.

Commercial sensors from Dalsa and Photonfocus have also reported similar responses [120, 121]. Though no records of the pixel being used could be obtained, it is expected that the pixels proposed by either Martin or by Fox, et.al., is being used in these sensors, based on the patents obtained by these companies.

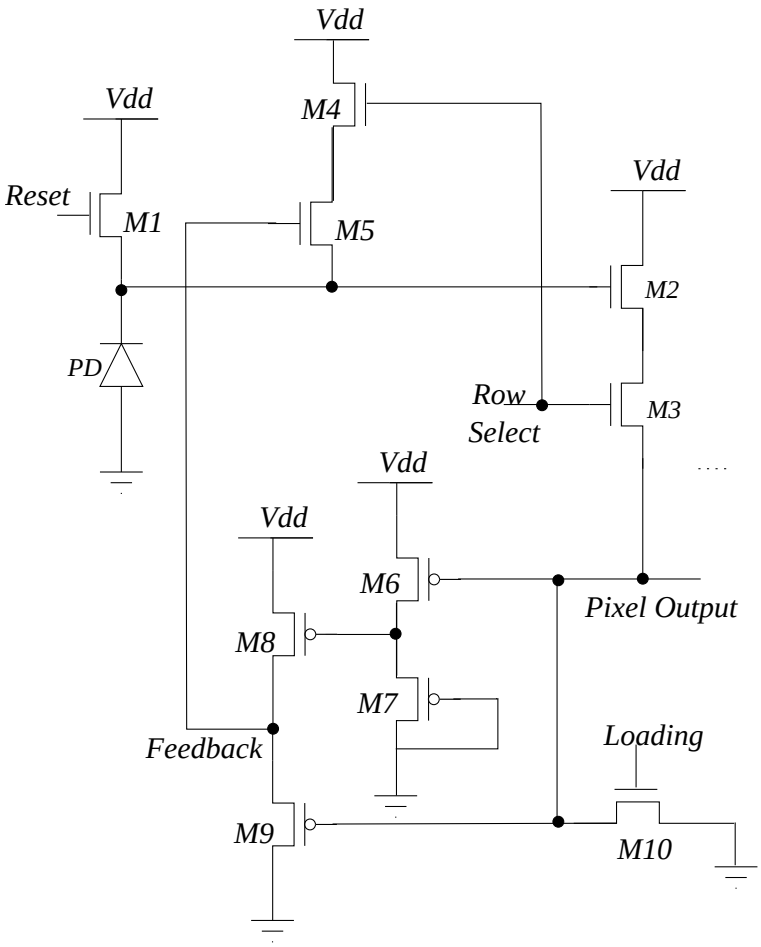

Figure 6.5: A pixel with combined linear and logarithmic response using a charge supply mechanism, proposed by Liu and co-workers

6.3 Two-equation model for LLCMOS pixels

Thus despite a complex relationship between the input and output, there is a significant interest in the response. The complexity of the response makes the output difficult to be represented on standard displays. Further, to extract the colour information, one requires the photocurrent flowing in each pixel. These two requirements call for a model to characterise the pixel response. The simplest approach to creating a model for the response of pixels, that combines a linear response at low illuminations with a logarithmic response at higher illuminations, would be to use one equation for the linear region and another one for the logarithmic region, together with a threshold point to determine which of the two equations should be used for a particular output. A simple model for the logarithmic region is the logarithmic pixel model of Joseph and Collins [62],

$$y = a + b\log(x + c) \tag{6.1}$$

where the terms have the same meaning as explained earlier in expressions 2.11, 2.12 and 2.13

The linear region operation of LLCMOS pixel could be modelled as $d + ex$, where d represents the offsets while e represents the gain in the linear region. As earlier, x represents the current flowing in the pixel

$$x \propto I_{photodiode} \tag{6.2}$$

Further, in the linear region, the pixel integrates the photo-generated charge on the diode capacitor, C, and hence the current-voltage relationship can be given as

$$I_{ph} + I_{dr} = C\frac{dV_{G,M2}}{dt} \tag{6.3}$$

Where I_{dr} is the dark current flowing through the diode without any light incident on it. On integrating the above expression, with limits set by the reset condition of $V_{G,M2} = V_{reset}$ at $t = 0$ and the pixel output $V_{G,M2} = V_{out}$ at $t = t_{int}$, one may obtain the following expression

for the linear region voltage.

$$V_{out} = V_{reset} - \frac{t_{int}(I_{ph} + I_{dr})}{C} \tag{6.4}$$

The gain e is, hence, given by the charging time constant t_{in}/C, where as the reset value gives the offset. This reset value depends on the type of the reset device used in the pixel. nMOS devices are preferred in conventional pixel design as they can be manufactured in the same well as rest of the circuit inside the pixel. However, the reset level for this device depends upon the photocurrent in previous frame. Thus, nMOS reset devices provide incomplete reset, as the diode voltage fails to reach a constant value for all photocurrents, at the end of reset interval. During this interval, the reset device attempts to operate in steady-state weak inversion. However, the interval is typically too small for the device to reach a steady state value for all photocurrents. This is true for most currents, in which the LLCMOS pixel is used in the linear region. For high currents, the reset device is able to reach steady-state operation; however, the output still depends on the current in previous frame. A pMOS type reset device on the other hand, is capable of providing complete reset and hence the reset value is always equal to the voltage at the drain node of the reset device.

To validate the two equation model, a LLCMOS pixel, with p-type reset device, was simulated for various integration times and photocurrents. A recursive algorithm was then used to extract the best fit parameters from the responses of the pixel in strict linear and logarithmic regions. Least mean square fit criterion was used to extract the parameters. A comparison of this two part model with the simulated response of a pixel shows that the model predicts the response of the pixel over most of its input range. However, as shown in Figure 6.6, this model fails to represent the transition region between the two types of response. Although, this region is quite small, the errors between the estimated and the actual photocurrent can be as large as 10%. This means that this model would not be able to predict the photocurrent to the accuracy of 1-2$\%$ needed to match the performance of human eye. A better model for the response of the pixel is therefore required to achieve reliable photocurrent extraction.

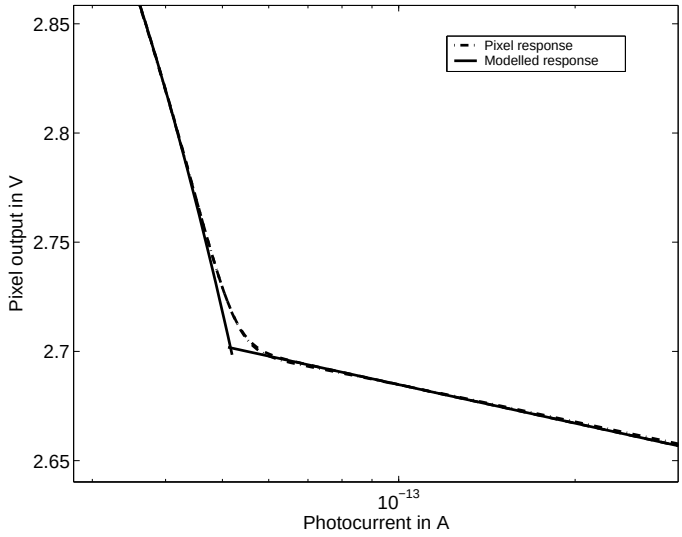

Figure 6.6: A comparison between the simulated response of a pixel and a model that assumes that the response is linear for photocurrents below a threshold value and logarithmic for higher photocurrents.

6.4 Device Physics based model

6.4.1 Model derivation

To obtain a better model for the pixel response, let us assume that the components in LLCMOS pixel, reproduced in Figure 6.7, are ideal. In this case, the reset device acts as an ideal switch that forces the pixel output voltage on the gate of transistor $M2$ to a particular voltage V_{reset}. The photogenerated current I_{ph} flowing through the photodiode PD will either discharge the capacitance on the gate of transistor $M2$ or flow through the load device $M1$. Using the model for the drain current proposed by Enz, Krummenacher and Vittoz [122]

$$I_{DS} = 2I_o \left[\ln \left(1 + \exp \frac{V_{GS} - V_T}{2n\phi_t} \right) \right]^2 \tag{6.5}$$

where $\phi_t = kT/q$, we may avoid any assumptions concerning the operating region of the load transistor. Then, since the source of the transistor $M1$ is connected to the gate of $M2$ and a voltage V_{bias} is applied to its gate

$$I_{ph} + I_{dr} = -C \frac{dV_{G,M2}}{dt} + 2I_o \left[\ln \left(1 + \exp \frac{V_{bias} - V_{G,M2} - V_{T,M1}}{2n\phi_t} \right) \right]^2 \tag{6.6}$$

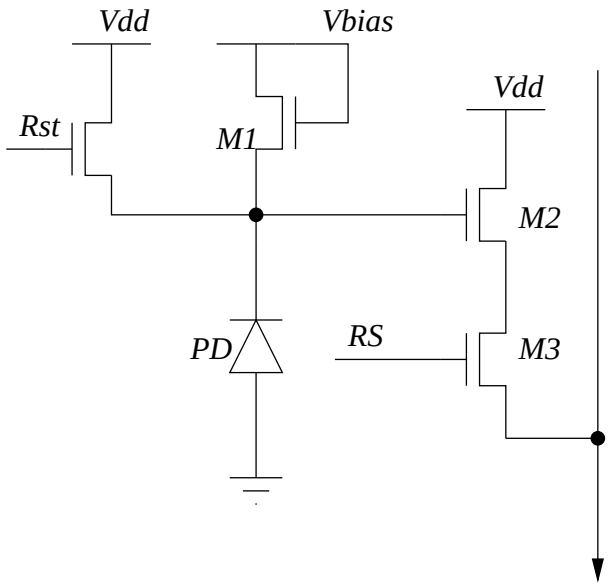

Figure 6.7: The LLCMOS pixel with combined linear and logarithmic response

Integrating this equation directly is difficult. To simplify the problem, let us consider the situation when the load transistor is operating in weak inversion. The logarithmic load in LLCMOS pixel works in weak inversion for the major part of operation and hence this assumption should be invalid only in a small region of very high currents. In weak inversion, the threshold voltage, $V_T > V_{GS}$. Then, the expression for the drain current becomes

$$I_{DS} = 2I_o \exp\left(\frac{V_{GS} - V_T}{2n\phi_t}\right) \tag{6.7}$$

and

$$I_{ph} + I_{dr} = -C\frac{dV_{G,M2}}{dt} + 2I_o \exp\left(\frac{V_{bias} - V_{G,M2} - V_T}{n\phi_t}\right) \tag{6.8}$$

Rearranging the equation by separating the variables,

$$-dt = \frac{CdV_{G,M2}}{I_{ph} + I_{dr} - 2I_o \exp\left(\frac{V_{bias}-V_T}{n\phi_t}\right) \exp\left(\frac{-V_{G,M2}}{n\phi_t}\right)} \tag{6.9}$$

Integrating this equation over an integration time t_{int}, using the conditions $V_{G,M2} = V_{reset}$ at $t = 0$ and $V_{G,M2} = V_{out}$ at $t = t_{int}$, and using $R = 2I_0 e^{(V_{bias}-V_{T,M1})/n\phi_t}$ for convenience gives

$$-t\Big]_{t=0}^{t=t_{int}} = \frac{n\phi_t C \log\left\{(I_{ph}+I_{dr})\exp\frac{V_{G,M2}}{n\phi_t} - R\right\}}{I_{ph}+I_{dr}}\Bigg]_{V_{G,M2}=V_{reset}}^{V_{G,M2}=V_{out}} \tag{6.10}$$

$$-t_{int} = \frac{n\phi_t C}{I_{ph}+I_{dr}}\left[\log\frac{(I_{ph}+I_{dr})\exp\frac{V_{out}}{n\phi_t} - R}{(I_{ph}+I_{dr})\exp\frac{V_{reset}}{n\phi_t} - R}\right] \tag{6.11}$$

Rearranging the above expression,

$$V_{out} = n\phi_t \log\left[\exp\left(\frac{V_{reset} - t_{int}(I_{ph}+I_{dr})/C}{n\phi_t}\right) + \frac{\left[1-\exp\left\{-t_{int}(I_{ph}+I_{dr})/(n\phi_t C)\right\}\right]R}{I_{ph}+I_{dr}}\right] \tag{6.12}$$

At low photocurrents or for a short integration time, the first part of the argument of the logarithm of this equation dominates and this equation reduces to the simple linear form

$$V_{out} = V_{reset} - t_{int}(I_{ph}+I_{dr})/C \tag{6.13}$$

Alternatively, at high photocurrents or after a long integration period, the second part of the argument dominates and equation 6.12 reduces to the form

$$V_{out} = V_{bias} - V_T - n\phi_t \log\frac{I_{ph}+I_{dr}}{2I_0} \tag{6.14}$$

which is equivalent to the model for the response of a logarithmic pixel developed by Joseph and Collins [62]. It is worth noting here that in most of the applications, LLCMOS pixel will be operated in logarithmic region, when the dark currents are negligible. This assumption may be used to remove dark current related terms in the second part of equation 6.12 and the logarithmic part of the equation 6.14.

The conditions that are needed for the logarithmic response to be observed are that

$$(1-\exp(-t_{int}(I_{ph}+I_{dr})/(n\phi_t C))) \approx 1 \tag{6.15}$$

and also that

$$\frac{2I_0 + I_{dr}}{I_{ph}} \exp\left(\frac{V_{bias} - V_{T,M1}}{n\phi_t}\right) > \exp\left(\frac{V_{reset} - t_{int}(I_{ph} + I_{dr})}{n\phi_t C}\right) \tag{6.16}$$

The first of these two conditions corresponds to a situation in which the voltage change caused by integrating the photocurrent, is large compared to $n\phi_t$. At normal operating temperatures, this corresponds to a voltage change of approximately 100mV and this condition is quickly satisfied. An equivalent interpretation of the second condition is most easily obtained following some simple algebra. This algebra shows that this condition is equivalent to

$$\frac{t_{int}(I_{ph} + I_{dr})}{C} > V_{reset} - V_{bias} + V_T - n\phi_t \log(2I_0/(I_{ph} + I_{dr})) \tag{6.17}$$

which is the condition needed to ensure that the source voltage of transistor $M1$ is low enough for all the photocurrent to flow through $M1$.

As expected, the model therefore simplifies to the two expected forms of response for low and high photocurrents. This is reassuring. However, the most important consequence of the fact that the model reduces to simpler forms at low and high photocurrents is that these simpler forms can be used to obtain the model parameters. In particular, if the pixel is operating in the logarithmic regime, it requires only two data points to be able to extract the additive offset and the gain parameters as shown in Section 4.1. The value of the capacitance can then be obtained from the output when the pixel is reset and a third data point corresponding to operating the pixel in its linear response mode. This value along with the pixel response at no light ($I_{ph} = 0$) may then be used to extract the dark current of the pixel using equation 6.13. With these parameters, the form of the model in Equation 6.12 means that the model can represent the response of a pixel to all photo-currents.

The validity of the model was verified using simulation results obtained from the Cadence Spectre simulator. Figure 6.8 shows the simulated response of a pixel with a p-type reset device for a constant integration time as a function of the photocurrent. For this integration time, the simulated pixel shows a linear response for photocurrents less than approximately $50fA$.

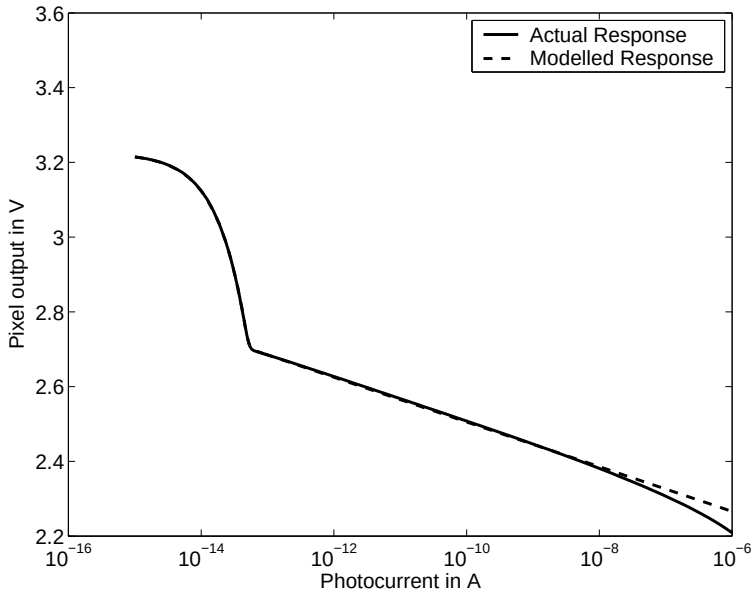

Figure 6.8: Response of a pixel at different photocurrents and a constant integration time

Then for larger currents the pixel shows a logarithmic response. Figure 6.8 actually shows the modelled response of the pixel as well as the simulated response. However, it is difficult to see the difference between the simulation results and the model for currents less than 1nA. In fact, as shown in Figure 6.9 with parameters extracted using the simple parameter extraction routine based upon only three data points, the model is capable of matching the simulated behaviour to an error of less than $1mV$.

The shape of the error curve in Figure 6.9 in logarithmic region is similar to the error curve obtained after simple parameter fitting on the response of a logarithmic pixel by Otim and co-workers [70]. This is because a very similar technique has been used to select the points used to extract the pixel parameters for this region of operation. In short, the best results are obtained when the two data points used to obtain the parameters for the logarithmic response are about three decades apart, while ensuring that neither point is when the load transistor is operating in moderate inversion.

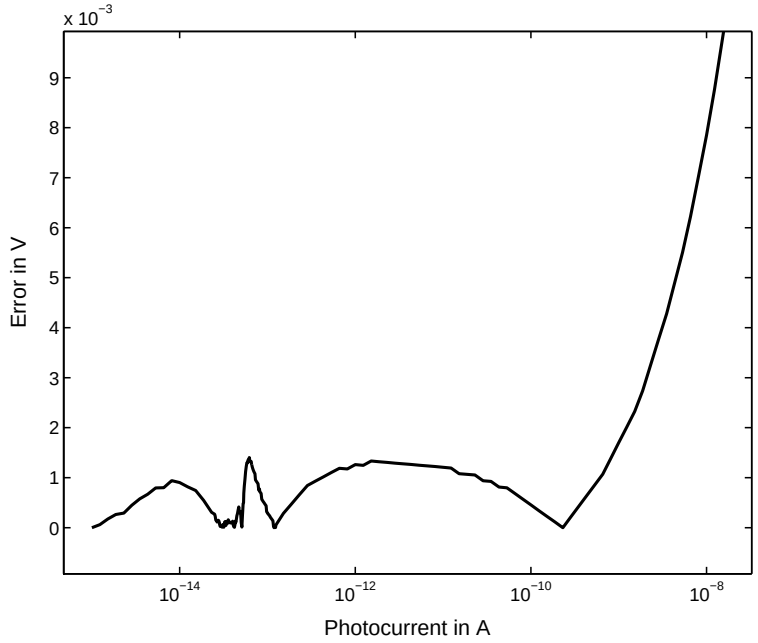

Figure 6.9: The plot of the error between the modelled and the simulated response of the LL-CMOS pixel

6.4.2 Modelling the very high intensity regions

The difference between the model and the simulated response at large currents occurs because the model assumes that transistor $M1$ is operating in weak inversion. This assumption can be avoided by solving equation 6.6. The solution to this equation must reduce to the solution to equation 6.12 at low currents. This condition leads to the solution

$$\begin{aligned} V_{out} &= n\phi_t \log \left[\exp\left(\frac{V_{reset} - t_{int}(I_{ph} + I_{dr})/C}{n\phi_t} \right) \right. \\ &+ \left. \frac{\left[1 - \exp\left\{-t_{int}(I_{ph} + I_{dr})/(n\phi_t C)\right\}\right] R}{\left(\exp\sqrt{I_P/2I_o} - 1\right)^2} \right] \end{aligned} \tag{6.18}$$

where again the parameter $R = e^{(V_{bias} - V_{T,M1})/n\phi_t}$ has been used for convenience.

This equation reduces to equation 6.13 for low photocurrents and/or short integration times. However, when equations 6.15 and 6.16 are satisfied, this equation reduces to the equation obtained by Otim and co-workers to model a logarithmic load, which operates either in weak or moderate inversion [70].

$$V_{out} = V_{bias} - V_T - 2n\phi_t \log\left(\exp\sqrt{I_P/2I_0} - 1\right) \tag{6.19}$$

As expected at comparatively low photocurrents, when

$$\exp\sqrt{I_P/2I_o} \approx 1 + \sqrt{I_P/2I_o} \tag{6.20}$$

this equation reduces to the equation obtained assuming that transistor $M1$ is operating in weak inversion.

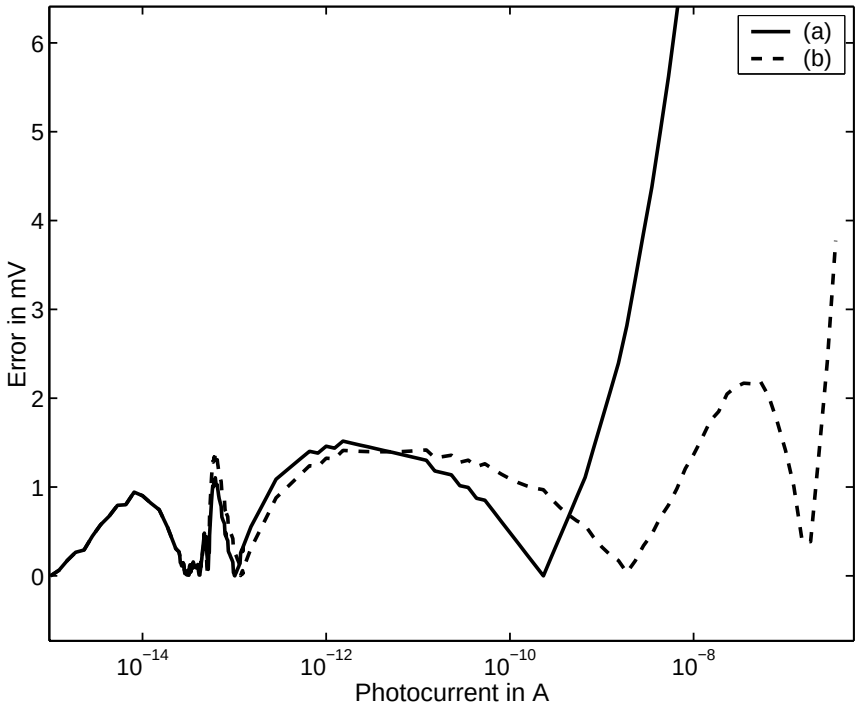

Figure 6.10: The plot of the error between the modelled and the simulated response of the combined response pixel. (a) Modelling weak inversion region using equation 6.12, (b) Modelling weak as well as moderate inversion region using equation 6.18.

The accuracy of the more complex model in equation 6.18, was verified using bounded nonlinear function minimization within MATLAB, to fit the model to simulated data. A comparison between the results of circuit simulations and this extended model, such as those shown in such as those shown in Figure 6.10, show that unlike the simpler model in equation 6.12, the extended model fits the pixel response at currents larger than $1nA$ accurately. Although this more complex model may be impractical for many applications, it clearly shows that the errors

with the simpler model at high currents arise from the fact that transistor $M1$ is no longer operating in weak inversion.

6.4.3 Modelling the readout circuits

To create a two dimensional array of selectable pixels suitable for an imaging sensor, each pixel must include readout circuits to selectively access to each pixel. Equation 6.12 has been derived without considering the effect of any readout circuit. This model therefore has to be modified to include the effect of these circuits. The most commonly used readout circuit is a selectable source follower circuit. This is a linear circuit that introduces a constant offset voltage between its input and output, the response of the readout circuits can therefore be represented using the equation

$$V_{out,readout} = O_r + G_r \times V_{out,pixel} \tag{6.21}$$

where O_r is the voltage offset and G_r is the gain. Equations 6.12 and 6.21 can be combined to show that the response of pixels including readout circuits can be represented using the equation

$$\begin{aligned} V_{out,readout} &= P' \log \left[\exp\left(\frac{V_{reset,out} - t_{int}(I_{ph} + I_{dark})Q'}{P'} \right) \right. \\ &\quad \left. + \frac{\{1 - \exp(-t_{int}(I_{ph} + I_{dark})Q'/P')\}\, R'}{(I_{ph} + I_{dark})} \right] \end{aligned} \tag{6.22}$$

where

$$V_{reset,out} = G_r \times V_{reset} + O_r \tag{6.23}$$

$$P' = G_r \times n\phi_t \tag{6.24}$$

$$Q' = G_r \times \frac{1}{C} \tag{6.25}$$

$$R' = 2I_0 \exp\left\{ \frac{G_r(V_{bias} - V_{T,M1}) + O_r}{P'} \right\} \tag{6.26}$$

The final form of the response as shown in equation 6.22 is very similar to that of pixel response model of equation 6.12 and hence can be broken in two simple equations in a way similar to that of equation 6.12. The output in the linear region can be given as

$$V_{out,readout,lin} = V_{reset,out} - t_{int}(I_{ph} + I_{dark})Q' \tag{6.27}$$

where as the output in the logarithmic region is given by

$$V_{out,readout,log} = P' \log R' + P' \log(I_{ph}) \tag{6.28}$$

Equations 6.27 and 6.28 enable a four-measurements scheme to extract the parameters to completely characterise the pixel. Two measurements in linear region are needed, one at a typical illumination to extract Q, while another at the dark response to extract I_{dark}. Similarly, in the logarithmic region, two measurements can be used to extract P and R, in a way similar to that for conventional logarithmic pixels.

Equally important is the fact that the model predicts the transition region and hence the shift in the transition regions of the image sensor, without explicitly incorporating a different parameter. Thus, the variation in the transition region from pixel to pixel can be predicted using the parameters from linear and logarithmic region of operation.

6.5 Comparison with experimental results

A pMOS reset device has the advantage that the pixel node is reset to the highest possible value and hence the parameter $V_{reset,out}$ of equation 6.22 is a constant for these pixels. The disadvantage of using this type of reset device is the large area required to form the n-well in which the pMOS device is manufactured. This means that an nMOS device which needs less area is the preferred means of creating a switch inside the pixel. The only difference that this makes to the model is that the voltage of the pixel after it is reset with an nMOS device is that dependent on the photocurrent at the time of reset. This parameter therefore has to be determined at the begin-

ning, or end, of the integration period. Using this measured value of the reset voltage, the model is able to predict the response of the pixel with an nMOS reset device, such as that shown in Figure 6.11. These simulation and model results clearly show the initial linear response of the pixel as the capacitance within the pixel is discharged by the photocurrent. Eventually, after about 2.3 ms in this particular case, the subthreshold current through the load transistor becomes significant and an equilibrium is achieved. Comparison of results from different simulations showed that as expected the voltage on the pixel node at equilibrium is proportional to the logarithm of the photocurrent. After a constant integration time, this pixel therefore shows the expected linear response for low photocurrents and logarithmic response for larger photocurrents.

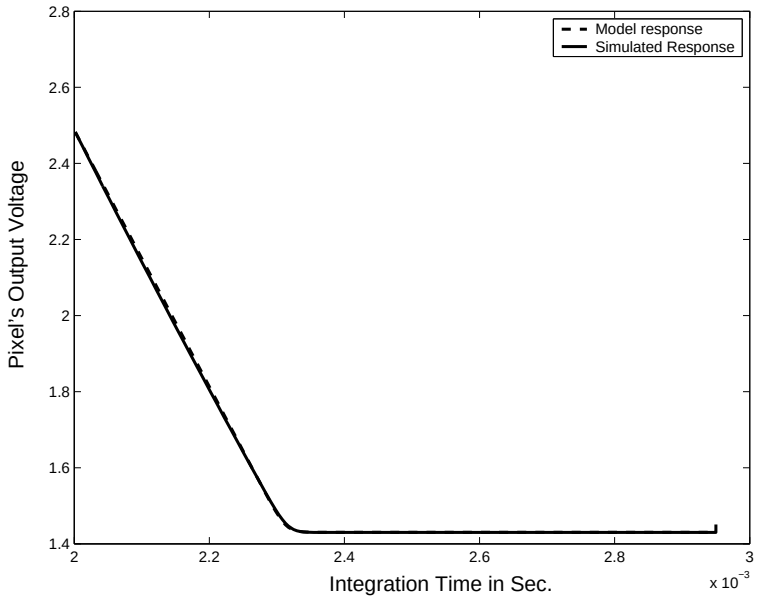

Figure 6.11: Response of a pixel to a constant photocurrent showing a linear response until 2.3 msec, followed by saturation to a value that represents the logarithm of the photo-current.

To verify the model, experiments were performed with pixels with nMOS type reset (Figure 6.7) fabricated using a typical $0.35\mu m$ CMOS process from Austria Microsystems. Each pixel has a pitch of 10 μm, with a fill factor of 44%. In addition to the basic LLCMOS pixel, provision was also made for calibration enable switch and calibration circuit, as used in the electronic calibration of logCMOS pixel. The pixel was tested using the optical and electronic assembly described in previous chapters. In addition to the light source (100 W, 12 V dc powered incandescent light source), the MOSFET present as the calibration device was also used to

generate pixel currents by using it as a voltage controlled current source.

The observed noise levels when measuring steady state values from the measurement system was 1.8 mV root mean squared. It was slightly higher than the previous set-up used for logCMOS pixel and the increase may be attributed to the fact the noise reducing capacitive filters were removed in the new measurement set-up to reduce their effect on the transient measurements. While measuring the pixel output in logarithmic region, the root mean squared noise levels were found to be 3.1 mV. It is difficult to confirm if this increase in noise arose from the pixel or the connection of the pixel to the measurement units through the pads and the packaging. The chip, described in Appendix A.2 did not have an on-chip analogue to digital converter and hence the analogue signals from the chip were converted to digital through an off-chip ADC. This meant that the pixel signal could have suffered additional interference and noise sources before it was digitised. Presence of on-chip ADC should have reduced the noise levels and hence should be considered in all future designs

To remove the temporal noise, the data from 25 frames was averaged in the logarithmic region. In the linear region, correlated measurement of reset voltage and the pixel output is expected to reduce the temporal noise. The measured response of a pixel including a source follower readout circuit is shown in Figure 6.12. Again these results show the expected transition from a linear response at small photocurrents and a logarithmic response at higher photocurrents. In addition, the different sets of data show that, as expected, the photocurrent, at which the transition between the two types of response occurs decreases when the either the integration time or the bias voltage increases. More specifically, as predicted from the condition for the transition between linear and logarithmic responses, these results show that the transition photocurrent is inversely proportional to the integration time and hence a three fold increase in integration time results in three fold decrease in the transition photocurrent. Further, the results also show that the transition voltage can be varied by changing the bias voltage. In fact, since the simulated gain of the readout circuits is 0.78, the change in bias voltage of 0.5 V is predicted to give a change in transition voltage of 0.39V. This compares well with the measured change of 0.38V.

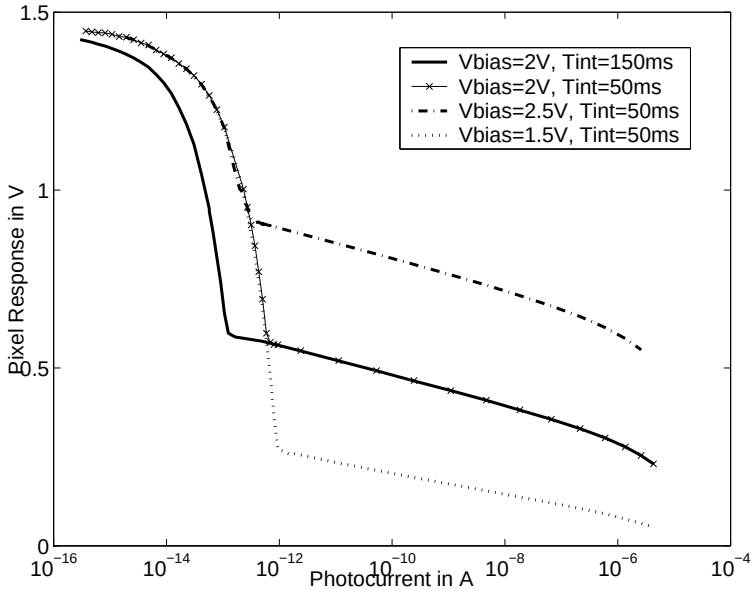

Figure 6.12: Experimental response curves from the pixel showing how the photo-current when the pixel changes from its linear to its logarithmic modes of operation can be controlled by changing either the integration time or the bias voltage on the load transistor.

Two procedures, a simple procedure based upon the response of the pixel at three photocurrents and a more complex least mean square error minimisation using many data points, were used to determine the parameters for typical pixels. The residual error with both methods of determining the model parameters was found to be below $2mV$ over a dynamic range of more than 6 decades. The slight increase in residual error with experimental data compared to the simulated values arises from the noise levels of the measurement system. Figure 6.13 shows the error between the measured response of the pixel and the response modelled, using parameters extracted using three calibration currents and the dark current. As predicted by the simulation results, the error between the two values increases at high intensities due to the load operating in moderate inversion. As also shown in Figure 6.13 this error can be further reduced by using the more complex model of equation 6.18. It was observed that the simple parameter extraction routine using two widely spaced data points in logarithmic region and one data point in linear region is sufficient to properly model the pixel response to a precision limited by temporal noise.

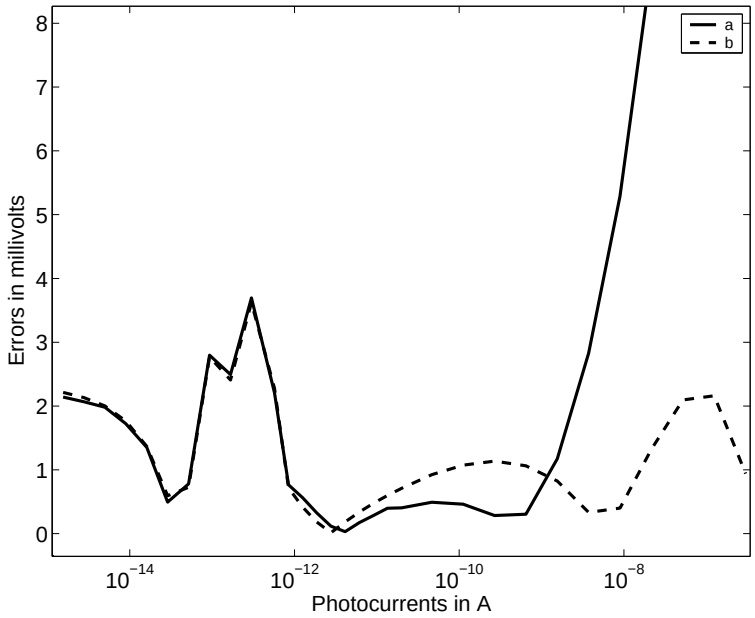

Figure 6.13: The errors between the predicted and the observed responses of the pixel. a) shows the errors from the simple model of equation 6.12, with parameters extracted using the three point method; and b) shows the errors from the more complex Equation no 6.18, with a least mean square error routine used to extract the parameters.

6.6 Conclusion

Pixels with linear response to low intensities and logarithmic response to high intensities are capable of providing high sensitivity in low intensity regions. They also improve the dynamic response of the logarithmic pixels, by ensuring a constant response time for any photocurrent. However, using simple linear and logarithmic expressions to model their complex response produces very high errors in the transition region between the linear and the logarithmic region of operation. A model based on the physics of the devices in the pixel has been derived and validated from simulated as well as experimental measurements. The model has also been extended to include the effect of the readout circuits as well as the very high intensity regions, where the logarithmic load device of the pixel starts operating in moderate inversion.

Chapter 7

Noise in Combined Response Sensors

All day I hear the noise of waters
Making moan,
Sad as the sea-bird is when, going
Forth alone,
He hears the winds cry to the water's
Monotone.
James Joyce

7.1 Parameter variations

As is the standard practice of designing pixel array, any design of LLCMOS pixels will try to maximise the photodiode area in the pixel to increase the amount of light captured and hence enhance sensitivity. This requires the use of small geometry devices. It has been shown in chapter 2, that the use of these devices is prone to high mismatch leading to fixed pattern noise in linear as well as logarithmic pixels. LLCMOS pixels operate in both these regimes and hence these pixels are also expected to suffer from fixed pattern noise. Fixed pattern noise has earlier been quantified as variations in model parameters. This approach may be extended to LLCMOS pixels.

The simple parameter extraction procedure introduced in the previous chapter was used to extract the parameters from 100×10 arrays of LLCMOS pixels manufactured in standard 0.35μm CMOS process from Austria Microsystems. Table 7.1 shows the average statistical

values of these parameters from a population of 10 chips. As expected, the parameter variations in the logarithmic regions are similar to those observed in the conventional logCMOS pixel with a source follower readout. The dark current levels are also similar to those reported earlier for this process. Among the linear region parameters, the gain has 0.9% variations which is slightly higher than the one obtained in logarithmic region. However, the pixel output in the linear region was observed to have variations of 48 mV peak to peak. Thus, the principal variations caused in the output are still additive and are evident through the $V_{reset,out}$ parameter.

Model	Parameter	Mean	Standard Deviation
P'	(mV/decade)	54.7	0.30
$V_{reset,out}$	(mV)	1430	8.75
Q'	(mV/msec-pA)	11.9	0.11
R'	($\times 10^{11}$)	17.8	9.9
I_{dark}	(fA)	0.82	0.25

Table 7.1: Statistics of the different model parameters of LLCMOS pixels from a population of chips(10 chips with 1000 pixels each)

It should be noted here that statistical data from these small arrays are only a representative figure of variations, as it does not include any spatial variations or the effects of second stage readout circuits present in larger arrays of pixels. Further, $V_{reset,out}$ is not an extracted parameter, rather a measured value. The data regarding this quantity was measured by forcing 0.1pA current to flow continuously through all pixels and averaged from several frames.

To identify the nature and the source of these variations, every constituent device of the pixel must be considered in detail. Figure 7.1 and equations 7.1-7.3 reproduce the schematic circuit diagram and the model of the combined response pixel, respectively. Equations 7.2 and 7.3 are also the expressions for a typical linear active pixel sensor and logCMOS pixel. Hence, the sources of parameter variations in these regimes will be identical to that of APS and logCMOS pixels. The analysis of FPN sources in logCMOS pixel presented in sections 2.1 and 3.3 will therefore be valid in the logarithmic regime of the LLCMOS pixel as well.

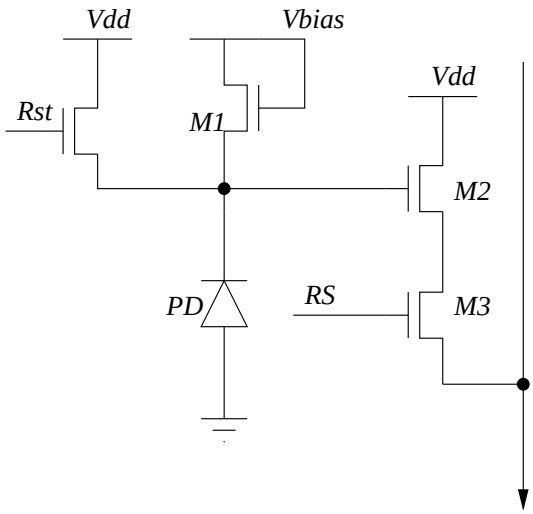

Figure 7.1: Pixel with combined linear and logarithmic response

$$V_{out,readout} = P' \log \left[\exp\left(\frac{V_{reset,out} - t_{int}(I_{ph} + I_{dark})Q'}{P'} \right) + \frac{\{1 - \exp(-t_{int}(I_{ph} + I_{dark})Q'/P')\}\, R'}{(I_{ph} + I_{dark})} \right] \quad (7.1)$$

$$V_{out,array,lin} = V_{reset,out} - t_{int}(I_{ph} + I_{dark})Q' \quad (7.2)$$

$$V_{out,array,log} = P' \log R' + P' \log(I_{ph}) \quad (7.3)$$

Further, the linear and the logarithmic operation regimes use the same readout circuit and hence the variations in the readout circuit are also shared by the two regimes. This means that the readout circuit introduces offset as well as gain variations in both regions of operation. The former owe their origins to the threshold voltage and current gain factor variations (Section 2.1). The later may be traced to higher order effects such as channel length modulation and body effect (Section 3.3). In addition, due to the non-steady state operation of the readout circuits in LLCMOS pixel, variations in the parasitic capacitances in the readout chain, can also introduce another form of fixed pattern noise [123].

Another principal source of FPN in the linear regime is the reset device, which affects the reset voltage of the pixel, $V_{reset,pixel}$. As explained in the previous chapter, with the preferred

nMOS reset device, the reset level depends on the photocurrent in the previous frame. The reset device attempts to reach weak inversion for this current, wherein its source voltage will be linearly related to $V_{DD} - V_{T,M_{rst}}$. However, due to the limited reset time, it fails to do so for most low currents. Even in these situations of incomplete reset, the reset voltage is dependent upon the threshold voltage of the reset device. This means that V_T variations in the threshold device would lead to an offset variation in the reset voltage. Further, since the final integrated value is dependent on this reset voltage; it will also suffer variations due to V_T variations in the reset device.

Any photodiode variations will play different roles in the two regimes. It has been shown earlier that the variations in diode area and quantum efficiency lead to offset variations in the logCMOS pixel. In the linear region however, these lead to gain variations, as is evident from equation 7.2. Further, variations in diode capacitance will also introduce another source of gain error.

Equally important is the pixel behaviour in the transition region between the linear and logarithmic region. This is dependent on the parameters of both linear as well as the logarithmic region. Variations in any of the parameters will affect the transition region of the pixel, thereby introducing an aspect to the fixed pattern noise which is not shared by conventional pixels. The levels of parameter variations recorded will shift the transition region from pixel to pixel. Any photocurrent extraction routine used to create an image may hence confuse the operating region of a pixel producing incorrect photocurrents.

7.2 FPN correction strategy

It has been observed that if uncorrected, these levels of parameter variations will lead to large contrast error in linear as well logarithmic pixels. Hence, LLCMOS pixels will also suffer from large contrast error unless FPN is corrected. Further, owing to different principles of operation in the two regions, the correction strategy should also be different. The strategy in the linear region should be very similar to the one used in linear pixels, on account of identical sources

and nature of the FPN. The same is true for the logarithmic region.

FPN correction schemes in linear pixels have been studied earlier in Section 2.2. Correlated or differential double sampling is used in these pixels to correct for the dominant additive fixed pattern noise. Removing the offset from equation 7.2, the signal may be represented as $t_{int}I_PQ$. Any variation in the gain will hence cause a linear error, k_{lin} in the extracted photocurrent, as follows

$$k_{lin} = \frac{\delta I_P}{I_P} = \frac{\delta Q'}{Q'} \tag{7.4}$$

As explained earlier, for the corrected image to display all intensities distinguishable by the end-user, this error should be less than the contrast threshold of the human visual system. This means k_{lin} should be less than 2% and hence to satisfy the equation 7.4, the gain variations in the linear region, should be less than 2% to achieve good quality images. The parameter spread reported earlier meets this requirement. However, systems have also been reported wherein this error is higher than this limit [124] and techniques have been proposed to correct for the gain variations in linear pixels as well [125, 126]. Therefore, linear gain variations should be measured in any future LLCMOS array in order to identify the correct procedure of FPN reduction.

For the logarithmic regions, gain as well as offset needs to be corrected, unless the gain variation to the gain ratio is sufficiently low, as discussed in Section 3.2. Schemes involving double sampling will produce a contrast error which is dependent on this ratio as well as the calibration current, as derived earlier

$$k_{log} = \frac{100\Delta P'}{P'} \log(I_{P,in}/I_{P,calib}) \tag{7.5}$$

With the linear region extending to 2 or 3 decades of intensity, the logarithmic region still extends to 5 or 6 decades. Again, as argued in Section 3.2, with the level of parameter spread recorded, both offset and gain parameters need to be corrected. The results of FPN correction using double sampling in the linear region and two parameter correction in logarithmic region

are expected to be similar to those obtained for APS and logCMOS pixels.

However, FPN correction in the transition regions needs further consideration. The pixel response in this region is complex and non-linear. Hence, the only way to correct for the FPN would be to extract the true photocurrent. In addition this extraction procedure will also remove the confusion regarding the operating region of the pixel due to spread in pixel parameters. Photocurrent extraction is also needed to convert the unique response of the pixel to any standard data encoding format. This is necessitated as data produced by any camera is often processed by various signal processing algorithms to assist in storage, display and analysis. These algorithms have been derived for standard data encoding formats and they will be unable to process the response of LLCMOS pixels. Considering this unique non-linear response, it is ideal to extract the amount of photocurrent flowing in each pixel and use this photocurrent to achieve the standard forms required by the signal processing algorithms. The extraction routine will hence be derived for the complete operating regime of the LLCMOS pixel.

7.3 Photocurrent extraction

From the model expression, it may be observed that simple expressions can be used to determine the photocurrent in the linear and logarithm regions. However, the same is not true in the transition region. In addition, parameter variations mean that it is difficult to predict the operating regime for currents near the transition and hence there is also a need to devise the strategy to determine the operating region of operation.

Further, the non-linear response means that the extraction procedure has to be either an exhaustive search process or an iterative process. To perform an exhaustive search, one needs to compute the response of a pixel at every photocurrent (limited only by the required resolution and the noise of the system). For a pMOS type reset pixel, this is a straightforward process, as the pixel response is determined by four constant parameters. For an nMOS type reset pixel, however, V_{reset} is measured with every output and is not constant. That means to prepare an exhaustive search matrix, this matrix must be calculated for every possible reset value, as well

(again limited by resolution required and noise levels). This will lead to a very large matrix and is not an efficient process.

An iterative process on the whole dynamic range, on the other hand, will be a process with very high time complexity. However, the simple pixel response in the strict linear and logarithmic regions can be used to reduce this complexity. The first step is to determine, if the pixel is operating in the strict linear or logarithmic regions. The easiest approach would be to use a threshold, above which every output is linear and another threshold, below which every output is logarithmic. However, these thresholds would change from pixel to pixel due to parameter variation. Hence, a better approach is to mathematically verify the region of operation. One way to do so would be to use the measured response to calculate two photocurrents. One, assuming the pixel was operating in linear region, I_{lin} and other assuming the pixel was operating in logarithmic region, I_{log}. The next step would be to compute the pixel response at these currents using the pixel model and extracted parameters. These two responses should be compared to the measured value. The photocurrent and the region of operation will be given by the value, whose difference from the measured response is within model error. These operations are performed through steps 2-6 of the algorithm presented in the box.

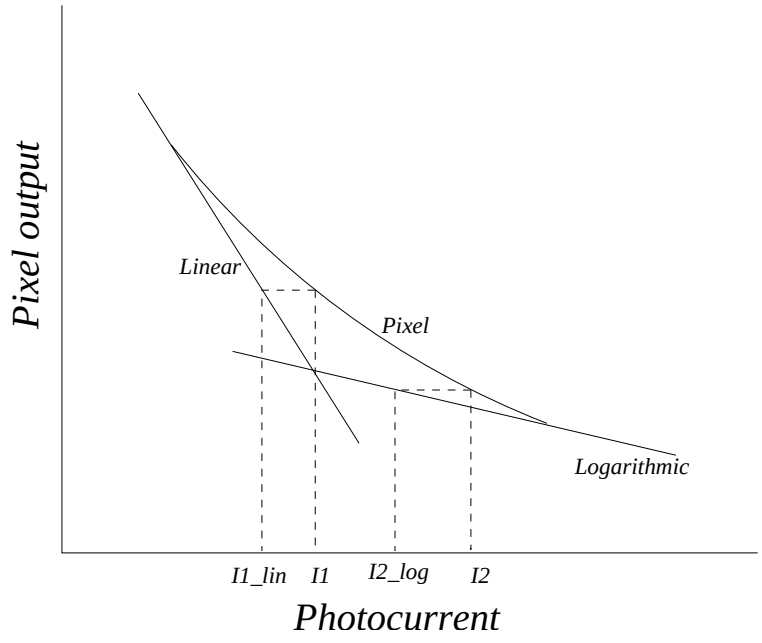

Figure 7.2: Figure showing the currents extracted in transition region assuming linear or logarithmic operation are always less than the actual current.

Algorithm - Intelligent Iterative Search

1. Compute the pixel parameters from simple parameter extraction procedure.
2. From the measured output and the reset levels, compute two photocurrents, which would have flown in the pixel, had it been completely linear or completely logarithmic for these values.
3. Compute the response of the pixel using its full model and its parameters at both of these currents.
4. Calculate the difference between these computed responses and the measured response of the pixel.
5. If either of the differences is below the maximum error bound, the corresponding current gives the current in the pixel. $\Rightarrow$ END
6. If neither of these produce differences below the error bound, the pixel is operating in transition region. Use the current corresponding to lower error as the starting point of iterative computation.
7. Use a divide-by-2 and conquer algorithm (Binary search) with starting point and a current one decade higher than the starting points as two seeds. Compute the error at these two currents and recursively converge to the photocurrent within the error bounds. $\Rightarrow$ END

If however, neither of the two currents produces a response within the model error, the pixel is operating in the transition region. Here, an iterative scheme is unavoidable. A simple divide-by-2 scheme (binary search) can be used for this purpose. One of the initial limits of the binary search algorithm could be the current producing the lower error in step 4 of the algorithm. To identify the other limit, let us consider Figure 7.2, which shows the extracted currents assuming linear or logarithmic operation of the pixel. These currents $I1_{lin}$ and $I2_{log}$, will always be

smaller than the actual current flowing in the pixel, $I1$ and $I2$. Further, the maximum transition region width measured from experiments is one decade and hence a higher limit of one decade away from the first current would encompass the whole transition region. Binary search is known to have complexity of $log_2 n$ and hence, it will converge within 10 iterations to an error below the model error in one decade of photocurrents.

Using the prescribed algorithm, currents have been extracted from simulation data. Figure 7.3 shows the absolute error in the extracted currents expressed as a percentage of the actual current. It is worth noting that the error shape is identical to that of the model error. It is further worth recalling that these absolute errors appear as systematic error in the output of every pixel and hence do not affect the relative contrast in the image [71].

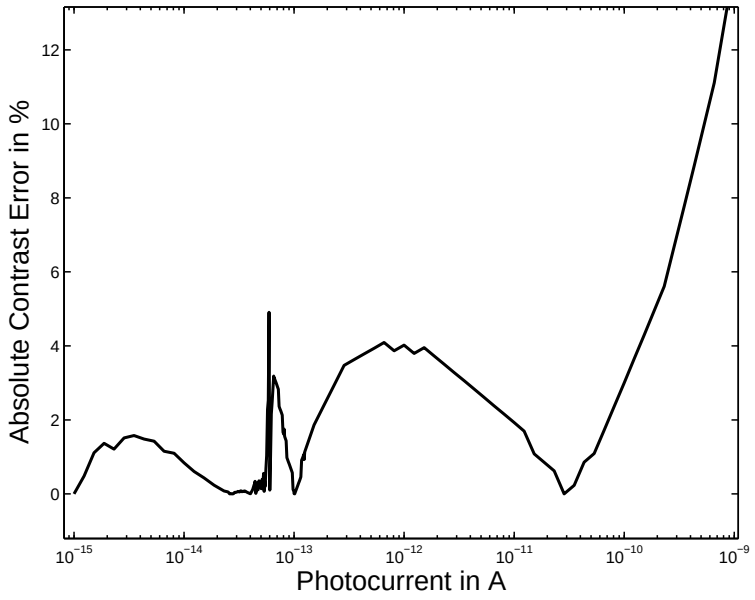

Figure 7.3: Absolute error as expressed as percentage of the photocurrent when using the proposed photocurrent extraction routine.

7.4 Temporal noise

Before extracting the pixel parameters and applying any correction strategy to remove FPN, one has to remove the temporal noise in the pixel. It has been observed in the last chapter that the temporal noise levels in the measurement system are as high as 3.1 mV rms. This will

lead to errors as high as 9% contrast change in the logarithmic region of operation. The effect of the noise on the photocurrent extraction procedure will change as the pixel changes from linear to logarithmic operation. This is because the high gain in linear region means that the current extraction procedure can withstand higher temporal noise than in logarithmic region. To better visualise this, let us consider the condition of obtaining less than 2% relative error in the extraction procedure. The noise level should be less than $0.02Q'$ (Q' is the gain in the linear region) in the linear region to meet this requirement. In the logarithmic region, the same figure is $P' \log(1.02)$. With $\log(1.02) \approx 0.02$, this means that the acceptable noise levels depends on gains, P'. The linear region gain Q' is much higher than the logarithmic region gain P' and hence more noise is tolerated in linear region. In the transition region, the noise level, which could be tolerated, changes smoothly between these two limits.

The temporal noise sources in both linear as well logarithmic pixels have been extensively studied [127, 36]. The LLCMOS pixels are expected to suffer from the same sources, which have been listed in the Table 7.2. Of these, the most prominent have been observed to be the ones originating in the channel of the reset and the logarithmic load device. The largest contribution in these has the form of "kTC" noise. In the linear or logarithmic region, the noise behaviour would be as expected for linear and logarithmic pixel. In the transition region, however, the two sources of "kTC" noise would interact. The net noise in transition region would still be correlated with the reset noise; however, the correlation would decrease as the pixel moves in logarithmic region.

Due to absence of an on-chip ADC, the correlated double sampling with the current design involves off-chip measurements, which add additional noise on the signal. This means CDS would be unable to remove temporal noise and hence averaging would be required in the linear region. Further, the only way to remove temporal noise in the logarithmic region data is to average it over several frames. In the transition region, correlated double sampling will reduce the temporal noise to some extent owing to some correlation between the reset and the integrated noise. However, to remove the rest of noise, one will have to average the pixel outputs from different frames.

Source of Noise	Type of Noise	Comments
Photodiode	Thermal, Shot, Flicker	Under no illumination, thermal excitation produces noise. Optical excitation produces two components of noise, photoexcitation fluctuations and fluctuations of generated carriers[128]
Logarithmic Load	Thermal, Shot	Low 1/f due to subthreshold operation [36]
Reset Device	Thermal, Shot	The reset device attempts to reach subthreshold operation [127, 129, 130]
Source Follower	1/f	Due to linear operation [127, 131, 132]
Switch	Thermal, 1/f	
ADC	Thermal, Quantisation	

Table 7.2: Sources of temporal noise in the LLCMOS pixel

A concern with averaging in transition region is that the net noise can move the pixel in different operating regimes in different frame, due to the very sharp transition region of the pixel. Hence, at a constant integration time, the pixel could be operating in transition region in one frame and in logarithmic (or linear) in another frame. This means that the averaging process will be averaging different noise sources in different frames and hence a much larger number of frames would be required to produce good quality image in the transition region. Another problem due to temporal noise is the bounding limits of the divide-by-2 search algorithm. For some currents in Figure 7.2, the temporal noise in the pixel output may lead to a condition, wherein the extrapolated current producing lower error is higher than the actual current. Hence the divide-by-2 algorithm would never converge.

With uncorrected temporal noise in the transition region, the errors from the photocurrent extraction procedure will increase. To study this effect, simulated data was used in the photocurrent extraction procedure with different amounts of Gaussian noise added to it. To remove the convergence errors due to temporal noise, the lower limit of binary search algorithm was placed at a current which was 20% lower than the extrapolated currents. Figure 7.4 shows the maximum error in the extracted photocurrent in the transition region. As discussed earlier, the error at zero noise is the model error and hence can be corrected systematically; however, the increasing errors at higher noise levels will introduce relative contrast error in the output image.

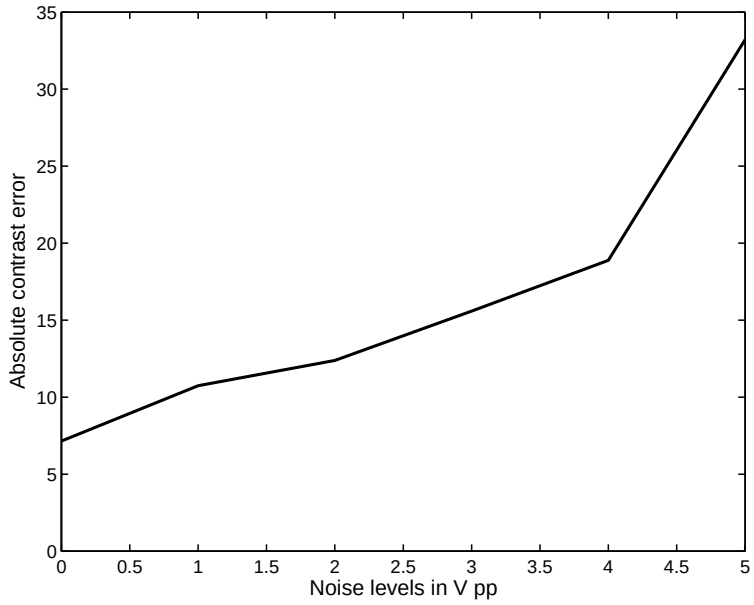

Figure 7.4: The highest contrast error expressed as % of the photocurrent, when applying the photocurrent extraction procedure on simulated data with Gaussian noise

7.5 Experimental results of FPN correction

To test the validity of the proposed FPN correction procedure, the small array was stimulated with uniform images generated electronically using the calibration current source. On these images, double sampling was performed in the linear region, offset and gain correction in logarithmic region and iterative extraction was used in the transition region. To reduce the temporal noise, the data from 20 frames was averaged to reduce the final error below 2% of the photocurrent in the logarithmic region.

The residual fixed pattern noise has been shown in Figure 7.5 as the relative contrast threshold of the imager at various currents. It may be observed that the shape of the error curve in logarithmic region is similar to the one reported earlier for logarithmic pixels (Section 4.4). The residual noise in the linear region is also below the required contrast limits. Thus from these results, it is evident that good quality images with relative contrast threshold of less than 2% could be produced in either region of operation in a LLCMOS sensor. The residual noise in the

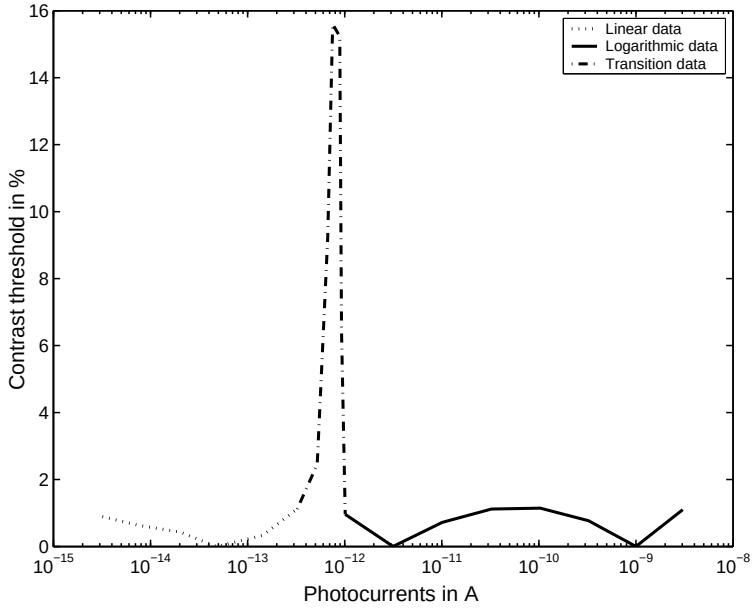

Figure 7.5: Residual fixed pattern noise expressed as relative contrast threshold after the FPN correction strategy

transition region is high. To test if the high errors are indeed due to high temporal noise, the data in the transition region from one of the chips was averaged over 80 frames and the correction procedure was applied. The residual contrast threshold obtained was observed to be below 2%. Clearly, low FPN can be produced even in transition region; however, requirement of large number of frames means that this is an impractical technique for most commercial applications.

7.6 Discussion

Having characterised the performance of the LLCMOS pixel, it is worth reflecting on the advantages and the disadvantages of this pixel. Having a linear response for low currents, LLCMOS pixel performs better than the logCMOS pixel, in low light regions. In particular, a higher gain is achieved, thereby making the low light areas, which suffered the lowest gain in the logCMOS pixel, regions of highest gain. The dynamic performance of the logarithmic pixel is also improved, removing any illumination-dependent transition fixed pattern noise. All these improvements are gained at the only additional signal expense of one extra DC signal.

However, these gains are achieved with at least two costs. First, the presence of linear data means it will have to be compressed at a later stage to reduce the number of bits required to represent the image, thereby requiring additional processing steps. This nullifies one of the advantages of logCMOS pixel described in the first chapter. Second, the smooth but quick transition from linear to logarithmic region means that the pixel has a complex response in this transition. The worst case transition region extends to about half a decade, which is a small fraction on the logarithmic scale. However, it should be noted that this is the high end of the linear region of operation and hence represents a large area on the linear scale. Further, this area is in the central range of illumination and hence would lead to high perception errors in these regions.

Complex equations have been derived to model this region and iterative schemes have been proposed which are able to extract the photocurrent within 10 iterations. However, for a megapixel camera operating in the worst case scenario of all pixels in the transition region, this would mean 10 million calculations per frame which has both large space as well large time complexities. Absence of complex computations had been an important factor favouring the use of logCMOS pixel to capture wide dynamic range. However, LLCMOS pixels lose even this advantage. To have simpler post-processing, one may revert back to the two-expression model of the pixel and accept the high level of error in the transition region. However, this would mean poor image quality in the mid-intensity regions of an image. This would generally be unacceptable for most applications.

The noise performance of LLCMOS pixel reported in this chapter is far from satisfactory. A low noise measurement assembly and an on-chip ADC could have reduced this noise significantly and hence any future large array of these pixels should include these. However, considering the pros and cons of extensive post-processing required, large scale usage of these pixels seems difficult. Any manufacturer should consider these issues before committing to design cameras with these pixels.

Chapter 8

Conclusions and Future Work

We shall not cease from exploration
And the end of all our exploring
Will be to arrive where we started
And know the place for the first time.
T.S. Eliot

This chapter is devoted to summarising this thesis and presenting ideas for possible future research. The first section provides an overview of the results already presented divided in three broad subsections. The first subsection revisits the problem of fixed pattern noise in logarithmic pixels, summarising the results and conclusions from the first four chapters. The second subsection summarises the thesis findings regarding means to reduce the dark current in logarithmic pixels, and hence is related to chapter 5. The final subsection is devoted to the wide dynamic range pixels with linear response to low light and logarithmic response to bright light scenes.

The rest of this chapter presents some ideas for future work. These include an outline of possible research on circuit improvements, solutions to the problems related to the storage of the high dynamic range data and means for displaying high dynamic range data. Possibilities for and hypotheses regarding some psychophysical studies on fixed pattern noise are also proposed.

8.1 Results and Conclusions

This thesis presented ways to improve the performance of wide dynamic range image sensors. The linear sensors currently popular in the market are unable to capture the wide dynamic range available in nature and hence are not able to produce images as would have appeared to the human visual system.

A review of the two major technologies used to manufacture digital image sensors, CCD and CMOS suggests that CMOS technology is fast becoming the technology of choice. Among other benefits, this technology offers low cost manufacturing, the ability to integrate with other circuits, thereby reducing cost and increasing speed. Further, the ability to modify the pixel has given rise to several options for capturing the wide dynamic range in scenes. Among these wide dynamic range imaging circuits, the logarithmic compression is closest to the natural visual systems. In addition, this approach also requires smaller number of storage bits as well as less post-processing compared to other systems. The easiest way to generate logarithmic output is to use a MOS device in weak inversion. However, these pixels are crippled by high fixed pattern noise, high dark current and poor transient response.

8.1.1 Fixed pattern noise in logarithmic circuits

An important requirement from a digital image sensor is to have high spatial resolution at minimum cost. Thus, smaller pixels are preferred. Further, to maximise the amount of light captured, the photosensitive area of each pixel is maximised. This means that small geometry devices are used for the non-photosensitive part of the pixel needed to readout the pixel response. Small geometry devices are susceptible to mismatch, which causes variations in the responses of the pixels. In a typical scene, this response variation appears as ‘salt and pepper’ granular noise at fixed position in the pixel array; and hence the noise is referred to as fixed pattern noise. A major part of this thesis was devoted to the reduction of the effect of this noise on the images produced by the logarithmic sensors.

Due to the small devices being used, every pixel array suffers from fixed pattern noise.

Various techniques have been proposed to reduce this noise. However, it is difficult to compare them due to different units of residual noise used by different researchers. Hence, a standard measure of the residual FPN was required. Contrast threshold defined as the minimum contrast which could be differentiated by the imager was suggested to be an ideal performance measure for the FPN in image sensors. This measure also allows comparison with the human visual system which is known to encode the contrast of an image.

Using contrast threshold as a measure for FPN in logarithmic pixels, mathematical analysis of the techniques proposed in literature has been performed. This analysis suggests that due to high gain variations in the pixel response, these techniques will fail to produce good quality images matching the performance of the human eye over high dynamic range. Hence gain variations and/or its ratio to pixel gain should be reduced for these techniques to be useful. Further analysis suggests that readout circuits could be a source of gain variations. Conventional pixels use the source follower as the readout circuit. Experiments with a small array of these circuits show that the ratio of gain variation to the gain is too high to produce good quality images. Hence, to increase the gain and/or reduce the gain variation, an alternative higher gain differential amplifier readout circuit was tested. The experiments with this circuit confirmed the higher gain from these readouts. However, the gain variations recorded from these circuits was similar to that of the conventional source follower circuit. The ratio of the gain variation to the gain also did not improve sufficiently so as to produce good quality image with the techniques suggested in literature.

This means that both the multiplicative as well as additive fixed pattern noise needs to be corrected if one has to produce images with contrast abilities matching that of the human eye over high dynamic range. An electronic calibration scheme capable of performing this correction, in a simple yet effective fashion, was proposed and verified experimentally. This scheme feeds two calibration currents to every pixel and computes the offset and gain of every pixel. These values are then used to correct the response of each pixel. Residual errors less than the contrast limits of human eye over 6 decades of input intensity change, were obtained from a two-dimensional array of logarithmic pixels, when using this new calibration technique.

8.1.2 Dark current reduction in logarithmic pixels

Having solved the problem of high fixed pattern noise in logarithmic sensors, it was observed that typical CMOS processes suffer from relatively higher dark currents. This limits the lowest intensity which can be captured by the image sensors manufactured in these technologies. In addition to this limit, the sensitivity of the logarithmic pixel was also observed to reduce in the low light areas of a scene due to this current. Further, the electronic calibration technique proposed earlier produces high residual FPN in low intensity regions of the scene due to high dark currents.

A detailed study of this dark current was undertaken in the Chapter 5. The sources of the high leakage current in a typical CMOS process were first identified. The ideal approach to reduce the leakage current would be to modify the manufacturing process. Several means to achieve this goal have been proposed in literature. However, any process modification is costly and increases the cost of the end-image sensor produced, thereby diminishing one of the major advantages of the CMOS process over CCDs.

Hence, circuit as well as layout techniques to reduce the effect of leakage current were investigated. It was observed in the current-voltage relationship of a diode that if the diode is biased at zero potential, the current flowing through the diode is purely of optical origin thereby removing any leakage current. A double current circuit with the promise of biasing the diode at zero volts was tested. However, owing to the restriction of using small devices in the pixel, this circuit failed to meet its goal.

A new layout of the logCMOS pixel was then proposed, which uses a polysilicon guard ring around the diode structure to remove any leakage current associated with the interfaces between the active region and the isolation structures. Experiments performed on arrays of these pixels show that the leakage current is reduced significantly. Not only was the averaged leakage current reduced, the worst case leakage current was also significantly reduced. Further, it is also possible to use the layout for linearising the response of logarithmic pixel at low intensities by proper biasing of the signals. The polysilicon guard structure may be used as an active gate with a reset pulse applied to it. This produces a linear response at low light and a logarithmic

response at high light scenes of an image, with a quick yet smooth transition between the two regions.

8.1.3 Pixels with combined linear and logarithmic response

The pixel with linear response at low light and logarithmic response at high light was investigated in detail. It is observed that not only does this pixel improve the low light sensitivity of the logarithmic pixel, it also improves the dynamic response. Considerable interest in this response was observed in the literature.

The complex relationship between the input and output of these pixels, however, poses problems for modelling the pixel response. Various models were investigated and a model based on the physics of the devices in the pixel was found to properly represent every region of operation of the pixel. This model is complex; however, it breaks down into simple expressions for the strict linear and logarithmic region of operation of the pixel. This means that simple parameter extraction routines can be used to extract the parameters of the pixel, despite its complex nature. The model was also extended to include the effect of the readout circuits and moderate inversion regions of the logarithmic load. These models were then verified using simulation as well as experimental results.

Parameter variations were observed in the responses of pixels in an array. The origins of these variations were investigated using the proposed model. Schemes to correct for these variations were proposed based on the FPN correction strategies used in linear and logarithmic pixel. However, the complex transition region response of the pixel means that the only way to correct in this region is to extract the photocurrent from the complex response. An intelligent iterative scheme was proposed to extract these currents within 11 iterations. However, this extraction as well as FPN correction is sensitive to temporal noise. The measured temporal noise from the system was too high to produce good quality images without averaging over a large number of frames.

The photocurrent extraction and the fixed pattern noise correction strategy developed use extensive computation in the transient region to reduce the errors below the contrast limits of the

human eye. In addition, the data from the linear operation of the pixel needs to be compressed to reduce the number of bits required to represent it. This means that even with a low frame rate, at least two of the advantages of the logarithmic pixel of requiring a small amount post-processing and low number of bits are already lost. Hence, this approach of wide dynamic range imaging is no more beneficial than several others cited in the first chapter. This means that these pixels can have only limited success in wide dynamic range imaging, unless the transition region is removed from the response of the pixel.

8.2 Future circuit improvements

Further circuit improvements could be investigated based on the results of this thesis. The first order enhancements would include designs of large arrays of low dark current logarithmic pixels with the capabilities of electronic calibration for standard resolution cameras. These camera chips would also need additional circuits including amplifiers, analogue to digital converters, on-chip clock generators and if possible, on chip memory banks to store pixel parameters. Alternative circuits able to maintain zero potential across the photodiode to completely remove the effect of the dark current in the pixel, could also be investigated.

The principal reason for the failure of the LLCMOS pixel was the unique non-linear response in the transition region. One way to avoid the transition region could be to capture two outputs at different exposure times within the same frame . A high speed column parallel readout similar to the ones proposed by Mase and co-workers may be used for this purpose [19]. The pixel voltage after the longer exposure time may be used for all intensities, which have linear or logarithmic response after this integration time. Hard conservative thresholds may be used to determine the transition region. For the currents leading to the transition region response after this integration time, the pixel output captured after the smaller exposure time may be used. At this time, the pixel output for these currents will correspond to linear region of operation of the pixel. This scheme has been shown in Figure 8.1. In this figure, the integration time for the frame is between $t1$ and $t3$. For currents I_1 and I_3, the pixel output is in linear and logarithmic

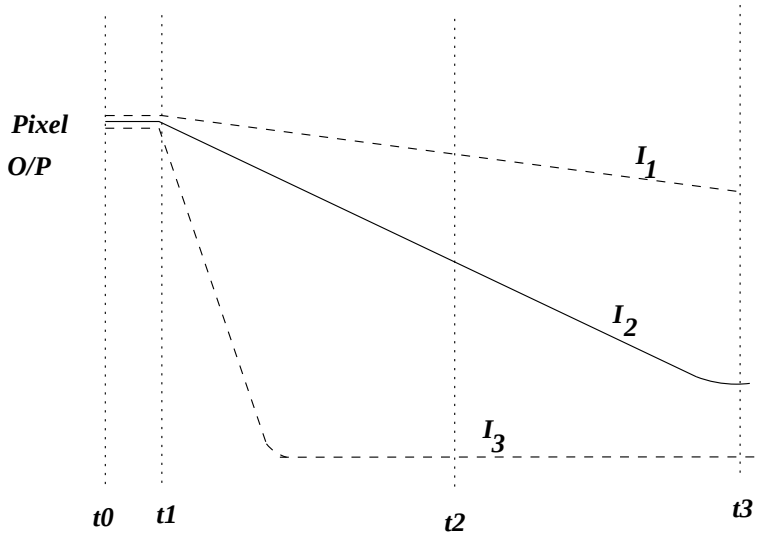

Figure 8.1: A scheme to remove the complex transition region of LLCMOS pixel by measuring two pixel output at two exposure times in a single frame. $t3$-$t1$ could be integral multiple of $t2$-$t1$

region and hence the output is used as a measure of the photocurrent. However, the pixel is in transition region at the end of the integration time. To remove the transition region effect, the pixel output is also measured during the integration period at a time $t2$. This output is used a measure for the photocurrent I_2. The frame time could be selected as an integral multiple of the smaller exposure time thereby having a simpler merging procedure for the output from sensor. The data from these measurement schemes will lead to a simple relationship between the input photocurrent and the output voltage using a linear and a logarithmic expression. The fixed pattern noise correction strategy would be much simpler for these data-sets.

Despite the additional exposure time signal used to remove the transition region, the logarithmic region response of the pixel will still suffer from high temporal noise. An important result of the studies of LLCMOS pixels is that the high gain logarithmic pixels would provide enhanced signal to noise ratios and hence have better chance of market popularity. With the standard logarithmic pixel, the only way to increase the gain is to have multiple logarithmic loads [116]. However, this comes at the cost of fill factor. In addition, temporal noise continues to affect the performance of logarithmic pixels and the pixel still suffers from poor dynamic performance. Hence, other approaches to obtain logarithmic response while enhancing the signal to temporal noise ratio and improving the transient effects should be investigated.

One approach could be to utilise an active pixel sensor to produce logarithmic output. This is possible if optical charge integration in the pixel is stopped at an instance when the integrated charge is logarithmic related to the input photocurrent. To better understand this, let us observe

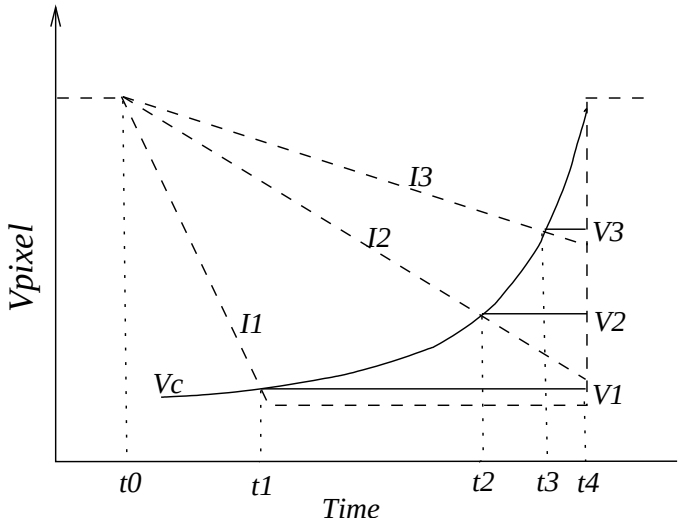

Figure 8.2: Signal flow in an integrating pixel with logarithmic output.

the signal diagram in Figure 8.2. The dashed lines show the integration of three different photocurrents in a typical active pixel sensor. The output during the integration may be compared to another signal V_c, and the integration may be stopped when the two signals are equal. This means for the high current, I_1, the integration will stop at lower voltage V_1 than the voltages for lower currents I_2 and I_3. The pixel output after the integration frame will thus depend on the V_c signal. This signal can be generated in such a way that pixel output is related to the logarithm of the photocurrent.

One circuit which is capable of producing this output is shown in Figure 8.3. In this figure, a pMOS switch is used to disconnect the integrating photodiode from the readout node. Use of a comparator, however will reduce the fill factor and introduce additional sources of fixed pattern noise. An alternative approach could be to use a pMOS transistor as a simple comparator as well as a disconnecting switch. A simple circuit having this arrangement is shown in Figure 8.4. The voltage on integration node, $N1$ will decrease with the integration of the photogenerated charge. The comparing voltage, V_c is initially smaller compared to the integrating voltage and hence the pMOS switch $M4$ is switched on, transferring the integrating voltage to the gate of the readout

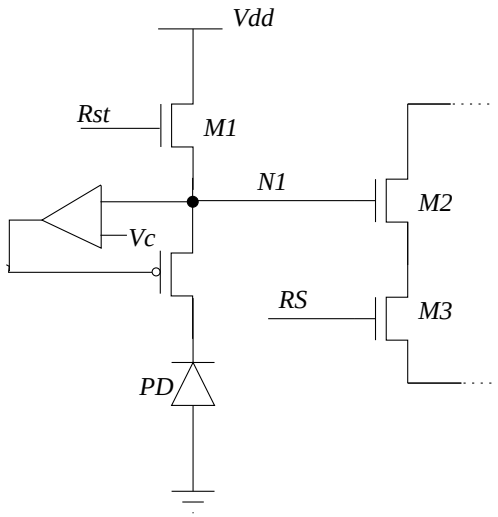

Figure 8.3: An integrating pixel capable of producing logarithmic output

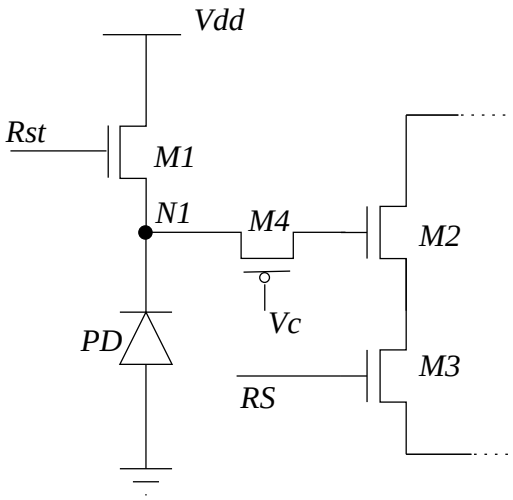

Figure 8.4: 4-transistor integrating pixel capable of producing logarithmic output

transistor. However, when the integrating voltage is higher than the V_c by the threshold voltage of device $M4$, this device will switch off. After this instance, integrating voltage continues to fall while V_c continues to rise. The pMOS switch will hence continue to be switched off. Thus, the voltage at the gate of readout transistor will become dependent on V_c, which in turn can be used to ensure that the output is logarithmically related to the input.

These descriptions have been limited to the production of logarithmic output signal from these pixels. However, it may be observed that the signal, V_c can be chosen to produce virtually any monotonic relationship between the input photocurrent and the output signal. A logarithmic

signal would be the preferred choice due to the minimum number of bits required to produce images matching the contrast threshold of the human eye. Another advantage of these pixels is that the pixel dynamic range can be arbitrarily enhanced or reduced by the external signal.

This idea needs to be developed further. In particular, analysis and experiments similar to that carried out for logarithmic and linear-logarithmic pixels in this thesis should be performed. The external comparing signal, V_c needs to be either derived mathematically or generated through software. The later approach can utilise an external memory bank, thereby reducing the amount of calculation required. Fixed pattern noise is expected to affect these pixels as well. Hence, a detailed analysis of the sources of the FPN should be carried out leading to derivation of a practical FPN correction procedure.

8.3 Post-processing of the logarithmic data

Having obtained logarithmic data either from logCMOS or LLCMOS or the new pixel, several blocks of the imaging systems need to be investigated. This thesis has been primarily involved with data being captured from the pixels. This data needs to be processed before it can be used meaningfully by the end user. This processing may involve compression to reduce the size of the image, colour processing and various filtering operations to enhance or reduce certain aspects of the image. These image processing algorithms have been widely studied [133]. However, their primary focus has been on linearly captured low dynamic range data. These algorithms need to be investigated for their effects as well as changes needed for operating upon wide dynamic range logarithmic data. The immediate concerns, however, are to devise an ideal file format and ways to produce the high dynamic range data on standard displays.

8.3.1 File encoding formats

The first area of research for any image processing algorithm would be to investigate the file format needed to store these wide dynamic range images. Several file formats suggested in literature to store the wide dynamic range images. These can be grouped under two broad

approaches. In the first of these, camera manufacturers store the image information in raw format [134, 135]. Archiving the data in raw file format gives the freedom of applying any signal processing on the image including any demosaicing algorithm, any colour space, white balance, etc. However, the raw files tend to be two to three times bigger than other formats. These formats include .cr2 and .crw by Canon, .nef by Nikon, .mrw by Minolt, .raf by Fuji, .pef by Pentax, .orf by Olympus, .3fr by Hasselblad and .x3f by Foveon [135, 136]. Most of these are based on variations of the hyper-extensible TIFF. Further, they are officially undocumented, proprietary and subject to change with each new camera model. Additional software and/or plugins to known image processing software are provided by these manufacturers to handle these raw files. Storing the information in raw format ensures no loss of data. However, raw file formats have not yet been standardised, thereby leading to different software for different cameras. Further, use of proprietary formats also poses of the danger of not having long time support. Adobe™has introduced a non-proprietary Digital negative (DNG) format to archive raw data from a camera [137]. DNG is an extension of TIFF (Tagged Image File Format) 6.0 and is compatible with TIFF-EP (TIFF for Electronic Photography) standard. DNG is supported by Adobe™Photoshop™and can be read by a variety of other software. Camera manufacturer support however, is fairly limited at this time.

Some standards for storing high dynamic range data have been produced by the image processing community, in particular the motion pictures community. One of the first standards was TIFF based log encoding developed by Pixar [138]. By using 11 bit encoding for every colour channel, this scheme was able to encode roughly 3.8 orders of magnitude.

Kodak developed the Cineon file format for the digital intermediate film production [139]. An interesting aspect of this file format was that the data was stored in negative format. The society for motion pictures and television engineers (SMPTE) standardized the format further into a related format called Digital Picture eXchange (DPX) which can store more varieties of image information as well as additional header information [140]. DPX uses a 10 bit log format to store the density of each colour channel. Though Cineon and DPX are not essential HDR image formats, they may be utilised to store high dynamic range images.

Industrial Light and Magic have also introduced yet another format, OpenEXR, for representing extended dynamic range [141]. OpenEXR is an open standard released under free software license. It uses 16-bits per channel half precision floating point values with a sign bit, five bits of exponent, and a ten-bit mantissa. Ward and co-workers have proposed two other file formats, SGI TIFF LogLuv [142] and Radiance RGBE [143] for storing the HDR images. RGBE uses 4-byte to store the mantissa for three colour channels and a universal exponent component. LogLuv format is more perception oriented and is based on the CIE space [138]. Yet another encoding scheme has been produced by Microsoft and HP and has been standardised as an IEC standard [144]. The format is referred as sRGB and offers 48-bit as well as a compact 36 bit standard. The two standards utilise 12 bit or 9bit colour encoding with encoding of gamma.

Hence, the battle for the ideal file format for high dynamic range data is far from over. The raw formats have been developed considering the camera hardware. Similar approaches may be pursued with the logarithmic cameras. However, it is worth noting that several of the standard file formats compute the logarithm of the camera output. With the logarithmic pixels, this function is available without any additional computation. It would be interesting to investigate whether this makes the process of converting raw data to the standard form a simple process.

8.3.2 Display of wide dynamic range images

Another area of research is the question of how to display the wide dynamic range data captured from these imagers. The standard displays used for images including paper and computer screens (both CRT as well as LCD) are capable of displaying only a small dynamic range. This means that even if a good quality image is captured, it can not be rendered on standard displays. Special purpose displays like Bright side's DR-37P with capacity to display data with high contrast change are available in the market [145, 146]. However, their high cost and high power consumption forms a large barrier to commercial success, especially in portable devices.

Algorithmic approaches to display high dynamic range images in low dynamic range displays have been highly active areas of research [5, 147]. Various methods of converting HDR images into a viewable format have been developed, generally called tone mapping. Several

approaches including simple intensity cutoffs, histogram equalisation and perception based encoding have been attempted. Otim and Collins have adapted tone mapping algorithms for images produced by logarithmic cameras [148]. The ideal way to render these images, however, is still an open question. One interesting aspect of tone mapping algorithms is that they convert their input to its logarithm. The logarithmic pixels hence should be able to perform tone mapping with less computation than their linear counterpart. This hypothesis needs to be further investigated. Further, on-chip tone mapping, either in digital or in analogue domain would also form an interesting research exercise.

8.4 Psychophysical studies

It has been observed in this as well as several other works, that fixed pattern noise affects all artificial image sensors. An interesting question to ask at this juncture is whether there is fixed pattern noise in natural image sensors and if so, how is it compensated for. An experimental investigation will require single cell recording from a large population of rods and cones simultaneously under uniform illumination, while is susceptible to large temporal noise. To the best knowledge of the author, no such measurements have been reported. However, considering the small sizes of photodetector in human eye (much smaller than typical digital detectors), there is a high probability of FPN. The FPN profile in eyes, however, should be different than that of digital cameras. The photoreceptor arrangement in eyes is generally radial with each pixel providing parallel readout, unlike cameras where it is not possible owing to limited bandwidth and hence detectors are arranged in x-y pattern with serial readout. Thus columnar FPN experienced in cameras may be replaced by radial or concentric noise in eyes. Further, if this hypothesis is true, there should be a mechanism for correction of FPN in natural visual systems. There has been some studies, which have shown that the colour perception is independent of number of colour photoreceptors [149], pointing towards a correction mechanism.

8.4.1 Probable correction mechanisms

Extending the current approaches used in artificial image sensors, one can speculate on systematic and/or algorithmic correction mechanisms for FPN. The systematic correction may consist of neural adaptation and/or difference encoding. The neural networks associated with the visual system develop with the eye and hence may adapt themselves to the variability in the photo-detectors. Further, one way to describe the eye is as a difference encoder between two scenes. FPN due to photo-detector's variability may be described as a constant image produced in front of the eye and hence the visual system may subtract it from every scene it captures.

Another strategy for FPN correction could be algorithmic correction either through calibration during post-processing and/or filtering. The visual areas in the brain may calibrate for the variations in the photo-receptors in the eye and remove FPN in a way similar to logarithmic cameras. This may require one or more reference frames for providing training to networks. One source of these reference frames could be our blinking operation or sleep. Median filtering on the whole image is a complex mathematical operation; however, the visual system operates parallely and hence may be able to perform efficient median filtering. The eye can be modelled as a spatio-temporal filter with local adaptation. Hence one way to correct for offset and gain variations could be this unique spatio-temporal filter. Yet another aspect of FPN correction could be motion based. Techniques have been proposed to correct the FPN using relative motion between a series of images [125]. The human eye could use motion between images to compensate for any pixel variations.

8.4.2 Contrast loss

It has been shown earlier that fixed pattern noise essentially degrades the contrast discriminating abilities of an image capturing device. Hence, another hypothesis can be made that one source of contrast loss in human or other natural visual system is high residual fixed pattern noise on account of failure of the involved correction mechanism. Contrast loss in natural visual systems is a well studied phenomenon, with several attributed sources including diseases (for example

Parkinson's disease [150], amblyopia [151], multiple sclerosis [152]), surgical procedure [153], influence of drugs/alcohol [154] and ageing [155]. Thus, if the first hypothesis is true, one source of these losses could be attributed to the failure of FPN correction mechanism. It can also be reverse argued that since there are known cases of contrast loss, there is uncorrected FPN in the visual system, thereby proving the first hypothesis. Verification of both these hypotheses requires further experiments with animal retina.

8.5 Concluding remarks

This thesis explored ways towards improving the performance of wide dynamic range logarithmic sensors manufactured in CMOS process. The fixed pattern noise in these sensors was extensively examined and a simple and yet highly effective correction procedure was evolved. The dark current in these sensors was also limited by use of different layout strategy. The low light performance of these sensors was further improved by linearising the low light response of the sensor. A new model for the response was derived and the model was used for characterising the pixel. A strategy for reducing the FPN in these sensors was also devised.

The work presented in this thesis can be extended to further improve the performance of logarithmic sensors. Two possible modifications have been suggested. In the first, the complex transition region of the LLCMOS pixel is removed leading to simple input-output relationship. In the second, a new pixel design is suggested which improves the gain of the logarithmic pixel. The logarithmic data captured by these imagers need further processing including processing for display and colour reproduction. A standard file format, hence, needs to be devised for these sensors. The logarithmic nature of current standards for high dynamic range data may be utilised towards this effect. The logarithmic nature of the output from these pixels may also assist in tone mapping algorithms to display these images. Hypothesis regarding the presence and correction of fixed pattern noise in natural visual systems are also presented asking new questions in our understanding of animal retina and hence require further investigation.

Appendix A

Test Chips

My tools are but common ones,
Simple shepherds all
My tools are no sight to see:
A little hempen string, and a post whereon to swing,
Are implements enough for me!
Thomas Hardy

A.1 Isis

Various results shown in this report are based on experiments carried out on two chips namely Isis and Cherwell. Isis was manufactured in 0.35μ 3-metal, 2-poly CMOS CSI process from Austrian Micro Systems. The simulations and design was performed using Cadence tool-set. The chip primarily consists of 6 regions. A symbolic diagram of the chip is shown in figure A.1.

The Smaller Arrays

The chip contains 4 small arrays of 100$\times$10 pixels. Each of these arrays has its individual row scanner. However, no column scanner is provided and hence ten output lines are available from these arrays. The first row as well as the first column is darkened by a metal layer on top of the array. The pixel dimension in each array was 10 μ x 10 μ. However, different arrays

have different types of pixels. The first two arrays have conventional logarithmic pixels with different readout circuits. One of the arrays uses the conventional source follower circuit while the second has the higher gain differential amplifier readout circuits. The results from these arrays have been presented in chapter 3. The third array contains the double current mirror pixel to control the leakage current in the pixel. The readout circuit used is of differential amplifier type. The results from this array are presented in chapter 5. The last array contains electronically calibratable pixel with differential amplifier readout circuits. The column circuit of this array also contains calibration current sources. These have been explained in chapter 4.

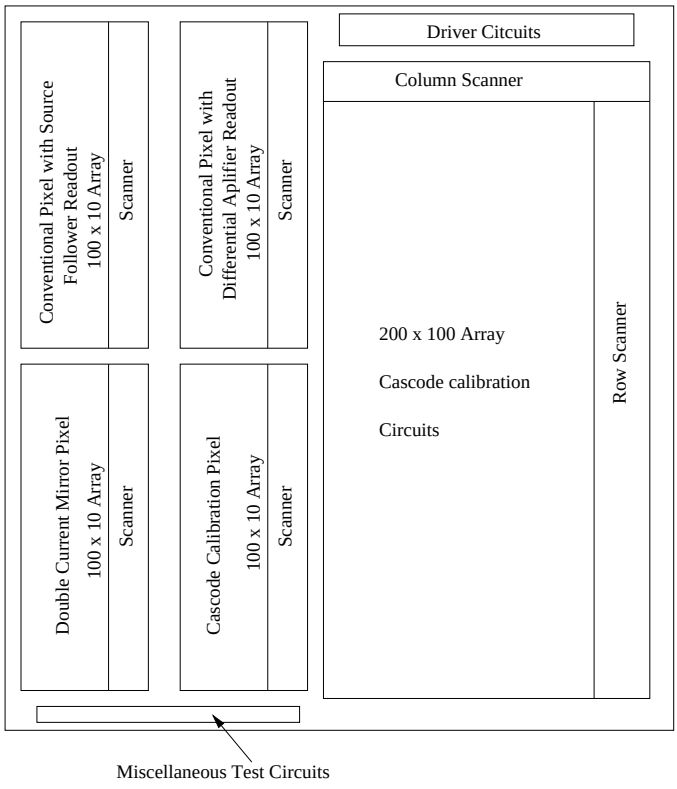

Figure A.1: Representative schematic of the test chip - Isis. There are 4 small arrays, one large array, test pixels and large photodiodes on the chip.

The Large Array

About half of the chip contains a large array of 200 x 100 electronically calibratable pixels, described in chapter 4. The readout circuits used are of differential amplifier type. This array has a row scanner as well as a column scanner, thereby providing access to every pixel using

Technology	0.35 μm 2-poly 3-metal CMOS
Chip size	3.3 $\times$ 3.3 mm^2
Pixel Size	10 $\times$10 μm^2
Larger Array	
Resolution	200 $\times$100
Pixel Type	Cascoded with Calibration Source
Readout	Differential Amplifier
Fill Factor	49$\%$
Smaller Array No 1	
Resolution	10 $\times$100
Pixel Type	Conventional
Readout	Source Follower
Fill Factor	58 $\%$
Smaller Array No 2	
Resolution	10 $\times$100
Pixel Type	Conventional
Readout	Differential Amplifier
Fill Factor	58 $\%$
Smaller Array No 3	
Resolution	10 $\times$100
Pixel Type	Cascoded with Calibration Source
Readout	Differential Amplifier
Fill Factor	49 $\%$
Smaller Array No 4	
Resolution	10 $\times$100
Pixel Type	Double Current Mirror Pixel
Readout	Differential Amplifier
Fill Factor	30 $\%$

Table A.1: Chip summary - Isis.

single output line. The column circuit of the array contains another stage of differential amplifier readout circuits along with the calibration current sources. In addition, an external reference pixel has also been designed with the array. The calibration source can be selectively connected to this pixel to approximate their variations.

Miscellaneous Circuits

In addition to the arrays, smaller test circuits have also been included on this chip. These include two pixels of all the four types used in the smaller arrays. These pixels can be directly read-out of the chip. One of these pixels has been covered with a metal layer. In addition, two large

photodiodes each of dimension 100 x 100 μ have also been manufactured on the chip. One of these has been shielded by metal layers. These photodiodes provide an on-chip light meter. Finally, for primary testing purposes, single nMOS and pMOS devices with sorted gates were also manufactured on the chip.

A.2 Cherwell

The second chip, Cherwell, was manufactured in 0.35μ 4-metal, 2-poly CMOS C35 process from Austrian Micro Systems. The change of process was necessitated due to unavailability of the previous process. This chip was result of several projects and hence contained circuits designed by various researchers. About a quarter of the chip contained circuits reported in this thesis. These image-sensing parts of the chip contain three small arrays of 100$\times$10 pixels, as shown in Figure A.2. The last array on the chip contained conventional logarithmic pixels with source follower pixels. The second array contained logarithmic pixels, wherein the photodiode was surrounded by a polysilicon guard ring structure. These pixels also utilised source follower readout circuits. The results from these pixels have been presented in chapter 5. The third arrays had pixels with combined linear and logarithmic response with simple layout and conventional source follower readout circuits. The results corresponding to these pixels have been presented in chapter 6 and 7. Scanners were manufactured in the chip to access individual pixels. However, unlike the previous chip, the same scanner was used for all arrays. Similar to Isis, a large photodiode was also manufactured to act as an on-chip light meter. Single pixel circuits of the three types were also manufactured for characterisation. Single transistors were also manufactured for primary testing of the chip. The non-photosensitive parts of the chips were covered by two of the top layer metals provided in the technology.

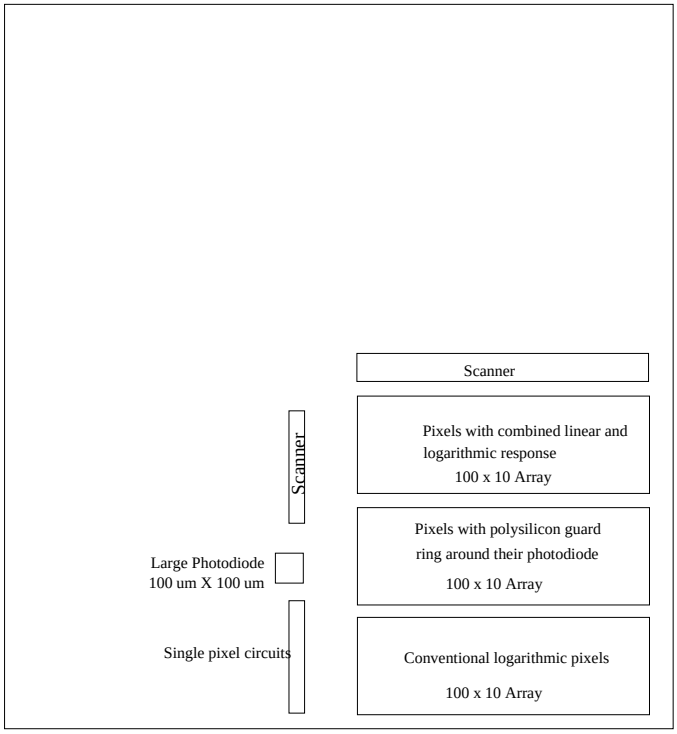

Figure A.2: Representative schematic of the test chip - Cherwell. Only a quarter of chip area is used for pixel circuits. There are three pixel array with scanners. Single pixels and large photodiode are also manufactured.

Technology	0.35 μm 2-poly 4-metal CMOS
Chip size	3.3 $\times$ 3.3 mm^2
Pixel Size	10 $\times$10 μm^2
Smaller Array No 1	
Resolution	10 $\times$100
Pixel Type	Linear - logarithmic response pixel
Readout	Source Follower
Fill Factor	44 $\%$
Smaller Array No 2	
Resolution	10 $\times$100
Pixel Type	Guarded photodiode pixel
Readout	Source Follower
Fill Factor	40 $\%$
Smaller Array No 3	
Resolution	10 $\times$100
Pixel Type	Conventional logarithmic
Readout	Source Follower
Fill Factor	40 $\%$

Table A.2: Chip summary - Cherwell

Appendix B

Publications from the Thesis

And listen why; for I will tell you now
What never yet was heard in tale or song,
From old or modern bard, in hall or bower.
John Milton

Chapters 3 and 4

- *"An electronic calibration scheme for logarithmic CMOS image sensors"*, IEEE Sensors Journal, Volume 6:4, pages: 950- 956, August 2006. with S. Ayoama, S. Otim, D. Joseph and S. Collins.
- *"Model based fixed pattern noise correction for high dynamic range logarithmic CMOS imagers"* accepted for publication in the IEEE Transactions on Instrumentation and Measurement, with S. Otim, D. Joseph and S. Collins.
- *"Simplified fixed pattern noise correction scheme for logarithmic pixels"*, In Proceedings of the IEEE workshop on CCDs and Advanced Image Sensors, Kobe, Japan, May 2005, with S. Otim, D. Joseph and S. Collins.
- *"A 200X100 array of electronically calibratable logarithmic CMOS pixels"*, In Proceedings of the Biennial Analogue Signal Processing Conference, Oxford, November 2004. With S. Ayoama, S. Otim, D. Joseph and S. Collins.
- *"An electronic calibration scheme for logarithmic CMOS pixels"*, In Proceedings of the IEEE International Symposium on Circuits and Systems, Vancouver, Canada, June 2004, with S. Ayoama, S. Otim, D. Joseph and S. Collins
- *"Modelling of high dynamic range logarithmic CMOS image sensors"* In Proceedings of the IEEE Instrumentation and Measurement Technology Conference, Como, Italy, May 2004. With S. Otim, D. Joseph and S. Collins.

Chapter 5

- *"Wide dynamic range CMOS pixels with reduced dark current"*, Accepted for publication in Journal of Analog Integrated Circuits and Signal Processing, with S. Collins.
- *"On dark current reduction techniques in logarithmic image sensors"*, In Proceedings of International Congress of Imaging Science, Rochester, USA, June, 2006, with S. Collins.
- *"Low dark current logarithmic pixels"*, In Proceedings of the 47th IEEE International Midwest Conference on Circuits and Systems, Cincinnati, August, 2005, with S. Collins. **Myril B. Reed award for the best paper**.

Chapter 6

- *"Models for pixels with wide dynamic range combined linear and logarithmic response"*, To appear in IEEE Sensors Journal, June, 2007, with S. Collins.

Chapter 7

- *"Fixed pattern noise correction in wide dynamic range pixels"*, To be presented at the 50th IEEE International Midwest Conference on Circuits and Systems, Montreal, August, 2007. with S. Collins.
- *"FPN correction in CMOS pixels with WDR combined linear and logarithmic response"*, In Proceedings of the Biennial Analogue Signal Processing Conference, Oxford, November 2006. with S. Collins.
- *"Fixed pattern noise in image sensors with combined linear and logarithmic response"*, In Proceedings of International Congress of Imaging Science, Rochester, USA, June, 2006, with S. Collins.

Chapter 8

- *"A Novel Wide Dynamic Range CMOS Image Sensor with Adjustable Logarithmic Photo-Response"*, Invited paper to appear in Mediterranean Journal of Electronics and Communications. with H.Y. Cheng and S. Collins.
- *"A Novel Wide Dynamic Range CMOS Image Sensor with Adjustable Logarithmic Photo-Response"*, In Proceedings of the Biennial Analogue Signal Processing Conference, Oxford, November 2006. with H.Y. Cheng and S. Collins.
- *"Fixed pattern noise in natural visual systems - A Possible Cause for Contrast Loss "*, Perception, Volume: 35(supplement), page: 51, 2006; presented at European Conference on Visual Perception, St. Petersburg, August 2006.

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