

# Investigation of IGBT Switching Energy Loss and Peak Overvoltage using Digital Active Gate Drives

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**Abstract**—This paper presents an experimental investigation of the switching energy loss and peak overvoltage occurring in a half-bridge Insulated Gate Bipolar Transistor (IGBT) converter which is switched using an Active Gate Drive. A range of voltage profiles is systematically applied to the IGBT gate and the resulting switching behaviour is measured to obtain the switching energy loss and peak overvoltage for each gate profile. The experimental apparatus which allows different gate waveforms to be tested is described, and the minimum achievable switching loss for a set overvoltage limit is found for turn-on using gate voltage waveforms of increasing complexity. A reduction in turn-on switching energy loss of 24% is achieved with the most sophisticated gate voltage waveform tested compared to a simple voltage ramp waveform. Turn-off overvoltage is controlled when using more complex gate waveforms whereas simpler voltage ramping fails to influence the turn-off voltage overshoot.

## I. INTRODUCTION

Active Gate Drives (AGDs) adapt the voltage or current profile applied to the controlling terminal of a power semiconductor device in order to alter the switching behaviour of the device. This can allow management of the energy dissipation, electromagnetic interference (EMI) generation, and device voltage stress during switching. In the common case of a converter that is hard-switching an inductive load, there is inevitable power dissipation during each switching transition when there is both a voltage across and current through one or more devices [1]. The energy that is dissipated in the power device during switching can be minimised by transitioning from conducting to blocking, or vice-versa, as rapidly as possible in order to minimise the time when power is dissipated. However, the resulting high rate-of-change of current will induce large voltages across the parasitic inductances in the commutation current path. These voltages appear across the active device that is transitioning from conducting to blocking, and therefore the active devices in the converter must be rated to withstand these voltage spikes.

Typically this results in the selection of power devices with breakdown voltage ratings well above the nominal operating voltage of the converter. As the drift region inside each device becomes longer to accommodate the depletion layer at large reverse voltages, the on-state resistance of the device increases, leading to devices with higher voltage ratings having larger conduction energy losses [1]. Devices with lower breakdown voltages (and lower conduction losses) can be used if circuit

overvoltages are reduced by slowing down the switching transitions. This however leads to increased switching losses. AGDs can be used to strike a balance between circuit peak overvoltages and switching energy loss by tailoring the gate signal in order to gain control over the switching behaviour.

Several AGDs have been discussed in the literature. One implementation uses high-bandwidth analogue circuitry to obtain closed-loop control of  $\frac{di_C}{dt}$  and  $\frac{dv_{CE}}{dt}$  during IGBT turn-on and turn-off [2], [3], [4], [5]. A single PI-controller is used for both  $\frac{di_C}{dt}$  and  $\frac{dv_{CE}}{dt}$  control, exploiting the natural separation between  $i_C$  and  $v_{CE}$  slopes during hard-switching. Effective control is demonstrated for switching times in the sub-microsecond range.

However, digital methods are attractive for reasons such as control flexibility, ability to respond to changes in operating conditions, complex device protection features, and ease of combining these features into a single controller [6]. Digital AGDs can produce gate control signals that are generated without measurements of switching behaviour (open-loop control) [7], [8], [9], or control signals can be generated in response to measurements taken at a previous switching edge (pseudo-closed-loop or iterative control) [6], [10], [11], [12]. True closed-loop control, where the instantaneous device behaviour is fed back into the control signal, is a challenge for digital AGDs because the latencies introduced by off-the-shelf analogue to digital converters (ADCs), processing hardware (FPGAs or DSPs), and digital to analogue converters (DACs), add up to create control loop delays that are unacceptably long for maintaining control during the sub-100 ns switching transients [10].

Digital hardware is now fast enough to realize some of the significant benefits of the open-loop and iterative control approaches, however, as demonstrated in [7] for fast-switching Gallium Nitride (GaN) Field Effect Transistors (FETs) using gate drive profiles generated ‘offline’. An array of pull-up and pull-down MOSFETs are switched on and off in the driver according to a predetermined profile, allowing the current supplied to the FET gate to be controlled. Reductions in switching-generated EMI are demonstrated for sub-20 ns switching transitions.

The full potential of this hardware can be realized when it is combined with a means to adapt the gate signal based on measurements of device behaviour. In [10], the energy loss

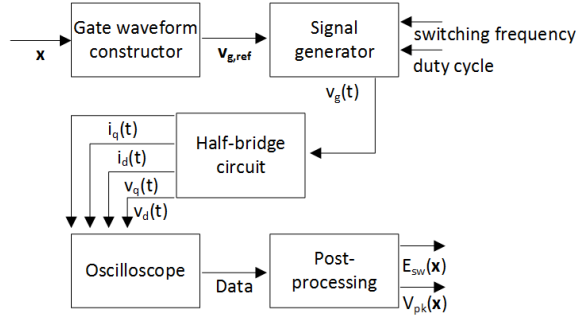


Fig. 1. Block diagram illustrating experimental process from gate waveform parameters  $\mathbf{x}$  to switching energy loss  $E_{sw}$  and peak circuit overvoltage  $V_{pk}$ .

and peak overvoltage information from a previous switching edge for sub-microsecond switching of an IGBT is used as the input to an optimisation procedure to generate the gate drive profile for the next switching edge. Device  $v_{CE}$  limits are respected during switching for varying load currents while minimising switching energy losses.

In [6], a programmable current source drives an IGBT, and a state machine implemented on an FPGA divides the switching transition into stages by comparing measurements of collector-emitter and gate-emitter voltage ( $V_{ce}$  and  $V_{ge}$ ) and collector current ( $I_c$ ) against set threshold values. A gate current is applied which is constant during each stage, but which can be modified between each switching transition to control  $\frac{di_c}{dt}$  during turn-on and  $\frac{dv_{ce}}{dt}$  during turn-off.

Peak  $\frac{dv_{ds}}{dt}$  and  $\frac{d^2v_{ds}}{dt^2}$  of MOSFET smart power switches are limited in [11] to achieve s-shaped switching transients, where the transients occur over time ranges of 20 to 200  $\mu\text{s}$ . An iterative learning control algorithm adapts the gate current reference between switching edges.

This paper lays the groundwork for further ‘online’ optimisation of gate waveforms, by demonstrating the effect that an AGD can have on the switching trajectory of an IGBT, showing that there exists an optimum gate waveform that minimises  $E_{sw}$  within a given voltage constraint, and illustrating how the optimum  $E_{sw}$  reduces as the gate waveform complexity increases. This is relevant for gate waveform optimisation as it helps address the issue of how many decision variables are appropriate for describing the gate waveform in an optimisation procedure. Section II outlines the experimental setup used to generate varying gate waveforms and measure the circuit  $E_{sw}$  and  $V_{pk}$  response. Section III illustrates the effect of the gate waveform on switching energy and peak overvoltage and compares gate waveforms of differing complexity. Section IV draws together the findings of the paper.

## II. EXPERIMENTAL METHOD AND EQUIPMENT

The block diagram of Figure 1 provides an overview of the experimental method used to measure the response of a half-bridge converter to varying IGBT gate waveforms. The function of each block is described in this section.

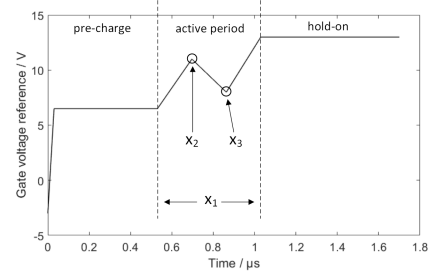


Fig. 2. An example gate reference waveform for turn-on.

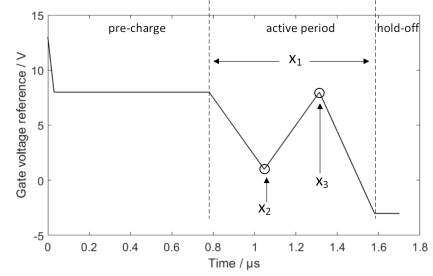


Fig. 3. An example gate reference waveform for turn-off.

### A. Gate waveform constructor

The ‘Gate waveform constructor’ block in Figure 1 creates a sequence of gate reference voltage points,  $\mathbf{v}_{g,ref}$ , based on an input vector  $\mathbf{x}$ . This block runs in MATLAB on a desktop PC. The reference is defined by three time periods, as shown in Figure 2 for turn-on and Figure 3 for turn-off.

First, there is a pre-charge interval of duration  $T_{pre}^{on/off}$  where the gate-emitter voltage is brought to  $V_{pre}^{on/off}$ , just below (for turn-on) or just above (for turn-off) the IGBT threshold voltage of approximately 7 V.

Second, there is an ‘active period’, the duration of which is given by the first element in the input vector, i.e.  $x_1$ . This period is split into  $N$  sections of equal duration, where the voltages at the  $N - 1$  points between the sections are given by the remaining elements in  $\mathbf{x}$ , i.e.  $x_2, x_3, \dots$ . The gate reference voltage between these points is found by linear interpolation. The input vector  $\mathbf{x}$  is therefore of length  $N$ .

Finally, the gate voltage is held at some high  $V_{hold}^{on}$  (for turn-on) or some low  $V_{hold}^{off}$  (for turn-off) to keep the IGBT fully on or off. The values of the parameters with which are fixed (those not in the input  $\mathbf{x}$ ) are listed in Table I. The signal is downsampled to 256 points and is sent from the host PC to the signal generator hardware over USB.

TABLE I  
VALUES OF FIXED GATE WAVEFORM PARAMETERS

Name	$T_{pre}^{on}$	$T_{pre}^{off}$	$V_{pre}^{on}$	$V_{pre}^{off}$	$V_{hold}^{on}$	$V_{hold}^{off}$
Value	0.50 $\mu\text{s}$	0.75 $\mu\text{s}$	6.5 V	9.0 V	15.0 V	-3.0 V

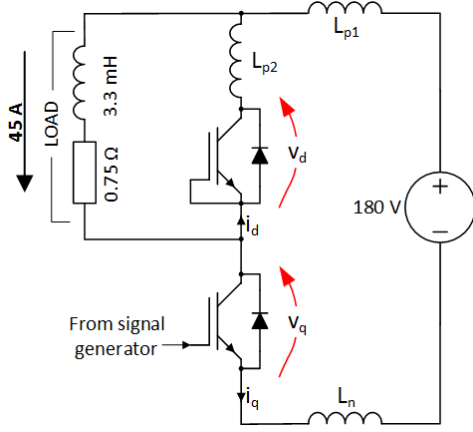


Fig. 4. The half-bridge circuit used to hard-switch a resistive-inductive load

### B. Signal generator

This sub-system converts the sequence of data points from the host PC into a continuous voltage signal that is applied to the power device gate. The data points are stored in RAM on an FPGA. The FPGA determines when it is time for a switching edge, based on a switching frequency  $f_{sw}$  and duty cycle  $d$  set by the host PC. In this paper,  $f_{sw} = 20$  kHz and  $d = 0.2$ . To initiate switching, the FPGA clocks out the sequence of 256 voltage points to a 14 bit DAC at a rate of 100 MSPS. The resulting signal from the DAC has a duration of

$$\frac{256}{100 \cdot 10^6} = 2.56 \mu s. \quad (1)$$

The DAC output current is converted to a voltage by a transimpedance amplifier stage, which holds the output voltage of the DAC within its compliance range. The signal is level-shifted, amplified, and buffered up to a maximum current of 4 A. A split supply of  $V_{ge}^+ = 22$  V and  $V_{ge}^- = -13$  V with respect to the IGBT emitter powers the analogue circuitry, giving  $v_{ge}$  a potential range of  $-11$  V to  $20$  V. The drive signal is applied to the power device gate through a  $1.25 \Omega$  gate resistor. As the gate is capacitive, the actual voltage at the IGBT gate is an RC-filtered version of the drive voltage.

### C. Half-bridge switching leg

Figure 4 is a schematic of the half-bridge circuit used. Hard-switching is created by supplying a  $3.3$  mH and  $0.75 \Omega$  load using a half-bridge switching leg as a buck converter. Power transfer is unidirectional from the  $180$  V d.c. bus to the load. With the load on the high side of the half-bridge, the lower switch is the control device and the upper switch is held off by shorting together the gate and the emitter. The  $1.2$  kV  $300$  A Fuji 2MBI300U4N-120-50 IGBT half-bridge power module is used.  $L_{p1}$ ,  $L_{p2}$ , and  $L_n$  represent parasitic inductances which are the cause of circuit overvoltages during switching.

### D. Data acquisition and control

The FPGA sends a trigger signal to an oscilloscope at the start of outputting a gate waveform of interest. On receiving

this trigger, the oscilloscope captures the following signals at 310 MSPS:

- The collector-emitter voltages of the upper and lower switches,  $v_d$  and  $v_q$  respectively
- The collector currents of the upper and lower switches,  $i_d$  and  $i_q$  respectively
- The gate-emitter voltage of the lower, control, switch,  $v_q$ .

The waveforms are transferred to the desktop PC running MATLAB. The power dissipation of each switch is calculated from the product of the collector-emitter voltage and collector current, and the integral of these powers over time gives the switching energy loss, i.e.

$$E_{sw} = \int_{t_1}^{t_2} [v_q i_q + v_d i_d] dt \quad (2)$$

where  $t_1$  and  $t_2$  demarcate the period when either of the switch powers is greater than a set threshold value of  $400$  W. This threshold is used to separate the switching loss from the conduction loss of the devices.

### E. Mapping $V_{pk}(\mathbf{x})$ and $E_{sw}(\mathbf{x})$

The peak circuit overvoltage and switching energy loss resulting from the application of a gate waveform can be expressed as a function of the corresponding  $\mathbf{x}$ , i.e.  $V_{pk}(\mathbf{x})$  and  $E_{sw}(\mathbf{x})$ . A picture of how  $E_{sw}(\mathbf{x})$  and  $V_{pk}(\mathbf{x})$  change can be built up by generating a mesh that covers all feasible  $\mathbf{x}$ , and measuring  $E_{sw}(\mathbf{x})$  and  $V_{pk}(\mathbf{x})$  when each instance of  $\mathbf{x}$  is applied to the experimental setup. To investigate the behaviour of switching energy loss under a circuit peak overvoltage constraint, a maximum allowable voltage  $V_{lim}$  of  $225$  V is chosen, representing  $25\%$  overshoot on a DC bus of  $180$  V.

An initial mesh was created by stepping  $x_1$  from  $0.1 \mu s$  to  $1.7 \mu s$  in  $0.1 \mu s$  increments, and stepping the voltage elements of  $\mathbf{x}$  in  $1$  V increments. At each  $\mathbf{x}$  the mean of several  $E_{sw}$  and  $V_{pk}$  measurements was taken to reduce measurement noise. The load current was held constant at approximately  $45$  A during the data acquisition.

Once the initial mesh had been evaluated, the mesh was refined around the feasible  $\mathbf{x}$  (those that satisfied the circuit overvoltage constraint) to give greater resolution in the region of interest. The switching energy loss and peak overvoltage were measured at the  $\mathbf{x}$  points in this new mesh.

This procedure was followed for  $N = 1, 2, 3$  (number of elements in  $\mathbf{x}$ ) to compare the performance of gate waveforms of varying complexity. The results are presented in Section III.

## III. RESULTS

### A. Turn-on

An illustration of the switching behaviour of the IGBT under different gate control signals is given in Figure 5, where Figure 5a shows a fast turn-on and Figure 5b shows a slow turn-on. The energy loss during the fast transition is much lower than for the slow transition. However, in the fast case, the rapid decay of the freewheeling diode's reverse-recovery current produces a high peak voltage across the upper device. In contrast,  $i_q$  rises more slowly during the slower turn-on,

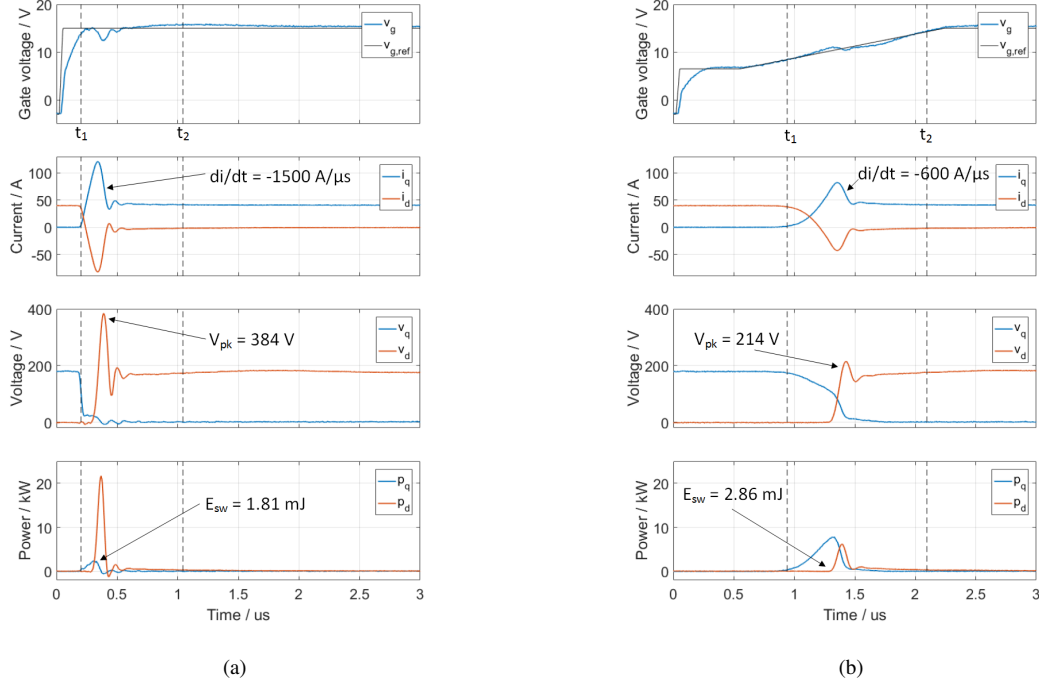


Fig. 5. IGBT gate voltages, collector currents, collector-emitter voltages, and power dissipation for a fast turn-on (a) and a slow turn-on (b).

producing a lower peak reverse-recovery current which decays more slowly. This reduces the voltage overshoot significantly but lengthens the switching duration.

Figure 6 illustrates the trade-off between  $E_{sw}(\mathbf{x})$  and  $V_{pk}(\mathbf{x})$  during turn-on when  $\mathbf{x}$  contains a single element: the duration of the active period. It is clear that longer switching durations reduce the peak overvoltage but increase the switching energy loss. Gate waveforms with  $N = 1$  are analogous to a conventional gate driver where the gate resistance is varied to change the charging speed of the gate capacitance.

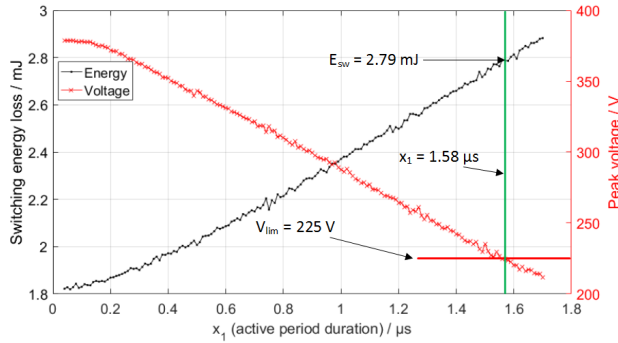


Fig. 6.  $E_{sw}$  and  $V_{pk}$  for turn-on when the duration of the active period,  $x_1$ , is varied. The voltage limit, minimum feasible duration, and corresponding switching energy loss are marked.

Figure 7a extends this to two dimensions of  $\mathbf{x}$ . It shows that the peak overvoltage reduces as switching duration increases, and that an  $x_2$  approximately halfway between  $V_{plat}$  and

$V_{hold}$  minimises  $V_{pk}$ . The adaptive meshing can be seen in the distribution of measurement points (blue dots), where the feasible region ( $V_{pk} \leq V_{lim}$ ) and surrounding area is scanned in greater detail. Figure 7b is the corresponding plot of  $E_{sw}$ , which shows  $E_{sw}$  increasing as  $V_{pk}$  reduces. The point where  $E_{sw}$  is minimised within the  $V_{lim}$  constraint is marked in Figure 7b.

Figure 8 illustrates the points evaluated when  $\mathbf{x}$  contains three elements. For clarity only those points satisfying the voltage limit of 225 V are plotted, although the entire three-dimensional volume within the variable ranges has been scanned. The orthogonal top view shows a negative diagonal trend between the feasible voltage points  $x_2$  and  $x_3$ , i.e. as the first voltage point increases, the second must reduce in order to satisfy  $V_{lim}$ . The perspective view reveals that the feasible  $x_1$ , the switching duration, ranges from  $0.225 \mu\text{s}$  to  $1.7 \mu\text{s}$ , but at faster switching the feasible ratio of voltages  $x_2$  to  $x_3$  must be greater, i.e. fast initial turn-on (high  $x_2$ ) which then slows down (lower  $x_3$ ). The colour of each point indicates the measured switching energy loss at that point. This energy peaks at slower switching when  $x_2$  and  $x_3$  are equal, and is minimised at fast switching when the  $x_2$  to  $x_3$  ratio is large.

Figure 9 shows the switching waveforms for operation at the optimum points for the  $N = 1, 2, 3$  cases. For  $N = 1$ , the period  $x_1$  must be long to avoid violating the voltage constraint. In 9b the additional voltage point  $x_2$  is barely noticeable, since it is nearly halfway between  $V_{plat}^{on}$  and  $V_{hold}^{on}$ , showing that there is little difference between the  $N = 1$  and  $N = 2$  cases when  $V_{lim}$  is tightly constrained. A significant improvement in behaviour is seen in 9c for the  $N = 3$  case. In

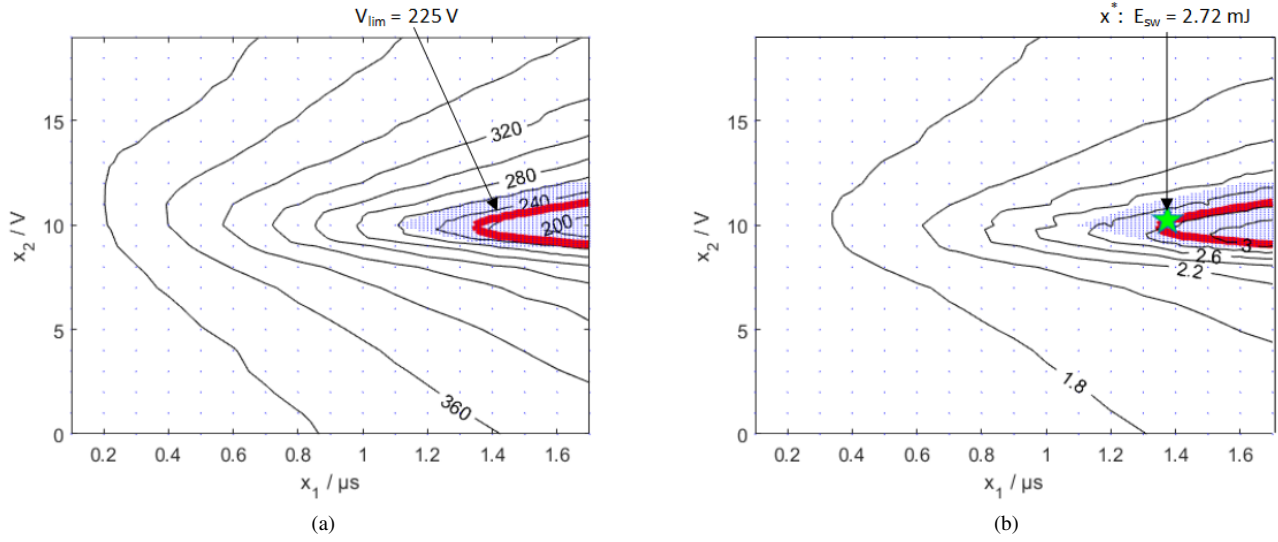


Fig. 7. (a) Circuit peak overvoltage in V and (b) switching energy loss in mJ for  $\mathbf{x}$  containing two elements.  $V_{lim} = 225 \text{ V}$  contour in bold red. Blue dots indicate evaluated points of  $\mathbf{x}$ , and the  $\mathbf{x}$  point that minimises  $E_{sw}$  subject to the voltage constraint is marked with star.

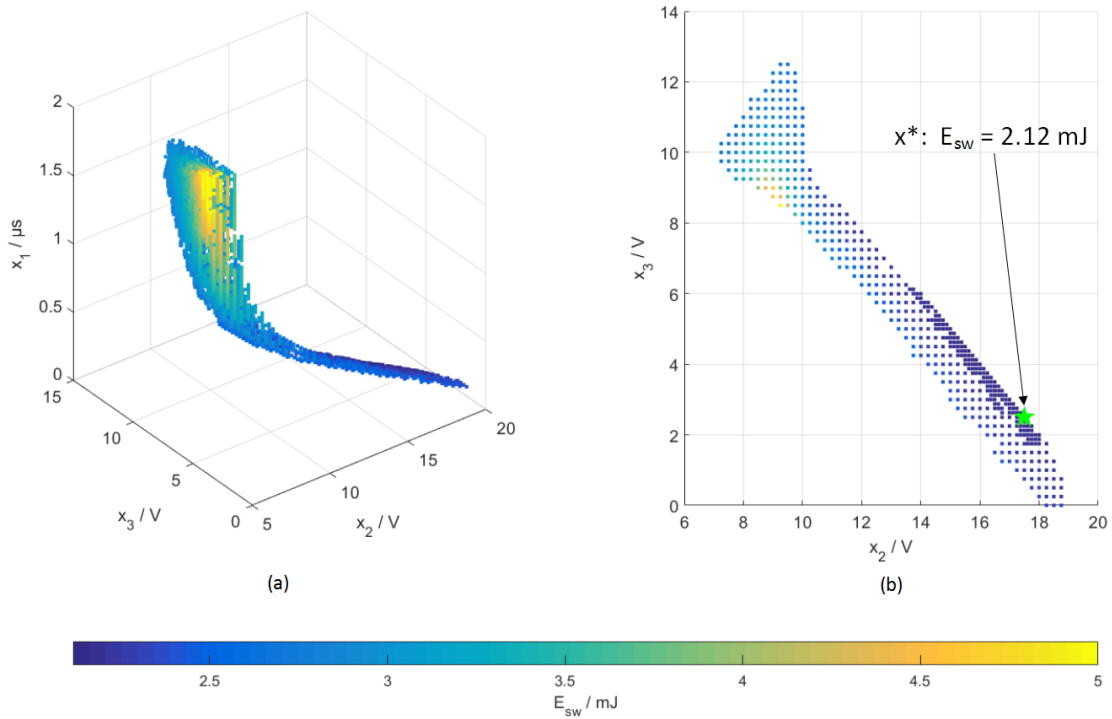


Fig. 8. Two views of the turn-on  $\mathbf{x}$  points which satisfy the voltage constraint of 225 V. The colour of each point indicates the switching energy loss recorded at that point. The star in (b) marks the point where  $E_{sw}$  is minimised.

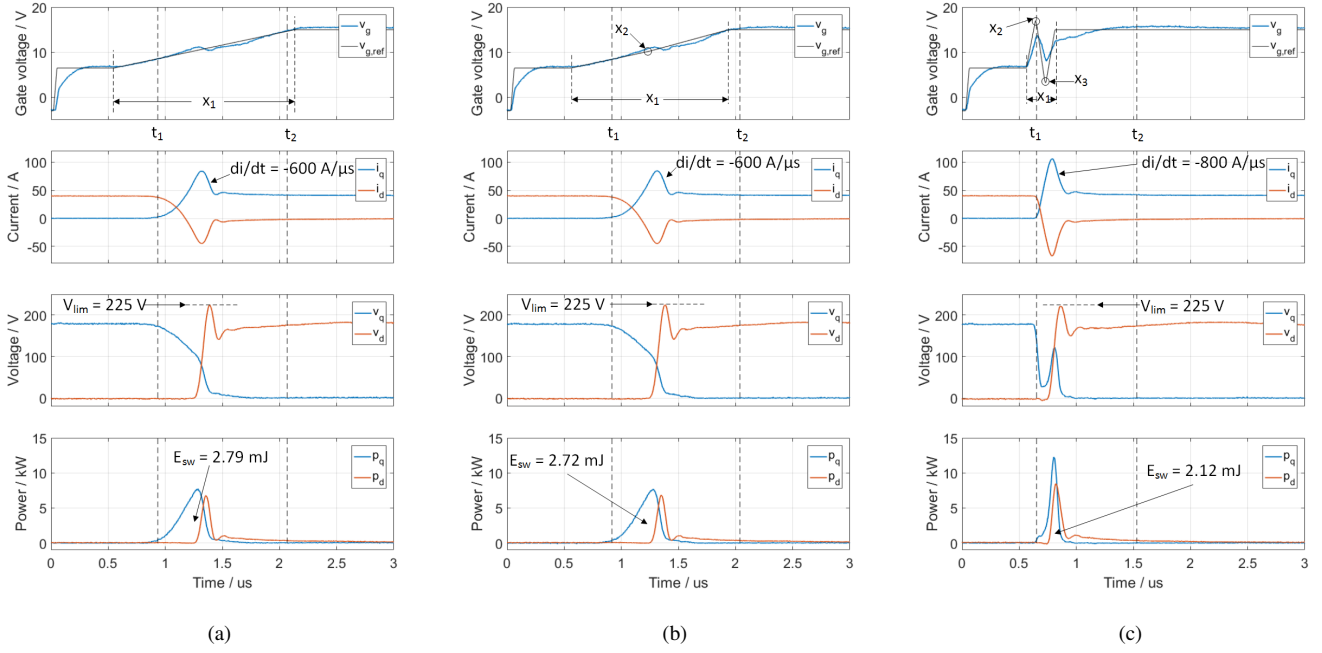


Fig. 9. Turn-on switching waveforms during operation at the optimum points for the  $N = 1$  (a),  $N = 2$  (b), and  $N = 3$  (c) cases.

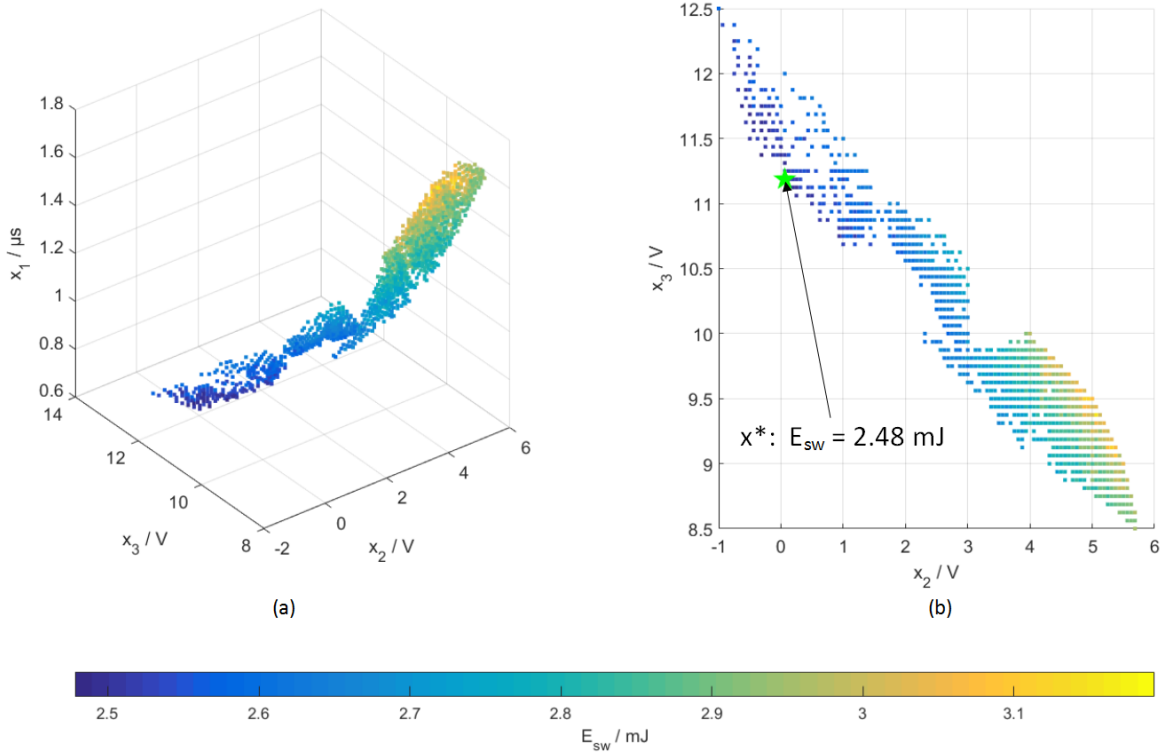


Fig. 10. Two views of the turn-off  $\mathbf{x}$  points which satisfy the voltage constraint 225 V. The colour of each point indicates the switching energy loss recorded at that point. The star in (b) marks the point where  $E_{sw}$  is minimised.

comparison with the  $N = 2$  waveforms, the control IGBT is driven hard on initially and its collector current rises rapidly, causing its collector-emitter voltage to fall rapidly as the d.c. bus voltage is dropped over the parasitic inductance  $L_n$  rather than the IGBT. This reduces power dissipation in the switch. The high  $\frac{di_q}{dt}$  reduces the switching duration, but also increases the peak reverse recovery current,  $I_{rr}$ , of the upper diode. The decay of this current once the diode becomes reverse-biased produces a voltage peak across the diode, however the impact of this is reduced because at the same time the IGBT gate voltage is momentarily reduced, increasing the IGBT collector-emitter voltage. This results in a sharing of the peak voltage between the IGBT and the diode, reducing the voltage stress on the upper device.

The optimum values of  $\mathbf{x}$  and the corresponding  $E_{sw}$  for the different cases are listed in Table II. Also included is the fast turn-on case where a square-edged gate reference is applied (see Figure 5a), which indicates the attainable  $E_{sw}$  if large voltage overshoot is acceptable. A small improvement is seen for the  $N = 2$  case compared to  $N = 1$  (2.5% reduction in  $E_{sw}$ ), however a much larger energy saving can be made when  $N = 3$  (24% reduction in  $E_{sw}$  as compared to  $N = 1$ ).

TABLE II  
THE MINIMUM FEASIBLE SWITCHING ENERGIES, PEAK OVERVOLTAGES,  
AND MINIMISING  $\mathbf{x}^*$ , FOR DIFFERENT DIMENSIONS OF  $\mathbf{x}$

$N$	$x_1^* / \mu\text{s}$	$x_2^* / \text{V}$	$x_3^* / \text{V}$	$E_{sw}(\mathbf{x}^*) / \text{mJ}$	$V_{pk} / \text{V}$
1	1.590	-	-	2.79	224
2	1.375	10.25	-	2.72	225
3	0.250	17.50	2.5	2.12	221
Fast	-	-	-	1.81	384

### B. Turn-off

The same procedure of scanning through different  $\mathbf{x}$  is followed for turn-off. For  $N = 1, 2$ , little control over  $V_{pk}$  and  $E_{sw}$  is attained, and all points violate the voltage constraint of 225 V. However, some influence is found when  $N = 3$ , as demonstrated in Figure 10 which shows the feasible points found ( $V_{pk} \leq 225 \text{ V}$ ). As with turn-on, the same negative diagonal relationship between the voltage points  $x_2$  and  $x_3$  can be seen, in this case representing a fast initial turn-off (low  $x_2$ ) which then is slowed down (higher  $x_3$ ). However, unlike turn-on, the range of feasible  $x_1$  for each  $(x_2, x_3)$  point is small, indicating that the IGBT is more sensitive to the gate waveform during turn-off. The switching waveforms for an infeasible  $N = 1$  gate signal, and a feasible  $N = 3$  signal, are shown in Figure 11.

## IV. CONCLUSION

This paper has introduced a method for evaluating the impact of varying gate voltage waveforms on IGBT switching energy loss and peak overvoltage. In a hard-switched half-bridge converter, switching energy losses and peak overvoltages have been measured for switching with a variety of gate waveform shapes of differing complexities. For turn-on, when the maximum overshoot voltage is constrained to

25% of the d.c. bus voltage (i.e. 225 V), a 24% reduction in switching energy loss is achieved by using a gate waveform with two variable voltage points, as compared to varying only the switching duration as conventional gate drivers do. This energy saving therefore represents the potential added value of using an AGD compared to a simple fixed driver. For turn-off, gate waveforms with two variable voltage points are shown to reduce the overshoot voltage while keeping switching durations short.

A key finding of this work is that significant improvements over conventional gate drivers can only be achieved if the gate waveform is formulated with enough degrees of freedom such that the power device can be switched quickly at first and then slowed down. This is accomplished here by using two voltage points as variables and scaling them in time. Further degrees of freedom may produce better switching behaviour, but also increase the range of possible waveforms. This is pertinent in the context of optimising the gate waveform during operation, as a solution must be found quickly if it is to be useful given the changing operating conditions of a real power converter.

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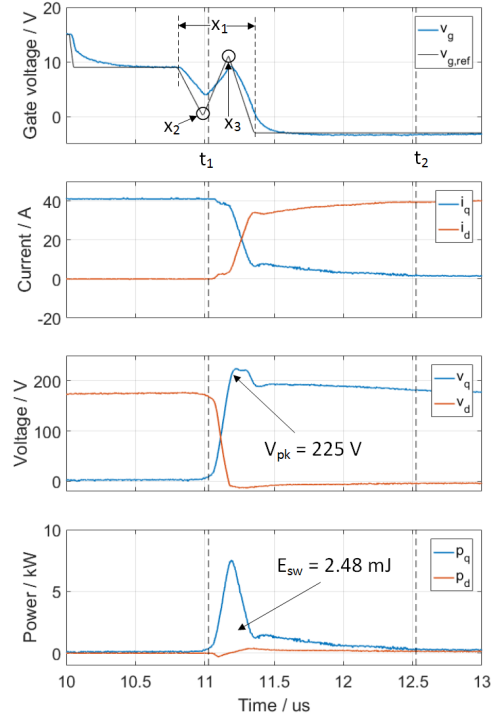
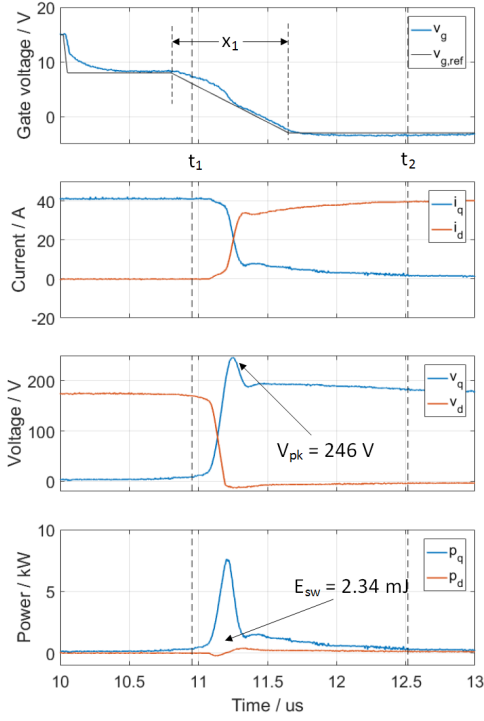


Fig. 11. Turn-off switching waveforms during operation for  $N = 1$  (a) and at the optimum point marked in Figure 10b for  $N = 3$  (b). No feasible points were found for  $N = 1$  and  $N = 2$  cases.