Removal of dislocation cores from multicrystalline silicon by etching

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Thesis submitted for the Degree of Master of Science

Hilary Term 2011

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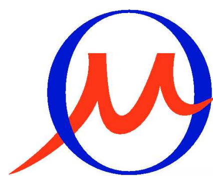

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Abstract

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Approximately 50% of solar cells are based on multicrystalline silicon (mc-Si). A major limiting factor in their efficiency is recombination of electron-hole pairs at dislocations. Manufacturers of mc-Si wafers are focussing on reducing dislocation densities by modified casting techniques. However, an alternative approach is to remove the dislocations after growth and wafering. This thesis aims to explore the feasibility of using chemical processing to remove dislocations from mc-Si wafers.

For measuring the depth to which dislocation cores are removed an angle lapping technique is first developed. This allows the pit diameters and depth of bulk material removed to be measured. The parameter "aspect ratio" is defined as the ratio of dislocation etch pit depth to diameter; a high aspect ratio is desirable. The results gained allow the dislocation core removal process to be studied and optimised.

The first etching system explored is the Secco etch (1 $K_2Cr_2O_7$ (0.15M):2 HF (49%)), a commonly used defect-revealing etch. Samples are immersed in Secco etch for various durations at a range of temperatures, and pits are formed at the locations of dislocations and grain and twin boundaries. Secco etch is found to remove dislocations to depths of up to 40μm. The activation energies for dislocation etching, etch pit widening and bulk etching are calculated as 0.20, 0.23 and 0.30eV respectively. Scanning electron microscopy is used to determine the geometry of the etch pits. Their structure is shown to be somewhat tubular, but the diameter of the pits is relatively large; too much bulk material is being removed. Further, at all temperatures the aspect ratio decreases with an increase in etch duration, so the aim of long, narrow etch tubes does not appear to be feasible using Secco etch.

Finding an alternative etching system with a lower bulk etch rate is the next aim. Anodic etching, where the silicon sample is biased whilst immersed in a solution, is therefore investigated, as control of the etch strength is provided by varying the electrical parameters. The overall etch rates for both dislocation etching and bulk etching are approximately two orders of magnitude lower; etch durations of over a day are needed to produce pits comparable to 20 minutes Secco etching. This, however, does not lead to improvements in aspect ratio, and the etching behaviour is hard to control. Anodic etching appears to be much more sensitive to small, local changes in condition, evidenced by varying results across different regions of a single sample.

Slower acting chemical etches are the final system that is investigated, and are chosen based on the strength of the oxidising agent present. The aim here is that the alternative etch solutions provide a very low bulk etch rate and are used at very long etch durations to produce long etch tubes with very high aspect ratio. An iodine-based etch (1 I_2 (0.01M):2 HF (49%)) is the only candidate found to produce good defect delineation, but the dislocation etch rate is very low and again the aspect ratio is unsuitable for removing dislocations deep into wafers.

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Chapter 1

Introduction

Photovoltaic energy can comfortably supply the world's energy demands using clean, safe technology. At present, 90% of solar cells are silicon based [1] and more than half of these use multicrystalline silicon (mc-Si) [2]. The technology involved in producing mc-Si solar cells is relatively mature yet one major materials problem remains - recombination of charge carriers at dislocations. The aim of this project is to investigate novel methods for removing dislocations from the material after growth, hence providing the potential to reduce recombination and increase mc-Si cell efficiencies. In this Chapter, the background to the project is discussed.

1.1 Project background

1.1.1 Energy demand

The need for alternative energy sources is driven by two main factors: a desire to reduce dependence on a diminishing fossil fuel supply [3]; and a need to minimize production of pollutants such as CO_2 that contribute to climate change [4], and in turn could lead to a global crisis [5]. In addition, as the worldwide population grows and increased development takes place, the total demand for energy is predicted to increase more than threefold by the end of the century [6]. Current and predicted worldwide energy use is shown in Figure 1.1. Although the accuracy of predictions so far into the future may be questionable, it is clear

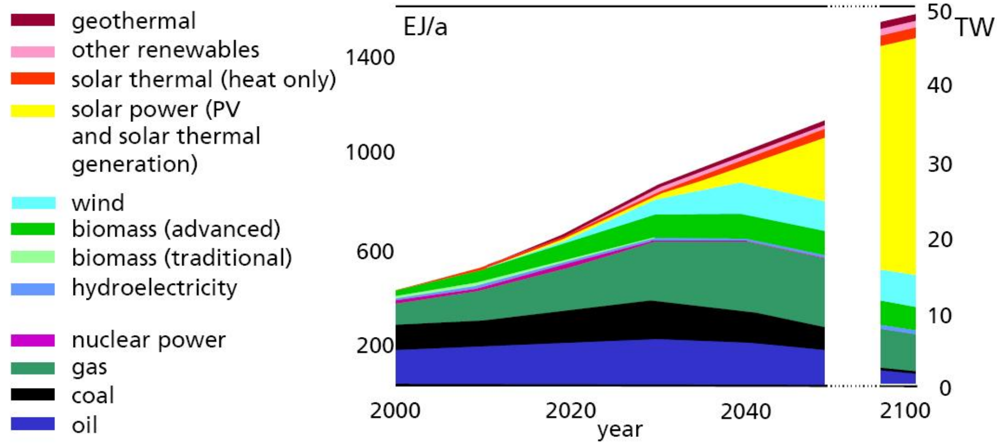


Figure 1.1: Predicted worldwide energy usage and proportions supplied by different sources, after [6].

	Gas	Coal	Nuclear	Wind	Biomass	Solar (PV)	Hydro
Cost ($0.01/kWh)	4.9-8.4	4.9-7.9	3.9-8.0	3.0-8.0	2.8-7.6	15-30	4.2-7.8

Figure 1.2: Energy generation costs of current technologies, after [7].

that a consensus has emerged that vastly more energy will be required, and that this energy must be cleaner.

Various studies [7, 8] have concluded that energy from clean renewable sources, particularly solar power, is not currently cost effective when compared with existing power generation techniques involving the combustion of fossil fuels, and one set of results is summarised by the table in Figure 1.2.

1.1.2 Solar power

The current worldwide energy usage estimate shown in Figure 1.1 is approximately equal to the radiation from the sun incident on the entire Earth's surface in 40 minutes [9], so it is clear that solar power has the potential to satisfy all our energy needs if technology can be developed that more fully exploits the sun's energy. Figure 1.3 shows how solar compares to wind and geothermal energy in terms of maximum available energy.

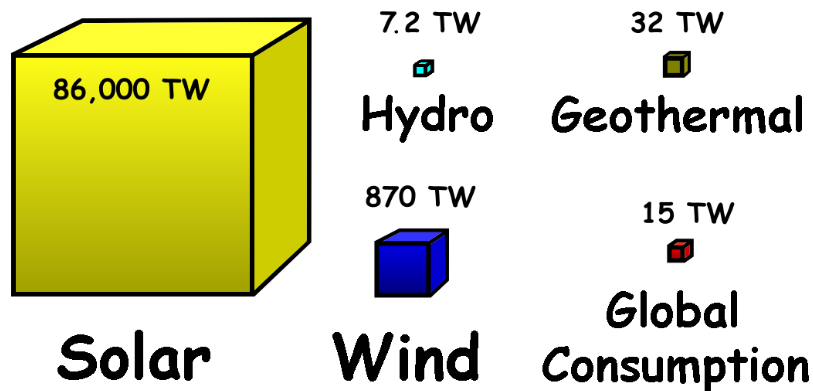


Figure 1.3: Graphical representation of maximum available energy from wind, geothermal and solar sources. Data collated from [10].

Solar power can be divided into two distinct fields:

- Photovoltaics
- Solar thermal

Photovoltaic devices, or solar cells, convert sunlight directly into electricity which is then either fed into the grid (usually from a large collection of connected modules, such as in Figure 1.4) or used to power equipment local to the installation, for example solar powered lighting or heating.

With the help of government subsidies the photovoltaic industry as a whole has grown by a factor of 200 over the past 20 years [12], but without them the cost/power ratio of today's solar technologies does not compare favourably with existing fossil fuel based supplies of grid electricity and some of the renewable technologies mentioned previously. However, assuming the current trends in cost reduction and performance improvement continue for the next few years, it is predicted that in some countries power from solar and fossil fuel sources will be at the same price by 2012 [13], with target costs of €1/W or $1/W [14] both being suggested. Of course, further research and development will be needed to make solar energy viable in all countries, including the UK.

Figure 1.4: 11MW, 0.6km^2 (land area) solar power plant in Serpa, Portugal after [11].

Solar thermal technology describes using sunlight to directly heat something (typically a fluid) and, like photovoltaics, has a wide range of applications ranging from small installations heating an individual swimming pool to grid-connected power plants where electricity is generated using a steam or gas turbine at temperatures of up to 1000 °C [15]. In the latter a complex array of mirrors is used to concentrate and focus the sunlight, and these have the ability to track the direction of the sun to maximise efficiency. Solar thermal, whilst an interesting technology, is not discussed further here.

1.1.3 Solar energy implementation

As Figure 1.2 shows, grid electricity derived from PV installations is not cost effective without subsidies when compared with electricity from either coal-fired power stations or other renewable sources. However, compared to other renewables, the possibilities for scaling up solar are almost endless as there is simply so much sunlight incident on the Earth (see Figure 1.3), and this is available in areas where the land is not otherwise in use. For example, building six very large PV plants spread around the world in remote desert locations would be able to provide 20TW at present efficiency levels [16], which is more than sufficient to supply all the

world's energy at current usage levels. It would require upgrades in power transmission and storage technology to efficiently transmit the power to consumers, but schemes involving DC backbones and compressed air storage have been proposed to solve this issue [9].

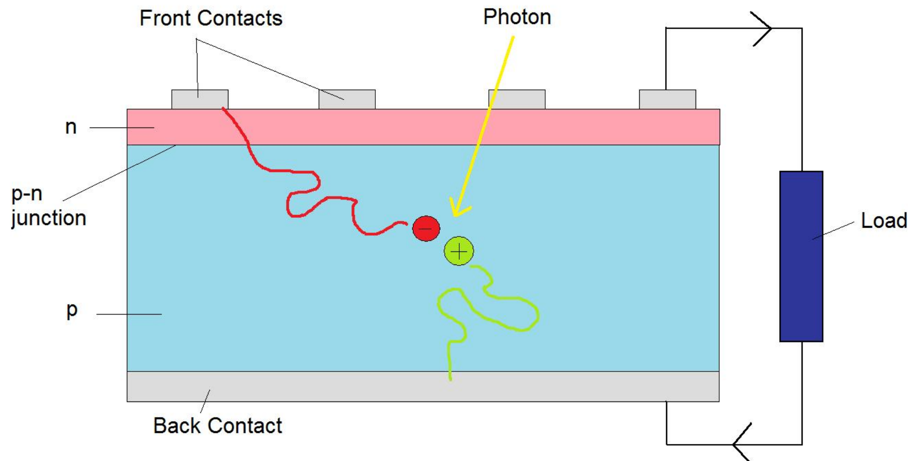


Figure 1.5: Simplified silicon solar cell structure. Recombination at defects (including dislocations) and surfaces has been ignored.

1.1.4 How do silicon photovoltaics work?

The structure of a typical solar cell is a semiconductor containing a p-n junction, with a contact either side of the junction connected to an external circuit (Figure 1.5). This kind of device typically has rectifying behaviour (i.e. a diode); small current under reverse bias and large, exponentially increasing current under forward bias due to the barrier heights for the respective transitions (Figures 1.6 and 1.7). In this case the device is designed to convert energy from light into useful electricity by making use of the photovoltaic effect, which was discovered by Becquerel in 1839 [17] (and specifically for silicon p-n junctions by Ohl in 1940 [18]). When photons with energies greater than or equal to the bandgap (1.1eV for silicon [19]) are incident on the cell, electron-hole pairs are generated and the internal field (produced by the p-n junction) separates them such that they reach the contacts and produce a current. This is a reverse, or leakage, current as it is the minority carrier concentration that is increased. The plot in Figure 1.7 shows how, by operating at a load where the current-voltage (I-V) product is maximised, this additional photogenerated current leads to useful power generation.

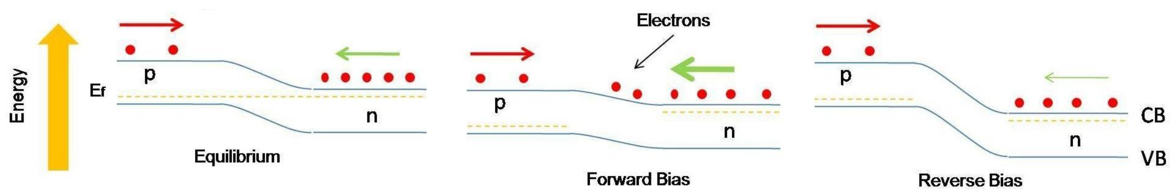


Figure 1.6: Energy diagram for a p-n junction under different bias conditions.

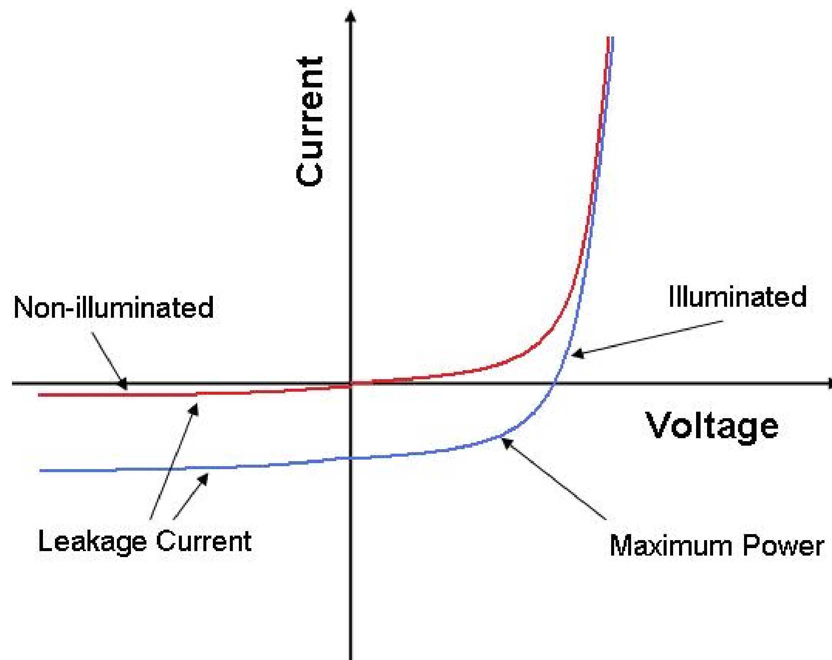


Figure 1.7: Schematic of p-n junction current-voltage characteristic.

Electrical properties of solar cells

The ideal-diode equation describes the current-voltage characteristics of non-illuminated solar cell p-n junctions [19]. The current density is defined as follows:

$$J = J_s(\exp\left(\frac{qV}{kT}\right) - 1) \qquad \text{Acm}^{-3} \tag{1.1}$$

$$J_s \equiv \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{po}}{L_n} \qquad \text{Acm}^{-3} \tag{1.2}$$

where

- J is the current density in Acm^{-3}
- J_s is the saturation current density (SCD) in Acm^{-3}
- D_p is the diffusion constant for holes in cm^2s^{-1}
- D_n is the diffusion constant for electrons in cm^2s^{-1}
- n_{po} and p_{no} are the equilibrium minority carrier concentrations of electrons and holes respectively in cm^{-3}
- L_n and L_p are the electron and hole diffusion lengths respectively in cm.

A simple circuit can be used to model a typical solar cell, shown in Figure 1.8. The series resistance arises from the contact between metal and semiconductor and from the resistance inherent in the doped layers. Shunts are physical manufacturing defects that allow the photogenerated current to be diverted to a path other than the solar cell junction, reducing the voltage from the cell. Shunts are modelled in the circuit as a parallel resistance, the lower this is the worse the power losses suffered by the cell.

Efficiency

A solar cell's energy conversion efficiency, η, is defined as the percentage of power converted (from incident light to electrical energy) and collected, when a solar cell is connected to an electrical circuit:

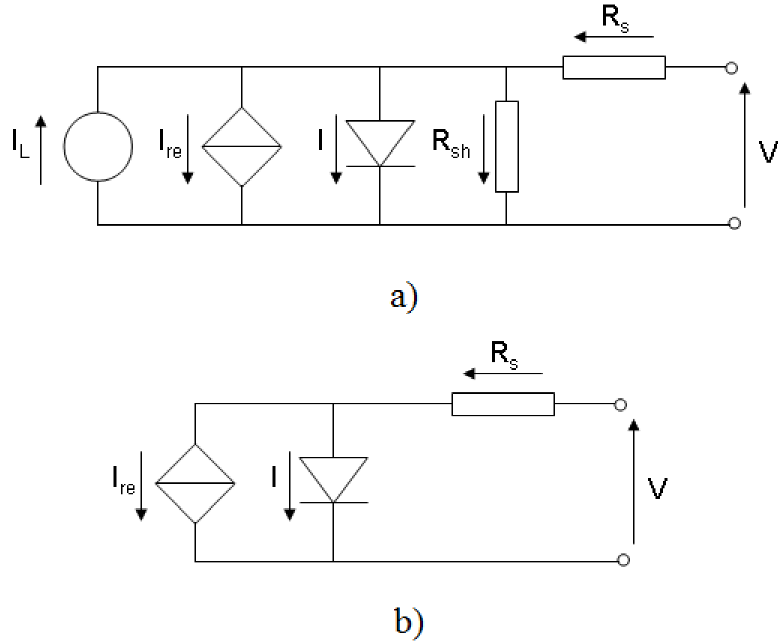


Figure 1.8: The equivalent circuit for a) an illuminated solar-cell and b) a non-illuminated solar-cell with shunt resistances ignored. (After Sze [19]).

$$\eta = \frac{P_m}{E \times A_c} \tag{1.3}$$

where

- P_m is the maximum power point in W
- E is the light irradiance in Wm^{-2}
- A_c is surface area of the cell in m^2.

Losses in efficiency can be categorised thus:

- reflectance losses
- resistive electrical losses
- thermodynamic efficiency losses
- recombination losses.

The first two categories are straightforward: some photons are not absorbed by the cell so cannot be converted into useful power; and the inherent resistance of contacts and the doped layers within a cell cause heat losses. The thermodynamic efficiency of a cell relates the energy of the incident photons to the band structure of the cell. Only photons with energies exactly equal to the bandgap are converted perfectly efficiently, those below do not generally generate carriers and those above provide the generated carriers with additional kinetic energy which is again usually lost as heat. This alone limits conversion efficiency to around 44% in a standard single junction cell [20]. This is further reduced to 31.0%, even for an optimal single-juction cell, due to the output voltage of the cell being less than the band gap potential - this is known as the Shockley-Queisser limit [21]. Recombination describes what happens to photogenerated electron-hole pairs that are not collected by the cell contacts. Defects in the material introduce deep levels into the band gap that aid recombination and therefore reduce carrier collection efficiency. This occurs when electrons transition down into the valence band via these recombination centres by emitting energy in the form of phonons or photons; Figure 1.9 is a schematic band diagram representation of how this occurs in silicon solar cells. The nature of these defects will be detailed in later sections.

1.1.5 Types of solar cell

Solar cells types are split into three generations in order to categorise them according to the order in which they were first developed. The nomenclature is somewhat misleading as there is a suggestion that later generations are improvements on earlier ones, whereas in practice the first generation devices stand alone from the newer cells as a competitor and are still both market leading and the subject of much ongoing research.

In terms of large-scale energy supply, first generation devices have been available commercially for a number of years, second generation are being commercialised presently and third generation are still under development. Figure 1.10 shows how the three generations compare in terms of projected efficiency and cost, and Figure 1.11 details the efficiencies reached by a variety of existing technologies. Note that the efficiency of an installed module is typically around 5% lower than the best figures for a given design of cell [23], which are generally

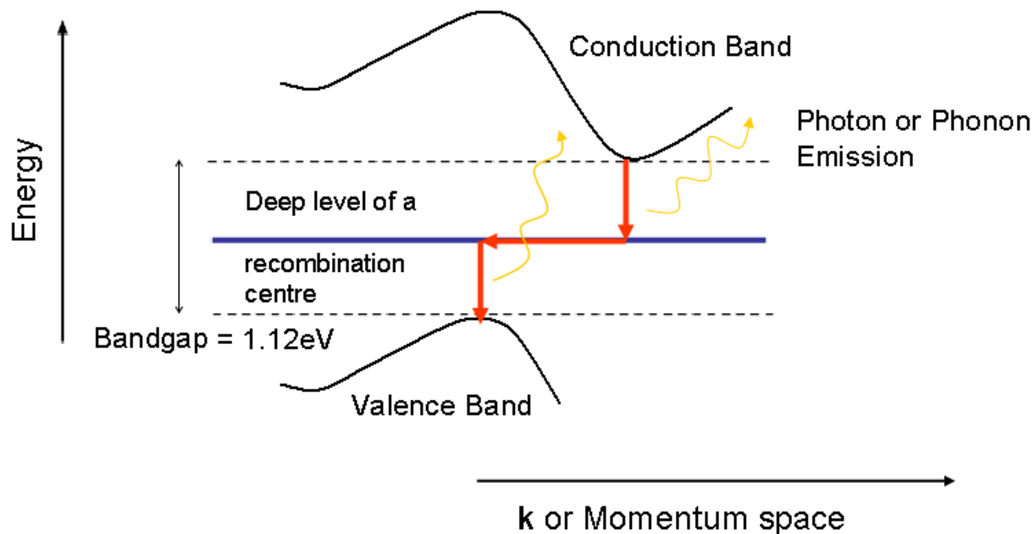


Figure 1.9: Simplified band diagram of silicon showing indirect recombination through carrier interaction with recombination centres [19, 22].

achieved in a laboratory environment.

1.1.6 First generation

First generation cells are typically large-area, high quality, single junction devices such as those made from bulk silicon. These cells accounted for around 90% of total worldwide production in 2007 [16], making them the dominant current technology. As well as being the second most abundant element in the Earth's crust, silicon is light, non-toxic and stable [26], making it ideally suited to the very large scale worldwide production and implementation needed to keep pace with a total PV market growing at 40% per annum [16]. At current efficiency levels first generation cells provide an energy payback of 1-5 years compared to a lifetime of up to 30 years [27]. In addition, thanks to decades of research into silicon's properties and processing by the integrated circuit industry, knowledge of silicon production is very mature and this information should allow the silicon solar cell industry to maintain its competitive advantage over other, newer technologies for the next few years as they are built up from a lower starting level in terms of existing expertise.

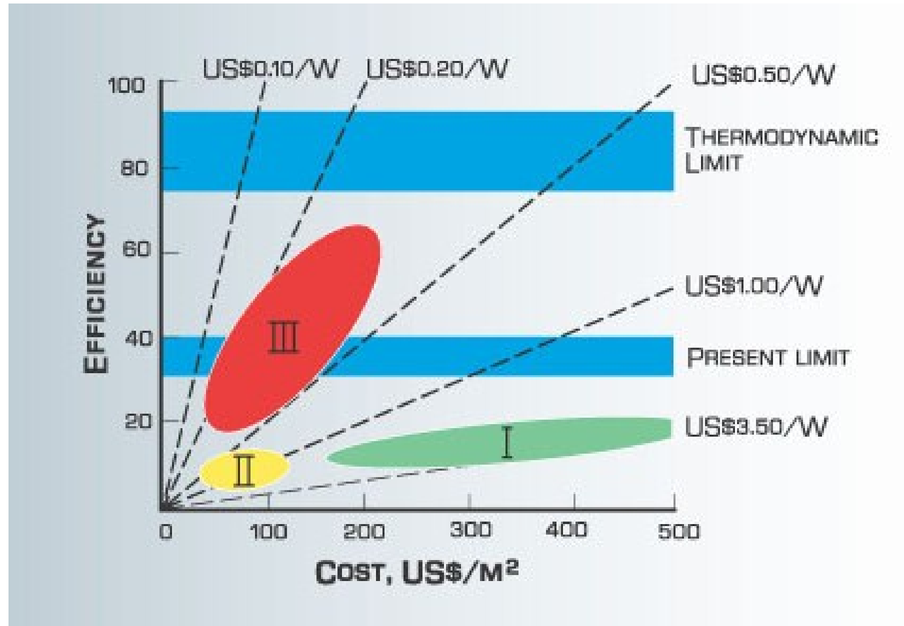


Figure 1.10: Efficiency and cost projections for first-, second- and third-generation photovoltaic technology (wafers, thin-films, and advanced thin-films, respectively), after [24].

The first generation market is divided into two main classes based on how the silicon is produced.

Single crystal silicon

Single crystal silicon, also known as monocrystalline silicon, is typically produced by the Czochralski method [28]. This uses a seed crystal to draw out large cylindrical ingots, typically 300mm in diameter and up to 2m long, from a crucible of molten silicon. Usually, a p-type dopant such as boron is added to the melt and the necessary p-n junction is created by diffusing in an n-type dopant such as phosphorus after the ingot is sawn into wafers. The impurity content of this material is highly controlled (due to partition coefficient effects most impurities are left in the melt) and the level of crystal defects (including dislocations) is almost negligible, which leads to high efficiencies in the final cells made from c-Si, but the growth process is relatively slow and expensive. The best efficiency for a complete solar module using Czochralski-grown silicon is 23% [29]. Using concentrators to multiply the amount of incident light can raise the efficiency to 27% [23]. The maximum theoretical efficiency of silicon based cells has been calculated as around 30% [19]. The main problem (ignoring

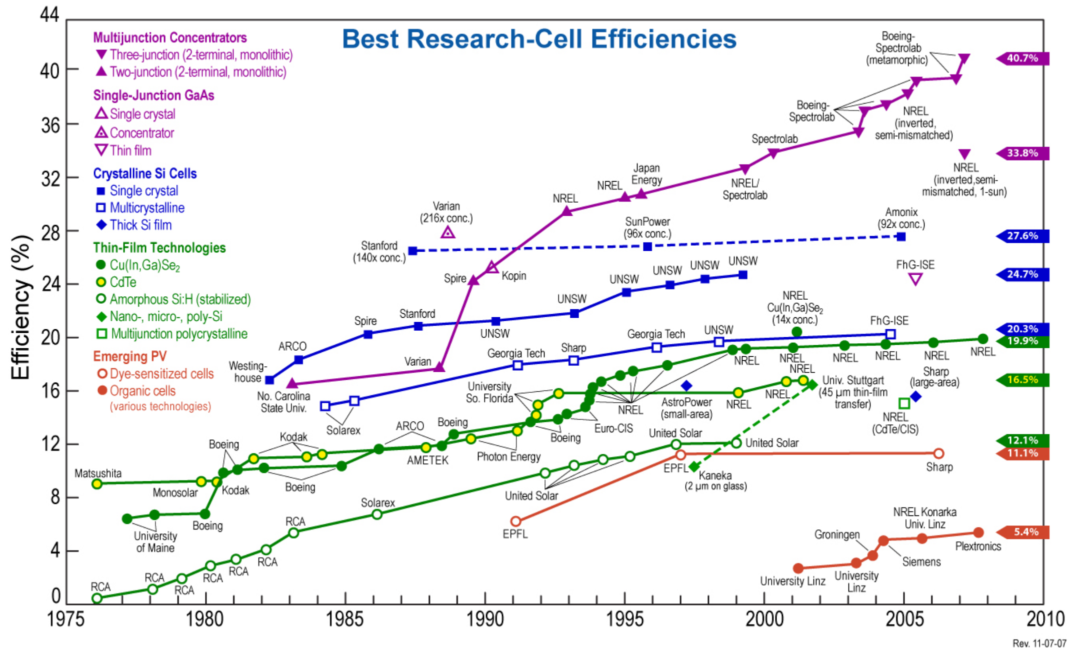


Figure 1.11: Timeline of cell efficiencies, after [25].

high cost of production) with single crystal material, involves a degradation of performance (efficiency is reduced by up to 10% relative) on exposure to light, due to the presence of light-activated boron-oxygen complexes that act as recombination centres [30, 31].

Multicrystalline silicon

Multicrystalline silicon, mc-Si, is a cast material produced by a variety of techniques, the most widely used being directional solidification of a melt into a very large (1m x 1m x 0.5m approx.) cuboidal ingot [32]. Compared to the Czochralski method, which uses a highly refined, extremely pure feedstock, the melt contains a higher concentration of metallic impurities, as the feedstock typically consists of either material rejected from single crystal production or recycled material due to shortages in silicon supplies. These impurities, in addition to the crystal defects (grain boundaries and dislocations) present due to the casting process, lead to a reduction in performance as they introduce energy levels into the band gap and cause recombination [33]. Any and all elements present in the feedstock are incorporated into the melt during production, and although solidification occurs such that most impurity atoms are collected in the end portion of the ingot which is later removed (thrown away

or recycled), some unwanted elements remain and this is clearly a disadvantage compared with the Czochralski process detailed above. The most detrimental contributions to reduced carrier collection efficiency (and therefore the overall cell efficiency) for mc-Si are transition metal impurities and dislocations [33], with the effects worsened when the thermal conditions involved in processing the cells allow the impurities to diffuse to and decorate the dislocations, either as point defects or precipitates [34, 35, 36]. Grain boundaries do not present too much of an issue, as it is easy to produce wafers with a grain size of more than 1cm by carefully controlling ingot cooling rates. At these grain sizes, the average distance of a charge carrier to a grain boundary is typically much longer than its diffusion length, thus their effect on recombination is negligible compared to the other defects present. The two key factors are dislocations and transition metals at the dislocations. Cells made from mc-Si lead to a module efficiency of only 15%, but can achieve similar $/W (a cost-per-power figure of merit) performance due to the chepaer manufacturing process [23]. Much research is being carried out to increase the efficiency of mc-Si cells, as described in Section 1.2.

1.1.7 Second generation

Second generation cells arose from a need to reduce processing costs further, with the focus on using less material in the active region of the cell. This lead to the development of thin-film technologies such as cadmium telluride (CdTe) and copper indium gallium selenide (CIGS). Another silicon-based cell design, using thin-film amorphous silicon (a-Si), is also classed as second generation. Commercialisation of these technologies has proved difficult to this date; in terms of PV market share CdTe and a-Si have around 5% each and CIGS has around 0.5% [37]. Efficiencies are low compared with first generation cells, but again the $/W figure is comparable [23]. There are also concerns over the toxicity of cadmium [38] and the availability of indium, tellurium and germanium [39].

1.1.8 Third generation

Third generation technologies aim to enhance poor electrical performance of second generation thin film technologies (with a target of doubling of tripling the 15-20% efficiencies found

in existing devices) while maintaining very low production costs, with projections shown in Figure 1.10. The most promising and well-developed of the candidate technologies is multijunction cells. These are fabricated by epitaxially depositing thin layers of semiconductors such as Ge, $GaInP_2$ and GaAs with different band gaps, into a stack, each absorbing a narrow range of photon energies [20]. In total this allows a much wider energy range of photons to be absorbed than can be achieved with a single material, increasing the theoretical efficiency limit (assuming an infinite stack) to 86.8% [40]. In practice, efficiencies of 40% have been achieved by combining multijunction cells with concentrators [25]. The epitaxial growth techniques used for these layered devices are very expensive and labour intensive, so mass production of multijunction cells in their current form would not be cost effective. Clearly in specialist applications where cost is a less important factor, multijunction cells are a viable option. Power for space satellites is an example of an application where high efficiency is desired almost regardless of the cost [41]. For the technology to be a viable solution for a worldwide solar effort, supplies of the various constituent elements would have to be increased massively, assuming they even exist in sufficient abundance. An increase in demand for any rare elements will initially cause a corresponding sharp increase in costs which could hinder any plans to scale up third generation cell production - even with production of cells currently at an embryonic stage gallium and germanium costs have started increasing.

Other proposed technologies at a very early stage of development include dye-sensitised solar cells [42], which use a combination of light-absorbing dye and n-doped titanium dioxide nanoparticles to convert the photons to electricity; and polymer solar cells [43]. Efficiencies are currently below 10% and there are concerns over cell stability [44], but in the future these may become a useful low-cost alternative for small-scale power generation off-grid.

1.2 Improving silicon solar cells

Without government subsidies, silicon-based photovoltaics are not currently cost effective for large scale power generation, but various cost-reducing and performance-improving technologies are helping close the gap to existing energy sources. There are two distinct ways to

improve solar cells in terms of commercial viability:

- Increase efficiency for a given cost level, or
- Reduce cost for a given performance level.

The former relies on improving the silicon material itself and the cell structure in order to minimise the efficiency losses described in Section 1.1.4; a range of efficiency improving techniques are discussed in the rest of this Section. Cost reductions require process improvements at the industrial scale such as reducing the quantity of silicon used, for example by making thinner cells [45], improving sawing techniques [46] and better recycling of substandard material; and also improving the casting process by using less energy [47], producing bigger ingots [48], increasing the growth rate [49] and further increasing feedstock tolerances [50]. Industrial process improvement is outside the scope of this thesis thus is not discussed further.

1.2.1 Wafer production

Reducing the amount of silicon used by producing thinner wafers has been occurring for around 30 years; from 400μm in the 1980s to under 200μm today [16, 14]. A graph of the decreasing thickness trend is shown in Figure 1.12. As the quality of mc-Si feedstock used today may be poorer in an attempt to minimise feedstock costs, reducing wafer thickness becomes important for another reason. For material with low minority carrier diffusion length, models predict that cell efficiency improves with decreasing thickness as the likelihood of a recombination event is related to the volume of material [51]. Figure 1.13 shows the relationship between thickness and efficiency for a range of minority carrier lifetimes.

1.2.2 Advanced cell structures

A range of features are used to maximise light absorption and minimise recombination; working from top of cell to bottom:

1. Anti-reflective coatings

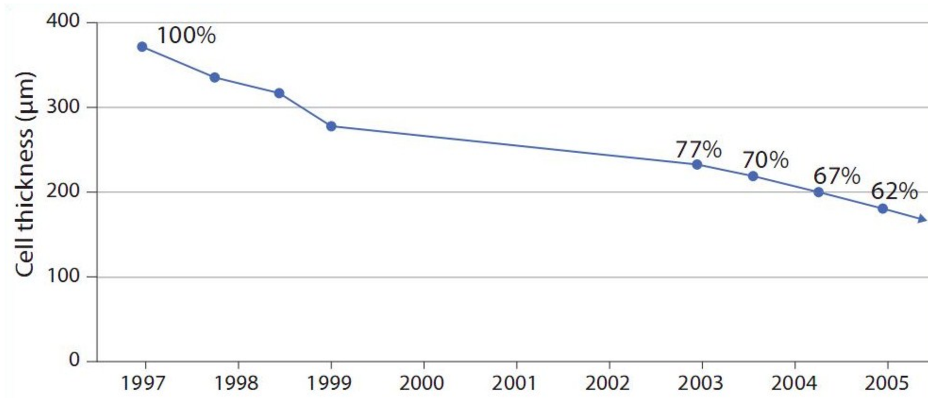


Figure 1.12: Graph showing trend of reducing wafer thickness [14].

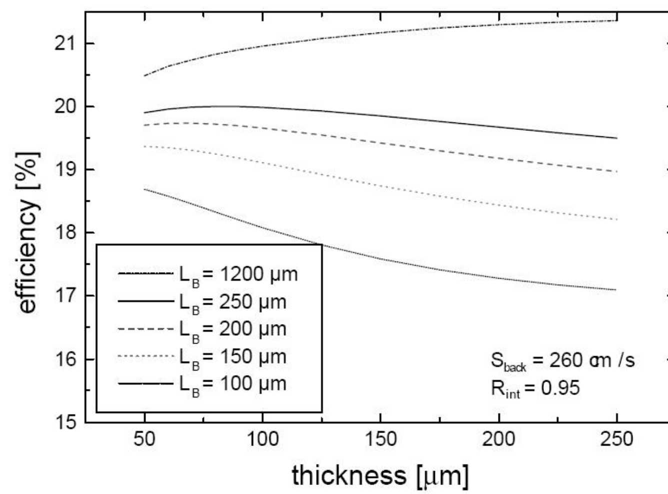


Figure 1.13: Solar-cell efficiency as a function of wafer thickness and minority carrier diffusion length, after Bruton [45].

2. Front surface texturing
3. Front surface passivation
4. Front contact optimisation
5. Bulk passivation
6. Gettering
7. Back surface passivation
8. Back contact optimisation

Developing novel cell structures that maximise the carrier collection efficiency becomes increasingly important as reduced quality (low lifetime) silicon feedstock is used in the manufacture of cells. From the list above, 1, 2, 4 and 8 fall into this category. As silicon is an indirect band gap semiconductor and therefore requires a thick (up to 1.5mm) [45] active layer to absorb the full solar spectrum, maximising absorption is particularly important. The first step is antireflective coatings, which work by introducing an additional interface into the path of the light (now air-coating and coating-silicon), which reduces reflection if the refractive index of the coating falls between that of air and silicon. Some examples of suitable materials are low-pressure chemical vapour deposited silicon nitride [52], chemical bath deposited zinc sulphide [53] and porous silicon [54]. Front surface texturing is used to further reduce reflective losses, which are dependent on the angle of incidence of the sunlight. Mechanical [52] and laser [55] techniques are used to produce a grooved surface such that some additional light that is initially reflected can be captured, as illustrated in Figure 1.14.

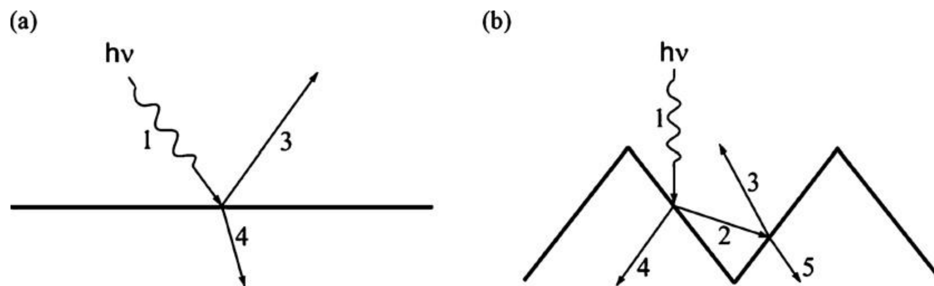


Figure 1.14: The influence of surface texture on light reflection: (a) planar surface and (b) textured surface. (1) Incident light, (2 and 3) reflected light and (4 and 5) absorbed light, after [56, 57].

The front cell contacts, typically a metallic grid, cause "shading" losses by blocking a fraction of the light incident on the top surface of a cell. However, reducing the area of the contacts would lead to poor carrier collection efficiency, so a compromise must be found to achieve the best balance. The buried contact [58] and angled buried contact [56] structures are designed so that much of the surface area of the contact is located below the front surface in the bulk of the cell, reducing absorption loss due to shading but retaining sufficient contact area to ensure good carrier collection efficiency. The back contact is a less critical region as there are obviously no issues with absorption or shading, the chosen geometry is simply that

which allows easy connection to the external module. Examples of metallization materials used in commercial cells include various alloys of nickel, copper and aluminium, chosen for their stability and conductivity.

A novel approach to reducing shading losses was devised by Gee *et al.* in the early 1990s [59] and developed more recently by Neu *et al.* [60]. Named the "emitter-wrap-through" design, both cell contacts are situated on the back side of the wafer in an interdigitated array; in order to eliminate the formation of rectifying p-n junctions between emitter and base the types of contact are separated by diffusion barriers. A range of alternative back contact designs also exist: metallization wrap around (MWA), metallization wrap through (MWT) and pin-up module (PUM) [61, 62, 63].

1.3 Multicrystalline silicon for solar cells

The focus of this project is mc-Si solar cells. In this section mc-Si growth processes are discussed, followed by the defects in the material and processing methods used to deal with them industrially.

1.3.1 Crystal growth

About five or so years ago, a worldwide silicon feedstock shortage [64] lead to multicrystalline silicon becoming increasingly favoured over single crystal material due to the wider feedstock tolerances it affords the manufacturer [65]. Although supply problems have now been mostly overcome as new solar-grade silicon production facilities have come onstream, a small shortage still exists today [66]. In turn, this has stimulated research efforts to increase mc-Si cell efficiencies such that they are competitive with Czochralski-grown material and recent advances claim to have lowered the gap [32].

Large ingots of mc-Si are grown by directional casting in a fused silica crucible, frequently with a silicon nitride non-stick lining. A predominantly columnar grain structure is produced by controlling the heat flow and thermal gradients. A schematic of the process is shown in Figure 1.15. In commercial ingot production, cooling rates are between 100 and 40°C per

hour [67]; this is an important factor in the type and distribution of the defects that will be contained in the ingot. The nitride coating is also reported to be responsible for some of the observed contamination [68].

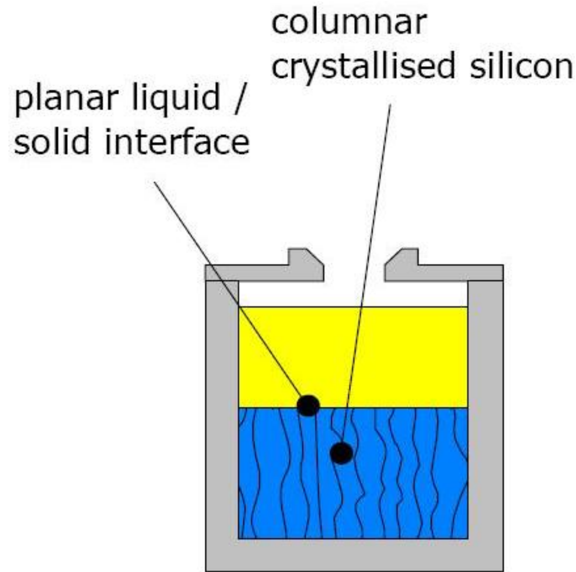


Figure 1.15: Schematic of the mc-Si directional solidification technique, after Weber [16, 69].

The texture and grain structure of typical cast mc-Si has been analysed by reflectometry [69] and in-situ measurements [70] so is well understood. A mixture of {111}, {110} and {100} grains are shown to be present, with grain sizes of around a centimeter being typical [71].

1.3.2 Defects

As introduced in Section 1.1.6, mc-Si contains a range of defects that affect cell performance.

Grain boundaries

Grain boundaries are present in the material, but due to the average grain size of cast mc-Si being over 1cm^2 and typical carrier diffusion lengths of order $100\mu\text{m}$, their effect on conversion efficiency is negligible [72]; this is helped by the absence of "horizontal" grain boundaries that results from the uniaxial crystal growth. Figure 1.16 shows a typical cast wafer, with the grain structure clearly visible. In material with high carbon content, large, non-metallic

Figure 1.16: Multicrystalline silicon wafer, with 2 x 1cm bar for scale.

precipitates, also known as filaments, of silicon carbide (see Figure 1.17) may be present in the grain boundaries [73]. These can short circuit the back side field and emitter of the cell, causing "ohmic shunts" and leading to low efficiency.

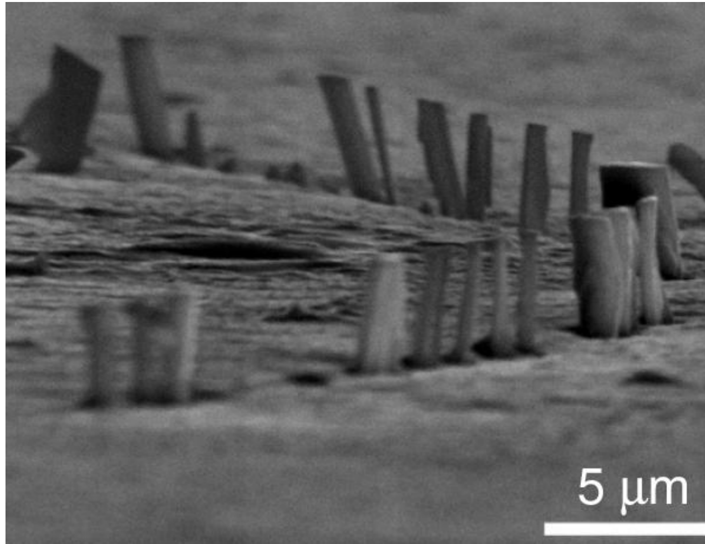


Figure 1.17: SEM image of SiC filament precipitates, after [73].

A recent EBIC study of grain boundaries in mc-Si [74] reveals that Fe contamination at the boundaries and small-angle boundaries are the two main causes of grain boundary-related recombination. The work concludes that clean, large-angle GBs are essentially electrically in-

active and therefore controlling the growth to favour these is crucial to good cell performance. It is interesting to note that small-angle grain boundaries are essentially rows of dislocations, so this study shows how detrimental dislocations are to solar cell performance.

Dislocations

Recombination of electrons and holes at dislocations in silicon has been acknowledged for decades [75, 76], but it is very difficult to mitigate their effect on cell efficiency as they are grown into the material on solidification. Dislocation densities of up to 10^6cm^{-2} are typical in cast mc-Si [77]. Figure 1.18 shows a typical dislocation pattern for a sample of wafer from a cast mc-Si ingot, revealed by chemical etching. Localised regions with dislocation densities of over 10^8cm^{-2} exist in cast ingots [78], and these have been shown to highly detrimental recombination sites [79]. Due to all regions of a solar cell being linked electrically, localised "bad" regions can dissipate power produced in the better performing areas [80] even after mitigation techniques such as gettering and passivation are applied. Counter-intuitively, there is clear evidence that dislocations themselves are not responsible for recombination; EBIC studies have shown that clean dislocations are electrically inactive [81]. It is only when decorated that dislocations become active and in mc-Si dislocations tend to be decorated by transition metal impurities.

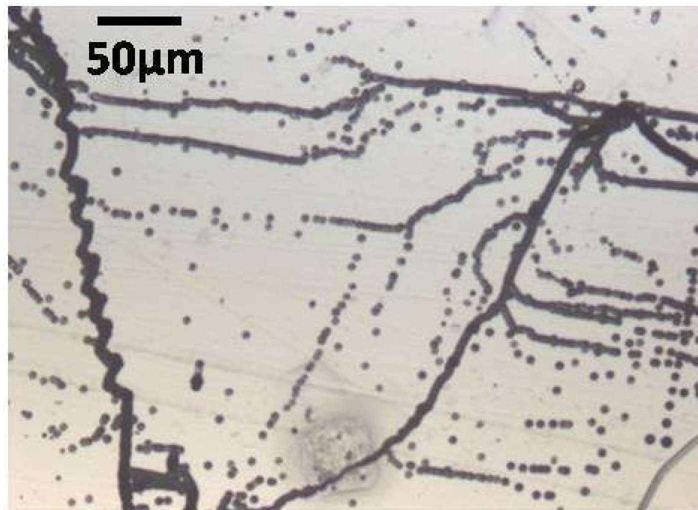


Figure 1.18: Optical micrograph of Secco etched mc-Si specimen, after [82].

Impurities

Metals are know to exist in commercial mc-Si material in concentrations as high as 10^{14}-10^{16} cm^{-3} [33, 83, 84], with large variations depending on the feedstock quality and the method of processing [85]. These impurities lead to reduced cell performance via a range of mechanisms, including direct shunting [86, 87], increased leakage current [88, 89, 90] and bulk recombination [91, 92]. The extensive study by Buonassisi *et al.* [85] of metal-rich precipitates identified two main types: metal-silicide nanoprecipitates (sub-200nm diameter) at or along grain boundaries and found in material from the edge region of ingots; and larger (several microns in diameter) metal oxide particles found dispersed within grains and at grain boundaries. The metals contained in the former tend to be faster diffusing species such as copper, nickel, and cobalt (and also the medium-rate diffuser iron) and are only observed in the most silicon-rich form of the available intermetallic compound for a given system (e.g. $NiSi_2$ or $FeSi_2$). This suggests that the nanoprecipitates in mc-Si are formed through precipitation of initially dissolved metal atoms. The larger oxide particles tend to consist of slower diffusing species such as titanium, and again iron. Most oxidised metal compounds are not expected to form within silicon under equilibrium conditions [93]; this suggests that the larger particles are inclusions - incompletely dissolved foreign particles introduced into the melt from low quality feedstock. Figure 1.19 shows diffusion and solubility data for a selection of impurities found in mc-Si.

When ingots are cooled rapidly from the melt (and in order to increase production rates this is increasingly important) a significant fraction (up to 1%, a concentration of 10^{12} cm^{-3}) of slower diffusing species such as iron and titanium may be incorporated into the material as highly detrimental supersaturated interstitial point defects [95]. These are much more difficult to image directly - often their electrical effects are observed but the elemental mapping techniques are unable to detect the very small concentrations of impurity atoms that are present outside of the aformentioned precipitates; see [85] for an example using a comparison of XBIC and XRF performed on the same regions of intentionally contaminated float-zone silicon (FZ-Si) samples. Recombination is observed in areas with no detectable impurities and cannot be attributed to crystal defects as these exist at extremely low levels in FZ-Si,

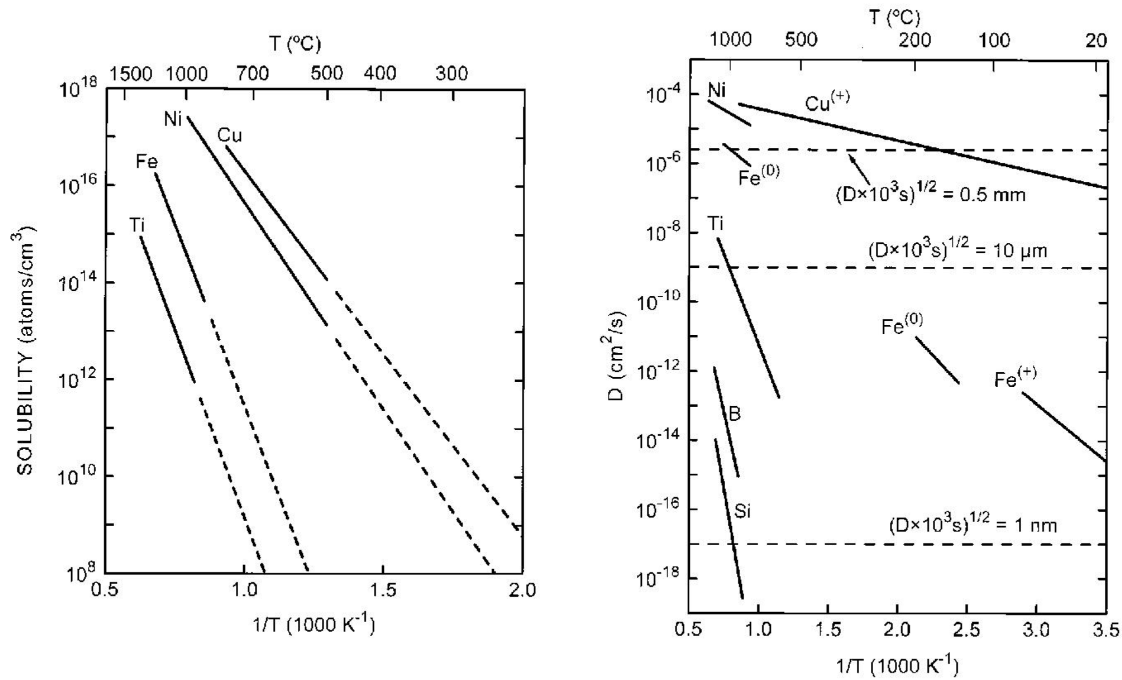


Figure 1.19: Plot of diffusion coefficients and solubilities of interstitial transition metals in Si and their variation with temperature, after [94]

suggesting that regions of mc-Si free of crystal defects and precipitates may still suffer from low lifetimes if ingot manufacture is not carefully controlled.

In addition to metallic impurities, oxygen related extended defects, or oxide precipitates, are an additional recombination centre that are known to cause reduced minority carrier lifetime [97], and therefore lower device performance.

1.3.3 Gettering

Gettering is defined as the process of removing device-degrading impurities such as transition metal atoms and precipitates from the active regions of the wafer. It can be performed during crystal growth or in subsequent fabrication processes, and by either intrinsic or extrinsic mechanisms. Gettering is a vital part of any mc-Si solar cell production process as without it the efficiency of the cells would be too low for them to be commercially viable.

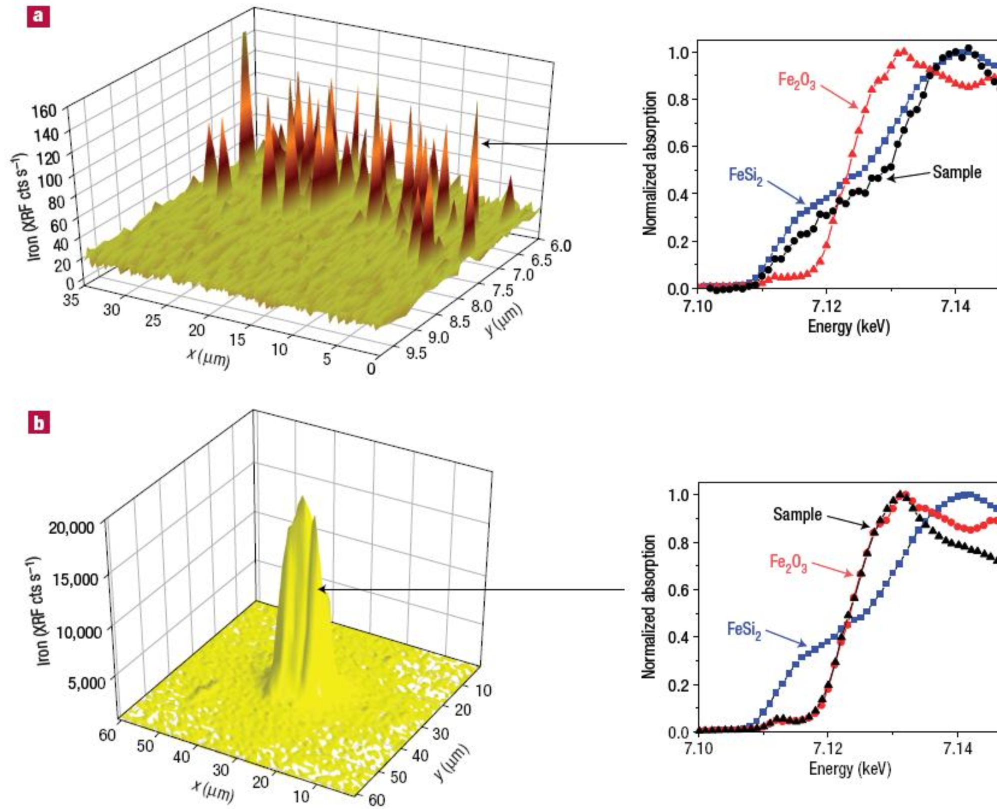


Figure 1.20: Examples of XRF maps for iron in mc-Si showing (a) small $FeSi_2$ nanoprecipitates and (b) large Fe_2O_3 inclusion, with corresponding X-ray absorption spectra, after [96].

Intrinsic gettering

Intrinsic mechanisms use defects already present in the silicon as sinks for impurities, effectively collecting harmful species in locations where they can do the least damage to device performance. This is activated either by annealing the material [98] or neutron irradiation [99] but is mainly used for Czochralski-grown silicon as the results are best when higher concentrations of oxygen are present. Work by Buonassisi *et al.* [95] has developed a novel intrinsic gettering technique for mc-Si (originally outlined by Plekhanov *et al.* [100]) where anneals are used to modify the transition metal distributions such that bigger, more dispersed precipitates are created at the expense of highly detrimental interstitial point defects. The process is yet to be optimised, but initial μPCD carrier lifetime measurements on samples having undergone 30 minute, 500°C anneals (performed after phosphorus emitter diffusion) are promising,

giving a 2.2% relative efficiency increase. Other time and temperature regimes may be needed to getter elements successfully with different diffusion behaviour. Grain boundaries in mc-Si can also be used as impurity sinks [100, 101, 102], recent work by MacDonald *et al.* using photoluminescence mapping confirms this for iron impurities [103].

Extrinsic gettering

Extrinsic mechanisms require some external means to alter the impurity distribution of the silicon. Potential impurity sinks are introduced either by physical damage (laser irradiation [104], ion bombardment [105] and abrasion [106]), or by additional chemical species such as phosphorus or aluminium layers, the latter being the choice for current commercial cell designs. Chemical gettering is typically performed by depositing the P- or Al-containing material on the back side of the cell and annealing at temperatures sufficient to cause diffusion of the unwanted impurities to the gettering sites. Phosphorus is typically applied by spinning a $POCl_3$ layer onto the wafer and heating at around 900°C [107]. The phosphorus atoms diffuse into the Si bulk and cause local defects in the lattice that act as trapping sites for impurities. Si-P precipitates are also formed and these are useful in removing nickel atoms [108]. The mechanism defining the interaction between crystalline defects, interstitial metal defects and precipitates is highly complex during phosphorus-diffusion gettering treatments and it is reported that one of the key factors is whether the impurities are bound to the dislocations [109]. This suggests that even when considering impurities, the presence of dislocations is important in defining the material properties.

Aluminium is applied by locally alloying the wafer with aluminium and annealing [110], this can be combined with the Al-BSF fabrication step mentioned in Section 1.3.4. An explanation of aluminium gettering of iron in terms of a Si-Al-Fe ternary phase diagram [111] has enhanced understanding of optimal gettering conditions. This is especially important for mc-Si as it is more sensitive to the annealing conditions used in gettering than single crystal material [112], as the higher concentration of impurities can lead to unwanted precipitation or dissolution of some species, changing device performance in a detrimental way.

A possible mechanical method uses the unavoidably created stresses and sawing damage

caused by the wafering process to generate dislocations to getter impurities [113]. The process involves annealing after wafering so that impurities can diffuse into the damaged regions and then removing the saw damage, and whatever metal atoms it has collected, with a planar etch.

1.3.4 Passivation

When applied to solar cells, the term passivation describes reducing the electrical activity of defects. At surfaces and at grain boundaries silicon atoms are incompletely bonded to their neighbours, creating a high density of dangling bonds. These introduce trapping states into the band gap, which in turn reduce the collection efficiency [114]. For a typical silicon solar cell, there are three passivation steps during manufacture: front surface, bulk, and back surface.

Front surface passivation techniques typically involve growth or deposition of a dielectric film in order to lower the surface state density. Thermal oxidation of a silicon surface at around 1000°C was the standard method for many years but the high temperatures needed can adversely affect the underlying device structure, and are also undesirable when energy cost and throughput are considered, so the technique has generally been replaced [115]. Plasma enhanced chemical vapour deposited silicon nitride [116] and evaporated titanium dioxide films [117] both produce good results, lowering surface recombination velocities and thus improving cell performance without the aforementioned downsides arising from high-temperature oxide generation. In addition these surface films act as anti-reflective coatings.

Bulk passivation of wafers is achieved by rapid annealing in hydrogen atmospheres at around 400°C [118]. Atomic hydrogen bonds to the dangling bond sites and this can reduce the trap state density by a factor of three [119]. An alternative method of introducing hydrogen into the bulk is by annealing at 600-800°C after the silicon nitride coating is deposited. The plasma enhanced deposition causes residual hydrogen from the silane and ammonia feedstocks to be contained in the coating and this diffuses into the bulk on annealing, leading to increased carrier lifetimes [120].

The most commonly used back surface passivation technique for p-type wafers is the fab-

rication of a p-p$^+$ junction [115]. The electric field associated with such a junction passivates the surface by repulsion of minority carriers. The standard material used is aluminium, usually applied by screen printing of an Al-containing paste into the correct pattern and firing at several hundred degrees to diffuse in the Al, then known as the aluminium back side field (Al-BSF) (for a detailed example of the Al-BSF production process see [58]). As solar cells become thinner the screen printing technique may cause issues with wafer warping, possible alternative techniques include plasma enhanced chemical vapor deposition of hydrogenated amorphous silicon (PECVD a-Si:H) layers [121] and boron diffusion [122].

1.4 Summary

Despite many competing renewable energy technologies, the potential offered by solar energy is enormous and, for energy security and environmental reasons, it should be exploited more fully than at present. Although marginally less cost-effective at the moment than some of these competing technologies, photovoltaic systems based on mc-Si cell technology are a promising option for providing reliable, clean energy to a mass worldwide market. Combining low cost fabrication with improved efficiency is the key aim of current research. Many of the issues with the technology and the material itself have been overcome, but the recombination of carriers at (decorated) dislocations remains a major problem and is the reason this project is being undertaken. The next Chapter will look at both the way this project intends to improve solar cell performance, and some alternative ideas.

Chapter 2

Project concept and relevant literature

The work in this project grew out of an idea to solve the main problem that causes reduced efficiency in mc-Si based solar cells - recombination at dislocations. If the dislocations could somehow be physically removed without too much incidental damage to the rest of the wafer, would this lead to increased cell performance? Designing the most effective way to remove dislocations became the initial aim of the project. In this Chapter various existing or proposed methods of improving mc-Si material performance are looked at, followed by a description of the method that will form the basis of this project and a description of some relevant literature.

2.1 Minimising dislocations in mc-Si for solar cells

2.1.1 Modified casting

The optimum way to produce mc-Si with a lower dislocation density is to somehow cast it with fewer defects in the first place, but this is not a simple challenge. Much research has been done on improving the casting process, but a majority of this is incremental progress in industry and is not generally of scientific interest. In this Section, some novel "defect engineering" processes are described which aim to use an improved understanding of the

fundamental materials science to improve substrate performance.

An in-situ analysis of the casting process by Fujiwara *et al.* [70] has lead to the same group demonstrating both "structure-controlled" mc-Si growth [123] and more recently "floating cast" mc-Si [124]. The former uses careful control of the solidification conditions to promote dendritic growth, which in turn leads to large, oriented grains forming in the ingot. An electron backscatter diffraction (EBSD) map illustrating this is shown in Figure 2.1. The latter uses similar control of the melt to suppress nucleation everywhere except the top-centre, leading to the crystal forming in reverse compared to conventional methods and growing out towards the walls of the crucible. The benefits over regular cast mc-Si are threefold. First, the average grain size is larger due to the reduced number of nuclei. Reduced contact between the solid crystal and the crucible wall accounts for the other two improvements - lower contamination of diffused impurities and fewer crystal defects (including dislocations) due to decreased residual strain. The claim about reducing crystal defects is not backed up by any measured fall in dislocation densities, but there are electrical testing results showing improved performance when real cells are made from the material. Fill factor increased from 0.70 to 0.75 for cells made in the same way from standard and floating cast material respectively, as shown in Figure 2.2.

Another novel material is Mono^2 silicon, produced by BP Solar, which is described by its developers as "Single crystal silicon... produced using a cast-in-place process usually used for multicrystalline ingot production" [125]. Electrical testing data have shown improved efficiencies compared with mc-Si wafers, which is attributed to the removal of grain boundaries and reduced dislocation density of the Mono^2 material [126]. This improvement is shown in Figure 2.3, which contains graphs comparing efficiencies of conventional mc-Si and Mono^2 materials. In addition, the pseudo-single crystal nature of the Mono^2 material provides advantages relating to reflectivity. The ingots are grown as (100) crystals which allows the wafers to be etched using standard alkaline/alcohol procedures [127], which do not work with the various crystallographic orientations observed on the surface of mc-Si wafers. Using a sodium hydroxide/isopropyl alcohol etch to produce a uniform pyramidal texture improves efficiency by another 0.5% [126]. Due to the commercial sensitivity associated with the product, there

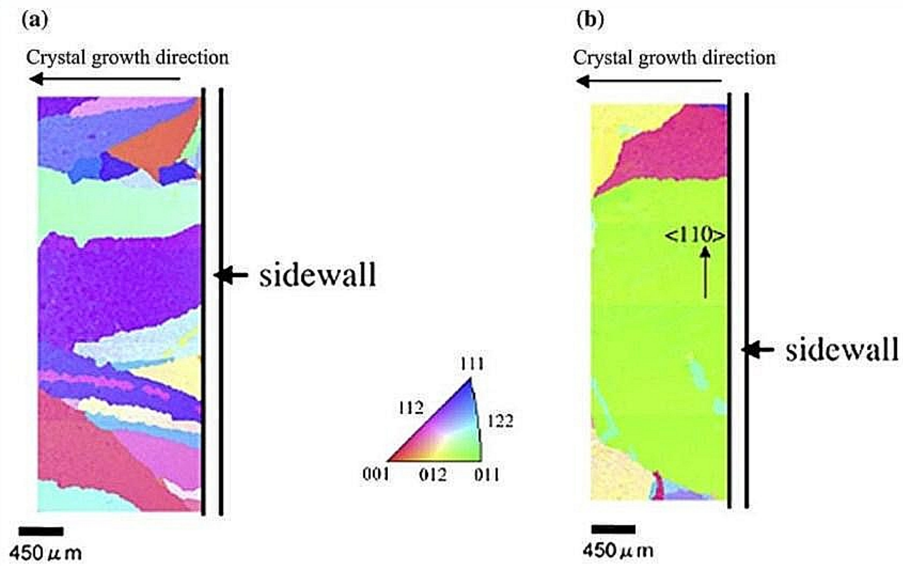


Figure 2.1: EBSD orientation maps of samples cooled at: (a) 1 K/min and (b) 50 K/min, after [70]. The increased cooling rate in (b) leads to rapid initial growth along the crucible wall that in turn leads to growth of large, oriented grains.

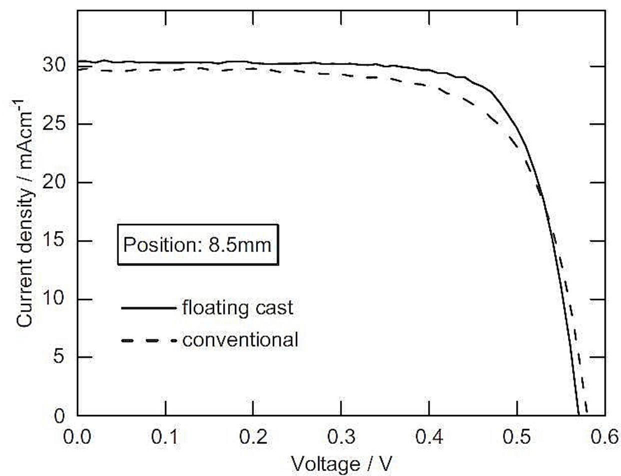


Figure 2.2: I-V curves comparing cells made from conventional and floating cast material (both wafers 8.5mm from bottom of ingot) (after [124]).

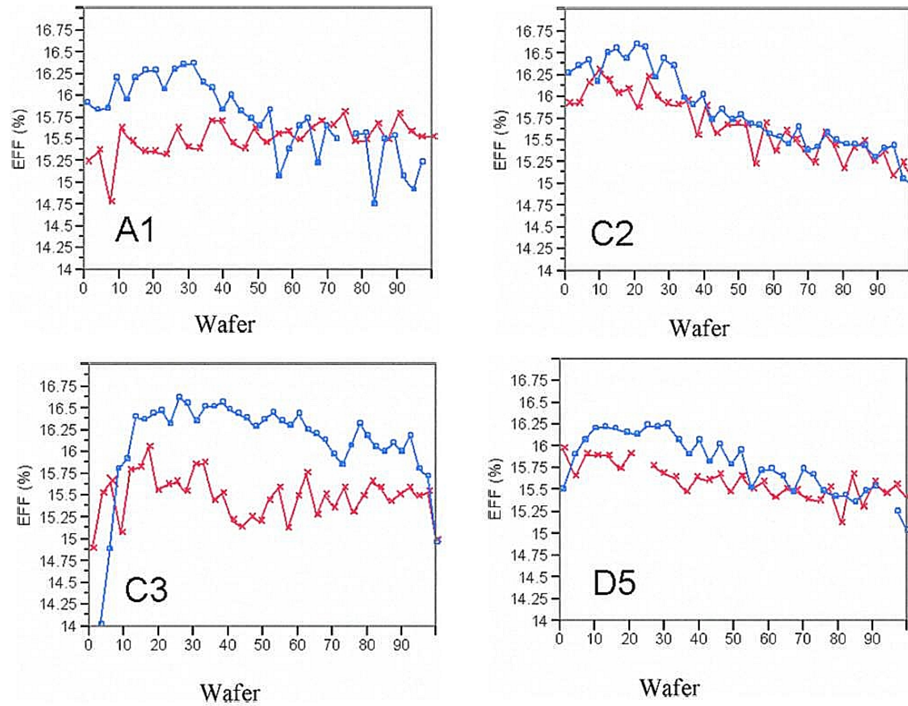


Figure 2.3: Cell efficiency results as a function of wafer position (0 is bottom of brick, 100 is top) for four multicrystalline (red) and Mono^2 (blue) bricks processed identically using isochemical texturing (after [126]).

is a lack of further published information available for Mono^2 silicon.

Despite promising research in the area of modified casting, it is clear that wafers produced by modified casting methods are a long way from achieving a significant share of the silicon solar cell market. Many expensive new ingot growing facilities were commissioned during the recent rapid growth of the silicon PV market and it would therefore be counter-productive to move to a new method of casting, with the associated expense of setting up new production equipment. It may instead make more economic sense to concentrate on post-growth treatments that use silicon cast using current technology, such as the methods in the next Section and this project.

2.1.2 High temperature annealing

An alternative method for minimising the detrimental effect of dislocations on cell performance is to remove them *after* growth. One such approach that has been trialled is the use

of high temperature annealing [80]. This technique relies on very high temperature ($\geq 0.8T_m$) treatments of mc-Si wafers such that dislocation motion is unconstrained by glide planes. This is thought to lead to pairwise annihilation of dislocations and a corresponding reduction in overall dislocation density. Figure 2.4 shows qualitatively the change in dislocation density after the application of the annealing treatment. The technique was further developed by controlling the stress applied to the material [128].

There is as yet no evidence that wafers modified in either fashion have been used to produce finished cells with improved efficiencies or even wafers with improved minority carrier lifetimes. At the high temperatures required, the solubilities of harmful impurities is so high (see Figure 1.19) that it will be difficult to process wafers sufficiently cleanly for this process to be viable on a large scale. Further, the testing has been limited to string ribbon mc-Si wafers, which are not widely used in solar cell production. The dislocation types in this ribbon-grown material are likely to be substantially different to those in cast mc-Si and it is therefore unclear whether this method will work at all in conventional cast material. Even if it does, the cost of running furnaces at over 1300°C for the long time periods required in a production line may be prohibitive.

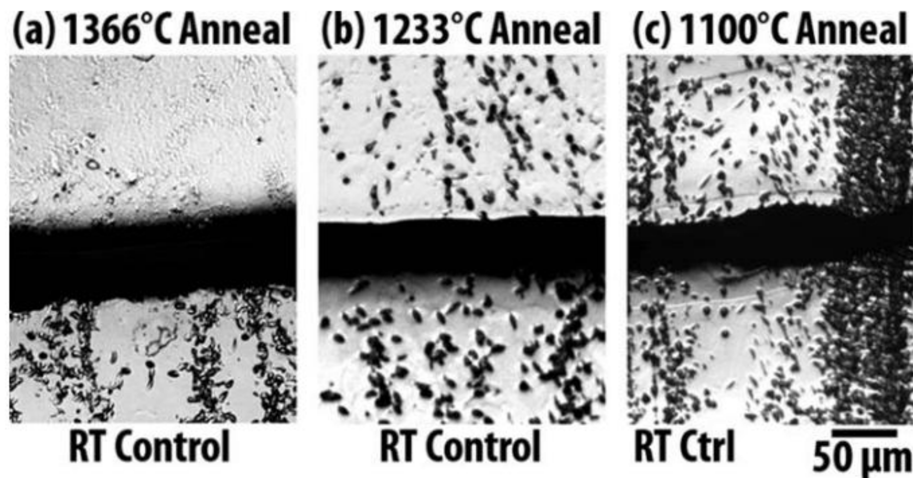


Figure 2.4: Dislocation etch pit images of three ribbon mc-Si samples annealed for 6 hours at (a) 1366°C, (b) 1233,°C and (c) 1100 °C. The lower pieces (adjacent pieces of material cleaved from the same wafer) are the corresponding room temperature unannealed control samples. A significant dislocation density reduction is observed at 1366°C, but hardly any at 1100°C (after [80]).

2.2 Project concept

2.2.1 Overview

The aim of this project is to develop a low cost method to remove dislocations from mc-Si after growth. It is well known that various chemical solutions attack, or etch, silicon [129] and that in some cases this attack is increased at crystalline defects in the material - this is the basis for etching as a technique for identifying defect distributions [130, 131, 132, 133, 134]. These "defect revealing" etches were designed purely for the purpose of quickly and simply identifying the defects present in a sample. If the selectivity of this chemical attack could be increased such that only the material directly adjacent to the dislocation is attacked then it maybe be possible to "etch out" dislocations to a certain depth and leave the bulk of the wafer behind. In this case the pits would perhaps be better referred to as "tubes". The schematic in Figure 2.5 illustrates the difference between the relatively shallow pits produced by a typical existing etch and the deep, narrow tubes that are the aim of this project. Filling in the tubes would result in a wafer with a lower dislocation density than an as-cast wafer. Assuming that dislocation removal and subsequent passivation of the newly created surface has the positive effect on minority carrier lifetime that is predicted, a final cell with corresponding better performance may be produced.

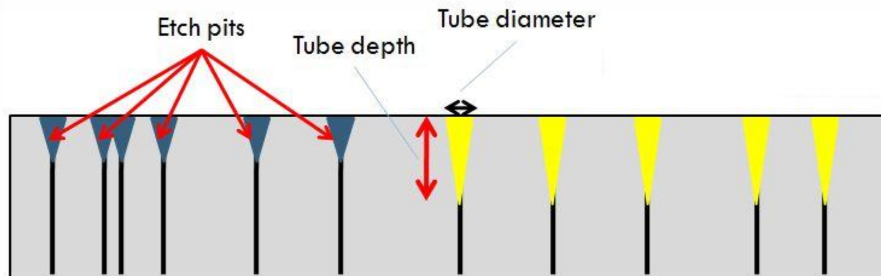


Figure 2.5: Schematic showing cross-section of mc-Si sample. Existing defect etching produces pits shown on the left in blue. This project aims to develop an etch that produces tubes as shown on the right in yellow.

Deciding how deep the tubes need to be can be estimated by considering the light absorption behaviour of silicon. Figure 2.6 is a plot of absorbed usable photon fraction against silicon thickness. It shows that approximately 95% absorption is reached at a depth of 100μm

so focussing on removing dislocations from the top half of a typical wafer (commercial cells today are around 200μm thick [135]) should be sufficient for improved performace, assuming the technique is successful. Existing etch processes are not optimised to produce tubes this deep, therefore it will be necessary to modify the compositions or the conditions that have been developed previously.

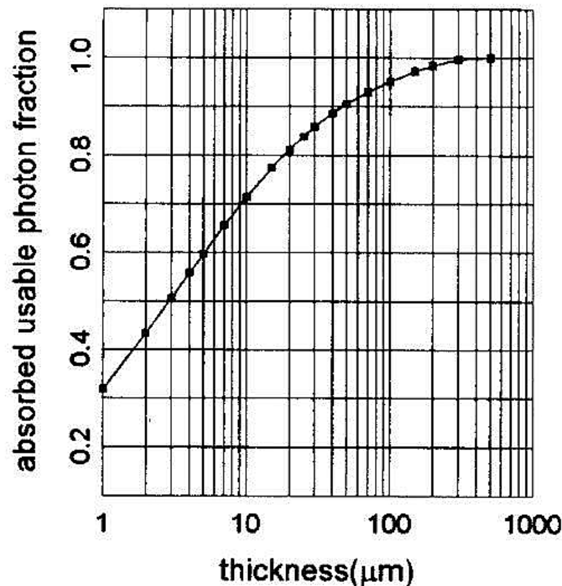


Figure 2.6: Absorbed solar photon fraction as a function of silicon thickness for AM1.5 illumination (after [136]).

There are many advantages to using a chemical etch compared with the other methods. First, chemical etching is already one of the process steps in solar cell manufacturing production lines, the surface textures that the mc-Si wafers require (to enhance light absorption) are applied by this method. Adding an extra, similar step would not require huge investment in new equipment or much of an increase in expertise. Like the high temperature anneals, this is a post-growth processing solution, but it has the advantage of being performed at close to room temperature. Therefore any transition metals that may come into contact with the material during handling are insoluble and will not dissolve into the wafer, ensuring no additional contamination from the process. The possible disadvantages are relatively minor, the chemicals involved are extremely toxic and although the industry in general is very familiar with the risks associated with handling large quantities of hydrofluoric acid, this would be an

unwanted additional consideration. Further, many defect etches are based on systems with either Chromium (III) or (VI) as the oxidising agent, these are also highly toxic and therefore undesirable unless no alternative can be found.

2.2.2 Challenges to be overcome

For dislocation removal etching to be a useful process in mc-Si solar cell production, it is necessary to overcome many challenges. The initial challenge is to develop an etching process which removes dislocation cores sufficiently deep into the material whilst only removing a minimal amount of the surrounding bulk material. Should this be achieved, the other challenges that need to be overcome include:

1. Can precipitates on the dislocations also be removed by the etching process?
2. After etching, can the additional surface easily be passivated?
3. Is the minority carrier lifetime of the material improved by the process?
4. Can a higher efficiency solar cell be produced from the etched wafers?

If these are all overcome, the process will provide a strong alternative to the modified casting and annealing procedures.

2.2.3 Scope of this thesis

This project will concentrate mainly on the initial challenge of developing a process to remove dislocations from mc-Si. The idea of removing dislocations by etching, rather than just highlighting where they intersect a surface, is highly novel and therefore there is very little previous work to use as a starting point. The issue of precipitates will not be systematically investigated in its own right, but observations can be made during the planned scanning electron microscopy that will be carried out on samples after etching. Evidence from this should give a strong indication as to whether precipitates block the etching reaction, and further work can be planned as necessary.

2.3 Etching

As etching is the focus of the novel processing method explored in this project, it is now necessary to review briefly the literature in this research area. Etching is a very important technique in silicon processing, and can be broadly separated into two categories - dry and wet. Dry etching uses reactive ions to remove material, micromachining the silicon into whatever shape is required for the device. Ions with different selectivities and anisotropies are used to control the shape and extent of the etching. This is not a relevant technique to this project and will not be discussed further. Wet etching, or chemical etching, uses various chemical solutions to dissolve material. Chemical etching can be further subcategorised into bulk etching and preferential (or defect revealing) etching - based on what material is attacked by the etchant. Anodic etching is a further subset of wet etching where the action of chemical reagents is enhanced by passing current through the silicon sample.

In the integrated circuit fabrication industry, etches that remove bulk material are used to accurately shape the microscopic features of devices [137] and in solar cell production, similar etches are used to give a favourable surface texture to the wafer after sawing [138]. Defect etching is a useful characterisation technique, as it allows the grain structure and dislocation density of a wafer to be elucidated from a very quick experiment. This occurs due to the silicon atoms at, or adjacent to, crystal defects such as dislocations and grain boundaries being oxidised preferentially by the etchant. A summary of the various possible reasons for this increased local etching rate is provided by Lehmann [139], and reproduced here:

1. The higher chemical energy of the elastic strain field present around a dislocation.

2. A high impurity concentration caused by gettering of impurities by a dislocation.

3. An impurity that has formed a precipitate, for example a metal silicide.

4. A different doping density.

5. Bubbles sticking randomly at the surface.

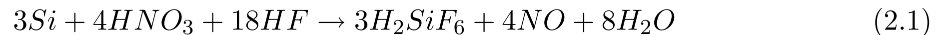
Some of the most common defect etches, and their properties, are detailed in Table 2.1.

Name	Etchant	Etch rate (μ/min)	Notes	Reference
Dash	1 HF: 3 HNO_3: 10 CH_3COOH	0.13 (100) 0.005 (111)	Works on (100) and (111) planes.	[132, 140]
Sirtl	0.3 CrO_3: 0.36 HF (100%): 1 H_2O	3.0	Works well on (111).	[133]
Shimmel	1 CrO_3 (1M): 2 HF: 1.5 H_2O	1.7 - 3.2	Sensitive to doping and agitation, works on (100).	[131]
Yang	1 CrO_3 (1.5M): 1 HF (49%)	1.5	Works on (100), (110) and (111).	[134]
Secco	1 $K_2Cr_2O_7$: 2 HF (49%)	1.5	Works on (100), needs agitation.	[141]
Sopori	36 HF (49%): 20 CH_3COOH (glacial): 1-2 HNO_3	5-20	Good for poly-Si.	[130]

Table 2.1: Table of preferential etches used in defect characterisation, adapted from [142].

2.3.1 Mechanisms of etching

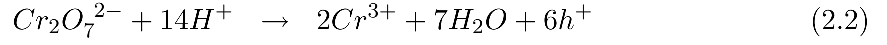
The mechanisms of chemical etching are well understood and have been studied for over 50 years. Research into the primary bulk etch, based on the HF, HNO_3 and CH_3COOH system and often referred to as a "planar etch", started with Robbins and Schwartz study of etch rates [143, 144, 145]. Their key hypotheses were the existence of a two-step etching process (oxidation of Si then dissolution of said oxide) and the importance of diffusion to the mechanism. Further, they calculated activation energies of 0.18eV for HNO_3 rich compositions and between 0.43 and 0.87eV for HF rich compositions. For the specific composition 8%HF (40%), 75%HNO_3 (69%) and 17% CH_3COOH (glacial) an activation energy of 0.28eV has also been reported by Murphy [146] for the following etching reaction:



$$3Si + 4HNO_3 + 18HF \rightarrow 3H_2SiF_6 + 4NO + 8H_2O \tag{2.1}$$

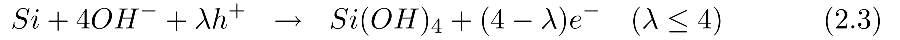
Studies specific to defect etches have also been performed. Seo *et al.* [147] analysed the HF and $K_2Cr_2O_7$ containing system. This work sets out the mechanism by which acid/oxidising agent based etches react with silicon and reports an activation energy of 0.34eV for single

crystal Si on a (100) orientation surface. There are two possible reaction routes, both starting with the oxidising agent reacting with H^+ ions to form holes on the silicon surface, depending on the HF concentration regime, as shown below.



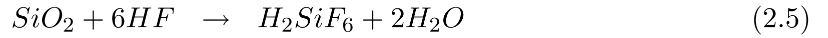
$$Cr_2O_7^{2-} + 14H^+ \rightarrow 2Cr^{3+} + 7H_2O + 6h^+ \quad (2.2)$$

For low concentration of HF,



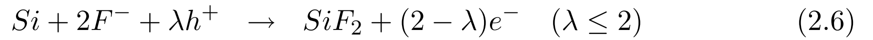
$$Si + 4OH^- + \lambda h^+ \rightarrow Si(OH)_4 + (4-\lambda)e^- \quad (\lambda \leq 4) \quad (2.3)$$

$$Si(OH)_4 \rightarrow SiO_2 + 2H_2O \quad (2.4)$$



$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (2.5)$$

For high concentration of HF,



$$Si + 2F^- + \lambda h^+ \rightarrow SiF_2 + (2-\lambda)e^- \quad (\lambda \leq 2) \quad (2.6)$$

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2 \quad (2.7)$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6 \quad (2.8)$$

This suggests that the etching rate is likely to be dependent on the hole generation that takes place on the silicon surface, and further that this process must somehow be enhanced at defects for the defect revealing etches to be successful. It should be noted at this point that controlling the light exposure of samples as they undergo etching is important as this is very likely to affect hole generation, attention will be paid to this in the experimental method of this project. Further work on potassium dichromate etching systems by Gabouze *et al.* [148] reports a similar mechanism for the etching of multicrystalline silicon, but no study into the increased etching rates specifically at the defects has been performed.

2.3.2 Anodic etching

Research into the behaviour of silicon electrodes in hydrofluoric acid based electrochemical cells has also been ongoing for around half a century [149, 150, 151]. Memming and Schwandt [152] demonstrated the mechanisms involved in the anodic dissolution of silicon and reported results from polarisation experiments. Typical polarisation curves for silicon

in a high-concentration HF electrolyte are shown in Figure 2.7. This graph has three distinct regimes: anodic, cathodic illuminated and cathodic non-illuminated. In the anodic regime, the current density increases exponentially with increasing potential. Memming and Schwandt postulated that this behaviour is due to the thermal activation required to cause SiF_2 groups to "swing away" from the silicon atom to which they are bonded [152]. This mechanism is initiated by holes that are attracted to the surface by the applied potential and become trapped, weakening adjacent Si-Si bonds. Further evidence for this is provided by the discovery of a similar mechanism in germanium by Beck and Gerischer [153]. The two cathodic curves are saturation currents and result from the discharge of protons, as evidenced by hydrogen gas evolution. The increase under illumination shows that in this regime the current is limited by electron diffusion.

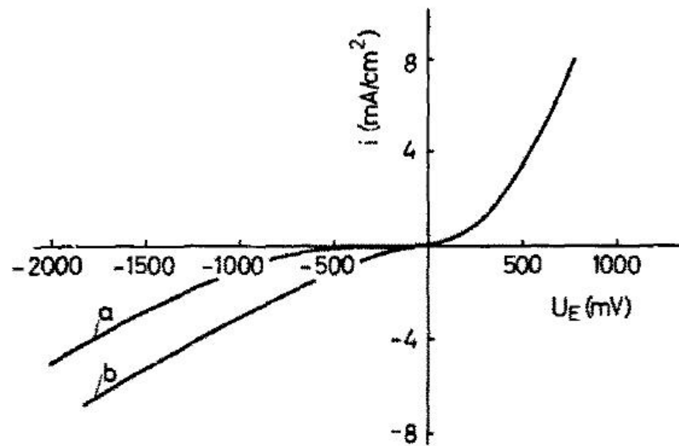


Figure 2.7: Current density vs. electrode potential for a p-type (1Ωcm) single crystal silicon electrode in 10M hydrofluoric acid and 0.5M ammonium fluoride: a) measured in the dark, b) under illumination, after [152].

From the previous Section, it is clear that the oxidising agent is only required as the first step in the process as a means to generate holes (Equation 2.2). If this can instead be done by biasing the silicon, etching can be performed in a more controlled fashion by applying potentials, and defect delineation similar to that mentioned in Table 2.1 can be achieved. This process is known as "anodic" etching, and was developed for silicon in the 1980s by Föll [154]. In summary, an electrochemical cell with silicon as the anode and a water, HF

and ethanol electrolyte is constructed. Different etching behaviour is noted when the applied voltage is varied, Figure 2.8 shows an example. The advantage over regular chemical etching is that only electrically active defects are etched at low applied potentials (-0.5 to +0.5V); this is useful in determining which defects are having an important impact on cell performance.

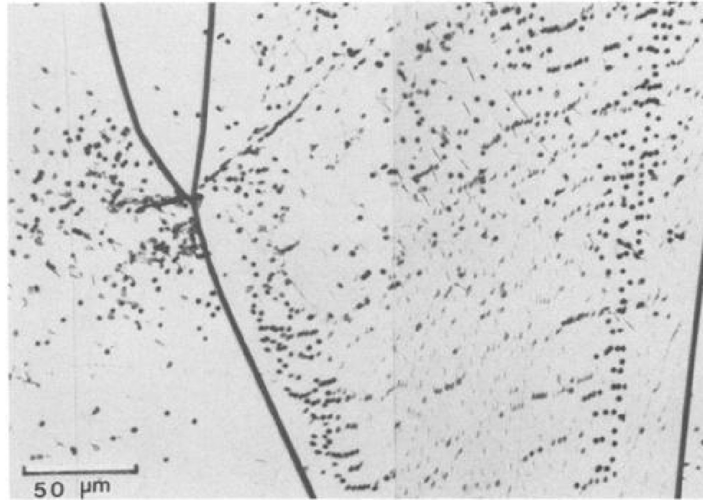


Figure 2.8: Optical micrograph of anodically etched mc-Si (40 minutes at 0V bias), after [154].

The explanation for this behaviour is not entirely clear. Föll suggests that the enhanced rate of dissolution at defects arises due to an effective shift in the polarisation curve at the defect sites [154]. This is most marked at dislocations and grain boundaries, which are strongly etched, but also noticeable at twin boundaries, which are only weakly etched. The suggested comparative current-voltage curves are shown schematically in Figure 2.9.

A possible issue with the quantitative aspect of Föll's results is that the potential in the cell was not controlled in the same way as in Memming and Schwandt's work. They used a reference electrode in addition to the platinum gauze electrode and silicon anode (*i.e.* the sample), and additionally kept the oxygen content of the electrolyte at a minimum by passing purified nitrogen through it. Föll uses a simpler cell with only the platinum and silicon electrodes, and it is possible that the electrical measurements taken at the terminals are not equal to the true values experienced by the sample. Oxygen evolution at the platinum electrode may occur, drawing an additional, varying current for a given voltage, leading to errors in the current-voltage characteristic.

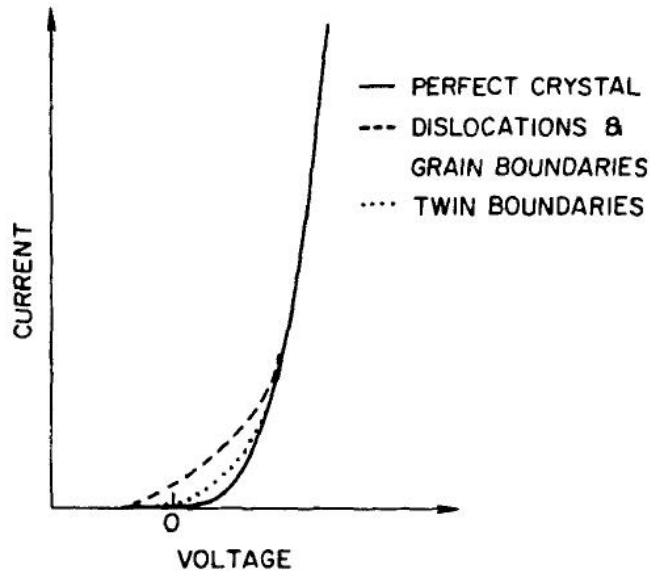


Figure 2.9: Schematic plot of current-voltage characteristic for various defects compared to bulk silicon, after [154].

2.4 Summary

This Chapter has reviewed some existing material improvement methods and introduced the idea at the centre of this project, dislocation core removal by etching, and how it could lead to improved mc-Si for solar cell applications. The advantages and disadvantages of this, and the various alternative processes are discussed, along with the feasibility of scaling them up for commercial use. Dislocation core removal depends strongly on chemical etching, so literature in this field was reviewed, with key mechanisms and conclusions highlighted. The next Chapter sets out which experimental methods will be required in this project and why.

Chapter 3

Experimental methods

This Chapter discusses the basic techniques used for some of the measurements made during the project. A more detailed explanation of the etch depth measurement procedure and how the final version was arrived at is contained in Chapter 4.

3.1 Sample preparation

This section discusses the steps taken from selecting a material to work with to preparing it for testing.

3.1.1 Material used

The silicon used in this project was intended to be representative of typical commercial mc-Si wafer that would go on to be processed into solar cells. To fulfil these requirements wafers were provided by both PV Crystalox and REC ScanWafer, in the standard size of 156mm square. The Crystalox wafers had been treated by a proprietary chemical etch and were 300μm in thickness whereas the REC material was received as-sawn and 200μm thick. The difference in surface finish was removed by polishing so not an issue during the etching process; the starting point for all etching was a flat, highly polished surface. A dislocation density of between 10^4 and 10^6 cm^{-2} is typical for these wafers.

Initially, wafers from Crystalox in the standard size of 156mm square were used for pre-

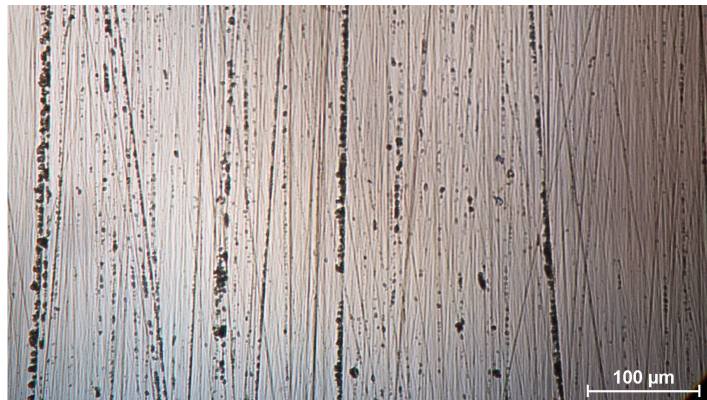
liminary experiments. The supplier was later changed to REC who provided thinner wafers, matching the current commercially used material more accurately. Sample size was not important for initial tests, although the technique was intended to be applicable to commercial wafer production. The requirements were that the samples be small enough to handle easily and reduce both material and chemical waste but large enough for a range of grain orientations and microstructural features to be present in a single sample. 15x10mm was decided on for chemical etches. The equipment for anodic etching and lifetime measurements required larger minimum sample sizes, 30x30mm and 50x50mm respectively.

3.1.2 Grinding and polishing

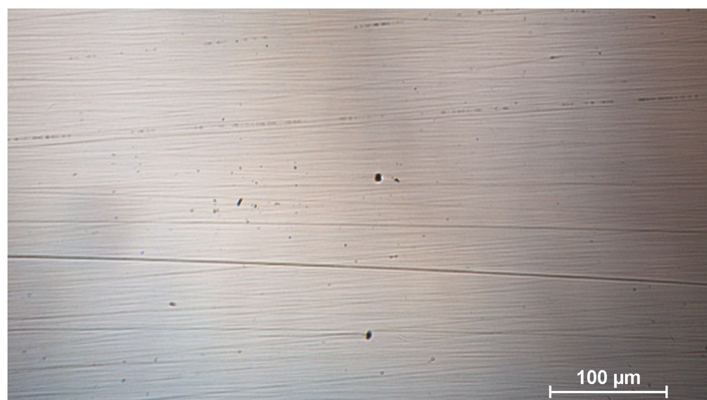
To make etched dislocations easy to observe and to provide an initial flat reference surface, samples were polished. It is not envisaged that this would be necessary for a commercial process, but made experimental observation considerably easier. The equipment used were Kemet lapping wheels and polishing was performed by hand, with water as the lubricant for grinding and Syton polishing and Kemet GW2 lubricant for diamond polishing. The steps, the results of which are shown in the series of optical micrographs in Figure 4.2, were:

1. Samples mounted on glass discs using wax.
2. P2500 grit grinding for 2 minutes.
3. 6μm diamond polish, performed at 90° to previous step until grinding marks are not visible, plus additional 4 minutes polishing to remove underlying damage.
4. 1μm diamond polish, again at 90° to previous step until all 6μm marks are removed, plus additional 4 minutes.
5. $\frac{1}{4}\mu$m diamond polish, again at 90° to previous step until all 6μm marks are removed, plus additional 4 minutes.
6. Chemo-mechanical Syton polishing until all visible surface damage removed, then additional 4 minutes.

(a) Optical micrograph of silicon surface after P2500 grinding step.



(b) Optical micrograph of silicon surface after 6μm polishing step.



(c) Optical micrograph of silicon surface after 1μm polishing step.

Figure 3.1: Series of micrographs showing various stages of sample preparation.

3.1.3 Wafer dicing and cleaving

A Loadpoint MicroAce 3 wafer dicer was used for dicing mc-Si samples, with the following settings:

- Feed rate 5 mm/s
- Spindle rate of 10k rpm
- Diamond saw blade

Any single crystal material used during testing was cleaved to size. This involves scoring the surface along a [110] direction using a diamond-tipped scribe and carefully snapping along the mark with the aid of a glass slide.

3.1.4 Sample cleaning

After polishing and dicing the silicon is likely to have picked up various surface contaminants due to general handling and the adhesives used during mounting. A clean surface is necessary to allow the etching solution to attack the wafer surface evenly and avoid any shadowing, in addition to limiting foreign species from altering the chemical properties of the etch. Samples were immersed in standard reagent grade acetone for 20 minutes to remove any adhesives, if this was insufficient an ultrasonic bath was used to speed up the process and remove more stubborn contaminants. After removal the samples were blown dry using compressed air.

3.2 Chemical etching

3.2.1 Use of inert equipment and HF precautions

PTFE beakers (50ml) were used for performing the etches due to their inert properties in hydrofluoric acid containing environments.

3.2.2 Etch preparation

Potassium dichromate powder, Sigma Aldrich Reagent Plus, $\geq$99.5% was used to make 0.15M solution in 200ml batches by heating and stirring - then stored in chemical bottles. In order

Figure 3.2: Chemical etching apparatus, water bath, teflon beaker and lid and thermocouple.

to make Secco etch solution, 1 part of the dichromate was added to 2 parts hydrofluoric acid (40%) as required. For standard size samples a total etch volume of 30ml was used. Controlling the volume so that all samples are exposed to the same amount of each reagent is important for reliability of results.

3.2.3 Temperature and incident light regulation

A Grant GD120 water bath controller in conjunction with a Haake EK12 chiller coil were used to provide stable temperatures in the range -15 to 45°C for etches. The bath was filled with a 50-50 mix of water and ethylene glycol based automotive antifreeze to enable the low temperatures to be reached. A plastic-coated type-K thermocouple was used to check the temperature of the etch solution inside the beaker. Although the water bath temperature was stable to approximately 0.5°C, the temperature of the solution in the beaker was difficult to keep stable due to the small volume and open top. To increase temperature stability a PTFE lid was produced, with an opening for the thermocouple, resulting in temperature fluctuations of less than a two degrees in the worst cases. A photograph of the equipment is shown in Figure 3.2, with the thermocouple in position in the beaker and connected to the RS display unit on the left.

As highlighted in Section 2.3.1, ambient light conditions are likely to have an effect on etch rates due to photogeneration of holes. Etch pits were investigated after etching in complete

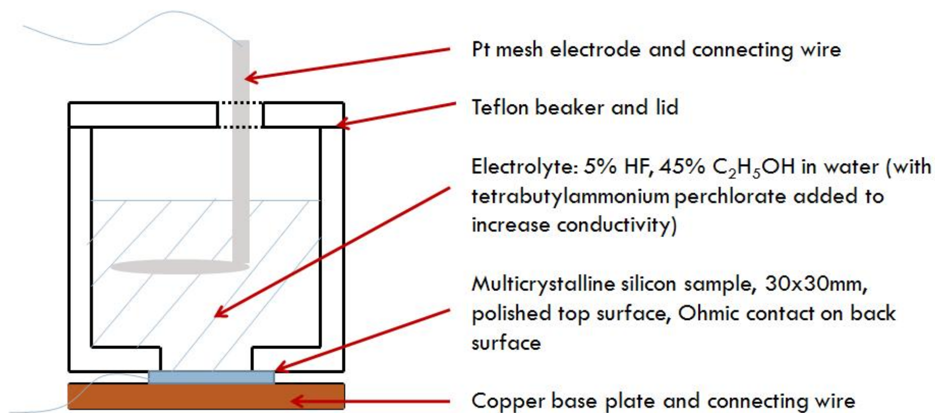


Figure 3.3: Schematic of original anodic etching cell.

darkness and ambient light (from ceiling mounted fluorescent strip lamps) and although the results were similar, i.e. within the experimental error, it was decided that for continuity all experiments would be performed in the same light controlled environment, with the laboratory lights off and a box over the beaker.

3.2.4 Lacomit masking

A 3 x 3mm approx blob of Lacomit varnish was applied to the surface to protect a region from etching. This produces a step on the surface that allowed the bulk etch rate to be calculated.

3.3 Anodic etching

Starting from the technique used by Föll [154], a process for anodic etching of mc-Si was developed.

3.3.1 Cell design

The first step was constructing a cell for containing the sample and electrolyte. The body was machined to shape out of teflon and the opening at the bottom contained a rubber O-ring to stop leakage. The copper base is screwed into the main body to secure the sample in position. A schematic of the cell design is shown in Figure 3.3.

There are three main components to the cell design, as shown in Figure 3.4: the lid and

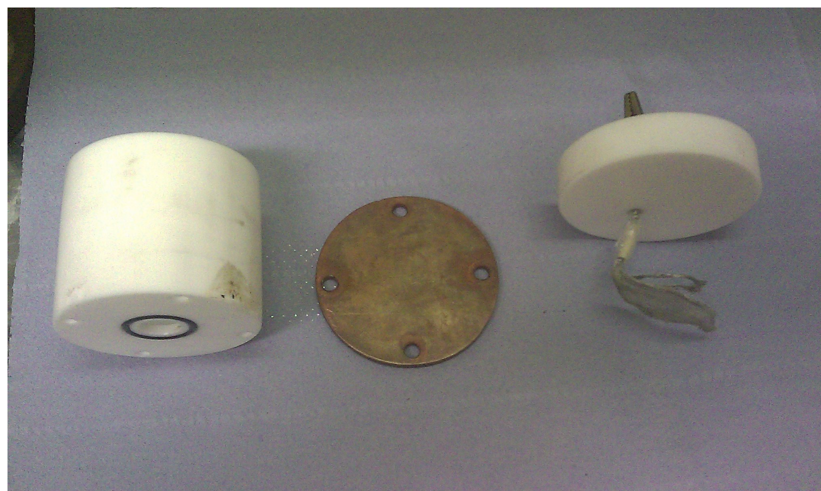


Figure 3.4: Photograph of components used to construct anodic etching cell. From l-r: main PTFE body, copper base and PTFE lid with platinum gauze electrode attached.

top contact assembly, the main body and the copper base. The cell is also shown assembled in Figure 3.5. Additional parts include screws for attaching the base and various interconnecting wires and crocodile clips for making up the required circuit.

The top electrical contact is made through the platinum gauze into the electrolyte, and the back contact is direct to the copper base. This contact is made Ohmic by the following procedure. First, the back of the sample is roughened with 600 grit silicon carbide grinding paper, which is cleaned off with a rinse in distilled water. Next, any native oxide is stripped off by brief (10 second) immersion in a 10% hydrofluoric acid solution, again followed by cleaning and drying. Finally, the indium-gallium, which is liquid at room temperature and therefore can be easily "painted" onto the sample, is applied in a thin layer using a cotton wool bud. The contact could be used at this stage but as the indium-gallium does not dry, painting over it with conducting silver dag paint (which does dry) ensures the contact remains in good condition.

To increase the stability of the currents seen by the sample, the cell was modified to include a third electrode. Additionally, the electrodes were switched from platinum gauze to single-crystal Czochralski silicon bars. A combined frame/lid was constructed to hold the new electrodes in place within the cell, as shown in Figure 3.6. The top 1cm of the bars are Ohmic contacts (made in the same way as the sample) which protrude through the top of

Figure 3.5: Photograph of fully assembled anodic etching cell

the lid. Attached to each contact is a short length of platinum wire, fixed in place by coating with silver dag paint. Connection to the external circuit is made by crocodile clip to these wires.

For many of the early etching runs and during testing of the process, no current was applied to the sample, so the external circuit simply consisted of connections to one or two multimeters such that the current and voltage could be observed. After the changes to the etching setup described above, and for polarisation curve measurements, a Thompson Electrochem Ministat low noise potentiostat with a three electrode setup was used to control the circuit. A comparison between the two different circuit layouts are shown in Figure 3.7.

3.3.2 Electrolyte

The electrolyte used in Föll's work [154], a solution of hydrofluoric acid made with a 50-50 (by volume) water ethanol mix, was tested and successfully revealed defects. However, the composition had not been optimised for etch depth and it was believed that the lack of conductivity would limit the achievable depth. Work on porous silicon [155] suggested

Figure 3.6: Photograph of reference and auxiliary electrodes and the frame used to secure them into the anodic etching cell.

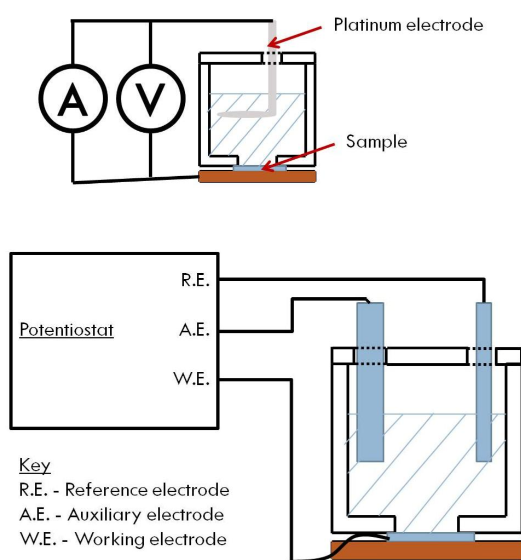


Figure 3.7: Circuit diagrams for basic two electrode system (top) and potentiostat-controlled three electrode system (bottom).

that adding 0.25M tetrabutylammonium perchlorate (TBAP) to electrolytes increased their conductivity so this was added to our composition. To avoid any issues with evaporation or the solution "going off", small batches were made when required, with the following quantities and specifications of reagents:

- 75ml distilled water
- 75ml ethanol (absolute, Fisher Scientific)
- 17ml hydrofluoric acid (analytical reagent grade, 40%, Fisher Scientific)
- 2g tetrabutylammonium perchlorate ($\geq$98% purum, Fluka)

This gives a final HF concentration of approximately 5%, and a TBAP concentration of around 0.04M (the 14g required to achieve the 0.25M mentioned previously would not dissolve in this particular solution).

3.3.3 Agitation

Some of the initial anodic etches were performed with the electrolyte under continuous agitation from a magnetic 10 x 2mm PTFE stirring rod, controlled by the combined hotplate/stirrer.

3.3.4 Multimeter and power source

The multimeter used for measuring the anodic etch parameters is a Thurlby Thandar Instruments 1906 Computing Multimeter, with maximum resolution of 1nA and 1μV. For experiments requiring an applied potential a Thurlby Thandar Instruments TSX3510P Programmable Power Supply was also used. For experiments performed with constant current a Keithley Instruments 225 Current Source was added to the circuit.

3.4 Characterisation techniques

3.4.1 Optical microscopy

Optical microscopy was used extremely frequently for basic characterisation and also was a critical part of the depth measuring technique. The instrument used was an Olympus BH2, with 50x, 100x, 200x, 400x and 1000x magnification lens options and a Nikon digital imaging system with Digital Sight DS-Fi1 5-megapixel camera and NIS-Elements D 3.00 image capture and processing software.

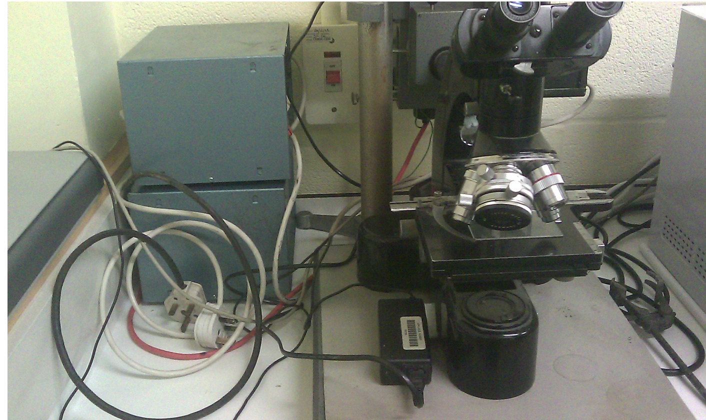
3.4.2 Scanning electron microscopy

The instrument used was the JEOL SEM840F field emission gun scanning electron microscope. The majority of images were taken with settings as follows: 10kV, 1 x 10^{-11}A probe current and 10mm working distance.

3.4.3 Interferometry

A Leitz Ortholux optical microscope with an accessory interferometer and sodium lamp, show in Figure 3.8 was used to map the slope of angled samples. This is achieved by aligning the interferometer with a known flat surface such that there is no directionality to the interference fringes. Moving to a sloped area produces a series of fringes with a characteristic spacing that can be used to measure the change in height. Performing the measurement requires switching between light sources - finding the etch pits is done in white light and then the sodium light is used to produce the fringes. To get the etch depth, count the fringes between the flat region and the last etch pit on the slope - for a sodium lamp the fringe spacing is 0.29μm.

Initial testing showed that although the technique could be used successfully, it was difficult to set up the condition where the interferometer is aligned with the flat surface. This is due to the imperfections on the sample surface that are introduced by the etching process; the surface is initially highly polished and flat but after etching the various pits and deposits that are produced alter this. This meant it was difficult to choose where the flat section finished, which leads to errors in the measured depths. An example of the technique is shown

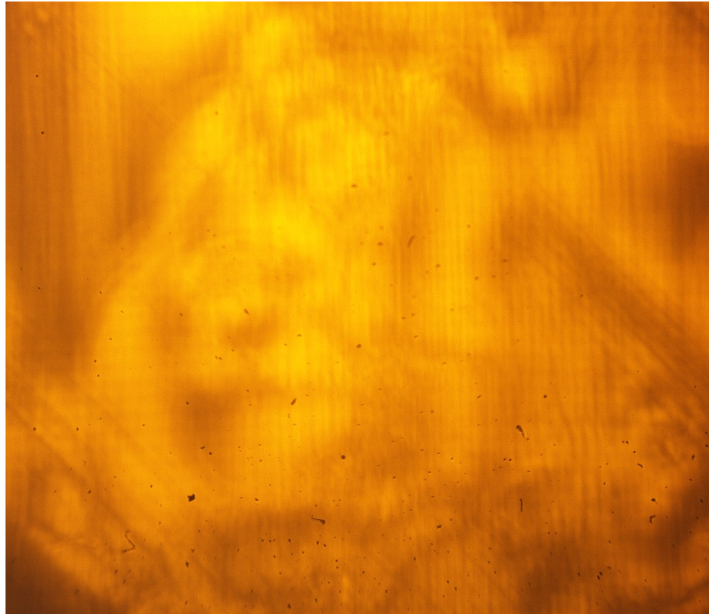


(a) Leitz Ortholux optical microscope with sodium lamp attachment.

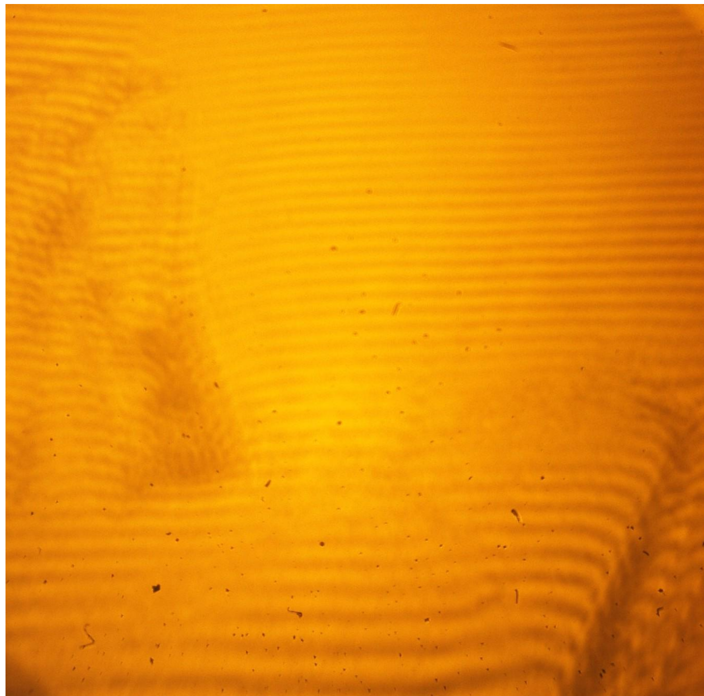
(b) Close up view of interferometer.

Figure 3.8:

in Figure 3.9, with an image of a flat section and an accompanying image of an adjacent sloped section. The image of the flat region shows sufficient fringes that defining an "edge" with any precision was not possible, plus the alignment of the interferometer is performed by eye whilst adjusting the mirrors by hand, so a human error is also introduced. The stylus profilometry method introduced in the next Section proved to be easier to use and produced more repeatable measurements so interferometry was not used in the main part of the project.



(a) Micrograph of interferometry pattern resulting from flat surface.



(b) Micrograph of interferometry pattern resulting from angle lapped surface.

Figure 3.9:

3.4.4 Surface profilometry

Stylus

A Veeco Dektak 6M stylus profilometer was used to map the surface of samples. It is limited to line scans but is very fast and easy to use. In combination with optical microscopy to find

the limits of the etching, the etch depth can be measured, as discussed in Chapter 4.

Optical

A MicroXAM 5000 3D surface profiler was also used for surface mapping. The scan area was too small to map from the flat area to the slope of the samples so this was no use for etch depth measurements.

3.5 Summary

This Chapter discusses the equipment used in this project, the reasons for choosing said equipment and the conditions under which it was used. Chapter 4 builds on this and discusses in detail how the main data gathering technique was developed. Details of specific experimental conditions will be displayed alongside the results.

Chapter 4

Development of a technique to measure the depth of etch tubes

4.1 Introduction

As discussed in Chapter 1, cast mc-Si has a columnar grain structure and many dislocations run normal to the wafer surface through the entire thickness of the material. As discussed in Chapter 2, this project aims to develop a chemical process which etches out the dislocations that are overwhelmingly the most detrimental defect type in mc-Si. To determine the effectiveness of different chemical processes, it was first necessary to develop a robust experimental technique to measure the depth to which the dislocations are removed. Development of a reliable technique was a major challenge. A variety of techniques were used during the early stages and the final method itself went through numerous iterations before the accuracy and reliability were satisfactory. In this Chapter the development of the method is documented and discussed.

4.2 Initial testing: thickness measurement

The initial idea was simple: after etching, remove material by polishing and measure the change in thickness between the start point and the level at which the etch pits disappear.

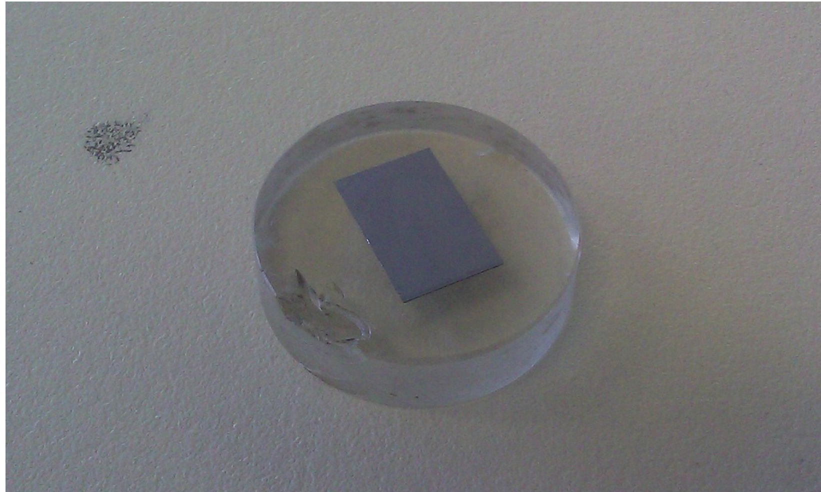


Figure 4.1: Polishing disc with a mc-Si sample attached with mounting wax.

This would measure the depth to which the etch removes dislocations. If required, micrographs at sequential depths would allow the pit depth to be studied for a large number of dislocations. In practice both the polishing and measuring were not straightforward.

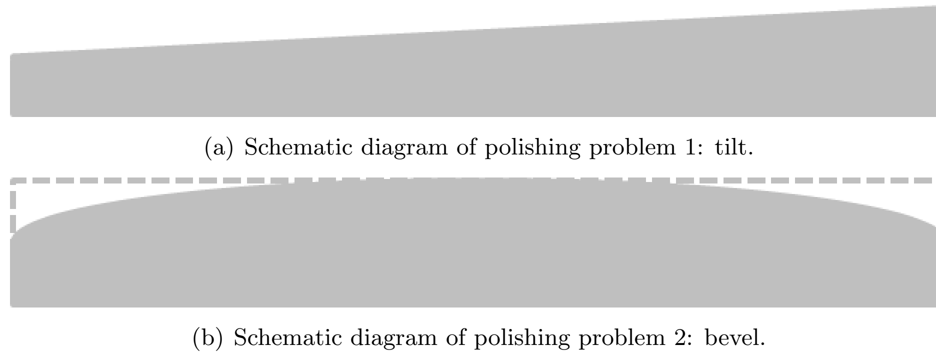
4.2.1 Micrometer measurement

Initial polishing was performed by hand with the etched mc-Si sample attached to a glass disc, as shown in Figure 4.1, using 6μm diamond-containing paste as the abrasive medium. Measurements were attempted by two methods. First, a micrometer was used to record the differential height between the stub and sample to the nearest 1μm. After mounting the etched sample, four measurements of stub height from different locations were recorded and then the total thickness of the stub and sample was measured for four corresponding adjacent locations of the sample. Polishing was performed for 5 minutes and the measurements were repeated. Problems became apparent immediately. The measurements showed that the polishing was not occurring evenly, with both a tilt and some bevelling being applied, as illustrated by schematic diagrams in Figure 4.2.

Two changes were made to try to reduce these effects:

1. Changing from Kemet PSU-M (medium) to PSU-H (hard) polishing cloths.

2. Mounting using the minimum of wax to try and keep the sample completely parallel to



(a) Schematic diagram of polishing problem 1: tilt.

(b) Schematic diagram of polishing problem 2: bevel.

Figure 4.2:

the stub.

The first change was designed to reduce bevelling, as the stiffer pads would deflect less around the edges of the sample. The second was intended to minimize any tilt that may appear due to uneven wax thickness.

The measurement itself was also not satisfactory, as there are clearly inherent problems when making two separate large measurements to make a small differential measurement. In this case, to find the change in thickness, which is of order 10μm, two separate measurements of around 8mm (the combined thickness of the stub and sample) must be made. Errors of 1% in the actual thickness equates to $\pm$ 80μm; if there was any random error included in this, correctly measuring the amount of material removed would be impossible.

4.2.2 Optical microscope measurement

The second measurement method uses the calibrated z-axis control of the Olympus BH2 optical microscope. By focussing in turn on a piece of the sample surface then an adjacent point on the disc and measuring the increase in stage height the thickness of the silicon can be measured. After material is removed by polishing, the measurement is repeated to determine how much the sample thickness has changed. This removes the issues with measuring large distances but still did not produce satisfactory results. It was difficult to repeat the height measurement for the disc as the focus point was very difficult to find due to the translucent quality of the glass. Additional error may have been introduced by very slight deformation of the wax layer during polishing; whatever was causing it the results were not good enough.

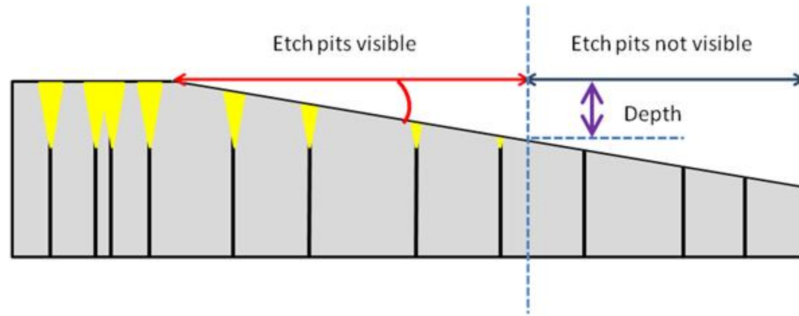


Figure 4.3: Schematic diagram of a sample after undergoing the angle lap technique.

4.2.3 Summary

Both thickness measurement methods produced unsatisfactory results during testing. Alternative methods were therefore developed.

4.3 Method 2: Angle lapping

An alternative method was developed to eliminate these problems, but would require the ability to trace particular etch pits down through the sample to be abandoned. A schematic of how the technique was designed to work is shown in Figure 4.3. The surface of the etched mc-Si sample is polished at an angle, such that the resulting sloped surface intersects the depth of the deepest etch pits at some point. Some original flat surface must be retained as a reference for depth measurements. With a 15mm long sample of 200μm thickness a quick calculation shows that only a very small angle is needed to provide both a flat region and an angled section that has enough depth to allow analysis of etch pits up to 100μm.

For example, an angle of 1° applied over half the sample length (7.5mm) gives an angled section with a depth of approximately 130μm:

$$7.5 \tan 1^\circ = d$$

$$d = 0.13\text{mm}$$

The depth at which the etch pattern disappears is the key parameter to be measured,

this was done by a combination of optical microscopy and surface profilometry as discussed in more detail later in the Chapter.

4.3.1 Preparing an angled specimen

Etched samples were mounted on a stub modified to enable polishing at approximately 1° off horizontal. The equipment required for this angled polishing was adapted from some items that already existed in the lab. The modification required to produce an angled surface was designed and constructed as follows. Pieces of scrap silicon wafer were used to construct a small angled platform: a piece of 200μm thick mc-Si was diced to 10x1mm and a piece of Cz-Si was cleaved to be just larger than the typical 10x15mm sample size. These were mounted onto the face of the stub using wax in the arrangement shown in Figure 4.4, providing a flat surface approximately 1° misoriented compared to the original flat surface. Precisely knowing this angle was not necessary for any later measurements. The stub, Figure 4.5, consists of a machined piece of stainless steel and a wooden shaft/handle. The steel part's face is flat and perpendicular to the sides. The wooden handle protrudes from the top of the frame and is used to hold the sample in a fixed orientation during polishing - it would rotate freely otherwise.

The angled platform described above was used in conjunction with a polishing frame, shown in Figure 4.6. This is another, larger piece of machined stainless steel, and is designed to fit round the stub and hold it perfectly flat against the polishing wheel. It has grooves on the base to allow the polishing media to reach the sample in central opening.

Polishing was again done in steps as per Section 2.1. As only part of the sample is polished the time required is reduced due to the smaller area in contact with the polishing pad; approximately 30 seconds grinding followed by a couple of minutes on each grade of diamond polish being sufficient to give a good finish. Once the angle polishing was complete the sample was removed from the stub and attached to a glass microscope slide, again with wax, ready for analysis and then storage. A typical sample after angle lapping and mounting is shown in Figure 4.7.

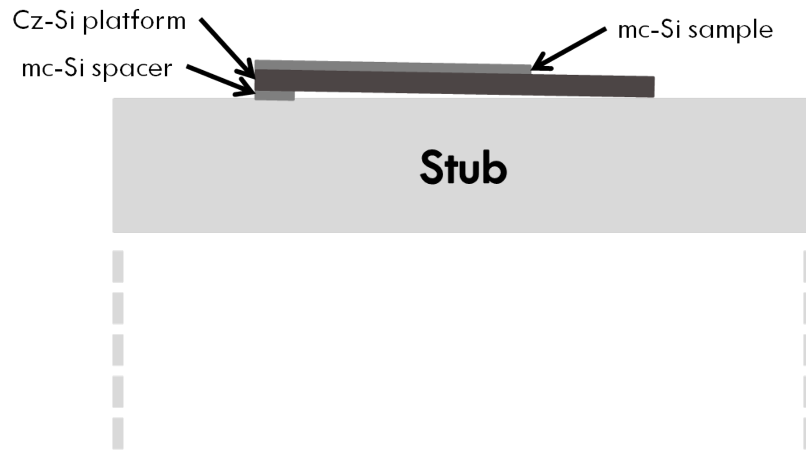


Figure 4.4: Schematic of stub design.

Figure 4.5: Photograph of flat stub showing handle and angled platform. Attached mc-Si sample measures 15 x 10mm.

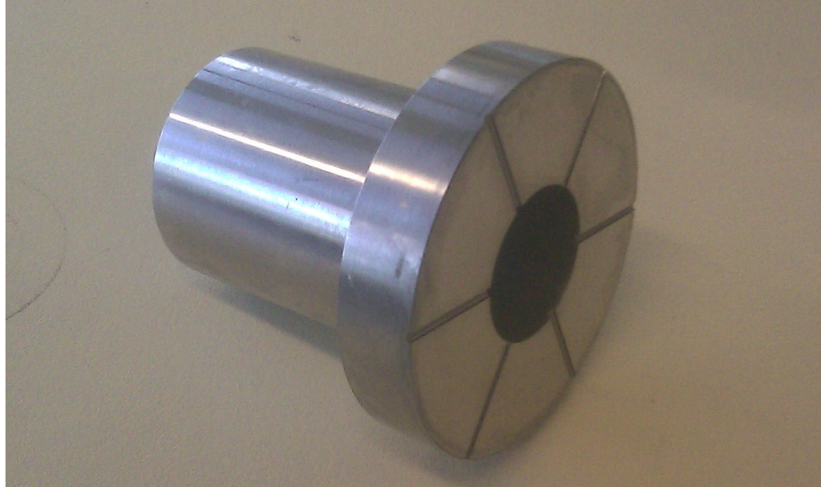


Figure 4.6: Photograph of polishing frame used in angle lapping. The diameter of the base is 8cm and the diameter of the opening is 3cm.

Figure 4.7: Etched and angle lapped mc-Si sample mounted on microscope slide.

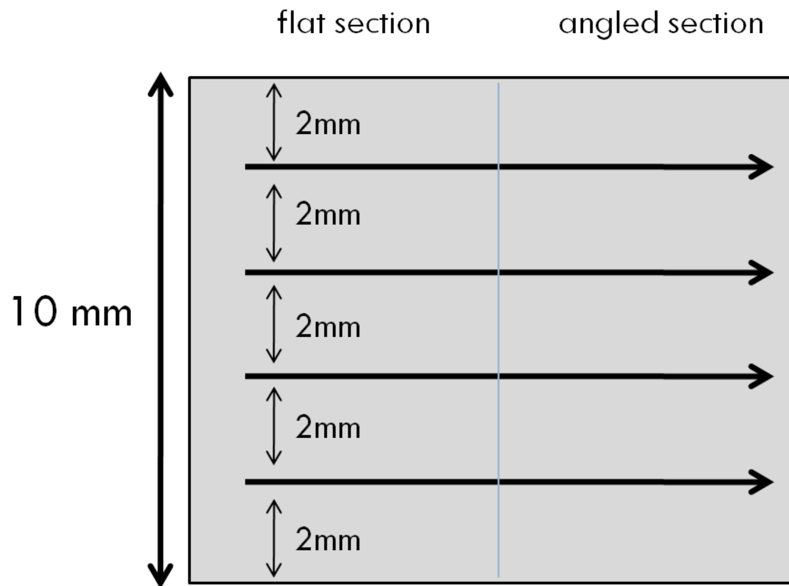


Figure 4.8: Schematic of profilometry line scans performed to measure surface geometry.

4.3.2 Surface profile measurements

Profilometry

The first step in the process is to map the surface of the angle polished specimen using the Dektak surface profilometer. It is only capable of performing line scans so for a sample with a width of 10mm profiles are taken at 2, 4, 6 and 8mm from one side, as illustrated by the schematic in Figure 4.8. It is important to include the transition from flat to slope and the lower edge as these will be used as references later during the measurement process. Figure 4.9 shows a typical resulting profile after a series of such scans had been performed and the data collated and plotted.

Accurately and reliably measuring the depth to which the etch pits reach was still difficult even with the improvements introduced by the angle lap method. With a good angle polish, where the sloped section and flat section meet at a line perpendicular to the sample edge, it should be straightforward to find the point at which the etch pits are no longer visible, and using the optical microscope to do this is the next step in the measurement process. Figure 4.10 shows how there is still some uncertainty due to the random nature of the etch pattern

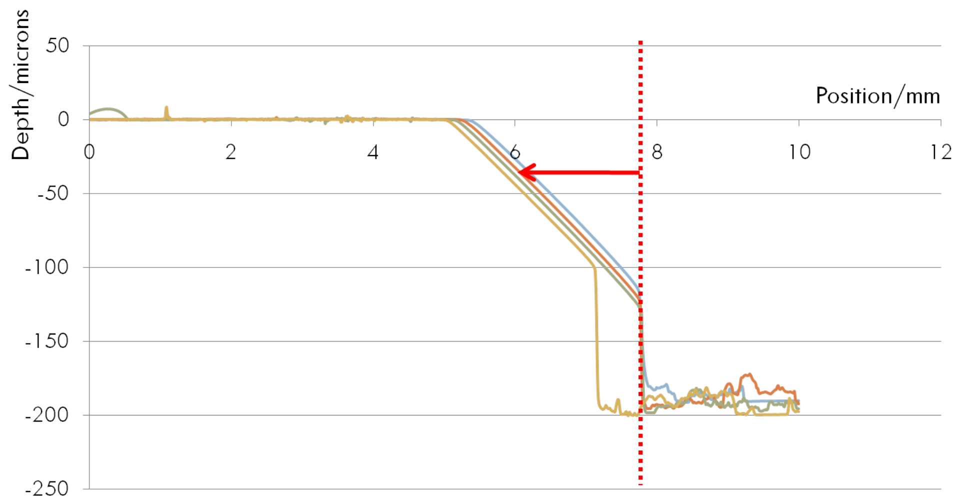


Figure 4.9: Typical surface profile of an angle-polished specimen.

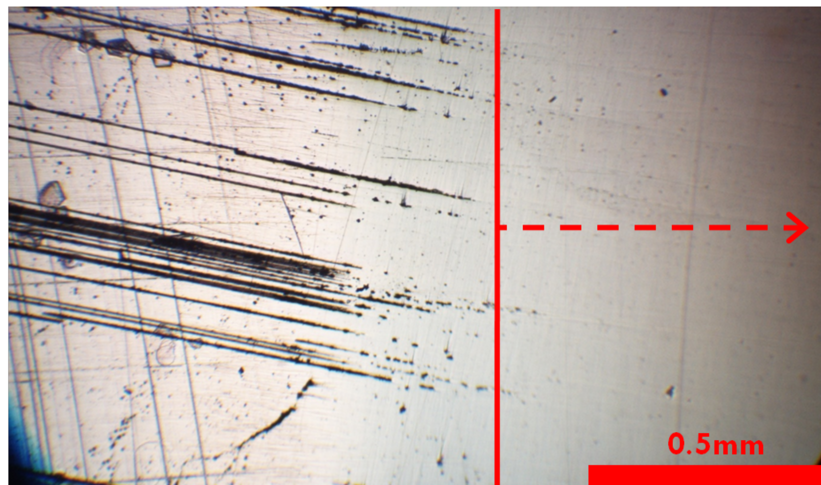


Figure 4.10: Optical micrograph of the sloped surface of an angle-lapped specimen.

and the presence of extraneous polishing marks either from original sample prep or the angle polish. It was possible to estimate the position of the extent of the etch pits in the optical microscope to the nearest 0.02mm, which by simple trigonometry (assuming an angle lap of 1° is applied) translates to an error of approximately $\pm$ 0.5μm in the depth measurement.

Once the point at which the pattern vanishes is decided upon as best as possible, the distance from it to the edge of the sample should be measured using the vernier scales on the microscope stage controls. These can be read to the nearest 0.1mm, so by the same trigonometric calculation as above lead to an error of approximately 2μm in the depth measurement.

The sample must be aligned parallel with the stage edges for this step. If the sloped section meets the flat section at an angle, multiple measurements must be made to coincide with the points where the profiles are taken (refer back to Figure 4.8 for details). Once this distance is known it is converted to a depth using the map produced by the profilometer. This depth is the maximum etch depth for the sample.

With a resolution of 2μm the accuracy of this final iteration of the technique is far superior to the alternatives.

Bulk etch depth measurement

Additionally, the profilometer can be used to measure the bulk etch depth of the sample thanks to a very simple additional technique. Before etching, a tiny spot of Lacomit varnish is applied to the corner of a sample using a paint brush (see Section 3.2.4). While the rest of the sample is being etched, the material under the varnish is protected from attack and remains unetched. After the etch is complete, the varnish is removed by immersing the sample in acetone for around 5 minutes, and the height of the unetched "step" can be measured by using the profilometer. This is achieved by running a scan across the interface of the etched and unetched regions.

4.4 Errors

This section will draw together any sources of error mentioned so far, highlight any additional sources that have not been explicitly covered and explain how they will be dealt with.

The temperature at which etches are performed was identified as a potential error, and steps were taken to minimise this (see Section 3.2.3). After the modifications to the beaker, temperature fluctuations were kept within 2°C. This will be acknowledged by using horizontal error bars on graphs showing temperature dependence.

The main errors arise in the various methods used for measuring etch parameters. The etch tube depth is covered previously (see Section 4.3.2), with the conclusion that the technique is accurate to $\pm 2\mu$m for all magnitudes of measurement. The tube plus bulk measurement

therefore has a maximum possible error of the sum of the two errors. Vertical error bars will be used to show the error magnitudes.

The diameter of etch pits will be measured using the Nikon software that accompanies the microscope (see Section 3.4.1). The resolution of the images at 400x, which was the magnification level used for measurements, is 0.16μm per pixel and this allows the human error of placing the measuring markers on the screen to be estimated. This is particularly noticeable for small diameter measurements, which may require the image to be digitally magnified, introducing some blurring effect. Testing the accuracy of this technique by attempting to mark a given point on a micrograph showed that the estimated maximum error is approximately 3 pixels, equivalent to 0.5μm. Further, the tubes are rarely perfectly circular where they intersect the surface, introducing additional uncertainty into the measuring process. This is dealt with by measuring 8 separate tubes and using the mean value to represent the data point. Again, vertical error bars will be used to acknowledge these errors, with whichever is the larger of the standard deviation and the 0.5μm highlighted here being used for the magnitude.

The error in the bulk etch measurements again arises from the imperfectly flat surfaces produced by the polishing and etching, and how the surface profiles representing these are interpreted. The values for vertical displacement in both the covered and exposed regions oscillate as a function of horizontal position, particularly in the exposed (*i.e.* etched) region, even for macroscopically flat areas. The recorded value is therefore arrived at by estimating the average displacement 1mm either side of the interface and calculating the difference, which can be done automatically using the "Statistics" function of the OriginPro graphing software as shown in the example in Figure 4.11. It is estimated that the technique is accurate to the nearest 10%, so appropriate vertical error bars will be added to the data points.

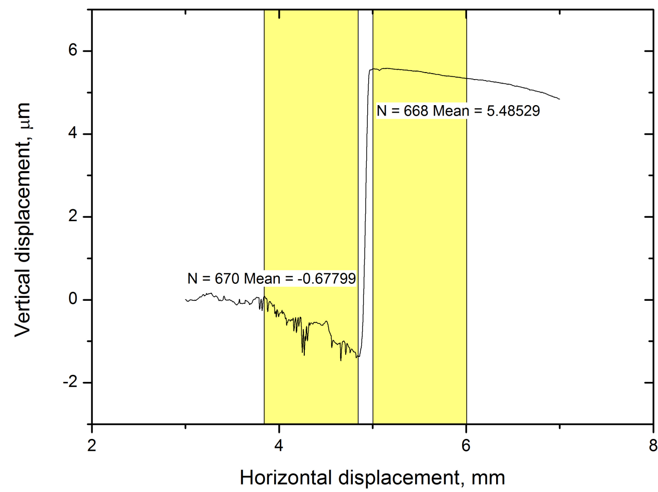


Figure 4.11: Example of measurement technique used for recording bulk etch depths. The line profile across the interface shows a distinct step, the bulk etch depth is the difference between the average vertical displacements of the 1mm regions to either side - in this case approximately 6μm.

4.5 Summary

In this Chapter, different techniques to measure the depth to which dislocations are etched in mc-Si were discussed. The thickness measurement and interferometry techniques were unsuccessful. The angle lap technique was successful and was shown to produce reliable results. It is used extensively in later Chapters to measure the effectiveness of different etching methods.

Chapter 5

Dislocation removal by Secco etching

5.1 Introduction

The aim of this project is to develop a process to etch out dislocations - a major cause of recombination in mc-Si - from the material *after* growth. A good starting point is to use a standard defect revealing etch (the Secco etch) which is already used in laboratories worldwide. This Chapter contains the results of an investigation into the etching behaviour of mc-Si in the Secco etch at various temperatures. Unlike previous work on this etch, where the focus was on its effectiveness as a defect revealing etch [141], the intent here is to ascertain whether there are conditions that produce deep, high aspect ratio pits where a high fraction of the dislocations in the material are removed. Times and temperatures of the etch were varied to perform a systematic study of the etch's ability to remove dislocations from mc-Si.

5.2 Methodology

Secco etching is a standard technique used for identifying defect structures in silicon, where samples are immersed in a solution of 0.15M potassium dichromate mixed with hydrofluoric acid (49%) [141]. Potassium dichromate acts as the oxidising agent in the etch, and

preferentially attacks silicon at defects (grain boundaries, twins and dislocations) due to the additional energy of atoms at these sites, etching them at a higher rate such that pits are formed (see Section 2.3).

A matrix of samples subjected to Secco etching for a variety of times and temperatures was studied. As introduced in Section 3.1.1, the samples were 10 x 15 mm pieces cut from as-sawn p-type mc-Si wafers provided by REC, and they were polished on one side.

The temperatures chosen were -15, 3, 25 and 45°C, and the times ranged from 3 to 120 minutes. With no previous work as a guide, the temperature range was selected mainly based on the limitations of the available equipment. Testing showed that the water bath's chiller unit was limited to a minimum stable temperature of -18°C (with ethylene glycol-based antifreeze added to the water), and at the upper limit there were concerns over the safety of a hydrofluoric acid containing solution at temperatures over 50°C, so the upper and lower bounds were chosen within these conditions. The time constraints were based on testing of the etch performed by the author, the minimum was designed to be the shortest duration that would produce clearly visible pits in an optical microscope and the maximum was chosen such that the etched samples retained enough strength to be angle lapped without fracturing.

Once a sample had undergone etching, it was characterised using the methods detailed in Chapter 4. Initial characterisation was performed using optical microscopy, which enabled the etch pit diameter to be measured. The samples were also subjected to an angle-lap, as described in Section 4.3.2 which enabled the etch pit depth to be determined. As well as removing material from the vicinity of grain boundaries and dislocations, the Secco etch also removed bulk material from the surface. The amount of bulk material removed was also determined, as described in Section 4.3.2.

A brief additional experiment entitled "repeat Secco etching" was also performed. Using the same Secco etch as the main investigation, it was designed to counteract any slowing of the dislocation etch rate due to the tubes filling with reaction product. Assuming that blocked tubes may be a problem when using Secco etching, this experiment will give information on the influence of diffusion on the process.

The same equipment as used in the experiments in the rest of the Chapter were used

here. For simplicity, the test was only performed at room temperature. The method used was identical to the steps described previously for performing chemical etching, apart from one distinction. Rather than immersing the sample into the etch solution and leaving it for the required duration, it was periodically removed and cleaned according to the steps itemised below, with the intention of clearing the etch pits of any built up reaction products or deposits.

1. After two minutes etching time, remove sample.
2. Rinse sample thoroughly in deionised water and dry carefully with compressed air.
3. Place sample in small beaker containing 30ml general lab acetone, then subject beaker to ultrasonic bath for 30 seconds.
4. Remove sample and again dry carefully. Place on clean hotplate, set to 80°C, in fume cupboard for 2 minutes.
5. Allow to fully cool then replace in etching solution for two minutes and go back to step 1.
6. After 10 cycles, 20 minutes total etch time, process is complete.

To ensure a fair test, a comparison sample that was etched for 20 minutes continuously, was processed on the same day, using the same batch of Secco etch solution and from an adjacent piece of the same mc-Si wafer.

5.3 Results

5.3.1 Microscopy

The first information collected was a set of optical micrographs of the etched samples. These were necessary to allow measurement of the dislocation tube diameters, as well as allowing useful qualitative comparisons between different temperature and duration etches. Scanning electron microscopy was then used to give additional detail on the geometry of the etch tubes created.

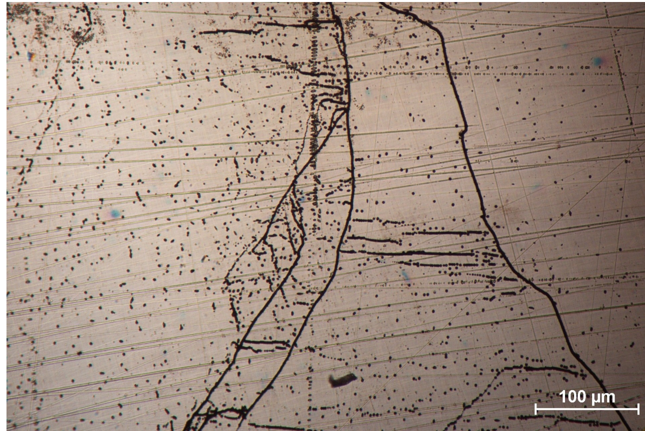
Optical micrographs

Multiple micrographs were acquired for all times and temperatures for measurement purposes. Only a selection are included in this section to give a representative idea of the etch behaviour at a range of times and temperatures. Tube diameters were measured using tools in the Nikon NIS Elements software that accompanies the optical microscope and is used for acquisition of digital micrographs and picture editing. An average of the diameters of eight tubes was taken to arrive at recorded value. For most samples, the variation observed in these data produced a standard deviation of around 10%. For smaller measurements the errors are higher due to the issue with magnification highlighted in Section 4.4.

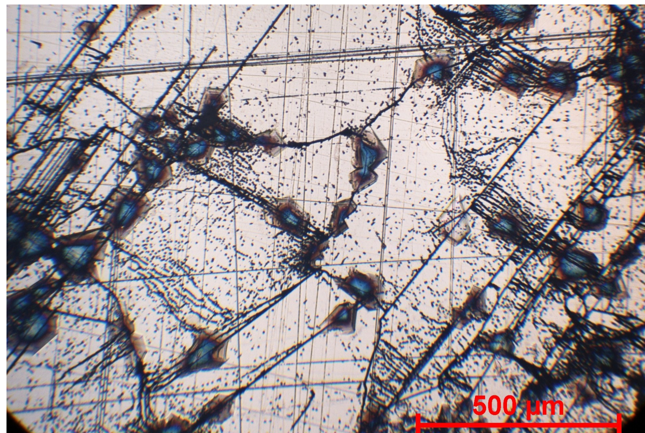
Figure 5.1(a) shows the dislocation pattern for a Secco etch of 40 minutes duration at -15°C and the etch pit diameter was measured at $3\pm0.5\mu$m for these conditions. Figure 5.1(b) shows a similar pattern but here the pit diameter, after 100 minutes of etching, has grown to $7.4\pm0.7\mu$m. Also observed in longer duration etches, and shown here, are crystalline deposits on the surface of the sample. Figure 5.1(c) is a micrograph from the same sample at higher magnification where two kinds of etch pit are visible; dark, circular pits and teardrop-shaped shallow pits. The feint, straight lines visible in all the images in Figure 5.1 are residual polishing damage that is also attacked by the etch.

Figure 5.2 shows examples from the etches performed at 3°C. Comparing the 40 minute samples for both -15 and 3°C, it is clear that the pits are bigger at the higher temperature; the measurements were $3\pm0.5\mu$m and $9\pm0.9\mu$m respectively, suggesting a strong dependence on temperature. 12 minutes at 3°C is sufficient to produce 3μm diameter pits, the micrographs for the -15°C-40 minute and 3°C-12 minute samples appear very much alike. Discovering the etch depths of samples that look similar on the surface should give information on the relative etch rates of bulk atoms and those at dislocation cores as the temperature is varied, and this will be investigated in Section 5.3.2.

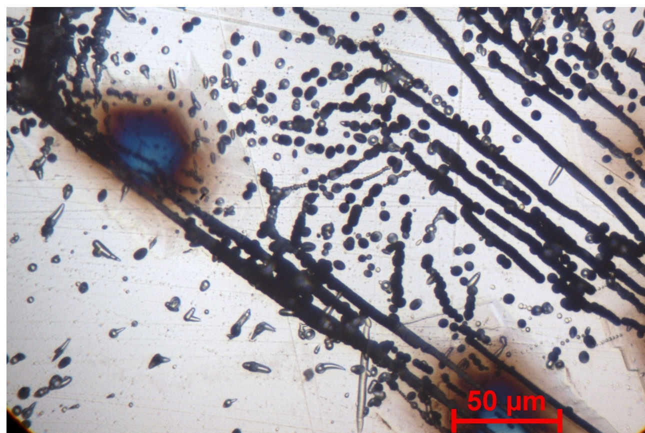
Figure 5.3 contains micrographs from the set of etches performed at 25°C. The etch pit diameters are $3\pm0.5\mu$m and $8\pm0.8\mu$m respectively. Disregarding the size of the pits, etches at all times and temperatures appear quite similar on the surface, being characterised by mainly circular pits surrounded by flat areas - that pattern continues here.



(a) Optical micrograph showing typical dislocation pattern after 40 minute Secco etch at -15°C.

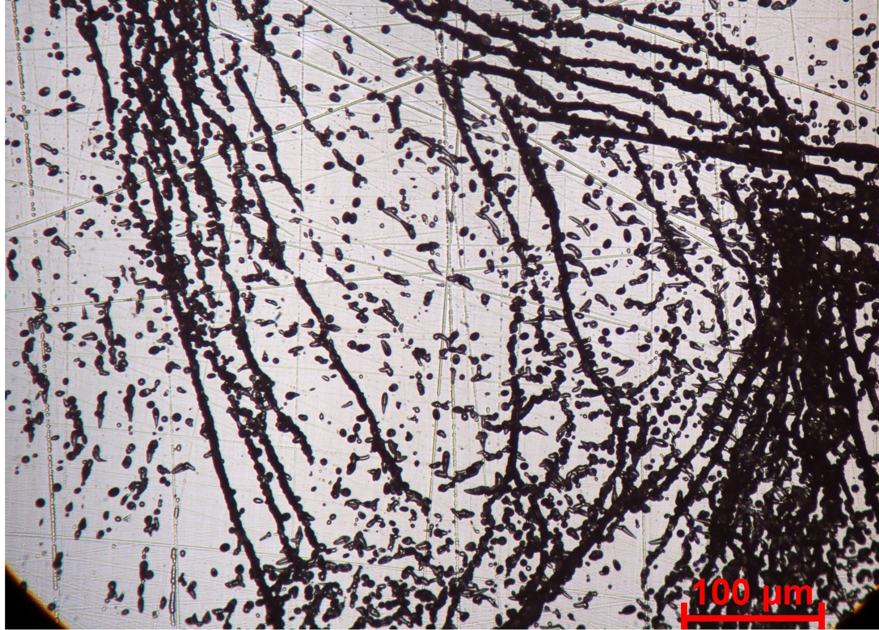


(b) Optical micrograph showing typical dislocation pattern, plus crystalline deposits, after 100 minute Secco etch at -15°C.

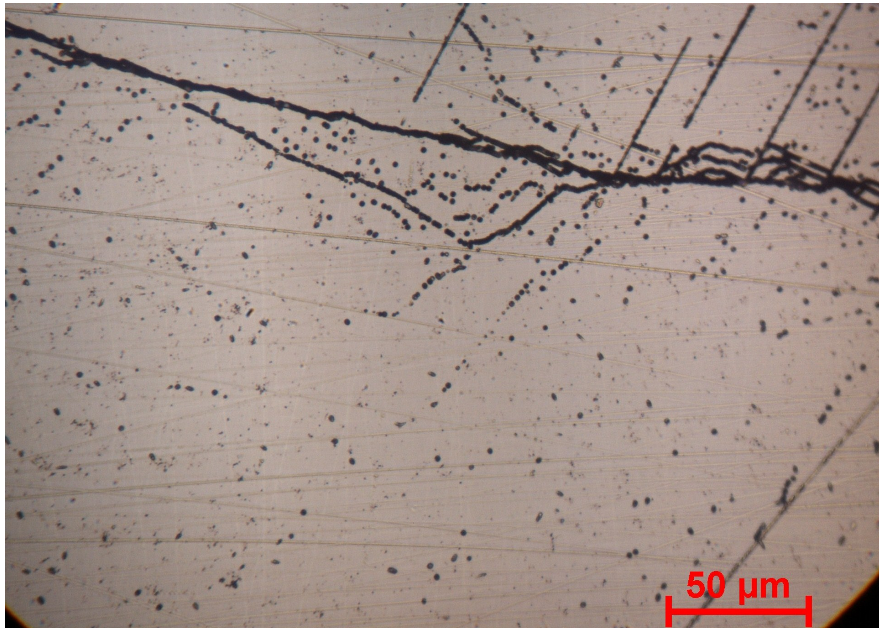


(c) Optical micrograph showing high magnification view of etch tubes after 100 minute Secco etch at -15°C.

Figure 5.1: Optical micrographs of mc-Si samples etched at -15°C.

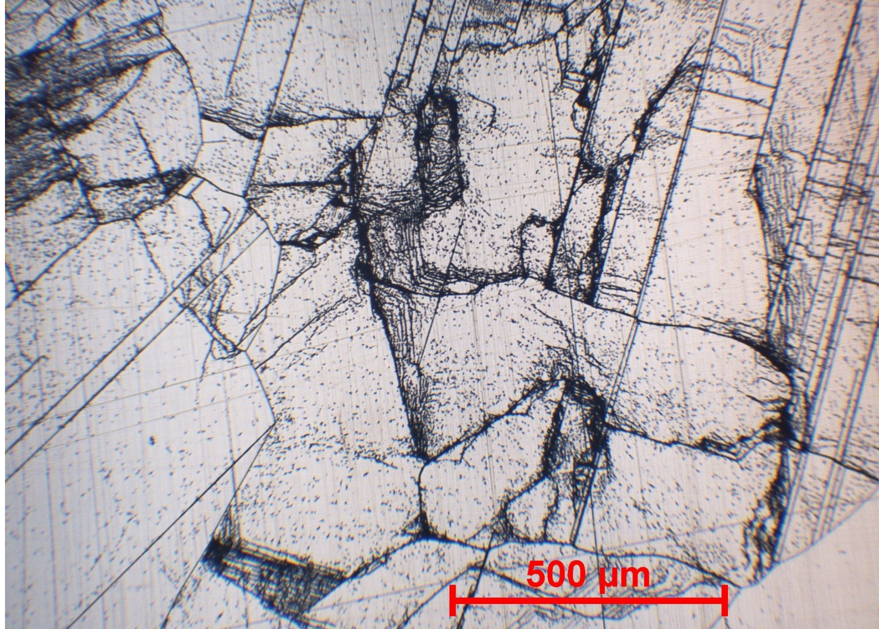


(a) Optical micrograph showing high magnification view of dislocation pattern after 40 minute Secco etch at 3°C.

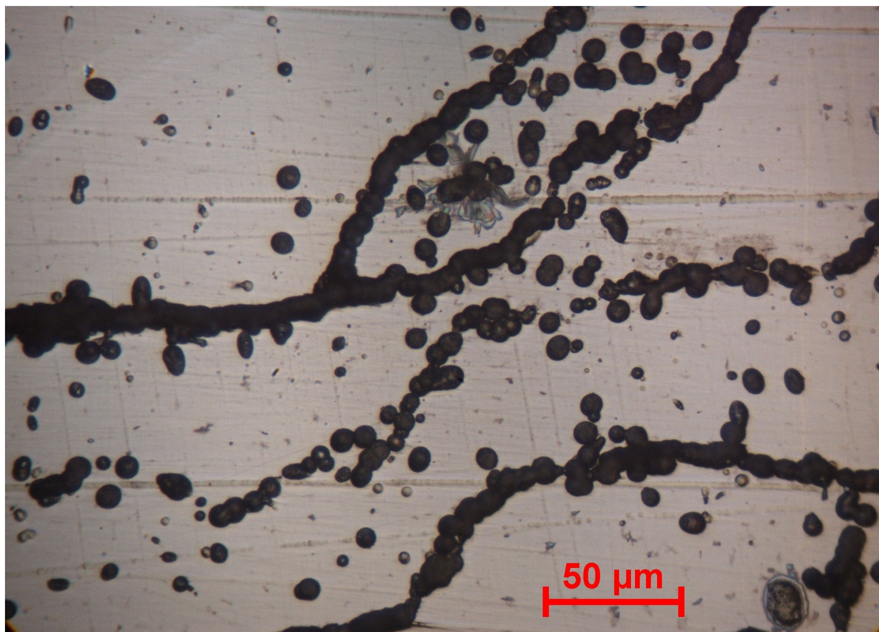


(b) Optical micrograph showing high magnification view of dislocation pattern after 12 minute Secco etch at 3°C.

Figure 5.2: Optical micrographs of mc-Si samples etched at 3°C.

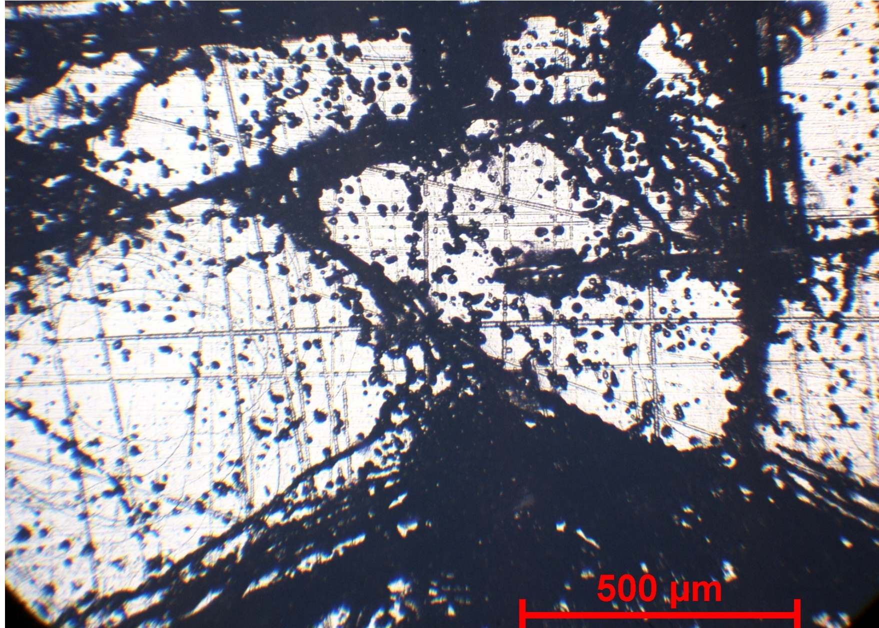


(a) Optical micrograph showing typical dislocation pattern after 7 minute Secco etch at 25°C.

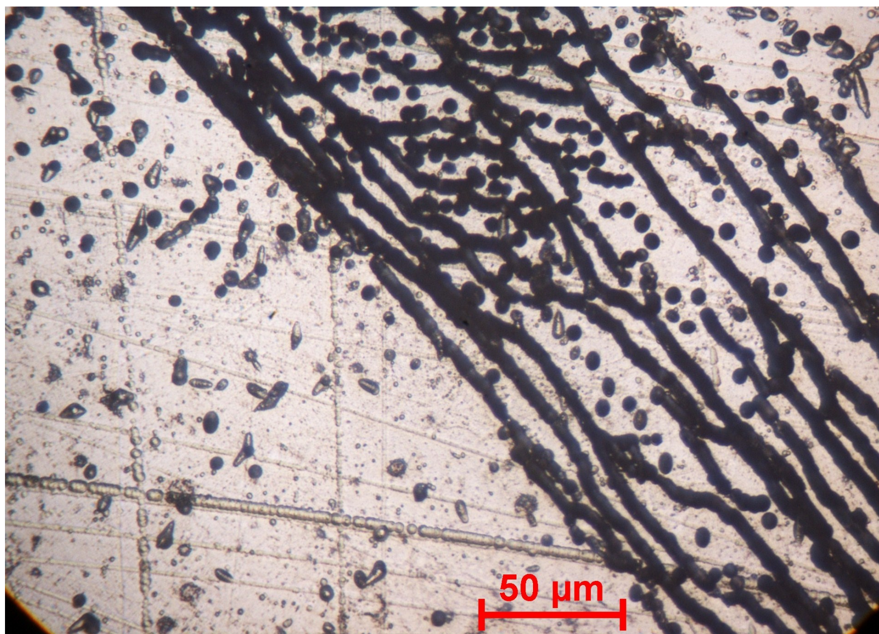


(b) Optical micrograph showing high magnification view of dislocation pattern after 20 minute Secco etch at 25°C.

Figure 5.3: Optical micrographs of mc-Si samples etched at 25°C.



(a) Optical micrograph showing dislocation pattern after 40 minute Secco etch at 45°C. Under these conditions the sample is very heavily etched causing pits to frequently overlap, as seen in the lower-right portion of the image.



(b) Optical micrograph showing high magnification view of dislocation pattern after 12 minute Secco etch at 45°C.

Figure 5.4: Optical micrographs of mc-Si samples etched at 45°C.

Figure 5.4 contains images of samples etched at 45°C. The etch pit diameters are 20±2μm and 5±0.5μm respectively, and the 45°C-40 minute sample is the most heavily etched sample that it was possible to produce before the silicon became too fragile to work with. The etch pits are so large that they frequently impinge upon one another in regions of high dislocation density, producing the large dark areas clearly shown in the micrograph. Measurements were taken from areas of lower dislocation density where the dimensions of the tubes are unambiguous. In other samples, no variation (outside the errors already described) in tube size relative to dislocation density was observed - disregarding extremely heavily etched regions should not affect the values recorded.

It is observed qualitatively that for a given sample the distribution of etch tube diameters tends to be narrow, with a large fraction of pits being of similar size. However, in some examples a bimodal distribution can be found, with a large fraction of "full size" pits as above plus a number of very small pits that appear more shallow. A good example of this is shown in the 45°C-12 minute sample, Figure 5.4(b); in the left of the image there are a series of small, circular pits that do not appear to be related to polishing since they are not aligned in any way, as well as the teardrop-shaped items seen earlier.

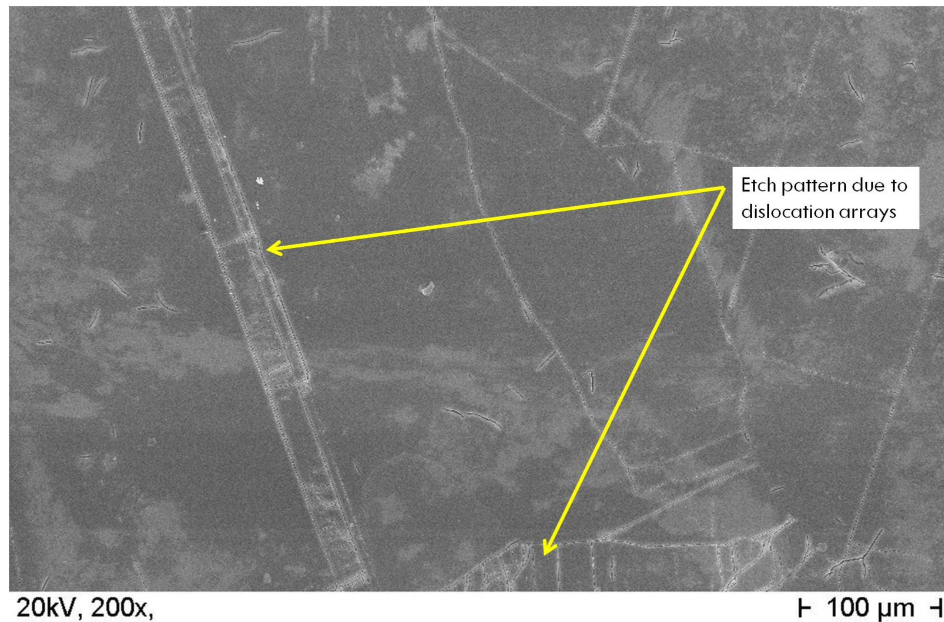


Figure 5.5: Scanning electron micrograph of sample surface after 12 minutes etching at 25°C, 200x magnification. A similar microstructural pattern, as seen in earlier optical micrographs, is shown in this low magnification image, with arrays of dislocation pits and etched grain boundaries visible.

Scanning electron microscopy

Scanning electron microscopy was used qualitatively to look in more detail at the etch pits. The higher resolution affords a much closer look at the geometry of individual pits, and the increased depth of field allows a view down into them - this is much more information than is available from the optical micrographs.

Figure 5.5 is a very low magnification picture and appears similar to the optical micrographs in the previous section, showing the defect structure revealed by the etch. Using a higher magnification, as shown in Figure 5.6, reveals that the tubes appear quite deep and in this case proceed down into the sample parallel both to each other and to the surface normal. A similar situation is observed in Figure 5.7, although here the two rightmost tubes clearly do not proceed down into the wafer at the same angle. Although there were far too many tubes to allow close investigation of all of them, overall it was noted that the majority were observed to be within 5° of vertical. Therefore, errors in depth measurements due to the inclination of dislocations are very small. Further, in both these high magnification images,

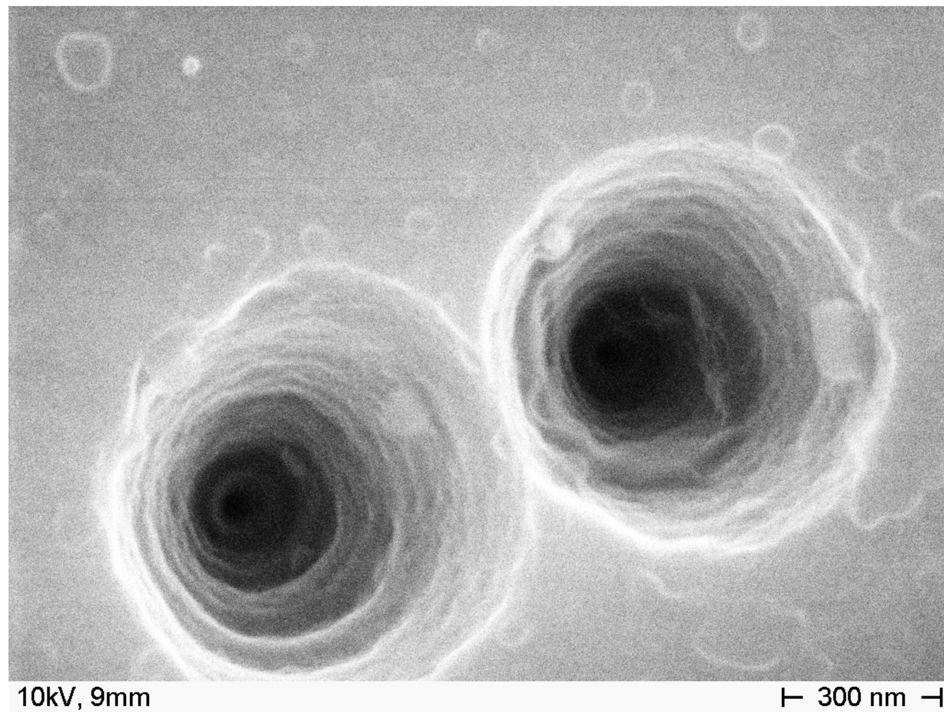


Figure 5.6: Scanning electron micrograph of sample surface after 12 minutes etching at 25°C, showing two parallel etch tubes.

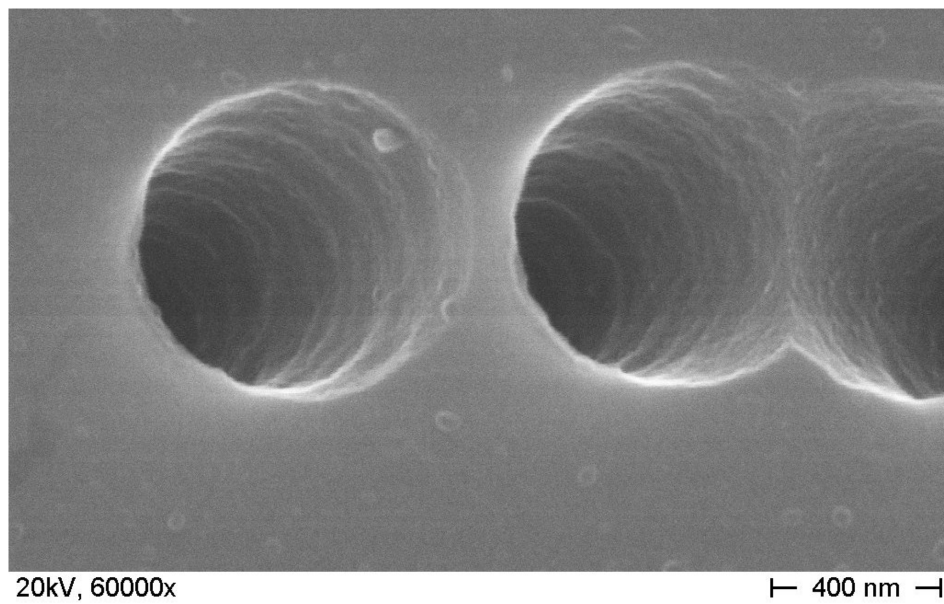


Figure 5.7: Scanning electron micrograph of tubes produced by 12 minutes etching at 25°C, 60000x magnification, showing etch tubes within the same grain proceeding into the wafer at different angles.

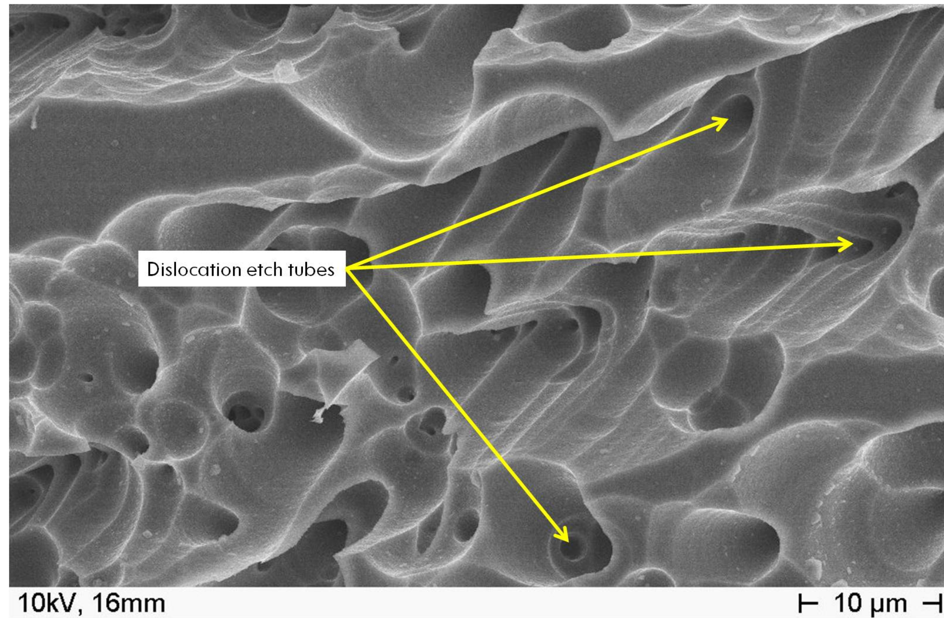


Figure 5.8: Scanning electron micrograph of sample surface after 30 minutes etching at 25°C, 2000x magnification. Shown here are dislocation tubes, but the surface in between them is noticeably less flat than in previous images, showing that the etch attacks the bulk.

the internal walls are seen to be scalloped, suggesting that etching takes place in a step-wise process.

Estimating the tube depth with any accuracy from these images is very difficult, but by comparing with the data from the angle lapping experiments a check for consistency can be made. For 12 minutes etching at 25°C, a tube depth of around 20μm would be expected. The steep sides of the tubes observed in Figures 5.6 and 5.7 do not qualitatively contradict this. For more evidence, a very simple calculation of the depth of field available in these images gives an approximate answer of 3μm. As the bases of the tubes appear to be well below the point at which features cease to be resolvable, it can be said with some certainty that the tubes are deeper than 3μm.

Figure 5.8 shows the heavily etched surface of a 25°C-30 minute sample. Whereas the optical micrographs appear to show flat surface in between the etch pits, in this image it is clear that bulk material is also attacked by the etch. Figure 5.9 is a low magnification image of the same sample, and clearly shows some of the crystalline deposits first mentioned in the previous section.

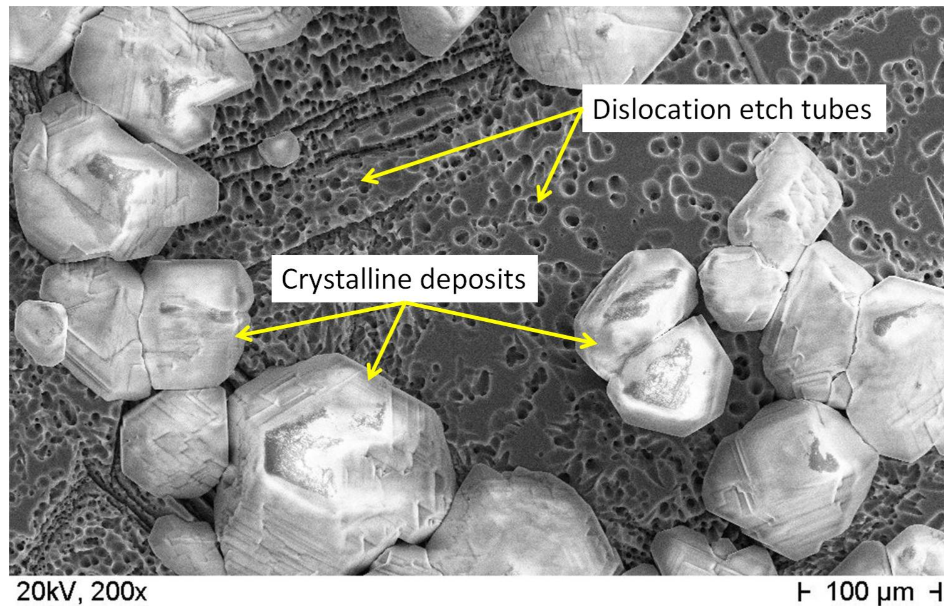


Figure 5.9: Scanning electron micrograph of sample surface after 30 minutes etching at 25°C, 200x magnification. The bright blocks shown here are crystalline deposits, a feature of samples that have been etched for longer durations.

5.3.2 Etch depth parameters

The angle lapping technique described in Chapter 4 was used to measure the etch parameters, and the data are presented in Figures 5.10 and 5.11. Etch pit depth plus bulk depth is also plotted on the graphs, which gives a measure of the etch pit depth relative to a fixed starting point - the original surface level. At all temperatures, etch pit diameter and bulk etch both increase approximately linearly with etch time, with very little scatter at -15, 3 and 25°C. At 45°C, an increase in points lying away from the best fit is noted. No truly anomalous data is observed in either the tube diameter or bulk etch depth measurements, all the points follow the overall trends.

The missing data points from the bulk depth measurements were due to the lacomit varnish (see Section 3.2.4) debonding from the sample surface (possibly due to insufficient drying time). Due to the time required for polishing a replacement sample, and the apparent high quality of the existing bulk depth data, these were not repeated. This problem did highlight that care should be taken to check that no etch solution could penetrate the varnish. It was confirmed that there was no evidence of etching in the varnished regions of any other

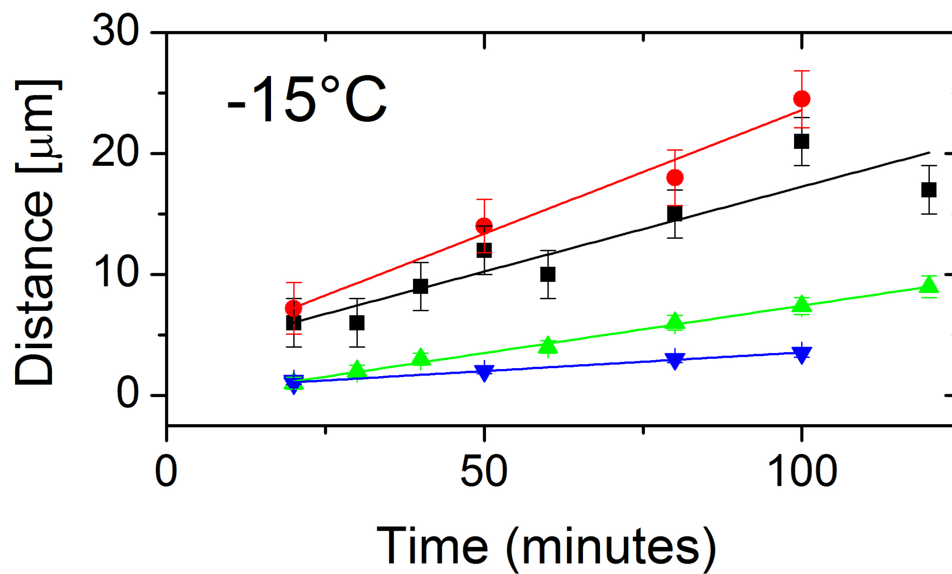
samples.

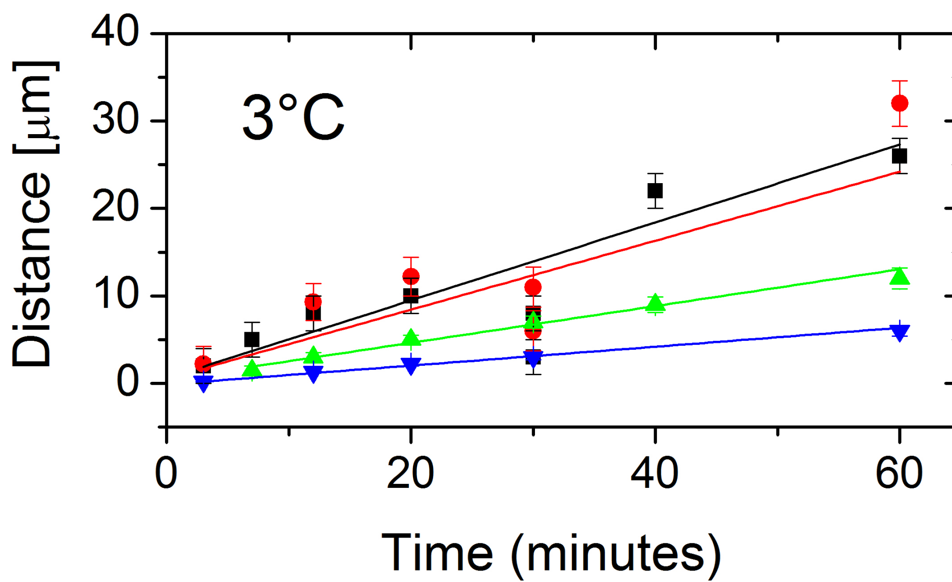
The data for tube depth contains far more variation. For all temperatures, there is an initial period of linear increase, with the rate between 4 and 10 times that of the bulk etch rate. It is interesting to note that at longer time durations, etch tube depth starts to plateau, most noticeably at 25°C. There are some strange data points, notably from the -15°C-100 min, 25°C-10 min, 3°C-30 min and 45°C-7 min samples. For the first two of these, when the maximum possible error is taken into consideration, the deviation from the overall trend is acceptable and certainly not so large as to suggest that the measurement was not conducted properly. The latter two anomalous points lie a long way off the overall trend and to point to an error in the measurement or a problem with the sample, such as the measurement region containing a very low dislocation density.

5.3.3 Repeat etching

The tube diameter is 8.2±0.8μm, based on the average of 8 pits, and the tube depth was measured using the angle lap method at 29±2μm. The experiment was performed twice, and the second attempt yielded results of 7.9±0.8μm tube diameter and 30±2μm for tube depth. When compared with the data from Section 5.3.2, 8±0.8μm and 30±2μm, there is no significant deviation from the result for 20 minutes continuous etching. An image of the repeat etched sample is shown in Figure 5.12.

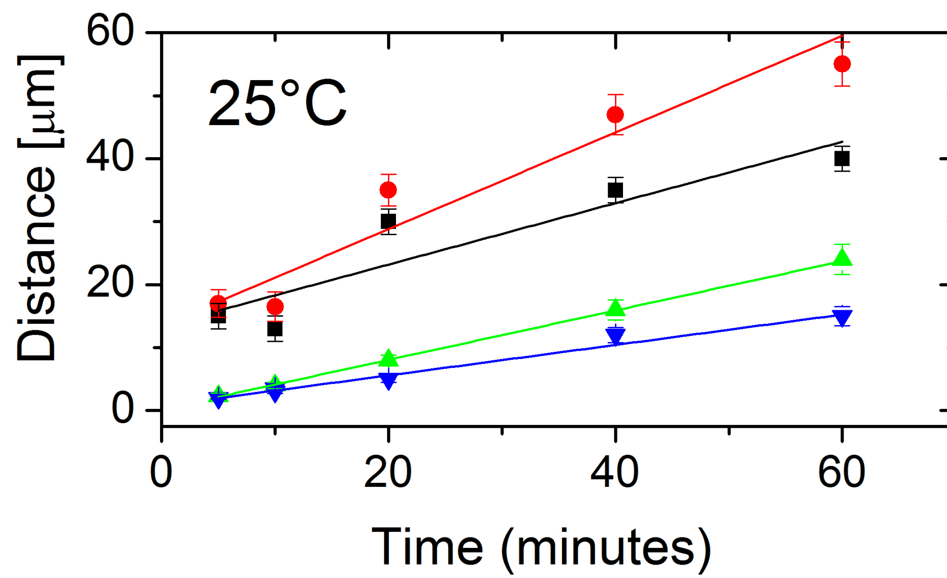
The extent of the repeat etching experiment was limited to this brief investigation, as it became clear after performing it that splitting 20 minutes of etching into ten separate periods had a negligible effect on the etch tube depth (or diameter, as expected). Assuming the hypothesis of reaction products blocking the tubes to be true, these results suggest that either the cleaning process did not remove the products, or that diffusion of reagents through the layer is not a rate determining step. Alternatively, the reaction products quickly diffuse out of tubes during normal, continuous etching, so there is no change in the process by breaking up the etching into steps.

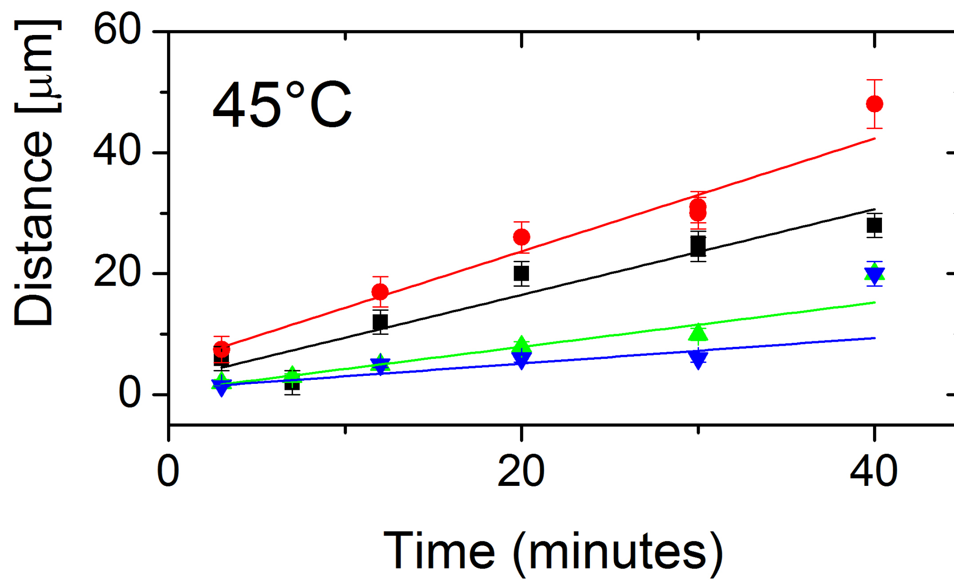




Key
● Tube plus bulk
■ Tube depth
▲ Tube diameter
▼ Bulk etch

Figure 5.10: Plot of Secco etch parameters as a function of time, for -15 and 3°C, including linear best fit lines drawn through Origin.





Key
- ● Tube plus bulk
- ■ Tube depth
- ▲ Tube diameter
- ▼ Bulk etch

Figure 5.11: Plot of Secco etch parameters as a function of time, for 25 and 45°C, including linear best fit lines drawn through Origin.

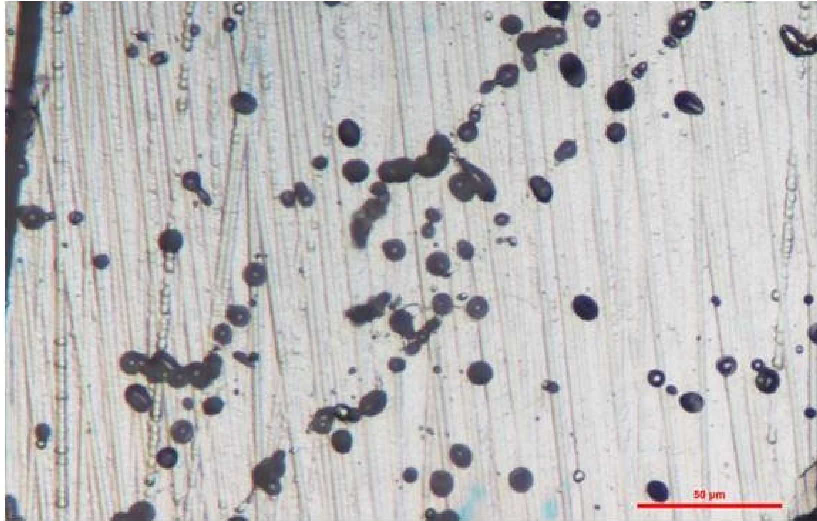


Figure 5.12: Optical micrograph of mc-Si sample after 10 x 2 minutes Secco etching.

5.4 Analysis of data

5.4.1 Introduction

As discussed in Section 2.3.1, etching behaviour may depend strongly on diffusion (which is a thermally activated process) and is therefore frequently characterised by measuring activation energies. In addition, the transition between the two stable states, which in this case are silicon atoms in the bulk (solid) and in solution, also has an activation energy associated with it; this is equal to the height of the potential barrier between the states. In defect revealing etches, the potential barrier for the dissolution of material varies locally depending on defects in the crystal structure (see Section 2.3). The rates at which various etch parameters proceed is determined by an activation energy in the Arrhenius equation:

$$J = J_0 e^{-E_a/kT} \tag{5.1}$$

where J is the reaction rate, J_0 is the attempt frequency, E_a is the activation energy in eV per atom, k is the Boltzmann constant and T is the absolute temperature.

For a given etch parameter, the calculated activation energy is an overall, apparent value that takes into account contributions due to diffusion and reaction rate, and any other un-

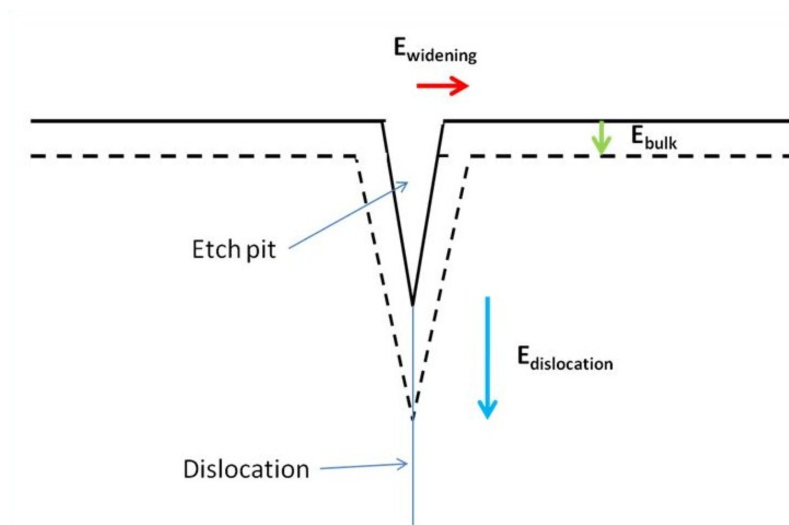


Figure 5.13: Schematic of typical etch pit illustrating the three activation energies that define pit geometry.

known effects. Defining regimes where different processes dominate the observed behaviour will be important in determining a mechanism that explains the results seen in this investigation.

5.4.2 Activation energy

For the Secco system explored in this project, three key activation energies can be defined:

1. E_{bulk},
2. E_{widening},
3. $E_{\text{dislocation}}$.

These are, respectively, the activation energies for bulk etching, for etch pit widening and dislocation etching, and the physical basis for them is illustrated schematically in Figure 5.13. In combination, they control the geometry of the pits/tubes produced by etching.

Before looking at the values of these energies, how the collected data relates to them must be defined. Choosing the rate to be used in Arrhenius calculations is straightforward for the bulk etch rate and widening rate as the relationships are simple proportionalities that hold for all times and temperatures used in the investigation. For dislocation etching, it is more

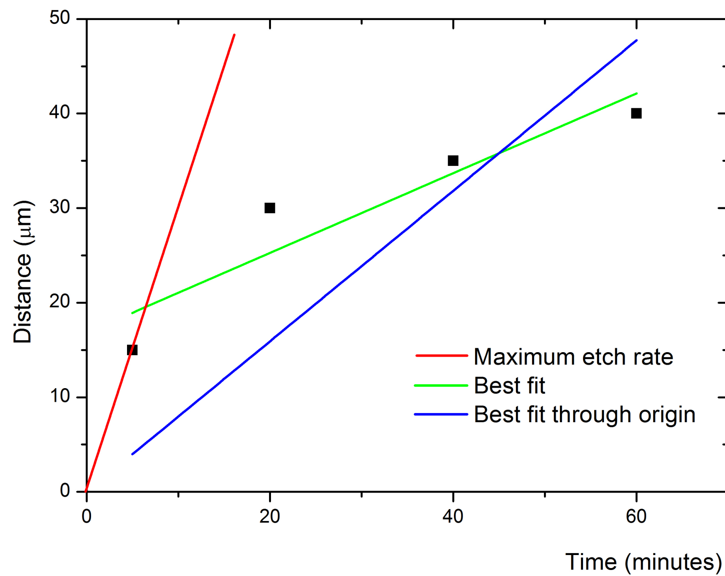


Figure 5.14: Example of possible methods used to calculate gradient for (illustrative) Arrhenius data.

complex, as the reaction rate varies with time. Three dislocation etch rates may be defined for each temperature; maximum, best fit and best fit through origin; each representing the rate at a given time. A schematic of how these terms relate to different measurements is shown in Figure 5.14. The maximum rates are found at t=0 in all cases and are therefore useful for determining the activation energy of the initial etch reaction. Possible reasons for the rate slowing down after this include; the reducing concentration of the reactants, possible build up of reaction products in the tubes, and increased diffusion distance from "fresh" solution to the reaction sites at the bottom of tubes. The activation energy calculated from the best fit lines is more useful for determining the "ongoing" driving force for the reaction, perhaps due to some other process that only becomes important as the pits grow or as the reaction products are formed. The "best fit through origin" results represent an overall rate for the reaction.

5.4.3 Etching mechanisms

The three different dislocation etch rates defined in the previous section allow two distinct analyses to be applied to the data. Firstly, a two stage reaction process, where the initial process is subsequently superseded or changed in some way, may be the best explanation for the behaviour. Therefore, modelling the system with two activation energy regimes is most suitable, and the "maximum" and "best fit" results should be used for this. Alternatively the system can be modelled as a single step with the overall "best fit through origin" results being used.

Arrhenius plots for the bulk etch rate, widening etch rate and dislocation etch rate are shown in Figure 5.15, using the "best fit" data for dislocation etching. These graphs allow the activation energies of the three processes to be calculated, providing information about the relative thermodynamic driving forces. To understand the behaviour fully, this information must be considered alongside the kinetics of the system, as there are many different species involved in the reactions that make up the etching process. Mechanisms of etching are discussed in Section 2.3.1.

By rearranging equation 5.1 and plotting lnJ, where J is the etch rate, against 1/T, the activation energies for the three etch processes can be calculated from their respective gradients as follows:

$$E_a \equiv -k \frac{\partial \ln J}{\partial (1/T)} \tag{5.2}$$

From the data shown in Figure 5.15, the activation energies are 0.30eV, 0.23eV and 0.20eV for the bulk, widening and dislocation etch rates respectively. The quality of the data means that there are clear limitations to the analysis. Only having results for four temperatures, due to the difficulties encountered with developing the angle lapping measurement technique and the limited range of the temperature control system, reduces the scope of any conclusions that can be made. However, it is still a useful approach for explaining some of the observed behaviours.

The alternative way of analysing the dislocation etch rate data, as a two-step process, is

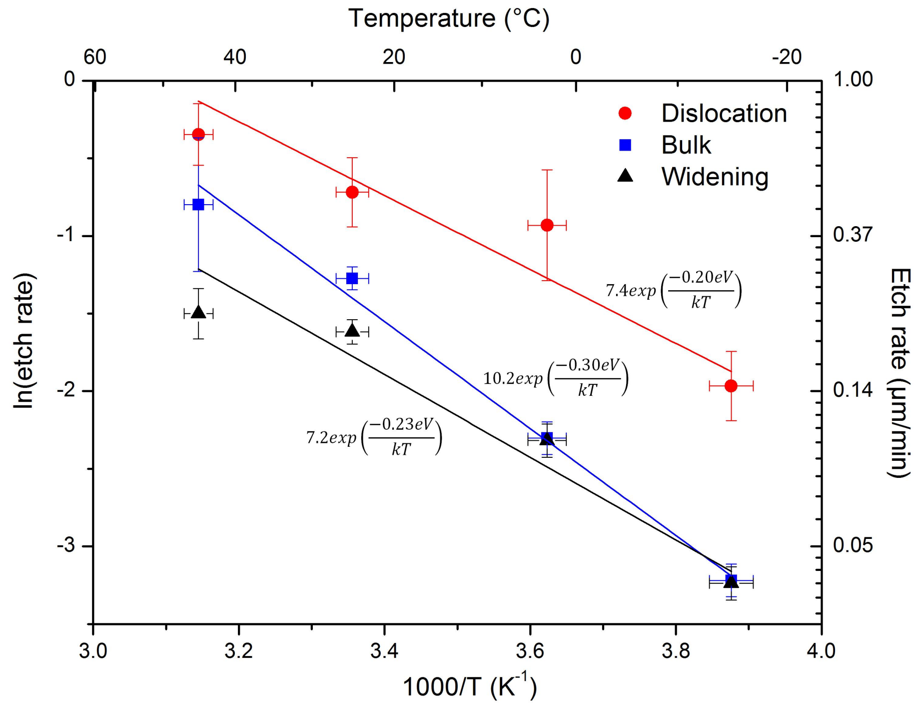


Figure 5.15: Arrhenius plot of bulk, widening and dislocation etch rates.

presented in Figure 5.16. This uses the initial and ongoing dislocation etch rate data and gives activation energies of 0.31eV and 0.20eV respectively. The result is surprising as one may intuitively expect the higher initial etch rate to be characterised by a lower activation energy. This suggests that the attempt frequency may differ between the top and bottom of a tube. Further, the maximum rate observed is at 25°C rather than 45°C, which again is unexpected. For a purely diffusion limited system the expected result is that all reaction rates would increase with increasing temperature.

5.4.4 Aspect ratio

A further metric can be used to look at the etching behaviour: aspect ratio. The aspect ratio of an etch tube is defined as the ratio of the pit depth to the pit diameter. As the pit depth has been measured both with respect to the initial and final surface height, two corresponding aspect ratio calculations are determined, and are shown in Figures 5.17 and 5.18. The plots show that the highest aspect ratios are found at short etch durations. There is no obvious

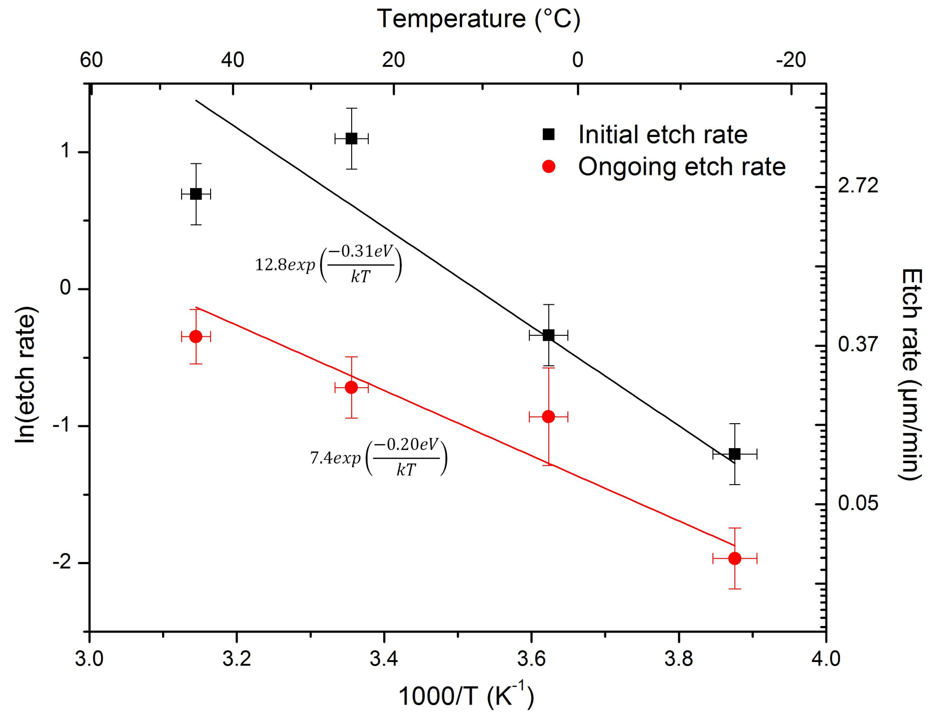


Figure 5.16: Arrhenius plot of initial and ongoing dislocation etch rates.

trend with respect to temperature, and there is a high amount of scatter in these data.

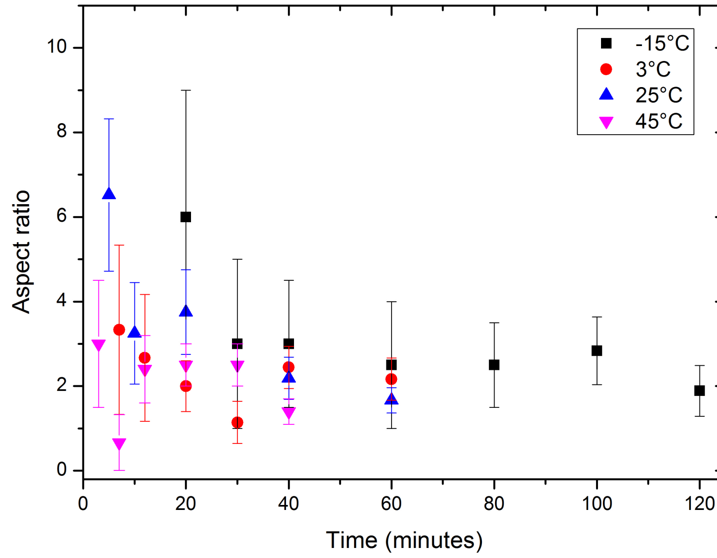


Figure 5.17: Graph of aspect ratio against time, using tube depth relative to the final surface position.

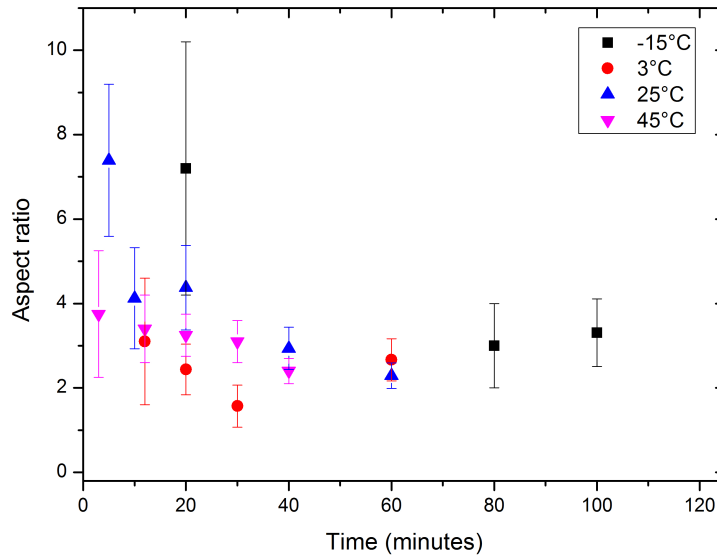


Figure 5.18: Graph of aspect ratio against time, using tube depth relative to the initial surface position (sum of tube depth and bulk parameters).

5.5 Discussion

5.5.1 Micrographs

The optical micrographs in this Chapter show the etch patterns produced by Secco etching and were necessary for measuring pit diameter. They also allow some qualitative insight into the mechanisms of etching. The distribution of pit sizes, with many pits around the maximum size, suggests that as soon as the sample is exposed to the solution, etching starts at all surface defect sites with minimal delay. The extra depth of field afforded by the SEM images confirms that these large pits are deep and somewhat tube-shaped, and also the existence of smaller, very shallow pits. This second type of pit may be due to imperfections in the polished surface, damage likely to have arisen either during one of the diamond polishing stages (see Section 3.1) or simply from handling the samples with tweezers. This deformation from scratching leads to generation of dislocations very close to the surface, which are also revealed by the etch. These are not comparable to the long dislocations that are grown in while the silicon solidifies during casting, and which are the subject of this investigation.

An interesting result from the SEM images is that a small minority of the larger dislocation etch tubes do not run parallel to each other, or normal to the surface. Even within the same grain, with pits less than one micrometer apart, differences in the angle between tube axis and surface normal are observed. If they follow the angle of their corresponding dislocation accurately, this suggests that the dislocations do not all run perpendicular to the wafer surface or even just along certain crystallographic planes. It is reported that dislocations in cast mc-Si "grow with the solid liquid interface vertically through the silicon block" [156], so the angle between a dislocation and the wafer surface normal should be negligible. Even allowing for the fact that poor polishing may have caused the sample surface to differ in orientation from the original wafer surface, the angle between neighbouring tubes such as that seen in Figure 5.7 cannot be explained by this.

The hypothesis of precipitates in the bulk of mc-Si samples possibly "blocking" the etch, first introduced in Section 2.2.2, was not discovered during any of the SEM investigations. An exhaustive search of every tube was not performed, and clearly this non-discovery does not

definitively show that the etch is not affected by *all* precipitates. However, there is a strong probability that, if precipitates are insoluble in Secco etch, one would have been noticed near the surface of one of the tubes in, for example, Figure 5.7. The surface precipitates shown in Figure 5.9 are very likely to be K_2SiF_6, which is deposited during the etching process as previously reported by Nahm *et al.* [157].

Additionally, the shape of the tube walls also offers some insight into the possible mechanism of etching. The scalloped surfaces of the walls suggest that there is a particular rate-limiting step in the process of etching vertically, which is the cause of periodic increased lateral etching. The centre of the etch tube is where the driving force for dissolution of silicon is strongest, due to local energy variation (see Section 2.3) and the small size of dislocation cores. The reaction rate here may be more susceptible to changes in the supply of "fresh" reagent species and reaction products temporarily blocking the site, it is suggested that insoluble K_2SiF_6 is being formed in some cases.

5.5.2 Etch parameters

To make sense of the results presented in the previous section, first the reactions taking place in the etching system must be considered. As discussed in Chapter 2, previous research into etching has provided some results for comparison. For the removal of bulk silicon by a potassium dichromate/hydrofluoric acid etch, an activation energy of 0.34eV was reported [147]. Different etching systems have also produced similar results, the activation energy for bulk etching by planar etch (75 HNO_3, 17CH_3COOH, 8 HF) is 0.28eV [146]. The similarity in these results suggests that silicon etching in general proceeds by a common mechanism.

The non-equality between energies for bulk and widening are somewhat surprising, given that in both cases the same reaction between etch and bulk silicon is occurring. The difference suggests that the environment in the pit may be different to the main body of the solution. If we consider more closely the geometry of an etch tube, the discrepancy between the activation energies of the bulk and widening rates may be explained. As a tube grows vertically downwards due to the increased reaction rate at a dislocation core, widening is occurring at all points on the walls of the tube. The measurement of tube diameter is clearly only made

at the surface, but due to the bulk etching that has already taken place, this final surface is actually a point several micrometers below the original surface. Therefore, initial widening at this point took place at the bottom of a dislocation tube, where the environment is very different to that near the surface.

This can be expanded upon by considering work by Robbins and Schwartz [145], which states that diffusion of reagents to the silicon surface is a key part of etching mechanisms. In this case, rather than a boundary layer, there is likely to be a high concentration of reaction products in the pit and it is possible that the results for pit widening are strongly dependent on diffusion of the dilute dichromate ions through this region, and overall are influenced by both the bulk and dislocation rates. That the value for activation energy of widening lies between the values for bulk and dislocation etching is therefore not surprising.

For dislocation etching, the measured activation energy is the lowest of the three values, in simple terms this makes sense since the etch attacks dislocations most strongly. As mentioned in Section 2.3.1, the etching process depends on a first step of generating holes. It is possible that the dislocations somehow enhance the hole generation, thus enhancing the etch rate. As reported by Wilshaw *et al.* [81] clean dislocations are electrically inactive so for this to be the case electrically active impurities and/or precipitates must be present at the dislocations. Given the impurity levels present in the wafers used for this study, it is likely the dislocations are indeed heavily decorated. Another possible explanation is that the strain energy associated with atoms at dislocations is linked to the increased ease with which the atoms at defects dissolve, it is more energetically favourable for the defect atoms to dissolve as they are already in a higher energy state.

Whether it is related to hole generation or not, there must be some additional driving force causing the rate to be higher at defects that intersect the silicon surface, as the chemical reactions taking place are the same - silicon is being dissolved in all three cases. Föll [154] suggested that differences in electrochemical potential between the silicon at the defects and the bulk silicon matrix are the cause of the different etch rates, this is another way of stating that the atoms at the dislocation core are in a higher energy state.

It is interesting to note that the activation energy for self-diffusion of water is approxi-

mately 0.20eV (between 0 and 55°C) [158]. This value is very similar to the value found in this work for dislocation etching, and given that the diffusion coefficients of dilute solutes in water are similar to that of water self-diffusion [159], it may be the case that the widening process is strongly controlled by diffusion. Further, the activation energy of water self-diffusion is reported to be temperature dependent [160], the variation of diffusion coefficient with temperature is shown in Figure 5.19. If the diffusion processes that control Secco etching are similarly temperature dependent it may be the case that the Arrhenius analysis is unsuitable.

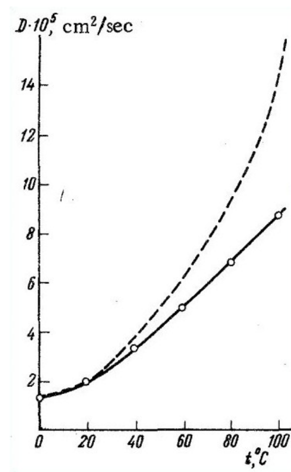


Figure 5.19: Graph of diffusion coefficient with respect to temperature for water self-diffusion. Dashed line represents calculated value assuming activation energy is independent of temperature. Points represent experimental results (after [161]).

The large difference between initial and ongoing etch rates, and the obvious plateauing of the tube depth, suggests a two-stage mechanism may exist. However, the data in Figure 5.16 is not of the highest quality - the high initial etch rate observed at 25°C causes a lot of the increased activation energy that is calculated.

The aspect ratio results show a trend of decreasing ratio as time increases. If a model is proposed where, after a long duration of etching, the widening rate at the "open" top of a tube is likely to be similar to the bulk etch rate, yet the dislocation etch is now limited by diffusion of reagent species from the solution above the surface, this result may be explained. It is likely that at very long etch durations a steady state will be found, where the diffusion limit slows the dislocation rate such that it is equal to the bulk rate, and the bottom of the pit does not move relative to the surface. If the problem is simplified to one of one-dimensional

vertical diffusion, as illustrated by the simplified diagram in Figure 5.20, an equation for the etch rate can be deduced. Starting from Fick's First Law of Diffusion, converting the flux to a rate is achieved by dividing through by the atomic density of silicon and the ratio of the ionisation change between silicon and the oxidising species.

$$J = -D\frac{\partial C}{\partial x} \tag{5.3}$$

$$V = \frac{-D}{AZ}\frac{\partial C}{\partial x} \tag{5.4}$$

where J is the flux, V is the etch rate, D is the diffusivity, C is the concentration, A is the atomic density, Z is the ionisation ratio and x the distance. Making the following assumptions about the system allows a value for V to be estimated:

- Desired etch tube length of 100μm.
- Diffusivity of ions in water = 10^{-5}cm^2/s.
- Atomic density of silicon is 5x10^{22}cm^{-3}.
- Minimum concentration for reaction to proceed (found at bottom of tube) is equal to 60% of initial concentration.
- Z = 4/3, as the ionisation change of Cr is 3, and of Si is 4.

Performing the calculation results in an approximate value for etch rate of 20μm per hour. The maximum dislocation etch rate for Secco etch at room temperature is 180μm per hour, falling to around 40, both of which are significantly higher. In order for a high aspect ratio tube to be achieved, systems with a lower etch rate are required, as this will keep the reaction proceeding at the bottom of the tube and avoid excessive widening at the top.

The final experiment in this Chapter, repeat etching, was an attempt to discover whether the drop-off in etch rate with respect to time was due to reaction products blocking the etch tubes. This produced results comparable to those achieved using the normal procedure. It is therefore likely that the rate decrease is not due to this effect.

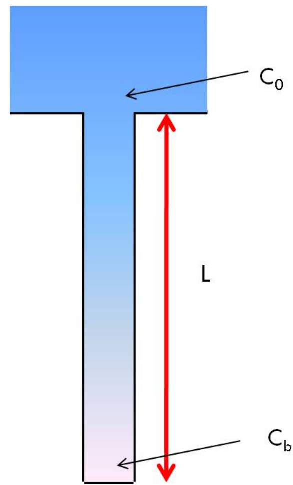


Figure 5.20: Schematic of simplified model diffusion system in a dislocation etch tube.

5.6 Summary

The behaviour of silicon in Secco etch was investigated in this Chapter, using the angle lap technique to measure etch parameters over a range of temperatures. In addition, optical and scanning electron microscope characterisation was performed on the samples post-etching. Secco etch is shown to remove dislocation cores at depths up to 40μm, but the corresponding bulk material removal and tube diameters are large - aspect ratios of around 3 are typical. SEM images confirm the tubular geometry and that the bulk is strongly attacked. In order to meet the criteria of this project, an alternative etch with a lower bulk etch rate is required.

Chapter 6

Dislocation removal by anodic etching

6.1 Introduction

The main conclusion of Chapter 5 is that using a chemical etch to remove dislocation cores (whilst minimising removal of bulk silicon) is successful only for low dislocation depths. The etch tubes become increasingly wide as they deepen; aspect ratio decreases with increases in depth and time. This is unsuitable when compared to the stated aim of removing dislocations throughout the top 100μm of wafers (see Section 2.2), so an alternative etching method is required.

One such process is anodic etching, which is a technique developed in 1980 by Helmut Föll [154] with the aim of revealing defects based on their electrical activity. In summary, an electrochemical cell is constructed with silicon biased as the anode, and the etching is controlled by the potential applied through a dilute hydrofluoric acid electrolyte. As with chemical etching, the technique was developed purely for observing defects, so it is likely that the optimal conditions for dislocation removal are different to anything yet reported (for further details, refer back to Section 3.3 and Figure 3.3). Unlike chemical etching, where the driving force for a reaction is fixed by the electrochemical potential of the oxidising agent, here it can be varied by altering the potential applied across the cell. This affords the possibility of

tailoring the reactivity such that only certain defects are etched, potentially leading to much higher aspect ratio pits. In this Chapter, some preliminary results are presented in which anodic etching is used to remove dislocations from mc-Si samples

6.2 Development of suitable etching process

Initial testing with the electrochemical cell showed that there was very little etching behaviour at the sub-hour times used by Föll [154]. Much longer durations proved successful so were used for the results reported in this section. Etch times used were 20, 40, 50 and 100 hours. Etching was initially performed with no *applied* voltage, with the actual voltage across the sample therefore the difference in potentials between the platinum electrode and the mc-Si sample (see Figure 3.7). Föll produced successful results using values for the applied voltage of 0.5V and -0.4V (on top of the built-in voltage of 0.7V). These were both used but did not produce etching behaviour, typically staining the sample surface or in some cases dissolving it completely. Other tests where the current was fixed produced similar results. Föll's results could not be reproduced.

Due to the design of the electrochemical cell (see Section 3.3.1), larger mc-Si samples were needed compared with chemical etching such that the cell remained sealed at the bottom. As cast square 156mm wafers were laser cut into 16 square 39mm segments by the supplier, REC Wafer. Polishing these large mc-Si samples to the required damage-free condition was extremely difficult compared to the smaller samples in the previous Chapter. Frequent breakages and uneven surface finish resulted in a very low yield of usable wafers and were stalling the etch experiments. In order to obtain samples with a suitable surface quality, 10 quarter wafers were sent to Kemet International's Flat Lapping division for polishing. Unfortunately, although the sample surfaces appeared to be damage-free, the wafers were again macroscopically uneven and warped. In addition, they were subjectively much more fragile, this was put down to the reduced thickness of the wafers as Kemet's method removed more material. Without a flat top surface, the angle lapping dislocation depth measuring process will not produce accurate results, so the warped material was used for trialling new etch conditions,

as at a microscopic level the surface was suitable for observing the etch patterns.

Due to these difficulties preparing suitable specimens, and the issues recreating the results seen by Föll [154], the investigation into anodic etching was not as comprehensive or systematic as planned. Angle lap data were unavailable for many of the conditions used, and applying fixed potentials or currents did not lead to etching behaviour in a lot of cases. The data collected are limited to a range of optical and scanning electron micrographs, from which the tube diameter was measured, and where available the tube depth is included.

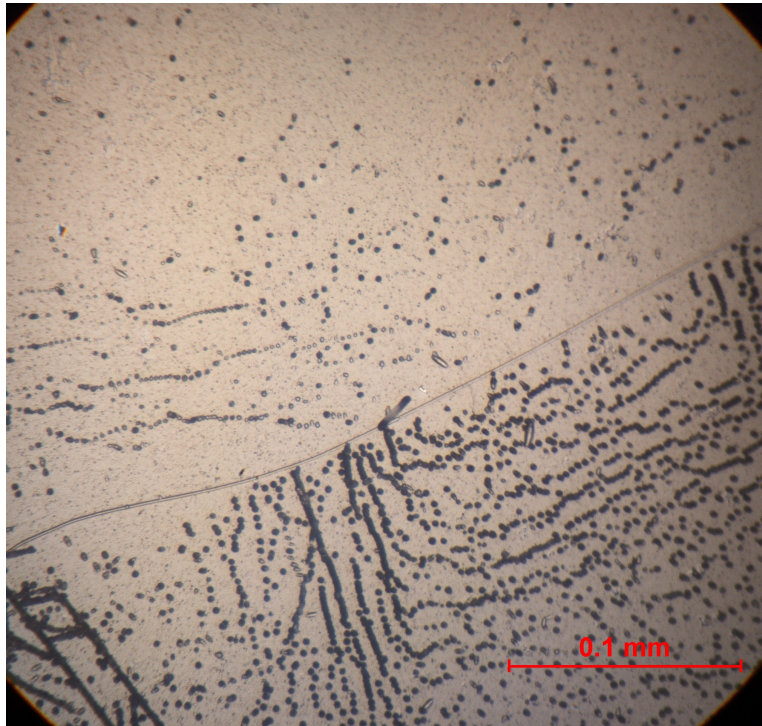
In addition to the etching investigation, experiments on the polarisation behaviour of both Cz-Si and mc-Si samples were undertaken (see Section 2.3.2 for a review of previous work). The aim of these was to further the understanding of the anodic etching behaviour, in particular the difference between the results seen in previous reported work [154] and the initial attempts in this project. The polarisation experiments were performed using 40ml buffered HF ($6NH_4F$:1HF) as the electrolyte. After the polarisation experiments were analysed, and with the three electrode cell (see Section 3.3.1) now available for use, a further attempt at performing etching with a fixed current applied was undertaken.

6.3 Results

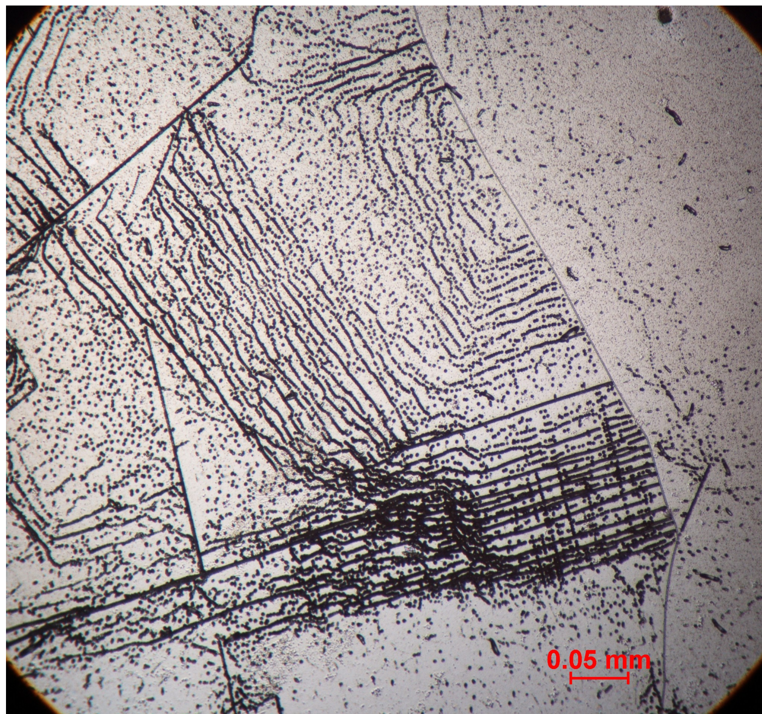
6.3.1 Optical microscopy

Figures 6.1(a) and 6.1(b) are images of different regions of the same sample, etched for 20 hours with no applied potential. The resulting etch pattern is very similar to those produced by the Secco etch, with a tube diameter of $1\pm0.5\mu$m being equivalent to less than 5 minutes Secco etching at 25°C (compare with Figure 5.3(a)). This result suggests that the widening rate for anodic etching under these conditions is over 100 times lower than for Secco etching. Figure 6.1(b) shows that grain boundaries are weakly etched, and both micrographs also show very clearly the difference in dislocation density between two neighbouring grains.

Figure 6.2 is an optical micrograph of a sample etched with no applied potential for 40 hours, showing increased etching of both dislocations and grain boundaries compared to the 20 hour sample. The tube diameter in this case being $3\pm0.5\mu$m. This image also shows a



(a) Optical micrograph of mc-Si anodically etched for 20 hours with no applied potential, showing etching of dislocations.



(b) Optical micrograph of mc-Si anodically etched for 20 hours with no applied potential, showing etching of dislocations and grain boundaries.

Figure 6.1: Optical micrographs of mc-Si samples anodically etched for 20 hours.

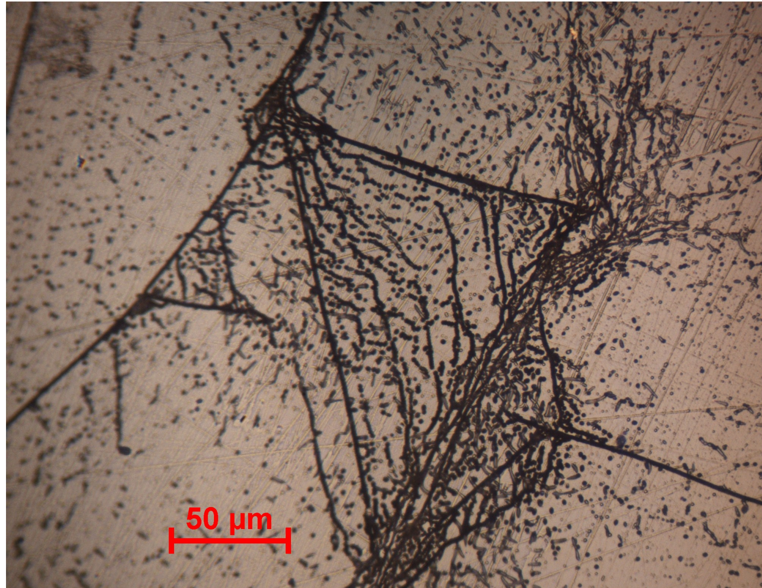


Figure 6.2: Optical micrograph of mc-Si anodically etched for 40 hours with no applied potential, showing etching of dislocations and grain boundaries.

larger number of smaller, shallower pits, similar to those highlighted in Figure 5.4(b). The tube depth was measured for this sample using the angle lap technique, with a result of $20 \pm 5 \mu$m (note that the increased error compared to measurements in the previous Chapter is due to the sample not being macroscopically flat, therefore the reference plane against which the depth is measured (see Section 4.3) is defined with less accuracy).

Figures 6.3 and 6.4 are images of the sample etched for 50 hours. The former shows that the etching at this duration is very heavy, with the dark regions evidence that etch tubes are impinging on each other. Figure 6.4 again shows a mixture of etch tubes and the very shallow pits. The diameter of the etch tubes was measured to be $5 \pm 0.5 \mu$m.

The etching behaviour after 100 hours (with no applied potential) appears very different to that shown by shorter durations, and was inconsistent across the sample. Grain boundaries are still etched strongly, producing noticeable steps and trenches at the interfaces, as shown in Figure 6.5, yet there is almost no evidence of dislocation etch tubes over most of the sample. A limited example of very weak dislocation etching is observed in Figure 6.7, yet the tube diameter, at under 2μm, is less than that observed in the 40 and 50 hour samples. The bulk surface (between the grain boundaries) has been strongly attacked and appears textured, as

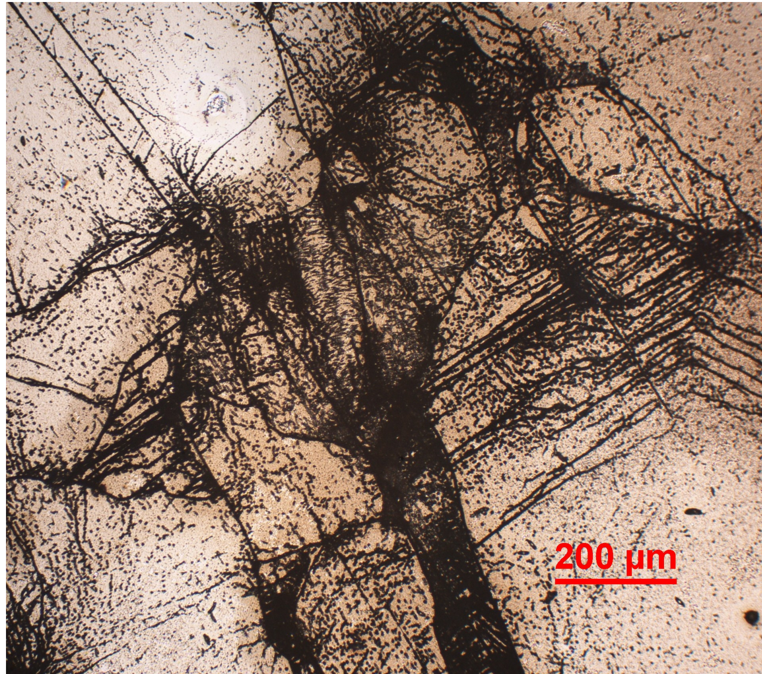


Figure 6.3: Optical micrograph of mc-Si anodically etched for 50 hours with no applied potential, showing strong etching of dislocations and grain boundaries.

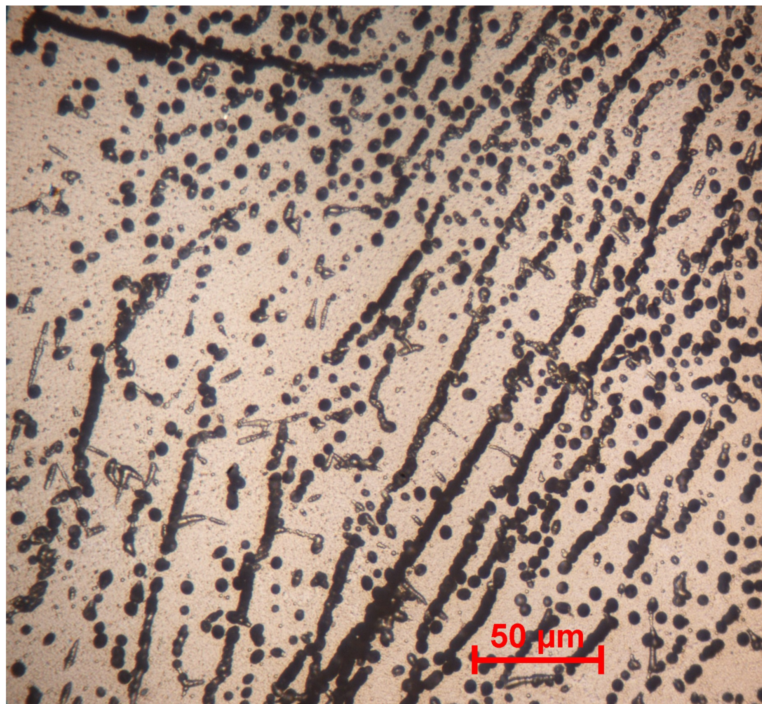


Figure 6.4: High magnification optical micrograph of mc-Si anodically etched for 50 hours with no applied potential, showing dislocation etch tubes.

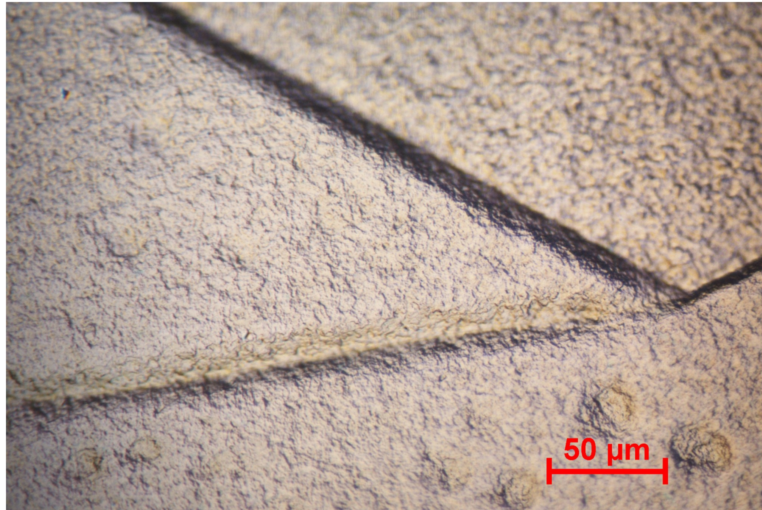


Figure 6.5: Optical micrograph of mc-Si anodically etched for 100 hours with no applied potential, showing strong etching of a grain boundary.

Figure 6.6: Optical micrograph of mc-Si anodically etched for 100 hours with no applied potential, showing rough surface texture.

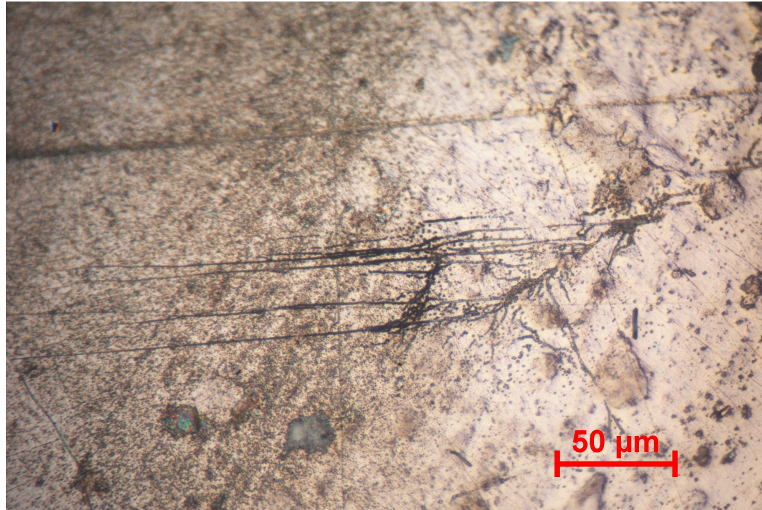


Figure 6.7: Optical micrograph of mc-Si anodically etched for 100 hours with no applied potential, showing small (<2μm diameter) dislocation etch pits.

shown in Figure 6.6.

6.3.2 Scanning electron microscopy

SEM micrographs were taken of the 20, 40 and 100 hour samples. The tube diameters were measured approximately, using the on-screen scale bars.

Figure 6.8 shows that both dislocations and grain boundaries are etched under the conditions of 20 hours, no applied voltage. The geometry of the etch tubes produced by these conditions is shown in Figure 6.9. They appear quite deep, but also seem to proceed down into the material via a network of tubes rather than a single continuous one. The tube width of 1μm is very similar to that measured in the optical micrographs in the previous section.

Figure 6.10 is an SEM micrograph of an mc-Si sample after anodic etching with no applied voltage for 40 hours. It shows etching of both dislocations and grain boundaries. Figure 6.11 is a high magnification image of the same sample, showing a series of dislocation etch tubes. The diameter of the tubes is approximately 2.5μm, again this matches quite well with the result obtained from the optical micrographs. The connected tubes in the centre of the image have a very round shape with steep sides and appear very deep, even with the increased depth of field available in an SEM the bottoms of the tubes are not visible. This image therefore does not contradict the angle lap measurement of 20μm from the previous section.

As expected, based on the optical micrographs, the SEM images of the sample etched for 100 hours are quite different to the 20 and 40 hour examples. Figure 6.12 shows a mix of elongated, shallow pits (approximately 3-5μm wide and 5-25μm long) and smaller rectangular pits. A high magnification view of the rectangular pits is shown in Figure 6.13, giving the size as approximately 2μm square, and an apparently shallow depth. Figure 6.14 shows an array of rectangular pits, possibly delineating a grain boundary, which appear deeper.

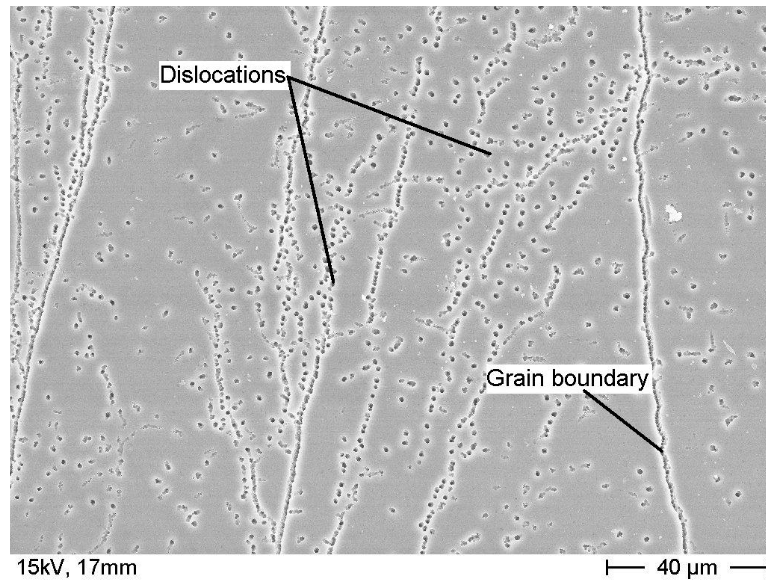


Figure 6.8: SEM micrograph of mc-Si sample anodically etched for 20 hours, showing etching of grain boundaries and dislocations.

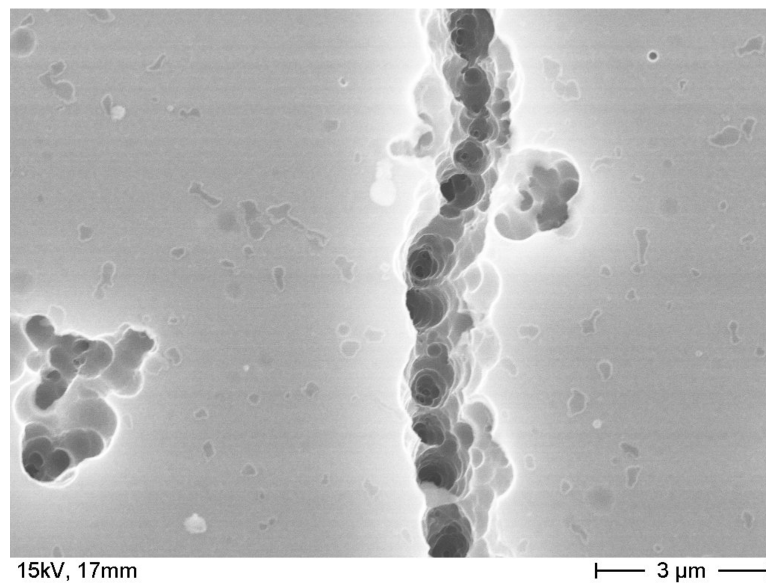


Figure 6.9: High magnification SEM micrograph of mc-Si sample anodically etched for 20 hours, showing etching of a grain boundary.

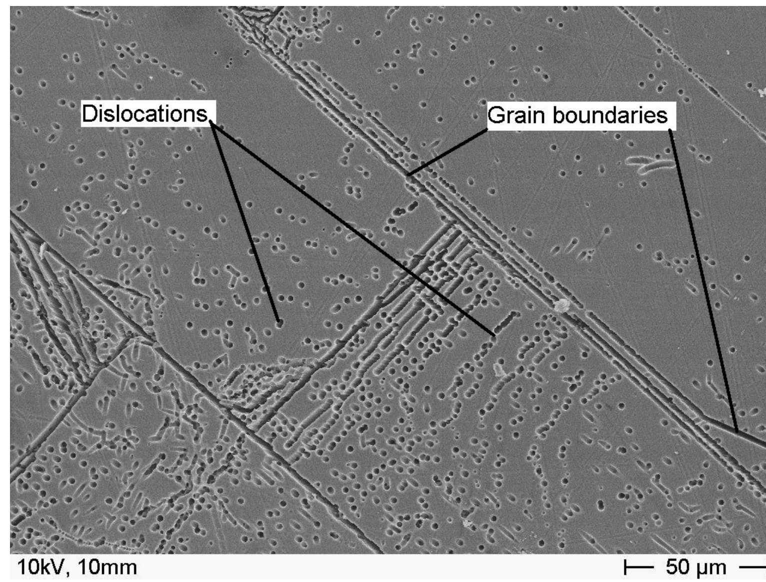


Figure 6.10: SEM micrograph of mc-Si anodically etched for 40 hours, showing etching of grain boundaries and dislocations.

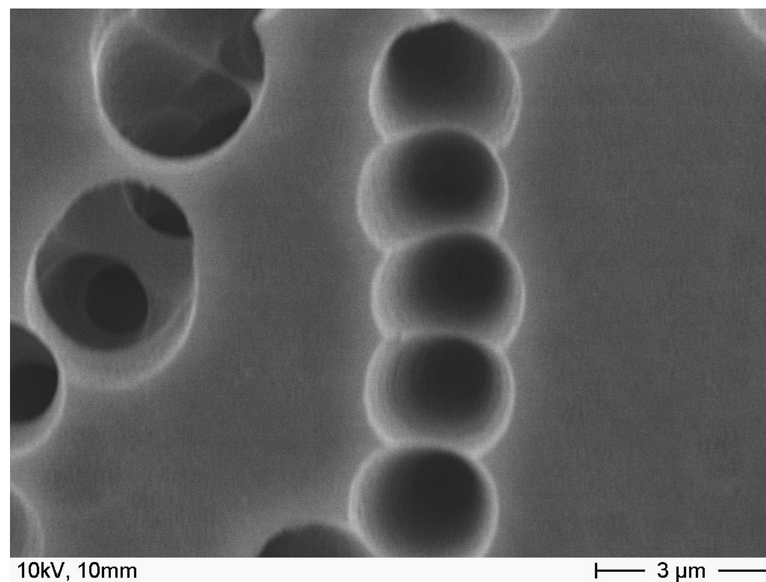


Figure 6.11: High magnification SEM micrograph of mc-Si anodically etched for 40 hours, showing an array of dislocation etch tubes.

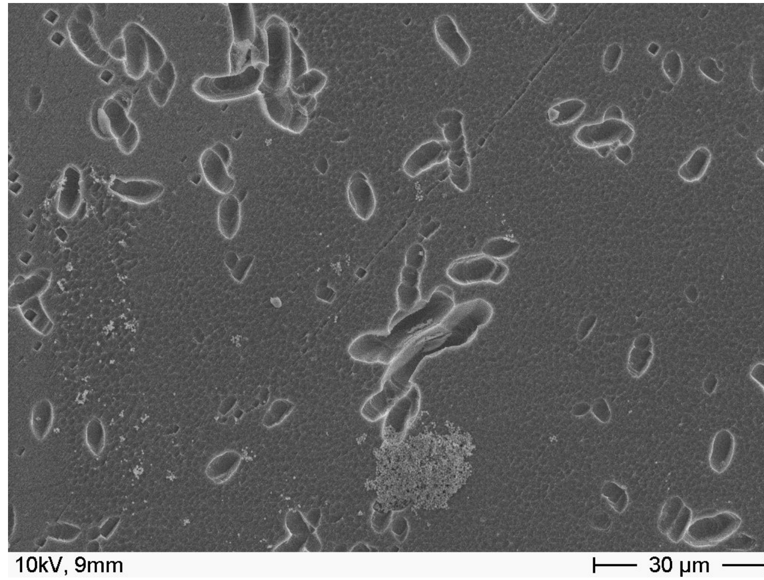


Figure 6.12: SEM micrograph of mc-Si anodically etched for 100 hours, showing mixture of large oval, and small rectangular, etch pits.

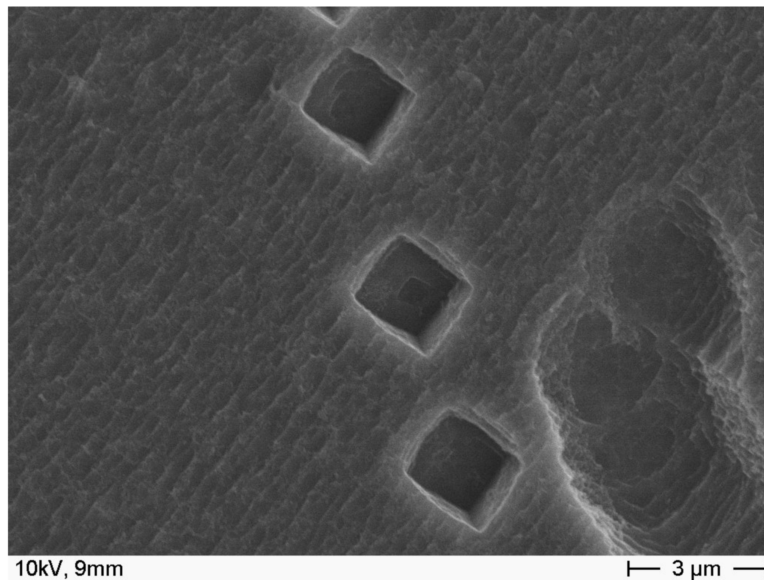


Figure 6.13: High magnification SEM micrograph of mc-Si anodically etched for 100 hours, showing rectangular etch pits.

6.3.3 Polarisation

Polarisation curves for both Cz-Si (p-type, 17Ωcm) and mc-Si (see Section 3.1.1 for specification) samples are shown in Figure 6.15. Corresponding Tafel plots of potential against the natural logarithm of the absolute current are also included in Figure 6.16.

Both curves in Figure 6.15 show similar characteristics to those in Figure 2.7, and the sudden jump in current here is due to the bulk dissolution of silicon that takes place at a certain potential. When combined with the schematic in Figure 2.9, and the accompanying discussion on relative energy levels of defects, the result for mc-Si suggests that fixing the current at around 10μA would hold the system at a point where the dissolution of bulk silicon would be very low, and possibly allow only defects to be attacked strongly, thus maximising the aspect ratio.

To test this hypothesis, an mc-Si sample was etched for 65 hours with the current held at 10μA. Optical micrographs from various areas of the resulting surface are shown in Figures 6.17 to 6.20. Figure 6.17 shows a region where dislocations have been etched, with a tube diameter of 1±0.5μm. Figure 6.18 shows that grain boundaries are also etched, plus many elongated, shallow pits are present throughout this region. The dislocation tubes appear darker and better defined, and have a diameter of 1.5±0.5μm in this case. Figure 6.19 shows no evidence of dislocation etching, but stronger delineation of grain boundaries and twins than the previous images. Figure 6.20 shows very weak dislocation etching, with a tube diameter that is not easily measurable using the microscope software, it is definitely under 1μm. All these observations suggest that the etching behaviour varies across different regions of the same sample, much like the samples where there was no fixed current or potential.

The very small diameter tubes are promising, as they suggest that a high aspect ratio may be achievable. However, in this case the angle lap could not measure a tube depth, so it can be concluded that the depth is below the detection limit of approximately 2μm. This leads to a maximum aspect ratio of 2, which is again not high enough.

6.4 Discussion

Overall, the optical microscopy results show that the anodic etching behaviour of mc-Si is inconsistent, and that the technique is difficult to precisely control. The strength of etching observed across samples varied and many of the attempted experiments did not produce useful defect etching at all. This suggests that the process may be highly sensitive to very small changes in a number of variables, such as current, potential, pH and electrolyte composition. The 20, 40 and 50 hour samples analysed in this section did show evidence of the desired etch tubes, but based on the limited data from this investigation their geometry and size is comparable to those achieved using Secco etch (at much shorter etch durations).

Compared to Secco etch, the geometry of the tubes produced in the 20, 40 and 50 hour samples is very similar. They are of circular cross-section and the walls are relatively steep-sided. Most tubes are aligned approximately with the normal to the sample surface. Based on the very limited available data the etch tube depths and aspect ratios also appear similar. However, a number of differences exist between the sets of samples. The extra detail in the SEM images shows that the bulk surface between defects remains free from etching (compare with Figure 5.8). Extending the etch duration to 100 hours, with the intent of further increasing the tube depth, instead produced very strangely shaped etch pits. It is possible that once the tubes grow to a certain size, they modify the local charge distribution such that dissolution of silicon does not continue to take place at defects, rather the tubes widen at the surface and develop into shallow pits.

The polarisation work provided some additional insight into the anodic etching process, suggesting the potential at which bulk etching is 'activated'. However, the additional fixed current anodic etching result that followed on from it produced very small diameter but very shallow etch tubes.

6.5 Summary

This Chapter contains the results of an investigation into anodic etching. It was found that the conditions under which anodic etching takes place were very different to those previously

reported, and that, despite a large difference in etch rate, the resulting etch tubes and pits were very similar to those found by Secco etching. The ability to vary the applied potential to control the way process of etching defects and bulk silicon was not fully explored.

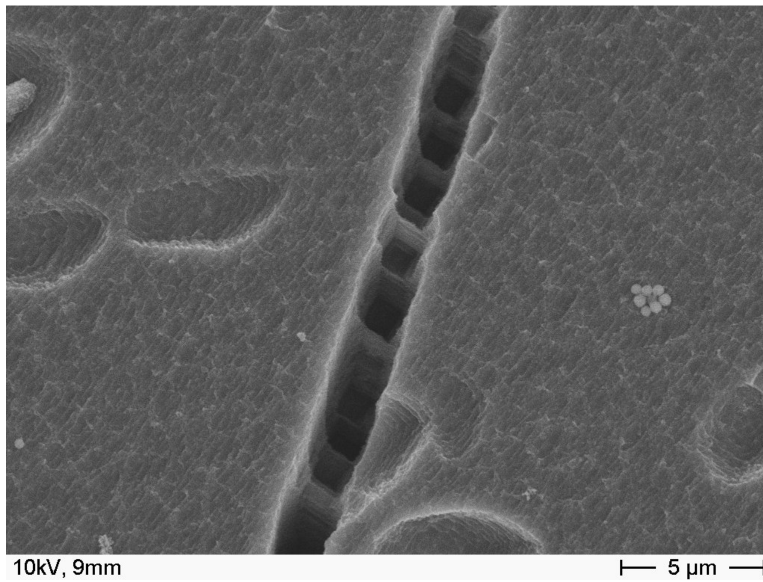
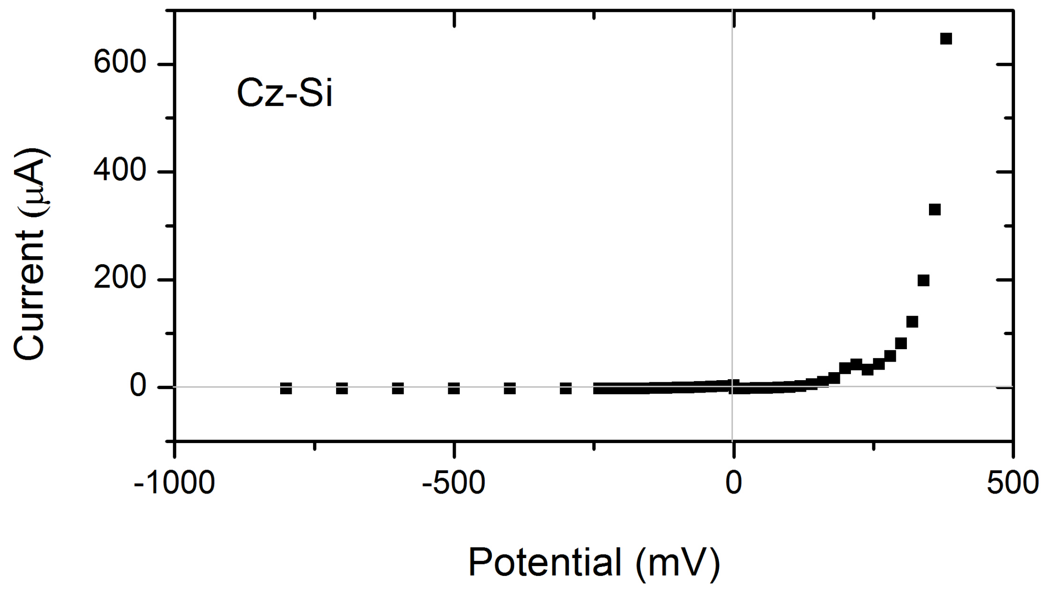


Figure 6.14: High magnification SEM micrograph of mc-Si anodically etched for 100 hours.



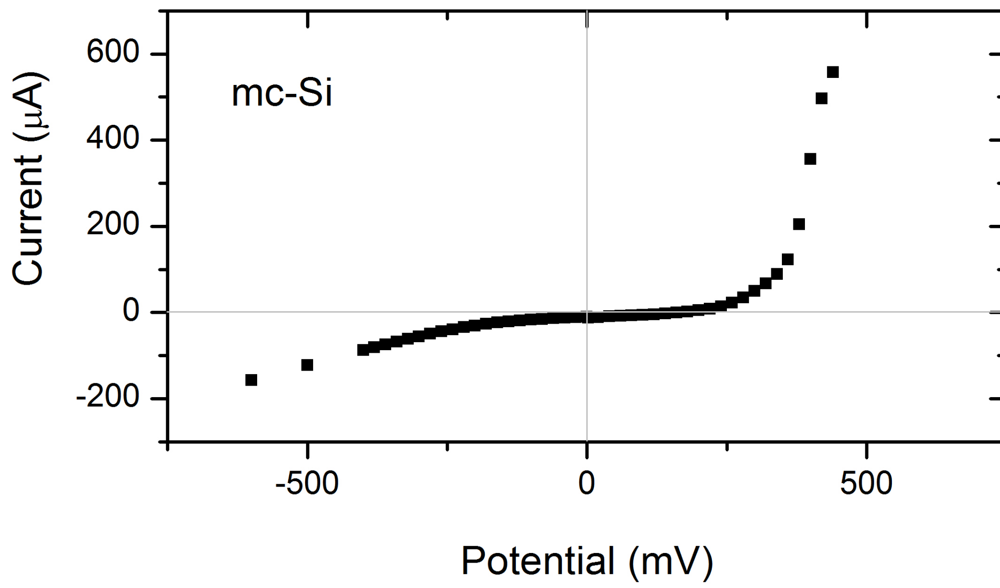


Figure 6.15: Polarisation curves for Cz-Si and mc-Si samples in buffered HF electrolyte.

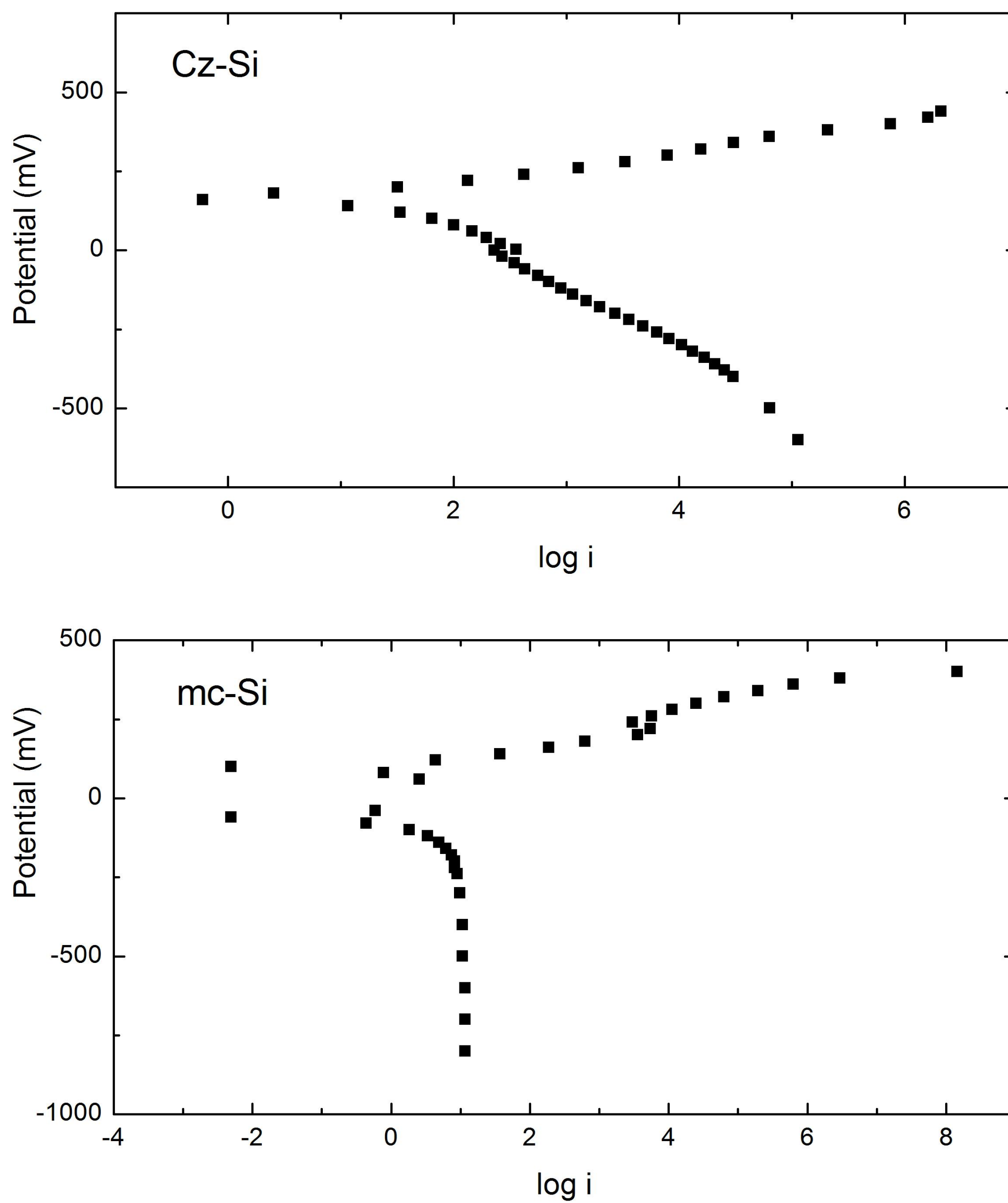


Figure 6.16: Tafel plots for Cz-Si and mc-Si samples in buffered HF electrolyte.

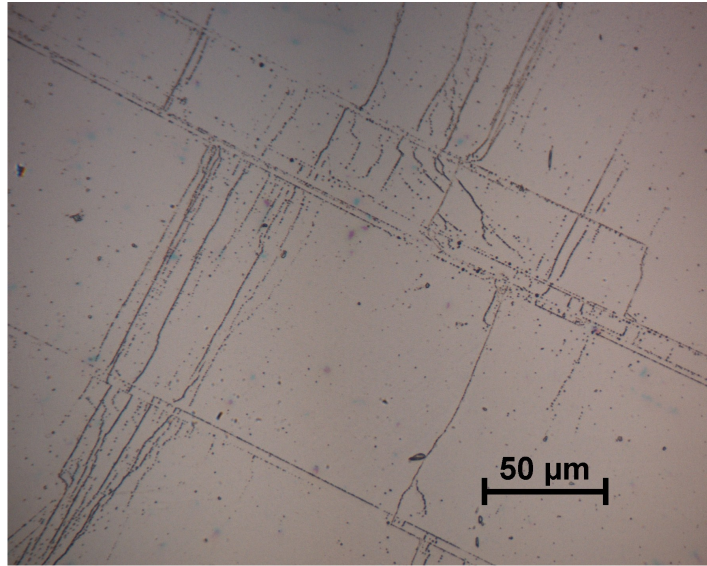


Figure 6.17: Optical micrograph of mc-Si sample after 65 hours anodic etch at 10μA, showing etching of dislocations.

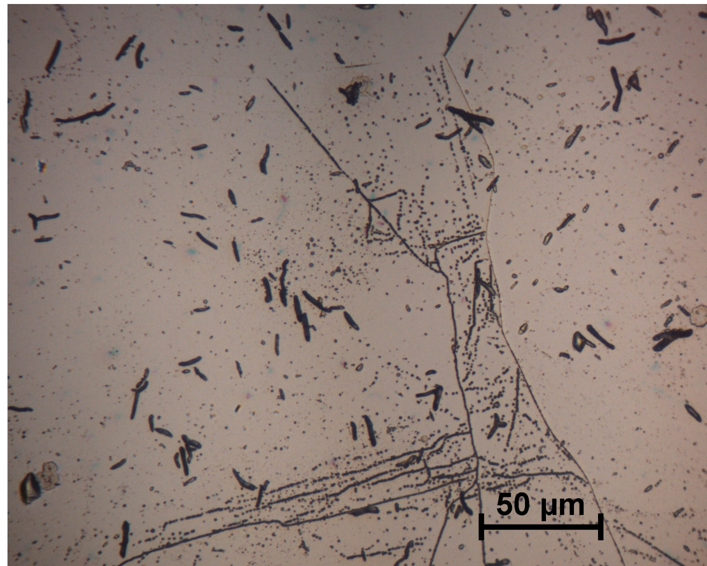


Figure 6.18: Optical micrograph of mc-Si sample after 65 hours anodic etch at 10μA, showing etching of dislocations and grain boundaries, plus elongated pits.

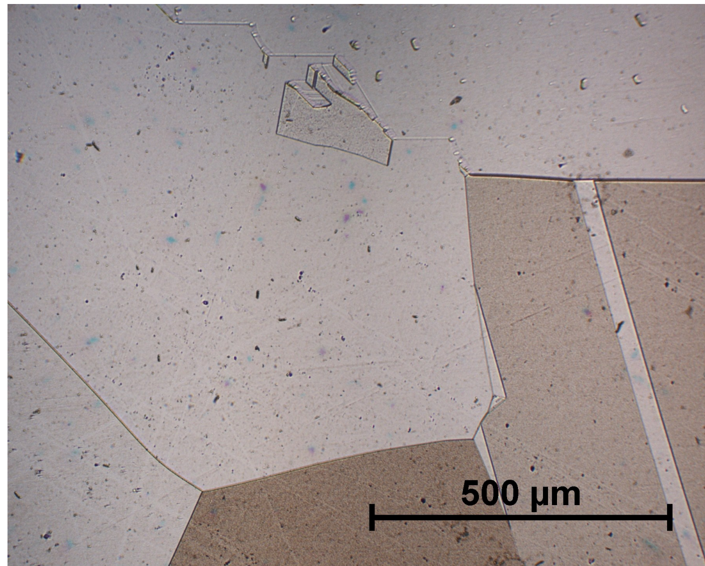


Figure 6.19: Optical micrograph of mc-Si sample after 65 hours anodic etch at 10μA, showing only etching of grain and twin boundaries.

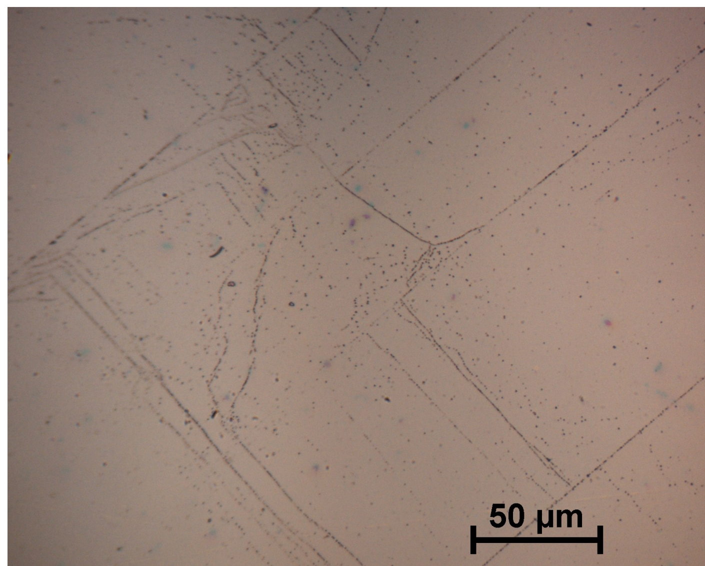


Figure 6.20: Optical micrograph of mc-Si sample after 65 hours anodic etch at 10μA, showing very weak dislocation etching.

Chapter 7

Possible alternative etches to remove dislocation cores

7.1 Introduction

The results of Chapters 5 and 6 showed that neither Secco nor anodic etching produced sufficiently high aspect ratio tubes. This Chapter contains results from a brief experiment looking into possible alternative etches for dislocation core removal. These etches will be based on oxidising agents that have not previously been used for defect etching, with an aim of increasing aspect ratio through improving etch selectivity.

The idea for these experiments grew from the result that Secco etch, with potassium dichromate as the oxidising agent, causes both the bulk silicon and silicon at dislocations (and other defects) to be etched, and these processes occur at different rates (producing etch pits/tubes due to the higher rate at defects). This can be summarised schematically in an energy diagram, shown in Figure 7.1.

If the strength of oxidising agent in the etch was reduced, could an etch that still reacts with silicon at defects but only very weakly with bulk silicon be designed? Typical defect revealing etches were designed and optimised to quickly show the defect distributions of samples, so it is possible that many slower acting solutions that produce similar etching exist but have never been used in this way. In this Project the requirements are different and long

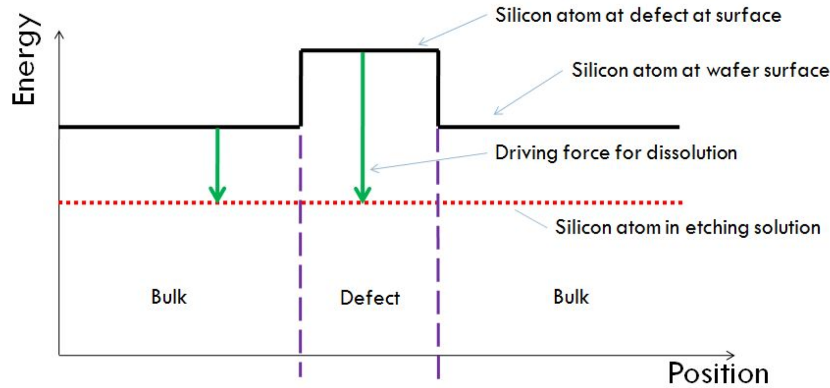


Figure 7.1: Schematic diagram of energy level theory for defect etching, showing increased driving force for silicon dissolution at defect sites compared with the bulk material.

etching times, although not desirable, are not impossible to work with.

The first step in this process is identifying the possible alternative oxidising agents. The main focus was on species that have lower standard electrode potentials than the Cr^{6+} to Cr^{3+} ($E^{\circ}_{25} = 1.33V$ [162]) reaction, plus were readily available and safe to use. The chemicals chosen were:

- Iodine, I_2
- Potassium permanganate, $KMnO_4$
- Potassium iodate, KIO_3
- Iron (III) chloride, $FeCl_3$

The corresponding redox reactions and their standard electrode potentials are as follows:

- $I_2(\text{in KI(aq)}) + 2e^- \rightarrow 2I^-(aq)$, $E^{\circ}_{25} = 0.54V$ [163]
- $Fe^{3+}(aq) + e^- \rightarrow Fe^{2+}(aq)$, $E^{\circ}_{25} = 0.77V$ [163]
- $2IO_3^-(aq) + 12H^+(aq) + 10e^- \rightarrow I_2(aq) + 6H_2O(l)$, $E^{\circ}_{25} = 1.19V$ [163]
- $MnO_4^-(aq) + 8H^+(aq) + 5e^- \rightarrow Mn^{2+}(aq) + 4H_2O(l)$, $E^{\circ}_{25} = 1.51V$ [163]

The reaction of permanganate (Mn^{7+}) to Mn^{2+} clearly has a standard electrode potential that is slightly higher than that of the chromium transition in Secco etch, but was added

for comparison as potassium permanganate was available in the laboratory, and also because on decomposition MnO_2 is formed. This is also an oxidising agent with a lower standard electrode potential of 1.23V for the Mn^{4+} to Mn^{2+} reaction.

7.2 Methodology

Experimental conditions that closely matched the Secco etching experiments in Chapter 5 were devised. The mc-Si samples were from the same supply of REC wafers and polished to the same surface quality as described in Section 3.1. The concentration of the oxidising agent in Secco etch, potassium dichromate, is 0.15M. However, this is then diluted by the addition of two parts hydrofluoric acid, resulting in a final concentration of 0.05M. The same procedure was followed for the alternative etches, with 0.15M solutions of the oxidising agents in water made up individually, then diluted with HF when required for etching. Rather than the 30ml solutions used for Secco etching, 60ml batches were used in this investigation as each mc-Si sample was etched alongside an equal-sized Czochralski silicon single crystal (Cz-Si) control specimen (p-type, 17Ωcm), maintaining the same volume of solution per sample. Observation of the control specimens was necessary to confirm that any surface patterns observed on the mc-Si test samples were due to etching of defects rather than other factors.

It should be noted that iodine is not sufficiently soluble in elemental form to achieve a final concentration of 0.05M, therefore potassium iodide, KI, was used instead, to provide the iodide ions in the correct concentration. A solution saturated with iodine was also used. It was only possible to dissolve 0.02g of iodine in the 60ml solution leading to a final concentration of approximately 0.003M.

Initial tests with these solutions showed that etching was indeed requiring longer durations before any effect was noticed, in the range of hours rather than minutes. Therefore, the samples were observed and photographed in the optical microscope after etching times of 1 hour and 16 hours. These were chosen to allow any relatively fast acting effects that occur in the first hour to be observed, along with any very slowly developing outcomes. In the event of potential etch tubes being formed and observed, additional durations will be

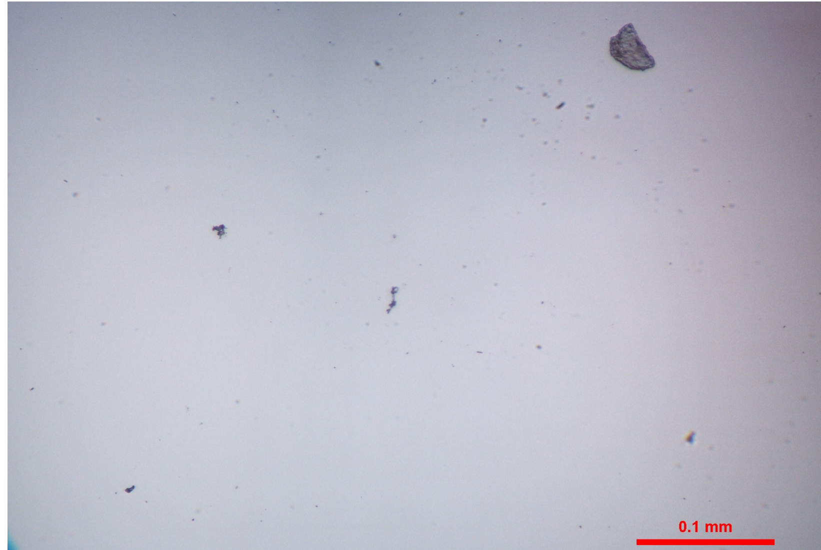


Figure 7.2: Optical micrograph of mc-Si sample after 1 hour in 0.003M iodine, showing negligible etching behaviour.

investigated to provide a fuller picture of the behaviour. The temperature was not varied in these experiments, and was controlled at 22±2°C by performing the etches in an air-conditioned part of the laboratory.

7.3 Results

The main results from this brief investigation are micrographs of the resulting surface after the etching is performed. Optical micrographs of all samples are presented, with additional SEM micrographs used to highlight some key features.

7.3.1 Iodine

Figure 7.2 shows that very little etching is evident after 1 hour exposure to the 0.003M iodine solution. Areas across the whole sample were investigated, with the same outcome. However, after 16 hours the case is very different, with etch pits visible across the whole sample, as shown in Figures 7.3 and 7.4. The etch patterns produced strongly resemble those achieved using Secco etch (and other defect revealing etches), with dislocations, twin boundaries and grain boundaries all preferentially attacked. Figure 7.5 shows that the pits appear much

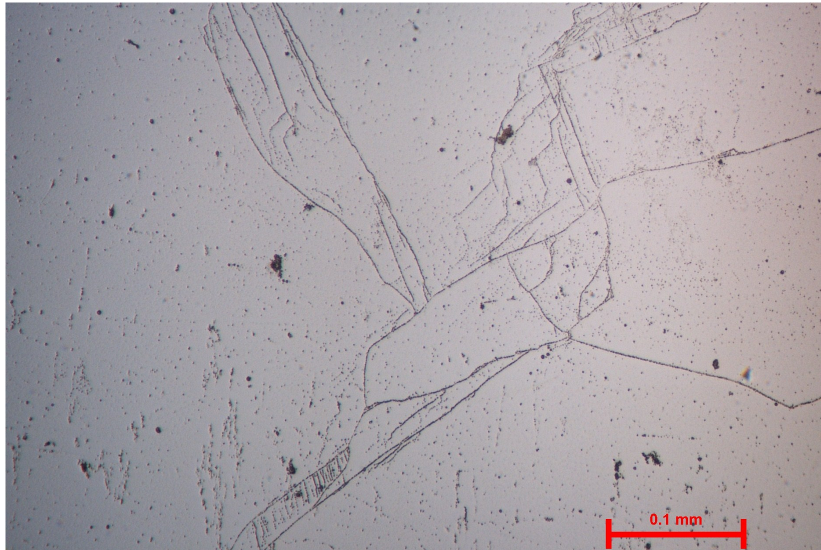


Figure 7.3: Optical micrograph of mc-Si sample after 16 hours in 0.003M iodine, showing etching of dislocations and grain boundaries.

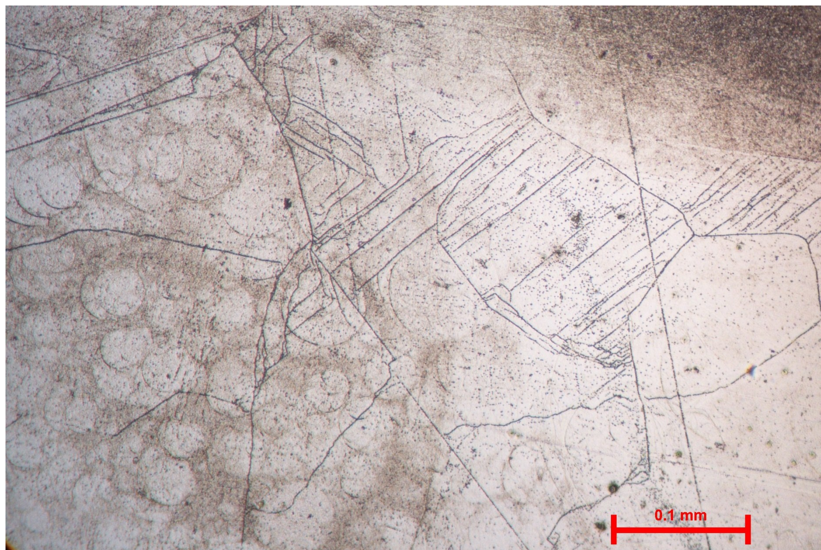


Figure 7.4: Optical micrograph of mc-Si sample after 16 hours in 0.003M iodine, showing etching of dislocations and grain boundaries, plus some staining.

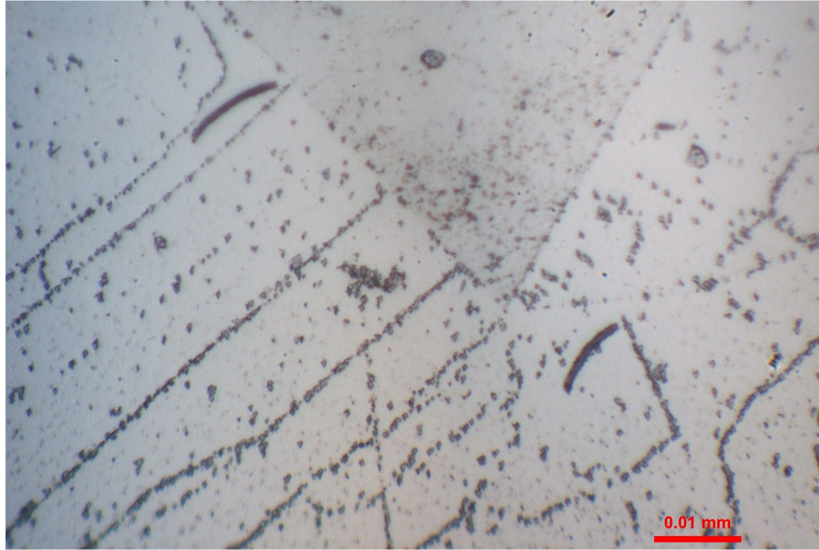


Figure 7.5: High magnification optical micrograph of mc-Si sample after 16 hours in 0.003M iodine, showing shallow etch pits with an irregular geometry.

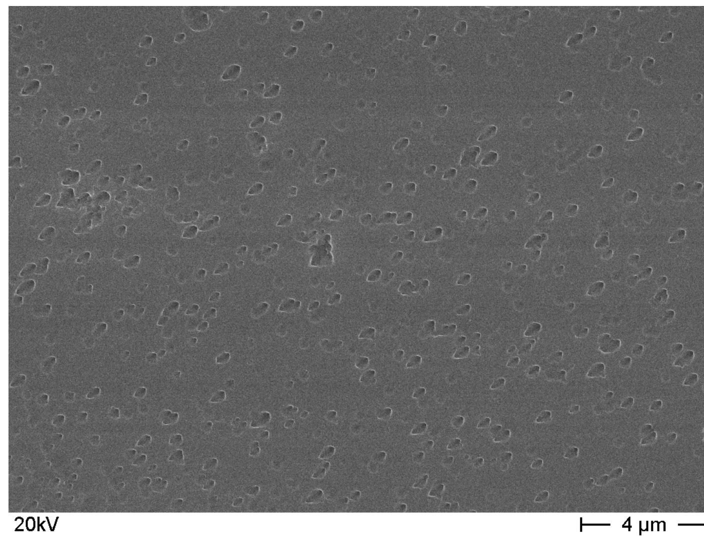


Figure 7.6: SEM micrograph of mc-Si sample after 16 hours in 0.003M iodine, showing dislocation etch pits.

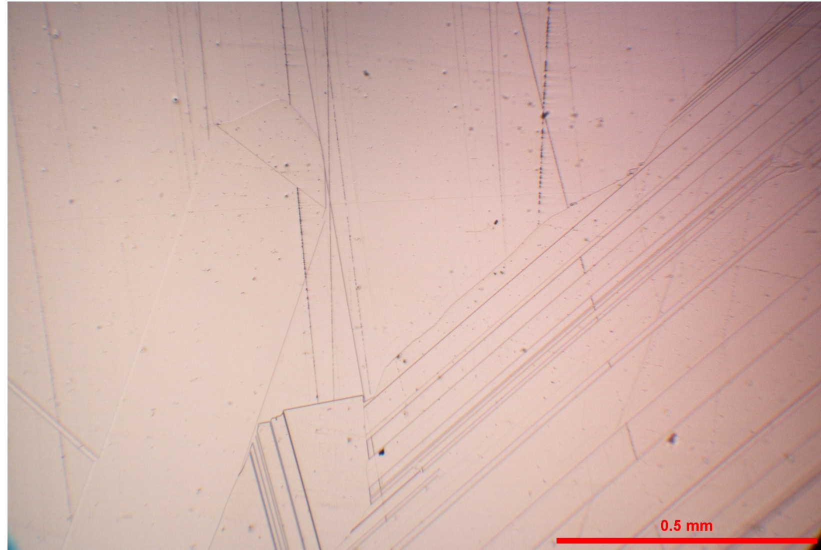


Figure 7.7: Optical micrograph of mc-Si sample after 1 hour in 0.05M potassium iodide, showing etching of twin and grain boundaries.

more shallow than those produced by Secco etching, and also that the shape of the pits is less rounded and regular (compare with Figure 5.3(b)). The jagged, shallow quality of the pits is shown in more detail by the SEM micrograph in Figure 7.6.

7.3.2 Potassium iodide

Figure 7.7 shows that for 0.05M potassium iodide, evidence of etching is visible after one hour, although it is limited to twin and grain boundaries and the effect is quite weak. After 16 hours the effect is observed more strongly, but still only at twin and grain boundaries, as shown in Figure 7.8. The staining that is seen in this image was representative of much of this sample, and makes identifying the presence of individual dislocations difficult. An image of some Czochralski silicon subjected to the same etching conditions (Figure 7.9) shows that many of the visible marks are not related to dislocations, but merely an effect of being exposed to the solution for long periods.

7.3.3 Potassium permanganate

Figures 7.10 and 7.11 are images of mc-Si and Cz-Si samples that have been subjected to one hour in a 0.05M potassium permanganate etch. The former shows strong evidence of

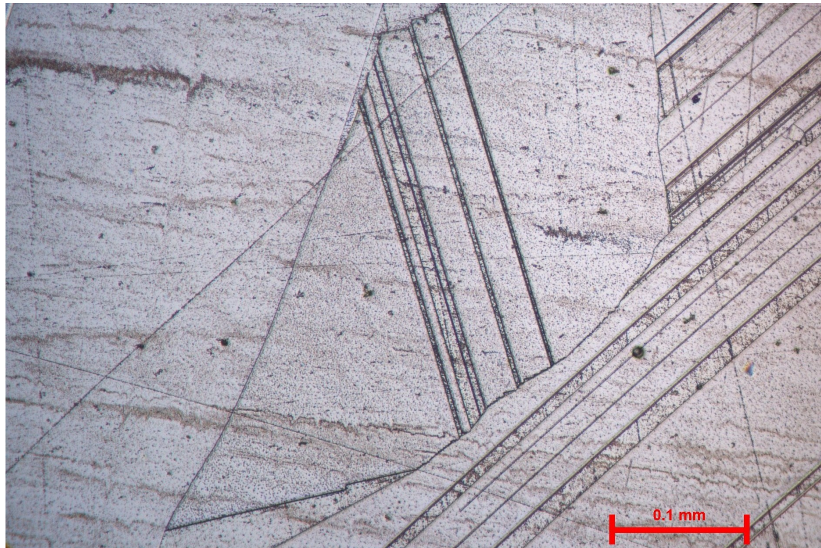


Figure 7.8: Optical micrograph of mc-Si sample after 16 hours in 0.05M potassium iodide, showing etching of twin and grain boundaries, plus some staining.

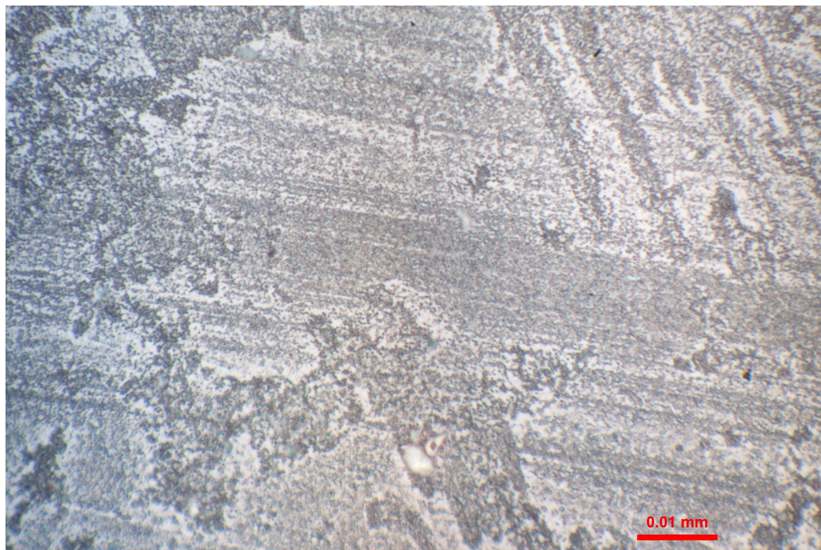


Figure 7.9: Optical micrograph of Cz-Si control sample after 16 hours in 0.05M potassium iodide, showing extensive staining.

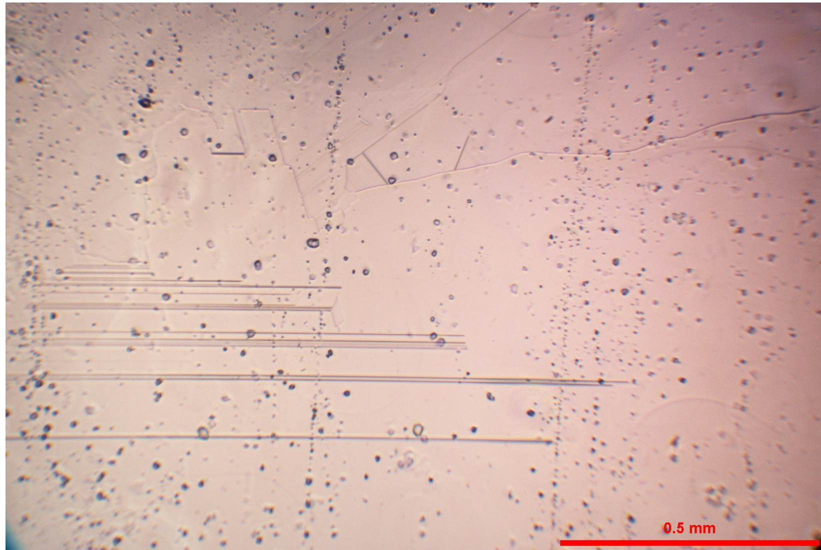


Figure 7.10: Optical micrograph of mc-Si sample after 1 hour in 0.05M potassium permanganate, showing etching of twin and grain boundaries.

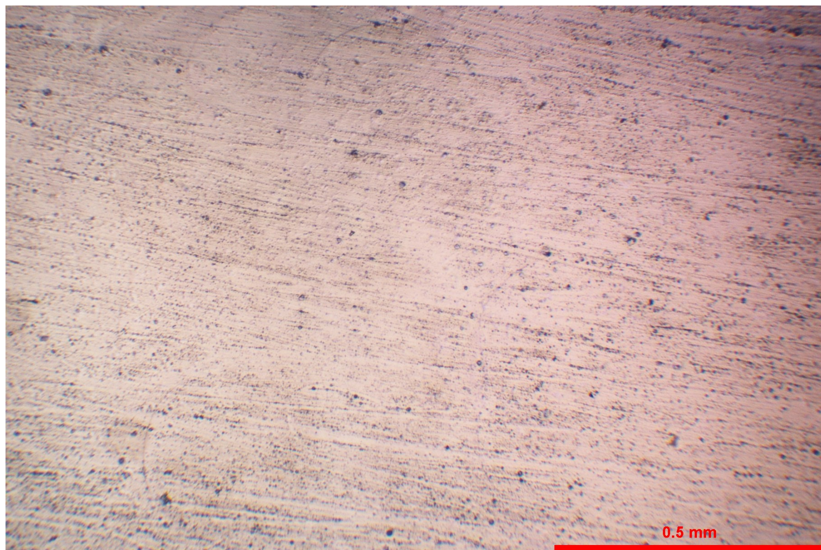


Figure 7.11: Optical micrograph of Cz-Si control sample after 1 hour in 0.05M potassium permanganate, showing staining.

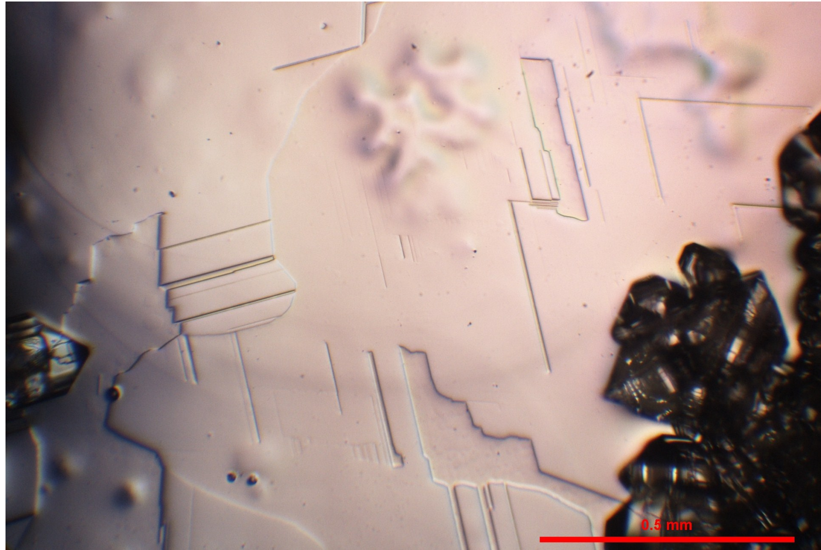


Figure 7.12: Optical micrograph of mc-Si sample after 16 hours in 0.05M potassium permanganate, showing etching of twin and grain boundaries, plus crystalline deposits.

twin boundary etching (the parallel lines in the bottom-left of the micrograph) and some weak grain boundary etching in the centre. The dark circles throughout the image initially appear to be dislocation etch pits, although their distribution is unlike any seen previously. However, comparison with Figure 7.11 shows that these are also found in material with no appreciable dislocation density, so are likely to be a form of stain. After 16 hours, the etching pattern appears quite similar, with clear delineation of both twin and grain boundaries, and no obvious dislocation etching, as shown by Figure 7.12. In addition, crystalline deposits are observed in the bottom-right of the image.

7.3.4 Potassium iodate

Figure 7.13 shows that, after exposure for one hour, 0.05M potassium iodate reveals the grain structure of mc-Si and delineates twin boundaries, and that the bulk silicon surface is also strongly attacked and becomes textured. In Figure 7.14, the dark circles throughout the image appear quite similar to dislocation etch pits, although the pattern does not appear like a typical mc-Si defect distribution. An image of the Cz-Si control sample is shown in Figure 7.15, and similar features are observed, suggesting that the circular marks are a surface texture resulting from the reaction with potassium iodate, rather than defect etching.

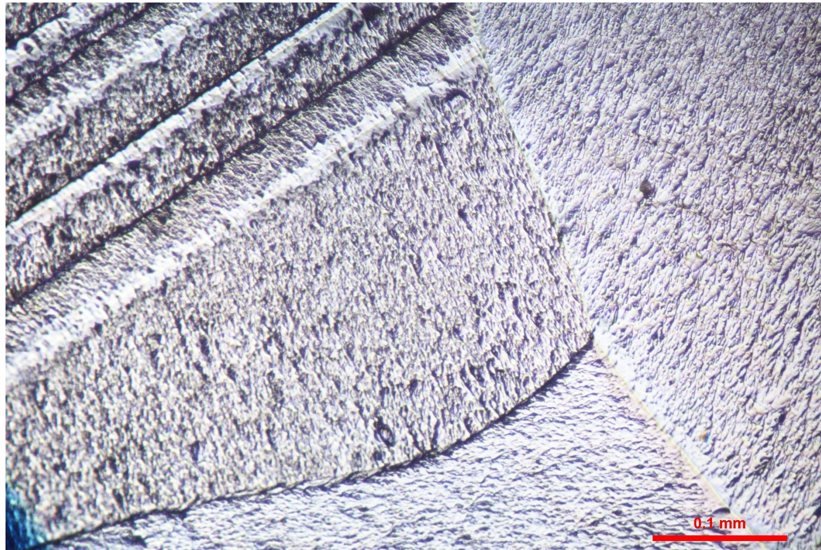


Figure 7.13: Optical micrograph of mc-Si sample after 1 hour in 0.05M potassium iodate, showing etching of twin and grain boundaries, and texturisation of the surface.

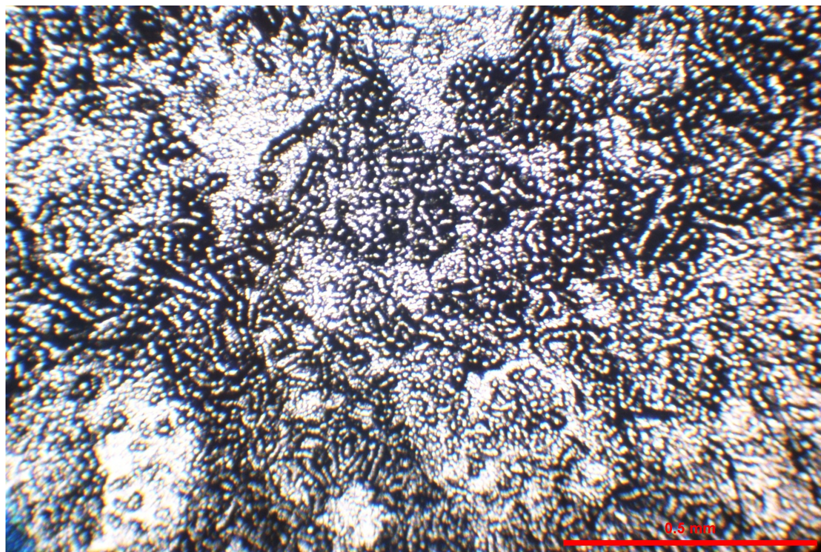


Figure 7.14: Optical micrograph of mc-Si sample after 1 hour in 0.05M potassium iodate, showing possible dislocation etch pits.

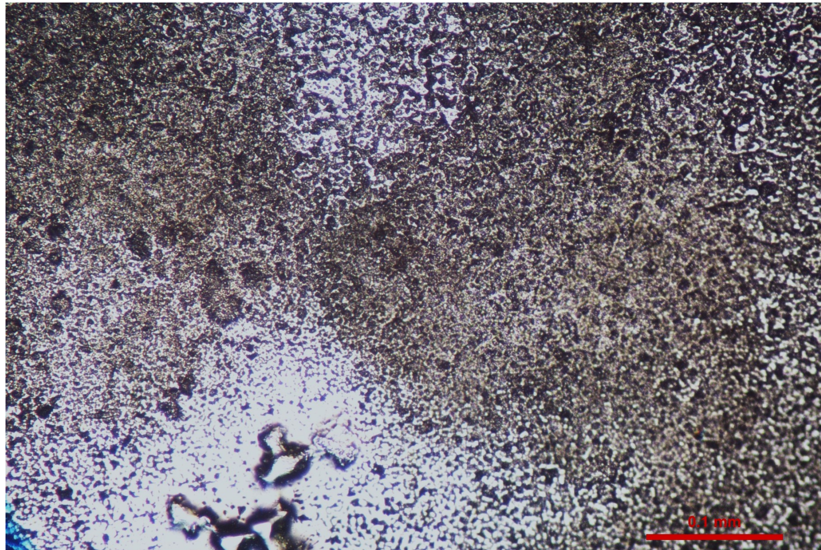


Figure 7.15: Optical micrograph of Cz-Si control sample after 1 hour in 0.05M potassium iodate, showing the resulting surface texture.

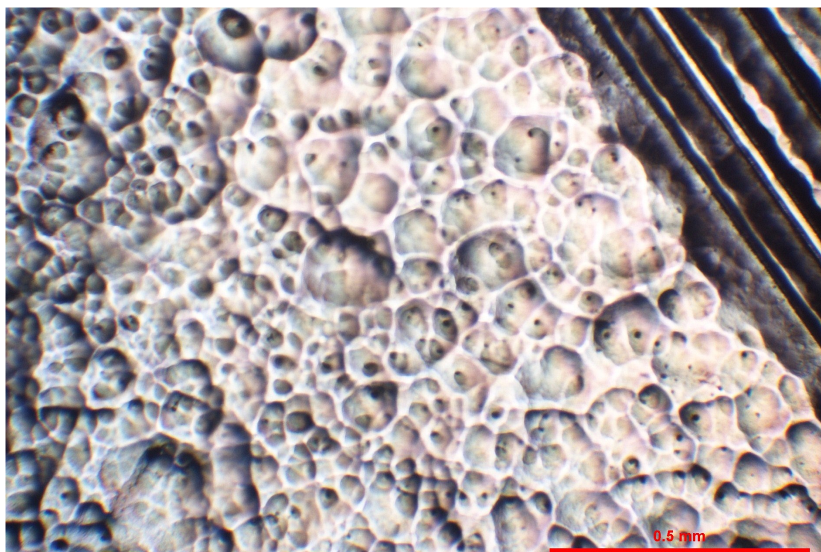


Figure 7.16: Optical micrograph of mc-Si sample after 16 hours in 0.05M potassium iodate, showing etching of twin boundaries and texturisation of the surface.

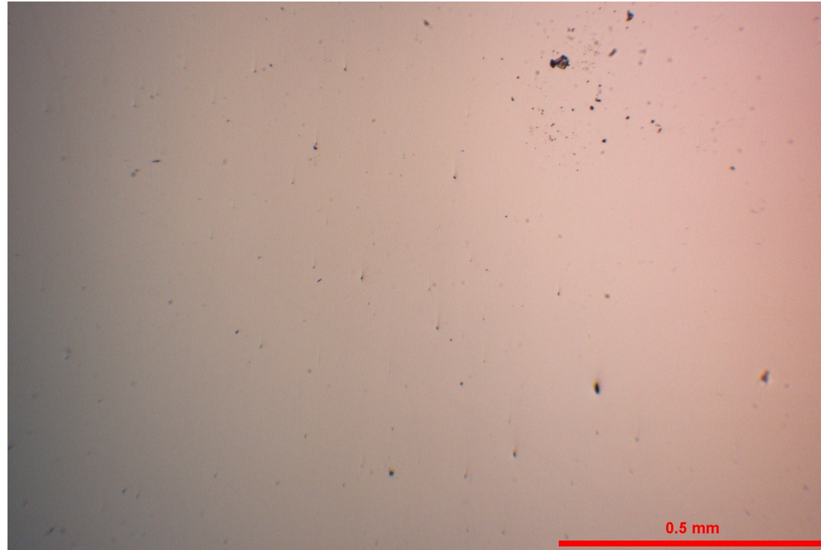


Figure 7.17: Optical micrograph of mc-Si sample after 16 hours in 0.05M iron (III) chloride, showing negligible etching behaviour.

Figure 7.16 shows an mc-Si sample after 16 hours etching in 0.05M potassium iodate. The twin boundaries in the top-right of the image are heavily etched, and the other surface of the sample is characterised by hemispherical impressions, some of which contain small, dark, circular features. Compared with the much larger size of the etch features that delineate the twin boundaries, it is likely that these small circles are not related to defects.

7.3.5 Iron (III) chloride

Etching mc-Si in 0.05M iron (III) chloride solutions had very little effect on the samples, as shown by the micrograph in Figure 7.17. Across the entire sample, the only noticeable features were blemishes due to imperfect polishing. A 0.5M solution was prepared and the result of an mc-Si sample exposed to this for 16 hours is shown in Figure 7.18, again with no evidence of etching.

7.4 Etch depth parameters

From the six solutions used for alternative etching, only the 0.003M iodine acted similarly to a typical defect revealing etch, and only after 16 hours exposure time. Therefore, this

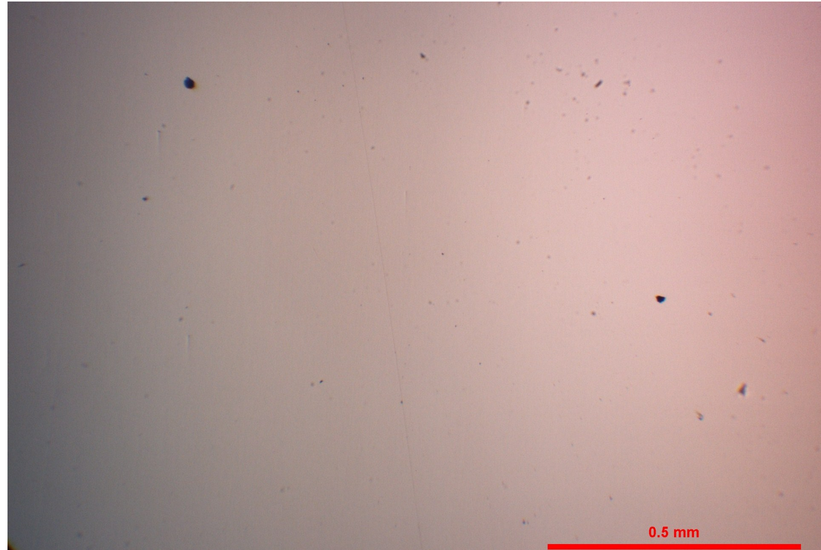


Figure 7.18: Optical micrograph of mc-Si sample after 16 hours in 0.5M iron (III) chloride, showing negligible etching behaviour.

was the only sample that was put through the angle lap technique to measure the depth to which dislocation cores are removed. However, the etch pits were too shallow to be measured, perhaps as expected when considering the images in Section 7.3.1. Estimating the detection limit of the technique to be approximately 2μm, and the pits to be around 1μm in diameter, the aspect ratio for 0.003M iodine is quite poor so going to even longer etch durations to try to achieve measurable depths would not be worthwhile.

7.5 Discussion

All of the alternative etches, bar iron (III) chloride, attacked the silicon and showed some evidence of preferential etching. This was mainly limited to strongly delineating the twin and grain boundaries, so from the point of view of this project was not a success. Regarding dislocations, only 0.003M iodine produced anything similar to the etch pits seen in the established defect etches, but after very long etch times the pits were very small and shallow, not the desired high aspect ratio tubes. Due to the lack of promise shown by the initial results in this Chapter it was decided not to further pursue this avenue of enquiry.

7.6 Summary

The aspect ratio of dislocation etch tubes produced by Secco etching was not high enough for effective dislocation core removal, and this is partly attributed to the relatively high rate at which it dissolves bulk silicon. In this Chapter a range of weaker oxidising agents were selected and tested such that an alternative etch composition with a lower bulk etch rate could be found, with the aim that this would increase the tube aspect ratio. It was found that, although defect etching was observed in some cases, none of the alternative etches produced high aspect dislocation etch tubes.

Chapter 8

Summary and further work

In addition to the conclusions drawn from the results presented in the preceding Chapters, this project has identified a series of additional investigations that would improve the understanding of silicon etching and determine whether dislocation removal could be used as a minority carrier lifetime increasing treatment. The aims of the project, and how fully they have been met, are also reviewed.

8.1 Etching

8.1.1 Secco etching

The results presented in Chapter 5 show that, with reference to the stated main aim in Section 2.2.2, dislocation cores are removed from the sample to a large depth (up to 40μm), but too much surrounding material is also removed. Therefore, the overall conclusion is that the system is unlikely to be able to produce the type of etch tube that would be required to lead to improved mc-Si for solar cells. Also, although the chemical etching treatment would be similar to the texturisation step used commercially, the etching times required to produce deep tubes are likely to be unsuitable for incorporation into the inline manufacturing process used to produce mc-Si wafers for solar cells. Texturisation typically takes 2-5 minutes [164], whereas etch times of over 30 minutes are required in this case. Further, the reagents used in Secco etch are highly toxic and the safe disposal of the vast quantities required when scaling

up such a process would present additional difficulties. However, although commercial success appears unlikely, the results have raised some questions about the mechanisms of etching that may warrant further investigation.

Any additional work should start by simply performing similar experiments at extra temperatures, both inside the -15 to 45°C range explored in this project and, assuming suitable equipment is available, outside it. This would improve the data used in the Arrhenius analysis and lead to a more thorough understanding of the behaviour when using activation energies.

The repeat etch experiment from Section 5.3.3, where the etching process was broken down into steps and the sample cleaned in between them, suggested no change from the normal etching behaviour. With more time a variety of cleaning solutions and methods could be tried before ruling out the possibility of an effect. The results of normal Secco etching show that etch rate decreases at longer etch durations, repeat etching results that differ may help understand this trend.

No evidence of precipitates was found in the etch tubes. Knowing that the presence of precipitates in commercial mc-Si is extremely likely (see Section 1.3.2), a specific investigation into the behaviour of typical mc-Si precipitates in Secco etch could be performed.

Some of the questions that could be answered include:

- Can a trend in aspect ratio be determined?
- What effect does modifying the concentration of the etch components have on etching behaviour?
- What significance does the attempt frequency (in the Arrhenius equation) have in this system?
- Does the behaviour continue at more extreme temperatures?
- Why does etch rate reduce with time, is this only linked to diffusion?
- How do typical precipitates found in mc-Si react with Secco etch?

In addition, by using the equipment and expertise from the anodic etching investigation, Secco etching could be performed whilst the electrical characteristics of the reaction are

monitored through the cell, producing polarisation curves. This result might suggest what magnitude and polarity of current could be applied to slow down the effect of the Secco etch, mitigating the problem with bulk material removal.

8.1.2 Anodic etching

Anodic etching initially appeared to be an ideal solution, with the ability to tune the relative reaction rates of bulk and dislocation etching. However, a lot of time was spent attempting to recreate previously reported results without success, and the reasons for this discrepancy are not understood. Due to the problems with preparing suitable samples, the work in this project was limited. Further work would allow a more systematic analysis of how the etch tube depth varies with time, plus other variables could be added for an even more comprehensive investigation. By modifying the cell such that the temperature of the sample and electrolyte could be controlled and monitored, it may be possible to perform an Arrhenius analysis and therefore allow comparison of activation energies with the Secco etch system. Varying the applied potential and/or current would also be used to modify the etching behaviour.

8.1.3 Alternative etching

The alternative etching work performed in this project did not produce an obvious candidate for an etching system suitable for producing high aspect ratio tubes. Even in the best system, 0.003M iodine/12M hydrofluoric acid, after 16 hours etching time only very small, shallow pits were produced. However, performing this experiment at an elevated temperature may lead to better results, and should be explored.

8.1.4 Further processing

Although this project stands alone as an investigation into etching behaviour, it also fits into a wider research effort looking at ways of improving mc-Si for solar cell applications. In that regard, the next phase would be determining the feasibility of passivating the additional surface created by dislocation core removal. Assuming suitably deep, high aspect ratio tubes are somehow produced, this would be essential in terms of creating a usable technology.

Work on novel passivation techniques and tubular geometry p-n junctions is ongoing within the Semiconductor Group and could be tied into this project neatly.

8.2 Electrical characterisation

The key parameter that defines performance in photovoltaic materials is minority carrier lifetime. This is usually measured using either quasi-steady-state photoconductance or microwave photoconductance decay spectroscopies. Using neighbouring wafers (or part-wafers) from the same ingot, samples with almost identical defect distributions can be created. This would allow a comparison between the electrical properties of a standard mc-Si sample, prepared using a typical processing route, and a sample with a large fraction of the dislocation cores removed by etching. If an improvement was noted in the etched sample, it would be necessary to confirm that the gains can be scaled up to full-size wafers and solar cells, requiring efficiency measurements to be made - this is done by performing current-voltage measurements under illumination.

A further technique that would prove useful in this investigation is electron beam induced current (EBIC), a semiconductor analysis technique performed in an SEM [165]. It is used to identify buried junctions or defects in semiconductors, or to examine minority carrier properties. EBIC depends on the creation of electron-hole pairs in the semiconductor sample by the microscopes electron beam to produce measurements, thus it is particularly useful for examining the behaviour of solar cell material where the devices operate using the same principle. An array of Schottky contacts is deposited on one surface of the sample, and an ohmic back contact is made. The internal field due to the Schottky contacts causes the electron-hole pairs to be separated by drift. If the semiconductor and Schottky contact are connected through a picoammeter, a current will flow. By using the signal from the picoammeter as the imaging signal, an EBIC image is formed on the screen of the SEM. When a semiconductor device is imaged in cross-section, the depletion region will show bright EBIC contrast. The shape of the contrast can be treated mathematically to determine the minority carrier properties of the semiconductor, such as diffusion length and surface recombination

velocity. This would produce a high-resolution map of the electrical properties of specific regions around the removed cores, which again could be compared to similar regions from neighbour wafers to quantify the effect of the treatment.

8.3 Summary

Judging this project against the main goal set out in Section 2.2.2 shows it to have been partially successful. The key aim of removing dislocations to large depths was achieved by using Secco etch, and the anodic etching technique also made good progress in this area. The results in Chapter 5 provide new understanding of the defect etching behaviour of mc-Si in the Secco etch system. The more novel etching systems investigated in Chapters 6 and 7 yielded some promising initial results, and with anodic etching in particular, further development could lead to very high aspect ratio etch tubes. However, the grander target of applying the idea of dislocation core removal to commercially produced mc-Si for solar cell applications remains very distant.

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