A High-Yielding Evaporation-Based Process for Organic Transistors Based on the Semiconductor DNTT

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Abstract

We report on the performance of organic thin film transistors manufactured in an all-evaporated vacuum roll-to-roll process. We show that dinaphtho [2,3-b:2',3'-f] thieno[3,2-b]thiophene (DNTT) is a suitable semiconductor material for deposition onto a flash evaporated polymer insulator layer to make bottom-gate top-contact transistors. Significantly, in batches of 90 transistors, the process approached a 100% yield of high mobility transistors with high on/off ratios and low gate-leakage. By contrast, a solution-deposited insulator layer led to significant gate leakage in a high proportion of transistors leading to poor yield. The performance of DNTT devices is shown to be superior to that of previously reported pentacene devices. Transistor performance is further enhanced by inclusion of a low-polarity surface modification, such as polystyrene, to the acrylate.. The devices show good environmental stability but we demonstrate also that they can be in-line encapsulated with an acrylate and a SiOx overlayer without damaging the underlying transistor. Finally, a first demonstration is made of organic vapour jet printing of the DNTT to manufacture transistors with a high semiconductor deposition rate.

Keywords: Organic thin film transistor, DNTT, polymer insulator, flash evaporation, organic vapour jet printing

1. Introduction

Organic transistors provide the basis for the development of mechanically flexible electronics with very low processing costs. Molecular semiconductors can show higher mobility than is typical of polymer semiconductors, while allowing high processing speeds and mechanical flexibility compared with typical sputter-deposited ceramic materials. Low processing costs can be realised utilising high web-speed roll-to-roll (R2R) production. We have previously reported the use of a high-speed, all-evaporated process [1,2] for the manufacture, in our roll-to-roll facility, of transistors incorporating the molecular semiconductor, pentacene, and a polymer gate dielectric layer, tripropyleneglycol diacrylate (TPGDA). Dinaphtho [2,3-b:2',3'-f] thieno[3,2-b]thiophene (DNTT) has been reported as a molecular semiconductor with good mobility and better stability than pentacene [3]. In this paper we report the application of DNTT in organic transistors utilising a vacuum-evaporated polymer dielectric layer, facilitated by developments in high yielding semiconductor purification. The transistors show good, consistent performance and exceptionally high yield. We also demonstrate the efficacy of an additional vacuum-evaporation process for device encapsulation. Finally, we report for the first time the deposition of DNTT using an Organic Vapour Jet Printing (OVJP) process to fabricate OTFTs on a moving substrate.

2. Experimental Methods

2.1 Materials

DNTT was prepared by the method of Takimiya [4] in three steps from 2-napthaldehyde and other commercially available reagents. Large bubble traps containing dilute hypochlorite solution were constructed and used to destroy volatile mercaptan by-products produced in the

first step. Early runs gave variable and poor yields of DNTT post-sublimation so the purification step was altered to eliminate the sublimation of the crude, and instead to comprise three recrystallizations from degassed 1,2-dichlorobenzene, cooling the solution from 150 °C. This was remarkably efficient, giving yields of up to 80% of bright yellow crystalline DNTT with all analytical data identical to the literature.

The TPGDA monomer, polystyrene (PS) and polyvinyl stearate (PVS) were all purchased from Sigma-Aldrich and used as-received.

2.2 Fabrication and characterisation of devices

Bottom-gate top-contact organic thin film transistors (OTFTs) were manufactured on 125μm thick polyethylene naphthalate (PEN) (or in some cases glass) substrates using a cross-linked TPGDA dielectric layer, ~450 nm or ~1 μm thick, deposited under vacuum by flash evaporation onto pre-patterned Al gate contacts and cured by plasma [2]. In some devices the TPGDA surface was modified by spin-coating onto it a 20-40 nm thick PS or PVS buffer layer from a solution in toluene (0.6 wt%), a process known to improve significantly the performance of organic devices [5,6,7,8]. In the 90-transistor arrays the thickness of the buffer layer was ~300 nm by spin-coating from a 3% wt% solution. To enable a comparative study of device yield, bottom gate OTFTs with a dielectric consisting of a single, 1μm thick layer of PS (no TPGDA) spin-coated from a 9% solution in toluene at 1000 rpm were also manufactured. In all cases the PS and PVS layers were annealed at 80°C for 10 minutes to remove residual solvent. Unless otherwise indicated, DNTT layers ~70nm thick were thermally evaporated onto the dielectric surfaces under vacuum at a rate of 1.2 nm/min, with substrates held at room temperature. Gold source/drain contacts were thermally evaporated onto the semiconductor through a shadow mask. The thickness of each layer was measured by Dektak profilometry. Semiconductor layers were also characterized by θ-2θ X-ray diffraction (Siemens D5000).

Transistor and inverter characteristics were measured in air or under controlled atmosphere using two source measure units (Keithley, Model 2400) or a Keithley model 4200 Semiconductor Characterization System following the IEEE Standard Test Methods for the Characterization of Organic Transistors and Materials [9]. In the saturation regime, the device current, I_D, is given by

$$I_D = \frac{W}{2L}\mu_{sat}C_i(V_G - V_T)^2 \quad (1)$$

where W and L are the channel width and length respectively, V_G the gate voltage and V_T the threshold voltage. The carrier mobility, μ_{sat}, was derived from the linear section of a plot of $I_D^{0.5}$ vs V_G and V_T from extrapolation to the voltage axis. The capacitance per unit area, C_i, of the dielectric layer was obtained from separate measurements on the OTFT dielectric.

3. Results and Discussion

3.1 Transistor Yield and Performance

The yield of working devices is a key parameter for any R2R production process to be used for the manufacture of organic electronic circuits. An early observation in our studies was the high yield achievable when devices were formed on TPGDA and especially on PS-buffered TPGDA. This high yield arises from the ability to deposit an extremely uniform polymer with a smooth surface (the surface roughness is much lower [10] than seen in the case of vapour deposition directly from the polymer [11]), and without the need to remove solvent from the layer. To confirm yield, we characterized 90-OTFT arrays fabricated on 5 cm x 5 cm PEN substrates. To provide a benchmark for the effectiveness of our vacuum flash-polymerized TPGDA dielectric, we also fabricated and characterized arrays of devices formed on spin-coated PS as the gate dielectric. All these devices were unencapsulated and measured in normal laboratory air.

Figure 1 shows an example of the output and transfer characteristics of a good OTFT formed on spin-coated PS as the gate dielectric. Excellent linear and saturation behaviour is seen in the output characteristics in Figure 1(a). Transfer characteristics in the linear (V_D = -2V) and saturation (V_D = -60V) regimes (Figure 1(b)) coincide over several orders of magnitude of current in the subthreshold region and no hysteresis occurred except at the lowest device currents.

The yield of such *high performance* OTFTs on the spin-coated PS, however, was low, even though 88 out of 90 devices showed transistor-like behaviour with an average μ_{sat}=0.95±0.14 $cm^2V^{-1}s^{-1}$. (Two devices failed due to a short-circuit in the gate dielectric) Of the working devices, 29 displayed very high gate leakage: in some cases $I_G > 0.1\ I_D$ in saturation. Only 52 devices combined high mobility, $\mu_{sat} \geq 0.8$ $cm^2V^{-1}s^{-1}$, with an on/off ratio $\geq 10^4$. For these devices V_T ranged from -5V to -20V. However, 16 of this sub-group showed gate leakage current, I_G > 100 pA at high V_G. Thus, of the original 90 OTFTs, only 40% gave acceptable performance.

Device parameters extracted from the characteristics of the 52 'good' transistors are listed in Table 1. The average hole mobility, μ_{sat} ~1 $cm^2V^{-1}s^{-1}$, is close to values previously reported for DNTT on other dielectrics [3,12]. In the best devices, such as that in Figure 1, the high mobility is coupled to low gate leakage currents, I_G <25 pA and low off-currents which lead to high on-off current ratios, I_{on}/I_{off}, $>10^6$. Threshold voltage, V_T ~ - 11 V and subthreshold slope, S ~ 2.0 V/decade.

By contrast, the TPGDA dielectric gave a much higher yield. Apart from a block of 9 TFTs which failed owing to a damaged track leading to the common gate electrode for this group of devices, **all** 81 remaining devices on the PS-buffered TPGDA dielectric operated satisfactorily. The output characteristics of all the TPGDA-PS devices (having a thicker PS

film) showed good linear and saturation regimes, and excellent transfer characteristics [13] similar to those for the PS-only dielectric in Figure 1.

In all these devices I_G was <100 pA,, I_{on}/I_{off} was $\geq 10^6$ except in three devices in which the values were in the 10^4 to 10^6 range, and V_T between -12 V and -17 V. The average μ_{sat} for the 81 PS-TPGDA devices was 1.51±0.17 $cm^2V^{-1}s^{-1}$. However, for devices with constant aspect ratio, W/L = 20, a systematic increase in μ_{sat} occurred with the mobility increasing from 1.34±0.04 to 1.77±0.19 $cm^2V^{-1}s^{-1}$ as the channel length, L, decreased from 200 μm to 50 μm. In a recent publication [13], this effect was seen to be larger when devices were operated in saturation, and was attributed to a parasitic source-drain current flowing outside the channel area. As device size reduced, this current became increasingly more significant. Interestingly, although the PS-only devices used the same design (W/L on each substrate ranging from 4000 μm/200 μm to 1000 μm/50 μm) no such parasitic current was observed and μ_{sat} was independent of channel dimensions.

To confirm that a parasitic current caused the geometry-dependent mobility, a small batch of 10 OTFTs were fabricated in which the width of the DNTT pattern defined the channel width rather than the source-drain electrodes. This design eliminated any possibility that a parasitic current of the type discussed above could occur. In these devices, the aspect ratio, W/L, was 5000 μm/200 μm for five devices and 2400 μm/200 μm for the second five devices, and the thickness of the PS buffer layer was reduced to ~40 nm. The nature of the characteristics for these devices was different (Figure 2) to those observed from the 90-device batches. V_T reduced to values in the range between -1V and -2 V leading to much higher I_D than devices of similar geometry biased at the same V_D and V_G. The parameters extracted from these new devices are listed in Table 1 and show that the average μ_{sat} is 0.95±0.17 $cm^2V^{-1}s^{-1}$ providing

strong evidence that a parasitic source-drain current was responsible for the elevated values of μ_{sat} presented above.

The 90-transistor batch made directly on TPGDA showed the same high yield as for the PS-buffered devices (again, 9 devices did not function owing to a poor connection to their common gate). As expected, without the PS buffer layer, device mobility was much lower with an average μ_{sat} = 0.46±0.19 $cm^2V^{-1}s^{-}1$ for the 81 operational devices. Again, the effect of a source-drain parasitic current was evident with a systematic increase occurring in μ_{sat} from 0.25±0.01 to 0.79±0.07 $cm^2V^{-1}s^{-1}$ as the device size decreased.

The high device yield when TPGDA is included in the gate dielectric, at least 90% and 100% when excluding the few devices with obvious track problems, demonstrates the strength of the solventless TPGDA process which leads to low gate leakage and consistent performance.

In addition to comparing DNTT device parameters on the different dielectric layers, Table 1 also compares these parameters with values reported previously for pentacene devices [8]. It is clear that buffering the TPGDA surface with PS significantly improved both the DNTT and pentacene devices but the former semiconductor is superior: in the DNTT device μ_{sat} is twice that in pentacene, I_{on}/I_{off} is an order of magnitude better, V_T is of smaller magnitude and the interface state density is less (S much lower).

High polarity dielectrics are known to result in mobility degradation [14] and this is likely to be the origin of the contrasting mobility values for the two insulator systems investigated here. Previous reports [5,6,7] have suggested that the inclusion of a PS buffer layer at the surface of the insulator layer before semiconductor deposition, substantially improves OTFT characteristics. We confirmed this finding for pentacene OTFTs by spin-coating a thin PS buffer layer on TPGDA [8] with preliminary results also being obtained for DNTT. The results here show that the thin PS buffer on TPGDA increases the mobility in DNTT OTFTs

to ~1 cm^2/Vs, the same as for the PS-only device and similar to values reported by others for different dielectric systems [12]. On/off current ratios are also higher in the PS and PS-TPGDA devices, partly owing to the higher mobility but mainly as a result of the lower off-current. Threshold voltage, V_T, is negative in all cases which is usually indicative of hole trapping in the gate dielectric or at the insulator/semiconductor interface. The more negative value in the thick PS layer than for the thinner buffer layer suggests that, in the former hole traps exist deep into the dielectric. The subthreshold slope, *S*, in the PS-TPGDA device is low, indicative of a low interface trap concentration. It should be noted that little hysteresis was observed in the PS and PS-TPGDA based devices.

3.2 Inverter demonstration

Based on the DNTT/PS-TPGDA transistors, unipolar inverters (inset Figure 3) consisting of a driver transistor (W = 25 mm, L=200 μm) and a saturated load transistor (*W* = 2.4 mm, *L*=200 μm) were fabricated. Figure 3 shows the voltage transfer characteristics of one such inverter for supply voltages, V_{dd}, of -20V, -30V and -50V. Even for V_{dd} = -20 V a gain of 2.2 was obtained which opens the way to further circuit functionality such as ring oscillators. Under a square wave input of period between 1 and 10 Hz with voltage from 0 V to -17 V and V_{dd} of -17 V, an output voltage swing from -15 V to -2 V was obtained. The unencapsulated inverter showed no degradation during 15 minutes of continuous operation in an enclosed chamber through which a flow of dry air (relative humidity < 10%) was maintained.

3.3 X-ray diffraction study of the DNTT and pentacene layers

We have shown previously [8] that, to achieve the highest mobility in TPGDA-based pentacene OTFTs, the polar part of the dielectric surface energy of a thin polymeric buffer layer on the TPGDA should be very low and ideally zero. From the respective X-Ray Diffraction (XRD) traces of 50 nm films of pentacene and DNTT on TPGDA and PS-

buffered TPGDA in Figure 4, we see that the presence of a non-polar buffer layer leads to clear differences in the crystalline nature of the semiconductor layers. The pentacene crystallites showed XRD traces commensurate with literature reports [15,16,17] with peaks at 2θ = 5.80°, 11.52°, 17.28° and 23.04° of gradually diminishing intensity corresponding to the (001), (002), (003) and (004) reflections respectively. The presence of (00*l*) reflections suggests excellent *c*-axis orientation of the crystallites to the substrate normal. The molecules, aligned to the crystallographic *c*-axis with *d* spacing of about 1.52 nm, are highly orientated perpendicular to the film surface. The side peaks near the (001) and (002) on the pentacene film indicates the co-existence of a minority phase in which the pentacene molecules are tilted at a slight angle to the substrate surface [15].

The DNTT is also characterized by a high degree of molecular and crystallite order perpendicular to the substrate plane, showing intense peaks at 2θ = 5.32° and 16.24° corresponding to the (001) and (003) reflections. The weak peaks at 2θ = 10.80° and 21.72° correspond to the (002), (004) reflections, with *d* spacing of about 1.65 nm. It is not clear why the intensities of the odd numbered reflection peaks are greater than those of the even numbered reflection peaks, but such a phenomenon has been reported previously by other researchers [18,19].

The high intensity of the main peaks and the lack of side peaks indicate that the DNTT is much more ordered than the pentacene, thus providing the probable explanation for the lower subthreshold slope, *S*, and hence interface state density in the DNTT devices. Of greater interest is that the signal peak intensity of both semiconductors (deposited in the same batch for each and with the same sampling area and testing parameters) is much higher on the PS-buffered surface than on TPGDA. This is a clear indication of the higher degree of crystalline order on the polystyrene-coated surface for both semiconductors, which is again reflected in the lower values observed in the subthreshold slope, *S*.

3.4 Environmental stability and encapsulation

Initially in this section we provide preliminary data to show that for DNTT OTFTs formed on buffered TPGDA, very little degradation of device parameters occurs when the transistors are stored in air over many months. Some degradation does occur, however, and is likely to be accelerated under operational conditions if devices remain unencapsulated. Consequently, we have developed a R2R compatible encapsulation method that could form the final stage in organic circuit production. In this section, therefore, we describe this process and provide evidence for the effectiveness of the method.

For the initial study of environmental stability, DNTT OTFTs were manufactured on 1μm thick TPGDA buffered with a spin-coated layer of poly(vinyl stearate), PVS. For these devices a glass substrate was used. Since PVS is similar to PS in providing a low polarity surface [8], similar results to those obtained from the PS-TPGDA devices were expected. The output and transfer characteristics of one of these devices shown in Figure 5, and the device parameters listed in Table 2 confirm this. The mobility was 1.2 $cm^2V^{-1}s^{-1}$, $I_{on}/I_{off} = 10^6$ and V_T = -2V. Figure 5 also shows the characteristics of the same device after eight months in the dark but exposed to ambient air in an unsealed container to keep out dust. As can be seen from Table 2, very little degradation of device parameters occurred. Carrier mobility decreased slightly to 1.1 $cm^2V^{-1}s^{-1}$, I_{on}/I_{off} remained stable at 10^6, and V_T decreased slightly to 0V. The only obvious degradation is in *S*, which almost doubled from 1.7 V/decade for a fresh device to 3.3 V/decade for the same device after long air exposure. The observed degradation is much less than for most acene transistors [19] and is similar to a DNTT OTFT with an Al_2O_3 dielectric and SAM buffer layer, reported by Zschieschang et al. [12]. Their transistors showed a mobility decreasing to 70% of its initial value, i.e. dropping from 2.1 $cm^2V^{-1}s^{-1}$ to 1.5 $cm^2V^{-1}s^{-1}$ after eight months of continuous exposure to air.

As some deterioration of properties is observed over time, even for DNTT devices on buffered TPGDA, we have explored a possible in-line encapsulation method compatible with a large-area, vacuum roll-to-roll process. Of concern was the possible damage, in particular to the underlying semiconductor, resulting from an in-line encapsulation process. Thus a device was encapsulated and re-tested to characterise any loss in performance arising from the encapsulation process itself. We report here the use of a TPGDA (600nm)/SiO_2 (80nm) double layer as a transparent encapsulation layer deposited directly onto the devices in our roll-to-roll facility. The TPGDA was flash-evaporated and e-beam cured at very low dose (40 mA nominal current and 2.0 kV e-beam voltage). This minimised any possible damage to the underlying device and provided a smoother surface for a barrier layer, in this case the SiO_2. The polymer deposition process, and a comparison between e-beam and plasma curing can be found in previous publications [1,2]. In this case e-beam curing was chosen because of the lower exposure dose experienced by the organic semiconductor using this method in our system. The dose was high enough to cure the monomer sufficiently for supporting a barrier layer, but would not have been enough to create a high quality dielectric layer for the OTFT. Following the TPGDA deposition, a top layer of SiO_2 was evaporated over the TPGDA to achieve a high barrier to water vapour. This manufacturing method for a gas barrier layer is already used commercially in roll-to-roll processing.

DNTT OTFTs were fabricated with a TPGDA-only dielectric on PEN at high thermal evaporation rates (10 nm/min). It was anticipated that such devices would more easily degrade owing to (a) the lack of a buffer layer on the TPGDA and (b) the poorer crystalline structure of the DNTT resulting from the high deposition rate. The transfer characteristics of the resulting OTFT measured in ambient air is shown in Figure 6(a) and the relevant device parameters given in Table 2. As anticipated, increasing the deposition rate clearly had adverse effects on device performance, c.f. values in Table 1. The hole mobility, μ_{sat}, is

much lower and the subthreshold slope, *S*, is much greater than in devices where the DNTT is evaporated at much lower rates. After storing in ambient air for three weeks, significant deterioration occurred in the transfer characteristics (Figure 6(b)) of these high deposition rate transistors making them good candidates for testing the effectiveness of a R2R encapsulation process. V_T shifted from -12 V to +7 V and *S* increased from 6.7 to 9.1 V/decade but the mobility increased from 0.05 to 0.10 $cm^2V^{-1}s^{-1}$ (Table 2), while I_{off} increased by an order of magnitude. However, these changes were largely reversible by placing the devices under vacuum. Not surprisingly, therefore, recovery was observed as a result of placing the sample under vacuum during the encapsulation process.

The recovery in performance on encapsulation indicates that the observed changes are related to the effect of reversible absorption of atmospheric components e.g. water and/or oxygen in the devices rather than to permanent degradation. Previously we reported [2] similar reversible behaviour when pentacene OTFTs were alternated between vacuum and ambient air measurements. The high I_{off} observed in the sample exposed to air probably arose from an increase in gate leakage current owing to the absorption of atmospheric moisture into the TPGDA leading to the enhancement of ionic currents. Oxygen doping of the DNTT in air, may also lead to an increase in carrier mobility in the channel as well as to an increase in parasitic source-drain currents. The positive shift in V_T likely arises from the creation of negatively charged interface trap states neutralizing an existing positive interface charge.

With the encapsulation applied, the recovery in device performance was sustained for at least two weeks of air exposure (Figure 6(c) and Table 2). I_{off} was two orders of magnitude lower resulting in an I_{on}/I_{off} ratio $>10^4$ and V_T returned back to -7V. Importantly *S* substantially improved from 9.1 V/decade in the device exposed to air, to only 3.8 V/decade after encapsulation. We have shown, therefore, that the encapsulation method employed here

could be transferred directly to a roll-to-roll process and used without damaging the underlying OTFT.

3.5 Organic Vapour Jet Printing

To realize roll-to-roll processing of flexible circuitry, the organic semiconductor needs to be deposited only in selected areas on the substrate, and for large area processing a high rate of deposition is required. A shadow mask approach, even if it could be implemented in a R2R process, would lead to substantial material wastage. A possible solution to these issues is organic vapour jet printing (OVJP), a solvent-free printing method, developed by Shtein *et al.* [21]. It is a scalable printing technique suited to small organic molecules that combines the advantages of inkjet printing and thermal evaporation, and can operate under vacuum. OVJP utilizes an inert carrier gas (argon in our case) to transport the vaporized organic molecules from a source cell to the substrate on which the organic vapour condenses to form a thin film. OVJP is a mask-free process in which the organic vapour is ejected through a nozzle so that a pattern can be printed directly. A line-width of less than 20 μm has been demonstrated using high-precision MEMS-based nozzles [22]. More recently, a digital-mode OVJP was introduced, by incorporating a pulsed-mode operation mechanism into the OVJP method [23]. This is analogous to drop-on-demand ink-jet printing, in which the drops of fluid are printed only as required at a given position in a digital manner. Pentacene OTFTs made with OVJP have already been reported with an average carrier mobility of 0.2 $cm^2V^{-1}s^{-1}$ [24] and Yun et al. [25] were able to achieve an average carrier mobility of 0.47 $cm^2 V^{-1}s^{-1}$ by combining chemical treatment of the gate dielectric layer with control of carrier gas temperature. Morphological analyses indicated that a combination of relatively high carrier gas temperature combined with low dielectric surface energy was the key to achieving a level of performance comparable to that of devices based on conventional technologies.

Previous reports on OVJP OTFTs utilised pentacene as the semiconductor and oxide thin films as dielectric layers, mostly on a Si substrate. Here, we report for the first time, the successful fabrication of bottom-gate top-contact OTFTs in a vacuum roll-to-roll environment using the OVJP process to deposit a localised area of DNTT onto a 450 μm thick PS-TPGDA dielectric layer on a moving substrate.

The in-line OVJP system used in this work was built in-house inside the chamber of an Edwards 306 thermal evaporator system. A source cell, loaded with the organic semiconductor, and an Ar gas line were independently heated. During deposition, the nozzle and semiconductor source cell were heated to 270°C and the gas pipe to 300°C. By flowing the argon carrier gas through the DNTT source cell at a rate of 10 sccm, 5 mm wide stripes of DNTT were deposited through a nozzle held a few mm from the PS-TPGDA dielectric substrates attached to a rotating drum to simulate a web moving at 0.02 m/min in a roll-to-roll process. The working pressure in the chamber was $3x10^{-4}$ mbar and >60 nm of DNTT was deposited in a single pass corresponding to a stationary deposition rate of 240 nm/min. This represents a significantly faster deposition rate than used for transistor production in section 3.1 (1.2 nm/min) and in section 3.4 (10 nm/min).

The output and transfer characteristics of a device produced using OVJP is presented in Figure 7. Device parameters extracted from the transfer plots (Table 1) are very encouraging: μ_{sat} = 0.5 $cm^2V^{-1}s^{-1}$, V_T = -4 V, I_{on}/I_{off} = 1 $x10^5$ and S = 0.7 are equal or superior to those for OTFTs prepared by slow thermal evaporation onto un-buffered TPGDA. We observed a deterioration in properties in the unbuffered-TPGDA samples on increasing the deposition rate from 1.2nm/min to 10nm/min (table 1&2). The extent of deterioration of properties observed between the OVJP samples over the slowly deposited DNTT on PS-buffered TPGDA, is comparable or smaller, despite the increase in deposition rate being an order of magnitude greater. Unfortunately, the area of the deposited DNTT was too small to

allow the use of XRD to confirm the degree of crystallinity in the layer. Nevertheless, this first demonstration of OVJP of DNTT devices shows promise as a roll-to-roll manufacturing method for transistor circuitry. With further optimisation of, for example, the gas flow rate, temperature, nozzle size and position, even higher deposition rates, smaller features, and higher mobilities are possible.

4. Conclusion

A flash evaporated polymer (TPGDA), which can be deposited at high rates in a roll-to-roll process, has been shown to be a highly effective gate dielectric layer in OTFTs. We have carried out a study of the yield of transistors in manufacture based on arrays of 90 transistors. Amongst the 81 transistors that did not show a failure in the metallized contact line, 100% yield was achieved with the flash-evaporated TPGDA layer, both with and without a PS buffer layer, and with a consistent device performance. We have shown the superiority of this polymer dielectric over a solution-deposited dielectric layer (PS), for which, due to gate leakage and poor on-off ratios in a significant number of transistors, showed a 40% yield of acceptable devices.

Unencapsulated devices manufactured with DNTT showed superior performance to those previously reported with pentacene, reaching typical mobilities of ~1 $cm^2\ V^{-1}s^{-1}$, when a thin (40 nm) PS dielectric surface modification layer is included, a low threshold voltage of -1V, high I_{on}/I_{off} of 10^7, and low subthreshold swing of ~0.5 V/decade. Such devices enabled us to demonstrate a unipolar, enhancement load inverter with a gain of 2.2.

DNTT shows greater device stability than has been reported previously with pentacene, only showing modest increases in *S* and the turn-on voltage after storage in air for eight months.

To further stabilise the devices over long term use in damp environments encapsulation would be desirable, and we have demonstrated that the OTFTs may be directly encapsulated

as part of an in-line roll-to-roll process by application of a TPGDA layer over the device followed by a suitable barrier layer, such as evaporated SiOx.

Finally, in the first step towards a patterned semiconductor layer within a high speed roll-to-roll process, we have demonstrated organic vapour jet printing of DNTT to produce devices of comparable performance to those produced by static thermal evaporation under high deposition rate conditions.

Taken together, these results form a strong demonstration of the applicability of flash-evaporated polymer dielectric/DNTT transistors for the manufacture of circuits by a high-speed roll-to-roll process.

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FIGURE CAPTIONS

Figure 1 (a) Output and (b) transfer characteristics of a good DNTT transistor (W = 2 mm, L = 85 μm) employing a 1 μm thick spin-coated PS layer as the gate insulator. The transfer characteristics were measured in the linear (V_D = -2V) and saturation (V_D = -60V) regimes.

Figure 2 (a) Output and (b) transfer characteristics, (at V_D = -30V), of a DNTT transistor (W = 2.4 mm, L = 200 μm) formed on 400 nm thick TPGDA buffered with a 40 nm thick spin-coated polystyrene layer.

Figure 3 Voltage transfer curves for a unipolar, saturated load inverter (see inset diagram) for different supply voltages.

Figure 4 XRD traces of evaporated films of pentacene and DNTT on polystyrene and TPGDA surfaces.

Figure 5 (a) Output and (b) transfer characteristics, measured at V_D = -30V, of a DNTT transistor (W = 1 mm, L = 200 μm) formed on PVS-buffered TPGDA on a glass substrate and measured in air shortly after device fabrication and after eight months of exposure to ambient air. As the device width was narrow compared to the semiconductor area, parasitic currents may be contributing to the output characteristics.

Figure 6 Transfer characteristics of a DNTT transistor (W =1 mm, L = 200 μm) fabricated on TPGDA on flexible PEN substrate. The DNTT was evaporated at 10 nm/min. The device was measured in air with for V_D =-30V (a) shortly after device fabrication, (b) after three weeks of exposure to ambient air and (c) two weeks after encapsulation with TPGDA and SiO_2 layers.

Figure 7 (a) Output and (b) transfer characteristics (at V_D=-30V) of an organic vapour jet printed (OVJP) DNTT transistor (W = 1 mm, L = 100 μm) fabricated on PS-TPGDA on a flexible PEN substrate in R2R mode. The DNTT deposition rate was 240 nm/min.

Table captions

Table 1 Comparison of the electrical parameters of OTFTs based on thermally evaporated (TE) and organic vapour jet printed (OVJP) DNTT devices. The TPGDA devices were fabricated on glass substrates with a 1 μm thick dielectric layer. All other devices were formed on PEN. Average mobility values and the standard deviation are based on 88 devices (PS), 81 devices (TPGDA), 81 devices (300 nm PS-buffered TPGDA) and 10 devices (40 nm PS-buffered TPGDA. Although a batch of 20 OVJP devices had mobilities in excess of 0.25 $cm^2V^{-1}s^{-1}$, the parameter values listed were obtained from the best characteristics obtained to date from this unoptimized process.

Dielectric	Deposition Method: nm/min	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_T (V)	I_{on}/I_{off}	S (V/decade)
	DNTT				
Spin-coated PS	TE: 1.2	0.97±0.17	-5 to -18	10^4 to $>10^6$	2.0
TPGDA†	TE: 1.2	0.46±0.19	-14 to -20	10^4 to 10^6	1.8
PS-TPGDA[1, †]	TE: 1.2	1.51±0.17	-11 to -17	$>10^6$	1.0
PS-TPGDA[2]	TE: 1.2	0.95±0.17	-1	10^7	0.5
PS-TPGDA[2]	OVJP: 240	0.5	-4	10^5	0.7
	Pentacene				
TPGDA[3]	TE: 1.2	0.10	-8	10^3	8.0
PS-TPGDA[3]	TE: 1.2	0.65	-16	10^6	2.0

[1] PS thickness 300 nm; [2] PS thickness = 40 nm; [3] Values taken from reference [8] †These devices were subject to parasitic currents, giving rise to apparently greater mobilities.

Table 2 Stability of electrical parameters of DNTT OTFTs deposited at low rates onto PVS-buffered TPGDA and at high rates onto TPGDA .

	TE rate (nm/min)	μ_{sat} (cm^2/Vs)	V_T (V)	I_{on}/I_{off}	S (V/decade)
PVS-TPGDA					
As-deposited	1.2	1.2	-2	10^6	1.7
8 months in air	1.2	1.1	0	10^6	3.3
TPGDA					
As-deposited	10	0.05	-12	10^3	6.7
3 weeks in air	10	0.10	7	10^3	9.1
2 weeks after encapsulation	10	0.05	-7	10^4	3.8

Fig 1

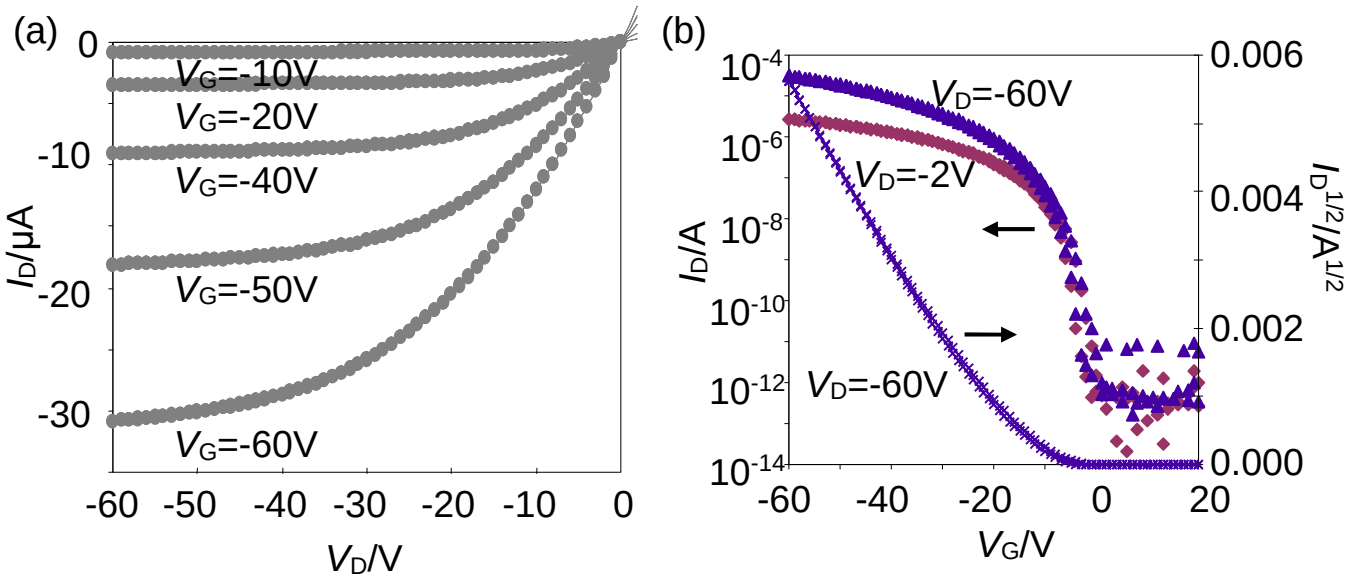

(a)
0
-10
-20
-30
I_D/μA
V_G=-10V
V_G=-20V
V_G=-40V
V_G=-50V
V_G=-60V
-60 -50 -40 -30 -20 -10 0
V_D/V
(b)
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
10^{-14}
I_D/A
V_D=-60V
V_D=-2V
V_D=-60V
0.006
0.004
0.002
0.000
$I_D^{1/2}$/$A^{1/2}$
-60 -40 -20 0 20
V_G/V

Fig 2

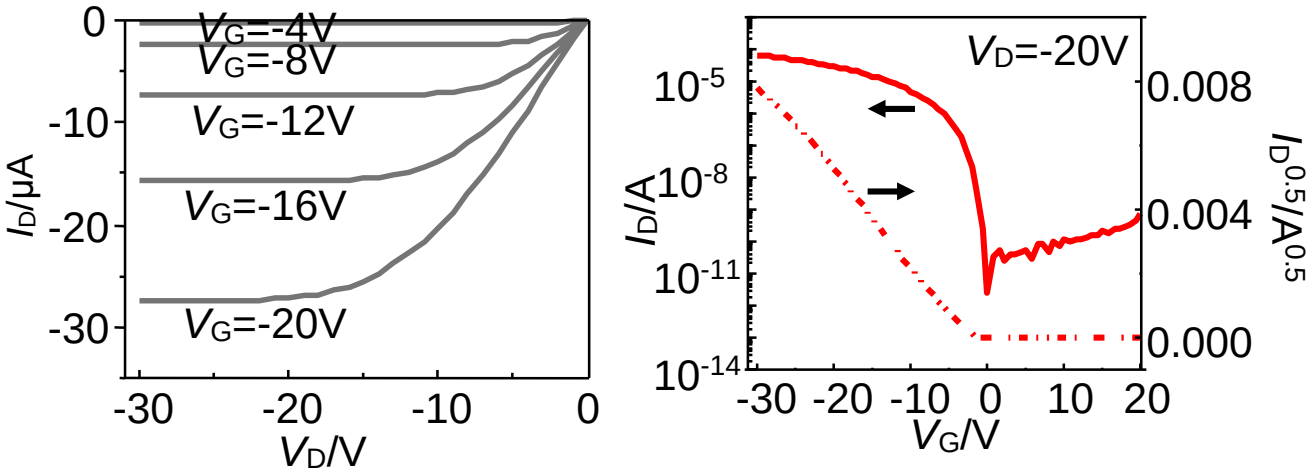

0
-10
-20
-30
I_D/μA
V_G=-4V
V_G=-8V
V_G=-12V
V_G=-16V
V_G=-20V
-30 -20 -10 0
V_D/V
10^{-5}
10^{-8}
10^{-11}
10^{-14}
I_D/A
V_D=-20V
0.008
0.004
0.000
$I_D^{0.5}$/$A^{0.5}$
-30 -20 -10 0 10 20
V_G/V

Fig 3

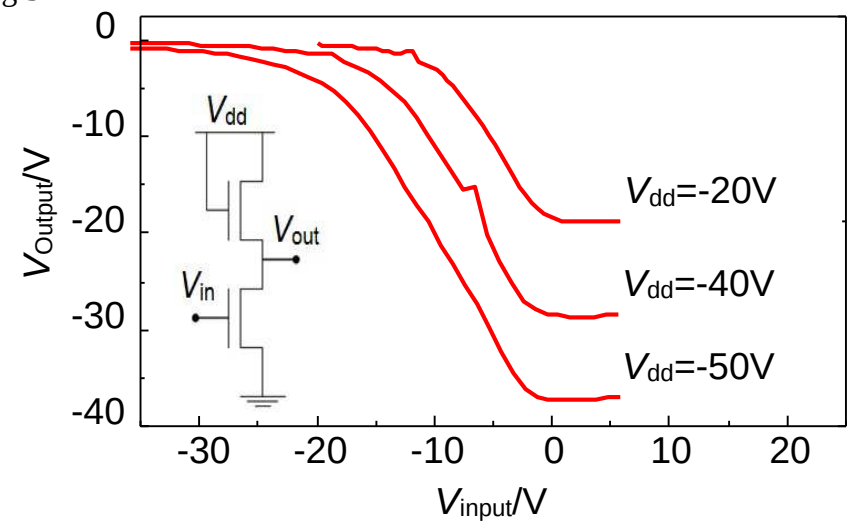

0
-10
-20
-30
-40
V_{Output}/V
-30
-20
-10
0
10
20
V_{input}/V
V_{dd}
V_{out}
V_{in}
V_{dd}=-20V
V_{dd}=-40V
V_{dd}=-50V

Fig 4

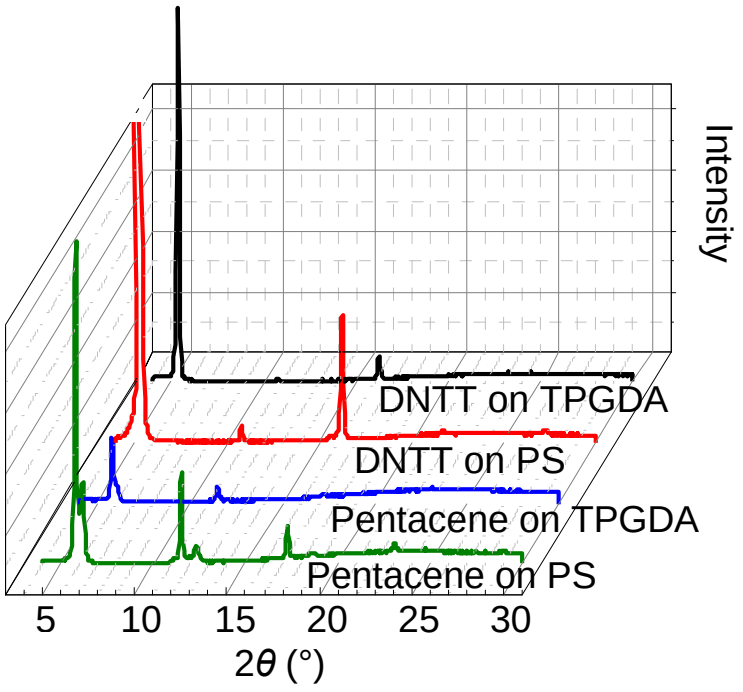

Intensity
DNTT on TPGDA
DNTT on PS
Pentacene on TPGDA
Pentacene on PS
5
10
15
20
25
30
2θ (°)

Fig 5

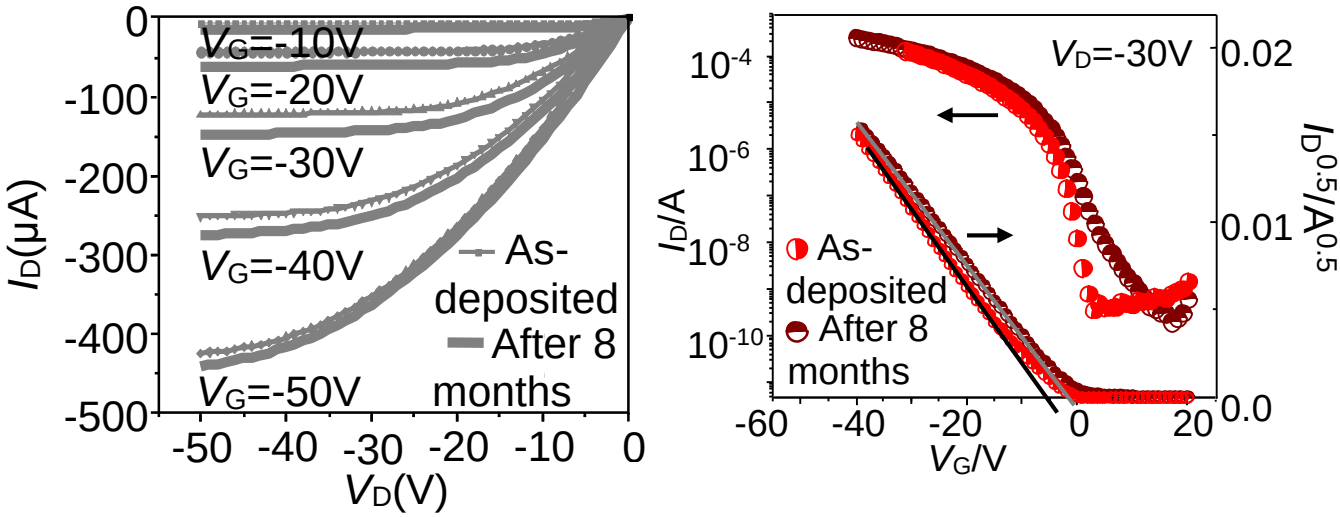

I_D(μA)
V_G=-10V
V_G=-20V
V_G=-30V
V_G=-40V
V_G=-50V
As-deposited
After 8 months
V_D(V)
I_D/A
V_D=-30V
As-deposited
After 8 months
V_G/V
$I_D^{0.5}$/A$^{0.5}$

Fig 6

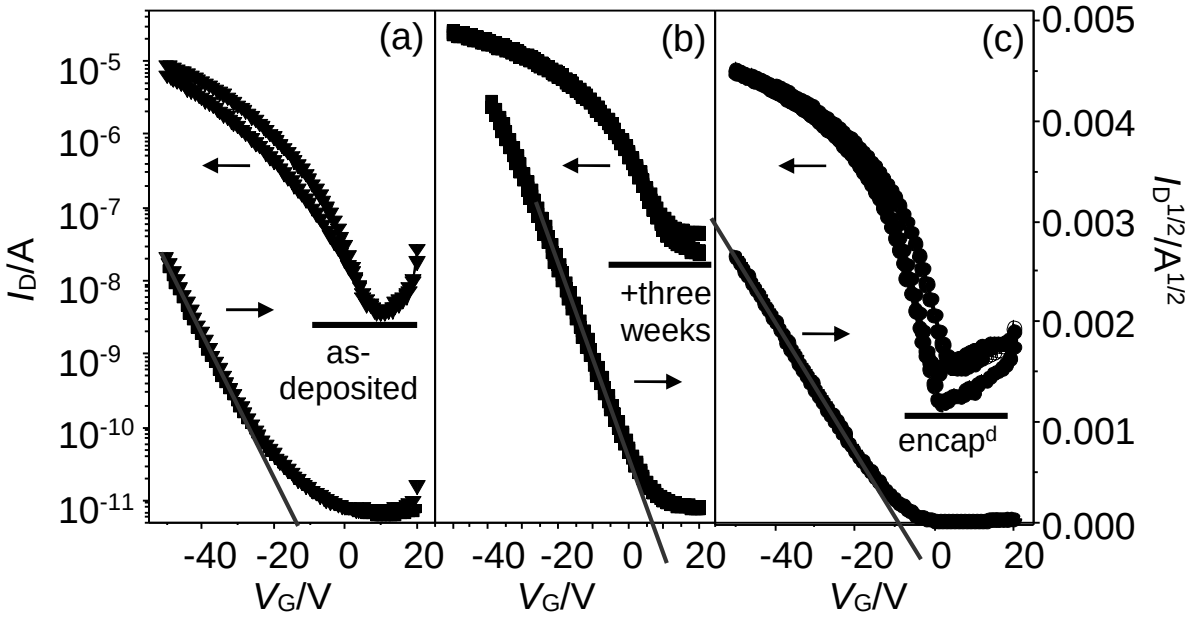
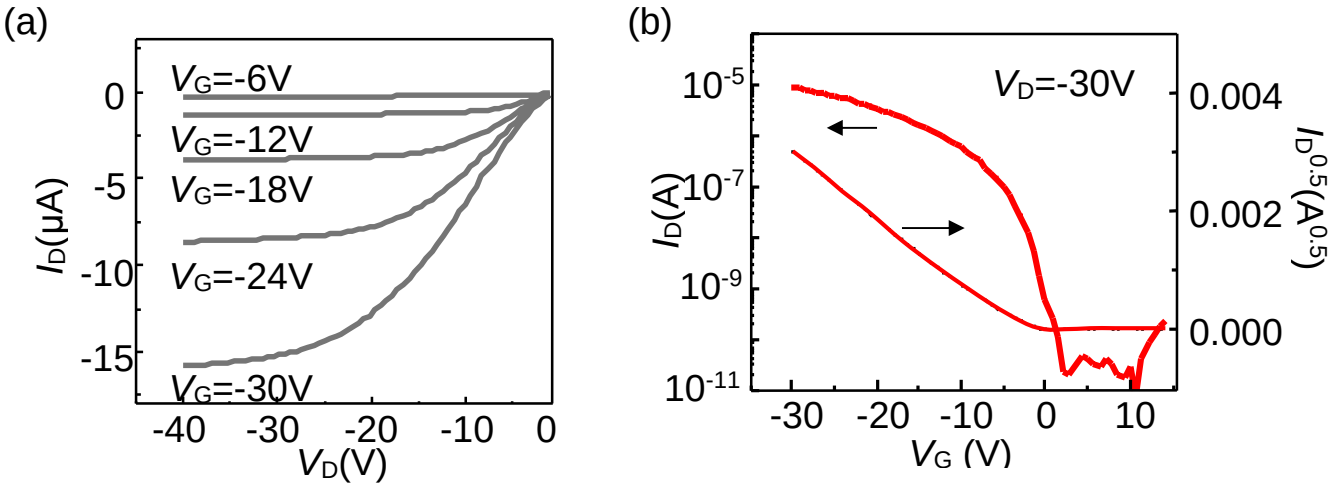

(a)
(b)
(c)
I_D/A
as-deposited
+three weeks
encap^d
V_G/V
$I_D^{1/2}$/A$^{1/2}$

Fig 7


(a)
V_G=-6V
V_G=-12V
V_G=-18V
V_G=-24V
V_G=-30V
I_D(μA)
0
-5
-10
-15
-40
-30
-20
-10
0
V_D(V)
(b)
V_D=-30V
I_D(A)
10^{-5}
10^{-7}
10^{-9}
10^{-11}
$I_D^{0.5}$($A^{0.5}$)
0.004
0.002
0.000
-30
-20
-10
0
10
V_G (V)