

An 8-Pixel Compact Focal Plane Array with Integrated LO Distribution Network

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Abstract— We present the design of an 8-pixel Superconductor-Insulator-Superconductor (SIS) array centred at 650 GHz, which comprises two nearly identical 1×4 planar array chips, stacked together to form a 2×4 focal plane array. The array is fed by a single local oscillator (LO) source, and the array size is extendable by either increasing the number of mixing elements in the array chip or the number of stacking. The LO and RF signals for each mixer in the array are combined on-chip via a microstrip-coplanar waveguide (CPW) crossover which allows control of the RF/LO coupling level for each mixing element. The use of this planar beam splitter enables us to simplify greatly the design of the array mixer chip, as well as the design of the mixer block, which is important for future large pixel arrays. In this paper, we describe the design of the various components of the array chip, and the design of the mixer array block including the simplified LO distribution network.

INTRODUCTION

The time available for observing at short sub-millimetre wavelengths in the heterodyning mode, above 600 GHz, is limited even at high dry sites such as the Atacama or South Pole. It is therefore vital to fully maximise the scientific returns within the available observing time by constructing a large focal plane array. However, the key technologies required to build heterodyne receivers with large number of pixels at high frequencies is still very challenging [1], which requires innovative ideas such as compact LO injection scheme [2], modular array design that is easily extendable [3], and highly integrated IF amplifiers [4]. In this paper, we aim to address these challenges by using advanced superconducting planar circuit technology, to build an 8-pixel demonstrator at 650 GHz that could be extended to form a large format focal plane array. These ideas were chosen such that we can target on developing the novel solutions that would have large impact in realising compact and scalable receiver architectures, which will enable the construction of kilo-pixel heterodyne array at THz frequencies.

PLANAR COMPACT ARRAY CHIP

A major challenge for constructing a compact arrays is that there are only two interfaces for each mixer element which requires three input/output ports i.e., the RF, LO and IF ports. Traditional arrays solve this by using either multiple split

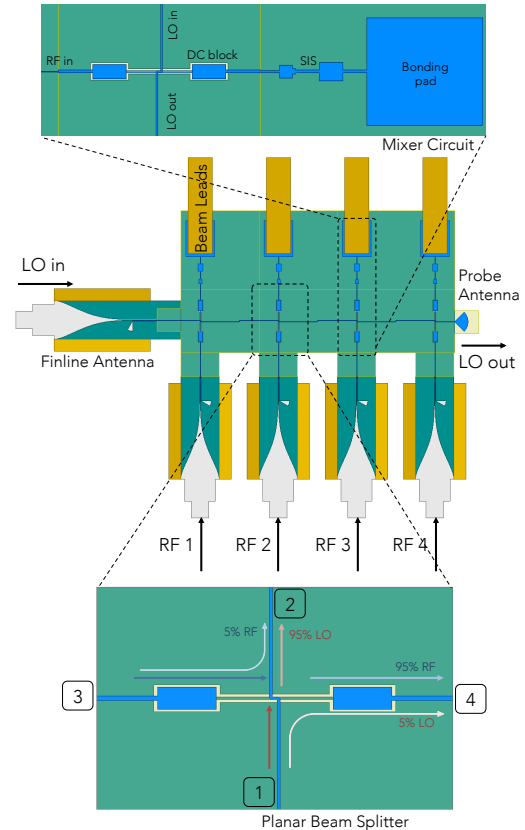


Fig. 1 Planar on-chip 4-pixel array with integrated planar beam splitters and mixer circuits deposited on a 15 μm thick silicon-on-insulator (SoI) substrate. The planar circuits are formed with 400 nm top and bottom Niobium layer sandwiching a 475 μm thick silicon monoxide dielectric. The bottom panel shows the transmission properties of the planar beam splitters, which divides power in a similar way as the traditional dielectric beam splitter.

blocks with a large waveguide coupler network [5], series of free-space beam splitter [6] or LO beam multiplexing [7], to inject the RF and LO signal to the mixer's input port. These solutions are often bulky and complicated. More importantly, the required LO power to feed all pixel may not be available by a single LO source. This is particularly vital for high-frequency applications where the LO power is limited. In our design, we replace these methods with a simple planar beam splitter that can be fabricated on-chip, directly integrated with

the mixer detector circuit, and therefore eliminate the need for large array block or bulky optical arrangement.

Fig. 1 shows the design layout of a 1×4 array chip. The LO power is coupled from the finline antenna on the left and delivered to each mixer through a planar beam splitter, and exit the array chip via a probe antenna. Each mixing pixel comprises an input finline antenna, a planar beam splitter, and the mixer itself. The finline antenna and the mixer circuit design are similar to our conventional SIS mixer which operate at wide RF/IF bandwidths [8]. The planar beam splitter, on the other hand, is the key component that enables us to integrate multiple individual mixer elements onto a single substrate.

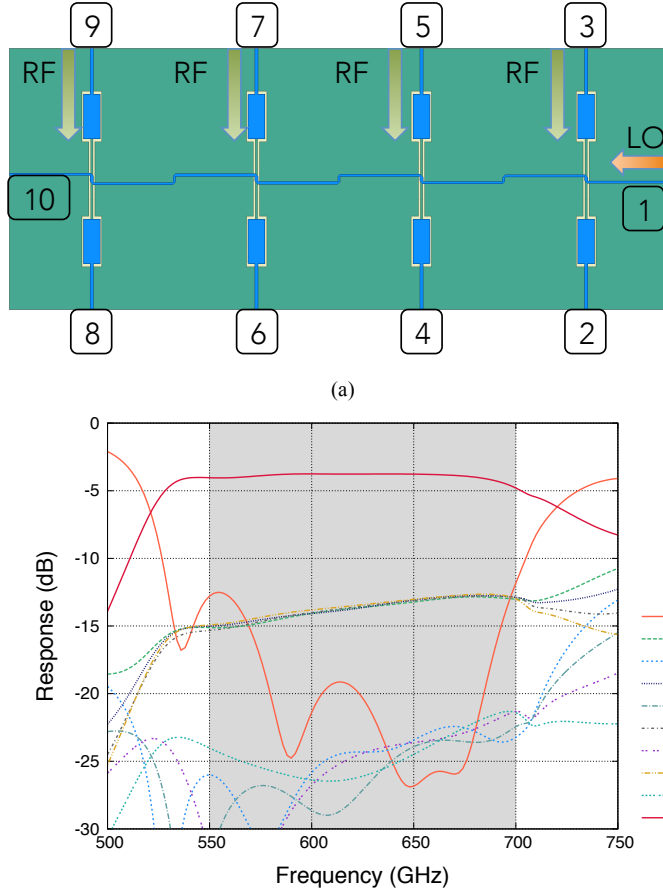


Fig. 2 (a) Zoom-in view of four planar beam splitters cascaded in series, and the port annotations. (b) The response of each output port in relation to the LO port (refer the port notation to panel above). Note that the LO power coupled to all the mixer ports ($S_{2,1}$, $S_{4,1}$, $S_{6,1}$ and $S_{8,1}$) are identical from 550–700 GHz.

The bottom panel of Fig. 1 shows the construction of the planar beam splitter, which is in fact similar to a coplanar waveguide (CPW) crossover reported in [9], except that in this case, instead of minimising the power coupling between the two crossing transmission lines, we aim to couple a small amount of power between them in a controllable fashion. This is achieved by bending a small section of the orthogonally oriented microstrip to align it with the CPW at the bottom layer (hereinafter Z-bend section). The detailed electromagnetic design of the planar beam splitter can be

found in [10], so we concentrate here on how it can be used to form a complete on-chip array.

One important feature of the planar beam splitter is that the coupling coefficient between the RF and LO paths can be controlled simply by altering the length of the microstrip Z-bend section. This is especially useful for constructing the LO power distribution network that needs to split the input power evenly between mixer branches of the array. In particular, the drop of LO power after each planar beam splitter can now be compensated for, by gradually increasing the Z-bend length, hence ensuring the power delivered to all mixers remains constant. As shown in Fig. 2, the performance of the planar beam splitter is broadband, with leakage well below -20 dB from 500–700 GHz, and the return loss is as low as -15 dB from 580–700 GHz. The coupling coefficient stays constant at -13 dB within the same range for all the mixers. The power coupling also gradually increases with frequency to compensate for the gradual loss of LO power at the higher frequency end.

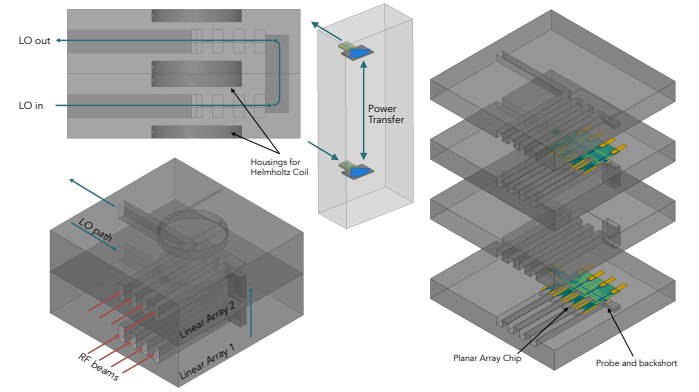


Fig. 3 Illustration of the array block design. Each 1×4 array can be stacked and the LO distribution network could be connected via a pair of radial probe antennas at the end of each array chip.

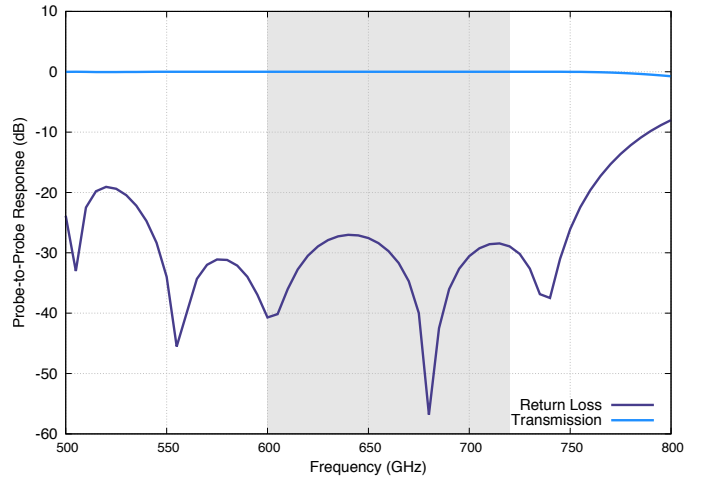


Fig. 4 The return loss and transmission characteristics of the probe-to-probe coupler, showing a broadband response.

Note that the remaining LO power after passing through the four SIS pixels arrays is still strong at $S_{10,1} = -4$ dB, and more importantly, remains flat across the operating frequency range. Hence, by cascading more mixers of the array chip in series,

the remaining LO power that pass through the planar beam splitter with small loss can be recycled for coupling to more mixer elements. This allows us to harness all of the available LO power and enable the use of a single LO source to feed multiple SIS pixels in a large focal plane array.

2×4 FOCAL PLANE ARRAY

The simple nature of the planar array chip design enables us to fabricate the array using the conventional split block technology, with the chip positioned at the E-plane of the input/output rectangular waveguides as shown in Fig 3. Two of these array blocks could be stacked together to form a 2×4 array. The array chip can also be populated with more pixels by simply duplicating more individual units of planar beam splitters and mixer circuits in series, and many more of these arrays can be stacked on top of each other to form an ever larger focal planar array. The spacing between each mixer unit could easily be adjusted to suite the Nyquist sampling of the required beams for a particular telescope. In the example shown in Fig. 3, the entire 1×4 array chip is only a few mm long, and compared to the traditional mixer array, this translates to almost an order of magnitude smaller array block. In order to feed the two arrays with a single LO source, the LO power could be coupled between each array via the radial probes at the end of the array chips. This is shown in Fig. 3 where two probes, one from each array chip, form a back-to-back coupling antenna with the aid of a pair of rectangular waveguide backshorts. The remaining LO power from the bottom array chip is coupled through the probe and the rectangular waveguide, to the probe of the top array chip. As shown in Fig. 4, this design is broadband with well below -25 dB return loss from near 500–750 GHz. Finally, a pair of Helmholtz superconducting coils can be inserted between the array to suppress the unwanted Josephson effects for the entire array of SIS junctions.

CONCLUSIONS

We have presented the design of an array chip comprising four SIS mixers fabricated on an SoI substrate. The LO distribution network for the array was integrated on-chip with the input antennas and the mixer circuits, through a series of cascaded planar beam splitters. We have shown that by gradually increasing the length of the microstrip Z-bend section of the planar beam splitter, we could compensate for the LO power loss after each mixer unit and ensure that the LO power coupled to each individual mixer is equal. Two of these array chips along with their housing blocks can be

stacked together to form a 2×4 compact array. In order to fully utilise the LO power, we coupled the remaining LO power after the first array chip to the second chip via a set of back-to-back probe antennas. The preliminary prediction from the electromagnetic simulation shows promising performance with broad bandwidth. Due to the simple design of the array chip and the block, the compact array size can be extended easily either by adding more mixer units along the array chip or increasing the number of stacked array blocks. This enables the construction of hundred or kilo-pixel array in the near future, in particular near the THz frequency region.

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