Large Area Vacuum Fabrication of Organic Thin-Film Transistors

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Abstract

A process has been developed to make the dielectric layer for organic thin-film transistors (OTFTs) in a roll-to-roll vacuum web coater environment. This dielectric layer combined with an organic semiconductor layer and metal layer deposited in vacuum allows a solvent-free process to make organic/inorganic multilayer structures for thin-film electronic devices on a flexible substrate at, potentially, high speed.

The polymeric gate dielectric layers were fabricated by flash evaporation of acrylic monomers onto a polymer film with pre-patterned metal gates followed by radiation curing by electron beam, ultra-violent light (UV) or plasma. With a non-polar dielectric surface, charge carrier mobility (μ) of 1 $cm^2 \cdot V^{-1}s^{-1}$; on/off current ratio of 10^8, sub-threshold swing (*SS*) of 0.3 V/decade and saturated output curve were routinely achieved in dinaphtho-[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) transistors with dielectric layer of tripropylene glycol diacrylate (TPGDA) of ~400 nm.

Apart from the TPGDA, monomer formulas including 1,6-Hexanediol diacrylate (HDDA) as well as several commercial acrylic resins have been used to make the dielectric layer. The highest areal capacitance of $41nF \cdot cm^{-2}$ was achieved with a pin-hole free film of less than 100 nm made of an acrylate mixture resin.

A non-polar dielectric surface treatment layer has been developed based on flash evaporation of lauryl acrylate and HDDA mixture. The transistors with the buffer layer showed constant performance and a mobility fivefold greater than those of untreated samples.

The effect of humidity, oxygen, and light during switching cycles of both pentacene and DNTT transistors were studied. Water and oxygen/illumination had a distinct effect on both pentacene

and DNTT transistors. Oxygen leads to acceptor-like charge traps under illumination, which shifted the turn-on voltage (V_{to}) to more positive values. In contrast, water in transistors gave rise to donor-like charge traps, which shifted the V_{to} and the threshold voltage (V_T) more negatively. The DNTT devices showed good stability in dry air without encapsulation, while pentacene transistors degraded with either repeating measurement or long term storage. A DNTT transistor with a PS-coated TPGDA dielectric layer showed stable drain current (I_d) of ~10^5A under bias stress of the gate voltage (V_g) of -20V and the drain voltage (V_d) of -20V for at least 144 hours. The V_{to} shift after the stress was less than 5 V and was recoverable when the device was kept in dry air for a few days. Possible reasons for the V_{to} shift have been discussed.

A page for my papa and mama

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Declaration of Originality

This thesis is an account of work carried out by the author in the Department of Materials, University of Oxford under the supervision of Dr Hazel Assender and Dr Gamal Abbas. Any other work that has been addressed in the thesis is acknowledged in the text, and lists of references are presented at the end of each chapter. No part of this thesis has been submitted towards the completion of another degree at the University of Oxford or elsewhere. Parts of this thesis have been submitted to or published in the following scientific journals or conference presentations:

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Chapter 1

Introduction

Silicon-based electronics have been the workhorse for the information revolution for almost half a century. These rigid chips have provided us with not only stunning calculating power but also the brains and nerves that are integrated with wide arrange of tools and instruments. These smart gadgets, together with PCs and the internet, form a network that we interact with day-in, day-out. There are, however, limitations to these silicon-based devices: they are relatively expensive to make, thus not feasible to be applied to mass production based products, e.g. smart packaging or labels, and, the core of silicon based electronics, integrated chips, are rigid and extremely fragile. This restricts product designs; and makes the chips unsuitable for wearable and body contact products e.g. body-contact sensing. Moreover, waste disposal of electronics components has been attracted great attention in the recent years[1-2]. The after-life issues of such electronics are not yet properly solved.

Flexible electronics, which usually consist of organic materials, in contrast, could potentially be fabricated with low cost in e.g. roll-to-roll process[3]. The flexibility enables them to be used in different design conditions. In addition, they can be made by putting active materials directly where they are needed thus reducing the cost of chemicals and making disposal easier. On the other hand, flexible electronics are not expected to have high computing power, comparable to silicon chips, due to the limited carrier mobility of organic semiconductors[4]. As a result, the application of flexible electronics will be rather different from the traditional silicon-based electronics. The foreseeable applications of

flexible electronics include: packaging labels, flexible displays, body sensors, simple memory devices, RFID tags etc[5-11]. Many of these applications require the device to be made at low cost with fast production speeds in order to be commercially viable. Therefore, an inexpensive processing route is one of the most important aspects for the success of flexible electronics.

The building blocks of flexible electronics are field effect organic thin-film transistors (OTFTs), which at its simplest consist of four layers of materials: gate (conductive) layer, dielectric (gate insulator) layer, semiconductor layer, and source and drain (conductive) contact layer (see **Figure 1-1**). Each of these layers needs to be deposited and patterned on top of the previous one on a flexible substrate to form transistors.

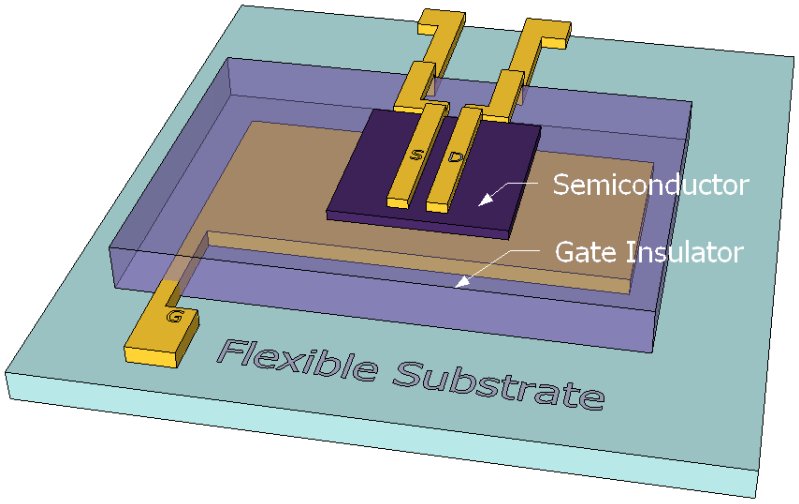


Figure 1-1 Schematic illustration of a bottom-gate top-contact transistor.

The fabrication of flexible transistors has been studied intensively in recent years. The processing techniques can be divided into two main streams: solution processes and vacuum processes. Solution processes, including inkjet printing[12], screen printing[13], and gravure printing[14], are widely investigated, but they show the following problems: 1). The precursors are difficult to prepare e.g. inks containing nanoparticles for conductive coating, thus the process can be expensive, 2). Layer interpenetration due to the effect of

the solvent, and residual solvent which could lead to leakage and poor performance of transistors[15]; 3). Post-treatment required for solvent evaporation or curing of materials that can lead to low overall processing speed.

Vacuum processes include thermal evaporation, sputtering and flash-evaporation[18-20]. Although thermal evaporation is widely used to deposit metal contacts and small molecular semiconductor layers, e.g. for organic light emitting diode in large scale[16-17] and for OTFTs in lab scale, vacuum process has not been considered for roll-to-roll fabrication for OTFTs by many researchers, probably due to the limited availability of roll-to-roll vacuum facilities in lab scale. In contrast to solution processes, vacuum deposition has the following merits: 1). No solvent is required, hence there is freedom to deposit multiple layers; 2). Materials or precursors can be used in their raw form; 3). The absence of oxygen can be beneficial for many deposition processes including curing of polymers, or deposition of semiconductors that are sensitive to oxygen and light as well as encapsulation layer deposition.

Although there are already established industrial processes for deposition of metal, ceramic and organic materials[18-20] it is still pioneering work to combine all the layers together to make functional transistors and circuits in vacuum, in a roll-to-roll based process.

This task can be divided in to four small packages: metal contact deposition and patterning, dielectric layer deposition and patterning, semiconductor layer deposition and patterning, and the integration of all the processes. This study focuses on the deposition of the dielectric layer in a roll-to-roll web coater whilst exploring the possibility of fabricating complete transistors in a vacuum environment.

The specific objectives of the project are to:

1). Develop a process to fabricate the dielectric layer at relatively high speed in a roll-to-roll environment;

2). Fabricate transistors by vacuum evaporation process based on the dielectric layer;

3). Improve the transistor performance by optimising the dielectric layer.

4) Characterise the performance and degradation behaviour of the transistors;

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Chapter 2

Literature Review

2.1 Introduction

Organic field effect transistors started to emerge in the 1986s[1] following the development of conjugated organic semiconductors, which form the active layer in a OTFT. To date, a great number of papers have been published on OTFTs from synthesis of organic semiconductor to transistor fabrication as well as device performance simulation[1-9]. One of the attention attracting aspects, in terms of processing especially, is the dielectric layer of transistors, which is responsible for transferring the electric field while insulating against electric current between the gate electrode and the semiconductor layer.

This review aims to give a comprehensive introduction from the fundamental understanding to recent fabrication technologies for OTFTs with an emphasis on the dielectric layer.

2.2 Fundamentals of Organic Thin-Film Transistors

In this section, the principle of operation of OTFTs, the methods by which they are typically characterised, as well as the fundamentals of dielectrics will be introduced.

2.2.1 Operation of Thin-Film Transistors

An organic thin-film transistor (OTFT) is a switch with source, drain and gate terminals. It can be considered as a Metal-Insulator-Semiconductor (MIS) junction with a pair of electrodes (source and drain) connected to the semiconductor layer (see **Figure 2-1**). Depending on the energy level alignment of the MIS junction, a conventional silicon transistor can be in four modes: accumulation, flat band, depletion and inversion. For an ideal MIS, the Fermi level of the gate electrode and the semiconductor align at the same energy (see **Figure 2-2** left), the transistor is off and is in the flat band mode. When a negative voltage is applied to the metal electrode, the energy level of the gate metal rises up. This electric field is transferred by the dielectric to the semiconductor dielectric interface, thus increasing both the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular level (LUMO) of the semiconductor near the dielectric surface, so called band bending. As the HOMO level of the semiconductor reaches the Fermi level, holes, in the case of p type semiconductors, will be generated and be able move near the dielectric surface. This layer of movable charge carriers connects the source and drain, so the transistor is on. This mode, the accumulation mode, is what most OTFTs operate in (see **Figure 2-2** right).

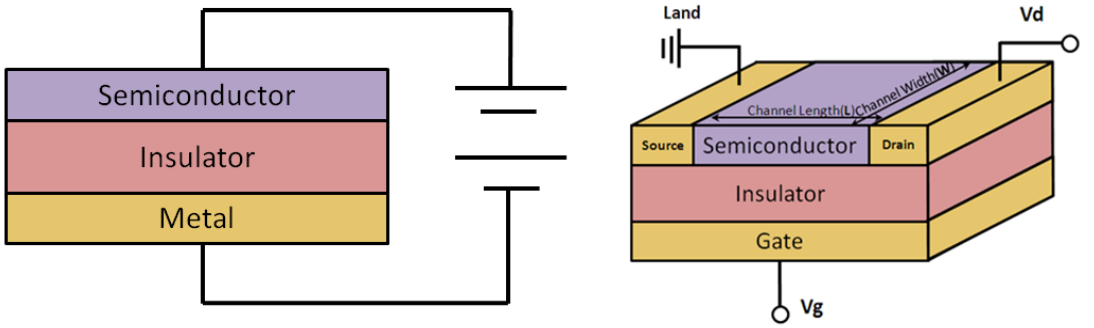


Figure 2-1 Schematic structure of a Metal-Insulator-Semiconductor (MIS) junction (left), and a bottom gate top contact field transistor (right).

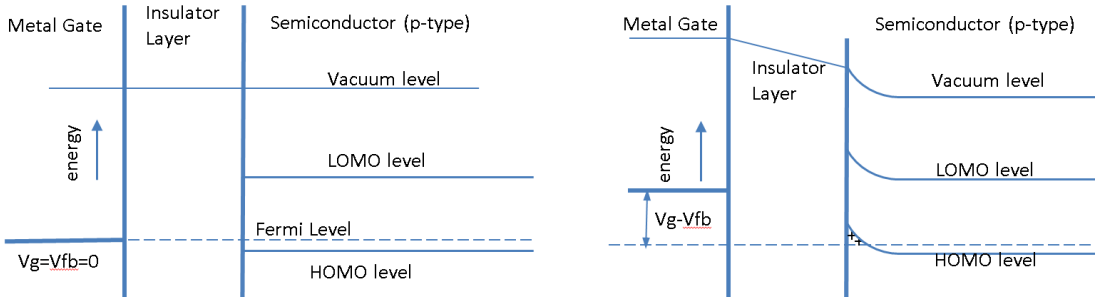


Figure 2-2 Schematic band structures of a MIS junction in flat band (left) condition and accumulation condition (right).

When the gate bias is positive, the HOMO level bends in the opposite direction, i.e. away from the Fermi level, and so a depletion region is formed at the interface between the dielectric and semiconductor. The connection between the source and drain is off and the device is in the, so called, depletion mode. When the positive bias is high enough, the LUMO level of semiconductor reaches the Fermi energy, the opposite charge carriers (electrons) will collect in the semiconductor and transistors will be turned on in the, so called, inverse mode. The inverse mode is very rarely observed in OTFTs[2] and is not the mode transistors are usually operated in. Therefore the study focus of transistor operation is on the depletion, flat band and accumulation modes. For the n-type semiconductor, the same situations are applied with voltage reversed i.e. accumulation of electrons happens in positive gate bias and depletion mode in negative bias.

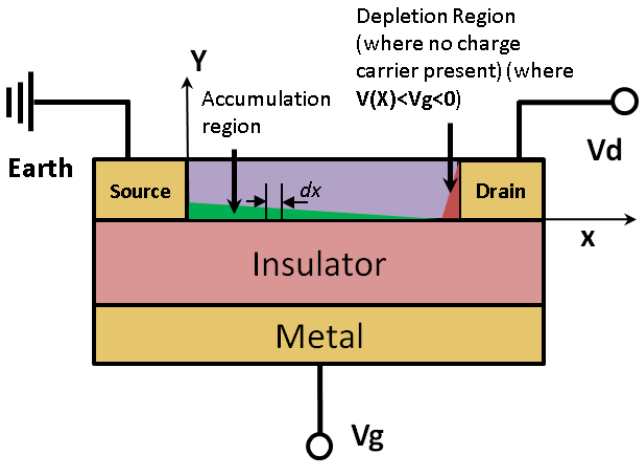


Figure 2-3 Schematic illustration of a cross section of a bottom gate field effect transistor.

2.2.2 Modelling of Drain Current of OTFTs

The general model for OTFTs was introduced by Horowitz[3] in 1998. It described the relation between gate voltage and drain current for OTFTs with common organic semiconductors, e.g. P3HT or pentacene. According to the model, the charge carriers that connect the source and drain consist of both the accumulated charge at semiconductor/insulator interface and the intrinsic free charge in the bulk of the organic semiconductor. The accumulated charge at the interface of the semiconductor and insulator Q_a is equal to

$$Q_a = C_i(V_g - V_{fb} - V(x)) \tag{1}$$

where C_i is the capacitance of the insulator layer, V_g is the gate bias, V_{fb} is the voltage needed for a flat band i.e. to counteract the work function difference between metal gate and semiconductor, $V(x)$ is the potential difference at the semiconductor at a point x from the source which is connected to the ground (see **Figure 2-3**). The bulk charge per unit area across the channel plane accounts for both positive and negative free charge in the semiconductor, equal to

$$Q_0 = n_0 qt \tag{2}$$

where n_o is the density of free charges, q is the elementary charge, t is the thickness of semiconductor.

Since the elemental resistance dR at elemental segment dx of the conductive channel is inversely proportional to channel width W, carrier mobility μ and the amount of free charge $|Q(x)|$, we have

$$dR = \frac{dx}{W\mu |Q(x)|} \tag{3}$$

From the above equation the elemental voltage can be then obtained

$$dV = I_d dR = \frac{I_d dx}{W\mu |Q_a(x) + Q_0|} \tag{4}$$

Therefore

$$I_d dx = W\mu |Q_a(x) + Q_0| dV = W\mu C_i((V_g - V_{fb} - V(x)) + n_0 qt)dV \tag{5}$$

By integrating equation (5) from the source $(x = 0, V = 0)$ to drain $(x = L, V = V_d)$, we have

$$I_d \int_0^L dx = W \int_0^{V_d} \mu[C_i(V_g - V_{fb} - V) + n_0 qt]dV \tag{6}$$

Therefore

$$I_d = \frac{W}{L}\mu C_i[(V_g - V_{fb} + \frac{n_0 qt}{C_i})V_d - \frac{V_d^2}{2}] \tag{7}$$

Defining the $V_{fb} - \frac{n_0 qt}{C_i}$ as threshold voltage, V_T, then

$$I_d = \frac{W}{L}\mu C_i[(V_g - V_T)V_d - \frac{V_d^2}{2}] \tag{8}$$

When $|V_g - V_T| >> |V_d|$, the drain current linearly increases with $|V_d|$, and the transistor is in the so-called linear region

$$I_d \approx \frac{W}{L}\mu C_i(V_g - V_T)V_d \tag{9}$$

The **linear mobility** can be estimated by the trans conductance g_m, i.e. slope of I_d vs V_g

$$g_m\left(\frac{\partial I_d}{\partial V_g}\right)_{V_d = const} = \frac{W}{L}\mu C_i V_d \tag{10}$$

When the drain voltage increases to $|V_g - V_T| \leq |V_d|$, the gate electric field is cancelled by the drain voltage at the drain. A depletion region will form near the area (see **Figure 2-3**). The area of depletion region increase with $|V_d|$. As a result, I_d becomes saturated and does not increase with increasing $|V_d|$. This leads to an approximation of drain current:

$$I_{dsat} = \frac{\mu C_i W}{2L}(V_g - V_T)^2 \quad (11)$$

With this equation, the **saturation mobility** of the semiconductor can be calculated by the slope of the $\sqrt{I_{dsat}}$ versus V_g curve. The saturation mobility is that usually quoted for OTFTs[2].

It should be borne in mind that this model is based on several assumptions: (i) the channel length is substantially larger than the insulator thickness; this assumption is usually satisfied in most cases for OTFTs, except devices with ultra-small channels. (ii) it does not account for the contact resistance between semiconductor and metal contact. (iii) the field effect mobility of the semiconductor is assumed to be constant and independent of gate voltage; this however, is not usually the case. Field effect mobility is experimentally and theoretically shown to be affected by factors such as the gate voltage and temperature, the nature of the semiconductor/insulator interface, injection of charge between semiconductor and insulator and the slow polarisation of the insulator[4-7]. Researchers are building models to take more of these factors into account, at the same time compact models are built to bridge between the transistor and circuit performance[8-9], but these models are not included in scope of the discussion in this review.

2.2.3 Characterisation of Transistors

IEEE Standard Test Methods for the Characterization of Organic Transistors and Materials[10] is available for systematically characterising organic transistors. According to this standard, two primary sets of measurements are required: the first is transfer measurement (I_d vs V_g) from which field effect mobility μ and threshold voltage, V_T can be calculated, and the second measurement is IV output (I_d vs V_d) that provides information on general performance of the OTFT, e.g. degree of drain voltage saturation.

Table 2-1 shows the basic parameters needed to describe a transistor's performance.

One issue worth mentioning here is the gate bias effect during measurement. This is a general term that describes undesirable changes in a transistor that result from application of a gate voltage for long times. For ideal devices, the gate bias would not affect device behaviour i.e. IV behaviour would be constant with the length of time the gate voltage is applied during a measurement, and with repetition of measurements. Real devices are, however, affected by gate bias for diverse reasons including ionic impurities in the insulator or semiconductor[11], traps at the semiconductor/insulator interface[12], slow polarisation of the dielectric etc. As a result, devices may have a shifted threshold voltage, a mobility dependent upon measuring history, or lack of IV saturation etc. To reveal these factors in transistors, a gate bias stress test and measurement of hysteresis during cyclical applied gate voltage are recommended.

Hysteresis measurements[11] may reveal the slow polarisation of the dielectric, or of trapping/detrapping at the semiconductor/dielectric interface, however there is no standardized process yet for hysteresis measurement.

Ideally, all the transistor measurements should be in dark, to prevent photo initiated charges and degradation of the semiconductor[13], and in vacuum or encapsulated to eliminate the effect of moisture and oxygen which have been reported to be the cause of hysteresis and operational degradation of transistors respectively[14-15]. The measurement environment should be recorded.

Table 2-1 List of transistor characteristic parameters to be reported [10]

Characteristic	Standard symbol	Units

Channel width	W	μm (<1mm) mm(≥ 1mm)
Channel length	L	μm
Field-effect mobility	μ	$cm^2 \cdot V^{-1}s^{-1}$
Threshold voltage	V_T	V
On/off ratio	I_{on}/I_{off}	Unit-less
Sub-threshold swing	SS	V/decade
Trans-conductance	g_m	S
Loss tangent of gate dielectric	d	Radians or degree

2.3 Dielectric layer

2.3.1 Fundamentals

When a dielectric material is subjected in an electric field, charges in the dielectric do not move freely, as in the case of conductors; instead they shift slightly from their equilibrium place thus forming a local field that counteracts the applied electric field. This process is called polarisation. The ability of a dielectric to polarise under an applied field is quantified by its permittivity ε. This describes how much separated charge (polarised groups) can be generated in a given area by a unit electric field. The SI unit for permittivity is farads per meter ($F \cdot m^{-1}$). More commonly, the relative permittivity ε_r which expresses the extent of the permittivity of a material compared with that of vacuum is used. Usually, in metal plate capacitors, high dielectric constant materials are desirable to increase the surface charge of capacitors without increase applied voltage (see equation below).

$$Q = CV = V\frac{\varepsilon_0 \varepsilon_r A}{d} \tag{12}$$

where the Q is the charge stored at capacitor's plate; V is the applied voltage; ε_0 is the dielectric permittivity of vacuum which is 8.85×10^{-12} $F \cdot m^{-1}$; ε_r is the relative dielectric permittivity; d is the distance between parallel plates of a capacitor; A is the overlapping area of parallel plates.

2.3.2 Polarisation of a Dielectric

Polarisation in a dielectric can be classified into four types according to its origin [16] (**Figure 2-4**). The first type is electronic polarisation, originating from distortion of electrons' orbits around the nucleus under an applied electric field. This distortion displaces the centre of negative electron charge from the positive nucleus forming a dipole with reverse local field to the applied field. The second type is ionic polarisation

in which the average position of positive and negative ions changes under an applied field. The net polarisation is the sum of the average place change moments for every ion pair in the system. The third type of polarisation originates from re-orientation of groups with permanent dipoles, e.g. organic functional groups. Compared with the previous two, the orientational polarisation takes a much longer time. The last type of polarisation originates from interface effects. For heterogeneous materials, charges separate at phase boundaries because they cannot move between two phases freely. These charges build up at the interfaces depending on the applied electric field, resulting in polarisation. This type of polarisation is even slower than the orientational polarisation because the free charges, which are much fewer than the dipole groups need to move a much greater distance. **Figure 2-5** summarises the different types of polarisation as a function of frequency.

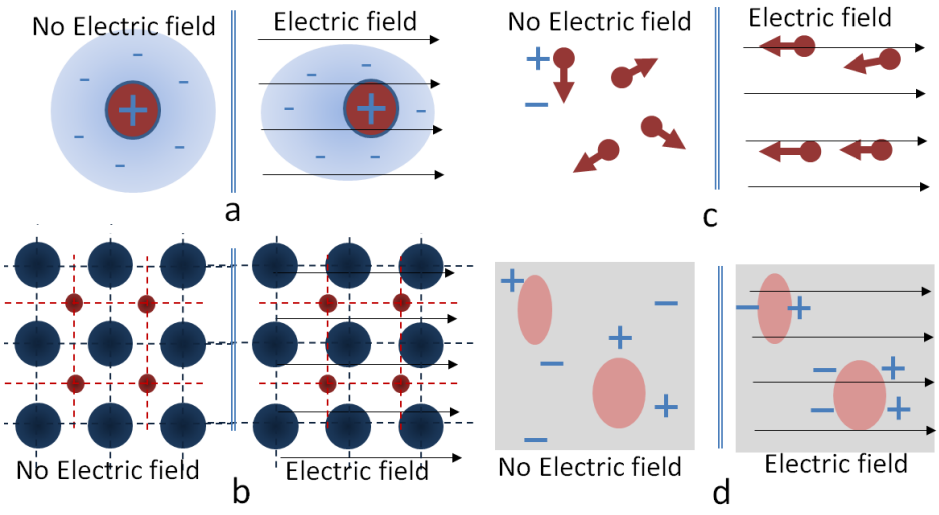


Figure 2-4 Schematic illustration of different polarisation processes a) electronic polarisation, b) ionic polarisation, c) orientational polarisation, d) interface polarisation[16].

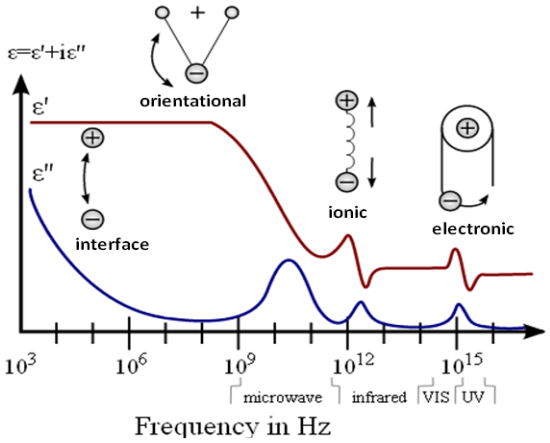


Figure 2-5 A dielectric permittivity spectrum over a wide range of frequencies. The real and imaginary parts of permittivity are shown, and various processes are depicted: ionic and dipolar relaxation, and atomic and electronic resonances at higher energies[17].

2.3.3 Permittivity

As discussed in **section 2.3.1**, permittivity reflects the extent of a dielectric response to an applied electric field by forming polarised states. Ideally, the dielectric polarisation happens immediately after the electric field is applied, however, for real materials, there is always a delay between the applied electric field and the polarising response of dielectric. Such a delay is described as relaxation which indicates the time it takes for the polarising units to rearrange themselves to a relaxed state under the electric field. To describe this relaxation delay, permittivity is expressed as a complex value shown below:

$$\hat{\varepsilon} = \frac{D_0}{E_0} = \mid \varepsilon \mid e^{i\delta} \tag{13}$$

where $\hat{\varepsilon}$ is the complex permittivity, D_0 and E_0 are the amplitudes of the electric displacement field and the applied electric field respectively, δ is the phase difference between displacement and electric field.

To separate the real part and imaginary part of the complex permittivity we can use the following convention

$$\varepsilon(\omega) = \varepsilon'(\omega) + i\varepsilon''(\omega) = \frac{D_0}{E_0}(\cos\delta + i\sin\delta) \quad (14)$$

Where ε'' is the imaginary part of the permittivity, ε' is the real part of the permittivity, ω is the frequency of applied field, and δ is the dielectric loss angle, $\tan\delta = \varepsilon''/\varepsilon'$. This equation can be physically understood as the complex permittivity consisting of both real permittivity, ε', which accounts for energy storage during the displacement process, and the imaginary permittivity, ε'', which accounts for energy loss during the process.

Complex permittivity can be measured by impedance spectroscopy, which is based on monitoring the interaction of the dielectric with an external oscillating electric field over a range of frequencies. Impedance spectroscopy can also be used to determine the presence of different dipole species in the dielectric, because of its high sensitivity to the relaxation rate.

2.3.4 Dielectric Strength

Dielectric strength is the maximum electric field strength that an insulator can withstand without breakdown i.e. experiencing failure of its insulating properties. The common unit for dielectric strength is $MV \cdot cm^{-1}$.

Theodosiou[18] speculated that breakdown of a polymer dielectric involves two main steps. The first step starts from charge injection: the injected electrons might cause ionisation of macromolecules thus transforming them to macro ions. In the second step, carbon bonds in the macro ions are weakened through a thermo-fluctuational mechanism when subjected to the electric field, and finally rupture in this process, leading to damage to polymer chain structures. This damage builds up with time and results in the final breakdown[19-21].

Polymer films usually give high leakage current before final breakdown, a so-called 'soft breakdown' [16]. Two main factors in polymers can lead to the high leakage: the first is the disorder of polymer chains, either in terms of chain tacticity or their 3D arrangement; and the second is chemical disorder of polymer chain structures. Both types of disorder induce localised states in the band-gap of the dielectric. The localised states then may lead to charge transport in the insulator by two possible mechanisms: one is incoherent tunnelling in which electrons tunnel resonantly between two or more consecutive sites that are characterised by potential wells [22-23]; the other is hopping [24-25] [24, 26-31] in which thermally activated electrons successively trap and detrap from each delocalised site thus passing through the insulator layer. The difference between tunnelling and hopping is that the latter one is able to occur over a greater distance between two localised sites. Charge transport in a polymer film may also be ascribed to other mechanisms, including, quantum tunnelling [32-33] and the Poole-Frenkel effect [32-36], which will not be discussed here.

2.4 Semiconductors

Organic semiconductors for thin-film field effect transistors are organic molecules or polymers with pi-conjugated aromatic components which give rise to delocalised filled and empty pi orbitals. According to their structures, these semiconductors can be classified into two main groups: long chain polymers and molecular materials (see **Figure 2-6**). The long chain polymers appear to be easier to apply in large area applications by solution based techniques [37-39], while the molecular semiconductors give better performance in terms of mobility because of they are more likely to obtain a highly ordered molecular organisation either from solution or vacuum processes. Although it is not known which class of material will dominate the future market, current research is more focussed on the latter type[40-41]. For more information on organic semiconductors for OTFTs, many good recent reviews are available[38, 42-45].

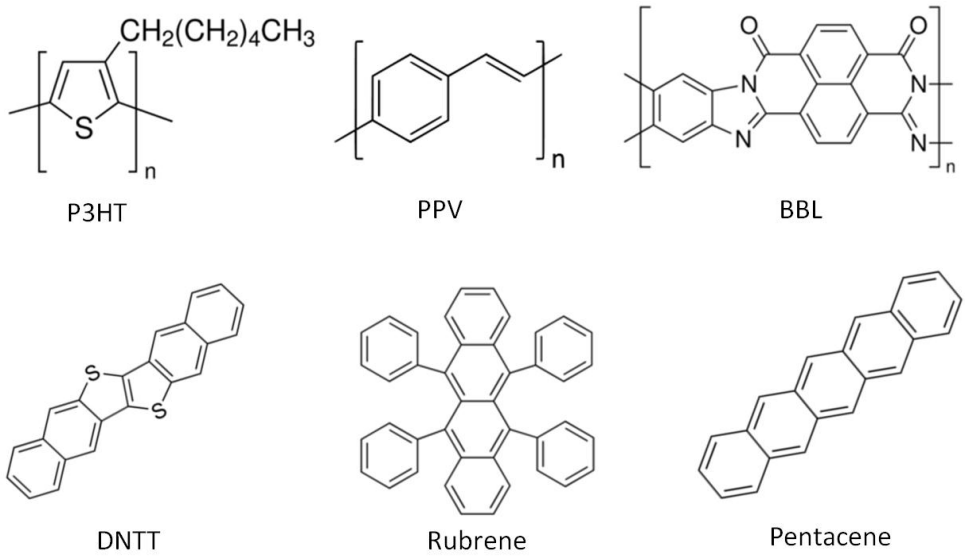


Figure 2-6 Molecular structure of conjugated polymers (top): poly(3-hexylthiophene)(P3HT), poly(p-phenylene vinylene) (PPV), Poly[(5,6-dihydro-5-octyl-4,6-dioxo-4*H*-thieno[3,4-*C*]pyrrole-1,3-diyl){4,8-bis[(2-butyloctyl)oxy]benzo[1,2-*b*:4,5-*b*′]dithiophene-2,6-diyl}] (BBL) and small molecules (bottom): Dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT), rubrene and pentacene.

2.5 Device Fabrication and Challenges

2.5.1 Configuration of Thin-Film Transistors

Depending on the arrangement of the MIS junction and source and drain contacts, four possible OTFT configurations can be made. They are top-gate bottom-contact transistors (TGBC), bottom-gate top-contact transistors (BGTC), top-gate top-contact transistors (TGTC) and bottom-gate bottom-contact transistors (BGBC) (see **Figure 2-7** below).

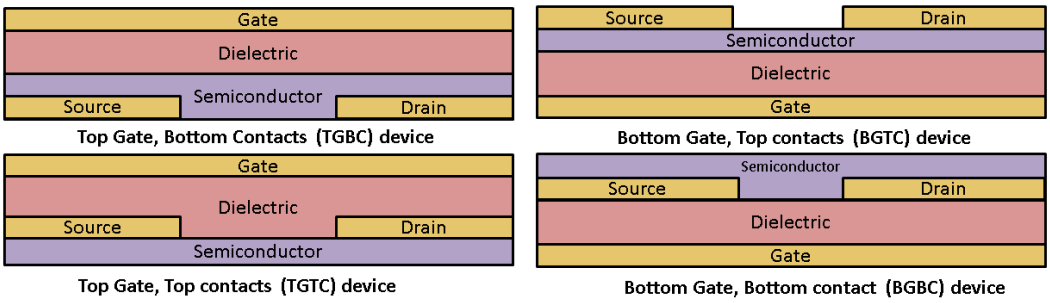


Figure 2-7 Schematic illustration of the different OTFTs configurations.

The most common configuration found in research papers is the BGTC[38, 45-46]. This is mainly due to processing convenience, since deposition of a dielectric layer on top of the semiconductor could lead to damage to organic semiconductors. The BGTC configuration also enables surface treatment of the dielectric layer e.g. self-assembled monolayer (SAM) or buffer layer treatment before deposition of semiconductor, which has been shown can improve OTFTs performance significantly[47]. In addition, a BGTC, as well as TGBC, configuration can provide a large area of semiconductor being sandwiched by the source and the gate leading to improvement of the carrier injection from the source contact to the semiconductor layer[48-49]. The major limitation of BGTC is the difficulty in patterning the source and drain layer on top of the semiconductor layer, especially in many large area-based process including screen printing, gravure printing etc., because these processes usually require the substrate i.e. semiconductor layer, to be in contact with the printing apparatus by which the semiconductor layer is prone to be damaged.

The mostly frequently used technique for source and drain deposition therefore is still traditional lab scale thermal evaporation through a shadow mask. The very few large scale processes reported include ink jet printing[50] and gravure printing[51]. The device performance is summarised in **Table 2-2**.

The TGBC configuration provides freedom for the source and drain layer deposition. High speed medium-resolution printing of source and drains is achievable[39]. Similar to the BGTC configuration, the charge carrier injection from drain to semiconductor in this case is easy. Another advantage of BCTG is that the gate and dielectric layer on top of the semiconductor provide protection for the semiconductor, which could be beneficial for the encapsulation layer deposition process, if required. However, the dielectric layer deposition on the semiconductor could be problematic. The material choice is limited to solution-based linear polymers e.g. poly(perfluoroalkenylvinyl ether) (Cytop), poly(t-butylstyrene) (PTBS), which require no curing[39]. The semiconductor layer deposition is also critical because apart from good semiconducting properties, the surface finish of the semiconductors has to be smooth for subsequent dielectric layer deposition to realise a trap free interface for carrier transport[39]. This makes the vacuum evaporated semiconductors unsuitable for BCTG configuration, since vacuum deposited semiconductors usually have high roughness due to crystallisation of the semiconductors.

The BGBC configuration, i.e. with semiconductor on top, also ensures that source and drain layer, as well as the dielectric layer could be printed and patterned without damaging the semiconductor layer. However, it usually leads to high contact resistance[52] due to a) small effective area of the source and activated semiconductor and b) the effect of the corner of the metal contact which leads to local disorder of the semiconductor crystals.

2.5.2 Dielectrics for Organic Thin-Film Transistors

A good dielectric layer for an OTFT is required to have high dielectric strength, low leakage, and high geometric capacitance. It should also lead to transistor devices with high on/off ratio, low hysteresis and reliable performance. In addition, it should be applicable in large scale low cost fabrication processes.

In the early studies, organic dielectric materials with high dielectric constant, k (k is considered equal to real permittivity ε') appear to be favoured by researchers because they are liable to provide high capacitance even with high thickness[1, 53-56]. One of the first successful fabrications of OTFTs with organic dielectrics was reported by Peng *et al.* [53] in 1990. By using cyanoethylpullulan (CYEPL; k ≈ 18.5 at 10KHz) as the dielectric layer and α-sexithienyl (α6T) as the semiconductor, transistors with a field effect mobility of 0.43$cm^2 \cdot V^{-1}s^{-1}$ were claimed. This was 100 times higher than that of the low k dielectrics, i.e. styrene, PVA, PMMA, used in this research. However, Veres *et al.*[12] pointed out that the high k dielectric CYEPL was strongly frequency dependent due to its slow polarisability. There were large deviations between the capacitance values for transistors and the measured capacitance by impedance spectroscopy, and the CYEPL brought large hysteresis for devices[57].

Veres *et al*. proposed that low k non-polar dielectrics are a promising route to provide better OTFT performance than high k dielectrics[57]. He compared polar dielectrics including PMMA (k≈3.5) and PVA (k≈7.5) with a low k nonpolar dielectrics: fluoro-polymer, poly(perfluoroethylene-co-butenyl vinyl ether) (k≈2.1) in both bottom and top gate poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA) (as semiconductor) transistors. The amorphous semiconductors PTAA, and the top gate transistor configuration enabled the authors to exclude dielectric film morphology effects on semiconductor field effect mobility. The results showed the low k polymer gave a

noticeable improvement to device performance in terms of hysteresis, mobility and shift in threshold voltage. It is worth criticising that all the k values quoted in this paper was not accompanied with the measuring frequency and temperature. Veres *et al.* extended the experiment to two other low k polymers including polyisobutylene, poly(4-methyl-1-petene), and copolymers of polypropylene. They all showed a higher field effect mobility than that of the polar dielectrics. The authors explained this effect as the polar groups in higher k dielectric broadening the density of states of the semiconductor, thus increasing the localisation effect for charge carriers. An alternative explanation was proposed by Hulea *et al.*[58]: the authors suggested Fröhlich polarons induced by polarity of the dielectric surface was responsible for low mobility of high k dielectrics. The detailed mechanism however is not yet fully understood.

In more recent papers, low k or medium k dielectrics have attracted more attention than the high k organic dielectrics. The low k dielectric layers for OTFTs published in recent years are reviewed here based on the processing route.

2.5.2.1 Spin Coating

All solution-based dielectrics can be deposited by spin coating, which, however, is a slow batch-to-batch process. The traditional spin-coated linear dielectrics e.g. PMMA[39, 57], PS[39] and PVA[53] are not reliable under high electric field, and they can be damaged by solvents, and therefore are generally not regarded as commercial candidates for dielectrics layers[59]. In contrast, one type of spin-coated fluorine based polymer, poly(perfluoroalkenylvinyl ether) (Cytop k=2.1)[57, 60] (**Figure 2-8**), showed leakage as low as 10^{-8} A·cm^{-2} under an electric field of 5 MV·cm^{-1} with thickness less than 100nm. Cytop also appears to have good solvent resistance during semiconductor deposition[60]. It also showed a low k dielectric surface which is desirable for p-type organic semiconductor transistors[59]. The polymer was used in batch-to-batch process for device fabrication according to the recent report by the Centre for Process Innovation (CPI) UK.

Cytop has also been used in large scale processing e.g. gravure printing, which will be introduced later.

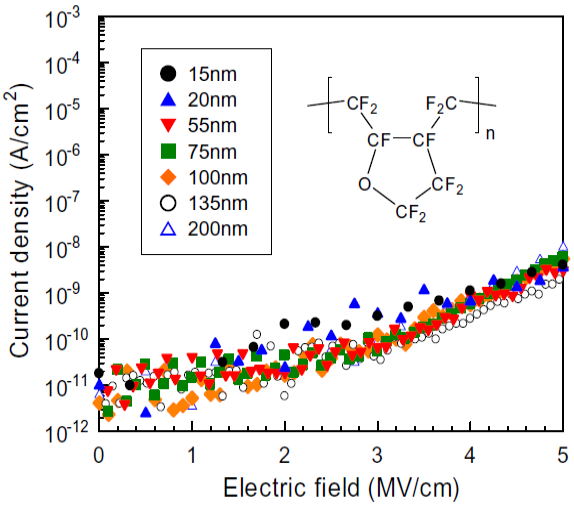


Figure 2-8 Current density-electric field (J-E) characteristics of thin films of amorphous fluoropolymer, Cytop. Thin films were formed by spin coating. The inset shows the chemical structure of Cytop[60] (Copyright (2008) permission from Elsevier)

Cross-linked polymers usually have better reliability in terms of thermal-mechanical robustness, solvent resistance and low leakage current[61], compared with non-cross-linked polymers, thanks to the covalent bonds between polymer chains[59]. The poly vinyl phenol (PVP) is one of the most frequently used cross-linkable polymers[61-62,63]. Its cross-linking formula is very well studied[64] and has been the subject of several patents[65]. A few crosslinking formulas are shown in **Figure 2-9**. It was observed that an ultra-thin 25 nm PVP film cured with 4',4'-(hexafluoroisopropylidene)diphthalic anhydride (HDA) cross-linker had a leakage current lower than 10^{-8}A·cm^{-2} under 1MV·cm^{-1}. Another advantage of PVP over other dielectrics is that its surface is suitable for the deposition of most p-type organic semiconductors, giving high mobility e.g. 0.7~1cm^2·V^{-1}s^{-1} (**Table 2-2**). However, the curing time of more than 20 minutes at elevated temperature of at least 100 °C is required for the cross-linking.

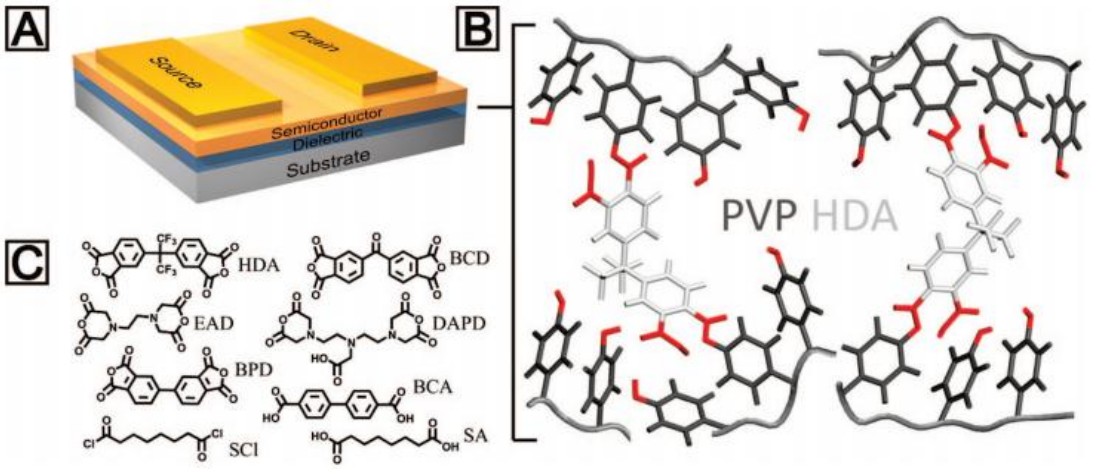


Figure 2-9. Schematic of an organic thin-film transistor (A) with the molecular structure of the cross-linked PVP with HAD (B). The molecular structure of a variety of dianhydrides and bifunctional carboxylic acids and acylchlorides is shown in (C)[64] (Copyright (2009) from American Chemical Society).

There are other cross-linkable polymers or oligomers e.g. cinamates[66], acrylates[63], that have been used as a dielectric. The details of the material formulas are presented in **Figure 2-10** and **Figure 2-11**, and the device performance is summarised in **Table 2-2**. In general, they showed reasonably good dielectric properties, however, as with PVP, a long curing time was required in all cases.

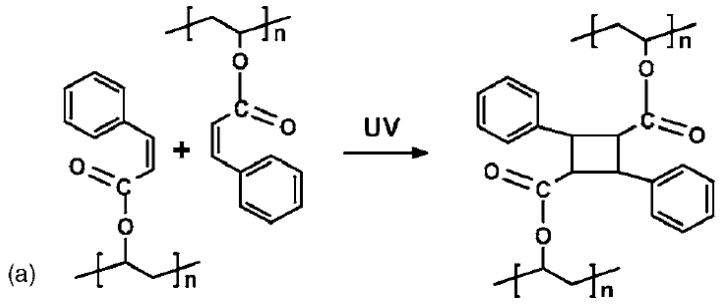


Figure 2-10 The chemical structures of PVCN (left) and photochemically cross-linked PVCN (right)[66].

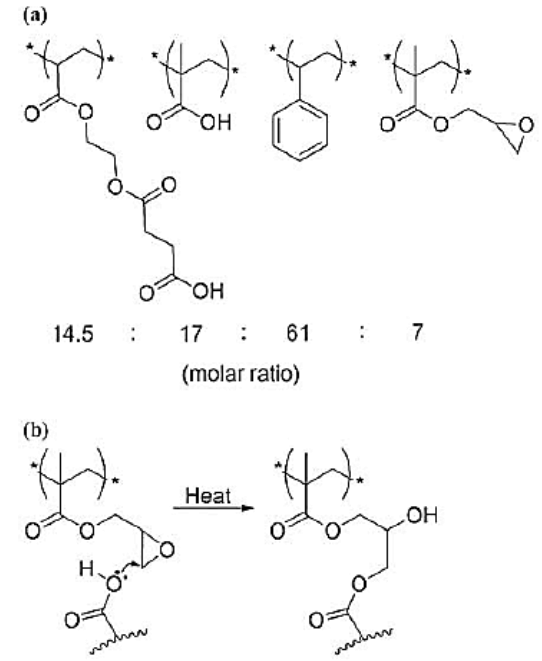


Figure 2-11 (a) Repeat units in PA copolymers and the corresponding molar ratios, (b) mechanism of cross-linking reaction between functional groups[63].

2.5.2.2 Gravure Printing

Gravure (rotogravure) printing enables film forming in a roll-to-roll based process at a speed of up to 15 meters per second and with substrate width of up to several meters[67]. The process employs a patterned gravure cylinder to print onto a flexible substrate that is constantly moving against a rotating roller (**Figure 2-12**).

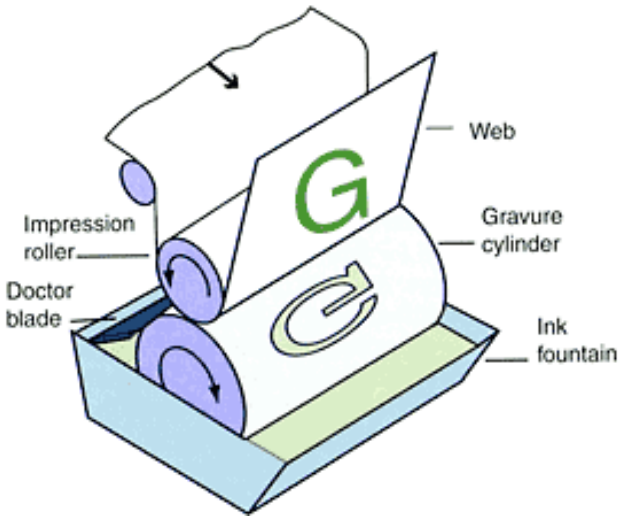


Figure 2-12 Diagram of rotogravure process[67].

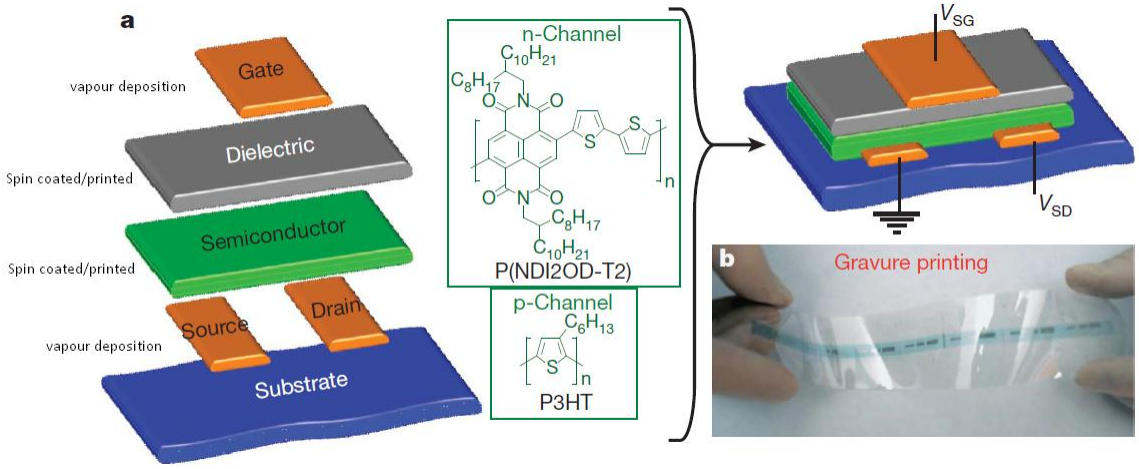


Figure 2-13 Organic thin-film transistor structure, fabrication and operational principles. a) Illustration of the TFT material components (left), chemical structure of P(NDI2OD-T2) and P3HT semiconducting polymers, and of the top-gate bottom-contact (TGBC) TFT architecture (right) used in this study. b) Optical images of gravure-printed TGBC TFTs on PET before top-gate contact deposition[39] (Reprinted by permission from Macmillan Publishers Ltd: *Nature*, copyright (2009))

PVP[50], BuS[68], $BaTiO_3$ nano-powder in PMMA[51] and polyolefin-polyacrylate (Activink D2200)[39] etc., have been used in gravure printing to make dielectric layers for thin-film transistors. Among them, the most successful case in terms of transistor performance was reported by Yan[39] in *Nature Materials*. Their work was based on bottom contact top gate transistors with poly{(N,N'bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)2,6diyl)-alt-5,5'-(2,2'-bithiophene)} (P(NDI2OD-T2) as the n-type semiconductor and poly 3-hexylthiophene(P3HT) as the p-type semiconductor (**Figure 2-13**). A family of low k dielectrics were used, which were deposited both by spin-coating and, in some cases, by gravure printing, i.e. polyolefin-polyacrylate (Activink D2200, k=3.2) and PMMA (k=3.6). Field effect mobility in the ranges 0.10-0.65 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 0.1-0.2 $cm^2 \cdot V^{-1} \cdot s^{-1}$ was observed in the n-type transistors with the Activink D2200 and PMMA respectively. The mobility appeared to be insensitive to variation between the dielectric layers, but was sensitive to processing method and surface finish of the

semiconductor layer, i.e. the roughness of the interface of dielectric and semiconductor. According to the authors, the top gate configuration provided a certain level of protection (encapsulation) for the semiconductors by covering it with dielectric layer and metal gate layer thus enabling the devices to have reliable performance and long life time in air.

2.5.2.3 Inkjet Printing

Inkjet printing is slower than gravure printing but consumes less raw material for deposition. It is suitable for semiconductor layer deposition in which the material cost is the main concern. Many fewer cases were found for dielectric layer deposition[69-70].

Eum[69] reported an inkjet printing process for organic thin-film transistors with PVP as the dielectric layer (see **Figure 2-14**). A gold gate was firstly deposited on the substrate using a shadow mask, then a 80 nm PVP dielectric layer was formed using an inkjet printer with a 50 μm printing head. The film was subjected to curing at an elevated temperature of up to 200 °C for 30 minutes. After curing, the film still showed leakage current of 10^{-6} V·cm^{-2} under bias of 20 V (equivalent to 2.5 MV·cm^{-1} for 80 nm film). The active layer was TIPS-pentacene deposited by a inkjet printer. A mobility of 0.055 cm^2·V^{-1}·s^{-1} and on/off ratio of 10^3 was observed.

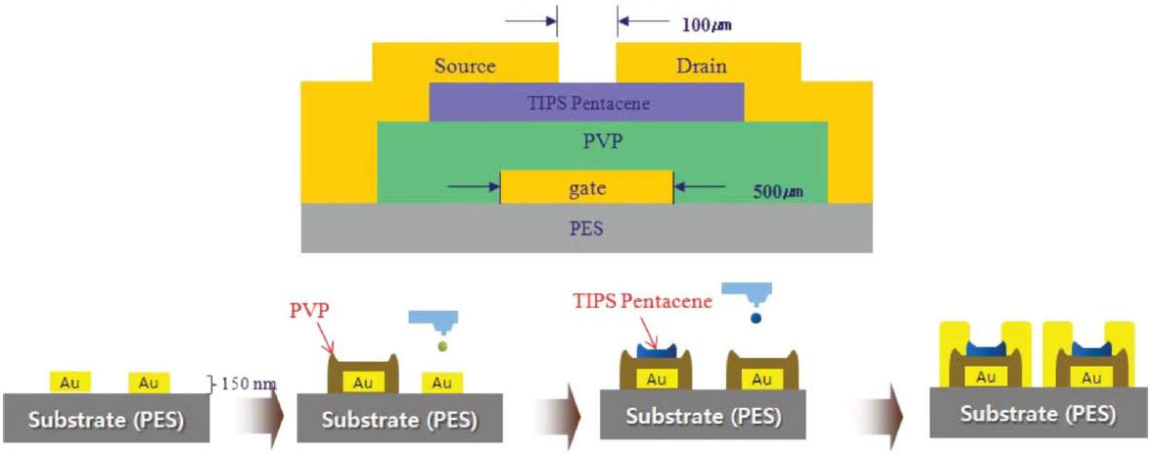


Figure 2-14 OTFT structure and process flow for devices fabricated using inkjet printing[69] (Copyright (2010), American Vacuum Society)

Jeong[70] reported inkjet deposition of a cross-linkable organosiloxane-based hybrid material. A leakage current of 10^{-6} A·cm^{-2} was claimed with a layer of thickness about 60 nm under voltage stress of 90 V (15 MV·cm^{-1}). No detailed IV curve was presented in the paper however. The device mobility was less than 10^{-2}·cm^2·V^{-1}·s^{-1} for bottom gate bottom contact transistors with α,ω-dihexylquaterthiophene (DH4T) semiconductor.

In general, the inkjet-printing of dielectric was still a relatively slow process that requires post curing annealing. The flatness of the deposited layer was also an issue of concern[69].

2.5.2.4 Vacuum Deposition

The vacuum evaporation method was another approach for dielectric deposition. Yoon [71] reported a 10-layer stack of bipolar gate dielectric deposited layer by layer by pulsed radio frequency (RF) plasma polymerisation[72] of allylamine and vinyl acetic acid monomers (see **Figure 2-15**). The polar groups in the consecutive layers (-NH_2) and (-COOH) are thought to interact with each other with the expectation that this would lend a distinctive mechanical and chemical robustness. The film gave a dielectric constant of 4.4. An extremely smooth surface with RMS roughness of 0.129 nm (1 μm by 1 μm) was achieved. The 10 layer film showed a dielectric strength in excess of 4 MV·cm-

[1], however a leakage current of 10^{-6} A at 2 MV·cm^{-1} was observed. The film was reported to be robust enough to withstand a conventional photolithographic process. With the P3HT organic semiconductor, a mobility of 0.0034 cm^2·V^{-1}·s^{-1} was observed.

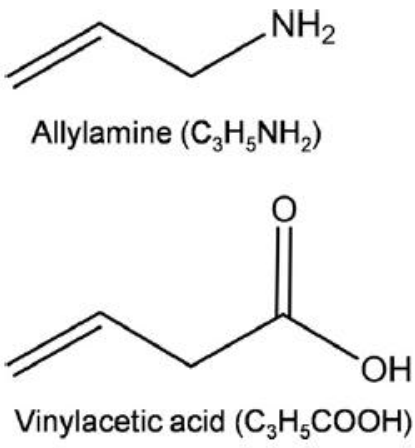


Figure 2-15 Chemical structure of monomers used for polymerization under pulsed RF plasma condition: an amine (–NH_2) containing monomer, allylamine ($C_3H_5NH_3$), and a carboxylic acid (–COOH) containing monomer, vinyl acetic acid (CH_3COOH)[71].

Vacuum evaporated OTFTs were also reported by Irimia-Vladu *et al.*[73-74]. In their earlier work, both the gate dielectric (polyaniline with RMS of 8-12nm) and the semiconductor (C_{60}) were deposited in successive steps without breaking the vacuum in the evaporation chamber (see **Figure 2-16** (b)). The polyaniline was evaporated from a precursor: emeraldine base. It was reported that the characteristics of the transistors are stable and reproducible. However, the on/off ratio was less than 1000.

In their later work, melamine was used as a dielectric layer. The melamine film showed a RMS roughness of 15nm and a dielectric constant of 4.5. With a 600 nm melamine layer the leakage current was less than 1 nA·cm^{-2} under an electric field of 0.3 MV·cm^{-1}. A field effect mobility of 0.1-0.3 cm^2·V^{-1}·s^{-1} was observed for C_{60} (measured in a glove box). The on and off ratio, however, was still less than 1000.

Vacuum flash evaporation is another approach to achieve large area deposition of a dielectric layer in vacuum; the details of this process will be introduced later in this dissertation. This process was firstly used in a transistor by Abbas et al.[75] in Oxford University. Before the work in this thesis started, it had been reported that by flash evaporating TPGDA followed by e-beam curing, a dielectric layer can be fabricated in a roll-to-roll process at a speed of several meters per minute. The thermally evaporated pentacene device showed an on/off ratio of 10^5 and a mobility of about 0.1 $cm^2 \cdot V^{-1} \cdot s^{-1}$. Following the work presented in this thesis, surface modification of a non-polar buffer layer, DNTT transistors based on the flash evaporated dielectric have achieved a mobility of ~1 $cm^2 \cdot V^{-1} \cdot s^{-1}$, on/off ratio of 10^6 with no hysteresis and low leakage[8, 47].

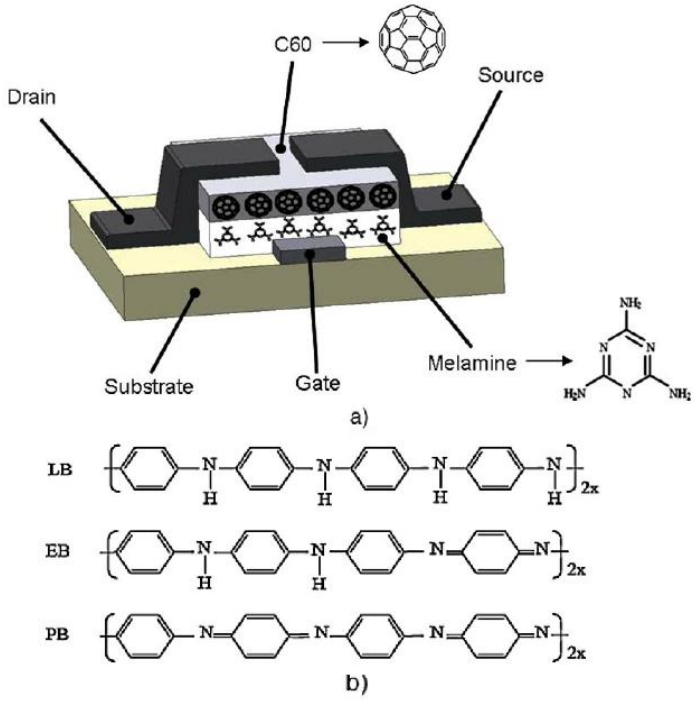


Figure 2-16 a) Schematic of the vapour deposited melamine-C_{60} OFET. The inset displays the schematic of the small-molecule melamine and C_{60}. b) A schematic of polyaniline in various oxidation states; LB) fully reduced (leucoemeraldine base), EB) half oxidized (emeraldine base), and PB) fully oxidized (pernigraniline base) forms[73-74] (Copyright (2009) permission from Elsevier,Copyright (2008) from John Wiley and Sons).

Table 2-2 Summary of dielectric layer and OTFT performance.

Ref	Dielectric	Deposition methods	Thickness (nm)	k	Dielectric strength(MV/cm)	C_i (nF/cm²)	Leakage (nA/cm²)	Mobility (cm²/Vs)	I_{on}/I_{off}	Semiconductor	Year	Channel Dimension (μm)
53	CYEPL	Cast		18.5		6		0.034		6T	1990	L=90; W=310
	PVA			7.8		10		0.00093		6T		
57	Cytop	SC	500-800	2.1				0.00331		PTAA	2003	L=40-120; W=1-31mm
	PMMA	SC	500-800	3.8				0.00048		PTAA		
76	PVP	SC	400-500					0.01-0.02		F8T2	2000	L=5, W=3mm
61	PVP-co	SC	380	4		11-12		2.9	10^5	P5	2002	L=130, W=170
	C-PVP	SC	260	3.6		11-12		3	10^5	P5		
62	C-PVP175°C curing	SC			1.5	5.2		0.07	10^5	P5	2006	W=500; L=90
	C-PVP 200°C curing	SC			<1.5	5..0		0.13	10^3	P5		
64	C-PVP (HDA cross linker)	SC	20-25			~200	100-1000	0.7	10^5	P5	2009	L=50; W=1mm
66	PVCN	SC	530	3.37		5.62		0.51	10^6	P5	2008	L=150; W=1.5mm
77	Photo-cross-linkable PVP	SC	10-500		>1		<10	0.3	10^5	P5	2007	L=100; W=5mm
78	PVP; Trimethylolpropane triglycidyl ether	SC		4.2		6.6		0.5	10^7	P5	2007	L=100; W=1mm
63	Poly-acrylate	SC	150	2.9-4.4	7	14-20	5(1MV/cm)	0.3-0.6	10^{4-5}	P5	2010	L=150; W=1.5mm
50	C-PVP (UV curing)	GP					3.8 (0.67 MV/cm)	0.02	10^4	Tips-P5	2011	L=47; W=247
51	PMMA $BaTiO_3$	GP	2300			6	50pA, 20V	0.15	10^4	SWCNT	2012	L=170; W=3mm
68	BuS	GP						0.0013	320	F8T2	2007	L=100; W=6mm;30mm
39	Cytop	SC	450-600	2				0.1-0.25	10^{6-7}	P(NDI2OD	2009	L=50; W=1mm
	PTBS	SC	600-800	2.4				0.1-0.4	10^{6-7}	-T2)		
	PS	SC	500-700	2.5				0.1-0.3	10^{6-7}			
	ActiveInk D2200	GP	350-500	3.2				0.1-0.65	10^{5-7}			
	PMMA	GP	600-900	3.6				0.1-0.2	10^{4-6}			
69	C-PVP	Inkjet	80	2.5-5				0.055	10^3	P5	2010	L=100; W=1.5mm
70	Hybrid	Inkjet	60	4.9	0.8	4.9	1000, (0.8M/cm)	0.002		DH4T	2008	L=100; W=3mm
71	Stack bipolar layer	PP	60	4.4	4	57.3	734 (2MV/cm)	0.0034	10^2	P3HT	2010	L=7; W=135
73	Polyaniline	TE	650-1750	3.35		1.63	1 (0.1MV/cm)	0.15-0.55	10^3	C_{60}	2008	L=100; W=1mm
74	Melamine	TE	600-1500	4.25		3.85	<1 (0.3MV/cm)	0.1-0.3	10^3	C_{60}	2009	L=100; W=1mm

Abbreviations: SC, spin coating; GP, gravure printing; PP, plasma polymerisation;, C-PVP, cross-linked PVP; PVP-co, PVP-copolymers; P5, pentacene; TE, thermal evaporation

2.5.3 Dielectric/Semiconductor Interface

The dielectric/semiconductor interface can affect the performance of OTFTs significantly. On one hand, in bottom gate devices, the dielectric surface conditions i.e. roughness and surface energy affect the morphology of semiconductor deposited onto it. On the other hand, the surface chemistry [79-80] and polarity [57, 81-82] of the dielectric surface affect the formation and performance of the conductive channel in the semiconductor close to the dielectric interface. Understanding the growth of semiconductor on the dielectric surface and the interface formed between the dielectric and semiconductor is crucially important for thin-film transistor design and fabrication. In this section, recent research related to vacuum based semiconductor growth on a dielectric surface and the dielectric semiconductor interface will be reviewed.

2.5.3.1 Growth of Semiconductors on a Dielectric Surface

Small molecule semiconductors, e.g. pentacene and its derivatives, have showed the highest field effect mobility and on/off ratio among organic semiconductors[44]. This high performance is achieved only when the small molecules are packed in certain regular structures, either through deposition, which commonly is organic vapour phase deposition[83] and thermal evaporation[84], or through controlled crystallisation processes during solvent evaporation. The crystal growth during a vacuum deposition process is the focus in this section.

Pentacene is the most intensively studied organic molecular semiconductor. At least four different pentacene crystal structures have been recognised[85], among these polymorphs, the bulk phase[13] and the thin film phase[86] are of most interest. Having studied pentacene growth on organic and inorganic surfaces with the assistance of XRD, AFM and Raman spectroscopy, Cheng [87] proposed that pentacene packing morphology varies through the film thickness during deposition (see **Figure 2-17**). The first pentacene layer on the dielectric surface appeared to standing perpendicularly to the substrate, forming the

'thin film' phase. This phase showed good pi-orbital overlap structure and thus is able to provide good conductivity for hole transport[88]. After the first few layers, the pentacene molecules gradually tilted to a certain degree. This tilted pentacene formed a bulk phase which has a poor degree of pi-orbital overlap and so is not preferred for hole transport. The authors also suggested that obvious inhomogeneity existed at the phase boundaries where the pentacene structure transfers from one phase to another. Such inhomogeneity sites have recently been directly observed by TEM[89]. They are believed to limit charge transport in the semiconductor and could result in degradation of OTFT performance [87].

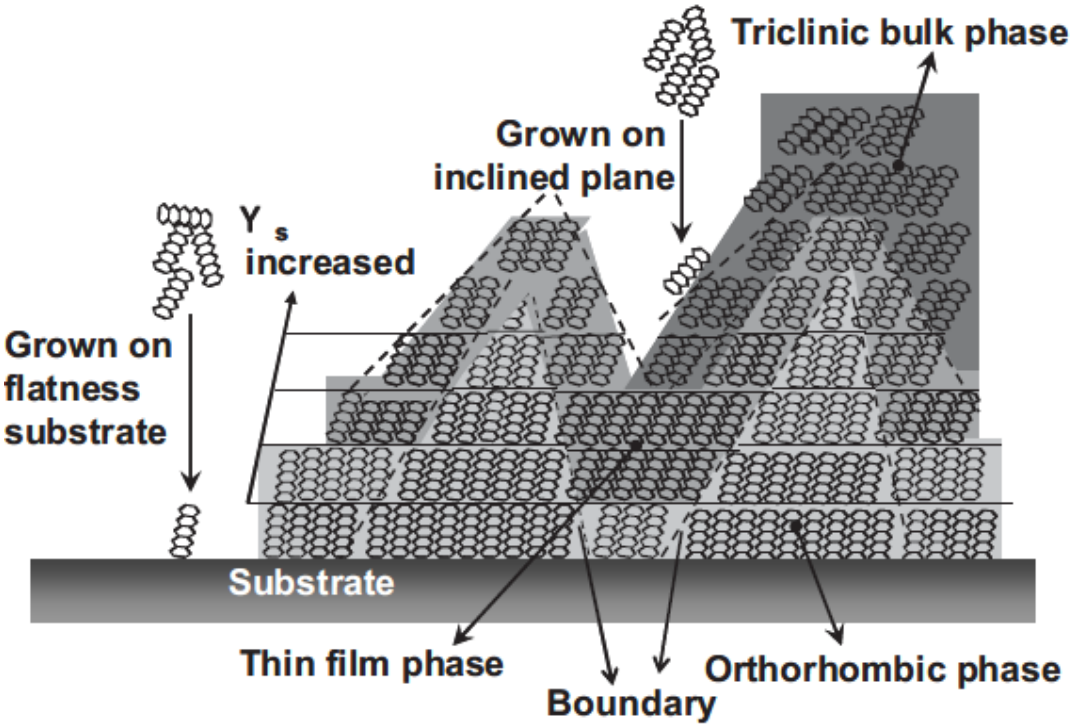


Figure 2-17 Schematic showing the evolution of thin-film polymorphs of pentacene film with increasing thickness[87] (Copyright 2007 from John Wiley and Sons)

Meyer zu Heringdorf[90] studied the nucleation of the first few layers of pentacene on a SiO_2 surface and the effect of substrate, deposition temperature and deposition rate. They reported that the nucleus size of the first few layers was closely related to both the

diffusion constant of the pentacene on the substrate and on the deposition rate. A much lower nucleation density was observed after using e-beam radiation to treat the substrate surface through which the diffusion constant of pentacene on the surface was increased. On the other hand, it is observed that decreased nucleation density resulted from a lower deposition rate.

Kim *et al.*[91] suggested that pentacene morphology was closely related to surface energy, deposition temperature, and deposition rate. He studied the growth of pentacene on organic (PVPs and PS) modified SiO_2 surfaces. The results showed that the PS surface, with a lower surface energy, provided a growth mode of "layer+island"[92] for the first pentacene layer. Kim proposed that a percolated pentacene film of the thin film phase, was formed first on the substrate. The following layers of pentacene started to build up vertically thus finally forming dendritic crystals. He also found the grain size increased with decreasing deposition speed. For the PVP surface, with a higher surface energy, the pentacene molecules tended to self-assemble directly into discrete islands of triclinic bulk phase on the substrate, rather than attach and spread on the substrate as continuous layer. Due to the existence of the rough discontinuous islands, pentacene crystals on this substrate were small. The mobility of film grown on the PS surface was about 4 times higher than on the PVP.

It is interesting that when the substrate temperature was increased to 80^{o}C, the pentacene growing on the PS surface transferred from the 'layer+island' mode to 'discrete island' mode and a much smaller grain size was observed. The authors argued that this transfer was due to the higher substrate temperature giving more freedom (energy) for pentacene, especially for the first few layers, to directly build vertically into islands rather than spread laterally into a percolated layer. However, similar research conducted on a SiO_2 surface showed pentacene dendritic grain size increased with

increased substrate temperature even when the substrate temperature surpassed 80°C[93]. As such, the change in growth mode in Kim's experiment was more likely due to the change of the surface of PS at high temperature. Kim *et al*. reported[94] that the viscoelasticity of the dielectric surface significantly affects growth of the semiconductor and thus the performance of devices. They revealed that the pentacene thin films grown on polymer gate dielectrics exhibit distinctive and abrupt morphological and microstructural transitions as the growth temperature increases (within a range well below the bulk glass transition temperature, T_g, of the polymers). In response to the changing crystal structure, device performance degraded greatly with the increasing growth temperature. Such a trend was not observed on SiO_2, by comparison (**Figure 2-18, Figure 2-19**). The authors ascribe this to the chain mobility on the surface of the polymer dielectrics increasing with increasing temperature: with the mobility of dielectric polymer chains on the surface increased, the pentacene crystals deposited on the dielectric surface became less ordered, especially for the thin film phase, for which a low growth temperature was preferred [95-96]. In a following paper [97], they employed photo curable PVCN (with different degrees of curing) as a top layer dielectric to investigate the correlation between dielectric surface viscoelasticity, pentacene crystal morphology and transistor performance. According to the authors, clear correlations were found between the pentacene film deposition temperature, the degree of polymer dielectric film cross-linking, the mode of pentacene growth, the semiconductor phase composition, and the OTFT carrier field effective mobility. When the dielectric surface was more mobile (low cross-link density and high temperature), a poor pentacene crystal structure (low thin film phase content, small crystal size) was obtained. Thus device performance was poor.

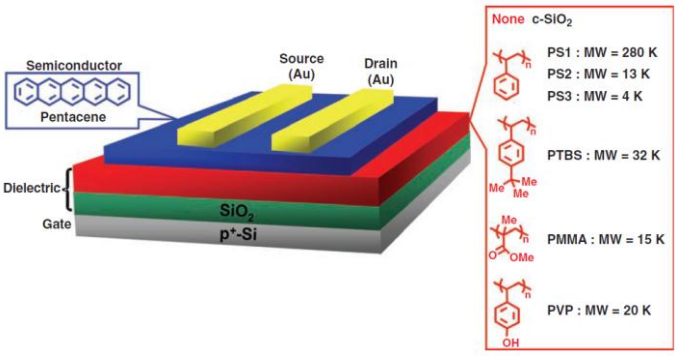


Figure 2-18 Schematic representation of the top contact, bottom-gate OTFT structure and the materials components used in this study [94] (Copyright (2007), The American Association for the Advancement of Science).

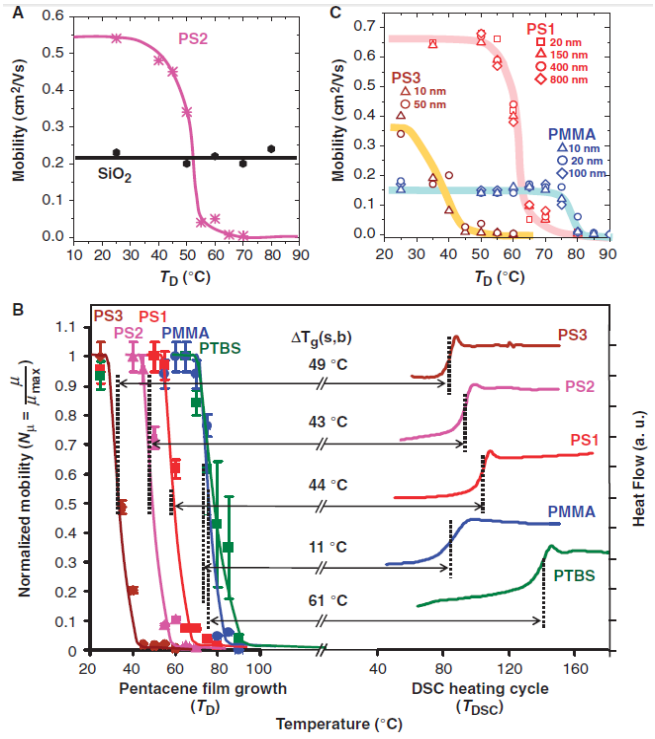


Figure 2-19 (A) Field-effect mobility μ for pentacene OTFTs fabricated at different deposition temperature T_D. (B) (Left) Normalized charge carrier mobility (μ= 0.68 (PS1); 0.54 (PS2); 0.34 (PS3); 0.18 (PMMA); and 0.63 (PTBS) at different T_D for pentacene OTFTs on various bilayer dielectrics. (Right) DSC scans for the polymers investigated. (C) Carrier field-effect mobility of pentacene TFTs as a function of T_D[94] (Copyright (2007), The American Association for the Advancement of Science).

According to most literature, pentacene grain size appears to be positively correlated

with device performance in terms of mobility [80, 93, 98-101]. For example, in Kim's study[94] a critical pentacene grain size were observed through which the carrier mobility of TFTs were well separated. (See **Figure 2-20**). With grain size higher than 0.8 μm, the mobility of devices were all greater than 0.1$cm^2 \cdot V^{-1} \cdot s^{-1}$, and vice versa.

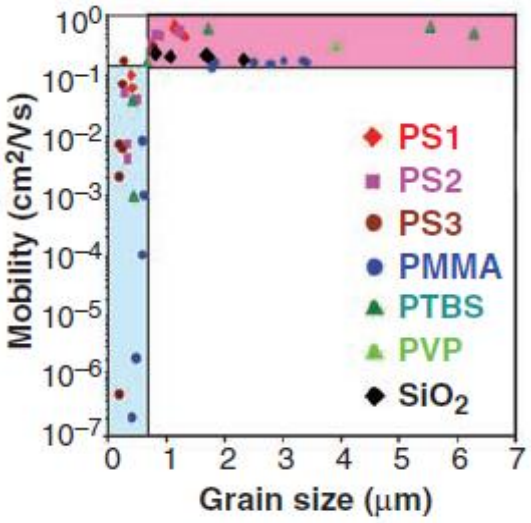


Figure 2-20 Mobility versus average grain size plot for pentacene TFTs. The blue- and red-shaded areas represent the low and high-carrier-mobility regions, respectively[94] (Copyright (2007), The American Association for the Advancement of Science).

This correlation between grain size and mobility is easy to accept because a large crystal size usually indicates a good pentacene insulator interaction thus giving good crystal order. However, conflicting observations were also reported. Shtein *et al.*[102] reported that SiO_2 treated with octadecyltrichlorosilane had smaller pentacene grain size compared with that of O_2 plasma treated SiO_2. The mobility of the former group was near 1.6 $cm^2 \cdot V^{-1} s^{-1}$ while that of the latter group was only 0.5 $cm^2 \cdot V^{-1} s^{-1}$. It was also reported that on a super hydrophobic surface very small grains were observed [103], while the corresponding device mobility was high. Both authors explained the results by suggesting that the coarse boundaries in large pentacene grains hindered charge carrier transport.

Lee *et al.*[104] reported that better interconnection of pentacene grains could be achieved by a two-step deposition with the first step at a slow rate and the second step at a high deposition rate. They proposed that the voids between the pentacene grains can be filled at the higher deposition rate. The AFM results showed smaller valley depths with the two-step deposition when compared with one step low speed deposition of the same film thickness. The mobility increase of 100-200% was achieved with the two-step deposition.

2.5.3.2 Dielectric Surface Chemistry

The surface chemistry of the dielectric layer is extremely important for both semiconductor growth and device performance.

Yoon *et al.*[105] designed a group of experiments in order to investigate the link between semiconductor-dielectric interfacial chemistry and field effect transistor characteristics. Combinations of various semiconductors and bilayer gate dielectrics consisting of SiO_2 layer as the main dielectric covered by various polymers (or HMDS) were examined in the experiment (see **Figure 2-21** and **Figure 2-22**). Based on the results, the authors pointed out that different dielectric chemistry induced large variations in the OTFTs performance especially for the air sensitive (generally high LUMO energy) n-type semiconductors, e.g. DFH-4T. Device performance of air-stable n-type and p-type semiconductors were affected by dielectric surface chemistry but to a much less an extent. They also proposed that the electron trapping due to silanol and carbonyl functional groups (see **Figure 2-22**) at the semiconductor/dielectric interface was the main origin for the sensitivity of mobility to different dielectric surfaces. They suggested that the thiophene-based n-type semiconductors exhibiting similar film morphologies and microstructures on various bilayer gate dielectrics provided a promising approach to investigate OTFT performance versus semiconductor/dielectric interface.

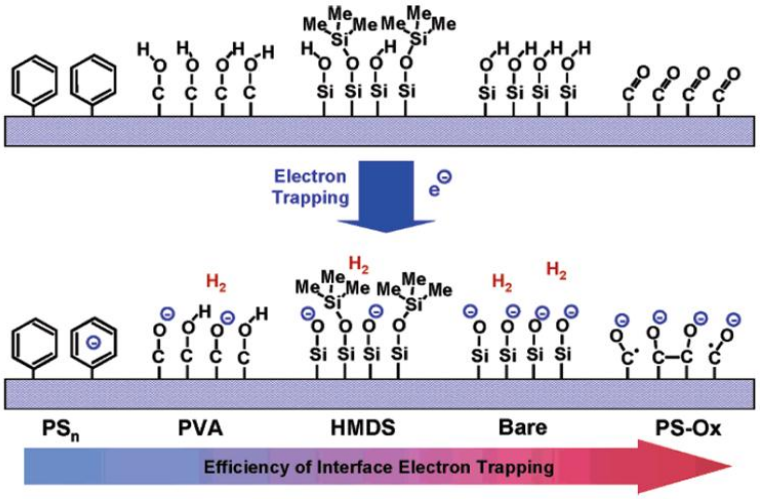


Figure 2-21 Schematic diagram of the variation in electron trapping efficiency with functional group on various bilayer dielectric surface[105] (Copyright (2006), American Chemical Society).

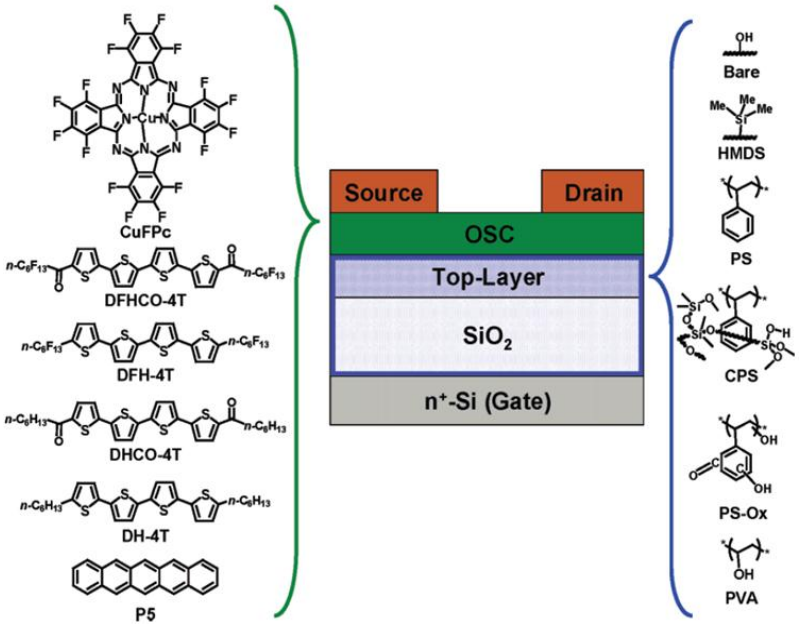


Figure 2-22 Chemical structure of the organic semiconductors (OSCs; left) and monolayers/polymers (right) employed in Yoon's study. The bottom gate OTFT device configuration is also shown (center)[105] (Copyright (2006), American Chemical Society).

Dielectric surface polarity was extensively studied by Veres *et al.*[87] as mentioned in **section 2.5.2**. The authors employed an amorphous semiconductor (PTAA), and thus excluded the effect of dielectric surface morphology on the semiconductor crystallinity,

to investigate the influence of dielectric surface polarity on the performance of transistors. The results showed that device performance was significantly increased by using the nonpolar low k dielectric, Cytop, compared with polar dielectrics including PMMA, PVA and polyhydroxlstyrene. They ascribed this fact to an increase of carrier localisation by the nearby polar sites on the dielectric surface. As illustrated in **Figure 2-23** (left), the DOS of the semiconductor was thought to be broadened by the polarity of the dielectric thus leading to more tail states which are responsible for carrier localisation. To support this theory, Richard *et al.*[82] developed a theoretical model that describes this DOS broadening effect by relating the broadening of a semiconductor's DOS with the distance of the semiconductor to a dipolar site. They also calculated the theoretical mobility of PTAA with the different dielectric materials that Veres used: the results fit with the experimental data obtained by Veres.

Another explanation for the correlation between the low k dielectric surface and high mobility is the absence of Fröhlich polarons at the interface of semiconductor and the dielectric layer[58]. The authors compare the field effect mobility of single crystal rubrene on various dielectric layers including, vacuum, parylene, SiO_2, Ta_2O_5 etc., and found that when the dielectric was polar enough a Fröhlich polaron presented at the interface, which could be responsible for the lower mobility observed on the more polar dielectrics.

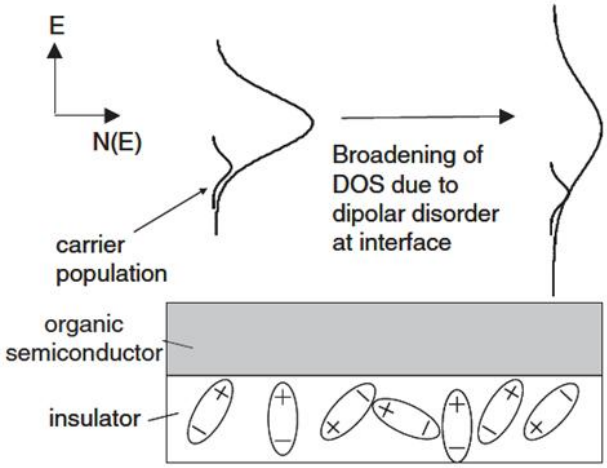


Figure 2-23 Suggested mechanism for the enhancement of carrier localisation due to poplar insulator interfaces[57]. (Copyright (2003), John Wiley and Sons)

2.5.3.3 Dielectric Surface Treatment

By surface engineering, the dielectric surface property can be improved to become more desirable for OTFTs. For example, it is very common in solution-based systems to use self-assembled monolayers (SAM) to modify a dielectric surface thus to cover undesirable chemical groups at the dielectric surface[80, 93, 106-108]; in addition, surface modification via O_2 plasma[100], UV/o-zone[101] and annealing etc. have been studied on diverse dielectric substrates for both organic and inorganic materials.

One simple but common surface treatment is spin coating of a polymer thin layer (a 'buffer') onto the main dielectric surface. Such surface coatings are usually able to 1). fill the pinhole, defects in the main dielectric [105]; 2). smooth dielectric surface; 3). screen unfavourable species on main dielectric, and thus provide a good substrate for semiconductors. One of the most popular buffer polymers perhaps is spin coated polystyrene (PS)[105 109]. PS is chemically and electrically inert, but at the same time it is easy to apply to various surfaces. Marked improvements in device performance in terms of field effect mobility, on/off ratio and hysteresis behaviour brought about by PS treatment have been reported[105, 109]. Cross linkable polymers have also been used as a

surface covering layer. Kim *et al.*[81] spin-coated a cross-linkable polyimide with n-octadecyl side chains onto a PVP dielectric layer: With the hydrophobic and low dielectric surface layer, the transistors showed better device performance, including saturated IV curves, better on/off ratio and higher mobility. However, even though spin coating is widely used in scientific experiments, it is difficult to apply in industrial processing.

UV/ozone surface treatment was frequently reported in recent papers[101, 103, 110-112]. In general, mild UV/ozone treatment tends to give a better dielectric surface[101, 110] for semiconductor growth. Liu[112] applied UV/ozone surface treatment for PVA/PS(top) bilayer dielectric. The results showed that the grain size of pentacene semiconductor grown on the dielectric was increased by the PS surface being treated by UV/ozone. The device mobility and on/off ratio was increased by a reasonable amount. However, with longer UV/ozone treatment time (longer than 10 minutes) the device performance decreased. The authors proposed that longer UV/ozone treatment brought chain damage and oxygen-containing polar groups into the PS layer while short time treatments provide a cleaner dielectric semiconductor interface. Similarly UV/ozone treatment for parylene-C dielectric[111] , which was more unstable in ozone compared with PS, resulted in a higher threshold voltage for transistors. This shift in threshold voltage was ascribed by the authors to the formation of polar groups during treatment. Oxygen plasma treatment of the dielectric surface was also reported to degrade the performance of TFTs[100] due to the formation of polar groups –OH, -CO-, -OCO-, and -COOH during treatment, while, mild CF_4 plasma (40W)[103] appeared to increase the hydrophobicity of dielectric surface and thus improved device performance to some extent.

SAM layers have been widely used in OTFTs, especially for inorganic dielectric surface treatment. There are many good reviews on the use of SAM layers[107-108], but being

generally unsuitable for vacuum deposition, SAM layers will not be discussed further here.

In general, solution-based buffer layers provide a significant improvement in carrier mobility for semiconductors. In contrast, radiation source treatments, including UV or plasma, showed less improvement in the dielectric surface in terms of transistors' performance. The deposition of additional layers or functionalization processes have not frequently been found in vacuum based processes.

2.6 Stability of Transistors

Device stability is an important issue for the application of transistors. The device stability can be affected significantly by the dielectric layer and its interface. In this section, the transistors' stability during both operation and storage is reviewed.

2.6.1 Hysteresis

Hysteresis is a difference in the source-drain current (I_{ds}) during forward and backward sweeps of the gate voltage (V_g). It represents the bias stress effect on a transistor. Although hysteresis could be used in non-volatile memory devices [113], for standard integrated circuits it should be avoided. Hysteresis can be classified into two types: higher back sweep current (HBSC) and lower back sweep current (LBSC) as shown in the figure below.

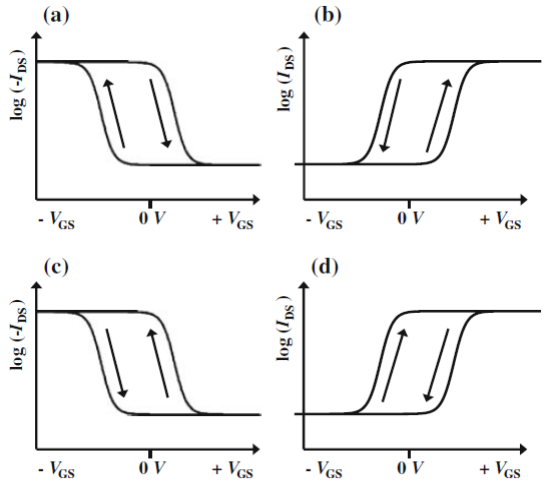


Figure 2-24 Schematic transfer curves (I_d versus V_g) of p-type (a, c) and n-type (b, d) OFETs. a) and b) show higher back sweep current (HBSC) hysteresis, c) and d) show lower back sweep current (LBSC) hysteresis[11] (Copyright (2009), Springer).

Although hysteresis can arise from the semiconductor or the dielectric, the dielectric layer is thought to be the major source[14, 21, 63, 109, 114-117]. This review focuses on hysteresis that is related with organic dielectric layer.

The most common type of hysteresis that arises from organic dielectric layers is the HBSC hysteresis. This type of hysteresis can be explained by three possible mechanisms. They are:

a). slow polarisation of the dielectric;

b). mobile ions in dielectric;

c). charge injected from the gate or channel.

Figure 2-25 illustrates the three mechanisms[11]. For the polarisation mechanism, when gate voltage is applied, polar groups in the polymer dielectric rearrange themselves gradually along the applied field. The reorientation of polar groups in the dielectric layer leads to a higher capacitance for the dielectric thus higher current is obtained at the back (on to off) sweep to the forward (off to on) sweep. The mobile ion mechanism is similar to the slow polarisation mechanism. Mobile ions rearrange themselves (drift) (as opposed to the polar groups in polarisation mechanism), thus altering the dielectric capacitance leading to higher back sweep current. It was reported that the mobile ion mechanism is highly temperature and sweep speed sensitive[118]. An increase in temperature or a decrease in sweep speed would increase hysteresis significantly, as these give ions energy and time to move. This could be used to identify the mobile ion mechanism. The third mechanism is related to charge injection from the gate to dielectric; the electrons injected during the switch-on process would lead to extra charge carriers accumulating at the channel, thus a higher current is observed during the back sweep than the forward sweep. Inserting a blocking layer between the gate electrode and dielectric could reduce such hysteresis [119] [12, 114-115].

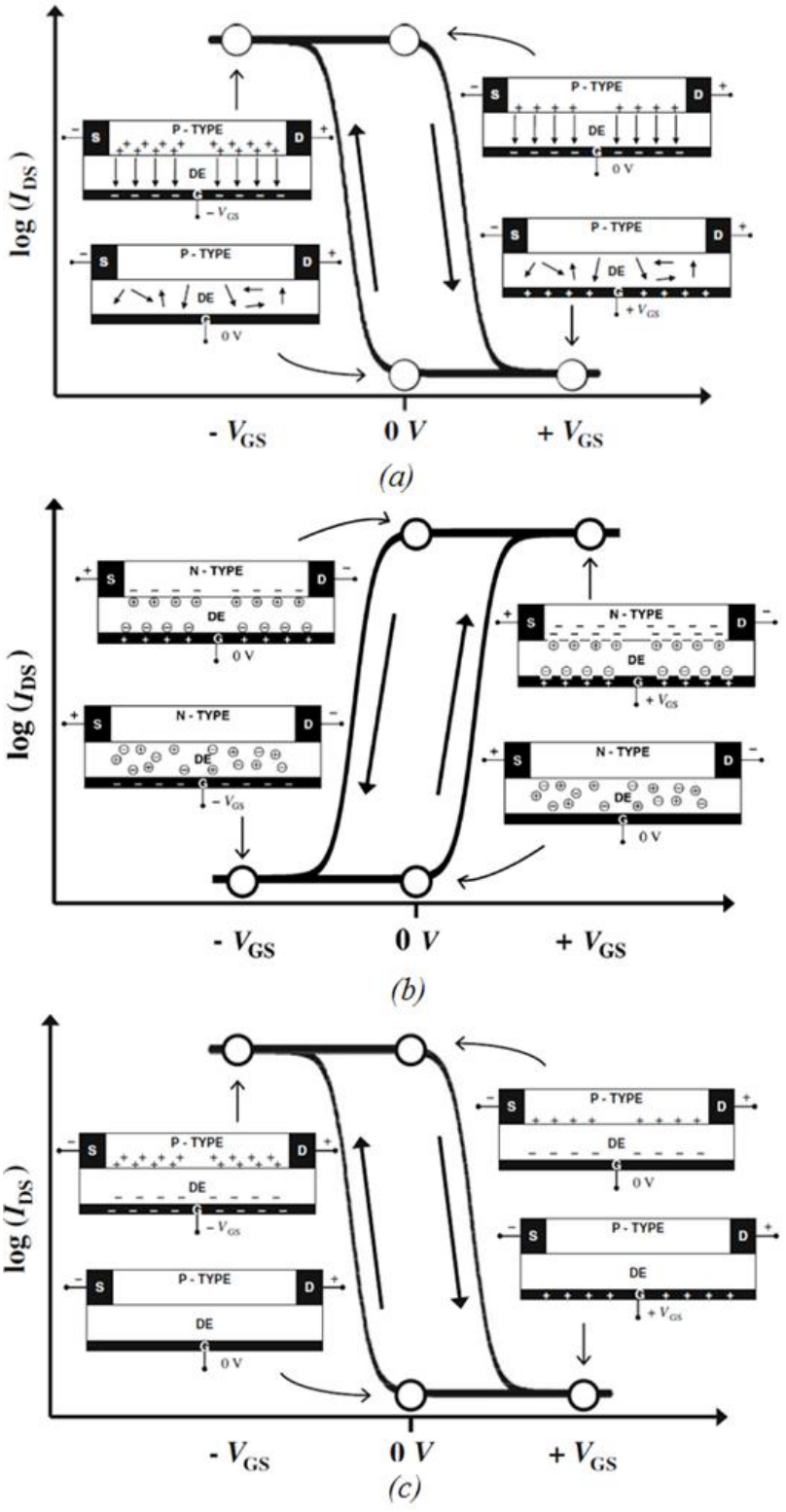


Figure 2-25 Illustration of three possible mechanisms of HBSC hysteresis, (a) slow polarisation; (b) mobile ions in dielectric; (c) charge injection from the gate [11](Copyright (2009), Springer).

Hwang *et al*. [116] investigated the hysteresis behaviour of devices with PVP dielectric layers cured for different times. The PVP cured at 175°C for 15 minutes, which was considered as insufficiently cured, showed the HBSC hysteresis. In comparison, the PVP cured for 1 hour showed almost no hysteresis at all. Such dependence of the hysteresis on the degree of curing was also found by other researchers[62-63]. Hwang proposed that the slow polarisation of uncured polar groups (e.g. –OH) in the polymer was the source of the hysteresis, although drifting of mobile ions in the polymer was not excluded as a possible cause for the hysteresis. To verify the dominant cause of hysteresis, Hwang investigated hysteresis behaviour of a SiO_2 and PVP bilayer system [115]. **Figure 2-26** shows the results of the experiments. On inserting a 200nm SiO_2 layer between the gate and the PVP dielectric, the charge injection from the gate was blocked; the author thus presumed that the slow polarisation mechanism was the dominant factor for the hysteresis in the bilayer system. They suggested that slow polarisation was likely the main source of hysteresis because slow polarisation–induced hysteresis is believed to be dependent on the number of dipolar groups (such as –OH) in the polymer layer. This idea is reinforced by the significant reduction of hysteresis with a thinner PVP (45nm) layer compared with 450nm PVP. In the same research, where an AlO_x oxide layer (which was thinner than the SiO_2) was also used as a blocking layer between the gate and PVP dielectric, hysteresis was clearly observed on the device even with PVP cured for 1 hour. Charge injection was considered as the main mechanism for the hysteresis in the AlOx case. Thus it is likely that the HBSC in the PVP was a combination of both polarisation and gate charge injection. However, the experiment still did not actually screen the possibility of mobile ions in the polymer, which is also thickness related.

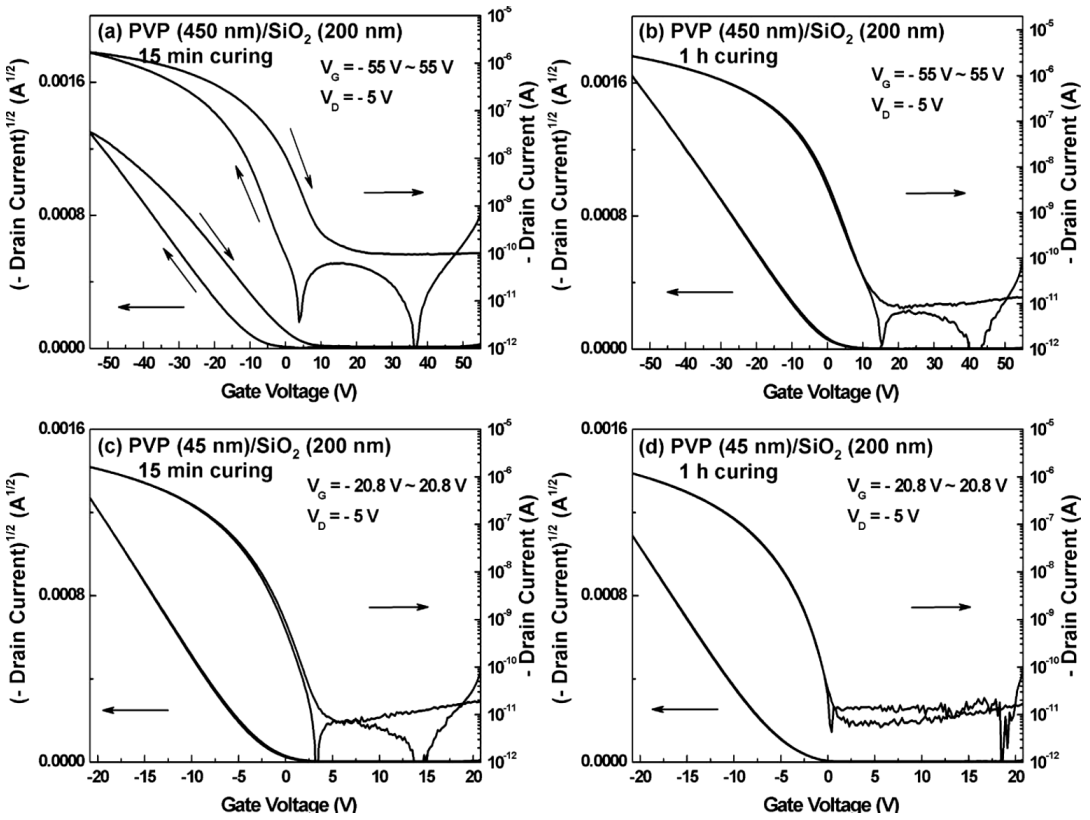


Figure 2-26 Transfer curves obtained under VD=−5 V (linear regime) from pentacene TFTs with PVP (450 nm)/SiO2(200 nm) bilayers prepared under two different PVP curing time conditions: (a) 15 min and (b) 1 h at 175 °C (vacuum). Similar plots obtained from TFTs with PVP (45 nm) /SiO_2 (200 nm) bilayers prepared with (c) 15 min and (d) 1 h curing[115] (Copyright (2008), AIP Publishing LLC).

Similar hysteresis behaviour was observed by Lee, *et al.*[21] in a PVA dielectric, while Lee presumed that the main mechanism of hysteresis was charge injection rather than polarisation or mobile ions. They believed that ions were not likely to move in the PVA in a sweep time as short as 1 min and polarisation of polymer should have a saturation point while no saturation was found in the experiment. In order to prove this view, Lee investigated the effect of inserting a SiO_2 layer with different thickness in between the metal gate and PVA dielectric layer [120]. By increasing the thickness of the inserted SiO_2 layer, the HBSC hysteresis of the device decreased and then reversed to LBSC when the SiO_2 layer reached a certain thickness. Based on the SiO_2 thickness-dependent hysteresis,

the author proposed again that the charge injection mechanism rather than the polarisation or mobile ions mechanism was the dominant factor for the hysteresis for the PVP dielectric, because otherwise the hysteresis should be independent with the presence of the SiO_2 layer as the polarisation or ion migration effect were only related with the polymer itself. The authors also proposed that the hysteresis behaviour of the PVA device was a result of balance between charge injection from the gate and from the channel. The hysteresis-free sample was at the point where the charge injection from gate and the channel counteract each other. A similar result was observed by Lee's group with a PVP dielectric [114].

Even though it is hard to find a common explanation for the origin of hysteresis in organic dielectrics, it is generally believed that insufficient curing, residual solvents, moisture from the air[14] and impurities in the raw resin[121] can all be sources for the HBSC hysteresis.

The lower back sweep current hysteresis is not as commonly observed in organic dielectric transistors as the HBSC hysteresis. Most LBSC reported in the literature was related with surface charge traps[122-124], for instance, when the SiO_2 dielectric surface encountered moisture, -OH groups may be formed and they act as hole traps thus leading to LBSC hysteresis[125]. Although some polymers e.g. PVP, may have similar charge traps, the majority of polymers are hydrophobic thus do not have the problem of charge traps at the channel. Some polymer and SAM molecules were even used as surface modification of an inorganic dielectric to prevent hysteresis [125].

2.6.2 Threshold Voltage Shift.

A shift in the threshold voltage can be classified into two types: operation-induced, and non-operation-induced shifts. The operation-induced threshold voltage shift usually has the same root as that of hysteresis, i.e. slow polarisation, mobile ions and injected

charges in dielectric layer that result from gate bias. The non-operational threshold voltage shift, as indicted by its name, can result from either environmental factors or from the built in factors of the transistors itself e.g. the dielectric surface polarity. In this section we focus on the threshold voltage shift that is associated with environmental effects e.g. moisture, oxygen and temperature.

Oxygen affects transistors by reacting with the semiconductor either chemically or physically[126-130]. Knipp[128] suggests that oxygen in the semiconductor, e.g. pentacene, induces acceptor-like traps, and therefore shifts the turn-on voltage towards a more positive potential. This accords with observations in other reports[131]. Accordingly, for pentacene devices, encapsulation is required to maintain a stable performance.

Light would shift a device's threshold voltage by the creation of photo-induced charge carriers, according to Wasapinyokul[132]. The OTFTs under illumination had positively shifted turn-on and threshold voltages. Dark measurement is required for device characterisation.

In general, environmentally-induced threshold voltage shifts are related to the semiconductor rather than the dielectric layers. Pentacene, the most frequently used organic semiconductor, has to be tested in the dark and the absence of oxygen to maintain stable performance.

2.6.3 Lifetime of Transistors

The lifetime of transistors is dependent on the semiconductor stability in the storage environment. Pentacene transistors showed a lifetime of less than a few months unless encapsulated[133-134]. This is due to the reactivity of pentacene in oxygen. In particular, oxidation reactions happen at the 6 and 13 carbon positions of the pentacene molecule[135-136]. By modifying the central carbon ring, either by substituting it, for example by a thienothiophene moiety[137], or by adding functional groups[136], the reactive

sites can be blocked, and the semiconductor could become more stable. Derivatives of pentacene e.g. dinaphtho-[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) showed stable performance for more than six months with relatively small loss in mobility with no encapsulation[138]. Similar devices also showed stability at elevated temperature up to 160ºC for medical sterilisation purposes[139].

2.7 Prospects

OFETs with mobility in the order of 1 $cm \cdot V^{-1} \cdot s^{-1}$, on and off ratio $\geq 10^5$ has been achieved by many groups using organic dielectrics in the lab.

However, to date, it is very difficult to find a cost fabrication process available for manufacturing reliable OTFTs with good mobility. One of the challenges is the dielectric layer deposition.

Polymeric materials have been used to fabricate dielectric layers because of their excellent processibility, good electrical properties and flexibility[140-143]. PVP and Cytop, showed the potential to provide reliable dielectric layer in large scale processes. However, problems associated with solution processing i.e. residual solvents, insufficient curing and the requirement for post treatment limited the performance of OTFTs and processing optimisation for fabrication.

Compared with traditional solution processing e.g. gravure printing, vacuum processing provides a contamination free process environment, solvent free deposition Therefore vacuum process could lead to large scale processing of dielectric layer for OTFTs.

2.8 References

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Chapter 3

Deposition of Gate Dielectric

3.1 Introduction

Polymer dielectric layers are desirable for flexible electronics due to their favourable processibility and their inherent mechanical flexibility. To deposit such a layer in a roll-to-roll environment, there are several aspects to be considered.

Firstly, the film deposition speed has to be fast enough to allow a high substrate speed so to keep process costs low for large area applications[1]. Secondly, the coverage of the film deposited has to be even so as to give a pinhole free film with constant thickness, and hence a constant areal capacitance, which is essential for electric circuits. Thirdly, the surface of the dielectric layer has to be smooth, especially in the bottom gate top contact configuration (see **Chapter 2, section 2.5.1**), so to provide a good surface for the following layers[2]. Furthermore, as a polymer has relatively weak intermolecular bonding, cross-linking is preferred (see **Chapter 2, section 2.5.2.1**) to improve its thermal-mechanical and electrical reliability[3]. To make a cross-linked polymer layer at high speed and at the same time to keep the damage to other layers to a minimum level has always been a challenge[4].

Flash evaporation[5-7] of liquid monomer followed by polymerisation of deposited monomer thin-film is a promising route to satisfy these criteria. This type of process involves flash evaporation of monomers at a temperature below both the decomposition temperature and the polymerisation temperature in vacuum, the monomer vapour then

condenses into a liquid film onto a moving substrate. The substrate, with its liquid film is transferred, at a maximum speed of hundreds meters per minute[5, 8], to a curing source where the liquid monomer is polymerised into a solid polymer film. Since the film is cured from a liquid on the substrate the surface roughness can be extremely low. By using multifunctional monomers, a cross-linked network is formed during polymerisation.

The most frequently used materials for the flash evaporation process are multifunctional acrylates or methyl acrylates[6] which polymerise and cross-link via free radical polymerisation. If the curing source is an electron beam (e-beam) or plasma, the free radicals for the polymerisation can be created directly by the curing source. If UV curing is applied, then an initiator is likely to be necessary. The other type of monomers are those polymerised by Lewis-acid and Bronstead-acid cationic polymerisation[9]. The cationic monomers cover a broader range of materials than the acrylates, but they need initiators to polymerise. Most initiators, however, tend to decompose and react with monomers below its evaporation temperature, hence this type of material is not as commonly used as the free radical polymerisers. This research focuses on the free radial polymerisation of acrylates.

Specifically, this work utilises a DC magnetron plasma source, an electron gun or a UV strobe to cure the deposited monomers of several chemical formulations, aiming to find an optimised system to make a dielectric layer a) with smallest thickness but free of pinholes, b) with high dielectric strength and c) at moderately high processing speed.

3.2 Experimental

3.2.1 Flash Evaporation and Capacitor Fabrication

The dielectric insulator layers were tested in a metal-insulator-metal capacitor configuration. The bottom electrodes of the capacitors were deposited by thermal evaporation of 50 nm Al onto 125 μm polyethylene naphthalate (PEN) substrates provided by DuPont Teijin Films or onto glass slides, through a shadow mask in an Edwards 306 thermal evaporator. The dielectric layer was deposited by flash evaporation (**Figure 3-1**) of acrylic monomers onto the pre-patterned substrates with the Al electrodes, followed by curing by plasma, electron beam or UV light. The liquid monomer was injected at a controlled rate of about 0.5 ml·min^{-1} by a syringe, into a hot tank heated to 250 °C where it was vaporised. The vapour passed through an evaporation nozzle which was also heated to 250 °C, then entered into the main coating chamber where it condensed into a thin liquid film onto the cool substrates attached to the rotating drum which then passed through the curing source. The drum rotated at a speed of 25 m·min^{-1} (5 m·min^{-1} in some cases) during deposition. For the experiments in this thesis, for ease of processing, the layers were not deposited in a roll-to-roll process, rather the substrate passed under the evaporation nozzle and curing sources sequentially for few times (~10). The monomer injection is restricted at very small amount to reduce the film thickness. Although single pass deposition and curing is preferred in the fabrication process for a high production rate, it requires the use of either a) very slow drum rotating speed for a web-free process to ensure the substrates pass the evaporation and curing source for exactly one time, or b) a roll-to-roll process which involves passing hundreds meters of plastic film from a web at high speed. The slow web-free approach is not representative for real roll-to-roll deposition condition, due to slow passing rate which could raise problems of de-wetting before curing. The roll-to-roll experiment is a good representative for the industrial process, but was not

practical for experimental investigation, due to significant material and time consumption. In contrast, the multi-pass process represents the roll-to-roll process in terms of substrate passing rate and curing duration during each pass. It is a good way to reveal the characters of monomer formula in terms of processing and electric properties and the efficiency of different curing methods. It may exaggerate the pin-hole free effect due to filling up the pinholes by additional passes, but, after all, a multiple pass process could be done in real roll-to-roll process, if necessary, by simply repeating the deposition process or by adding additional evaporation and curing sources alongside the film path

To describe the overall deposition speed regardless of the various deposition times, number of substrate passes, and drum speed in different runs, the yielding speed v (nm·m·min^{-1}) is exploited to give a universal measure of film deposition rate

$$v = \frac{T \times C}{t} \tag{15}$$

where T is total thickness of deposited film, C is the circumference of the drum which is 1.8 m, and t is total monomer delivery time.

The v is a measure of the amount of material that is attached to the substrate at a unit substrate rate in a single pass, given the deposition efficiency is assumed to be independent to the drum rotating speed. The total deposition time, total monomer injection and deposition speed for each run is presented in **Table 3-1, page 82**. Capacitor fabrication was finished by thermal evaporation of a 50 nm gold layer on top of the dielectric layer through a shadow mask in an Edwards 306 thermal evaporator.

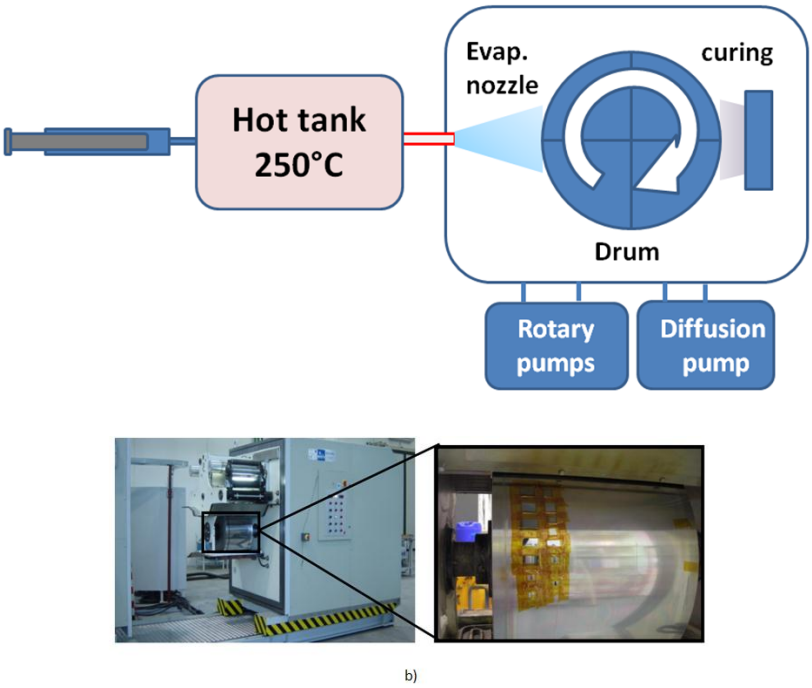


Figure 3-1 a) Schematic of flash evaporation of liquid monomer and curing in a vacuum web coater; b) Oxford vacuum web coater substrate drum, with a variety of substrates attached with polyimide tape.

3.2.2 Materials

The molecular structure of the acrylic monomers used in the experiment is shown in **Figure 3-2**. The details of each formula are as follows:

- Tri(propylene glycol) diacrylate (TPGDA)

TPGDA 90% mixture with isomers was purchased from Sigma Aldrich. In the plasma or e-beam curing process the TPGDA was directly injected into the hot tank for flash evaporation. In the UV curing process, TPGDA was firstly mixed thoroughly with a photo-initiator: 4,4'-bis(N,N-dimethylamino)-benzophenone, i.e. Michler's Ketone (Sigma Aldrich) at a concentration of 5 vol% two hours prior to deposition.

- 1,6-Hexanediol diacrylate (HDDA)

HDDA 80% mixture with isomers was purchased from Sigma Aldrich. It was used directly in the deposition with no pre-treatment.

- 1,6-Hexanediol dimethacrylate (HDDMA)

HDDMA (containing 100 ppm hydroquinone inhibitor) was purchased from Sigma Aldrich. A part of the monomer was filtered through a photo-initiator remover tube (purchased from Sigma Aldrich) twice prior to flash evaporation. Both filtered and un-filtered HDDMA were used in deposition process.

- Scott Bader PD10374

PD10374 is a acrylate functionalised branched macro-monomer dissolved in 30 % vinyl toluene (w/w) provided by Scott Bader Ltd The material was diluted with an equal volume of vinyl toluene (from Scott Bader Ltd.) to reduce its viscosity. This material is a commercial formulation, so its structure is not disclosed.

- Mixture of acrylates

Pentaerythritol tetraacrylate (PTTA) purchased from Sigma Aldrich, was mixed with HDDA at 1:9, i.e. 10 vol%; and was mixed with TPGDA at 3:7 i.e. 30vol%.

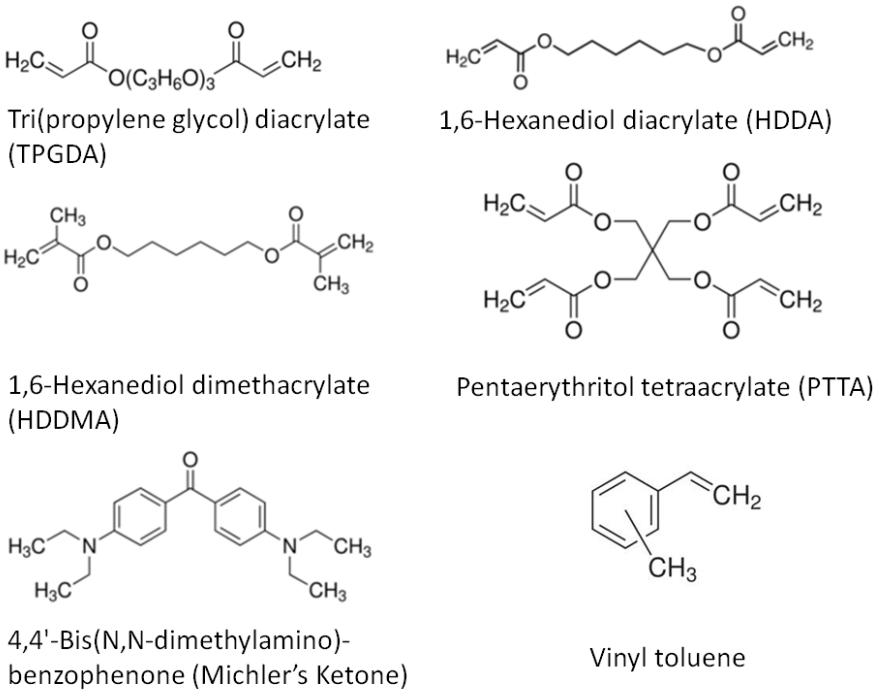


Figure 3-2 Molecular structure of monomers, photo-initiator and solvent used in depositions.

3.2.3 Curing Source

- Plasma curing

DC plasma from a passivated magnetron sputtering source was used to cure deposited monomer film. The passivation was done by oxidation of the surface of the aluminium sputtering target. The oxidised surface coating therefore prevents the aluminium from being sputtered from the source at the powers used. **Figure 3-3** shows the general mechanism of a DC magnetron sputtering plasma: a negatively charged cathode is placed in a low pressure inert gas atmosphere in which a plasma is struck by the electric field and contained by a magnetic field by the magnets behind the cathode. Positively charged inert gas ions in the plasma are accelerated toward the cathode by the applied electric field. The accelerated gas ions bombard the cathode surface and sputter secondary electrons out from the surface into the low pressure inert gas atmosphere. The electrons in the plasma follow a helical path within the inert gas due to the applied magnetic field,

ionising more inert gas atoms which will then be attracted to the cathode, and so the bombardment continues. In this case, the sputtering of atoms from the target is minimised by the surface passivation of the target and by keeping the target current low (less than 8 A), hence any incorporation of target atoms into the sample was minimised. UV light and heat are also generated in this process.

In this experiment, a plasma was struck when the pressure of the chamber reached 1×10^{-4} mbar or lower. 200 sccm Ar was introduced into the chamber, raising the chamber pressure to of 3×10^{-4} mbar, to make a low pressure Ar atmosphere, then the plasma was initiated by switching on the main power supply. The current control was set at 6 A. Before applying a monomer film under the plasma, the sputtering target i.e. cathode surface was firstly oxidized/passivated to prevent aluminium sputtering. This was done by introducing high dose of oxygen of 40 sccm, along with the Ar, into the plasma for half an hour. The oxygen dose was then reduced to 10 sccm to make sure the target was always oxidized during ion bombardment. This could be confirmed by the relatively high target voltage associated with a fully 'poisoned' target. Once the target had been passivated, this passivation process was not repeated until the target was used in other purposes e.g. sputtering. A fully oxidized Al target gave a stable plasma at 200 V with 6 A controlled DC input at 200 sccm Ar and 10 sccm oxygen at $3\cdot10^{-4}$-$4\cdot10^{-4}$ mbar. To test whether the passivation was effective, XPS analysis had been done on plasma treated dielectric surface (see **Chapter 5, section 5.3.3**): no Al signal was detected from the plasma treated polymer surface.

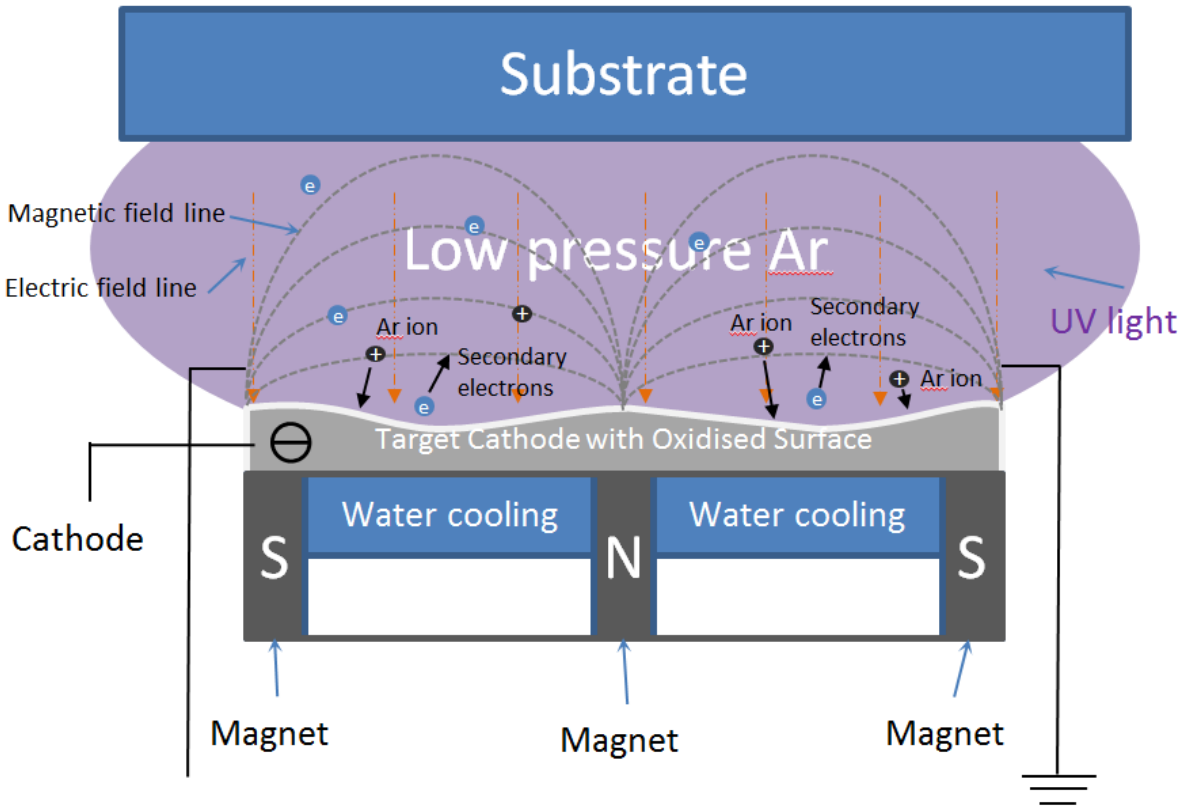


Figure 3-3 Schematic illustration of a DC magnetron sputtering plasma.

- Electron Beam

The electron beam was formed by a diode-sputter-cathode which was mounted in an earthed metal box with a slit of about 4 mm width and 400 mm long directly facing the cathode[10] (**Figure 3-4**). The electron gun operates at between -2 to -5 kV. In a low pressure inert gas atmosphere, the high voltage on the cathode strikes a plasma which contains abundant electrons. These electrons are accelerated by the cathode and exit the box through the slot, forming an electron beam. In our experiment, the e-beam was initiated by introducing 180 sccm Ar into the metal box at vacuum level of about 1×10^{-4} mbar and then gradually increasing the voltage input control to 2.6 kV. This voltage input generates 175 mA current in the electron gun. The actual e-beam output was, however, much smaller. This current was measured using a setup shown in **Figure 3-4**. An aluminium foil was located in front of the slit, covering the projection area of the e-

beam. This foil was linked to a current measuring unit, then to the earth so that the output electrons can be collected by the foil and measured by a current meter. The measured current from the foil to earth was 2 mA. This is considered as the actual beam current that is able to hit the substrate. The energy of the electrons in the beam should be of 2.6 k eV or lower.

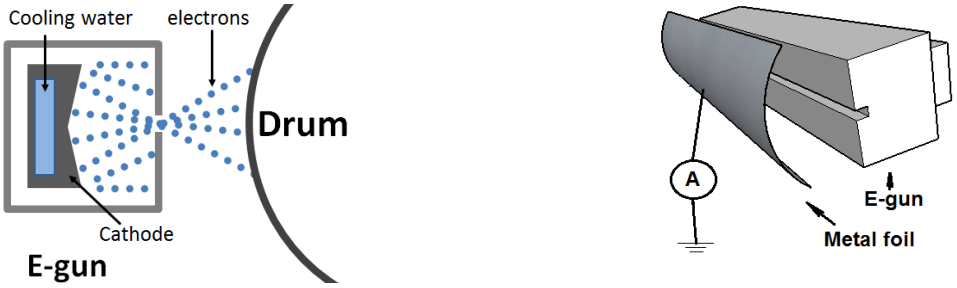


Figure 3-4 Schematic illustration of electron gun and e-beam current measurement setup.

- UV strobe

A xenon UV strobe modified from an Equinox Wildzap 1500 W disco light was used as a UV source. The lamp was reassembled to allow the UV bulb to be located inside the vacuum chamber while the power circuit was kept outside the vacuum chamber to prevent overheating and arcing during operation (**Figure 3-5**).

This UV strobe gave a typical xenon lamp radiation output ranging from about 200 nm to 1000 nm, however, the low wavelength radiation was blocked by the fused glass tube, hence the actual output spectrum of the UV light was from wavelengths greater than 350 nm, as confirmed using an Ocean Optics USC+2000 spectrometer.

A post-curing step was applied for all the UV-cured samples to improve cross linking: the cured samples passed the UV strobe three extra times at drum speed of 1 $m \cdot min^{-1}$.

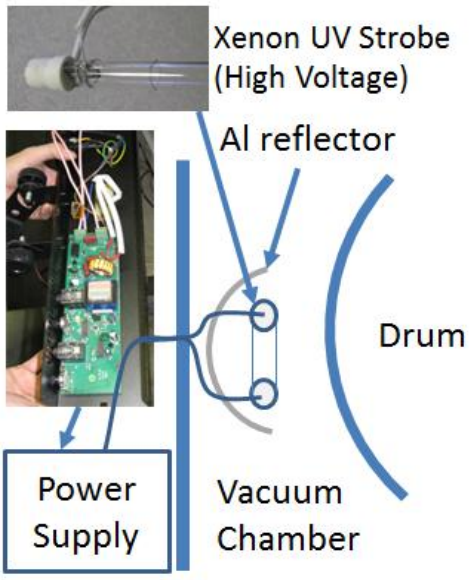


Figure 3-5 Schematic of UV strobe curing source

3.2.4 Characterisation

- Film thickness

The thicknesses of the dielectric films on glass or PEN were measured by a Veeco Dektak 6M Stylus Profiler, taking an average from at least three readings.

- Impedance spectroscopy

Capacitors were measured by impedance spectroscopy using a Solartron SI 1260 impedance analyser. Each sweep was conducted at conditions of 1 V AC bias and 0 V DC bias; from 1 MHz to 100 Hz at 25 points per decade and 100 cycles per point. Unit area capacitance C_i was calculated from the measured capacitance divided by area by which the electrodes overlap, which is 0.0625 cm^2.

- Leakage current test

Capacitor leakage was measured by applying a sweeping voltage applied to the capacitor from 0 V to up to 80 V (depending on device capability) with each step less than 0.5 V by a source measuring unit (Keithley 2400). The holding time for each current reading was

1000 ms. The break-down strength is defined as the electric field applied to a capacitor at which the stabilised leakage current passed $1 \cdot 10^{-7}$ A·cm^{-2}.

- IR spectrum

A Varian Excalibur Fourier-Transform Infrared (FTIR) spectrometer with attenuated total reflectance (ATR) instrument was used to characterise the curing condition of the acrylates. The samples were obtained by scratching material from a glass substrate.

3.3 Results and discussion

3.3.1 TPGDA

The TPGDA (**Figure 3-2**, **page 69**) cured by plasma or e-beam, and the TPGDA mixed with Michler's Ketone cured by UV all solidified on curing, but the TPGDA without photoinitiator did not solidify on exposure to UV. The plasma and e-beam cured TPGDA and UV cured TPGDA with Michler's Ketone had thickness of 430, 650, and 770 nm respectively (**Table 3-1**). The TPGDA without photoinitiator exposed to UV showed liquid like film after curing treatment, as radiation of wavelength greater than 350 nm does not directly lead to cross-linking. The plasma and e-beam cured films were colourless. The UV cured TPGDA+Michler's ketone showed very light yellow colour indicating that the photo-initiator was evaporated and deposited onto the substrate along with the TPGDA. All the films were highly transparent to eyes and showed a homogenous interference colour indicating the surface was smooth, and film thickness was generally even. The RMS of such flash evaporated TPGDA film can be as low as ~0.1nm[12] over an area of 2 μm by 2 μm. plasma cured samples had a capacitor yield of 100 % i.e. 8 out of 8 capacitors worked. The TPGDA film cured by e-beam and UV in contrast, had yield of 88% and 75% respectively despite their greater thickness compared with the plasma cured samples. The remaining 12% and 25% of devices short circuited, probably due to defects e.g. pinholes or areas of poorly cured material.

The 430nm plasma cured TPGDA showed unit area capacitance of 10.1 nF·cm^{-2} at 10 kHz (**Figure 3-6**) which is approximately the frequency at which the organic electronics circuits are expected to work. The frequency dependence of the film was within 20% over the frequency range from 1 MHz to 100 Hz. The capacitors generally sustained at least 1.3 MV·cm^{-1} before a significant increase of leakage current, i.e. reaching above $1 \cdot 10^{-6}$ A·cm^{-2}, occurred. This leakage value and break-down strength is comparable to

the equally thick solution-processed PVP film which required at least 20 minutes curing time in elevated temperature[3].

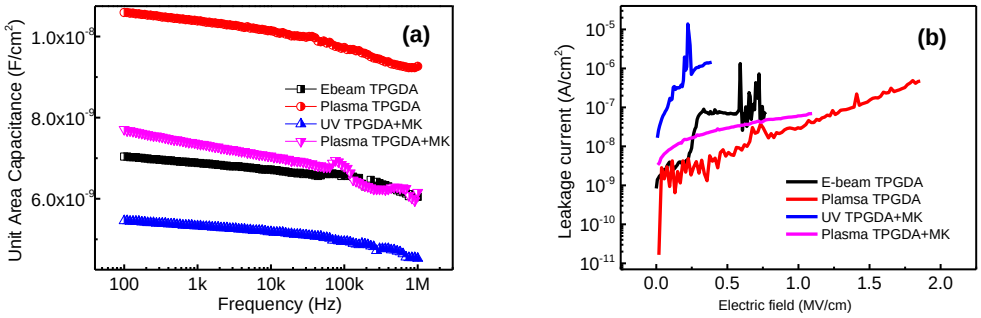


Figure 3-6 Areal capacitance a) and leakage current b) of TPGDA dielectric film cured by e-beam, plasma; UV and plasma cured TPGDA with Michler's Ketone 5 vol%.

The e-beam and UV cured samples showed 6.7 nF·cm^{-2} and 5.2 nF·cm^{-2} areal capacitance respectively. Their insulating property is less good than the plasma-cured TPGDA. The 650 nm e-beam cured film became very leaky by about 0.3 MV·cm^{-1}. The 770 nm UV cured sample showed even higher leakage and only sustained about 0.2 MV·cm^{-1} before significant arcing and break-down.

This high leakage of e-beam and UV cured samples was most likely due to insufficient curing of the monomers. From the IR spectrum we can estimate the double bond conversion rate i.e. the more intense the absorption peaks due to residual double bonds, the lower the curing degree for acrylates[11]. The IR spectra (**Figure 3-7**) of the three films show that the plasma cured samples had the lowest concentration of residual carbon double bonds, e.g. the peak at 810 cm^{-1} was least intense, while the UV cured samples had the highest. The lack of curing was further proved by annealing, which can be used to give a more thorough curing for acrylates: the e-beam cured samples annealed in vacuum for 1 hour at 150 °C showed a much lower leakage current after annealing[12]. By

contrast, the plasma cured sample showed no improvement after the same heat treatment. There was no opportunity to apply the annealing to the UV cured films, due to break-down of the lamp after several runs. An additional experiment, however, was conducted to cure the TPGDA+Michler's Ketone mixture properly. This was achieved by plasma curing a 730 nm film of the mixture. The leakage current of the capacitors (**Figure 3-6**) was as small as that of TPGDA cured by plasma, i.e. the material was well cured. This indicated that the TPGDA+Michler's Ketone mixture was curable as long as an effective radiation source is applied. The UV lamp, in contrast to the plasma, was not effective, probably due to the poor absorption of the UV light (mainly 350 nm and above) by the sub-micron transparent film, even with addition of 10 % photo-initiator. In contrast, the plasma radiation contains mainly ions and electrons as well as UV which could be absorbed regardless of the transparency and the thickness of the deposited film. Therefore even though the UV had a higher total energy output compared with the plasma, the curing effect is still much poorer.

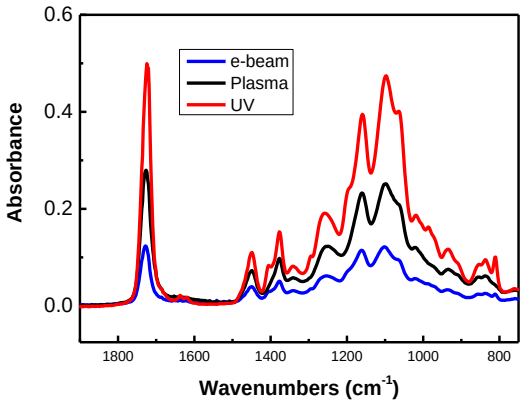


Figure 3-7 IR spectrum of e-beam, plasma cured TPGDA and UV cured TPGDA with Michler's Ketone of 5 wt%.

The small current from the e-beam gun was the most likely reason for the difference in behaviour between the plasma and e-beam. As shown in **section 3.2.3** , the e-beam had

an output of only 2 mA while the plasma had 6 A, though of course this current did not all end up on the substrate in both cases.

3.3.2 HDDA and HDDMA

The HDDA (**Table 3-1**) had a lower deposition rate (~400 nm·m·min^{-1}) compared with TPGDA, probably due to its lower boiling point, i.e. it is more difficult for it to condense on the substrate. The HDDA sample, 300 nm thick on PEN, had 100 % yield of capacitors. The capacitors had unit area capacitance of 14.1 nF·cm-^{2} at 10 kHz and less than 10% frequency dependence which were both much lower compared with the TPGDA samples (**Figure 3-8**). This was probably due to TPGDA's higher content of oxygen in the molecule, as the local molecular polarity is responsible for slow polarisation of the polymer in the low frequency range. The 300 nm HDDA film showed a leakage of less than 10^{-7} A·cm^{-2} at an electric field of 1.2 MV·cm^{-1} or below, similar to the TPGDA film cured by plasma.

In order to improve the cross-linking further, the HDDA was mixed with 10 vol% of poly functional acrylate PTTA. This mixture showed a similar deposition rate compared with HDDA. The insulating property, however, was slightly worse: low leakage current only up to 1 MV·cm^{-1} (compared with 1.2 MV·cm^{-1} for HDDA), and only 88% yield of capacitors. The areal capacitance value was 14.9 nF·cm^{-2} for the 250 nm film. A similar mixture of TPGDA and 30% PTTA was also tested but instead of improvement, the break-down field was decreased to 0.4 MV·cm^{-2} (**Table 3-1**).

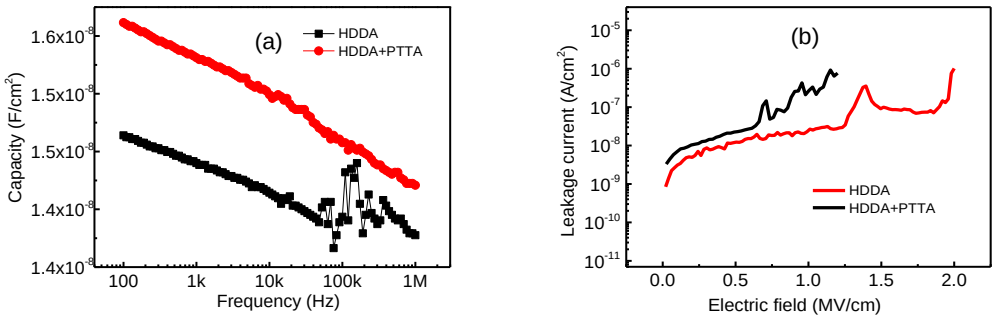


Figure 3-8 Areal capacitance a) and leakage current b) of dielectric film made from plasma cured HDDA and HDDA with 10% PTTA.

The other similar acrylate: HDDMA, with/without inhibitors, resulted in no deposition, despite its similar boiling point and molecular structure to HDDA. Perhaps the methyl group increased the reactivity of the polymer dramatically such that the monomer cross-linked inside the hot tank before being evaporated.

3.3.3 Scott Bader PD10374

A poly-functional acrylic resin was provided by Scott Bader Ltd. This resin had very high viscosity, preventing it from being delivered to the heated tank, and hence required dilution before use (**section 3.2.2**). The deposition speed of this resin was 180 nm·m·min^{-1}, which was much slower than the TPGDA, given that the monomers' volume delivery rate was similar. This was partly because of the dilution, but also, more significantly, due to its higher boiling point, which inhibit it from being evaporated. Residual material was found in the heat tank after evaporation, proving that only a portion of the monomers was evaporated, even when the tank reached 300°C during evaporation. Since the deposition rate was much slower, the drum speed was reduced to 5 m·min^{-1} accordingly. The film gave a yield of 100 % working capacitors with an areal capacitance of about 41 nF·cm^{-2} which is competitive among polymeric dielectric film in publications. The film showed low leakage at electric fields lower than 1.8 MV·cm^{-1} (**Figure 3-9**). The loss angle of the PD10374, TPGDA and HDDA are close to -90 degree

at low frequency, indicated a low dissipation factor for all the three materials at around 1KHz. The high loss at high frequency was probably due to serial resistance.

It is very interesting that the PD10374 was able to give such a high yield of capacitors in such low thickness with low leakage. This will enable the transistors to be switched on/off within a low voltage range, which could not only extend the scope of OTFTs application but also lower the power consumption of the device. However, the formulation of PD10374 is protected from disclosing, it is therefore difficult to investigate it further in this project.

The TPGDA and HDDA materials, in comparison, showed leakage through the insulator in a significant proportion of samples when the film thickness was lower than 300 nm. One possible explanation is that the PD10374 may give better coverage of the substrate thanks its high viscosity: viscous liquids have no time to de-wet on the substrate, so there is less possibility to form pinholes. The other possible reason is that the curing time per unit thickness of the films was higher in PD10374 than the others. Longer curing time might give more thorough curing, however, increasing the post-curing time (post-deposition plasma treatment) for a group of plasma-cured TPGDA samples of 250 nm thickness showed neither higher yield nor better insulating properties. A final, likely, reason is the fundamentally different formulation of PD10374 compared to the TPGDA or HDDA, perhaps the higher molecular weight, indicated by its viscosity, of the monomers in the PD10374 can lead to better entangled/cross linked molecular network in the cured materials. This highly cross linked/entangled film could give better insulating properties (see **Chapter 2, section 2.5.2.1**).

The dielectric constant of the dielectric layer is not affected significantly by their formula variation and was between 4-6 (**Table 3-1**).

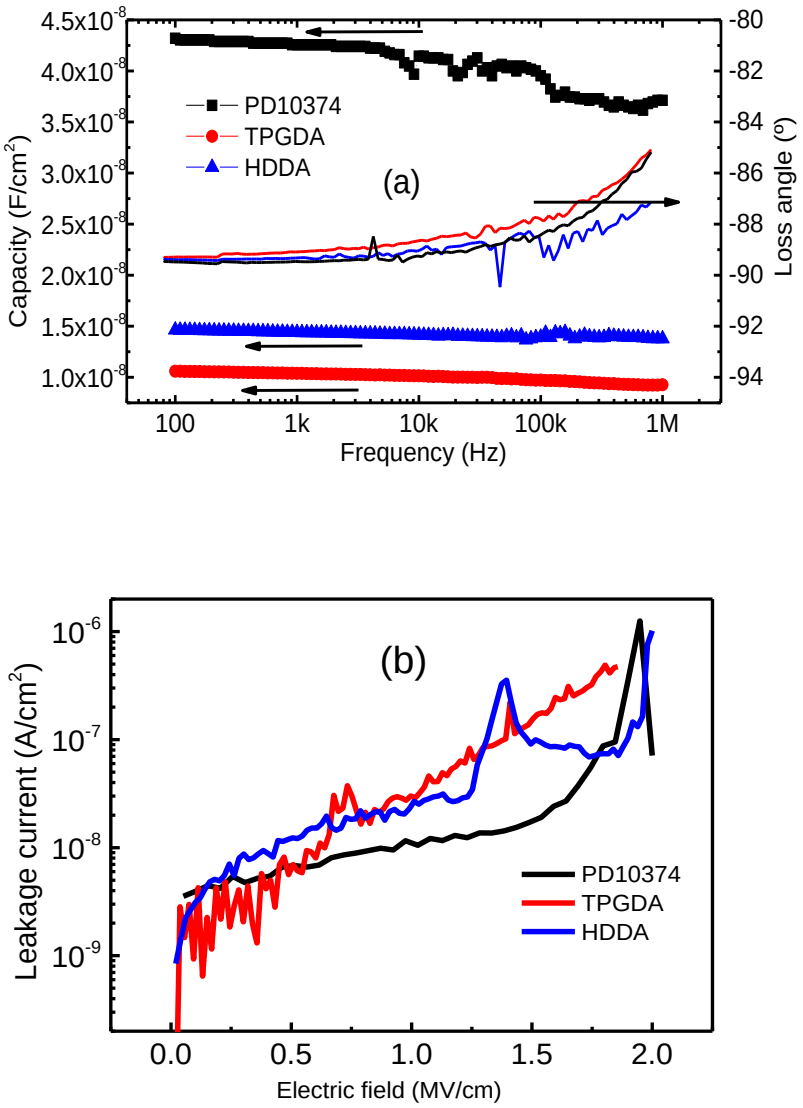


Figure 3-9 Areal capacitance, loss angle versus frequency a) and leakage current b) of dielectric film made from plasma cured PD10374 TPGDA and HDDA.

Table 3-1 Deposition parameters and film characters of acrylic thin films deposited by flash evaporation process.

Monomer	Drum speed ($m \cdot min^{-1}$)	Approx. Total inject.(ml)	Injection speed ($ml \cdot min^{-1}$)	Thickness (nm)	Deposition speed ($nm \cdot m \cdot min^{-1}$)	Curing method	Yield	*Ci* at 10kHz ($nF \cdot cm^{-2}$)	*k* at 10kHz	Break-down Strength ($MV \cdot cm^{-1}$)	Break-down Voltage (V)
TPGDA	25	0.5	0.5	430(PEN)	774	plasma	100%	10.1	4.7	1.4	60
TPGDA	25	0.9	0.5	650(PEN)	650	e-beam	87.5%	6.7	4.7	0.4	20
TPGDA	25	0.5	0.5	N/A	N/A	UV	0	N/A	N/A	N/A	N/A
TPGDA+MK5%	25	0.9	0.5	770(Glass)	770	UV	75%	5.2	4.3	0.08	6
TPGDA+MK5%	25	0.8	0.5	730(Glass)	822	plasma	100%	7.1	5.6	>1	>80
HDDA	25	1	0.8	300(PEN)	432	plasma	100%	14.1	4.6	1.3	40
HDDA+PTTA(10vol%)	25	1	0.8	250(PEN)	360	plasma	87.5%	14.9	4.1	0.9	22
TPGDA+PTTA(30vol%)	25	0.6	0.5	580(PEN)	870	plasma	100%	9.2	5.8	0.4	23
HDDMA	25	3	0.8	No film	0	plasma	N/A	N/A	N/A	N/A	N/A
PD10374	5	0.5	0.5	<100(PEN)	180	plasma	100%	41.4	~4.5	>1.8	18

3.4 Summary

TPGDA, HDDA and PD10374 were deposited and cured in a multiple pass process to form pinhole-free dielectric layers with 100 % capacitor yield. The plasma source provided better curing than the e-beam and UV sources. In addition, PD10374 resin cured by plasma showed high yield of capacitors with one third the thickness (<100 nm) compared with the other acrylates, and thus gave a three times greater dielectric areal capacitance. Finally, the addition of poly-functional acrylates did not improve the dielectric property of the TPGDA and HDDA. The HDDA film showed slightly better insulating property than that of TPGDA and lower level of frequency dependence for dielectric constant, possibility due to its lower oxygen content in the molecular structure.

3.5 References

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Chapter 4

Dielectric Surface Modification

4.1 Introduction

A polymer dielectric layer is a key component for flexible organic thin-film transistors (OTFTs). Linear polymers e.g. polystyrene (PS) may be used as a low k dielectric layer[1]. However, such materials, deposited as polymers, either from solution or by thermal evaporation, may have high gate leakage due to, for example, pinhole defects. In order to make reliable transistors, it is necessary to constrain the dielectric polymer chains by cross-linking[2]. This involves using polymers with reactive sites such as acid anhydride,[2] cinnamate[3-4], silane[5], epoxy or acrylate[6] groups that can cross-link during deposition, or with a cross-linking agent *in-situ*. These chemical groups react under certain conditions, e.g. heat or radiation, to form covalent bonds between the polymer chains to yield a dielectric layer with better mechanical and electrical reliability.

Use of these cross-linkable materials, however, inevitably leaves such polar cross-link sites, such as ester groups, on the surface. Surface polar groups are believed to affect the growth of subsequently deposited organic semiconductors[7] and are undesirable for achieving high carrier mobility in OTFTs[1]. Accordingly, there is a tradeoff between the desirability of a non-polar surface, and the processibility as well as reliability of the bulk of the dielectric layer, which requires polar groups to form the cross-linking network.

The work in this chapter demonstrates that cross-linked, flash-evaporated TPGDA is an effective dielectric layer for organic thin-film transistors, and more importantly it presents the results of a systematic investigation (a) to understand the role of surface chemistry of the acrylic polymer on transistor performance and (b) to identify the characteristics of a suitable surface buffer layer for cross-linked TPGDA that will enhance its surface properties while maintaining its excellent bulk properties. In particular, this work investigates the effect of surface ester group concentration on OTFT performance by examining a range of thin, spin-coated, surface buffer layers of polymers with different ratios of ester group to alkyl carbon atoms, i.e. polar to non-polar ratio, in their molecular structure.

4.2 Experimental

4.2.1 Device Fabrication

Bottom gate top contact transistors (**Figure 4-1**) were fabricated. The cross-linked TPGDA dielectric layer, ~450 nm thick, was deposited by flash evaporation onto glass slides with pre-patterned gold gate contacts, and cured by plasma[24,27,28] following the process described in the previous chapter (**Chapter 3, section 3.2.1**). In some samples the TPGDA surface was then modified by the addition of a 20-40 nm thick polymer buffer layer (**Figure 4-2**).

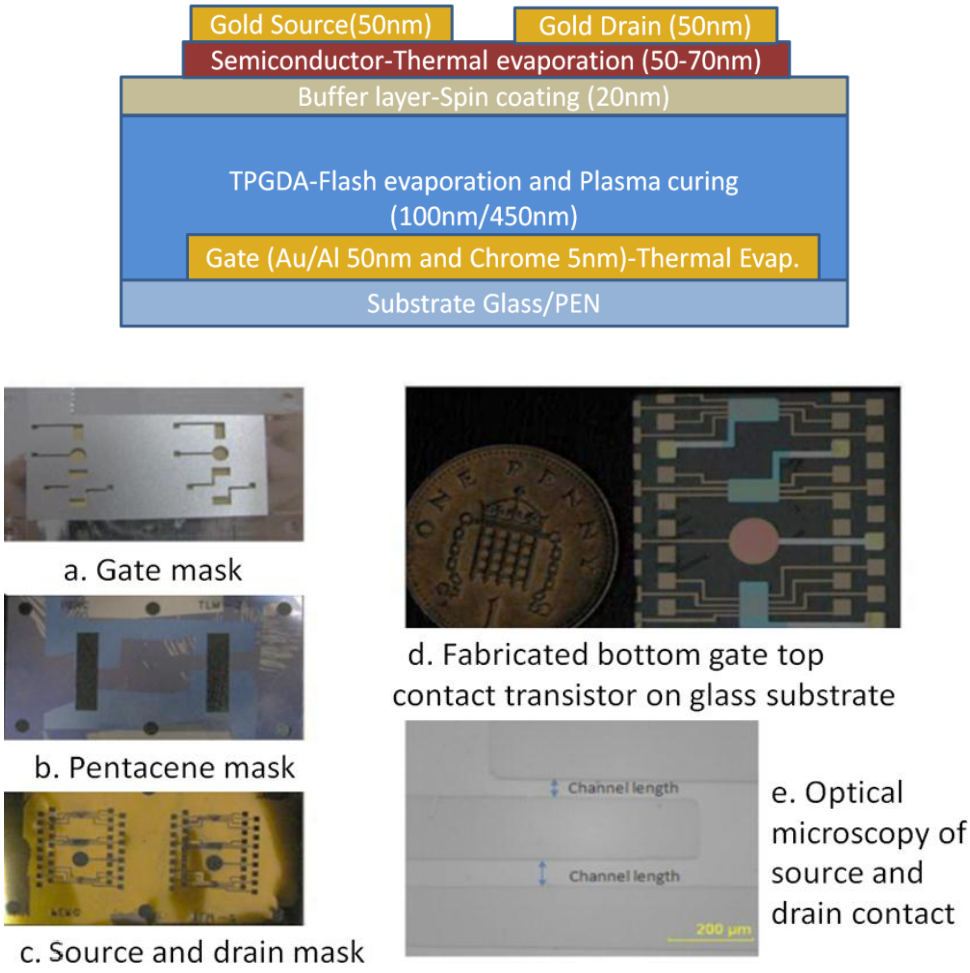


Figure 4-1 (Top) Schematic representation of the cross-section through a bottom-gate top-contact OTFT indicating the approximate thickness of key layers; (Bottom) masks for different layers.

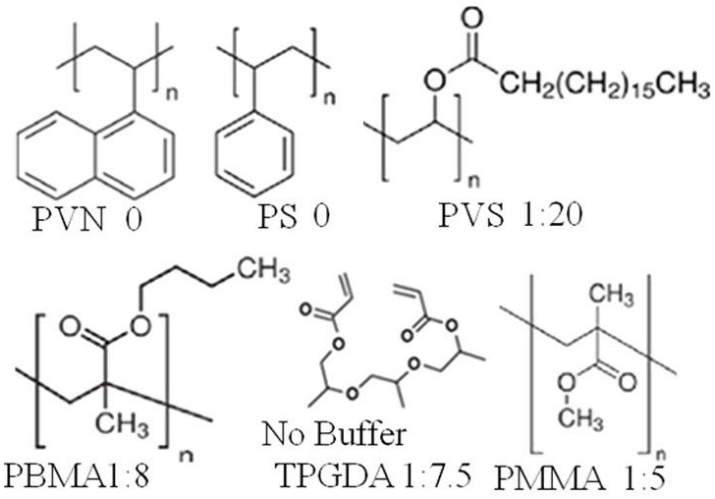


Figure 4-2 Molecular structure of the TPGDA monomer and each of the buffer layer materials, arranged in order of increasing ester group concentration in the chain relative to carbon content (given below each molecule).

The polymer buffer layers were spin-coated from toluene solutions at the following concentrations: poly(1-vinylnaphtalene) (PVN), 0.6 wt%; polystyrene (PS), 0.6 wt%; poly(vinyl stearate) (PVS), 0.6 wt%; poly(butyl methacrylate) (PBM), 0.6 wt%; and poly(methyl methacrylate) (PMMA), 0.6 wt%. The treated dielectric layers were annealed at 80 °C for 10 minutes to remove solvent from the spin-coated layer. Bare TPGDA reference layers were also annealed along with the buffer treated dielectric layers. A pentacene or DNTT film 50-70 nm thick was thermally evaporated at a rate of 0.2-0.8 Å/s on top of the dielectric surfaces through a shadow mask with the substrates at room temperature. The gold source/drain contacts (L = 200 μm, W = 2400 or 5000 μm) were thermally evaporated onto the pentacene layer through a shadow mask. The TPGDA monomer, buffer polymers and pentacene were all purchased from Sigma-Aldrich. The DNTT was synthesised based on the method of Takimiya[8] by Dr. John Morrison in Manchester University. After fabrication, the pentacene devices were encapsulated using microscope cover slides sealed with paraffin wax. This encapsulation effectively prevented the transistors from degrading during repeated measurements in air. The DNTT devices proved to be stable, and were not encapsulated.

4.2.2 Characterisation

The polar (γ^{polar}) and dispersive ($\gamma^{dispersive}$) components of the surface energy of the buffer layers were calculated based on contact angle measurements using water and diiodomethane following Fowkes's method[9]. The contact angle measurement was conducted by Dr. Veronica Sanchez, in Manchester University.

Buffer layer thicknesses were measured by coating directly onto microscope slides for measurement with a MicroXAM 5000B 3d ADE Phase shift interference contrast optical profiler. The edge steps were created using a knife to scratch part of the film out. Surface topographies of the dielectric, buffer and semiconductor layers were characterized by an Auto Probe CP Atomic Force Microscope using noncontact mode.

The semiconductor layers were further characterised using a Siemens D5000 θ-2θ X-ray diffraction analyser employing copper kα radiation (λ=0.15406 nm) and a secondary monochromator. The samples were scanned using a step size of 0.04° 2θ in the range 4° to 30° 2θ and a count time of 18 seconds per step.

Transistor characteristics were measured in air using two source measurement units (Keithley, Model 2400) following the IEEE Standard Test Methods for the Characterization of Organic Transistors and Materials[30]. The calculation of charge carrier mobility, μ, was based on the conventional square law equation[31] (**Equation (11) from the Chapter 2, section2.2.2)**:

$$I_{\mathrm{dsat}} = \mu \frac{W}{2L} C_{\mathrm{i}} \left(V_{\mathrm{g}} - V_{\mathrm{t}}\right)^2 \qquad (11)$$

where I_{dsat} is the saturation source-drain current; W and L are the channel length and width respectively; C_i is the capacitance per unit area of the dielectric layer; V_g is the gate voltage; V_t is the threshold voltage. By plotting the $\sqrt{I_{dsat}}$ versus V_g, the mobility is

calculated from the slope of the linear section of the $\sqrt{I_{dsat}}$-V_g curve. Extrapolating the linear section of this curve to voltage axis, V_t is obtained.

4.3 Results and Discussion

4.3.1 Dielectric Surface Properties

With no buffer layer, the root mean square, RMS, surface roughness of flash evaporated TPGDA films was about 0.4 nm over a 3 μm by 3 μm sample area. This is close to that of thermally grown SiO_2 on Si, often used as a gate dielectric[7]. Table I shows that with the spin-coated buffer layers the surface roughness was reduced slightly to ~0.3 nm. The polar and dispersive components of the surface energy of each surface are given in the same table. As expected, the polymers without ester groups i.e. PS, PVN, were found to have highly non-polar surfaces. The low ester content PVS and PBMA also showed low polarity (γ^{polar} ≤1.2 mN/m) while bare TPGDA and PMMA surfaces had much higher values: 8.5 mN/m and 6.4 mN/m respectively. The polar component of the surface energy of TPGDA is greater than in PMMA, probably as a result of exposure to the plasma during curing[10]. The dispersive part of the surface energy and the total surface energy were generally not correlated with the ester group concentration, as evidenced by the data in **Table 4-1**.

Table 4-1 Surface ester/carbon ratio, roughness, surface energy and XRD peak intensity/position of pentacene (001) face on different buffer surfaces; also provided are hole mobility (μ) of transistors with different buffer layers.

Surface & Ester/carbon ratio		RMS (nm) 3x3μm	Surface energy			XRD of Pentacene		μ(cm²/Vs)
			γ^{total} (mN/m)	$\gamma^{dispersive}$ (mN/m)	γ^{polar} (mN/m)	Intensity (counts per second)	position 2θ (°)	
Bare TPGDA	1:7.5	0.44	43.1	34.7	8.5	5588	5.76	0.02±0.01
PVN	0	0.23	43.1	42.0	1.1	3644[a]	5.76[a]	0.03±0.01
PS	0	0.33	47.5	47.5	0.0	26656	5.80	0.22±0.09
PVS	1:20	0.33	23.1	23.1	0.0	73154	5.76	0.20±0.12
PBMA	1:8	0.20	42.1	40.9	1.2	4711	5.76	0.05±0.01
PMMA	1:5	0.25	43.4	37.0	6.4	93707	5.76	0.04±0.01

4.3.2 Semiconductor Morphology

There have been plenty of reports on the relation between dielectric surface energy and pentacene morphology[10-14]. Large pentacene grains have been reported on dielectric surfaces with the total surface energy ranging widely from 25 to 55 mN/m.[10, 13] Here, the aliphatic ester-containing PMMA surface, with γ^{total} of 37 mN/m and γ^{polar} of 6.4 mN/m resulted in large pentacene grains greater than 1.5 μm in diameter (**Figure 4-3**) and the highest XRD signal intensity (Table 4-1, **Figure 4-4**). Large pentacene grains with diameter reaching 1 μm were also observed on the non-polar ester-free PS (γ^{total}=47.5, γ^{polar}=0.0 mN/m) and the ultra-low surface energy non-polar: PVS (γ^{total}=23.1, γ^{polar}=0.0 mN/m) buffer layers. The naphthalene-containing PVN, which might be expected to give large pentacene grains due to the molecular similarity of the naphthalene units to the semiconductor, resulted in a grain size much smaller than that of PS, despite their comparable surface energy.

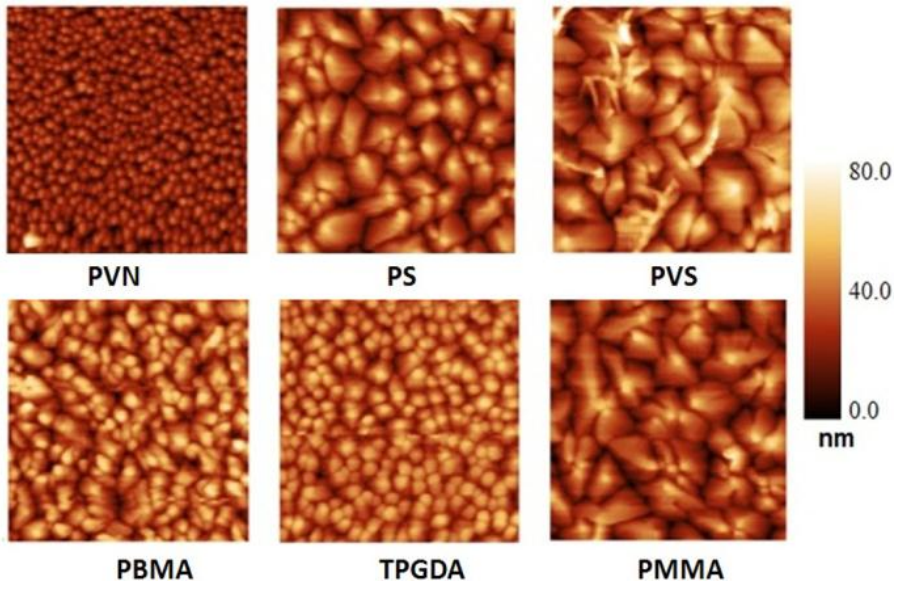


Figure 4-3 AFM topography images (3X3 μm) of pentacene grown on different dielectric surfaces.

The XRD signal peak intensity (**Figure 4-4, Table 4-1**), which provides a rough measure of crystalline order in the pentacene films[7], is generally correlated with the pentacene

grain size observed by AFM. The detailed cryptography of pentacene can be found in reference 7 and **section 2.5.3.1, page 34**. The pentacene crystal showed XRD traces commensurate with literature reports[15-17] with peaks at 2θ = 5.8°,11.52°, 17.28°and 23.04° of gradually diminishing intensity corresponding to the (001), (002), (003) and (004) reflections respectively. This suggests that the molecules are highly oriented perpendicular to the film surface by the crystallographic *c* axis with *d* spacing of about 15.2Å. The side peaks near the (001) and (002) on the pentacene film indicates the co-existence of a minority phase in which the pentacene molecules in the thin-film are tilted at a slight angle.

The XRD traces for 50-70 nm DNTT on PS PMMA and on a TPGDA surface are also shown in parallel with that of pentacene on TPGDA (**Figure 4-5**). Similarly to the pentacene, the DNTT that is grown on the bare TPGDA dielectric surface showed a much lower signal intensity compared with that grown on a PS or PMMA surface.

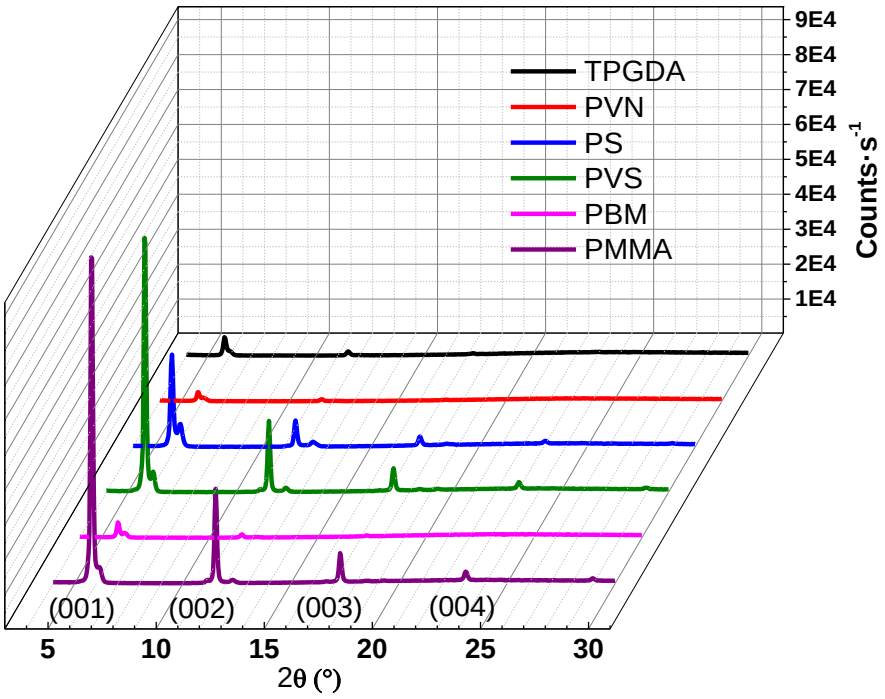


Figure 4-4 XRD traces of pentacene on as-cured TPGDA, PVN, PS, PVS, PBM and PMMA surfaces.

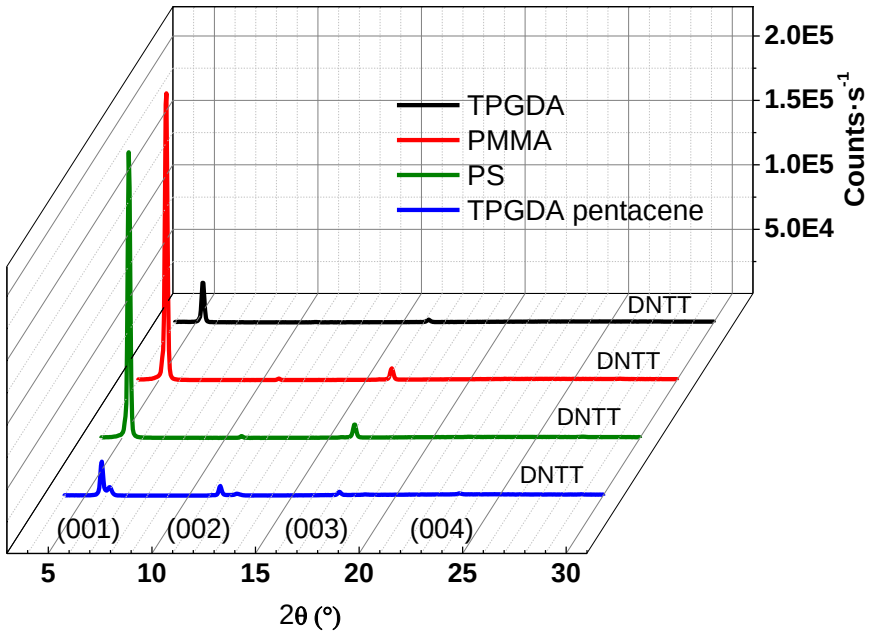


Figure 4-5 XRD traces of pentacene and DNTT on polystyrene and as-cured TPGDA surfaces.

The DNTT similar to pentacene also seem to orient perpendicularly to the substrate layer by layer, (ref to **Figure 2-17, page 35**), showing intense peaks at 2θ = 5.32° and 16.24° corresponding to the (001) and (003) reflections; and weak peaks at 2θ = 10.80° and 21.72° corresponding to the (002), (004) reflections, with a d spacing of about 16.5Å, slightly greater than that of pentacene. It is not clear why the intensity of the odd numbered reflection peaks are greater than that of the even numbered reflection peaks, but such a phenomenon has been reported previously by other researchers[18-19]. The high intensity of 20,000 counts per second of the main peaks and the lack of side peaks indicate that the DNTT crystal is much more ordered than the pentacene.

It is concluded, therefore, that pentacene and DNTT crystalline morphology does not correlate with the presence/absence of either ester or aromatic groups on the dielectric surface. Furthermore, it does not correlate with the surface energy of the underlying substrate, as both weakly and strongly polar/dispersive surface energy gave large crystals in some cases. The pentacene and DNTT growth might be affected by other factors associated with the dielectric surface e.g. T_g or surface molecular arrangement/morphology[20]. Of course, the transistor performance is likely to be dominated by the pentacene order very close to the dielectric surface which may be very different from the bulk and free-surface morphology, as suggested by the "layer+island" crystal growth mode for the first few layers of pentacene[12-13, 21].

4.3.3 Transistor Performance

Table 4-1 and **Figure 4-6** present the charge carrier mobility of OTFTs with a bare TPGDA dielectric surface and with different dielectric surfaces buffers. The mobility is calculated from the saturation region of the transfer curves using the conventional square law equation[22-23] (**Equation (11)** in **Chapter 2, section 2.2.2)**. The presented values are averages obtained from at least four, and up to 24, individual transistors. All

pentacene layers were deposited simultaneously in the same run, thus excluding effects that may arise from batch-to-batch inconsistencies in the pentacene evaporation process (the pentacene film on PVN was deposited in a separate run for XRD with deposition parameters kept the same). Among the surfaces that gave large crystals greater than 0.5 μm in diameter i.e. PS, PVS, PMMA, the highest mobilities of about 0.2 cm^2/Vs, were observed on the PS and the PVS surfaces which have zero and one ester per 20 carbon atom respectively, and displayed a near-zero polar surface energy. The PMMA surface, despite showing a large pentacene grain size greater than 1 μm, high XRD signal intensity and similar signal peak position as that of PS and PVS, led to a mobility no better than that of PVN and PBMA for which the grain size was much smaller. The PBMA, bare TPGDA, and PVN with smaller grain size showed the expected much lower mobility less than 0.05 cm^2/Vs.

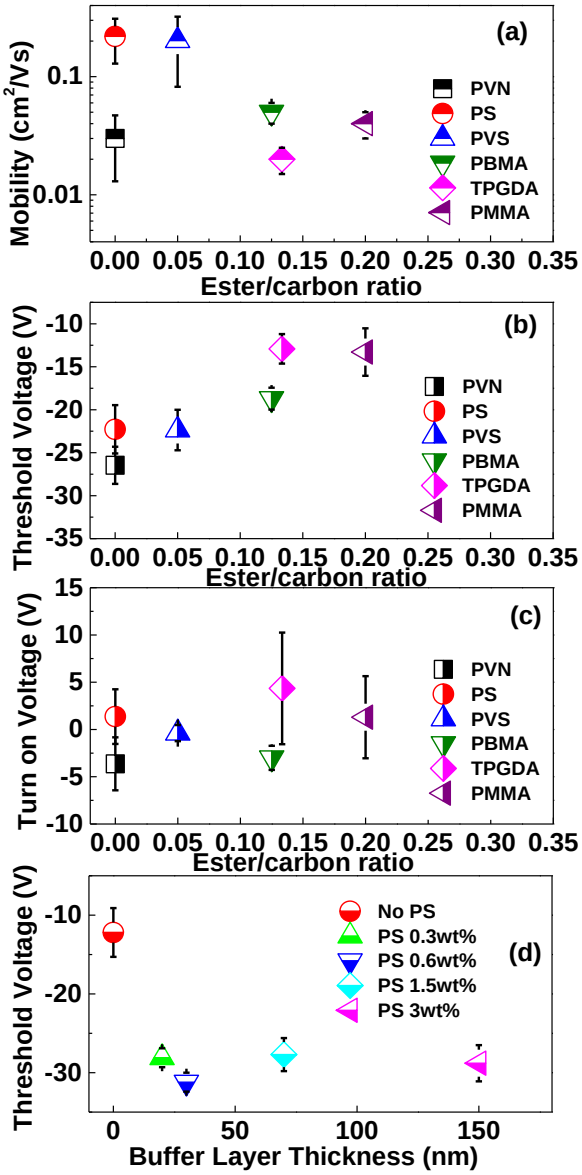


Figure 4-6 a) Hole mobility versus ester/carbon ratio of the buffer polymer. b) The threshold voltage of transistors versus ester/carbon ratio of the buffer polymer. c) Turn-on voltage of transistors versus ester/carbon ratio of the buffer polymer. d) Threshold voltage of transistors with PS buffer layers of different thicknesses prepared from solutions with the concentrations indicated: 20 nm (0.3 wt%), 30 nm (0.6 wt%), 70 nm (1.5 wt%) and 150 nm (3 wt%).

To confirm the improvement brought by the low ester content nonpolar surface, experiments were repeated on PS buffered and bare TPGDA. **Figure 4-7** shows the

average charge carrier mobilities and threshold voltages of transistors in 20 individual groups in ten pairs. Each group had at least 3 and up to 11 devices. Each pair was prepared in the same pentacene deposition run. At least a four times higher average mobility was observed with a PS buffer layer compared with that without the PS buffer. The highest average mobility of 0.72 cm^2/Vs was observed in a batch of 6 transistors with a PS buffer layer. The scattered value of the mobility between different batches was most likely due to a) differences in the handling time and the environment during each step of fabrication and before measurement, and b) differences in pentacene crystal morphology due to variation of deposition parameters including speed, angle and raw material quality.

An optimised fabrication process was finally found by i) reducing the handling time between each step and encapsulating the pentacene immediately after fabrication; ii) keeping the pentacene powder and transistors in the dark; and iii) control the semiconductor deposition rate at strictly 0.2 $Å \cdot s^{-1}$ for the first 10 nm.

By applying the optimised process for pentacene as well as DNTT devices with PVS, PS, PMMA and bare TPGDA, devices were obtained and their performance is shown in **Figure 4-8** and **Figure 4-9**. The DNTT devices showed much better transfer behaviour compared with that of pentacene: the mobility of the DNTT devices reached $\sim 1.00 cm^2/Vs$ on PVS and PS surfaces, with on/off ratio of about 10^6-10^7. They also showed a lower subthreshold swing of 0.7 $V \cdot dec^{-1}$. More importantly, the DNTT device required no encapsulation and was much more stable in various environments compared with the pentacene devices. This will be discussed in **Chapter 6, section 6.3.2**. As for pentacene, the semiconductor only showed high mobility on the PS and PVS buffered surfaces but not on the bare TPGDA and PMMA surfaces despite a large crystal size (**Figure 4-9** insert) and high XRD intensity.

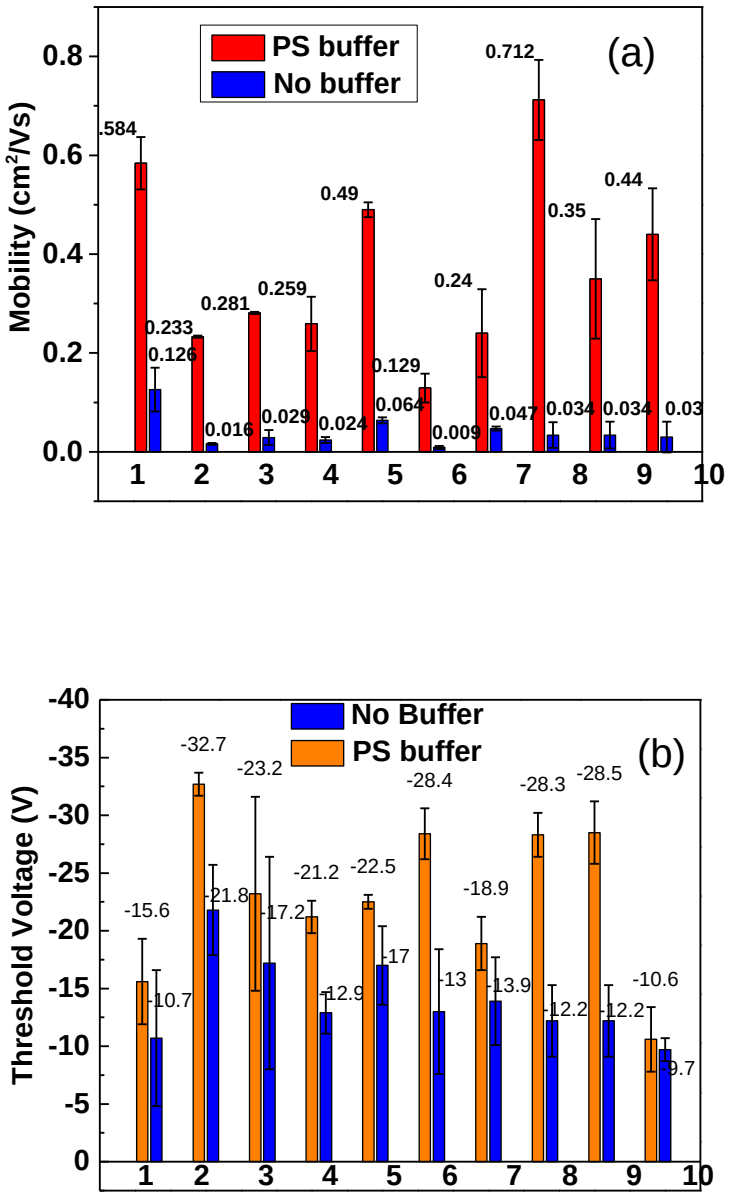


Figure 4-7 Average mobilities (a) and threshold voltage (b) of transistors with TPGDA dielectric and PS buffer layer coated TPGDA dielectric layer in ten separate batches.

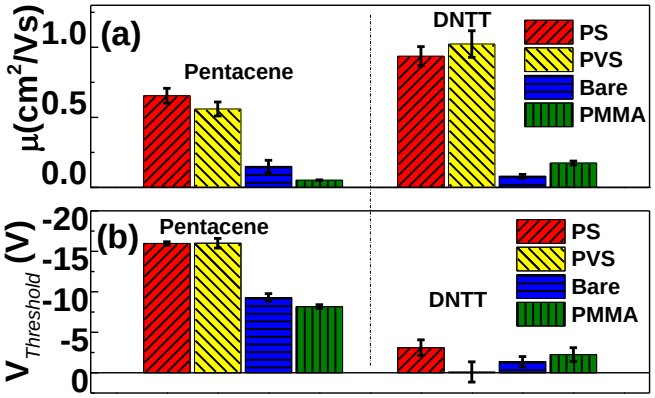


Figure 4-8 a) Hole mobility and b) threshold voltage of transistors with pentacene and DNTT on different buffer surface.

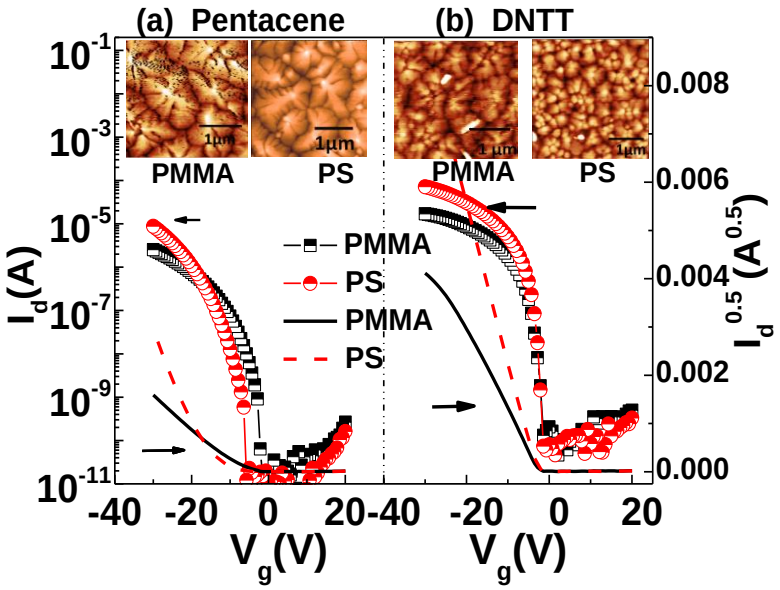


Figure 4-9 Typical transfer curves of a) pentacene and b) DNTT transistors formed on PMMA-buffered and PS-buffered TPGDA. The inserts are the typical AFM images of pentacene and DNTT on the PMMA/PS-buffered surface.

The low mobility associated with the high ester content TPGDA and PMMA buffer, despite the favourable morphology, is in good agreement with the review by Veres *et al*[24]. They summarised that a polar/high k dielectric surface restricts OTFTs mobility due to its polarity, and conversely a non-polar surface gives high mobility. Two different

models, i.e. a density of states (DOS)[25] broadening model based on hopping transport of charge carriers and a Fröhlich polaronic coupling model[26], have been built to explain the observation, however the detailed mechanism is still not confirmed.

While improving carrier mobility, the reduction in surface ester concentration caused a systematic change of ~15 V to more negative values in the threshold voltage, V_T, of the pentacene devices (**Figure 4-6** (c)). A similar trend was observed in the group of devices with optimised pentacene deposition (**Figure 4-8** (right)) although the extent of the shift was smaller. This is in contrast to the turn-on voltage, V_{to}, which was scattered around 0 V (**Figure 4-6** (c)), suggesting a sensitivity to interface defects and/or contaminants[27], where defects or contaminations could act as either hole or electron traps at the semiconductor or semiconductor/dielectric interface that affect the flat band voltage.

Threshold voltage is a key transistor parameter so that shifts in its value due to dielectric surface modification have been studied intensively. In the case of self-assembled monolayers (SAMs), the dipole field across the SAM thickness is thought to be the cause of such shifts[28]. In our case, since the polymer buffers are amorphous, the average dipole moment across the film is likely to be zero and so cannot be the origin of the shift in V_T observed here. This is further confirmed by the lack of dependence of V_T on the buffer layer thickness (**Figure 4-6** (d))[29].

According to Kobayashi[30], the difference in electron affinity between a dielectric and semiconductor can also induce a dipole across the insulator/semiconductor interface leading to differences in V_T from one dielectric material to the other. However, V_{to} should also follow the same trend - clearly this is not the case here for pentacene (**Figure 4-6** (c)).

Further evidence that neither of these explanations apply is seen in the comparison between DNTT and pentacene. Firstly, the different dielectric surfaces cause only a 2-3 V difference in the V_T of DNTT (**Figure 4-8** (b)). Secondly, the V_{to} is close to zero in all cases (**Figure 4-9** (b)), so the difference between threshold voltage and turn on voltage, V_T-V_{to}, for the DNTT is almost negligible while that of pentacene devices is obvious. This suggests that interfacial and bulk trap states are much fewer in DNTT compared with pentacene. This is confirmed in simulations undertaken with Silvaco's UOTFT model, which suggest an almost ideal behavior for DNTT transistors utilizing PS buffering[31]: mobility was found to be insensitive to the applied gate voltage, V_G, resulting in the ideal square-law dependence on V_G of the device current, I_D, in saturation (**Figure 4-9**(b)). In contrast, pentacene devices formed on the PS-buffered TPGDA display a high mobility only at high V_G – the strong dependence of mobility on V_G leading to the non-linear plot of $I_D^{0.5}$ vs V_G in **Figure 4-9** (a), a feature consistent with the presence of trap states in the semiconductor. The presence of trap states is highly likely to be the reason for the different performance of pentacene and DNTT transistors[30], and perhaps is also responsible for the threshold voltage shift observed with the different buffer layers with pentacene.

4.4 Summary

In conclusion, this work has shown that vacuum flash-evaporated and cross-linked TPGDA is a viable approach to produce stable, high mobility transistors from both pentacene and DNTT, so long as the insulator surface is buffered with a layer with a surface ester group content less than one per 20 carbon atoms. For pentacene devices, however, the higher mobility was accompanied by a detrimental shift of threshold voltage to more negative values. For DNTT devices, by contrast, buffering TPGDA with PS and PVS yielded a higher mobility accompanied by relatively low threshold voltage. Consequently, the development of a vacuum-based roll-to-roll process is concentrating on DNTT devices and on alternative, vacuum-compatible, methods of reducing the surface ester concentration of TPGDA.

Finally, although the primary goal was to establish the role of ester groups on transistor performance, the systematic modification of surface ester group concentration has shown that the overall dielectric surface energy is not the primary factor in determining grain size in subsequently evaporated films of pentacene and DNTT. Furthermore, this work has shown that larger grain size does not necessarily lead to high mobility - it must be coupled with a low value for the polar component of the surface energy. These observations may go some way towards reconciling conflicting reports in the literature on such effects.

4.5 References

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Chapter 5

Evaporated Buffer Layers for Surface Modification

5.1 Introduction

As shown in the previous chapter, a non-polar dielectric surface is important for organic thin-film transistors. Spin-coated PS or PVS[1] layers on the TPGDA have improved device mobility at least fivefold, reaching 1 $cm^2 \cdot V^{-1}s^{-1}$ and devices with this surface modification showed on/off ratio of at last 10^5 and sub-threshold slope of less than 0.7 $V \cdot dec^{-1}$. Fabrication of such a layer in vacuum is a necessary step to enable all-vacuum-evaporated transistor fabrication in roll-to-roll based production. It is, however, difficult to achieve because: firstly, polymerisation of non-polar long chain polymers from non-polar monomers or oligomers that can be vaporised easily in vacuum is difficult due to lack of reactivity of the hydrocarbon molecules; while oligomers that contain functional groups[2-5], which polymerise or cross-link under moderate conditions, usually contain polar sites. Secondly, it is difficult to evaporate long chain/solid polymers without reducing the molecular weight[6]. This leads to a lower T_g and thus reduced thermal-mechanical stability for the polymer film especially on its surface. Thirdly, evaporated polymers are usually prone to form a rough dielectric surface[7] which is undesirable for semiconductor growth. Given the above reasons, there are a very limited number of reports found on deposition of non-polar polymer dielectric layers in vacuum[7]. The only

case found, which had real application in industry, was parylene-N deposition by a pyrolysis process, which is used in encapsulation for electronics[8-9]. This process, however, is a batch to batch process and requires a relatively long deposition time.

To solve this problem, work has been done on testing a range of polymer deposition processes and materials including the parylene-N deposition in a roll-to-roll environment, thermal evaporation of alkyl chain polymers and flash evaporation of acrylates with long alkyl segments to make a buffer layer on top of a flash evaporated TPGDA dielectric layer for DNTT OTFTs.

5.2 Experimental

The buffer layers were deposited on a layer of flash evaporated TPGDA (400-530 nm) cured by plasma on a polyethylene naphthalate (PEN) film of 125 μm. Al patterns were pre-deposited on the PEN substrate before the TPGDA deposition. The area capacitance of the dielectric layers were between 9.6 $nF \cdot cm^{-2}$ to 12.8 $nF \cdot cm^{-2}$.

5.2.1 Thermal Evaporation of Polystyrene and Tetratetracontane (TTC)

Polystyrene (purchased from Sigma Aldrich) was thermally evaporated via a tungsten boat in an Edwards 306 evaporator onto the TPGDA substrates held stationary in the chamber during evaporation. The evaporation speed was monitored by a quartz crystal thickness monitor by setting the density value at 1 $g \cdot cm^{-3}$ and the acoustic constant, Z, to a value of 2.55[10]. Evaporation speed was controlled between 5 $Å \cdot s^{-1}$ to 15 $Å \cdot s^{-1}$. A total thickness of 20 nm PS was deposited.

Tetratetracontane (TTC) (purchased from Sigma Aldrich) (**Figure 5-1**) was evaporated in a Eurocoater thermal evaporator from an alumina crucible. The substrates were attached to a sample holder on top of the crucible. The deposition speed was monitored

by a quartz crystal monitor by setting the density value at 1 g·cm^2 and Z value at 2. Deposition speed was controlled at 1-3 Å·s^{-1}.

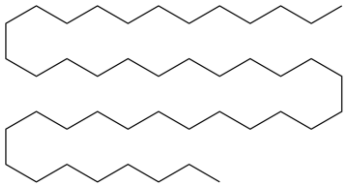


Figure 5-1 molecular structure of tetratetracontane.

5.2.2 Parylene-N Deposition

Two batches of [2-2]paracyclophane (Parylene-N), was purchased from Suzhou Jiangnan Fine Chemical Co., Ltd. (500 g, 99% purity) and Sigma Aldrich (5 g, 97% purity). Parylene-N was deposited via two approaches: a) plasma-assisted thermal evaporation and b) thermal evaporation followed by pyrolysis, in both cases using deposition systems built and developed as part of this work.

Plasma assisted thermal evaporation were carried out in the Oxford vacuum web coater. 3g of Parylene-N (99%) was contained in an aluminium evaporation cell with a slit 3 mm wide and 100 mm long. The cell was located close to the DC magnetic sputtering plasma source in the web coater (**Figure 5-2**). The projection path from the cell to the drum was covered by a shutter to prevent the evaporated parylene-N from going directly to the substrate without reacting with plasma.

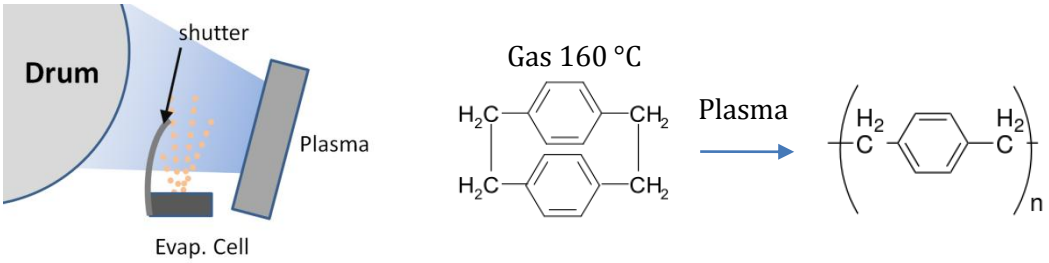


Figure 5-2 Schematics of plasma-assisted parylene deposition (left), molecular structure of parylene-N dimer and cross-linked parylene-N (right).

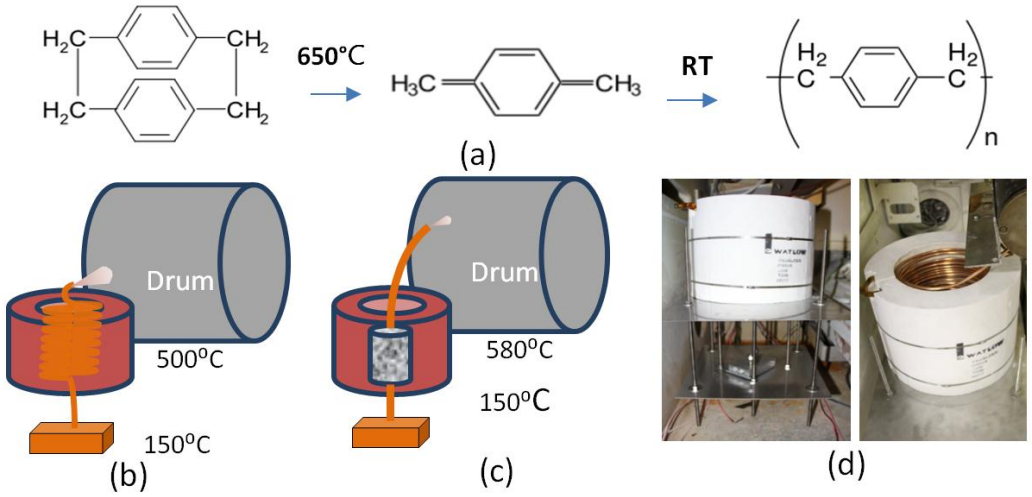


Figure 5-3 Schematics of parylene-N polymerisation reaction via pyrolysis (a) with copper pipe heating setup (b); with quartz tube filled with silica beads heating setup (c); and photos of furnace for pyrolysis (d).

For deposition, the evaporation cell was heated by two 225 W cartridge heaters to parylene-N's vaporisation temperature: 150 °C, then Ar gas of 200 sccm was introduced into the vacuum chamber in the vicinity of the cathode. DC power of 6 A was provided to the cathode to strike the Ar plasma (see **Chapter 3, section 3.2.3**). The drum was then set rotating at a speed of 5 m·min^{-1}, and so the evaporated material could condense onto the substrate fixed to the rotating drum over a period of 2 minutes, during which the evaporation cell temperature reached 180 °C, probably due to the heat of the plasma; the

voltage of the plasma increased and reached 400 V due to cathode poisoning. After deposition, the plasma and thermal evaporation cell was switched off immediately.

The other deposition route was vaporisation followed by pyrolysis which was more similar to the established industrial process[8-9, 11-13]. The parylene-N was evaporated firstly at its vaporisation temperature of about 150°C in vacuum then the vapour passed through a furnace of 450-700°C where it is activated into its monomer form. The active monomers exited the furnace and condensed onto substrate: polymerisation happens after the monomer condensation on the substrate. The homemade evaporation system consisted of a sealed aluminium evaporation cell powered by two 225 watt cartridge heaters, the cell was connected to a copper pipe of ten meters long and 3 mm in inner diameter. The copper pipe was fitted into a 1500 W Watlow furnace with the open end of the pipe facing the substrate (drum) with a gap of about 1 cm (**Figure 5-3** (b)) between the pipe end and the substrate. Three thermocouples were fitted: on the evaporation cell, on the inside wall of the furnace and at the exit of the copper pipe. The whole system was fitted on the Oxford vacuum web coater. For deposition, the vacuum chamber was firstly evacuated to a pressure of 10^{-4} mbar, the furnace was heated to 500°C, and this temperature was maintained, then the evaporation cell containing the dimer was heated to 160-170 °C. The deposition was monitored through an inspection window. After the deposition had stabilised, determined by observing the growth of a ring of parylene-N on the substrate facing the pipe end, the drum was set rotating at speed of 3 $m \cdot min^{-1}$, and material was continuously deposited on the substrates fixed to the rotating drum for a period of 1-3 min.

Another configuration, which gave higher heating surface area for the parylene vapour was also tested (**Figure 5-3** (c)). The spiral copper tube was replaced by a quartz tube of 15 cm in length and 8 cm in diameter. The quartz tube was filled with silica beads with

diameter of 3 mm. This system was expected to provide better heating for the parylene-N vapour and also to prevent the vapour from contacting copper surface, which was suspected to deactivate parylene-N monomer[14]. This setup was heated up to 600°C twice for 4 hours before deposition was attempted to make sure the system was free of evaporable contamination. During evaporation the furnace were heated to 580°C and held for 1 hour before deposition started in order to make sure the core of the quartz tube reached the same temperature as the furnace.

5.2.3 Deposition of Acrylate Containing Long Alkyl Segments

Mono-acrylate with a long alkyl chain section to the monomer was deposited using flash evaporation followed by plasma or electron beam curing in the Oxford vacuum web coater. Liquid monomer including mono acrylate of hexyl acrylate (Sigma Aldrich), lauryl acrylate (Sigma Aldrich) and their mixture with the diacrylate: HDDA (Sigma Aldrich) (**Figure 5-4**) at concentration of 5:1 (monoacrylate : diacrylate) in volume were used as liquid precursors.

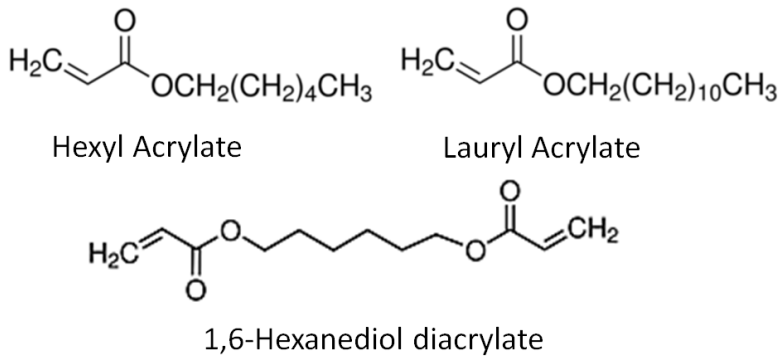


Figure 5-4 molecular structure of Hexyl acrylate, Lauryl acrylate and 1,6 hexanediol diacrylate (HDDA)

The liquid monomers were injected into the heating tank of 260°C; Ar plasma of 6 A, 200 V was used to cure the samples. The lauryl acrylate and HDDA mixture were also cured

by an electron beam of 2.6 kV and 90 mA. The substrate, attached to the drum (17°C), passed the evaporation nozzle and the curing source at a speed of 5 $m \cdot min^{-1}$ multiple times. The multiple pass process was used for processing convenience. Single pass roll-to-roll process should be achieved as long as curing power is sufficient.

5.2.4 Transistor Fabrication

A DNTT layer of 70 nm was thermally evaporated on top of the buffers through a shadow mask. A gold source and drain layer was then deposited on top. The fabrication parameters were the same as those of **Chapter 4, section 4.2.2**.

5.2.5 Characterisation

The surfaces were characterised by AFM, FTIR and Dektak thickness profiler the same as described in **Chapters 4 and 5**. X-ray photoelectron spectroscopy was conducted by Dr. Philip Holdway to analyse the element distribution on the polymer buffer surface. XPS was performed using a 200 Watt unmonochromated magnesium X-ray excitation. The analyser was operated at constant pass energy of 100 eV. Data was processed using CASAXPS software. The transistors were characterised by two source measuring units (Keithley 2400 module) following the procedure in **Chapter 4, section 4.2.2**.

5.3 Results and Discussion

5.3.1 Thermally Evaporated Polystyrene

The 20 nm thick layer of evaporated PS (E-PS) was characterised by AFM in non-contact mode. The polystyrene appears as small lumps, 1-2 μm across, on the TPGDA surface. These small lumps were observed to have aggregated in the area probed during the AFM scan (**Figure 5-5**), suggesting that they are mobile on the surface. The root mean square (RMS) roughness of the surface was measured to be 30-40 nm for a 3 μm by 3 μm area. This morphology is in contrast to the spin-coated PS layer, which showed a very smooth surface with RMS roughness of 0.3-0.4 nm on the TPGDA surface. It is highly likely that the chain mobility of the evaporated PS chains was much higher than that of spin-coated material: the T_g of the evaporated PS may be lower due to polymer chain scission during thermal evaporation, and the molecules may not be well-entangled in the evaporated case. The surface roughness problem was not improved by using a different evaporation speed (up to 15 Å·s^{-1}) or by increasing the layer thickness to 100 nm.

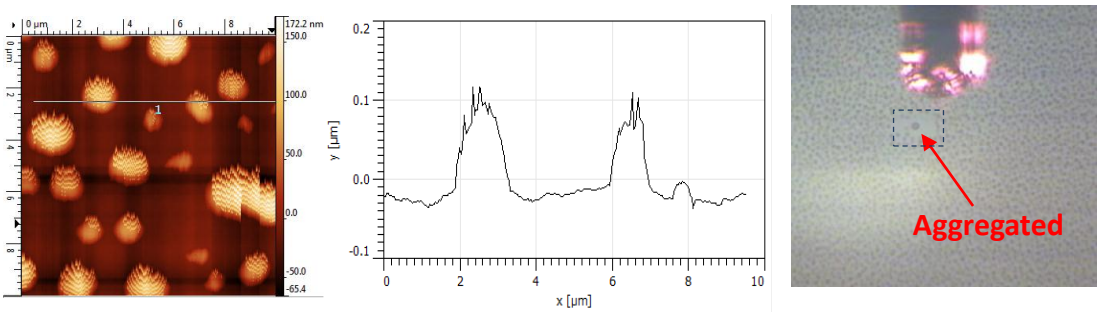


Figure 5-5 AFM image of thermally evaporated polystyrene on TPGDA surface (left), line profile of thermally evaporated polystyrene on TPGDA surface (middle). Optical micrograph of the thermally evaporated PS surface including the area scanned by AFM, indicated by the dashed rectangle (right).

Figure 5-6 and **Figure 5-7** (c) show mobility and transfer characteristics of DNTT transistors with E-PS buffer along with other buffer surfaces. The evaporated polystyrene surface would be expected to give poor transistor performance for all the

devices due to the physically unstable and rough surface, however, interestingly, some DNTT transistors still showed relatively good performance and high mobility similar to that of spin coated polystyrene. This resulted to an average mobility of 0.4 $cm^2 \cdot V^{-1}s^{-1}$, but with a very large standard deviation of ±0.36 $cm^2 \cdot V^{-1}s^{-1}$. It is likely that the evaporated PS formed an uneven buffer surface, which included some "good" areas that able to provide high mobility in between the unstable and rough area[15].

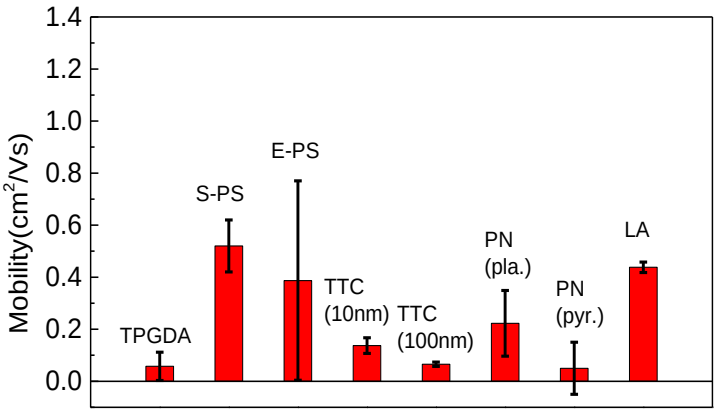


Figure 5-6 Mobility of transistors with bare TPGDA dielectric and with different evaporated buffer layers on TPGDA surface prior to DNTT deposition. S-PS denotes spin coated polystyrene, E-PS denotes evaporated polystyrene, PN(pla.) denotes parylene-N by plasma-enhanced deposition, PN(pyr.) denotes parylene-N by pyrolysis.

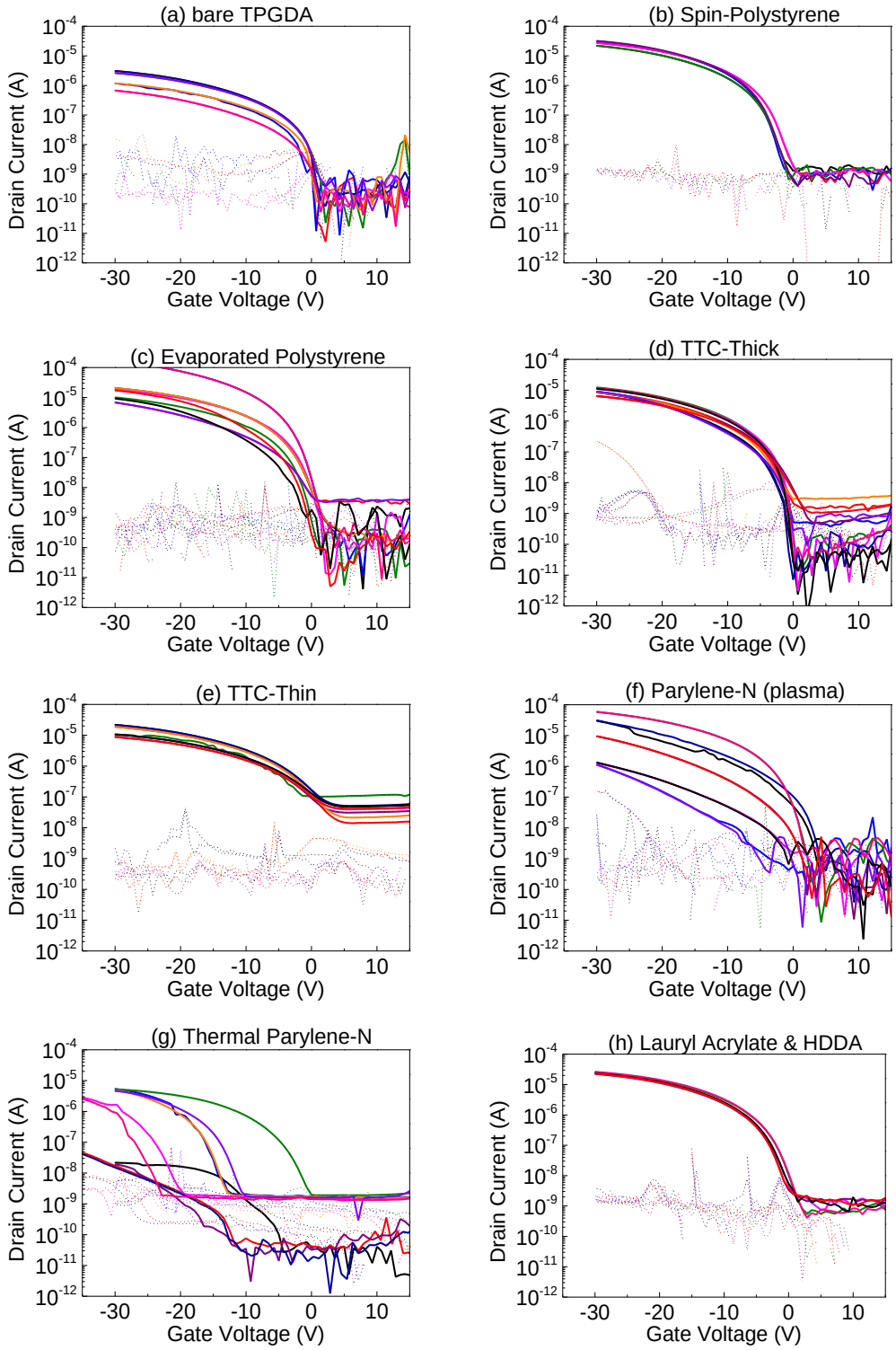


Figure 5-7 Transfer characteristics (V_d=-20V) and gate leakage (dashed line) of transistors with (a) bare TPGDA dielectric of layer of 530nm; (b) Spin coated polystyrene on TPGDA of 400nm; (c) Evaporated polystyrene on TPGDA of 530nm; (d) Evaporated TTC (100 nm) on 450nm TPGDA; (e) Evaporated TTC (10nm) on 450nm TPGDA; (f) Parylene-N deposited by plasma assisted deposition on 530nm

TPGDA; (g) Thermally evaporated parylene-N on 530nm TPGA; (h) Flash evaporated lauryl acrylate and HDDA mixture on TPGDA of 400nm.

5.3.2 Thermally Evaporated TTC

It was reported that an evaporated TTC layer could provide a flat and stable surface on the main dielectric layer to give transistors with good performance[16]. The TTC film produced in this work however, was found to be rough, i.e. with an RMS of 44.5 nm for a film of 100 nm thick on a 3 µm by 3 µm surface. Small grains with diameter of about 0.5 µm were observed by AFM (**Figure 5-8**). By reducing the layer thickness to about 10 nm, the roughness of the surface was reduced to about 2-3 nm.

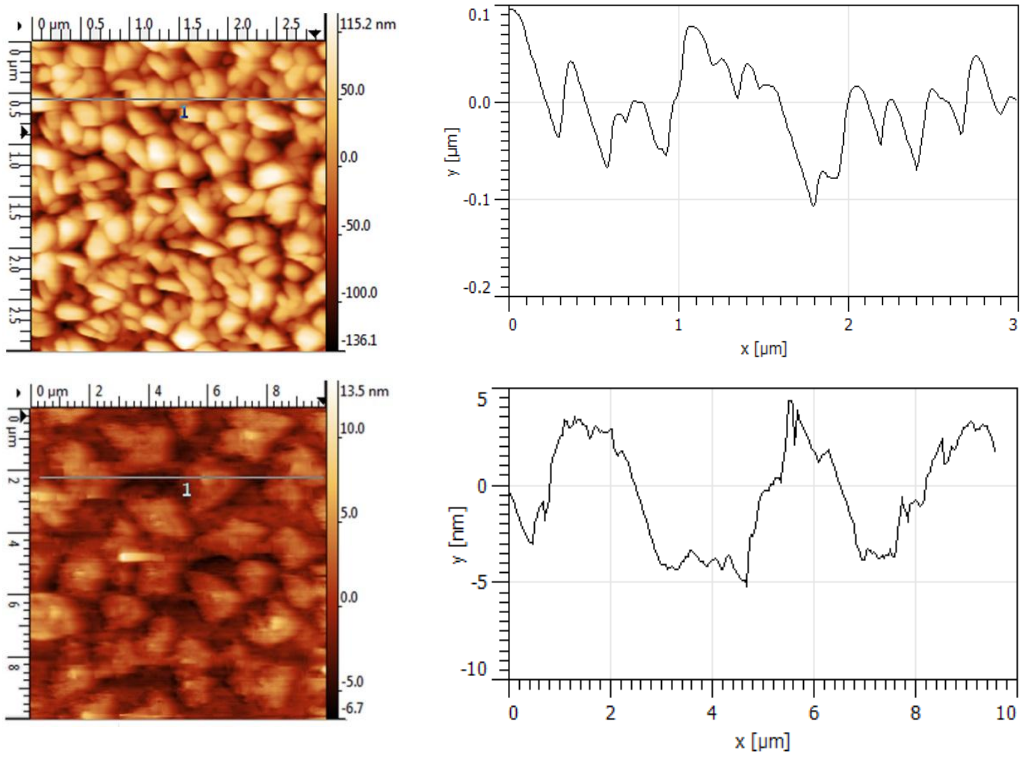


Figure 5-8 AFM topography image and line profiles of TTC of 100nm (top) and 10nm (bottom) thickness on a TPGDA surface.

Figure 5-7 (d) and (e) show the DNTT transistor performance on these two buffer surfaces. The devices with thick TTC layer showed a relatively consistent performance. Most of the transistors showed a sharp switch-on indicating a low density of trap states

at the interface between dielectric and DNTT[17-18]. The mobility of the transistors was, however, less than 0.1 $cm^2 \cdot V^{-1}s^{-1}$, probably because of the high roughness leading to disorder in the semiconductor. The performance of the devices with the thin TTC buffer was different: they showed higher mobility but with a larger spread of performance, a high off-current and greater sub-threshold swing. The higher mobility was expected due to the lower roughness of the thin TTC buffer. However, it was not clear why the thin TTC had a much higher off-current and sub-threshold swing, despite the DNTT deposition being carried out in the same run as the thick TTC group. Possible reasons could be the insufficient coverage of the TTC on the TPGDA surface or device degradation during handling.

5.3.3 PN Plasma-Enhanced Deposition

Parylene-N was deposited onto the substrate at an average speed of 20 nm per pass with drum speed of 15 $m \cdot min^{-1}$. 100 nm films were obtained in a 1 minute run. The parylene film deposited via plasma-assisted reaction had a low surface roughness, as shown in **Figure 5-9**. The film on a glass substrate was solid, and strong enough to resist wiping with a cotton tip.

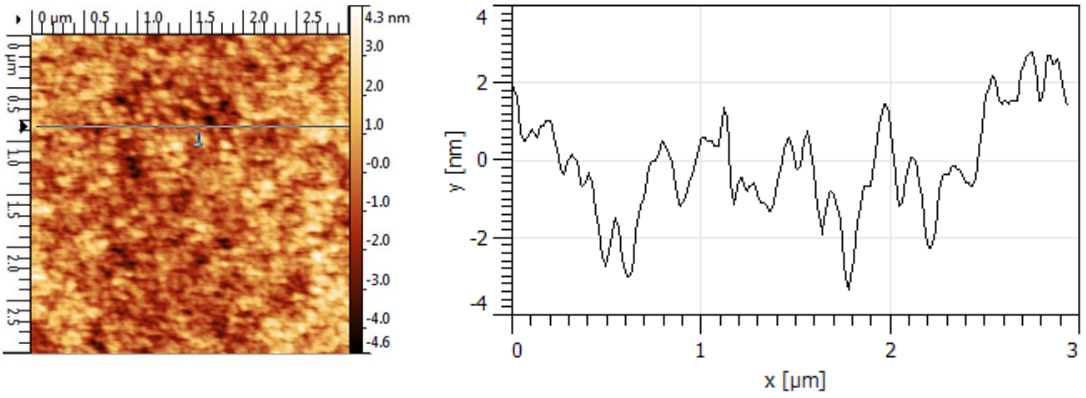


Figure 5-9 AFM topography image and line profile of parylene-N surface of 100 nm thick deposited with plasma assistance.

The XPS surface analysis (**Figure 5-10, Figure 5-11**) showed that the oxygen content at the dielectric surface was significantly reduced by the coating. Excluding the oxygen in the form of silicon dioxide which was possibly from the glass substrate, the atomic content of oxygen on the surface was only 6%. This was about 2 times lower than that of TPGDA. The XPS data also proves that no Al was sputtered from the target. The trace amount of fluorine and nitrogen peaks are probably due to evaporation tank contamination.

The IR spectrum of the deposited parylene-N film (**Figure 5-12**) showed strong absorption at 600-1800 cm^{-1} and 2500-3500 cm^{-1}, and was totally different from the commercial reference spectrum of cross-linked parylene-N, shown in **Figure 5-14**. Together with the observation that the cathode became contaminated with black carbon during deposition, it was indicated that severe breakdown of the parylene had happened during the deposition. The high power density of the plasma is the probable reason for the breakdown.

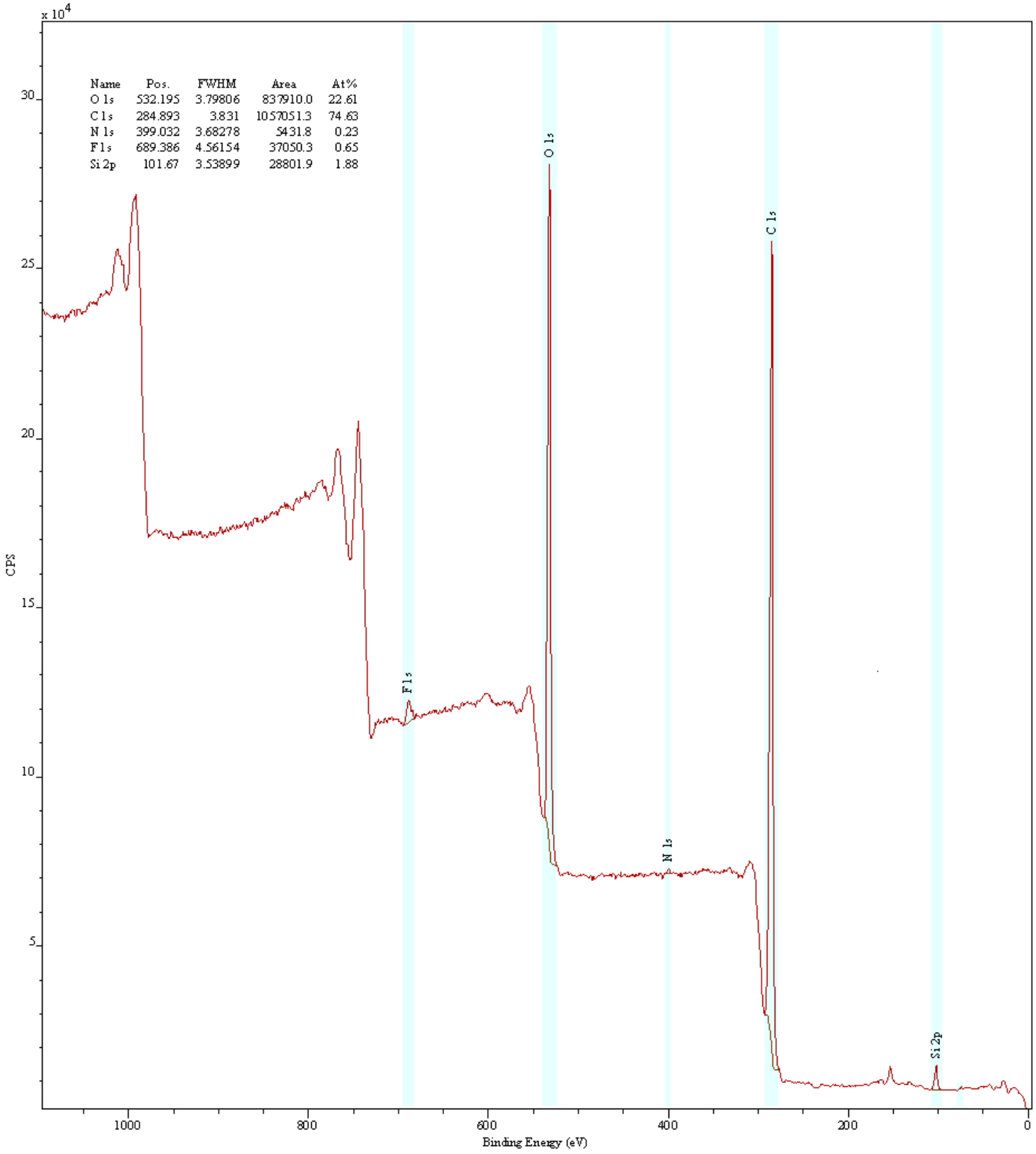


Figure 5-10 XPS of TPGDA surface

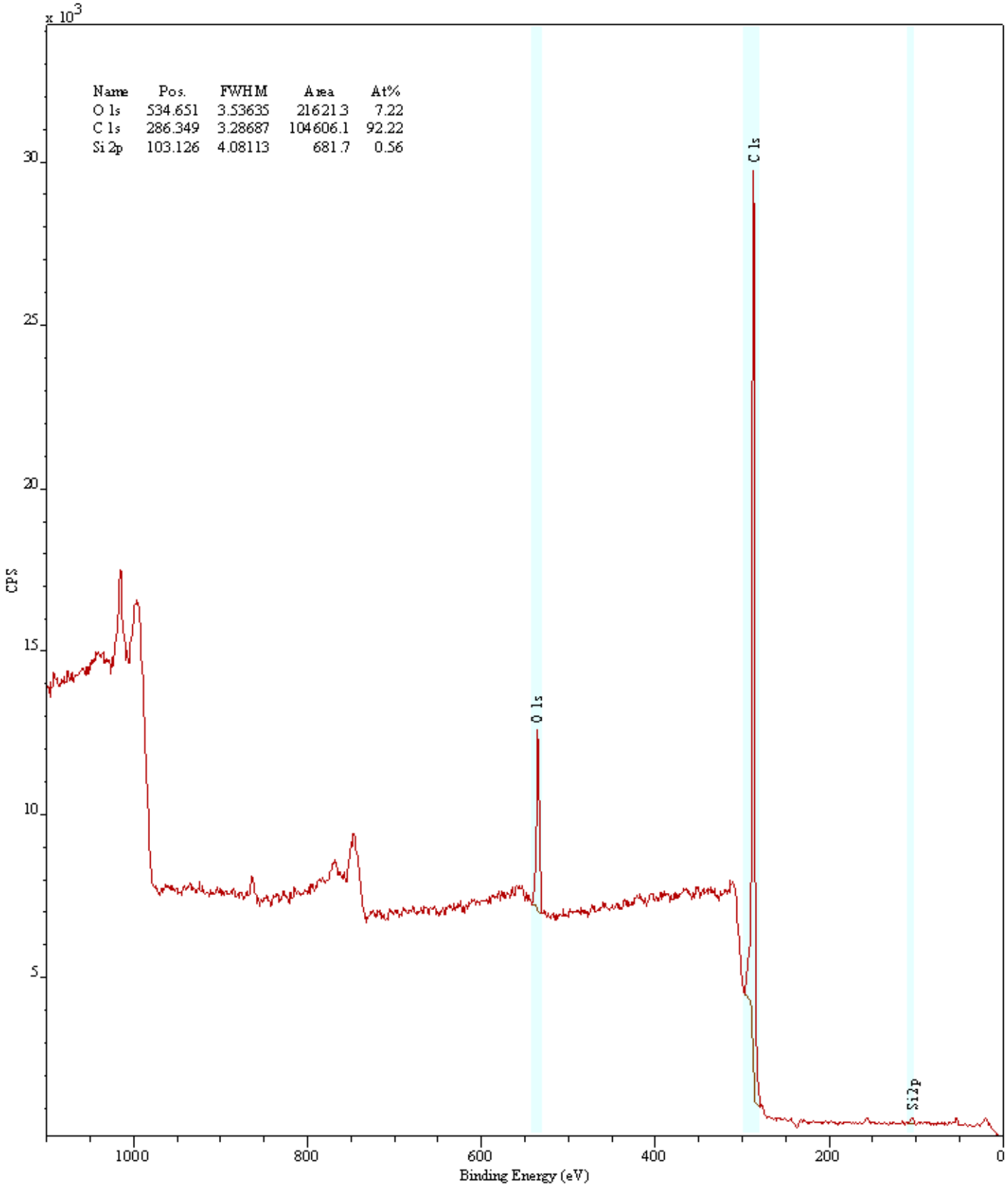

x 10^3
Name Pos. FWHM Area At%
O 1s 534.651 3.53635 21621.3 7.22
C 1s 286.349 3.28687 104606.1 92.22
Si 2p 103.126 4.08113 681.7 0.56
O 1s
C 1s
Si2p
CPS
Binding Energy (eV)
30
25
20
15
10
5
1000
800
600
400
200
0

Figure 5-11 XPS of parylene-N coated TPGDA surface

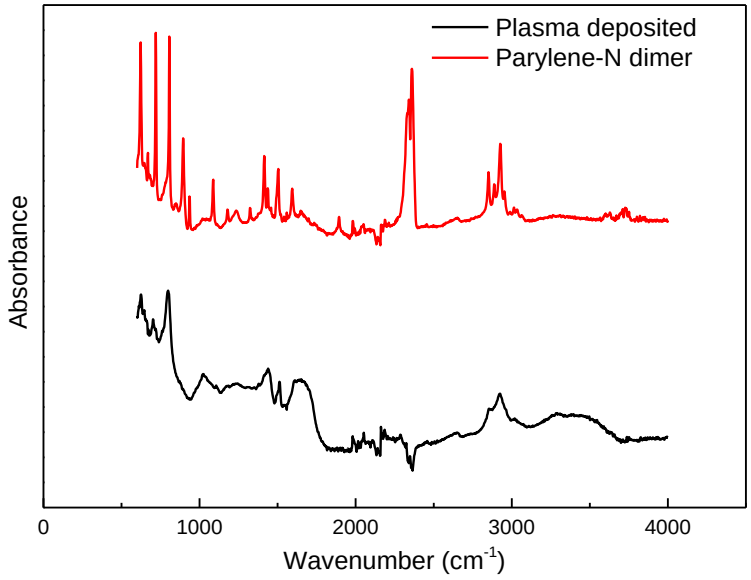


Figure 5-12 IR spectrum of parylene-N dimer purchased from Jiangnan Chemical and parylene-N film deposited by plasma assisted vacuum evaporation.

Parylene contamination on the cathode induced cathode poisoning. The carbon materials i.e. parylene dimer and its fragments generated in the plasma coated the surface of the cathode resulting in a residual layer which increased the work function of the cathode surface resulting in less plasma current (a dimmed plasma) and increasing of cathode voltage from 200 V to about 400 V during the few minutes of the deposition process.

Figure 5-7 (f) shows the transistors' performance with a plasma assisted parylene-N buffer. Similarly to the thermal evaporated polystyrene case, the transistors showed scattered performance. Some devices had high mobility but most other devices were poor. The average mobility of the P-N layer were about 0.2±0.21 $cm^2 \cdot V^{-1}s^{-1}$. Since, it was

not possible to maintain a stable plasma in the chamber due to cathode contamination, it was difficult to develop the deposition process further. A remote plasma with lower energy density would probably be needed for further developments.

5.3.4 Pyrolysis Parylene-N

Parylene-N films were also deposited onto Al-coated PEN substrate by the pyrolysis process at speeds of up to 1 μm for each pass at a drum speed of 3 m·min^{-1}. This speed was similar to that of flash evaporation, although the film covered a strip only 10-20 mm wide in this instance. The film showed good transparency and appeared to have very low surface roughness since an interference pattern was observed from the film (**Figure 5-13**). The material, however, was sticky and could be wiped off by a cotton tip. When the film thickness reached up to microns, it showed a yellowy colour and appeared to be viscous.

Interestingly, the deposited parylene film could etch the Al layer resulting in "pinholes". These pinholes grew in air with time, turning the reflective Al surface black, then transparent as time passed. This reaction only happened after the samples were moved to air. Steam appeared to accelerate the reaction.

The IR spectrum of the deposited material along with the raw material and commercially available cross linked parylene-N are presented in **Figure 5-14**. The peaks of the deposited film shifted significantly from the raw parylene-N and became close to that of the commercially available reference. There was also absorption in areas, e.g. around 900 cm^{-1}, outside the range of the reference spectrum.

From the above results, it is likely that the polymerisation had happened to some extent but the resulting molecular weight was probably very low. It is highly likely that there

were other compounds formed in the film to give it the yellow colour and chemical reactivity to etch the Al from the substrate.

According to the literature, the parylene monomer needs to be activated into its triplet state to polymerise. Transition metals such as copper will deactivate the triplets into singlet states[14] preventing polymerisation from happening. Accordingly, the copper pipe used for pyrolysis was a potential barrier to polymerisation, so a quartz tube was used to replace the copper pipe. The quartz tube was filled with silica beads of diameter 2-3 mm, to increase the contact area of parylene-N vapour with hot surfaces. However, despite the higher reaction temperature (580°C) and the metal-free reaction tube, the new setup gave the same yellowy film with poor mechanical properties. The IR spectrum of the deposited film was even further away from the reference.

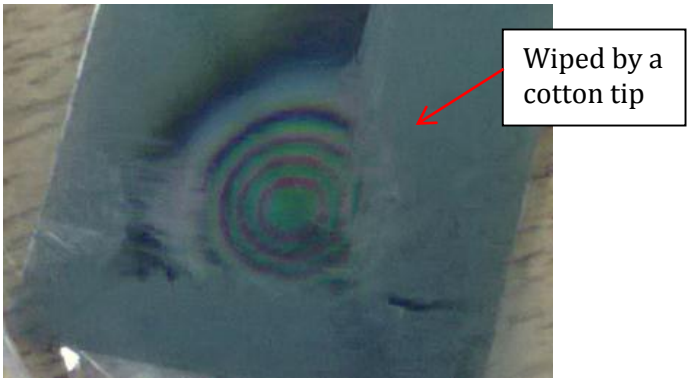


Figure 5-13 A photo of deposited parylene-N film by pyrolysis process on Al coated PEN substrate. The substrate stopped for few seconds resulted in thickness gradient that lead to interference rings.

The commercial process uses a relatively large pyrolysis chamber to allow a large amount of parylene-N vapour to stay active in the triplet state; the copper pipe or quartz tube by contrast only had an effective volume of less than 200ml. Therefore it was possible that the evaporated parylene-N vapour from the first stage cell went into the vacuum chamber without being properly activated by the furnace. This lack of buffer

volume between the sublimation cell and vacuum chamber could also lead to a problem of inconstancy of deposition rate. The relatively low furnace temperature for pyrolysis was another possible reason for the failure. Although 580 °C, which is 30°C higher than the reaction starting temperature, was reached in the deposition, this is still 100°C lower than the commercial process. Therefore the extent of activation of the dimer could be limited[19].

In conclusion, the deposition of parylene-N in a roll-to-roll environment by our homemade evaporation apparatus was not very successful. However, this work demonstrated the potential of depositing an organic film with no need for post treatment and with the substrate being held at room temperature at an ultra-high speed in a roll-to-roll environment. Although polymerisation of parylene-N was difficult, other parylene materials e.g. dichloro[2.2]paracyclophane (parylene-C), which are much more reactive than parylene-N, still hold the potential to be applied in the process to make coatings.

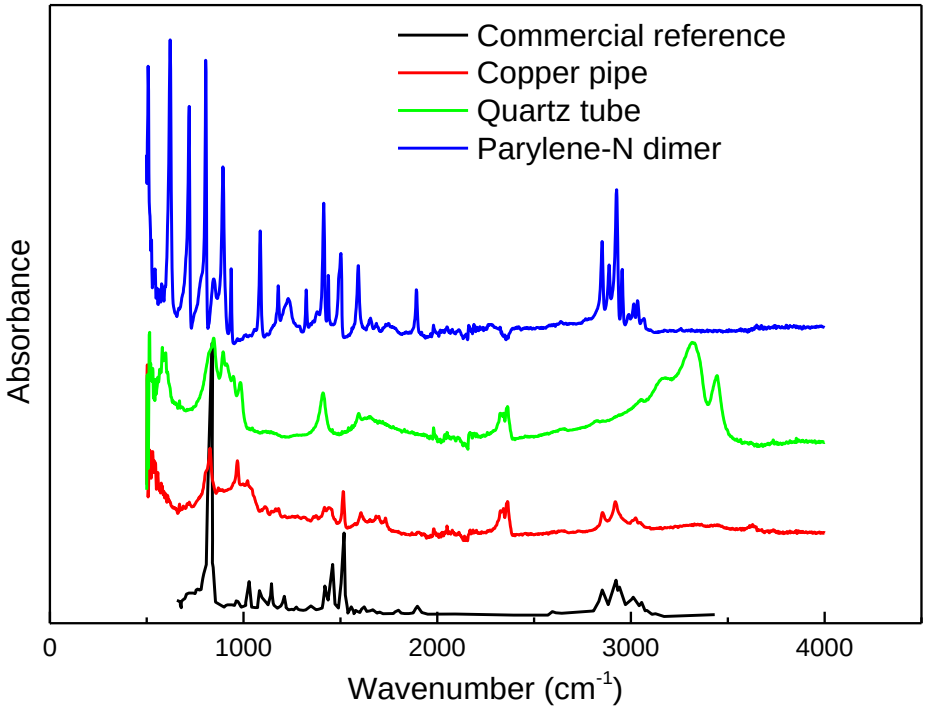


Figure 5-14 IR spectrum of parylene-N purchased from Sigma Aldrich, parylene-N deposited by thermal evaporation and pyrolysis in a copper pipe and a quartz pipe, and parylene-N film via commercially process[20].

5.3.5 Flash Evaporation of Acrylates Containing Long Alkyl Segments

Lauryl acrylate and hexyl acrylate, which both contain long alkyl units, were deposited by flash evaporation and cured by plasma onto a TPGDA coated glass substrate. The cured acrylates, however, proved to be unstable on the substrate: rather than forming a solid film, the layer was a viscous liquid and that could be wiped away by a cotton tip. This was likely due to a lack of curing resulting from the low concentration of acrylic groups in the chain. To compensate for the lack of cross link sites, and thus to achieve a better film stability, a mixture of lauryl acrylate and HDDA (5:1) was deposited by flash evaporation and cured by e-beam in our Oxford vacuum web coater at drum speed of 5 $m \cdot min^{-1}$ (see details in **section 5.2.3**).

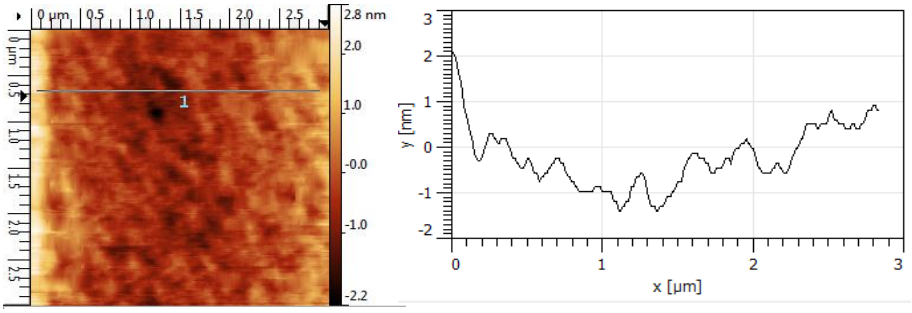


Figure 5-15 AFM topography image of lauryl acrylate plus HDDA (5:1) deposited by flash evaporation cured by e-beam on TPGDA surface on a glass substrate.



Figure 5-16 Contact angle of water on TPGDA on glass and lauryl acrylate plus HDDA (5:1) on a glass substrate.

The resulting film showed an RMS roughnes of about 0.5 nm and homogenous coverage on the surface (**Figure 5-15**) and it was strong enough to withstand wiping with a cotton tip. The film showed a water contact angle of 90°, one week after fabrication

Figure **5-16**), which is much higher than the 60° of the TPGDA substrate. The same values were observed a month after fabrication, indicating that the surface energy of the substreate was changed and maintained by the buffer layer.

Table 5-1 summarises device performances extracted from the transfer characteristics for devices in this batch of samples. It is worth mentioning here that the mobility values in this group were relatively low compared with those in the previous chapter, probably because that the semiconductor deposition was conducted in a different thermal evaporator for which the DNTT deposition parameters were not yet optimised. However, this batch, despite its lower overall mobility, serves as a useful comparitor of the different surface modifications. The transistors with these buffer layers showed

high consistancy of transfer characteristics, even better than spin coated polystyrene (**Figure 5-7** (h)). The transisors, 5 in one batch, had a mobility of 0.44±0.02 $cm^2 \cdot V^{-1}s^{-1}$, *SS* of 1 $V \cdot Dec^{-1}$ and a threshold voltage of less than -4 V.

Table 5-1 summary of transistors performance on TPGDA, LA+HDDA buffer coated HDDA and PS coated TPGDA.

	SS **(V/decade)**	**Mobility** **(cm^2/Vs)**	$I_{on/off}$ **ratio**	**Off current (A)**	V_T **(V)**	V_{to}**(V)**
No buffer	1.6	0.08	10^5	10^{-9}	-5V	-2V
LA+HDDA	1	0.44±0.02	10^5	10^{-9}	-4V	-2V
PS	0.9	0.52±0.1	10^5	10^{-9}	-3V	0V

5.4 Summary

In summary, dielectric surface buffer layers, including polystyrene, TTC, parylene-N and lauryl acrylate were deposited in this work. Among all the buffer layers, only the flash evaporation of lauryl acrylate mixed with HDDA followed by e-beam curing resulted in stable non-polar dielectric surface that improved DNTT transistors' hole mobility fivefold and give consistent device performance. While more work could be done to optimise the deposition parameters and monomer formula, this work has demonstrated this technique as suitable for a roll-to-roll in-vacuum process.

5.5 References

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Chapter 6

Device Stability

6.1 Introduction

Organic thin-film transistors (OTFTs) have been under development for more than two decades[1], however, they have not been put in use in electric products, largely due to their poor stability. For example, pentacene transistors, which are one of the most frequently studied p-type OTFTs, show substantial changes in performance during operation, even in mild conditions. The devices give shifted threshold voltage (V_T) and turn on voltage (V_{to}) under moderate gate bias[2]. They also showed increased sub-threshold slope (*SS*) and increased off current (I_{off}) when exposed to light in air[3]. In addition, hysteresis[4] is usually observed and the mobility, μ, degrades after a relatively short period of storage in air[5]. The major cause for the unstable performance was the low ionisation potential of pentacene, which makes it vulnerable to oxygen in air. In particular, oxidation happens at the 6 and 13 carbon positions of the pentacene molecule[6-7]. By substituting the central carbon ring by a thieno moiety, the ionisation potential of the semiconductor is increased and the reaction sites are blocked. The new semiconductor named, dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) has been reported to show much better stability and long life time in a few papers[5, 8-9]. Such a semiconductor or its derivatives could be the key to open up the general application of OTFTs. In order to explore their possible application, it is crucially important to obtain a detailed understanding of the device performance in different environments and to measure and understand its degradation behaviour. This work investigated the performance of DNTT transistors with the flash

evaporated TPGDA dielectric layer under various measurement conditions in comparison with pentacene in order to a) obtain a comprehensive understanding of DNTT transistor stability during intensive operation, b) to assess DNTT transistors' long term stability over a period of months and c) to evaluate the reliability of flash evaporated TPGDA with buffer layers during storage and operation.

6.2 Experimental

Environmental tests were conducted using a small bell jar vacuum-able chamber (**Figure 6-1**). A sample holder made of a piece of stripboard (also known as Veroboard) was placed in the bell jar and was electrically connected to the outside by a ribbon cable with 14 separated wires via a feed-through on the bell jar's lid. The wires' terminals inside the chamber were soldered to the contact points on the stripboard which were connected to electrodes of the transistors via gold wires, 25 μm thick, and silver paste. The resistance of each contact into the chamber was less than 2 Ohm, which is negligible compared with the transistors s/d resistance mega Ohm. A total of six transistors can be measured in each load.

After wiring up, the whole chamber was placed in a light proving shell. The chamber was evacuated by a rotary pump to a pressure of 10^{-2} mbar within five minutes for vacuum measurement.

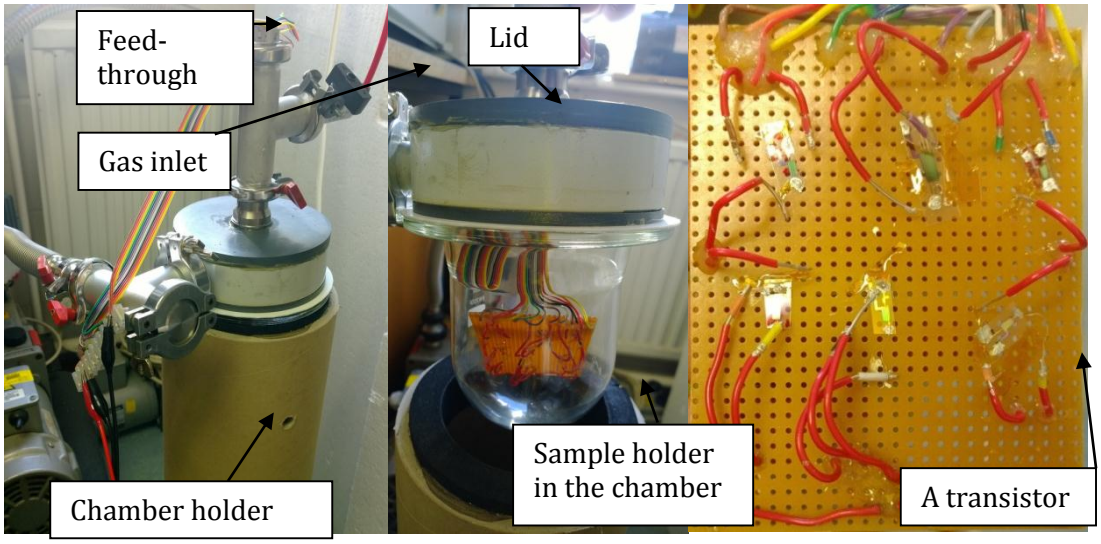


Figure 6-1. Photographs of a homemade measurement chamber and sample holder.

For the dry air measurement, air from a compressor with humidity of less than 5% at 20°C was induced into the bell jar by a gas line. A Lascar EL-USB-1-LCD temperature data

logger with LCD screen was placed in the jar to monitor the humidity and temperature during device measurement.

A damp air environment was achieved by passing the dry air from the compressor through a bubbler filled with water before it entered into the chamber. The humidity in the chamber was controlled by the rate of this air feed and was monitored by the humidity sensor on-line. The humidity range was controllable from 10% to 60% at temperature of 20°C. A relative humidity of about 55% at 20 °C was used for damp air measurements of transistors.

Uncontrolled air measurement was conducted either in the bell jar chamber or on a probe station covered by a light-blocking blanket. The relative humidity of uncontrolled air was within the range of 30%-50 % at 15-25 °C.

Transistor measurements were carried out using two source measurement units (Keithley 2400). The repeating scans were controlled by Labtracer 2.0 software with the gate voltage sweep speed set at 100 ms and 0.7 V per step. The hysteresis sweeps were controlled by a Labview program with the gate voltage sweep speed set at its maximum 0.5 s and 1 V per step. All the transistors, expected for ones indicated, were stored in dry air in the dark for at least two days after fabrication.

6.3 Results and Discussion

6.3.1 Operational Stability

The operational stability of the transistors was characterised by repeating transfer characterisations in different environments. Both pentacene and DNTT transistors with bottom-gate top-contact configuration were characterised in this work.

6.3.1.1 Pentacene Transistors

Figure 6-2, Figure 6-3 shows transfer curves of pentacene transistor with a 20 nm PS buffer layer on a TPGDA dielectric layer 800 nm thick selected from a batch of 5 devices with similar performance. **Figure 6-4** shows transfer curves of pentacene transistors on a PTGDA dielectric layer 800nm thick without PS buffer layer.

The devices were tested in four different environments including vacuum, dry air, uncontrolled air and damp air. The effect of oxygen and humidity, therefore, can be assessed separately, knowing that pentacene OTFTs are inert to nitrogen in air[10].

6.3.1.1.1Effect of Oxygen

Oxygen appears to increase the V_T and I_{on} during repeating measurements. In vacuum (**Figure 6-2** (a)), the 10 transfer cycles were almost identical. The hole mobility at the saturation region was 0.31 $cm^2 \cdot V^{-1}s^{-1}$; the *SS* was 1.5 $V \cdot dec^{-1}$; the V_T was -1 V; the V_{to} increased slightly from 6 V to 7 V with repeating measurements and the $I_{on/off}$ decreased from $1 \cdot 10^6$ to $5 \cdot 10^5$. When dry air of relative humidity 5% was introduced into the measurement chamber at atmospheric pressure, the V_{to} started to shift (**Figure 6-2** (b)) from 6 V towards 10V during the ten measurement cycles. The V_T, however, only increased slightly from -2 V to -1 V. The *SS* increased slightly from 1.5 $V \cdot dec^{-1}$ to 1.8 $V \cdot dec^{-1}$. The μ and the $I_{on/off}$ did not change.

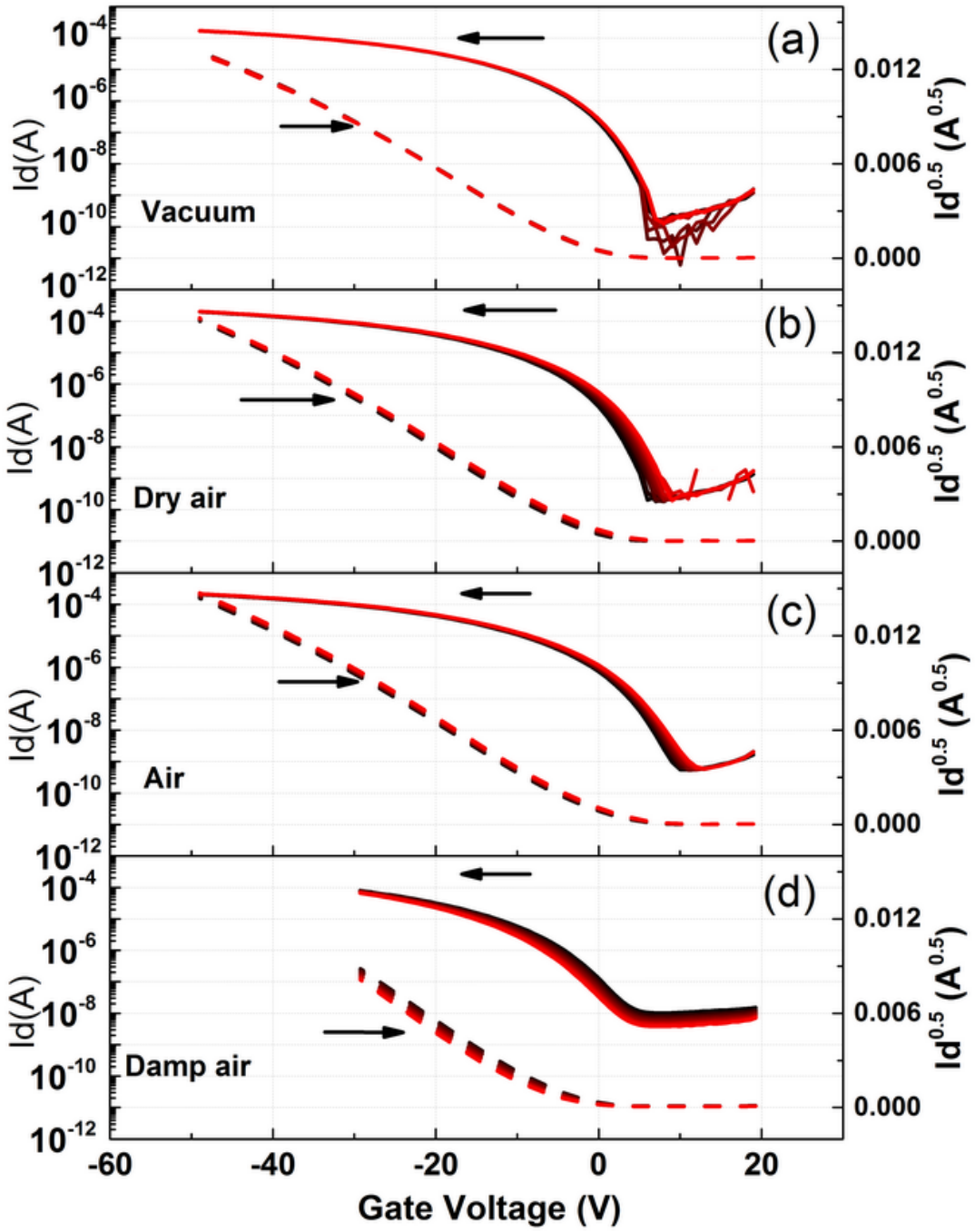


Figure 6-2 Transfer curves of 10 repeat measurements (indicated by solid lines from black to red) of a pentacene transistor with PS buffered TPGDA dielectric layer measured in (a) vacuum of 10^{-2}mbar, (b) dry air of 5% relative humidity at 20°C, (c) uncontrolled air of 30-50% relative humidity at 20 °C and (d) kept in damp air of 50-60% relative humidity at of 20 °C overnight measured in 50-60% relative humidity at of 20 °C.

The observed increase of V_{to} in air accorded with reports by the Han[11] group and the Knipp[3] group. They indicated that oxygen in air interacted with pentacene to create acceptor-like (electron) traps that shifted the onset (turn on) voltage and increased the *SS*. The trap density can be estimated by calculating the voltage difference between flat band and the V_{to} according to the equation used by Knipp, which is also discussed in **Chapter 2, Section 2.2.2**:

$$N_{area} \approx \frac{V_{onset} - V_{fb}}{q} \cdot C_G \tag{16}$$

where the V_{onset} is the turn-on voltage, V_{fb} is the flat band voltage, q is the elementary charge, C_G is the capacity of dielectric film.

Based on the result in this work, it is estimated that the oxygen-induced acceptor-like trap density in the pentacene transistor was about $\sim 10^{11}$ cm^{-2} by taking the value of the V_T as the flat band voltage. This trap density value is similar to that found in Ref. 3 for device with a hexamethyldisilazane (HMDS)-treated silicon oxide dielectric layer.

Interestingly, the degradation behaviour in dry air or laboratory air was observed only when the devices were subjected to high operational current. The device stored in dry air in the dark showed no obvious shift in the V_{to} over a period of a few weeks. In addition, devices that were not operated at high current, e.g. pentacene on PS operating in low voltage (**Figure 6-3**) or transistors with pentacene on TPGDA (**Figure 6-4** (b)) were affected to a much smaller extent: a shift in V_{to} of 0.5 V and 0.1 V compared with the 3 V shift of a device operated at large current (**Figure 6-2** (b)). The device was also put under gate bias stress of -30 V for several minutes, without applying a drain voltage. The performance was not affected. This excluded the possibility that the shift resulted from the dielectric layer being under bias, leading e.g. to charge injection, or slow polarisation. Therefore, it is likely that oxygen reacts with the pentacene transistor when it is

activated during hole transportation. A similar effect was found in pentacene transistors measured in air under illumination, which, in a similar way as high current, could lead to large number of charge carriers in the semiconductor layer. Despite operating within a low current range (**Figure 6-5** (a)), the device under illumination showed significant degradation over 10 measurement cycles. In contrast, in the absence of oxygen, (**Figure 6-5** (b,c)), the same device showed no operational degradation under light.

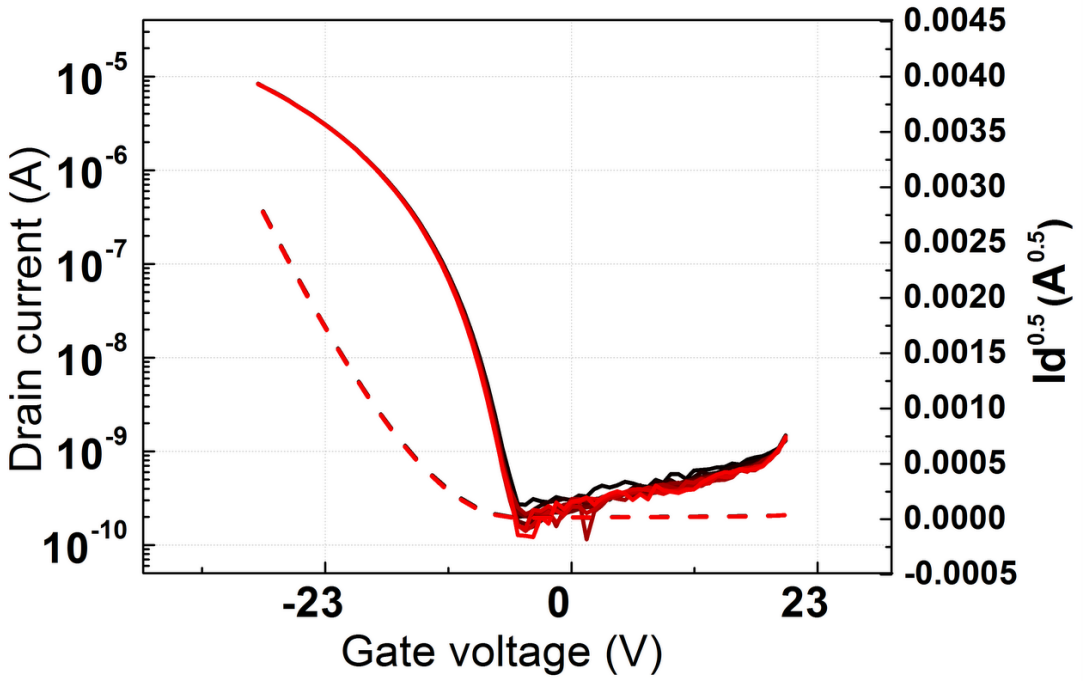


Figure 6-3 Transfer characteristics (indicated by solid lines from black to red) of a pentacene transistor with PS buffered TPGDA dielectric layer measured in air in the dark under relatively low gate voltages.

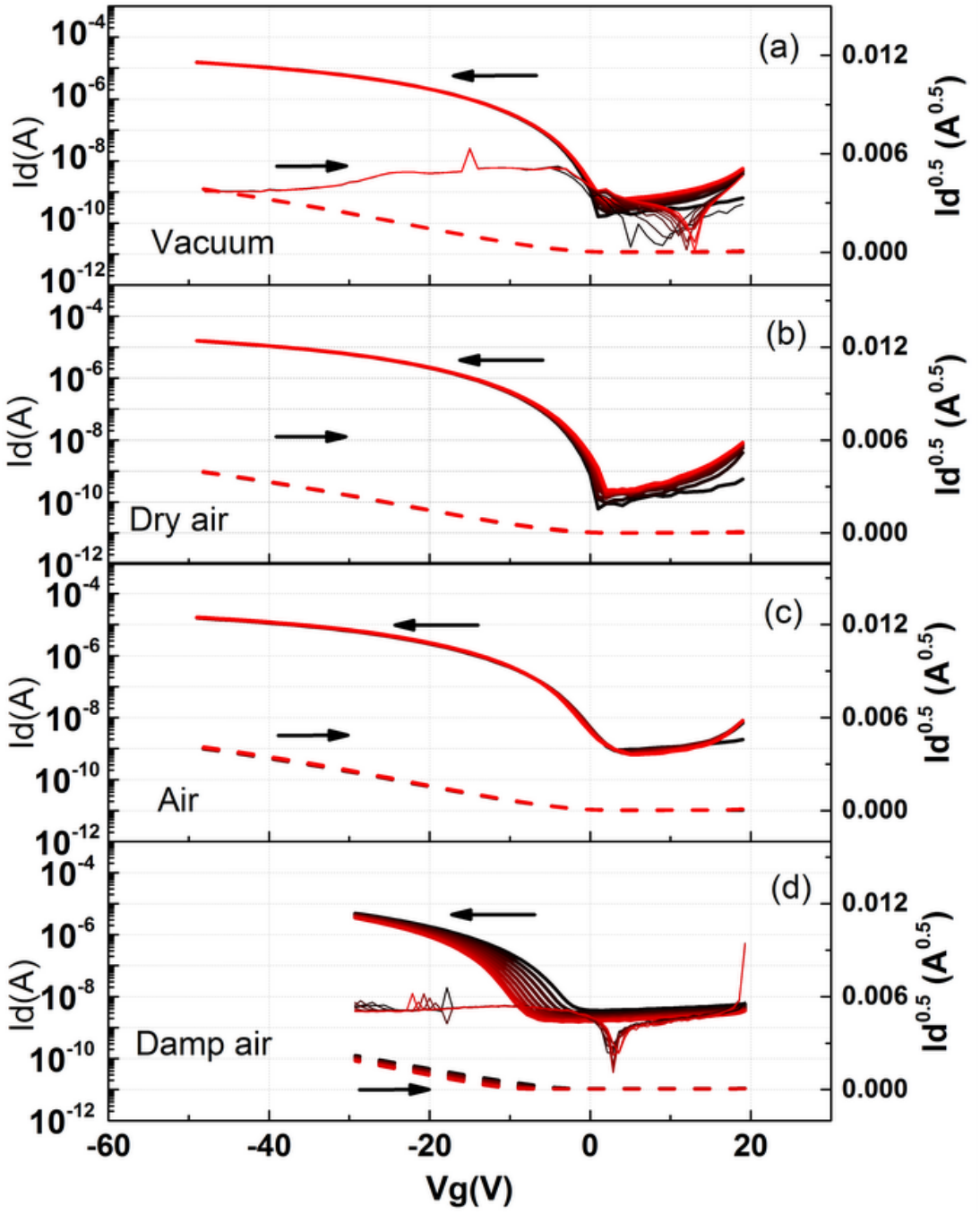


Figure 6-4 Transfer curves of a pentacene transistor on TPGDA measured in 10 repeat gate voltage sweeps (indicated by solid lines from black to red)) in (a) vacuum of 10^{-2} mbar, (b) dry air of 5% relative humidity at 20°C, (c) air of 30% relative humidity at 20 °C and (d) damp air of 50-60% relative humidity at of 20 °C. The red solid lines in (a) and (d) show the gate-source (gate leakage current) during transfer measurement.

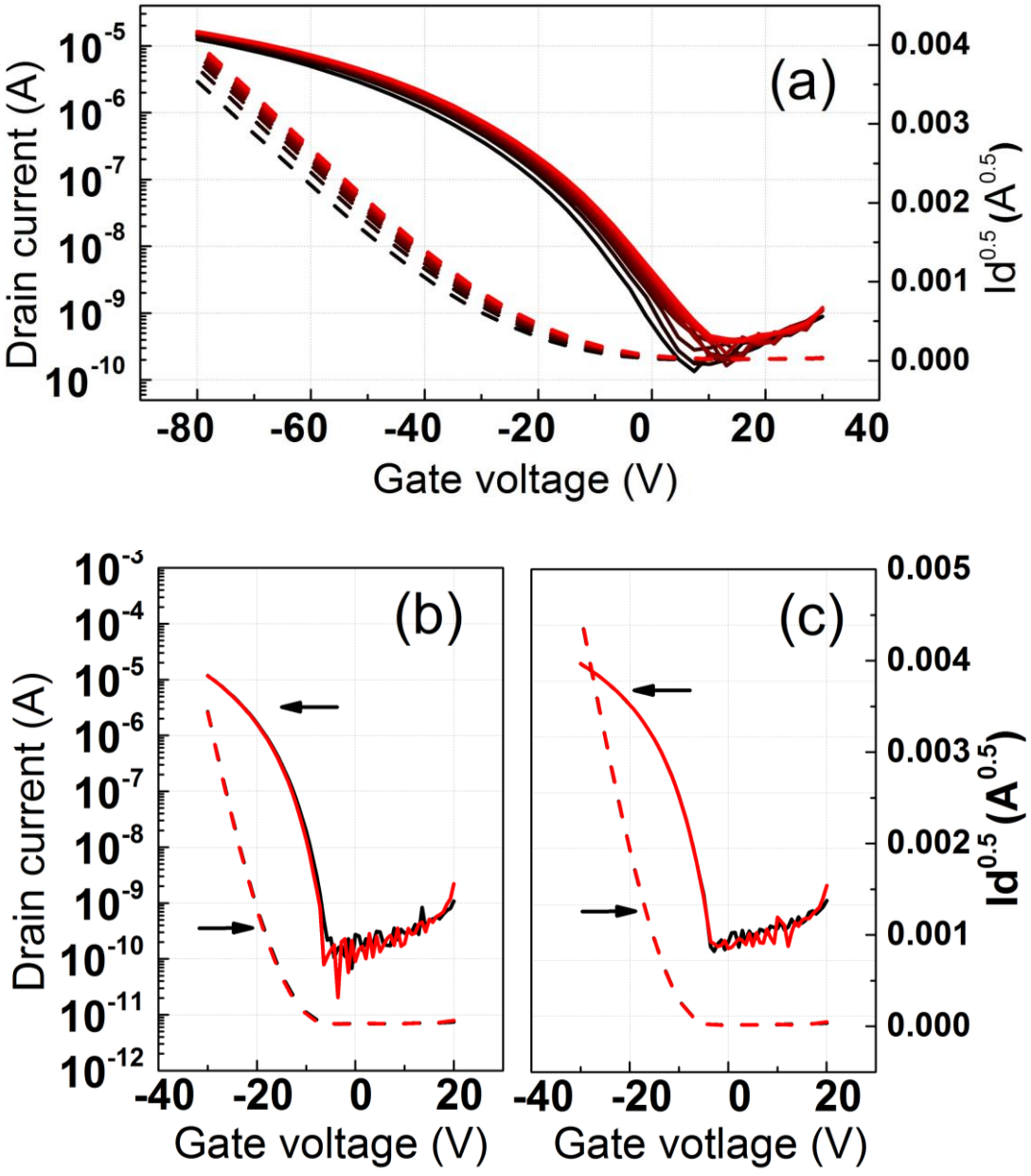


Figure 6-5 Transfer curves of a pentacene transistor on a TPGDA dielectric layer measured over 10 repeating gate voltage sweeps (indicated by solid lines from black to red) in (a) ambient air under laboratory light; (b) in the dark in vacuum; (c) under lab light in vacuum.

6.3.1.1.2 Effect of Moisture

In a relatively low humidity (30-50%) environment, the device showed a similar deterioration trend as in dry air (**Figure 6-2** (c)). The V_{to} increased further than in the

case of dry air (10 V) to 12 V, the V_T increased slightly from 0 V to 1V, the *SS* increased to 2.8 V·dec^{-1} after the 10 measuring cycles. The I_{off} increased threefold compared with the dry air measurement.

A higher concentration of water, 50%-60% relative humidity, seemed to affect the device in a somehow opposite manner. After keeping the devices in damp air overnight without measurement (**Figure 6-2** (d)), the transfer curves shifted to lower potential: the V_{to} moved back from 12 V to 5 V, V_T decreased from -1 V to -4.5 V. In addition, the turn-on of the device was softened: the *SS* increased substantially to 5.6 V·dec^{-1} from the value of 2.8 V·dec^{-1}; and the I_{off} increased tenfold. When repeat measurements started, the I_{off} reduced threefold and the square root of the transfer curves shifted further to the left: V_T moved from -4.5 V to -7.5 V within ten cycles. Although the V_{to} was not changed, the transfer curves appeared shifted to the bottom, i.e. the increase in drain current (I_d) was suppressed. In the meantime, the *SS* and the hole mobility were not affected by the repeat measurements.

Regarding the negative shift of the V_{to} and V_T in **Figure 6-2** (d) induced by humidity, it has been reported that the polar nature of water induces donor-like traps at either the grain boundaries[11-13] or within the crystal lattice[14] in pentacene. These traps immobilise hole carriers in the conductive channel between source and drain, thus leading to suppression of I_d and negative shift of V_T. The observation in **Figure 6-2** (d) accorded with this literature.

To check whether the dielectric surface affects the device behaviour in both dry air and damp air, a device without a PS buffer layer was tested under the same environments (**Figure 6-4**). The same trend was observed in the transistors. The only difference was that the TPGDA pentacene without the PS buffer device gave higher extent of shift (**Figure 6-4** (d)) when measured in damp air, which could apparently be explained by

the greater hydrophilicity of the TPGDA surface compared with that of PS[8]. This also suggested that the water at the dielectric-semiconductor interface is affecting the device behaviour.

It is worth mentioning the high starting I_{off} in **Figure 6-4** (d) and **Figure 6-2** (d) in damp air. The I_{off} was almost tenfold greater than that in dry air, and it decreased with repeating measurements. The increased I_{off} was recoverable if the device was measured in dry air or in vacuum again. It is likely that the water absorbed loosely by the device resulted in an ionic current which was responsible for the increased I_{off}. The decrease of the ionic current with repeating measurements could possibly be due to reduction of ion density in the channel due to applied potential. The work also confirmed that the gate leakage was low during the repeating measurements (**Figure 6-4** (a)(d)).

6.3.1.1.3 Summary

It can therefore be concluded that water and oxygen have distinctive effects on devices. Water leads to increase of I_{off} and, at the same time, prevents the I_d being switched on during operation due to donor-like traps (**Figure 6-6** right). The increased I_{off} could be due to ionic currents between source and drain. In contrast, the oxygen tends to move the transfer curve to more positive potentials due to generation of acceptor-like charge traps (**Figure 6-6** left). Light enhanced the generation of such acceptor traps.

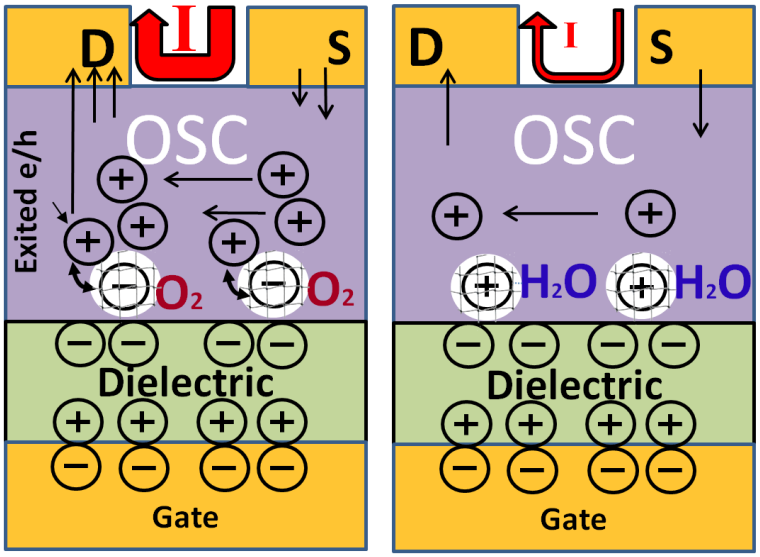


Figure 6-6 Schematic illustration of how, during transistor operation, oxygen-induced acceptor-like (electron) traps increase I_d in the semiconductor layer, and water induced donor-like (hole) traps at the conductive channel area, trap holes from the drain, decreasing I_d .

6.3.1.2 DNTT Transistors

Transistors with DNTT as the semiconductor were measured in vacuum, dry air, air, humid air, vacuum with illumination and air with illumination. Therefore the oxygen, water and illumination effect on transistor during operation was separated. The devices have been stored in dry air in the dark for few weeks before the measurements.

6.3.1.2.1 Effect of Oxygen

The performance of a representative transistor with PS-buffered TPGDA dielectric layer is presented in **Figure 6-7**. A constant V_{to} of 0V, V_T of -2 V and mobility of 1 $cm^2 \cdot V^{-1}s^{-1}$ is recorded for devices measured in vacuum. The sub-threshold swing, instead of degrading, decreased from 0.60 $V \cdot dec^{-1}$ to 0.43 $V \cdot dec^{-1}$ with repeating measurement of 30 cycles within about 15 minutes. The device was also relatively stable, in contrast to pentacene, in air (**Figure 6-7** (b)): only a small increase of V_{to} of 0.7 V and an increase of sub-threshold swing from about 0.62 $V \cdot dec^{-1}$ to 0.81 $V \cdot dec^{-1}$ were observed within the first two operating cycles. The performance of the devices over 3-10 cycles was constant.

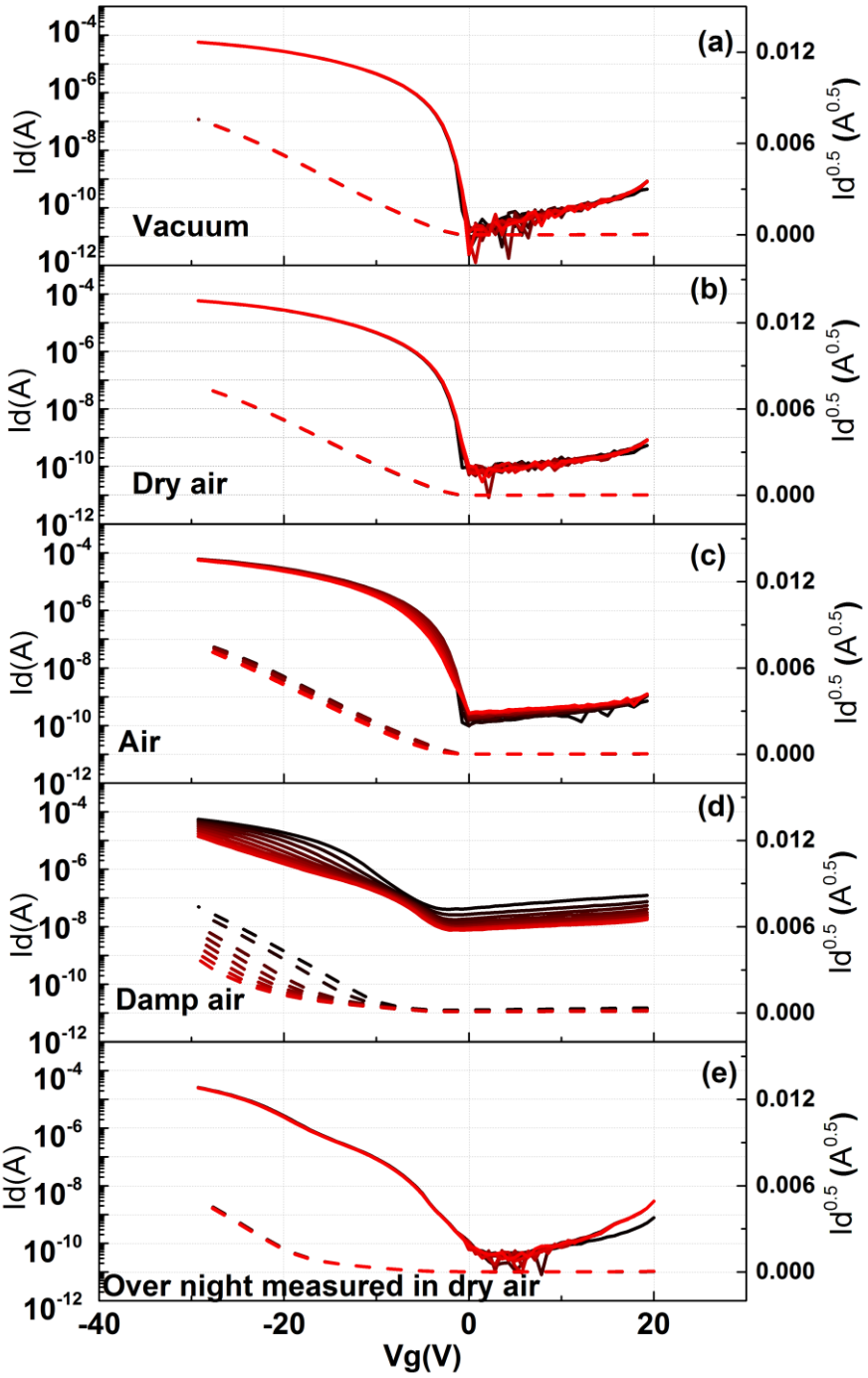


Figure 6-7 Transfer curves of 10 repeat measurements (indicated by solid lines from black to red) of a DNTT transistor with PS buffered TPGDA dielectric layer measured in (a) vacuum of 10^{-2} mbar, (b) dry air of relative humidity of 5% at 20°C, (c) air of relative humidity of 30% at 20 °C and (d) damp air of relative humidity of 50-60% at of 20 °C and (e) measured again after in vacuum for two hours plus stored in dry air over night.

6.3.1.2.2 Effect of water

Degradation was found when a device was measured in uncontrolled air with relative humidity of about 30% at 20°C (**Figure 6-7** (c)): the I_{off} increased fivefold, while the on-current decreased by 20%. The V_T of the device shifted from -2 V to -4 V. The sub-threshold swing increased from 0.63 V·dec^{-1} to 1.47 V·dec^{-1}.

Severe changes were observed when the relative humidity increased to 55 %: the transfer curve was distorted and shifted to the left after about 40 measurement cycles; the last ten cycles are presented in the **Figure 6-7** (d). The square-root of the transfer curve moved leftwards significantly, leading to a V_T shifted to a value as negative as -20V. Such a shift was not recovered after leaving the device in vacuum for two hours and then in dry air overnight in the dark (**Figure 6-7** (e)). Despite all the changes that happened, the saturation mobility of the device was stable under all conditions in **Figure 6-7**.

Water in organic transistors has been studied previously. Except the mechanisms that have been discussed in the **section 6.3.1.1** for pentacene, i.e. ion conduction and donor-like traps, there are two other possible ways the device can be affected. The first, reported by Li[12], Richard[15] and Park[10], was that water exists at the interface between source/drain and semiconductor, forming charge carrier traps. Trapped holes built up with time and ultimately lead to an injection barrier from metal electrode to semiconductor. This, however, is probably not the case in the transistors measured here, since by swapping the I_d direction the suppression of the current is still found to be at the same level, which disproved the presence of traps and accumulated holes near the source that only should affect carrier injection in one direction. The second mechanism, offered by Park[10] and Noh[4] is that water at the interface of dielectric and semiconductor layer forms dipoles that reorientate with gate bias and lead to clockwise hysteresis for transistors. In our case, however, such hysteresis was only observed in very few cases under very high humidity. Anti-clockwise hysteresis, in contrast, was more frequently

found in samples measured in damp air and uncontrolled air (**Figure 6-8**) which is consistent with the decreasing I_d with repeating measurement in **Figure 6-7** (d). Therefore the phenomenon of suppression of I_d in damp air was probably not due to the dipole orientation of water molecules at the dielectric surface. Accordingly, the donor-like traps, brought about by water molecules in the semiconductor, and ionic conductivity are the major causes for the changes of transistor behaviour.

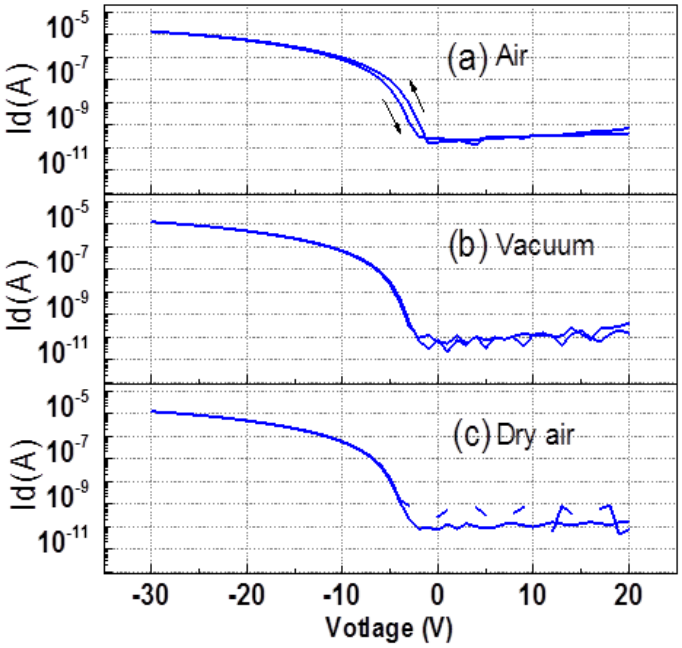


Figure 6-8 Transfer characteristics of a DNTT transistor measured in (a) uncontrolled air, (b) in vacuum of 10^{-2} mbar, (c) in dry air of 5% humidity at 20°C in the dark.

6.3.1.2.3 Effect of Illumination

Illumination and vacuum

Transistors with a PS buffer layer on TPGDA dielectric were measured in vacuum with illumination. The behaviour of a typical transistor is shown in **Figure 6-9**. Except for an

instant increase of 20 % in the on-current and a minor shift of V_{to} from -1V to 0V, the transfer characteristics were the same as those measured in the dark. No degradation was observed with repeating measurements. These minor changes disappeared immediately after the device was placed in the dark again.

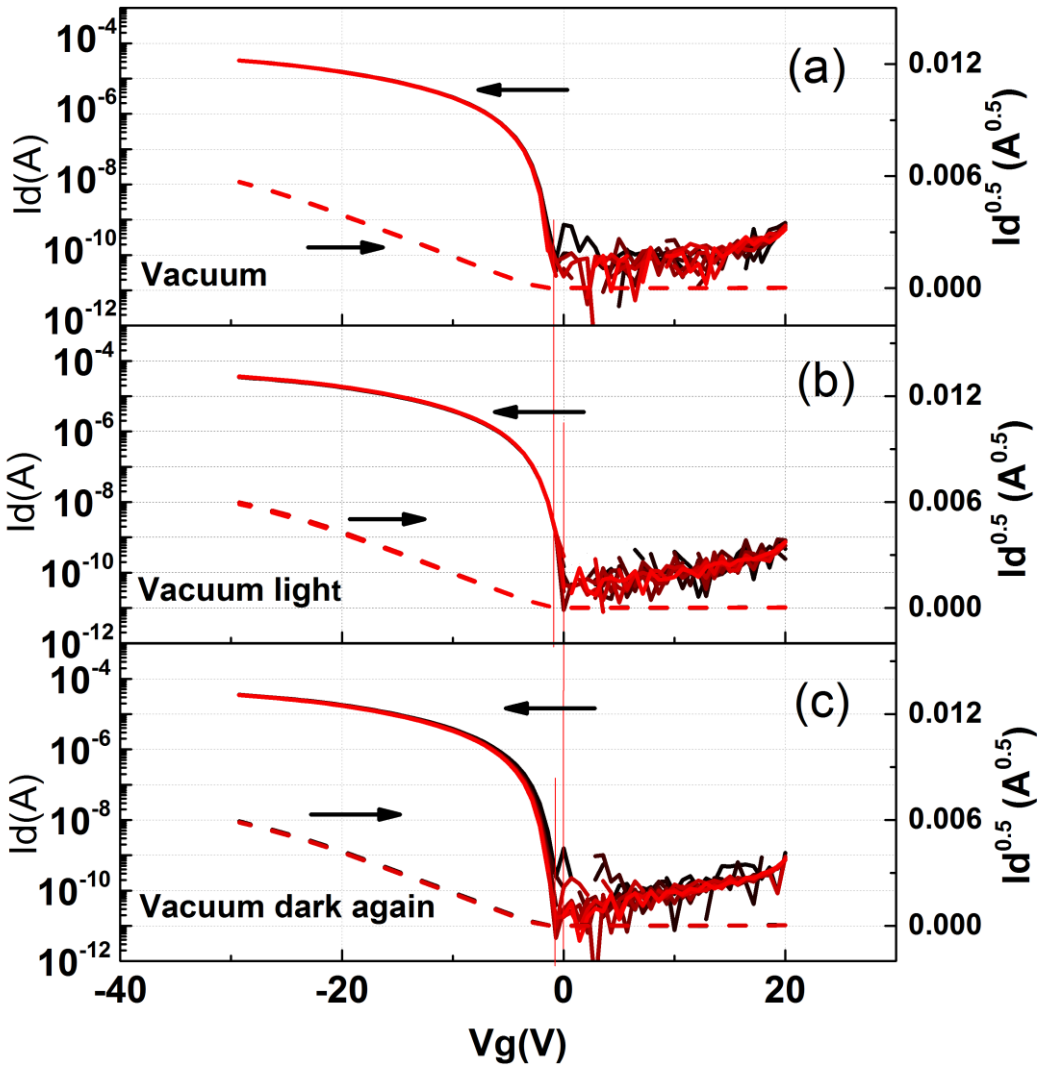


Figure 6-9 Transfer curve of DNTT transistor with PS buffer layer on flash evaporated TPGDA dielectric measured in vacuum in the dark (a), vacuum under illumination (b), and dark (c) again.

Illumination and dry air

The same illumination experiment was conducted in dry air (**Figure 6-10**), on the same device. The V_{to} shifted instantly from 3 V to 5 V with illumination, then it gradually shifted further to 8 V with repeating measurement (**Figure 6-10** (b)). The increased V_{to} was reduced to 6 V and stabilised immediately when the devices were moved back into the dark in dry air (**Figure 6-10** (c)). When this device was then measured under vacuum, a very small recovery in V_{to} of about 0.5 V was observed after the first five minutes in vacuum of 10^{-2} mbar (**Figure 6-10** (d)). After 2 hours of evacuation the transfer curves fully recovered back to their state before illumination (**Figure 6-10** (d)).

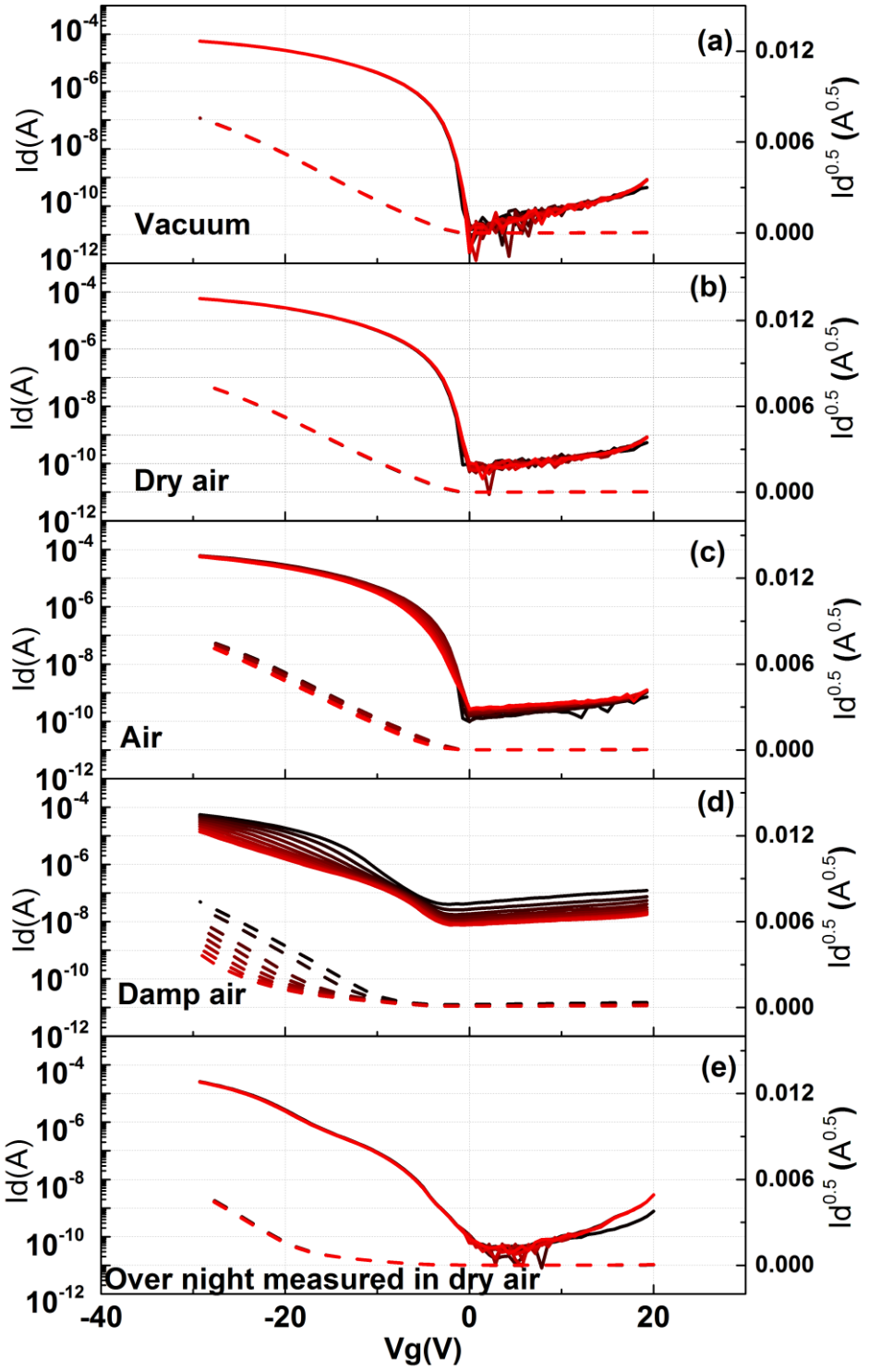


Figure 6-10 Transfer characteristics of a DNTT transistor on PS buffered TPGDA dielectric measured in repeat gate sweeps (indicated by solid lines from black to red) under (a) dark dry air, (b) dark with illumination, (c) dry air in the dark, (d) vacuum in the dark for 5 minutes, (e) vacuum in the dark for 2 hours.

Illumination and damp air

Transistors were also measured under light in damp air. Interestingly, illumination appears to be able erase the degradation of DNTT device observed in a damp atmosphere. **Figure 6-11** showed a transistor measured repeatedly in uncontrolled air with relative humidity between 30%-50%, at 20 °C. The device was measured on a probe station under a light-blocking black blanket. Similarly to the device characteristics shown in **Figure 6-7** (c) and (d) the device I_d decreased with repeating measurements, while after exposure to illumination for less than five minutes the I_d increased back to an even higher level. In contrast to the **Figure 6-7** device, the V_{to} shifted gradually with repeating measurements and finally reached 10 V after exposure to light. The shift in the dark measurements could possibly be because of un-blocked light from the edge of the blanket, given the blanket cover was not as effective as the enclosed measuring chamber. The exposure time during transistor handling and probe alignment could also contribute to the shift.

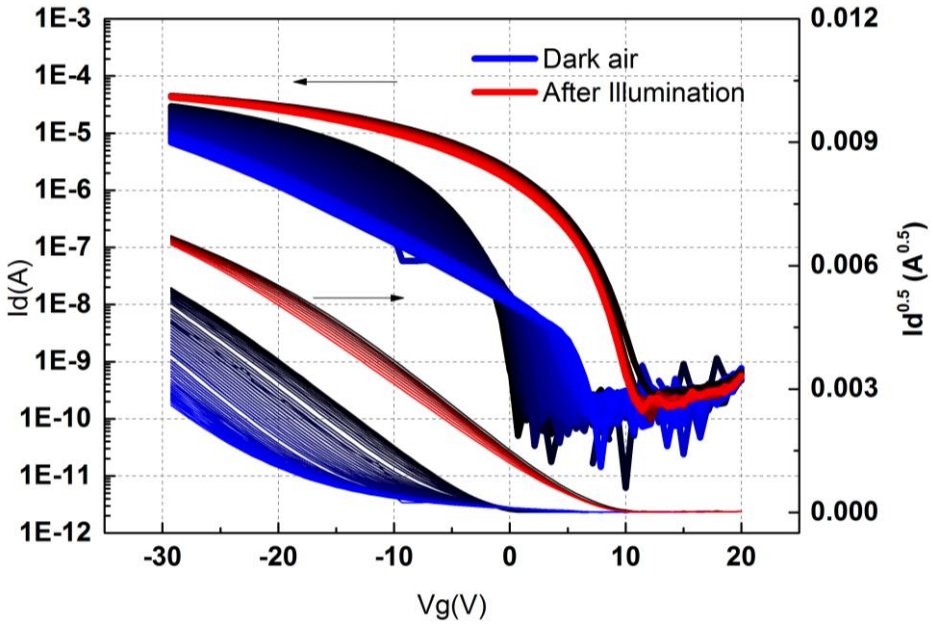


Figure 6-11 Transfer characteristics of a DNTT transistor on TPGDA dielectric with PS buffer layer, measured in air in the dark for 60 cycles (indicated by solid lines from black to blue); measured after exposure under laboratory light for 5 minutes, 10 cycles (indicated by solid lines from black to red).

When the devices were illuminated in damp air, almost no degradation was observed during the repeating measurements. **Figure 6-12** shows two groups of devices made on a TPGDA surface without any buffer layer. The device measured in damp air under laboratory light showed constant transfer curves while that measured in the dark degraded significantly.

Three groups of transistors with a lauryl acrylate dielectric buffer, a PS dielectric buffer and no buffer on TPGDA were also measured in dark and light (**Figure 6-13**). In each case, the devices measured in light for two repeat cycles showed straighter square root of transfer curves and slightly shaper turn-on. The V_T and V_{to} of the transistors measured in light were less negative than those in the dark. The transfer curves were constant within two measuring cycles under light, while those measured in the dark showed quite obvious leftwards shift.

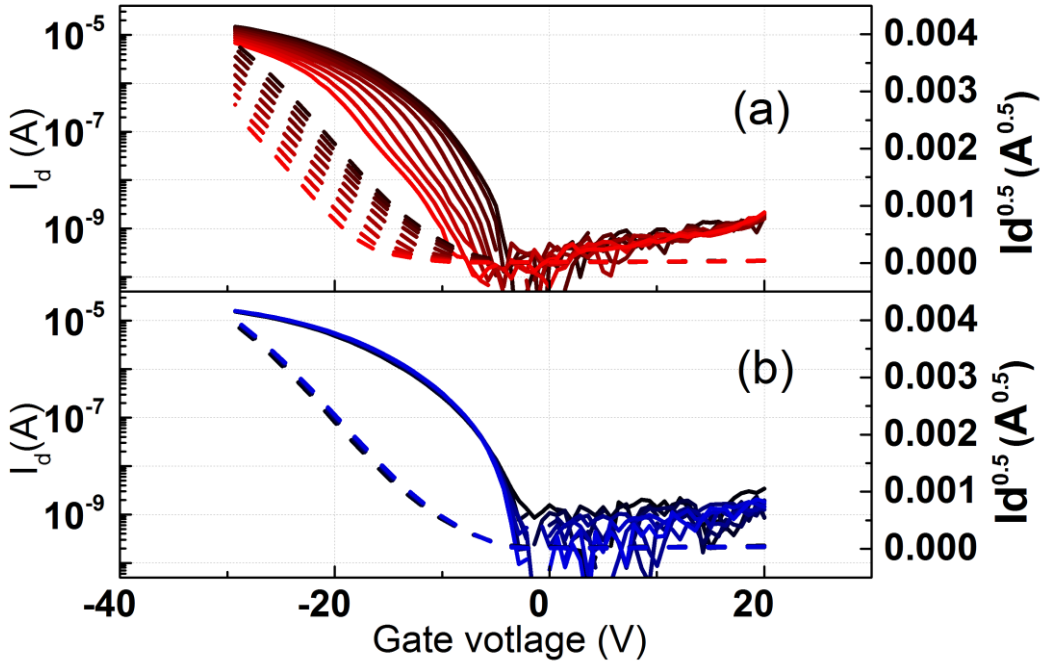


Figure 6-12 Transfer characteristics of a DNTT transistor on TPGDA dielectric with no buffer layer, measured under repeating gate voltage sweeps (a) in air in the dark (indicated by solid lines from black to red) and (b) in air under laboratory light (indicated by solid lines from black to blue).

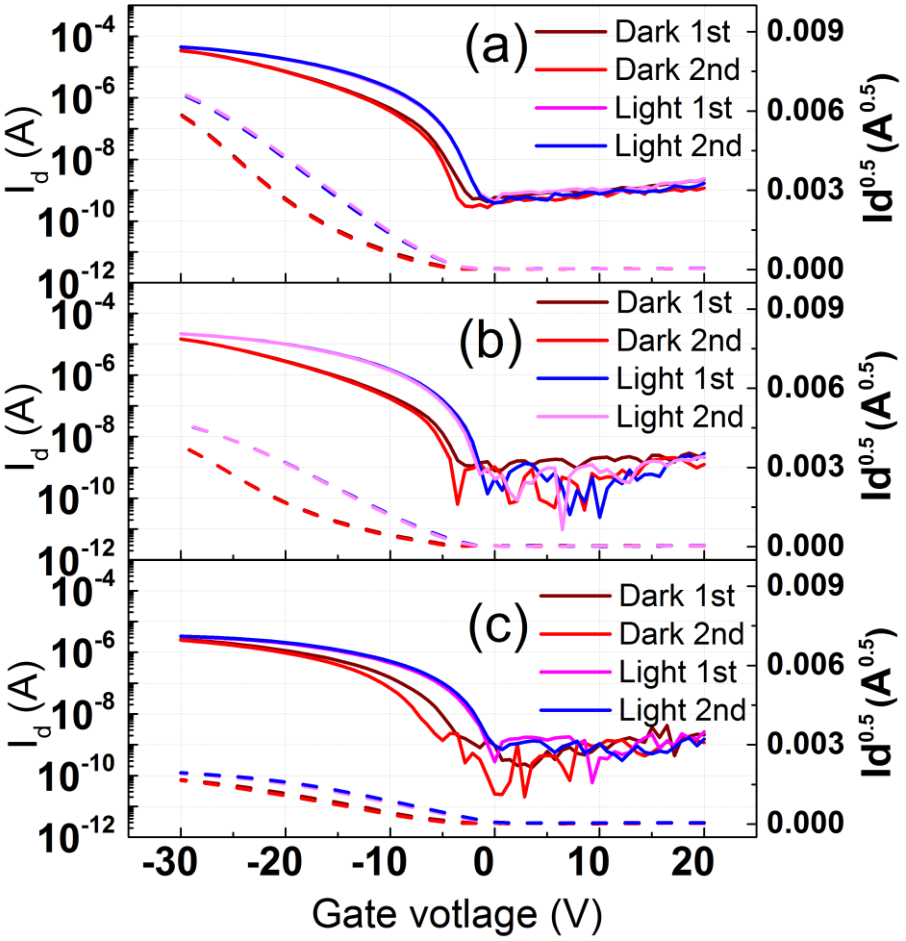


Figure 6-13 Transfer characteristics of three groups of DNTT transistors with (a) PS buffer layer, (b) flash evaporated lauryl acrylate dielectric layer and (c) no buffer layer, measured in the dark and under light in air. Each blue line represents an individual transistor measured in light, and each red line represents an individual transistor measured in the dark.

Discussion of the effect of light illumination

Three types of effect of illumination on organic transistors have been found in the literature, including photo-assisted oxidation[13,14], photoconductive behaviour and photo-voltage behaviour[16].

Photo-oxidation leads to disintegration of semiconductor molecules and thus significant reduction of charge carrier mobility[17]. However, this was not observed for the DNTT devices during either the repeating measurements or during the long term

environmental testing discussed in **section 6.3.2.2**. The molecular design, i.e. substitution of the central carbon ring by a thieno moiety is effective in preventing photodegradation.

Photoconductive behaviour, which is due to photo-generated mobile carriers, i.e. holes in our case, would lead to an immediate increase of I_d over the gate voltage sweep range. **Figure 6-9** shows an instant increase of on current for devices measured under illumination in accord with the photoconductive behaviour, and a quick recovery when the devices are returned to the dark.

The photo-voltage behaviour, due to photo-generated electrons accumulated and trapped near the interface of semiconductor and dielectric layer, leads to a much greater increase of on current and a shift of V_{to} and V_T. This could explain the behaviour found in **Figure 6-10**, a device measured in dry air under light. The much smaller change in devices measured in vacuum under light suggested that such an effect in these devices was associated with oxygen. It is assumed that the oxygen doping, either physical or chemical, in the DNTT with assistance of illumination leads to a higher concentration of acceptor-like trap states for electrons (**Figure 6-6** (left)), and therefore leads to a much stronger slow response of photo-voltage behaviour i.e. shift of V_{to} with repeating measurement under light. In the case of damp air with illumination, the hole traps induced by water were cancelled out and overwhelmed by the opposite electron traps induced by illumination and air, hence constant transfer behaviour with repeating measurement with small shift of V_{to} was observed in some devices.

6.3.1.2.4 Bias Stress Test

A bias stress test was conducted on a DNTT transistor with PS buffered TPGDA. A V_g of -30 V and V_d of -20V (i.e. linear region and I_d fully turned on) were applied to the device for 12 hours in vacuum. A 15% increase in on-current was observed (**Figure 6-14** (a))

during the course of the stress. The device's transfer characteristics were measured immediately after the bias test (**Figure 6-14** (b,c)). Except for a shift by 2 V of V_{to}, the transfer behaviour was the same as before the stress. The stress test was conducted on the same device again in dry air for 15 hours. A 25% current increase was observed; the transfer characteristics shifted a further 3 V to more positive potential (**Figure 6-15**). Although such a shift did not recover after one day "cooling down" in vacuum, two weeks later, after storage in dry air, the shifted V_{to} recovered (**Figure 6-16** (a)). The mobility of the device remained the same for all the measurements.

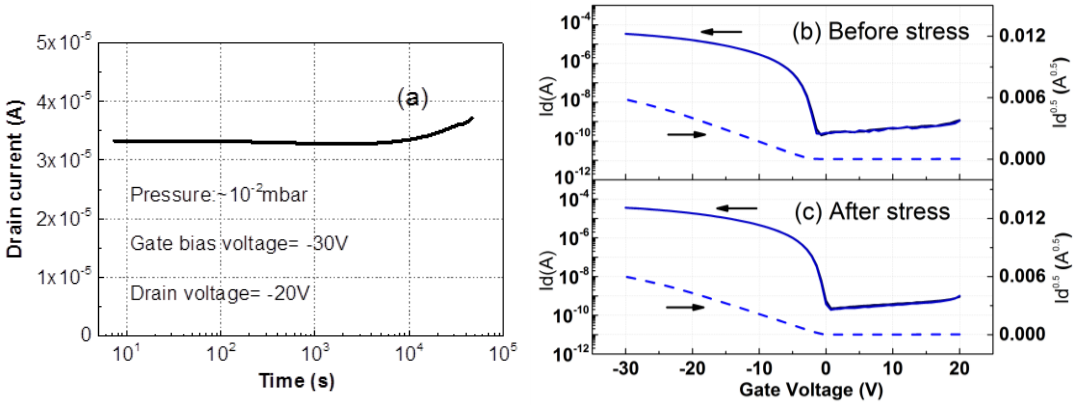


Figure 6-14 (a) I_d of a DNTT transistors with PS buffer layer under bias in vacuum in the dark for 12 hours, and transfer characteristics of the transistor before (b) and after (c) the bias stress.

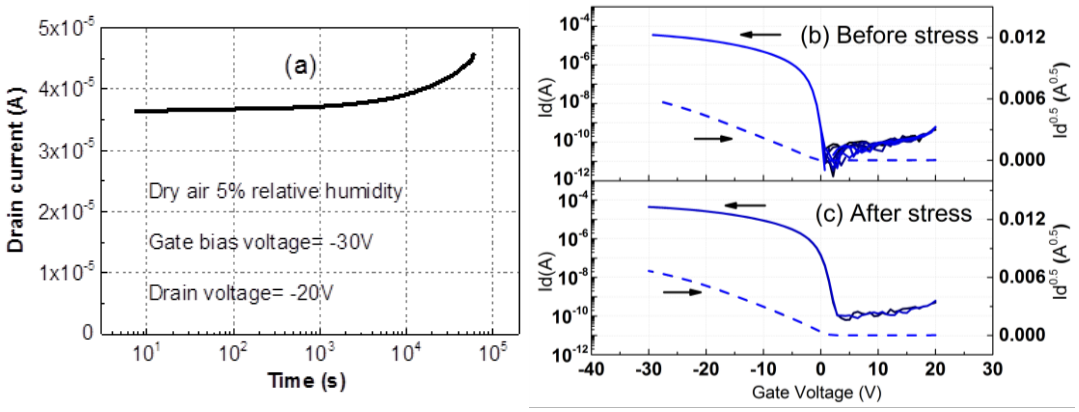


Figure 6-15 (a) I_d of a DNTT transistor with PS buffer layer under bias in dry air in the dark for 15 hours, and transfer characteristics of the transistor before (b) and after (c) the bias stress.

This observed device behaviour under long-term bias, i.e. a) increased on current with bias, b) constant mobility before and after bias and c) recoverable transfer characteristics after bias, has not previously been reported in the literature. Similar work was done by Zschieschang[5] on DNTT transistors with a SAM treated alumina as the dielectric layer. In contrast to the increase of I_d observed in this work, they reported that I_d started to reduce after an hour of bias stress and became 70% of the original after 24 hours. The devices also showed degraded *SS* and shifted threshold voltage. No recovery was observed after several days' relaxation.

The recovery time of gate bias induced shift, which could be weeks, was much longer than those from repeating measurements (**section 6.3.1.2.2** and **section 6.3.1.2.3**), which was hours according to **Figure 6-10**, indicating the origin of the shift was different.

To find out the cause for the V_{to} shift during bias stress, a bias of -30V was applied between the gate and source but the drain was left floating (**Figure 6-16**). Hence, no I_d was running between source and drain, so there was no charge carrier trapping. After 12 hours in air, the device's transfer characteristics shifted significantly to the more positive

potential by about 6 V, the sub-threshold swing increased from 0.59 V·dec^{-1} to 1.19 V·dec^{-1} which was even more significant than that due to bias with current flowing. After the negative bias, a reversed gate voltage of +30V was applied with the drain still kept floating. The opposite stress shifted the V_{to} to more negative potential and the transfer curves were slightly distorted. This indicated that factors originating from the electric field, including slow polarisation of dipolar groups in/on the dielectric layer, and/or charge injection from the gate into the dielectric layer were involved in the bias stress behaviour. On the other hand, the charge carrier accumulation and trapping processes, which are associated with current flow in the conductive channel, were less likely to be the cause for the V_{to} shift in bias test. At this stage, it is difficult to differentiate the exact cause of the shift between the charge injection and the slow polarisation mechanisms.

To test the limitation of the device operating time under bias, the same transistor was measured with a slightly lower gate voltage of -20 V and drain voltage of -20 V for 144 hours in dry air in the dark (**Figure 6-17**). Although I_d was doubled during the bias stress, there was no sign of degradation on the device performance. The gate leakage and I_{off} were kept very small. The V_{to} shifted moderately to 2.8 V, and showed the trend to recover after storage in dry air. The mobility of the transistor was the always the same before and after the test. The device also showed very similar *SS* before and after bias.

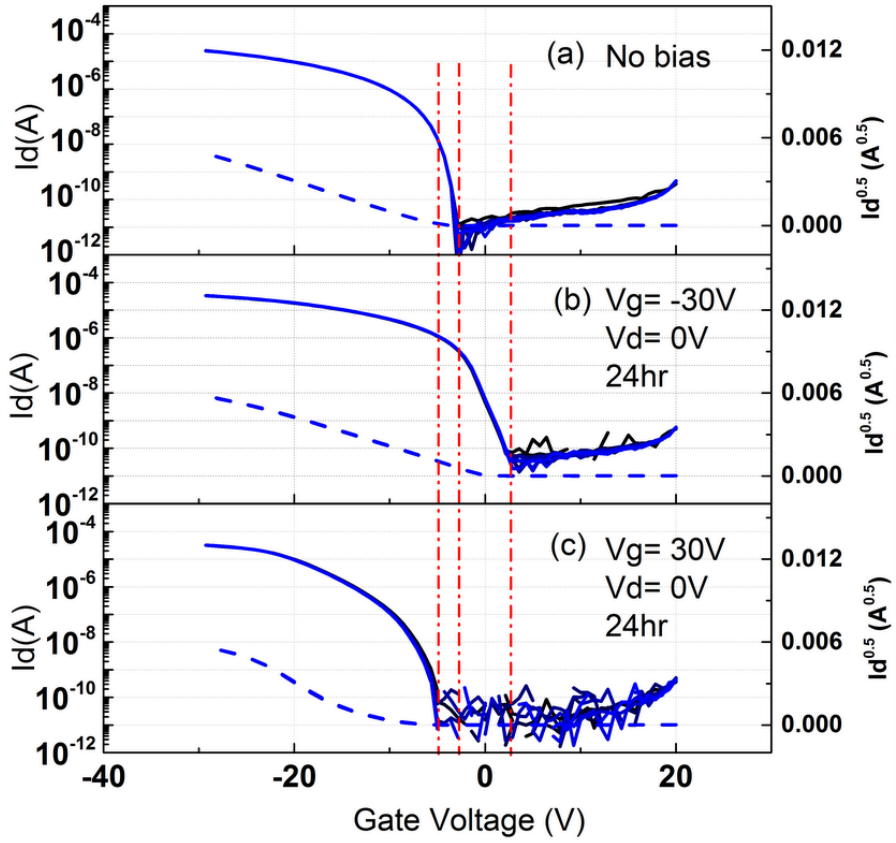


Figure 6-16 Transfer characteristics of the DNTT transistor with PS buffer layer measured (a) before negative bias, (b) after negative bias of 12 hours and (c) after positive bias of 24 hours with drain floating.

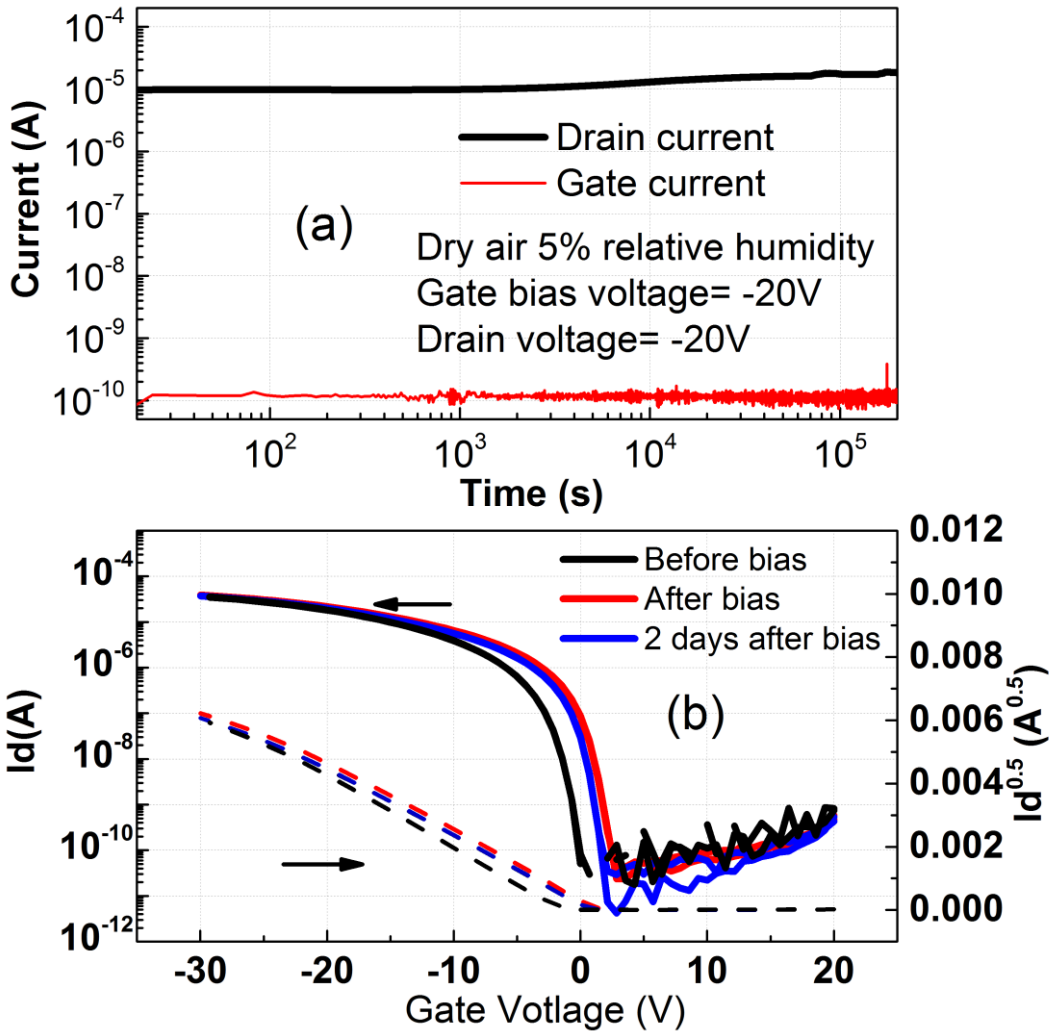


Figure 6-17 (a) I_d and gate leakage current of the transistor measured under bias for 144 hours in dry air; (b) transfer curves of the transistor measured before bias, immediately after the bias test and after stored in dry air for two days.

6.3.1.2.5 Summary

The DNTT devices were generally stable in a dark and dry environment under intensive operation. A device sustained a bias measurement for up to 144 of hours without losing its mobility and high on/off ratio. There were three major factors that changed DNTT transistor behaviour: a) water, which, in a similar way as that in pentacene transistors, shifted the transfer curves to more negative potential and reduced I_d. The shift was recoverable by exposing the device to light; b) light together with air, gave a shift for the transfer curves to more positive potential. While, differently from pentacene devices, dry

air without illumination did not appear to lead to device degradation; and c) long time gate bias stress shifted the V_{to} in the opposite direction to the bias stress. Most of these changes were recoverable by storing the device in dry air for a period of time.

Hole traps originating from water in the transistor and electron traps formed by assistance of oxygen and light were the origin of the negative V_{to} shift in damp air and positive V_{to} shift under light in dry air respectively. This work also suggests that the device degradation during long-term bias has a different origin from that observed under repeating measurements: either the charge injection from gate to dielectric layer or the slow polarisation of dielectric layer could be the cause of the change under long term bias.

6.3.2 Environmental Effects

Degradation during storage could affect device performance and decide the lifetime of a transistor. Interestingly, however, the environmental factors do not always cause degradation.

6.3.2.1 Improvement During Storage

It has been observed that DNTT devices as-fabricated showed a poorer performance compared with that of devices stored in air for several days. **Figure 6-18** shows DNTT transistors measured as-fabricated (a) and after two days aging in air (b). The square root of the transfer curve of as-fabricated devices was not straight, indicating a mobility that is dependent on gate voltage, a sign of imperfection[9], e.g. contact resistance, of a transistor. After storage in dry air for a few days the curves became straight, and the on-current increased slightly.

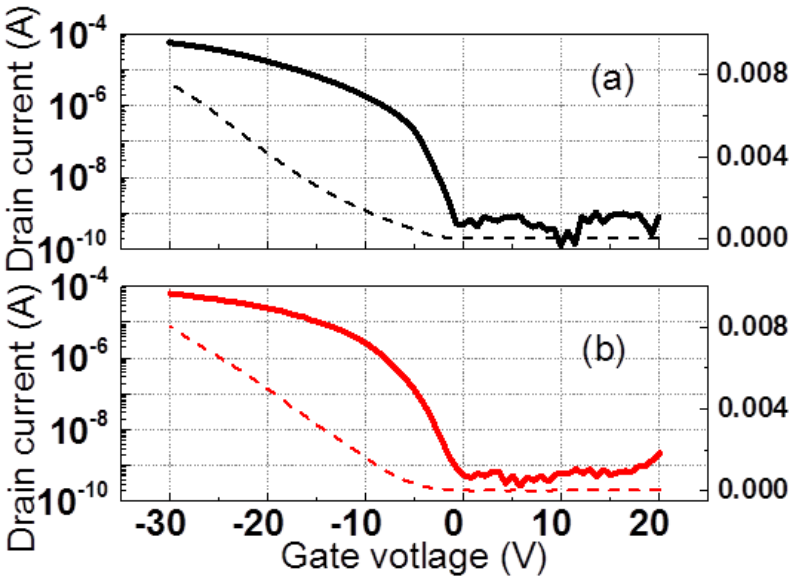


Figure 6-18 Transfer characteristics of a DNTT device (a) measured as fabricated and (b) after stored in dry air for two days.

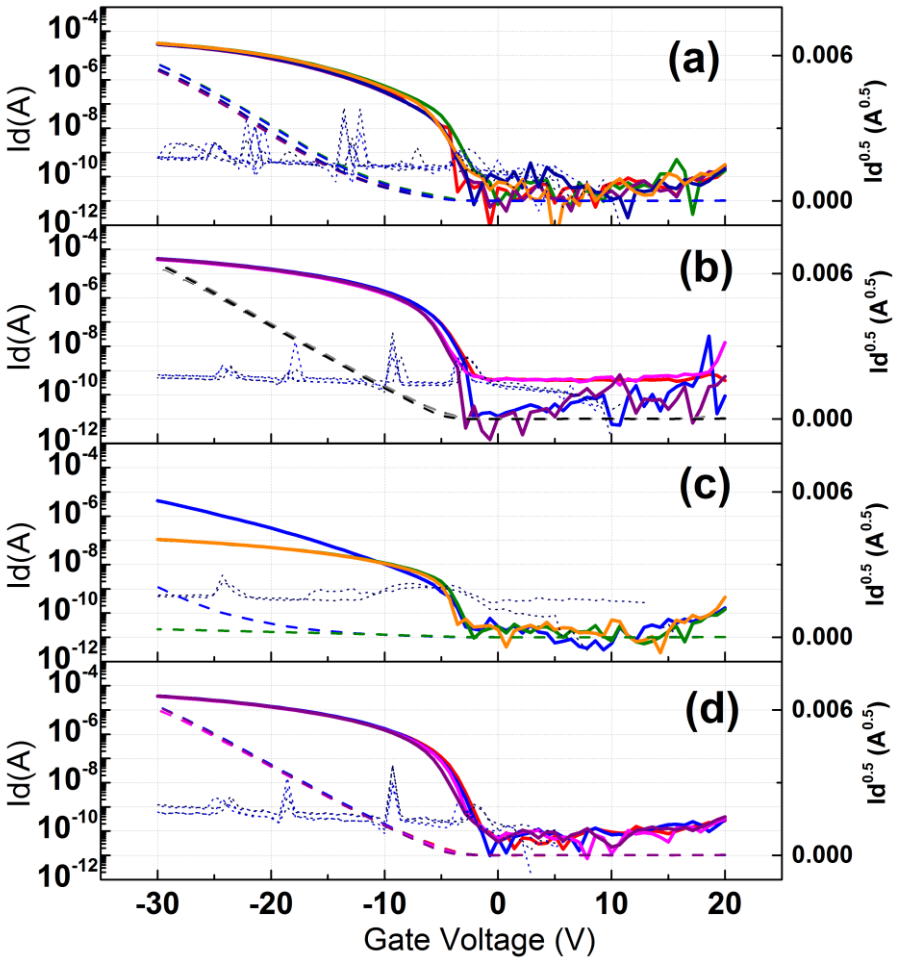


Figure 6-19 (a) DNTT transistor aged for two days in air before source and drain contacts were applied; (b) the same device measured after storage in dry air for another two days; (c) a DNTT transistor stored in vacuum for two days after fabrication; (d) the same device after storage in air for two days.

There are two possible explanations for this improvement: i) as the devices were removed from vacuum (after manufacture), they may react with air, which could lead to improvement of the contact between source/drain to the semiconductor layer, or ii) reaction with oxygen could transform the semiconductor grain boundaries or other domains to a more favourable form for charge carrier transportation.

To check whether the improvements come from the S/D contact, a group of devices were stored in dry air without putting on the source and drain electrodes, and after two days

the source and drain were deposited and the devices were measured. These devices showed a non-linear square-root of transfer curves (**Figure 6-19** (a)) similar to that in the **Figure 6-18** (a). Then, after another two days storage in air, the square-root of the transfer curves became straight (**Figure 6-19** (b)). This indicated that changes at the semiconductor-metal contact do affect the performance of the DNTT device over the first couple of days exposed to the air. Aging of the contact area may help to provide a better junction for hole injection. A different transistor from the same group of devices was stored in vacuum after fabrication (with source and drain) for two days (**Figure 6-19** (c)). These devices showed very poor performance - even worse than the devices in the same batch measured immediately after fabrication, shown in **Figure 6-18** (a), but the performance was recovered after two days stored in air (**Figure 6-19** (d)). It is not clear what caused the degradation of the device on storage under vacuum.

6.3.2.2 Long Term Environmental Stability

To investigate the long term environmental stability of DNTT devices, three groups of transistors (with a 450nm TPGDA insulator and PS buffer layer on a PEN substrate) were tested over a period of nine months. The first group of devices was stored in a dry box with relative humidity of 5-10% at 20°C in the dark, a second group was stored in a clean-room atmosphere with relative humidity of 30-50% at 15-25°C in the dark. The third group was stored in uncontrolled ambient air under laboratory light. All the transistors were measured in the dark. A batch of pentacene devices was also stored in ambient air in the dark at 15-25°C in the lab, and was measured over four months for comparison with the DNTT. Representative transfer curves of the transistors during the measurement period are shown in the **Figure 6-20**. The hole mobility and sub-threshold swing extracted from the transfer curves are presented in **Figure 6-21**.

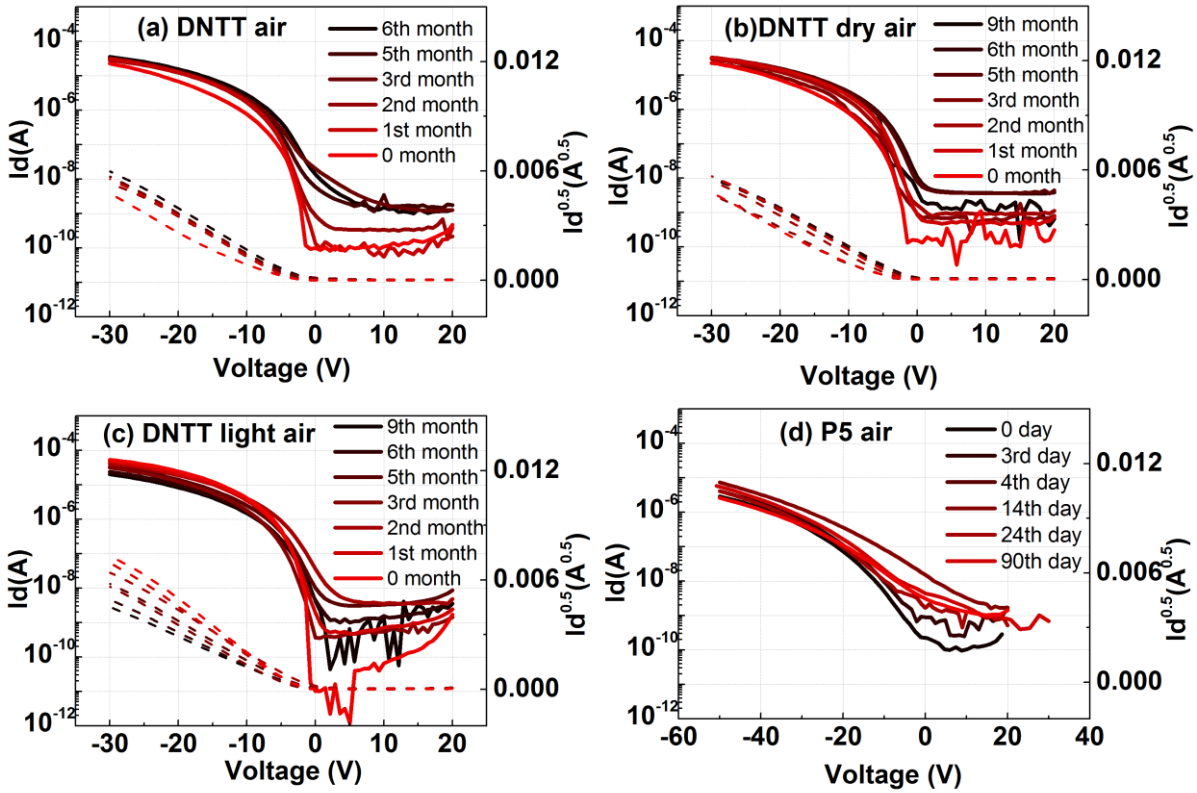


Figure 6-20 Transfer curves of three DNTT transistors stored in (a) dry air in the dark, (b) air in the dark, (c) air in the light; and (d) a pentacene transistor stored in air.

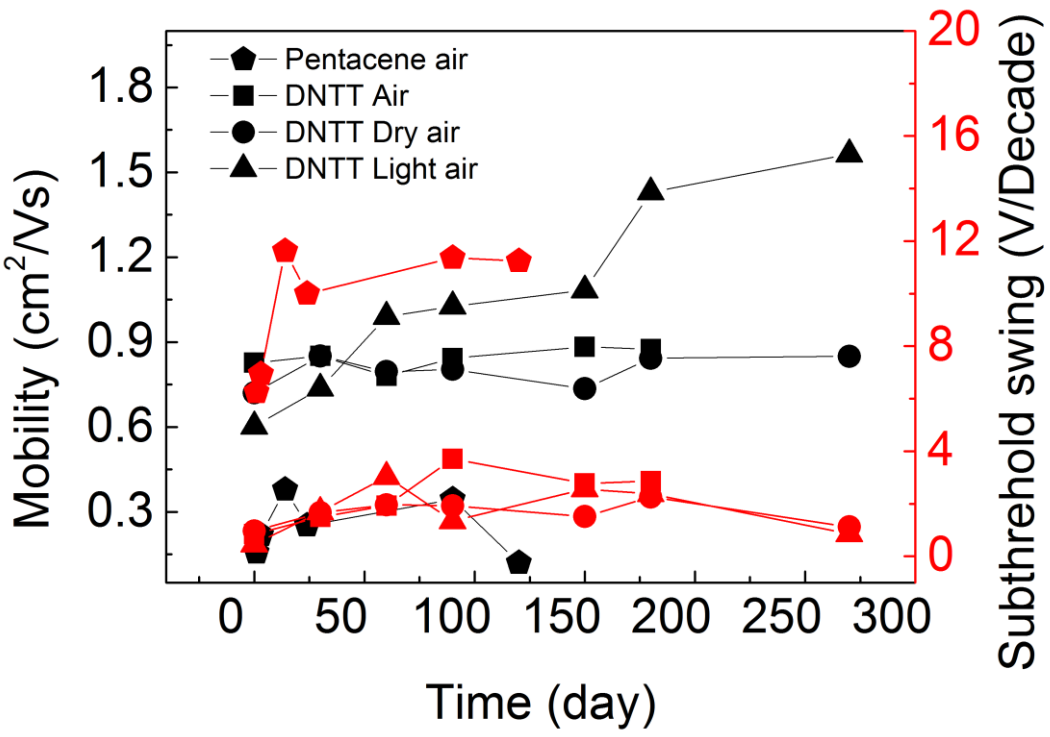


Figure 6-21 Extracted hole mobility and sub-threshold swing of device in Figure 6-20.

The DNTT showed much better environmental stability compared with the pentacene. The mobility of our DNTT device stored in the dark barely shifted over six months, irrespective of the environment. The pentacene, on the other hand, showed unstable performance. The mobility increased during the first two weeks from 0.15 $cm^2V^{-1}s^{-1}$ to about 0.40 $cm^2V^{-1}s^{-1}$ then stabilized at 0.30 $cm^2V^{-1}s^{-1}$ before finally decreasing after three months. The increase in the mobility of the pentacene is probably due to doping of oxygen molecules into the semiconductor[18]; and came at the price of increased I_{off} and significantly increased *SS*[3] due to trap states[19-20]. This device degraded and finally stopped showing transistor behavior after four months, presumably due to oxidation/disintegration of pentacene in air. For the DNTT device stored in light in air, the mobility gradually increased with storage time, from 0.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$ to 1.5 $cm^2 \cdot V^{-1} \cdot s^{-1}$ after nine months. Such an increase could also possibly be due to doping of oxygen

molecules into the semiconductor, whereas DNTT is chemically much more stable in oxygen, so there is no further oxidation, hence no deterioration on mobility.

The greater *SS* and the shift of V_T towards higher potential for the devices kept in the dark in atmosphere compared with the one stored in dry air suggested that a higher concentration of acceptor-like traps was associated with water. This is somehow in conflict with the results observed on repeating cyclical bias (**section 6.3.1.1.2** and **section 6.3.1.2.2**), where the traps induced by water suppressed the device being turned on, i.e. water caused donor-like traps. There is no proper explanation for this yet.

It has been reported[10], and our studies suggest, that most of the impact from oxygen or humidity to pentacene kept in a moderately damp atmosphere for a period is reversible by putting the device in dry air for a period of time. However, in the case of the DNTT device stored in air for long periods, it was not possible to completely recover the increased I_{off} back to the previously low value by putting the devices in vacuum of 10^{-5} mbar for 24 hours, perhaps suggesting some less reversible effect in this case.

It is clear that substituting the central ring of pentacene with the dithieno moiety renders DNTT far less susceptible to oxidative degradation and thus a better candidate for device and circuit applications.

6.4 Summary

In conclusion:

(a) DNTT transistors with a flash evaporated TPGDA dielectric layer were stable under repeating measurements in a dry environment in the dark. The transistors maintain a high mobility and on/off ratio after being held under bias for 144 hours in dry air. Although the bias stress, moisture and illumination could all alter the device behaviour moderately, the changes were mostly recoverable by storing the devices in dry air. The hole carrier mobility was constant under all the measuring conditions.

(b) Pentacene devices showed worse stability compared with DNTT. Degradation was observed with repeating measurements in dry air in the dark. Illumination accelerated the degradation during repeated measurements. Water also affected the device performance by ionic current and carrier traps. The degradation of transfer characteristics of pentacene devices was recoverable only to a limited extent.

(c) Water and oxygen had distinctive effects on both DNTT and pentacene transistors. Water not only lead to an increased I_{off}, but also, more obviously, suppresses/delays the I_d being switched on, i.e. increases the *SS*, shifts the V_{to}, and reduces the I_d during operation. The suppression of I_d could be due to donor-like hole traps resulting from water in the semiconductor. In contrast, the oxygen tends to move the transfer curve towards a more positive voltage due to generation of acceptor-like charge traps. For DNTT however, the shift is only observed when the devices were measured under illumination in air. In addition, illumination appears to be able to eliminate the degradation in behaviour brought about by water.

(d) The gate bias, in contrast, affected the devices via the dielectric layer. The V_{to} shifted by several volts in the opposite direction to the bias stress after a few hours due to either charge injection from the gate into the dielectrics, or by slow polarisation of dielectric layer. The shift of the V_{to} was recoverable with time or with a counter-bias.

(e) DNTT transistors could survive storage in dry air, air, or air with illumination for more than nine months. The mobility of the transistors was stable over the nine months as long as the devices were stored in the dark. Illumination increased the mobility of DNTT transistors more than 2-fold over the nine month period, probably due to a light-assisted oxygen doping effect. All devices showed increased I_{off} and decreased *SS* over the period of storage. Such degradation was generally not recoverable. This was different from the effect observed over repeated measurements and the exact reason for the degradation has not been confirmed. The pentacene devices, in contrast, degraded over four months and the mobility was unstable throughout their lifetime.

6.5 References

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Chapter 7

Conclusion and Future Work

7.1 Conclusion

i. TPGDA, HDDA and PD10374 dielectric materials have been deposited and cured in a multiple pass process in a roll-to-roll web coater to form pinhole-free dielectric layers with ~100% capacitor yield. The plasma curing provided a dielectric strength of about 1.5 MV·cm^{-1} for the TPGDA and HDDA and >1.8 MV·cm^{-1} for the PD10374. The TPGDA and HDDA film showed a minimum functional thickness of about 300 nm, below which the capacitors became significantly leaky. In contrast, the minimum thickness of PD10374 was less than 100 nm thus leading to threefold greater dielectric areal capacitance of 41 nF·cm^{-2}.

ii. Transistors made from these dielectric layers showed stable, high mobility for both pentacene and DNTT semiconductors, so long as the insulator surface is buffered with a layer with a surface ester group content less than one per 20 carbon atoms. It was found that the overall dielectric surface energy is not the primary factor in determining grain size in subsequently evaporated films of pentacene or DNTT. Furthermore, larger grain size does not necessarily lead to high mobility: a non-polar dielectric surface is also required.

For pentacene devices, however, a non-polar dielectric surface also leads to a remarkable shift of threshold voltage to more negative values. For DNTT

devices, in contrast, PS and PVS buffer layer on TPGDA yielded a higher mobility accompanied by relatively low threshold voltage.

iii. A vacuum deposit-able buffer layer was made by flash evaporation of lauryl acrylate mixed with HDDA followed by e-beam curing. The resulted non-polar dielectric surface improved DNTT transistors' hole mobility fivefold and lead to consistent device performance. The highest mobility achieved by a device made in an all vacuum evaporation process is about 0.5 $cm^2 \cdot V^{-1}s^{-1}$ has been.

iv. A device stability study has been made of both pentacene and DNTT transistors on TPGDA. DNTT transistors with a flash evaporated TPGDA dielectric layer were stable with repeat measurements in a dry environment in the dark. The transistors maintain reasonably good performance (high on/off, high mobility, low *SS*) after 144 hours bias stress in dry air. Although the device behaviour could alter moderately under stress, moisture and illumination, the changes were mostly recoverable by storing the devices in dry air.

The acceptor-like traps brought by water and donor-like traps brought by oxygen/light in the semiconductor are proposed as the main causes for the performance change during repeating operation. In contrast, the hole injection or slow polarisation in the dielectric layer was responsible for the device performance change under bias stress.

v. The DNTT devices showed storage life longer than nine months in dry air, atmosphere and atmosphere under illumination. The mobility of the transistors was stable over the nine months in the dark. Exposure to light during storage increased the mobility by more than twofold over the nine months, probably due to a light-assisted oxygen doping effect.

Pentacene devices showed worse stability than DNTT devices, either during repeating operation or storage. The storage lifetime was less than four months in the dark and less than a week under illumination.

7.2 Future Works

A thinner dielectric layer with high areal capacitance is always preferred for transistors. The application of the OTFTs could be broadened, if the V_T is reduced to sub-ten volts range, which meets the voltage output of many batteries including flexible lithium ion battery arrays[1]. Flash evaporation of a fluorine-containing polymer, which has shown exclusively good dielectric strength in solution processing, could be explored.

Although the flash evaporated lauryl acrylate and HDDA mixture buffer layer on dielectric surface has provided considerable improvement for the transistors, it is still not as good as that of SAM layer deposited by a solution process in terms of maximum carrier mobility. A vacuum depositable monolayer buffer layer with polymerisable groups anchored on the substrate and with long non-polar side groups on the surface might be expected to perform well.

Scaling up the semiconductor layer deposition is a problem that not yet properly solved in either solution nor vacuum processes. This is, for certain, a task that has to be accomplished before achieving roll-to-roll fabrication of organic electronics. Vapour jet printing of semiconductor could be an interesting process in vacuum for further development.

Except for the conventional logic functions, OTFTs have shown the potential to be used as sensors in various types including glucose sensing, TNT sensing, pH sensing etc[2]. Hopefully, with certain amount of clever engineering on these low cost OTFTs, they could be applied as smart sensors in a broad range of applications.

7.3 References

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