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Roll-to-Roll Manufacturing of Flexible Thermoelectric Semiconductors Using Low-Level Direct-Current Sputtering

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ABSTRACT

Direct-current (DC) sputtering combined with roll-to-roll processing offers a highly competitive approach for scaling up the manufacturing of flexible functional thin films. However, its application to less-conductive functional materials, such as semiconductors, remains limited due to charge buildup and arcing on the target. This study investigates the intrinsic relationships between DC sputtering power and the surface topography, elemental composition, crystallography, and thermoelectric properties of flexible thin-film semiconductors. We explore low-level DC power for room-temperature roll-to-roll sputtering of Bi-Te thermoelectric films, identifying an optimal power window that avoids charge-buildup effects on the semiconductor target. Low-power DC sputtering enables controlled crystallographic, microstructural, and compositional characteristics, thereby modulating electrical transport properties and, consequently, thermoelectric performance. As a result, a room-temperature figure of merit of ~0.1 is achieved at an optimal power of 0.22 kW while maintaining high-throughput roll-to-roll manufacturability. Device-level validation is demonstrated using a flexible thermoelectric generator, showing output performance consistent with COMSOL simulations.

1 | Introduction

Scaling laboratory advancements in flexible materials to commercial production remains a critical challenge, particularly in addressing the growing demand for the Internet of Things [1]. Among the various microfabrication approaches for flexible electronics [2–5], roll-to-roll (R2R) processing [6, 7] offers a compelling solution, widely adopted in industry for cost-effective, high-throughput fabrication of coatings. Sputtering is particularly well-suited for R2R processing of multi-element functional semiconductors. To prevent target charging and arcing during sputtering of semiconductor, radio frequency power is commonly employed [8], however, direct current (DC) power has gained favor due to its lower cost and significantly higher sputtering rates, which maximize throughput in industrial R2R manufacturing [9]. The key challenge lies in optimizing the DC sputtering power for these low-conductance semiconductor materials, preventing target melting/arcing while maintaining high R2R throughput and materials performance.

Here, we address this challenge using an R2R sputtering platform to produce Bismuth Telluride (Bi-Te) thin films, a well-studied thermoelectric (TE) material with a small bandgap (E_g) of approximately 0.2 eV [9]. Thermoelectric generators (TEG) are ideal candidates as localized power sources for wearable electronics [10], integrating energy generation, sensing, and storage functionalities [11, 12], as they can convert the temperature difference between the human body and ambient into electricity through the Seebeck effect [13]. Decoupling the intrinsic relationships among thermoelectric properties is a central challenge in materials

science [14], as these parameters are inherently interdependent and difficult to optimise simultaneously. For example, charge carriers that contribute to electrical conduction also transport heat, leading to low electrical resistivity but high thermal conductivity—an unfavourable combination for achieving a high thermoelectric figure of merit (ZT; see Equation 1). Recent studies on nanostructured Bi-Te materials have demonstrated promise for enhancing TE performance (ZT) by decoupling the intrinsic relationships among S, ρ, and κ [15], for example, reducing dimensionality [16], defect engineering [17], and compositional engineering [18].

$$ZT = \frac{S^2 \cdot T}{\rho \cdot \kappa} = PF \cdot \frac{T}{\kappa} \tag{1}$$

where S is the Seebeck coefficient, ρ is the electrical resistivity, κ is the thermal conductivity, T is the absolute temperature, and PF is the power factor.

Bi-Te thin-film thermoelectrics are an ideal test case for evaluating the feasibility of DC sputtering of functional semiconductors in our R2R context. Research on the optimal DC power range for sputtering Bi-Te is limited. Prior work by Kianwimol et al. [19] investigated flexible Bi-Te films sputtered at varying DC powers but reported uncontrolled thickness and predominantly micron-thick films, rendering them unsuitable for high-speed R2R processing. In this study, we successfully demonstrate R2R manufacturing of very thin Bi-Te films onto a fast-moving polymer web at an in-line speed of 25 m/min using DC sputtering at room temperature. By optimizing the DC power to 0.22 kW, we achieved high-throughput deposition while maintaining exceptional material performance. A systematic investigation of the relationship between DC sputtering power and the films' surface topography, elemental composition, crystallography, and thermoelectric properties enabled these advancements. This work integrates low-level DC sputtering with R2R processing to overcome arcing and melting in the deposition of less-conductive semiconductors, marking a significant step toward industrial-scale production of flexible functional thin films.

2 | Results and Discussion

2.1 | R2R DC-Sputtered Bi-Te Thin Film: Surface Morphology & Phase Identification

Figure 1a illustrates the R2R sputtering process, in which a flexible polymer web moves through the sputtering source. In this study, the flexible substrate was mounted on a rotating coating drum at 25 m/min and passed through the sputtering sources multiple times. An MDX DC power supply was used with various sputtering parameters. When grown on a ~125 μm-thick PET substrate (DuPont), the deposited film exhibits excellent flexibility. This is demonstrated by cyclic buckling fatigue tests (Figure S1), during which negligible changes in electrical resistance are observed under buckling strains up to 1.8%. More detailed investigations of the mechanical flexibility of both the films and the TEG devices have been reported in our previous studies [20, 21]. Table S1 presents the thicknesses of the as-deposited films alongside their respective sputtering conditions. In sputtering processes, the sputter rate typically rises and then falls with increasing power [22]. At lower powers, the plasma density is lower, and insufficient voltage may limit the energy for Ar ions to eject the target material, resulting in a low sputter rate. As power increases, the plasma density and energy intensify, thereby boosting the sputter rate. However, excessively high power levels can diminish the rate due to (1) increased energy loss of Ar ions during collisions, (2) restrictions on sputtered atoms passing through a denser plasma region, and (3) potential substrate/thin film etching from a dense and extended plasma zone. Here, an increase in film thickness correlates with higher sputtering power, as expected due to increased sputter rates, and the power does not become sufficiently high to reduce the thickness again. Figure S2a illustrates a plot of measured deposition rate versus power for a series of films deposited over 3 min. There is a nearly linear increase in deposition rate with power, although it does not increase as rapidly at the highest power level (0.75 kW). It is noteworthy that at 0.22 kW, the sputter rate is slightly lower than at 0.2 kW, attributed to differences between the two modes in the MDX power source in the Oxford R2R system; specifically, the corresponding current at 0.22 kW (0.8 A) is smaller than at 0.2 kW (0.85 A), resulting in lower plasma density and hence a reduced sputter rate. The electrical conductivity of the target semiconductor material, Bi_2Te_3, was capable of sputtering under moderate DC power, whereas higher power levels (0.75 kW) led to melting of the Bi_2Te_3 target. To allow for comparison at different power levels without the influence of film thickness, two samples were also fabricated under 0.22 kW to have a similar thickness as samples from two other powers by adjusting the deposition time (refer to Table S1).

The film surface was examined using atomic force microscopy (AFM) and scanning electron microscopy (SEM) (see Figure 1a; Figures S3 and S4 in Supplementary Information). In SEM micrometer views, the surface morphology appears notably fine and smooth. However, with increasing power, circular features become visible (Figure S4), with their quantity and size tending to increase. Such defects are typically attributed to arcing phenomena, as reported by Sarkar [23] and Panjan et al. [24] in their studies on sputtering poorly conductive materials. During DC sputtering, when the plasma density is high, and the incoming ion flux cannot be efficiently dissipated through the target, charge accumulation can occur on the target surface. This charge buildup increases the local electric field and target temperature, potentially leading to arcing and local melting. These effects are particularly pronounced for poorly conductive materials or when excessively high DC power is applied. Therefore, optimisation of the plasma density, for example, through careful control of sputtering power, is essential to achieve high-quality films while avoiding charge accumulation and arc discharge at the target. The energy-dispersive X-ray spectroscopy (EDX) analysis (Figure S4h) indicates a lower concentration of the Te element in these defects. In AFM nanometer-scale views, the film exhibits a granular structure consistent with our previous findings [25–27], suggesting an island-growth mechanism for films sputtered onto a polymer substrate at room temperature. Note that when referring to 'grains' in morphology, we do not imply that each grain represents a crystal within the material. This distinction is confirmed by examining both the grain size and the crystallite size (see Figures S3–S5). This terminology aligns with how 'grains' denote regions of material growth from initial islands or nuclei.

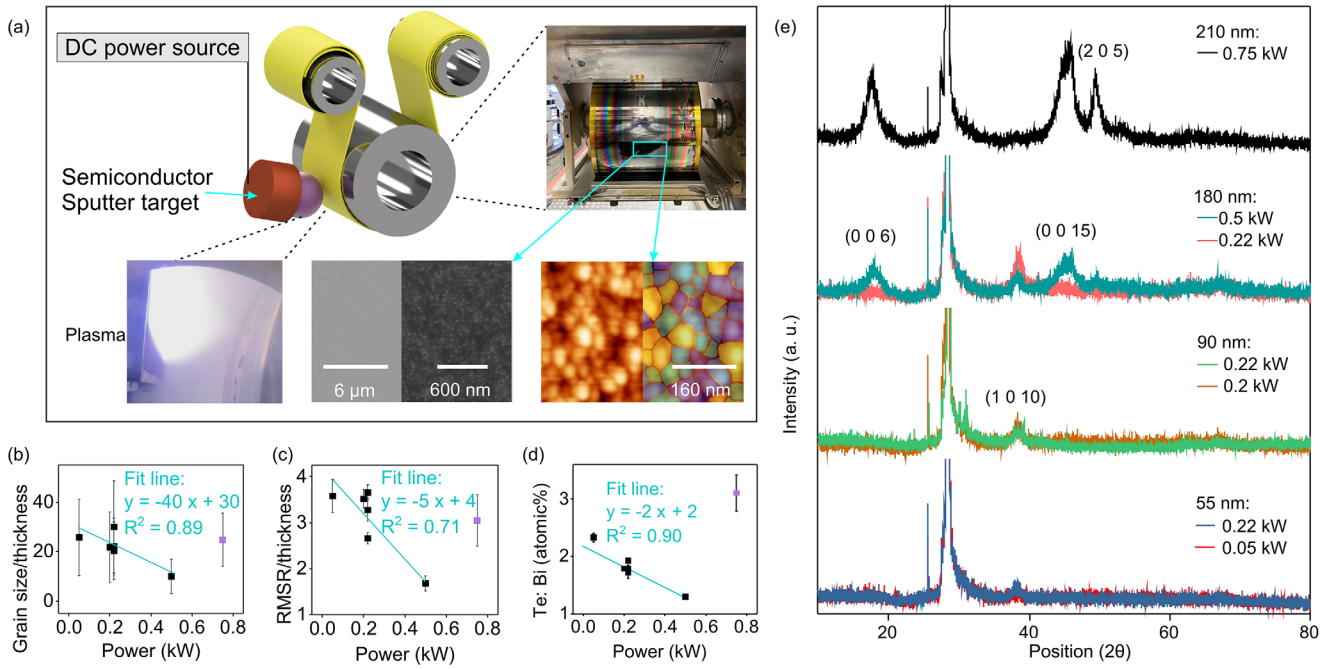

FIGURE 1 | (a) R2R sputtering system with pictures of the plasma, SEM image of the 0.2 kW sample, and AFM image of the 0.05 kW sample; (b) The grain size (measured from AFM) normalized against sample thickness (measured by Dektak) vs power; (c) The RMSR (measured from AFM) normalized against sample thickness (measured by Dektak) vs power; (d) Elemental composition (measured from EDX) vs power; (e) XRD traces of samples grown under different powers (Miller indices are instructed using reference: ICSD #193330). The fit lines in (b–d) do not consider the 0.75 kW sample (the purple dots in the figures) because the sputtering target melted. The error bars are analyzed from several identical samples: three images for RMSR, five locations for thickness, and elemental composition. The average grain size is analyzed from an area of 400 × 400 nm.

In sputtering processes, the grain size of deposited films strongly depends on the mobility of adatoms reaching the substrate [28]. For room-temperature deposition, adatom mobility is governed by the kinetic energy retained by sputtered atoms upon reaching the substrate. This energy is determined by Ar ion bombardment of the target (controlled by voltage) and is diminished by collisions within the plasma (controlled by current). These competing mechanisms significantly influence film surface morphology, as high power typically involves both increased voltage and current. Specifically, when voltage predominates, enhanced adatom mobility promotes the formation of larger grains [29, 30]; conversely, when current predominates, a higher density of plasma collisions reduces the kinetic energy of sputtered atoms but increases nucleation site density, resulting in the formation of smaller grains [31, 32]. Hence, high voltage tends to produce larger grains, while high current results in smaller grains. In practice, both voltage and current typically increase with power during sputtering, so the dominant effect on grain growth depends on which parameter (current or voltage) increases more significantly. It is important to note that this study focuses specifically on DC sputtering conducted at room temperature, without applying external heating to the substrate, as would be preferred for an R2R process.

When comparing each pair of samples that have similar film thickness, as summarized in Table 1, the 55 and 180-nm cases show that both voltage and current increase with power, and the grain size decreases. This suggests that the effect of increased current dominates under these conditions—stronger plasma collisions reduce the kinetic energy of sputtered atoms, thereby lowering adatom mobility and resulting in smaller grains. The ~90-nm pair clearly demonstrates the expected behavior: the 0.22 kW sample exhibits a higher voltage and lower current than the 0.2 kW sample, resulting in a larger grain size. These observations support the conclusion that higher adatom mobility—and hence larger grain size—is achieved under conditions of high voltage and low current during sputtering.

When comparing all samples rather than individual pairs, film thickness should be considered, as it significantly influences grain size. Hence, a simple correlation between grain size and sputtering power is insufficient (Figure S2b). In our previous study [25], under the same sputtering power, grain size generally increased with film thickness, indicating that initial grain formation starts smaller and enlarges as the film thickens. The observations for samples sputtered at different powers (Figure S2c) broadly align with this trend. When grain size is normalized for thickness (Figure 1b), a clearer decreasing trend is observed (R^2 = 0.89) as power increases. This trend corresponds to increasing voltage and increasing current (see Table S1), which have opposing effects on grain size: voltage tends to promote larger grains through enhanced adatom mobility, while current promotes smaller grains by limiting adatom mobility through increasing plasma collisions and reducing kinetic energy. The normalized data in Figure 1b consistently show a reduction in grain size with increasing power, suggesting that in this study, the effect of current dominates. Similarly, surface roughness (RMSR) is also affected by adatom mobility and film thickness (Figure S2d,e). When RMSR is normalized for thickness

TABLE 1 | Dominant effect on grain size associated with sputtering power. An increase in grain size (↑) requires an increase in voltage (↑) and a decrease in current (↓). 'Voltage↑ < Current↑' indicates that the increase in current has a stronger effect than the increase in voltage. Power, voltage, and current values are directly recorded from the MDX series power supply display. See Table S1 and Figure S2 for additional details.

Cases	Power (kW)	Voltage (V)	Current (A)	Grain size (nm^2)	Dominant effect	Results
55 nm pair	0.05	308	0.35	1468	Voltage↑ < Current↑	Grain size↓
	0.22	372	0.8	1210		
90 nm pair	0.2	348	0.85	2045	Voltage↑, Current↓	Grain size↑
	0.22	372	0.8	2488		
180 nm pair	0.22	372	0.8	3521	Voltage↑ < Current↑	Grain size↓
	0.5	406	1.55	1859		

(Figure 1c), a decreasing trend ($R^2 = 0.71$) is also observed, as RMSR is influenced by both in-plane and out-of-plane grain size.

The EDX results in Figure 1d indicate that the as-deposited films are Te-rich compared to stoichiometric Bi_2Te_3 target materials, with a decrease in Te content as sputter power increases, with a linear fit of $R^2 = 0.9$. The film exhibiting extremely high Te-excess at 0.75 kW is likely due to target melting. Kianwimol et al. [19] attributed the increasing Bi content with power to a decrease in the Te/Bi sputtering yield ratio under higher power, influenced by more energetic Ar ions, whereas Zang et al. [33] did not observe changes in elemental composition with varying sputter power. Transmission electron microscopy (TEM) image (Figure S1) confirms that the Bi-Te film exhibits a polycrystalline structure, although the extent of crystallinity is lower than that of thermally annealed Bi-Te films reported previously [34]. In Figure 1e, XRD diffraction peaks at 2θ angles of 17.7°, 38.1°, 45.4°, and 49.5° correspond to planes (0 0 6), (1 0 10), (0 0 15), and (2 0 5), respectively, referenced from the standard trigonal Bi_2Te_3 phase (ICSD #193330). The peak (1 0 10) at 38.1° diminishes, while new peaks (0 0 6), (0 0 15), and (2 0 5) appear and grow at the higher powers (0.5 and 0.75 kW). These peaks are characteristic of the Bi_2Te_3 phase, although BiTe phases with overlapping peaks could also exist. This change with power may represent either a change in phase or a change in the orientation population of the crystals in the Bi-Te layer. The crystallite size (D) and microstrain (ε) were calculated from the (1 0 10) peak using the Scherrer method (Equation 2). Figure S5 demonstrates that D increases and ε decreases with higher sputter power.

Thus, DC sputtering power governs both the surface morphology and crystallographic characteristics of Bi-Te films. Higher voltage enhances adatom mobility and favours grain growth, whereas increased current reduces adatom kinetic energy through plasma collisions, leading to smaller grains. In practice, both parameters increase with sputtering power, and the dominant effect depends on their relative contributions. Using our DC power supply, the grain size decreases with increasing power. Crystallographically, the (1 0 10) reflection dominates at lower sputtering powers, indicating preferred orientation and smaller crystallite sizes, with the extent of grain-size control depending on the characteristics of the power supply. These variations in microstructure and crystallography directly influence the electrical transport properties of the thermoelectric films, including carrier mobility (μ) and carrier concentration (n). The resulting effects on thermoelectric performance are analysed in the following section (see Figure 2; Figure S6).

2.2 | Thermoelectric Characterization

The effects of the surface morphology and phase of Bi-Te films sputtered under various DC powers were further analyzed to understand their impact on thermoelectric performance. In Figure 2a, PF, calculated as S^2/ρ, achieves the highest value at 0.22 kW by balancing the relationship between S and ρ, which are interrelated through μ and n [35, 36]. While higher DC power (where it leads to greater deposition rate) is desirable for high-throughput industrial manufacturing, it can compromise film performance. At higher powers (0.5 and 0.75 kW), although crystallinity and crystallite size increase — which should theoretically decrease ρ — the arcing-induced surface defects (see Figure S4) can negatively impact ρ. Suppressing arcing could thus allow for higher TE performance, enhancing the functional film production rates without sacrificing performance. The Bi-Te films sputtered at 0.22 kW exhibit a favorable PF, indicating an optimal balance between S and ρ. Films sputtered below 0.22 kW show lower S, while those sputtered above 0.22 kW demonstrate higher ρ. The highest PF, $4\,(\pm 0.1) \times 10^{-4}$ W m^{-1} K^{-2}, is achieved with a ~55-nm thick Bi-Te film sputtered at 0.22 kW. This finding highlights the importance of optimizing sputtering power to enhance thermoelectric performance while maintaining feasible production rates in R2R manufacturing.

To further analyze the variations in S and ρ, the measured data for μ, n, and E_g from all samples are presented in Figure 2b, and further analyzed in Figure 2c–h; Figure S6. As expected, the measured results broadly align with the relations $S \propto \mu^{0.2}$ [37], $S \propto (n)^{-2/3}$ [38], with a strong linear fit of $R^2 \geq 0.96$. The crystallite size and microstrain show a clearer correlation with ρ, where the much larger grain size contains multiple crystals with smaller strain, with a linear fit of $R^2 = 0.96$. The 0.75 kW sample is excluded from these fitting trends because the target melted during deposition, resulting in an anomalously high Te content and different XRD phases. The coupling relationship between S and ρ strongly depends on the competition between μ and n. In a thin-film configuration, many factors can affect μ and n, as summarized in Table 2. μ is likely correlated with the film composition, whereas n appears to correlate with the bandgap (see Figure 2g,h). However, no

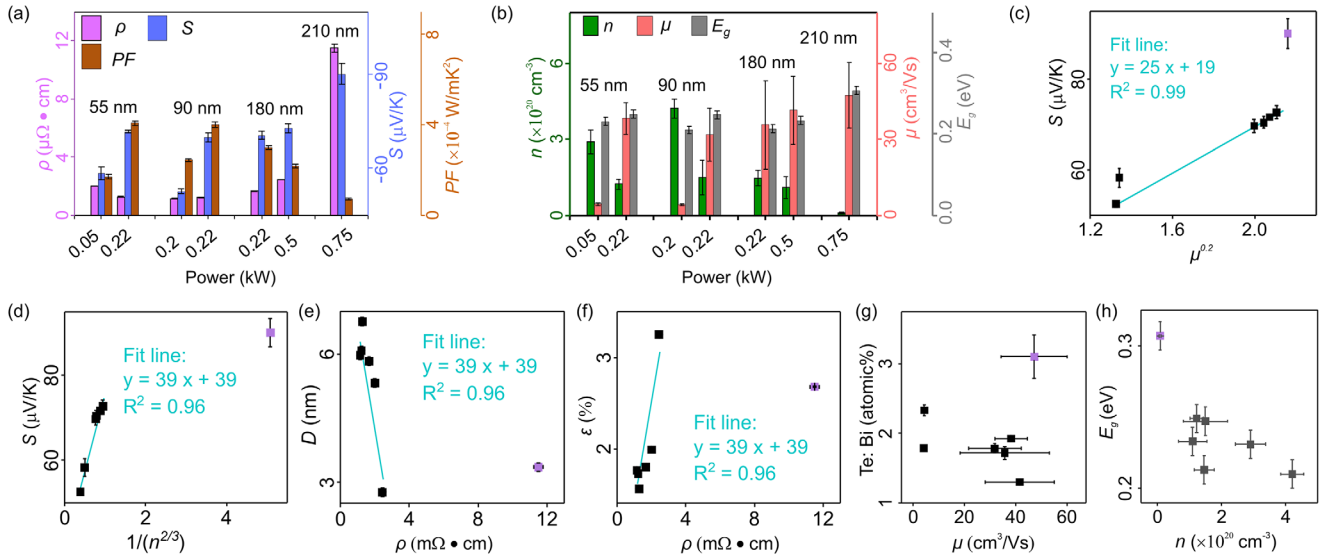

FIGURE 2 | (a,b) ρ, S, PF, μ, n, and E_g of Bi-Te films sputtered under different DC powers; (c-e) Plots of S vs $\mu^{0.2}$, S vs $1/n^{2/3}$, D vs ρ, ε vs ρ; Te: Bi vs μ, and E_g vs n. The 0.75 kW sample (i.e., the purple data in c-h) is excluded from these fitting trends because the target melted during deposition.

TABLE 2 | Thermoelectric behaviour determined by μ and n.

Factors affecting μ	Factors affecting n
Crystallite/Grain size [39–41]	Elemental composition/Defects/Doping [39, 42]
Microstrain [43]	
Dislocation density [44]	Bandgap [45]
Crystallinity [46, 47]	
Surface roughness [48]	Energy barrier at grain boundary [45, 49]
Elemental composition [50, 51]	

clear correlations with other factors were observed, as shown in Figure S6. This indicates a complex relationship where various factors combine to influence μ and n, thus the TE performance. These factors, altered by different DC sputtering powers, affect the crystalline texture, microstructure, and stoichiometry of the films.

The total thermal conductivity κ is the sum of the electronic (κ_e) and lattice (κ_L) components (Equation 7). To calculate the temperature-dependent κ_e, the temperature-dependent ρ is estimated from the room-temperature measured ρ and the linear relationship between resistance and temperature of a Bi-Te specimen (see Figure S7 a). Figure S7b–d shows the calculated trends of κ_e and κ_L with temperature for specimens deposited under different DC powers. As the temperature increases, κ_e rises due to the increased ability of thermally generated carriers to conduct heat, while κ_L decreases because of stronger phonon scattering at higher temperatures. Although there are limitations to this calculation method (see Supplementary Information for details), the values of κ_L and the total κ are consistent with recent reports [52], at approximately ~0.75 and ~1.25 W m^{-1} K^{-1}, respectively. Similar to the observations in *PF*, the specimens sputtered at 0.22 kW demonstrate superior results in *ZT* (see Figure 3a). The highest *ZT* (0.1) is achieved with a 55-nm-thick Bi-Te film sputtered at 0.22 kW. This value is 4.2 times higher than the *ZT* (~0.05) of a 1-μm thick Bi-Te film fabricated by sputtering, as reported in [52]. It is noteworthy that a film as thin as ~55 nm is compatible with high-throughput roll-to-roll processing and patterning [53].

The best-performing Bi-Te film, sputtered at 0.22 kW, was selected to fabricate a single n-type TEG. The contact material is a 97 (±8) nm thick Cu film with ρ of 0.032 (±0.003) mΩ·cm and κ of 22.36 (±0.77) W/(m·K). The κ of the Cu film, consistent with values reported in [54], was calculated using the same method as for Bi-Te films, and the crystallite size was determined using XRD results (see Figure S8). The *S* of a Bi-Te strip was measured at 57 (±0.6) μV/K using a custom-built Seebeck system, which is about 18% lower than the 69.7 (±1) μV/K obtained with a commercial MMR Seebeck system. This discrepancy is attributed to the MMR system's smaller sample size and temperature difference, as well as direct heater contact with the film rather than the polymer substrate. Figure 3b simulates heat conduction in a five-TE-strip TEG, with heat applied to the bottom side of the polymer substrate in the white region. Unlike conventional thin-film thermoelectric generator designs, where p-type and n-type thermoelectric materials are connected in series [55], our device connects identical thermoelectric elements in series using metal interconnects. This simplified architecture enables straightforward characterisation of a single thermoelectric material without complications arising

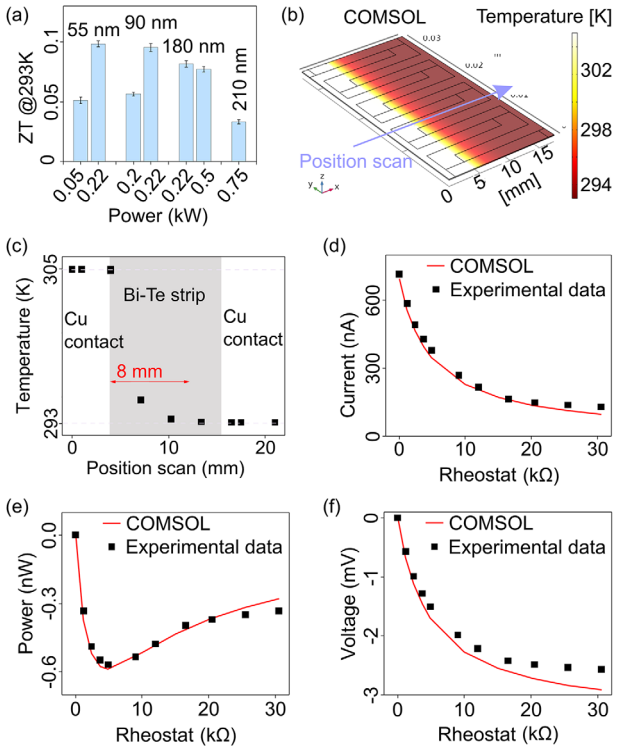

FIGURE 3 | (a) ZT of Bi-Te films sputtered under different DC powers; (b) COMSOL simulation of heat transfer in a TEG (the PET substrate: 23 mm × 34 mm × 125 μm; the 'I' shape Bi-Te strip and the '∫' shape Cu contact: 21 × 2 mm; the hot side, 305 K, is applied to the bottom side of PET covering the one-side block of '∫' shape Cu contact, i.e. the white region, to simulate the real measured situation as demonstrated in Figure S9; the ambient temperature is fixed at 293 K and there is no cold temperature applied on the other side); (c) The temperature scan at the top surface of a Bi-Te strip from the hot side along the x-axis in (b); (d–f) The COMSOL simulated and experimental measured data of current, voltage and power. The highest power output is achieved when the load resistance equals the internal resistance of the TEG [13].

from the presence of a complementary thermoelectric type. A potential concern is that the metal interconnects may conduct heat from the hot side to the cold side, thereby reducing the effective temperature gradient and thermoelectric output. To assess this, COMSOL simulations were performed to verify that this device configuration can generate electrical power (Figure 3). The simulations also provide the temperature profile along the thermoelectric strip. As shown in Figure 3c, the temperature decreases sharply from the hot side (305 K) over the first ~8 mm and subsequently approaches the ambient temperature (293 K), indicating that the applied hot-side temperature does not significantly influence the cold side over this device length. The simulated power output broadly matches the experimental data (Figure 3d–f).

3 | Conclusion

This study investigates DC sputtering of flexible semiconductor functional materials and demonstrates large-scale manufacture of high-performance Bi-Te thermoelectric films on a fast-moving polymer web (in-line speed of 25 m min^{-1}) at room temperature using an industrial-scale roll-to-roll facility. Charge-buildup-induced arcing effects on the Bi-Te target were identified at high DC powers, consistent with defect formation observed in SEM images. By defining an optimal DC sputtering power window, correlations between microstructural and crystallographic characteristics and electrical transport properties (carrier concentration and mobility) were established. Consequently, Bi-Te films sputtered at room temperature at 0.22 kW exhibit the best thermoelectric performance, achieving a room-temperature figure of merit of ~0.1-more than four times higher than previously reported values for room-temperature-sputtered Bi-Te films. Finally, a thermoelectric generator comprising five Bi-Te strips was validated, showing performance consistent with COMSOL simulations.

4 | Experimental Details

4.1 | Thin-Film Fabrication

An industrial-type web coater (*Aerre Machine* vacuum R2R web coater) was employed to sputter Bi-Te onto a flexible polymer substrate through DC magnetron sputtering of a three-inch Bi_2Te_3 target (99.999% purity, *Mi-Net Technology Ltd.*). ~125-μm thick PET (polyethylene terephthalate) sheet was attached to a fast-moving coating drum (in-line speed of 25 m min^{-1}) thus allowing multiple passes of the target source during a single deposition process (the target source was horizontally directed to the coating drum). The base pressure, Ar flow rate, working pressure, and target-to-substrate distance were 2.0×10^{-4} mbar, 250 sccm, 5.5×10^{-4} mbar, and 6 cm, respectively. A DC power source (MDX series, *Advance Energy*) was applied with two modes: fixed current and fixed power. Three fixed power values (0.22, 0.5, and 0.75 kW) and two fixed current values (0.5 A and 1 A, corresponding to 0.05 and 0.2 kW, respectively) were used under a 3-min sputtering. These produced samples with various thicknesses because of different sputtering rates under these powers. Next, the deposition time was varied under a specific power to fabricate films at different powers but with the same thickness. In each case, before the film deposition, a 3-min pre-sputter process was conducted to clean the target surface.

4.2 | Materials Characterization

A *Veeco* Dektak 6 M stylus profilometer was used to measure the thickness of films grown on Si wafers (1196) that were attached alongside the polymer substrates during coating, and masked during deposition to make a step between coating and substrate regions (averaged results from five locations).

Buckling fatigue tests were performed using rectangular samples (5 × 37 mm) in a custom-built buckling system. In this setup, the cold-side stage was displaced at a constant speed of 0.3 mm s^{-1} using a 24 V DC geared motor, as described in Ref. [20].

TEM images were acquired using a JEOL JEM-3000F operated at 200 keV under high-vacuum conditions and equipped with a Gatan Imaging Filter (GIF) 2000 and CCD cameras [56].

The material phase was identified by X-ray diffraction (XRD) using a *Rigaku Miniflex* diffractometer with Cu k_α radiation ($\lambda = 0.154$ nm) under 30 mA and 30 kV ($2\theta = 10° - 80°$, step size = 0.007°). The XRD profile was processed using a peak analyzer (Gaussian fit) in Origin software to extract the peak information (i.e., position, width, and area) used to calculate the crystallite size [57] using the Scherrer equation, and the lattice strain [58].

$$D = \frac{K\,\lambda}{\beta\,cos\theta} \tag{2}$$

where D is the crystallite size, K is the dimensionless shape factor (typically 0.9), λ is the X-ray wavelength (0.154 nm), β is the full width at half maximum (FWHM) of a peak, θ is the Bragg angle.

$$\varepsilon = \frac{\beta}{C\,tan\theta} \tag{3}$$

where ε is the microstrain, and C is a constant value (typically 4) dependent on the assumptions made concerning the nature of inhomogeneous strain.

The film's surface morphology was characterized using AFM and SEM. AFM images (400 × 400 nm) were captured using and *Agilent* 5400 applying a tip (NCHV-A, *Bruker Ltd.*) in tapping mode (0.5 lines s^{-1}, 512 points $line^{-1}$), to analyze the surface roughness over three independent locations (*WSxM* 5.0 Develop 9.0 software) and grain size (*MIPAR* image processing software, which can reliably detect twinned grain structures and characterize the size through a suite of deep learning-based solutions for automated grain structure analysis). A larger surface morphology (in μm view) was imaged using a field emission SEM (FE-SEM *Zeiss Merlin*) under a working distance of 6 mm, a magnification of 40 kX, a voltage of 3 kV, and a current probe of 100 pA. The film stoichiometry was characterized using a point ID mode in EDX over five independent locations.

The in-plane ρ was measured using an in-house custom in-line four-point probe system over five independent locations. By applying a current (10^{-3}–10^{-7} A) in the outer two probes, the voltage across the inner two probes was measured using an *Agilent* 34420 A Nano Volt/Micro Ohm meter, and then ρ was calculated using the following equation [59]:

$$\rho = \frac{\pi\,t}{ln2}\,\frac{V}{I} \tag{4}$$

where t is the film thickness, I is the current applied, and V is the voltage recorded.

The in-plane S was obtained using a commercial Seebeck system (*MMR Technologies Inc.*) under a temperature difference (ΔT) of 0.1–0.45 K in a nitrogen atmosphere chamber. S was determined by the voltage (ΔV) generated between hot and cold sides and the ΔT applied, using the Equation [60]:

$$S = \frac{\Delta V}{\Delta T} \tag{5}$$

E_g was extracted by a Tauc plot from the absorbance spectra (200–3300 nm) measured using a *Cary* Varian 5000 UV-visible-NIR spectrometer.

Carrier concentration and mobility of the fabricated films were measured using a home-built Hall effect system. Samples were fabricated as squares, in van der Pauw (vdP) geometry, following the conditions outlined in [61]. To ensure good contact between the sample and the probes, a 200-nm Cu layer (0.15 × 0.15 cm) was sputtered onto the four corners of a square-sized Bi-Te specimen (1 × 1 cm). Signal generation and measurement were conducted using a *Keysight Technologies* B2901A Source Measure Unit (SMU), controlled remotely via a virtual instrument programmed in LabVIEW. A consistent probe connection was kept between measurements to minimize thermoelectric offsets and geometric asymmetry. Wiring materials and length were also kept equivalent to reduce electrical noise and thermoelectric voltage.

To calculate n and μ, the vdP resistivity was first measured. For vdP resistivity measurement, I-V characteristics were acquired with 80 data points, and the slope was recorded in two configurations perpendicular to each other. These I-V slopes were used to calculate resistivity using the vdP equation [61]. For measurement of the Hall effect, the samples were positioned between the two poles of a permanent magnet. The magnetic flux density (B) of the permanent magnet was calculated as 0.165 T based on a calibration using a floatzone silicon wafer with known carrier mobility. The Hall voltage was then determined through the measurement of the difference in voltages under both positive and negative magnetic fields. To reduce errors associated with misalignment and offset, the mean value across opposing field directions and current orientations was taken. With measured Hall voltage (V_H), resistivity (ρ), and sample thickness (t), and known magnetic flux density (B), and applied current (I), the carrier concentration and mobility can be calculated following the equation [61]:

$$n = \frac{V_H t}{IB\rho} = \frac{qnV_H t}{IB} \tag{6}$$

Batch-to-batch variation was assessed through three batches: 4.4% in the film thickness, 3.0% in the electrical property, and 1.5% in the Seebeck performance. The sample-to-sample variation was included in the result.

4.3 | Modelling of Thermal Conductivity

The total κ is a sum of two contributions: electronic and lattice components.

$$\kappa = \kappa_e + \kappa_L \tag{7}$$

where κ_e is the electronic thermal conductivity, and κ_L is the lattice thermal conductivity arising from contributions by phonons of all frequencies [62], thus being called phonon thermal conductivity as well.

κ_e is estimated/calculated using the Wiedemann-Franz law [63]:

$$\kappa_e = \frac{L_0\,T}{\rho} \tag{8}$$

where L_0 is the Lorenz number (typically 2.44×10^{-8} W Ω K^{-2} or V^2 K^{-2} [64]), and T is the absolute temperature.

TABLE 3 | Parameters used to calculate κ_L in MATLAB.

ν (m s^{-1})	θ_D (K)	ω (10^{12} s^{-1})	A (10^{-42} s^3)	B (10^{-17} s K^{-1})	C (10^{-8} K^{-3})
2000	165	4.2	1.036	0.944	1.358

κ_L is examined using the Debye-Callaway model [65, 66], which has been extensively applied in thin-film studies [41, 44, 67, 68].

$$\kappa_L = \frac{k_B}{2\,\pi^2\,\nu}\left(\frac{k_B}{\hbar}\right)^3 T^3 \int_0^{\theta_D/T} \frac{\tau_c\, x^4\, e^x}{\left(e^x-1\right)^2}\, dx \tag{9}$$

$$\tau_c{}^{-1} = \frac{\nu}{D} + \frac{\nu}{t} + A\,\omega^4 + B\,\omega^2\,T\exp\left(-\frac{\theta_D}{3\,T}\right) + C\,\omega \tag{10}$$

where k_B is the Boltzmann constant (1.38×10^{-23} J K^{-1}), ν is the velocity of sound in the material, $\hbar$ is the reduced Planck constant (1.05×10^{-34} J s), T is the absolute temperature, θ_D is the Debye temperature dependent on the material, τ_c is the relaxation time, $\tau_c{}^{-1}$ is the overall relaxation rate, D is the crystallite size, t is the film thickness, ω is the phonon frequency dependent on the material, and coefficients of A, B, C are the temperature-independent lattice thermal conductivity fitting parameters.

In Equation (10), the first two terms denote boundary scattering, the third term represents the point-defect scattering, the fourth term represents the three-phonon Umklapp scattering, and the fifth term represents the carrier-phonon scattering [67]. It is reported that D mainly determines the change in κ_L [41, 67]. Hence, only D and t are experimentally measured in this study, while all other parameters are taken from published data referenced from [69, 70] (see Table 3):

4.4 | Fabrication and Characterization of Flexible Thermoelectric Generators

4.4.1 | Device Fabrication by Flexible Mask

A single n-type TEG [71] was fabricated by sputtering through shadow masks. The mask was made by laser cutting (TS 3040 40 W Laser Cutter) of flexible PET sheets because a flexible polymer mask can closely attach to the substrate, thus avoiding shadowing issues (i.e., an unclear pattern) as typically occurs with a solid stainless-steel mask. Figure S9 shows masks of the Bi-Te and Cu patterns. Cu strips behaved as a metal contact to connect TE strips in the plane, which was also made by sputtering in *Aerre Machine* vacuum R2R web coater (0.22 kW, 250 sccm Ar flow, 99.999% Cu target, *Mi-Net Technology Ltd.*).

4.4.2 | Seebeck Measurement

The fabricated TEG was assessed using a home-built Seebeck system, which applied a ΔT using two Peltier modules between the two ends of a TEG, and measured the power output with a simple external Ohm's circuit. The ΔT, ~11.4 K, considered the real situation of human body temperature, the ambient temperature, and the temperature loss at the contact between TEG and the human body. The resistance of the external load resistor varied from 0.84 to 30 kΩ, which covered the internal resistance of TEG in this study (to obtain the maximum power output when the internal resistance equals the load resistance [13]).

4.4.3 | COMSOL Simulation

TEG were simulated in COMSOL Multiphysics software using the module of heat transfer in solids under a stationary study, as detailed in [21]. Most of the material properties were taken directly from the materials library in COMSOL, while only S, ρ, and κ were adjusted according to the results obtained in this study. The dimensions of TEG and applied conditions were set to simulate the Seebeck measurement. There were three physical phenomena considered in this simulation: heat flux, surface-to-ambient radiation, and thermal contact.

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Conflicts of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section.

Supporting File 1: admt70729-sup-0001-SuppMat.docx.

Supporting File 2: admt70729-sup-0002 DataFile.docx.