

**Thermal Processes and their Impact on Surface Related Degradation**

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Surface Related Degradation (SRD) is a phenomenon whereby recombination in the near-surface region of silicon wafers increases under elevated temperatures with or without carrier injection. Because of its importance for solar cell processing and operation, SRD occurring under light soaking at temperatures between 80-200°C has recently attracted great interest. This letter looks at two post-firing processes that can affect the formation of SRD. The first is the replacement of the passivating dielectric layers and the second is the use of thermal annealing between 300-400°C. Post-firing etching and re-deposition of dielectric layers has minimal impact on subsequent degradation. In contrast, a thermal anneal at 400°C for 30 min can reduce the extent of SRD by a factor of 6. The implications of these results are that the interface between silicon and the dielectric itself is not the critical factor in the formation of SRD. The most likely explanation is that thermal processing causes an alteration in the silicon substrate that affects subsequent formation of SRD.

**1. Introduction**

Silicon solar cells are subject to several degradation mechanisms, whereby the effective carrier lifetime decreases with exposure to elevated temperatures and carrier injection.

Bulk degradation mechanisms such as the boron-oxygen defect (B-O)<sup>[1,2]</sup> and Light and elevated Temperature Induced Degradation (LeTID)<sup>[3,4]</sup> have received significant research and commercial attention. While the actual structure of these defects remains a point of debate, effective measures have been found to avoid or mitigate their impact on commercial devices.<sup>[5–10]</sup> More recently an additional degradation affecting silicon surfaces has been observed<sup>[11]</sup> and labelled Surface Related Degradation (SRD). SRD characteristically shows an initial degradation followed by a recovery in a similar manner to B-O and LeTID, albeit on a longer timescale. It has important implications for long term stability testing<sup>[12]</sup> and can reduce long-term performance for certain solar cell architectures in the field.<sup>[13–15]</sup>

SRD has been observed to affect silicon wafers passivated with plasma enhanced chemical vapour deposited (PECVD) silicon nitride ( $\text{SiN}_x\text{:H}$ ), thin thermal oxides capped with nitride ( $\text{SiO}_2/\text{SiN}_x\text{:H}$ ), and aluminium oxide (PECVD or atomic layer deposited (ALD)) capped with silicon nitride ( $\text{AlO}_x\text{:H}/\text{SiN}_x\text{:H}$ ,  $\text{Al}_2\text{O}_3/\text{SiN}_x\text{:H}$ ).<sup>[11,16]</sup> More recently there have been observations of a similar defect in structures using polysilicon/tunnel oxide passivating contacts.<sup>[13,14]</sup> The mechanism appears to differ between passivation schemes. Wafers passivated with  $\text{SiN}_x\text{:H}$  see an increase in recombination active defects at or near the surface, with no change in the fixed surface charge. In contrast, wafers passivated with  $\text{AlO}_x\text{:H}/\text{SiN}_x\text{:H}$  stacks see no increase in defect concentration but a significant decrease in fixed (negative) charge.<sup>[17]</sup>

The thermal history of the wafers plays a critical role in the evolution of SRD. In previous experiments SRD was only observed in wafers that have been subjected to a high temperature step in the presence of a hydrogen containing dielectric.<sup>[18,19]</sup> This has been taken as evidence for the potential involvement of hydrogen in SRD, in a similar manner to experiments looking at a link between hydrogen and LeTID.<sup>[20–22]</sup> An alternative explanation is that the thermal process affects the silicon/dielectric interface or the

dielectric itself in such a manner as to cause SRD. It is therefore important to establish which part of the structure is affected by thermal processes in such a way as to lead to SRD. Is it the dielectric, the dielectric/silicon interface, or the silicon itself?

It has been observed that extended post-firing anneals at temperatures between 300-400°C reduce the extent of LeTID.<sup>[8,9]</sup> Given the numerous parallels between SRD and LeTID it is also worth investigating whether such anneals affect SRD in a similar manner. There has already been one study in the literature by Hammann *et al.*<sup>[23]</sup> It was observed that firing with a maximum temperature of 800°C resulted in a slower formation rate for SRD. Anneals at lower temperatures, either post-firing or with no firing, had negligible impact. However, both this study and another by the same group<sup>[24]</sup> show both LeTID and SRD in unfired samples. This contrasts with the majority of observations in the literature,<sup>[13,18,19]</sup> and may be a result of the specific direct plasma PECVD nitrides used. It is therefore proposed to investigate post-firing annealing on samples which do not exhibit SRD without a firing step.

The two questions this letter will attempt to address are thus:

- 1) Is SRD after firing related to changes in the dielectric and/or interface itself, or linked to changes in the silicon substrate?
- 2) Can post-firing annealing in the 300-400°C temperature range affect SRD in samples that exhibit no SRD when un-fired?

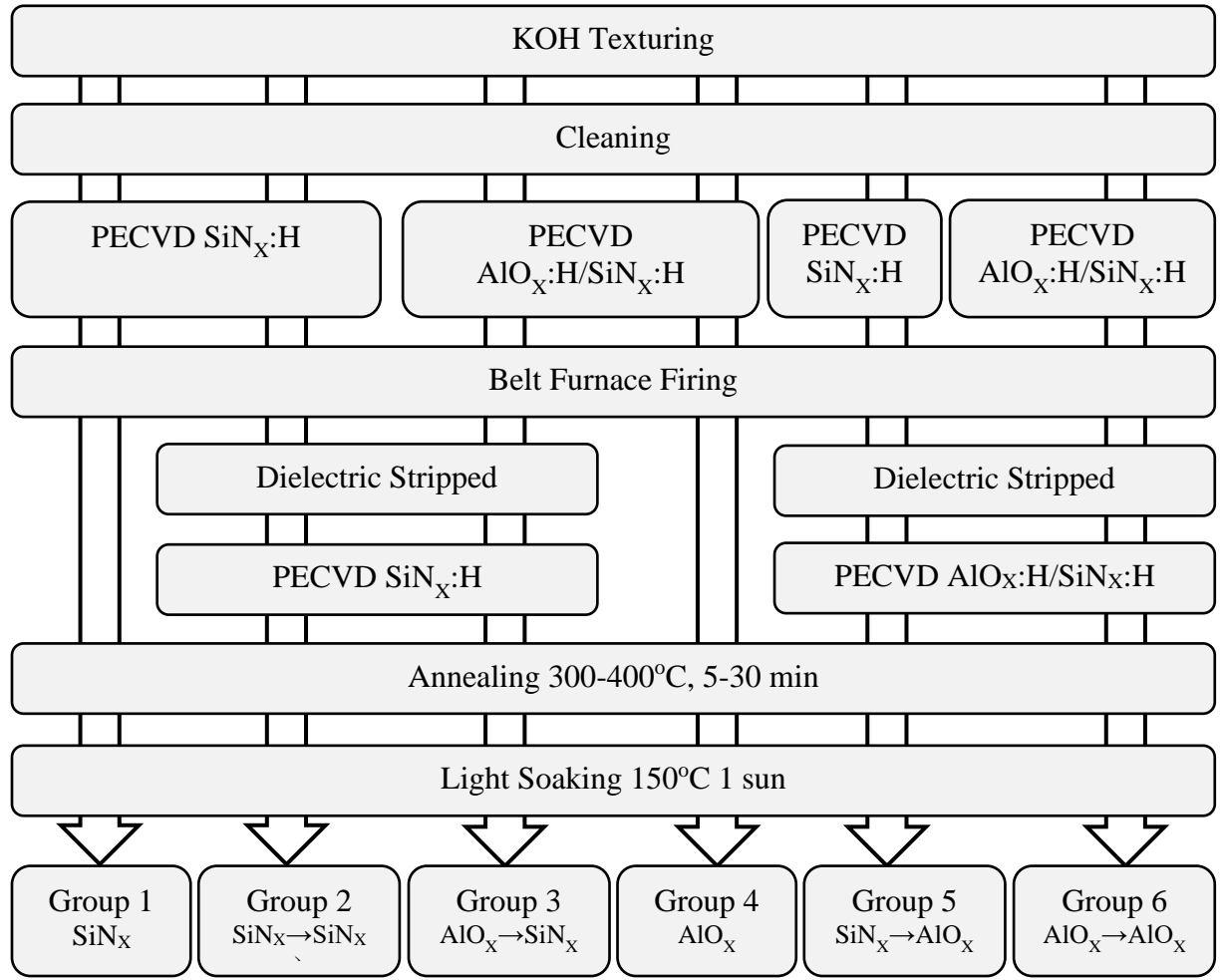
## 2. Methodology

Figure 1 presents the workflow for the experiments in this paper. 156×156 mm 1.6 Ω.cm boron doped p-type Czochralski silicon wafers were used. The wafers were textured in a KOH/IPA solution to remove saw damage and texture both surfaces. They were then given an RCA2 clean followed by a HF dip to remove any native oxide before dielectric deposition.

All dielectric depositions were carried out in a Meyer Burger MAiA remote PECVD tool. Half of the wafers (Groups 1,2,5) were coated with SiN<sub>x</sub>:H at a set point of 400°C, with a target thickness of 75 nm and refractive index (RI) of 2.08. The other wafers (Groups 3,4,6) were coated with an AlO<sub>x</sub>:H/SiN<sub>x</sub>:H stack. The AlO<sub>x</sub>:H layer was deposited at a set point of 400°C with a target thickness of 24 nm and RI of 1.588, while the SiN<sub>x</sub>:H layer was deposited at a set point of 350°C with a target thickness of 80 nm and RI of 2.08. The dielectric deposition parameters match those used in a previous study, which demonstrated no significant SRD without firing.<sup>[18]</sup>

All wafers were fired in a Meyer Burger Camini belt firing furnace with a peak firing set temperature of 855°C. The dielectric layers of wafers from Groups 2,3,5 and 6 were then stripped in a HF solution. Groups 2 and 3 were then re-coated with a SiN<sub>x</sub>:H layer, while groups 5 and 6 had a fresh AlO<sub>x</sub>:H/SiN<sub>x</sub>:H stack deposited. In both cases deposition parameters were identical to those used initially.

Wafers were then laser cleaved into 52×52 mm lifetime samples for annealing and light soaking. A hotplate was used to anneal samples from each group at temperatures of 300, 350 and 400°C for 5 or 30 minutes in the dark. Annealed and non-annealed samples were then light soaked in a GSola GCD-4 LID Test chamber at 150°C under 1 sun equivalent illumination.



**Figure 1.** Flowchart for sample preparation and final sample groups

The injection dependent effective carrier lifetime was measured ex-situ throughout light soaking using a Sinton Instruments WCT-120 lifetime tester. Measurements were taken with the 1/1 flash and analyzed using the generalized method.<sup>[25]</sup> In order to allow a reasonable comparison between structures with differing initial lifetimes the concept of lifetime equivalent defect density ( $\Delta N_{leq}$ ), also known as normalized defect density,<sup>[26]</sup> is used:

$$\Delta N_{leq} = \frac{1}{\tau_{eff}} - \frac{1}{\tau_{eff.initial}}$$

In this work  $\tau_{eff.initial}$  is taken to be the highest effective lifetime measured either before or during light soaking. In the case of samples passivated with  $\text{SiN}_x\text{:H}$  this occurred within the first 2 hours of light soaking, whereas for samples passivated with  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  stacks the situation was more complicated. Because SRD has the greatest effect on effective lifetime at high injection levels, and to avoid trapping effects,  $\Delta N_{leq}$  was calculated at a minority carrier density (MCD) of  $1 \times 10^{16} \text{ cm}^{-3}$  in this work.

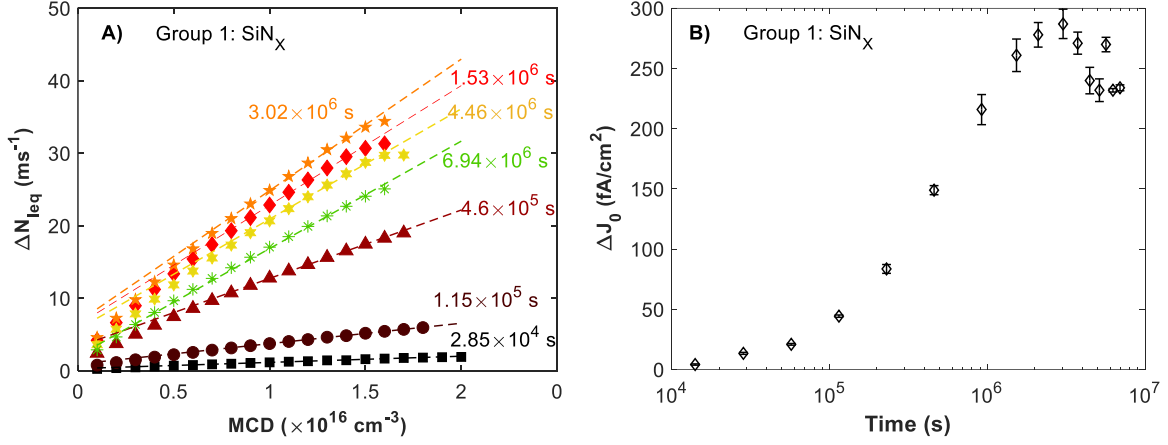
### 3. Results

#### 3.1. Separating Surface and Bulk Degradation

In the presence of multiple degradation mechanisms, it is important to establish to what extent each affects  $\Delta N_{leq}$ . Boron doped Cz wafers can potentially be affected by both the B-O defect and LeTID. B-O degradation and recovery typically takes place on a much shorter (<30 minutes at  $150^\circ\text{C}$ ) timescale than SRD, however SRD degradation can overlap with the recovery process for LeTID.

The calculated  $\Delta N_{leq}$  as a function of minority carrier density for samples with a single  $\text{SiN}_x\text{:H}$  layer (Group 1) is shown in Figure 2A. Degradation due to LeTID would manifest as a preferential increase in  $\Delta N_{leq}$  at low injection levels, which was not observed. Instead, the curves were reasonably well described by a  $\Delta J_0$ , as per the work of Herguth.<sup>[26]</sup> This  $\Delta J_0$  was obtained through a linear fit to the data through minority carrier densities of  $8 \times 10^{15}$ - $1.5 \times 10^{16} \text{ cm}^{-3}$  and is presented as a function of time in Figure 2B.

At low injection levels there was a deviation of the calculated  $\Delta N_{leq}$  from the  $\Delta J_0$  fit. This was likely due to trapping and appears to increase along with the extent of SRD. This is an interesting topic for further investigation but was not material to the questions addressed in this paper.



**Figure 2.** A) Calculated  $\Delta N_{leq}$  as a function of MCD for samples passivated with a  $\text{SiN}_x\text{:H}$  layer on both sides and B) Extracted  $\Delta J_0$  for each time step. Error bars reflect the combined uncertainty in measurement ( $\pm 1\%$ ) and confidence bounds on fit.

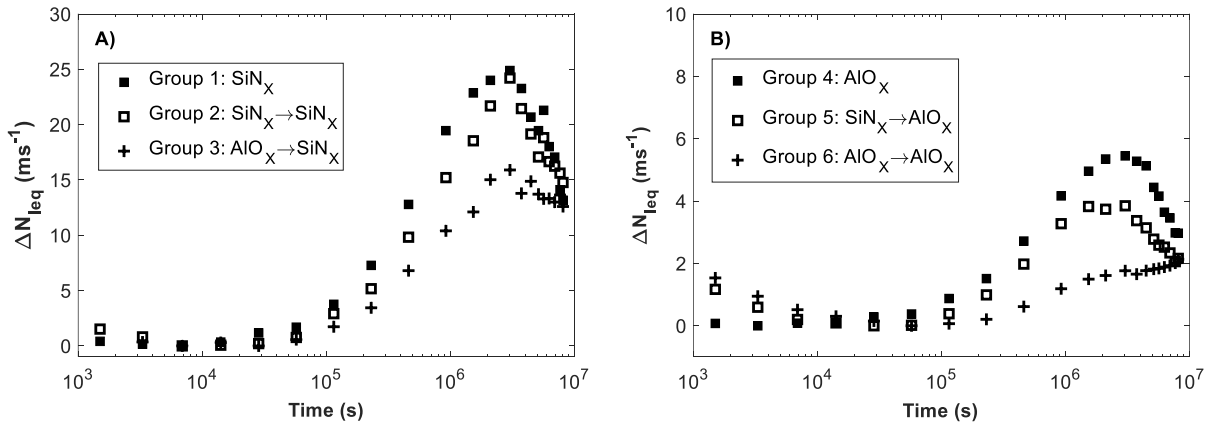
These results provide confidence that the degradation observed in this work are dominated by surface effects, particularly when  $\Delta N_{leq}$  was determined at a minority carrier density of  $1 \times 10^{16} \text{ cm}^{-3}$  or above.  $\Delta J_0$  is an alternate metric that could be used in some cases, however SRD in samples with  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  stacks is not well described by  $J_0$  fitting<sup>[16]</sup> and the metric also fails to capture all the effects occurring when there is a distribution of defects extending beyond the interface itself.<sup>[27]</sup>

### 3.2. Etching and Re-depositing dielectric layers

Figure 3 presents  $\Delta N_{leq}$  for samples where the passivation layer during light soaking was A)  $\text{SiN}_x\text{:H}$  and B)  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$ . The sample from group 1 with no replacement of the  $\text{SiN}_x\text{:H}$  dielectric exhibits a typical degradation followed by recovery, with the maximum degradation extent occurring at  $\sim 3 \times 10^6 \text{ s}$ . The group 2 sample where the  $\text{SiN}_x\text{:H}$  was replaced after firing shows nearly identical behaviour. In the group 3 sample where the  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  present during firing was replaced with  $\text{SiN}_x\text{:H}$  a slightly lower maximum extent of SRD was observed. The behaviour was otherwise similar.

In the case of samples shown in Figure 3B, measurements of groups 5 and 6 are affected by an improvement of surface passivation during light soaking, most noticeably for times less than  $1 \times 10^4$  s. This is consistent with the activation of  $\text{AlO}_x\text{:H}$  passivation via thermal annealing.<sup>[28]</sup> We have chosen to calculate  $\Delta N_{\text{leq}}$  using the time at which the measured effective lifetime was greatest. However, for samples from groups 5 and 6 this occurs when SRD is already affecting the effective lifetime. This acts to slightly reduce the measured  $\Delta N_{\text{leq}}$ . We therefore conclude that group 5, which had a  $\text{SiN}_x\text{:H}$  layer present during firing which was replaced with  $\text{AlO}_x\text{:H}/\text{SiN}_x\text{:H}$  stack before light soaking, exhibits similar behaviour and maximum extent of SRD to group 4, where the  $\text{AlO}_x\text{:H}/\text{SiN}_x\text{:H}$  stack present during firing was not replaced. This is consistent with the result in Figure 3A for  $\text{SiN}_x\text{:H}$ . Where an  $\text{AlO}_x\text{:H}/\text{SiN}_x\text{:H}$  layer was deposited before and after firing there does not appear to be any recovery process after  $3 \times 10^6$  seconds. This is likely an artifact which will be discussed in more detail in section 3.2.

It was noted that the maximum  $\Delta N_{\text{leq}}$  is much lower for samples passivated with  $\text{AlO}_x\text{:H}/\text{SiN}_x\text{:H}$  than for those passivated with  $\text{SiN}_x\text{:H}$ . This was true regardless of the minority carrier density at which  $\Delta N_{\text{leq}}$  is calculated. This was most likely an effect of the different SRD mechanisms for  $\text{SiN}_x\text{:H}$  and  $\text{AlO}_x\text{:H}/\text{SiN}_x\text{:H}$ . However, both dielectric schemes demonstrated degradation and recovery with nearly identical timescales.



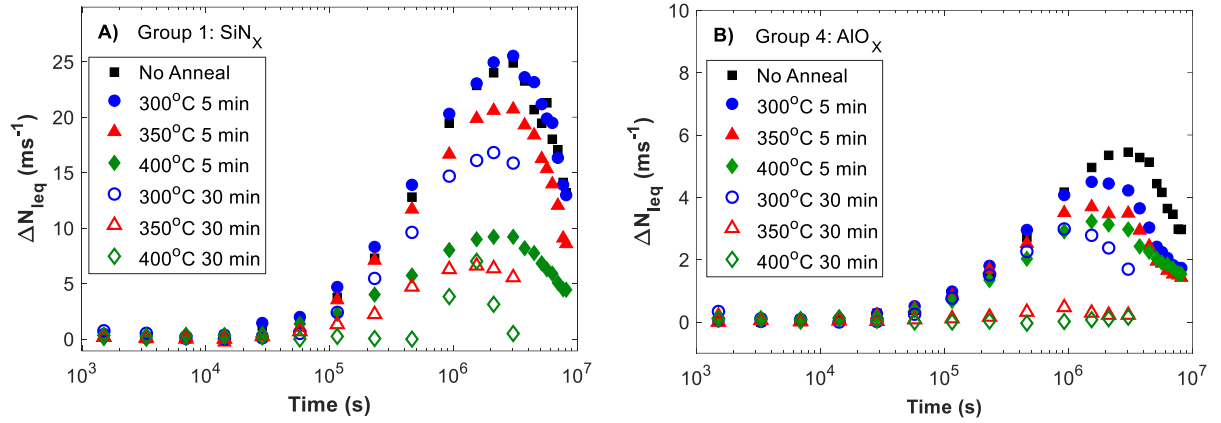


**Figure 3.**  $\Delta N_{leq}$  calculated at an MCD of  $1 \times 10^{16} \text{ cm}^{-3}$  during light soaking at  $150^\circ\text{C}$  and 1 sun for A) samples passivated with a  $\text{SiN}_x\text{:H}$  layer on both sides and B) samples passivated with an  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  dielectric stack on both sides.

### 3.3. Effect of post-firing anneals

Figure 4 shows  $\Delta N_{leq}$  for samples with no post-firing anneal and samples annealed for between 5-30 minutes at  $300\text{-}400^\circ\text{C}$ . For both  $\text{SiN}_x\text{:H}$  and  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  dielectric stacks the maximum extent of SRD is reduced with an increase in post-firing anneal temperature. The primary effect on samples passivated with  $\text{SiN}_x\text{:H}$  is a reduction in the maximum extent of SRD. The maximum  $\Delta N_{leq}$  for samples with no anneal was  $25.5 \text{ ms}^{-1}$  c.f.  $6.6 \text{ ms}^{-1}$  for a sample annealed at  $350^\circ\text{C}$  for 30 minutes. The kinetics appear otherwise unchanged. The exception is the samples annealed at  $400^\circ\text{C}$  for 30 minutes, which showed very little degradation over most of the measurement period and then a sudden spike up to an  $\Delta N_{leq}$  of  $7.0 \text{ ms}^{-1}$  at  $1.5 \times 10^6 \text{ s}$ . It is highly possible that this was a measurement error, with these samples having a maximum  $\Delta N_{leq}$  of  $3.8 \text{ ms}^{-1}$  if this measurement is ignored.

For samples passivated with  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  there appears to have been a change in the rate of recovery, with the maximum extent of degradation occurring at earlier times with longer light soaking. In this case the sample annealed at  $400^\circ\text{C}$  for 30 minutes showed no significant SRD at all, with a maximum  $\Delta N_{leq}$  of  $0.15 \text{ ms}^{-1}$ . For both cases  $\text{SiN}_x\text{:H}$  and  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  there was a clear trend of reduced degradation with increasing thermal budget, with higher temperatures and longer anneals clearly providing the greatest benefits.

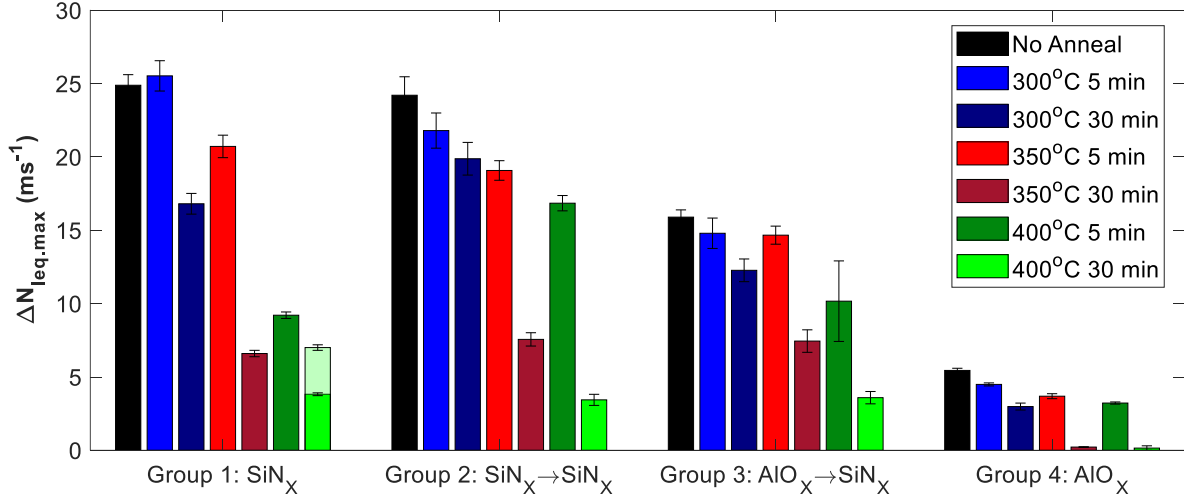


**Figure 4.**  $\Delta N_{\text{leq}}$  calculated at an MCD of  $1 \times 10^{16} \text{ cm}^{-3}$  during light soaking at  $150^\circ\text{C}$  and 1 sun for samples with A)  $\text{SiN}_x\text{:H}$  passivation and B)  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  passivation with no replacement of dielectrics post firing. Result are presented for samples with no post-firing anneal (black squares), with post firing thermal anneals for 5 minutes (closed symbols) and 30 min (open symbols) at  $300^\circ\text{C}$  (blue circles),  $350^\circ\text{C}$  (red triangles) and  $400^\circ\text{C}$  (green diamonds).

Figure 5 shows the maximum equivalent defect density  $\Delta N_{\text{leq,max}}$  during light soaking for samples from groups 1-4 when annealed between  $300\text{--}400^\circ\text{C}$  for 5 or 30 minutes. Here it is demonstrated that the reduction in the maximum  $\Delta N_{\text{leq}}$  seen in Figure 3 was replicated for samples from groups 2 and 3 in which the dielectric was replaced with  $\text{SiN}_x\text{:H}$  after firing. In both cases the lowest extent of degradation was observed for samples annealed at  $400^\circ\text{C}$  for 30 minutes.  $\Delta N_{\text{leq,max}}$  went from  $21.8 \text{ ms}^{-1}$  (no anneal) to  $3.4 \text{ ms}^{-1}$  ( $400^\circ\text{C}$  30 min) for samples with  $\text{SiN}_x\text{:H}$  present during firing and  $14.8 \rightarrow 4.0 \text{ ms}^{-1}$  for samples with  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  present during firing. Annealing at  $350^\circ\text{C}$  for 30 minutes was also sufficient to more than halve the extent of SRD in all cases.

One point for additional consideration is how the thermal budget of the dielectric deposition process affected SRD mitigation. An example temperature profile for the deposition of an  $\text{AlO}_x\text{:H}$  layer (without nitride) is provided in supporting information. According to this graph and the process details for the other depositions samples were estimated to spend between 5-10 minutes at temperatures between  $300\text{--}360^\circ\text{C}$  during depositions. The degree of uncertainty was too great to be explicit on the expected impact,

but it is an open question as to whether surface conditions during the annealing process are important for SRD mitigation.

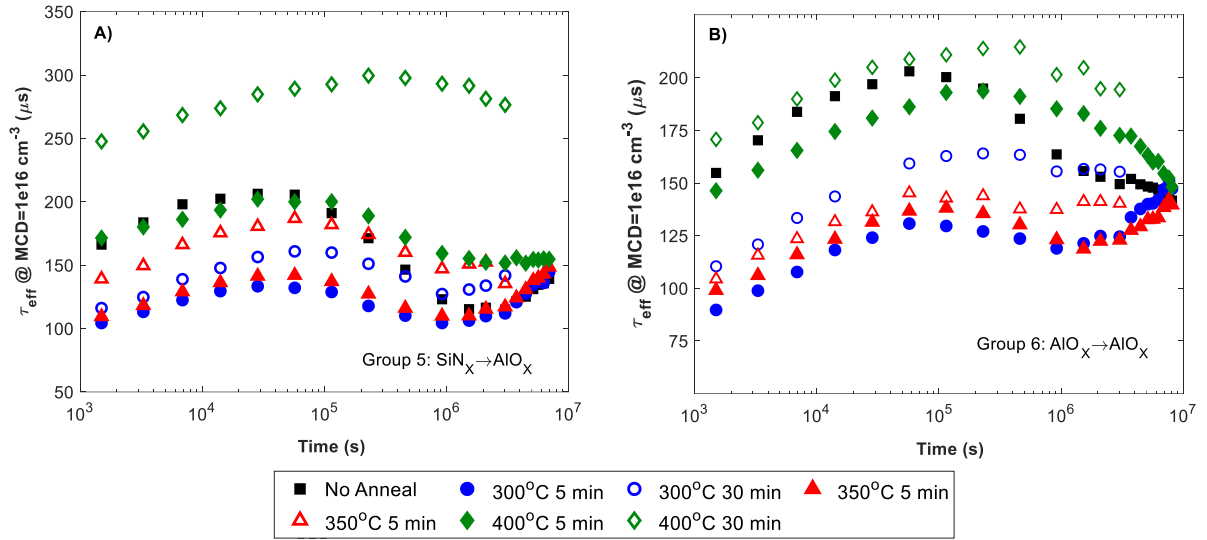


**Figure 5.** Maximum change in lifetime equivalent defect density  $\Delta N_{\text{leq,max}}$  calculated at an MCD of  $1 \times 10^{16} \text{ cm}^{-3}$  during light soaking for samples annealed between 300–400°C for 5–30 minutes. Results are presented for groups 1–4. For the group 1 SiN<sub>x</sub> samples  $\Delta N_{\text{leq,max}}$  is shown with and without the anomalous measurement (lighter green segment). Error bars reflect measurement uncertainty ( $\pm 1\%$ ) and uncertainty in maximum lifetime (lifetime spread in first 2 hours of measurement).

In samples where the dielectric was replaced with AlO<sub>x</sub>:H/SiN<sub>x</sub>:H after firing the behaviour is more complicated. Figure 6 shows the effective lifetime measured at an MCD of  $1 \times 10^{16} \text{ cm}^{-3}$  for samples from groups 5 and 6 where the dielectrics present during firing were replaced with another AlO<sub>x</sub>:H/SiN<sub>x</sub>:H stack before annealing and light soaking. It is readily apparent that there were at least two effects at work. Because SRD in samples passivated with AlO<sub>x</sub>:H/SiN<sub>x</sub>:H is not well described by a simple  $\Delta J_0$  accurate separation of these effects is difficult.

A degradation effect at a time of around  $2 \times 10^6 \text{ s}$  was visible in some cases, which we have interpreted as the effect of SRD. A second effect was possibly the activation of the surface passivation by AlO<sub>x</sub>:H. This effect was expected to be most pronounced for samples that were not previously annealed, since annealing at 300–400°C should at least partially activate the passivation.<sup>[28]</sup> However, it appears that post-firing anneals at 300°C and

350°C lead to a decrease in initial effective lifetime, while the effective lifetime of samples that were not annealed and those annealed at 400°C were similar. At the end of the light soaking process all samples (excepting those annealed at 400°C for 30 minutes) showed very similar effective lifetimes, suggesting that the effects of SRD at this point were minimal compared with other effects. More work is required to accurately describe the different effects observed, but it is reasonable to suggest that the samples annealed at 400°C, as well as those annealed for 30 minutes at 300 and 350°C, displayed less SRD effects than the other samples.



**Figure 6.** Effective lifetime measured at an MCD of  $1 \times 10^{16} \text{ cm}^{-3}$  for samples from A) group 5 ( $\text{SiN}_x \rightarrow \text{SiN}_x$ ) and B) group 6 ( $\text{AlO}_x \rightarrow \text{AlO}_x$ ) during light soaking.

#### 4. Discussion

There are three primary observations from the results in section 3. They are:

1. While the extent of SRD differs between samples passivated with  $\text{SiN}_x\text{:H}$  and  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  stacks, there is negligible difference in the time constants of the SRD process.
2. SRD still occurs in fired samples when the dielectric present during firing is etched off and replaced with a new passivation stack. In the case of samples fired with a  $\text{SiN}_x\text{:H}$  layer present the subsequent degradation is similar in magnitude to that

observed with the original dielectric in place. For samples fired with an  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  stack the subsequent degradation is noticeably reduced.

3. Post-firing annealing at temperatures between 300-400°C suppresses SRD, with the extent of suppression increasing with thermal budget.

The first point is unsurprising as it has already been reported that the mechanism of SRD differs between  $\text{SiN}_x\text{:H}$  and  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  stacks.<sup>[29]</sup> However, the fact that the rate constants and behavior with annealing remain similar provides evidence that there is a common root cause.

The second observation provides evidence that the common cause is due to a change in the substrate during firing, rather than any change in the dielectric or silicon/dielectric interface. This is evident from a comparison of unfired samples, which generally do not demonstrate SRD,<sup>[18]</sup> with samples with dielectrics replaced after firing which show significant SRD. This requirement for firing is a point of similarity between SRD and LeTID. In the case of LeTID this has been taken as evidence for the involvement of hydrogen in the bulk in the process of defect formation.<sup>[20–22]</sup> This provides support for the suggestion that hydrogen is involved in SRD,<sup>[16]</sup> as does the slightly lower extent of SRD observed when samples are fired with  $\text{AlO}_x\text{:H/SiN}_x\text{:H}$  stacks compared to  $\text{SiN}_x\text{:H}$  alone. Importantly, these results would indicate that it is hydrogen in the bulk, not in the dielectric layers, that is most critical for SRD formation.

Another similarity between SRD and LeTID appears in their response to post-firing anneals. Post-firing thermal processes have been demonstrated to suppress LeTID,<sup>[8–10]</sup> and in this paper a corresponding suppression of SRD is observed for such processes. The thermal budgets required for effective suppression of SRD appears to be slightly higher than those needed for LeTID. It has been reported that LeTID can be almost eliminated with annealing for less than 30 minutes at 400°C.<sup>[8,30]</sup> In contrast noticeable SRD is still present after the same treatment.

Previous reports in the literature have seen no suppression of SRD in direct PECVD nitride passivated samples through thermal annealing.<sup>[23,24]</sup> In contrast, annealing at 400°C was found to improve both the passivation and subsequent stability of n-type wafers with polysilicon/tunnel oxide passivation.<sup>[14]</sup> This suggests that the passivation scheme is important for the response to post-firing annealing. Further work is required to determine what the critical parameters for this process might be.

This evidence is all consistent with a model the authors have previously proposed whereby hydrogen in the bulk redistributes to the surface during light soaking.<sup>[18,31]</sup> A build-up of hydrogen at the surface has been widely reported to lead to defect formation,<sup>[32,33]</sup> and an effect on effective lifetime was explained by Steingrube *et al.*<sup>[27]</sup> using a defect profile that extended beyond the surface. However, this is in apparent contradiction to at least two reports in the literature where nitride passivated p-type silicon substrates were light soaked until SRD reached its maximum extent, the dielectrics were then stripped and replaced with room temperature chemical passivation resulting in a completely recovered lifetime.<sup>[19,34]</sup> One factor to consider is that the chemical passivation methods used, iodine/ethanol and superacid,<sup>[35]</sup> have been reported to induce an increase in surface hole concentration in the underlying silicon.<sup>[36,37]</sup> This means that the p-type surfaces would be in accumulation, rather than the inversion caused by the presence of SiN<sub>x</sub>:H. In general, this would be expected to reduce the rate of recombination in the near surface region during measurement. However, the fitting of Steingrube *et al.*<sup>[27]</sup> found a carrier lifetime ratio  $\tau_n/\tau_p$  of  $6.4 \times 10^{-2}$  for the near surface defect. In this case recombination where electrons are the minority carriers (accumulation) should not be vastly reduced from when holes are the minority carriers (inversion). Using a different defect profile to the exponential distribution previously assumed<sup>[27]</sup> might result in a different extracted  $\tau_n/\tau_p$ , thus resolving this contradiction.

#### 4. Conclusion

In this paper we have shown that SRD occurs even when the dielectric present during firing is replaced before light soaking. Furthermore, we have shown that in some cases it is possible to greatly reduce the effects of SRD through post-firing dark anneals at temperatures between 350-400°C. These results demonstrate that the firing process alters something within the silicon substrate itself to make the structure susceptible to SRD. They also show how thermal treatments can be used to manipulate subsequent formation of SRD in a similar manner to post-fire treatments for LeTID.

## 5. Acknowledgements

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## 6. References

- [1] J. Schmidt, A.G. Aberle, and R. Hezel, in *Conference Record of the Twenty Sixth IEEE Photovoltaic Specialists Conference-1997* (1997), pp. 13–18.
- [2] J. Schmidt and K. Bothe, *Physical Review B* **69**, 24107 (2004).
- [3] K. Ramspeck, S. Zimmermann, H. Nagel, A. Metz, Y. Gassenbauer, B. Brikmann, and A. Seidl, in *Proceedings of the 27th European Photovoltaic Solar Energy Conference*, pp. 861–865, (2012).
- [4] F. Kersten, P. Engelhart, H.C. Ploigt, A. Stekolnikov, T. Lindner, F. Stenzel, M. Bartzsch, A. Szpeth, K. Petter, J. Heitmann, and J.W. Muller, *2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, pp 1-5, (2015).
- [5] B. Hallam, A. Herguth, P. Hamer, N. Nampalli, S. Wilking, M. Abbott, S. Wenham, and G. Hahn, *Applied Sciences*, **8**, 10, (2017).
- [6] A. Herguth, G. Schubert, M. Kaes, and G. Hahn, in *2006 IEEE 4th World Conference on Photovoltaic Energy Conference*, pp. 940–943, (2006)
- [7] P. Hamer, B. Hallam, M. Abbott, C. Chan, N. Nampalli, and S. Wenham, *Solar Energy Materials and Solar Cells* **145**, pp. 440-446, (2016).

- [8] C. Sen, M. Kim, D. Chen, U. Varshney, S. Liu, A. Samadi, A. Ciesla, S.R. Wenham, C.E. Chan, and C. Chong, *IEEE Journal of Photovoltaics* **9**, 40 (2018).
- [9] M. Yli-Koski, M. Serué, C. Modanese, H. Vahlman, and H. Savin, *Solar Energy Materials and Solar Cells* **192**, 134 (2019).
- [10] R. Eberle, W. Kwapil, F. Schindler, S.W. Glunz, and M.C. Schubert, *Energy Procedia*, pp. 712–717, (2017).
- [11] D. Sperber, A. Herguth, and G. Hahn, *Energy Procedia* **92**, 211 (2016).
- [12] D. Sperber, A. Graf, A. Heilemann, A. Herguth, and G. Hahn, *Energy Procedia* **124**, 794 (2017).
- [13] D. Kang, H.C. Sio, D. Yan, W. Chen, J. Yang, J. Jin, X. Zhang, and D. Macdonald, *Solar Energy Materials and Solar Cells* **215**, 110691 (2020).
- [14] M. Winter, S. Bordihn, R. Peibst, R. Brendel, and J. Schmidt, *IEEE Journal of Photovoltaics* **10**, 423 (2020).
- [15] A. Herguth, C. Derricks, and D. Sperber, *IEEE Journal of Photovoltaics* **8**(5), 1190-1201 (2018).
- [16] D. Sperber, A. Graf, D. Skorka, A. Herguth, and G. Hahn, *IEEE Journal of Photovoltaics* **7**, 1627 (2017).
- [17] D. Sperber, A. Schwarz, A. Herguth, and G. Hahn, *Solar Energy Materials and Solar Cells* **188**, 112 (2018).
- [18] K. Kim, R. Chen, D. Chen, P. Hamer, A. Ciesla Nee Wenham, S. Wenham, and Z. Hameiri, *IEEE Journal of Photovoltaics* **9**, 97 (2019).
- [19] D. Sperber, F. Furtwängler, A. Herguth, and G. Hahn, *Proceedings of the 32nd European Photovoltaic Solar Energy Conference and Exhibition* 523 (2016).
- [20] M.A. Jensen, A. Zuschlag, S. Wiegold, D. Skorka, A.E. Morishige, G. Hahn, and T. Buonassisi, *Journal of Applied Physics* **124**, 085701 (2018).
- [21] D. Bredemeier, D.C. Walter, R. Heller, and J. Schmidt, *Physica Status Solidi - Rapid Research Letters* **1900201**, 1 (2019).
- [22] A. Ciesla, S. Wenham, R. Chen, C. Chan, D. Chen, B. Hallam, D. Payne, T. Fung, M. Kim, and S. Liu, in *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC)* (2018), pp. 1–8.
- [23] B. Hammann, J. Engelhardt, D. Sperber, A. Herguth, and G. Hahn, *IEEE Journal of Photovoltaics* **10**, 85 (2020).
- [24] D. Sperber, F. Furtwängler, A. Herguth, and G. Hahn, in *AIP Conference Proceedings* (2019), p. 140011.
- [25] H. Nagel, C. Berge, A.G. Aberle, H. Nagel, C. Berge, and A.G. Aberle, *Journal of Applied Physics* **86**, 6218 (1999).
- [26] A. Herguth, *IEEE Journal of Photovoltaics* **9**, 1182 (2019).
- [27] S. Steingrube, P.P. Altermatt, D.S. Steingrube, J. Schmidt, and R. Brendel, *Journal of Applied Physics* **108**, 14506 (2010).
- [28] P. Saint-Cast, D. Kania, M. Hofmann, J. Benick, J. Rentsch, and R. Preu, *Applied Physics Letters* **95**, 151502 (2009).
- [29] D. Sperber, A. Schwarz, A. Herguth, and G. Hahn, *Solar Energy Materials and Solar Cells* **188**, 112 (2018).
- [30] P. Hamer, H. Li, C. Chan, C. Sen, R.S. Bonilla, and P. Wilshaw, in *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC)*, (2018), pp. 1682–1686.
- [31] D. Chen, P.G. Hamer, M. Kim, T.H. Fung, G. Bourret-Sicotte, S. Liu, C.E. Chan, A. Ciesla, R. Chen, M.D. Abbott, B.J. Hallam, and S.R. Wenham, *Solar Energy Materials and Solar Cells* **185**, (2018).
- [32] N.M. Johnson, F.A. Ponce, R.A. Street, and R.J. Nemanich, *Physical Review B* **35**, 4166 (1987).



- [33] N.H. Nickel, G.B. Anderson, N.M. Johnson, and J. Walker, *Physical Review B* **62**, 8012 (2000).
- [34] D. Sperber, A. Heilemann, A. Herguth and G. Hahn, *IEEE Journal of Photovoltaics* **7**, 463 (2017).
- [35] N.E. Grant, T. Niewelt, N.R. Wilson, E.C. Wheeler-Jones, J. Bullock, M. Al-Amin, M.C. Schubert, A.C. van Veen, A. Javey, and J.D. Murphy, *IEEE Journal of Photovoltaics* **7**, 1574 (2017).
- [36] A.I. Pointon, N.E. Grant, R.S. Bonilla, E.C. Wheeler-Jones, M. Walker, P.R. Wilshaw, C.E.J. Dancer, and J.D. Murphy, *ACS Applied Electronic Materials* **1**, 1322 (2019).
- [37] N.E. Grant and J.D. Murphy *Physica Status Solidi – Rapid Research Letters* **11**(11) 1700243 (2017).