Exploiting Ion-Charged Dielectrics for High Efficiency Solar Cell Architectures

by

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The secret of getting ahead is getting started.
Mark Twain

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Abstract

This thesis studies the production and performance of p-type inversion layer (IL) Si solar cells. IL cells use an electric field to induce an inversion layer and create a *pn* junction. Compared with the mainstream diffused *pn* junctions, the advantages of field-induced junctions include lower fabrication costs and less carrier recombination. IL cells have been studied since the 1970s. In previous work, intrinsic charge in dielectric materials has been used to induce the inversion layer. However, the charge density was not high enough to induce a sufficiently conductive junction emitter (n-type surface layer). In this thesis, a field and temperature-assisted ion migration method was used to incorporate a controllable amount of positive ionic charge into dielectric thin films and fully exploit IL cells.

The ion migration method was first used to induce an electron accumulation layer on n-type substrates. The lowest accumulation layer sheet resistance (R_{sh}) obtained is 950 Ω/sq, which is the lowest reported in the literature. A model was developed in Sentaurus TCAD to study the formation and properties of field-induced layers. The simulation results suggested that the R_{sh} is determined by charge density, band-tail interface state density, and illumination. With optimised charge density and interface parameters, the lowest IL R_{sh} that can be achieved in the dark is 1.1 kΩ/sq. Although such R_{sh} is ~7 times higher than that of typical n-type phosphorous-diffused emitters (150 Ω/sq), the cell performance evaluated by device simulations is not limited by the high R_{sh}. The simulation model comprises a field-induced emitter and a PERC-like structure at the rear. The best simulated IL cell shows an efficiency of 24.8%, comparable to the best predicted for PERC. This indicates that field-induced emitters can perform as well as P-diffused emitters.

Proof-of-concept IL cells were fabricated via laser doping, annealing, ion migration, and light-assisted electroplating. The formation and uniformity of the field-induced emitter were confirmed by taking a photocurrent map of the IL cell. The champion cell presents an efficiency of 10.8%, demonstrating that IL cells can be fabricated using the ion migration method. Although the efficiency is low, simulation results suggest that an efficiency of as high as 24.8% can be achieved with optimised processing. With low fabrication costs and high potential cell efficiencies, field-induced emitters can become competitive alternatives to P-diffused emitters in commercial applications.

Preface

This thesis is an account of the work I have carried out as a postgraduate student at the Department of Materials, University of Oxford. I have not previously submitted any part of this thesis for a degree at this University or elsewhere. The work of other authors is duly acknowledged in the text, and appropriate references are given.

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I. Al-Dhahir, X. Niu, **M. Yu**, S. McNab, Y. Lin, P.P. Altermatt, C.E. Patrick, R.S. Bonilla, Ion-Charged Dielectric Nanolayers for Enhanced Surface Passivation in High Efficiency Photovoltaic Devices, Adv. Mater. Interfaces. In press.

M. Yu, M. Wright, J. Chen, Y. Shi, B. Hallam, E. Hwu, N. Grant, P. Wilshaw, S. Bonilla, Towards High Efficiency Inversion Layer Cells Based on Ion-Charged Dielectrics, in: WCPEC-8 Proc., 2022.

M. Yu, M. Wright, S. McNab, I. Al-Dhahir, P. Pietro, R.S. Bonilla, Probing the Interface State Densities Near Band Edges from Inductively Coupled Measurements of Sheet Resistance, in: AIP Conf. Proceedings, Silicon PV Conf., 2022.

I. Al-Dhahir, R. Kealy, S. Kelly, **M. Yu**, S. McNab, K. Collett, J. Liu, C. Grovenor, P.R. Wilshaw, R.S. Bonilla, Electrostatic Tuning of Ionic Charge in SiO2 Dielectric Thin Films, ECS J. Solid State Sci. Technol. 11 (2022) 063010.

S. McNab, **M. Yu**, I. Al-Dhahir, E. Khorani, T. Rahman, S. Boden, P. Altermatt, P. Wilshaw, R. Bonilla, Alternative Dielectrics for Hole Selective Passivating Contacts and the Influence of Nanolayer Built-In Charge, AIP Conf. Proceedings, Silicon PV Conf. (2021).

Y. Shi, M. Voss, **M. Yu**, E.T. Hwu, R.S. Bonilla, NanoLBIC Characterisation of Silicon Solar Cells Based on a Blue Laser Pick-up Unit, in: AIP Conf. Proceedings, Silicon PV Conf., 2021.

I. Al-Dhahir, S. McNab, **M. Yu**, E. Shaw, P. Hamer, R. Bonilla, The Influence of Surface Electric Fields on the Chemical Passivation of Si-SiO2 Interfaces after Firing, in: AIP Conf. Proceedings, Silicon PV Conf., 2021.

M. Yu, S. McNab, I. Al-Dhahir, C.E. Patrick, P.P. Altermatt, R.S. Bonilla, Extracting band-tail interface state densities from measurements and modelling of space charge layer resistance, Sol. Energy Mater. Sol. Cells. 231 (2021) 111307.

M. Yu, Y. Shi, J. Deru, I. Al-Dhahir, S. McNab, D. Chen, M. Voss, E. Te Hwu, A. Ciesla, B. Hallam, P. Hamer, P.P. Altermatt, P. Wilshaw, R.S. Bonilla, Assessing the Potential of Inversion Layer Solar Cells Based on Highly Charged Dielectric Nanolayers, Phys. Status Solidi - Rapid Res. Lett. 15 (2021).

M. Yu, R. Zhou, P. Hamer, D. Chen, X. Zhang, P.P. Altermatt, P.R. Wilshaw, R.S. Bonilla, Imaging and quantifying carrier collection in silicon solar cells: A submicron study using electron beam induced current, Sol. Energy. 211 (2020) 1214–1222.

R.S. Bonilla, I. Al-Dhahir, **M. Yu**, P. Hamer, P.P. Altermatt, Charge fluctuations at the Si–SiO2 interface and its effect on surface recombination in solar cells, Sol. Energy Mater. Sol. Cells. 215 (2020) 110649.

R. Zhou, **M. Yu**, D. Tweddle, P. Hamer, D. Chen, B. Hallam, A. Ciesla, P.P. Altermatt, P.R. Wilshaw, R.S. Bonilla, Understanding and optimizing EBIC pn-junction characterisation from modelling insights, J. Appl. Phys. 127 (2020).

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List of Acronyms

Al-BSF	Aluminium back surface field
ALD	Atomic layer deposition
BSG	Borosilicate glass
CB	Conduction band
CV	Capacitance-voltage
CVD	Chemical vapour deposition
CZ	Czochralski
DI	Deionised
ECV	Electrochemical capacitance-voltage
EPR	Electron paramagnetic resonance
FGA	Forming gas anneal
FZ	Float zone
ICM	Inductively coupled measurements
IL	Inversion layer
IPA	Isopropyl alcohol
IV	Current-voltage
KP	Kelvin probe
LBIC	Light beam-induced current
LCOE	Levelised cost of electricity
MIS	Metal-insulator-semiconductor
MLDA	Modified local-density approximation
MOSFET	Metal-oxide-semiconductor field-effect transistors
PECVD	Plasma-enhanced chemical vapour deposition
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene) polystyrene sulfonate
PERC	Passivated emitter and rear cell
PSG	Phosphorus silicate glass
PTFE	Polytetrafluoroethylene
PV	Photovoltaics
QSS	Quasi-steady state
SHJ	c-Si/a-Si heterojunction
SPV	Surface photovoltage
SRH	Shockley-Read-Hall
SRV	Surface recombination velocity
TOPCon	Tunnelling oxide/poly-Si passivated contact
UNSW	University of New South Wales
UV	Ultraviolet
VB	Valence band
VdP	Van der Pauw

List of Symbols

E_F	Semiconductor Fermi energy (eV)
V_{OC}	Open-circuit voltage (V)
D_{it}	Density of interface states ($eV^{-1}cm^{-2}$)
$\Delta n/\Delta p$	Concentration of photo-generated carriers (cm^{-3})
ε_0	Vacuum permittivity ($F\cdot cm^{-1}$)
E_g	Bandgap of crystalline Si (1.12 eV)
Φ_{ms}	Work function difference between metal and silicon (eV)
ϕ_{scr}	Semiconductor surface potential due to the space charge region (V)
G	Carrier generation rate (s^{-1})
J_{SC}	Short circuit current density ($mA\cdot cm^{-2}$)
K_i	Relative permittivity
μ_n/μ_p	Electron and hole mobility ($cm^2V^{-1}s^{-1}$)
n/p	Electron and hole density (cm^{-3})
R	Carrier recombination rate (s^{-1})
S_{eff}	Effective surface recombination velocity ($cm\cdot s^{-1}$)
σ_n/σ_p	Carrier capture cross-sections for electrons and holes (cm^2)
τ	Minority carrier lifetime (ms)
τ_{Auger}	Auger lifetime (ms)
τ_B	Bulk lifetime (ms)
τ_{rad}	Radiative lifetime (ms)
τ_S	Surface lifetime (ms)
τ_{SRH}	SRH lifetime (ms)

Chapter 1 Introduction

1.1 Climate Change

Climate change refers to the shift in temperatures and weather patterns in the world which due to its consequences has become a major concern for humanity to address within this century. Figure 1-1 shows the global mean temperature since 1880 relative to the global mean for the 20th century [1]. The figure shows that the mean temperature has increased at a steady rate of about 1.4 °C per year from 1920 to 2022. The global temperature rise has led to an increased frequency of extreme weather patterns, such as droughts, floods, and wildfires [2]. These events have had a harmful effect on biodiversity on both land and ocean, and pose a threat to the survival of human beings [3]. The temperature rise is primarily caused by the emission of greenhouse gases, which trap infrared radiation and prevent it from escaping the Earth, resulting in heating. Fossil fuel-related carbon dioxide (CO_2) emissions are recognised as the major cause of global warming. The future temperature rise is expected to depend strongly on the cumulative CO_2 released [4]. Therefore, it is necessary for a transition from fossil fuels towards a sustainable energy system to limit further global warming.

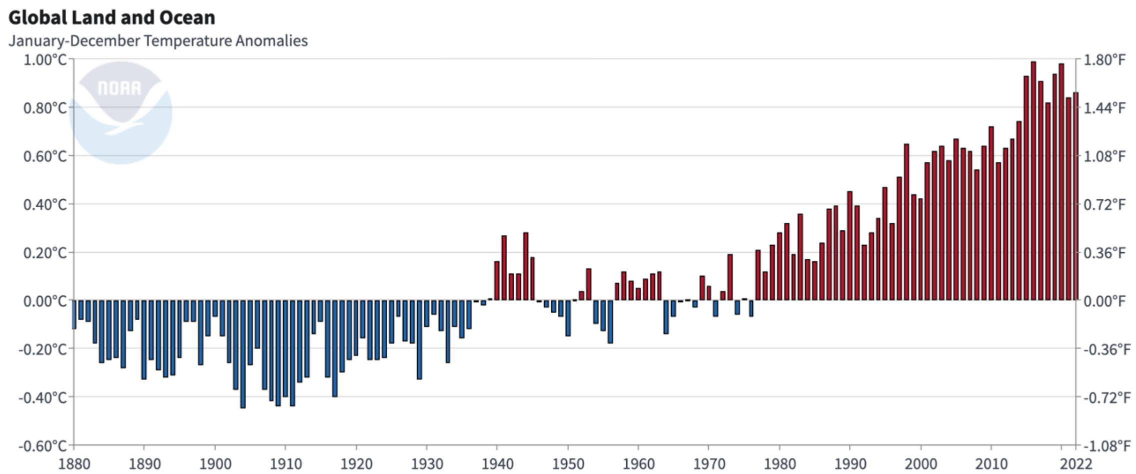

Figure 1-1 Changes in global mean temperature since 1880 relative to the global mean for the 20th century [1].

1.2 Renewable Energy

Solar, wind, hydro and biomass are considered clean energy sources since the amount of CO_2 emitted per kWh of electricity generated is minimal compared to fossil fuel counterparts. Large-scale deployments of such renewables are imperative for a transition towards an eco-friendly energy system. One pre-requisite of such transition is the cost competitiveness of electricity generation by renewables compared to that by fossil fuels. Figure 1-2 shows the cost of electricity generation in Germany in 2021 [5]. The figure shows that although solar energy and wind energy cannot be utilised throughout the year, the cost of electricity generation is the lowest for these two energy sources. It was also reported by IRENA that renewables are the lowest-cost power generation technologies across the globe in 2022 [6]. Figure 1-3 presents a comparison of the cost of electricity by solar and by wind from 2010 to 2020 [7]. The figure shows that both technologies have evidenced a decrease in electricity cost in this period, in which solar photovoltaics (PV) has seen a dramatic drop by ~84%. Hence, solar and wind energy are projected to be the primary sources of power generation in the future. Bogdanov et al. described a pathway to a global renewable electricity system

by 2050 in [8]. A roadmap of power capacities and generations towards such sustainable energy system is shown in Figure 1-4. In this study, it is projected that onshore wind turbines will be installed the most in the near future due to their low cost. Solar PV will take a larger share at a later stage following (i) further reductions in cost, and (ii) the reduction in the most efficient wind generation sites. The same study projected that in 2050 the global generation capacities will exceed 28 TW, of which ~70% will be solar PV and ~18% will be wind turbines [8]. The advancements in solar and wind technologies will enable a further decline in electricity costs, accelerate the deployment of renewables, lubricate the transition towards a sustainable energy system, and ultimately mitigate global warming.

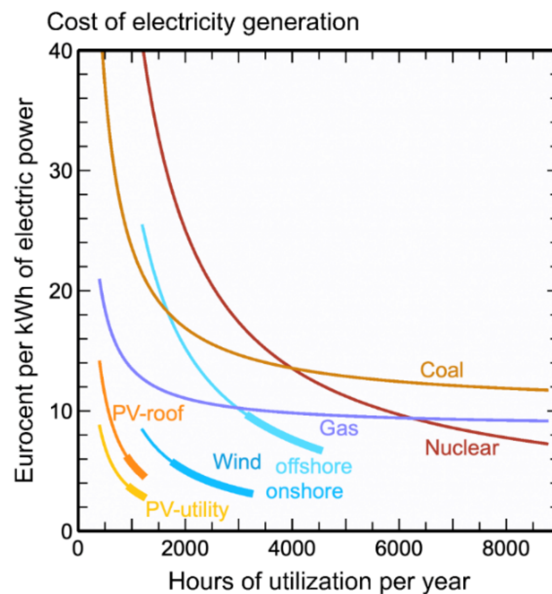

Figure 1-2 Cost of electricity generation in Germany in 2021 [5].

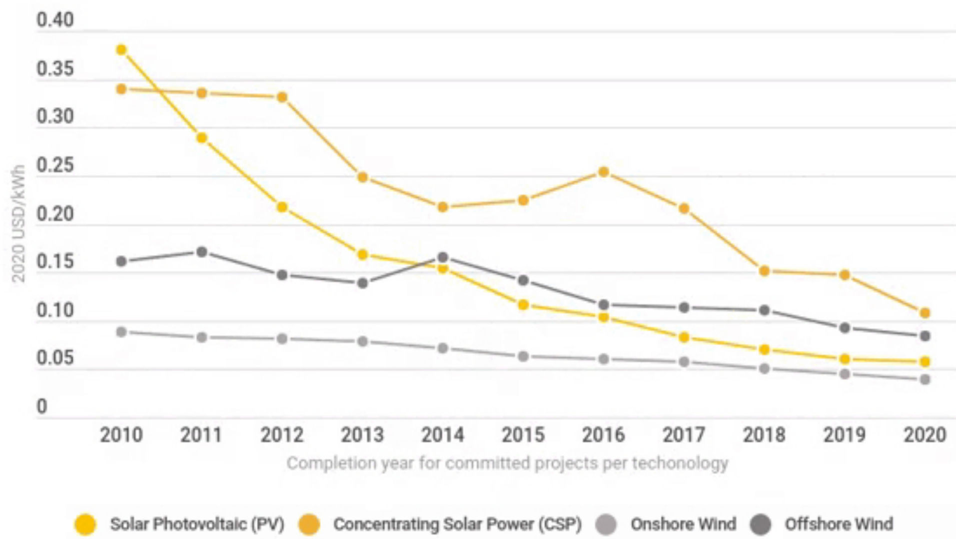

Figure 1-3 Cost of electricity for solar photovoltaic, concentrating solar power, onshore wind, and offshore wind, 2010-2020 [7].

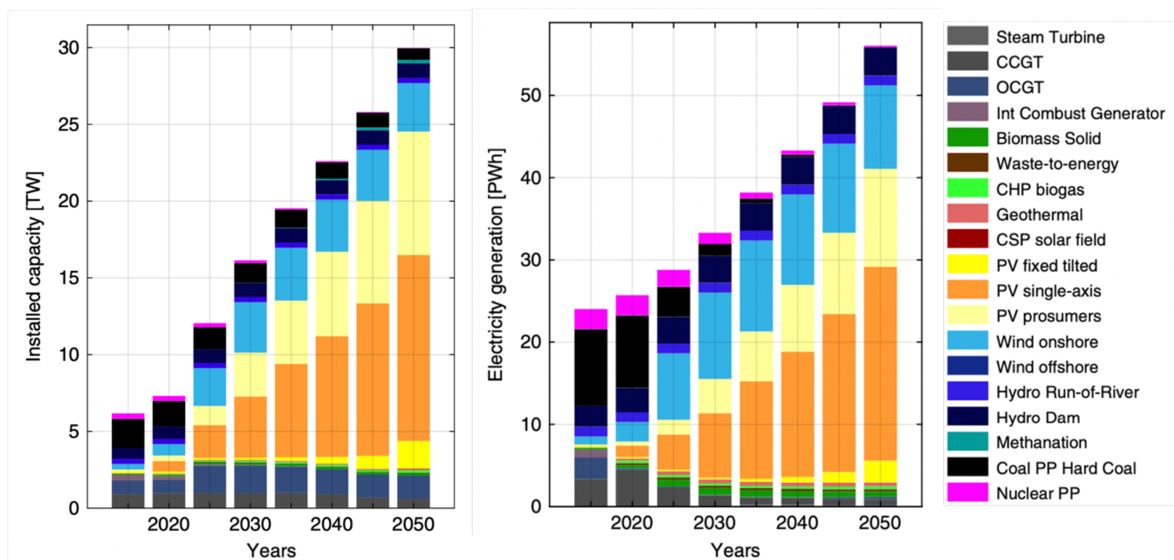

Figure 1-4 Power capacity and power generation roadmap towards sustainable electricity from 2015 to 2050 [8].

1.3 Silicon Photovoltaics

The solar PV market is dominated by three cell technologies: mono-crystalline silicon, multicrystalline silicon, and thin film [9]. Mono-crystalline silicon holds the largest market

share at 92% among these technologies [9], primarily due to its high efficiency, longevity, and relatively low cost. Further research is to be carried out for cost reduction, performance improvement, and resolving sustainability issues to guarantee large-scale deployments of mono-crystalline silicon modules. In this section, pathways for cost reduction and performance improvement will be introduced.

1.3.1 Reduction of Silicon PV Cost

Figure 1-5 shows the learning curve of module price as a function of cumulative PV module shipments [10]. The figure shows that the cost of solar modules has reduced significantly since 1979. The last 16 years has witnessed a more dramatic reduction in module price. It is noticed that the reduction occurred as a function of modules shipped, such that the more the modules fabricated, the lower the production cost. The continuous cost reduction has been realised by advancements in cell technology, module technology and fabrication processes. The learning curve will be projected into the future only by continued implementation of cost reduction measures and cell improvements. The trend in module price indicates that eventually the cost of electricity generation will be less dependent on module price and more dependent on the cost of the balance of a complete system, which encompasses wiring, inverters, mounting and batteries. At such low module cost, the margin for further reducing the cost will be small. In this case, the levelised cost of electricity (LCOE) will be more effectively reduced by improving the performance of solar panels than reducing the cost of modules since increases in efficiency impact the cost of the entire electricity supply chain [11].

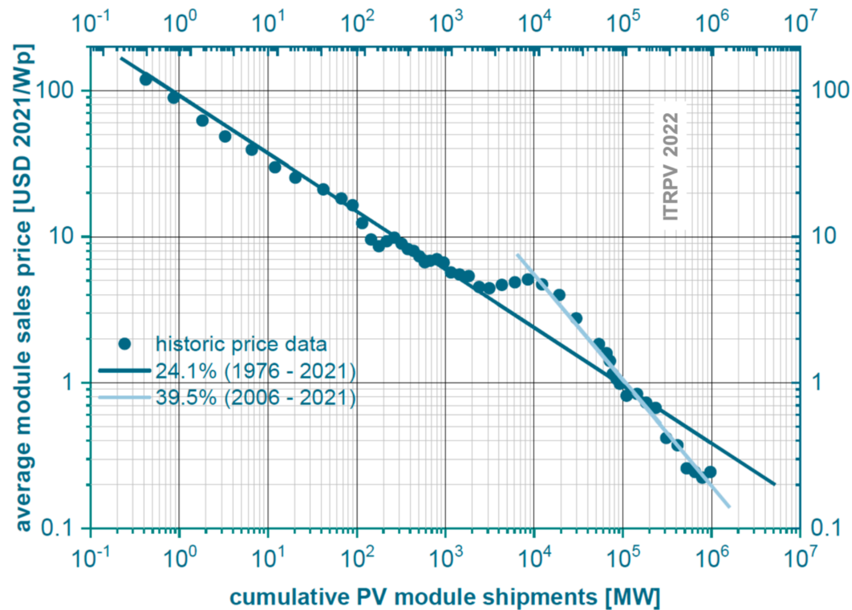

Figure 1-5 Learning curve for module price as a function of cumulative PV module shipments [10].

1.3.2 Cell Efficiency Improvement

1.3.2.1 Fundamentals of Silicon Solar Cells

Solar cells convert energy from light into electricity. In crystalline silicon, electrons in the valence band absorb energy from light and get excited into the conduction band, leaving behind holes in the valence band. Both excited electrons and holes can move freely in the lattice. Silicon can be doped into n-type or p-type by introducing dopant atoms. P-type silicon contains excess holes and can be realised by introducing acceptor atoms like boron or gallium. N-type silicon contains excess electrons and can be realised by introducing donor atoms like phosphorus. A *pn* junction is formed at the interface between n-type and p-type silicon to introduce an asymmetry in the semiconductor device. Electrons will diffuse from n-type silicon into p-type silicon at the interface. The charge from the dopant atoms left behind forms an electric field in what is known as a depletion region. Figure 1-6 shows the band diagram of a *pn* junction in the dark and under illumination. The population of

electrons is described by the Fermi level (E_F), which is constant across the *pn* junction in the dark. Under illumination, the free carriers are redistributed due to the introduction of photo-generated carriers. The Fermi level splits into quasi-Fermi energies, E_{Fn} and E_{Fp}, which describe the population of carriers in the conduction band and the valence band separately. The photo-generated electron-hole pairs are separated at the *pn* junction thanks to the electric field and form a photocurrent. The difference between E_{Fn} and E_{Fp} is the voltage available to the external circuit, which is termed open-circuit voltage (V_{OC}) in a current-voltage curve for solar cells. The generation of photocurrent together with the voltage transforms the energy from irradiation into electrical power.

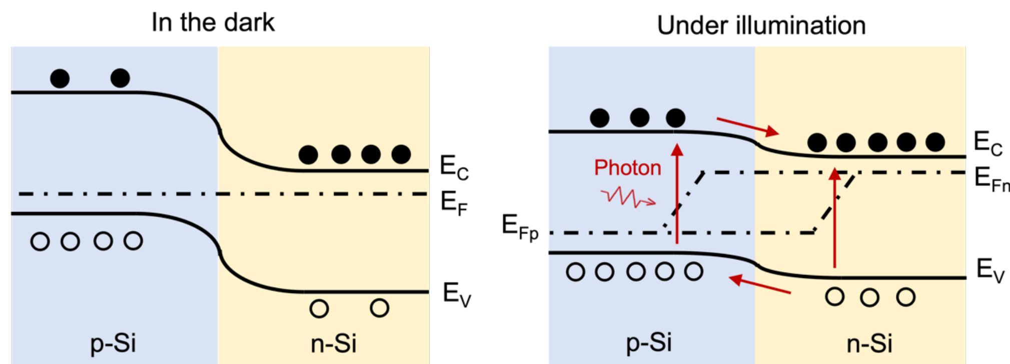

Figure 1-6 Band diagram of a *pn* junction in crystalline silicon in the dark and under illumination depicting the formation and migration of photo-generated carriers.

1.3.2.2 Carrier Losses in Silicon Solar Cells

Photo-generated carriers must travel within silicon before being separated at the *pn* junction and collected at metal contacts. During this process, the excited electrons in the conduction band can lose their energy and re-occupy the states in the valence band. This process is termed recombination and is the primary source of power losses in silicon solar cells. Recombination can occur via several mechanisms: radiative recombination, Auger recombination, and defect-assisted recombination (also known as Shockley-Read-Hall or

SRH recombination). Figure 1-7 shows schematic diagrams of the three recombination mechanisms. For radiative recombination, an electron recombines with a hole and releases the energy by emitting a photon. This process requires the presence of one electron and one hole. For Auger recombination, three particles are involved (either two electrons and one hole, or two holes and one electron). The energy released from the recombination is transmitted to the third particle. The third particle then thermalises quickly and transmits the energy to the silicon lattice as phonons. The SRH recombination mechanism involves a defect level within the bandgap. The recombination requires the defect state to capture an electron and a hole. These states are named recombination centres and originate from impurities, crystallographic imperfections and material interfaces. Recombination causes loss in photocurrent and hence performance of a solar cell, and therefore should be minimised as much as possible.

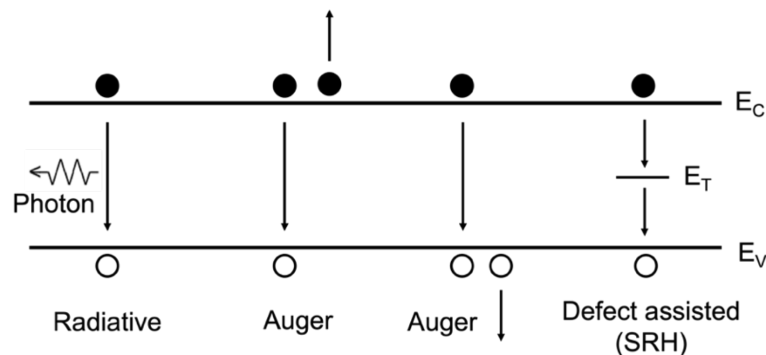

Figure 1-7 Schematic diagrams of different recombination mechanisms: radiative, Auger, and defect-assisted recombination.

In bulk silicon, the carrier losses can be attributed to all three recombination mechanisms. Radiative recombination and Auger recombination are intrinsic properties of silicon and cannot be avoided. Since silicon has an indirect bandgap, in silicon solar cells radiative recombination contributes little to total recombination losses and does not limit cell performance. Auger recombination is a three-particle process. The Auger recombination rate

is thus proportional to carrier density. Auger recombination can be reduced by lowering the doping level in bulk silicon. For defect-assisted recombination, impurities and defects in the bulk can be reduced by further advancing the material processing technology. In addition, atomic hydrogen has been used to passivate the recombination centres for reduced SRH recombination, for example, boron-oxygen complexes, commonly found in boron-doped p-type silicon [12], [13]. In summary, the carrier recombination in the bulk can be minimised by reducing dopant density, defects and impurities in the bulk, and H passivation.

In terms of surface recombination, unsaturated bonds at the silicon surface can act as recombination centres. They create continuum energy states within the bandgap. The origin and characteristics of energy states within the bandgap will be reviewed in Section 1.3.2.3. Surface recombination can be reduced in two ways: chemical passivation and field-effect passivation. Figure 1-8 shows the band diagram of silicon with the two surface passivation mechanisms. Chemical passivation reduces the density of recombination centres. It can be achieved by (i) depositing dielectric layers on the surface, and (ii) introducing atomic hydrogen to saturate the dangling bonds. For field-effect passivation, the surface charge is used to provide a static electric field near the surface. The electric field will lead to the accumulation of majority carriers near the surface and change the local carrier concentration. Figure 1-8.c shows the band diagram of n-type silicon in the presence of positive surface charge. The accumulation of electrons and depletion of holes near the surface leads to a downward band bending. This results in a low probability for the defect states to capture holes and thus reduced surface recombination. Both high-quality bulk material and well-passivated surfaces are necessary for minimum carrier recombination and maximum solar cell efficiency.

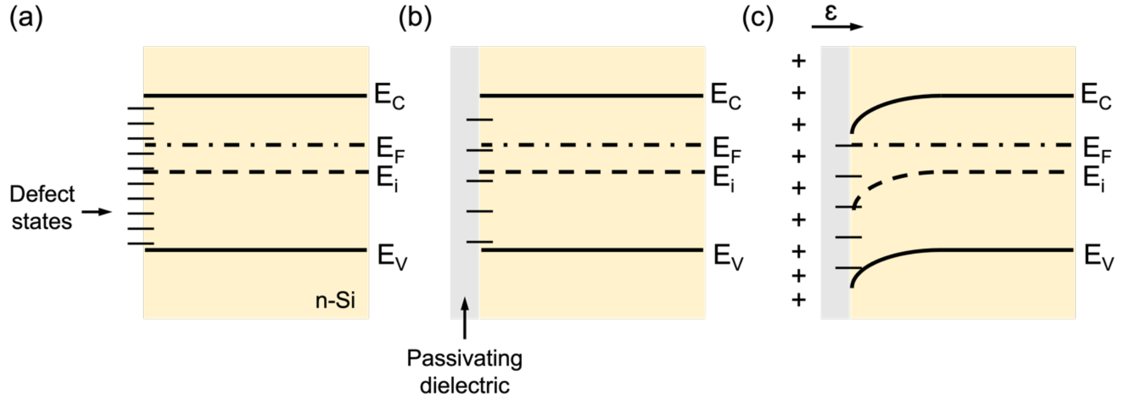

Figure 1-8 Band diagram at the surface of n-type silicon (i) in an un-passivated state, (ii) passivated chemically, and (iii) passivated via field-effect.

Minority carrier lifetime (τ) is defined as the average time it takes for a minority carrier to recombine and is used as a metric to describe recombination and quality of passivation. Since recombination mechanisms differ in different regions, the carrier lifetime is typically different near the surface and in the bulk. An effective lifetime parameter (τ_{eff}) is used to integrate the recombination at the interface and in the bulk following Eq (1-1),

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_B} + \frac{1}{\tau_S} \qquad \text{Eq (1-1)}$$

where τ_S represents the surface lifetime and τ_B represents the bulk lifetime. The bulk lifetime can be separated into radiative lifetime (τ_{rad}), Auger lifetime (τ_{Auger}) and SRH lifetime (τ_{SRH}) following Eq (1-2):

$$\frac{1}{\tau_B} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} \qquad \text{Eq (1-2)}$$

It is noted from Eq (1-1) and Eq (1-2) that the recombination mechanism with the lowest lifetime limits the overall effective lifetime. Strategies have been adopted in the evolution of cell architectures to maximise the effective lifetime, which will be introduced in Section 1.3.2.4.

1.3.2.3 Energy States at Silicon-Dielectric Interfaces

The interface defect state density is a critical property of semiconductor-dielectric interfaces. Since these states have their energy levels in the bandgap, they can act as strong recombination centres or store large concentrations of charge, both of which may be detrimental to photovoltaic devices [14]. The origin and characteristics of interface states at silicon-dielectric interfaces are reviewed in this section. Fundamentally, these states are formed as a result of the interruption of translational symmetry when the two bulk materials are brought together to form an interface. However, the precise origin of these states and their role in device physics have been the subject of study for many decades (see Ref. [15] for a review). The states can be classified broadly as either intrinsic or extrinsic [16]. The extrinsic states come from forming defects such as vacancies, interstitials, impurities and especially silicon dangling bonds in the case of the surface. Dangling bonds are unsaturated silicon atoms with one or more unpaired valence electrons. They introduce energy states within the bandgap and provide sites for carrier recombination. These dangling bonds can be saturated by bonding with other atoms, for example, oxygen from a SiO_2 layer, and hydrogen. The energy level of these defect states is determined by the atomic configuration and orientation of the silicon substrate [17]. Here SiO_2-passivated silicon surfaces are used as an example. P_b centres are formed on (111) surfaces. P_{b0} and P_{b1} centres are formed on (100) surfaces. P_b and P_{b0} centres are on silicon atoms that are back-bonded with three other silicon atoms. For P_{b1} centres, the silicon atoms are back-bonded with two silicon atoms and one oxygen atom. All three types of dangling bonds have been shown to introduce defect states within the bandgap [18]–[20]. Figure 1-9 shows a schematic of the P_{b0} and P_{b1} densities of states [20]. The DOS for both P_{b0} and P_{b1} centres contain two peaks. This is due to the amphoteric nature of dangling bonds. The defect centres can lose the unpaired electron

and become positively charged or capture an electron and become negatively charged depending on the Fermi level. The dangling bonds can be either donor-like or acceptor-like, resulting in the two-peak feature in Figure 1-9. The energy level of the defect states appears to lie towards the middle of the bandgap and is hence detrimental [21]. In terms of device performance, these deep levels act as traps for carriers, greatly increasing the probability of recombination and decreasing the excess carrier density.

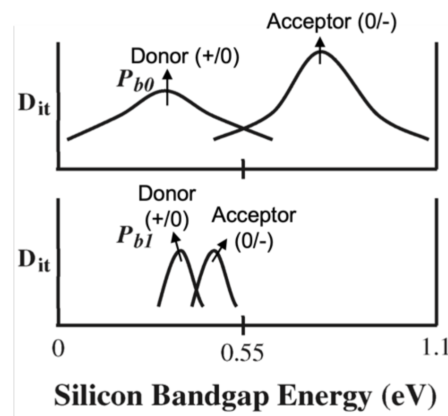

Figure 1-9 A schematic illustration of the P_{b0} and P_{b1} densities of states [20].

In the intrinsic case, terminating the periodicity of bulk material leads to a continuum of exponentially decaying states whose energies lie in the bandgap of the bulk material. These states were first introduced in the context of metal-semiconductor junctions [22]. As indicated by the name, they are an intrinsic and fundamental property of the material. They can be understood as Bloch states of the bulk semiconductor with complex wave vector [23] and can be viewed as having valence or conduction band character depending on their energies. Often the large density of these states at the interface provides an effective mechanism to pin the Fermi level and explain the energy-level alignment at semiconductor interfaces [23]. The effect of intrinsic states on the energy levels at the interface, conveniently characterised through the density of states, is more continuous in nature. As an illustration, consider the first-principles density-functional theory calculations of layer-

resolved density-of-states for a defect-free Fe/GaAs interface as reported in [24]. They show how the interface broadens the GaAs band edges such that they form tails which decay exponentially with energy towards the middle of the gap. A more pertinent example is calculations on model Si/SiO_2 interfaces which demonstrate the evolution of the band structure as one moves between the Si and SiO_2 regions [25], [26].

Altogether, the interface states have a distribution of energy at different sections of the bandgap [27], which affects interface properties in different ways. For example, there is an asymmetry in probability for capturing an electron or hole, quantified as the cross-section of electron or hole capture, σ_n and σ_p, respectively, in units of cm^2. Near mid-gap, the Coulomb interaction of charged defect states usually dominates the recombination activity in covalently bonded semiconductors like silicon. Near the band edges, on the other hand, the shape of the atomic orbitals often plays a significant role. Whether a defect state acts as an effective recombination centre does not only depend on its σ_n and σ_p, but also on the SRH statistics [28], [29]. Both an electron and a hole must be captured for recombination to happen, and the less likely carrier limits the recombination rate. In the shallow defects at the band tails, the re-emission probability of one carrier is large, making these states often inefficient for recombination except at very high dopant density, very high injection density, or substantial band bending [28], [29]. Therefore, interface states at mid-gap are the primary concern for achieving high surface passivation. Such mid-gap D_{it} continues to be intensively studied and is nowadays widely used as a metric for surface passivation [30]–[32].

The fundamental properties of band-tail states, on the other hand, were only studied experimentally in the 1980s and 1990s [27], [33]–[39]. An exponential increase in density towards the conduction/valence band edge was observed in such works, in agreement with theoretical calculations. A consolidation of known Si/SiO_2 interface state densities in the

literature, including band tails, is shown in Figure 1-10. It is demonstrated that processing conditions can largely affect the interface properties and that much less data exists for the true densities in the tails. Due to the relatively low recombination rate in such band-tail states, they have not been as prominently studied as the mid-gap strong recombination states. Despite the lack of attention, state density at the band tails can be several orders of magnitudes higher than that at mid-gap. These states can trap large concentrations of charge carriers when the Fermi level reaches the band tails. The trapped charge at the interface can alter the carrier distribution near the interface and may affect the performance of the final device.

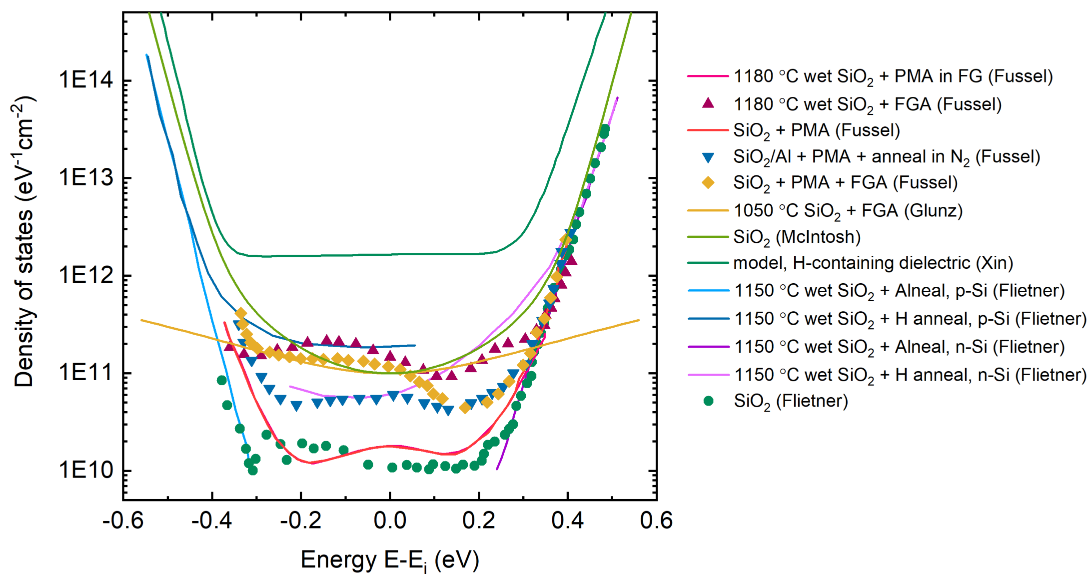

Figure 1-10 Density of states distribution of various Si/SiO_2 interfaces, redrawn from [27], [33], [36], [38]–[40]. PMA: post-metallisation anneal; FGA: forming gas anneal; FG: forming gas; Alneal: a method to introduce atomic hydrogen to Si/SiO_2 interfaces [41].

This section reviews the origin and characteristics of interface states within the bandgap. Silicon dangling bonds introduce deep energy levels within the bandgap which are strong recombination centres. These defect states can be passivated by saturating the dangling bonds by, for example, depositing dielectric material and introducing atomic hydrogen.

Band-tail interface states are intrinsic properties of the surface of bulk silicon and have been shown to increase exponentially in concentration towards the conduction/valence band edges. These states lie near the band edges and do not often lead to a high recombination rate, but the high density of the band-tail states can trap charge carriers at the interface which may in turn affect the carrier distribution near the interface and therefore the performance of the final device. Carrier recombination at the interface has been a major source of power losses in Si-based solar cells. Passivation techniques have been developed to minimise such carrier recombination.

1.3.2.4 Evolutions of Cell Architecture

Continuous improvements in solar PV technologies have been achieved by processing and device architectures that reduce charge carrier losses [42]–[44]. Figure 1-11 shows the structure of four types of silicon solar cells, named aluminium back surface field (Al-BSF) cell, passivated emitter and rear cell (PERC), tunnelling oxide/poly-Si passivated contact (TOPCon) cell and c-Si/a-Si heterojunction (SHJ) cell. For Al-BSF, PERC and TOPCon cells, the *pn* junction is formed by diffusing phosphorus atoms into p-type silicon substrates, or boron atoms into n-type silicon substrates. The diffused region is commonly termed an emitter due to the nomenclature followed for bipolar transistors [45]. Figure 1-11.a shows the structure of an Al-BSF cell. The front surface is passivated by a SiO_2/SiN_x stack and is contacted by localised metal fingers. The SiO_2/SiN_x stack provides both chemical passivation and field-effect passivation. The dangling bonds are saturated by SiO_2 and atomic hydrogen from the SiN_x layer. The hydrogen is introduced during the deposition of the SiN_x layer using plasma-enhanced chemical vapour deposition (PECVD). The SiN_x layer is known to carry positive charge, typically of a magnitude of 10^{12} cm^{-2} [46], which can provide field-effect passivation on the n-type side. The rear of the cell has a full-area screen-

printed aluminium paste for hole-extracting contact. An anneal afterwards will allow the in-diffusion of Al atoms into bulk silicon, forming an electric field for reduced recombination at the rear contact. The maximum efficiency of Al-BSF cells is about 20.5% [47]. Heavy carrier recombination has been found at silicon-metal contacts [48]. To minimise such losses, cell architectures with reduced silicon-metal contact areas were implemented. The current mainstream that replaced Al-BSF is PERC technology. Its structure is shown in Figure 1-11.b. PERC has become the industrial standard thanks to the developed AlO_x/Si_xN_y passivating stack, which in combination with a reduced metal-silicon contact area has led to lower recombination losses at the rear surface. Additionally, its fabrication compatibility with Al-BSF ensured a smooth transition to PERC with minimal processing additions or changes [49]–[51]. Despite these advantages, the classical PERC design and its unavoidable contact losses limit the commercial efficiency to just above 24% [52], [47]. The strongest contenders to supersede PERC are designs using passivating contacts to minimise silicon-metal contact losses and enhance the silicon/dielectric interface passivation. Out of several passivating contacts recently proposed, the TOPCon [53], [54], as well as the SHJ structure [55], have gained the most attention since they allow for both excellent contact passivation and low contact resistance. The TOPCon structure is shown in Figure 1-11.c. Although the carrier recombination is reduced, the TOPCon design requires more processing steps than PERC cells, lacks a passivating contact at the front, and is limited by Auger recombination in the boron-diffused emitter. Figure 1-11.d shows the structure of a SHJ cell. SHJ cells perform well because they have passivating contacts at both the front and the rear surface. However, their performance is limited by parasitic absorption in the front a-Si layer. For both TOPCon and SHJ cells, the efficiency is limited to ~26% [47]. Figure 1-12.a shows the average cell efficiency of current silicon PV technologies and potential future technological

developments based on historical efficiency increases (0.5-0.6% absolute per year) [47]. In the figure, the transition of the cell architecture from Al-BSF to PERC, and then to the designs with passivating contacts has enabled the increase in cell efficiency since 2014. While passivating contacts will reach their limit through advancements in fabrication processes, the improvement in efficiency is expected to be continued by developing silicon-based tandem cells. Silicon-based tandem cells involve the addition of a semi-transparent solar cell on top of silicon cells with a larger bandgap. In tandem cells, each sub-cell is optimised for harvesting the photon energy in each section of the spectrum, such that a higher overall cell efficiency can be reached. Figure 1-12.b provides estimations of market shares for different technologies. It is predicted that Al-BSF cells will fade out from the market by 2024, accompanied by a continuous increase of SHJ cells and silicon-based tandem cells. PERC and its variants (PERL, PERT) together with TOPCon will remain mainstream until 2032. It is noted that diffused emitters are used in the mainstream cell technologies. The fabrication process and recombination losses in diffused emitters will be reviewed in the next section.

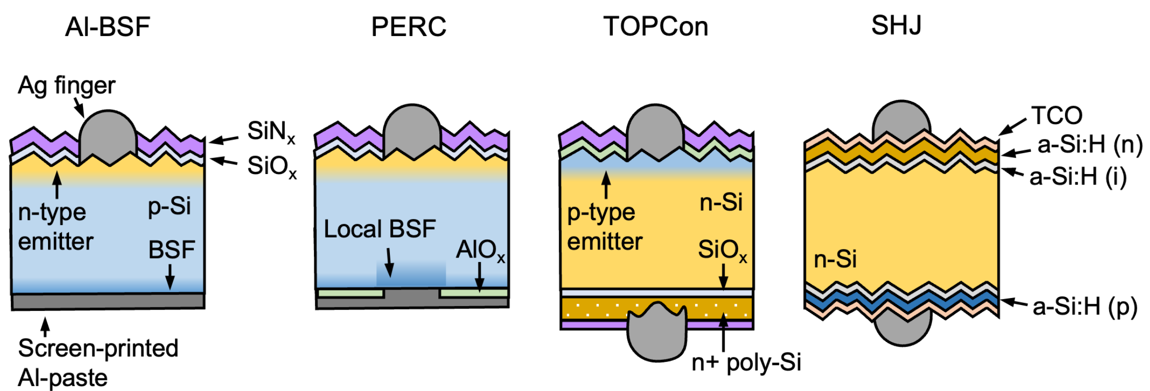

Figure 1-11 Schematic illustration of different single junction silicon cell architectures.

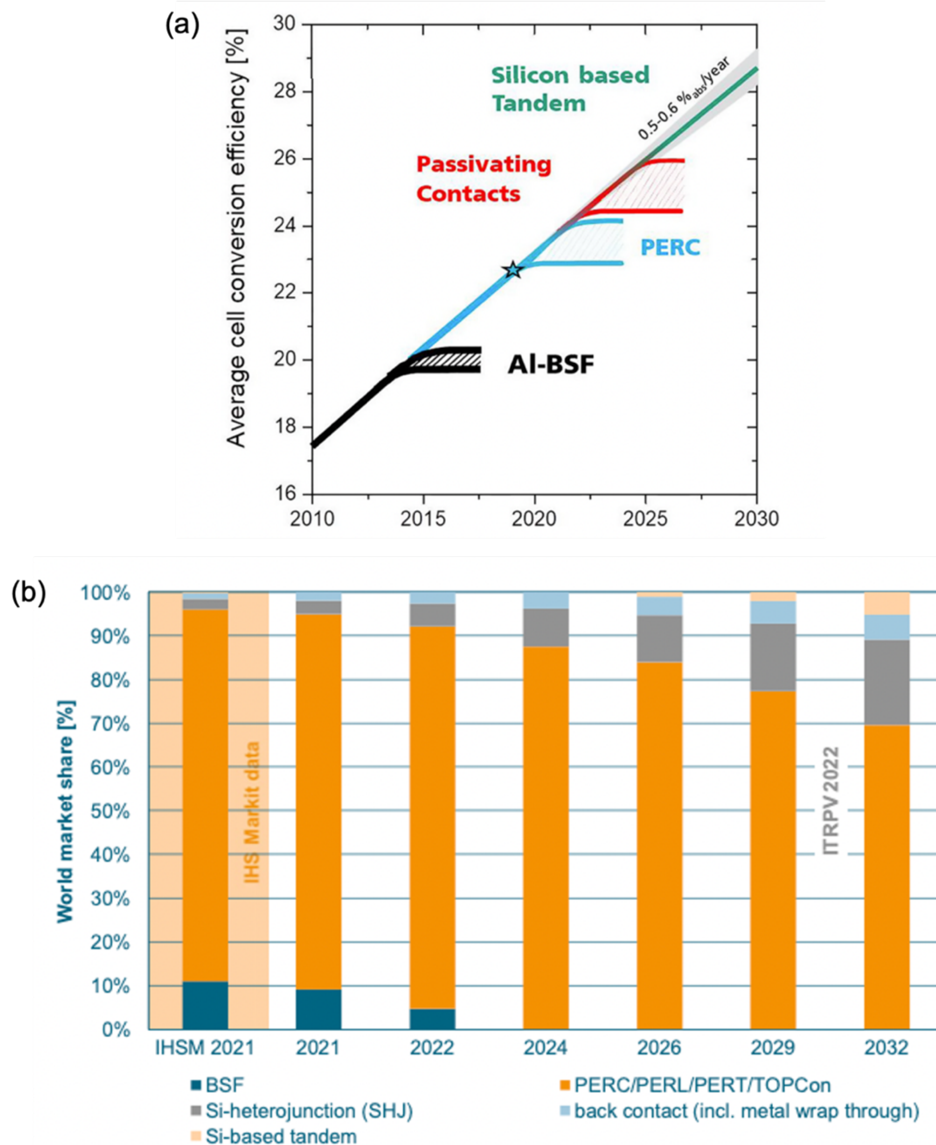

Figure 1-12 (a) Potential further technological development in silicon PV based on historical efficiency increases (0.5-0.6% absolute per year) and the current silicon PV technologies being investigated [47]. (b) Predicted market shares for different cell technologies from 2021 to 2032 [10].

1.4 Diffused Emitters

N-type emitters are formed by diffusing phosphorus atoms into p-type substrates (P-diffused emitter). P-type emitters are often formed by diffusing boron atoms into n-type substrates (B-diffused emitters). The diffusion process will lead to high dopant densities and high carrier concentrations in diffused emitters. A high dopant density indicates a high density of

defects, resulting in increased SRH recombination. A high carrier concentration suggests large carrier losses via Auger recombination. Emitter sheet resistance has been used as an indicator of the carrier concentration in emitters. In terms of fabrication, a high thermal budget is required to form diffused emitters. This section reviews the fabrication procedure and recombination losses in diffused emitters.

1.4.1 Fabrication of Diffused Emitters

P-diffused emitters can be fabricated in two steps: pre-deposition and drive-in [56]. The pre-deposition step involves exposing silicon wafers to $POCl_3$ and O_2 gas at 800-900 °C to form phosphosilicate glass (PSG) on the surface. The phosphorus dopant density is at its solubility limit (approximately 3×10^{20} cm^{-3}) in silicon at the surface. $POCl_3$ gas is stopped during the drive-in process. A subsequent ~60 min at 800-900 °C allows phosphorus atoms to diffuse into bulk silicon from the PSG layer. B-diffused emitters are formed in a similar way. Silicon wafers are exposed to BCl_3 or BBr_3, and O_2 gas at 850 °C for 30 min to form a borosilicate glass (BSG) layer, followed by a drive-in step at 850-970 °C for more than 60 min [57]. Figure 1-13 shows a phosphorus doping profile in a P-diffused emitter of a PERC cell and a boron doping profile in a B-diffused emitter of a TOPCon cell measured by electrochemical capacitance-voltage (ECV) [58]. The corresponding sheet resistance is 155 Ω/sq for the P-diffused emitter and 95 Ω/sq for the B-diffused emitter. The recombination losses in the diffused emitters and limitations in fabrication will be introduced in the following sections.

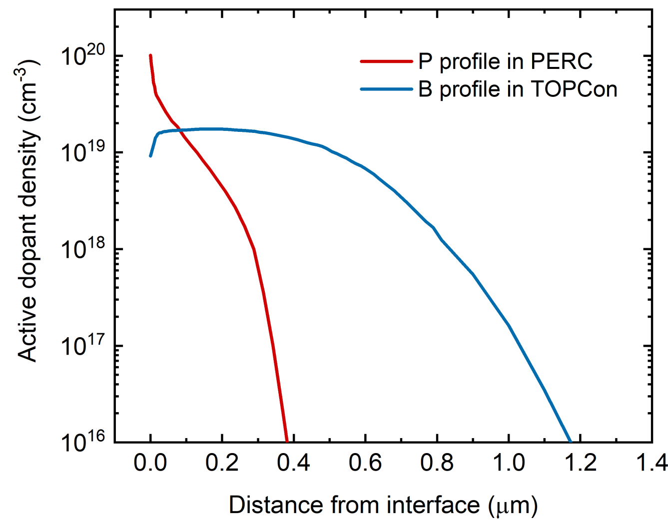

Figure 1-13 Typical doping profiles in diffused emitters in the industry, measured by ECV [58].

1.4.2 Intrinsic Recombination

Section 1.3.2.1 showed that Auger recombination scales with carrier density, which in turn is determined by the active doping concentration. The high dopant density in diffused emitters will lead to increased Auger recombination. Figure 1-14 shows the minority carrier lifetime in B-doped bulk silicon and calculated lifetimes by each recombination mechanism [59]. It is evident in the figure that Auger recombination increases with doping concentration and will dominate the recombination at doping levels above 10^{16} cm^{-3}. In a typical B-diffused emitter, as shown in Figure 1-13, the active boron dopant density is kept above 10^{16} cm^{-3} for ~1.2 um from the surface, indicating heavy Auger recombination. Figure 1-15 shows the simulated recombination current density at the maximum power point of an n-type silicon solar cell with an industrial B-diffused emitter [60]. It is shown that with improved rear passivation, Auger recombination together with bulk SRH recombination will dominate the total losses. Adjusting doping profiles for reduced Auger recombination therefore gains more importance in advanced cell technologies where all losses must be minimised.

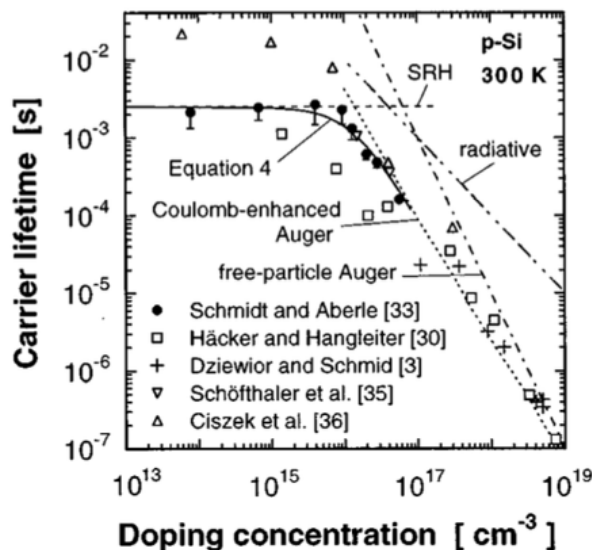

Figure 1-14 Carrier lifetime in B-doped bulk Si at 300 K at low injection, compared to SRH recombination, Coulomb-enhanced Auger recombination, free-particle Auger recombination, and radiative recombination [59].

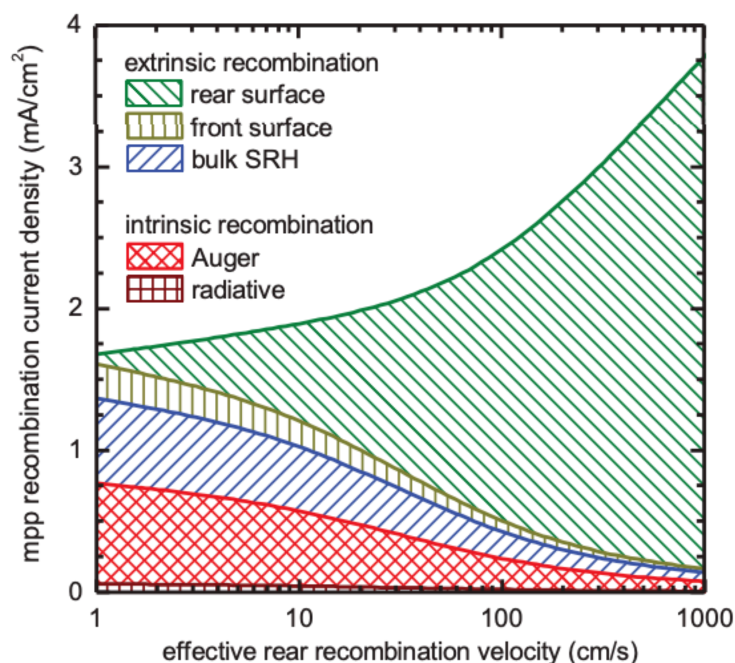

Figure 1-15 Simulated recombination current density in different recombination mechanisms at the maximum power point as a function of the effective rear recombination velocity on an n-type silicon solar cell by PC1D. The model comprises a 150 µm thick, 1 Ω·cm n-type silicon substrate and an industrial B-diffused emitter [60].

For cell designs with direct metal-silicon contacts, a high doping level is required underneath the metal contact for low contact resistivity, while a relatively low dopant density is favourable for reduced Auger recombination. For P-diffused emitters, a selective emitter geometry has been developed to maintain low contact resistivity, low Auger recombination, improved carrier selectivity, and reduced carrier recombination at the interface [61], [62]. The geometry has the region underneath the metal contact heavily doped while keeping a relatively low doping density in the rest of the area. The selective emitter can be achieved by implementing doped silicon inks, an oxide mask layer, ion implantation, an etch-back process or laser doping [61]. Laser doping has been the most commonly utilised for mass production in the industry [62]. Figure 1-16 shows the estimation of sheet resistance of diffused emitters by 2032 [10]. For P-diffused emitters, an increase in emitter sheet resistance is expected for both homogeneous emitters and lowly-doped regions in the selective emitter geometry. For B-diffused emitters, the realisation of the geometry is more complicated and requires more costly processing procedures [63]–[65]. It has been reported that laser doping has been used in 10% of p-type emitters in mass production and is expected to dominate by 2027 [9]. Figure 1-16.b shows that similar to P-diffused emitters, the sheet resistance of B-diffused emitters is also expected to increase in the coming years [10]. Screen print paste manufacturers are constantly developing new pastes to contact more lightly doped emitters. The trend is therefore expected to continue. The increase in emitter sheet resistance will lead to reduced Auger recombination in the final PV devices. Geometries and fabrication methods that can further increase the emitter sheet resistance while maintaining low contact resistance are to be explored.

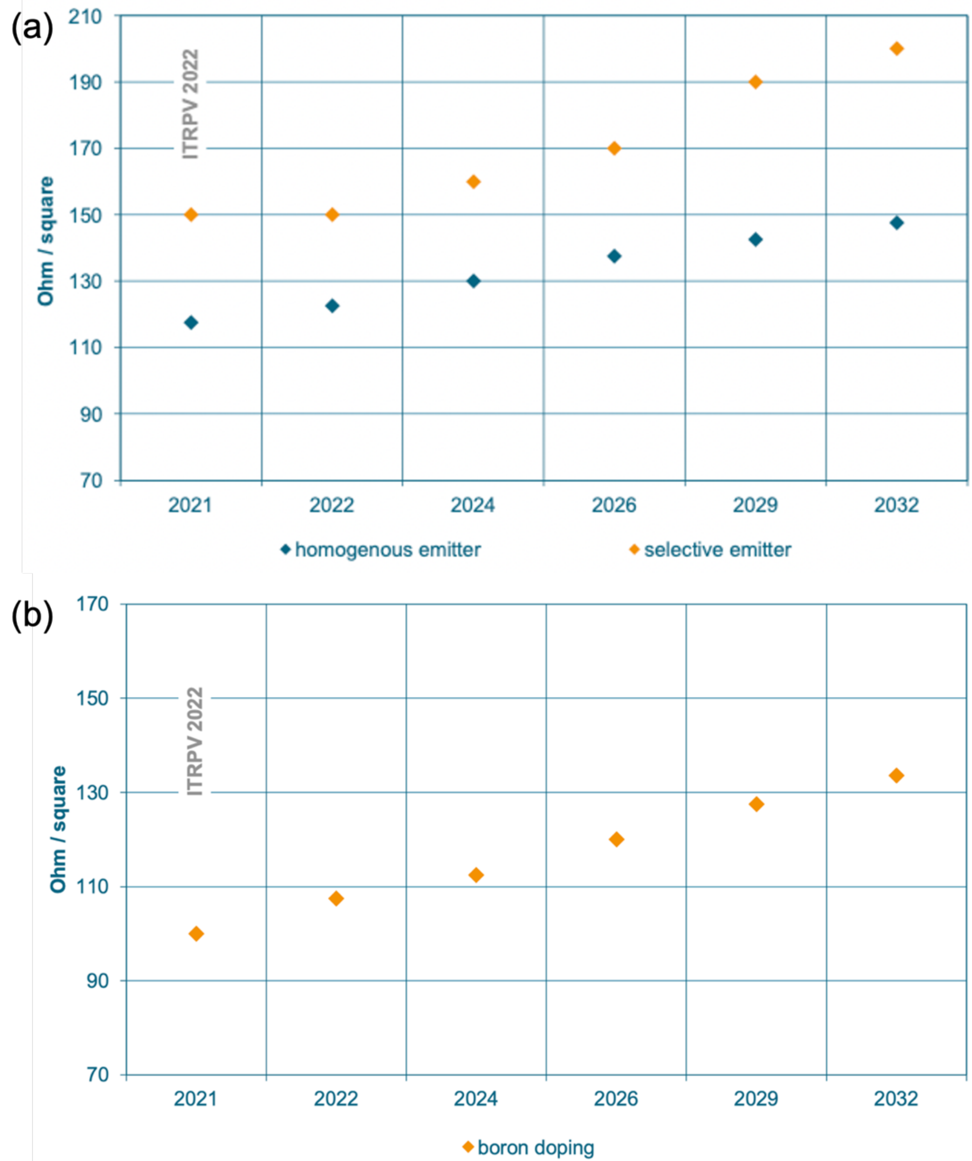

Figure 1-16 (a) Expected trend for emitter sheet resistance of P-diffused emitters for p-type cells. The selective emitter sheet resistance refers to the lower doped region. (b) Expected trend for emitter sheet resistance of B-diffused emitters for n-type cells. [10]

1.4.3 SRH Recombination

A high doping density will lead to an increased concentration of recombination sites in the bulk and at the interface via three mechanisms. Firstly, the high concentration of dopant atoms will strain the silicon lattice and lead to the formation of defects. The strain near the surface can extend into the bulk and cause further reduction in carrier lifetime. Secondly,

there will be electrically inactive phosphorus atoms in the emitter. This is due to the reduced solubility limit of phosphorus inside of bulk silicon when the temperature drops from above 800 °C to room temperature during cooling. The electrically inactive phosphorus atoms may exist in the form of interstitials, clusters and silicon phosphate precipitates, which can act as recombination centres [66], [67]. Most of the inactive phosphorus atoms have been found near the interface [66]. Carrier recombination at the phosphorus precipitates used to dominate the total recombination in some industrial emitters [67]. This effect has been alleviated by adjusting the diffusion process so that there are fewer inactive dopants [56]. In addition to increased recombination sites in the bulk, heavy doping will also lead to a high density of defect states at the interface, and thus increased interface recombination [68], [69]. The increased recombination sites due to heavy doping will lead to carrier losses and detrimentally impact the cell performance.

A similar effect has been observed in B-diffused emitters. Reference [57] showed that a boron-rich layer is formed beneath the BSG. The boron-rich region contains SiB_6. The thermal expansion coefficients of SiB_6 and silicon are different, and the mechanical stress produced during the cool-down process will lead to the formation of defects. In addition, the size misfit between boron atoms and the Si lattice in the heavily doped region will cause tension in the lattice and lead to the formation of dislocations. These defects formed near the surface can diffuse past the *pn* junction into the bulk and cause degradation in the bulk. It has been observed that the formation and thickness of the boron-rich layer are correlated with bulk lifetime and that a boron-rich layer of >10 nm thickness is detrimental to the bulk lifetime [57]. Therefore, BSG thickness and drive-in temperature need to be well-adjusted to ensure sufficient boron doping while maintaining minimum lifetime degradation. This leaves a narrow processing window to fabricate B-diffused emitters [57].

Overall, it is shown that the high doping density in both boron- and phosphorus-diffused emitters will cause an increase in SRH recombination in the bulk and at the interface. This effect can be alleviated by lowering the doping concentration, which is expected to happen in coming years [10].

1.4.4 Difficulties in Fabrication of Boron-Diffused Emitters

P-type emitters are needed in solar cell architectures developed on n-type silicon substrates. These cells typically benefit from the higher bulk lifetime of n-type silicon substrates and are thus attractive in the industry [70], [71]. B-diffused emitters have been used in TOPCon cells for example. However, compared with P-diffused emitters, their fabrication is not favourable due to the following reasons:

(i) A high thermal budget is required to form B-diffused emitters (850-970 °C for more than 90 min [57]).

(ii) Silicon wafers are exposed to a mixture of BBr_3 and O_2 gas at a high temperature to form a layer of B_2O_3. Liquid B_2O_3 condenses on both the silicon wafers and furnace walls. The thermal expansion coefficient mismatch between the B_2O_3 layer and the furnace wall can cause potential danger during the heating and cooling process. Periodical cleaning and replacement of the furnace tubes are necessary, which are costly and unfavourable in the industry.

(iii) The thickness of the BSG layer is inhomogeneous across the wafer surface, which causes inhomogeneity in the boron-rich layer and finally dopant density in the emitter [57].

(iv) The narrow processing window in the fabrication of B-diffused emitters mentioned above.

(v) It is difficult and costly to form a selective emitter geometry for reduced Auger and SRH recombination.

1.4.5 Summary

It is expected that the silicon PV market will be dominated by PERC and TOPCon cells in the following 10 years [10]. The major difference between these cell architectures is the passivation, while both cell architectures use either a phosphorus- or a boron-diffused emitter. The high dopant density in the emitters leads to an increase in both Auger recombination and SRH recombination. The extent of the increased recombination is correlated with dopant concentration and emitter thickness, which can be represented by emitter sheet resistance. Emitter sheet resistance is expected to increase for both phosphorus- and boron-diffused emitters in the following 10 years [10], such that the recombination losses will be mitigated. A selective emitter geometry has been designed to reduce the area with high recombination and has been widely utilised in P-diffused emitters in the industry. However, this geometry has not been integrated into the fabrication of B-diffused emitters due to technical difficulties and high costs. Additionally, as explained in Section 1.4.4, the fabrication of B-diffused emitters is not favourable in the industry. One other approach to reduce the recombination in the emitter is to replace the diffused emitter altogether. A field-induced inversion layer can be produced where no dopant atoms are introduced into bulk silicon and thus avoid extra recombination. This concept is explored next.

1.5 Inversion Layer Cells

Inversion layer cells utilise a special device architecture in which surface charge is used to create an accumulation of minority carriers near the surface, often termed an inversion layer. This inversion layer serves as an emitter to aid charge separation. For example, in p-type IL

cells, the *pn* junction is formed by introducing positive charge into the front dielectric layer, such that mirror electrons will accumulate near the silicon-dielectric interface. In the case where the electron density (minority carrier in p-type substrates) near the interface exceeds the hole density, the region is inverted from p- into n-type, creating a *pn* junction. Figure 1-17 shows the band diagram of an n-type inversion layer. Unlike diffused emitters, no dopant atoms are introduced to produce the field-induced inversion layer and therefore do not lead to increased SRH recombination. The sheet resistance of a field-induced inversion layer is typically lower than that of diffused emitters [72], [73]. This can result from a combination of lower majority carrier concentration and a thinner emitter depth, which leads to less Auger recombination. In addition, no high-temperature diffusion procedure is required in the fabrication of an inversion layer, which gives reduced cleanliness requirements, fewer material degradation issues, and a large reduction in production costs. With no high-temperature diffusion process required, no dopant atoms introduced, and less Auger recombination, field-induced emitters have the potential to replace diffused emitters in solar cell architectures.

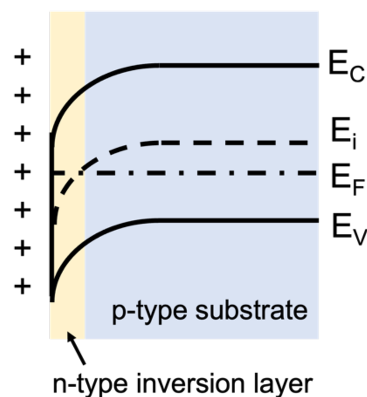

Figure 1-17 Band diagram of an n-type inversion layer.

IL cells have been studied for two decades, yet they did not progress to successful commercialisation. In IL cells, a high charge density is required to induce a sufficiently

conductive emitter. In previous works [72]–[76], fixed charge in titanium oxide, silicon oxide, tantalum oxide and aluminium oxide thin films was used to induce the inversion layer. Silicon nitride was first introduced in IL cells in the 1980s and has since been widely studied due to its high charge density and good charge stability [75]. Introducing caesium before nitride deposition has been found to boost the charge density up to 1.1×10^{13} cm^{-2} [77]. However, this concentration was not high enough to induce a sufficiently conductive emitter to compete with diffused emitters at the time. With high emitter sheet resistance, metal fingers must be separated by a small distance so that the average distance charge carriers must travel to reach the metal fingers is small to reduce resistive losses. However, a narrow finger spacing leads to a large total surface area that is covered by metal fingers. The fingers block light injection into the cell. The consequent loss in photocurrent is referred to as shading loss. Therefore, it is crucial to produce high charge densities in the dielectric layer, which has been limiting the efficiency of the IL cells [73], [78]–[81].

1.6 Aims and Objectives

It has been recently demonstrated that a high charge density in dielectric thin films is possible via a field and temperature-assisted ion injection technique [82]. The technique embeds permanent charge into a dielectric layer in the form of solid-state ions. This technique was originally developed for field-effect passivation in Bonilla et al.'s work [41], [83], [84] since it enables control of charge inside passivating dielectrics. Their work has demonstrated charge densities of above 5×10^{12} cm^{-2}. The details of this technique will be reviewed in Section 2.2. In this thesis, this technique was leveraged and applied to IL cells to maximise charge density and minimise the sheet resistance of field-induced emitters. The conditions required for the technique include an application of ion precursor, a strong

electric field across the dielectric, and an anneal at a temperature below 500 °C. Considering the low cost and the high compatibility of the process with the mainstream technology, the field-induced emitter can be a viable replacement for the diffused emitter.

This work aims to develop an IL cell with a field-induced emitter comparable in performance to a P-diffused emitter while maintaining simpler and lower temperature (hence lower-cost) manufacturing processes. The objectives include:

(i) Obtain maximal charge density in the dielectric layer of the order of 10^{13} cm^{-2}.

(ii) Obtain a sufficiently conductive inversion layer exploiting the ion injection technique.

(iii) Develop a prototype inversion layer cell.

(iv) Investigate the performance potential of inversion layer cells based on this new processing route.

1.7 Structure of this Thesis

To begin, Chapter 2 reviews previous studies on IL cells and points to limiting factors preventing the commercialisation of IL cells. Chapter 3 includes a detailed description of the experimental and characterisation methods used in this work. The results presented in this thesis comprise four main parts (Chapter 4-Chapter 7). Chapter 4 studies the formation of field-induced inversion layers. Novel results are shown on how the ion injection technique was used to induce an electron accumulation layer. A model was developed in Sentaurus TCAD to explore the lowest inversion layer sheet resistance possible and pathways to achieve it. Chapter 5 demonstrates the impact of interface defect states on the formation of field-induced layers and introduces a method to characterise them. Chapter 6 comprises the efforts in the fabrication and characterisation of proof-of-concept IL cells. Chapter 7

explores the efficiency potential of IL cells and points to ways to improve the cell architecture. Chapter 8 summarises the major findings in this thesis and provides an outlook of future research directions on this topic.

Chapter 2 History and Design of Inversion Layer Cells

2.1 Previous Research on Inversion Layer Cells

The emitter of an inversion layer cell is formed by the accumulation of charge carriers that are induced by an external electric field. For a p-type inversion layer cell, the electric field attracts electrons to the surface so that the local electron density exceeds the hole density in the substrate and forms an n-type inversion layer. The opposite is the case for an n-type inversion layer cell. The electric field can be accomplished by (i) a voltage, (ii) a work function difference between silicon and metal, and (iii) fixed surface charge often contained inside dielectric coatings. Voltage application is used in metal-oxide-semiconductor field-effect transistors (MOSFET) to manipulate the conductivity of the device. The need for a voltage source limits its application in PV devices. Schottky barrier solar cells utilise the work function difference between metal and semiconductor to form an emitter [85]. In inversion layer cells, the electric field is provided by fixed charge in dielectric layers [72]–[76]. Previous work and cell designs of inversion layer cells are reviewed in this section.

2.1.1 Low-Work Function Metal to Induce an Inversion Layer

Figure 2-1 depicts the structure of a Schottky barrier solar cell developed by Andersen et al. [85]. In their work, the inversion layer was induced on a 2 Ω·cm p-type silicon substrate by

full-area coverage of low-work function semi-transparent metal, in this case, 4.4 nm of chromium. Copper fingers of 5.8 nm in thickness were deposited for improved conductivity. A silicon oxide layer of 69 nm in thickness was deposited in between fingers as an antireflection coating. This structure resulted in an efficiency of 8%. The factors limiting the cell performance include (i) low light transmittance due to full-area semi-transparent metal coverage, (ii) high lateral resistance in the thin metal layer, and (iii) low V_{OC} as V_{OC} is limited by the work function difference between metal and silicon substrate. These limitations indicate that a cell architecture with full-area semi-transparent metal coverage at the front is not ideal for harvesting solar power.

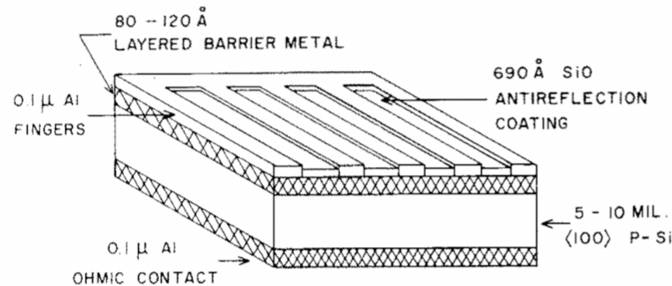

FIG. 1. Structure of a layered Schottky-barrier solar cell.

Figure 2-1 Structure of a layered Schottky barrier solar cell by Andersen et al. [85].

2.1.2 Fixed Dielectric Charge to Induce an Inversion Layer

Fixed charge in dielectric material can be used to induce the inversion layer while maintaining low parasitic absorption. In addition, the thickness and refractive index of the dielectric layer can be engineered to allow maximum light transmittance. It was reported in 1978 [74] that intrinsic charge in silicon oxide thin films grown by chemical vapour deposition (CVD) has been used to induce the IL. Later on, in 1980, Thomas et al. applied spin-on tantalum oxide layers containing silicon oxide onto a silicon substrate and achieved a charge density of 1-3 × 10^{12} cm^{-2} [72]. They proposed that there are trapped ions at the

interface due to the presence of unsaturated tantalum bonds and that these trapped ions are responsible for the charge. This has led to the formation of IL emitters with a sheet resistance of 7-15 kΩ/sq being induced on 8-10 Ω·cm p-type silicon substrates. Hezel et al. reported silicon nitride grown by CVD as a stable source of positive charge in 1981 [75]. In their work, a charge density of 7×10^{12} cm^{-2} has been confirmed. In the same work, they demonstrated that by applying an external bias, the charge density can be boosted to 1.4×10^{13} cm^{-2}. However, the extra charge has been proved unstable at elevated temperatures. The same group has later observed that the addition of caesium before depositing silicon nitride can provide a charge density of 1.1×10^{13} cm^{-2} [77], [86]. In the literature reviewed thus far, the positive charge has been used to induce n-type emitters on p-type substrates. With negatively charged dielectrics p-type emitters can be formed on n-type substrates. The work by Werner et al. [73] in 2014 has demonstrated that aluminium oxide deposited by plasma-assisted atomic layer deposition (ALD) can provide negative charge with a density of -4×10^{12} cm^{-2}. In this work, they proposed that the negative charge originates from oxygen-related point defects at the Si/AlO_x interface. In the same study, they have demonstrated that the aluminium oxide layer can induce a p-type inversion layer with the sheet resistance of 15-18 kΩ/sq on 1.5-1.6 Ω·cm n-type silicon substrates in the dark, and < 4 kΩ/sq under typical solar cell operating conditions. Later in the same year, the same group reported in [87] that by applying an external bias, the net negative charge in aluminium oxide can be boosted to -10^{13} cm^{-2}. However, the extra charge is a result of charge carriers trapped at the interface or in the dielectric material and is unstable. The boosted charge has been observed to decay at elevated temperatures (300-350 °C) and is not compatible with commercial PV devices. Table 2-1 shows a summary of dielectric materials used to induce inversion layers in previous studies. The table shows that sheet resistance reported for field-induced emitters

(7-18 kΩ/sq) is significantly higher than that of typical diffused emitters (90-160 Ω/sq [10]). This will lead to higher resistive losses in field-induced emitters compared to diffused emitters. Narrow finger spacings of 100-500 μm have been used in cell designs to compensate for the high resistive losses, while finger spacings of 0.7-1.6 mm [88] are used for P-diffused emitters in mainstream PERC devices. The narrow finger spacing will lead to a large metallisation area, which indicates (i) high shading losses for IL cells with a front-emitter design, and (ii) high recombination losses due to the large metal-silicon contact area. Previous works on IL cells indicate that the charge densities are not high enough to induce a sufficiently conductive emitter to compete with diffused emitters. The first challenge in developing IL cells is therefore to produce higher charge densities in the dielectric layer, reduce lateral resistive losses and relax the need for narrow finger spacings [73], [78]–[81].

Table 2-1 Summary of dielectric materials used to form induced IL emitters in previous studies.

Dielectric material	Charge polarity	Charge density (10^{12} cm^{-2})	Emitter R_{sh} (kΩ/sq)	Base resistivity (Ω·cm)	Finger spacing (μm)	Efficiency	Citation
SiO_x				2.5-12	100	12%	[74]
Ta_xO_y/SiO_x	+	1-3	7-15	8-10	254	16%	[72]
SiN_x	+	7		0.5	150	12.4%	[75]
SiN_x	+	14					[75]
SiN_x with Cs	+	>10					[86]
SiN_x with Cs	+	11		1-2		14.5%	[77]
AlO_x	-	4	15-18 in dark <4 under illumination	1.5-1.6			[73]
AlO_x	-	4		5	500	18.1%	[73]
AlO_x	-	10					[87]

2.1.3 Metallisation Design in Inversion Layer Cells

Metallisation that connects to the inversion layer is necessary so that carriers separated at the *pn* junction can transport to the external circuit. For cell designs with localised metallisation, the formation of the inversion layer underneath the metals may be interrupted since there is no charged dielectric material or low-work-function metal in such contact regions. Therefore, measures are required to ensure that the inversion layer is effectively connected to the carrier-extracting metal electrodes.

One geometry that enables both metallisation and formation of the inversion layer is a metal-insulator-semiconductor (MIS) structure. Schottky barrier solar cells use an MIS geometry at the front [79], [85]. The full-area metal coverage can both induce an inversion layer and collect separated carriers. The insulating silicon oxide layer is typically 1-2 nm thick [79], which allows carriers to tunnel through while keeping the surface well passivated. Figure 2-2.a shows the band diagram of an MIS structure [85]. Despite the limitations of Schottky barrier solar cells, the MIS structure can be utilised locally for metallisation while dielectric material with fixed charge can be deposited elsewhere to induce the inversion layer. Figure 2-2.b depicts the structure of an MIS-IL cell [74]. In this design, the fixed charge in the dielectric layer and the low-work function metal (aluminium in this case) ensures a complete n-type inversion layer, so that carriers generated across the cell can transport to the metal fingers. In Schottky barrier cells, the metal layer is 4-5 nm thick because of the trade-off between electrical resistance and optical transmittance [79], [85]. In the MIS-IL design, the dielectric material in most of the surface area allows high transmittance. The requirement for a thin metal layer is thus relaxed, such that the metal fingers are thicker in MIS-IL cells. The MIS-IL geometry has been utilised in IL cells reported in [74], [72], [75], [77],

demonstrating a complete electrical path for separated carriers to reach the external circuit. However, the limitations in fabricating the MIS-IL structure include the following [78]:

(i) The process requires thermal evaporation of aluminium that needs a vacuum and is therefore a low-throughput and costly process.

(ii) The process is not compatible with high-temperature procedures. The contact will be damaged at temperatures above 400 °C as the tunnel oxide will be reduced by the overlying aluminium. This indicates that high-temperature procedures are to be avoided after the formation of the MIS structure. This requirement can lead to a complicated fabrication procedure.

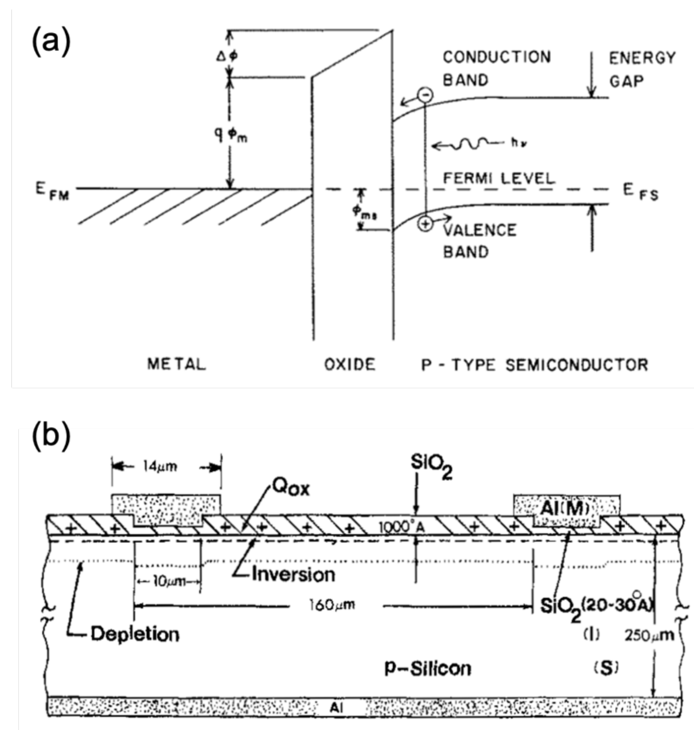

Figure 2-2 (a) Energy band diagram of an MIS structure [85]. (b) Schematic of an MIS-IL cell structure [74]

Another strategy to ensure a complete n-type emitter layer is via laser doping. Laser doping is a fast and cost-effective way to ensure local doping underneath metallisation. This process requires the presence of a dopant precursor. Upon laser beam scanning, the dielectric

material will be ablated while the silicon underneath will melt, allowing dopant atoms to diffuse in and the region to be counter-doped. This technique is compatible with current commercial technologies and has been commercialised in the solar cell industry for various applications. For example, it has been used to ablate dielectric material for localised contacts [89] and selectively introduce additional dopant atoms in P-diffused emitters [62]. It has also been used for contact formation in IL cells [73]. Figure 2-3 shows the schematic of an IL cell reported by Werner et al. [73]. The IL cell has a rear-emitter design. The AlO_x layer at the rear has been used (i) to provide fixed negative charge to induce an emitter, and (ii) as an aluminium dopant precursor so that the region underneath can be counter-doped into p-type. After laser doping, they deposited full-area aluminium paste at the rear for electrical contact. The rear-emitter design removed the difficulty of having a high area fraction being used for metallisation since the metal is now at the rear where no light is shining. The AlO_x dielectric layer together with laser doping and the rear-emitter design has demonstrated a proof-of-concept IL cell with an efficiency of 18.1%. In the same work, they suggested that with optimised processing, an efficiency of 26.3% can be achieved. Apart from full-area metallisation, laser doping is also compatible with electroplating, which allows the fabrication of self-aligned metal fingers without the use of high-temperature steps or photolithography. An electroplated Ni/Cu/Ag stack has been developed and has been shown promising for implementation in industry [90], [91]. A thin nickel layer serves as a seed layer as well as a diffusion barrier that prevents copper from contaminating bulk silicon. Copper is cheap, abundant, with a high conductivity comparable to silver. It is used in the stack to ensure low grid resistance. A thin silver layer on top protects the copper from oxidation and from reacting with EVA encapsulants [90]. With recent progress in electroplating, a finger width of 12 μm has been demonstrated in [91]. The research

reviewed above indicates that laser doping together with electroplating allows fast and low-cost self-aligned metallisation and is therefore promising to be used for metallisation of IL cells.

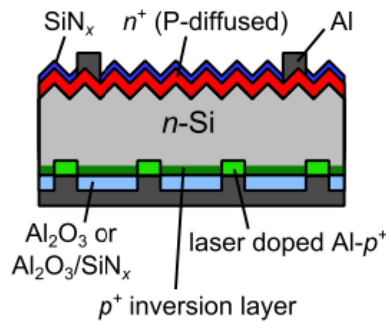

Figure 2-3 Schematic of an n-type inversion layer cell with a rear-emitter design [73].

2.1.4 Discussion and Summary

To form a field-induced emitter, the accumulation of charge carriers near the surface can be achieved by work function difference between metal and silicon substrate and/or by fixed charge in dielectric thin films. For Schottky barrier solar cells, the inversion layer is induced by a full-area deposition of a low-work function metal. The metal layer needs to be thin for maximum light transmittance, which inherently leads to high lateral resistance. The work function difference between the metal layer and silicon substrate determines the maximum V_{OC} possible for the cell. The trade-off between transmittance and resistive losses together with the low-work function difference limits the performance of Schottky barrier solar cells.

In IL cells where emitters are induced by fixed dielectric charge, the thickness of each layer in the dielectric stack can be adjusted for maximum light transmittance. SiO_x, Ta_xO_y, SiN_x, SiN_x with the inclusion of Cs, and AlO_x have been used to induce inversion layers [72]–[75], [77], [86], [87]. Using such charged dielectrics, an emitter sheet resistance in the order of several kΩ/sq has been achieved, while the corresponding finger spacing lies in the range of

100-500 μm. For typical diffused emitters, the sheet resistance is 90-160 Ω/sq [10], and the finger spacing is 0.7-1.6 mm [88]. In comparison with diffused emitters, the field-induced emitters are much more resistive. This indicates narrower finger spacings necessary and therefore unavoidable larger metallisation area. This will lead to large shading losses and carrier recombination at the metal-silicon contact. The efficiency of the IL cells has therefore been limited by the high emitter sheet resistance. The maximum stable charge density that has been achieved in the literature is 1.1×10^{13} cm^{-2} [77]. Higher charge densities may be necessary to obtain more conductive emitters and higher IL cell efficiencies.

For IL cells with the emitter induced by charged dielectrics and localised metallisation, the formation of the inversion layer may be interrupted under metallisation due to the absence of charged dielectric material. Therefore, local doping underneath the contact is necessary to ensure electrical connection from the metal to the inversion layer. Despite the limitations of Schottky barrier cells, the MIS structure has been used for metallisation in IL cells where charged dielectrics are used to induce the inversion layer in the rest of the area [74], [72], [75], [77]. The efficiencies of such designs are in the range of 12-16%. Although the requirement for a thin metal layer in the MIS structure has been relaxed, the MIS-IL structure is limited by (i) the requirement of a vacuum for thermal evaporation and (ii) that the MIS structure is not compatible with high-temperature procedures. Laser doping in combination with electroplating is a fast and cost-effective method for self-aligned metallisation. Laser doping is a developed technology and has been commercialised in the solar cell industry for various applications. Recent progress in electroplating has shown promising results with a finger width of 12 μm [91]. Since this technique fulfils the requirements of both local doping and metallisation, it can be integrated into the fabrication of IL cells.

2.2 Ion-Charged Oxides for Inversion Layer Cells

Intrinsic charge in dielectric materials or at the silicon-dielectric interface has been used to induce the emitter in IL cells [72]–[75], [77], [86], [87]. The efficiency of those IL cells has been limited by their high emitter sheet resistance, which is due to the low charge density in the dielectric thin films. An ion injection method has shown the potential to reach high charge densities on a silicon-silicon oxide system [82]. This method may be able to reach higher charge densities so that the emitter sheet resistance can be brought down. This method was developed by Bonilla and Wilshaw in 2014 [82] to provide a high dielectric charge density for field-effect passivation. The method involves the incorporation of a controllable concentration of positive alkali ions into silicon oxide thin films. In their work [82], [83], a sub-monolayer concentration of alkali salt, such as potassium chloride, was delivered onto the surface of an oxide-silicon structure to avoid crystallisation. The method then utilises a combined drift and diffusion mechanism at an elevated temperature to migrate positive alkali ions through silicon oxide and reach the oxide-silicon interface. They explained the kinetics of the ion migration process with the help of simulations in [83]. Figure 2-4 shows the energy diagram of ion traps in the air-silicon oxide-silicon system and the effect of an external electric field. Their simulation results revealed that the positive alkali ions at the air-oxide interface will de-trap at a high temperature, diffuse into the oxide, and eventually reach the low-energy states at the oxide-silicon interface. Collett et al. have demonstrated that the migration can be finished in under 2 s at 450 °C and that the ions will then freeze at the oxide-silicon interface upon cooling down to room temperature [92]. The same group reported in [83] that a charge density of 5×10^{12} cm^{-2} has been achieved. This implies that with more ion precursors, it is possible to obtain higher charge densities. In the same work, the passivation quality was monitored over 1500 days in laboratory conditions and has been

tested stable. It has been demonstrated that the ion injection method provides a fast and cost-effective way to incorporate high concentrations of positive alkaline ions into the dielectric thin film. The high charge density with good stability suggests the promising application of the ion injection method in the fabrication of IL cells.

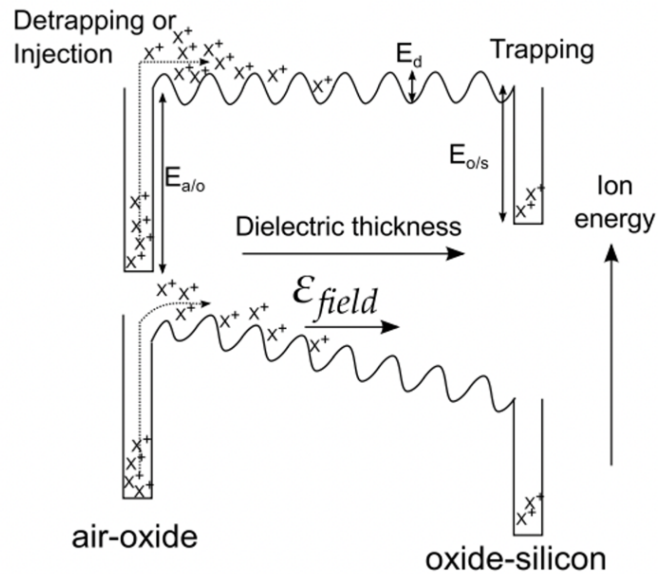

Figure 2-4 Energy diagram of ion traps in the air-silicon oxide-silicon system and the effect of an external electric field [83].

Chapter 3 Experimental Methods

3.1 Silicon Substrate Material

Silicon substrates can be fabricated into n-type or p-type depending on the dopant atoms. Both types are used to fabricate single crystalline silicon solar cells in industry. The current mainstream PERC technology uses p-type silicon substrates [93]. The emerging technologies with passivating contact designs, TOPCon and SHJ, are moving towards n-type silicon substrates thanks to their higher carrier lifetimes [93], [47]. The advantages of p-type substrates include: (i) lower fabrication cost [94], [95], and (ii) higher minority carrier (electrons) mobility [96] so that carriers generated farther from the *pn* junction can contribute to the photocurrent. It has been noticed that silicon substrates have been fabricated thinner [10] and that the thicknesses are equal to or lower than the diffusion length [97]. Therefore, the diffusion length does not limit the cell performance anymore. For n-type substrates, although the fabrication cost is higher [94], [95], they are inherently more tolerant to metal impurities because the capture cross-section is higher for electrons than for holes [70]. In this work, boron-doped p-type substrates were used to demonstrate the properties of the field-induced electron layer as an emitter. Although gallium doping is dominating in p-type wafers in industry [9], boron doping was the mainstream at the beginning of this project. For simplicity in characterisation, the field-induced electron layer was induced on n-type substrates as an accumulation layer.

Silicon substrates can also be categorised by fabrication method. The majority of silicon substrates used in the industry are produced using Czochralski (CZ) method due to its low production cost and high throughput [98]. However, silicon ingots produced using this method contain high concentrations of oxygen impurities (5-11 × 10^{17} cm^{-3}), leading to electrically active defects [99]. Additionally, the electrical resistivity has been shown to be inhomogeneous both azimuthally and radially in the ingot to the extent of 1-3% [100]. Purer silicon wafers with better doping homogeneity can be fabricated using the float zone (FZ) method. FZ silicon substrates have not been used in mass production due to their high production cost [101], [102]. A review of the CZ and FZ methods can be found in references [98] and [101]. Silicon substrates fabricated using both CZ and FZ methods were used in this thesis. Details of the silicon substrates and their surface finish are described in the following subsections.

3.1.1 Silicon Wafers

Table 3-1 shows a summary of silicon substrates used. The FZ silicon wafers are 200 μm thick, 1 Ω·cm doped with either boron or phosphorus atoms. The surface was chemically polished on both sides, exposing (100) planes. They were received from Fraunhofer ISE with thermal silicon oxide grown on both sides, as described in Section 3.2. The CZ wafers are 180 μm thick, 1 Ω·cm doped with boron atoms. They were received from the University of New South Wales (UNSW). These wafers have a pyramid-textured surface, thermal silicon oxide grown on both sides, and rear metallisation. The FZ wafers were labelled as Set A. The CZ wafers were labelled as Set B.

Table 3-1 Summary of silicon substrate materials used in this thesis.

	Resistivity	Thickness (μm)	Sample size	Surface	Source
n-type FZ Si	1 Ω·cm	200	Circular wafers 200 mm diameter	Polished	Fraunhofer ISE
p-type FZ Si	1 Ω·cm	200	Circular wafers 200 mm diameter	Polished	Fraunhofer ISE
p-type Cz Si	1 Ω·cm	180	4 × 4 cm^2	Textured	UNSW

3.1.2 Surface Finish

The surface morphology of silicon substrates is important in terms of the optical properties of silicon solar cells. Pyramid-textured surfaces are commonly used in the PV industry since light reflected from a textured surface is more likely to be redirected to other surface regions compared with polished planar surfaces. This leads to more photons absorbed by the silicon substrate and increased cell efficiency. The texturing of Set B specimens was carried out by submerging bare silicon wafers into an anisotropic etching mixture of KOH and IPA (isopropyl alcohol). (100) planes are etched preferentially in such solutions [103], leaving only (111) planes exposed at the surface. Due to the crystalline structure of silicon, pyramid-like features were formed across the surface, termed random pyramid texture. Although this textured surface improves light absorption, it leads to an increase in surface area. In addition, (111) planes are known to have a higher density of interface states than (100) planes [104]. These factors combined will result in more carrier recombination at the surface/interface. This work investigates field-induced charge layers near the surface. The impact of surface texture and (100)/(111) planes on the field-induced charge layers needs to be considered.

Since the current path within the charge layers is less complicated for substrates with planar surfaces, Set A specimens with planar surfaces were used to study the properties of the charge layers. Set B specimens with the random pyramid texture were used in the fabrication of prototype inversion layer cells for improved light trapping.

3.2 Silicon Oxide Growth

Silicon surface dangling bonds introduce energy states deep in the bandgap that act as strong recombination centres. Saturating the dangling bonds reduces the density of these energy states and can in turn improve the minority carrier lifetime. These energy states can be passivated chemically using dielectric materials. A silicon oxide layer is commonly used for this purpose. Both Set A and Set B samples have silicon oxide thermally grown on both sides. This process requires a high temperature and an oxygen-rich atmosphere. For Set A samples, the wafers were heated to 950/1050 °C in an atmosphere of oxygen and dichloroethylene to form a silicon oxide layer of 10/100 nm thick, respectively. For Set B samples, 20/100 nm thermal oxide was formed on the surface in a dry oxygen atmosphere at a temperature of 890/1000 °C for 25 min, respectively. The labelling of the subsets will be introduced in Section 3.4.

3.3 Extrinsic Chemical Passivation

The passivation of silicon dangling bonds can be enhanced by introducing hydrogen. Hydrogen atoms are small and can diffuse within dielectric materials to the interface and saturate the remaining dangling bonds. Hydrogen was introduced by annealing the samples in a 5% H_2/95% N_2 gas atmosphere at 425 °C for 30 min. This process is termed forming

gas anneal (FGA). Some Set A samples underwent this process, creating additional sample subsets.

3.4 Sample Labelling

Set A and Set B specimens were processed differently regarding surface finish, oxidation, and hydrogenation. Each sample geometry was assigned a label. After surface finish and oxidation, metallisation was formed on the rear of Set B samples. This process will be described in Section 3.7.1. Table 3-2 shows a list of all sample sets used in this work.

Table 3-2 Summary of sample sets used in this thesis.

Sample label	Silicon substrate	n/p-type	Oxide thickness	Oxidation temperature	Hydrogenation
A1	FZ, planar	n-type	100 nm	1050 °C	FGA
A2	FZ, planar	n-type	100 nm	1050 °C	None
A3	FZ, planar	n-type	10 nm	950 °C	FGA
A4	FZ, planar	p-type	100 nm	1050 °C	None
B1	CZ, textured	p-type	20 nm	890 °C	None
B2	CZ, textured	p-type	100 nm	1000 °C	None

3.5 Field and Temperature-Assisted Ion Migration Method

The aim of this thesis is to obtain a high dielectric charge density for improved conductivity of field-induced emitters in IL cells. The approach is to incorporate a high concentration of positive K^+ ions into oxide thin films using a field and temperature-assisted ion migration method. Figure 3-1 shows a schematic of the procedure. This method requires (i) the presence of an ion precursor at the dielectric surface for which I used a KCl salt, (ii) an electric field that drives the positive K^+ ions into the oxide, and (iii) an anneal step that

provides energy for K^+ ions to migrate through the silicon oxide thin film and reach the Si/SiO_2 interface. The subsections below will introduce these steps in detail.

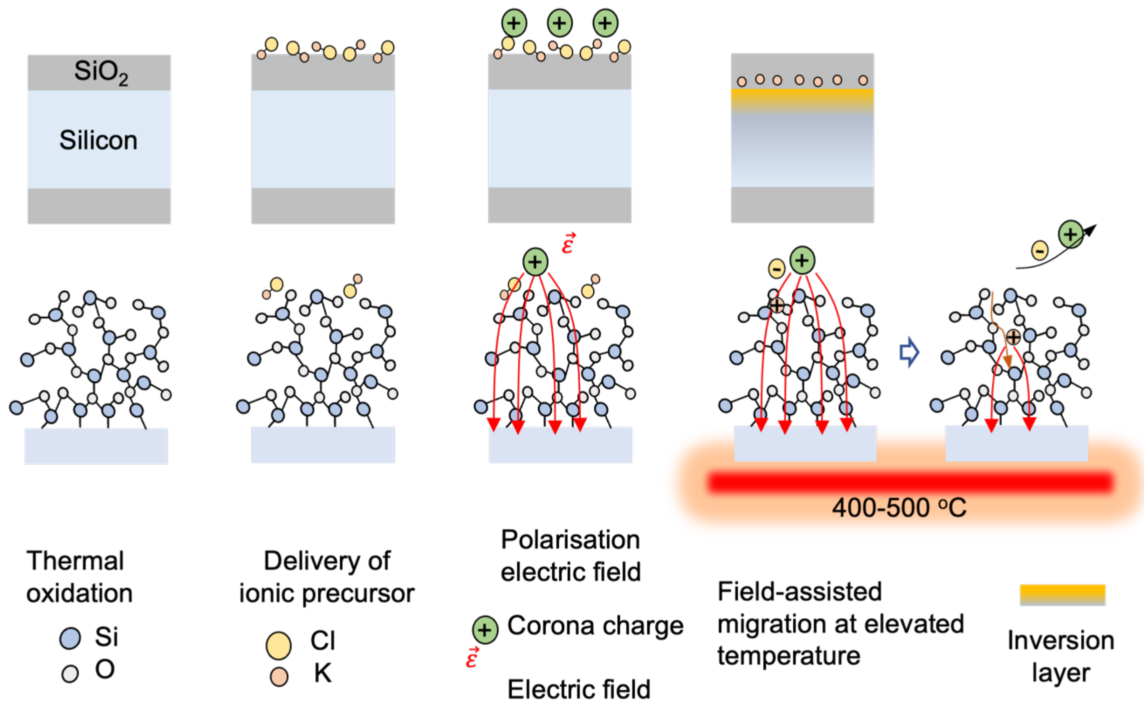

Figure 3-1 Processing method of field and temperature-assisted migration of K^+ ions into surface dielectrics: delivery of ion precursor, applying a polarisation electric field, and annealing.

3.5.1 Introducing Ion Precursor

The ion precursor can be delivered via spin coating, spray coating or thermal evaporation [92]. All three methods have been proved efficient [92]. Spin coating was used in this work for simplicity. Potassium chloride salt was dissolved into a mixture of 30% deionised (DI) water and 70% IPA. The solution was spin-coated onto the sample surface. IPA was added to the solvent to improve the wettability of the solution to the dielectric surface and allow faster evaporation of the solvent at room temperature. The solution was pipetted onto the sample surface and distributed by a two-step spin process. The spin coater was first kept at a low spin speed of 500 rpm for 6.5 s so that the entire surface was covered by the solution.

The spin speed was then increased to 3000 rpm to reach the desired film thickness. The spin speed of 3000 rpm was maintained for 30 s for the solvent to evaporate. The spin coating process was developed by S. Du [105]. The ion precursor solution should be prepared such that the concentration is sufficiently low to avoid crystallisation while providing enough ion atoms for charge embedding. The ion density of a monolayer in the KCl lattice is calculated as follows:

$$\text{Ion density (KCl)} = 2 \times \frac{\rho}{M} \times N_A \times \frac{a}{2} \qquad \text{Eq (3-1)}$$

where M is the molar mass of KCl (74.55 g/mol), ρ is the density of KCl crystal (1.98 g/cm^3), N_A is the Avogadro constant, and a is the lattice constant of the face-centred cubic crystal structure of KCl (6.36 Å). As a result, the ion density in a monolayer is 1.02×10^{15} $ions/cm^2$, which can be used as a reference to prepare the KCl solution. For the spin speed of 3000 rpm, the approximate thickness of the film is 4 μm [105]. KCl solutions with two different concentrations were prepared in this work: 10^{-3} mol/L (Concentration A) and 5×10^{-3} mol/L (Concentration B), corresponding to an ion density of 4.8×10^{14} $ions/cm^2$ and 2.4×10^{15} $ions/cm^2$ on the sample surface, respectively. Concentration B is just above the limit for sub-monolayer distribution. This may lead to KCl crystallisation at the sample surface and inhomogeneity in the distribution of K^+ charge in the dielectric. This should be avoided in future experiments. However, the concentration is not excessively higher than the limit and should still provide a large concentration of potassium atoms for ion migration. With multiple ion migration processes, Concentration A demonstrated the gradual formation of the field-induced electron layer. Concentration B allows a higher density of positive K^+ ions to be incorporated into the oxide thin film after each spin coating and was used for faster ion incorporation.

3.5.2 Corona Discharge

Corona discharge was used to provide an electric field across the dielectric material and drive the migration of the positive K^+ ions. Figure 3-2.a shows a schematic of the corona discharge rig. A voltage was applied between two electrodes. One is a sharp stainless-steel pin (discharge electrode). The other is a grounded metal plate. The discharge electrode was kept 20 cm above the grounded electrode. During corona discharge, a high voltage (±30 kV) was applied between the two electrodes, generating an electric field in between, as illustrated in Figure 3-2.a. The electric field is strong around the sharp discharge electrode, which ionises surrounding air molecules [106]. The electric field will then drive the charged molecules towards the grounded electrode. Corona ions in both charge polarities can be generated. Previous reports showed that the positive corona ions are mostly $(H_2O)_nH^+$, and the negative corona ions are CO_3^- [107], [108]. The samples in this work were placed on the grounded electrode. Upon corona discharge, positive/negative corona ions will be deposited onto the dielectric surface, providing an electric field across the thin oxide film.

The uniformity of the corona ion deposition can be represented by variations in current density across the area where samples were placed. The current density (J) was estimated using Warburg's law [109], [110]:

$$J = J_0 \cos^5(\theta) \qquad \text{Eq (3-2)}$$

where J_0 is the peak current density, θ is the angle relative to the plate normal. The geometry is illustrated in Figure 3-2.b. For a given radial distance from the point electrode, θ will decrease with increased pin-to-plate distance. This will lead to a more uniform deposition of corona ions on the sample. For the 20 cm pin-to-plate distance in the rig, the variation in

corona ion density is less than 1% across a 4 × 4 cm^2 area, which is the size of the largest sample used in this work. The corona charge density is thus considered homogeneous.

The density of corona ions was altered by adjusting the corona discharge time. The relation was calibrated using the Kelvin Probe technique, introduced in Section 3.6.1. The calibration will be shown in Section 3.6.2. The corona ions deposited onto the dielectric surface are known to be unstable in the uncontrolled laboratory atmosphere. It has been reported that the adsorption of water molecules will increase the lateral conductivity at the dielectric surface, which can accelerate the dissipation of the corona charge [111], [112]. Here the samples were annealed immediately after corona discharge to allow ion migration without corona leakage effects.

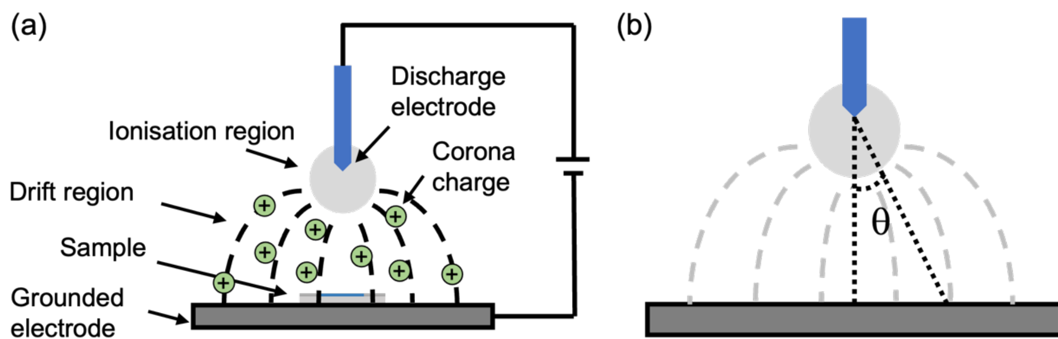

Figure 3-2 (a) Schematic of the corona discharge rig. (b) Schematic of the pin-to-plate geometry.

3.5.3 Ion Migration

With the ion precursor delivered to the dielectric surface and corona ions providing an electric field across the oxide thin film, the samples were annealed at 430 °C for 10 s on a hot plate. The anneal provides the K^+ ions with sufficient energy to de-trap from the air-oxide interface, migrate through the oxide layer in a combined drift and diffusion mechanism, and reach the low-energy states at the oxide-silicon interface [83]. The positive

K^+ ions induce mirror electrons in bulk silicon, forming a field-induced inversion/accumulation layer. Corona discharge and anneal cycles were repeated multiple times to allow migration of as much K^+ ions as possible delivered to the dielectric surface towards the oxide-silicon interface. Higher charge densities can be obtained by further replenishment of the KCl ion precursor by spin coating, and subsequent corona discharge-anneal cycles after each spin coating.

3.6 Electrical Characterisation

3.6.1 Kelvin Probe Measurements

Kelvin Probe (KP) was used to measure the density of corona ions deposited on the dielectric surface. KP is a non-contact method that detects the difference in work function between two surfaces. In the Kelvin Probe (KP020JS by KPTechnology) tool used in this work, the work function difference between a gold probe with known work function (Φ_m) and the dielectric/silicon structure was measured. Figure 3-3 shows a schematic of the metal probe-air-dielectric-silicon structure and its band diagram. The gold probe was electrically connected to the silicon substrate and was brought close to the dielectric surface. The gold probe forms a capacitor with the dielectric/silicon structure. Due to the difference in the work function of the two electrodes, the capacitor will be charged when no external bias is applied, following the equation:

$$Q = C \times V \quad \text{Eq (3-3)}$$

where Q represents the charge stored in the capacitor, C is the capacitance, and V is the contact potential difference. The metal probe oscillated above the dielectric/silicon structure,

leading to an alternating change in the distance between the probe and the sample, and hence the capacitance and the charge. This will result in a detected current (I_b) in the circuit:

$$I_b = \frac{dQ}{dt} = \frac{dC}{dt}V \qquad \text{Eq (3-4)}$$

The current was monitored during the measurement. A bias, termed backing potential (V_b), was applied to the silicon substrate. When the applied V_b cancels the contact potential difference, I_b in equation Eq (3-4) will be zero. Baikie's method [113] was used to find the backing potential that nullifies I_b. In Baikie's method, a range of V_b values are applied to the sample. V_b and the recorded I_b are then plotted and extrapolated to find the V_b that nullifies the current. The V_b found is the contact potential difference between the two electrodes and is labelled V_{KP}.

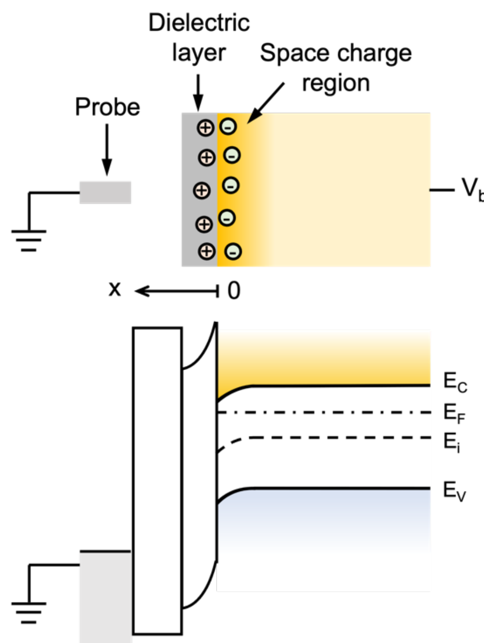

Figure 3-3 Schematic of the metal probe-air-dielectric-silicon structure in a Kelvin probe setup and the band diagram of the structure with an external bias applied to the silicon substrate so that the Kelvin probe current is nullified. Redrawn from [114].

The contact potential difference can also be represented as:

$$V_{KP} = \frac{\Phi_{ms}}{q} + \phi_{scr} + V_i \qquad \text{Eq (3-5)}$$

where Φ_{ms} is the work function difference between metal (gold) and silicon, q is the electron elementary charge, ϕ_{scr} is the surface potential due to the space charge region, and V_i is the potential difference across the insulating dielectric layer. The work function of gold is 5.1 eV [115]. The work function of silicon is a function of dopant type and dopant density and has been well understood [116]. ϕ_{scr} can be calculated following Girish's algorithm [117]. Previous work in [118] has proved that $|\phi_{scr}|$ is below 0.25 V for surface charge densities below 10^{13} cm^{-2} when the charge is located far from the silicon surface, for example, at the surface of a 100 nm SiO_2 film. The ϕ_{scr} term can thus be neglected. In Eq (3-5), with measured V_{KP} and known Φ_{ms}, V_i can be obtained to work out the density of corona ions deposited. Assuming no charge in the air gap, V_i can be calculated as:

$$V_i = \frac{1}{K_i \varepsilon_0} \int_0^t x \rho_i(x) dx \qquad \text{Eq (3-6)}$$

where K_i is the relative permittivity of the dielectric material, ε_0 is the vacuum permittivity, x is the distance from the silicon-dielectric interface, $\rho_i(x)$ is the local density of charge in the dielectric material, and *t* is the thickness of the dielectric layer. Here all charge in the dielectric layer was assumed to be at a plane of distance x_c from the silicon-dielectric interface. A Dirac function was hence used to describe this surface charge distribution:

$$\rho_i = \mathrm{Q} \times \delta(\mathrm{x} - x_c) \qquad \text{Eq (3-7)}$$

V_{KP} can then be represented as:

$$V_{KP} = \frac{\Phi_{ms}}{q} + \frac{Q \cdot x_c}{K_i \varepsilon_0} \qquad \text{Eq (3-8)}$$

In this work, the Kelvin Probe technique was used to measure the density of corona ions deposited at the dielectric surface. The distance of the charge plane to the silicon-dielectric interface is thus given by the thickness of the dielectric layer. The corona charge density can then be worked out using Eq (3-8).

3.6.2 Calibration of Corona Discharge Rate

In this work, corona ions in both polarities were deposited on the sample surface by corona discharge at a voltage of ±30 kV. The density of corona ions deposited was controlled by the time under corona discharge. The corresponding charge density was calibrated on A2 specimens. The surface charge concentration for corona ions in both polarities was measured using the Kelvin Probe technique after every 10 s of corona discharge for up to 180 s. Figure 3-4.a shows the recorded contact potential difference. Figure 3-4.b shows the linear fits to work out the rate of charge deposition. The deposition rate is 5.46×10^{11} cm^{-2} per 10 s for positive corona ions and -6.56×10^{11} cm^{-2} per 10 s for negative corona ions.

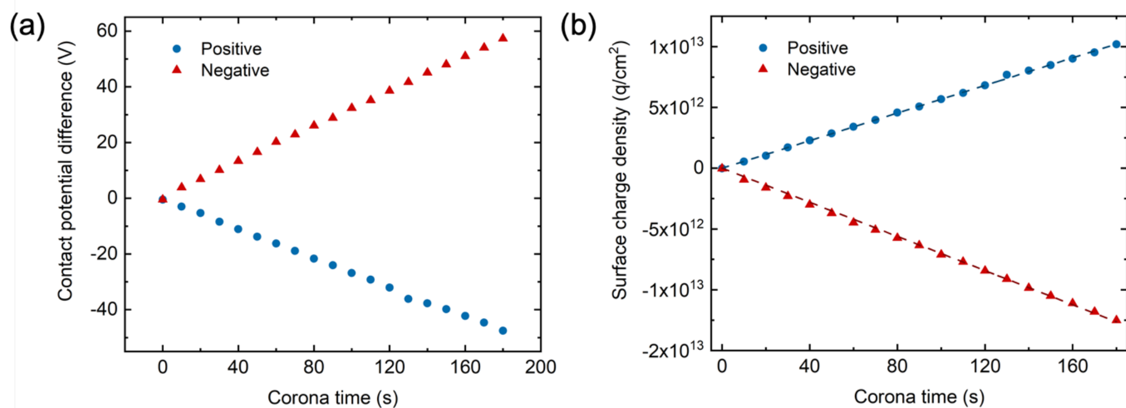

Figure 3-4 (a) Contact potential difference and (b) surface charge density measured after every 10 s of corona discharge at a voltage of ±30 kV for both polarities.

3.6.3 Sheet Resistance Measurements

Two methods were used to characterise the sheet resistance of silicon substrates that contain field-induced charge layers: the Van der Pauw (VdP) method and inductively coupled measurements. These two methods are different in terms of sample preparation and regions where free carriers contribute to measured conductance. This will lead to the methods applicable to different sample geometries.

3.6.3.1 Van der Pauw Method

Van der Pauw developed a resistance measurement method in 1958 [119]. The method is able to measure the resistivity of flat samples of arbitrary shapes. The measurement requires four infinitesimally small contacts at the perimeter of the sample. Figure 3-5.a shows a schematic of such sample. Van der Pauw proved that the following equation holds for this sample geometry:

$$e^{-\frac{\pi R_{AB,CD} d}{\rho}} + e^{-\frac{\pi R_{BC,DA} d}{\rho}} = 1 \qquad \text{Eq (3-9)}$$

where ρ is the resistivity of the material, d is the thickness of the sample. $R_{AB,CD}$ is defined as:

$$R_{AB,CD} = \frac{V_D - V_C}{I_{AB}} \qquad \text{Eq (3-10)}$$

where $V_D - V_C$ is the potential difference between contact C and contact D while a current I_{AB} is passed through contact A and contact B. The definition is similar for $R_{BC,DA}$. To isolate the resistivity in Eq (3-9), the equation is rewritten in the form:

$$\rho = \frac{\pi d}{ln2} \frac{R_{AB,CD} + R_{BC,DA}}{2} f(\frac{R_{AB,CD}}{R_{BC,DA}}) \qquad \text{Eq (3-11)}$$

where f is a function of $\frac{R_{AB,CD}}{R_{BC,DA}}$ and can be expressed as:

$$\frac{R_{AB,CD} - R_{BC,DA}}{R_{AB,CD} + R_{BC,DA}} = f \cdot arccosh\{\frac{\exp\,(ln\,2/f)}{2}\} \qquad \text{Eq (3-12)}$$

It has been demonstrated that f approaches 1 when $\frac{R_{AB,CD}}{R_{BC,DA}}$ approaches 1 [119]. Eq (3-11) can thus be simplified by implementing symmetrical sample geometries. For example, Figure 3-5.b shows a square sample geometry where $R_{AB,CD}$ is approximately equivalent to $R_{BC,DA}$. Eq (3-11) is then simplified as:

$$\rho = \frac{\pi d}{ln2} \cdot \frac{V_{DC}}{I_{AB}} \qquad \text{Eq (3-13)}$$

Due to practical difficulties in making contacts, i.e., the contacts are not often infinitesimally small, the contact size may vary, and the contact may not be at the perimeter of the sample, the accuracy of the measurement may be compromised. To eliminate the impact of contact size on the measurement, Chwang et al. calibrated the correction factor for contacts with selected shapes and a range of sizes on square samples [120]. Figure 3-5.c shows the correction factor for square and triangular contacts [120]. In this work, the square sample geometry and the triangular contacts were used for sample preparation. The resistivity can be obtained by measuring the sample thickness, taking two resistance measurements, and including a correction factor as per [120].

Figure 3-6 shows the sample geometry used in this work. Silicon wafers from group A were diced into 1 × 1 cm^2 squares. The surface dielectric at the corners was removed using a diamond scriber. Aluminium contacts 100 nm thick were deposited at the corners by masked thermal evaporation. As illustrated in Figure 3-6, the ratio of contact size to sample size

along the sample edge is 0.25, corresponding to a correction factor of 1.033 in Figure 3-5.c.

The sample sheet resistance can be obtained following:

$$R_{sh} = \frac{\rho}{d} = 1.033 \cdot \frac{\pi}{ln2} \cdot \frac{R_{AB,CD} + R_{BC,DA}}{2} \quad \text{Eq (3-14)}$$

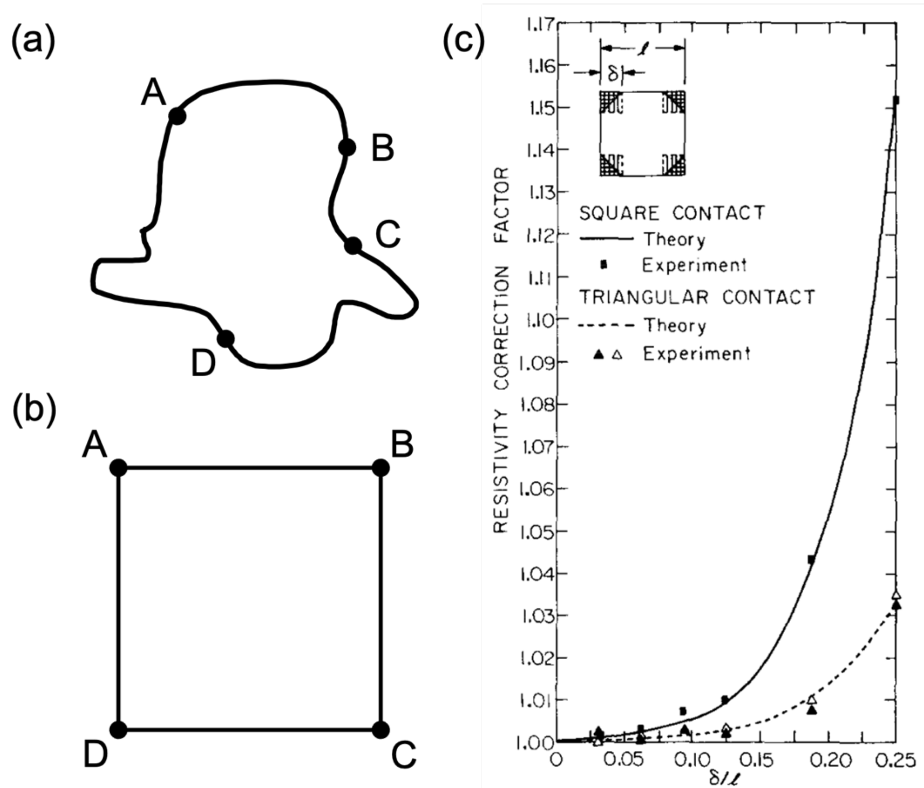

Figure 3-5 (a) Schematic of a flat sample of arbitrary shape with four contacts at arbitrary places on the perimeter of the sample. (b) A square sample geometry where four contacts are at the four vertices. (c) Correction factors for finite contact effect on resistivity measurements using the Van der Pauw method [120].

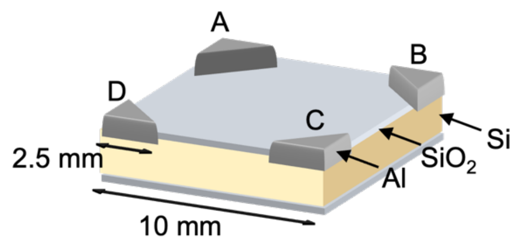

Figure 3-6 Sample structure designed for Van der Pauw measurements.

In this thesis, the Van der Pauw method was only used to measure the sheet resistance of the specimens in the accumulation regime. The reasons for this will be explained in Chapter 4. Figure 3-7 shows the schematic of the sample with/without the presence of positive surface charge. An approximation was performed using the following calculations to extract the sheet resistance of the accumulation layer. The accumulation layer sheet resistance is given by:

$$R_{sh-acc} = \frac{1}{\int \sigma(A)\, dt} = \frac{1}{\int \sigma\,(A+B)dt - \int \sigma(B)\, dt} \qquad \text{Eq (3-15)}$$

where σ is conductivity, t is thickness. Region A and B are labelled in Figure 3-7. $R_{sh}(\,A_0 + B_0) = \int \sigma(A_0 + B_0)\, dt^{-1}$ and $R_{sh}(\,A + B) = \int \sigma(\,A + B)\, dt^{-1}$ are the measurable sheet resistances of the whole wafer, prior to and after surface charge deposition. Since the accumulation of mirror electrons is supposed to lead to a significant increase in local conductivity, $\int \sigma\,(A_0)dt \ll \int \sigma\,(A)dt$ is assumed. Considering that the accumulation only occurs near the interface, for region B/B$_0$ away from the interface, $\int \sigma\,(B)dt \approx \int \sigma(B_0)\, dt$ was also assumed. The accumulation layer sheet resistance can then be calculated from the two measurable quantities as follows:

$$\begin{aligned} R_{sh-acc} &\approx \frac{1}{\int \sigma(A+B)\, dt - \int \sigma\,(A_0 + B_0)dt} \\ &= \frac{1}{R_{sh}(A+B)^{-1} - R_{sh}(A_0 + B_0)^{-1}} \end{aligned} \qquad \text{Eq (3-16)}$$

All accumulation layer sheet resistance measured experimentally presented in this thesis used this approximation. Sentaurus simulations were conducted for this sample geometry to evaluate the error of these approximations. The model used will be described in Chapter 4. The approximation was compared with sheet resistance calculated using Eq (3-15). The depth of the accumulation layer was defined as where the change in electron density per µm

in depth is below 5×10^{15} cm^{-3}, which is the dopant density of 1 Ω·cm n-type silicon substrates. The simulations indicate that, for surface charge densities above 2×10^{13} cm^{-2}, the approximation produced an error below 2.3%. The details of such simulations are included in an Appendix.

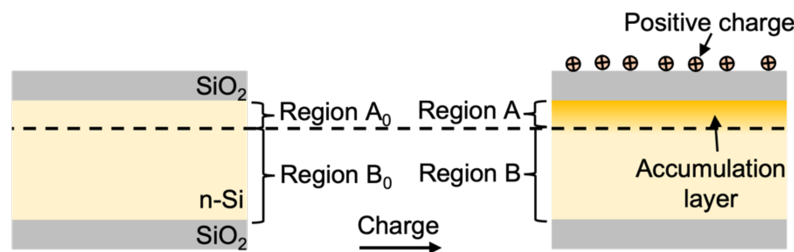

Figure 3-7 Schematic of sample structure prior to and after surface charge deposition.

3.6.3.2 Inductively Coupled Measurements

Conductance of silicon wafers can be obtained by inductively coupled measurements. A Sinton WCT-120 photo-conductance lifetime tester was used for the measurements. Figure 3-8 shows a schematic of the conductance measurement stage of the instrument. The sample is placed near the coil. The sample size needs to be larger than the coil to minimise the edge effects. An alternating current is passed through the coil, which generates an alternating magnetic field. The alternating magnetic field will induce an eddy current inside the wafer. The eddy current is opposite to the current in the coil and generates a magnetic field opposite to the original magnetic field. The eddy current and hence the overall magnetic field depend on the sheet conductance of the silicon wafer, which is determined by the sample thickness, carrier density and carrier mobility inside the silicon wafer. The change in the overall magnetic field is detected and used to work out the sheet conductance of the silicon sample. This is a non-contact characterisation tool. It was used in this thesis to monitor the sheet conductance of silicon samples in the presence of positive/negative surface charge.

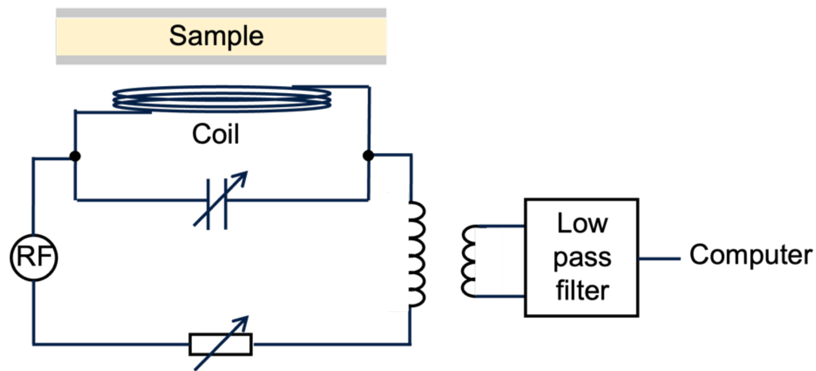

Figure 3-8 Schematic of the conductance measurement stage of a Sinton WCT-120 photo-conductance lifetime tester. Adapted from [121].

3.6.4 Recombination Characterisation

Carrier recombination at the dielectric-silicon interface is one major source of performance losses in solar cells. This work explores a novel method of forming an emitter. Crucial differences between the field-induced emitter and the mainstream diffused emitter include (i) the carrier distribution in the emitter, (ii) the presence of a high concentration of K^+ ions at the interface, and (iii) the lack of a high density of dopant atoms in the emitter. These can lead to a difference in carrier recombination at the interface. To evaluate the effect of incorporating K^+ ions on interface recombination, the minority carrier lifetime of specimens with/without K^+ ions incorporated was measured as a function of surface charge. This can reflect the interface recombination in flat-band, inversion and accumulation regimes.

3.6.4.1 Minority Carrier Lifetime

A Sinton WCT-120 photo-conductance lifetime tester was used to measure the effective minority carrier lifetime. Figure 3-9 shows a schematic of the instrument, which comprises a lamp and a conductance measurement stage. The stage detects conductance via inductively coupled measurements as introduced in Section 3.6.3.2. Upon a high-intensity flash, electron-hole pairs will be generated inside the silicon substrate. The sample size needs to

be larger than the coil to minimise the impact of carrier recombination at the edge. While the conductance of the silicon sample is constantly monitored by the stage, the conductance decay after the flash is used for lifetime analysis. The change in conductance is directly related to the concentration of photo-generated carriers (Δp). The relation can be expressed as:

$$\Delta\sigma = q\Delta p(\mu_n + \mu_p) \quad \text{Eq (3-17)}$$

where μ_n and μ_p are the electron and hole mobility, respectively. The change in excess carrier concentration over time can be calculated using the carrier generation rate (G) and carrier recombination rate (R):

$$d\Delta p = (G - R)dt \quad \text{Eq (3-18)}$$

The recombination rate can be represented as:

$$R = \frac{\Delta p}{\tau_{eff}} \quad \text{Eq (3-19)}$$

Combine Eq (3-17) to Eq (3-19), the effective minority carrier lifetime can be written as:

$$\tau_{eff} = \frac{\Delta\sigma}{Gq(\mu_n + \mu_p) - \frac{d\Delta\sigma}{dt}} \quad \text{Eq (3-20)}$$

Two analysis modes can be used to work out the minority carrier lifetime: transient mode and quasi-steady state (QSS) mode. Transient mode is used for samples with a lifetime > 100 μs and QSS mode is used for lifetimes < 100 μs. In transient mode, the conductance decay is recorded after a short flash where no excess electron-hole pairs are generated and thus G = 0. In QSS mode, a longer light pulse is used. The conductance is measured during the flash, where the excess carriers in the silicon substrate are in steady state condition and $d\Delta\sigma/dt$ is zero. The intensity of the flash is measured by a sensor near the sample on the

stage [122]. Generation is calculated based on the optics of the dielectric layer on the sample, the absorption coefficient, and the thickness of the silicon substrate.

Set A samples were used to investigate the impact of ion incorporation on interface properties. The interface recombination is dependent on both chemical passivation and field-effect passivation. Since the positive ionic charge will contribute additional field-effect passivation, no direct comparison can be made on chemical passivation. Therefore, the surface potential of the silicon samples was adjusted to eliminate this effect. This technique will be explained next.

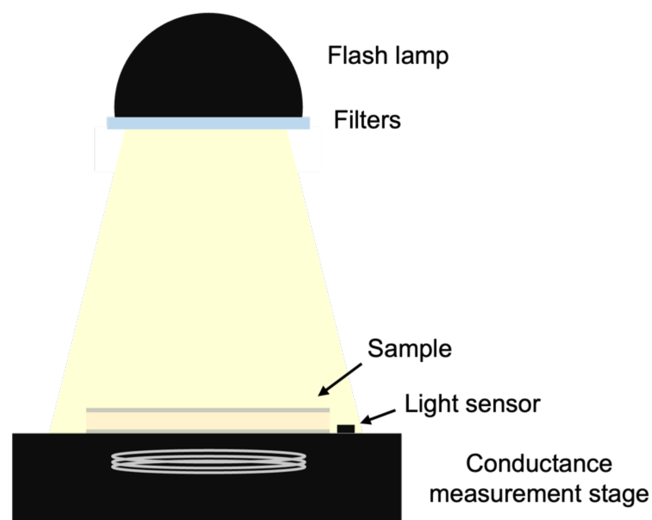

Figure 3-9 Schematic of a Sinton WCT-120 photo-conductance lifetime tester.

3.6.4.2 Lifetime as a Function of Surface Potential for Interface Characterisation

Bonilla developed a method to monitor the effective minority carrier lifetime while adjusting the surface potential of silicon substrates [123]. This will generate a lifetime curve as a function of surface potential, which can reflect the carrier recombination in flat-band, inversion and accumulation regimes. This technique can be used to evaluate the quality of surface passivation and dielectric charge density [46]. The characterisation comprises two steps: (i) obtaining the effective lifetime of the sample while regulating the surface potential,

and (ii) fitting the experimental data using an analytical model so that the interface parameters can be extracted [46]. The experimental setup to obtain the lifetime curve is illustrated in Figure 3-10. A Sinton WCT-120 photo-conductance lifetime tester was used to acquire the effective lifetime. A 3.0-4.0 wt. % poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) solution in water was coated on both sides of the sample as a transparent gate electrode. The films were annealed at 120 °C for 20 s on a hot plate to allow the solvent to evaporate and to increase the film conductivity [124], [125]. The silicon substrate was contacted by removing the dielectric material using a diamond scriber and application of Gallium-Indium eutectic and silver paint. A voltage was applied between the silicon substrate and both the front and the rear gate electrode to adjust the surface potential. The effective lifetime was recorded while the gate voltage was incrementally changed. An analytical model was used to fit the experimental data [46]. The model used Girisch and Aberle's iterative algorithm [46], [47] to work out the carrier density at the interface, n_s and p_s. With known n_s and p_s, the surface recombination velocity (SRV) can be worked out following the SRH theory [28], [29]:

$$\mathrm{SRV} = \frac{1}{\Delta n}\int_{E_v}^{E_c} \frac{(n_s p_s - n_i^2)}{\frac{n_s + n_1(E)}{v_{th} D_{it}(E)\sigma_p} + \frac{p_s + p_1(E)}{v_{th} D_{it}(E)\sigma_n}} dE \qquad \text{Eq (3-21)}$$

where v_{th} is the thermal velocity, σ_p and σ_n are the carrier capture cross-sections, $n_1(E)$ and $p_1(E)$ are the trap occupancy factors, which are expressed as:

$$p_1(E) = p_0 e^{\frac{E-E_F}{k_B T}} \qquad \text{Eq (3-22)}$$

$$n_1(E) = n_0 e^{\frac{E_F-E}{k_B T}} \qquad \text{Eq (3-23)}$$

The model considers fluctuations of fixed charge Q_f by introducing a Gaussian distribution of fluctuations with standard deviation σ_q [46]:

$$SRV = \int_{-\infty}^{+\infty} SRV\left(D_{it}, \sigma_n, \sigma_p, Q_f, \Psi_s\right) * \frac{1}{\sigma_q\sqrt{2\pi}} \exp\left(\frac{(Q_f - Q_{f0})^2}{2\sigma_q^2}\right) d\,Q_f \qquad \text{Eq (3-24)}$$

The analytical lifetime curve can then be calculated using:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_B} + \frac{1}{\tau_S} = \frac{1}{\tau_B} + SRV \qquad \text{Eq (3-25)}$$

Perfect bulk lifetime was assumed in the model, not considering the processing impurities and carrier recombination at the edge. This will lead to a larger error in the regions with strong field-effect passivation where the bulk lifetime term is more prominent in Eq (1-1). With a proper assumption of the capture cross sections σ_n and σ_p, the D_{it} profile, Q_f, and σ_q can be extracted from the fit of the experimental data.

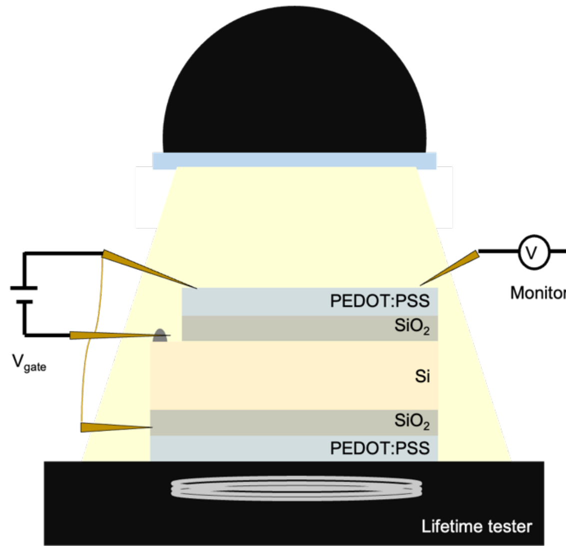

Figure 3-10 Schematic of the experimental setup to obtain the effective lifetime of silicon wafers as a function of surface potential. Redrawn from [127].

3.7 Device Fabrication Techniques

Set B samples have pyramid-textured surfaces and were used in this thesis to fabricate proof-of-concept inversion layer cells. The procedure includes rear metallisation, formation of the field-induced emitter, laser doping and electroplating for front metallisation. The ion incorporation process has been introduced in Section 3.5. The rest of the procedure will be described in the following subsections. It is important to note that the processing sequence used here is limited to the fabrication tools available in the Oxford laboratory and the geometry of samples received from collaborators.

3.7.1 Rear Contact

Rear openings were produced using a laser scriber prior to rear screen-printing of full-area aluminium paste. The wafers were baked for the solvents to evaporate and were then fired at ~825 °C set temperature for 3 s in a SCHMID (previously Sierratherm) belt furnace to form local Al-BSF. The rear metallisation was processed at UNSW.

3.7.2 Laser Doping

For inversion layer cells, local doping underneath the metal contact is necessary for the electrical connection of the field-induced emitter to the external circuit. In this thesis, laser doping was used for this purpose. For silicon substrates passivated by dielectric layers, laser doping brings in the additional benefit of exposing bare Si in the laser-doped region, which facilitates self-aligned metallisation by electroplating in a subsequent step. Figure 3-11 shows a schematic of the laser doping process. An 85% phosphoric acid solution was used as a dopant precursor and was spin-coated onto the sample surface. A laser beam was focused on the sample surface to both ablate the dielectric and melt the silicon underneath.

This allows the diffusion of phosphorus atoms into the molten region. The region will then recrystallise upon cooling and become counter-doped into n-type.

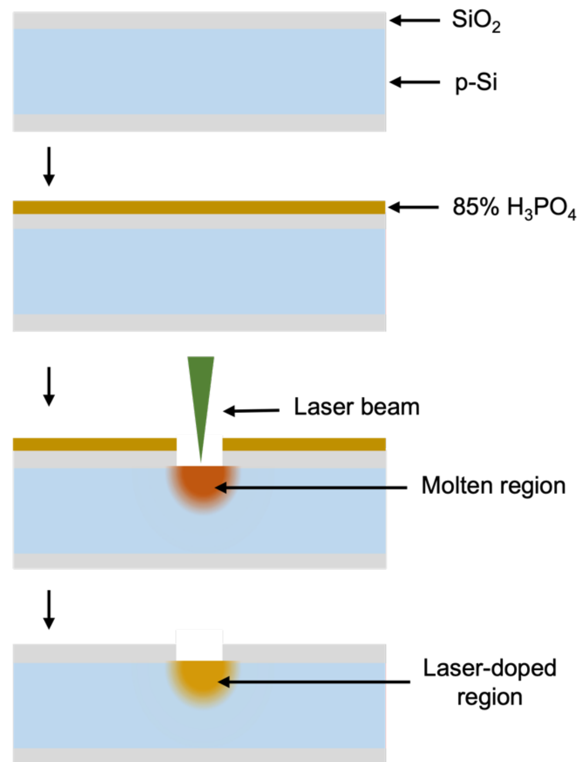

Figure 3-11 Schematic of the laser doping process.

Two different lasers were used in this work for laser doping. The first is a 355 nm nanosecond pulsed laser. The second is a 532 nm continuous wave, 20 W laser. The 532 nm laser was used to laser dope B2 samples, which were processed by partners at UNSW. An 85% phosphoric acid solution was spin-coated at a spin speed of 8000 rpm for 50 s. The laser was scanned across the same region twice at a speed of 2 m/s to ensure sufficient incorporation of dopants. The 355 nm laser became available later in Oxford and allowed for further experimentation and tuning of parameters. The 355 nm laser was used on B1 samples. An 85% phosphoric acid solution was spin-coated onto the sample surface at a spin speed of 12000 rpm for 50 s. The laser scan speed was set to 400 mm/s. The laser pulse

frequency was set to 60 kHz. The pulse length was 0.13 μs. The laser-doped B1 samples were used to fabricate prototype IL cells.

3.7.3 Light-Assisted Electroplating

Light-assisted electroplating was used for the front metallisation of Set B samples to fabricate inversion layer cells. After laser doping, bare silicon was exposed in the laser-doped regions. Positive K^+ ions were then incorporated into the dielectric layer using the ion migration method described in Section 3.5. With the field-induced emitter, photocurrent generated under illumination can contribute to the plating current and allow faster plating. Since high-temperature steps are involved in the laser doping and the ion migration process, there will be a thin oxide layer formed on the laser-doped region. A 1% HF solution was used to treat the front surface for 30 s to remove the oxide. The samples were then ready for electroplating. Figure 3-12 shows a schematic of the experimental setup. The sample was mounted onto a polytetrafluoroethylene (PTFE) rig with an opening and an O ring at the bottom and was secured by bolting a stainless-steel plate to the rig. An aluminium foil sheet was placed in between the sample and the stainless-steel plate to allow an electrical connection to the sample. Commercial NB SEMIPLATE NI 100 nickel sulfamate from NB Technologies was used as the electrolyte. A 99.98% pure, 0.5 mm diameter nickel wire was used as the anode. The rig was placed on a hot plate to heat the electrolyte to 48-52 °C. A white LED lamp (6 W) was used for illumination. A voltage of 1.1 V was applied between the nickel wire and the sample for 4 min to form nickel fingers on the laser-doped regions. Here nickel fingers were electroplated for front metallisation on proof-of-concept inversion layer cells for simplicity. Section 2.1.3 reviewed the previous literature showing that electroplated Ni/Cu/Ag contacts are a promising alternative for the industrial production of silicon solar cells [90], [91].

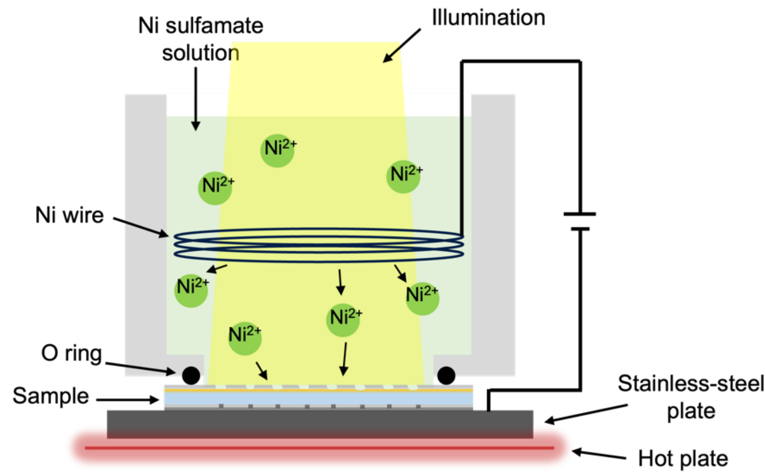

Figure 3-12 Schematic of light-assisted nickel electroplating.

3.8 Solar Cell Device Characterisation

Proof-of-concept inversion layer cells were fabricated in this thesis. The performance of the cells was monitored throughout the fabrication procedure using Suns-V_{OC}, light beam-induced current and current-voltage characteristics.

3.8.1 Suns-V_{OC} Measurements

A Suns-V_{OC} instrument has been widely used to characterise cells/cell precursors with a *pn* junction. This technique was used in this thesis to (i) confirm the formation of the field-induced emitter, and (ii) assess the material quality and passivation quality of precursor cells. A Sinton Suns-V_{OC} MX tester was used for these measurements. Figure 3-13 shows a schematic of the tester. The sample is placed on the stage, and the rear of the sample is contacted by a conductive metal plate on the stage. The front of the sample is contacted using a metal probe. During measurements, the sample is illuminated by a high-intensity flash. The light intensity decays gradually afterwards. The photovoltage generated by the *pn* junction is recorded at open-circuit conditions as a function of light intensity. The

characterisation is also known as illumination V_{OC}. With assumed Jsc, a pseudo IV curve can be calculated with no impact from the series resistance. The pseudo IV curve shows the highest potential performance of the material. The technique can therefore be used to assess the material quality and passivation quality after junction formation, allowing optimisation of each processing step afterwards. In this thesis, inversion layer cell precursors fabricated on Set B samples were characterised using this method. For the front side, the laser-doped n-type region was exposed and contacted by a spring-loaded tungsten or gold probe. For these measurements, Suns-V_{OC} at 1-sun illumination was recorded throughout the various processing steps.

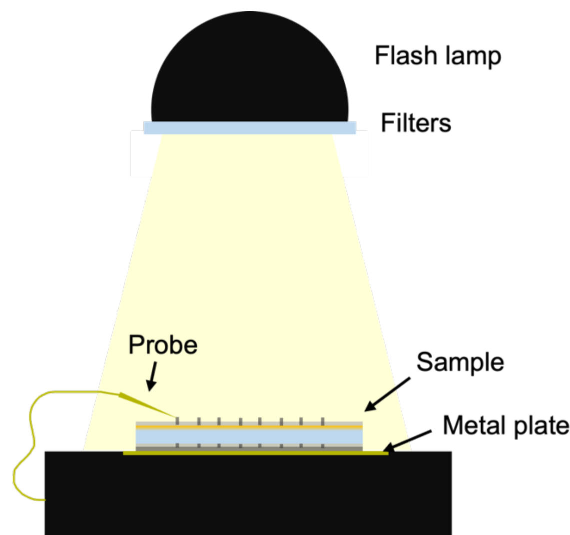

Figure 3-13 Schematic of a Sinton Suns-V_{OC} MX tester.

3.8.2 Light Beam-Induced Current

The light beam-induced current (LBIC) technique was used to confirm the formation and assess the uniformity of the field-induced emitter. This technique measures the photocurrent collected by the sample while a laser beam is scanned across the sample surface. Figure 3-14 shows a schematic of the experimental setup [128]. A 405 nm wavelength blue laser with sub-micron spot size was used as the localised light source. Further details of this setup can

be found in [128]. A map of the LBIC current was constructed after the scan. The contrast in the current signal comes from variations in the collection efficiency of the sample. This suggests that the map can be used to detect local structural defects with sub-micron resolution.

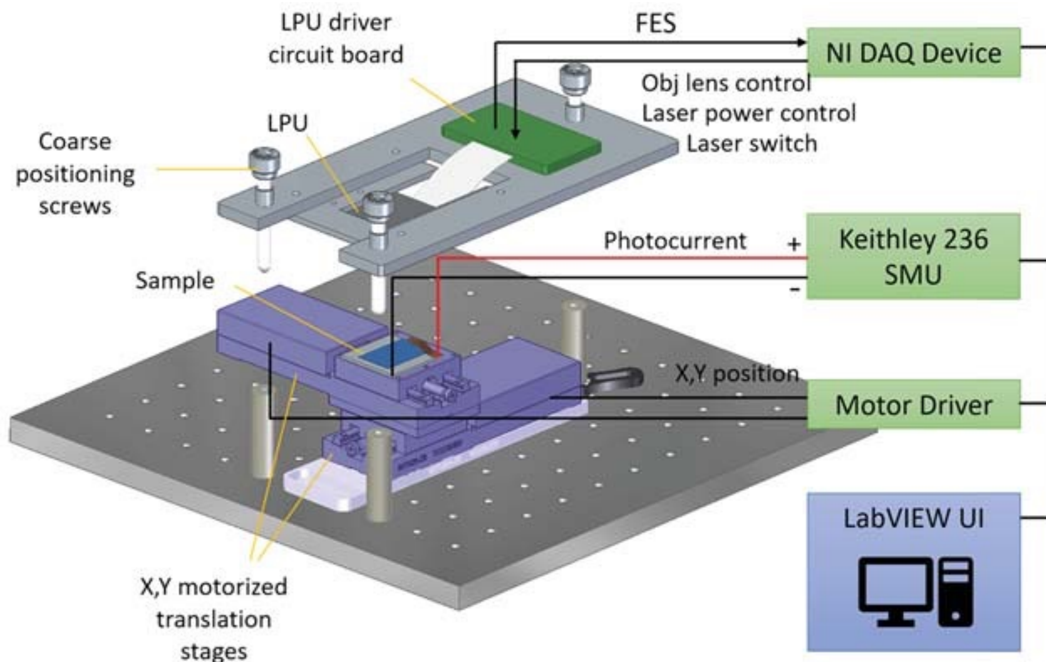

Figure 3-14 Schematic of the light beam-induced current measurement setup [128].

3.8.3 Current-Voltage Characteristics

The performance of the proof-of-concept inversion layer cells was evaluated by current-voltage (IV) characterisation. An LOT-QuantumDesign sun simulator was used to provide 1-sun illumination. The sun simulator comprises a high-pressure Xe arc lamp filtered to match the air mass 1.5 global (AM 1.5G) spectrum. The spectrum represents the distribution of sunlight's energy across different wavelengths as it passes through the Earth's atmosphere at an average air mass of 1.5 according to standard ASTM G-173 spectra [129]. A 1 × 1 cm^2 aperture was mounted on top of the cell to control the area under illumination. The sample was placed on an aluminium sheet to contact the rear metallisation. The front metallisation

was contacted using a spring-loaded gold probe. The IV curve was traced using a Keysight B2901A source measure unit.

3.9 Stability Tests

Ultraviolet (UV) irradiation is known to break bonds at the interface and result in an increase in interface defect state density [76]. At an elevated temperature, potential degradations such as loss of positive K^+ ions or degradations that would lead to an increase in interface state density are expected to occur at a higher rate and will hence have a higher possibility to be observed. In this thesis, the stability of sheet resistance of field-induced charge layers and V_{OC} of inversion layer precursor cells were tested against UV irradiation and an elevated temperature for two months.

3.9.1 UV Irradiance

An in-house UV exposure chamber was used for the stability test. Figure 3-15.a shows a schematic of the setup. Four Osram DULUX UVA lamps were implemented for UV irradiation, providing a total optical irradiance of ~5 $mWcm^{-2}$. The spectrum of the lamp is shown in Figure 3-15.b [130]. The chamber allows single-sided UV exposure. For the samples tested, the side with positive K^+ ions incorporated was exposed to UV irradiation. The samples were kept inside the UV chamber for two months except for periodic sheet resistance and Suns-V_{OC} measurements.

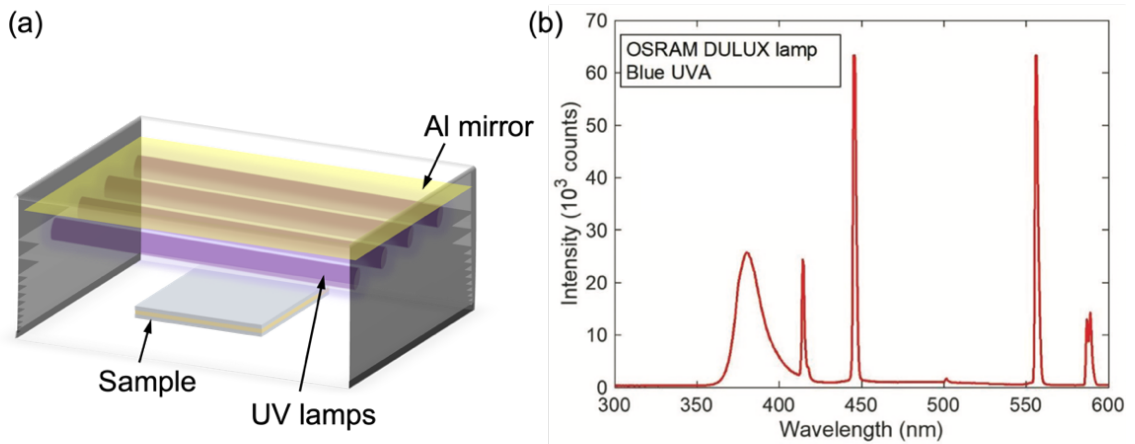

Figure 3-15 (a) Schematic of the experimental setup of an in-house UV exposure chamber. (b) Ultraviolet spectral irradiance [130].

3.9.2 Box Furnace

A Carbolite CSF 1200 box furnace was set to 120 °C for the stability test. The atmosphere in the chamber was not controlled. The samples were kept in the furnace chamber in the dark for two months and were only taken out for sheet resistance and Suns-V_{OC} measurements during the two-month period.

Chapter 4 Field-Induced Charge Layers

Chapters 1 and 2 showed that the performance of IL cells is limited by low emitter sheet conductance [73], [78]–[81]. The sheet conductance of a field-induced inversion layer is dependent on the charge density in the dielectric thin film. The optimal design of an IL cell, therefore, requires a high charge density to achieve high emitter sheet conductance. So far, only the intrinsic charge of dielectric thin films has been used to induce the inversion layer [72]–[77], with the highest charge density being 1.1×10^{13} cm^{-2} [77]. Dielectric materials that can provide higher charge densities are required to improve the emitter sheet conductance. This work approaches this hurdle by using an ion-charged oxide thin film, which allows the incorporation of controllable amounts of ionic charge and has demonstrated charge densities above 5×10^{12} cm^{-2} [83]. This chapter explores the potential of obtaining higher charge densities in ion-charged oxide thin films such that the limitation of current dielectrics can be overcome. The maximum sheet conductance in the field-induced inversion layer and pathways to achieve it are investigated.

4.1 Field-Induced Electron Accumulation Layer

A practical way of maximising the dielectric charge density is by incorporation of ionic charge. This work begins with the development of a method for introducing a high density of positive alkali ions into an oxide thin film, which in turn induces an electron-rich layer near the semiconductor surface. The Van der Pauw method was used to monitor the sheet resistance of field-induced layers in this thesis. However, the electron inversion layer cannot

be measured directly because the measurement requires direct contact with the inversion layer, and the formation of the inversion layer will be interrupted underneath the aluminium contacts. Figure 4-1.a shows a schematic of the sample structure for VdP measurements with an electron inversion layer formed on a p-type silicon substrate. No inversion layer is formed underneath the aluminium contacts due to the absence of ion-charged dielectric material. The p-type regions underneath the aluminium contacts form a *pn* junction with the n-type inversion layer. This will lead to nearly zero charge flowing through the inversion layer. So the inversion layer sheet resistance cannot be measured in this sample geometry, and local doping is necessary to ensure electrical contact with the inversion layer. Due to the experimental difficulty in measuring the sheet resistance of an inversion layer, in this section, an electron accumulation layer was induced on an n-type silicon substrate instead. Figure 4-1.b shows a VdP sample structure with an electron accumulation layer formed on an n-type substrate where it is evident that charge can flow from high to low n-type doped regions, allowing efficient measurements.

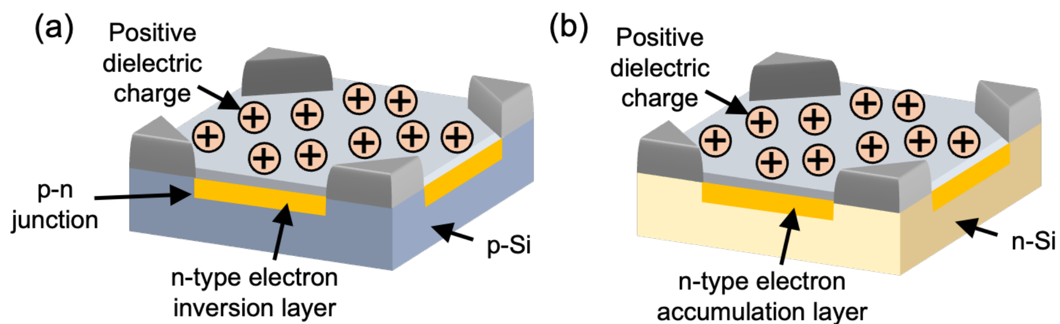

Figure 4-1 Schematic of a field-induced electron layer on (a) a p-type and (b) an n-type Van der Pauw sample structure.

An ion-injection method (Section 3.5) was used to incorporate positive K^+ ions into silicon oxide thin films on n-type A1 samples to induce electron accumulation layers. The sheet resistance of the electron accumulation layers was characterised to demonstrate the

capability of the ion injection method. The ion precursor was delivered to the sample surface by spin coating of a KCl solution of 10^{-3} mol/L, in a DI water:IPA 30:70 solvent (KCl concentration A), at 3000 rpm for 30 s. Corona ions were deposited on the dielectric surface by corona discharge at a voltage of 30 kV for 30 s to provide an electric field across the oxide thin film. The samples were then annealed at 430 °C for 10 s on a hotplate in the non-controlled laboratory atmosphere. The anneal provides the K^+ ions with sufficient kinetic energy to migrate through the oxide thin film, reach the Si/SiO_2 interface, and induce a mirror electron accumulation layer. Each deposition of corona ions followed by an anneal is considered one cycle of ion migration. Multiple corona discharge-anneal cycles were carried out to allow migration of most of the K^+ ions delivered to the dielectric surface. After that, the ion precursor was replenished by further KCl spin coating which was followed by additional corona discharge-anneal cycles to provide higher ionic charge density. The sheet resistance was recorded by VdP measurements after each corona discharge-anneal cycle. The KCl spin coating, followed by the subsequent corona discharge-anneal cycles, was repeated until the sheet resistance plateaued. Figure 4-2 shows the accumulation layer sheet resistance of two A1 samples. Each data point represents a measurement taken after a corona discharge-anneal cycle. Each change of colour represents a replenishment of the KCl ion precursor. The figures show a reduction of accumulation layer sheet resistance as more positive K^+ ions were introduced into the SiO_2 film and migrated to the interface. The lowest accumulation layer sheet resistance values of the two samples are 1.19 kΩ/sq and 1.12 kΩ/sq, respectively. However, these same samples were measured 30 days later and were found to have reduced to 0.99 kΩ/sq and 1.03 kΩ/sq. When measured after a short anneal (430 °C, 20 s) the resistance values were found to have further reduced to 0.95 kΩ/sq and 0.96 kΩ/sq. The lower sheet resistance measured 30 days after processing implies a higher density of

electrons in the accumulation layer than that produced immediately after processing. The density of the ionic charge embedded cannot be measured using regular characterisation methods like capacitance-voltage measurements. This is because the voltage required to reach the flat-band condition is out of range for the equipment available in the Oxford Materials laboratories. The charge density will instead be estimated in Section 4.5 with the help of simulations. These results demonstrate the effective formation of an electron accumulation layer from an ion-charged dielectric. The lowest accumulation layer sheet resistance obtained is 0.95 kΩ/sq, which is the lowest reported in the literature as can be seen when compared to data in Table 2-1 for previous works. This implies that the highest density of charge, ionic in this case, has been achieved inside the oxide thin film.

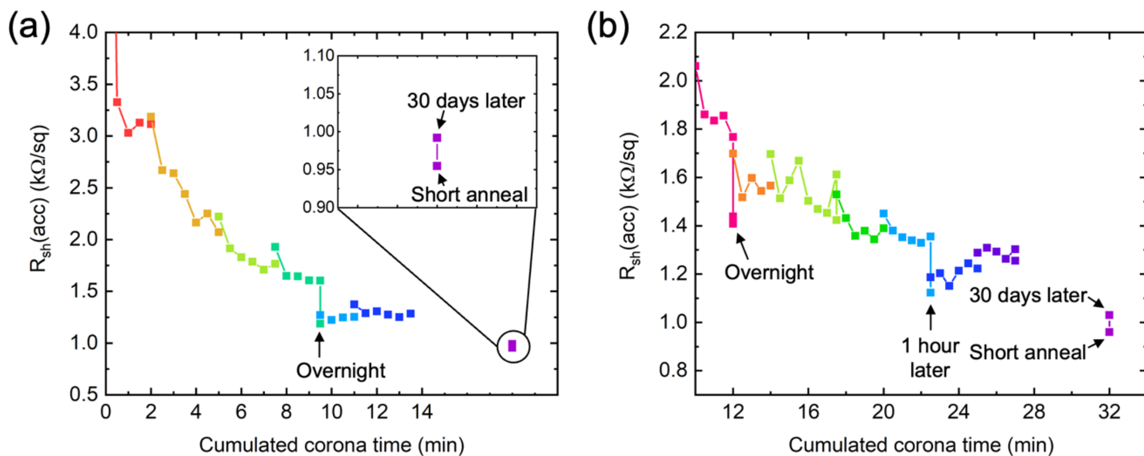

Figure 4-2 Recorded accumulation layer sheet resistance for two A1 samples (a), (b), where positive K^+ ions induce the electron accumulation layer by the supply of the ion precursor (KCl), electrostatic charging (30 kV, 30 s), and annealing (430 °C, 10 s). Each point was taken after a corona-anneal cycle, and each change of colour represents a replenishment of KCl.

It is noted in Figure 4-2 that abrupt increases in sheet resistance appear after replenishment of the KCl ion precursor and when the samples were kept in laboratory conditions for hours or 1 month. The sheet resistance measured immediately after each spin coating of the KCl

solution was found to be higher than the previously recorded one. This increase can be explained by the unintentional adsorption of negatively charged molecules at the sample surface during spin coating. The negative charge partially compensates for the positive ionic charge embedded in the dielectrics. The sheet resistance thus appears higher than that measured before the spin coating. The negative charge was driven off the sample surface during the following corona discharge-anneal cycles, leaving the net charge only originating from the positive K^+ ions inside the oxide thin film. Another aspect worth noticing is the unexpected reduction in sheet resistance observed 30 days after processing, with even lower values recorded after a short anneal (430 °C, 20 s). A hypothesis is that a change in charge distribution near the Si/SiO_2 interface took place. Figure 4-3 shows a schematic of the carrier distribution hypothesised. Apart from the positive K^+ ions, the corona ions deposited on the dielectric surface will lead to more electrons accumulated near the interface and thus a stronger band bending. The subsequent anneal provides the electrons with extra energy so that they can overcome a potential barrier and be trapped at the interface or inside the oxide thin film. This is often referred to as hot electron injection [131]. These electrons will partially compensate for the positive K^+ ionic charge and lead to an increase in accumulation layer sheet resistance. These electrons will decay to ground states gradually afterwards and bring the net charge concentration back up, and thus the sheet resistance down. The reduction in sheet resistance observed at the points labelled 'overnight' and '1 hour later' in Figure 4-2 can be explained by the same effect. Since the specimens were kept in a non-controlled laboratory atmosphere, the further reduction in accumulation layer sheet resistance after a short anneal can be explained by the drive-off of negative molecules adsorbed on the dielectric surface. These results suggest that the carrier distribution near the interface is of great importance for the final carrier density in the accumulation layer and

hence its sheet resistance. The effect of the adsorption of charged molecules at the surface and hot carrier injection needs to be considered while taking sheet resistance measurements.

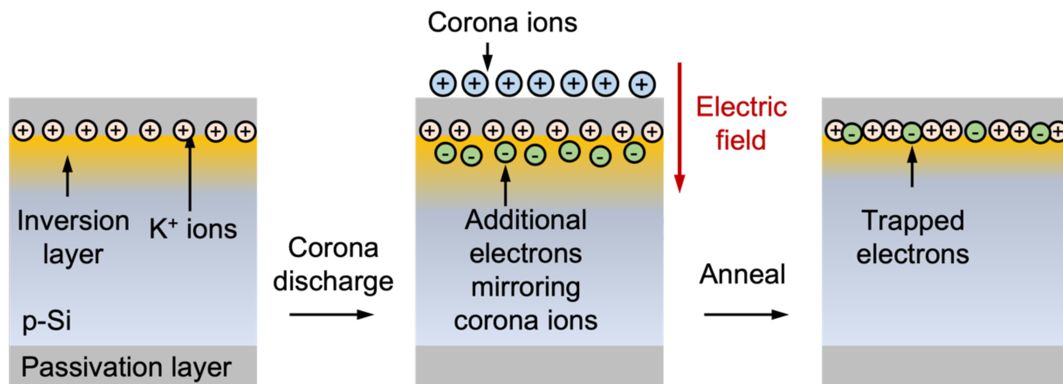

Figure 4-3 Schematic of possible carrier distribution near the interface upon corona discharge and annealing.

In this section, the ion migration method was used to incorporate a high density of positive K^+ ions into the oxide thin film and induce an electron accumulation layer on an n-type silicon substrate. An accumulation layer sheet resistance as low as 950 Ω/sq was obtained, which is the lowest reported in the literature, suggesting a high charge density in the ion-charged dielectric. It was observed that the adsorption of charged molecules at the surface and the effect of hot carrier injection will impact carrier distribution near the interface and hence the measured accumulation layer sheet resistance. The adsorbed molecules were driven off by annealing. The impact of hot carriers was minimised by taking the measurement after most of the injected carriers have decayed back to the ground states.

4.2 Simulation and Understanding of Field-Induced Charge Layers

A low emitter sheet resistance is required for the best operation in IL cells. While a low accumulation layer sheet resistance of 950 Ω/sq was obtained in Section 4.1, it is still

significantly higher than that of typical mainstream P-diffused emitters (120-150 Ω/sq). In this section, a numerical model was developed and used to explore the lowest IL sheet resistance possible and the pathways to achieve it.

4.2.1 Model Development

A finite element model was developed in Sentaurus TCAD [132]. The model reflects the characteristics of A1 samples. The model comprises a 200 µm thick, 1 Ω·cm p-type Si substrate, with a symmetrical oxide passivating layer on both sides. The dielectric fixed charge was defined at the front Si/SiO_2 interface. Figure 4-4.a shows a schematic of the model. The interface was defined following the parametrisation reported in [133], with interface state densities at mid-gap and band tails as primary parameters. These parameters will be defined in Section 4.2.1.1. More information on the presence and nature of interface states is included in Section 1.3.2.3. The carrier mobility is affected by phonon scattering, impurity scattering, carrier-carrier scattering, surface scattering and Coulomb scattering [134]. The mobility hence varies with factors such as dopant concentration and distance from the interface. Choosing an appropriate mobility model is critical to develop a model that correctly represents the experimental data and that remains physically possible. The Lombardi model [135], [136] was used for charge carrier mobility throughout the sample bulk and in the space charge layer. The choice of the mobility model will be covered in Section 4.2.1.3. A modified local-density approximation (MLDA) quantum-mechanical model was used to account for the confined carrier distributions occurring near semiconductor-insulator interfaces [137]. Since the interface states are able to trap field-induced carriers [14], their impact on carrier density in the field-induced charge layer needs to be considered. This has not been considered in most work in the literature. Figure 4-4.b shows a band diagram of a p-type silicon substrate near the interface. As illustrated in the

figure, in the presence of positive charge, the electric field will lead to the accumulation of electrons near the interface, so that the bands bend downwards and the Fermi level (E_F) appears close to the conduction band edge at the interface. This leads to most acceptor-like interface states below the Fermi energy being occupied by trapped immobile electrons. These immobile electrons will compensate for the positive dielectric charge, resulting in a lower electron density being induced in the inversion layer. The carrier density in the inversion layer is thus determined by both the dielectric charge density and the density of interface states that can accommodate immobile electrons. To develop a model for a better understanding of the formation of an inversion layer, it is necessary to calibrate the interface states in the model.

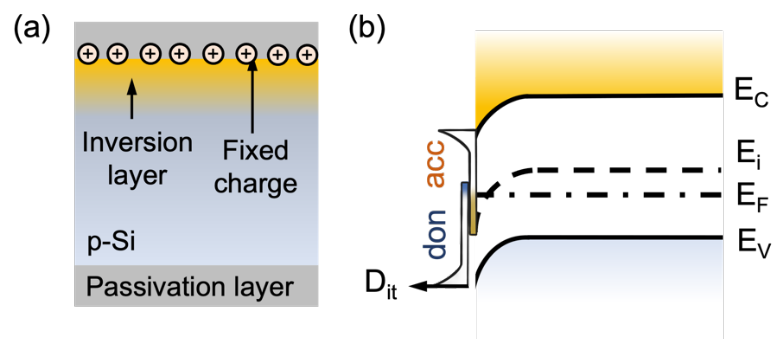

Figure 4-4 (a) Schematic of the model developed in Sentaurus TCAD. (b) Band diagram of a p-type Si substrate near Si/SiO_2 interface in the presence of positive surface charge.

In the following, the interface parameters used to describe the interface states will be introduced and defined. After that, the interface parameters were adjusted to calibrate the model with experimental data. The model was then ready for investigation of the formation of field-induced charge layers. Lastly, field-induced layers were simulated using different carrier mobility models to demonstrate the importance of the choice of the mobility model.

4.2.1.1 Interface Parameters

Interface parameters that are used to describe the interface states within the bandgap are as follows. The interface state density (D_{it}) profile was defined by a superposition of three components. Figure 4-5 shows a profile of the three components. The first is a constant $D_{it—midgap}$ defined across the bandgap to represent the energy states introduced by silicon dangling bonds at the interface. The interface states above E_i were defined as acceptor-like and those below E_i were defined as donor-like. The presence of both acceptor- and donor-like states is due to the amphoteric nature of dangling bonds [138]. The distribution and energy level of these states are different for different types of dangling bonds on (111) and (100) surfaces [138], [20]. In this work, the density of these interface states is assumed constant near the middle of the bandgap, and thus, in average, the transition from acceptor- to donor-like states is set to occur at E_i. For the interface states near the band tails, the density of acceptor/donor-like states increases exponentially towards the conduction/valence band edge [27], [33]–[39]. The band-tail interface state density is described by the following equations:

$$D_{it-acc}(E) = D_{it-CB} \times e^{-\frac{(E_g - E)}{E_{0,CB}}} \quad \text{Eq (4-1)}$$

$$D_{it-don}(E) = D_{it-VB} \times e^{-\frac{E}{E_{0,VB}}} \quad \text{Eq (4-2)}$$

where D_{it-acc} and D_{it-don} represent the density of acceptor- and donor-like interface states across the bandgap. D_{it-CB} and D_{it-VB} are the maximum interface state densities at the conduction and valence band edge. E_g is the bandgap of crystalline Si (1.12 eV). E is the energy from the valence band edge in eV. $E_{0,CB}$ and $E_{0,VB}$ determine the slope of D_{it} near the conduction and valence band edge. Here $E_{0,CB}$ and $E_{0,VB}$ were set to 0.028 eV and 0.024 eV, respectively, to reflect average values extracted from experimental and simulated

results in previous work [27], [33], [36]. The D_{it} profile across the bandgap can then be described using three key parameters: $D_{it\text{-}midgap}$, $D_{it\text{-}CB}$ and $D_{it\text{-}VB}$.

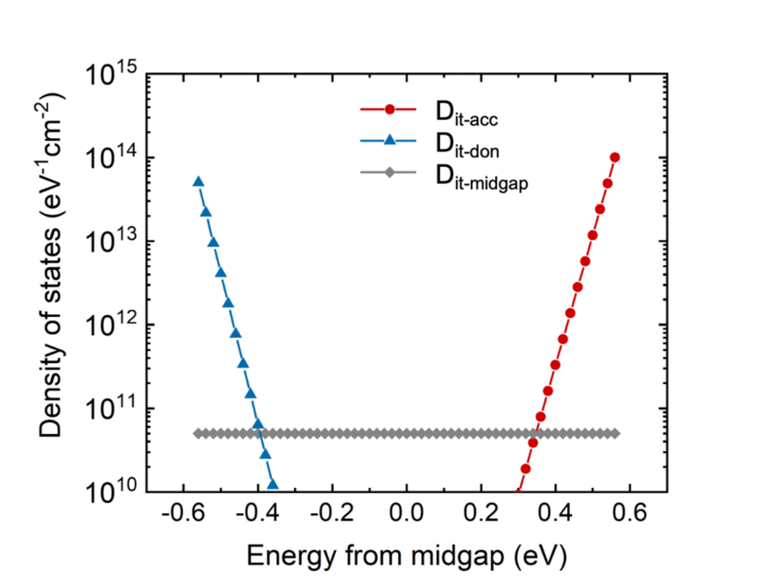

Figure 4-5 Profiles of interface state density in three components across the bandgap with $D_{it\text{-}midgap}$ set to 5×10^{10} $eV^{-1}cm^{-2}$, $D_{it\text{-}CB}$ set to 10^{14} $eV^{-1}cm^{-2}$ and $D_{it\text{-}VB}$ set to 5×10^{13} $eV^{-1}cm^{-2}$.

4.2.1.2 Calibration of Interface Parameters

The sheet resistance of field-induced charge layers is determined by both the dielectric charge density and the density of interface states. Since the sheet resistance can be simulated and is measurable experimentally, its response to charge density was used as a metric to calibrate the interface parameters. To extract the sheet resistance from simulations, the equilibrium state was simulated and the carrier density and mobility in bulk silicon were extracted as a function of distance from the Si/SiO_2 interface. As an example, Figure 4-6 shows profiles of the extracted carrier density and mobility inside an n-type Si substrate when a positive charge density of 9×10^{12} cm^{-2} was defined at the Si/SiO_2 interface. The product of the carrier density and mobility was integrated over the entire sample thickness to calculate the sheet resistance as follows:

$$R_{sh} = \frac{1}{\int_0^{thickness} \left(nq\mu_n + pq\mu_p\right) dt} \qquad \text{Eq (4-3)}$$

where n and p are electron and hole densities, μ_n and μ_p are electron and hole mobilities, and q is the elementary charge. The accumulation layer sheet resistance was calculated using the approximation introduced in Section 3.6.3.1, which requires an additional simulation with no dielectric charge specified. To obtain the response of sheet resistance to charge density experimentally, corona ions were deposited on the dielectric surface of A1 samples, while the VdP method was used to record the sheet resistance. The corona charge density was monitored using KP. The experimental data are plotted in symbols in Figure 4-7. The corona charge density is up to 8×10^{12} cm^{-2}, which approaches the practical limit of gate breakdown field in most thin film materials [139], [140]. For the interface parameters in the model, $D_{it\text{-}midgap}$ was set to 5×10^{10} eV^{-1}cm^{-2}, $D_{it\text{-}CB}$ and $D_{it\text{-}VB}$ were set to 10^{14} and 5×10^{13} eV^{-1}cm^{-2}, respectively. The choice of these values will be justified in Chapter 5. Figure 4-7 shows the simulated response of wafer sheet resistance (Figure 4-7.a) and accumulation layer sheet resistance (Figure 4-7.b) to surface charge density in dashed lines. The simulated curves show good agreement with the experimental data. This indicates that the model can represent the real specimen in terms of carrier density and mobility for charge densities up to 8×10^{12} cm^{-2}.

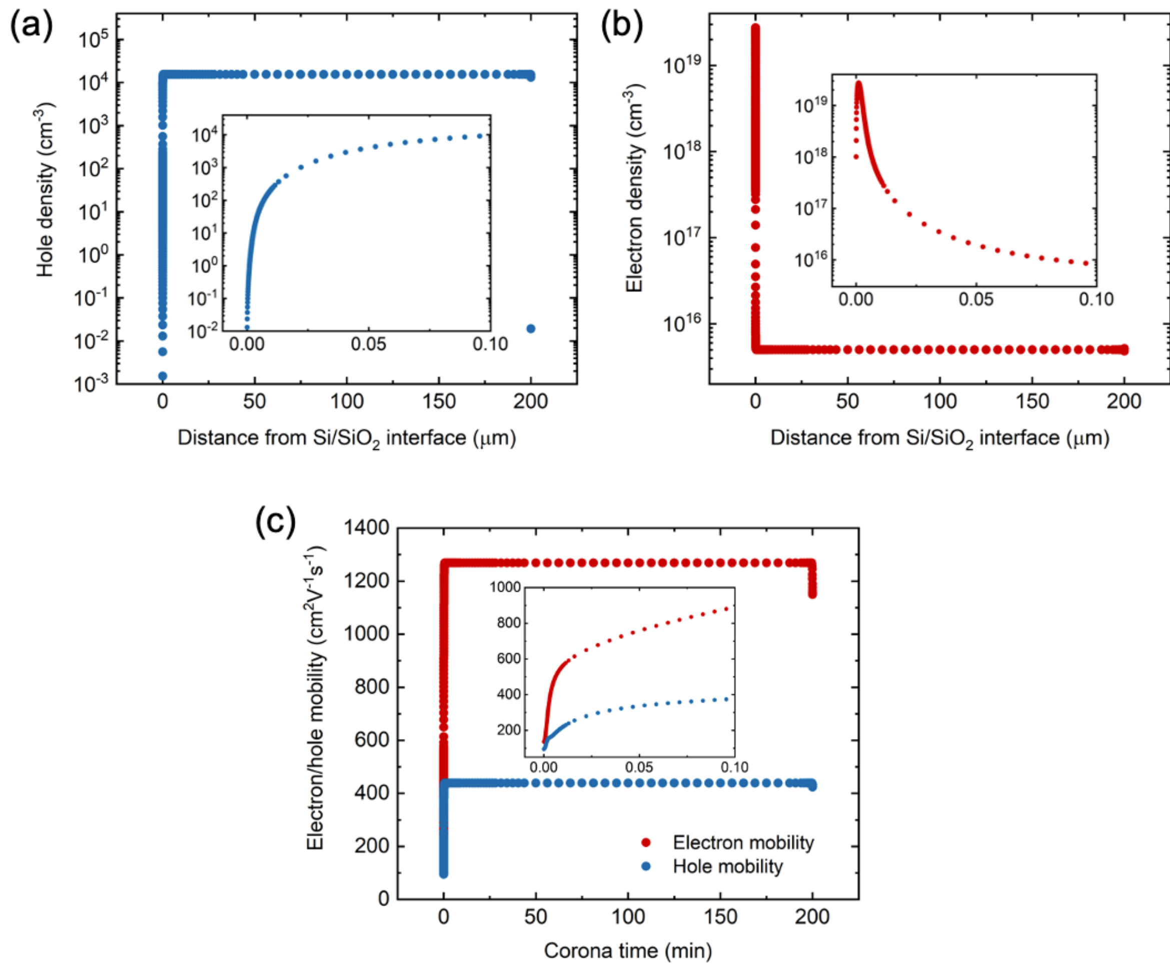

Figure 4-6 Simulated (a) hole density, (b) electron density, and (c) carrier mobilities extracted from a 1 Ω·cm, n-type Si model with a positive charge density of 9×10^{12} cm^{-2} defined at the front Si/SiO_2 interface.

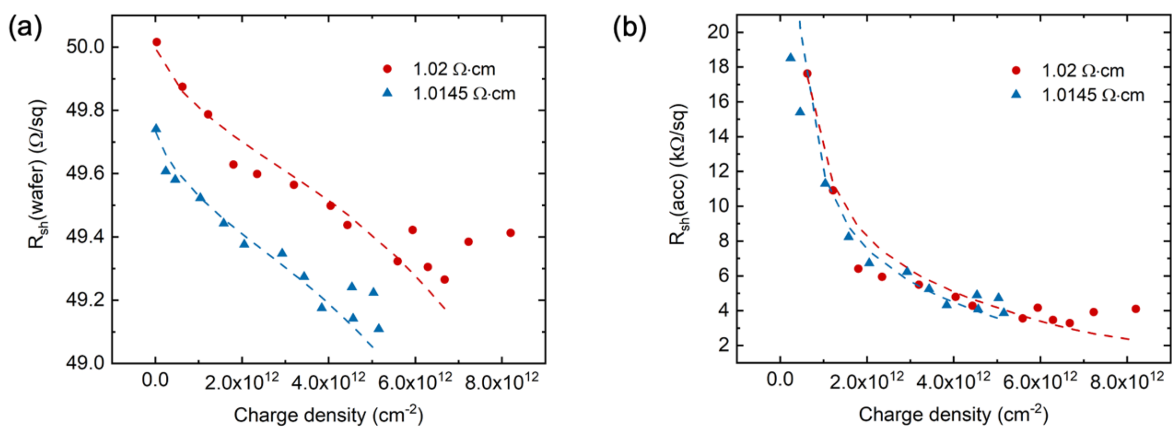

Figure 4-7 Simulated (dashed lines) and experimental (symbols) response of (a) wafer sheet resistance and (b) accumulation layer sheet resistance from a 1 Ω·cm, n-type Si model to surface charge density.

To test the reliability of the model for charge densities above 8×10^{12} cm^{-2}, positive K^+ ions were introduced into the oxide thin film of A2 samples. This was done by 4 repeated spin coatings of the KCl solution (concentration B: 5×10^{-3} mol/L, 3000 rpm, 30 s) with each followed by 8 corona discharge (30 kV, 30 s)-anneal (430 °C, 10 s) cycles. The ionic charge density after one spin coating of the KCl solution and the subsequent corona discharge-anneal cycles was characterised using the method introduced in Section 3.6.4.2. The lifetime was recorded as a function of surface potential. The resulting ionic charge density is 9.6×10^{12} cm^{-2}. The results will be elaborated in detail in Section 4.3. It was assumed here that the repetition of the ion migration process leads to an equivalent increase in charge density with each iteration. Figure 4-8 shows the wafer sheet conductance recorded after multiple ion migration procedures. Data points in different colours represent sheet conductance measured from a group of identical samples. It is noted that the wafer sheet conductance scatters by ~5% across samples. This may result from that the samples were cut from different wafers. The dashed line is the simulated sheet conductance as a function of charge density up to 4×10^{13} cm^{-2}. The simulated curve agrees well with the experimental data, indicating that the model is reliable for charge densities up to 4×10^{13} cm^{-2}. It is noted that repeating the spin coating by 4 times may not result in 4 times the charge density achieved by one single spin coating. This is because the positive charge at the interface may counteract the electric field in the dielectric. However, in Figure 4-8, the increase in sheet conductance is minor when more than 2 spin coatings were carried out. This suggests that the quality of the fit may persist even if the precision of the assumption is compromised for the points taken after 2/3/4 spin coatings. The parameters used in the simulations are summarised in Table 4-1. Since the model was calibrated to the experimental data for charge densities up

to 4 × 10^{13} cm^{-2}, it was then ready to be used to investigate the properties of field-induced charge layers.

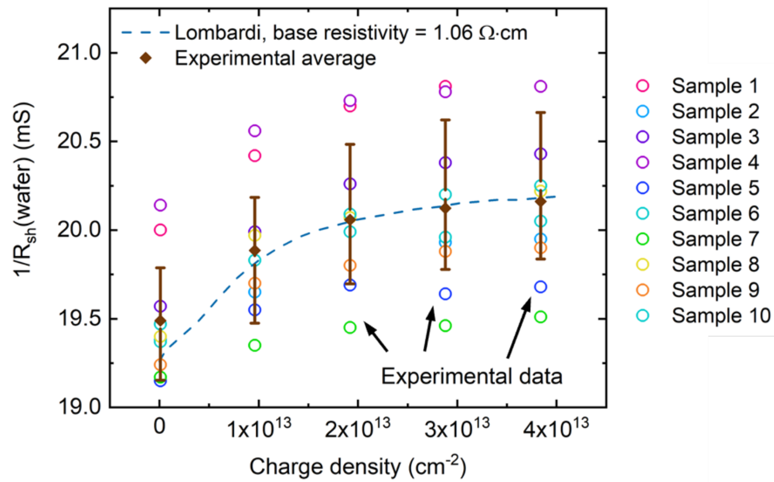

Figure 4-8 Wafer sheet conductance of an A2 sample with positive K^+ ions embedded in the oxide layer on one side after the 1st, 2nd, 3rd, and 4th spin coating of the KCl ion precursor.

Table 4-1 Summary of parameters used for simulation of field-induced layers in Sentaurus TCAD.

Parameter	Value
Wafer thickness	200 μm
Bulk base resistivity	n-type, ~1 Ωcm
SRH bulk lifetime	τ_n = 0.371 ms, τ_p = 3.71 ms
Dielectric charge density	0-4 × 10^{13} cm^{-2}
$D_{it\text{-}midgap}$	5 × 10^{10} $eV^{-1}cm^{-2}$
$D_{it\text{-}CB}$	10^{14} $eV^{-1}cm^{-2}$
$D_{it\text{-}VB}$	5 × 10^{13} $eV^{-1}cm^{-2}$

4.2.1.3 Mobility Model

The model developed above shows good agreement with experimental data. The Lombardi mobility model [135], [136] was used in the model to describe the carrier mobility inside field-induced layers. Here, simulations using different mobility models were compared to point out the importance of the choice of a good mobility model. Figure 4-9 illustrates the simulated carrier mobility profiles in bulk Si with the charge density set to 10^{13} cm^{-2} at the

Si/SiO_2 interface using different mobility models. Klaassen's mobility model (PhuMob) considers the impact of phonon scattering, impurity scattering, and carrier-carrier scattering [141]. Based on Klaassen's model, IALMob model [135], [142] and the Lombardi model [135], [136] include the effect of acoustic surface phonons and surface roughness. However, these two models predict a significant difference in carrier mobility near the interface. The last model shown in the figure includes the effect of Coulomb scattering by interface charge, referred to as the interface charge model here. For the interface charge model, the mobilities reduce to nearly 0 within 0.025 μm from the interface. In my attempt of calibrating the interface parameters as described in Section 4.2.1.2, no fit was obtained for the IALMob and the interface charge model. IALMob has been mainly tested in MOSFETs that use base dopant densities of the order of > 10^{16} cm^{-3} [135], [142], while a typical dopant density in this work is below 5×10^{15} cm^{-3}. The interface charge model appears to underestimate the mobility near the interface and leads to unrealistic sheet resistance-charge density curves. Lombardi's model is the only model explored in this work that can explain the experimental data for charge densities up to 4×10^{13} cm^{-2}. Therefore, the Lombardi model was used in all simulations in this thesis.

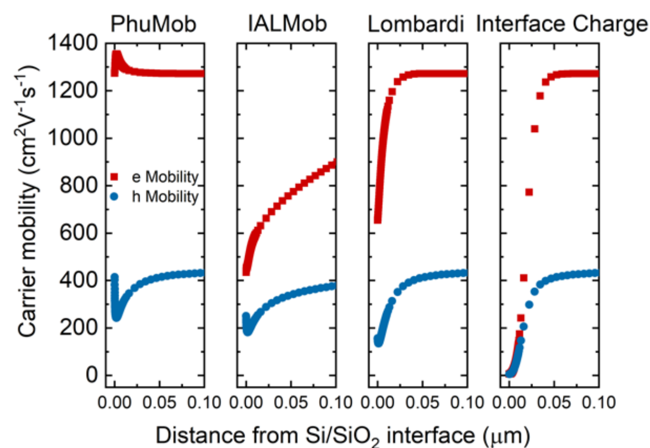

Figure 4-9 Simulated carrier mobility profiles near the Si/SiO_2 interface using various mobility models.

4.2.2 Field-Induced Inversion Layers by Simulation

In this subsection, the model developed above is used to study the formation of a field-induced inversion layer and factors that may affect its sheet resistance. An inversion layer is formed by applying positive charge on the surface dielectric so that mirrored electrons accumulate near the surface and invert the p-type base into an n-type layer. The inversion layer sheet resistance is determined by both the dielectric charge density and the interface state density. In the following, the impact of charge density and interface state density on the inversion layer will be studied. The lowest sheet resistance possible and the requirements to achieve that will be investigated. Since the p-type region will be depleted before being inverted into n-type, the initial carrier density and therefore the substrate resistivity may affect the final carrier density in the inversion layer. The significance of this effect will also be evaluated. Lastly, illumination will introduce photo-generated carriers in the emitter. The extent of the increase in emitter sheet conductance upon illumination will be investigated.

4.2.2.1 The Effect of Charge Density

The inversion layer was simulated with varied charge densities defined at the Si/SiO_2 interface. In the model, $D_{it\text{-}midgap}$, $D_{it\text{-}CB}$, and $D_{it\text{-}VB}$ were set to 5×10^{10}, 10^{14} and 5×10^{13} $eV^{-1}cm^{-2}$, respectively. The thickness of an inversion layer was defined as the distance from the Si/SiO_2 interface at which the hole density exceeds the electron density. The inversion layer sheet resistance was calculated using Eq (4-3), where the thickness is that of the inversion layer. Figure 4-10.a shows the simulated inversion layer sheet resistance and its reciprocal, sheet conductance, as a function of charge density. It is shown that the inversion layer sheet conductance increases with charge density and plateaus at charge densities above 2×10^{13} cm^{-2}. The minimum inversion layer sheet resistance shown is 1.1-1.2 kΩ/sq on 1 Ω·cm p-type Si substrates. Since sheet conductance is dependent on both carrier mobility and

carrier density, the plateau can be attributed to two factors. The first is that at high charge densities, the Fermi level at the interface will reach the band-tail near the conduction band edge. This may lead to most electrons induced by the dielectric charge above the density of 2×10^{13} cm^{-2} being trapped at the interface, and thus Fermi level pinning [116]. These electrons are immobile and will not contribute to the conductivity, resulting in a reduced slope in the sheet conductance curve at high charge densities. The other factor is the increased surface scattering and thus reduced carrier mobility with increased charge density. In an n-type inversion layer, the majority carriers are electrons, which dominate the sheet conductance. Figure 4-10 shows profiles of electron density, electron mobility and the product of electron density and electron mobility near the interface with varied charge densities. In Figure 4-10.b it is observed that electron density increases with an increased charge density. Figure 4-10.c shows that electron mobility decreases significantly with an increased charge density within 4 nm of the surface. The product of electron density and electron mobility is plotted in Figure 4-10.d. The simulation results demonstrate that the inversion layer sheet conductance at high charge densities is mostly limited by the reduced carrier mobility due to increased surface scattering. The lowest inversion layer sheet resistance achievable is ~1.1 kΩ/sq. The extent of the impact of interface states will be investigated next.

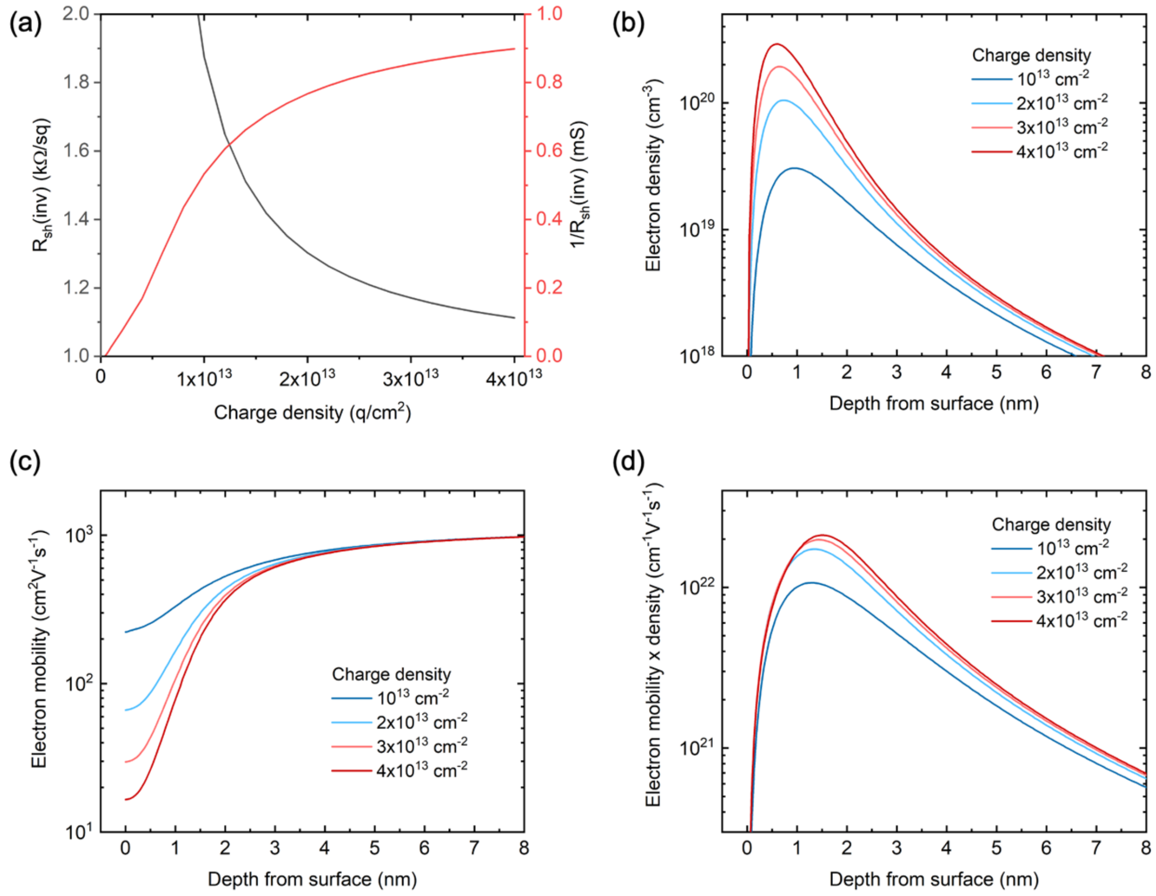

Figure 4-10 (a) Simulated inversion layer sheet resistance (left axis) and sheet conductance (right axis) on a 1 Ω·cm p-type Si substrate as a function of positive charge density. (b) Electron density, (c) electron mobility, and (d) electron density × mobility profiles near the interface on a 1 Ω·cm, p-type Si substrate in the presence of varied positive charge densities.

4.2.2.2 Interface Defect State Density

Interface states can trap field-induced charge carriers and may therefore affect the inversion layer sheet resistance. The interface parameters in the simulations above were calibrated to A1 samples and may vary for different silicon/dielectric interfaces. For mid-gap interface states, $D_{it\text{-}midgap}$ is below 10^{12} $eV^{-1}cm^{-2}$ for most passivated interfaces [14], [143]. Compared with the dielectric charge density discussed in this work, mid-gap interface states provide few sites to trap field-induced electrons. Their impact on the inversion layer is thus neglected. $D_{it\text{-}CB}$ is commonly orders of magnitudes higher than $D_{it\text{-}midgap}$ [27], [33]–[39]. The impact of $D_{it\text{-}CB}$ is therefore of most interest and was investigated in this section. Figure 4-11.a

shows the inversion layer sheet conductance as a function of charge density with varied D_{it-CB}. A significant increase in sheet conductance can be observed by reducing D_{it-CB} from 10^{15} to 10^{14}, and further to 10^{13} $eV^{-1}cm^{-2}$. The trend is more evident in Figure 4-11.b, which shows the sheet conductance as a function of D_{it-CB} with varied charge densities. These results indicate that passivating the band-tail interface states is effective in improving the inversion layer sheet conductance. However, the sheet conductance plateaus for D_{it-CB} below 10^{14} $eV^{-1}cm^{-2}$. This is because the number of electrons trapped at acceptor interface states for D_{it-CB} below 10^{14} $eV^{-1}cm^{-2}$ is small compared with the density of the field-induced electrons in the conduction band. These results demonstrate the extent to which passivating the band-tail interface states is necessary to obtain high inversion layer sheet conductance.

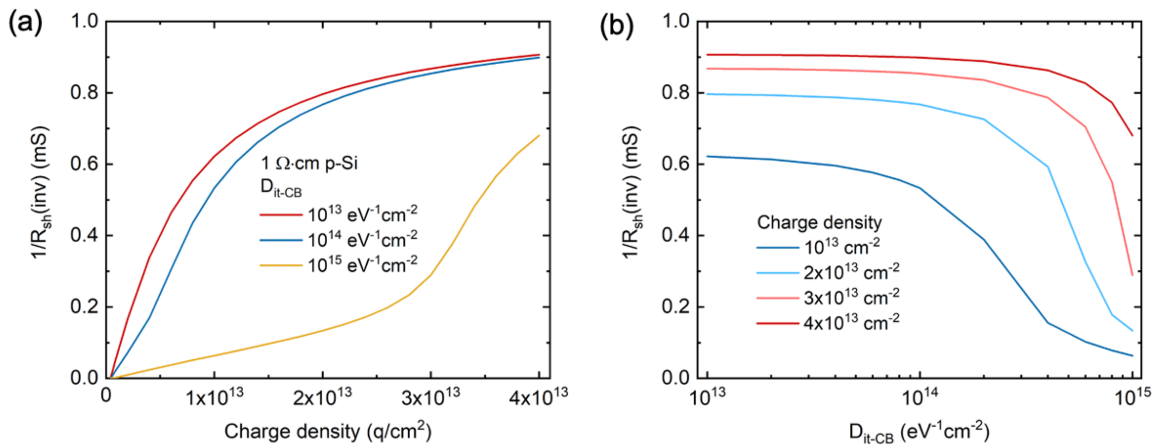

Figure 4-11 (a) Calculated inversion layer sheet conductance on a p-type Si substrate as a function of interface charge density with varied D_{it-CB}. (b) Calculated inversion layer sheet conductance on a p-type Si substrate as a function of D_{it-CB} with varied interface charge densities.

4.2.2.3 Substrate Resistivity

The impact of base resistivity on an inversion layer was investigated here. Figure 4-12 shows the simulated inversion layer sheet conductance as a function of charge density with varied D_{it-CB} values and base resistivities. Except for D_{it-CB} of 10^{15} $eV^{-1}cm^{-2}$, the sheet conductance at different base resistivities converges at charge densities above 10^{13} cm^{-2}. These results

suggest that the substrate resistivity has a minor effect on inversion layers provided well-passivated surfaces and high charge densities.

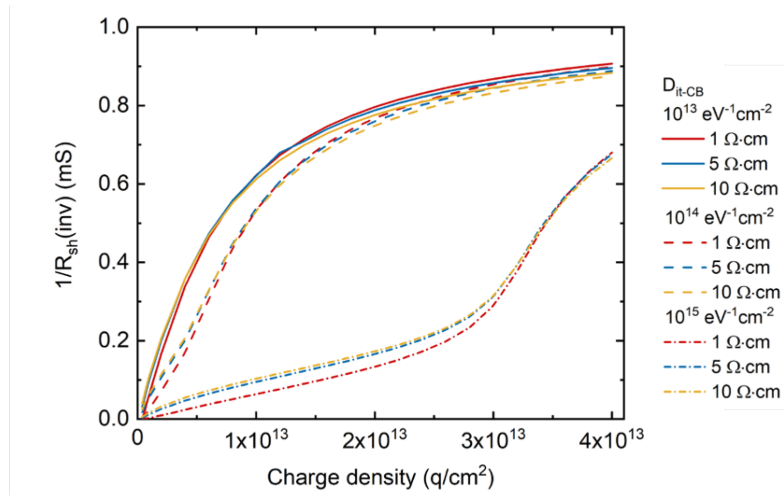

Figure 4-12 Calculated inversion layer sheet conductance on a p-type Si substrate as a function of interface charge density with varied $D_{it\text{-}CB}$ and base resistivities.

4.2.2.4 Illumination

Photo-generated carriers under illumination will lead to an increase in carrier density and thus an increase in emitter sheet conductance. The lowest inversion layer sheet resistance achievable in the dark (~1.1 kΩ/sq) is about 7 times higher than that of typical P-diffused emitters (150 Ω/sq) [10]. The inversion layer sheet resistance should therefore see a more significant increase upon illumination than that of P-diffused emitters. The impact of illumination on a field-induced emitter and a P-diffused emitter are compared here.

Thermal equilibrium of a field-induced emitter and a P-diffused emitter with no illumination was simulated on 1 Ω·cm, p-type Si substrates. In the models developed for both emitters, $D_{it\text{-}midgap}$ was set to 5×10^{10} eV^{-1}cm^{-2}, $D_{it\text{-}CB}$ and $D_{it\text{-}VB}$ were set to 10^{14} and 5×10^{13} eV^{-1}cm^{-2}, respectively. For the P-diffused emitter, a charge density of 10^{12} cm^{-2} was defined at the Si/SiO_2 interface, which is the typical charge density of a SiN_x layer used for solar cell passivation [144]. An active phosphorus doping profile measured from a P-diffused emitter

of a commercial PERC cell was used in the model [58]. Figure 4-13.a shows the doping profile. Figure 4-13.b-d show the electron density, electron mobility, electron density × electron mobility profiles of the P-diffused emitter and those of the field-induced emitter with varied charge densities. For field-induced emitters, it is observed that electron density drops rapidly with distance from the interface. For the P-diffused emitter, electron density depends on the doping profile and is kept above 10^{20} cm^{-3} for a significantly deeper region (> 8 nm). It is also noted that electron mobility in the P-diffused emitter is evidently lower than that in field-induced emitters. As a result, compared with field-induced emitters, the P-diffused emitter is thicker and more conductive in the dark.

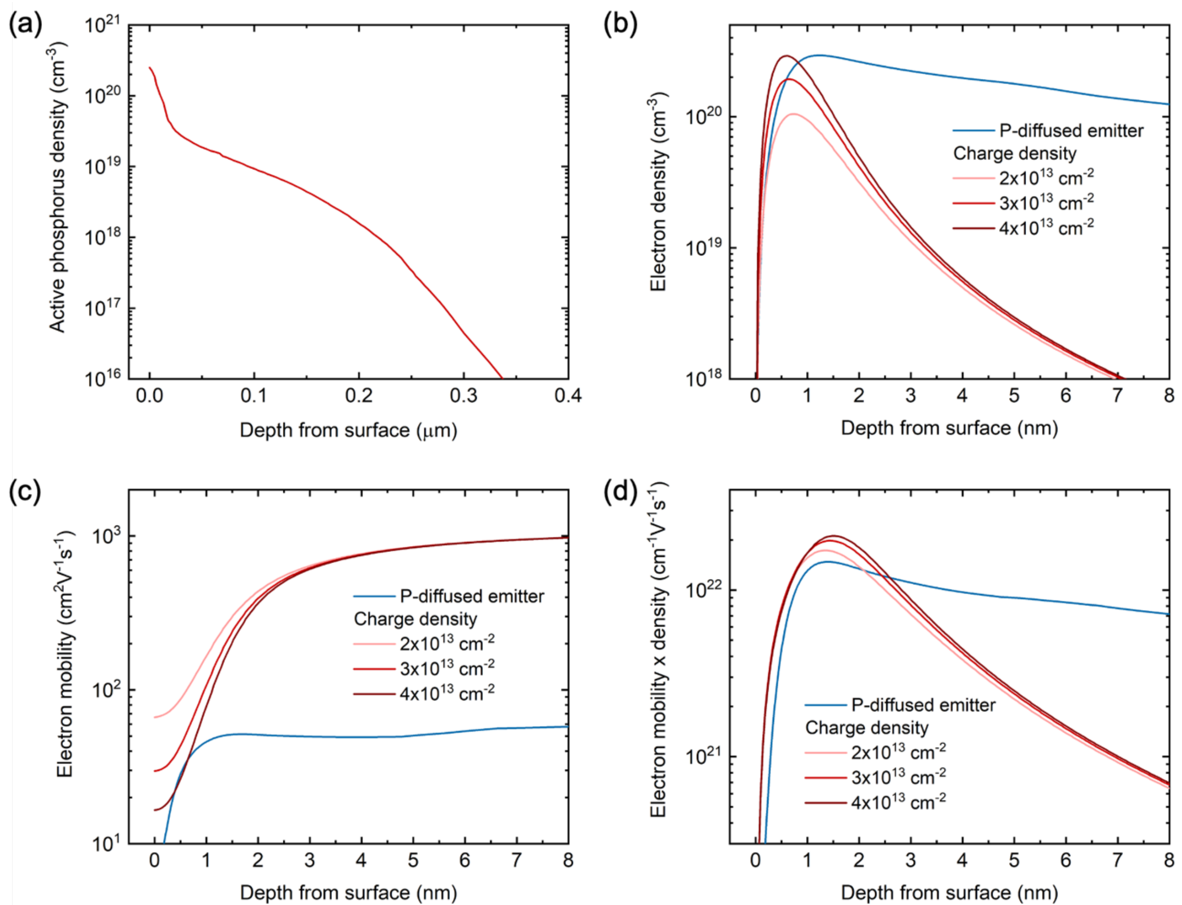

Figure 4-13 (a) Active phosphorus doping profile in a typical P-diffused emitter [58]. (b) Electron density, (c) electron mobility, and (d) electron density × mobility profiles of a field-induced inversion layer with varied charge densities and a P-diffused emitter on a 1 Ω·cm, p-type Si substrate in the dark.

A generation profile was used to simulate the distribution of photo-generated carriers under illumination. The generation profile was obtained from ray tracing using Sunrays and altered to mimic a pyramid-textured surface with 0.1 μm height under 1-sun illumination [145]. Figure 4-14 shows the generation profile. Figure 4-15 shows the carrier density profiles of a field-induced emitter with the charge density set to 2×10^{13} cm^{-2} and that of the P-diffused emitter in the dark and under illumination. Under illumination, both the majority and the minority carrier densities increase, leading to an increase in local conductivity. It is also noted that the depth of the *pn* junction is altered upon light injection. For the P-diffused emitter, the junction shifts from 375 nm to 340 nm from the interface, corresponding to a 10% reduction in thickness. For the field-induced emitter, the junction shifts from 100 nm to 60 nm from the interface, presenting a 40% reduction in thickness. As a result of the increased carrier density and reduced emitter thickness collectively, the sheet resistance of the P-diffused emitter drops from 196.6 to 195.1 Ω/sq upon illumination, corresponding to a 0.8% increase in sheet conductance. While for the field-induced emitter, the sheet resistance drops from 1.30 to 1.21 kΩ/sq, corresponding to a 7.4% increase in sheet conductance. These results show a more significant change in sheet conductance for the more resistive field-induced emitter. Additionally, the field-induced emitter is thinner than the P-diffused emitter, which means that the region with a high carrier density is smaller. It is noted from Figure 4-13 that for the P-diffused emitter, the doping concentration remains above 10^{18} cm^{-3} until a depth of 200 nm, while for the field-induced emitter, the electron density falls below the same value within a depth of 10 nm (Figure 4-15). These indicate overall lower Auger recombination in field-induced emitters compared with P-diffused emitters.

In summary, compared with P-diffused emitters, field-induced emitters appear to be thinner, more resistive, more sensitive to light injection, and may result in less Auger recombination. An increase in inversion layer sheet conductance by 7.4% upon illumination means lower resistive losses in an IL cell. It is noted that in these simulations a high charge density of 2 × 10^{13} cm^{-2} was used to induce the inversion layer. For lower charge densities, for example, -4 × 10^{12} cm^{-2} as is the typical charge density of an AlO_x layer, Werner et al. [73] reported a reduction in emitter sheet resistance from 15-18 kΩ/sq in the dark to 4 kΩ/sq on 1.5-1.6 Ω·cm n-type substrates under illumination. The effect of photo-generated carriers needs to be considered while evaluating the resistive losses in IL cells.

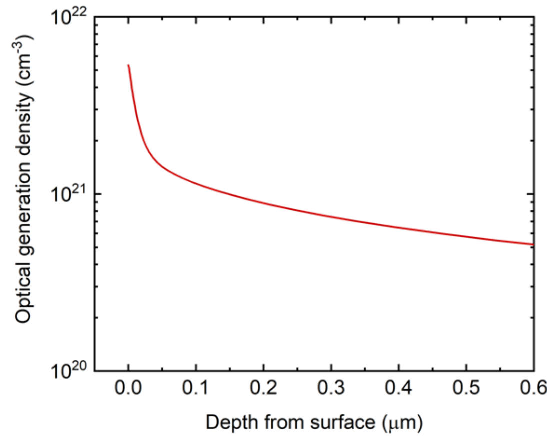

Figure 4-14 Generation profile used for simulations with illumination.

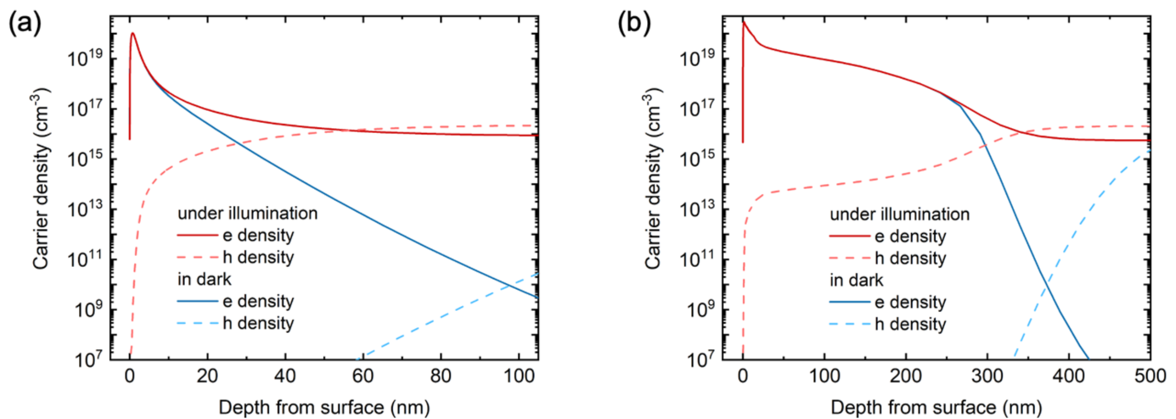

Figure 4-15 Simulated carrier density profiles of (a) a field-induced inversion layer with a positive charge density of 2 × 10^{13} cm^{-2}, and (b) a P-diffused emitter near the interface in the dark and under illumination.

4.2.3 Summary

In this section, a model representing the characteristics of A1 samples was developed in Sentaurus TCAD. The interface parameters were calibrated to A1 samples using the sheet resistance response to charge density as a reference experiment. The model was demonstrated to be reliable for charge densities up to 4×10^{13} cm^{-2}, and was used to study the properties of field-induced inversion layers. It was observed that the sheet conductance increases with charge density. However, due to the increased surface scattering and thus reduced carrier mobility, the sheet conductance plateaus for charge densities above 2×10^{13} cm^{-2}. Passivating band-tail interface states was shown to be important in obtaining high sheet conductance, while reducing $D_{it\text{-}CB}$ to below 10^{14} $eV^{-1}cm^{-2}$ was proved less effective in improving the sheet conductance. As a result, the lowest inversion layer sheet resistance achievable is ~1.1 kΩ/sq, which is 7 times higher than that of typical P-diffused emitters [10]. The impact of substrate resistivity on inversion layers was found to be minor for $D_{it\text{-}CB}$ below 10^{14} $eV^{-1}cm^{-2}$ and charge densities above 10^{13} cm^{-2}. The inversion layer sheet resistance is thus determined by dielectric charge density and band-tail interface state density. The density of ionic charge introduced using the ion migration method and band-tail interface state densities will be evaluated in Section 4.5 and Chapter 5, respectively, to estimate their impact on field-induced charge layers. Upon illumination, the inversion layer sheet conductance can be boosted by 7.4%. This needs to be considered while determining the optimum sheet resistance and finger spacing for IL cells. This section investigated the impact of charge density, band-tail interface state density, substrate resistivity and illumination on inversion layer sheet resistance. Their significance on IL cells will be evaluated by using this understanding as input for complete solar cell device simulations in Chapter 7.

4.3 Impact of Ion Embedding on Surface Passivation

In solar cells, mid-gap interface states are often efficient recombination centres according to SRH statistics. A low $D_{it\text{-}CB}$ is necessary to ensure low sheet resistance in field-induced emitters. Both $D_{it\text{-}midgap}$ and $D_{it\text{-}CB}$ are important to the performance of IL cells. This section investigates the impact of ionic charge inside the oxide thin film on the surface passivation of the interface as given by the mid-gap and band-tail interface state densities.

The interface of one pristine A2 sample and that of one ion-charged A2 sample were characterised and compared to determine the damage caused during the ion injection process. Positive K^+ ions were incorporated by one spin coating of the KCl solution (KCl concentration B: 5×10^{-3} mol/L, 3000 rpm, 30 s) and 8 subsequent corona discharge (30 kV, 30 s)-anneal (430 °C, 10 s) cycles. The ion embedding was processed symmetrically on both sides of the sample. The lifetime was measured as a function of surface potential to extract the interface parameters (Section 3.6.4.2). Figure 4-16 shows the lifetime data recorded for the two samples. The dashed lines are the corresponding lifetime curves generated using the analytical model. The extracted interface parameters are listed in

Table 4-2. In Figure 4-16, the shift of the valley from 0 V to -45 V upon ion injection corresponds to an increase in charge density from 10^{11} cm^{-2} to 9.7×10^{12} cm^{-2}. The broadening of the valley results from the inhomogeneity of charge density across the specimen, evidenced by an increase in σ_p from 5×10^{10} to 10^{12} cm^{-2}. Upon incorporating the ionic charge, $D_{it-midgap}$ increases by one order of magnitude from 2.8×10^{10} to 3.6×10^{11} $eV^{-1}cm^{-2}$, demonstrating the damage to surface passivation. The hypothesis is that the accumulation of K^+ ions at the interface causes strain that generates defects and leads to an increase in $D_{it-midgap}$. This effect has been observed in prior work [127]. The Si substrates used in this experiment were passivated solely by 100 nm thermal oxide without hydrogenation steps. A subsequent experiment is the addition of a hydrogenation step, which can be achieved by the deposition of a SiN_x or AlO_x layer and an activation anneal for improved surface passivation. Such methods should be explored in future work but were not applied here due to the lack of available deposition equipment. As explained in Section 3.6.4.2, the model assumes a perfect bulk lifetime. This will lead to a large error in the regions with a strong field effect, which is where D_{it-CB} and D_{it-VB} were extracted. In addition, the measurement may be limited by the breakdown strength of the oxide at large potentials, where the current going through the dielectric may be high. Therefore, the accuracy of D_{it-CB} and D_{it-VB} extracted using this method is compromised. These results demonstrate that surface passivation is degraded during the ion migration process. Methods to re-passivate the defect states or to reduce the damage should be explored in future work.

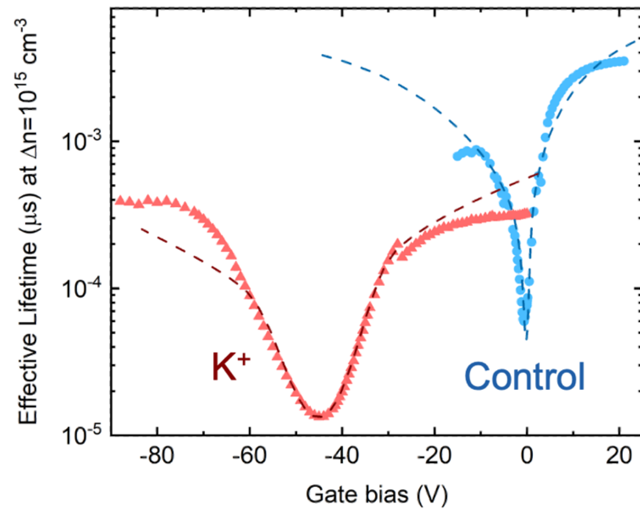

Figure 4-16 Experimental data (dotted line) and its analytical fitting (dashed line) of the effective lifetime of one sample with no ionic charge and one sample with K^+ ions incorporated by one spin coating and the subsequent drive-in.

Table 4-2 Interface parameters used in the analytical model to fit the experimental data of one sample with no ionic charge and one sample with K^+ ions incorporated.

	Control	**K^+ ions introduced**
$D_{it\text{-}midgap}$ ($eV^{-1}cm^{-2}$)	2.8×10^{10}	3.6×10^{11}
$D_{it\text{-}CB}$ ($eV^{-1}cm^{-2}$)	9×10^{13}	7.5×10^{14}
$D_{it\text{-}VB}$ ($eV^{-1}cm^{-2}$)	5×10^{13}	3.5×10^{14}
Q_f (cm^{-2})	10^{11}	9.7×10^{12}
σ_q (cm^{-2})	5×10^{10}	10^{12}

Despite the surface passivation being degraded, little bias is applied in the working condition of a solar cell. Therefore, surface recombination with no external bias applied should be considered. Figure 4-17.a shows the calculated effective surface recombination velocity (S_{eff}) of a 200 µm, n-type silicon substrate at an injection level of 10^{15} cm^{-3} as a function of charge density. The charge density and interface parameters from the fit of the pristine sample were used in this calculation. Due to field-effect passivation, S_{eff} decreases with charge density and plateaus at high charge densities. Figure 4-17.b shows a comparison of S_{eff} of (i) the pristine sample, (ii) the ionically charged sample and (iii) an ionically charged sample assuming no damage occurred to the chemical surface passivation. The third model assumed a charge density of 9.6×10^{12} cm^{-2} and used the interface parameters of the pristine sample. When there is no external charge in the dielectric, both models with ionic charge (blue and yellow) show less recombination than that of the pristine sample (red). These results indicate that although the surface passivation is degraded during the ion injection process, the IL cell design compensates for some of this damage thanks to the strong field-effect passivation. The stronger the electric field the better the tolerance to chemical interface degradation. Despite this tolerance, it is noted that the best device efficiencies require both highly charged dielectrics and high-quality chemical interfaces.

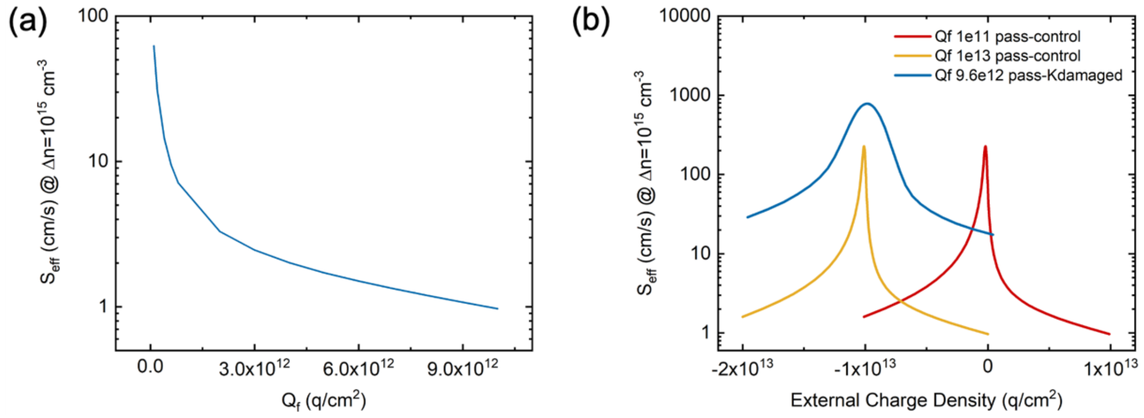

Figure 4-17 Calculated S_{eff} as a function of external charge density (a) with interface parameters extracted from the fit of the pristine A2 sample, and (b) a comparison of that with/without K^+ ions incorporated.

4.4 Stability of Field-Induced Electron Accumulation Layer

The stability of accumulation layer sheet resistance was tested against elevated temperature and UV irradiation. Figure 4-18 shows the average accumulation layer sheet resistance measured from four identical samples after the ion migration process. This is done by repeating 4 times the spin coating of the KCl solution (concentration B: 5×10^{-3} mol/L, 3000 rpm, 30 s) with each followed by the 8 subsequent corona discharge (30 kV, 30 s)-anneal (430 °C, 10 s) cycles. The samples were stored at room temperature in the dark until the sheet resistance stabilised. In equilibrium, the sheet resistance is determined by charge density and band-tail interface state density. However, the recorded sheet resistance shows a reduction within 25 days after processing. This can be explained by the effect of hot carrier injection, which was also observed in the results presented in Section 4.1. The stability of the sheet resistance was then tested against an elevated temperature (120 °C) and UV irradiation (5 mWcm^{-2}) separately for 2 months. During the 2-month period, no increase was observed for the samples kept at the elevated temperature nor for the ones kept under UV

irradiation, demonstrating promising stability of sheet resistance of the field-induced electron accumulation layers.

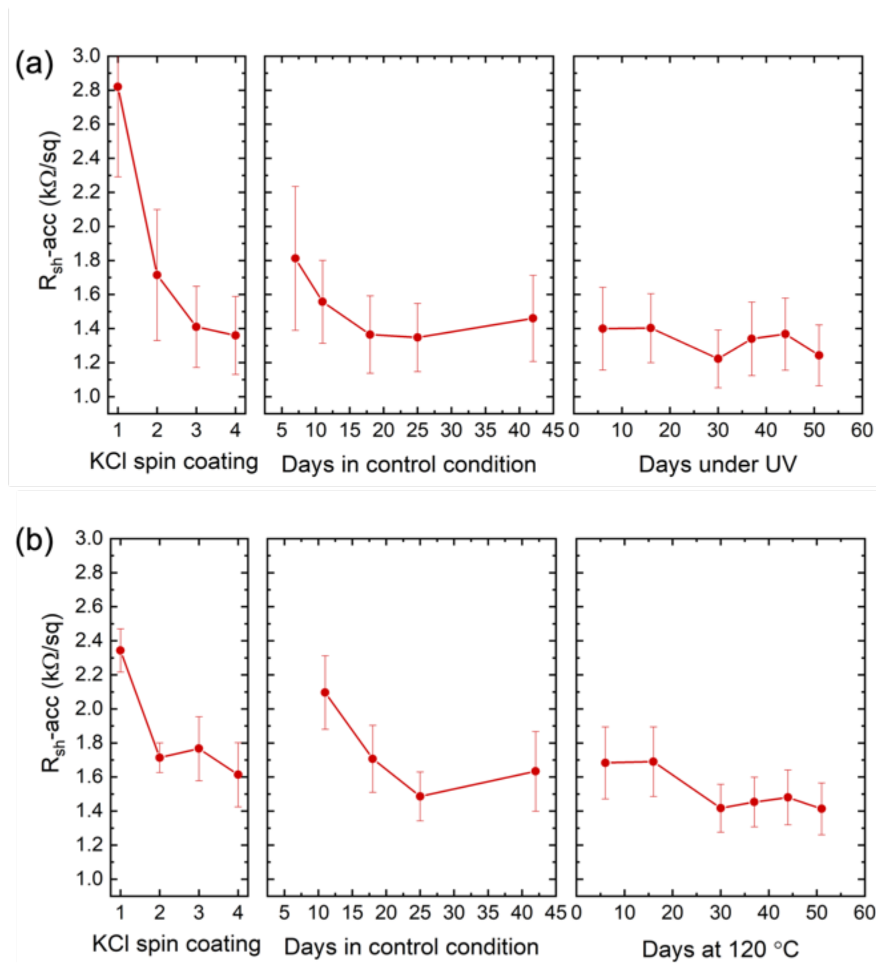

Figure 4-18 Accumulation layer sheet resistance on A2 samples upon drive-in of K^+ ions delivered by spin coating of the KCl solution by 4 times and kept (a) under UV irradiation, (b) at 120 °C for 2 months.

4.5 Discussion

An accumulation layer sheet resistance of 950 Ω/sq was achieved experimentally using the ion injection method. To my knowledge this is the lowest value achieved in the research field of IL cells [72], [73]. The charge density was not measurable since it was out of range for most regular characterisation methods. The accumulation layer sheet resistance was simulated here to estimate the corresponding ionic charge density. The results are plotted in

Figure 4-19. The accumulation layer sheet resistance is expected to fall into the range of 1-1.2 kΩ/sq at a charge density of 2-4 × 10^{13} cm^{-2}. This suggests that the charge density obtained experimentally for the 950 Ω/sq sheet resistance is in the order of 10^{13} cm^{-2}. The fact that the measured sheet resistance of 950 Ω/sq is lower than the lowest simulated sheet resistance can be explained by the following reasons: (i) the actual charge density introduced is unknown and may exceed 4 × 10^{13} cm^{-2}, (ii) the model deviates from the physical sample and does not provide precise predictions of the accumulation layer at such high charge densities, especially with regard to the exact carrier mobility, and (iii) possible error in the measurements. Nonetheless, these results indicate that charge densities in the order of 10^{13} cm^{-2} can be obtained using the ion migration method. This is the highest charge density achieved in the literature (Table 2-1). According to the simulation results, for well-passivated surfaces, inversion layer sheet resistance plateaus for charge densities above 2 × 10^{13} cm^{-2}. This suggests that the ion injection method may be capable of achieving the highest IL cell efficiency if implemented in the IL cell fabrication procedure.

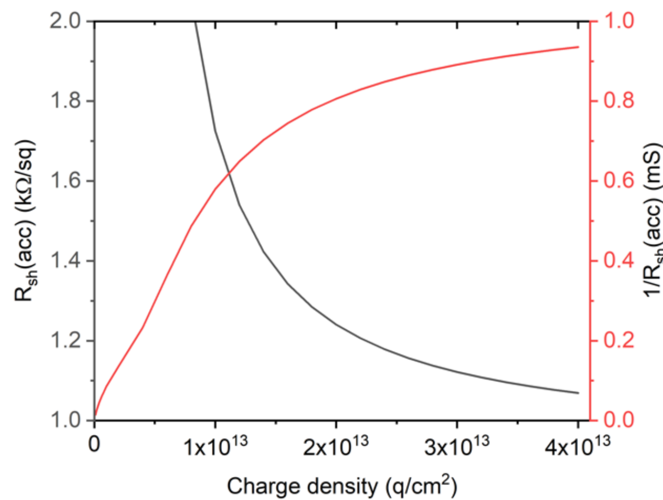

Figure 4-19 Simulated accumulation layer sheet resistance (left axis) and sheet conductance (right axis) on a 1 Ω·cm, n-type Si substrate as a function of positive charge density.

The simulation results showed that both a high charge density and a low band-tail interface state density are critical in obtaining high inversion layer sheet conductance. The impact of interface states on the formation of a charge-induced emitter has not been discussed in most work in the literature. The highest charge density has been demonstrated using the ion injection method. In terms of the band-tail interface states, they originate from the termination of the periodicity of bulk silicon. Methods to reduce the density of the states need to be explored. A characterisation methodology to detect the tail states was developed and will be introduced in Chapter 5. This method can be used to evaluate the effectiveness of any passivation methods.

The inversion layer sheet resistance can reach ~1.1 kΩ/sq on 1 Ω·cm, p-type silicon substrates in the dark. Although it is high compared with that of P-diffused emitters (150 Ω/sq), the optimum emitter sheet resistance is still under debate. Ref [10] shows a tendency for diffused emitters to move to higher sheet resistance for less carrier recombination. Whether the 1.1 kΩ/sq sheet resistance limits the IL cell performance will be evaluated by device simulations in Chapter 7. In addition, photo-generated carriers will be introduced under illumination and will also contribute to emitter sheet conductance. This effect should be considered while determining the resistive losses in the emitter. The simulation results have shown a higher dependence of emitter sheet conductance on illumination for IL emitters than for diffused emitters. This can be explained by the difference in carrier density in the dark. The inversion layer simulated on a 1 Ω·cm substrate with a charge density of 2×10^{13} cm^{-2} showed a reduction in sheet resistance from 1.30 to 1.21 kΩ/sq upon 1-sun illumination. Werner et al. [73] reported that for an inversion layer induced by a negative charge density of -4×10^{12} cm^{-2} on 1.5-1.6 Ω·cm n-type substrates, the sheet resistance reduced from 15-18 kΩ/sq to 4 kΩ/sq upon illumination. This different

extent of sheet conductance increase can be explained by the difference in the dielectric charge density and thus the carrier density in the IL emitter. The density of photo-generated carriers under illumination is dependent on the minority carrier lifetime in the emitter. Therefore, carrier recombination should be minimised to obtain high IL emitter sheet conductance. Further studies on the impact of carrier recombination on emitter sheet resistance under illumination and IL cell performance should be carried out in the future.

The accumulation of K^+ ions near the interface has been shown to damage surface passivation. This will lead to a trade-off between a high charge density for low emitter sheet resistance and a low charge density for reduced damage to surface passivation. Methods to re-passivate the states or to reduce the damage, for example, by hydrogenation through depositing a SiN_x or AlO_x layer, should be tested in the future.

4.6 Summary

An ion injection method was used to incorporate positive alkali ions into a silicon oxide thin film. An electron accumulation layer sheet resistance as low as 950 Ω/sq was achieved using the method. The 950 Ω/sq is the lowest value achieved in the research field of IL cells [72], [73]. A model was developed to study the formation and characteristics of field-induced charge layers. The simulation results showed that both a high charge density and a low band-tail interface state density are necessary to obtain low inversion layer sheet resistance. With optimised charge density and $D_{it\text{-}CB}$, inversion layer sheet resistance is limited to ~1.1 kΩ/sq in the dark. For an inversion layer induced by a charge density of 2×10^{13} cm^{-2} on a 1 Ω·cm, p-type Si substrate, an increase in inversion layer sheet conductance by 7.4% was demonstrated under 1-sun illumination. It was confirmed that the surface passivation is damaged during the ion migration process, resulting in an increase in $D_{it\text{-}midgap}$. However,

while no bias is applied, the SRV of the ion-charged sample is lower than that of the pristine sample due to strong field-effect passivation. The stability of accumulation layer sheet resistance was tested against an elevated temperature and UV irradiation. No evident degradation was observed during the 2-month period, demonstrating promising stability of the field-induced electron layer.

Chapter 5 Characterisation of Defect States at Dielectric-Silicon Interfaces

The interface state density at the band tails has been shown several orders of magnitudes higher than that at the mid-gap. Therefore, in the case of inversion layers on p-type silicon substrates, high electron populations at the surface cause the Fermi level to approach the edge of the conduction band where the band-tail interface states can trap a large portion of these electrons. The band-tail interface states can hence strongly influence the carrier distribution near the interface. Chapter 4 has shown how this dependence requires that a low $D_{it\text{-}CB}$ is achieved to obtain a high sheet conductance in the field-induced electron layer. It is therefore important to explore methods to characterise and passivate the band-tail interface states. Here I present a characterisation method I developed to best understand band-tail interface states at semiconductor-dielectric interfaces with the help of simulations.

5.1 Impact of Interface States on Field-Induced Layers

Field-induced charge carriers can be trapped at the interface. The amount of trapping can hence be used to infer the interface state density. In this section, the impact of trapped carriers on the resistance of field-induced layers will be explained. After that, the feasibility of using the resistance dependence of charge density as a reference to determine band-tail interface state density will be tested via simulations.

5.1.1 Carrier Trapping at Interface States

Figure 5-1 illustrates the band diagram of an n-type Si substrate near a silicon-dielectric interface with (a) no surface charge specified, (b) in the presence of positive and (c) negative surface charge. The acceptor- and donor-like interface states, as explained in Chapter 1, are also shown in the figure. At the interface, electrons will be trapped at the acceptor-like states below the Fermi level, and holes will be trapped at the donor-like states above the Fermi level. In Figure 5-1.a, for an n-type silicon substrate with no surface charge specified, the net charge of the carriers trapped in the interface states is negative, leading to a depletion of electrons near the interface and hence an upward band bending. In the presence of positive surface charge, in Figure 5-1.b, the electric field will lead to an accumulation of mirrored electrons near the interface and thus a downward band bending. With sufficiently high positive charge density, the Fermi level will approach the conduction band edge so that more electrons will be trapped at the acceptor-like band-tail interface states. In the presence of negative surface charge, the reverse is the case, where the region near the interface will first deplete and then be inverted into p-type providing a sufficiently high charge density. With negative surface charge, the Fermi level will lie close to the valence band edge and allow the band-tail donor-like interface states to trap holes. In both scenarios, the band-tail interface state density is several orders of magnitudes higher than the mid-gap interface state density. Therefore, in heavy accumulation/inversion regimes, the trapped carriers at the interface will lead to a significant reduction in the concentration of free charge carriers induced in the accumulation/inversion layer. This will lead to a reduction in the sheet conductance of the field-induced charge layers. Since the conductivity is determined by both the surface charge density and the interface states, this dependence can be used as a reference to characterise the interface states. Its practicability will be evaluated next.

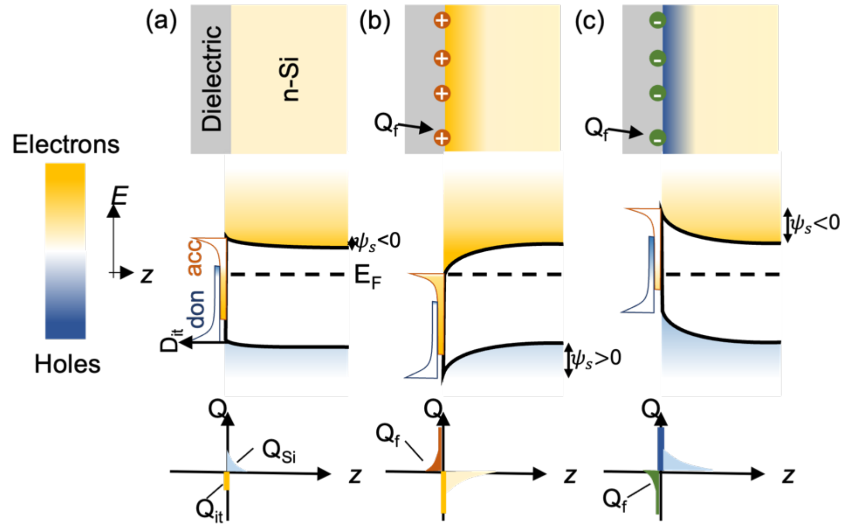

Figure 5-1 Schematic energy diagram near a silicon-dielectric interface (a) with no surface charge specified, in the presence of (b) positive, and (c) negative dielectric charge. Redrawn from [46].

5.1.2 The Dependence of Resistance on Surface Charge and its Link to Band-Tail Interface States

This subsection investigates the impact of interface states on the sheet resistance of field-induced charge layers. The relation between inversion/accumulation layer sheet resistance and surface charge density was simulated with varied $D_{it\text{-}midgap}$, $D_{it\text{-}CB}$, and $D_{it\text{-}VB}$. The model developed in Chapter 4 was used for the simulations. The sheet resistance of the entire wafer is measurable experimentally. For simplicity, wafer sheet resistance instead of inversion/accumulation layer sheet resistance was simulated. In the model, the dependence of band-tail interface state density on energy (E) was defined as follows:

$$D_{it-acc}(E) = D_{it-CB} \times e^{-\frac{(E_g - E)}{E_{0,CB}}} \qquad \text{Eq (5-1)}$$

$$D_{it-don}(E) = D_{it-VB} \times e^{-\frac{E}{E_{0,VB}}} \qquad \text{Eq (5-2)}$$

following the same variable definition stated in Section 4.2.1.1. E is the energy from the valence band edge in eV. Since $E_{0,CB}$, $E_{0,VB}$, D_{it-CB}, and D_{it-VB} may vary at different silicon/dielectric interfaces [146], the band-tail interface state density was integrated into single metrics N_{it-acc} and N_{it-don}:

$$N_{it-acc} = \int_0^{E_g} D_{it-acc}(E)dE \qquad \text{Eq (5-3)}$$

$$N_{it-don} = \int_0^{E_g} D_{it-don}(E)dE \qquad \text{Eq (5-4)}$$

N_{it-acc} and N_{it-don} describe the total concentration of band-tail interface states available for occupation. In this thesis, $E_{0,CB}$ and $E_{0,VB}$ were set to 0.028 eV and 0.024 eV, respectively, to reflect average values extracted from previous work [27], [33], [36]. With fixed $E_{0,VB}$, N_{it-don} can be worked out as:

$$\begin{aligned} N_{it-don} &= \int_0^{E_g} D_{it-CB} \times e^{-\frac{E}{E_{0,VB}}} dE \\ &= E_{0,VB} \times D_{it-CB} \times \int_{-\frac{E_g}{E_{0,VB}}}^{0} e^{-\frac{E}{E_{0,VB}}} d\left(-\frac{E}{E_{0,VB}}\right) \qquad \text{Eq (5-5)} \\ &= 0.024\, eV \times D_{it-CB} \times (e^0 - e^{-\frac{1.12\, eV}{0.024\, eV}}) \\ &\approx 0.024\, eV \times D_{it-CB} \end{aligned}$$

Similarly, N_{it-acc} can be represented as:

$$N_{it-acc} \approx 0.028\, eV \times D_{it-CB} \qquad \text{Eq (5-6)}$$

Using the above definitions for band-tail interface states, the sheet resistance of a 200 μm thick, 1 Ω·cm n-type silicon substrate was simulated as a function of positive/negative surface charge density and is plotted in Figure 5-2. D_{it-CB} was set to 10^{14} $eV^{-1}cm^{-2}$ and D_{it-VB}

was set to 5×10^{13} $eV^{-1}cm^{-2}$ in this section unless specified otherwise, corresponding to $N_{it\text{-}acc}$ and $N_{it\text{-}don}$ of 2.8×10^{12} and 1.2×10^{12} cm^{-2}, respectively. In Figure 5-2.a and Figure 5-2.b, $D_{it\text{-}midgap}$ was varied while $N_{it\text{-}acc}$ and $N_{it\text{-}don}$ were set constant. It is evident that $D_{it\text{-}midgap}$ has a minor effect on wafer sheet resistance for $D_{it\text{-}midgap}$ below 10^{12} $eV^{-1}cm^{-2}$, which is the case for most passivated surfaces [14], [147]. Therefore, the impact of charge carriers trapped at the mid-gap interface states on the field-induced charge layers is negligible. In Figure 5-2.c and Figure 5-2.d, $D_{it\text{-}midgap}$ was set to 5×10^{10} $eV^{-1}cm^{-2}$ and N_{it} was varied. In previous work, N_{it} has been reported of the order of 10^{12} cm^{-2} [146], [148]. To account for the possible variations in N_{it} due to different surface treatments, a range of N_{it} from 10^{11} cm^{-2} to 10^{13} cm^{-2} was used in the simulations. In Figure 5-2.c and Figure 5-2.d, significant changes are observed in both the total wafer sheet resistance and its dependence on charge density. It is noted that the reduction in wafer sheet resistance is larger in the case of positive surface charge than negative surface charge. This is due to the higher electron mobility than hole mobility, as it is known in the field from parametrisations in the work of [132]. Figure 5-3 shows the simulation results on p-type silicon substrates, where similar trends are observed: large dependence of resistance on the density of tail states, and marginal dependence on mid-gap states. The simulation results suggest that in both the accumulation and inversion scenarios, the resistance dependence on surface charge density can be used for the determination of the band-tail interface state density. The simulated resistance will be correlated with experimental data in the next section.

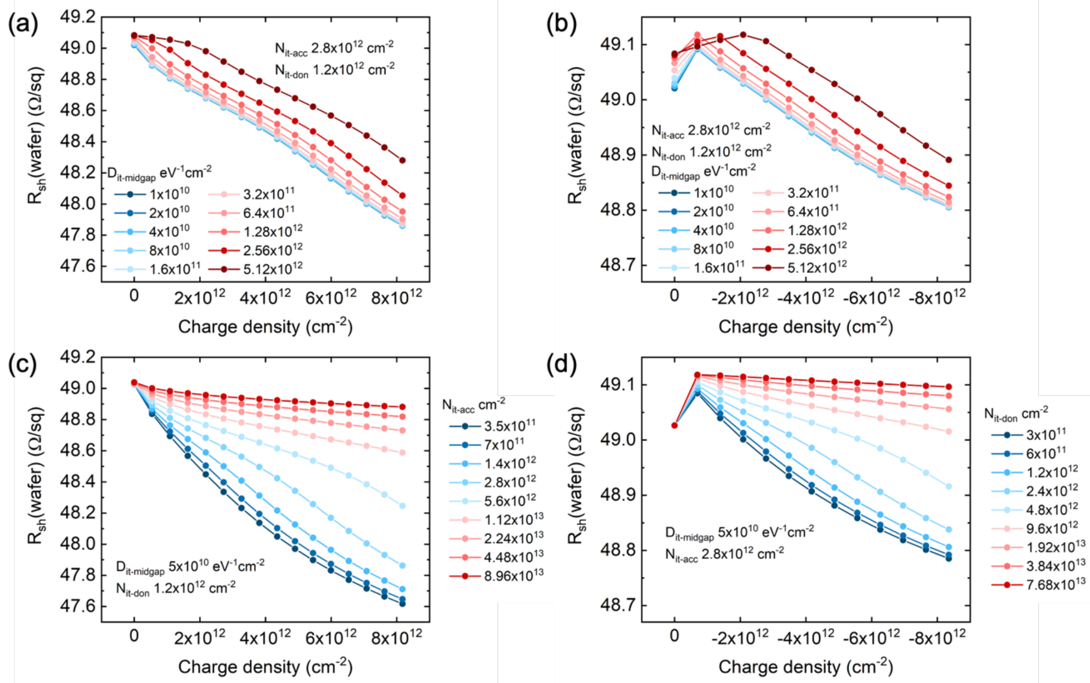

Figure 5-2 Simulated wafer sheet resistance as a function of charge density in both polarities of a 200 µm thick, 1 Ω·cm n-type Si substrate with varied (a), (b) $D_{it\text{-}midgap}$, (c) $N_{it\text{-}acc}$ and (d) $N_{it\text{-}don}$.

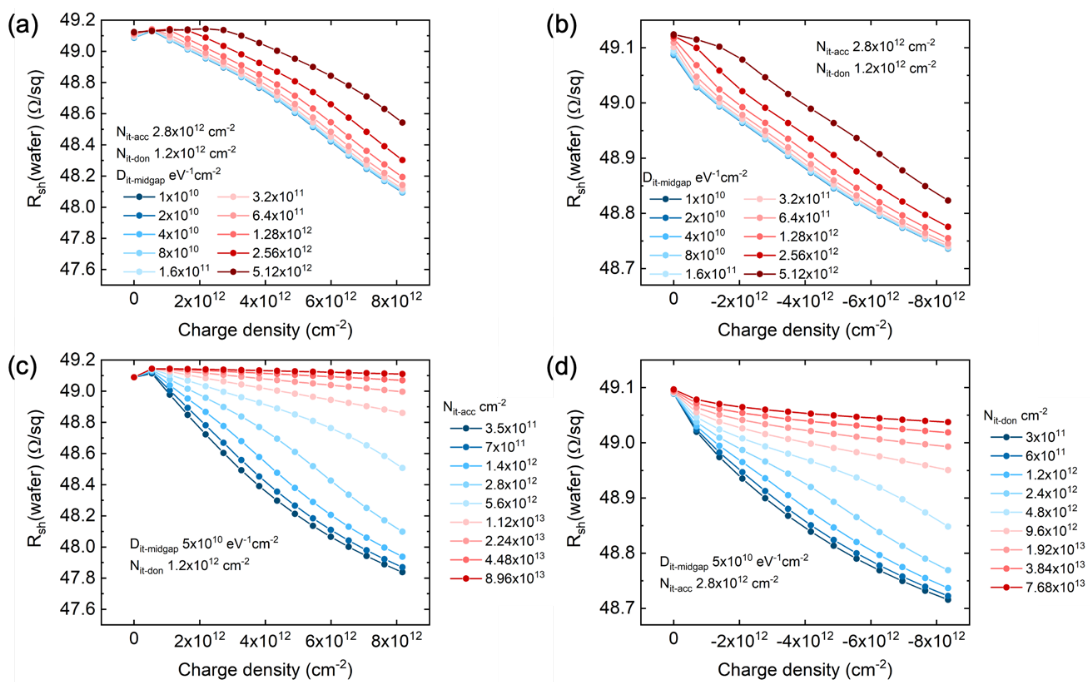

Figure 5-3 Simulated wafer sheet resistance as a function of charge density in both polarities of a 200 µm thick, 1 Ω·cm p-type Si substrate with varied (a), (b) $D_{it\text{-}midgap}$, (c) $N_{it\text{-}acc}$ and (d) $N_{it\text{-}don}$.

5.2 Characterising Band-Tail Interface States

5.2.1 The Method

The method uses an experimentally obtained resistance-surface charge density relation as a reference and reproduces the observed trend via simulations. Figure 5-4 shows the process sequence of the method. Firstly, a sheet resistance (R_{sh})-charge density (Q) relation is obtained experimentally by recording the wafer sheet resistance while introducing controlled amounts of corona charge to the sample surface. R_{sh}-Q curves are then generated via simulations with wafer resistivity and band-tail interface state density adjusted to fit the experimental data. The quality of the fit can be evaluated using the mean squared error. Finally, the interface parameters in the best fit are extracted to describe the silicon-dielectric interface.

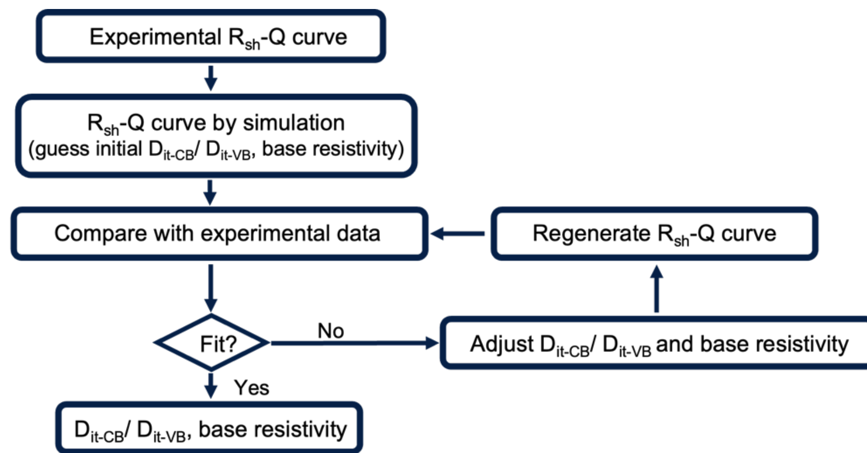

Figure 5-4 Process sequence of the band-tail interface state density characterisation method.

5.2.2 Reliability of the Method

First I evaluate the reliability of the method in practical applications. The range of N_{it} applicable and the impact of variations in base resistivity were investigated. The method uses resistance-surface charge density relation as a reference. For simplicity, a new metric,

ΔR_{sh}(wafer), is used here to evaluate the method's sensitivity. ΔR_{sh}(wafer) is defined as the difference in wafer sheet resistance between the surface charge density being set to $\pm 8 \times 10^{12}$ cm^{-2} and when no surface charge is specified:

$$\Delta R_{sh}(wafer) = R_{sh}(wafer)_{Q=0} - R_{sh}(wafer)_{Q=\pm 8\times 10^{12}\ cm^{-2}} \quad \text{Eq (5-7)}$$

A higher ΔR_{sh}(wafer) indicates that the change in resistance can be more easily detected experimentally. In addition, for $N_{it\text{-}acc}$ or $N_{it\text{-}don}$ to be distinguished, they should lead to observable changes in ΔR_{sh}(wafer). ΔR_{sh}(wafer) was simulated as a function of N_{it} on a 200 µm thick, 1 Ω·cm n-Si substrate. Figure 5-5 shows the simulation results. In Figure 5-5.a, it is evident that a significant drop in ΔR_{sh}(wafer) occurs in the range from $N_{it\text{-}acc} = 10^{12}$ to 4×10^{13} cm^{-2}, indicating that this method is most sensitive to $N_{it\text{-}acc}$ within this range. For $N_{it\text{-}acc}$ below 10^{12} cm^{-2}, the contribution of tail states approaches the contribution from that of mid-gap states and it becomes difficult to differentiate them. For $N_{it\text{-}acc}$ above 4×10^{13} cm^{-2}, the concentration of charge-induced free carriers in the silicon near surface does not change substantially, resulting in a reduced change in ΔR_{sh}(wafer). This will lead to $N_{it\text{-}acc}$ above 4×10^{13} cm^{-2} being difficult to differentiate. In Figure 5-5.b, similar trends can be observed for $N_{it\text{-}don}$. However, ΔR_{sh}(wafer) for $N_{it\text{-}don}$ is one order of magnitude lower than that of $N_{it\text{-}acc}$, suggesting that $N_{it\text{-}don}$ is more difficult to detect. To conclude, in terms of variations in ΔR_{sh}(wafer) against N_{it}, this characterisation method is most sensitive for N_{it} in the range of 10^{12} to 4×10^{13} cm^{-2}. Another point to note is that ΔR_{sh}(wafer) must be high enough to be detected experimentally. For N_{it} that produces low ΔR_{sh}(wafer), the error of the resistance measurement technique must be considered to determine if such changes can be detected above the error threshold.

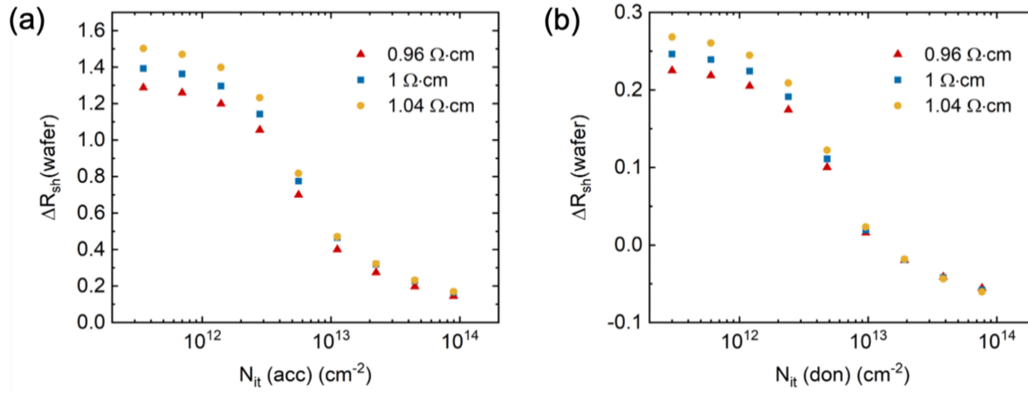

Figure 5-5 Simulated ΔR_{sh}(wafer) as a function of (a) $N_{it\text{-}acc}$ and (b) $N_{it\text{-}don}$ on a 200 µm thick, 1 Ω·cm n-Si substrate with varied base resistivities.

Variations in base resistivity can cause a shift in wafer sheet resistance. Since base resistivity in commercial CZ silicon wafers can scatter by 1-3% [100], it was varied in the model to simulate its impact on the characterisation. Figure 5-5 includes the simulation results where the base resistivity was varied by ±0.04 Ω·cm. The results indicate that the variation will cause an evident change in ΔR_{sh}(wafer), especially in the regions with low N_{it}. This means that the accuracy of N_{it} obtained using this method depends strongly on the accuracy of the input wafer resistivity. The base resistivity will thus be adjusted in the fits of the R_{sh}(wafer)-Q relations. N_{it} can then be determined using this method with no evident artefacts originating from wafer resistivity variations.

5.3 Band-Tail Interface States at a Si-SiO_2 Interface

In this section, the characterisation method was applied to four sample sets with their surfaces treated differently to demonstrate the capability of this technique. Experimental R_{sh}-Q data was obtained by recording R_{sh} while controlled amounts of corona ions were deposited onto the dielectric surface. The density of corona ions was controlled by the corona discharge time. A calibration of the deposition rate was included in Section 3.6.2.

The wafer sheet resistance was recorded after every 10 s of corona discharge. The resistance was monitored by the Van der Pauw method or the inductively coupled measurements, as described in Section 3.6.3. Examples using both resistance measurement techniques are shown next.

5.3.1 Sheet Resistance Measurements by Van der Pauw Method

$N_{it\text{-}acc}$ of three sets of n-type specimens (A1, A2, and A3) were characterised. The samples were diced into 1 × 1 cm^2 squares. As described in Chapter 3, the dielectric layer at the corners was removed using a diamond scriber. An aluminium layer of 100 nm was deposited onto the corners for electrical contact. Positive corona ions were deposited onto the sample surface to induce an electron accumulation layer. During Van der Pauw measurements, the current can take the path via either the electron accumulation layer or the n-type base (Section 4.1). Hence the Van der Pauw method measures the sheet resistance of the entire sample. Figure 5-6 shows the recorded wafer sheet resistance as a function of surface charge density. The uniformity of the corona charge density was tested in reference [149] by constructing a 3 × 3 cm^2 map of surface potential using Kelvin Probe measurements, showing a standard deviation of 3.5%. An error bar is included in charge density in Figure 5-6 to account for this variation. The resistance measurement was carried out on an A1 sample for 40 times with each taken after an anneal at 430 °C for 10 s. The resistance stabilised after the first 9 measurements. The last 31 points showed an error of 0.12%. An error bar of 0.12% is included in the wafer sheet resistance in Figure 5-6. In the numerical model, wafer resistivity and $N_{it\text{-}acc}$ were adjusted to obtain the best fit for each data set. The simulated curves are plotted in dashed lines in Figure 5-6. The corresponding parameters extracted from the fits are listed in

Table 5-1. No evident drop in $N_{it\text{-}acc}$ is observed for the Si/SiO_2 (100 nm) samples after an FGA, indicating that the enhanced chemical passivation by FGA is not evident at the band tail. For the two sets with FGA, the set with 10 nm of oxide presents lower $N_{it\text{-}acc}$ values than the one with 100 nm of oxide, which may originate from the difference in oxidation temperature (1050 °C for 100 nm oxide vs. 950 °C for 10 nm oxide). However, for all three sample sets, $N_{it\text{-}acc}$ is within a narrow range of 3-6 × 10^{12} cm^{-2}. The trends presented are extracted from only two samples in each sample set. A larger group of data would be required to draw a conclusion.

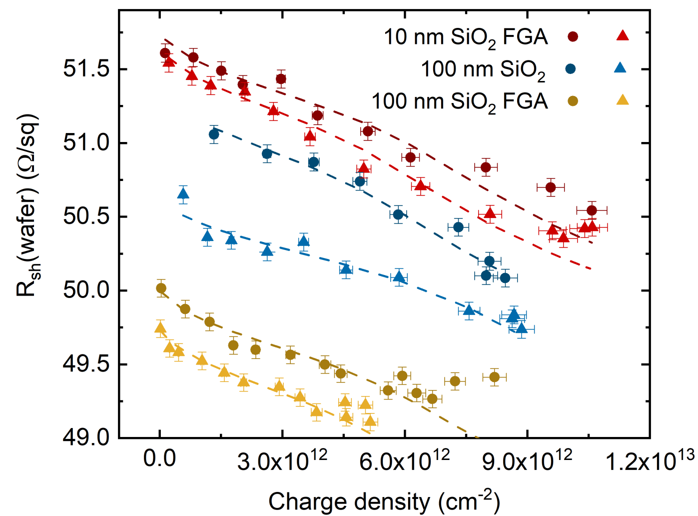

Figure 5-6 Experimental (symbols) and simulated (dashed lines) wafer sheet resistance-charge density relations.

Table 5-1 Summary of parameters extracted from the fits of the experimental wafer sheet resistance-charge density relations for A1, A2, and A3 specimens.

	10 nm oxide, FGA		**100 nm oxide**		**100 nm oxide, FGA**	
Specimens	A3-1	A3-2	A2-1	A2-2	A1-1	A1-2
Wafer resistivity (Ω·cm)	1.054	1.056	1.033	1.048	1.0145	1.02
$D_{it\text{-}CB}$ (10^{14} $eV^{-1}cm^{-2}$)	1.2	1.5	2	1.2	1.1	1.4
$N_{it\text{-}acc}$ (10^{12} cm^{-2})	3.36	4.2	5.6	3.36	3.08	3.92
Mean Squared Error (10^{-2})	1.7	1.5	0.54	0.40	0.46	2.6

Negative corona charge is required to characterise $N_{it\text{-}don}$ for n-type specimens. This will result in the formation of a p-type inversion layer. As explained in Section 4.1, an inversion layer cannot be directly contacted using the same sample structure shown in Figure 3-6. An additional p-type local doping underneath the aluminium patches is necessary to ensure a complete electrical path through the inversion layer, so that the sheet resistance of only the inversion layer, instead of the entire wafer, can be measured. Due to the lack of p-type local doping tools in our laboratory, extracting $N_{it\text{-}don}$ from an inversion layer using this method was not demonstrated in this thesis. Instead, the potential of the method was evaluated assuming that p-type doping under the contacts is possible via appropriate local doping techniques. Figure 5-7 shows the simulated inversion layer sheet resistance as a function of negative charge density. The thickness of the inversion layer was determined by the depth at which the electron density exceeds the hole density. The sheet resistance is plotted on a log scale. It is observed that $N_{it\text{-}don}$ has a significant impact on the inversion layer sheet resistance, allowing the determination of $N_{it\text{-}don}$ with the aid of numerical simulations. Based

on the analysis above, Van der Pauw measurements in combination with device simulations are shown to be a suitable method to characterise band-tail interface states near both band edges.

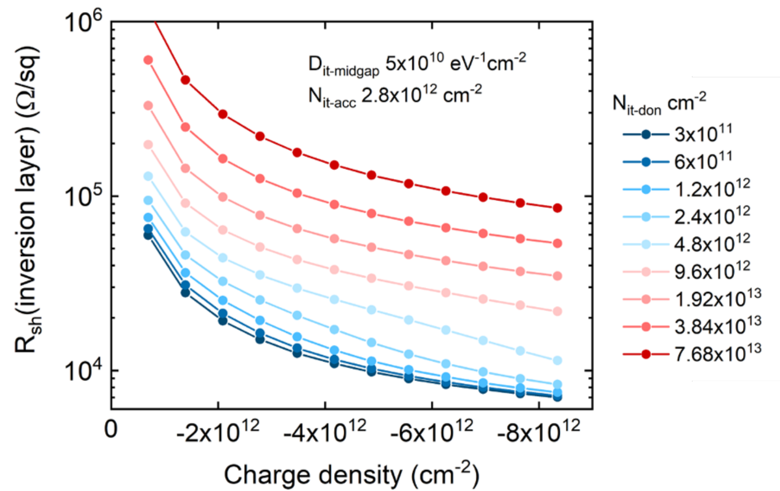

Figure 5-7 Simulated inversion layer sheet resistance as a function of negative charge density on a 200 µm thick, 1 Ω·cm n-Si substrate with varied $N_{it\text{-}acc}$.

5.3.2 Sheet Resistance Measurements by Inductively Coupled Measurements

In this subsection, a Sinton lifetime tester was used to monitor the wafer sheet resistance via inductively coupled measurements (ICM) as described in Section 3.6.3.2. In ICM free carriers in both the field-induced charge layer and the substrate contribute to the measured conductance. Compared with the Van der Pauw method, the advantages of this method include (i) simple sample preparation since no metal contacts are required, and (ii) wafer sheet resistance in both the accumulation and inversion scenarios can be measured, allowing characterisation of $N_{it\text{-}acc}$ and $N_{it\text{-}don}$ on a same sample set with no additional processing. n-type A2 specimens and p-type A4 specimens were characterised to demonstrate the method. The sheet resistance of the specimens was recorded while positive or negative corona ions

were deposited onto the dielectric surface. The sheet resistance as a function of surface charge density is plotted in symbols in Figure 5-8. As described in Section 5.3.1, an error bar of 3.5% is included in charge density in Figure 5-8 to account for the variation in corona charge density [149]. Figure 5-9 shows the sheet resistance of an A2 sample measured 25 times upon corona discharge for up to 160 s in both polarities, corresponding to charge densities ranging from -1.1×10^{13} to 8.7×10^{12} cm^{-2}. Each data point was taken after a re-positioning of the sample to take into account the error introduced by sample handling. The standard deviation was calculated from the last 20 points to eliminate the transient effects that arise from the application of an eddy current to the sample causing a change in defect occupation [150]. This resulted in an error of 0.02-0.05%. An error bar of 0.05% is included in the wafer sheet resistance in Figure 5-8. In the numerical model, wafer resistivity and N_{it} were varied so that the simulated curves (solid lines in Figure 5-8) fit the experimental data. Since $D_{it-midgap}$ has been shown to have a minor effect on the resistance, $D_{it-midgap}$ was set to 3×10^{10} $eV^{-1}cm^{-2}$ in all simulations in this subsection. This value was obtained from the characterisation in Section 4.3 on A2 specimens. The parameters extracted from the fits are summarised in Table 5-2. The resulting interface state density profiles are plotted in Figure 5-8.e for A2 specimens and Figure 5-8.f for A4 specimens. The extracted N_{it} for n-type A2 specimens is 2.94×10^{12} cm^{-2} near the conduction band edge and 1.2×10^{12} cm^{-2} near the valence band edge. The extracted N_{it} for p-type A4 specimens is 2.24×10^{12} cm^{-2} near the conduction band edge and 1.2×10^{12} cm^{-2} near the valence band edge. It is noted that no significant difference is observed in N_{it} near both band edges between the n-type and the p-type sample sets. Another point to note is that for both sample sets, N_{it-acc} is larger than N_{it-don}. The dashed lines in Figure 5-8 were simulated as a reference to show the accuracy of the method, including curves with a deviation of $\pm 8.4 \times 10^{11}$ cm^{-2} for N_{it-acc} and $\pm 7.2 \times 10^{11}$ cm-

^{2} for N_{it-don}. Such deviation in N_{it} represents an increase in the mean squared error of the fits by 1.2-2.1-fold, suggesting that the quoted values of N_{it} extracted from the solid lines are of sufficient accuracy.

Table 5-2 Summary of parameters extracted from the fits of the experimental wafer sheet resistance-charge density relations for A2 and A4 specimens.

	n-Si Figure 5-8.a	n-Si Figure 5-8.c	p-Si Figure 5-8.b	p-Si Figure 5-8.d
Base Resistivity ($\Omega\cdot$cm)	1.021	1.0172	0.855	0.846
D_{it-CB} (10^{14} eV^{-1}cm^{-2})	1.05		0.8	
N_{it-acc} (10^{12} cm^{-2})	2.94		2.24	
D_{it-VB} (10^{14} eV^{-1}cm^{-2})		0.5		0.5
N_{it-don} (10^{12} cm^{-2})		1.2		1.2
Mean Squared Error (10^{-3})	6.7	1.6	8.5	0.6

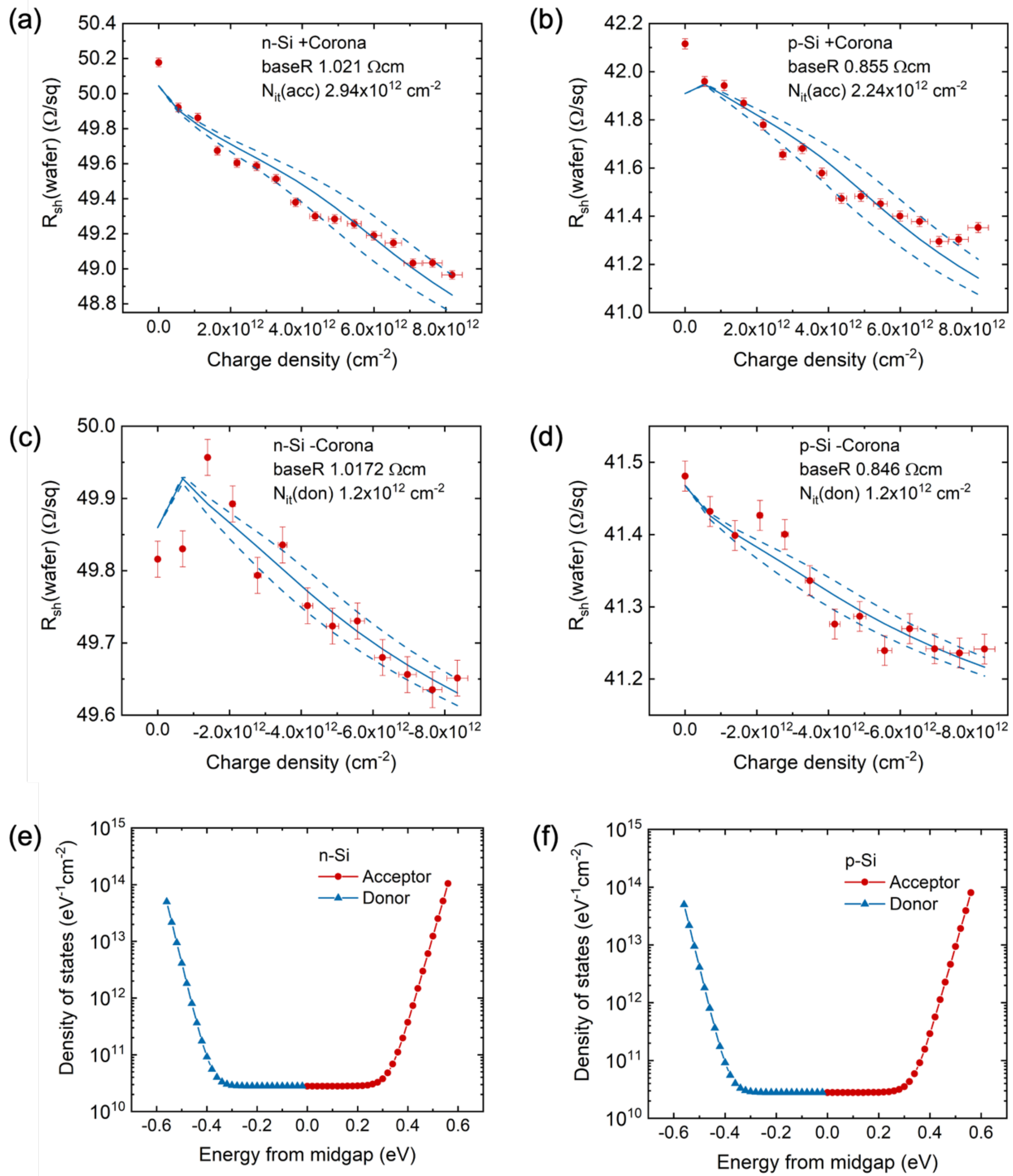

Figure 5-8 Simulated (lines) and experimental (symbols) wafer sheet resistance as a function of corona charge density of an (a), (c) n-type A2 specimen, and a (b), (d), p-type A4 specimen. Extracted D_{it} profile across the Si bandgap of (e) n-type A2 specimens, and (f) p-type A4 specimens.

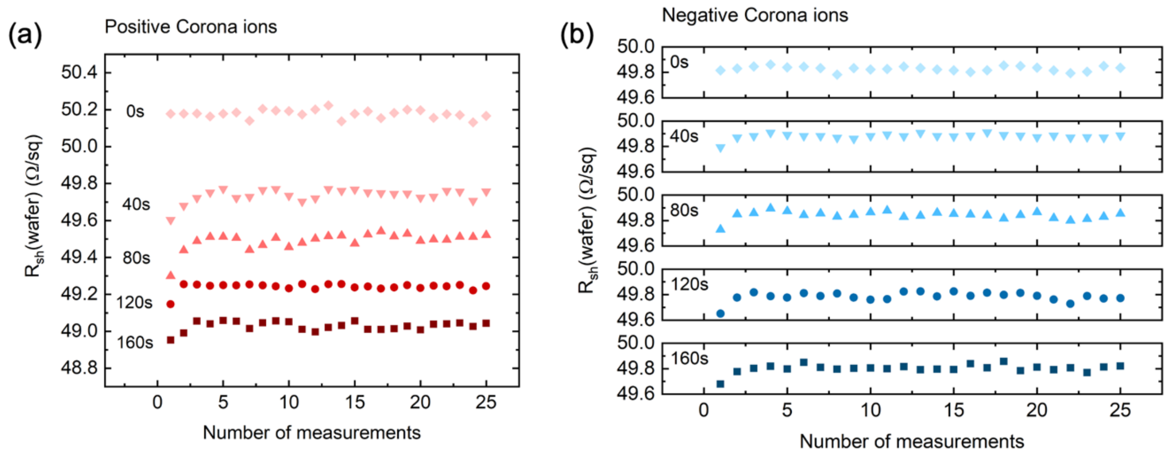

Figure 5-9 Sheet resistance of an A2 n-type specimen measured multiple times upon deposition of corona ions on a single side for up to 160 s in both polarities.

5.3.3 Summary

In this section, the characterisation method was tested on four sample sets. The Van der Pauw method and inductively coupled measurements were used to monitor the resistance. Both methods are effective for sheet resistance measurements. For the Van der Pauw method, metal contacts are required. With the sample geometry used in this thesis, only $N_{it\text{-}acc}$ was characterised in the accumulation regime. The characterisation of $N_{it\text{-}don}$ in the inversion regime has been shown to be possible, provided additional local doping is conducted. For the inductively coupled measurements, the sample preparation is simple with no metal contact required. The conductivity in both the field-induced inversion/accumulation layer and the substrate contribute to the measured conductance, allowing N_{it} near both band edges to be characterised. Base resistivity, $D_{it\text{-}CB}$, and $D_{it\text{-}VB}$ were adjusted in the numerical model to enable accurate characterisation of N_{it}. In terms of the interface states, the results suggest that (i) the difference in oxide thickness, oxidation temperature, and FGA anneal does not lead to a significant change in band-tail interface state density, (ii) $N_{it\text{-}acc}$ appears to be larger

than N_{it-don}, and (iii) the dopant type in the substrate does not result in an evident difference in N_{it}.

5.4 Significance of the Method in Predicting Performance of PERC

Chapter 4 showed that a low band-tail interface state density is required to obtain a low emitter sheet resistance in IL cells. Apart from IL cells, there are other devices and techniques where surface carrier concentration plays an important role [151]–[156]. In this section, the performance of PERC was simulated as an example to demonstrate the benefit of passivating the band-tail interface states. Figure 5-10.a shows a schematic of a model of PERC developed in Sentaurus TCAD. The parameters of the model are listed in Table 5-3. An equal density of positive/negative charge (5×10^{12} cm^{-2}) was defined at the front/rear surface of the cell, respectively, to account for field-effect passivation provided by surface dielectrics. The charge can lead to a reduced minority carrier concentration near the interface and thus less carrier recombination. With lower band-tail interface state density, there will be fewer majority carriers trapped at the interface and thus lower minority carrier density due to the mass-action law. Passivating the band-tail interface states should therefore enhance field-effect passivation and lead to less interface recombination. Figure 5-10.b shows the simulated IV curves with N_{it} varied by two orders of magnitude, which presents a difference in efficiency by 0.1% absolute. Methods to passivate the band-tail interface states are to be investigated to achieve this level of improvement, which requires the aid of interface characterisation tools such as the method demonstrated in this chapter.

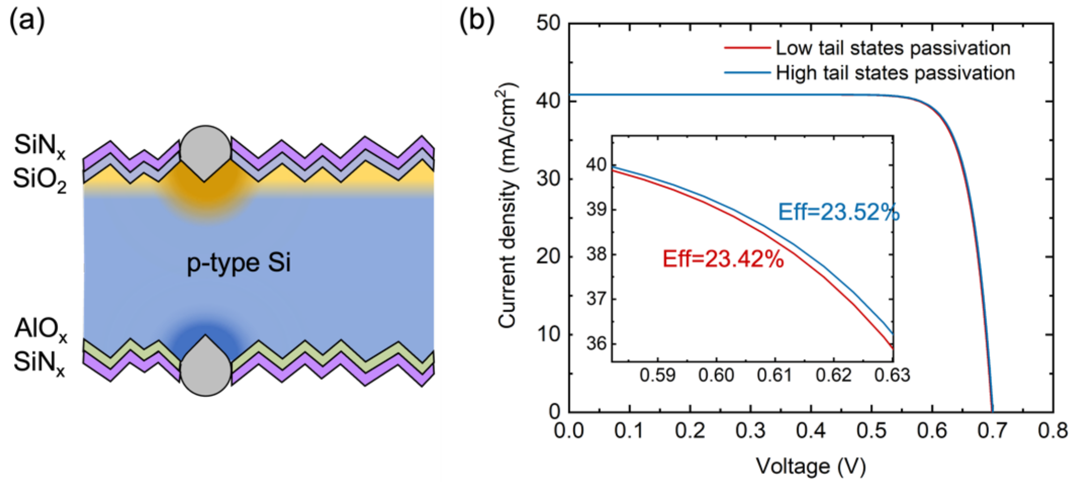

Figure 5-10 (a) Schematic of a model of PERC. (b) Simulated IV curves of PERC with 5×10^{12} cm^{-2} of positive/negative charge defined at the front/rear surface for field-effect passivation at different levels of band-tail interface state density.

Table 5-3 Summary of parameters used for simulations of PERC in Sentaurus TCAD.

Parameter	**Value**
Cell thickness	170 μm
Bulk base resistivity	p-type, 2 Ω·cm
SRH bulk lifetime	τ_n = 2 ms, τ_p = 20 ms
Finger width	25 μm
Finger spacing	1.4 mm
$D_{it\text{-}midgap}$	10^{11} eV^{-1}cm^{-2}
$D_{it\text{-}CB}$ (red)	5×10^{15} eV^{-1}cm^{-2}
$D_{it\text{-}CB}$ (blue)	5×10^{13} eV^{-1}cm^{-2}
Grid resistance	0 Ω
Contact resistance (front)	2×10^{-3} Ω·cm^2
Contact resistance (rear)	5×10^{-3} Ω·cm^2

5.5 Discussion

Chapter 4 concluded that a low band-tail interface state density is essential in achieving a low sheet resistance in field-induced layers. Methods to passivate the band-tail interface states should hence be investigated in the future. The characterisation tool developed in this chapter can be used to determine the effectiveness of any passivation method. Apart from IL cells, this method can lead to a deeper insight into the interfacial properties of various

optoelectronic devices, especially in techniques where manipulating surface carrier concentration is important. This includes the use of field-effect passivation to minimise recombination in commercial PERC devices [152]–[154]. In the TOPCon structure, it is demonstrated that heavy doping in the poly-silicon layer can enhance conductivity and reduce recombination at the passivating contact [155], [156]. Recent work has also shown that in the TOPCon structure, further field-effect passivation can be attained via charge in the tunnelling oxide [151]. The detection of band-tail interface state density is necessary for understanding and manipulating carrier distribution at the interface. It can point to new directions for the improvement of devices involving field effect.

In terms of interface characterisation tools, capacitive (CV) techniques are reliable for the detection of state density at the mid-gap while lacking sensitivity on the states at the band tails [34], [157]. Surface photovoltage (SPV) can be used to acquire state density across the whole bandgap but with compromised accuracy at the band tails where the state density varies significantly in terms of energy [34]. Electron paramagnetic resonance (EPR) spectroscopy is capable of detecting the states that are paramagnetic, for example, silicon dangling bonds at the Si/SiO_2 interface [17] and the Si/SiN_x interface [158]. These correspond to the states at mid-gap rather than at the band tails [33]. No technique has yet been developed that can quantify the band-tail interface states with high sensitivity. The method developed in this chapter fills this gap in interface characterisation tools.

The method I developed uses the resistance dependence of silicon substrates on surface charge density as a reference. It extracts the interface parameters from numerical simulations. Two resistance measurement techniques were used in this thesis: the Van der Pauw method and inductively coupled measurements. The ICM is a non-contact technique and measures the conductivity in both the field-induced layer and the substrate. This leads to simple

sample preparation and the capability of characterising both N_{it-acc} and N_{it-don} on the same sample set. Although the Van der Pauw method requires metal contact and additional local doping to measure the inversion layer, this method applies to complicated multi-layer structures. For the Van der Pauw method, free carriers only within the contacted layer contribute to the conductivity, while in ICM conductivity from all layers on the sample structure contribute to the measured sheet conductance.

In this method, the final N_{it} is determined by adjusting the base resistivity and interface parameters in the computer model. This indicates that the accuracy of N_{it} obtained from this method depends heavily on the model used. Therefore, the parameterisation of the interface states should be chosen carefully for the interface studied. A tested model to describe the carrier mobility and carrier density in field-induced layers for dopant densities commonly used in PV devices is also necessary. Additionally, it is noted that this method is only applicable to specimens with a planar surface. For samples with a textured surface, the current path within the field-induced layer and thus the calculation of resistance is more complicated due to the additional surface area. The correlation between surface charge density, interface parameters, and resistance is to be studied to develop a model for specimens with a textured surface.

Figure 5-11 shows a comparison between band-tail interface state densities of silicon-thermal oxide interfaces measured in this work and those reported in the literature [27], [33], [36], [38]–[40]. In the figure, N_{it-acc} and N_{it-don} extracted from this work are lower than that reported in the literature. The silicon substrates, oxidation process, hydrogenation process and interface characterisation techniques used in this work and the literature are listed in Table 5-4. Band-tail interface states are known to be consequences of stretched Si-Si bonds in the silicon lattice near the surface [36]. The discrepancy in N_{it} obtained may result from

the difference between (100) and (111) surfaces, errors in the characterisation techniques used, and differences in surface treatments, such as oxidation temperature, annealing, and hydrogenation. Further characterisation on the same sample sets should be carried out to compare SPV, CV, and the technique developed in this work.

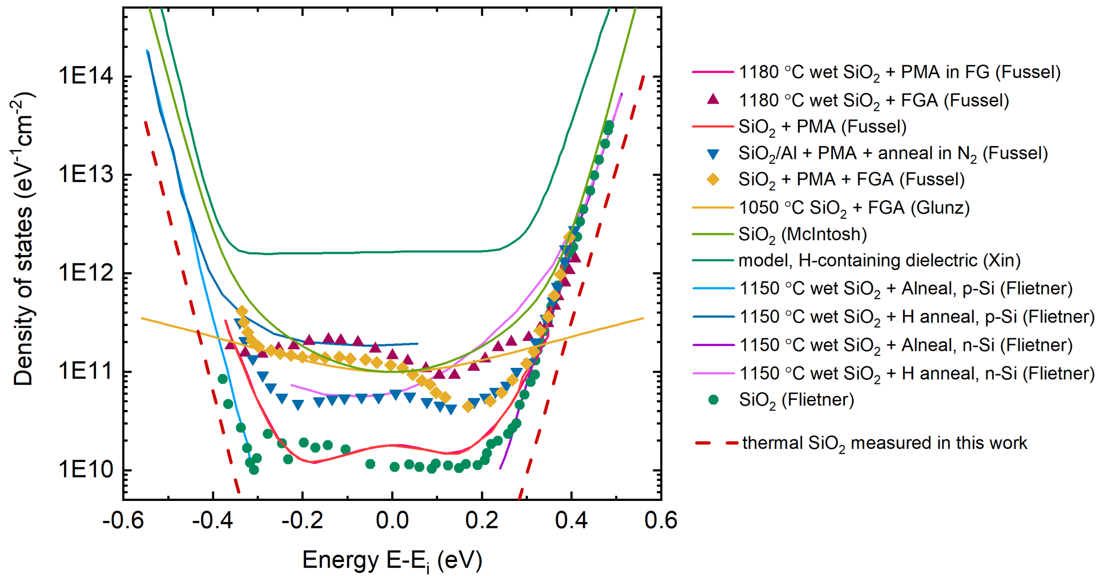

Figure 5-11 Comparison between band-tail interface state densities of Si-SiO_2 interfaces measured in this work and those reported in the literature [27], [33], [36], [38]–[40].

Table 5-4 Silicon substrates, oxidation process, hydrogenation process, and techniques used for characterising Si-SiO_2 interfaces in this work and the literature.

Silicon substrate	Surface	Silicon oxide	Hydrogenation	Characterisation	Citation
FZ, 1 Ω·cm, n/p-Si	(100)	Thermal oxide, 1050 °C, 100 nm		ICM + simulations	This work
FZ, 4.6-5.4 Ω·cm, n-Si	(100)	Thermal oxide, 950 °C, 20 nm + 70 nm TiO_2	FGA	CV	McIntosh [39]
10 Ω·cm, n-Si	(111)	Thermal oxide, 1180 °C	FGA	SPV	Füssel [36]
n/p-Si	(111)	Thermal oxide, 1150 °C, 100 nm	FGA		Flietner [33]
n/p-Si	(111)	Thermal oxide, 1150 °C, 100 nm	Alneal		Flietner [33]
10 Ω·cm, n-Si	(100)	Thermal oxide		CV	Flietner [27]

It has been concluded that a low band-tail interface state density benefits the conductivity of field-induced emitters in IL cells. The Si-SiO_2 interface characterised from A1 to A4 specimens shows that the difference in oxidation temperature and enhanced chemical passivation does not lead to a significant change in band-tail interface states. This suggests that the nature of these states must be better understood to explore methods to passivate them.

5.6 Summary

An easy and accurate method to characterise band-tail interface states was developed. It was demonstrated by simulations that mid-gap interface states have a minor impact on the sheet resistance of field-induced charge layers. Band-tail interface states were found to have a significant effect on both the resistance of the field-induced layers and its dependence on surface charge density. The response of the resistance to surface charge density was used as a reference to characterise the band-tail interface states. The characterisation requires (i) a method to introduce a controlled amount of surface charge, (ii) accurate monitoring of the sheet resistance, and (iii) a model that reflects the physics of carrier density and mobility in silicon. A corona discharge rig with calibrated deposition rate was used to introduce the surface charge. Both the Van der Pauw method and ICM were used to monitor the resistance. The Sentaurus model developed in Chapter 4 was used to generate simulated R_{sh}-Q relations to fit the experimental data. The method was tested on both n-type and p-type samples with their surfaces passivated differently. The characterisation technique has been shown to allow sensitive detection of band-tail interface states, which complements existing interface characterisation techniques to provide a more detailed analysis of the interface.

Chapter 6 Development of Inversion Layer Cells

It was demonstrated in Chapter 4 that dielectric charge densities in the order of 10^{13} cm^{-2} have been achieved using the ion migration method. This is the highest dielectric charge density reported in the literature [72], [73], [75], [77], [86], [87] in the research field of inversion layer cells. The simulation results in Chapter 4 showed that for well-passivated surfaces, the emitter sheet conductance plateaus for charge densities above 2×10^{13} cm^{-2}. This suggests that with optimised processing, the ion-migration method may be able to provide the highest sheet conductance possible in a field-induced emitter. In this chapter, the ion migration method was used to incorporate positive K^+ ions into oxide thin films to produce field-induced emitters. Proof-of-concept inversion layer cells were fabricated on Set B samples via laser doping, ion migration, and light-assisted electroplating. The performance of the cells was characterised and evaluated. The difficulties in the fabrication procedure and future strategies to resolve them are also included in this chapter.

6.1 Inversion Layer Cells Fabrication

The proof-of-concept inversion layer cells were fabricated on Set B samples, which comprise 180 μm thick, 1 Ω·cm p-type boron-doped silicon substrates. These substrates have pyramid-textured surfaces for light trapping. The surface was passivated by 20 or

100 nm thermal silicon oxide. The effective lifetime of the specimens is ~50 µs. The rear metallisation was established by laser opening and full-area screen printing of aluminium paste followed by firing. Figure 6-1 shows a schematic of the procedure that Set B samples underwent to fabricate IL cells. It includes laser doping, ion migration, and light-assisted electroplating. As explained in Section 4.1, local doping underneath the metal contact is necessary to ensure the electrical connection of the field-induced emitter to the external circuit. Laser doping was used to both ablate the silicon oxide and counter-dope the region underneath the contacts to n-type. After that, positive K^+ ions were incorporated into the oxide thin film using the ion migration method to induce the emitter. Finally, light-assisted electroplating was used to deposit a nickel grid onto the laser-doped region for front metallisation. The details of each fabrication step and the sample characterisation will be described in the following sections.

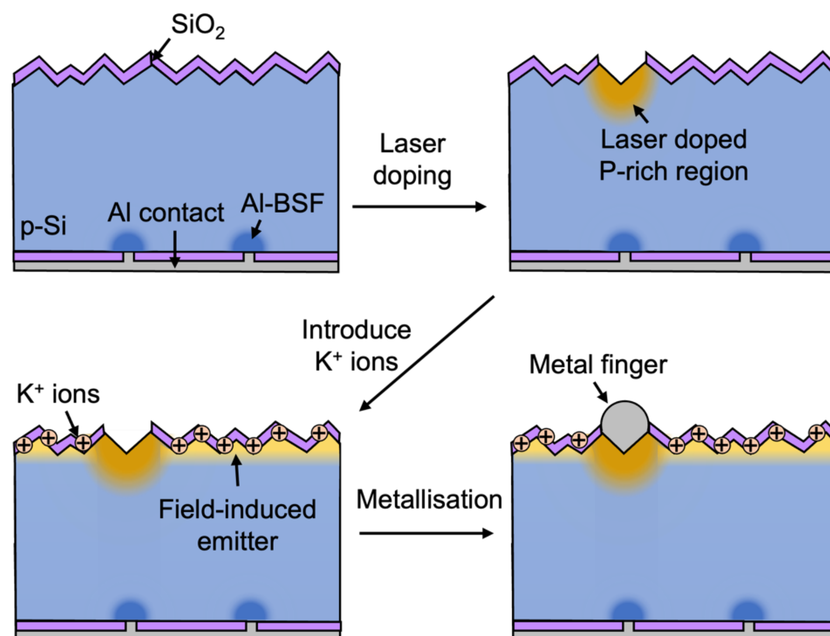

Figure 6-1 Fabrication procedure for a proof-of-concept inversion layer cell.

6.2 Laser Doping

Laser doping comprises two steps: (i) delivery of a dopant precursor onto the sample surface, and (ii) lasing the sample surface to ablate the dielectric material and dope the region underneath. An 85% phosphoric acid solution was spin-coated onto the sample surface as the dopant precursor. One 355 nm nanosecond pulsed laser and one continuous wave, 532 nm, 20 W laser were used for laser doping. Two difficulties were encountered in the laser doping process with both lasers used in this work. The first is that a wider region in the oxide thin film was ablated, which I termed parasitic ablation in this thesis. The second is that the oxide adjacent to the laser-doped region was found to be damaged such that no inversion layer was formed in the region underneath. This will cause an interruption in the n-type emitter layer. The laser-induced damage, the hypothesises to explain the cause, and methods to mitigate the damage are introduced in this section.

6.2.1 Parasitic Ablation

The 355 nm laser was used for laser doping on B1 samples. The 355 nm laser is a pulsed laser. Each pulse leads to ablation and melting in a circular region, termed laser spot here. Firstly, the laser parameters were adjusted on a B1 sample with no phosphoric acid coating. The pulse length was adjusted to achieve the smallest laser spots possible while maintaining the homogeneity of the spot size. The frequency and speed of the laser were adjusted so that the laser spots overlap and form a continuous line. The optimal operation was given by a scan speed of 400 mm/s with the frequency set to 60 kHz and the pulse length set to 0.13 µs. The working distance between the laser and the sample was subsequently adjusted so that the width of the laser-ablated line was the thinnest when the laser was completely in focus at the sample surface. Figure 6-2.a shows an optical micrograph of the laser-ablated line

with the lowest line width, which is about 20 μm. No value of working distance is reported since it was adjusted empirically using a z-axis micro-translator. The same laser parameters and working distance were used for laser doping. An 85% phosphoric acid solution was spin-coated onto the sample surface at 8000 rpm for 50 s prior to lasing. Figure 6-2.b shows an image of the laser-doped line. It is evident that apart from the 20 μm wide laser-doped line, the oxide thin film of 100 μm on each side of the region was removed or ablated. The hypothesis is that the focal point of the laser beam was shifted downwards by the phosphoric acid coating (refractive index = 1.43). This leads to the sample surface being out of focus and thus an enlarged spot size. Figure 6-2.c shows a schematic of the light path. The laser doping and simultaneous side damage can be explained by the widened laser beam at the surface and the overlapping of laser spots. An example of the overlapping is illustrated in Figure 6-2.d. During the laser doping process, for the samples with phosphoric acid coating, the laser beam will be shifted and result in the oxide being removed in a large area. The phosphoric acid coating will be removed during this process and hence will not affect the light path of the laser in the subsequent pulses. The subsequent pulses will generate the 20 μm feature. This effect is termed parasitic ablation in this thesis.

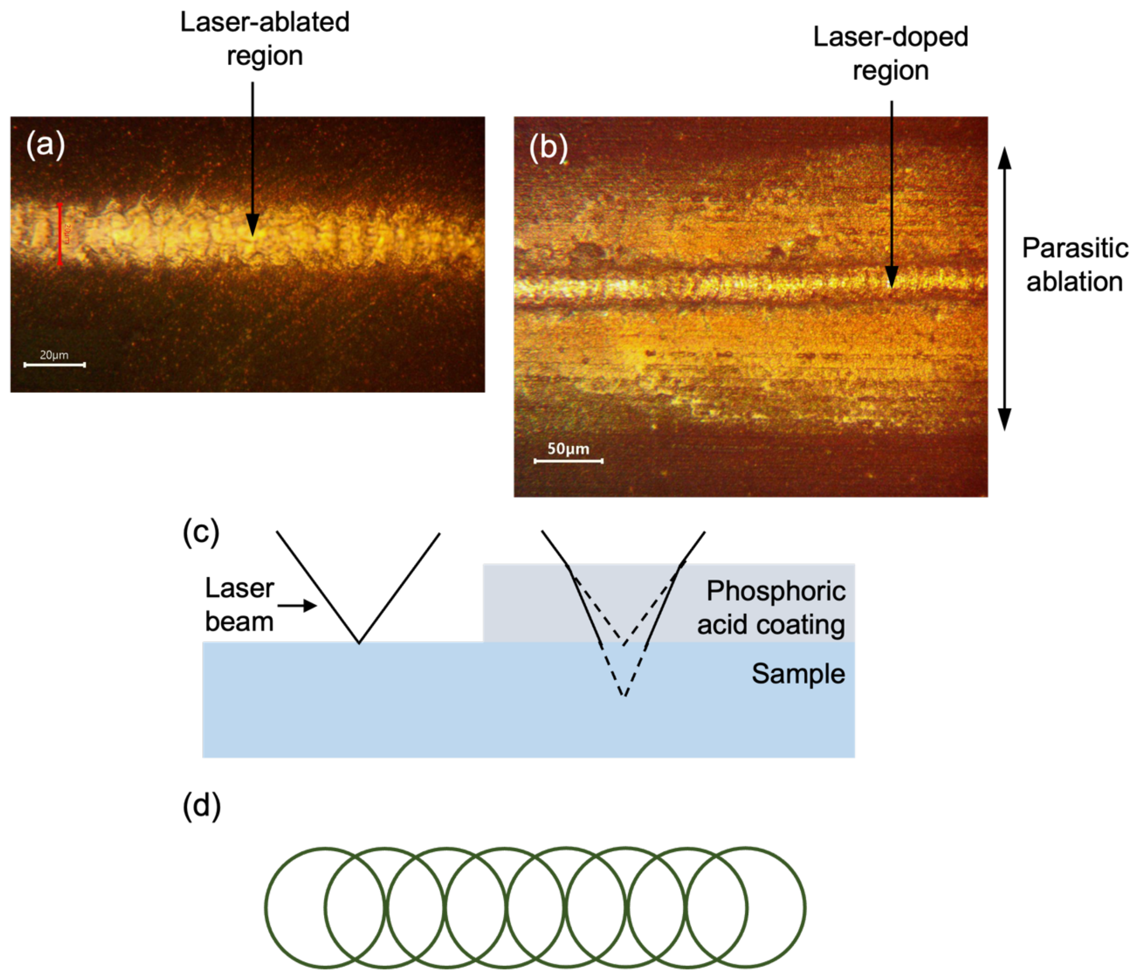

Figure 6-2 Optical micrographs of laser-ablated lines on B1 specimens (a) without and (b) with phosphoric acid coating. Schematic of (c) light path for laser doping and (d) overlapping of laser spots by multiple laser pulses.

Two strategies were adopted to minimise parasitic ablation. The first is to adjust the working distance, such that the spot size in the two scenarios with and without the presence of the phosphoric acid coating coincides, or the fluence in one scenario is sufficiently low and damage to the dielectric layer is negligible. Figure 6-3.a-g shows optical micrographs of the laser-doped lines with varied working distances. Evident parasitic ablation can be observed in Figure 6-3.a-c, while the extent of the damage is alleviated with increased working distance. No parasitic ablation is observed in Figure 6-3.d-g. However, at large working distances, intermittent regions appear where the laser fluence was insufficient to ablate the

dielectric material. This may result from the instability of the laser power. The laser-doped line in Figure 6-3.d shows no evident parasitic ablation while maintaining continuous ablation and melting. The working distance used in Figure 6-3.d is the optimised value for the sample and the ion precursor used. The width of the laser-doped line is 36 μm.

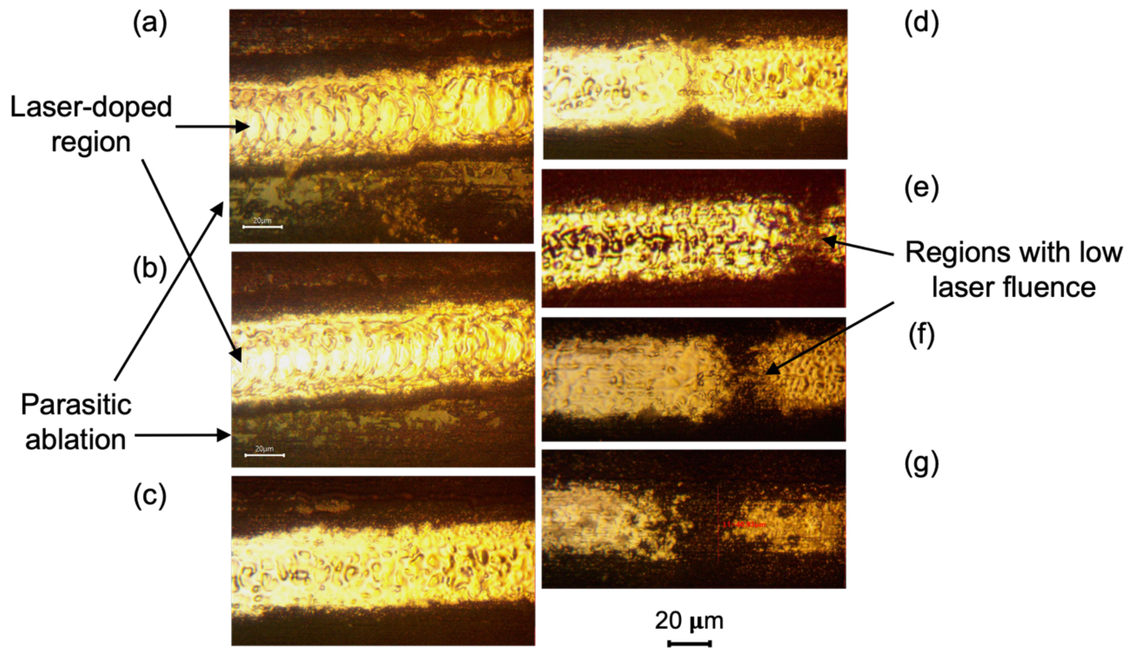

Figure 6-3 Optical micrographs of laser-doped lines with varied working distances. The working distance increases from a to g.

The second strategy is to reduce the thickness of the phosphoric acid coating, such that the difference in the spot size in the two scenarios with and without the phosphoric acid coating is less prominent. This is accomplished by increasing the speed during spin coating. Figure 6-4 shows optical micrographs of the laser-doped lines with varied spin speeds. The working distance was adjusted for minimum parasitic ablation for each spin speed. In Figure 6-4, multiple laser-doped lines were overlapped with a line distance of 30 μm to form a wide laser-doped region as a busbar. In the figure, more prominent parasitic ablation is observed in the marked red boxes beside the busbars than beside the single laser-doped lines. The hypothesis is that the laser beam in one of the two scenarios with or without the phosphoric

acid coating is de-focused and the fluence is not sufficient to cause parasitic ablation in a single laser pass. However, while multiple laser-doped lines were overlapped to form a busbar, the marked region beside the busbar was exposed to the de-focused laser beam multiple times. The accumulated laser fluence led to the removal of the oxide. The region beside the busbar can thus be used to determine the effectiveness of thinning down the phosphoric acid coating. Figure 6-4 shows that the extent of parasitic ablation is mitigated with increased spin speed. No evident parasitic ablation is observed for the spin speed of 12000 rpm. The 12000-rpm spin speed and the working distance optimised for it were used for later experiments. Although no parasitic ablation is observed under the optical microscope, the de-focused laser beam may affect the surface passivation and compromise the final cell efficiency. Further optimisation of the laser doping process should be carried out in future work to minimise laser-induced damage to the passivating dielectric.

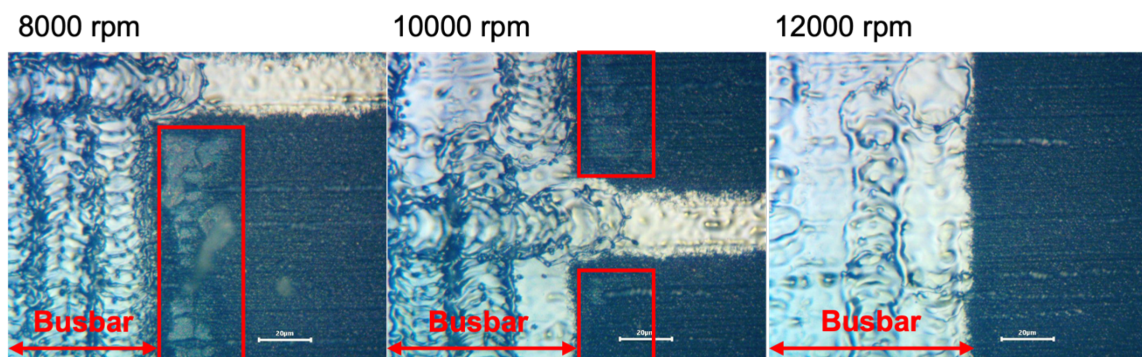

Figure 6-4 Optical micrographs of laser-doped lines with varied spin speeds.

6.2.2 Interruption of Inversion Layer

The second difficulty encountered is the interruption of the inversion layer. The laser doping process has been previously found to damage the dielectric material adjacent to the laser-doped region [73]. Figure 6-5 shows a schematic of this effect. The damage prevents the formation of the inversion region underneath the dielectric adjacent to the contacts, resulting

in an interruption of the n-type emitter layer. This effect was confirmed in this thesis by taking IV measurements between two adjacent laser-doped lines while depositing positive corona ions onto the dielectric surface. B2 samples were used in this experiment. An 85% phosphoric acid solution was spin-coated onto the sample surface at 8000 rpm for 50 s. The 532 nm laser was used for laser doping at the speed of 2 m/s with two laser passes. Positive corona ions (30 kV) were deposited onto the sample surface to induce an inversion layer. With no inversion layer formed, the IV curve between two adjacent laser-doped lines should show the features of an *npn* junction, i.e., high emitter-collector resistance. Upon the formation of the inversion layer, a complete n-type emitter layer should lead to a change in IV curve and a reduction in resistance. Figure 6-6.a shows the IV curves measured while positive corona ions were deposited onto the sample surface incrementally for up to 120 s of corona discharge time. The IV curves present the feature of an *npn* junction, and the resistance remains unchanged throughout the experiment, indicating the interruption of the n-type emitter layer. Several damage mechanisms can be involved, including (i) the damage to surface passivation during heating and cooling in the laser doping process due to the thermal mismatch between silicon and silicon oxide, (ii) the formation of amorphous silicon after the laser-melted region recrystallises, and (iii) the change in phosphorus doping efficiency through the amorphous-crystalline interface. In this work, the samples were annealed after laser doping to improve the doping efficiency at the edge of the laser-doped region, and to allow bond regeneration at the Si-SiO_2 interface. Figure 6-6.b shows the IV curves of a specimen annealed at 400 °C for 30 min. A decrease in resistance was observed from the IV curves after 10 s of corona discharge, indicating the formation of a complete n-type emitter layer. These results confirm the impact of the laser-induced damage and that the damage can be partially recovered upon annealing.

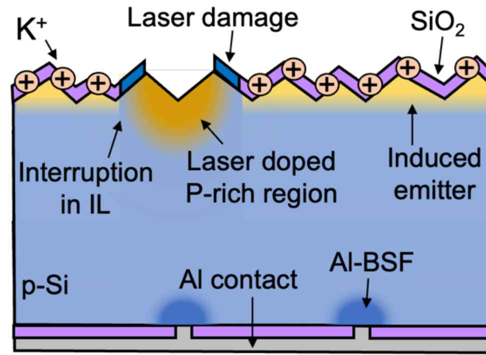

Figure 6-5 Schematic of an inversion layer cell in which the n-type inversion layer is interrupted due to laser-induced damage.

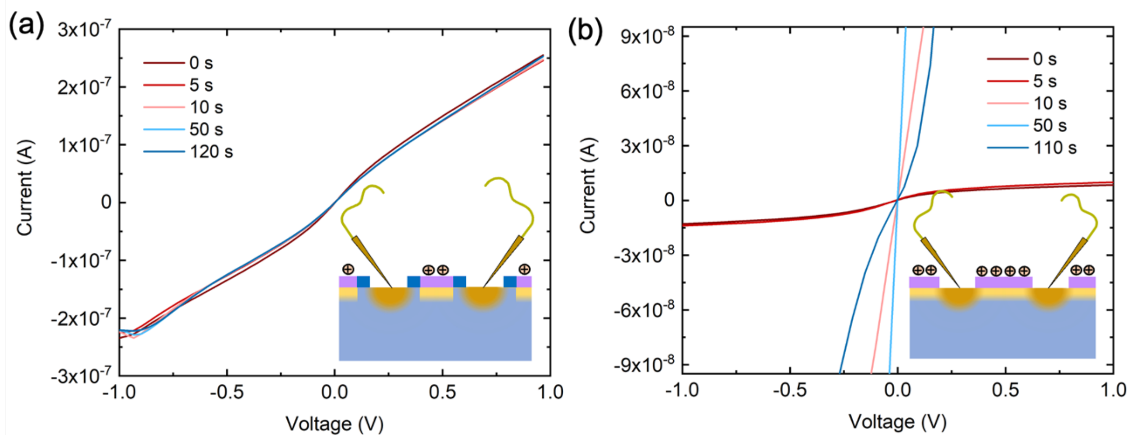

Figure 6-6 IV curves between two adjacent laser-doped lines on B2 specimens with varying amounts of corona charge deposited onto the sample surface (a) after laser doping, and (b) after annealing at 400 °C for 30 min.

The thermal budget required to recover the laser-induced damage was tested for both the 532 nm laser on B2 samples and the 355 nm laser on B1 samples. Suns-V_{OC} was measured at the laser-doped region as a function of annealing time and was used to demonstrate the recovery of the damage. Since no ionic charge was incorporated into the dielectric in these samples, no IL emitter was induced, and the voltage measured originated only from the *pn* junction formed between the n-type laser-doped region and the p-type substrate. The increase in Suns-V_{OC} upon annealing may result from (i) the formation of an oxide layer at the surface of the laser-doped region, (ii) the regeneration of bonds at the Si-SiO_2 interface

in the laser-damaged region, and (iii) enhanced doping efficiency. Although the increase in Suns-V_{OC} does not exclusively come from the recovery of the damage, the condition where Suns-V_{OC} plateaus with annealing time represents the largest extent of recovery that can be obtained using this method. Figure 6-7.a and Figure 6-7.b show the laser doping patterns used for the two sample sets. The recorded Suns-V_{OC} is plotted in Figure 6-7.c and Figure 6-7.d. For B2 samples laser-doped using the 532 nm laser, Suns-V_{OC} plateaus at 30 min with an annealing temperature of 430 °C. For B1 samples laser-doped using the 355 nm laser, a higher thermal budget is required (560 °C for 1 hour) for Suns-V_{OC} to plateau. Possible explanations for this distinction in damage are related to the laser-Si interaction. The 532 nm laser is continuous wave while the 355 nm laser has a pulsed beam. The absorption coefficient of the 355 nm laser in crystalline silicon is higher than that of the 532 nm laser. Therefore, the ablation, melting, and recrystallisation should happen at a shallower region for the 355 nm laser. The difference in the thermal budget required to recover the damage for the two lasers may result from the difference between a continuous wave laser and a pulsed laser, and the location of the induced damage. Another point to note is the difference in the maximum Suns-V_{OC} obtained, which is 580 mV for B2 samples and 525 mV for B1 samples. This may result from the different extents of laser-induced damage and recovery. In the fabrication of inversion layer cells in this work, to ensure complete n-type emitter layers, prior to ion migration, samples laser-doped using the 532 nm laser were annealed at 430 °C for 30 min and samples laser-doped using the 355 nm laser were annealed at 560 °C for 1 hour.

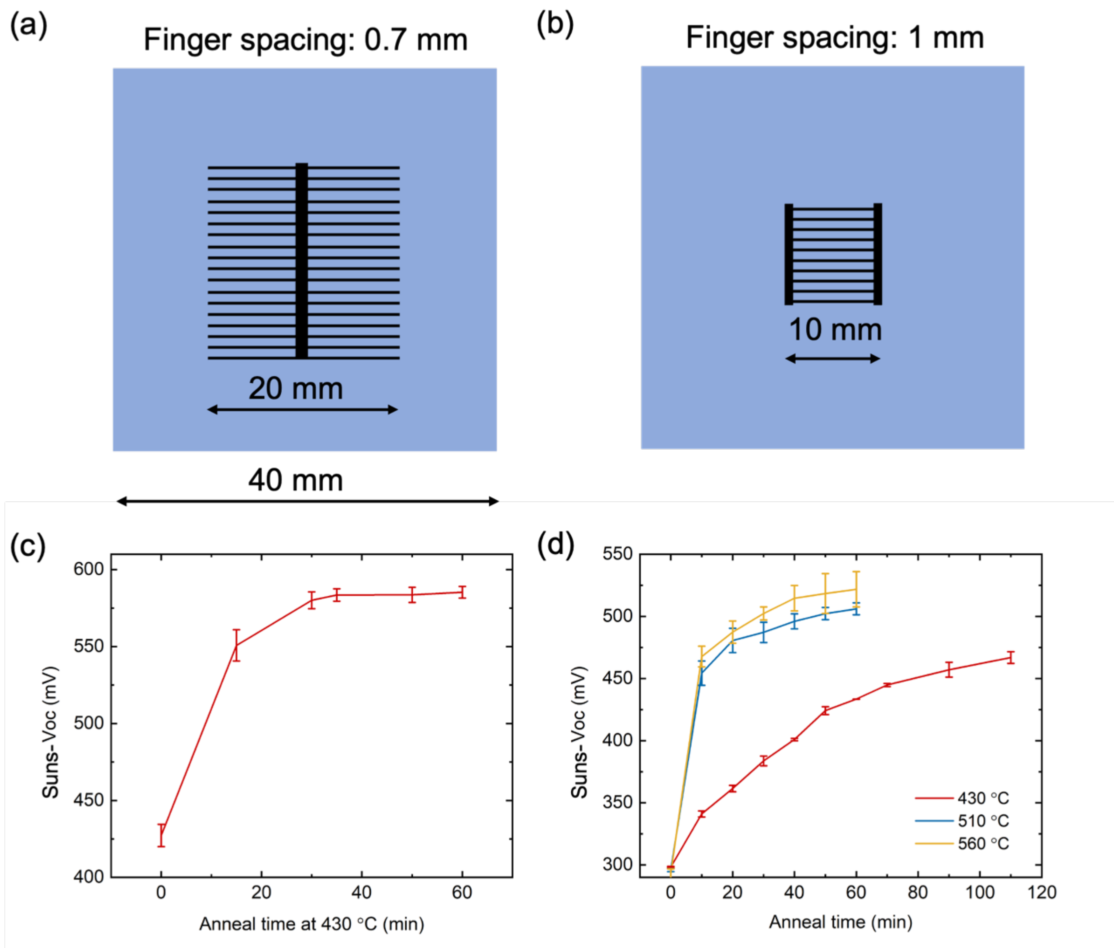

Figure 6-7 Laser doping patterns for (a) B2 specimens using the 532 nm laser, and (b) B1 specimens using the 355 nm laser. Recorded Suns-V_{OC} of (c) B2 specimens annealed at 430 °C, and (d) B1 specimens annealed at 430 °C, 510 °C, and 560 °C after laser doping.

6.2.3 Summary

Two difficulties were encountered in the laser doping process: parasitic ablation and interruption of the inversion layer. The parasitic ablation is caused by the shift of the focal point by the phosphoric acid coating. It can be alleviated by adjusting the working distance and reducing the thickness of the coating. The laser doping process was also shown to damage the dielectric material adjacent to the laser-doped line. This results in the interruption of the inversion layer underneath and thus poor contact between the laser-doped region and the field-induced emitter. Annealing has been demonstrated to be capable of

partially recovering the laser-induced damage and ensuring complete n-type emitter layers. The laser parameters and annealing conditions corresponding to the least parasitic ablation and the highest Suns-V_{OC} were found and used to fabricate inversion layer cells as explored in the following sections.

6.3 Unmetallised Inversion Layer Precursor Cell

After laser doping and annealing, positive K^+ ions were incorporated into the oxide thin film to fabricate inversion layer precursor cells on set B samples. The 5×10^{-3} mol/L KCl solution (concentration B) was spin-coated onto the sample surface at 3000 rpm for 30 s. The K^+ ions were driven into the oxide thin film by 8 corona discharge (30 kV, 30 s)-anneal (430 °C, 10 s) cycles. The ionic charge density obtained after one spin coating was characterised in Section 4.3 to a value of approximately 9.6×10^{12} cm^{-2}. The spin coating and the subsequent corona discharge-anneal cycles were repeated 4 times to ensure a sufficiently high dielectric charge density. Assuming that the repetition of the ion migration process would lead to an equivalent increase of the charge density each time, the final charge density will be ~3.8×10^{13} cm^{-2}. It is noted that this is unlikely to be the case as the interface concentration could saturate and prevent the migration of further K^+ ions. According to the simulation results in Chapter 4, charge densities in the order of 10^{13} cm^{-2} are sufficient for the emitter sheet conductance to plateau. The formation and uniformity of the field-induced emitter were monitored using Suns-V_{OC} and LBIC.

The laser doping pattern shown in Figure 6-7.a was used for B2 samples. The samples were annealed at 430 °C for 30 min for the laser-induced damage to recover. Both the annealing and the ion migration process were monitored using Suns-V_{OC}. Figure 6-8 shows the recorded Suns-V_{OC} of two B2 samples. During the first 30 min of annealing, Suns-V_{OC}

increased by 150-160 mV from 420 mV to 570-580 mV and plateaued. The subsequent data points reflect the formation of the IL emitter. Each colour change represents a replenishment of the ion precursor by spin coating of the KCl solution. Each data point was obtained after two corona-anneal cycles. Multiple points plotted were measured by placing the probe at different positions on the busbar. The variability is reflected by the error bars in the plots. Suns-V_{OC} was boosted by 10-20 mV at the first point taken during the ion migration process, indicating the appearance of the field-induced emitter and the complete electrical path from the inversion layer to the busbar. Suns-V_{OC} plateaus after the drive-in of the K^+ ions delivered by the first spin coating. Little increase is observed while more K^+ ions were incorporated into the oxide thin film. This indicates that the carrier collection at the *pn* junction is not limited by dielectric charge density. In Figure 6-8.b, the final Suns-V_{OC} obtained is ~604 mV. Taking into account the dimension and the geometry of the cell, and the lack of gettering or hydrogenation in the bulk, 604 mV is considered high. Figure 6-8.b also shows that the Suns-V_{OC} measured 4 months after processing is higher, with a further increase detected after a short anneal. This agrees with the findings reported in Chapter 4 where the accumulation layer sheet resistance was found to reduce 1 month after ion migration. This effect can be explained by the decay of hot carriers as per the explanation introduced in Chapter 4. Figure 6-9 shows LBIC images of one inversion layer precursor cell and one control sample with no ionic charge incorporated. In Figure 6-9.a, the regions with low photocurrent represent the laser-doped fingers. The high photocurrent between the fingers indicates the uniform formation of the field-induced emitter. This also demonstrates that the electrical path from the field-induced emitter to the laser-doped busbar, which is where the probe is placed, is not interrupted by the laser-induced damage. Figure 6-9.b shows the LBIC image around a laser-doped finger in higher magnification. The reduced

photocurrent within ~10 μm from the laser-doped line illustrates that carrier collection is affected by laser damage adjacent to the laser-doped fingers. Figure 6-9.c shows the LBIC image of the control sample with no ionic charge incorporated. The large blue area with low photocurrent between the fingers indicates the absence of an emitter. The photocurrent generated in the red area near the laser-doped lines comes from the *pn* junction formed between the n-type laser-doped region and the p-type silicon substrate. Although the *pn* junction also exists at the laser-doped lines, low photocurrent is observed in these regions. This can be explained by the high density of recombination sites in the laser-doped region after recrystallisation and un-passivated surfaces. The Suns-V_{OC} and LBIC results demonstrate the uniform formation of a field-induced emitter and its uninterrupted electrical path to the laser-doped fingers.

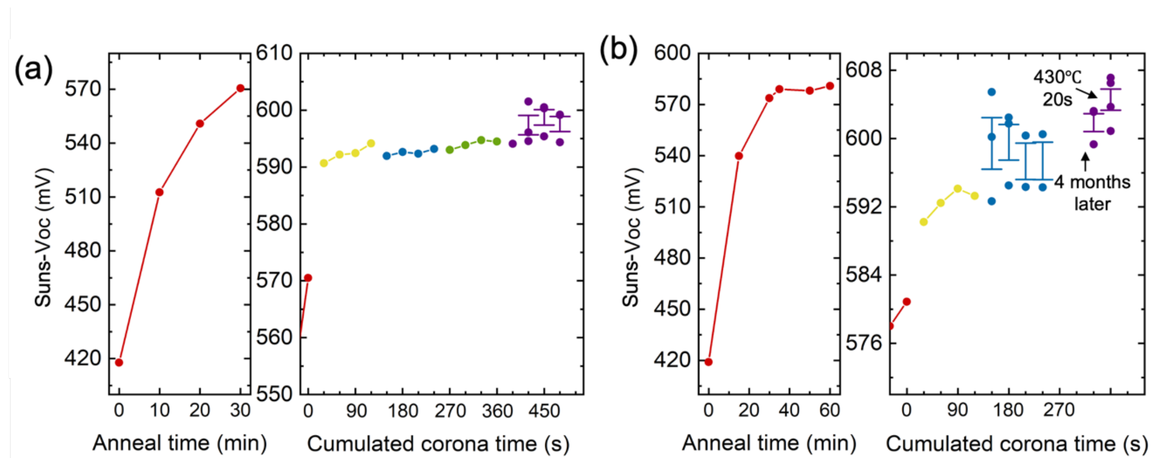

Figure 6-8 Recorded Suns-V_{OC} of two B2 specimens, which were annealed at 430 °C, followed by spin coating of the KCl solution and corona-anneal cycles to incorporate positive K^+ ions into the oxide thin film.

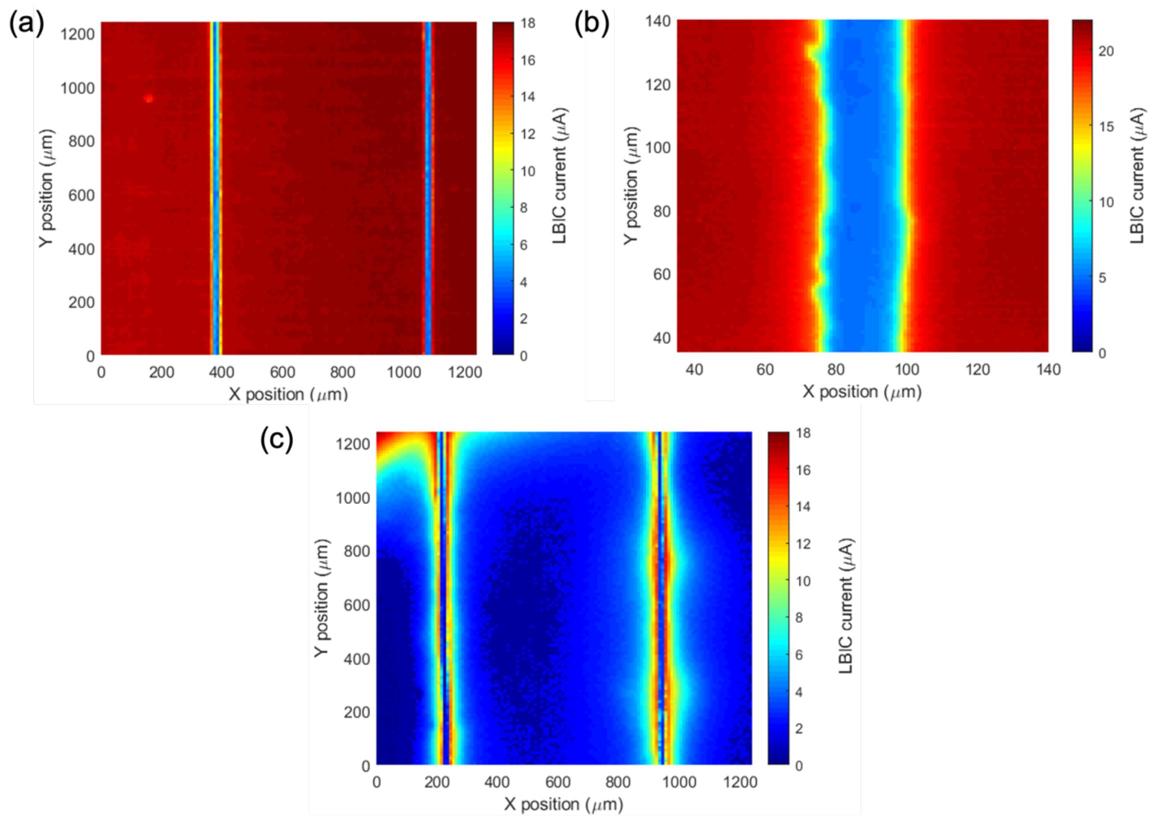

Figure 6-9 Map of LBIC current collected from (a) an inversion layer precursor cell, (b) the precursor cell in higher magnification, and (c) a control sample with no ionic charge incorporated.

For B1 samples, the 355 nm laser was used for laser doping. Figure 6-10 shows the optical micrographs of laser-doped lines with single and double laser passes. The line width is less homogeneous for the laser-doped line with a single laser pass. This may be due to the irregularity in laser power. This effect can be compensated by running the laser over the same region by multiple times. The laser-doped line with double laser passes shows improved homogeneity in line width. The laser doping pattern is shown in Figure 6-7.b. The samples were annealed at 560 °C for 1 hour for the laser-induced damage to recover. Suns-V_{OC} of the precursor cells with both single and double laser passes was recorded and is plotted in Figure 6-11. Similar to Figure 6-8, Suns-V_{OC} in both cases was boosted upon formation of the field-induced emitter and shows a minor change with further incorporation of K^+ ions. The results show that specimens with double laser passes present higher Suns-

V_{OC} than those with a single laser pass. The difference may come from the absence of under-doped inhomogeneous regions shown in Figure 6-10, and a change in the phosphorus doping profile by an additional laser pass. These results demonstrated the formation of IL emitters and their electrical connection to the laser-doped lines for B1 samples. B1 precursor cells were used in the following experiments to fabricate proof-of-concept inversion layer cells.

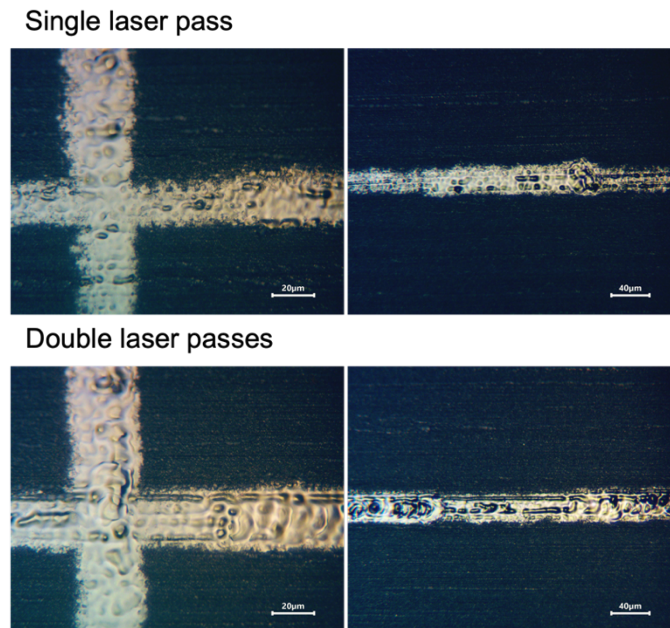

Figure 6-10 Optical micrographs of laser-doped lines with single and double laser passes.

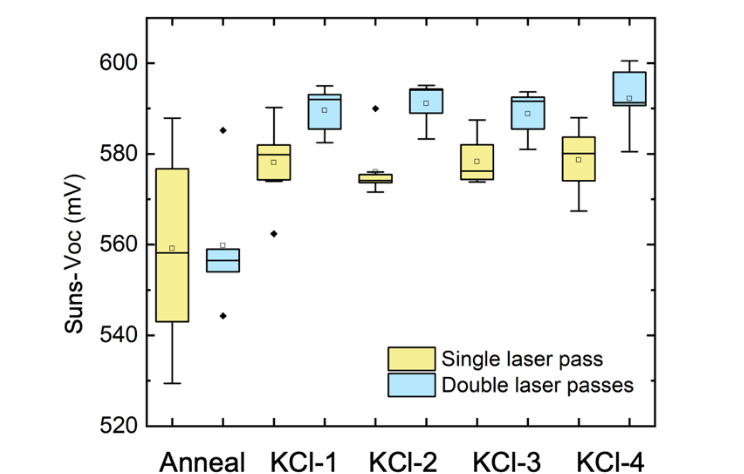

Figure 6-11 Recorded Suns-V_{OC} of B1 specimens, which were annealed at 560 °C for 1 hour, followed by spin coating of the KCl solution and corona-anneal cycles to incorporate positive K^+ ions into the oxide thin film.

6.4 Light-Assisted Electroplating

During laser doping, the dielectric material was ablated off so that bare silicon was exposed in the laser-doped regions. This allows self-aligned metallisation via electroplating. In this work, a processing sequence was developed to achieve light-induced electroplating of nickel fingers on B1 precursor cells for front metallisation. Electroplating was performed after junction formation such that photo-generated carriers collected by the emitter can contribute to the plating current. Before electroplating, silicon oxide in the laser-doped regions formed during laser doping and annealing was removed by applying a 1% HF solution to the front surface for 30 s. The samples were then mounted onto an electroplating rig as described in Chapter 3. A ready-for-use commercial nickel sulfamate solution was used as the electrolyte. A nickel wire was used as the anode. The sample and the electrolyte were heated to ~52 °C. A voltage of 1.1 V was applied between the anode and the precursor cell for 4 min to form the nickel grid. Figure 6-12 shows the optical micrographs of the sample prior to and after electroplating. The laser-doped line is 25 µm-wide, while the nickel finger is 50 µm-wide. The excessive finger width will lead to high shading losses. Figure 6-13 shows the SEM images of the cross-section of the nickel finger. The fingers are 2-6 µm thick. The low aspect ratio will lead to high grid resistance. The excessive finger width and low aspect ratio are a result of the not optimised electroplating process. Further optimisation is required for reduced shading losses and resistive losses.

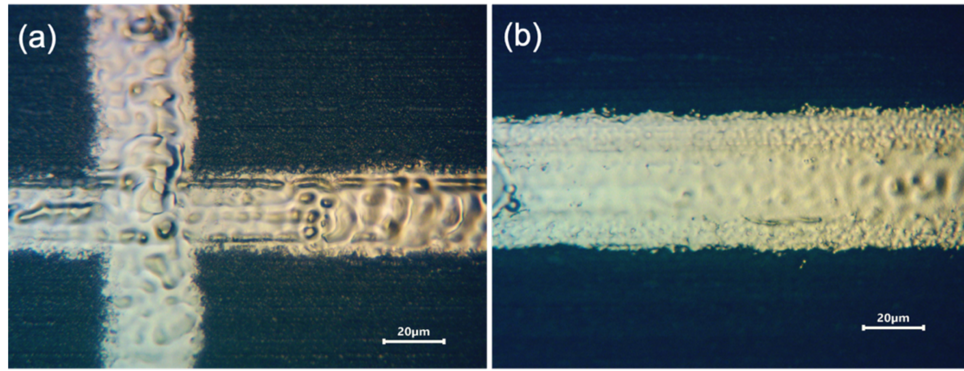

Figure 6-12 Optical micrographs of (a) a laser-doped line and (b) a nickel finger after light-assisted electroplating.

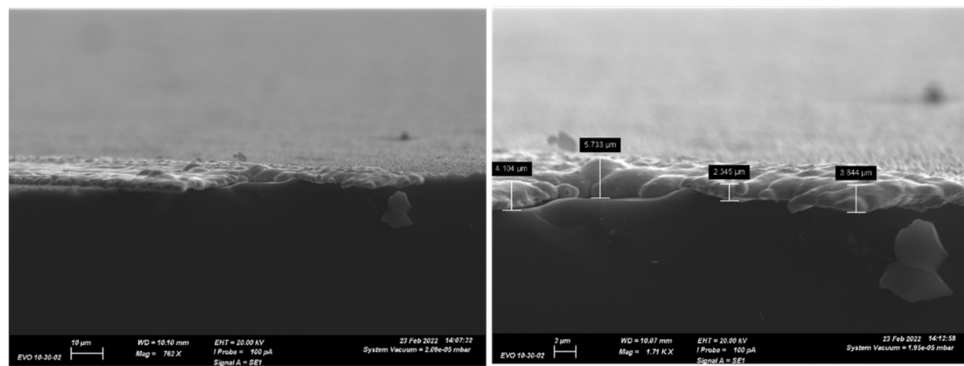

Figure 6-13 SEM images of the cross-section of electroplated nickel fingers.

6.5 Performance of Proof-of-Concept Inversion Layer Cells

Proof-of-concept inversion layer cells were fabricated on B1 specimens. Their performance was assessed using LBIC and IV characteristics. Figure 6-14.a shows an LBIC image of a 500 × 500 μm^2 area of the cell. The blue low-photocurrent region (3-5 μA) in the middle represents the nickel finger, which is ~80 μm in width. The variation of the finger width from what is shown in Figure 6-12 is due to the inhomogeneity of the electroplated nickel fingers. The large area with a high photocurrent (13-14 μA) represents the field-induced emitter. The reduced photocurrent (11-13 μA) in the regions adjacent to the nickel finger is due to the recombination sites introduced by the laser-induced damage. In addition to the features also observed in the precursor cell shown in Figure 6-9, discrete dots with a

relatively low photocurrent of 10-12 μA can be seen in the emitter region. This feature comes from the electroplating process, during which the voltage applied may cause a breakdown of the dielectric layer and plating at unwanted areas. I term this phenomenon parasitic plating. This suggests the necessity of optimising the passivating layer stack and the metallisation process. Figure 6-14.b shows the IV curve of the champion cell. The inset in Figure 6-14.b is the laser doping pattern. Instead of using a wide busbar as illustrated in Figure 6-7.b, the fingers are connected by single laser-doped lines, so that the laser-induced damage and the metal-silicon contact area with high recombination are reduced. The IV curve shows a V_{OC} of 559 mV, a J_{SC} of 33.9 mA/cm^2, and an efficiency of 10.8%. Although the efficiency of 10.8% is low, the results demonstrate that the inversion layer cells can be fabricated using the ion migration method. It is also noted that this is the first silicon solar cell fully produced in the Oxford Materials laboratories. All prior work had only investigated the formation of ion-charged oxide layers, but this work takes a step forward by exploiting such layers to realise a complete device architecture.

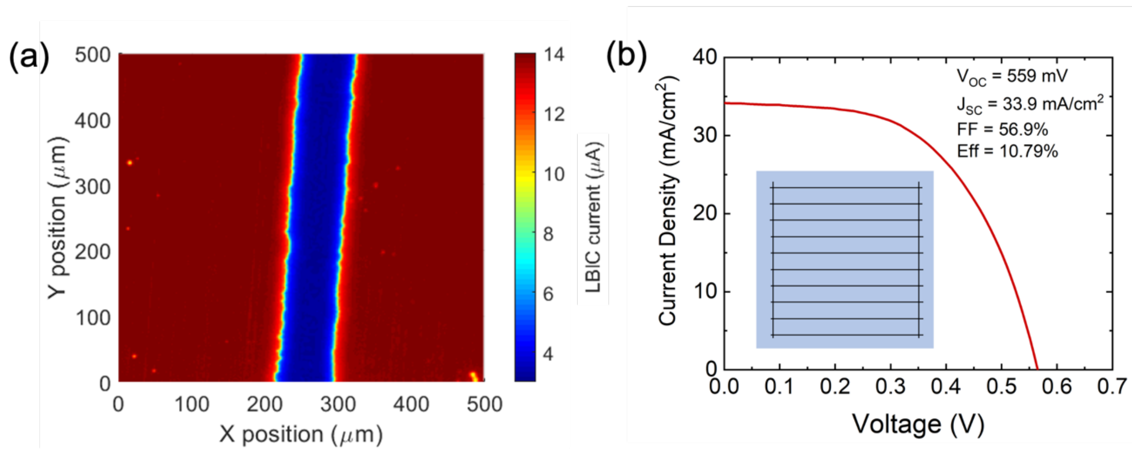

Figure 6-14 (a) LBIC photocurrent map of an inversion layer cell. (b) IV curve of the champion inversion layer cell with a 10.8% efficiency.

Table 6-1 shows a summary of the fabrication procedure of the proof-of-concept inversion layer cells. Several aspects of the fabrication procedure can be improved for better cell performance. V_{OC} can be improved by reducing carrier recombination via (i) optimising the laser doping process for minimum laser-induced damage, (ii) introducing atomic hydrogen for enhanced chemical passivation on both the front and the rear surfaces, (iii) using high-resistivity silicon substrates with ms-level lifetimes, (iv) replacing the rear PERC-like structure with passivating contacts, and (v) utilisation of large wafers for reduced impact of edge recombination. J_{SC} can be improved by (i) addition of a SiN_x layer for anti-reflection coating, (ii) optimising the electroplating process for thinner metal fingers and lower shading losses, and (iii) optimising texturing and rear reflector for reduced optical losses. To obtain a higher fill factor, the aspect ratio of the metal fingers needs to be improved for reduced grid resistance. The Ni-Si contact can be annealed to form a nickel silicide alloy for reduced contact resistance. Furthermore, a Ni/Cu/Ag structure can be used for metallisation for both high grid conductance and to prevent the grid from oxidation. These are existing technologies that are well-studied and already implemented in the industry [89], [91], [159]–[162], which implies immediate improvements in cell performance are possible. Although a low efficiency of only 10.8% was obtained for the proof-of-concept inversion layer cell, the efficiency potential of such cell design will be evaluated via device simulations in Chapter 7.

Table 6-1 Summary of the fabrication procedure of proof-of-concept inversion layer cells.

Process	Parameters
Starting material	B1 specimens
Spin coating	85% phosphoric acid solution spin-coated at 12000 rpm for 50 s
Laser doping	355 nm laser, 400 mm/s scan speed, 0.17 μs pulse width, 60 kHz frequency
Anneal	560 °C, 1 hour
Ion migration	4 spin coating of a 5 × 10^{-3} mol/L KCl solution at 3000 rpm for 30 s with each followed by 8 corona discharge (30 kV, 30 s)-anneal (430 °C, 10 s) cycles
Remove oxide in laser-doped area	1% HF, 30 s
Light-assisted electroplating	1.1 V, 4 min, 52 °C

6.6 Stability Test

The stability of B1 precursor cells was monitored against an elevated temperature and UV irradiation for 2 months. For B1 precursor cells, double laser passes were used for laser doping. The laser doping pattern is shown in Figure 6-7.b. The cell performance was monitored by taking Suns-V_{OC} measurements throughout the 2-month period. Figure 6-15 shows the recorded Suns-V_{OC} of three sample sets. After the drive-in of the K^+ ions, one sample set was kept in a box furnace at 120 °C, one sample set was kept under UV irradiation, and a control sample set was kept in the dark at room temperature for comparison. In all three sample sets, it is observed that Suns-V_{OC} decreased with the amount of K^+ ions incorporated into the oxide thin film. This agrees with the finding reported in Chapter 4 where surface passivation is shown to be damaged upon accumulation of K^+ ions near the interface. Methods to introduce atomic hydrogen are to be tested for improved surface

passivation. Upon keeping the samples at 120 °C, under UV irradiation, and at the control condition, a reduction in Suns-V_{OC} ranging from 3 to 8 mV is observed for all three sample sets within 7 days. The variations afterwards are not significant enough to show any further degradation. Since similar trends are observed in all three sample sets in Figure 6-15, it is concluded that the degradation in Suns-V_{OC} triggered, or accelerated at an elevated temperature or under UV irradiation is minor in the 2-month period.

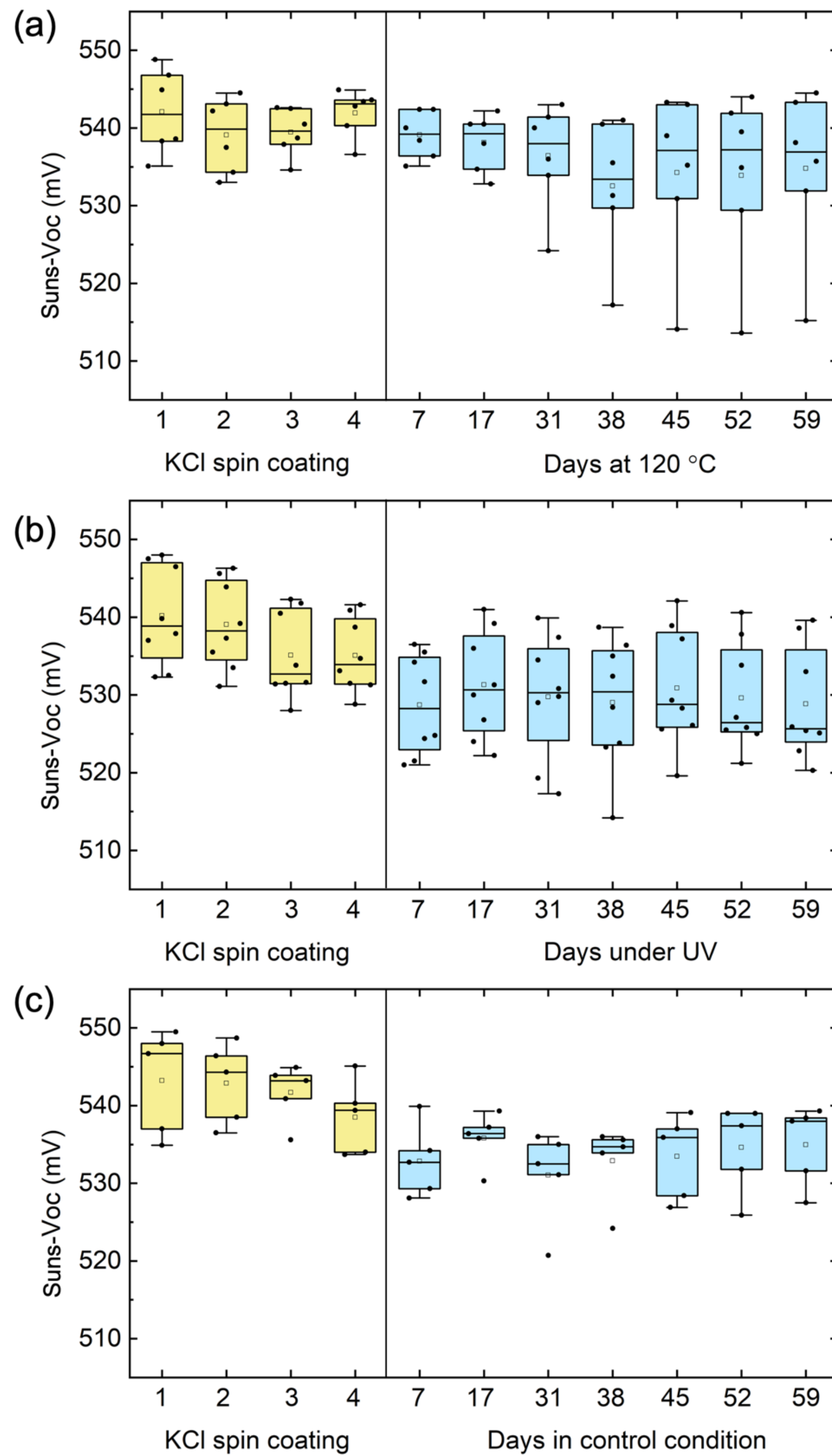

Figure 6-15 Recorded Suns-V_{OC} of inversion layer precursor cells kept (a) at 120 °C, (b) under UV irradiance, and (c) at room temperature in the dark for 2 months.

6.7 Discussion

In this chapter, the formation and uniformity of the field-induced emitters were confirmed. Chapter 1 introduced the advantages of field-induced emitters over diffused emitters, including less carrier recombination and lower fabrication cost. Table 6-2 lists the time and temperature of each processing step used to fabricate the proof-of-concept inversion layer cells in this thesis. Apart from the anneal at 560 °C for 1 hour, all other steps can be accomplished within minutes or seconds at temperatures below 500 °C. It has been demonstrated in Section 6.3 that for the 532 nm laser, an anneal at 430 °C for 30 min is sufficient for the laser-induced damage to recover. The thermal budget can be further reduced by optimising the laser doping process so that the damage is mitigated. Compared with the thermal budget required to fabricate P-diffused emitters (800-900 °C for ~60 min [56]), the fast and low-temperature processes to fabricate field-induced emitters can lead to lower fabrication costs. With potentially lower LCOE and minor performance degradation observed for the proof-of-concept inversion layer cells in this thesis, field-induced emitters can become competitive in commercial applications.

Proof-of-concept inversion layer cells were fabricated on B1 specimens with a procedure of laser doping, annealing, ion migration, and light-assisted electroplating. While the intrinsic charge in dielectric materials was used to induce the inversion layer in the literature [72]–[75], [77], [86], [87], Chapter 4 showed that ionic charge densities in the order of 10^{13} cm^{-2} have been achieved using the ion migration method. This is the highest demonstrated in the field of inversion layer cells [1]–[6] and should result in an improvement in cell efficiency. However, the champion inversion layer cell fabricated in this work presented a low efficiency of 10.8%. Apart from the already-mentioned improvements to be carried out in the fabrication procedure, the laser doping pattern and the ionic charge density can be further

optimised. For a set finger width, increasing the finger spacing will lead to an increase in resistive losses in the emitter and reduced shading losses. The optimum finger spacing can be determined with the aid of simulations. In terms of the ionic charge density, it was shown in Chapter 4 that the accumulation of K^+ ions at the interface damages the surface passivation, while a high charge density is required to obtain a high emitter sheet conductance. This trade-off should be considered while determining the optimum ionic charge density. The fabrication procedure designed in this work is limited by the specimens and fabrication tools available. The efficiency potential of inversion layer cells will be evaluated via device simulations in Chapter 7.

Table 6-2 Time and temperature of each processing step used to fabricate proof-of-concept inversion layer cells.

Process	Time	Temperature
Spin coating of phosphoric acid	1 min	Room temperature
Lasing	< 1 min	Room temperature
Anneal	1 hour	560 °C
Spin coating of KCl solution	< 1 min	Room temperature
Corona discharge	30 s for each cycle	Room temperature
Short anneal	10 s for each cycle	430 °C
Remove oxide in laser-doped area	30 s	Room temperature
Light-assisted nickel electroplating	< 5 min	40-56 °C

A phosphoric acid coating (1.7-3.3 µm [105]) was used as a dopant precursor for laser doping. The focal point of the laser beam was shifted by the coating, which caused parasitic ablation. The extent of the shift is determined by the thickness and the refractive index of the coating. In this work, the parasitic ablation was mitigated by adjusting the working

distance and increasing the spin speed for thinner coatings. The damage can be further reduced by implementing ultra-thin n-type dopant precursors. For example, in the fabrication of the selective emitter geometry for P-diffused emitters [61], a ~20 nm PSG layer [163] was used as the source of P atoms. Werner et al. fabricated p-type inversion layers on n-type substrates [73]. In their work, a 20 nm AlO_x layer was used to both induce the inversion layer and as a source of Al atoms. Thin and homogeneous n-type dopant sources are required to avoid severe parasitic ablation.

6.8 Summary

Proof-of-concept inversion layer cells were fabricated on Set B specimens via laser doping, ion migration, and light-assisted electroplating. Two difficulties were encountered for laser doping: parasitic ablation and interruption of the inversion layer. Strategies were adopted to mitigate or recover the damage. Upon incorporating the positive K^+ ions, the formation and uniformity of the field-induced emitter, and its electrical connection to the external circuit were confirmed. Proof-of-concept inversion layer cells were fabricated after front metallisation, with the champion cell presenting a 10.8% efficiency. The characteristics demonstrated that the field-induced emitter can be fabricated using the ion migration method. Although the efficiency is low, it can be significantly improved if the already-developed technologies in surface passivation, laser doping, and metallisation can be integrated into the fabrication procedure. The stability of B1 precursor cells was tested against an elevated temperature and UV irradiation, with minor degradation observed in the 2-month period. This suggests promising applications of the field-induced inversion layer in commercial photovoltaic devices.

Chapter 7 Device Simulations of Inversion Layer Cells

The low emitter sheet conductance has been considered one of the major concerns for IL cells. Chapter 4 demonstrated that the sheet resistance of field-induced emitters is dependent on charge density and band-tail interface state density. It was concluded that with optimised surface passivation and charge density, the emitter sheet resistance could reach values as low as ~1.1 kΩ/sq in the dark. Although the 1.1 kΩ/sq sheet resistance is about 7 times higher than the sheet resistance of a typical P-diffused emitter (150 Ω/sq) [10], whether such emitter still limits the IL cell performance must be evaluated by full device simulations. A proof-of-concept inversion layer cell with an efficiency of 10.8% was fabricated in Chapter 6. The low efficiency is expected since each processing step is yet to be optimised. This chapter studies the highest efficiency possible for IL cells and the pathways to achieve it.

7.1 Model Development

The simulations used a full device model in Sentaurus TCAD [132]. The model was developed based on the inversion layer model introduced in Chapter 4. Figure 7-1 shows a schematic of the model. The model comprises a 170 μm thick, boron-doped silicon substrate with both surfaces passivated by a dielectric layer. The base resistivity was varied from 1 to 10 Ω·cm to reflect its influence on the cell performance. The corresponding bulk lifetime

was set to $\tau_p = 10 \times \tau_n = 3.7$ ms for 1 Ω·cm, as may be reached in Ga-doped wafers if the Fe concentration is sufficiently low, $\tau_p = 10 \times \tau_n = 15$ ms for 5 Ω·cm, and $\tau_p = 131$ ms, $\tau_n = 1.14$ ms for 10 Ω·cm as referred from [52], [162], [164]. For the interface, $D_{it\text{-}midgap}$ was set to 5×10^{10} $eV^{-1}cm^{-2}$, which is typical for high-quality Si-SiO_2 interfaces on (100) surfaces [46]. For the band-tail interface states, $N_{it\text{-}acc}$ and $N_{it\text{-}don}$ were introduced in Chapter 5 to account for the variations in both $E_{0,CB}/E_{0,VB}$ and $D_{it\text{-}CB}/D_{it\text{-}VB}$. In this chapter, $E_{0,CB}$ and $E_{0,VB}$ were set constant. $D_{it\text{-}CB}$ and $D_{it\text{-}VB}$ are the parameters adjusted in the model and are thus used here to describe the band-tail interface states. The band-tail interface state densities characterised from A2 and A4 specimens in Chapter 5 were used here, which are 10^{14} $eV^{-1}cm^{-2}$ and 5×10^{13} $eV^{-1}cm^{-2}$ for $D_{it\text{-}CB}$ and $D_{it\text{-}VB}$, respectively. The dielectric charge was defined at the silicon-dielectric interface. Positive charge was defined at the front interface to induce the inversion layer. A negative charge density of -5×10^{12} cm^{-2} was defined at the rear interface for enhanced field-effect passivation, which is typical for a SiO_2/AlO_x passivating stack [165]. Finger spacing was set the same for the front and the rear metallisation. The finger width was set to 25 μm for front contact since recent progress in metallisation technologies shows that such thin metal fingers are possible using screen printing, or a combination of laser doping and electroplating [160], [161]. The rear finger width was set to 67 μm, which is a typical value used in PERC cells. A local phosphorus doping was implemented underneath the front metal contact so that the n-type inversion layer is electrically connected to the external circuit. A local aluminium doping was implemented underneath the rear contact to resemble Al-BSF for reduced contact resistivity and surface recombination. The phosphorus and aluminium dopant profiles were taken from those measured in commercial cells and are plotted in Figure 7-2 [58]. While a flat surface was defined in the model, the generation profile was acquired from ray tracing using Sunrays

[145] and altered to mimic a pyramid-textured surface with 0.1 μm height under 1-sun illumination. Despite the potential of developing a bifacial cell, in this work, only light injection from the front surface was considered for simplicity. The parameters used in the model are summarised in Table 7-1.

Table 7-1 Summary of parameters used for inversion layer cell simulations in Sentaurus TCAD.

Parameter	Value
Cell thickness	170 μm
Bulk base resistivity	p-type, 1/5/10 Ω·cm
SRH bulk lifetime	1 Ω·cm: τ_n = 0.371 ms, τ_p = 3.71 ms 5 Ω·cm: τ_n = 1.5 ms, τ_p = 15 ms 10 Ω·cm: τ_n = 1.14 ms, τ_p = 131 ms
Rear dielectric charge density	-5×10^{12} cm^{-2}
Front finger width	25 μm
Rear finger width	67 μm
Finger spacing	0.8-1.8 mm
SRV at front contacts	$S_n = 10^7$ cm/s, $S_p = 10^7$ cm/s
SRV at rear contacts	$S_n = 4 \times 10^4$ cm/s, $S_p = 10^7$ cm/s
Front contact resistivity	2 mΩ·cm^2
Rear contact resistivity	5 mΩ·cm^2
$D_{it\text{-}midgap}$	5×10^{10}-10^{11} eV^{-1}cm^{-2}
$D_{it\text{-}CB}$	10^{13}-10^{15} eV^{-1}cm^{-2}
$D_{it\text{-}VB}$	10^{13}-5×10^{14} eV^{-1}cm^{-2}

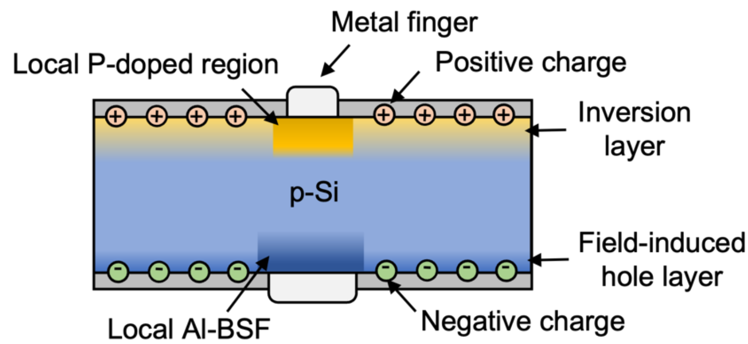

Figure 7-1 Schematic of the inversion layer cell model (not to scale).

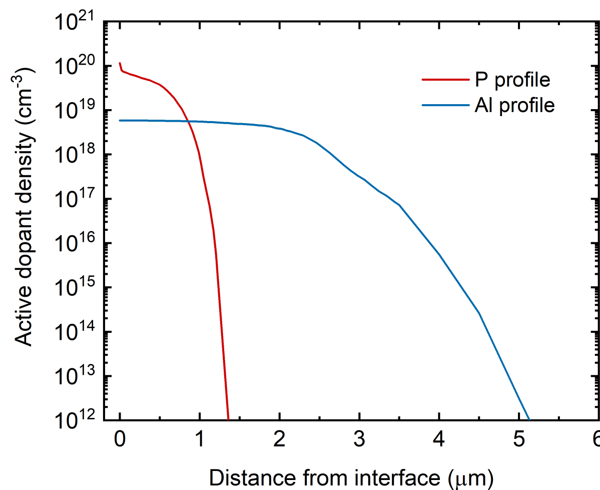

Figure 7-2 Phosphorus and aluminium doping profiles in the local doping region beneath the front and the rear metallisation, respectively [58].

7.2 Efficiency Potential of Inversion Layer Cells

In this section, the performance of IL cells was simulated. The impact of charge density, band-tail interface state density, base resistivity, finger spacing and finger width on the IL cell performance was investigated. The results can guide the fabrication of IL cells and point to directions for further optimisation of the cell design.

Figure 7-3 shows the simulated IL cell efficiency as a function of charge density and finger spacing. The substrate resistivity was set to 1/5/10 Ω·cm. The simulation results show that

(i) cells with higher base resistivities present higher efficiencies, (ii) the efficiency peak shifts from < 0.8 mm finger spacing for 1 Ω·cm substrates to 1.4-1.6 mm for 5 and 10 Ω·cm substrates, and (iii) the efficiency increase with charge density is significant for 1 Ω·cm substrates but is less evident for 5 and 10 Ω·cm substrates. These can be explained by the difference in substrate resistivity and higher bulk lifetimes defined in the model for more resistive substrates. For 5 and 10 Ω·cm substrates with higher bulk lifetimes, there will be less carrier recombination in the device, resulting in higher cell efficiencies. The peak in the efficiency vs. finger spacing curves occurs when the performance gain due to reduced shading losses is outweighed by the increased resistive losses in the IL emitter for larger finger spacings. The efficiency peak shifting from < 0.8 mm for the 1 Ω·cm substrates to 1.4-1.6 mm for the 5/10 Ω·cm substrates indicates the formation of a more conductive emitter, which implies lower resistive losses. One possible explanation for the increased emitter sheet conductance is that the initial hole density is low for high-resistivity substrates. The concentration of field-induced electrons required to compensate and eventually invert the region into n-type for high-resistivity substrates is low, leaving a high proportion of free electrons contributing to the emitter sheet conductance. However, the simulation results in Section 4.2.2 showed that the dark emitter sheet conductance for 1/5/10 Ω·cm substrates coincides at charge densities above 10^{13} cm^{-2}, suggesting that the difference in base resistivity is not the main cause. Another explanation is the difference in bulk lifetime. The bulk lifetime of 5/10 Ω·cm substrates is higher than that of 1 Ω·cm substrates. With a higher bulk lifetime, upon illumination, the density of photo-generated carriers will be higher, which will lead to a higher emitter sheet conductance. Low emitter sheet conductance has been considered one of the major concerns for IL cells. For the 5/10 Ω·cm substrates, the efficiency peak is expected to appear at finger spacings of 1.4-1.6 mm. Considering that 0.7

- 1.6 mm [88] is used in the industry for the mainstream PERC, emitter sheet resistance does not appear to be the limiting factor in the efficiency potential for IL cells, provided high-resistivity substrates are used. These simulation results indicate (i) the necessity of moving to high-resistivity substrates with high lifetimes; and (ii) that an efficiency of 24.8% can be obtained with optimised processing.

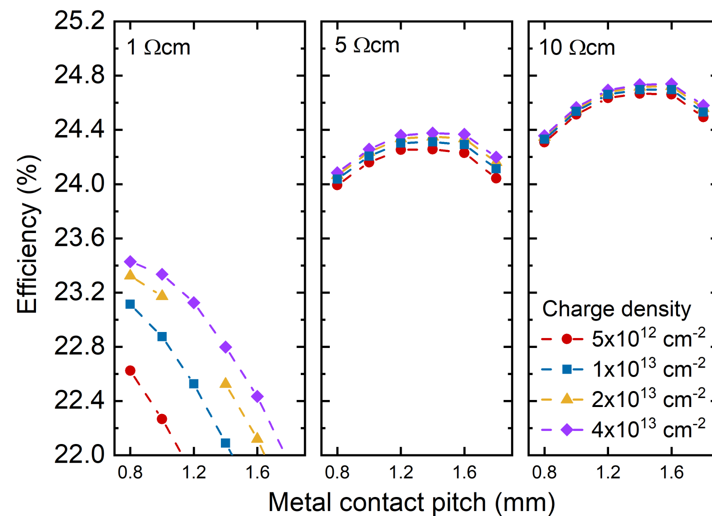

Figure 7-3 Simulated inversion layer cell efficiency with wafer resistivity set to 1/5/10 Ω·cm at charge densities in the range of 5×10^{12} cm^{-2} to 4×10^{13} cm^{-2} and various finger spacings. $D_{it\text{-}midgap}$, $D_{it\text{-}CB}$, and $D_{it\text{-}VB}$ were set to 5×10^{10}, 10^{14}, and 5×10^{13} eV^{-1}cm^{-2}, respectively.

Chapter 4 showed the importance of maintaining a low $D_{it\text{-}CB}$ in obtaining high emitter sheet conductance. In Figure 7-3, $D_{it\text{-}CB}$ was set to 10^{14} eV^{-1}cm^{-2}. In real devices, the surface conditions and passivating dielectrics may vary. These may result in variations in $D_{it\text{-}CB}$/$N_{it\text{-}acc}$. In Figure 7-4, $D_{it\text{-}CB}$ in the range of 10^{13} eV^{-1}cm^{-2} to 10^{15} eV^{-1}cm^{-2} was simulated to show the impact of such variations. The charge density in standard dielectric layers is 1-5 × 10^{12} cm^{-2} (Table 2-1), while charge densities in the order of 10^{13} cm^{-2} have been demonstrated in Chapter 4. In these simulations, charge densities were set to 5×10^{12} cm^{-2} and 2×10^{13} cm^{-2} to show the benefits of implementing higher charge densities in IL devices.

In the figure, a significant increase in efficiency is observed by reducing D_{it-CB} from 10^{15} to 10^{14} $eV^{-1}cm^{-2}$, while the improvement is less evident by further decreasing D_{it-CB} to 10^{13} $eV^{-1}cm^{-2}$. This agrees with the conclusion drawn in Chapter 4 that for charge densities above 10^{13} cm^{-2}, the emitter sheet conductance will reach its maximum at D_{it-CB} of 10^{14} $eV^{-1}cm^{-2}$ and shows no evident improvement while D_{it-CB} is further reduced. Additionally, reducing D_{it-CB} from 10^{15} to $10^{14}/10^{13}$ $eV^{-1}cm^{-2}$, the efficiency peak shifts from 1.2 mm to 1.4-1.6 mm in finger spacing, indicating an increase in emitter sheet conductance as expected. For the simulations with D_{it-CB} set to 10^{14} $eV^{-1}cm^{-2}$, an efficiency increase by 0.05-0.1% absolute is observed as the charge density is increased from 5×10^{12} cm^{-2} to 2×10^{13} cm^{-2}. The simulation results demonstrate the necessity of maintaining a low D_{it-CB} and obtaining high charge densities.

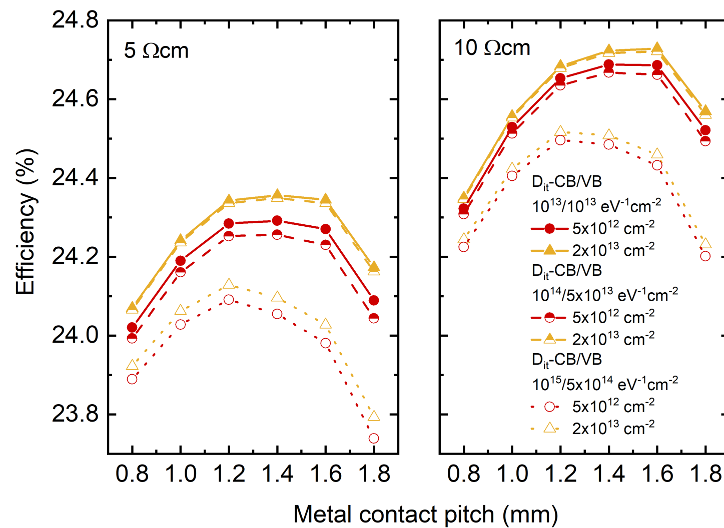

Figure 7-4 Simulated inversion layer cell efficiency with wafer resistivity set to 5/10 Ω·cm at charge densities of 5×10^{12} cm^{-2} and 2×10^{13} cm^{-2}, with varied finger spacings and band-tail interface state densities.

A negative charge density of -5×10^{12} cm^{-2} was defined in the model at the rear interface for field-effect passivation. However, higher negative charge densities of above -10^{13} cm^{-2} have been achieved at c-Si/AlO_x interfaces [87] and in c-Si/SiO_2/AlO_x stacks [166]. In

addition, it is projected that the finger width by screen printing will reduce to 18 μm in the industry by 2032 [10]. Narrower fingers down to 12 μm have been demonstrated by Cu plating [91]. Two sets of simulations were carried out to show the improvement in cell performance by implementing higher rear negative charge densities and narrower front fingers. The first set has a negative charge density of -5 × 10^{12} cm^{-2} and a finger width of 25 μm. The second set has the rear negative charge densities as high as the front positive charge densities and a finger width of 15 μm. $D_{it\text{-}CB}$ was kept at 10^{13} $eV^{-1}cm^{-2}$ in these simulations. Figure 7-5 shows the simulation results. The 15 μm finger width leads to a shift of the efficiency peaks from 1.4-1.6 mm to 1.2 mm in finger spacing, which can be explained by the reduced shading losses. The higher negative charge densities and narrower finger width lead to an increase in cell efficiency by 0.11-0.15% absolute, with the highest cell efficiency being 24.84%. These results emphasise the importance of improving the rear surface passivation and advancing the metallisation technology.

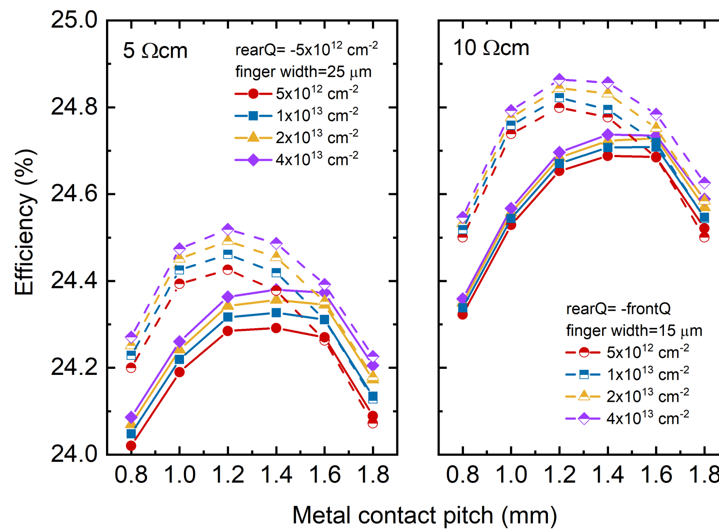

Figure 7-5 Simulated inversion layer cell efficiency with wafer resistivity set to 5/10 Ω·cm at charge densities in the range of 5 × 10^{12} cm^{-2} to 4 × 10^{13} cm^{-2} and various finger spacings. The density of negative charge at the rear dielectric was varied. $D_{it\text{-}midgap}$, $D_{it\text{-}CB}$, and $D_{it\text{-}VB}$ were set to 5 × 10^{10}, 10^{13}, and 10^{13} $eV^{-1}cm^{-2}$, respectively.

In the simulation results shown in Figure 7-3, $D_{it\text{-}midgap}$ was set to 5×10^{10} $eV^{-1}cm^{-2}$, $D_{it\text{-}CB}$ and $D_{it\text{-}VB}$ were set to 10^{14} and 5×10^{13} $eV^{-1}cm^{-2}$, respectively. These parameters were characterised from Si-SiO_2 interfaces of specimens with FZ silicon substrates and planar (100) surfaces. These are some of the best-passivated surfaces in the field [30]. Pyramid-textured surfaces are most commonly used in commercial solar cells for light trapping. Since the surface area is larger for the pyramid-textured surfaces and the (111) facets exposed correspond to a higher interface state density [104], the surface passivation will be reduced. Simulations where $D_{it\text{-}midgap}$, $D_{it\text{-}CB}$, and $D_{it\text{-}VB}$ were increased to 10^{11}, 10^{15}, and 5×10^{14} $eV^{-1}cm^{-2}$, respectively, were conducted and the results are plotted in Figure 7-6. The simulations show a significant increase in efficiency by increasing the front charge density from 2×10^{13} cm^{-2} to 4×10^{13} cm^{-2}, and by increasing the rear charge density for stronger field-effect passivation. This again suggests the importance of chemical passivation and maintaining high charge densities at both the front and the rear surface.

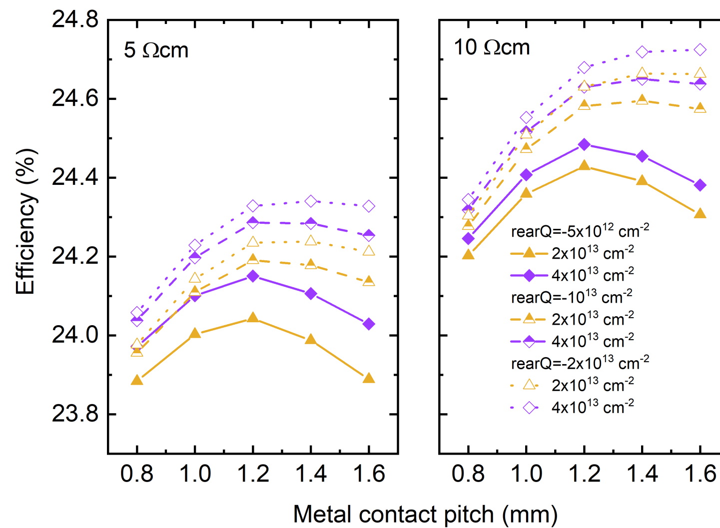

Figure 7-6 Simulated inversion layer cell efficiency with wafer resistivity set to 5/10 Ω·cm at charge densities of 2×10^{13} cm^{-2} and 4×10^{13} cm^{-2}. The finger spacing and negative rear charge density were varied. $D_{it\text{-}midgap}$, $D_{it\text{-}CB}$, and $D_{it\text{-}VB}$ were set to 10^{11}, 10^{15}, and 5×10^{14} $eV^{-1}cm^{-2}$, respectively.

7.3 Loss Analysis

The model used in this chapter has a field-induced emitter and a PERC-like rear structure. A loss analysis was carried out on the simulation presenting the highest efficiency in Section 7.2 to identify the limiting problems of the current cell design. Figure 7-7 shows the IV curve of the best-simulated cell. The model comprises a 170 μm, 10 Ω·cm p-type Si substrate. Both the front and rear surfaces were assumed to be well-passivated ($D_{it\text{-}midgap} = 5 \times 10^{10}$ $eV^{-1}cm^{-2}$, $D_{it\text{-}CB} = D_{it\text{-}VB} = 10^{13}$ $eV^{-1}cm^{-2}$). The fingers were set 15 μm wide and were kept 1.2 mm apart. A positive charge density of 4×10^{13} cm^{-2} was defined at the front interface to induce the emitter, while a negative charge density of -4×10^{13} cm^{-2} was defined at the rear interface for field-effect passivation. The simulation shows an efficiency of 24.84%, a fill factor of 82.16%, a V_{OC} of 719.39 mV, and a J_{SC} of 42.03 mA/cm^2. This result is close to the best efficiency predicted for PERC [52], [47]. Additionally, Section 7.2 showed that the optimum finger spacing for IL cells is similar to that used for PERC. It is concluded that with optimised surface passivation and charge density, the induced emitter can perform as well as a diffused emitter.

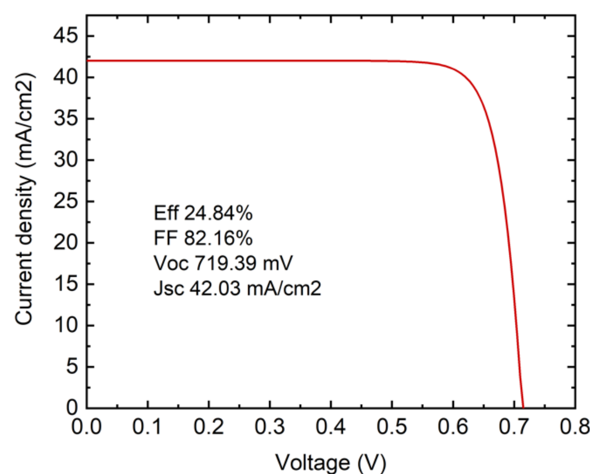

Figure 7-7 IV curve of the best simulated IL cell with an efficiency of 24.84%.

A loss analysis was performed on the cell with 24.84% efficiency. Figure 7-8 shows the recombination current density extracted from different loss mechanisms. The recombination current density by each loss mechanism at the maximum power point is listed in Table 7-2 and indicated by the dashed vertical yellow line in Figure 7-8. It can be observed that recombination at top and bottom surfaces does not appear in the scale, indicating that it is orders of magnitude lower than the losses shown in the figure, while half of the recombination current results from the rear contact. This is because the model has a PERC-like rear structure where direct silicon-metal contact leads to a high recombination velocity [48]. The focus of this work is the properties and potential of the field-induced emitter. The direct silicon-metal contact at the rear can be replaced by passivating contact geometries for reduced carrier recombination. The second and the third largest recombination sources are intrinsic and bulk SRH recombination in the emitter, and Auger recombination in the absorber, accounting for 19% and 11% of the total recombination current, respectively. These can be reduced by improving the bulk material and switching to thinner silicon wafers while maintaining efficient light management to avoid losses in J_{SC}. The loss analysis presented in this section focuses on the loss of excess carriers. A detailed analysis on resistive losses should be carried out in future work.

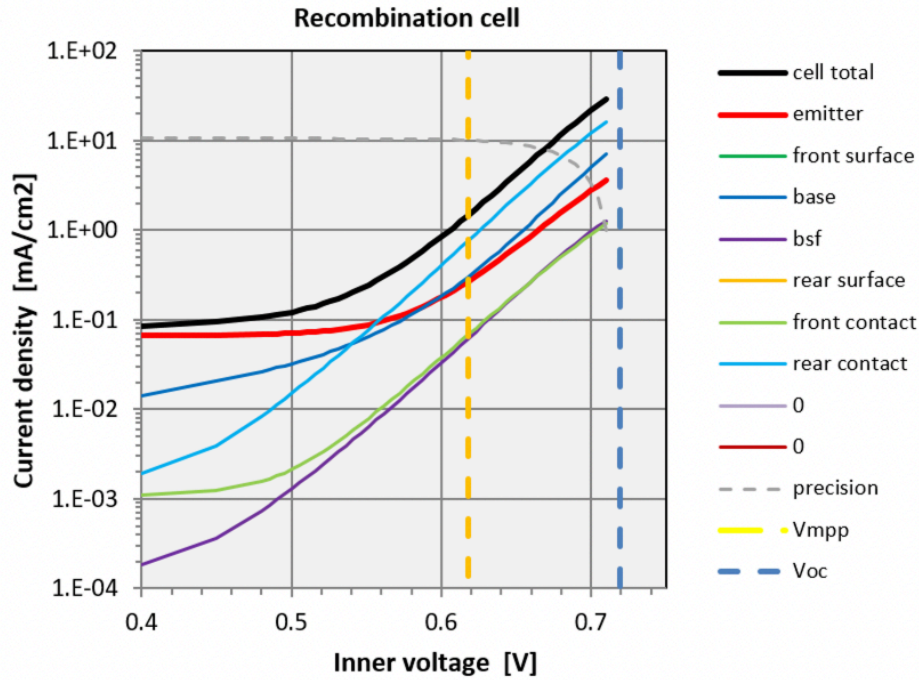

Figure 7-8 Recombination current density assigned to different loss mechanisms.

Table 7-2 Recombination current density by different loss mechanisms at the maximum power point.

	mA/cm^2	% of total
Intrinsic and bulk SRH in the emitter	2.36×10^{-1}	19%
Front contact	5.74×10^{-2}	5%
Front surface	1.45×10^{-6}	0%
SRH in absorber	5.34×10^{-2}	4%
Auger in absorber	1.33×10^{-1}	11%
Radiative in absorber	7.22×10^{-2}	6%
BSF	5.16×10^{-2}	4%
Rear contact	6.34×10^{-1}	51%
Rear surface	8.54×10^{-22}	0%

7.4 Discussion

In this chapter, the performance of field-induced emitters was evaluated by performing full-device simulations. The model comprises a field-induced emitter at the front and a PERC-like structure at the rear. In the literature, the performance of IL cells has been limited by their high emitter sheet resistance [73], [78]–[81]. In this chapter, the simulation results showed that with optimised processing, efficiencies as high as 24.8% can be achieved, around the highest efficiency predicted for PERC [52], [47]. This suggests that (i) the high emitter sheet resistance is not limiting the IL cell performance, and (ii) field-induced emitters can perform as well as diffused emitters. Despite field-induced emitters presenting higher sheet resistance than diffused emitters, they have several operational and fabrication advantages, including: (i) they are cheaper to fabricate due to a lower thermal budget required, (ii) less Auger recombination, (iii) lower surface recombination velocity due to reduced dopant density, and (iv) higher bulk lifetime due to reduced concentration of inactive dopants. These can result in potentially higher cell performance while maintaining lower fabrication costs than diffused emitters. The simulation results have shown that the model with a field-induced emitter can present equivalent cell performance as PERC. With lower fabrication costs, field-induced emitters can become competitive alternatives to diffused emitters in future solar modules.

The highest efficiency shown in the simulation results is 24.84%. The loss analysis shows that half of the recombination occurs at the rear contact. A PERC-like structure was used for rear contact in the model which has known contact losses. Higher efficiencies can be obtained by adjusting the cell design in the following ways:

(i) Replace the PERC-like rear structure with passivating contacts, both front and rear.

(ii) Induce p-type inversion layers on n-type silicon substrates. Such design can benefit from the inherently higher bulk lifetime and reduced degradation for n-type silicon substrates [70], [71]. Additionally, the results in Chapter 5 have shown that for A2 and A4 specimens, $N_{it\text{-}acc}$ is ~2 times higher than $N_{it\text{-}don}$. The sheet resistance of the p-type inversion layer may benefit from the reduced carriers that are trapped at the band-tail interface states.

(iii) Implementing a rear-emitter design providing a high bulk lifetime and well-passivated surfaces. For a field-induced emitter with a high sheet resistance, a narrow finger spacing is required to limit the resistive losses. In the case of a rear-emitter design, metallisation to the field-induced emitter is at the rear and does not block light injection, such that the requirement for high emitter sheet conductance is relieved. In the simulation results reported by Werner et al., an efficiency of 26.3% can be achieved using such rear-emitter design [73].

The second and the third largest sources of recombination are intrinsic and bulk SRH recombination in the emitter, and Auger recombination in the absorber. The simulation results have demonstrated the necessity of switching to high-resistivity silicon substrates with high bulk lifetimes. This will reduce the bulk SRH recombination in the emitter and Auger recombination in the absorber. Auger recombination in the absorber can also be alleviated by implementing thinner silicon wafers. It was projected in ITRPV [10] that the p-type wafer thickness will reduce to 140-145 μm by 2032. The effectiveness of implementing such strategies can be evaluated via simulations.

For IL cells with well-passivated surfaces ($D_{it\text{-}midgap} = 5 \times 10^{10}$ $eV^{-1}cm^{-2}$, $D_{it\text{-}CB} = 10^{14}$ $eV^{-1}cm^{-2}$, and $D_{it\text{-}VB} = 5 \times 10^{13}$ $eV^{-1}cm^{-2}$) and 5/10 Ω·cm silicon substrates, the simulation results showed that the variation in cell performance is within 0.2% absolute for charge densities in the range of 5×10^{12} cm^{-2} to 4×10^{13} cm^{-2}. For the simulation results with 1 Ω·cm substrates and a low bulk lifetime, the emitter appears to be more resistive and the variation in cell efficiency is 0.9% absolute for the same charge density range. Chapter 4 has shown that, in the dark, the emitter sheet conductance for 1/5/10 Ω·cm substrates coincides for charge densities above 10^{13} cm^{-2}. Under illumination, the higher bulk lifetimes defined in the model for 5/10 Ω·cm substrates lead to a higher density of photo-generated carriers in the emitter, and therefore higher emitter sheet conductance. These results suggest that carrier injection must be accounted for when considering the emitter resistance in IL cells, and thus carrier recombination in the emitter should be minimised to obtain high emitter sheet conductance under illumination. The emitter sheet conductance under illumination is therefore determined collectively by the charge density, band-tail interface state densities, irradiance, and the minority carrier lifetime in the emitter. The results also indicate a strong dependence of emitter sheet conductance and hence the IL cell performance on illumination, which should be considered while evaluating the performance of solar modules on the ground depending on the operation conditions.

7.5 Summary

This chapter explored the efficiency potential of a hybrid cell with a field-induced emitter and a PERC-like rear structure. The simulation results demonstrated the benefit of moving to silicon substrates with high base resistivities (5/10 Ω·cm) due to the improved bulk lifetime. Similar to the conclusion drawn in Chapter 4, low band-tail interface state densities

and high charge densities are required to obtain high efficiencies for IL cells. Additionally, for 5/10 Ω·cm silicon substrates, the efficiency peaks appear at the finger spacing of 1.4-1.6 mm, which is in the same range as used for commercial PERC cells. This indicates that although the dark emitter sheet resistance remains above 1 kΩ/sq, it does not limit the IL cell efficiency. The simulation results have also emphasised the importance of improving rear surface passivation and advancing metallisation technologies. With optimised processing and a finger width of 15 μm, the IL cell efficiency can reach beyond 24.8%. This is close to the best efficiency predicted for PERC [52], [47]. This suggests that the field-induced emitter can perform as well as a diffused emitter. The model used in this chapter has a PERC-like rear structure, which accounts for half of the carrier recombination in the best-simulated cell. While the field-induced emitter has been demonstrated to perform well, it can be integrated with other cell designs for better performance, for example, a rear-emitter design, passivating contacts, and the use of n-type silicon substrates.

Chapter 8 Conclusions and Further Work

8.1 Conclusions

Inversion layer cells have been studied since the 1970s [72]–[76]. However, this cell type has not been widely exploited or adopted in the industry. This is because the cell performance has been limited by the high emitter sheet resistance [73], [78]–[81]. In previous work, intrinsic charge in dielectric materials has been used to induce the inversion layer [72]–[76], [77]. The highest charge density reported is 1.1×10^{13} cm^{-2} [77]. In this thesis, a field and temperature-assisted ion migration method was used to incorporate a controllable amount of positive ionic charge into dielectric thin films. An accumulation layer sheet resistance as low as 950 Ω/sq was demonstrated, which is the lowest reported in the literature [72], [73]. A model was developed in Sentaurus TCAD [132] to achieve deep insights into the formation and properties of field-induced charge layers. The simulation results showed that the resistance is determined collectively by charge density, band-tail interface state density, illumination and carrier recombination:

> **Charge density**: The emitter sheet conductance increases with charge density. However, due to reduced carrier mobilities at strong interface electric fields, the emitter sheet conductance plateaus at high charge densities. For well-passivated surfaces, the emitter sheet conductance plateaus at ~1.1 kΩ/sq in the dark for charge densities above 2×10^{13} cm^{-2}.

Band-tail interface states: A low band-tail interface state density was shown necessary to obtain a high emitter sheet conductance. However, reducing band-tail interface state densities below 10^{14} $eV^{-1}cm^{-2}$ has been shown ineffective in further increasing the emitter sheet conductance.

Illumination: Photo-generated carriers were shown to lead to an increase in the carrier density in bulk silicon and hence (i) a change in emitter thickness and (ii) an increase in emitter sheet conductance. As an example, the simulation results showed that for an inversion layer induced on a 1 Ω·cm p-type Si substrate by a charge density of 2×10^{13} cm^{-2}, under 1-sun illumination, the junction will shift from ~100 nm to 60 nm from the interface and the emitter sheet conductance will increase by 7.4%.

According to the simulation results, the accumulation layer sheet resistance of 950 Ω/sq obtained experimentally corresponds to a dielectric charge density greater than 10^{13} cm^{-2}. This is on par with or higher than the highest achieved in the literature [72]–[76], [77]. This suggests that inversion layer cells fabricated using the ion migration method should lead to a significant improvement in efficiency. Since a low band-tail interface state density is important in obtaining a high emitter sheet conductance, methods to minimise the state density should be explored in the future. A characterisation method was developed in this thesis for the sensitive detection of band-tail interface states near both band edges with the help of simulations. This method can be used to determine the effectiveness of any passivation methods on the band-tails. The dependence of field-induced emitters on illumination was shown to be stronger than that of P-diffused emitters. The impact of illumination should be considered to determine the resistive losses in field-induced emitters.

A high dielectric charge density and a low band-tail interface state density are necessary to achieve the highest sheet conductance for field-induced emitters.

Compared with the mainstream P-diffused emitters, the advantages of field-induced emitters include lower fabrication costs and less carrier recombination. The simulation results showed that the field-induced emitters are thinner than P-diffused emitters. This will lead to less Auger recombination. Additionally, due to the absence of dopant atoms in field-induced emitters, there will be less SRH recombination both in the bulk and at the interface [66]–[69]. In terms of the fabrication cost, a lower thermal budget is required in fabricating field-induced emitters, with most of the processing steps accomplished within minutes at temperatures below 500 °C. Previously, the drawback of field-induced emitters was thought to be the high emitter sheet resistance. Simulation results showed that with optimised surface passivation and charge density, the lowest dark emitter sheet resistance that can be reached is 1.1 kΩ/sq. For emitters with a high sheet resistance, narrow finger spacings are necessary to limit resistive losses. This will lead to high shading losses. Although the 1.1 kΩ/sq emitter sheet resistance is about 7 times higher than that of typical P-diffused emitters (150 Ω/sq) [10], the optimum emitter sheet resistance is still under debate. It was predicted in [10] that the sheet resistance of P-diffused emitters will increase to 200 Ω/sq by 2032. Whether the 1.1 kΩ/sq sheet resistance will be limiting the inversion layer cell efficiency was evaluated by device simulations. The model comprises a field-induced emitter and a PERC-like structure at the rear. The highest cell efficiency appeared at a finger spacing of 1.2 - 1.6 mm, which is in the range of the finger spacing used for P-diffused emitters [88]. This suggests that despite the high emitter sheet resistance, the performance of inversion layer cells is not limited by the resistive losses in the emitter or shading losses. The highest inversion layer cell efficiency simulated is 24.84%, which is comparable to the best predicted for PERC

[52], [47]. This indicates that field-induced emitters can perform as well as P-diffused emitters. A loss analysis was performed on the champion inversion layer cell, showing that half of the carrier recombination occurs at the PERC-like rear structure. Since the field-induced emitter is the focus of this project, it can be integrated with passivating contacts to achieve better cell performance. With low fabrication costs and high potential cell efficiencies, field-induced emitters can become competitive alternatives to P-diffused emitters in commercial applications.

Proof-of-concept inversion layer cells were fabricated in this thesis. Laser doping was used to both ablate the silicon oxide and counter-dope the region underneath into n-type. The samples were annealed to recover the laser-induced damage and to ensure a complete n-type emitter layer. Positive K^+ ions were incorporated into the oxide thin film to induce the emitter. An electroplated nickel grid was used for front metallisation. The formation and uniformity of the field-induced emitter were confirmed using Suns-V_{OC} and LBIC. The champion cell presented an efficiency of 10.8%, demonstrating that inversion layer cells can be fabricated using the ion migration method. Although the cell efficiency is low, simulation results have shown that with optimised processing, an efficiency of as high as 24.8% can be achieved. The performance of the proof-of-concept cells was limited by the specimens and fabrication tools available. The techniques for laser ablation, oxide removal, electroplating, firing, and hydrogenation have been well-studied and implemented in the industry. Therefore, cell performance can be immediately improved if those techniques can be integrated into the fabrication procedure. The performance of inversion layer precursor cells has been demonstrated stable against an elevated temperature at 120 °C and UV irradiation for 2 months. In this thesis, I have demonstrated the fabrication of inversion layer cells based

on a novel ion-charged oxide thin film. Further optimisation of each processing step should be carried out to improve cell efficiency.

8.2 Further work

This thesis demonstrated that the sheet resistance of field-induced emitters is determined by charge density, band-tail interface state density, illumination and carrier recombination. With optimised surface passivation and charge density, an emitter sheet resistance of 1.1 kΩ/sq can be achieved. To ensure a low emitter sheet resistance in practical applications and to understand the properties of field-induced charge layers better, the following challenges should be addressed:

- Low band-tail interface state densities have been demonstrated important in obtaining a high emitter sheet conductance. The properties of band-tail interface states and methods to reduce them should be investigated in the future with the aid of the characterisation tool developed in this thesis.
- The accumulation of positive K^+ ions near the interface has been shown detrimental to surface passivation. Methods to reduce the damage or to chemically re-passivate the interface states should be investigated.
- In this thesis, field-induced charge layers were studied on specimens with a flat (100) surface. The interface parameters used in the Sentaurus model were characterised from samples with a flat (100) surface. For commercial applications, silicon substrates with pyramid-textured (111) surfaces are used for light trapping. The current path within field-induced emitters will be more complicated with such surfaces. Therefore, interface parameters of (111) surfaces and inversion layers induced on pyramid-textured surfaces should be studied in the future.

- The sheet resistance of field-induced charge layers obtained from simulations is heavily dependent on the model used to describe the carrier density and carrier mobility in bulk silicon. The Lombardi mobility model [135], [136] was the only one that can be used to explain the experimental results in this work. Further calibration of carrier mobilities at extremely high interface electric fields is required for accurate predictions of properties of field-induced charge layers.
- Photo-generated carriers under illumination contribute to the emitter sheet conductance. The concentration of photo-generated carriers in the emitter is dependent on irradiance and carrier recombination. The impact of mid-gap interface state density and bulk lifetime on emitter sheet conductance and the IL cell efficiency should be investigated in future work.

Proof-of-concept inversion layer cells were fabricated in this thesis, with the champion cell presenting an efficiency of 10.8%. The low cell efficiency obtained is due to the lack of optimisation in the processing steps. The performance can be improved if:

- A silicon substrate with a millisecond-level lifetime and a higher base resistivity is used as the starting material.
- A large silicon substrate is used for reduced impact of edge recombination.
- A SiN_x layer is added for hydrogenation and anti-reflection.
- The texturing and rear reflector is optimised for reduced optical losses.
- The laser doping process is optimised for reduced laser damage.
- The electroplating process is improved to achieve a higher aspect ratio for the metal fingers.
- The Ni-Si contact is annealed to form NiSi alloy for reduced contact resistance.

The model used for device simulations comprises a field-induced emitter and a PERC-like rear structure. The simulation results showed that an efficiency of 24.8% can be achieved, provided it is possible to optimise all processing steps. The cell performance can be enhanced if the cell structure is modified in the following ways:

- For the inversion layer cell model used in this work, the loss analysis showed that the rear contact is responsible for 51% of carrier recombination. The possibility of integrating the field-induced emitter with passivating contacts on both the front and the rear surface should be explored in future work.
- A rear-emitter design can be used to avoid extra shading losses for highly resistive emitters that require narrow finger spacings. The feasibility and potential of such cell design should be evaluated in future work.
- A negative dielectric charge, for example, intrinsic charge in AlO_x layers, can be used to induce p-type inversion layers on n-type silicon substrates. This cell design can benefit from the intrinsically high bulk lifetime of the n-type substrates [70]. Additionally, the results in this thesis have shown that the band-tail interface state density near the conduction band edge is twice as high as that near the valence band edge. For p-type inversion layers induced on n-type silicon substrates, there will be fewer field-induced carriers trapped at the interface. However, the sheet resistance of the p-type layer can be limited by the intrinsically lower hole mobility than electron mobility. The potential of a field-induced p-type inversion layer should be investigated in future work.

The loss analysis of the best simulated cell focuses on the loss of excess carriers. A detailed power loss analysis should be carried out in future work to better understand the limitations of cells with a field-induced emitter.

References

[1] NOAA National Centers for Environmental information, "Climate at a Glance: Global Time Series," *June 2022*. [Online]. Available: https://www.ncdc.noaa.gov/cag/. [Accessed: 15-Jun-2022].

[2] *Climate Change 2013 The Physical Science Basis*. New York: Intergovernmental Panel on Climate Change - Cambridge University Press, 2013.

[3] A. J. McMichael, R. E. Woodruff, and S. Hales, "Climate change and human health: present and future risks.," *Lancet*, vol. 367, no. 9513, pp. 859–69, Mar. 2006, doi: 10.1016/S0140-6736(06)68079-3.

[4] T. Physical and S. Basis, *Climate Change 2021—The Physical Science Basis*, vol. 43, no. 4. 2021.

[5] P. P. Altermatt, "With storage to 100% renewable power supply." [Online]. Available: https://www.changeanyway.com/with-storage-to-100-renewable-power-supply/. [Accessed: 27-Oct-2022].

[6] International Renewable Energy Agency, *Renewable Power Generation Costs in 2021*. 2022.

[7] IRENA, "Majority of New Renewables Undercut Cheapest Fossil Fuel on Cost." [Online]. Available: https://www.irena.org/news/pressreleases/2021/Jun/Majority-of-New-Renewables-Undercut-Cheapest-Fossil-Fuel-on-Cost. [Accessed: 27-Oct-2022].

[8] D. Bogdanov *et al.*, "Radical transformation pathway towards sustainable electricity via evolutionary steps," *Nat. Commun.*, vol. 10, no. 1, pp. 1–16, 2019, doi: 10.1038/s41467-019-08855-1.

[9] ITPRV, "International Technology Roadmap for Photovoltaic," *Itrpv*, vol. 14th Editi, no. April, p. 53, 2023.

[10] "International Technology Roadmap for Photovoltaic (ITRPV)," *Itrpv*, vol. 13th Editi, no. March, pp. 1–81, 2022.

[11] I. M. Peters, C. D. Rodriguez Gallegos, S. E. Sofia, and T. Buonassisi, "The Value of Efficiency in Photovoltaics," *Joule*, vol. 3, no. 11, pp. 2732–2747, 2019, doi: 10.1016/j.joule.2019.07.028.

[12] S. Martinuzzi and O. Palais, "Hydrogen passivation of bulk defects and surface in silicon," *MRS Online Proc. Libr.*, vol. 813, no. 1, pp. 451–456, 2004, doi: 10.1557/PROC-813-H4.5.

[13] B. J. Hallam *et al.*, "Hydrogen Passivation of B-O Defects in Czochralski Silicon,"

Energy Procedia, vol. 38, pp. 561–570, 2013, doi: https://doi.org/10.1016/j.egypro.2013.07.317.

[14] A. G. Aberle, *Crystalline silicon solar cells : advanced surface passivation and analysis*. Sydney: Centre for Photovoltaic Engineering, University of New South Wales, 2009.

[15] J. F. Wager and K. Kuhn, "Device Physics Modeling of Surfaces and Interfaces from an Induced Gap State Perspective," *Crit. Rev. Solid State Mater. Sci.*, vol. 42, no. 5, pp. 373–415, 2017, doi: 10.1080/10408436.2016.1223013.

[16] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *J. Vac. Sci. \& Technol. B Microelectron. Nanom. Struct. Process. Meas. Phenom.*, vol. 18, no. 3, pp. 1785–1791, 2000, doi: 10.1116/1.591472.

[17] C. R. Helms and E. H. Poindexter, "The silicon-silicon dioxide system: Its microstructure and imperfections," *Reports Prog. Phys.*, vol. 57, no. 8, pp. 791–852, 1994, doi: 10.1088/0034-4885/57/8/002.

[18] J. P. Campbell, S. Member, P. M. Lenahan, and A. T. Krishnan, "Observations of NBTI-Induced Atomic-Scale Defects," vol. 6, no. 2, pp. 117–122, 2006.

[19] J. P. Campbell, P. M. Lenahan, A. T. Krishnan, and S. Krishnan, "Direct observation of the structure of defect centers involved in the negative bias temperature instability," *Appl. Phys. Lett.*, vol. 87, no. 20, pp. 1–3, 2005, doi: 10.1063/1.2131197.

[20] P. M. Lenahan, T. D. Mishima, J. Jumper, T. N. Fogarty, and R. T. Wilkins, "Direct experimental evidence for atomic scale structural changes involved in the interface-trap transformation process," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6 I, pp. 2131–2135, 2001, doi: 10.1109/23.983184.

[21] H. Feichtinger, "Deep Centers in Semiconductors," in *Handbook of Semiconductor Technology*, John Wiley & Sons, Ltd, 2000, pp. 167–229.

[22] V. Heine, "Theory of Surface States," *Phys. Rev.*, vol. 138, no. 6A, pp. A1689--A1696, Jun. 1965, doi: 10.1103/PhysRev.138.A1689.

[23] J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," *Phys. Rev. Lett.*, vol. 52, no. 6, pp. 465–468, Feb. 1984, doi: 10.1103/PhysRevLett.52.465.

[24] T. Iffländer *et al.*, "Local Density of States at Metal-Semiconductor Interfaces: An Atomic Scale Study," *Phys. Rev. Lett.*, vol. 114, no. 14, p. 146804, Apr. 2015, doi: 10.1103/PhysRevLett.114.146804.

[25] F. Giustino and A. Pasquarello, "Electronic and dielectric properties of a suboxide interlayer at the silicon–oxide interface in MOS devices," *Surf. Sci.*, vol. 586, no. 1, pp. 183–191, 2005, doi: https://doi.org/10.1016/j.susc.2005.05.012.

[26] S. Markov, P. Sushko, C. Fiegna, E. Sangiorgi, A. Shluger, and A. Asenov, "From ab initio properties of the Si-SiO2 interface, to electrical characteristics of metal-oxide-

semiconductor devices," *J. Phys. Conf. Ser.*, vol. 242, p. 12010, Jul. 2010, doi: 10.1088/1742-6596/242/1/012010.

[27] H. Flietner, W. Füssel, N. D. Sinh, and H. Angermann, "Density of states and relaxation spectra of etched, H-terminated and naturally oxidised Si-surfaces and the accompanied defects," *Appl. Surf. Sci.*, vol. 104–105, pp. 342–348, 1996, doi: 10.1016/S0169-4332(96)00168-7.

[28] W. Shockley and W. T. Read, "Statistics of the Recombinations of Holes and Electrons," *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sep. 1952, doi: 10.1103/PhysRev.87.835.

[29] R. N. Hall, "Electron-Hole Recombination in Germanium," *Phys. Rev.*, vol. 87, no. 2, p. 387, Jul. 1952, doi: 10.1103/PhysRev.87.387.

[30] R. S. Bonilla, B. Hoex, P. Hamer, and P. R. Wilshaw, "Dielectric surface passivation for silicon solar cells: A review," *Phys. Status Solidi Appl. Mater. Sci.*, vol. 214, no. 7, pp. 1–30, 2017, doi: 10.1002/pssa.201700293.

[31] J. Schmidt, R. Peibst, and R. Brendel, "Surface passivation of crystalline silicon solar cells: Present and future," *Sol. Energy Mater. Sol. Cells*, vol. 187, no. January, pp. 39–54, 2018, doi: 10.1016/j.solmat.2018.06.047.

[32] S. W. Glunz and F. Feldmann, "SiO2 surface passivation layers – a key technology for silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 185, no. April, pp. 260–269, 2018, doi: 10.1016/j.solmat.2018.04.029.

[33] H. Flietner, "U-Shaped Distributions at Semiconductor Interfaces and the Nature of the Related Defect Centres," *Phys. Status Solidi*, vol. 91, no. 1, pp. 153–164, 1985, doi: 10.1002/pssa.2210910120.

[34] Y. W. Lam and E. H. Rhoderick, "Surface-state density and surface potential in MIS capacitors by surface photovoltage measurements. II," *J. Phys. D. Appl. Phys.*, vol. 4, no. 9, pp. 1376–1389, 1971, doi: 10.1088/0022-3727/4/9/319.

[35] H. Flietner, "Spectrum and nature of defects at interfaces of semiconductors with predominant homopolar bonding," *Surf. Sci.*, vol. 200, no. 2–3, pp. 463–471, 1988, doi: 10.1016/0039-6028(88)90553-5.

[36] W. Füssel, M. Schmidt, H. Angermann, G. Mende, and H. Flietner, "Defects at the Si/SiO2 interface: Their nature and behaviour in technological processes and stress," *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 377, no. 2–3, pp. 177–183, 1996, doi: 10.1016/0168-9002(96)00205-7.

[37] M. H. Cohen, M. Y. Chou, E. N. Economou, S. John, and C. M. Soukoulis, "Band Tails, Path Integrals, Instantons, Polarons, and All That," *IBM J. Res. Dev.*, vol. 32, no. 1, pp. 82–92, 1988, doi: 10.1147/rd.321.0082.

[38] S. W. Glunz, D. Biro, S. Rein, and W. Warta, "Field-effect passivation of the SiO2-Si interface," *J. Appl. Phys.*, vol. 86, no. 1, pp. 683–691, 1999, doi: 10.1063/1.370784.

[39] K. R. McIntosh, S. C. Baker-Finch, N. E. Grant, A. F. Thomson, S. Singh, and I. D. Baikie, "Charge Density in Atmospheric Pressure Chemical Vapor Deposition TiO2 on SiO2-Passivated Silicon," *J. Electrochem. Soc.*, vol. 156, no. 11, p. G190, 2009, doi: 10.1149/1.3216029.

[40] Z. Xin *et al.*, "An Improved Methodology for Extracting the Interface Defect Density of Passivated Silicon Solar Cells," *IEEE J. Photovoltaics*, vol. 6, no. 5, pp. 1080–1089, 2016, doi: 10.1109/JPHOTOV.2016.2576685.

[41] K. A. Collett *et al.*, "An enhanced alneal process to produce SRV < 1 cm/s in 1 Ω cm n-type Si," *Sol. Energy Mater. Sol. Cells*, vol. 173, no. April, pp. 50–58, 2017, doi: 10.1016/j.solmat.2017.06.022.

[42] N. M. Haegel *et al.*, "Terawatt-scale photovoltaics: Trajectories and challenges.," *Science*, vol. 356, no. 6334, pp. 141–143, Apr. 2017, doi: 10.1126/science.aal1288.

[43] W. C. Sinke, "Development of photovoltaic technologies for global impact," *Renew. Energy*, vol. 138, pp. 911–914, 2019, doi: 10.1016/j.renene.2019.02.030.

[44] M. A. Green, "Photovoltaic technology and visions for the future," *Prog. Energy*, vol. 1, no. 1, p. 013001, 2019, doi: 10.1088/2516-1083/ab0fa8.

[45] A. Cuevas and D. Yan, "Misconceptions and Misnomers in Solar Cells," *IEEE J. Photovoltaics*, vol. 3, no. 2, pp. 916–923, 2013, doi: 10.1109/JPHOTOV.2013.2238289.

[46] R. S. Bonilla, I. Al-dhahir, M. Yu, P. Hamer, and P. P. Altermatt, "Charge fluctuations at the Si–SiO 2 interface and its effect on surface recombination in solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 215, no. May, p. 110649, 2020, doi: 10.1016/j.solmat.2020.110649.

[47] M. Hermle, F. Feldmann, M. Bivour, J. C. Goldschmidt, and S. W. Glunz, "Passivating contacts and tandem concepts: Approaches for the highest silicon-based solar cell efficiencies," *Appl. Phys. Rev.*, vol. 7, no. 2, 2020, doi: 10.1063/1.5139202.

[48] A. Cuevas, P. A. Basore, G. Giroult-Matlakowski, and C. Dubois, "Surface recombination velocity of highly doped n-type silicon," *J. Appl. Phys.*, vol. 80, no. 6, pp. 3370–3375, Sep. 1996, doi: 10.1063/1.363250.

[49] A. Blakers, "Development of the PERC Solar Cell," *IEEE J. Photovoltaics*, vol. 9, no. 3, pp. 629–635, May 2019, doi: 10.1109/JPHOTOV.2019.2899460.

[50] T. Dullweber and J. Schmidt, "Industrial Silicon Solar Cells Applying the Passivated Emitter and Rear Cell (PERC) Concept—A Review," *IEEE J. Photovoltaics*, vol. 6, no. 5, pp. 1366–1381, Sep. 2016, doi: 10.1109/JPHOTOV.2016.2571627.

[51] M. A. Green, "The Passivated Emitter and Rear Cell (PERC): From conception to mass production," *Sol. Energy Mater. Sol. Cells*, vol. 143, pp. 190–197, Dec. 2015, doi: 10.1016/j.solmat.2015.06.055.

[52] B. Min *et al.*, "A Roadmap Toward 24% Efficient PERC Solar Cells in Industrial Mass Production," *IEEE J. Photovoltaics*, vol. 7, no. 6, pp. 1541–1550, Nov. 2017, doi: 10.1109/JPHOTOV.2017.2749007.

[53] F. Feldmann, M. Bivour, C. Reichel, M. Hermle, and S. W. Glunz, "Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent transport characteristics," *Sol. Energy Mater. Sol. Cells*, vol. 120, no. PART A, pp. 270–274, 2014, doi: 10.1016/j.solmat.2013.09.017.

[54] Y. Chen *et al.*, "Mass production of industrial tunnel oxide passivated contacts (i-TOPCon) silicon solar cells with average efficiency over 23% and modules over 345 W," *Prog. Photovoltaics Res. Appl.*, vol. 27, no. 10, pp. 827–834, 2019, doi: 10.1002/pip.3180.

[55] T. G. Allen, J. Bullock, X. Yang, A. Javey, and S. De Wolf, "Passivating contacts for crystalline silicon solar cells," *Nat. Energy*, vol. 4, no. 11, pp. 914–928, 2019, doi: 10.1038/s41560-019-0463-6.

[56] H. Wagner *et al.*, "Optimizing phosphorus diffusion for photovoltaic applications: Peak doping, inactive phosphorus, gettering, and contact formation," *J. Appl. Phys.*, vol. 119, no. 18, pp. 1–9, 2016, doi: 10.1063/1.4949326.

[57] M. A. Kessler, T. Ohrdes, B. Wolpensinger, and N. P. Harder, "Charge carrier lifetime degradation in Cz silicon through the formation of a boron-rich layer during BBr3 diffusion processes," *Semicond. Sci. Technol.*, vol. 25, no. 5, 2010, doi: 10.1088/0268-1242/25/5/055001.

[58] P. P. Altermatt, "private communication." .

[59] P. P. Altermatt, J. Schmidt, G. Heiser, and A. G. Aberle, "Assessment and parameterisation of Coulomb-enhanced Auger recombination coefficients in lowly injected crystalline silicon," *J. Appl. Phys.*, vol. 82, no. 10, pp. 4938–4944, 1997, doi: 10.1063/1.366360.

[60] A. Richter, F. Werner, A. Cuevas, J. Schmidt, and S. W. Glunz, "Improved parameterization of Auger recombination in silicon," *Energy Procedia*, vol. 27, pp. 88–94, 2012, doi: 10.1016/j.egypro.2012.07.034.

[61] G. Hahn, "Status of Selective Emitter Technology," *25th EUPVSEC*, no. September, pp. 1091–1096, 2010.

[62] B. Hallam *et al.*, "Efficiency enhancement of i-PERC solar cells by implementation of a laser doped selective emitter," *Sol. Energy Mater. Sol. Cells*, vol. 134, pp. 89–98, 2015, doi: 10.1016/j.solmat.2014.11.028.

[63] Y. Tao, K. Madani, E. Cho, B. Rounsaville, V. Upadhyaya, and A. Rohatgi, "High-efficiency selective boron emitter formed by wet chemical etch-back for n-type screen-printed Si solar cells," *Appl. Phys. Lett.*, vol. 110, no. 2, 2017, doi: 10.1063/1.4973626.

[64] A. D. Upadhyaya, K. Madani, V. Upadhyaya, B. Rounsaville, Y.-Y. Huang, and A. Rohatgi, “Boron Selective Emitter Formation With Un-metallized J0e of 13fA/cm2 For Silicon Solar Cell Applications,” in *2020 47th IEEE Photovoltaic Specialists Conference (PVSC)*, 2020, pp. 1626–1629, doi: 10.1109/PVSC45281.2020.9300546.

[65] G. Poulain *et al.*, “Laser-Induced Boron Diffusion for Selective Emitter n-Type Solar Cells,” in *European Photovoltaic Solar Energy Conference and Exhibition*, 2012, pp. 2075–2078.

[66] M. Steyer, A. Dastgheib-Shirazi, G. Hahn, and B. Terheiden, “New Method for Determination of Electrically Inactive Phosphorus in n-type Emitters,” *Energy Procedia*, vol. 77, pp. 316–320, 2015, doi: 10.1016/j.egypro.2015.07.045.

[67] B. Min, H. Wagner, A. Dastgheib-Shirazi, A. Kimmerle, H. Kurz, and P. P. Altermatt, “Heavily doped Si: P emitters of crystalline Si solar cells: Recombination due to phosphorus precipitation,” *Phys. Status Solidi - Rapid Res. Lett.*, vol. 8, no. 8, pp. 680–684, 2014, doi: 10.1002/pssr.201409138.

[68] P. P. Altermatt *et al.*, “Numerical modeling of highly doped Si:P emitters based on Fermi-Dirac statistics and self-consistent material parameters,” *J. Appl. Phys.*, vol. 92, no. 6, pp. 3187–3197, 2002, doi: 10.1063/1.1501743.

[69] R. R. King, R. A. Sinton, and R. M. Swanson, “Studies of Diffused Phosphorus Emitters: Saturation Current, Surface Recombination Velocity, and Quantum Efficiency,” *IEEE Trans. Electron Devices*, vol. 37, no. 2, pp. 365–371, 1990, doi: 10.1109/16.46368.

[70] D. Macdonald and L. J. Geerligs, “Recombination activity of interstitial iron and other transition metal point defects in p- and n-type crystalline silicon,” *Appl. Phys. Lett.*, vol. 85, no. 18, pp. 4061–4063, 2004, doi: 10.1063/1.1812833.

[71] J. Schmidt, A. Cuevas, S. Rein, and S. W. Glunz, “Impact of light-induced recombination centres on the current - voltage characteristic of Czochralski silicon solar cells,” *Prog. Photovoltaics Res. Appl.*, vol. 9, no. 4, pp. 249–255, 2001, doi: 10.1002/pip.373.

[72] R. E. Thomas, R. B. North, and C. E. Norman, “Low Cost - High Efficiency MIS/Inversion Layer Solar Cells,” *IEEE Electron Device Lett.*, vol. 1, no. 5, pp. 79–80, 1980.

[73] F. Werner, Y. Larionova, D. Zielke, T. Ohrdes, and J. Schmidt, “Aluminum-oxide-based inversion layer solar cells on n -type crystalline silicon: Fundamental properties and efficiency potential,” *J. Appl. Phys.*, vol. 115, no. 7, 2014, doi: 10.1063/1.4865962.

[74] J. V. M. Paul Van Halen, Robert P. Mertens, Roger J. Van Overstraeten, Raye E. Thomas, “New TiOx-MIS and SiO2-MIS Silicon Solar Cells,” *IEEE Trans. Electron Devices*, vol. 25, no. 5, pp. 507–511, 1978.

[75] R. Hezel, “Silicon nitride for the improvement of silicon inversion layer solar cells,”

Solid State Electron., vol. 24, no. 9, pp. 863–868, 1981, doi: 10.1016/0038-1101(81)90103-9.

[76] K. Jager and R. Hezel, “Optical stability of silicon nitride MIS inversion layer solar cells,” *IEEE Trans. Electron Devices*, vol. 32, no. 9, pp. 1824–1829, Sep. 1985, doi: 10.1109/T-ED.1985.22204.

[77] K. Jager and R. Hezel, “Optical Stability of Silicon Nitride MIS Inversion Layer Solar Cells,” *IEEE Trans. Electron Devices*, vol. 32, no. 9, pp. 1824–1829, 1985, doi: 10.1109/T-ED.1985.22204.

[78] R. Hezel, “Recent progress in MIS solar cells,” *Prog. Photovoltaics Res. Appl.*, vol. 5, no. 2, pp. 109–120, 1997, doi: 10.1002/(SICI)1099-159X(199703/04)5:2<109::AID-PIP160>3.0.CO;2-8.

[79] G. Cheek and R. Mertens, “Metal-insulator-semiconductor silicon solar cells,” *Sol. Cells*, vol. 8, no. 1, pp. 17–32, 1983, doi: 10.1016/0379-6787(83)90037-6.

[80] B. Kuhlmann, “Simulation and optimization of metal-insulator-semiconductor inversion-layer silicon solar cells,” *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2167–2178, 2000, doi: 10.1109/16.877180.

[81] I. Martín, R. Lövblom, and Alcubilla, “High-efficiency solar cells based on inversion layer emitters,” *24th Eur. Photovolt. Sol. Energy Conf.*, no. 21-25 September 2009, pp. 1985–1990, 2009.

[82] R. S. Bonilla and P. R. Wilshaw, “A technique for field effect surface passivation for silicon solar cells,” *Appl. Phys. Lett.*, vol. 104, no. 23, pp. 2–7, 2014, doi: 10.1063/1.4882161.

[83] R. S. Bonilla and P. R. Wilshaw, “Potassium ions in SiO2: electrets for silicon surface passivation,” *J. Phys. D. Appl. Phys.*, vol. 51, no. 2, p. 25101, 2018.

[84] R. S. Bonilla, K. Collett, L. Rands, G. Martins, R. Lobo, and P. R. Wilshaw, “Stable, Extrinsic, Field Effect Passivation for Back Contact Silicon Solar Cells,” *Solid State Phenom.*, vol. 242, pp. 67–72, Oct. 2015, doi: 10.4028/www.scientific.net/SSP.242.67.

[85] W. A. Anderson, A. E. Delahoy, and R. A. Milano, “An 8% efficient layered Schottky-barrier solar cell,” *J. Appl. Phys.*, vol. 45, no. 9, pp. 3913–3915, 1974, doi: 10.1063/1.1663886.

[86] R. Hezel, K. Blumenstock, and R. Schorner, “Interface States and Fixed Charges in MNOS Structures With APCVD and PECVD Silicon Nitride,” *J. Electrochem. Soc.*, vol. 131, p. 1679, 1984.

[87] F. Werner and J. Schmidt, “Manipulating the negative fixed charge density at the c-Si/Al 2O3 interface,” *Appl. Phys. Lett.*, vol. 104, no. 9, 2014, doi: 10.1063/1.4867652.

[88] Y. Zhang, L. Wang, D. Chen, M. Kim, and B. Hallam, “Pathway towards 24%

efficiency for fully screen-printed passivated emitter and rear contact solar cells," *J. Phys. D. Appl. Phys.*, vol. 54, no. 21, 2021, doi: 10.1088/1361-6463/abe900.

[89] M. Gebhardt, T. Kießling, and M. Grimm, "Laser Contact Opening of High Efficient Solar Cells," *Laser Tech. J.*, vol. 11, no. 1, pp. 18–20, 2014, doi: 10.1002/latj.201400016.

[90] A. ur Rehman and S. H. Lee, "Review of the Potential of the Ni/Cu Plating Technique for Crystalline Silicon Solar Cells," *Materials (Basel).*, vol. 7, pp. 1318–1341, 2014.

[91] B. Grübel *et al.*, "Progress of plated metallization for industrial bifacial TOPCon silicon solar cells," *Prog. Photovoltaics Res. Appl.*, vol. 30, no. 6, pp. 615–621, 2022, doi: 10.1002/pip.3528.

[92] K. A. Collett *et al.*, "Scalable Techniques for Producing Field-Effect Passivation in High-Efficiency Silicon Solar Cells," *IEEE J. Photovoltaics*, vol. 9, no. 1, pp. 26–33, 2019, doi: 10.1109/JPHOTOV.2018.2872032.

[93] G. M. Wilson *et al.*, "The 2020 photovoltaic technologies roadmap," *J. Phys. D. Appl. Phys.*, vol. 53, no. 49, 2020, doi: 10.1088/1361-6463/ab9c6a.

[94] A. ur Rehman and S. H. Lee, "Advancements in n-type base crystalline silicon solar cells and their emergence in the photovoltaic industry.," *ScientificWorldJournal.*, vol. 2013, p. 470347, 2013, doi: 10.1155/2013/470347.

[95] B. Singha and C. S. Solanki, "N-type solar cells: advantages, issues, and current scenarios," *Mater. Res. Express*, vol. 4, no. 7, p. 72001, Jul. 2017, doi: 10.1088/2053-1591/aa6402.

[96] J. E. Cotter, J. H. Guo, P. J. Cousins, M. D. Abbott, F. W. Chen, and K. C. Fisher, "P-type versus n-type silicon wafers: Prospects for high-efficiency commercial silicon solar cells," *IEEE Trans. Electron Devices*, vol. 53, no. 8, pp. 1893–1901, 2006, doi: 10.1109/TED.2006.878026.

[97] L. C. Andreani, A. Bozzola, P. Kowalczewski, M. Liscidini, and L. Redorici, "Silicon solar cells: Toward the efficiency limits," *Adv. Phys. X*, vol. 4, no. 1, 2019, doi: 10.1080/23746149.2018.1548305.

[98] W. Zulehner, "Czochralski growth of silicon," *J. Cryst. Growth*, vol. 65, no. 1, pp. 189–213, 1983, doi: https://doi.org/10.1016/0022-0248(83)90051-9.

[99] K. Hoshikawa, H. Kohda, H. Hirata, and H. Nakanishi, "Low oxygen content czochralski silicon crystal growth," *Jpn. J. Appl. Phys.*, vol. 19, no. 1, pp. L33–L36, 1980, doi: 10.1143/JJAP.19.L33.

[100] S. P. Kobeleva, I. M. Anfimov, V. S. Berdnikov, and T. V. Kritskaya, "Possible causes of electrical resistivity distribution inhomogeneity in Czochralski grown single crystal silicon," *Mod. Electron. Mater.*, vol. 5, no. 1, pp. 27–32, 2019, doi: 10.3897/j.moem.5.1.46315.

[101] W. Dietze, W. Keller, and A. Mühlbauer, “Float-Zone Grown Silicon,” in *Silicon*, 1981, pp. 1–42.

[102] J. Vedde, T. Clausen, and L. Jensen, “Float-zone silicon for high volume production of solar cells,” in *3rd World Conference onPhotovoltaic Energy Conversion, 2003. Proceedings of*, 2003, vol. 1, pp. 943-946 Vol.1.

[103] W. Chen *et al.*, “Difference in anisotropic etching characteristics of alkaline and copper based acid solutions for single-crystalline Si,” *Sci. Rep.*, vol. 8, no. 1, p. 3408, 2018, doi: 10.1038/s41598-018-21877-x.

[104] S. C. Baker-Finch and K. R. McIntosh, “The contribution of planes, vertices, and edges to recombination at pyramidally textured surfaces,” *IEEE J. Photovoltaics*, vol. 1, no. 1, pp. 59–65, 2011, doi: 10.1109/JPHOTOV.2011.2165530.

[105] S. Du, “Ionic Field Effect Surface Passivation For Silicon Solar Cells,” 2018.

[106] M. Schofthaler, R. Brendel, G. Langguth, and J. H. Werner, “High-quality surface passivation by corona-charged oxides for semiconductor surface characterization,” in *Proceedings of 1994 IEEE 1st World Conference on Photovoltaic Energy Conversion - WCPEC (A Joint Conference of PVSC, PVSEC and PSEC)*, 1994, vol. 2, pp. 1509–1512 vol.2, doi: 10.1109/WCPEC.1994.520237.

[107] M. M. Shahin, “Mass-spectrometric studies of corona discharges in air at atmospheric pressures,” *J. Chem. Phys.*, vol. 45, no. 7, pp. 2600–2605, 1966, doi: 10.1063/1.1727980.

[108] M. M. Shahin, “Nature of Charge Carriers in Positive and Negative Corona Discharges,” pp. 85–89, 1969, doi: 10.1109/ceidp.1968.7725075.

[109] V. Scholtz, J. Julák, V. Kríha, and J. Mosinger, “Decontamination effects of low-temperature plasma generated by corona discharge. Part I: an overview.,” *Prague Med. Rep.*, vol. 108, no. 2, pp. 115–127, 2007.

[110] B. L. Henson, “A derivation of Warburg’s law for point to plane coronas,” *J. Appl. Phys.*, vol. 52, no. 6, pp. 3921–3923, 1981, doi: 10.1063/1.329241.

[111] R. S. Bonilla, C. Reichel, M. Hermle, P. Hamer, and P. R. P. R. Wilshaw, “Long term stability of c-Si surface passivation using corona charged SiO2,” *Appl. Surf. Sci.*, vol. 412, pp. 657–667, 2017, doi: 10.1016/j.apsusc.2017.03.204.

[112] A. J. Sprenkels, W. Olthuis, and P. Bergveld, “Application of silicon dioxide as an electret material,” pp. 165–169, 1988, doi: 10.1109/ise.1988.38543.

[113] I. D. Baikie, S. Mackenzie, P. J. Z. Estrup, and J. A. Meyer, “Noise and the Kelvin method,” *Rev. Sci. Instrum.*, vol. 62, no. 5, pp. 1326–1332, 1991, doi: 10.1063/1.1142494.

[114] R. S. Bonilla, “Modelling of Kelvin probe surface voltage and photovoltage in dielectric-semiconductor interfaces,” *Mater. Res. Express*, vol. 9, no. 8, p. 85901,

2022, doi: 10.1088/2053-1591/ac84c8.

[115] S. M. Sze and M. K. Lee, *Semiconductor Devices: Physics and Technology*. John Wiley and Sons, Inc.

[116] D. A. Neamen, *Semiconductor Physics and Devices Basic Principles*, vol. 9, no. 5. 2006.

[117] R. B. M. Girisch, R. P. Mertens, R. F. Dekeersmaecker, and R. F. De Keersmaecker, "Determination of Si-SiO2 Interface Recombination Parameters using a Gate-Controlled Point-Junction Diode under Illumination," *IEEE Trans. Electron Devices*, vol. 35, no. 2, pp. 203–222, 1988, doi: 10.1109/16.2441.

[118] R. S. Bonilla, "Surface passivation for silicon solar cells," 2015.

[119] L. J. van der Pauw, "A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shape," *Philips Res. Reports*, vol. 13, no. 1, pp. 1–9, 1958.

[120] R. Chwang, B. J. Smith, and C. R. Crowell, "Contact size effects on the van der Pauw method for resistivity and Hall coefficient measurement," *Solid State Electron.*, vol. 17, no. 12, pp. 1217–1227, 1974, doi: 10.1016/0038-1101(74)90001-X.

[121] R. Petres, "Amorphous Silicon Compound Films for Surface Passivation and Antireflection Coating of Crystalline Silicon Solar Cells," 2010.

[122] R. A. Sinton, A. Cuevas, and M. Stuckings, "Quasi-steady-state photoconductance, a new method for solar cell material and device characterization," in *Conference Record of the Twenty Fifth IEEE Photovoltaic Specialists Conference - 1996*, 1996, pp. 457–460, doi: 10.1109/PVSC.1996.564042.

[123] R. S. Bonilla, "Controlling Surface Carrier Density via a PEDOT:PSS Gate: An Application to the Study of Silicon-Dielectric Interface Recombination," *Sol. RRL*, vol. 2, no. 10, 2018, doi: 10.1002/solr.201800172.

[124] Q. Feng, K. Du, Y. K. Li, P. Shi, and Q. Feng, "Effect of annealing on performance of PEDOT:PSS/n-GaN Schottky solar cells," *Chinese Phys. B*, vol. 23, no. 7, 2014, doi: 10.1088/1674-1056/23/7/077303.

[125] B. Friedel *et al.*, "Effects of layer thickness and annealing of PEDOT:PSS layers in organic photodetectors," *Macromolecules*, vol. 42, no. 17, pp. 6741–6747, 2009, doi: 10.1021/ma901182u.

[126] A. G. Aberle, S. Glunz, and W. Warta, "Impact of illumination level and oxide parameters on Shockley-Read-Hall recombination at the Si-SiO2 interface," *J. Appl. Phys.*, vol. 71, no. 9, pp. 4422–4431, 1992, doi: 10.1063/1.350782.

[127] I. R. Al-dhahir, "Exploiting Extrinsic Passivation on Thin Film Dielectrics for High Efficiency Solar Cells," 2021.

[128] Y. Shi, M. Voss, M. Yu, E. T. Hwu, and R. S. Bonilla, "NanoLBIC Characterisation

of Silicon Solar Cells Based on a Blue Laser Pick-up Unit," in *AIP Conference Proceedings, Silicon PV Conference*, 2021.

[129] NREL, "Reference Air Mass 1.5 Spectra." [Online]. Available: https://www.nrel.gov/grid/solar-resource/spectra-am1.5.html. [Accessed: 29-Aug-2023].

[130] I. Al-dhahir *et al.*, "Ion-Charged Dielectric Nanolayers for Enhanced Surface Passivation in High Efficiency Photovoltaic Devices," *Adv. Mater. Interfaces*.

[131] E. Conwell, *High field transport in semiconductors*. 1976.

[132] Synopsys, "Sentaurus Device." [Online]. Available: https://www.synopsys.com/silicon/tcad/device-simulation/sentaurus-device.html. [Accessed: 29-Apr-2021].

[133] S. W. Glunz, S. Rein, J. Knobloch, W. Wettling, and T. Abe, "Comparison of boron- and gallium-doped p-type Czochralski silicon for photovoltaic application," *Prog. Photovoltaics Res. Appl.*, vol. 7, no. 6, pp. 463–469, 1999, doi: 10.1002/(SICI)1099-159X(199911/12)7:6<463::AID-PIP293>3.0.CO;2-H.

[134] "Sentaurus Device, manual 2021.06, Synopsys, Mountain View, CA." .

[135] M. N. Darwish, J. L. Lentz, M. R. Pinto, P. M. Zeitzoff, T. J. Krutsick, and H. H. Vuong, "An improved electron and hole mobility model for general purpose device simulation," *IEEE Trans. Electron Devices*, vol. 44, no. 9, pp. 1529–1538, 1997, doi: 10.1109/16.622611.

[136] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 7, no. 11, pp. 1164–1171, 1988, doi: 10.1109/43.9186.

[137] G. Paasch and H. Übensee, "A Modified Local Density Approximation. Electron Density in Inversion Layers," *Phys. Status Solidi*, vol. 113, no. 1, pp. 165–178, 1982, doi: 10.1002/pssb.2221130116.

[138] L. A. Ragnarsson and P. Lundgren, "Electrical characterization of Pb centers in (100)Si-SiO2 structures: The influence of surface potential on passivation during post metallization anneal," *Doktorsavhandlingar vid Chalmers Tek. Hogsk.*, vol. 1510, no. 1511, pp. 1–13, 1999.

[139] H. Bartzsch *et al.*, "Electrical insulation properties of sputter-deposited SiO2, Si3N4 and Al2O3 films at room temperature and 400 °C," *Phys. status solidi*, vol. 206, no. 3, pp. 514–519, 2009, doi: https://doi.org/10.1002/pssa.200880481.

[140] V. Leonov, C. Van Hoof, M. Goedbloed, and R. Van Schaijk, "Charge injection and storage in single-layer and multilayer inorganic electrets based on SiO2 and Si3N4," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 19, no. 4, pp. 1253–1260, 2012, doi: 10.1109/TDEI.2012.6259999.

[141] D. B. M. Klaassen, “A Unified Mobility Model for Device Simulation - I. Model Equations and Concentration Dependence,” *Solid State Electron.*, vol. 35, no. 7, pp. 953–959, 1992.

[142] Syed Aon Mujtaba, “Advanced Mobility Models for Design and Simulation of Deep Submicrometer Mosfets,” *Thesis*, no. December, 1995.

[143] A. G. Aberle, “Surface Passivation of Crystalline Silicon Solar Cells: A Review,” *Prog. Photovoltaics Res. Appl.*, vol. 8, pp. 473–487, 2000, doi: 10.1007/978-3-319-75377-5_8.

[144] G. Kaur *et al.*, “Ultra-thin LPCVD SiNx/n+poly-Si passivated contacts - A possibility?,” *Conf. Rec. IEEE Photovolt. Spec. Conf.*, pp. 2679–2683, 2019, doi: 10.1109/PVSC40753.2019.8980624.

[145] R. Brendel, “Coupling of Light into Mechanically Textured Silicon Solar Cells: a Ray Tracing Study,” *Prog. Photovoltaics Res. Appl.*, vol. 3, pp. 25–38, 1995.

[146] R. A. Street, *Hydrogenated Amorphous Silicon*. 1991.

[147] A. G. Aberle, “Surface passivation of crystalline silicon solar cells: a review,” *Prog. Photovoltaics Res. Appl.*, vol. 8, no. 5, pp. 473–487, Sep. 2000, doi: 10.1002/1099-159X(200009/10)8:5<473::AID-PIP337>3.0.CO;2-D.

[148] J. Werner and M. Peisl, “Exponential band tails in polycrystalline semiconductor films,” *Phys. Rev. B*, vol. 31, no. 10, pp. 6881–6883, May 1985, doi: 10.1103/PhysRevB.31.6881.

[149] R. S. Bonilla and P. R. Wilshaw, “On the c-Si/SiO2interface recombination parameters from photo-conductance decay measurements,” *J. Appl. Phys.*, vol. 121, no. 13, 2017, doi: 10.1063/1.4979722.

[150] M. Yu *et al.*, “Assessing the Potential of Inversion Layer Solar Cells Based on Highly Charged Dielectric Nanolayers,” *Phys. Status Solidi - Rapid Res. Lett.*, vol. 15, no. 12, 2021, doi: 10.1002/pssr.202100129.

[151] S. McNab *et al.*, “Alternative Dielectrics for Hole Selective Passivating Contacts and the Influence of Nanolayer Built-In Charge,” *AIP Conf. Proceedings, Silicon PV Conf.*, 2021.

[152] J. Schmidt *et al.*, “Advances in the surface passivation of silicon solar cells,” *Energy Procedia*, vol. 15, no. 2011, pp. 30–39, 2012, doi: 10.1016/j.egypro.2012.02.004.

[153] J. Schmidt, A. Merkle, R. Brendel, B. Hoex, M. C. M. van de Sanden, and W. M. M. Kessels, “Surface passivation of high-efficiency silicon solar cells by atomic-layer-deposited Al2O3,” *Prog. Photovoltaics Res. Appl.*, vol. 16, no. 6, pp. 461–466, 2008, doi: https://doi.org/10.1002/pip.823.

[154] C. H. Hsu *et al.*, “Enhanced Si Passivation and PERC Solar Cell Efficiency by Atomic Layer Deposited Aluminum Oxide with Two-step Post Annealing,” *Nanoscale Res.*

Lett., vol. 14, 2019, doi: 10.1186/s11671-019-2969-z.

[155] H. Park *et al.*, "Role of polysilicon in poly-Si/SiO: X passivating contacts for high-efficiency silicon solar cells," *RSC Adv.*, vol. 9, no. 40, pp. 23261–23266, 2019, doi: 10.1039/c9ra03560e.

[156] M. K. Stodolny *et al.*, "Material properties of LPCVD processed n-type polysilicon passivating contacts and its application in PERPoly industrial bifacial solar cells," *Energy Procedia*, vol. 124, pp. 635–642, 2017, doi: 10.1016/j.egypro.2017.09.250.

[157] C. N. Berglund, "Surface States at Steam-Grown Silicon-Silicon Dioxide Interfaces," *IEEE Trans. ele*, vol. ED-13, no. 10, pp. 701–705, 1966, doi: 10.1080/10408437308245838.

[158] D. Jousse, J. Kanicki, and J. H. Stathis, "Observation of multiple silicon dangling bond configurations in silicon nitride," *Appl. Phys. Lett.*, vol. 54, no. 11, pp. 1043–1045, 1989, doi: 10.1063/1.101558.

[159] B. Min *et al.*, "A Roadmap Toward 24% Efficient PERC Solar Cells in Industrial Mass Production," *IEEE J. Photovoltaics*, vol. 7, no. 6, pp. 1541–1550, Nov. 2017, doi: 10.1109/JPHOTOV.2017.2749007.

[160] G. Beaucarne, G. Schubert, L. Tous, and J. Hoornstra, "Summary of the 8th Workshop on Metallization and Interconnection for Crystalline Silicon Solar Cells," *Energy Procedia*, no. September 2019, p. 1, 2019, doi: 10.1016/j.egypro.2016.10.076.

[161]R. S. Davidsen *et al.*, "Black silicon laser-doped selective emitter solar cell with 18.1% efficiency," *Sol. Energy Mater. Sol. Cells*, vol. 144, pp. 740–747, 2016, doi: 10.1016/j.solmat.2015.10.018.

[162] P. P. Altermatt *et al.*, "Learning from the past to look beyond the roadmap of PERC Si solar cell mass production," *35th Eur. Photovolt. Sol. Energy Conf. Exhib.*, vol. September, pp. 215–221, 2018, doi: 10.4229/35THEUPVSEC20182018-2BP.1.1.

[163] C.-H. Du *et al.*, "A Well-Controlled PSG Layer on Silicon Solar Cells against Potential Induced Degradation," *ECS J. Solid State Sci. Technol.*, vol. 4, no. 3, pp. P97–P100, 2015, doi: 10.1149/2.0201503jss.

[164] N. E. Grant *et al.*, "Gallium-Doped Silicon for High-Efficiency Commercial Passivated Emitter and Rear Solar Cells," *Sol. RRL*, vol. 5, no. 4, pp. 1–8, 2021, doi: 10.1002/solr.202000754.

[165] G. Agostinelli *et al.*, "Very low surface recombination velocities on p-type silicon wafers passivated with a dielectric with fixed negative charge," *Sol. Energy Mater. Sol. Cells*, vol. 90, no. 18–19, pp. 3438–3443, 2006, doi: 10.1016/j.solmat.2006.04.014.

[166] H. Patel, C. Reichel, A. Richter, P. Masuch, J. Benick, and S. W. Glunz, "Effective charge dynamics in Al2O3/SiO2 multilayer stacks and their influence on silicon surface passivation," *Appl. Surf. Sci.*, vol. 579, no. November 2021, p. 152175, 2022,

doi: 10.1016/j.apsusc.2021.152175.

Appendix

An approximation was performed to calculate the sheet resistance of field-induced accumulation layers in this thesis (Eq (3-16)). The error of the approximation was evaluated by conducting simulations in Sentaurus TCAD. The model developed in Chapter 4 was used for the simulations. The model comprises a 200 µm thick, 1 Ω·cm n-type silicon substrate with both surfaces passivated by 100 nm SiO_2. The charge density is defined at the front Si/SiO_2 interface. The approximation was compared with accumulation layer sheet resistance calculated using Eq (3-15). The depth of the accumulation layer was defined as where the change in electron density per um in depth is below 5×10^{15} cm^{-3}, which is the dopant density of 1 Ω·cm n-type silicon substrates. Table A-1 shows the comparison of accumulation layer sheet resistance calculated using the two methods. The sheet resistance calculated using the approximation is labelled R_{sh}-acc A. The sheet resistance calculated using the other method is labelled R_{sh}-acc B. The results show that for charge densities above 2×10^{13} cm^{-2}, the approximation produced an error of less than 2.3%.

Table A-1 Accumulation layer sheet resistance calculated using two methods by simulations.

Charge density (10^{12} cm^{-2})	R_{sh}-wafer (Ω/sq)	R_{sh}-acc A (Ω/sq)	R_{sh}-acc B (Ω/sq)	Error (%)
1	48.82	11728	9749	20.30%
2	48.70	7361	6502	13.22%
4	48.47	4286	3980	7.69%
6	48.17	2754	2624	4.94%
8	47.88	2055	1982	3.69%
10	47.67	1725	1673	3.09%
12	47.51	1540	1498	2.76%
14	47.39	1422	1387	2.55%
16	47.30	1342	1311	2.41%
18	47.22	1284	1255	2.30%
20	47.16	1240	1213	2.22%
22	47.11	1206	1181	2.16%
24	47.07	1179	1154	2.11%
26	47.03	1156	1133	2.07%
28	47.00	1138	1115	2.04%
30	46.97	1122	1100	2.01%
32	46.95	1108	1087	1.99%
34	46.93	1096	1075	1.97%
36	46.91	1086	1065	1.95%
38	46.89	1077	1057	1.93%
40	46.88	1069	1049	1.92%