Bidirectional Current Source Converter: Design, Control and Performance Evaluation

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***Abstract*—This paper investigates feasibility of a current source converter (CSC) for battery energy storage applications. An inherent feature of the converter is boosting of the DC-link voltage. We discuss the converter operation principle and choice of circuit parameters with effects on system performance. A model that includes switching harmonics is derived to predict accurate behavior of various voltages and currents. Using the model, the performance of the CSC is investigated for a range of practical operating conditions. A control scheme for regulating load current and DC-link voltage is proposed. The validity of both the model and control scheme is shown using simulation results of a 1 kW system.**

I. Introduction

Over the last couple of decades, several converter topologies and control schemes have become popular for various low to high power applications, including battery energy storage systems, and microgrids [3]–[8]. Several voltage source converters (VSCs) as listed in [9]–[11] have been developed for battery storage systems and can be configured as single-stage or two-stage systems. Each configuration has its own advantages and disadvantages. A systematic review already exists in the literature and, hence, these configurations are not further discussed. Current source converters (CSCs) have emerged in parallel to VSCs [12]–[14]. CSCs have recently become popular for both photovoltaic and energy storage applications, because of a low input current ripple, direct control of the input current and flexibility in connecting multiple power sources [15].

This paper investigates the performance of a CSC shown in Fig. 1 for battery energy storage applications. It should be noted that some work on similar converter topologies has been presented previously [16], [17], but this paper differs from the existing work in a number of ways. In particular, a detailed model of the CSC is presented to give an accurate insight into the behaviour of the converter. In comparison to existing models, which are based on the duty cycle and phase shift of the switches, the proposed model accounts for the harmonics of the switching signals. Furthermore, the presentation of the control scheme is generalised, making the converter suitable for various applications, such as high frequency motor drives and dual active bridge (DAB) based converters.

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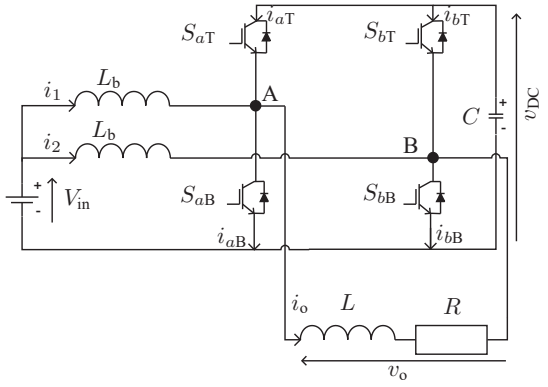

Fig. 1. Schematic of a bidirectional current source converter.

The CSC allows boosting of the supply voltage, V_in, to a higher DC-link voltage, v_DC, and then creation of a high frequency AC output voltage, v_o. A detailed analysis of the scheme showing how the performance of the converter is affected by the increased voltage is presented. With this scheme, the DC-link voltage and as a result the maximum output voltage increases, but the output power of the converter does not increase above its nominal value and this is shown using analytical solutions.

II. Bidirectional Current Source Converter

The setup of the single-phase bidirectional CSC under consideration is shown in Fig. 1. Here, a boost inductor, L_b, is connected in between a DC voltage source, V_in, and midpoint of switches $S_{r\mathrm{T}}$ and $S_{r\mathrm{B}}$, $r \in \{a, b\}$. Each phase-leg has its own inductor and this interleaving of two inductors minimises ripple in the supply current. Instead of using a single inductor, the interleaving lowers the current flowing through the switches and thus reduces current ratings of the switches. In each phase-leg, switch pair $S_{r\mathrm{T}}$ and $S_{r\mathrm{B}}$, and inductor L_b form a bidirectional converter, where the higher voltage appears across the DC-link capacitor, C. All the four switches and the capacitor form a full-bridge converter that is connected to a load comprising a resistor, R, and an inductor, L. The operation principle of the converter is given in the following paragraphs.

The normalized voltage references of the top and bottom switches can be defined as

$$u_{r\mathrm{T}} = \frac{1}{2}(1 + m_r), \quad r \in \{a, b\} \tag{1a}$$

$$u_{r\mathrm{B}} = \frac{1}{2}(1 - m_r), \quad r \in \{a, b\}, \tag{1b}$$

where m_r is the reference of the voltage at node r. It is clear from (1) that the average duty cycle of both the switches is 0.5. Using principles of a boost converter, the average DC-link voltage, therefore, is twice that of the supply voltage. The DC-link voltage, v_{DC}, however can be changed by manipulating the average duty cycle of each switch. Therefore, an offset term, $k \in [-1, 1]$, is added to the voltage reference of nodes A and B, as given below:

$$m_a = \frac{4\mathrm{M}}{\pi} \sum_{n=1}^{\infty} \frac{(-1)^{n-1}}{2n-1} \cos((2n-1)\omega t) + k \tag{2a}$$

$$m_b = \frac{4\mathrm{M}}{\pi} \sum_{n=1}^{\infty} \frac{(-1)^{n-1}}{2n-1} \cos((2n-1)\omega t - (2n-1)\theta) + k, \tag{2b}$$

where $\mathrm{M} \in [0, 1]$, and θ is the phase shift between the nodes. The modulation index, M, defines the maximum output voltage of the converter, v_{o}. It should be noted that the range of the reference values, m_a and m_b, is [-1, 1], otherwise, the converter enters a nonlinear overmodulation mode, which is known to generate low-order harmonics. Furthermore, the converter cannot produce the expected voltage if the reference values are outside the range. Therefore, the maximum modulation index, M, of the converter is limited to $\mathrm{M} = 1 - |k|$. The above references can easily be adapted for other modulation strategies, such as PWM, by dropping the $\frac{4}{\pi}$ term and using only a fundamental term, i.e. for $n = 1$, in (2).

The average duty cycle of the bottom switch, which determines the DC-link voltage, can be obtained by taking an average of its reference, $u_{a\mathrm{B}}$. The average value in phase a, for example, is given by

$$\overline{u_{a\mathrm{B}}} = \frac{1-k}{2}. \tag{3}$$

The average input voltage, V_{in}, and average DC-link voltage, V_{DC}, can be related to the average duty cycle, $\overline{u_{a\mathrm{B}}}$, by

$$\frac{1-k}{2} = 1 - \frac{V_{\mathrm{in}}}{V_{\mathrm{DC}}}, \tag{4}$$

which gives the relationship between the voltages and the offset term

$$V_{\mathrm{DC}} = \frac{2V_{\mathrm{in}}}{1+k}, \quad k \in [-1, 1]. \tag{5}$$

It is apparent from (5) that the lower limit of the DC-link voltage is equal to the input voltage when $k = 1$. The voltage boost ratio or ratio of the DC-link to input voltage is plotted in Fig. 1 for a range of k values. For a given input voltage, the DC-link voltage increases as the value of k decreases. In an actual system, however, the upper limit of the voltage is defined by various losses in the circuit.

This topology has two degrees of freedom for controlling the output voltage. Firstly, the output voltage can be controlled directly by the offset term, k, while keeping M at its maximum allowed value of $1 - |k|$. Secondly, for a given k, the voltage can be controlled by adjusting $\mathrm{M} < (1 - |k|)$.

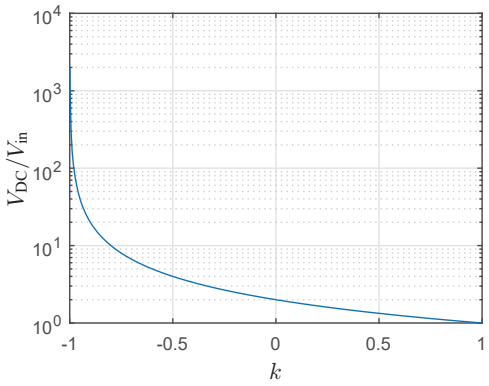

Fig. 2. Voltage boost ratio.

III. Model

It can be established using network analysis that there are three independent currents in the topology. Therefore, the load current, i_{o}, and boost inductor currents, i_1 and i_2, are chosen to be independent state variables, which can be related as follows:

$$L_{\mathrm{b}} \frac{\mathrm{d}i_1}{\mathrm{d}t} = -R_{\mathrm{b}} i_1 + V_{\mathrm{in}} - u_{a\mathrm{T}} v_{\mathrm{DC}} \tag{6}$$

$$L_{\mathrm{b}} \frac{\mathrm{d}i_2}{\mathrm{d}t} = -R_{\mathrm{b}} i_2 + V_{\mathrm{in}} - u_{b\mathrm{T}} v_{\mathrm{DC}} \tag{7}$$

$$L \frac{\mathrm{d}i_{\mathrm{o}}}{\mathrm{d}t} = -R i_0 + u_{a\mathrm{T}} v_{\mathrm{DC}} - u_{b\mathrm{T}} v_{\mathrm{DC}} \tag{8}$$

where R_{b} models the losses of the boost inductors. The state equation of the capacitor voltage is

$$C \frac{\mathrm{d}v_{\mathrm{DC}}}{\mathrm{d}t} = -\frac{v_{\mathrm{DC}}}{R_{\mathrm{c}}} + u_{a\mathrm{T}}(i_1 - i_0) + u_{b\mathrm{T}}(i_2 + i_0) \tag{9}$$

where R_{c} models the parasitic losses of the DC-link capacitor, C. The model of the converter is presented in Fig. 3. With this model, the switch pairs are replaced either by controllable voltage or current sources. The control input to the sources is the reference signal of the switches, $u_{a\mathrm{T}}$ and $u_{b\mathrm{T}}$.

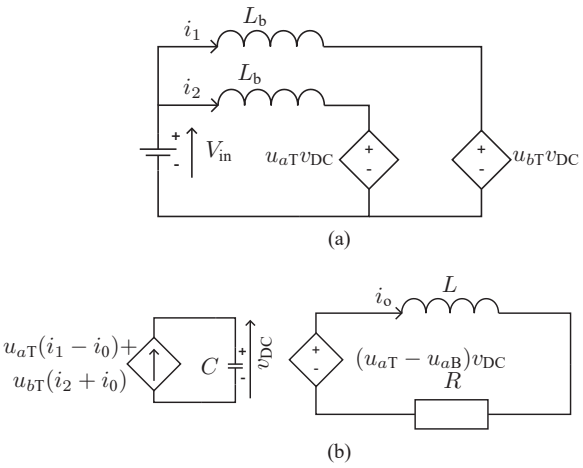

Fig. 3. Model of the bidirectional current source converter.

By ignoring $R_{\rm b}$, the differential equations can be solved to give the following expressions:

$$i_1 = \mathrm{I}_1 - \frac{2\mathrm{M}V_{\rm DC}}{\pi\omega L_{\rm b}} \sum_{n=1}^{\infty} \frac{(-1)^{n-1}}{(2n-1)^2} \sin((2n-1)\omega t) \tag{10}$$

$$i_2 = \mathrm{I}_2 - \frac{2\mathrm{M}V_{\rm DC}}{\pi\omega L_{\rm b}} \sum_{n=1}^{\infty} \frac{(-1)^{n-1}}{(2n-1)^2} \sin\Big((2n-1)\omega t - (2n-1)\theta\Big) \tag{11}$$

$$i_o = -\frac{4\mathrm{M}V_{\rm DC}}{\pi} \sum_{n=1}^{\infty} \frac{(-1)^{n-1}}{(2n-1)} \frac{\sin((2n-1)\frac{\theta}{2})}{\sqrt{R^2 + ((2n-1)\omega L,)^2}} \times \sin\big((2n-1)\omega t - (2n-1)\frac{\theta}{2} + \phi_{2n-1}\big) \tag{12}$$

where I_1 and I_2 are the average values of the boost inductor currents, and $\phi_{2n-1} = \tan^{-1}(-\frac{(2n-1)\omega L}{R})$. The variations of the DC-link voltage are ignored while deriving the above expressions, because such variations are relatively small with an appropriate selection of the capacitance C.

It is clear from (10) and (11) that the current through the boost inductors has both DC and AC components. The AC components have the same frequency as that of the output current. The magnitude of the AC components can be reduced by increasing the inductance, which increases the footprint of the converter. Alternatively, this can be reduced by increasing the frequency of the output current.

Because of the squared term, $(2n-1)^2$, in the dominator of (10) and (11), the magnitude of the higher order components is significantly smaller than that of the fundamental component. Therefore, the fundamental component can be used for selecting an inductance value. The peak-peak amplitude of the fundamental current component can be limited to a ratio x of the DC current and these quantities can be related as

$$\frac{x\mathrm{I}_1}{2} = \frac{2\mathrm{M}V_{\rm DC}}{\pi\omega L_{\rm b}}, \tag{13}$$

and from which inductance value can be derived after substituting (5) in (13) as $L_{\rm b} = \frac{1-|k|}{1+k}\frac{8V_{\rm in}}{\pi\omega x\mathrm{I}_1}$. For a converter with symmetrical component values, both I_1 and I_2 are equal, and hence an equivalent series resistance of the converter as seen by the DC source is $R_{\rm equ} = V_{\rm in}/(\mathrm{I}_1+\mathrm{I}_2) = V_{\rm in}/2\mathrm{I}_1$. Therefore, the inductance can also be written in terms of $R_{\rm equ}$ as

$$L_{\rm b} = \frac{1-|k|}{1+k}\frac{16R_{\rm equ}}{\pi\omega x}. \tag{14}$$

The above equation is used to calculate inductance values for various frequency and k values, and results are presented in Fig. 4. The inductance values are determined for x = 0.1 and represented as a percentage of the $R_{\rm equ}$. It is clear from (14) and Fig. 4 that inductance reduces as the frequency increases. With the given frequency, the inductance decreases by increasing the value of k. The reduction in the inductance value over k values is only observed when $k > 0$, because the modulation index is restricted to $1-|k|$. At higher frequencies, the weighting of the terms related to k is significantly smaller than that of the angular frequency, ω, and, therefore, further reduction in the inductance values is minimal over k values.

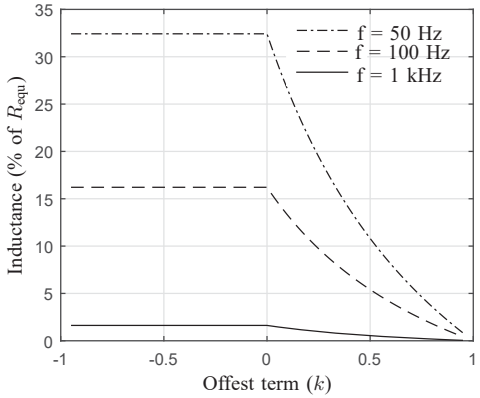

Fig. 4. Boost inductance for a range of frequency and offset term values.

The DC component of the inductor current is in proportion to the average output power, $\overline{\mathrm{P}}_{\rm o}$, and is given by

$$\mathrm{I}_1 = \mathrm{I}_2 = \frac{\overline{\mathrm{P}}_{\rm o}}{2V_{\rm in}}. \tag{15}$$

The output power, $P_{\rm o}$, of the converter is given by $P_{\rm o} = v_{\rm o}i_{\rm o}$ and for $v_{\rm o} = V_{\rm DC}(m_a - m_b)$, $P_{\rm o}$ is

$$P_{\rm o} = V_{\rm DC}(m_a - m_b)i_{\rm o}. \tag{16}$$

Substituting (2), (5) and (12) in (16), the following expression is derived

$$P_{\rm o} = 64\frac{(1-|k|)^2}{(1+k)^2}\frac{V_{\rm in}^2}{\sqrt{R^2+\omega^2L^2}}\sin^2(\frac{\theta}{2})\Big(\cos(\phi_1) - \cos(2\omega t - \theta - \phi_1)\Big). \tag{17}$$

Note that (17) is derived using the fundamental component of the load current i.e. for $n = 1$. As expected with the single phase converter and also evident from (17), the output power has both DC and second harmonic quantities. The output power is also a function of the offset term, k. The ratio of output to nominal power or power gain ratio is defined as $\frac{(1-|k|)^2}{(1+k)^2}$ and plotted in Fig. 5. Unlike the DC-link voltage, the power does not increase above its nominal value, $P_{o,\rm nom}$.

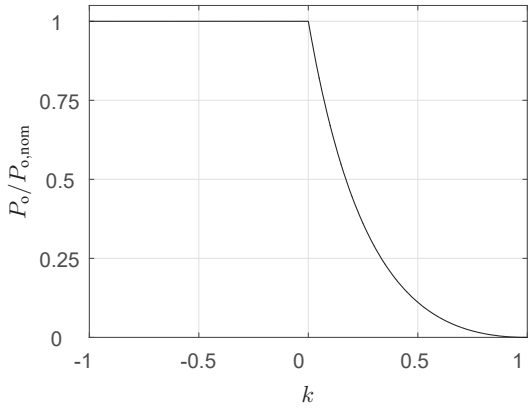

Fig. 5. Power gain ratio.

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The current supplied by the DC voltage source is obtained by adding (10) and (11) as

$$i_{\text{in}} = \text{I}_1 + \text{I}_2 - \frac{4\text{M}V_{\text{DC}}}{\pi\omega L_{\text{b}}} \sum_{n=1}^{\infty} \frac{(-1)^{n-1}}{(2n-1)^2} \cos\big((2n-1)\frac{\theta}{2}\big) \times \sin\big((2n-1)\omega t - (2n-1)\frac{\theta}{2}\big). \quad (18)$$

It is evident from (18) that the ripple of the source current is minimal for $\theta = \pm\pi$. The switch currents are given by

$$i_{a\text{T}} = -(i_1 - i_{\text{o}})u_{a\text{T}} \quad (19a)$$
$$i_{a\text{B}} = (i_1 - i_{\text{o}})u_{a\text{B}} \quad (19b)$$
$$i_{b\text{T}} = -(i_2 + i_{\text{o}})u_{b\text{T}} \quad (19c)$$
$$i_{b\text{B}} = (i_2 + i_{\text{o}})u_{b\text{B}}, \quad (19d)$$

Using a fundamental component of the load current and substituting (10) - (12) in (9), an expression for the capacitor voltage is derived (20).

IV. Control Scheme

A variant of the control scheme commonly used for DABs is proposed, where duty cycle is modified to control both the DC-link voltage and the load current. A block diagram of the scheme is shown in Fig. 6. One of the primary objectives of the scheme is to maintain RMS magnitude of the load current. A proportional-integral (PI) compensator is used to evaluate θ, where the error between the RMS load current, I_{o}, and its reference value, I_{ref}, is the input to the compensator.

A triangle wave generator generates the angle $\omega t \in [0,\ 360^\circ]$ at a frequency of 20 kHz, and the sine of the angle is used to determine the positive and negative halves of the load current waveform. The sine values in each phase-leg are then multiplied with M and added to k. This manipulated sine value when greater than or equal to zero gives the turn-on duration of the top switch, $S_{r\text{T}}, r \in \{a, b\}$.

The value of k is given by another PI compensator, which is used to maintain average DC-link voltage, V_{DC} around its reference value, $V_{\text{DC,ref}}$. Because the manipulated sine value is compared to zero, the range of k is limited to $[-0.5\ 0.5]$. The switches will either remain turned-on or -off if k is outside this range. It should be noted that this limitation can be overcome by employing a PWM strategy, where references are compared to carrier waveforms covering the entire range of $[-1\ 1]$.

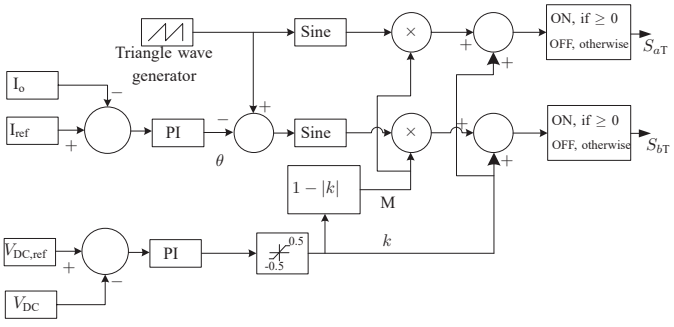

Fig. 6. Block diagram of the control scheme.

V. Simulations

The proposed control scheme as well as the mathematical model are validated using simulations of 1 kW CSC, as shown in Fig. 1. The parameters for the converter are given in Table I. For simulations, the control scheme is implemented in Matlab/SIMULINK software. The value of the k and θ is set to 0 and π, respectively. With this value of k, the voltage across the DC-link capacitor is twice of that the supply voltage. The waveforms that are produced using the proposed mathematical model include the first 100 harmonics.

TABLE I
Ratings and parameters of the converter used in simulations.

Ratings and parameters		
Power output	P_{o}	1 kW
Supply voltage	V_{in}	50 V
Boost inductance	L_{b}	100 μH
DC-link capacitance	C	100 μF
Load inductance	L	30 μH
Load resistance	R	5 Ω
Rated frequency	f_{rat}	20 kHz

Fig. 7 shows the waveforms of the boost inductor currents over 50 μs (one fundamental period). Both the modelled and simulated waveforms are similar in value and shape, demonstrating that the model is able to accurately describe low to high order harmonics of the currents. The waveform of the load current is shown in Fig. 8. Again, the two curves are very similar in shape and value, with the only slight difference occurring near the peak of the current.

The waveform of the DC-link voltage for one fundamental period is shown in Fig. 9. Since (20) does not account for higher order harmonics, there is a noticeable difference between model and simulation. However, since the peak-peak amplitude of the voltage is around 1.5% of the average value this difference has a minimal impact on average DC link voltage.

The RMS value of the load current, I_{o}, for a range of θ values is shown in Fig. 10, where the current waveform is symmetrical around $\theta = 0^\circ$. The RMS currents of the top, $\text{I}_{a\text{T}}$, and bottom, $\text{I}_{a\text{B}}$, switches of phase-leg a are also plotted in Fig. 10. Current through the bottom switch is higher than that of the top switch over the range of θ values considered. This uneven distribution of current among the switches is due to the DC current required for boosting the DC-link voltage. The load current and, as a result, DC value of the supply or boost inductor current increases with the magnitude of θ. Consequently, the unequal current distribution among the switches increases with the magnitude of θ. Furthermore, this also results in uneven distribution of switch power losses. The current through both the switches of phase-leg a is marginally similar when $\theta \in [-70^\circ\ 10^\circ]$, and similarly the current through the switches of phase-leg b, although not shown, is same when $\theta \in [-10^\circ\ 70^\circ]$.

Fig. 11 shows the average value of the supply current (18) for a range of θ values, where the current shows a similar trend to that of the load current shown in Fig. 10. The magnitude of the ripple current is also plotted for a range of considered

$$v_{\mathrm{DC}} = V_{\mathrm{DC}} - \frac{4\mathrm{M}^2 V_{\mathrm{DC}}}{C\pi^2\omega}\frac{\sin(2\omega t-\theta+\phi_1)}{\sqrt{(R^2+\omega^2L^2)}}\sin^2(\frac{\theta}{2}) + \frac{4\mathrm{IM}}{C\pi\omega}\sin(2\omega t-\frac{\theta}{2})\cos(\frac{\theta}{2}) + \frac{2\mathrm{M}(1+k)V_{\mathrm{DC}}}{L_{\mathrm{b}}\omega^2\pi C}\cos(\omega t-\frac{\theta}{2})\cos(\frac{\theta}{2}) + \frac{2\mathrm{M}^2 V_{\mathrm{DC}}}{L_{\mathrm{b}}\omega^2\pi^2 C}\cos(2\omega t-\theta)\cos(\theta). \quad (20)$$

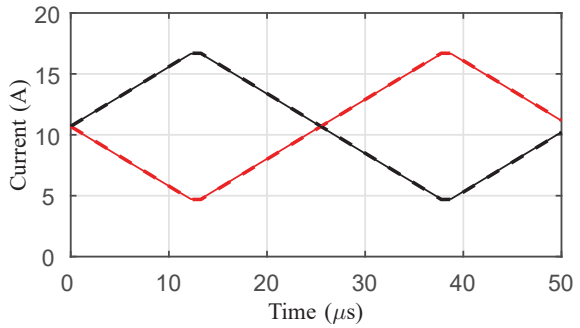

Fig. 7. Boost inductor currents with simulations (solid lines) and model (dashed lines).

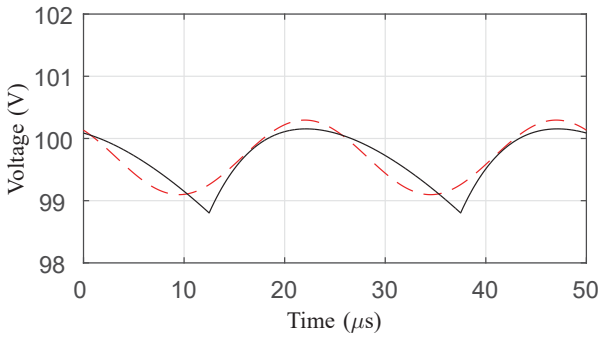

Fig. 9. DC-link voltage with simulations (solid line) and model (dashed line).

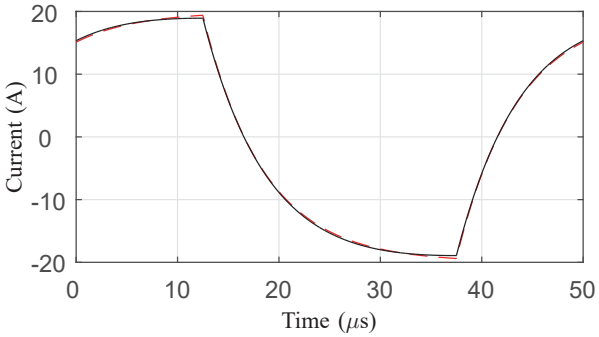

Fig. 8. Load current with simulations (solid line) and model (dashed line).

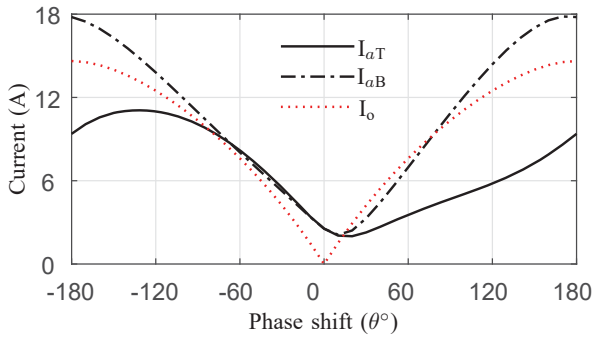

Fig. 10. RMS load and switch currents in phase-leg a for a range of θ values.

points. As described in section III that the ripple current increases as θ approaches zero in (18), where its peak value is limited by the reactance and resistance of the boost inductors. Although the average value of the current is zero with $\theta = 0°$, the increased ripple can have detrimental effects on the battery, if used as a voltage source. This ripple can be reduced by increasing the boost inductance, which increases the footprint of the converter, or by the resistance, which can compromise the efficiency. Therefore, the converter should be operated using a θ value close to $\pm 180°$. Alternatively, the ripple can be reduced by increasing the operating frequency of the converter.

Simulations are also carried out for a conventional topology without boost inductors and where DC-link capacitor is replaced with a voltage source. The control scheme as described for the CSC is also used for the conventional topology. It should be noted that the DC-link voltage is 100 V, allowing direct comparison between both the topologies.

The RMS current of top and bottom switches in phase-leg a and load current is shown in Fig. 12. The currents through the switches of phase-leg b are identical to that of phase-leg a and are not shown in the figure. In comparison to Fig. 10, the switches of the conventional topology carry less current. Furthermore, currents are evenly distributed over the range of phase delays, because of the absence of DC current that is required with the proposed CSC.

The average and ripple current supplied by the DC-link is shown in Fig. 13. In comparison to the CSC, the ripple current is significantly higher when converter supplies full power i.e. with $\theta = \pm 180°$. If a battery is connected directly across the DC-link, then it has to supply this ripple current. However, the current ripple is significantly lower with the CSC.

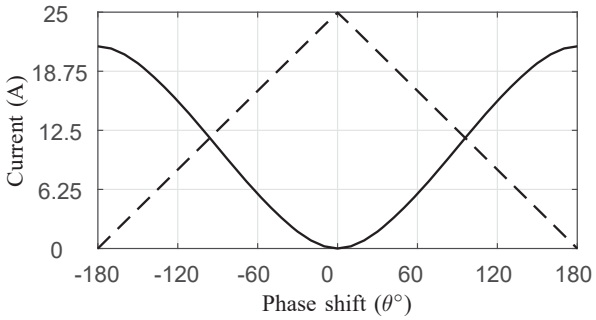

Fig. 11. DC supply current: average (solid line) and magnitude of the ripple current (dashed line) for a range of θ values.

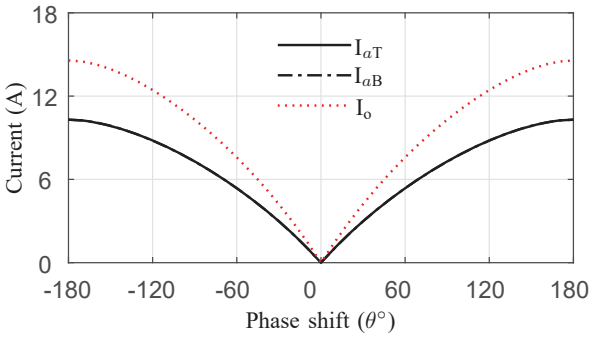

Fig. 12. RMS load and switch currents in phase-leg a for a conventional topology.

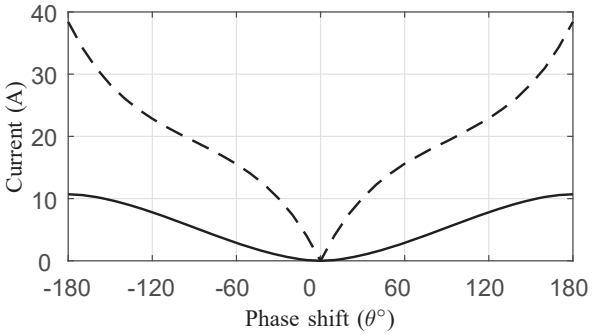

Fig. 13. DC supply current: average (solid line) and magnitude of the ripple current (dashed line) for a conventional topology.

VI. Possible Applications of the CSC

This current source converter is suitable for DAB converters that are connected to batteries, where battery voltage drops with the state of charge of a battery. With an appropriate control scheme, the DC-link voltage, and as a result, the output voltage of the converter can be regulated for a varying battery voltage.

Another feature of the topology is that the maximum output voltage of the converter can be increased while keeping the modulation index in the linear operating range. The converter, therefore, does not enter the nonlinear overmodulation range, and in the case of a PWM strategy the number of pulse transitions in the output voltage are not affected. This feature makes the converter suitable for high frequency motor drives.

VII. Conclusions

A generalised mathematical model is derived to accurately predict the behaviour of a current source converter. The accuracy of the model is improved by including harmonics of switch inputs as well as circuit parameters. It has been shown that each phase-leg of the converter can be modelled as a controllable voltage source, which is a function of the DC-link voltage and switch inputs. Detailed analysis of the converter shows that the DC-link voltage can be increased by adding an offset to the voltage reference of each phase leg. Design guidelines for selecting the circuit parameters are given to achieve appropriate performance of the converter. Simulated results for a 1-kW converter demonstrate the feasibility of the model, which is then used to estimate current rating of the switches for a range of operating conditions.

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