

Saw damage gettering for industrially relevant mc-Si feedstock

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The silicon photovoltaic industry is currently shifting towards lightly doped emitters. These have electrical properties that benefit solar cells, compared to the traditional heavily doped emitters. This move brings new challenges as gettering efficiencies of impurities are lowered as the doping reduces. This is particularly problematic in multicrystalline silicon (mc-Si) since cell performance is typically boosted by the effective gettering of such impurities. In prior work we proposed the novel gettering technique, Saw Damage Gettering (SDG), which improved effective carrier lifetime of standard performance mc-Si red zone material. In this work we expand the study of SDG to various types of industrially relevant mc-Si: Upgraded Metallurgical Grade (UMG), high

performance bottom red zone (HPRZ), and diamond sawn high performance (DHP). The optimal condition for SDG is found to be an annealing temperature of 850 °C. With this condition it was demonstrated that the effective carrier lifetime can be increased in all silicon types upon SDG. The largest increase was observed for HPRZ material by a factor of 10, and the largest final effective lifetime post SDG was that of UMG, with $\tau_{eff} = 61.3 \mu s$. SDG is a potentially viable gettering method to work in conjunction with lightly doped emitters in removing the impurities of mc-silicon feedstock and thus improving the efficiency of cells made therefrom.

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1 Introduction

1.1 Motivation Silicon solar cells account for ~ 90% of the photovoltaics (PV) market [1]. Although monocrystalline silicon allows more efficient cells to be manufactured, the majority of solar cells use multicrystalline silicon (mc-Si). It is considerably easier and cheaper to manufacture due to the casting method employed [2][3]. However, this production method comes at a cost in the final device performance [4]. This is a result of increased recombination in the bulk due to the presence of crystallographic defects, such as grain boundaries and dislocations, as well as a larger concentration of impurity atoms in comparison with monocrystalline material [5][6].

The impurities of greatest interest are the transition metals. These are known to be effective recombination sites [5]. Therefore it is vital to reduce their concentration within the active regions of silicon devices. As transition metals have very low segregation coefficients between solid and liquid silicon [7], they preferentially remain within

the liquid silicon [8]. As a result, during casting of multicrystalline ingots the highest concentration of these impurities is found at the top of the ingot [8], i.e. the last section to solidify [9]. Impurities also diffuse into the melt from the crucible wall, at the edges and bottom of the ingot [9]. These low purity sections are termed ‘red zone’ regions. They exhibit a poor minority carrier lifetime, and are thus currently discarded by the solar cell manufacturing industry. This wasted, or necessarily reprocessed, material can account for up to 20% of the ingot [10].

1.2 Gettering Techniques Post-casting processes are employed to increase the quality of silicon by reducing the harmful effects of impurities and defects as carrier recombination centres. These processes are termed gettering. With regards to transition metals in the bulk, high temperatures can be used to allow impurities to diffuse to less critical regions of the wafer where they can either be removed, or where they can re-precipitate and thus the impact of their recombination activity is greatly reduced.

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Table 1 Sample parameters.

Supplier	Type	Bottom Red Zone	Thickness (μm)	Resistivity ($\Omega\text{ cm}$)	Sample Size (cm)
A	Standard Red Zone	Yes	180	1-3	4.15×4.15
B	Upgraded Metallurgical Grade (UMG)	No	195	1-2	3×3
C	High Performance Red Zone (HPRZ)	Yes	195	2-4	3×3
D	Diamond sawn High Performance (DHP)	No	195	1-2	3×3

The most common form of gettering is Phosphorus Diffusion Gettering (PDG), as it can also form the emitter layer for solar cells whilst gettering. It is deposited via either a gas phase source (POCl_3), or spin on techniques (H_3PO_4), with a subsequent thermal treatment applied to cause impurities to diffuse to the phosphorus layer, where they have increased solid solubility.

Whilst having a heavy diffusion of phosphorus in to the surface would seem the obvious choice to maximise gettering efficiency, such a heavy emitter also forms a “dead layer” at the surface, where the electrical properties are compromised due to the heavy doping. In addition the high concentration of dopants and precipitates in heavily doped emitters contribute significantly to device recombination currents [11]. These effects are detrimental to solar cell efficiency, and thus there is a trend of moving to more lightly doped emitters to avoid this effect [12]. Lighter doping has been observed to reduce the efficacy of PDG, presumably due to the reduction in the number of suitable sites to which impurities segregate [11]. Alternate gettering mechanisms need to be considered to be used in conjunction with PDG in light emitters [13]. Such processing will be particularly applicable to wafers which are more heavily contaminated such as the red zone material described above.

One such method has been proposed in prior work [14], and termed Saw Damage Gettering (SDG). This is a simple and effective gettering method. It utilises the damage introduced at the silicon surface from the wire-sawing process as gettering centres. Wafers are heated to a sufficiently high temperature so that most metal precipitates dissolve and the impurities homogenise throughout the wafer. The wafer is then cooled so that the impurities become supersaturated. The saw damage at the surface includes cracks and dislocations which provide excellent nucleation sites for impurity precipitates which, on cooling, form in this region preferentially compared to the bulk of a wafer. These precipitates can then be readily removed from the wafer by etching the damaged surface region - a process which must, in any case, be performed. By reducing the number of impurity atoms in the bulk, the quality of the silicon material can be improved. This makes silicon which

previously contained high impurity concentrations appropriate for solar cell production. However, SDG must overcome other competing sites for precipitate nucleation in the bulk of a wafer, such as grain boundaries and dislocations, to ensure impurities precipitate at the surface and are thus removed.

1.3 Materials Multicrystalline silicon (mc-Si) for solar cells is continually evolving, with new materials being developed to deliver lower costs and increased performance. The materials most of interest for this study are those containing high impurity concentrations. In particular, upgraded metallurgical-grade silicon and red-zone material. Upgraded metallurgical-grade (UMG) Si has higher purity than metallurgical grade (MG) but is inferior to that of conventionally purified silicon. Metallurgical methods are used to purify MG mc-Si as opposed to the Siemens process for purification [15], which reduces energy expenditure. Several methods can be used in conjunction to remove different impurities from the silicon to produce improved purity overall [16]. Regardless of the metallurgical purification used, the impurity content of UMG is still greater than standard solar grade silicon. Gettering methods are thus highly advantageous to improve UMG quality for solar cell applications [17].

While SDG has been seen to be effective on standard red-zone material it is also important to demonstrate it on new high performance silicon. High Performance mc-Si (HP mc-Si) has increased electrical performance over MG and UMG Si and has set two new world records, the most recent with an efficiency of 21.25% [18][19]. HP mc-Si performs better due to the reduced content of dislocations and increased content of relatively electrically inactive grain boundaries [20]. Not only has the 21% efficiency barrier been broken for mc-Si but it was done using low-cost techniques that can be incorporated into production.

The production of HP mc-Si is achieved by adjusting the cooling rate to achieve a greater number of preferential grain boundaries which are coherent and also electrically inactive [20]. Smaller grains are grown to reduce the thermal stress within the grain and therefore the number of dislocations [20][21].

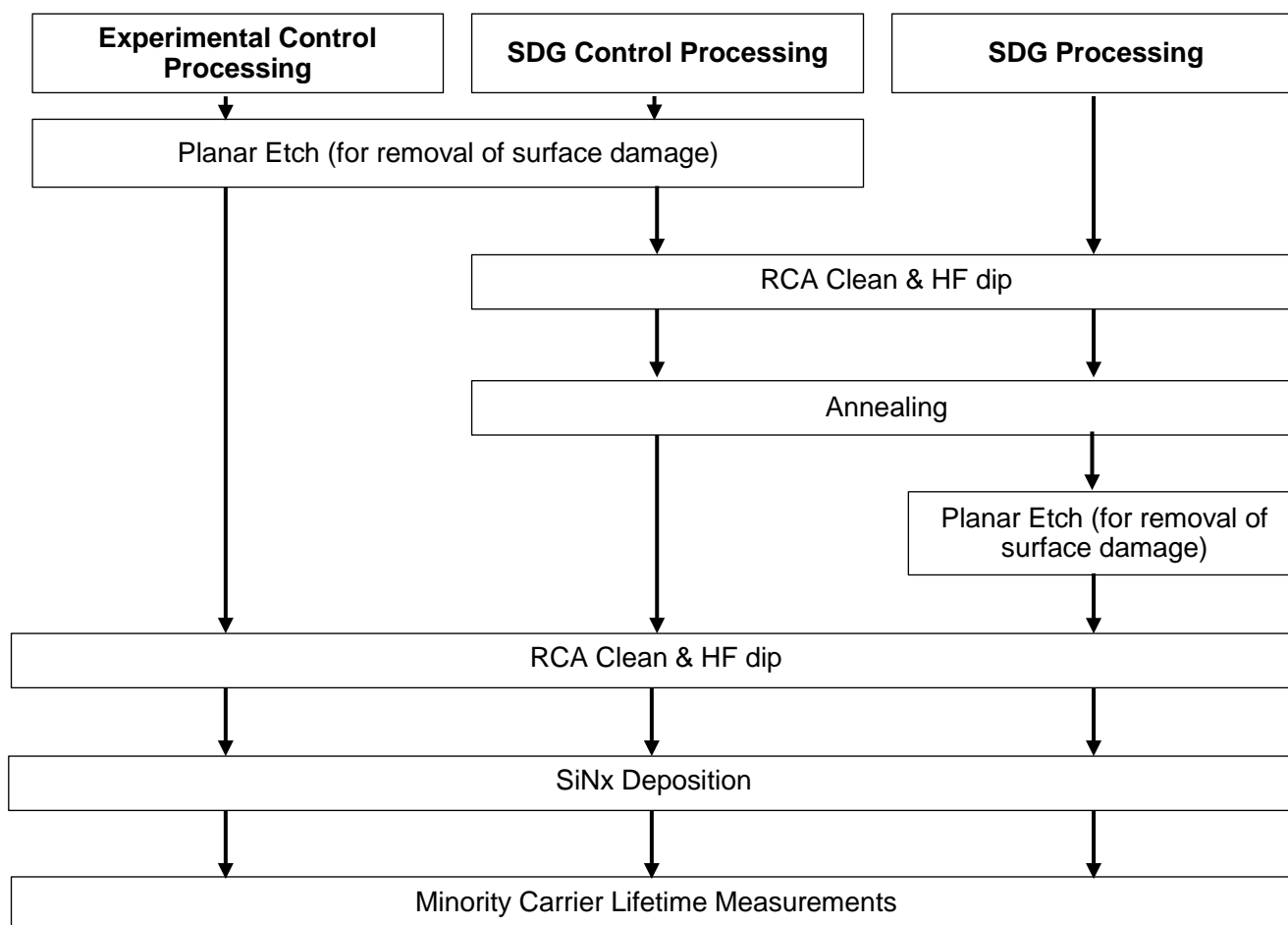


Figure 1 Processing routes for the three sister wafers in each group

Another recent development in the fabrication of multicrystalline wafers is the use of diamond wire-sawing. This technology is becoming increasingly popular compared to traditional slurry based methods since it wastes less material [12]. This trend is most prominent in monocrystalline silicon, but uptake has been slow for multicrystalline silicon due to difficulties with achieving acceptable surface textures [22][23]. For SDG the reduced damage from the diamond wire sawing process may impact the number of damage related gettering sites and hence reduce its effectiveness.

In this paper, the effectiveness of SDG on different types of mc-Si is demonstrated. These include standard performance mc-Si red zone material, seeded cast Upgraded Metallurgical Grade Silicon (UMG), high-performance red zone mc-Si (HPRZ), and diamond sawn high-performance mc-Si (DHP).

2 Experimental methods

Saw damage gettering has been performed on four types of mc-Si. For each type of mc-Si a test specimen for SDG was accompanied by two controls. The three wafers were taken from immediately adjacent positions in the ingot so as to have similar defect and impurity distributions.

Such wafers are called sister wafers. The first control had all saw damage removed before the anneal – so removing any effect of the saw damage on gettering. This is referred to as the “No-SDG” control. The second control, referred to as the “As-Cast” control had all saw damage removed but was not annealed, thus retaining the distribution of impurities from casting. The SDG processed wafers were annealed and then had the saw damage, together with the impurities gettering to the saw damage, etched away. The full processing for each wafer is outlined in Figure 1 and the parameters of each wafer are outlined in Table 1.

For each material, four 3 x 3 cm² specimens were cut from adjacent wafers within the ingot. Due to the quantity of material available, for standard performance red zone material anneals were only performed at 850 °C. For UMG samples, a region was chosen containing both single crystal and multicrystalline regions, thus only one sample per wafer was tested, at both 850 °C and 900 °C.

Saw damage removal was performed using a planar etch of buffered hydrofluoric, nitric, and acetic acid in 1:3:7 ratio, at room temperature. Samples were etched until 12 µm - 20 µm had been removed from each side of the surface, depending on the wafer type. Before annealing,

wafers were subject to an RCA clean followed by a hydrofluoric acid dip. All equipment that was used to handle the wafers also underwent RCA cleaning. The furnace was stabilised for at least 20 minutes before annealing and had a continual flow of 1 litre/minute of nitrogen gas to reduce oxidation of the wafers. Wafers were loaded into a quartz boat for annealing in the furnace and were pushed straight into the hot zone at the beginning of the anneal.

An example of the furnace thermal profile is shown in Figure 2. The continual change in thermal gradient is to ensure that the characteristic impurity diffusion length (for iron) at all temperature segments is equal.

Starting with equation (1) for diffusion length:

$$L = (Dt)^{1/2} \quad (1)$$

where L is the characteristic diffusion length, t is the time since diffusion began, and D is the diffusion coefficient which is taken for iron and is calculated using :

$$D = D_0 \exp(E_a/kT(t)) \quad (2)$$

Where $D_{Fe} = 1.3 \times 10^{-3} \exp(-0.68[\text{eV}]/kT) \text{ cm}^2\text{s}^{-1}$ [24]. By substituting (2) into (1) and differentiating with respect to time:

$$\frac{dL}{dt} = \sqrt{D_0 e^{-E_a/kT(t)}} \left(\frac{1}{2\sqrt{t}} + \frac{1}{2} \left(\frac{E_a}{kT(t)^2} \right) T'(t) \sqrt{t} \right) \quad (3)$$

An exponential cooling rate was used of the form:

$$T(t) = T_0 \exp(-\lambda t). \quad (4)$$

Substituting (4) into (3) with the requirement that $\frac{dL}{dt} = 0$:

$$\lambda = \left(\left(\frac{k}{E_a t} \right) T_0 e^{-\lambda t} \right) \quad (5)$$

This can be evaluated iteratively with a constant timestep Δt . In this work the factor $(k/E_a \Delta t)$ was taken to be $7 \times 10^{-7} \text{ s}^{-1}$ [25]. Full details of the mathematical treatment can be found in [25]. Samples were removed from the furnace when the temperature reached 500°C . Due to the exponential dependence of diffusion on temperature, gettering below this temperature was deemed insignificant.

After the anneal, the saw damage was etched from the samples where it was still present. All samples were then RCA cleaned and underwent a HF dip. Silicon nitride (SiN_x) was then deposited on both sides of the silicon to act as a passivation layer. This was performed using Plasma Enhanced Chemical Vapour Deposition (PECVD), in an Oxford Instruments PlasmaLab 80+ reactor. The recipe was optimised following the findings in reference [26]. Gas flow rates of ammonia, silane, and nitrogen were set to 20, 400, and 600 sccm, and a pressure of 400 mTorr, with the sample held at 400°C . A set of p-type float zone wafers, $\sim 2 \text{ }\Omega\text{cm}$ and $200 \text{ }\mu\text{m}$ thick, were used to optimise the SiN_x deposition. A 70 nm layer was deposited and, in the optimal passivation layer, a minority carrier lifetime exceeding

$150 \text{ }\mu\text{s}$ was measured at a minority carrier density (Δn) of 10^{15} cm^{-3} . This is sufficient to distinguish the changes in bulk lifetimes for mc-Si. Minority carrier lifetimes were tested using a WCT-120 Sinton Lifetime tester in Generalised (1/1) mode [27]. Effective lifetimes are reported at an injection level of 10^{15} cm^{-3} .

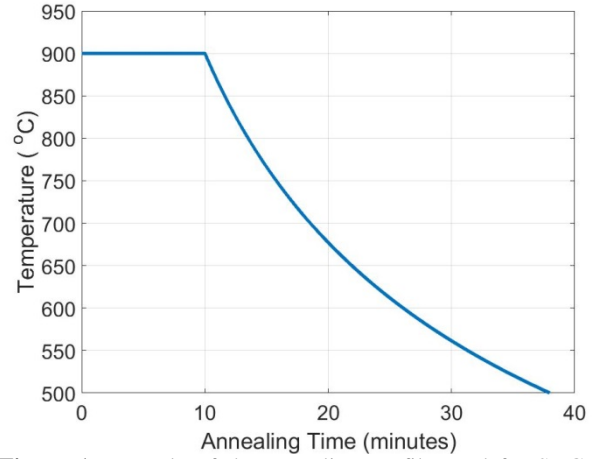


Figure 1 Example of the annealing profile used for SDG processing.

Spatial photoluminescence (PL) imaging was used to determine regions of high and low recombination activity within samples. A BTi imaging LIS-R1 photoluminescence tool was used with 1 sun illumination and a 1 second exposure time. To deconvolute images and reduce photon smearing a Point Spread Function (PSF) was used in the MATLAB software PL Pro [28].

3 Results and discussion

Figure 3 shows the resulting average effective lifetime for SDG and all control specimens. Four samples of each material type were tested at 850°C and 900°C , except for UMG in which only one sample was used. It is clear that for standard performance bottom red zone material SDG is very effective. The technique is seen to increase the effective lifetime by up to a factor of 1.7 compared with the As-Cast control, with the highest increase in effective lifetime of $34 \text{ }\mu\text{s}$. Gettering was also effective in HPRZ, despite the increased number of grain boundaries in the bulk [21]. The increased number of defects would cause a high quantity of impurities released across the material at higher temperatures. Some of these impurities may getter back to the grain boundaries and thus not be removed from the material. Not only will this increase recombination activity at the grain boundaries and lower the minority carrier lifetime but as they are not removed from the material they have the potential to be re-released in to the bulk on subsequent thermal processing. The largest increase in effective lifetime was by a factor of ~ 10 for HPRZ, equivalent to an absolute increase of $37 \text{ }\mu\text{s}$ for gettering at 850°C . The average effective lifetime and average increase in effective life-

Table 2 Comparison of average effective lifetime and average increase in effective lifetime between materials after SDG. Increases in lifetime are between the SDG samples and the SDG controls.

Material Type/ Gettering Temperature	Average Lifetime (μs)		Average Increase in Lifetime (μs)	
	850 °C	900 °C	850 °C	900 °C
Standard Performance Bottom Red Zone	37	-	30	-
UMG	61*	39*	45*	21*
HPRZ	36	36	32	33
DHP	53	48	27	16

* UMG material only had one sample for each group thus the values given for UMG are from one sample only.

time after gettering, for each sample set, is shown in table 2.

It was also observed that wafers subjected to the high temperature treatments without a saw damage layer experienced a reduction in lifetime, in comparison to the As-Cast controls that did not undergo thermal processing.

This may be attributed to dissolution of impurities from grain boundaries, dislocations and precipitates to the bulk material. If these are not subsequently gettered they may exist as interstitial impurities or form smaller precipitates in the intra-grain regions, leading to increased recombina-

tion activity [6]. In the UMG material, on the other hand, the effective lifetime after thermal processing slightly increased compared to the As-Cast control, perhaps indicating that, for the monocrystalline regions in the UMG, slight gettering to the wafer surface occurs even in the absence of saw damage. It should be noted that, in a solar manufacturing line, wafers undergo thermal processing at maximum temperatures ~ 850 °C. Hence the samples SDG processed at ~ 850 °C should not release substantially more impurities on further processing, moreover their cleanliness will be further improved by whatever effect PDG and any

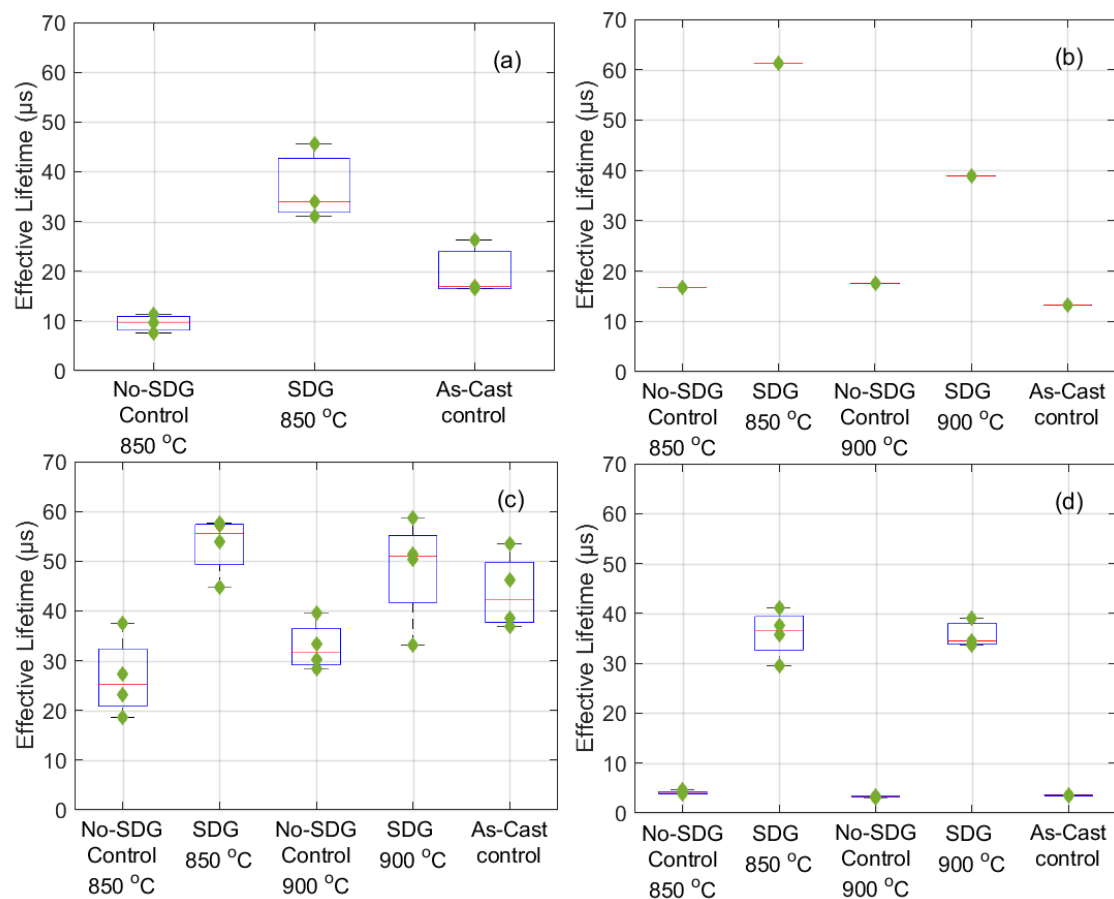


Figure 2 Effective lifetime results for a) standard performance bottom red zone b) UMG c) DHP d) HPRZ . All effective lifetimes are reported for injection levels of 10^{15} cm^{-3} .

subsequent aluminium gettering have.

From Figure 3, annealing at 850 °C is seen to be more effective than at 900 °C. One explanation proposed to account for this [14], is that at the higher temperature some of the saw damage is annealed away so reducing its effectiveness as a site for precipitate nucleation on cooling. An alternative explanation is that at the higher temperature some precipitates release significant quantities of slow diffusing impurities, such as titanium, which on cooling diffuse too slowly to be effectively gettering to the saw damage region. They thus remain distributed in the bulk of the wafer as electrically active recombination centres.

If the results of SDG for 850 °C are compared to those for a PDG process [29], it can be seen that the improvements that SDG produces are not as good but are of a similar magnitude. The initial lifetime prior to PDG was 2.92 μ s and effective lifetime improvements, are in the range of 10.15 μ s - 87.96 μ s. The effective lifetime improvements reported in this paper, from SDG, are in the range 5 μ s - 45 μ s. It is also worth noting that, for PDG, there is a severe drop off in effective lifetime between results for 900 °C and those for 950 °C. This can be attributed to α -FeSi₂ forming at approximately 920 °C which has high binding energies [29]. It is noted that it is envisaged that if SDG is used in an industrial context the SDG would be followed by PDG and the gettering processes would, to some extent, be additive.

With regards to DHP, SDG still provides an increase in lifetime, but not to the same degree as that of the other material types. This effect can be attributed to the reduction in the quantity of saw damage at the surfaces, thus reducing the number of gettering sites for impurities to precipitate at. However, it is clear that even with the reduced damage present in DHP material, SDG is still effective. The extent to which the SDG process works will depend on the amount of dissolution of impurity precipitates in the bulk and subsequent impurity diffusion to the surface. This in turn will depend on the length of time the material is held at elevated temperature and the subsequent cooling rate. These parameters were not investigated in the present work and so the process described here should not be considered fully optimised.

Photoluminescence results for UMG are presented in Figure 4. Lighter regions within the images correspond to low recombination activity and dark regions to high recombination activity. With regard to SDG, the light regions indicate a reduction in impurity concentration and therefore an increase in lifetime. Figure 4 c) and e) confirm that SDG is most effective when performed at 850 °C, rather than 900 °C. This is evident because there is a greater quantity of lighter regions than in the corresponding controls, figure 4 b) and d), and thus a greater reduction in recombination activity.

When comparing SDG samples to their No-SDG controls, the greatest reduction in recombination activity is found in sections of the wafer where there are predomi-

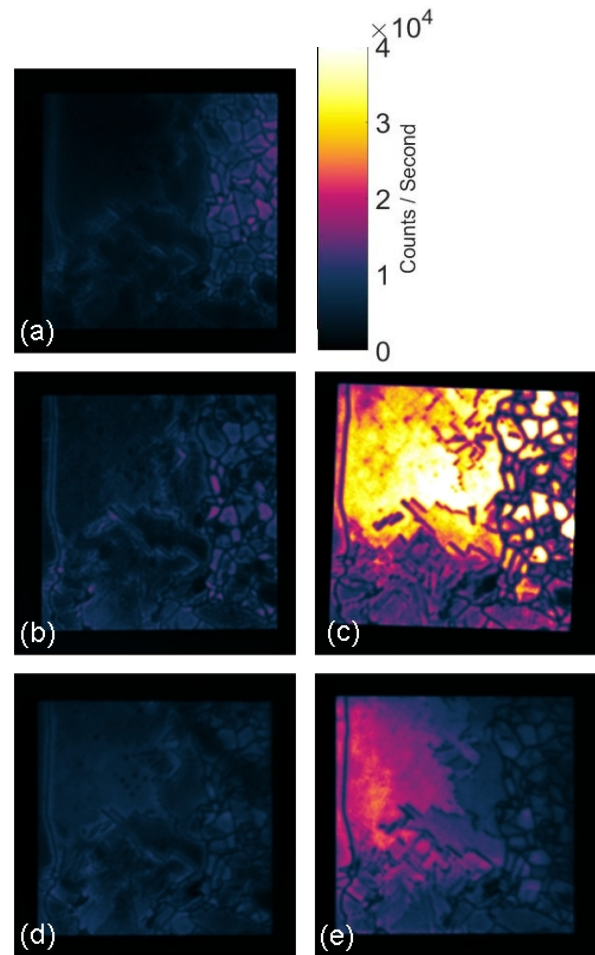


Figure 4 Photoluminescence images of UMG samples, a) As-Cast Control, b) 850 °C No-SDG Control, c) 850 °C SDG, d) 900 °C No-SDG Control, e) 900 °C SDG.

nantly mono-like characteristics. Thus, the largest mono-like section (the top left of the SDG samples, figs c) and e)), shows the greatest reduction in recombination when compared to the No-SDG control for 850 °C. Some smaller grains also exhibit great improvement in their recombination activity between No-SDG and SDG at 850 °C. This is potentially due to the different quantity and types of defects present within the grain compared to other small grains which yield poorer lifetimes. Further investigation in to the crystallographic structure of the grains is required to determine the nature of the difference of recombination activity.

4 Conclusions

Saw Damage Gettering (SDG) has been shown to increase substantially effective carrier lifetime in a variety of industrially relevant mc-Si materials. These materials, which because of their high impurity concentration, were previously thought not suitable for solar cell manufacture, might be re-integrated into the processing line after a SDG

process. This includes red zone material that would otherwise have been discarded from manufacture of solar cells. The largest increase in lifetime was seen on High Performance red zone material, when annealed at 850 °C. Effective lifetime increased by a factor of ~10 from 4 μs to 41 μs. The highest effective lifetime post gettering was found in Upgraded Metallurgical Grade material treated at 850 °C yielding a lifetime at 61 μs. It has also been shown that SDG is effective on Diamond Sawn High Performance material, albeit with a reduction in efficacy. This reduction likely comes from the reduced surface damage.

The dissolution of impurities in the bulk of the wafer and their ability to diffuse, whilst cooling, to damage precipitation sites are important factors in process optimisation. In the present work, dissolution at 850 °C followed by at least a 35 minute exponential cool is shown to be a viable process for improving silicon containing high concentrations of impurities.

Future work on this topic would include determining whether SDG works in conjunction with PDG, particularly light diffusions as this is what industry is moving towards.

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References

- [1] B. Burger, K. Kiefer, C. Kost, S. Nold, S. Philipps, R. Preu, J. Rentsch, T. Schlegel, G. Stryi-Hipp, G. Willeke, H. Wirth, I. Brucker, A. Haberle, and W. Warmuth, "Photovoltaics Report," Freiburg, 2016.
- [2] D. Sarti and R. Einhaus, "Silicon feedstock for the multicrystalline photovoltaic industry," *Sol. Energy Mater. Sol. Cells*, vol. 72, no. 1–4, pp. 27–40, Apr. 2002.
- [3] L. Frantzis, E. Jones, A. D. Little, C. Lee, M. Wood, and P. Wormser, "Opportunities for cost reductions in photovoltaic modules," in *Proceedings of the 16th European PVSEC*, 2000.
- [4] K. Arafune, T. Sasaki, F. Wakabayashi, Y. Terada, Y. Ohshita, and M. Yamaguchi, "Study on defects and impurities in cast-grown polycrystalline silicon substrates for solar cells," *Phys. B Condens. Matter*, vol. 376, pp. 236–239, 2006.
- [5] M. A. Green, *Silicon Solar Cells Advanced Principles & Practice*. Sydney: Centre for Photovoltaic Devices and Systems, 1995.
- [6] A. A. Istratov, T. Buonassisi, R. J. McDonald, A. R. Smith, R. Schindler, J. A. Rand, J. P. Kalejs, and E. R. Weber, "Metal content of multicrystalline silicon for solar cells and its impact on minority carrier diffusion length," *J. Appl. Phys.*, vol. 94, no. 97, 2003.
- [7] H. Lemke, "Substitutional transition metal defects in silicon grown-in by the float zone technique," *Mater. Sci. Forum*, vol. 196–201, no. pt 2, pp. 683–688, 1995.
- [8] A. Laugier, E. Borne, H. E. Omari, G. Goaer, and D. Sarti, "Transient thermal effects into a 155 kg POLIX ingot," *Conf. Rec. Twenty Fifth IEEE Photovolt. Spec. Conf.*, pp. 609–612, 1996.
- [9] G. Coletti, "Impurities in silicon and their impact on solar cell performance," *Dr. Thesis*, p. 114, 2011.
- [10] G. Zhong, Q. Yu, X. Hunag, and L. Liu, "Influencing factors on the formation of the low minority carrier lifetime zone at the bottom of seed-assisted cast ingots," *J. Cryst. Growth*, vol. 402, pp. 65–70, 2014.
- [11] H. Li, K. Kim, B. Hallam, B. Hoex, S. Wenham, and M. Abbott, "POCl₃ diffusion for industrial Si solar cell emitter formation," *Front. Energy*, vol. 11, no. 1, pp. 42–51, Mar. 2017.
- [12] S. I. Association, "International Technology Roadmap for Semiconductors," 2016.
- [13] M. Kim, P. Hamer, H. Li, D. Payne, S. Wenham, M. Abbott, and B. Hallam, "Impact of thermal processes on multi-crystalline silicon," *Front. Energy*, vol. 11, no. 1, pp. 32–41, Mar. 2017.
- [14] G. F. Martins, P. MacDonald, T. Burton, R. S. Bonilla, and P. R. Wilshaw, "Saw Damage Gettering for Improved Multicrystalline Silicon," *Energy Procedia*, vol. 77, pp. 607–612, 2015.
- [15] O. Mara W.C., Herring R.B., Hunt I.P., *Handbook of Semiconductor Silicon Technology*. Noyes Publications, 1990.
- [16] G. Tranell, J. Safarian, and M. Tangstad, "Processes for Upgrading Metallurgical Grade Silicon to Solar Grade Silicon," *Energy Procedia*, vol. 20, no. January 2017, pp. 88–97, 2012.
- [17] S. Y. Yoon, J. Kim, and K. Choi, "Gettering of Metal Impurities by Using Phosphorus Diffusion in UMG Silicon Wafers," *J. Korean Phys. Soc.*, vol. 60, no. 12, pp. 2079–2082, 2012.
- [18] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, E. D. Dunlop, D. H. Levi, and A. W. Y. Ho-Baillie, "Solar cell efficiency tables (version 49)," *Prog. Photovoltaics Res. Appl.*, vol. 25, no. 1, pp. 3–13, 2016.
- [19] Trina Solar, "Press Releases | Trina Solar Announces New Efficiency Record of 21.25% Efficiency for Multi-Crystalline Silicon Solar Cell," 2015. [Online]. Available: <http://ir.trinasolar.com/phoenix.zhtml?c=206405&p=irol-newsArticle&ID=2110256>. [Accessed: 28-Feb-2017].
- [20] Y. M. Yang, A. Yu, B. Hsu, W. C. Hsu, A. Yang, and C. W. Lan, "Development of high-performance multicrystalline silicon for photovoltaic industry," *Prog. Photovolt. Res. Appl.*, vol. 23, no. 3 (2015), pp. 340–351, 2015.
- [21] P. Krenckel, S. Riepe, F. Schindler, and T. Strauch, "Optimized grain size of seed plates for high performance multicrystalline silicon," in *32nd European PV Solar Conference and Exhibition*, 2016.
- [22] U. Gangopadhyay, S. K. Dhungel, P. K. Basu, S. K. Dutta, H. Saha, and J. Yi, "Comparative study of different approaches of multicrystalline silicon texturing for solar cell fabrication," *Sol. Energy Mater. Sol. Cells*, vol. 91, no. 4, pp. 285–289, 2007.
- [23] P. Panek, M. Lipiński, and J. Dutkiewicz, "Texturization of multicrystalline silicon by wet chemical etching for

- silicon solar cells,” *J. Mater. Sci.*, vol. 40, no. 6, pp. 1459–1463, 2005.
- [24] E. R. Weber, “Transition metals in silicon,” *Appl. Phys. A Mater. Sci. Process.*, vol. 30, no. 1, pp. 1–22, 1983.
- [25] G. Martins, R. S. Bonilla, T. Burton, P. MacDonald, and P. R. Wilshaw, “Minority carrier lifetime improvement of multicrystalline silicon using combined saw damage gettering and emitter formation,” *Solid State Phenom.*, vol. 242, pp. 126–132, 2016.
- [26] J. Schmidt and M. Kerr, “Highest-quality surface passivation of low-resistivity p-type silicon using stoichiometric PECVD silicon nitride,” *Sol. Energy Mater. Sol. Cells*, vol. 65, no. 1, pp. 585–591, 2001.
- [27] H. Nagel, C. Berge, A. G. Aberle, H. Nagel, C. Berge, and A. G. Aberle, “Generalized analysis of quasi-steady-state and quasi-transient measurements of carrier lifetimes in semiconductors Generalized analysis of quasi-steady-state and quasi-transient measurements of carrier lifetimes in semiconductors,” vol. 6218, 1999.
- [28] D. N. R. Payne, C. Vargas, Z. Hameiri, S. R. Wenham, and D. M. Bagnall, “An advanced software suite for the processing and analysis of silicon luminescence images,” *Comput. Phys. Commun.*, vol. 215, pp. 223–234, 2017.
- [29] D. Lotfi and E. Hatem, “Phosphorus diffusion gettering process of multicrystalline silicon using a sacrificial porous silicon layer,” *Nanoscale Res. Lett.*, vol. 7, no. 1, p. 424, Jul. 2012.