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Development of TORCH readout electronics for customised MCPs

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ABSTRACT: The TORCH detector is being developed for low-momentum particle identification, combining time-of-flight and Cherenkov techniques to achieve charged particle $\pi/K/p$ separation up to 10 GeV/c over a flight distance of 10m. This requires a timing resolution of 70 ps for single photons. Based on an existing scalable design, production and testing of a TORCH readout system has been undertaken over the past year, and a novel customized Micro Channel Plate (MCP) photomultiplier device with 128-channels has been instrumented. This paper will report on the development of the readout system which is being used to measure time-of-flight in a test-beam, and its performance. We will also discuss the communication and data alignment between the TORCH system and the TimePix3 telescope in order to provide track reconstruction.

KEYWORDS: Cherenkov detectors; Instrumentation and methods for time-of-flight (TOF) spectroscopy; Photon detectors for UV, visible and IR photons (solid-state)

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1 Introduction

The Time Of internally Reflected Cherenkov light (TORCH) detector [1] is proposed for the low-momentum particle identification upgrade of the LHCb experiment [2], and an R&D project is currently underway [3]. The TORCH detector measures Time-Of-Flight (TOF) using the Cherenkov technique to achieve positive $\pi/K/p$ separation up to 10 GeV/c over a flight path of approximately 10m from the interaction region. Cherenkov photons are generated when a charged particle traverses a 1 cm-thick quartz plate of overall dimension $5 \times 6 \text{ m}^2$, as shown in figure 1, and segmented into 11 individual modules. The photons propagate by total internal reflection to the periphery of the plate where they are focused onto an array of Micro Channel Plate (MCP) photomultiplier detectors which measure their position and time their arrival. In order to achieve the required π/K separation, a TOF

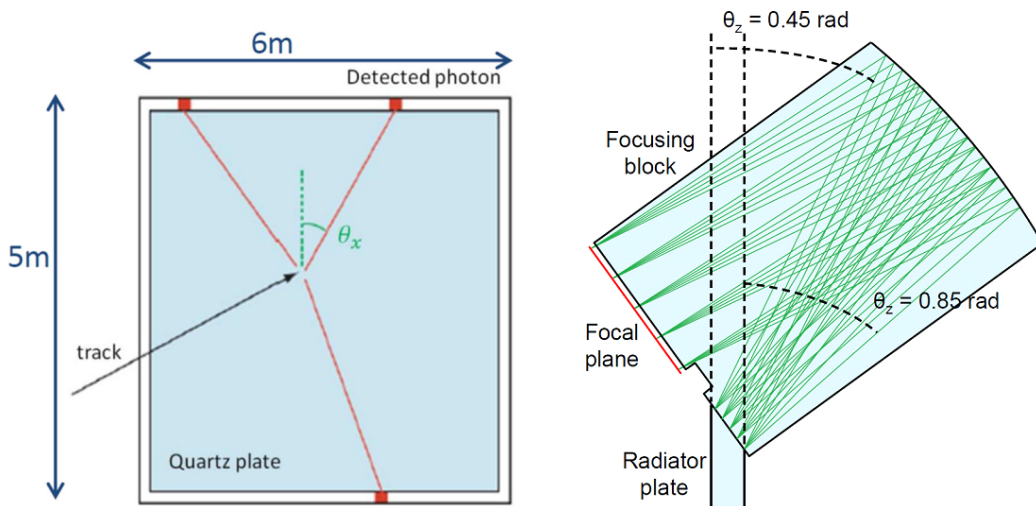


Figure 1. (Left) The TORCH quartz plate and (right) the focusing block.

resolution of 15 ps per track is required which, given ~ 30 detected photoelectrons, necessitates a 70 ps time resolution per single photon.

This paper will report on the recent developments of the TORCH TOF readout system and first measurements, as well as the preparation of the system for test-beam operation.

2 The TORCH photon detectors

The TORCH detector will use an array of novel MCP photomultipliers to detect the Cherenkov photons. The MCP device needs to provide a stable gain up to at least 5 C/cm^2 of integrated charge. The detector concept [1, 3] requires the photon detector to have a physical granularity equivalent to 8×128 pixels over a $53 \times 53 \text{ mm}^2$ active area within a $60 \times 60 \text{ mm}^2$ physical dimension, as shown in figure 2. Such an MCP is under development by our industrial partner, Photek, U.K [4]. The final device will use a 64×64 -channel physical layout. The channels are externally connected together in groups of eight along the coarse direction, while a charge sharing technique between two adjacent channels will be applied along the fine direction, in order to achieve the 8×128 granularity requirement. Currently a quarter-scale prototype with 32×32 -channels is being tested, giving a layout equivalent to 4×32 channels. Commercial 32×32 -channel Planacon devices [5] from Photonis, U.S.A., are also being investigated, where 4 channels are grouped along the coarse direction to form an 8×32 layout.

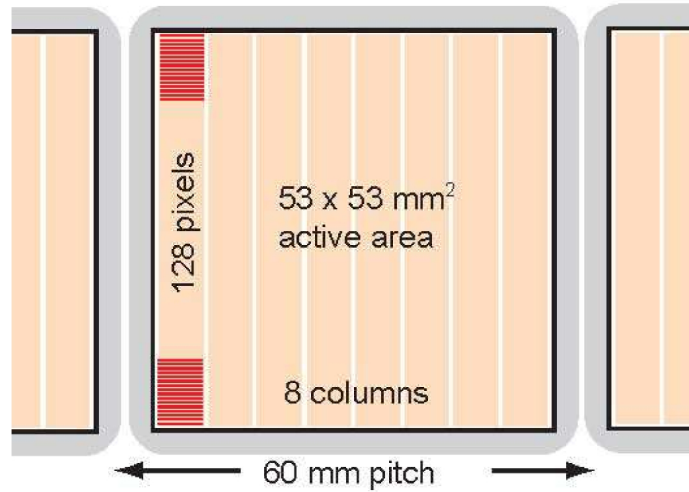


Figure 2. The required MCP layout for the TORCH detector.

3 Electronics and data acquisition development

3.1 System description

Figure 3 shows the main data flow of the TORCH readout system [6, 7]. The system consists of a NINO board, an HPTDC board, a readout board and a backplane. A photograph of the electronics components is shown in figure 4. Firstly, 32-channel NINO (IRPICS2) ASICs [8] amplify the signals from the MCP and measure the Time-Over-Threshold (TOT) according to a user-defined

threshold. The NINO ASIC is a pre-amplifier and discriminator that measures the input charge and gives an output whose signal width is proportional to the input charge. Then HPTDC ASICs [9], operated in 32-channel mode, measure the arrival time of both edges of the output from the NINOs. The measurements are buffered on the HPTDCs to be read out. One NINO and HPTDC board contains two of each ASICs respectively, giving 64 channels. The HPTDC data are buffered in an on-board FPGA and are subsequently transmitted to a readout board and thence to a DAQ PC.

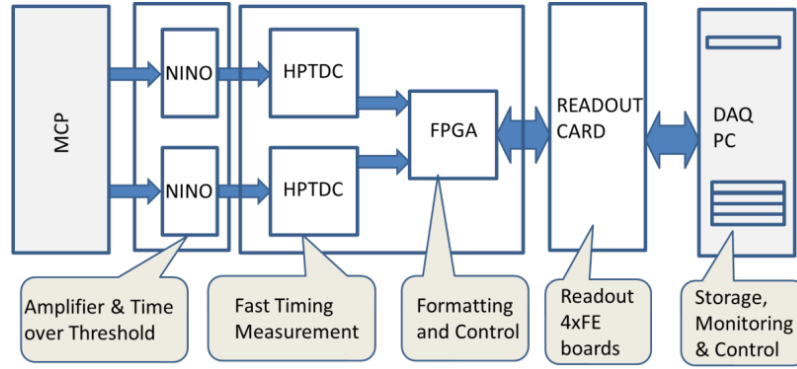


Figure 3. The data flow for the TORCH readout system.

The system has a modular and scalable design, where up to eight NINO/HPTDC boards can be used for a single MCP within its $60 \times 60 \text{ mm}^2$ physical envelope, giving 8×64 channels to fulfil the final TORCH requirement. The modular design also gives flexibility to instrument different types of MCP photon detectors during the development phase. Separating the readout board from the NINO/HPTDC boards allows using an independent readout framework, e.g. the LHCb data acquisition system, at a later stage of the project.

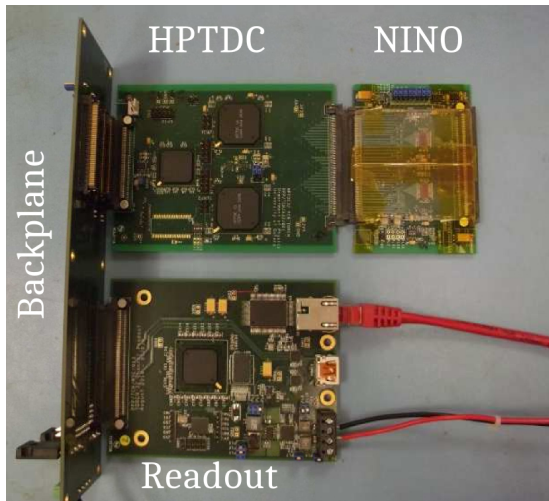


Figure 4. The TORCH electronics readout system.

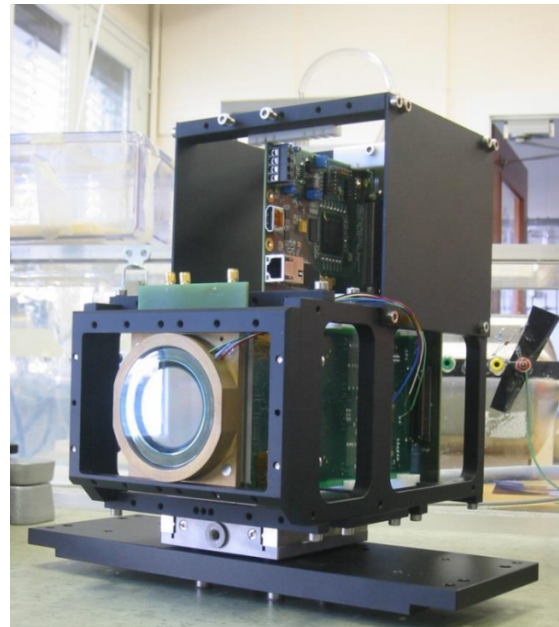


Figure 5. The readout system mounted to a Photek MCP.

On the NINO board, two NINO ASICs are wire-bonded onto the PCB. The NINO chips perform TOT measurements according to a threshold value that can be set by an on-board DAC or potentiometers for quick adjustment.

The HPTDC board consists of two HPTDC ASICs that provide 64-channel fast timing measurements up to 34 ps RMS resolution. A Xilinx Spartan 3AN FPGA [10] reads and buffers the output from the HPTDCs. The FPGA also provides the functions of command decoding (control and configuration), HPTDC configuration, data formatting and NINO threshold control. The control commands and configuration streams are transmitted from the readout board and decoded on this FPGA. The FPGA also programs the DAC on the NINO board using an SPI interface through the connector in order to set up the threshold values for the NINOs.

The readout board consists of a Xilinx Spartan 6 LX45T FPGA [11], a Gigabit Ethernet PHY chip, a 1G-bit DDR3 RAM and low-jitter clock fan-out ASICs. In addition to the data transferring and controls, the board provides fan-out of four clock and four trigger signals. The clock and trigger signals are taken from the HDMI connector shown on the right side of the board. The HDMI connector is pin-compatible with the AIDA Trigger Logic Unit (TLU) [12], which is used in a number of experiments, including the Timepix 3 telescope [13]. Raw Ethernet protocol over the Gigabit Ethernet link is implemented to achieve the best efficiency.

Figure 5 shows a photograph of the readout system connected to a Photek MCP. The connection is via an MCP interface board; mechanically-compatible interface boards can be designed and interchanged according to the specific MCPs that are being evaluated. The system shown is instrumented with two NINO and two HPTDC boards, giving 128 channels for the quarter-scale 4×32 development MCP. Laboratory studies and calibrations have been carried out with a pulsed laser. An uncorrected 88 ps resolution has been obtained, as shown in figure 6. When the NINO is used to measure TOT with a given threshold, the variation of the input signal height introduces a time-walk [7]. The system is calibrated with a set of known pulses and the results are used to correct this effect. The HPTDCs are also known to have Integral Non-Linearity (INL) [9]. This can be corrected by via calibrated values from a look-up-table. After these corrections the system gives an 80 ps resolution, which also includes a 20 ps jitter in the laser system. We are also working on fine tuning the NINO threshold to achieve a better time-walk correction in order to further improve the timing resolution.

3.2 Firmware development

A set of firmware has been specifically developed for test-beam use. The main firmware incorporates the HPTDC configuration via newly-developed JTAG drivers, replacing the previously adopted commercial JTAG cable. This feature has allowed users to control the module via a single Ethernet cable. Removing the need for an external programmer has made the system much more compact and robust.

An addressing scheme has been developed in the readout firmware as well as for the matching DAQ control software which has allowed commands to be sent to a specific board. For example, it allows adjust of the DAC output individually channel by channel. This adjustment has been very useful to compensate a threshold voltage offset, which varies from channel to channel on every NINO board. It is also possible to transmit a command or configuration stream to address all HPTDC boards, for instance when a “Start” or “Reset” command is sent.

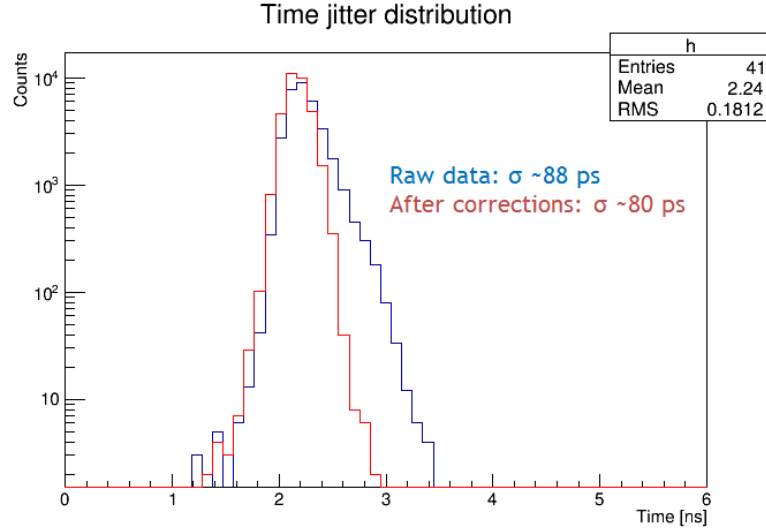


Figure 6. Timing resolution of the Photek MCP mounted to the TORCH readout system.

A block-based readout scheme is used. Here an HPTDC board will build up data in the readout buffer and once the size is over a pre-defined limit, the HPTDC board will instruct the readout board to retrieve data from its buffer. Since there are multiple HPTDC boards in the system, those boards with no data to be read out will insert 32-bit dummy data blocks to the readout stream.

3.3 Trigger handling and data synchronisation

Trigger handling functions have been incorporated into the system. From the DAQ software interface, users can choose from the main trigger input on the HDMI connector, an auxiliary trigger input or an internal (simulated) trigger. The HDMI trigger input is designed for working with the AIDA TLU. The auxiliary trigger input is located at a pair of pin headers on the readout board. This is available to most instruments, i.e. signal generator, through a Lemo to pin socket adaptor. The internal trigger is generated on the HPTDC boards at 156 kHz for testing the system stand-alone. In addition to the three trigger inputs, two trigger modes can be selected from the DAQ software. The HPTDC requires a 25ns-wide trigger signal that is synchronised with the clock. If an external triggering device, for instance the TLU, is capable to provide such a trigger, a “direct trigger” mode can be used. In this mode the trigger is send directly to the HPTDCs through fan-out and matched delay routes. Otherwise, an edge trigger mode can be switched on from the DAQ. In this mode, the FPGA detects the rising edge of the trigger and regenerates a 25 ns synchronised trigger signal for the HPTDCs.

The TLU enables working with the TimePix3 telescope or other external devices in test-beams. Via this interface, time-stamps between the TORCH detector and the telescope can be synchronised to identify tracks through the detector. The TLU gives triggers and records their time-stamps for data alignment. It also has busy handling functions to prevent buffer over-run in each system. By raising a busy signal the TLU will stop issuing triggers to all systems to keep the trigger numbers in line.

3.4 System production and testing

A total of ten HPTDC boards and five readout boards have been produced following an iterative design. The PCB assembly was carried out with a pick'n place machine. Future production can be carried out with the existing machine setup in an automated fashion. Firmware and hardware were also developed to allow for effective production testing.

To minimise the possibility of dusting on the high voltage connections of the MCP and the optical components, a new power supply module to work with only passive air cooling has been designed. It is equipped with two Texas Instrument TPS75901 [14] Low Drop-Out regulators, which provide 2.5 V and 3.3 V at a maximum 7.5 A to the HPTDC and NINO boards, connected through the backplane. In the test-beam setup, where the system has been instrumented with two NINO boards and two HPTDC boards, the regulator temperature has been retained at below 65°C.

4 Present and future test-beam activities

This paper reports the development of a precision TOF system for the TORCH detector. The hardware and firmware designs are introduced. The physical layout and modularity is suitable for the requirement of the TORCH detector. So far, an 80 ps timing resolution has been obtained in the laboratory and we are investigating further improvements including an evaluation of NINO thresholds.

Several systems have been produced to instrument MCPs in the laboratory as well as in test-beams. A preliminary test-beam run was carried out in May 2015 at the SPS, CERN, in which data were taken with a Photek Phase-2 MCP. A follow-up test-beam period is underway in October 2015 at the CERN PS. The TORCH test-beam system includes a radiator plate of size $1 \times 12 \times 35\text{cm}^3$ and a focusing prism, shown in figure 7. Analysis of the May test-beam data is on-going.

In a year's time, a final 8×64 -channel square 2-inch MCP will be delivered from Photek. The full readout system for this device, outlined in this paper, is in preparation.

Acknowledgments

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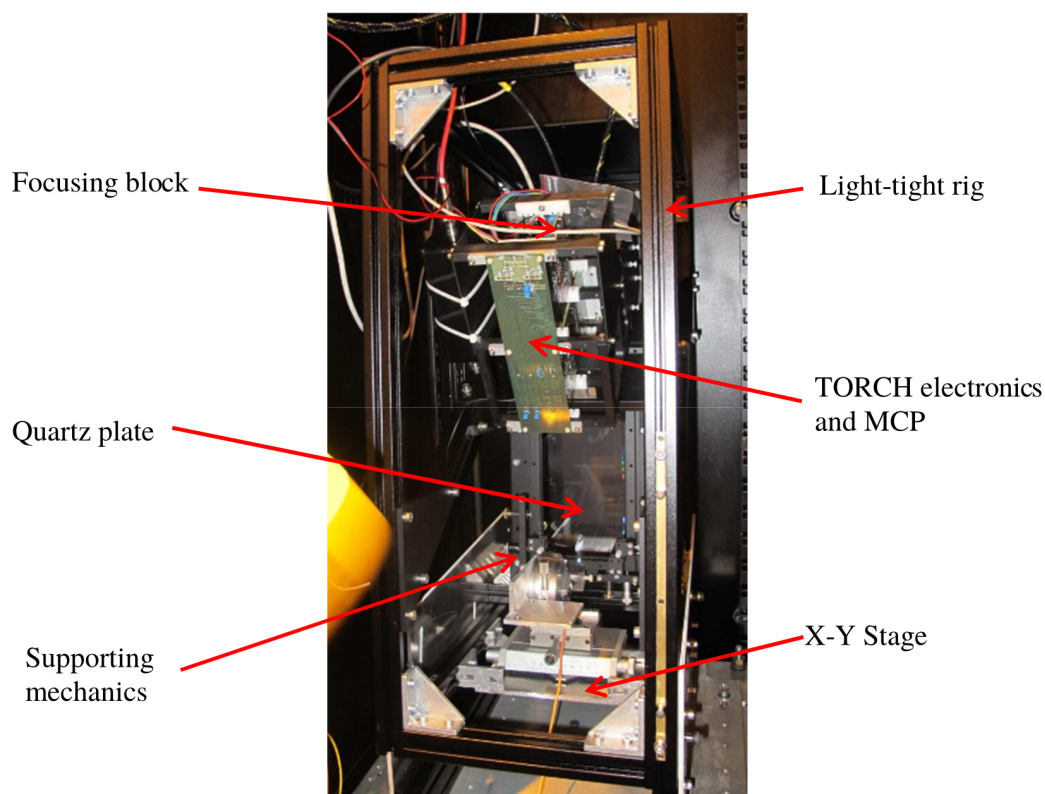


Figure 7. The TORCH test-beam system.

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