

Fabrication and simulation of organic transistors and functional circuits

D. Martin Taylor^{a*}, Eifion R. Patchett,^a Aled Williams,^a Ziqian Ding,^b Hazel E. Assender,^b John J. Morrison^c and Stephen G. Yeates^c

^a School of Electronic Engineering, Bangor University, Dean Street, Bangor, Gwynedd LL57 1UT, UK

^b Department of Materials, Oxford University, Parks Road, Oxford OX1 3PH, UK

^c School of Chemistry, University of Manchester, Oxford Road, Manchester, M13 9PL, UK

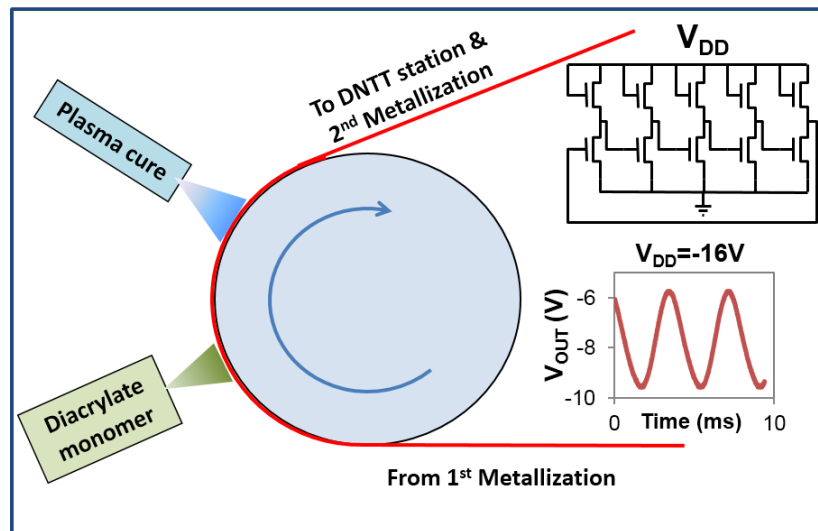
Abstract

We report the development of a vacuum-evaporation route for the roll-to-roll fabrication of functioning organic circuits. A number of key findings and observations are highlighted which influenced the eventual fabrication protocol adopted. Initially, the role of interface roughness in determining carrier mobility in thin film transistors (TFTs) is investigated. Then it is shown that device yield is higher in devices fabricated on a flash-evaporated-plasma-polymerised tri(propyleneglycol) diacrylate (TPGDA) gate dielectric than for TFTs based on a spin-coated polystyrene (PS) dielectric. However, a degradation in mobility is observed which is attributed to the highly polar TPGDA surface. It is shown that high mobility and excellent stability are restored when the surface of TPGDA was buffered with a thin, spin-coated PS film. The resulting baseline process allowed arrays of functional circuits such as ring oscillators, NOR/NAND logic gates and S-R latches to be fabricated with high yield and their performance to be simulated.

* corresponding author email: d.m.taylor@bangor.ac.uk

Key words: Organic TFT, Organic Electronics, Organic Circuits, Roll-to-Roll production, Vacuum-evaporation.

Graphical Abstract



Highlights

- Development of roll-to-roll fabrication protocol for organic TFTs and circuits
- Bottom-gate polystyrene/DNTT TFTs much better than top-gate TFTs
- Higher yield but lower mobility with vacuum-evaporated TPGDA insulator
- High-yield and high mobility with polystyrene-buffered TPGDA
- Fabrication of functional circuits – ring oscillators and logic gates
- New baseline process allows TFT parameter extraction and circuit simulation

1. Introduction

The most widely adopted approaches for the roll-to-roll (R2R) fabrication of organic electronic devices and circuits are generally based on solution processing e.g. inkjet [1,2] and gravure [3-6] printing which have also been used in combination with other methods including screen and flexo printing [7,8]. However, devices fabricated using only solution processing can suffer from poor yield arising mainly from a defective gate insulating layer and layer interdiffusion. Open- or short-circuited electrodes and tracks can also become issues as device sizes are reduced and production speeds increase. The best performing organic circuits to date are achieved by combining solution processing with a photolithographic step [9]. The latter allows much higher resolution features to be formed which is especially important for defining the source-drain gap (channel length, L) in thin film transistors (TFTs). However, incorporating a photolithographic step into a roll-to-roll process is not trivial.

Given these problems and limitations, it is surprising perhaps that only limited interest has been shown in developing a fabrication method based on the vacuum-evaporation of all the device layers – metal, insulator and semiconductor. Such an approach overcomes many of the problems associated with solution processing. It is usually argued that the capital cost is prohibitive, yet commercial equipment is already available for (a) producing high resolution metal patterns on plastic sheets in a R2R process [10,11] and (b) depositing organic and inorganic barrier layers onto moving plastic webs [11-13] – in both cases by evaporation under vacuum.

We reported on the feasibility of a vacuum-evaporation route for organic thin film transistor (OTFT) fabrication some years ago [13]. The key step in the process was the production of the gate insulator in a vacuum R2R environment by deposition and subsequent electron-beam polymerisation of the deposited monomer tri(propyleneglycol) diacrylate (TPGDA). In this early work, the hole mobility in bottom-gate top-contact (BGTC) pentacene OTFTs was only $\sim 0.09 \text{ cm}^2/\text{Vs}$ and the characteristics tended to be unstable. Also, pentacene is prone to long-term oxidative degradation so that identification of a high mobility, air-stable replacement semiconductor was essential. Although not reported earlier, top-gate bottom-contact (TGBC) OTFTs were also fabricated but showed much poorer performance. At the

time, this was thought likely to be due to degradation of the pentacene by the high energy electron-beam used to polymerise the TPGDA.

In the following, previously unpublished results and data are used to trace, from this modest beginning, the development of a high-yield, baseline vacuum-evaporation process for the production of OTFTs with reproducibly good performance [14,15] which in turn has allowed the demonstration of functioning circuits [16].

2. Materials and Methods

Dinaphtho[2,3-b:2',3'-f] thieno[3,2-b]thiophene (DNTT) was chosen for this work since it has a similar mobility to pentacene but with better environmental stability [17] due to a reduced tendency to oxidize. It was synthesised following a previously published route [18] from 2-naphthaldehyde with 35% overall yield. By repetition of 300 mg scale iodine-catalysed ring closure followed by two recrystallisations from *o*-dichlorobenzene, high purity DNTT was obtained as bright yellow microcrystals in 1g batches. TPGDA monomer and polystyrene ($M_w=350,000$) were purchased from Sigma Aldrich and used without further purification.

Arrays of TFTs and circuits were fabricated on precleaned, 5 cm x 5 cm, 125 μm thick polyethylene naphthalate (PEN) substrates (Dupont-Teijin). Full details of our vacuum-fabrication procedures have been given in previous publications [13-15,19]. Briefly, aluminium gate electrodes and associated tracks were vacuum evaporated onto the substrates through shadow masks. Subsequently, the substrates were attached to a cooled web-coater drum (Aerre Machines). With the drum rotating at a linear speed of 25 m/min under vacuum, flash-evaporated TPGDA monomer vapour which condensed onto the substrates was cross-linked by exposure, *in situ*, to a plasma. For circuit fabrication, the insulator was patterned using shadow masks to define rectangular areas separated by 1 mm gaps to act as vias for inter-layer metallic connections. The substrates were then transferred into an evaporator (Minispectros, Kurt Lesker) integrated into a nitrogen glovebox for the vacuum-deposition (2.4 nm/min) of DNTT onto the insulator. Without exposing the substrates to ambient air, the gold source/drain metallisation layer was deposited through a shadow mask in the same evaporator.

The OTFT masks defined an 18 x 5 array of 90 transistors with 5 capacitors arranged diagonally across the substrate. The channel length L in each row increased

in steps from 50 μm to 200 μm . Each row comprised of two blocks of 9 OTFTs. In the left hand blocks the channel width, W , was 2 mm, yielding W/L ratios ranging from 40 in the first row down to 10 in the fifth row. In the right hand blocks of 9 OTFTs, a constant W/L ratio of 20 was maintained so that W ranged from 1 mm in the first row to 4 mm in the fifth row. Arrays of logic gates and ring oscillators were prepared on other PEN substrates using the fabrication protocols developed for the OTFTs [14,16].

To counter the deleterious effects that the high-polarity TPGDA dielectric had on TFT characteristics, it was found beneficial to passivate the insulator surface prior to depositing the semiconductor [20]. This was achieved by spin-coating at 1000 rpm, in a nitrogen glovebox, a thin film of polystyrene (3% w/w in toluene) and heating on a hot plate at 100°C for 10 mins. Also, for comparing the performances of top-gate versus bottom-gate TFTs and process yield, some OTFT arrays were fabricated using thicker, spincoated layers of polystyrene (no TPGDA) as the gate insulator.

Topographic images of the various film layers were obtained in tapping mode using a Veeco Dimension 3100 Atomic Force Microscope (AFM). OTFT characteristics were measured in air using a Keithley model 4200 Semiconductor Characterization System in ambient dark conditions. Inverter transfer characteristics were obtained using the same system. The time responses of logic gates and ring oscillators were recorded by connecting the output of each circuit to a digital oscilloscope (Agilent DSO-X 2014A) via a buffer amplifier to minimise oscilloscope loading effects on the circuits. Device parameter extraction and circuit simulations were undertaken using Silvaco's Universal Organic Thin Film Transistor (UOTFT) Model (Level=37) and Smartspice Circuit Simulator.

3. Results and Discussion

3.1 Bottom-gate versus top-gate OTFTs

Our initial investigations into the use of vacuum-deposited TPGDA as a gate insulator had established that bottom-gate, top-contact (BGTC) pentacene TFTs were superior to top-gate, bottom-contact (TGBC) devices. Since this could have been due to the detrimental effect of plasma processing of the insulator on top of the semiconductor layer in the top-gate structures, an investigation was carried out using spin-coated PS as the gate insulator in both device types.

In Fig.1 is shown the output (I_D vs V_D) and transfer ($\log I_D$ vs V_G) characteristics of a typical PS-based TGBC TFT. The inset in Fig. 1(b) shows the gate-voltage dependence of the device mobility, μ , extracted in the linear regime using the equation

$$\mu_{lin} = \frac{\partial I_D}{\partial V_G} \cdot \frac{L}{WC_i V_D} \quad (1)$$

and in saturation

$$\mu_{sat} = \left(\frac{\partial \sqrt{I_D}}{\partial V_G} \right)^2 \cdot \frac{2L}{WC_i} \quad (2)$$

where C_i is the capacitance per unit area of the gate dielectric layer.

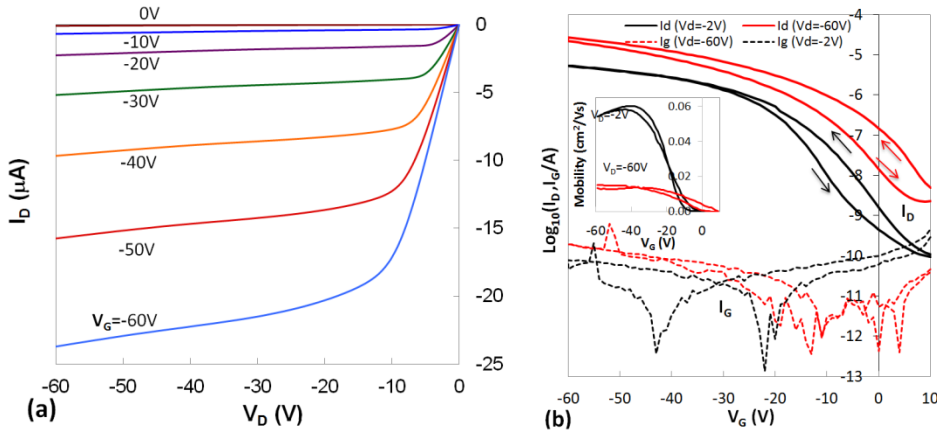


Fig. 1 (a) Output (I_D vs V_D) and (b) transfer ($\log I_D$ vs V_G) characteristics for a top-gate, DNTT transistor ($W=15.0$ mm, $L=30$ μ m) with a 1.2 μ m thick polystyrene gate insulator. The transfer characteristics were obtained in both the linear ($V_D = -2$ V) and the saturation ($V_D = -60$ V) regimes. Shown dotted is the corresponding gate leakage current, I_G . The inset in (b) shows the gate-voltage dependence of the mobility.

Although the gate leakage current, I_G , is low for these relatively large devices, all other performance criteria are poor. The output characteristics do not show good saturation. The on-off current ratio is only $\sim 10^4$. While mobility in the linear regime is significantly higher than in saturation, nevertheless, it is still low, rising to a maximum of ~ 0.06 cm^2/Vs , almost two orders of magnitude lower than expected [17]. The transfer characteristics are also unstable, displaying anticlockwise hysteresis.

This may be contrasted with the behaviour of BGTC devices (Fig. 2). Now the output characteristics show good linear and saturation regions. The transfer characteristics are stable with little hysteresis. The mobility in both the linear and

saturation regimes is $\sim 1 \text{ cm}^2/\text{Vs}$, which is higher than a previously reported value for vacuum-deposited films [17], but with μ_{in} here slightly greater than μ_{sat} . The combination of higher mobility and lower off-currents leads to an on-off ratio between 10^6 and 10^7 . Gate leakage currents are also low at $\sim 10 \text{ pA}$.

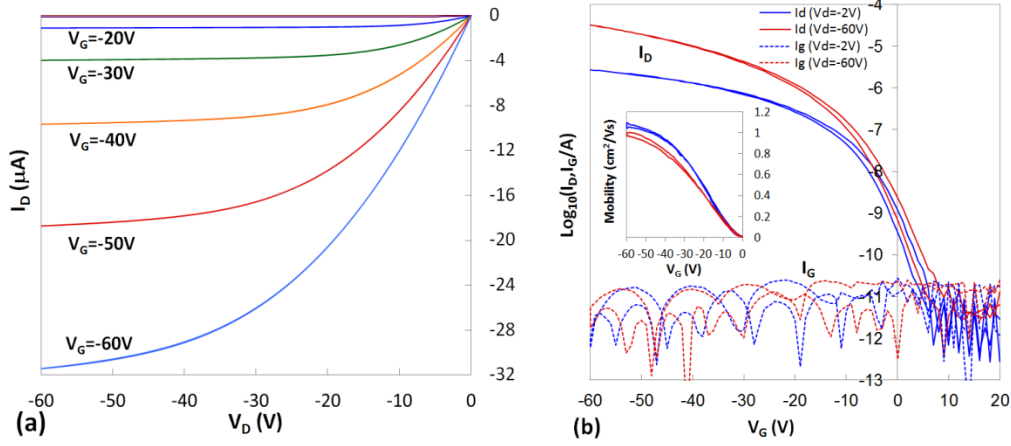


Fig. 2 (a) Output (I_D vs V_D) and (b) transfer ($\log I_D$ vs V_G) characteristics for a bottom-gate, DNTT transistor ($W=2.0 \text{ mm}$, $L=100 \mu\text{m}$) with a $1.0 \mu\text{m}$ thick polystyrene gate insulator. The transfer characteristics were obtained in both the linear ($V_D = -2 \text{ V}$) and the saturation ($V_D = -60 \text{ V}$) regimes. Shown dotted is the corresponding gate leakage current, I_G . The inset in (b) shows the gate-voltage dependence of the mobility.

This difference in behaviour is readily understood from the AFM images in Fig. 3. In (a) is shown the surface topography of a DNTT film evaporated directly onto the PEN substrate. The RMS surface roughness over the $2 \mu\text{m} \times 2 \mu\text{m}$ area is 6.4 nm with differences of up to 12 nm between the peak height of the DNTT grains and the inter-grain troughs. On the other hand, the RMS roughness of the PS film was only 0.69 nm - an order of magnitude lower. Evidence has already been presented [21] about the importance of interface topography in determining the mobility in pentacene OTFTs. Here, both the interface topography and the low polarity of the PS surface are important, as will be discussed later.

The clear outcome of this study is that the surface of evaporated DNTT is too rough and of insufficiently good quality for top-gate OTFTs, and that the loss of mobility in the top gate case observed in our earlier study of pentacene OTFTs could not be solely ascribed to the effect of electron-beam irradiation. Accordingly, all further work concentrated on bottom-gate top-contact devices.

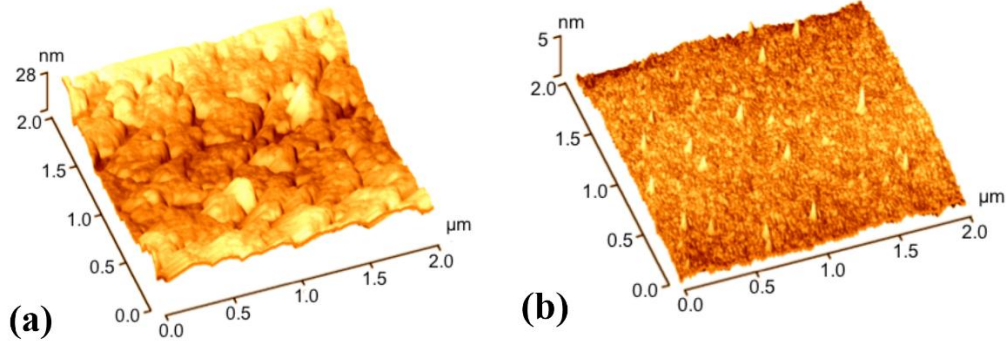


Fig. 3 AFM topographical images of the surfaces of (a) evaporated DNTT and (b) spin-coated polystyrene on PEN. RMS roughness is 6.4 nm and 0.69 nm respectively.

Table 1 summarises the average maximum values extracted from plots such as the inset in Fig. 2(b) for μ_{lin} and μ_{sat} . The data were obtained from a 90-OTFT array of bottom-gate OTFTs formed on spin-coated PS. Each value should represent the average and standard deviation for the 9 OTFTs with the indicated channel dimensions. In practice, however, the number of working devices was only 61, representing a yield of ~68%. Nevertheless, that mobility is independent of channel dimensions confirms the linear dependence of I_D on device dimensions – an important finding for subsequent circuit simulation for which the ability to scale device dimensions is important. Furthermore, the low standard deviation reflects the good reproducibility between devices – again an important consideration for circuit design and simulation.

Table 1 Average maximum mobility and standard deviation for bottom-gate DNTT OTFTs with a spin-coated polystyrene gate dielectric.

		Average maximum mobility (cm ² /Vs)				
Row		A	B	C	D	E
L (μm)		50	75	100	150	200
$W = 2$ mm	01-09 Linear	0.93±0.03	1.12±0.02	1.10±0.04	1.07±0.13	1.06±0.04
	01-09 Saturation	0.94±0.06	1.05±0.05	1.02±0.03	0.98±0.13	0.96±0.05
$W/L = 20$	10-18 Linear	0.98±0.04	1.12±0.09	1.02±0.19	1.14±0.07	0.92±0.03
	10-18 Saturation	0.96±0.04	1.02±0.07	0.95±0.15	1.02±0.10	0.67±0.20

3.2 TPGDA Bottom-Gate Dielectric

Having established that bottom-gate devices were superior to top-gate, in this section we proceeded to investigate the use of vacuum-deposited and plasma polymerised TPGDA as the bottom-gate dielectric with the DNTT evaporated directly onto the TPGDA surface. AFM images show that the RMS roughness of the TPGDA layer was 0.44 nm over an area $3\ \mu\text{m} \times 3\ \mu\text{m}$ and even flatter, therefore, than the spin-coated polystyrene surface. Of immediate interest is the improved yield on TPGDA. Every device in the 90-OTFT array operated except for 1 block of 9 common-gate devices, resulting in a yield of 90%. Typical output and transfer characteristics are shown in Fig. 4.

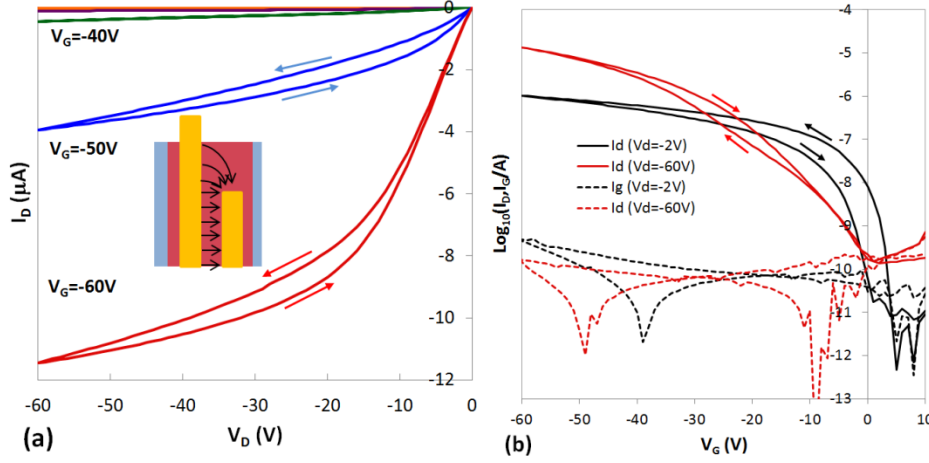


Fig. 4 (a) Output (I_D vs V_D) and (b) transfer ($\log I_D$ vs V_G) characteristics for a bottom-gate, DNTT transistor ($W = 2\ \text{mm}$, $L = 200\ \mu\text{m}$) with a TPGDA gate insulator (850 nm thick). The transfer characteristics were obtained in both the linear ($V_D = -2\ \text{V}$) and the saturation ($V_D = -60\ \text{V}$) regimes. Shown dotted is the corresponding gate leakage current, I_G . The inset in (a) shows current flow lines for both the true channel current and the parasitic fringe current outside the main channel area.

In both cases, there is significant hysteresis with the output characteristics also showing poor saturation. Interestingly, in the transfer plots, hysteresis is anticlockwise arising from a negative shift of the flatband voltage, a common observation in organic TFTs owing to interface hole trapping. In saturation, the hysteresis is clockwise and arises from the appearance of a plateau-like feature at $-25\ \text{V}$ during the negative voltage sweep. The origin of this feature is unclear, but may be related to the presence of interface states [18].

As above, equations (1) and (2) were used to extract values for the gate voltage dependence of μ_{lin} and μ_{sat} . The average maximum values together with the standard deviations are given in Table 2.

The standard deviations are again relatively low, confirming good reproducibility between devices of the same geometry. Now however, μ_{lin} is less than μ_{sat} in all but one case. Of greater significance is the increase in mobility with decreasing channel geometries. This is particularly marked for the devices in which $W/L=20$ while L decreases from 200 to 50 μm . For these devices, the extracted μ_{lin} and μ_{sat} are a factor 3-4 higher in the small devices compared to the larger devices. After carefully removing the DNTT from the channel region in these smaller devices, a significant source-drain current still flowed, confirming that the increase in mobility arose from the presence of a parasitic source-drain current flowing outside the channel area (see inset Fig. 4(a)). We conclude, therefore, that in bottom-gate devices fabricated on TPGDA the mobility is significantly lower than for the equivalent PS-based devices.

Table 2 Average maximum mobility and standard deviation for bottom-gate DNTT OTFTs fabricated on the TPGDA gate dielectric.

		Average mobility (cm^2/Vs)				
Row		A	B	C	D	E
L (μm)		50	75	100	150	200
$W = 2 \text{ mm}$	01-09 Linear	-	0.40 ± 0.03	0.38 ± 0.03	0.36 ± 0.05	0.22 ± 0.01
	01-09 Saturation	-	0.56 ± 0.03	0.42 ± 0.01	0.33 ± 0.04	0.33 ± 0.04
$W/L = 20$	10-18 Linear	0.66 ± 0.09	0.41 ± 0.08	0.34 ± 0.06	0.20 ± 0.02	0.15 ± 0.03
	10-18 Saturation	0.79 ± 0.08	0.65 ± 0.13	0.38 ± 0.05	0.27 ± 0.03	0.25 ± 0.01

Since the surface of TPGDA is extremely flat we may eliminate surface topography as a contributory factor to the low mobility. The most likely origin of the poor performance lies in the highly polar nature of the TPGDA surface. It is well-known [22] that a high-k dielectric surface degrades carrier mobility, with dipolar dispersion of the semiconductor density of states being given as a possible reason [23]. Such effects may be overcome by applying a low polarity passivating layer to

the dielectric surface. We have shown [20] that a thin, spin-coated film of polystyrene is particularly effective in passivating TPGDA. X-ray diffraction studies [15] confirm that the resulting increase in mobility is linked to a significant improvement in the DNTT crystal structure on the passivated surface. In the following two sections, therefore, we focus on OTFTs and circuit elements fabricated on PS-buffered TPGDA.

3.3 Bottom-gate OTFTs on PS-buffered TPGDA

The fabrication of 90-OTFT arrays based on PS-buffered TPGDA was achieved at high yield (~90%) but again with 1 block of 9 common-gate TFTs failing [14]. Fig. 5 shows typical output and transfer characteristics of an OTFT from this earlier work. The output characteristics show good linear and saturation regions with no hysteresis discernible in the transfer plots, confirming that the devices are highly stable. The on-off ratio was between 10^6 and 10^7 and gate leakage current, I_G , ~ 10 pA over most of the voltage ranges. As before, equations (1) and (2) were used to extract the average maximum values and standard deviation of μ_{lin} and μ_{sat} listed in Table 3. This time, μ_{sat} was only slightly greater than μ_{lin} but a tendency for mobility to increase with decreasing device dimensions was again observed, albeit not to the same extent as with the unbuffered TPGDA devices.

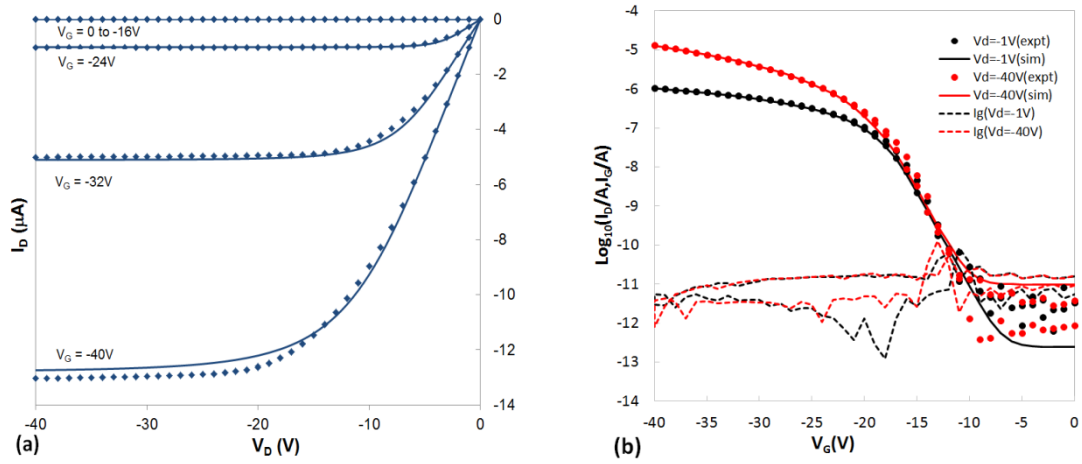


Fig. 5 (a) Output (I_D vs V_D) and (b) transfer ($\log I_D$ vs V_G) characteristics for a bottom-gate, DNTT transistor ($W = 2$ mm, $L = 200$ μm) formed on a PS-buffered TPGDA surface. The transfer characteristics were obtained in both the linear ($V_D = -1$ V) and the saturation ($V_D = -40$ V) regimes. Experimental results are shown by the data points while the solid curves are simulations used for parameter extraction. Shown dotted in (b) is the corresponding gate leakage current, I_G .

As reported earlier [14], the true mobility in these devices is $\sim 1 \text{ cm}^2/\text{Vs}$, i.e. the same as for transistors formed on the spin-coated PS dielectric (Section 3.1). Since the three sets of mobility data presented in Tables 1-3 were obtained from device arrays produced using the same TFT designs, it appears that the magnitude of parasitic source-drain currents is dependent on the nature of the underlying dielectric. For the spin-coated PS dielectric the parasitic current is negligible, for unbuffered TPGDA it becomes a serious problem as device size decreases but one that is mitigated by the passivating effect of the PS buffer layer. This unexpected observation, which has implications beyond the present work, may be associated with possible polarization effects occurring in the TPGDA outside the channel region. However, further investigations are required to arrive at a definitive explanation.

Table 3 Average maximum mobility and standard deviation for bottom-gate DNTT OTFTs fabricated on the PS-buffered TPGDA gate dielectric.

		Average mobility (cm^2/Vs)				
Row		A	B	C	D	E
L (μm)		50	75	100	150	200
W = 2 mm	01-09 Linear	1.24 \pm 0.05	1.12 \pm 0.13	1.13 \pm 0.25	1.16 \pm 0.11	-
	01-09 Saturation	1.59 \pm 0.09	1.50 \pm 0.07	1.39 \pm 0.21	1.46 \pm 0.07	-
W/L = 20	10-18 Linear	1.36 \pm 0.12	1.23 \pm 0.08	1.20 \pm 0.07	1.08 \pm 0.09	0.92 \pm 0.01
	10-18 Saturation	1.77 \pm 0.20	1.62 \pm 0.08	1.50 \pm 0.10	1.43 \pm 0.06	1.34 \pm 0.04

In contrast to the TPGDA-only devices, the characteristics of the PS-buffered TFTs were highly stable. This allowed excellent fits (solid curves in Figure 5) to be obtained *simultaneously* to both the output and transfer characteristics using Silvaco's UOTFT parameter extraction software. The Silvaco model [24] is an extension of that developed for amorphous and polycrystalline silicon TFTs. Within the framework of a channel conductivity [25] based on variable range hopping and percolation concepts [26], the dependence of the effective mobility, μ_{FET} , on gate voltage is given by the equation

$$\mu_{FET} = \mu_{ACC} \left[\frac{V_G - V_T}{V_{ACC}} \right]^\gamma. \quad (3)$$

Here μ_{ACC} defines the mobility at the onset of strong channel accumulation and V_{ACC} a fitting parameter assumed to be unity in all our simulations. Carrier mobility in the OTFT channel is often dependent on V_G and described by a power-law, with the value of the exponent, γ , reflecting the degree of departure from the ideal ($\gamma = 0$) as a result of carrier trapping in the channel. Other parameters required to achieve a good fit are listed in Table 3 and include the characteristic voltage for the carrier density of states, V_O , which also includes the effects of interface states, λ a measure of the output conductance in saturation, M_{SAT} and A_{SAT} fitting parameters which adjust the shape of the characteristics in the transition from linear to saturation regimes, σ_0 the minimum semiconductor bulk conductance and $R_{S/D}$ the zero-bias source/drain series resistances. The parameter values used to fit the OTFT characteristics in Fig. 5 are listed in Table 4 and were used subsequently in a model card for the circuit simulations discussed in the next sections.

Table 4 OTFT parameters used to fit the experimental data in Fig. 5.

Parameter	Value	Parameter	Value
W (μm)	2000	γ	0.031
L (μm)	200	λ (S)	0
C_i (F/cm ²)	4.83×10^{-9}	M_{SAT}	3.90
V_T (V)	-17.86	A_{SAT}	1.19
V_O (V)	0.948	σ_0 (S)	8.66×10^{-15}
V_{ACC}	1	R_S (Ω)	0
μ_{ACC} (cm ² /Vs)	1.07	R_D (Ω)	0

The simulations confirm that in strong accumulation, carrier mobility is ~ 1 cm²/Vs and that the dependence on V_G is weak ($\gamma = 0.031$). Furthermore, the source and drain series resistances R_S and R_D respectively are both zero.

3.4 Circuits and circuit simulations

Using the same protocols as for the OTFTs fabricated on the PS-buffered TPGDA we have fabricated arrays of basic circuits, all with 100% yield. For example, in Fig. 6 is shown the performance of a 5-stage ring oscillator. The circuit begins to oscillate with a supply voltage, V_{DD} as low as -16 V. On increasing V_{DD} to -90 V the output frequency exceeded 2 kHz. A 7-stage RO ran continuously at $V_{DD} = -60$ V for 8 hours with little change in output frequency although a reduction occurred in the

output amplitude [14]. ROs stored under normal laboratory conditions for a month operated as new, showing no signs of environmental degradation.

Simulations using Silvaco Smartspice and utilising an OTFT model card incorporating the extracted parameters from Table 4, suggested that the ROs should have oscillated at significantly higher frequencies than those observed. For example, at $V_{DD} = -40$ V and -60 V, a 5-stage RO should be capable of oscillating at 7 kHz and 20 kHz respectively [14] i.e. more than an order of magnitude higher than observed in practice. It was shown that the discrepancy arose from the presence of parasitic gate-drain and gate-source capacitances with the former being more dominant [14].

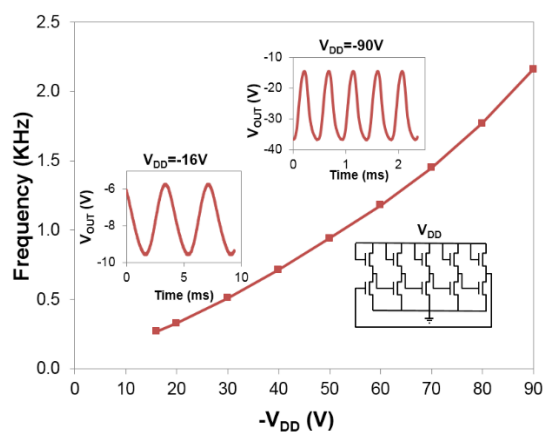


Figure 6 Output frequency of a 5-stage ring oscillator (shown as an inset) plotted as a function of the supply voltage, V_{DD} . Also shown as insets are examples of the output signals for $V_{DD} = -16$ V the lowest voltage at which the circuit operated and at $V_{DD} = -90$ V the highest voltage applied.

A range of logic circuits have also been fabricated including inverters, NOR/NAND gates and Set-Reset latches [16] which show switching times in the sub-millisecond range. When parasitic capacitances were included in the circuit, simulations reproduced closely the observed experimental performance [16].

4. Conclusions

In the foregoing we have described the development of a vacuum-evaporation-based approach for the roll-to-roll fabrication of organic electronic circuits. The technology is based on the vacuum-evaporation and subsequent polymerisation of TPGDA to form the gate insulator. This solventless process led to significantly improved yield (>90%) compared with a spin-coated polystyrene dielectric (~68%).

The carrier mobility extracted from the characteristics of OTFTs incorporating evaporated films of the organic semiconductor DNNT was seen to be dependent on several factors. BGTC devices employing spin-coated polystyrene as the gate insulator were superior to TGBC devices owing to channel formation at the much smoother semiconductor/insulator interface in the former case. However, a smoother interface on its own was insufficient for achieving high mobility in BGTC DNNT devices formed on the bare TPGDA insulator. The lower mobility and unstable threshold voltage in this case was probably associated with the poorer crystalline structure of DNNT when evaporated onto the highly polar TPGDA surface.

Buffering the surface of TPGDA with a thin, spin-coated film of polystyrene gave highly stable TFTs with reproducibly high mobility. In turn this allowed relevant device parameters to be extracted from device characteristics, and a realistic model card obtained for simulating a range of fabricated circuits including ring oscillators and logic gates.

On-going work is now concentrating on developing (a) a vacuum-compatible process for buffering TPGDA and (b) methods for additive patterning of the gate insulator and semiconductor using techniques such as organic vapour jet printing. On successful completion of these next stages, a roll-to-roll process for fabricating organic electronic circuits will have been established, based entirely on vacuum-evaporation.

Acknowledgments

This work was supported by funding from the Engineering and Physical Sciences Research Council (UK) via a Flagship Grant (FS/01/01/10) from the Innovative electronic-Manufacturing Research Centre, Loughborough. The authors are grateful to Dr. A. Nejim of Silvaco UK Ltd for access to and support for the UOTFT and Smartspice simulation software.

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