A 220 GHz Finline Mixer with Ultra-Wide Instantaneous Bandwidth

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***Abstract*—We describe the design and fabrication of a 220 GHz superconductor-insulator-superconductor (SIS) mixer with ultra-wide IF bandwidth. The mixer is fabricated on a 100 μm thick quartz substrate, with planar circuit on-chip integration. The RF power is coupled to the tunnel junction via a unilateral finline taper and a slotline-to-microstrip transition. We used a double-stub tuning network to tune out the junction's parasitic capacitance at a broad RF bandwidth, and matched the output impedance of the mixer to the input impedance of the IF amplifier (50 Ω) from 4–18 GHz using a 6-stage IF impedance-transformer. We have fabricated these devices and have measured good DC current-voltage (IV) characteristic curves. The heterodyne mixing performance of these devices is currently being measured, and we expect to present the results in the forthcoming ISSTT conference in March.**

I. INTRODUCTION

A broad instantaneous frequency (IF) bandwidth heterodyne receivers at millimetre (mm) and sub-millimetre (sub-mm) frequencies is important for several reasons. For example, it enables the telescope to capture multiple astronomical spectral emission lines in a single observation run, improving both the calibration process and the speed of observation. Also, the receiver sensitivity is proportional to the IF bandwidth hence increasing the IF bandwidth of the mixer is a very effective way of reducing the integration time, in particular for mixers operating well below the superconducting gap. Current state-of-the-art mm and sub-mm telescopes normally require at least 8 GHz of IF bandwidth, and in recent years, there has been extensive efforts to further increase the IF bandwidth to values higher than 15 GHz (see e.g., [1], [2]).

One factor that limits the IF bandwidth of a superconductor-insulator-superconductor (SIS) mixer receivers is the tunnel junction capacitance itself. This contribution can however be minimised by reducing the size of the tunnel junction (say to $\approx 1\mu$), or by employing distributed tunnel junctions [3]. Another significant factor that limits the IF performance of an SIS mixer is the geometric impedance induced by the on-chip planar circuit components. Large geometric impedance presented at the IF port can create an equivalent RLC circuit of the mixer that resonates at low ν_0 within the IF band, causing both the real and imaginary parts of the impedance to plunged to near zero values at a significant portion of the bandwidth determined by the width of the resonance [4]. Since the device output is almost shorted, it is impossible to match the impedance of the mixer to the amplifier in this range, therefore reducing the useful IF bandwidth of the mixer. This effect that we will investigate in this paper is more dominant at low frequencies since the surface area of the planar circuitry is larger than high frequency mixers.

Here, we present the design of a 220 GHz SIS mixer where we matched the mixer output impedance using a multi-stage microstrip IF transformer fabricated with standard printed circuit board (PCB) technology. This matching network transforms the dynamic impedance of the SIS mixer with a junction capacitance of 80 fF/μm^2 to a 50 Ω output at broad IF bandwidth. Our mixer chip design employs components with relatively large capacitance such as radial stubs and tuning circuits, hence the generation of an RLC resonance is possible. We will however show that by careful control the dimension of the RF planar circuit components fabricated on-chip, it is possible to shift the RLC resonance outside desirable IF band and achieve good mixing performance up to almost 20 GHz.

II. MIXER DESIGN

Our mixer design employs fully integrated planar circuit technology with all the RF circuit components deposited on one side of a 100 μm thick quartz substrate, without the use of any lumped element components. The ground layer of the planar circuits is formed using a $\sim$ 250 nm niobium (Nb) layer while the wiring layer is of 400 nm Nb. To abstain the desired characteristic impedance for the microstrip circuit, a silicon monoxide dielectric layer (SiO, 490 nm) is used.

The RF path of our mixer chip comprises a unilateral finline taper and a slotline-to-microstrip transition. The finline taper transforms the incoming RF waves from the waveguide mode into a slotline mode, by gently narrowing down the slot width to about 2.5 μm, reducing the characteristic impedance from $\sim$ 500 Ω to values comparable to those microstrip ($\sim$40 Ω). This ensure efficient coupling of the incoming field from slotline to microstrip, with an aid of two radial stubs (see Fig. 1) of approximately $\lambda_g/4$ in radius [5]. Finally the loaded waveguide was matched to the empty waveguide by a single substrate notch taper formed before the finline.

The tuning circuit of the mixer comprises two inductive strips before and after the junction, and a broadband multi-stage transformer. The two inductive strips are used to pro-

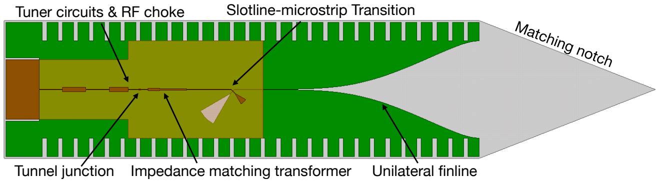


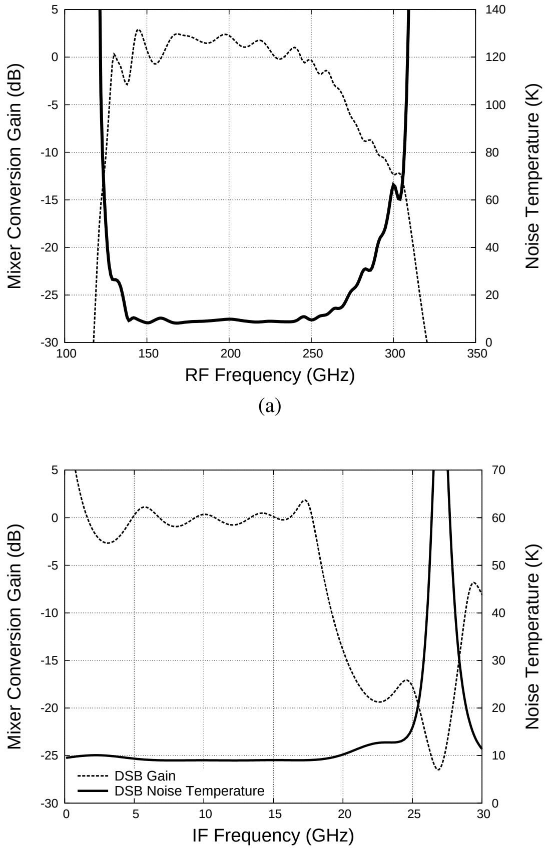
Fig. 1. The planar mixer chip comprising the unilateral finline taper, slotline-to-microstrip transitions, impedance matching transformer, tuner circuit and RF choke, working in conjunction with a 1.5 $\mu\mathrm{m}^2$ circular Nb/AlO$_x$/Nb SIS tunnel junction.

vide broadband tuning response [5], and a 3-step quarter-wavelength transformer is deposited before this tuning circuit to match the impedance of this section to the slotline-to-microstrip transition. This tuning network was designed to work with a 1.5 $\mu\mathrm{m}^2$ circular Nb/AlO$_x$/Nb SIS tunnel junction, with a normal resistance of approximately 15 Ω (assuming a current density of 10 kA/cm^2) and a junction capacitance of $\sim$ 120 fF. The final design of the entire planar circuit structure was optimised using Ansys High Frequency Structure Simulator (HFSS), to include the effect of the complex surface impedance of the superconductor material, dielectric thickness, loss tangent, and other factors that cannot accurately be calculated from transmission line theory.

The IF output of the mixer chip was matched to a 50 Ω IF output through a multi-stage IF transformer PCB board [6], optimised in the frequency range of 4–18 GHz. The design of the IF transformer was done using a lumped element software package (Ansys Designer). The scattering matrix of the mixer chip generated through HFSS was imported to the Ansys Designer's circuit model, and several microstrip components from the software library were cascaded to match the scattering matrix representing the output impedance of the chip to the amplifier. In this work, we used a 6-stage IF transformer, where the first two microstrip sections served as two inductive strips to tune out the mixer chip's capacitance over a wide IF bandwidth, while the subsequent four sections transformed the real resistance to a 50 Ω output.

The heterodyne performance of the final mixer design was verified using CalTech's superconducting mixer design package SuperMix, which is based on Tucker's quantum theory of mixing [7]. We imported the scattering matrices generated by both HFSS (for RF components) and Ansys Designers (IF transformer) into SuperMix to form the mixer model. The results of SuperMix calculations are shown in Fig. 2. The predicted noise temperatures are low from 140–260 GHz, while the double sideband (DSB) gain stays reasonably flat throughout the designated RF bandwidth. This broad RF bandwidth can in fact cover both the Band 5 (163–211 GHz) and the Band 6 (211–275 GHz) requirement of the Atacama Large Millimetre/Sub-millimetre Array (ALMA). However, it is worthwhile noting that these predicted results do not take into account the effect of optical losses before the mixer chip, hence they should only be considered as a guide to designing a mixer with best performance.

Fig. 2(b) shows the SuperMix predicted mixer DSB gain and noise temperature at the IF frequencies. It can be seen that when the mixer output is matched with the IF transformer, the gain remains relatively flat from 5–17.5 GHz, and the predicted noise temperature remains below 10 K from 0–20 GHz. This bandwidth is large enough to cover the full-band operation of a majority of cryogenic low-noise amplifier (LNA) available commercially (typically 4–12 GHz), and is wide enough for most astronomical applications. The RLC resonance described earlier can clearly be seen near 27 GHz, where the noise temperature has shot up abruptly. This indicates the success of our design to shift the resonant frequency of the the parasitic RLC circuit outside the required IF band, hence having a high performance mixer in an IF bandwidth of more than 15 GHz.



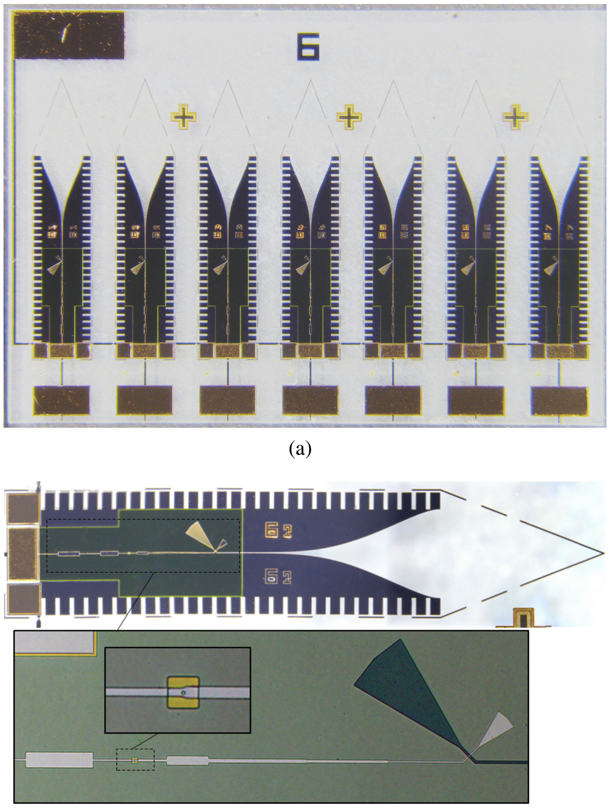
(a)

(b)

Fig. 2. (a) The RF mixing performance of the mixer simulated using SuperMix model. The conversion gain stays around 0 dB and the noise temperature predicted to be around 10 K from 140–260 GHz. (b) The IF heterodyne mixing performance of the mixer simulated using SuperMix model. The mixer gain is flat around 0 dB from $5-18$ GHz, while the noise temperature remains below 10 K up to $\sim$ 20 GHz. It is clearly seen that the RLC resonance is located outside the designated IF band at approximately 27 GHz, freeing up a 20 GHz band for impedance matching.

III. DEVICE FABRICATIONS

A batch of device with the above-described design was fabricated in Paris Observatory's clean room facility using photolithography and self-aligned processing techniques based on the well-known niobium/aluminium (Nb/Al) fabrication technique. The $\mathrm{Nb}_{(200\mathrm{nm})}/\mathrm{Al}_{(\sim10\mathrm{nm})}$-$\mathrm{AlO}_{x(\sim1\mathrm{nm})}/\mathrm{Nb}_{(100\mathrm{nm})}$ trilayer is first in-situ deposited on 300 μm thick quartz substrate (thinned to 100 μm after processing). The finline taper and the ground plane structures were defined using ionic etching



(a)

(b)

Fig. 3. (a) A sub-sector of a 2” wafer containing 7 fabricated SIS mixer devices. (b) Optical microscope image of the 220 GHz SIS mixer device. The tunnel junction is clearly seen in the inset (the circle located at the centre of the yellow square). The yellow square indicates the area where the upper (250 nm) SiO layer was not deposited, so that the Nb wiring layer can have a better contact to the tunnel junction.

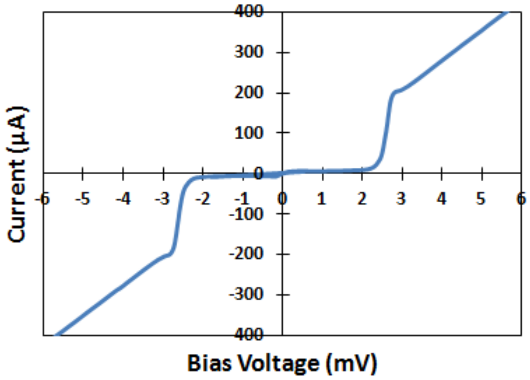


Fig. 4. Typical DC current-voltage (IV) curve of the fabricated SIS mixer devices, measured at liquid helium temperature.

off the trilayer. The 1.5 μm^2 SIS junction was defined using optical lithography and a selective niobium self-aligned etch process, where the upper Nb layer was removed by reactive ionic etching, and then the area around the junction was replaced with a 240 nm thick SiO layer. A new photolithographic step followed up by the deposition of 250 nm SiO layer allowed us to achieve the required SiO thickness of 490 nm in order to realise the designed Nb/SiO/Nb RF tuning microstrip circuit. An upper 400 nm thick Nb layer was then sputtered to provide contact to the tunnel junction and form the Nb/SiO/Nb microstrip wiring layer.

Fig. 4 shows the IV curve of one of the fabricated devices measured at liquid helium temperature. The Josephson current was suppressed by rapid switching of the biasing circuit. As can be seen from the measured IV curve, the fabricated mixer have a very low leakage current (9–10 mA) characteristic, and the tunnel junctions shows a quality ratio (R_{sg}/R_n) of about 15 for a critical current density of $J_c = 9 - 10$ kA/cm^2. We would like to emphasise that the slight slant of the curve near the gap is not intrinsic to the junction behaviour, but is caused by the series resistance introduced by the electronics used to measure these devices.

IV. CONCLUSION

We have presented an SIS mixer design that have broad RF and IF operating bandwidths. We optimised the mixer design using a combination of rigorous electromagnetic and quantum mixing softwares, combining HFSS and SuperMix. The simulation model predicts a broad RF bandwidth of 120 GHz centred around 200 GHz, with the noise temperature remains quantum-limited in the IF frequency range of 0–20 GHz . We have fabricated a batch of these mixer chips on a 100 μm quartz wafer, and we have measured good DC IV characteristic curves. We are currently preparing to measure the RF heterodyne mixing performance of these mixers, and we hope to present the measured results in the forthcoming ISSTT conference in March.

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