Dead-Time Distortion as a Fidelity Limit in Switched Mode Power Amplifiers



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This thesis is dedicated to
my mother,
for her unconditional love.

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Abstract

Switched mode power amplifiers (SMPAs) convert a low-power reference signal into a high-power one. A half bridge is the basic building block of many SMPAs. The nonlinear transfer characteristics of SMPAs lead to undesired distortion in the output. Often, the switching frequency is much larger than the fundamental frequency. Therefore, the output is approximated as a DC output over several consecutive switching cycles in an SMPA. The essential insertion of dead-time in each switching period is one of the dominant sources of distortion. This thesis investigates the dead-time distortion by answering the following questions:

Can the distortion caused by dead-time be completely eliminated by compensation techniques in a half-bridge based on the quasi-static situation? If not, to what extent can this distortion be minimised?

Three models of a half-bridge are investigated to answer these questions. Model 1 assumes all the components are ideal. Models 2 and 3 both include the source-to-drain voltage drop of transistors during the dead-time. Model 2 considers a fixed switching-node capacitor, and Model 3 considers a non-linear capacitor.

A complete analysis of the dead-time distortion of the model 1 is demonstrated. All possible discontinuous conduction modes during the dead-time are considered, and this analysis is valid for all duty cycles. The small ripple approximation is assumed. Based on this analysis, an accurate model of the compensating voltage near the current zero-crossings is proposed. The analysis shows that, by varying the duty cycle, the average voltage error caused by dead-time can be eliminated completely. This is true for any given duty cycle and output current in theory (i.e., with perfect measurements of the inductor current, ideal components and known circuit parameters). However, the removal of the instantaneous voltage error cannot be guaranteed, i.e., the instantaneous voltage error is not zero under some conditions. Experiments show that this model predicts the output voltage to within a few percent.

The analysis of model 2 shows that four situations can occur and reiterate based on the direction of the inductor current and the occurrence of its zero-crossing during the dead-time. An algorithm is proposed to provide numerical solutions to Model 2. Only numerical solutions are possible for Model 3. An improvement in the accuracy is shown in Models 2 and 3 compared with Model 1, through simulation. No significant difference is found between models 2 and 3.

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List of Abbreviations

SMPA . . . . . Switched Mode Power Amplifier

LPA . . . . . Linear Power Amplifier

PWM . . . . . Pulse Width Modulator

ACM . . . . . Approximate Compensation Method

MCU . . . . . Microcontroller

MRI . . . . . Magnetic Resonance Imaging

PCB . . . . . Printed Circuit Board

DCM . . . . . Discontinuous Conduction Mode

GaN . . . . . Gallium Nitride

FET . . . . . Field Effect Transistor

MOSFET . . . Metal Oxide Semiconductor Field Effect Transistor

IGBT . . . . . Insulated-Gate Bipolar Transistor

2DEG . . . . . Two-Dimensional Electron Gas

UART . . . . . Universal Asynchronous Receiver/Transmitter

NPLC . . . . . Number of Power Line Cycles

SSM . . . . . State Space Model

SNR . . . . . Signal-to-Noise Ratio

THD . . . . . Total Harmonic Distortion

THD+N . . . Total Harmonic Distortion plus Noise

List of Symbols

$t_{\mathbf{d}}$ Dead-time.

$T_{\mathbf{sw}}$ Switching period.

τ Normalized dead-time, $\tau = \frac{t_{\mathrm{d}}}{T_{\mathrm{sw}}}$.

$g_{\mathbf{1}}$ Gate signal of the top swtich in a half-bridge.

$g_{\mathbf{2}}$ Gate signal of the bottom swtich in a half-bridge.

x^* Variable x of of an ideal system ($t_{\mathrm{d}} = 0$).

D Duty cycle, i.e., the proportion of time when the top transistor is ON over one switching period.

$T_{\mathbf{on}}(x)$ The ON period of the signal x.

d Duty cycle of g_1^*, i.e., the proportion of the ON period of g_1^* , $T_{\mathrm{on}}(g_1^*)$, over one switching period.

s The reference signal as an Input to the PWM generator.

$I_{\mathbf{o}}$ Average output current.

$V_{\mathbf{i}}$ Input voltage.

$V_{\mathbf{o}}$ Output voltage, which is constant over one cycle.

$i_{\mathbf{L}}$ Inductor current.

$v_{\mathbf{m}}$ Midpoint voltage.

Δv Instantaneous voltage error: $\Delta v(t) = v_{\mathrm{m}}(t) - v_{\mathrm{m}}^*(t)$.

$\langle \Delta v \rangle$ Average voltage error over one switching period: $\langle \Delta v \rangle = \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}} \Delta v(t)\, \mathrm{d}t$.

$t_{\mathbf{0}}$ Time duration when Discontinuous Conduction Mode (DCM) occurs.

$\tau_{\mathbf{0}}$ Time duration when Discontinuous Conduction Mode (DCM) occurs, normalized by T_{sw}.

$t_{\mathbf{a}}$ The amount of time that the ON period of g^* is increasesd or decreased, to generate g in a compensated system.

$\tau_{\mathbf{a}}$ The amount of time that the ON period of g^* is increasesd or decreased, to generate g in a compensated system, normalized by T_{sw}.

M DC conversion ratio in an uncompensated system, i.e., $M = \frac{V_{\mathrm{o}}}{V_{\mathrm{i}}}$ when $t_{\mathrm{d}} > 0$. ($M = D$ when $t_{\mathrm{d}} = 0$).

$M_{\mathbf{meas}}$ The measured DC conversion ratio in the experiment.

$M_{\mathbf{thry}}$ The theretically derived DC conversion ratio.

$\Delta i_{\mathbf{L}}$ Inductor current ripple.

$c_{\mathbf{sw}}$ Switching-node capacitance.

$v_{\mathbf{ds}}$ The bias voltage between the drain and source terminals of a transistor.

$c_{\mathbf{oss}}$ Output capacitance of a transistor as a function of v_{ds}.

$C_{\mathbf{oss}}$ Output capacitance of a transistor as a fixed value.

$C_{\mathbf{L}}$ Parasitic capacitance of a filter inductor.

$C_{\mathbf{pcb}}$ Parasitic capacitance caused by the PCB layout.

$C_{\mathbf{probe}}$ Input capacitance of a probe.

$C_{\mathbf{boot}}$ Bootstrap capacitor.

$i_{\mathbf{boot}}$ Current through the bootstrap capacitor.

$v_{\mathbf{boot}}$ Voltage across the bootstrap capacitor.

$f_{\mathbf{r}}$ Self-resonant frequency of an inductor.

$f_{\mathbf{m}}$ Resonant frequency of v_{m} and i_{L} during the dead-time, caused by the filter inductor and the switching-node capacitance.

$v_{\mathbf{bd}}$ Voltage drop across the transistor from the source to the drian terminal during the dead-time.

ΔD The amount of duty cycle that is increasesd or decreased, to generate g in a compensated system in conventional compensation methods.

$D_{\mathbf{comp}}$ The new duty cycle after compensation methods are implemented in conventional compensation methods.

$I_{\mathbf{th}}$ Threshold current in conventional compensation methods.

$\lambda_{\mathbf{th}}$ Normalized threshold current in conventional compensation methods.

$V_{\mathbf{th}}$ The threshold voltage of a transistor, i.e., the minimum gate-to-source voltage to create a conducting channel between the source and drain terminals.

$v_{\mathbf{gs}}$ The bias voltage between the gate and the source terminals of a transistor.

$v_{\mathbf{gd}}$ The bias voltage between the gate and the drain terminals of a transistor.

$V_{\mathbf{cc}}$ The bias voltage supply to charge the bootstrap capacitor in a gate drive circuit.

$f_{\mathbf{clk}}$ The clock frequency.

$T_{\mathbf{clk}}$ The clock period.

$N_{\mathbf{clk}}$ The number of MCU clocks per switching period: $N_{\text{clk}} = \frac{f_{\text{clk}}}{f_{\text{sw}}}$.

$n_{\mathbf{r}}$ The time instant of the rising edge of a signal in the number of MCU clocks.

$n_{\mathbf{f}}$ The time instant of the falling edge of a signal in the number of MCU clocks.

$t_{\mathbf{off}}$ The time instant of the falling edge of a signal.

$f_{\mathbf{c}}$ Cut-off frequency of a filter.

o Filter order.

1 Introduction

This thesis investigates the dead-time distortion thoroughly and proposes a compensation method. Chapter 1 presents the relevant theoretical backgrounds and motivation of this study, provides a brief introduction of how the insertion of dead-time causes distortion, summarises previous studies, proposes research questions and shows the thesis structure.

1.1 Background

Power amplifiers are electronic devices that convert a low-power reference signal into a high-power one. They are widely employed in domestic and industrial applications, including usage in audio amplification, electrodynamic shaker, Magnetic Resonance Imaging (MRI), and integrated circuit (IC) manufacturing. A common use case is an audio amplifier with the typical narrowest acceptable bandwidth of 20 Hz - 20 kHz. Such amplifiers are used to drive a loudspeaker, which is a coil that further drives the mechanical load. Power amplifiers of electrodynamic shakers are almost the same, apart from the fact that they have a narrower bandwidth, usually up to several kilohertz [1], and higher power ratings. The MRI employs gradient power amplifiers to provide currents into coils, which generate spatially linear variations in the magnetic field to localise the Magnetic Resonance (MR) signal in the area of

interest [2, 3]. High-precision power amplifiers are used for lithographic exposure in IC manufacturing, where they provide current to actuators that move semiconductor wafers and reticles at a sub-nanometer scale [4]. Table 1.2 provides examples of power amplifiers employed in these applications. Their specifications are also listed.

From these examples, we can see that power amplifiers are often employed to drive electromagnetic coils, which may be represented by an inductor in series with a resistor, as shown in Fig. 1.1. The relationship between the ideal output signal of power amplifiers, $x_{\mathrm{o}}(t)$, and the input reference signal, $x^*(t)$, is expected to be:

$$x_{\mathrm{o}}(t) = Ax^*(t), \tag{1.1}$$

where A is the gain of the power amplifier, constant over the bandwidth; x is a voltage or current signal that is a function of time t. The phase shift is not considered in this equation.

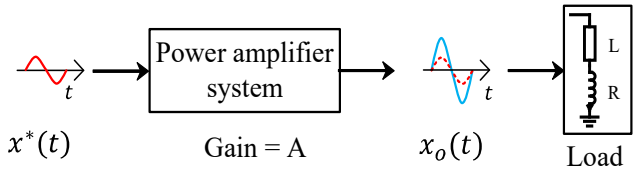


Figure 1.1: Block diagram of a power amplifier system. Typically, the load can be modelled as an inductor in series with a resistor, which is driven directly by the amplifier system.

In practice, undesired signals appear in x_{o} such that (1.1) does not hold. These undesired signals are categorised into noise ($x_{\mathrm{n}}(t)$) and distortion ($x_{\mathrm{d}}(t)$) based on their generation source:

$$x_{\mathrm{o}}(t) = Ax^*(t) + x_{\mathrm{n}}(t) + x_{\mathrm{d}}(t). \tag{1.2}$$

Distortion arises from the time-invariant nonlinear transfer characteristics of power amplifiers. Distortion signals, often referred to as *harmonics*, have their power contained at specific frequencies, i.e, frequencies that are multiples of the fundamental frequency. This result is illustrated by the Fourier series, where a periodic signal of the fundamental frequency is decomposed into a sum of sinusoidal waves, which are multiples of the fundamental frequency. Noise, on the other hand,

comes from random processes or interference. Its power spreads over a certain frequency band, as shown in Fig. 1.2.

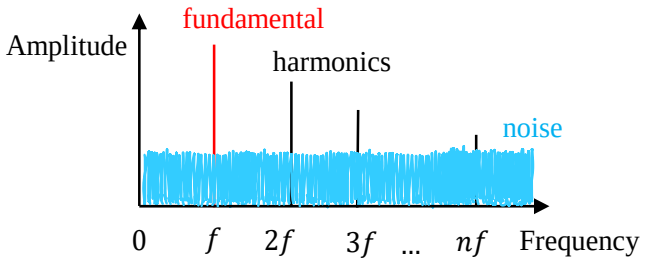


Figure 1.2: Distribution of noise and distortion in the frequency domain. f is the fundamental frequency. The fundamental component is in red. Harmonics are in black. Noise is in blue. Harmonics appear at the multiples of f while noise spreads over a wide spectrum.

1.2 Switched mode power amplifiers and linear power amplifiers

Power amplifiers typically are the end stage of a signal chain, which actually transfers the energy from power supplies to the load. Therefore, efficiency is particularly important as much more heat is dissipated in power amplifiers than that in other stages. For the same power rating, more efficient power amplifiers provide a more compact (remove the demand for a bulky cooling system) and low-cost (savings from less energy consumed, minimal cooling, and extension of battery life) system, which also enables high-power applications.

Power amplifiers can be categorised into Linear Power Amplifiers (LPAs) and Switched Mode Power Amplifiers (SMPAs). LPAs operate transistors in the linear region, which leads to high fidelity. This fact also results in their low efficiency as power amplification is realised when voltage and current occur simultaneously. LPAs include class A, class B, class AB, and class C amplifiers, which are classified by conduction angle, θ, i.e., the percentage of time (described in degrees) of a sinusoidal input that the transistors in an LPA conduct. A conduction angle of 360° ($\theta = 360°$) suggests the transistors conduct over the full period of the input signal, while $\theta = 180°$ implies they only conduct over the half period. Class C amplifiers have

a narrow bandwidth and are typically used for radio-frequency amplification. Its design is a specific topic, and so it is not considered here. SMPAs operate transistors in cut-off and saturated regions, where the current or voltage in the transistors is zero, thus resulting in high efficiency. Typically, pulse width modulation is utilised to convert the reference signal into a pulse format, which is then employed to switch the transistors. A low-pass filter removes the intrinsic distortion caused by the modulation scheme. However, due to various imperfections in SMPAs, for example, deviation in duty cycle due to the finite switching speed of transistors [5], SMPAs tend to have lower linearity. Table. 1.1 summarizes the characters of LPAs and SMPAs [5]. The last column in this table, THD, is discussed in detail in Section 1.3.

Table 1.1: A summary of characteristics of LPAs and SMPAs [5]. η refers to efficiency.

Cat.	Class	θ (°)	η (% theoretical)	η (% typical)	THD (dB)
LPA	A	360	25	10∼20	can be less than -80
	B	180	78.5	50∼ 60	
	AB	180∼ 360	78.5	50∼ 60	
SMPA	D	0	100	85∼ 95	typically -60∼-40

LPAs are intrinsically limited by low efficiency, resulting from their topologies. This cannot be improved, as described in [6]. SMPAs, on the other hand, have the potential to further improve their linearity through other stages, such as the implementation of feedback/feedforward control. This thesis focuses on the improvement of the linearity of SMPAs. This study particularly focuses on a half-bridge-based SMPA as

1. A half-bridge is the simplest topology to implement an SMPA, which simplifies analysis when one individual distortion source is considered.

2. A half-bridge is the basic building block of many complex topologies that are used in an SMPA [7].

1.3 Performance metrics in distribution

Total harmonic distortion (THD) compares the power of all the harmonics against the power of the fundamental signal. It indicates the purity of the fundamental signal and is a commonly used metric that measures distortion. THD is expressed as:

$$\mathrm{THD(dB)} = 20\log_{10}\sqrt{\frac{\sum_{n=2}^{\infty} X_{\mathrm{n}}^2}{X_1^2}} = 10\log_{10}\frac{P_{\mathrm{distortion}}}{P_{\mathrm{signal}}}, \tag{1.3}$$

where X_1 is the amplitude of the fundamental signal; X_{n} is the amplitude of its n^{th} harmonic; $P_{\mathrm{distortion}}$ is the power of harmonics; P_{signal} is the power of the fundamental signal. A high-fidelity audio power amplifier features a THD less than -40 dB [5].

In practice, the THD is measured by setting the input of a power amplifier ($x^*(t)$) to a pure sinusoidal wave at a specific frequency, and then separating fundamental power and harmonic power of $x_{\mathrm{o}}(t)$ [8]. A sinusoidal signal, whose power is contained at the fundamental frequency only, is used as a reference, such that harmonics from the output come from the non-linearity of the amplifier. Typically, the THD of an audio amplifier is measured using a 1 kHz fundamental signal. The distortion of the generator should be much smaller than the lowest distortion value measured by the amplifier. Usually, a margin of at least 10 dB is expected [8]. To find the harmonic power, the amplitude of each harmonic should be known. A highly-selective tunable bandpass filter, such as the one in spectrum analysers, is used to achieve this, as shown in technique (a) in Fig. 1.3. Applying the Fourier series to the measured $x_{\mathrm{o}}(t)$ also finds the amplitude of each harmonic, as shown in technique (b) in Fig. 1.3. The number of harmonics considered to find THD depends on the upper bandwidth limit of the amplifier. For instance, if an audio amplifier with 20 kHz bandwidth has a reference signal of 1 kHz fundamental frequency, then 20^{th} is the highest order of harmonic to be considered. Most harmonic power is contained in the first few harmonics, and many non-linearities lead to harmonic power dominantly contained in the odd harmonics. The fundamental frequency of $x^*(t)$ for THD measurement should be less than a third of the upper bandwidth limit of the amplifier. Typically, THD varies with the amplitude and frequency of the reference signal.

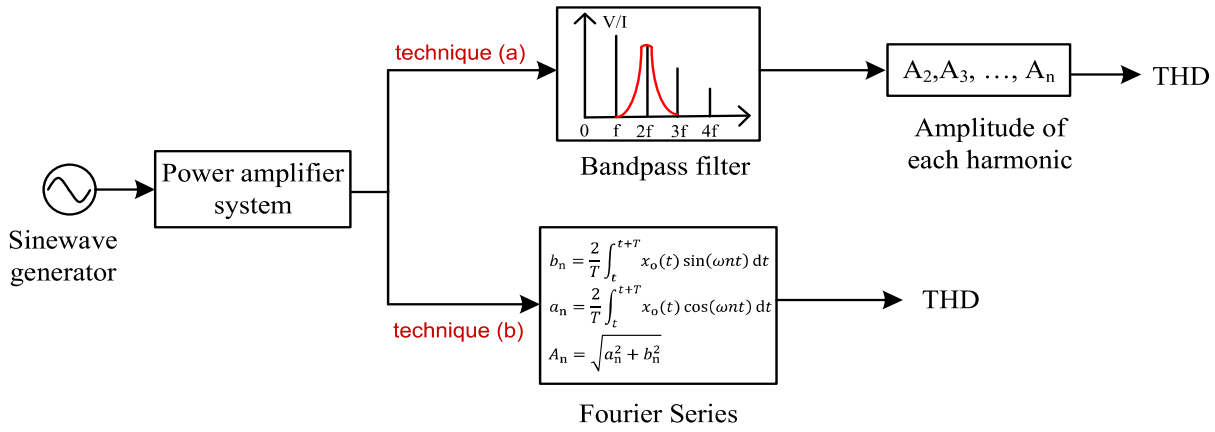


Figure 1.3: Measurement of THD in practice, where a pure sinusoidal wave serves as the reference. The amplitude of each harmonic is found by either applying a tunable bandpass filter or Fourier series, to the output signal. THD is then calculated via (1.3).

Signal-to-noise ratio (SNR), defined as the ratio of signal power (P_{signal}) over noise power (P_{noise}), is a common metric to quantify noise in a system:

$$\text{SNR(dB)} = 10\log_{10}\frac{P_{\text{signal}}}{P_{\text{noise}}}. \tag{1.4}$$

As noise is distributed over a wide frequency spectrum, bandwidth must be specified when SNR is provided.

Total harmonic distortion plus noise (THD+N), defined as the ratio of the power of both harmonics and noise over that of the fundamental signal, is a figure of merit of the overall performance of a system:

$$\text{THD+N(dB)} = 10\log_{10}\frac{P_{\text{noise}} + P_{\text{distortion}}}{P_{\text{signal}}}. \tag{1.5}$$

In practice, THD+N is measured by applying a notch filter, suppressing the power at the fundamental frequency, then applying a bandpass filter, which removes power out of the desired bandwidth, as shown in Fig. 1.4.

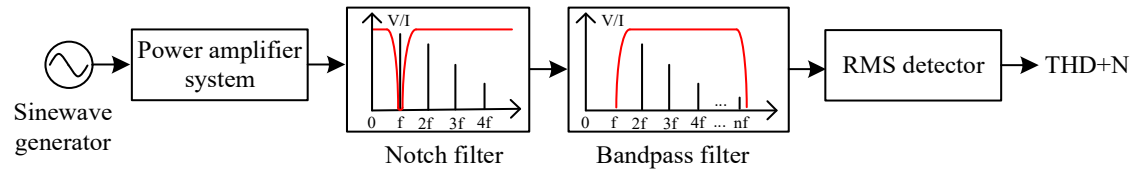


Figure 1.4: Measurement of THD+N in practice. This whole process occurs in a THD+N analyser. RMS detector measures signal power.

Measurement of THD+N is much more convenient than that of THD because it does not need to measure the power of each harmonic separately. Note that often for amplifiers, distortion dominates the power of undesired signals such that THD+N is a good estimate of THD. The lowest value among THD, THD+N, and -SNR (as SNR compares the ratio of P_{signal} over P_{noise}) represents the fidelity performance of an amplifier when it is compared with other amplifiers described by different figures of merit.

Table 1.2 demonstrates a selection of power amplifiers and their key features.

Table 1.2: A review of a selection of power amplifiers in terms of key features: fidelity, bandwidth, efficiency, and power rating.

Cat.	Ref.	Type	Application	THD (min. value) dB	THD+N (min.value) dB	SNR (max. value) dB	Figure of merit dB	Bandwidth Hz	Efficiency (max. value) %	Power Rating (max. value)
Consumer audio amplifiers	[9]	SMPA	Audio	n/a	-74	108	-74	0 - 100 k	90	200 W
	[10]	SMPA	Audio	n/a	-70	110	-70	0 - 192 k	90	38 W
	[11]	SMPA	Audio	n/a	-70	108	-70	0 - 143 k	82.5	20 W
	[12]	SMPA	Audio	n/a	-80	108	-80	0 - 96 k	87	350 W
	[13]	LPA	Audio	n/a	-74	105	-74	0 - 20 k	81.9[0]	3.1 W
	[14]	LPA	Audio	n/a	-64	104	-64	0 - 20 k	70.2	1.25 W
	[15]	LPA	Audio	n/a	-60	105	-60	0 - 20 k	78	1.2 W
	[16]	LPA	Audio	n/a	-63	n/a	-63	0 - 20 k	n/a	1.1 W
Industrial product	[17]	SMPA	MRI	-42	n/a	n/a	-42	> 10 k	n/a	28 kW[∞]
	[18]	SMPA	MRI	-52	n/a	n/a	-52	> 10 k	n/a	70 kW
	[19]	SMPA	Shaker	-52	n/a	n/a	-52	5 - 5 k	95	4.9 kVA
	[20]	SMPA	Shaker	-46	n/a	n/a	-46	5 - 2 k	95	10.4 kVA
Academic research	[4]	SMPA	IC mfg.	-102	n/a	108	-102	10 k	95	10 kVA
	[21]	SMPA	Audio	-80	n/a	95	-80	10 - 20 k	85	1.46 W
	[22]	SMPA	Audio	-68	n/a	n/a	-68	1 - 20 k	89.5	0.1 W
	[23]	SMPA	Audio	-68	n/a	88	-68	20 - 20 k	n/a	16 W
	[24]	SMPA	Audio	n/a	-70	110	-70	0 - 200 k	89.5	3.1 W

This number is incorrect. Equation (8) is correct in [13]. Equation(10) is not, as it ignores the fact that the maximum peak voltage of the load is the value of the DC supply. This efficiency is calculated based on a 5 V (DC supply), 8 Ω (load resistance), and 1.8 W (output power) system on page 16, using equation (10). To achieve 1.8 W output, the DC supply voltage should be 5.4 V instead of 5 V.

1.4 Dead-time as a fidelity limit

1.4.1 Motivation

Previous studies have demonstrated that distortion in a half-bridge based SMPA comes from the insertion of dead-time [25, 26, 27], the Pulse-Width Modulator (PWM) [28, 29, 30, 31], parasitic elements [5, 32, 33], limited DC bus capacitance [34, 35], quantisation distortion from the digital reference signal and digital carrier [36, 37], the nonlinearity of passive filters and the control loop [38, 39]. It is shown that switching harmonics from the PWM and dead-time insertion are the dominant distortion sources in SMPAs [31, 40, 41]. Study [42] points out that dead-time is the most significant contributor to a half-bridge-based SMPA.

Switching harmonics, introduced by the PWM, as well as low-pass filters, typically used to reduce these harmonics, are well understood and thoroughly explained in textbooks, for example, books [5, 31]. Distortion caused by dead-time, compared with switching harmonics and the filter design, is less investigated. Fig. 1.5 shows an example of a half-bridge with a low-pass filter, where o is the order of the filter and f_c is its cut-off frequency.

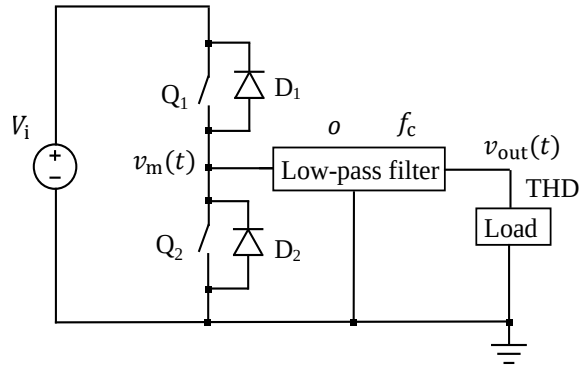


Figure 1.5: A half-bridge with a low-pass filter.

Switching harmonics include carrier harmonics, which occur at multiples of f_sw, and sideband harmonics, which occur around each carrier harmonic with a frequency gap of multiples of the fundamental frequency[1]. They are usually removed

[1]Regular sampled PWM introduces baseband harmonics. They are often negligible because their amplitudes are significantly suppressed with sine-triangular sampled PWM at high modulating ratios, as illustrated in [31].

by a low-pass filter. For switching harmonics, with a specified THD, increasing f_{sw} leads to a less strict filter design, i.e., a low-pass filter with lower o and larger f_{c}. This results in a less complex and more compact design of an SMPA in practice. The insertion of dead-time leads to baseband harmonics [43]. Baseband harmonics cannot be suppressed by the low-pass filter as they are around the fundamental signal, as shown in Fig. 1.6. Study [43] shows that the amplitudes of these baseband harmonics have a linear relation with the ratio of the dead-time over the switching period, $\tau = \frac{t_{\mathrm{d}}}{T_{\mathrm{sw}}}$. Approaches to reduce their amplitudes are (i) reduce τ, i.e., decrease f_{sw} as t_{d} is fixed based on the semiconductor devices used; (ii) correction techniques to eliminate or minimise dead-time distortion.

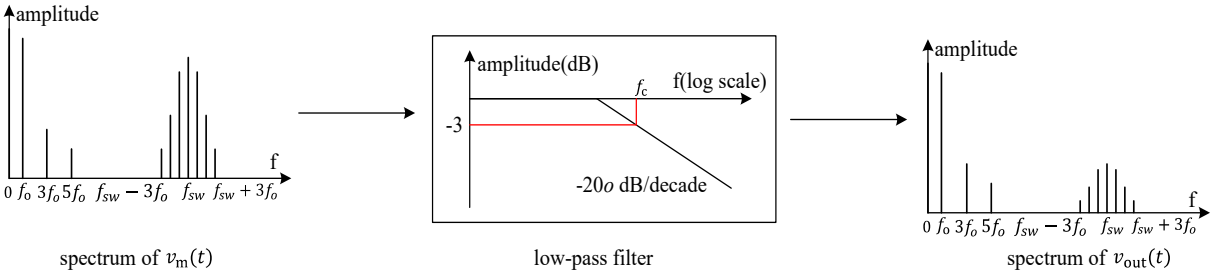


Figure 1.6: A low-pass filter suppresses carrier and sideband harmonics introduced by the PWM. However, it cannot reduce baseband harmonics introduced by t_{d}. The fundamental frequency is denoted as f_{o}.

For an SMPA with a given filter, increasing f_{sw} suppresses switching harmonics further, including carrier harmonics and sideband harmonics. On the other hand, increasing f_{sw} leads to a larger τ, which results in larger baseband harmonics from dead-time. The black curve in Fig. 1.7 demonstrates this process. The switching frequency f_{b} is the break-even point where the harmonics caused by the PWM and the harmonics caused by the dead-time have the same power. Therefore, the THD has its minimum value at f_{b}. When $f_{\mathrm{sw}} < f_{\mathrm{b}}$, switching harmonics are dominant, thus THD drops as f_{sw} increases; when $f_{\mathrm{sw}} > f_{\mathrm{b}}$, baseband harmonics due to dead-time insertion become dominant, thus THD increases as f_{sw} increases.

With dead-time correction techniques implemented, the amplitudes of baseband harmonics are suppressed, which is shown in the red curve in Fig. 1.7. Therefore, the new break-even switching frequency, f'_{b}, where the harmonics caused by the

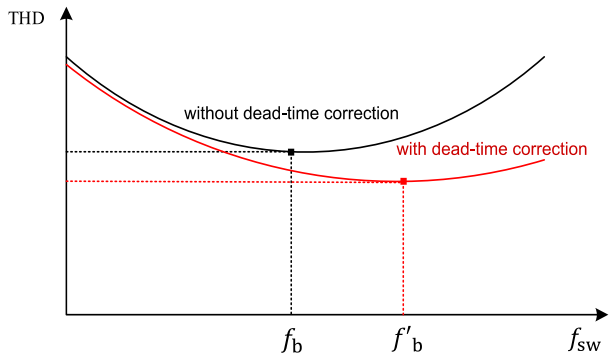


Figure 1.7: Variation of THD v.s. f_{sw} with dead time inserted with a fixed filter. Black curve: SMPAs without dead-time correction techniques; Red curve: with dead-time correction techniques.

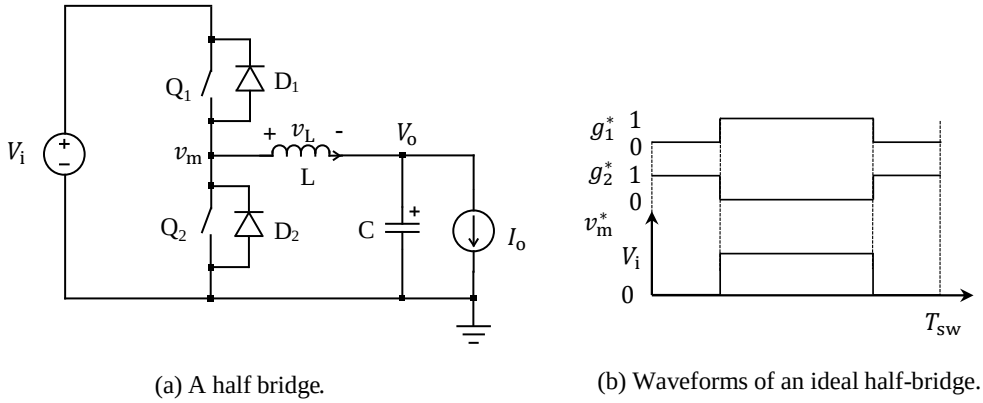
PWM have the same power as those caused by the dead-time, is increased compared to f_b. Compared to the black curve, when $f_{sw} < f'_b$, THD decreases a little, as switching harmonics dominate distortion; when $f_{sw} > f'_b$, THD decreases a lot, as baseband harmonics from dead-time insertion dominate distortion, and its power is decreased by correction techniques.

In brief, the dead-time insertion is one of the dominant distortion sources in an SMPA. It introduces baseband harmonics near the fundamental frequency that are hardly removed by a low-pass filter. These baseband harmonics can be suppressed by decreasing f_{sw}. However, a smaller f_{sw} leads to a strict design of the low-pass filter. An alternative solution to suppress the baseband harmonics caused by the dead-time insertion is to investigate correction techniques. This is the subject of this thesis.

1.4.2 A brief introduction to dead-time distortion

SMPAs normally produce AC output. The switching frequency of most SMPAs is much larger than the frequency of their AC output. Therefore, the output of SMPAs is often approximated as a DC output over several consecutive switching cycles. In the rest of this thesis, the output of a half-bridge is approximated as a DC output. The THD of this output is thus non-applicable. Dead-time is inserted in every switching cycle [44, 31]. In most literature, the distortion on each cycle is investigated and then compensated, assuming a DC output.

Ideal transistors switch instantly. In an ideal half-bridge, which consists of two ideal transistors, the other is turned off simultaneously when one transistor is turned on. Duty cycle, $D \in [0, 1]$, refers to the proportion of time when the gate signal of the top switch in an ideal system, g_1^*, equals logic one over one switching period. Assume in an ideal half-bridge, the gate signal of the top transistor Q_1 is g_1^*, and the gate signal of the bottom transistor Q_2 is g_2^*, then $g_2^* = \overline{g_1^*}$. Fig. 1.8 (a) shows a half-bridge. Fig. 1.8 (b) demonstrates an example of waveforms of the middle-point voltage v_m, gate signals g_1^* and g_2^* in an ideal half-bridge.



(a) A half bridge.

(b) Waveforms of an ideal half-bridge.

Figure 1.8: (a) An example of a PWM half-bridge with an LC filter. If the inductor current i_L flows out of the commutating point, it is defined as positive ($i_\mathrm{L} > 0$). (b) Waveforms of v_m, g_1^* and g_2^* in an ideal half-bridge.

As shown in Fig. 1.8 (b), the waveform of v_m in an ideal half-bridge only depends on g_1^* and V_i, i.e., $v_\mathrm{m} = g_1^* V_\mathrm{i}$. Therefore, the output voltage averaged over one switching cycle, V_o, that depends on D and the input voltage, V_i, is expressed as:

$$V_\mathrm{o} = \frac{1}{T_\mathrm{sw}} \int_0^{T_\mathrm{sw}} v_\mathrm{m} \, \mathrm{d}t \tag{1.6}$$

$$= \frac{V_\mathrm{i}}{T_\mathrm{sw}} \int_0^{T_\mathrm{sw}} g_1^* \, \mathrm{d}t \tag{1.7}$$

$$= DV_\mathrm{i}, \tag{1.8}$$

In practice, however, transistors cannot be turned on instantly. It takes a non-zero amount of time for transistors to transition from a fully-on state to a full-off state. Vice versa. Due to this finite turn-on and turn-off time, if one transistor is turned on immediately after the other transistor is turned off, they may both partially conduct, which causes a short-circuit from the power supply to the

ground through these two partially-on transistors. This short-circuit is also called "shoot-through". To avoid this short-circuit, it is essential to insert a short period of time into the gate signals, so that one transistor of a half-bridge is guaranteed to be completely off before the opposite one is turned on. This short period is known as dead-time (sometimes called "blanking time").

During the dead-time when both transistors are turned off, the inductor current i_{L} freewheels through one of the anti-parallel diodes of the transistors. It may cause v_{m} to differ from the middle-point voltage in an ideal half-bridge, v_{m}^*. This leads to an *instantaneous voltage error*, Δv:

$$\Delta v = v_{\mathrm{m}} - v_{\mathrm{m}}^*. \tag{1.9}$$

This Δv may lead to an *average voltage error*, $\langle \Delta v \rangle$, over one cycle:

$$\langle \Delta v \rangle = \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}} \Delta v \, \mathrm{d}t = V_{\mathrm{o}} - V_{\mathrm{o}}^*. \tag{1.10}$$

A deviation in V_{o} from V_{o}^* exists if the average voltage error is not zero ($\langle \Delta v \rangle \neq 0$). Fig. 1.9 illustrates this deviation caused by the dead-time with two simple examples when $i_{\mathrm{L}} > 0$ and $i_{\mathrm{L}} < 0$. As shown in Fig. 1.9, the middle point voltage v_{m} depends on g_1^*, t_{d} and i_{L}. This deviation are quantified by $\langle \Delta v \rangle$:

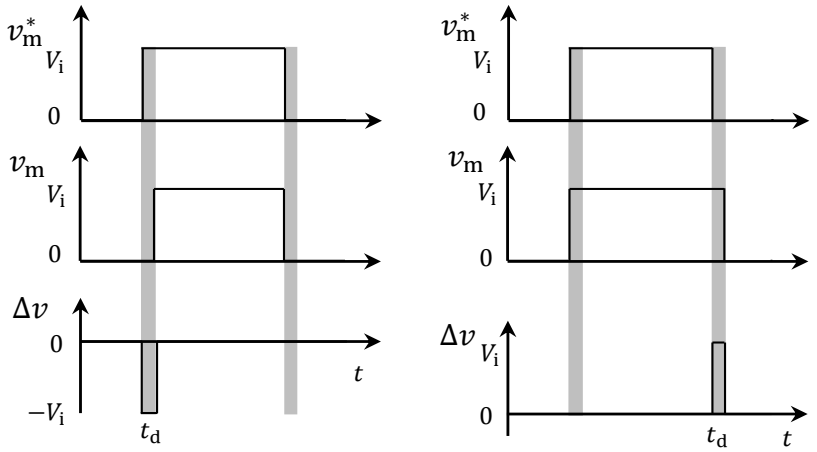
$$\langle \Delta v \rangle = -\frac{V_{\mathrm{i}} t_{\mathrm{d}}}{T_{\mathrm{sw}}} \mathrm{sgn}\left(i_{\mathrm{L}}\right), \tag{1.11}$$

where

$$\mathrm{sgn}\left(x\right) = \begin{cases} 1, & x > 0; \\ -1, & x < 0. \end{cases}$$

Fig. 1.10 demonstrates $\langle \Delta v \rangle$ caused by the dead-time by comparing V_{o} and V_{o}^*.

In this thesis, the *ideal system* refers to a half-bridge with $t_{\mathrm{d}} = 0$, where $g_1 = g_1^*$, $g_2 = \overline{g_1^*}$. The *uncompensated system* refers to a half-bridge with $t_{\mathrm{d}} > 0$. The *compensated system* refers to a half-bridge with $t_{\mathrm{d}} > 0$ and dead-time compensation implemented. The variables of an ideal system are noted with *. The small ripple approximation is assumed such that the output voltage V_{o} is considered constant over one cycle [44] (discussed in Section 1.6.1). All the components are ideal.



(a) $i_L > 0$. (b) $i_L < 0$.

Figure 1.9: The instantaneous voltage error, $\Delta v(t)$, caused by t_d.

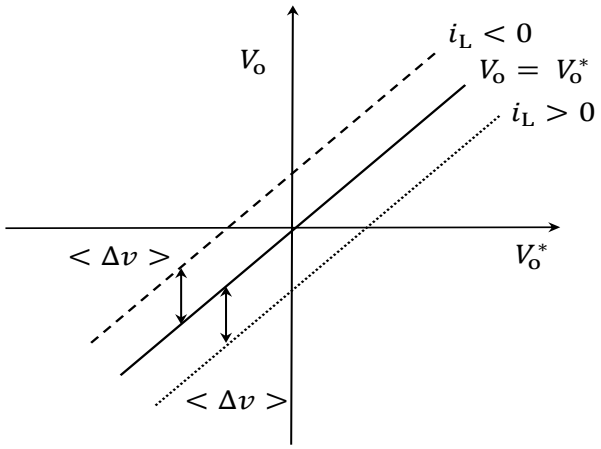


Figure 1.10: The average voltage error, $\langle \Delta v \rangle$, caused by t_d.

1.5 Studies in dead-time compensation

Reference [25] in 1987 first pointed out the existence of dead-time distortion. After that, numerous studies related to dead-time have been published. These studies generally cover two themes:

- development of correction techniques to reduce dead-time distortion [45, 46, 47, 48, 49, 26, 27, 50, 51, 52, 53, 33, 54, 55, 56];
- implementation of correction techniques [57, 58, 59, 60, 61].

Numerous studies have proposed various methods to correct the voltage error

caused by dead-time. These methods can be sorted into two categories: elimination and compensation. Elimination methods remove the requirement to insert t_{d} with novel topologies, such as switching cells [45, 46, 47] and the dual buck [48, 49]. Compensation methods modify the gate signal to obtain V_{o} as close to V_{o}^{*} as possible when $t_{\mathrm{d}} > 0$ [25, 55, 62, 50, 63, 51]. Compensation is more common than elimination. Reasons are as follows:

- Compensation is implemented through the gate signals (software side). An auxiliary circuit (mostly a sensor) is often included to detect the current. No extra modification to the gate drive or the power circuit is required, i.e., a benefit that is easily gained by adding an auxiliary circuit and modifying codes. Elimination is often realised by changes to the power circuit.

- Topologies that do not need the insertion of dead-time sacrifice in other aspects. For example, the dual-buck leads to more power losses by circulating an offset current over the switching cycles [49, 54, 48, 53].

In the compensation methods, two steps are critical:

- identification of the voltage error Δv;

- compensation principles.

An *operating mode* is characterised by the behaviour of v_{m} and i_{L} over one cycle. Models to identify Δv have evolved over time (details in Section 1.5.1), including more operating modes are identified during the dead-time [26, 27, 52, 50], and other factors that can contribute to the distortion during the dead-time are investigated, such as output capacitors [64, 51, 33, 59]. After the model to identify the voltage error is selected, different compensation principles could be used, as discussed in Section 1.5.2.

In th category of implementation of reduction techniques, as shwon in Fig. 1.11, popular topics include: integration of correction techniques into various circuit topologies, for example, three-phase converters [65, 66], multilevel inverters [67, 68];

detection of the polarity of the inductor current, for example, reconstruction of the current [69, 70], and external circuits to detect the polarity [45, 71].

Fig. 1.11 illustrates key topics that are related to the dead-time distortion. There is no distinct boundary among these topics. Often, a study investigates several topics simultaneously. Studies on different topics support and inspire each other's exploration. This thesis focuses on compensation methods.

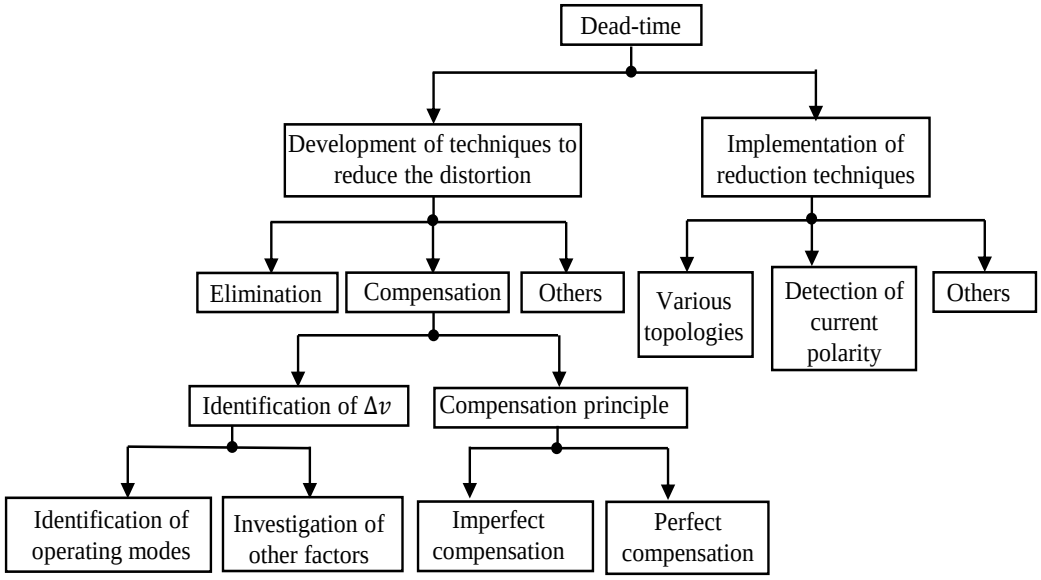


Figure 1.11: Summary of different topics in the dead-time field.

1.5.1 Identification of voltage error

Study [26] proposed the compensation method to minimise this distortion. In that study, the voltage error, Δv, is assumed to rely on the direction of the output current, I_{o}, only. A two-level approximate compensation method, which is described in Section 1.7, is first proposed. Later, study [27] implemented the two-level Approximate Compensation Method (ACM) in digital and analogue methods. A follow-up study [64] considered the impact of the output capacitors on the output voltage during the dead-time, and then put forward a modified two-level ACM which compensates for the distortion caused by the dead-time and the output capacitors.

Study [50] in 2010 first took the impact of the current ripple on i_{L} into account. An additional operating mode, where $i_{\mathrm{L}} < 0$ during the rising-edge dead-time and

$i_{\mathrm{L}} > 0$ during the falling-edge dead-time, is identified. In this operating mode, the average voltage error $\langle \Delta v \rangle$ is zero, and so no compensation is required. Based on this discovery, the three-level and linear ACM are proposed in the study [50] (see Section 1.7 for details). In these three operating modes, i_{L} is continuous over the dead-time, and so SMPAs work in continuous conduction mode over the cycle.

Study [52] demonstrated four transitional operating modes when the inductor current i_{L} crosses zero during the dead-time. In these four operating modes, SMPAs work in discontinuous mode. The actual conversion ratio and the boundaries among these scenarios are presented. Later, a study [51] considered the impact of output capacitors of transistors on the current ripple. As the current i_{L} may charge the output capacitors during the dead-time, the voltage error, Δv, relates to the initial value of i_{L} at the beginning of the dead-time and the output capacitor. By comparing the initial value of i_{L} and $\frac{CV_{\mathrm{i}}}{t_{\mathrm{d}}}$, where C is the sum of the output stray capacitance in the top and bottom transistors, the voltage error Δv is found, which leads to the extra amount of duty cycle that needs to be added or subtracted from the original one to compensate the dead-time distortion.

The key studies that significantly contribute to the evolution of an accurate model to identify Δv are summarised in Fig. 1.12. Many other researchers integrate other topics into the identification proposed in these studies.

1.5.2 Compensation principle

The widely-used compensation methods are generally divided into two categories based on the compensation principle: 1. the instantaneous voltage error is always zero, i.e., $\Delta v \equiv 0$; 2. the average voltage error is always zero, i.e., $\langle \Delta v(t) \rangle \equiv 0$.

One compensation method aims to have Δv always equal to zero, i.e., $\Delta v \equiv 0$, by shifting the rising or falling edges of gate signals [27]. So the average voltage error is always zero ($\langle \Delta v \rangle = 0$). This method is also known as a pulse-based dead-time compensator [27]. Its capability to eliminate dead time effect has been shown in studies [33, 27], with two operating modes, where i_{L} is either positive

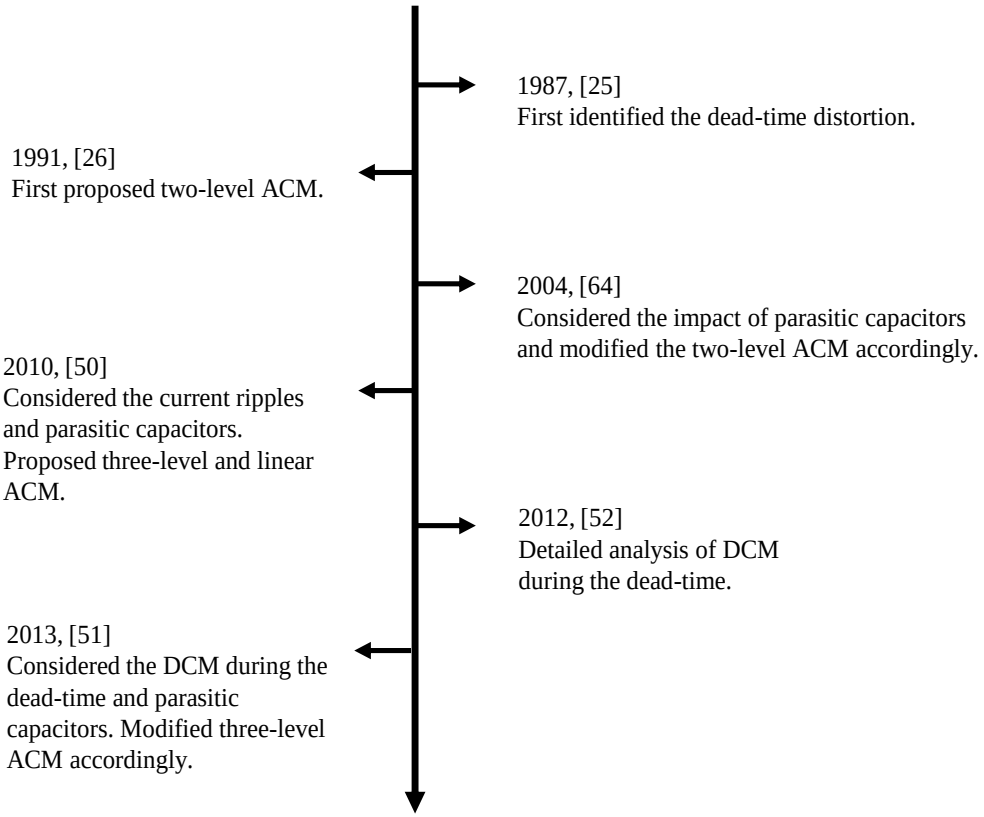


Figure 1.12: Summary of key contributions to the evolution of an accurate model to identify Δv.

or negative, considered. The result of implementing this compensation rule leads to *perfect compensation*, as stated in Section 2.1.

The other compensation method aims to have $\langle \Delta v \rangle$ always equal to zero over one $T_{\rm sw}$, i.e., $\langle \Delta v(t) \rangle \equiv 0$, which can be achieved by decreasing or increasing the original duty cycle [26]. For this method, the instantaneous voltage error $\Delta v(t)$ may not be zero at certain time intervals during the switching period. The result of implementing this compensation rule leads to *imperfect compensation*, as stated in Section 2.1.

The identification of Δv, along with the principle of compensation, determines the effect of compensation, i.e., after compensation, how close $V_{\rm o}$ is to $V_{\rm o}^*$.

1.6 Half-bridge models

This thesis investigates three half-bridge models with different layers of complexity. A trade-off among accuracy, complexity, and computational efforts exists. This

section provides a brief introduction to them.

1.6.1 A half-bridge model with ideal components

This thesis completes the analysis of a half-bridge model that was initially presented in study [52]. All the possible operating modes over the full range of duty cycles are investigated. Components are ideal. The small ripple approximation is widely used in the analysis of converters [44]. It states that for a well-designed converter, the ripple on its output is completely negligible compared with its DC component, and so the output voltage is well approximated by its DC component. This approximation is assumed such that V_{o} can be considered constant over one cycle. The analysis of this model is based on the inductor volt-second balance and the capacitor amp-second balance. That is, in steady state, the net change of inductor current over one switching period is zero, and the net change of capacitor voltage over one switching period is zero:

$$\int_0^{T_{\mathrm{sw}}} v_{\mathrm{L}}\, d\mathrm{t} = 0, \tag{1.12}$$

$$\int_0^{T_{\mathrm{sw}}} i_{\mathrm{C}}\, d\mathrm{t} = 0, \tag{1.13}$$

where v_{L} is the voltage across the filter inductor, i_{C} is the current of the filter capacitor. This half-bridge model is labelled as Model 1.

1.6.2 Half-bridge models with switching-node capacitance and self-commutated reverse conduction

Various factors could affect the accuracy of the half-bridge model presented above. The dominant factor is the switching-node capacitance, c_{sw}. The capacitor c_{sw} is charged and discharged at switching transitions. It includes the output capacitance of the transistors and other parasitic capacitors in the power circuit. The charging and discharging during the dead-time delays the rising or falling of the middle point voltage, which results in a deviation in the output voltage. Voltage drops across transistors during the dead-time could also affect the accuracy, especially when Gallium Nitride (GaN) transistors are used in the half-bridge. A GaN transistor

reversely conducts during the dead-time, and so the inductor current flows through the channel between the source and drain terminals. This is called self-commutated reverse conduction (SCRC), which leads to a higher voltage drop compared to that of the Metal Oxide Semiconductor Field Effect Transistors (MOSFET). This thesis uses GaN transistors in a half-bridge configuration as experimental validation (see Chapter 3). The impact of SCRC and c_{sw} is discussed as follows.

1.6.2.1 Self-commutated reverse conduction

In most half-bridge configurations (see Fig. 1.8 (a)), an inductor L connects to the middle point to filter out high-frequency switching harmonics. When one of the switches is on, the inductor current, i_{L}, flows through the on switch, the inductor, and the load. During the dead-time, this inductor current cannot become zero instantly, so a path must exist for i_{L} to freewheel. A diode in parallel with the switch provides such a path. When the switch is on, this diode is shorted and the current i_{L} flows through the switch. During the dead-time, the inductor current i_{L} freewheels through this diode until one of the switches is on.

MOSFETs are widely used voltage control devices for half-bridge configurations. Each of them has an intrinsic diode, called the body diode, in parallel with the drain-source channel, due to its physical structure [44]. Insulated-Gate Bipolar Transistors (IGBTs) are another widely used devices in half-bridges. They do not have body diodes, so an external diode must be placed in parallel to provide the freewheeling path [44].

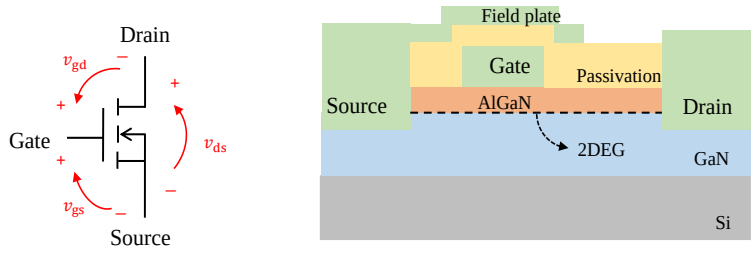
A GaN FET (Field Effect Transistor) has a lateral structure without the p-n doping drift region, so it does not have a body diode [72], as shown in Fig. 1.13. The drain and source are connected through a two-dimensional electron gas (2DEG) channel. The conductivity of this channel relies on the voltage bias between the gate and one of the other terminals. When the bias voltage between the gate and source, v_{gs}, is greater than the threshold voltage, V_{th}, the drain and source are connected through the 2DEG channel so that a current can flow from the drain to the source. When a bias voltage between the gate and the drain, v_{gd},

is greater than V_{th}, a current from the source to the drain can flow through the 2DEG channel. This characteristic allows i_{L} to freewheel through the channel during the dead-time. This feature, that the inductor current i_{L} flows through the 2DEG channel from the source to the drain when $v_{\text{gd}} > V_{\text{th}}$, is named SCRC. The voltage across the drain and the source is:

$$\begin{cases} v_{\text{ds}} = v_{\text{gs}} - v_{\text{gd}}, \\ v_{\text{gd}} \geq V_{\text{th}}. \end{cases} \tag{1.14}$$

In this experiment, the gate is shorted to the source when GAN FETs are OFF, and therefore

$$v_{\text{ds}} = -v_{\text{gd}} \leq -V_{\text{th}}. \tag{1.15}$$



(a) Circuit symbol of a GaN FET. (b) The lateral structure of a GaN FET.

Figure 1.13: (b) is reproduced from [73]. The 2DEG is a very thin layer at the boundary of AlGaN and GaN, which is shown in a dashed line in (b).

The threshold voltage V_{th} is often greater than the forward voltage drop of a body diode. Due to this diode-like behaviour during the dead-time, an ideal GaN FET is often approximated as an ideal switch in parallel with a body diode with a forward voltage drop of v_{th}. This thesis does the same in the following sections. Fig. 1.14 shows an example of the third-quadrant behaviour of a GaN FET.

1.6.2.2 Output capacitor

Due to its structure as shown in Fig. 1.15, GaN FETs have parasitic capacitance between terminals, similar to MOSFETs. The gate-to-drain capacitor, c_{gd}, is the capacitance between the gate terminal and the 2DEG channel. The drain-to-source

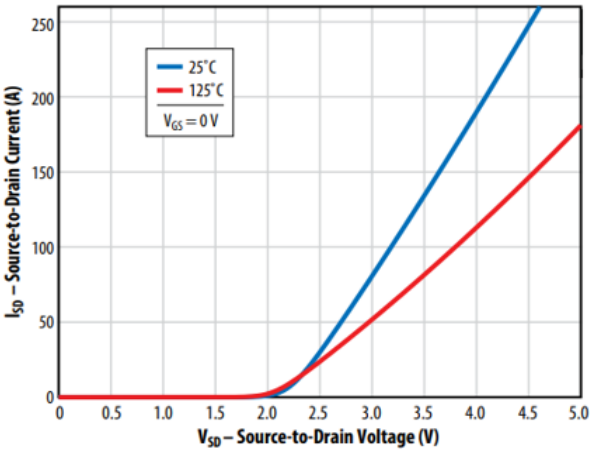


Figure 1.14: An example of the third quadrant operation of a GaN FET. This is the Figure 8 from [74].

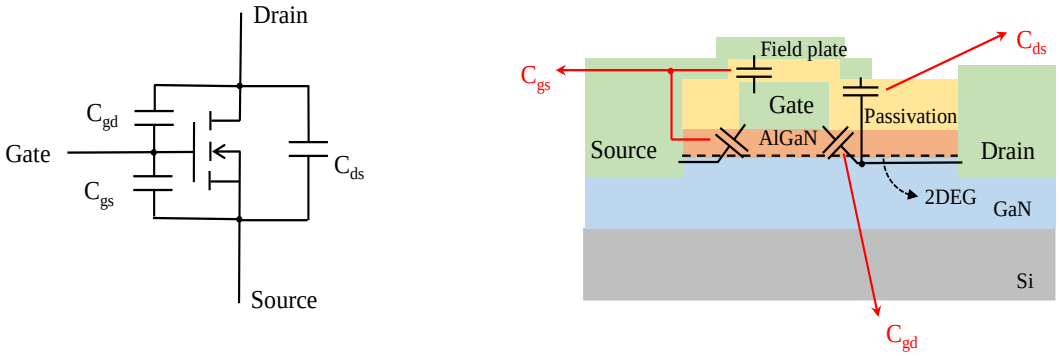
capacitor, c_{ds}, is the one between the field plate and the drain in the channel. The output capacitance, c_{oss}, is the sum of these two [72]:

$$c_{\mathrm{oss}} = c_{\mathrm{gd}} + c_{\mathrm{ds}}. \tag{1.16}$$

This parasitic capacitance is charged and discharged during the switching transition. It is nonlinear, and a function of v_{ds}. A greater v_{ds} extends the depletion region laterally, which increases the distance between the field plate of the source and the drain. Therefore, an increase in v_{ds} leads to a decrease in c_{oss}. As an example, Fig. 3.13 (a) shows c_{oss} of one GaN FET in the EPC23104 chip [75].[2]

During the dead-time, if the current i_{L} reverses its direction (the zero-crossing occurs), the output capacitor c_{oss} of the transistor whose body-diode i_{L} is going to flow through is discharged. The output capacitor c_{oss} of the other transistor is charged by i_{L} simultaneously. After this charging and discharging period, the inductor current i_{L} then flows through the body diode. This process leads to a slow rising and falling edge of v_{m}, which causes a deviation between the theoretical V_{o} and the measured V_{o} (demonstrated in Fig. 3.10 (a) and further discussed in Fig. 3.11 later).

[2]EPC states that each power FET in EPC23104 has the same output capacitance as EPC2252, as they use the same technology and have the same die size.



(a) Parasitic capacitors of a GaN FET.

(b) Location of parasitic capacitors in a GaN FET.

Figure 1.15: Parasitic capacitors exist in a GaN FET due to its physical structure. (b) is reproduced from [73].

1.6.2.3 Other capacitance

Apart from the output capacitor c_{oss}, the switching node capacitor c_{sw} has other contributors.

Small capacitors exist between two proximate turns of the windings of an inductor. These capacitors are defined as the parasitic capacitance of the filter inductor, C_{L}. In the equivalent circuit, the filter inductor C_{L} is parallel with the inductor. An impedance analyser can be used to find C_{L} of an inductor:

$$C_{\text{L}} = \frac{1}{4\pi^2 L f_{\text{r}}^2,} \tag{1.17}$$

where

f_{r}: self-resonant frequency of an inductor.

A capacitor is formed between the switch-node copper on the top layer and the ground layer underneath in the half-bridge Printed Circuit Board (PCB). This capacitor, C_{pcb}, can be estimated by:

$$C_{\text{pcb}} = \frac{A\epsilon_0\epsilon_{\text{r}}}{d,} \tag{1.18}$$

where

A: the overlapped area between the switch-node copper and the ground;

ϵ_0: the permittivity of free space;

ϵ_{r}: the relative permittivity of prepreg;

d: the distance between the switch node layer and the ground layer.

The passive probe measuring v_{m} has an input capacitor, C_{probe}, that contributes to c_{sw}. Fig. 1.16 shows these contributors in a half-bridge.

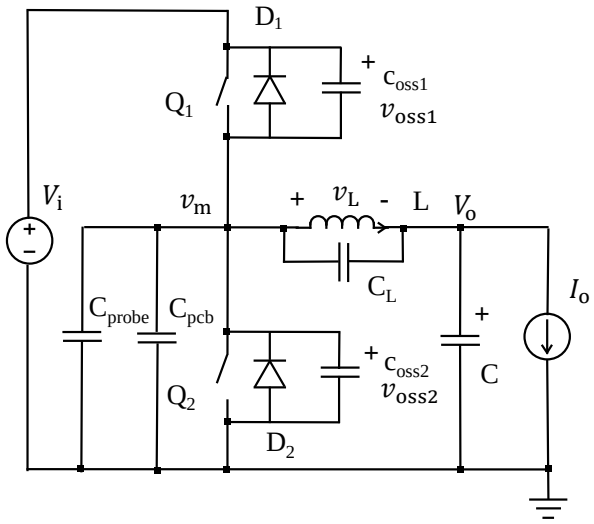


Figure 1.16: A half-bridge with contributors to c_{sw}. In most cases, $c_{\mathrm{oss1}} = c_{\mathrm{oss2}} = c_{\mathrm{oss}}$.

The value of c_{sw} can be approximated from the measured waveforms of v_{m} and i_{L}:

$$c_{\mathrm{sw}} = \frac{\int_{t_1}^{t_2} i_{\mathrm{L}} \mathrm{d}t}{v_{\mathrm{m}}(t_2) - v_{\mathrm{m}}(t_1)}, \tag{1.19}$$

where

t_1: the beginning of a time period used to find c_{sw};

t_2: the end of a time period used to find c_{sw};

$v_{\mathrm{m}}(t_1)$: the magnitude of v_{m} at t_1;

$v_{\mathrm{m}}(t_2)$: the magnitude of v_{m} at t_2.

Based on the above discussion, another two half-bridge models are investigated:

- a half-bridge considering **fixed** C_{oss}, other parasitic capacitance and SCRC, which is labelled as the Model 2;
- a half-bridge considering **variable** c_{oss}, other parasitic capacitance and SCRC, which is labelled as the Model 3.

A trade-off among complexity, accuracy and computational efforts of models exists. Although half-bridge models with c_{sw} and SCRC are more accurate, only numerical solutions are available. The analytical solutions of the Model 1 are presented in Chapter 2, which are polynomial equations. A state space model of the Model 2 during the dead-time is presented in Chapter 4. The analytical equations to calculate v_{m} and i_{L} based on this state space model are presented, assuming initial values of v_{m} and i_{L} are known. However, based on the behaviour of v_{m} and i_{L}, four situations can happen and reiterate in a dead-time, as discussed in Section 4.1, it is too complex to provide an analytical solution to calculate the v_{m} and i_{L} directly by the end of the dead-time. An algorithm, which reiterates analytical equations of the state space model based on the behaviour of v_{m} and i_{L}, is provided to find the numerical solution of V_{o} of Model 2. Only numerical solutions are available for Model 3.

Models 1, 2, and 3 predict the average output voltage to within a few percent. A large c_{sw} is observed in the experiment (see Chapter 3), which leads to errors within [0.03, 0.05] in a small group of cases in models 1,2 and 3. Section 4.3 discusses the contributors to this large c_{sw}. To identify the voltage error more accurately, the impact of the gate driver circuitry could be considered in a half-bridge model. Model 4, which includes the bootstrap capacitor from the gate driver, is thus proposed. Only two cases are simulated in Model 4 to explore whether C_{boot} leads to these errors.

Table 1.3 summarises these models.

1.7 Conventional compensation methods

There are three widely-used compensation methods: two-level ACM [76, 77, 78, 79], three-level ACM [80, 81, 50, 51] and linear ACM [82, 83, 50, 51].

Two-level ACM is proposed based on the two obvious operating modes, where i_{L} is assumed either positive or negative over the switching cycle. When $I_{\mathrm{o}} > 0$, the extra amount of duty cycle over a switching period, ΔD, is added to D, such that the

Table 1.3: Summary of half-bridge models. Models 1, 2 and 3 have a small group of cases where errors are within [0.03, 0.05]. The fourth column 'error' lists the maximum error apart from that group.

Model	Factors considered	Solution	Error
1	ideal components.	analytical	0.03 (see Fig. 3.9)
2	fixed C_{oss}, parasitic capacitors, SCRC.	numerical	0.02 (see Fig. 4.5 (a))
3	variable c_{oss}, parasitic capacitors, SCRC.	numerical	0.02 (see Fig. 4.5 (b))
4	C_{boot}, fixed c_{oss}, parasitic capacitors, SCRC.	numerical	N/A (see Fig. 4.15 and 4.16)

updated duty cycle which compensates the dead-time distortion, D_{comp}, becomes:

$$D_{\text{comp}} = D + \Delta D. \tag{1.20}$$

When $I_{\text{o}} < 0$, the expression of D_{comp} is:

$$D_{\text{comp}} = D - \Delta D, \tag{1.21}$$

where $\Delta D = \frac{V_{\text{i}} t_{\text{d}}}{T_{\text{sw}}}$. Fig. 1.17 (a) shows the compensation rules of the two-level ACM.

Three-level ACM considers the current ripple. Apart from the two operating modes that are included in the two-level ACM, a third operating mode, where $i_{\text{L}} > 0$ during the rising-edge dead-time and $i_{\text{L}} < 0$ during the falling-edge dead-time, is considered. In this operating mode, the average voltage deviation is zero intuitively, and so no compensation rule is required. A threshold current, I_{th}, is identified to find D_{comp}:

$$\begin{cases} D_{\text{comp}} = D + \Delta D, & I_{\text{o}} > I_{\text{th}}; \\ D_{\text{comp}} = D, & -I_{\text{th}} \leq I_{\text{o}} \leq I_{\text{th}}; \\ D_{\text{comp}} = D - \Delta D, & I_{\text{o}} < -I_{\text{th}}. \end{cases} \tag{1.22}$$

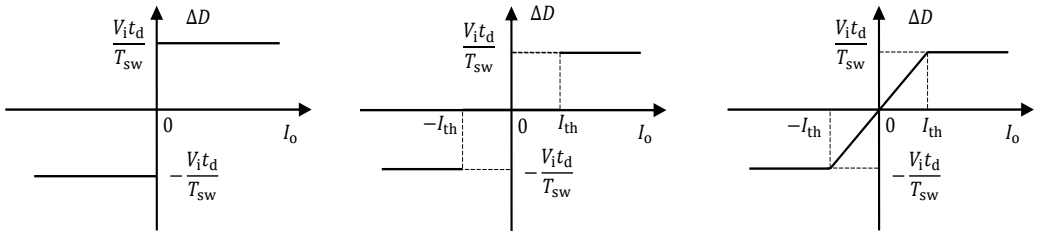
Fig. 1.17 (b) shows the compensation rules of the three-level ACM.

Linear ACM considers transitional operating modes apart from the three operating modes that the three-level ACM includes. It assumes that ΔD is linear

to I_{o} over the threshold period:

$$\begin{cases} D_{\mathrm{comp}} = D + \Delta D, & I_{\mathrm{o}} > I_{\mathrm{th}}; \\ D_{\mathrm{comp}} = D + \frac{\Delta D I_{\mathrm{o}}}{I_{\mathrm{th}}}, & -I_{\mathrm{th}} \leq I_{\mathrm{o}} \leq I_{\mathrm{th}}; \\ D_{\mathrm{comp}} = D - \Delta D, & I_{\mathrm{o}} < -I_{\mathrm{th}}. \end{cases} \tag{1.23}$$

Fig. 1.17 (c) shows the compensation rules of the linear ACM.



(a) Two-level ACM. (b) Three-level ACM. (c) Linear ACM.

Figure 1.17: ΔD in three conventional compensation methods. This is reproduced from [51].

Even though these ACMs are commonly used in the dead-time compensation, the equation to find I_{th} is unclear. No literature has investigated what the value of I_{th} is to implement these widely-used ACMs. Therefore, different studies use different equations to calculate I_{th}, as mentioned in [56]. As shown in Section 2.4, this thesis, for the first time, points out the equation to find I_{th} in (2.112). Reasons are presented in that section.

1.8 Research questions and thesis outline

No literature has investigated all the possible operating modes over the full range of duty cycle. Therefore, the voltage error caused by the dead-time insertion is not fully understood. Currently, an oversimplified approximation of the compensating voltages is often taken near the current zero-crossings [50, 51, 82, 55, 83, 81, 80].

This thesis fills this research gap by answering the following questions:

Can the distortion caused by dead-time be completely eliminated by compensation techniques in a half-bridge based on the quasi-static situation?

If not, to what extent can this distortion be minimised?

The rest of the thesis is organised as follows.

Chapter 2 presents the mathematical analysis of Model 1 over the full range of duty cycle. Actual conversion ratios are demonstrated. Based on that, compensation rules that minimise the dead-time distortion are proposed. It shows that, in some cases, the compensation rules completely eliminate this distortion. This compensation method is compared with conventional ones analytically. When the dead-time is relatively large compared with the switching period, the proposed compensation rules are closer to the linear ACM. When the dead-time is relatively small compared with the switching period, the proposed compensation rules are closer to the three-level ACM.

Chapter 3 presents an experiment to measure the actual conversion ratios. The setup of the power circuit and the generation of gate signals are demonstrated. The measurement accuracy is discussed. 15,500 cases are conducted, and the values of V_{in}, V_{out}, and I_{o} are automatically measured. Model 1 agrees with the experimental results within an error band. Most cases have an error of less than 0.03. A small region has an error between 0.03 and 0.05. Waveforms of a case with a small discrepancy and waveforms of a case with a large discrepancy are discussed as examples. The proposed compensation method is compared with the three conventional ones via interpolation of the experimental dataset. The proposed one reduces errors within 0.03 while the others have a maximum error of 0.1 ($\tau = 0.1$ in this experiment).

Chapter 4 introduces Models 2 and 3, where switching-node capacitance and SCRC are considered. Model 2 includes a fixed C_{oss}. Based on whether i_{L} changes its direction (i) at the beginning of the dead-time, (ii) during the dead-time, four situations are identified. An analytical equation is presented to find i_{L} and v_{m}. An algorithm that considers the reiteration of the four situations is proposed. Model 3 includes a variable c_{oss}. Simulated results of Models 2 and 3 are presented and compared to the measured ones. Model 2 further reduces errors compared to Model 1. Simulated results of the Model 3 are very similar to those of Model 2. To identify the voltage error caused by the dead-time more accurately, Model 4, which

includes the bootstrap capacitor from the gate drive circuitry, is explored. Simulated waveforms from Models 2, 3 and 4 are compared to the measured waveforms.

Chapter 5 summarises the key contributions of this study and proposes future work.

The material presented in this thesis has been drafted for publication in an abbreviated format in the following publication:

Pengling Li and Dan Rogers, "A complete analysis of dead-time distortion and compensation in symmetric pulse width modulated half-bridges".

2

Analysis of the half-bridge model and its compensation

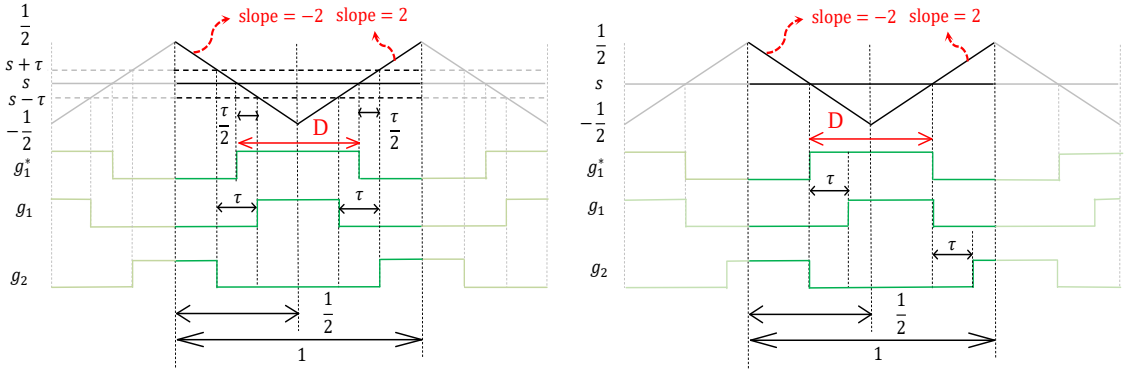
Chapter 2 presents a complete analysis of the dead-time distortion in the half-bridge model (model 1) shown in Fig. 1.8 (a), where two assumptions hold: (i) The output voltage V_o is constant over a switching period. (ii) Components are ideal. This analysis is valid for all duty cycles, considering all possible discontinuous conduction modes during the dead-time. There are eleven distinct operating modes, of which four are new. DC conversion ratios for these operating modes are derived. A compensation method is proposed based on the analysis. It shows that by varying the duty cycle, the average voltage error caused by dead-time can be eliminated completely for any given duty cycle and output current. This compensation method is compared with conventional compensation methods, and agreement is shown with the three-level compensation method when the ratio of the dead-time to the switching period is very small.

2.1 Problem Setup

There are two widely-used options to insert dead-time into gate signals of an ideal system (g_1^* and g_2^*) to generate gate signals for an uncompensated system (g_1 and g_2) [84, 85, 86, 63, 87]:

1. symmetric insertion: the rising edges of g_1^* and g_2^* are delayed by $\frac{\tau}{2}$ and the falling edges are advanced by $\frac{\tau}{2}$ to generate g_1 and g_2, as shown in Fig. 2.1 (a).

2. asymmetric insertion: the rising edges of g_1^* and g_2^* are delayed by τ to generate g_1 and g_2, as shown in Fig. 2.1 (b).



(a) Symmetric insertion. (b) Asymmetric insertion.

Figure 2.1: Dead-time insertion. s: reference signal as an input. D: duty cycle. g_1^*: the gate signal of the high-side switch in an ideal system. g_1 and g_2: gate signals of high-side and low-side switches in an uncompensated system, respectively. (a) The dead-time is symmetric about the central axis. (b) The dead-time is asymmetric about the central axis.

The only difference between these two options is that gate signals in option 2 are delayed by $\frac{\tau}{2}$ relative to gate signals in option 1 in the time domain, i.e., a phase-shift. In the steady state of DC-DC conversion, where the same gate signals repeat over switching cycles, the phase-shift has no imapct to the output voltage. The waveforms of i_{L} and v_{m} have the same phase shift accordingly. However, if the low-side gate signal is set as a reference, the relative waveform of any signals in both options is the same. Option 1 is chosen to present the analysis. This analysis can also be applied to option 2, and to other insertion options that produce gate signals with any phase shifts compared to those in option 1. The difference in the results is that all the wavewfoems have the same phase-shift as that in the gate signals.

Option 1 operates as follows: The reference signal, s, is the input to a symmetric double-edged PWM generator. The carrier varies from $-\frac{1}{2}$ to $\frac{1}{2}$. Within the

generator, two values, $(s-\tau)$ and $(s+\tau)$, are compared with the carrier. When $(s-\tau)$ is greater than the carrier, a logic high appears in g_1; When $(s+\tau)$ is greater than the carrier, a logic low appears in g_2. g_1 and g_2 are then employed to drive the switches Q_1 and Q_2 respectively.

The duty cycle, D, is a key parameter in much of the literature related to the dead-time. As shown in Fig. 2.1, due to similarity in triangles, the relation between D and s is:

$$\frac{D}{1} = \frac{(s+\frac{1}{2})}{1}. \tag{2.1}$$

We define $s \in \left[-\left(\frac{1}{2}+\tau\right), \frac{1}{2}+\tau\right]$. The expression, $D = s + 0.5$, does not hold all the time. The relation bwteen D and s is based on the range of s, as shown in Fig. 2.2.

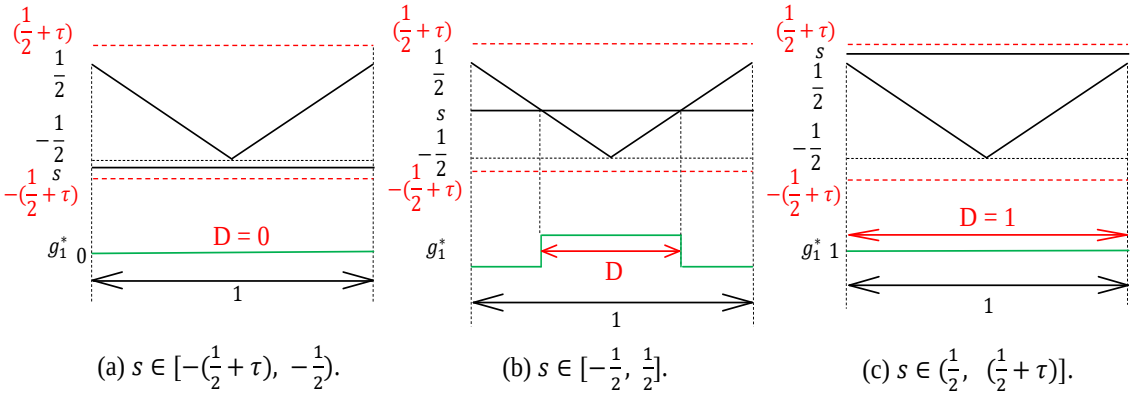


Figure 2.2: Relationship between D and S based on the range of s.

As shown in Fig. 2.2, the relation is expressed as:

$$D = \begin{cases} 0, & s \in \left[-\left(\frac{1}{2}+\tau\right), -\frac{1}{2}\right); \\ s+\frac{1}{2}, & s \in \left[-\frac{1}{2}, \frac{1}{2}\right]; \\ 1, & s \in \left(\frac{1}{2}, \frac{1}{2}+\tau\right]. \end{cases} \tag{2.2}$$

This thesis uses the notation s instead of D in the analysis. Reasons are as follows:

- The reference signal s describes all the possible cases with t_d inserted. The duty cycle D only describes the cases with $s \in [-0.5, 0.5]$. The difference among cases with $s \leq -0.5$ is not reflected by the duty cycle, as $D = 0$ in these cases. Similarly, the difference among cases with $s \geq 0.5$ is not reflected

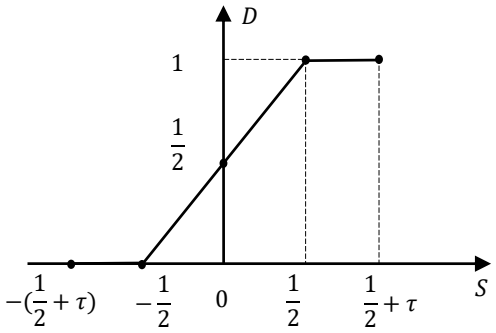


Figure 2.3: Expression of the relationship between D and S, as shown in (2.2).

by the duty cycle as $D = 1$. Fig. 2.4 demonstrates two examples to show the limitations of the notation D.

- The main reason why the duty cycle D is widely used in literature is that, when the dead-time distortion is not considered, key variables of a half-bridge, i.e., the output voltage V_o and gate signals, can be easily described by D:
  (i) The output voltage, V_o, is a linear function of D, as shown in (1.8), such that V_o is easily calculated from a given D.
  (ii) The on and off period of gate signals is clear for a given D.
  However, when the dead-time distortion is considered, the output voltage V_o is no longer linear with D. This is because V_o depends on t_d and i_L, as shown in Fig. 1.9. Therefore, the duty cycle D is less informative in the analysis related to dead-time.

- The reference signal s simplifies the analysis by making equations and plots symmetric about the origin in the coordinate plane made of s and the normalised output current, λ, as discussed later.

In this study, the output current I_0 and the dead-time t_d are normalized to produce λ and τ:

$$\lambda = \frac{2I_0 L}{V_\mathrm{i} T_\mathrm{sw}}, \tag{2.3}$$

$$\tau = \frac{t_\mathrm{d}}{T_\mathrm{sw}}. \tag{2.4}$$

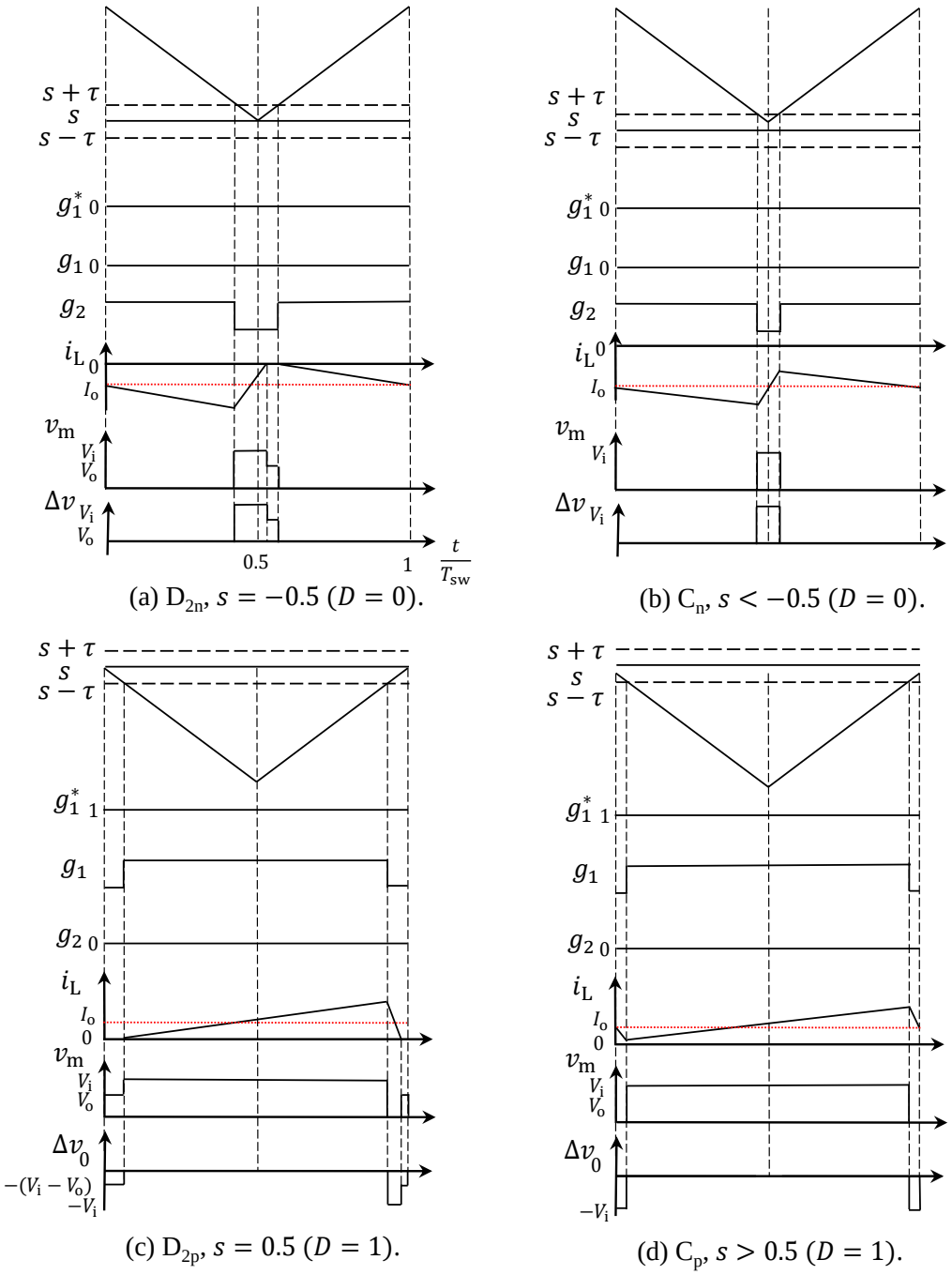
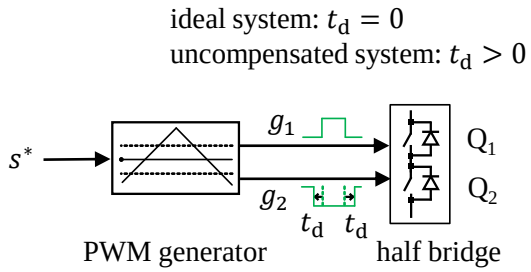


Figure 2.4: Examples of limitation in D to describe cases. Examples in (a) and (b) have the same I_o and $D=0$. Examples in (c) and (d) have the same I_o and $D=1$.

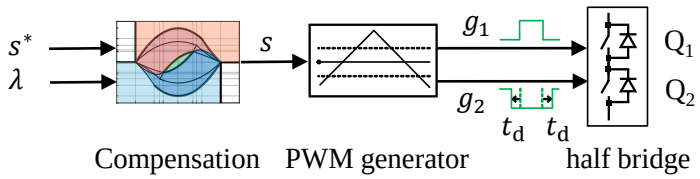
The reason to use λ is mainly that (i) the term $\frac{2I_0L}{V_iT_{sw}}$ repeatedly appears in the mathematical equations (see Section 2.2). Use of λ simplifies these equations. (ii) The previous study [52] uses λ in its derivation. This study keeps this notation. Current ripple, $2\Delta i$, is propotional to $\frac{V_iT_{sw}}{L}$. Therefore, λ indicates how large the

current ripple is compared with the output current. A small λ means that the current ripple is comparable with the output current; a large λ means that the current ripple is negligible compared with the output current.

Fig. 2.5 demonstrates the gate signal generation in an ideal, compensated and uncompensated half-bridge, respectively.



(a) Generation of gate signals with t_d inserted.



(b) Generation of gate signals with t_d inserted in a compensated system.

Figure 2.5: A symmetric double-edged PWM generator is employed to generate gate signals with dead-time.

The results of implementing a compensation method can be divided into two categories:

- *Perfect correction* achieves $\Delta v \equiv 0$ (and so $\langle \Delta v \rangle \equiv 0$), i.e., $v_{\mathrm{m}}^* \equiv v_{\mathrm{m}}$.
- *Imperfect correction* achieves $\langle \Delta v \rangle \equiv 0$ but $\Delta v \not\equiv 0$. In this category, Δv is non-zero at some intervals during one cycle.

Both perfect and imperfect correction guarantee $V_{\mathrm{o}} \equiv V_{\mathrm{o}}^*$.

2.2 Analysis of dead-time distortion

Study [52] identified seven operating modes, showing expressions of M for each one when the range of D is

$$\frac{1}{2} + \check{s} \leq D \leq \frac{1}{2} + \hat{s} : \tag{2.5}$$

2. Analysis of the half-bridge model and its compensation

1. C_p: Positive continuous conduction mode;

2. D_{2p}: Second positive discontinuous conduction mode;

3. D_{1p}: First positive discontinuous conduction mode;

4. C_0: Zero continuous conduction mode;

5. D_{1n}: First negative discontinuous conduction mode;

6. D_{2n}: Second negative discontinuous conduction mode;

7. C_n: Negative continuous conduction mode.

The symbols $\check{s}$ and $\hat{s}$ are:

$$\check{s} = -\frac{\sqrt{1-4\tau}}{2}, \tag{2.6}$$

$$\hat{s} = \frac{\sqrt{1-4\tau}}{2}. \tag{2.7}$$

This section completes the analysis in [52] by extending the range of D into $[0, 1]$. However, it uses s notation. Four additional operating modes are identified and called:

1. D_{pn}: Discontinuous conduction mode at positive and negative edges;

2. D_{np}: Discontinuous conduction mode at negative and positive edges;

3. C_{0p}: Positive continuous conduction mode at small duty cycles, where $s^* \leq (\tau - \frac{1}{2})$, $\lambda \geq 0$;

4. C_{1n}: Negative continuous conduction mode at large duty cycles, where $s^* \geq (\frac{1}{2} - \tau)$, $\lambda \leq 0$.

Table 2.1: Operating modes and their counterparts in an uncompensated system.

derivation	operating mode	counterpart
ref [52]	C_p	C_n
	D_{2p}	D_{2n}
	D_{1p}	D_{1n}
this work	D_{pn}	D_{np}
	C_{0p}	C_{1n}

These operating modes have rotational symmetry about the point of $s^* = 0, \lambda = 0$ (see Fig. 2.20). Or equivalently, they have a reflection about the axis $s^* = 0$ and the axis $\lambda = 0$. Table 2.1 pairs these operating modes.

The conversion ratio, M, is defined as:

$$M = \frac{V_o}{V_i}. \tag{2.8}$$

During the dead-time, the inductor current i_L flows through the body diode of one transistor. When i_L freewheels through D_1 ($i_L < 0$), the middle point voltage equals the input voltage ($v_m = V_i$), and so the value of i_L decreases at the slop of:

$$\frac{di_L}{dt} = \frac{V_i - V_o}{L}. \tag{2.9}$$

When i_L freewheels through D_2 ($i_L > 0$), the middle point voltage equals zero ($v_m = 0$), and so the value of i_L decreases at the slop of:

$$\frac{di_L}{dt} = \frac{V_o}{L}. \tag{2.10}$$

As the current i_L decreases during the dead-time, it may become zero before one of the transistors is turned on. The time period when $i_L = 0$ during the dead-time is defined as t_0. The symbol τ_0 is defined as the normalized t_0 against T_{sw}:

$$\tau_0 = \frac{t_0}{T_{sw}}. \tag{2.11}$$

During the time period t_0, as the inductor current i_L remains zero, the voltage across the inductor L is zero ($v_L = 0$). Therefore, the middle point voltage equals the input voltage ($v_m = V_o$).

2.2.1 Existing operating modes

The analysis of the seven operation modes that are presented in [52] is demonstrated as follows, with notations applied in this thesis. Fig. 2.13 summarises the waveforms of all the operating modes.

2.2.1.1 Operating mode C_p

Fig. 2.6 shows the waveforms of C_p. In this operating mode, the current i_L is always positive. During the dead-time, the current i_L flows through D_2, and so the middle point voltage equals zero ($v_m = 0$). The expression of M is:

$$M = s + 0.5 - \tau. \tag{2.12}$$

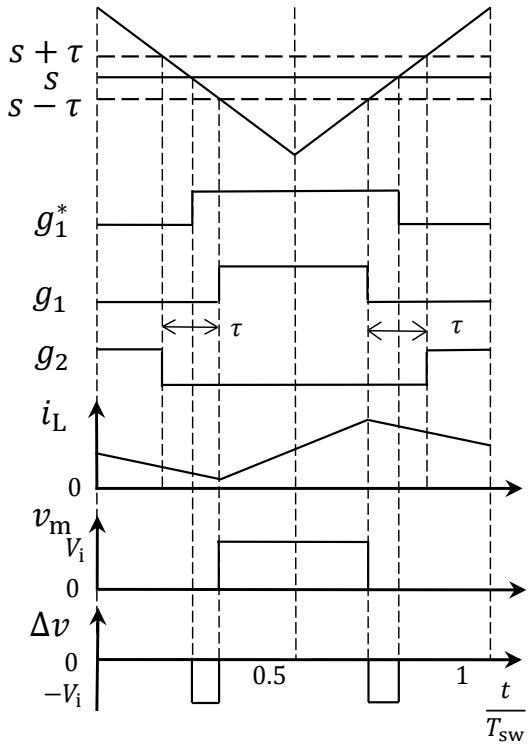


Figure 2.6: Waveforms of the operating mode C_p.

2.2.1.2 Operating mode D_{2p}

Fig. 2.7 shows the waveforms of D_{2p}. During the rising-edge dead-time, the current i_L is initially positive, flowing through D_2, and so the middle point voltage equals zero ($v_m = 0$). Then the current i_L decreases to zero, and stays at zero until Q_1 is turned on. During this period t_o, the middle point voltage equals the input voltage ($v_m = V_o$). In the falling-edge dead-time, as the current i_L remains positive and freewheels through D_2, the middle point voltage equals zero ($v_m = 0$). The expression of M is:

$$M = \frac{(s + 0.5 - \tau)^2}{(s + 0.5 - \tau)^2 + \lambda}. \tag{2.13}$$

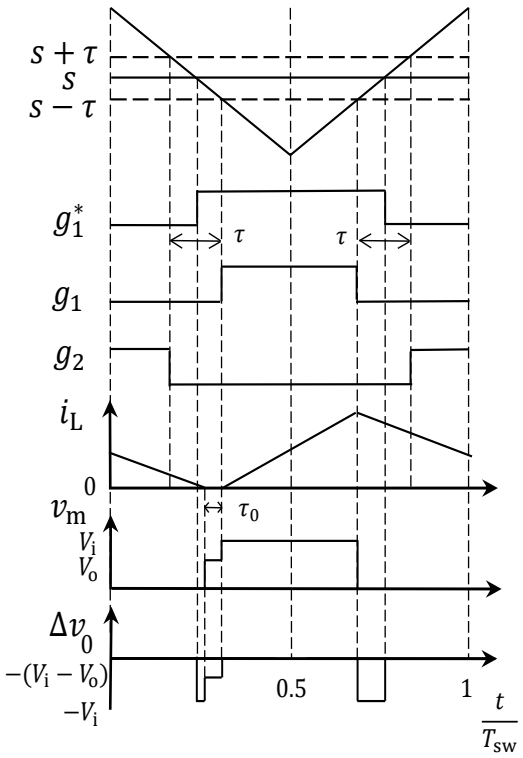


Figure 2.7: Waveforms of the operating mode D_{2p}.

2.2.1.3 Operating mode D_{1p}

Fig. 2.8 shows the waveforms of D_{1p}. During the rising-edge dead-time, the current i_L is initially negative, flowing through D_1, and so the middle point voltage equals the input voltage ($v_m = V_i$). The current i_L decreases to zero, and then stays at zero until Q_1 is turned on. During the time period t_o, the middle point voltage equals the output voltage ($v_m = V_o$). In the falling-edge dead-time, as i_L remains positive and freewheels through D_2, the middle point voltage equals zero ($v_m = 0$). The expression of M is:

$$M = \frac{(s-0.5)^2}{(s+1.5-2\tau)(0.5-s))-\lambda}. \tag{2.14}$$

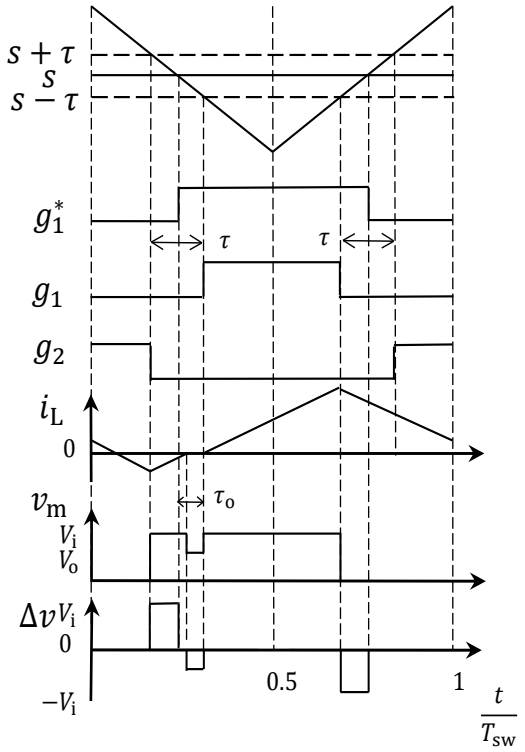


Figure 2.8: Waveforms of the operating mode D_{1p}.

2.2.1.4 Operating mode C_0

Fig. 2.9 shows the waveforms of C_0. During the rising-edge dead-time, the current i_L is negative always, flowing through D_1, and so the middle point voltage equals the input voltage ($v_m = V_i$). In the falling-edge dead-time, as the current i_L remains positive and freewheels through D_2, the middle point voltage equals zero ($v_m = 0$). The voltage gain obtained in the rising-edge dead-time is cancelled out by the voltage loss obtained in the falling-edge dead-time. Therefore, the average voltage error $\langle \Delta v(t) \rangle$ caused by dead-time is intrinsically zero. The expression of M is:

$$M = s + 0.5. \tag{2.15}$$

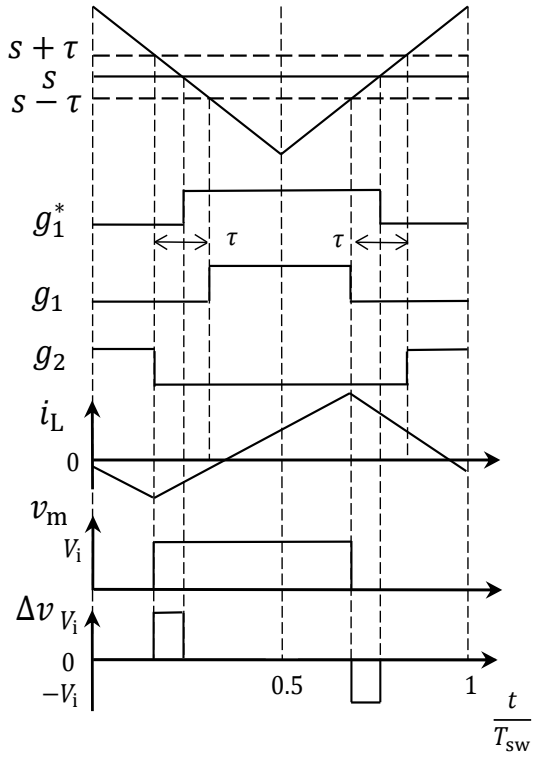


Figure 2.9: Waveforms of the operating mode C_0.

2.2.1.5 Operating mode D_{1n}

Fig. 2.10 shows the waveforms of D_{1n}. During the rising-edge dead-time, the current i_L is negative always, flowing through D_1, and so the middle point voltage equals the input voltage ($v_m = V_i$). In the falling-edge dead-time, the current i_L is positive initially, freewheeling through D_2, the middle point voltage equals zero ($v_m = 0$). After i_L becomes zero, the middle point voltage equals the output voltage ($v_m = V_o$) until Q_2 is turned on. The expression of M is:

$$M = \frac{(s+0.5)^2}{(s+0.5)(1.5-s-2\tau)+\lambda}. \tag{2.16}$$

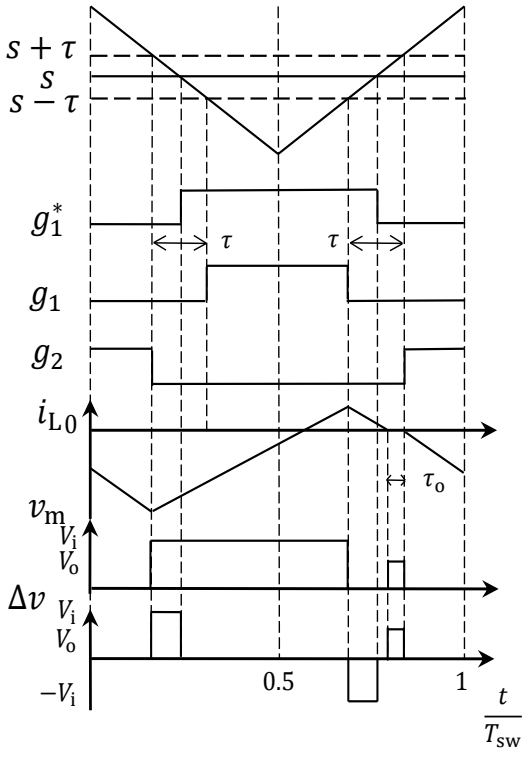


Figure 2.10: Waveforms of the operating mode D_{1n}.

2.2.1.6 Operating mode D_{2n}

Fig. 2.11 shows the waveforms of D_{2n}. During the rising-edge dead-time, the current i_L is negative always, flowing through D_1, and so the middle point voltage equals the input voltage ($v_m = V_i$). In the falling-edge dead-time, the current i_L is negative initially, freewheeling through D_1, the middle point voltage equals the input voltage ($v_m = V_i$). After i_L becomes zero, the middle point voltage equals the output voltage ($v_m = V_o$) until Q_2 is turned on. The expression of M is:

$$M = 1 - \frac{(0.5 - s - \tau)^2}{(0.5 - s - \tau)^2 - \lambda}. \tag{2.17}$$

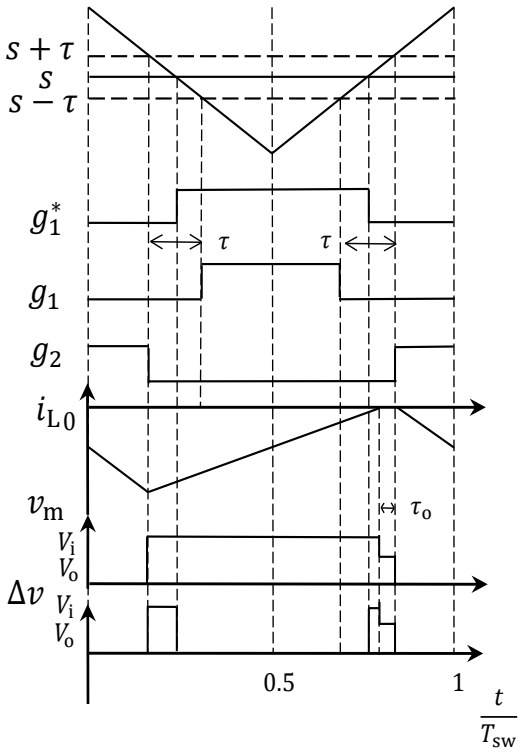


Figure 2.11: Waveforms of the operating mode D_{2n}.

2.2.1.7 Operating mode C_n

Fig. 2.12 shows the waveforms of C_n. The current i_L is always negative. During the dead-time, the current i_L flows through D_1, and so the middle point voltage equals the input voltage ($v_m = V_i$). The expression of M is:

$$M = s + 0.5 + \tau. \tag{2.18}$$

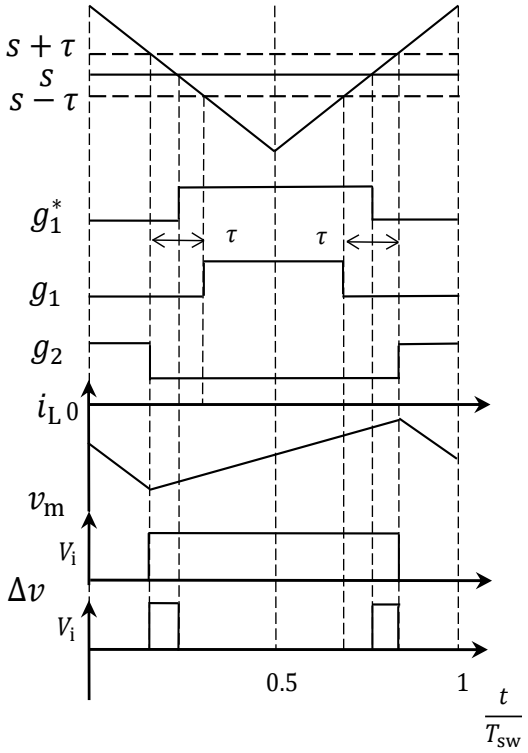


Figure 2.12: Waveforms of the operating mode C_n.

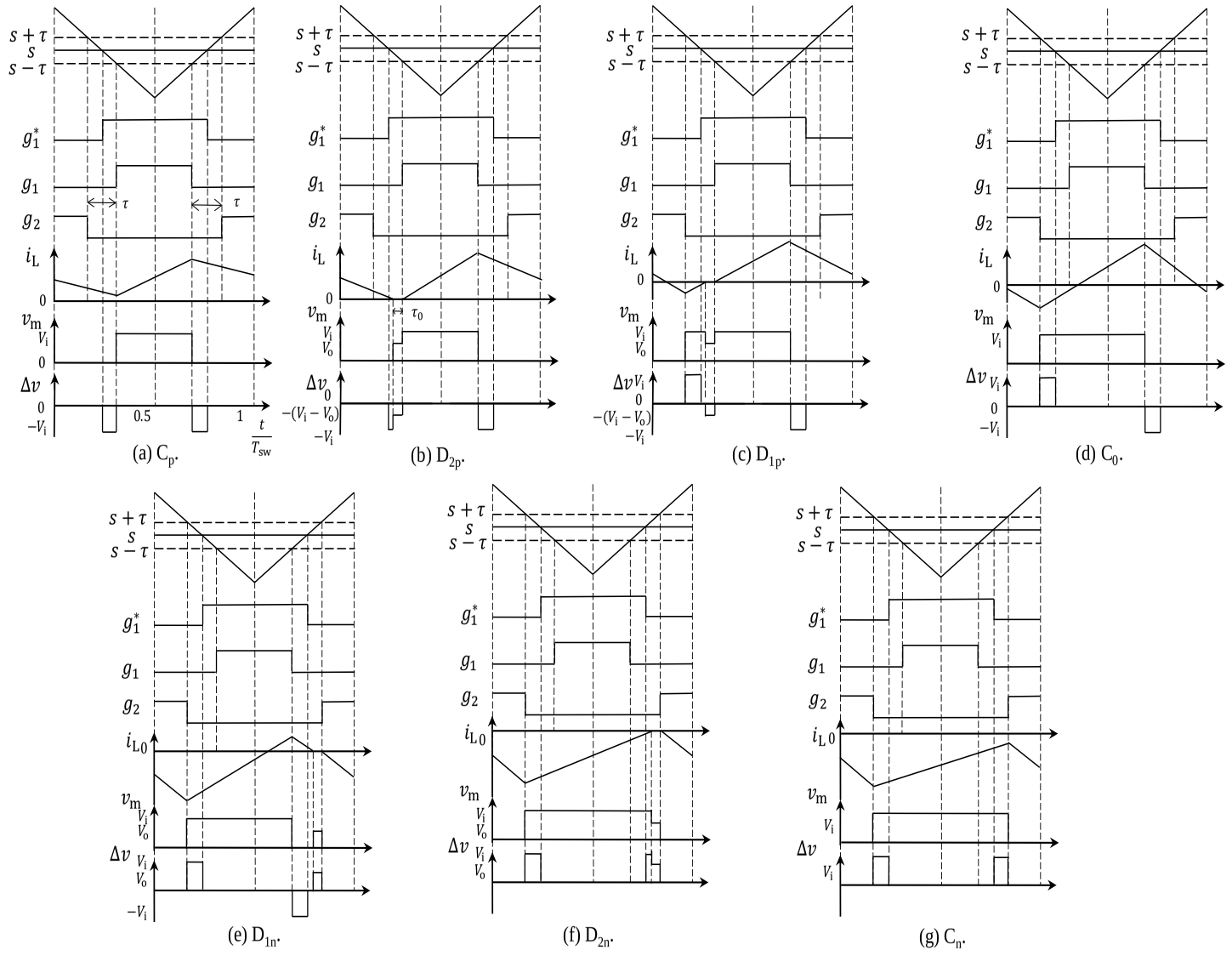


Figure 2.13: Seven operating modes that are identified in [52] when $\check{s} \leq s \leq \hat{s}$. This figure is reproduced from Figure 2 in [52] with notations used in this thesis.

Fig. 2.14 demonstrates the boundary conditions between two adjunct operating modes. Based on these conditions, boundaries can be found mathematically as:

$$\lambda_{\mathrm{o,2p}} = (s - \tau + 0.5)(0.5 - s + \tau). \tag{2.19}$$

$$\lambda_{\mathrm{o,1p}} = (s - \tau + 0.5)(0.5 - s). \tag{2.20}$$

$$\lambda_{\mathrm{o,0p}} = (s - 2\tau + 0.5)(0.5 - s). \tag{2.21}$$

$$\lambda_{\mathrm{o,0n}} = -(s + 0.5)(0.5 - s - 2\tau). \tag{2.22}$$

$$\lambda_{\mathrm{o,1n}} = -(s + 0.5)(0.5 - s - \tau). \tag{2.23}$$

$$\lambda_{\mathrm{o,2n}} = -(s + 0.5 + \tau)(0.5 - s - \tau). \tag{2.24}$$

Operating modes, $\mathrm{D_{2n}}$, $\mathrm{C_n}$, $\mathrm{D_{2p}}$, and $\mathrm{C_p}$, have extended into areas where $s \leq -0.5$ or $s \geq 0.5$. The equations to find M in these operating modes in the study [52] cannot apply to these extended regions because these areas cannot be described by D, as shown in Fig. 2.4.

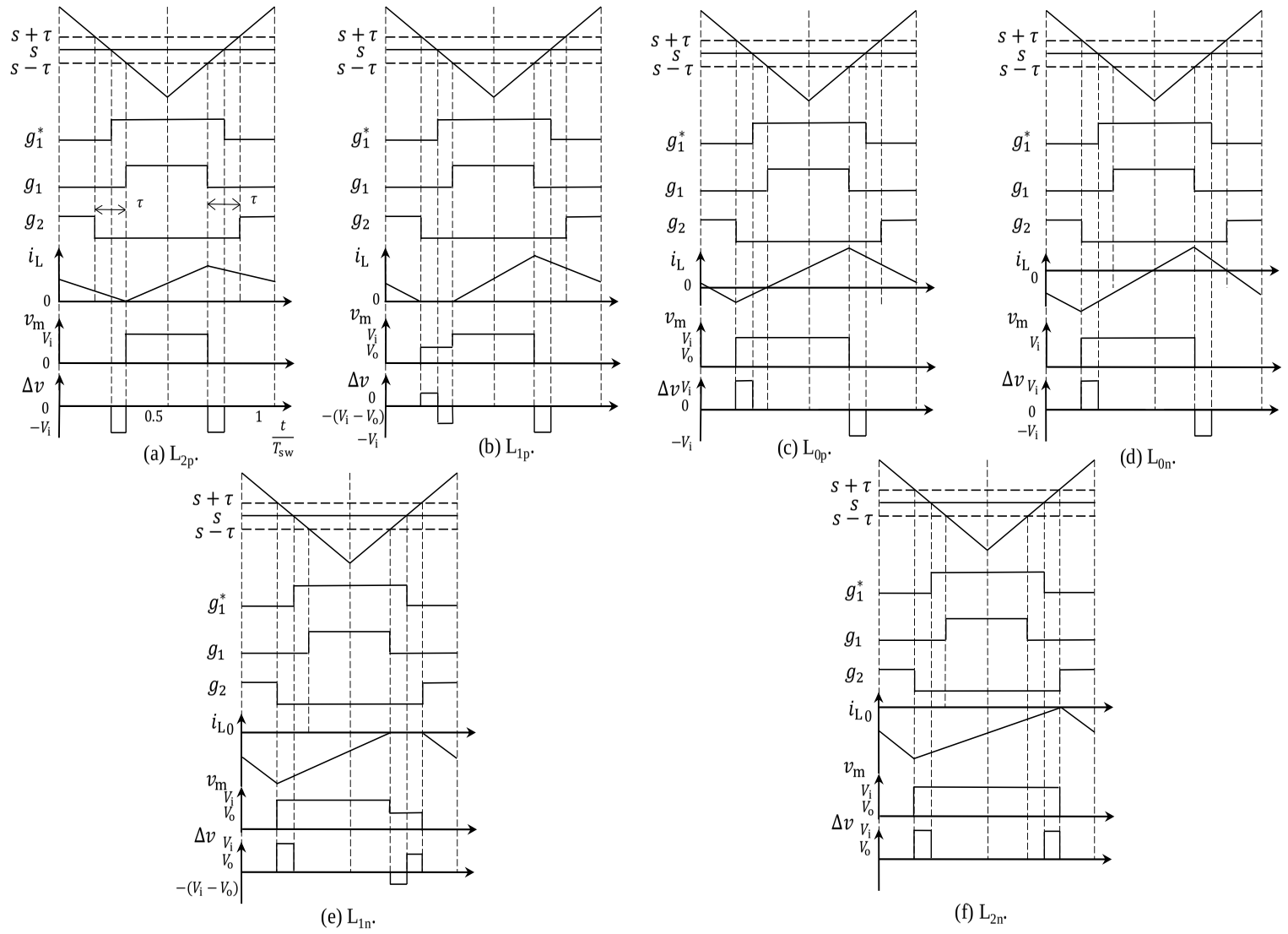


Figure 2.14: Six boundary conditions among the seven operating modes [52] when $\check{s} \leq s \leq \hat{s}$. Boundary equations, (2.19), (2.20), (2.21), (2.22), (2.23) and (2.24) are derived with inductor volt-seconds balance and capacitor amp-seconds balance. This figure is reproduced from Figure 2 in [52] with notations used in this thesis.

2.2.2 Newly identified operating modes

The analysis of the four new operating modes is demonstrated as follows. Fig. 2.19 summarises the waveforms of these operating modes.

2.2.2.1 Operating mode D_{pn}

Fig. 2.15 shows the waveforms of the operating mode D_{pn}. In the rising edge dead-time, as the inductor current $i_L < 0$, the diode D_1 conducts so the middle point voltage equals the input voltage ($v_m = V_i$). When the current i_L is zero, the middle point voltage v_m becomes V_o. Then, the switch Q_1 is on for t_{on}, thus the middle point voltage equals the input voltage ($v_m = V_i$). In the falling edge dead-time, as the current $i_L > 0$, the switch D_2 conducts so the middle point voltage equals zero ($v_m = 0$). When the inductor current is zero ($i_L = 0$), the middle point voltage v_m becomes V_o. Then, the switch Q_2 is on for t_{off}, thus the middle point voltage equals zero ($v_m = 0$). The conversion ratio is:

$$M = \frac{\lambda + 2(s^* + \frac{1}{2} - \tau)^2 - \sigma_1}{\sigma_2}, \tag{2.25}$$

where

$$\sigma_1 = \sqrt{\lambda^2 + 4(s^* + \frac{1}{2} - \tau)^2 (s^* + \tau - \frac{1}{2})^2}, \tag{2.26}$$

$$\sigma_2 = 2\left(\lambda + 2s^*(1 - 2\tau)\right). \tag{2.27}$$

For D_{pn} to occur, the following inequalities need to be satisfied:

$$0 < \tau_{01} < \tau, 0 < \tau_{02} < \tau, \tag{2.28}$$

where τ_{01} is the time period τ_0 in the rising edge dead-time, τ_{02} is the time period τ_0 in the falling edge dead-time:

$$\tau_{01} = \frac{\tau + M(s^* - \frac{1}{2})}{1 - M}, \tag{2.29}$$

$$\tau_{02} = \frac{\tau + (s^* + \frac{1}{2})(M - 1)}{M}. \tag{2.30}$$

The boundary λ_{pn} is determined by (2.28) - (2.30).

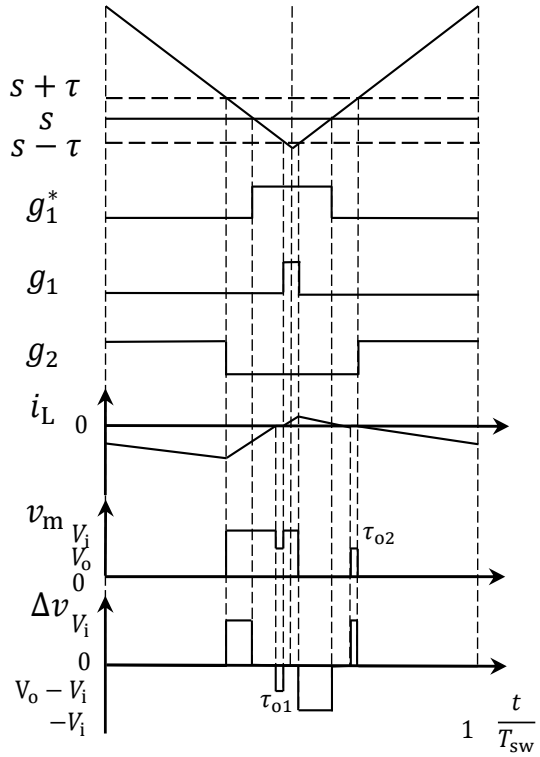


Figure 2.15: Waveforms of the operating mode $\mathrm{D_{pn}}$.

2.2.2.2 Operating mode D_{np}

Fig. 2.16 shows the waveforms of the operating mode D_{np}. The same equations and analysis in D_{pn} also apply to D_{np}, and so it is not repeated here.

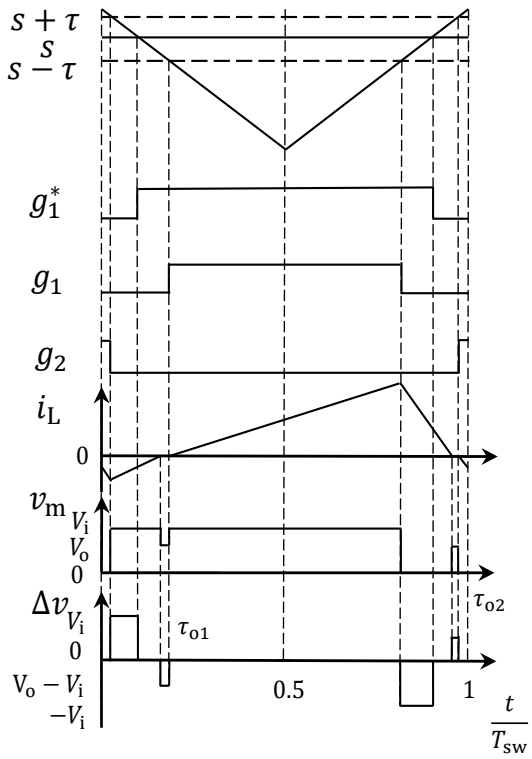


Figure 2.16: Waveforms of the operating mode D_{np}.

2.2.2.3 Operating mode C_{0p}

Fig. 2.17 shows the waveforms of the operating mode C_{0p}. This operating mode occurs when $s \leq (\tau - 0.5)$ and $\lambda \geq 0$. In this operating mode, the gate signal g_1 is always zero ($g_1 \equiv 0$). When the inductor current i_L remains positive over the switching period, it flows through Q_2 when Q_2 is on and freewheels through D_2 when Q_2 is off. Therefore, the middle point voltage is always zero ($v_m \equiv 0$). The switch Q_2 always conducts. A constant current I_o from the current source circulates through L. If at any point during one switching cycle $i_L < 0$, it cannot become positive. Therefore, the expression of M is:

$$M = 0. \tag{2.31}$$

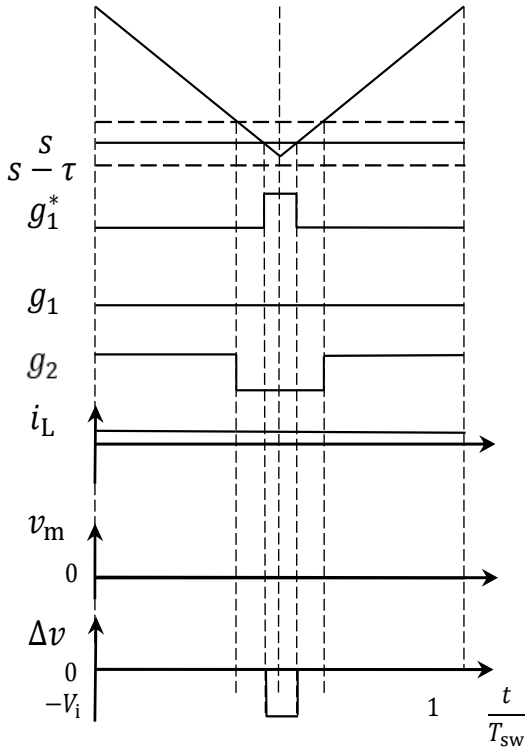


Figure 2.17: Waveforms of the operating mode C_{0p}.

2.2.2.4 Operating mode C_{1n}

Fig. 2.18 shows the waveforms of the operating mode C_{1n}. C_{1n} occurs when $s \geq (0.5 - \tau)$ and $\lambda \leq 0$. In this operating mode, the gate signal g_2 is always zero ($g_2 \equiv 0$). When the inductor current i_L remains negative over the switching period, it flows through Q_1 when Q_1 is on and freewheels through D_1 when Q_1 is off. Therefore, the middle point voltage is always equal to the input voltage ($v_m \equiv V_i$). The switch Q_1 always conducts. A constant current I_o from the current source charges the power supply. If at any point during one switching cycle $i_L > 0$, it cannot become negative. Therefore, the expression of M is:

$$M = 1. \tag{2.32}$$

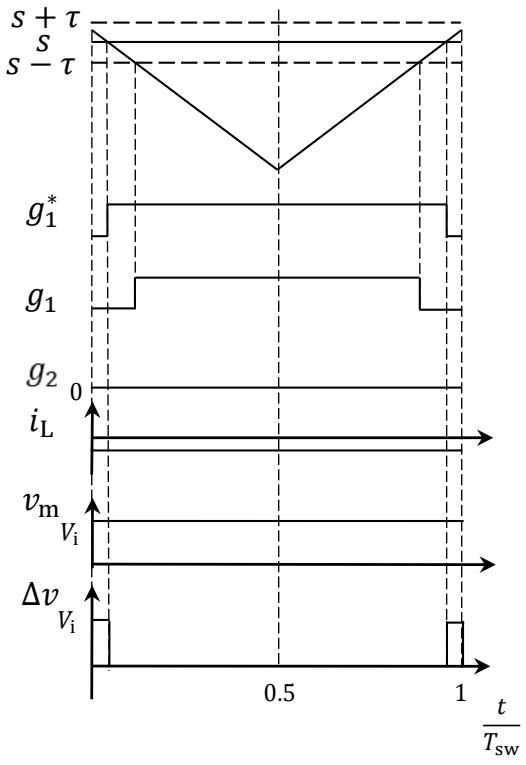
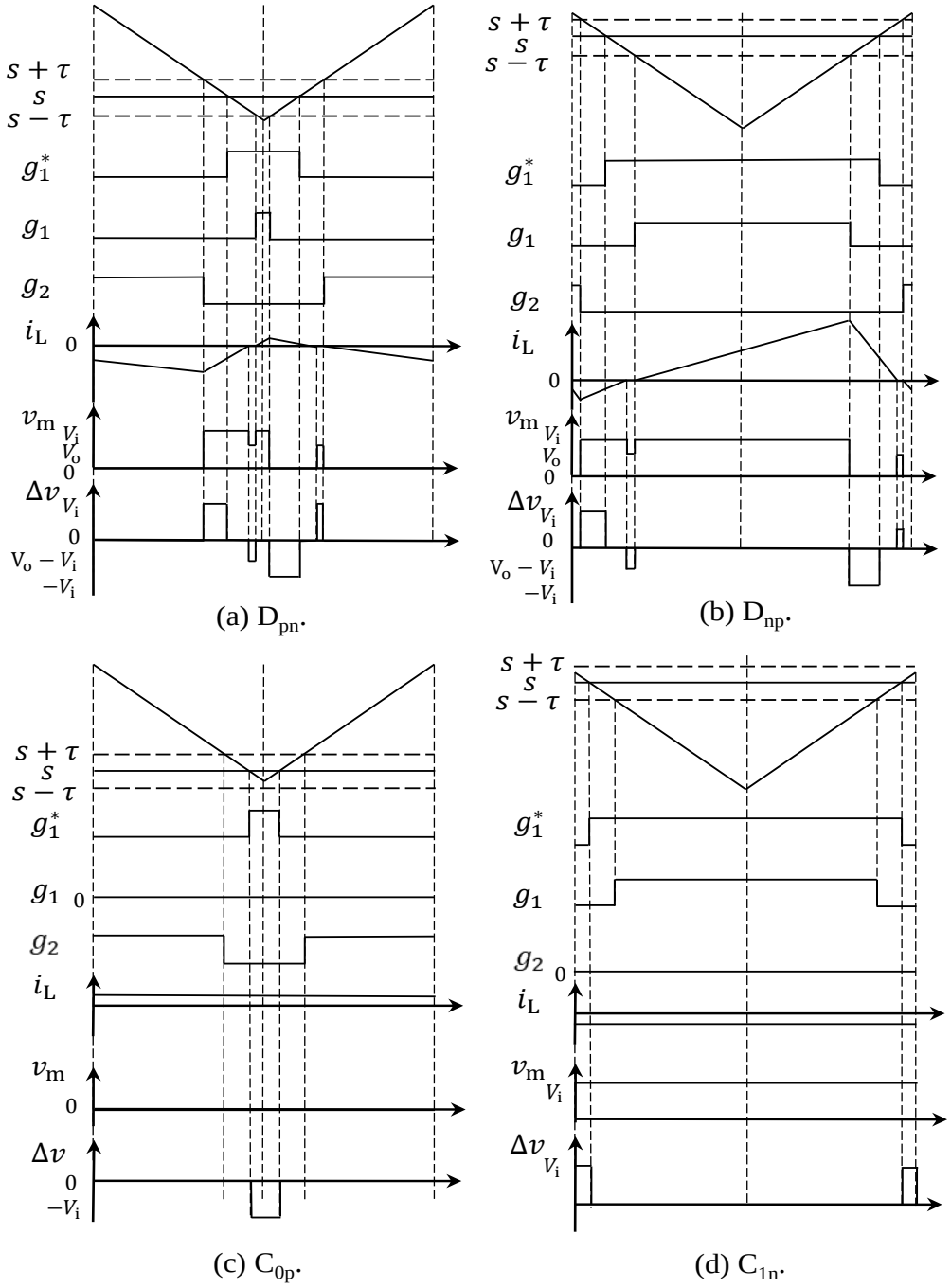


Figure 2.18: Waveforms of the operating mode C_{1n}.

As suggested in Table 2.1, equations of M and equations of boundaries in one operating mode and its counterpart are symmetric about the origin, where $s = 0$ and $\lambda = 0$.



(a) D_{pn}. (b) D_{np}.

(c) C_{0p}. (d) C_{1n}.

Figure 2.19: Waveforms of the four operating modes that are identified in this thesis. In C_{0p} and C_{1n}, one transistor is always off. The current source, that is regarded as a load in Fig. 1.8 (a), drives the flow of i_L.

2.2.3 Summary

Based on the analysis above, Fig. 2.20 shows all the operating modes with their boundaries. Fig. 2.21 shows the conversion ratio M, given s^* and λ of an uncompensated system.

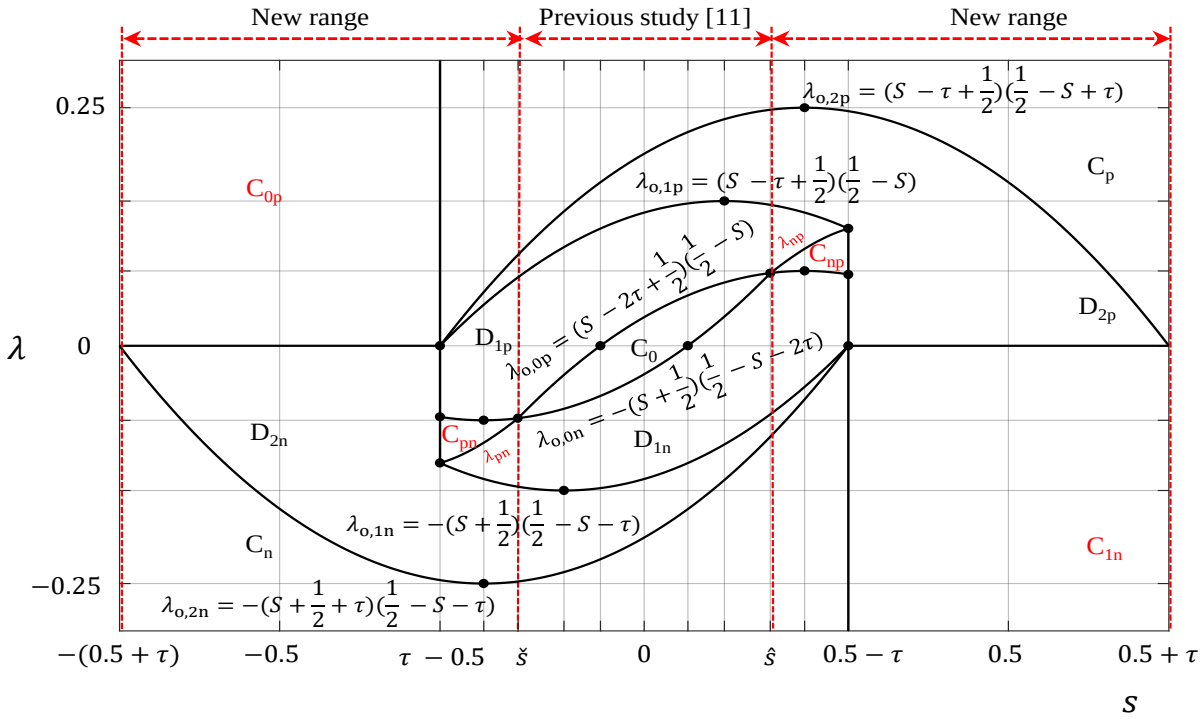


Figure 2.20: Boundaries of all the operating modes in an uncompensated system. Newly-identified operating modes (C_{0p}, C_{1n}, C_{pn} amd C_{np}) and boundaries (λ_{pn} and λ_{np}) are shown in red. $\tau = 0.22$ in this diagram.

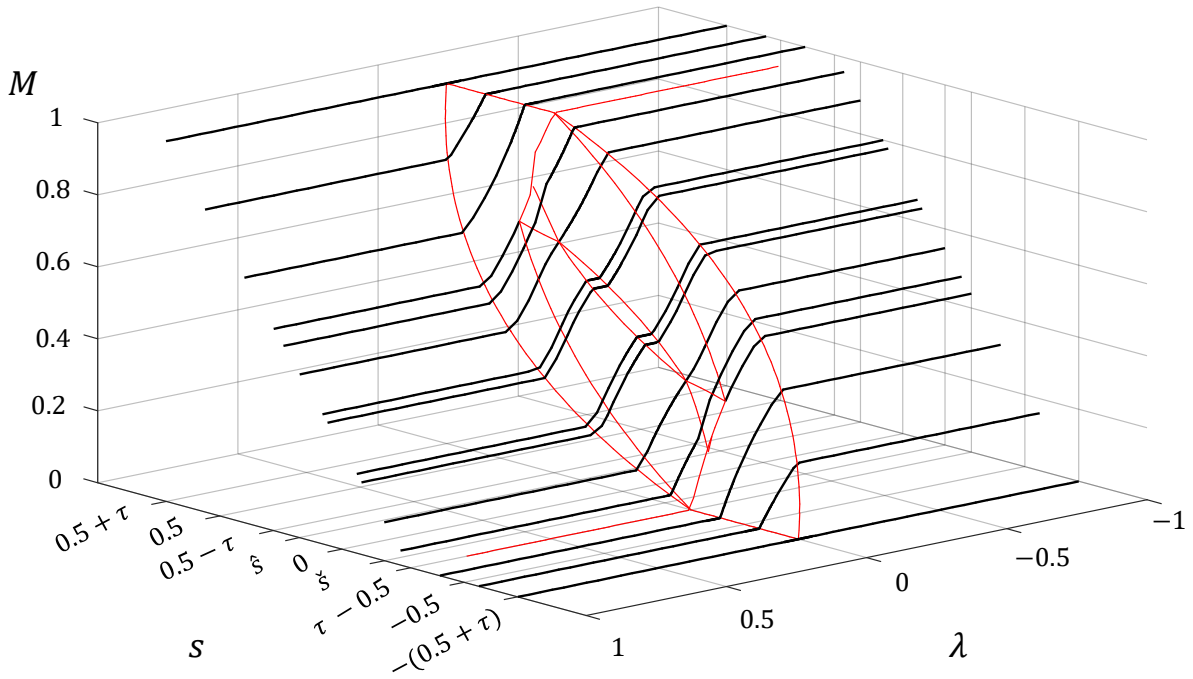


Figure 2.21: Conversion ratio, M, as a function of s and λ, where boundaries that separate different operating modes are indicated by the red lines. Fig. 3 and 4 in [52] demonstrate the same relationship but with $s \in [\hat{s}, \check{s}]$. Derivation of $\lambda_{o,2p}$, $\lambda_{o,1p}$, $\lambda_{o,0p}$, $\lambda_{o,2n}$, $\lambda_{o,1n}$ and $\lambda_{o,0n}$ is in [52]. $\tau = 0.22$ in this diagram.

2.3 Dead-time compensation

The compensating rule proposed here produces perfect correction whenever possible. If not, imperfect correction is achieved. Based on the result of the compensation and the compensating rule applied, the $s^* - \lambda$ plane can be divided into seven regions:

α : increase s^* by τ, i.e., $s = s^* + \tau$;
β : increase s^* by τ_a, i.e., $s = s^* + \tau_\mathrm{a}$;
ψ : keep the same s^*, i.e., $s = s^*$;
ϕ : keep the same s^*, i.e., $s = s^*$;
α' : decrease s^* by τ, i.e., $s = s^* - \tau$;
β' : decrease s^* by τ_a, i.e., $s = s^* - \tau_\mathrm{a}$;
ψ' : keep the same s^*, i.e., $s = s^*$.

These regions are symmetric about the origin, where $s^* = 0, \lambda = 0$. The counterparts of regions α, β, ψ and ϕ are denoted with a prime, as shown in Table 2.2. The equations to find the discontinuous time period during the dead-time τ_o, the amount of extra s that needs to be added for compensation τ_a, and a group of inequalities to describe boundaries in a counterpart, can be found by substituting s^* with $-s^*$, λ with $-\lambda$ in the corresponding inequalities and equations of this region.

Table 2.2: Compensation regions and their counterparts in a compensated system.

compensation region	counterpart
α	α'
β	β'
ψ	ψ'

Fig. 2.22 shows these regions. The region β includes regions β_1, β_2, β_3 and β_4. They are separated as they have different operating modes, as shown in Fig. 2.36. Therefore, they use different equations to calculate t_a.

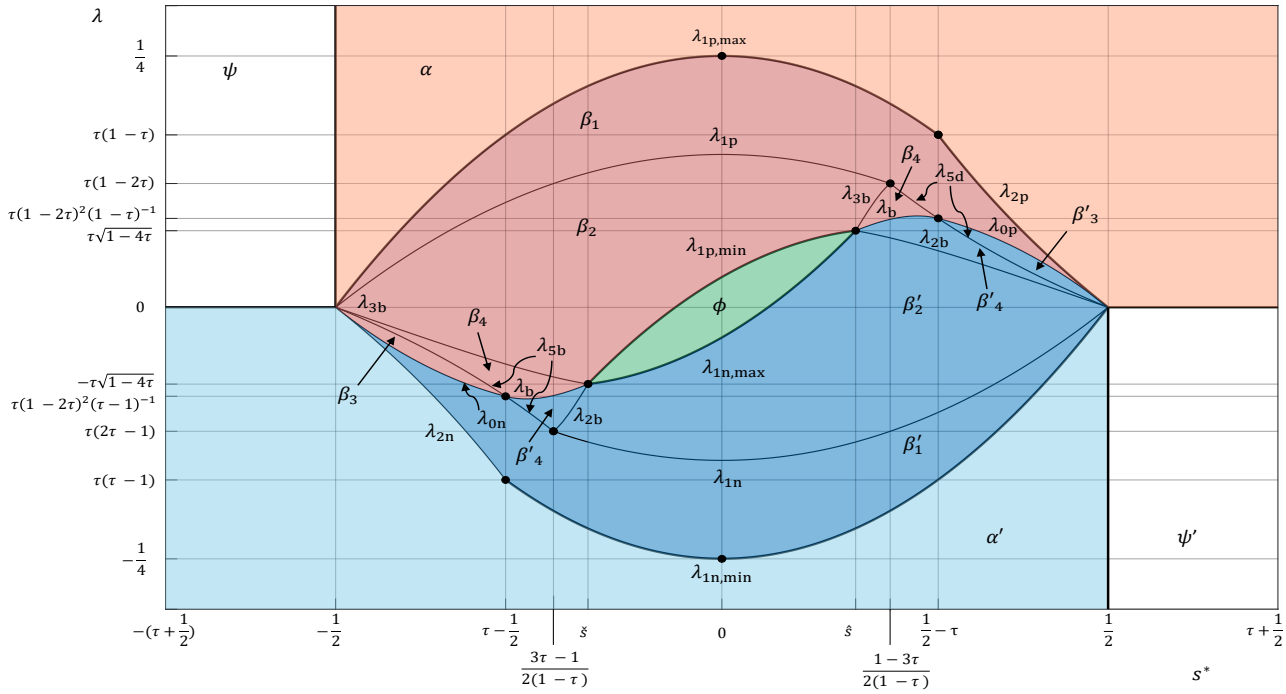


Figure 2.22: Boundaries of α, β, ψ, ϕ, α', β' and ψ' in a compensated system. Compensating results are shown by the shades of colour: Light, i.e., light red/blue/white: perfect correction; Dark, i.e., dark red/blue/green: imperfect correction. Regions with red colour: increase s^* for compensation; Blue colour: decrease s^* for compensation. Cases lying on the curves λ_{0n}, λ_b and λ_{0p} are compensated intrinsically with imperfect correction, i.e., $s = s^*$. Both the boundaries among various compensating rules and the results of compensation have rotational symmetry around the point (0, 0). In this diagram, $\tau = 0.22$.

2.3.1 Perfect and imperfect correction

2.3.1.1 Region α (perfect correction)

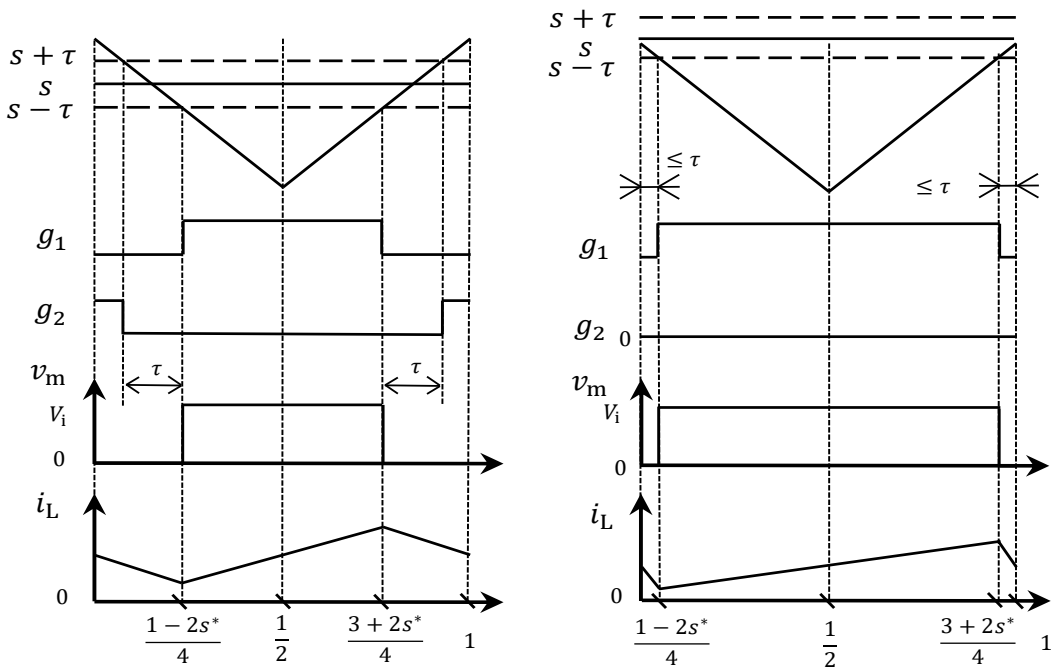
In this region, $s = s^* + \tau$. Fig. 2.23 shows the waveforms. It occurs when one of the inequalities holds:

$$\begin{cases} \lambda_{1\mathrm{p,max}} \leq \lambda, \\ -\frac{1}{2} \leq s^* < \frac{1}{2} - \tau. \end{cases} \tag{2.33}$$

$$\begin{cases} \lambda_{2\mathrm{p}} \leq \lambda, \\ \frac{1}{2} - \tau \leq s^* < \frac{1}{2}. \end{cases} \tag{2.34}$$

$$\begin{cases} 0 \leq \lambda, \\ \frac{1}{2} \leq s^* \leq \left(\frac{1}{2} + \tau\right). \end{cases} \tag{2.35}$$

During the dead-time, as the inductor current $i_\mathrm{L} > 0$, the diode D_2 conducts, thus the middle point voltage equals zero ($v_\mathrm{m} = 0$). Therefore, the middle point voltage always equals the the middle point voltage in an ideal system ($v_\mathrm{m} \equiv v_\mathrm{m}^*$), i.e., $\Delta v \equiv 0$. Fig. 2.23 (b) demonstrates a scenario where $s^* \geq \left(\frac{1}{2} - \tau\right)$, i.e., $s = s^* + \tau \geq \frac{1}{2}$, $s + \tau > \frac{1}{2}$, $s - \tau = s^* < \frac{1}{2}$. The gate signal g_2 equals zero over the cycle, so the switch Q_2 is turned off all the time. In this scenario, the time period when both switches are off is less than 2τ.



(a) α, $s = s^* + \tau$.

(b) α when $s^* \geq \frac{1}{2} - \tau$.

Figure 2.23: Waveforms of the region α.

2.3.1.2 Region β (imperfect correction)

In this region, $s = s^* + \tau_{\mathrm{a}}$. In the β region, the occurrence of discontinuous conduction mode results in a voltage loss, i.e., $M < D$, and so s^* should be increased to compensate for this loss.

The reason why β cannot be corrected perfectly is as follows. Increasing s^* to a certain point where at the beginning of the rising-edge dead-time, the inducotr current is negative ($i_{\mathrm{L}} \leq 0$), or the current i_{L} is slightly greater than 0, still results in DCM. If the current $i_{\mathrm{L}} > 0$ always holds in the rising edge dead-time, after increasing s^*, the current i_{L} is always positive over one cycle, which implies that λ is beyond its boundary and instead becomes part of region α. Fig. 2.36 (a) (b) (c) (d) shows the waveforms, which are discussed in detail in Section 2.3.2.

2.3.1.3 Region ψ (perfect correction)

In this region, $s = s^*$. It occurs when

$$\begin{cases} 0 \leq \lambda, \\ -\left(\frac{1}{2} + \tau\right) \leq s^* < -\frac{1}{2}. \end{cases} \tag{2.36}$$

The same description of $\mathrm{C_{0p}}$ in Section 2.2 applies here. Fig. 2.19 (c) shows the waveforms. Region ψ achieves perfect correction intrinsically.

2.3.1.4 Region ϕ (imperfect correction)

In this region, $s = s^*$. Fig. 2.24 shows the waveforms. It occurs when

$$\begin{cases} \lambda_{1\mathrm{n,max}} \leq \lambda \leq \lambda_{1\mathrm{p,min}}, \\ \check{s} \leq s^* \leq \hat{s}. \end{cases} \tag{2.37}$$

As dead-time does not cause average voltage error in this operating mode, $s = s^*$. During the rising edge dead-time, as $i_\mathrm{L} < 0$, the diode D_1 conducts, thus the middle point voltage equals to the input voltage ($v_\mathrm{m} = V_\mathrm{i}$); During the falling edge dead-time, as $i_\mathrm{L} > 0$, the diode D_2 conducts, thus the middle point voltage equals to zero ($v_\mathrm{m} = 0$). Compared with the middle point voltage from an ideal system v_m^*, the middle point voltage v_m is advanced by $\frac{\tau}{2}$ in time. This time shift can be eliminated by using asymmetric PWM modulation.

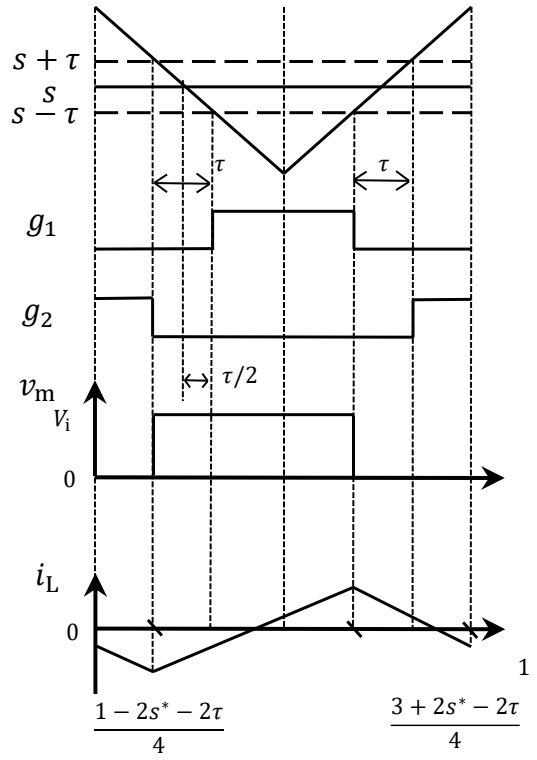


Figure 2.24: Waveforms of the region ϕ.

2.3.1.5 Region α' (perfect correction)

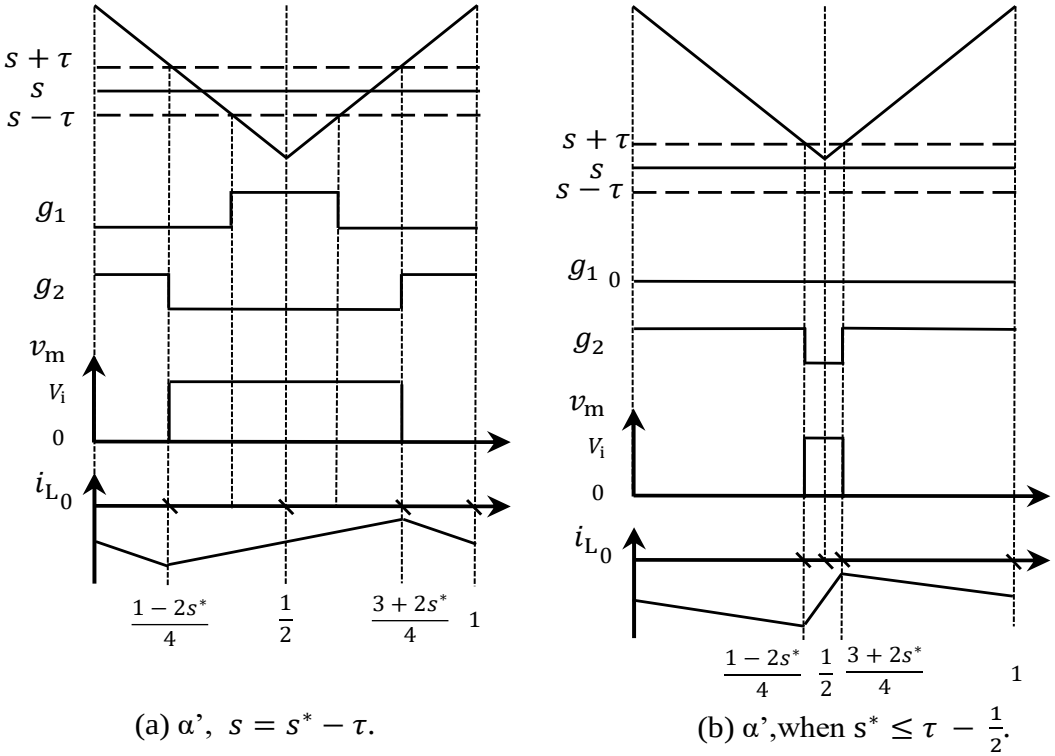
In this region, $s = s^* - \tau$. It occurs when one of the inequalities holds:

$$\begin{cases} \lambda \leq \lambda_{1\mathrm{n,min}}, \\ \tau - \frac{1}{2} \leq s^* < \frac{1}{2}. \end{cases} \tag{2.38}$$

$$\begin{cases} \lambda \leq \lambda_{2\mathrm{n}}, \\ -\frac{1}{2} \leq s^* < \tau - \frac{1}{2}. \end{cases} \tag{2.39}$$

$$\begin{cases} \lambda \leq 0, \\ -\left(\frac{1}{2} + \tau\right) \leq s^* \leq -\frac{1}{2}. \end{cases} \tag{2.40}$$

During the dead-time, as the inductor current $i_\mathrm{L} < 0$, the diode D_1 conducts, thus the middle point voltage equals the input voltage ($v_\mathrm{m} = V_\mathrm{i}$). Therefore, the middle point voltage equals the middle point voltage of an ideal system ($v_\mathrm{m} \equiv v_\mathrm{m}^*$), i.e., $\Delta v \equiv 0$. Fig. 2.25 (b) demonstrates a scenario where $s^* \leq \left(\tau - \frac{1}{2}\right)$, i.e., $s = s^* - \tau \leq -\frac{1}{2}$, $s + \tau > -\frac{1}{2}$, $s - \tau < -\frac{1}{2}$. The gate signal equals zero ($g_1 = 0$) over the cycle, so the switch Q_1 is turned off all the time. In this scenario, the time period when both switches are off is less than 2τ.



(a) α', $s = s^* - \tau$. (b) α',when $s^* \leq \tau - \frac{1}{2}$.

Figure 2.25: Waveforms of the region α'.

2.3.1.6 Region β' (imperfect correction)

In this region, $s = s^* - \tau_a$. In the β' region, the occurrence of discontinuous conduction mode results in a voltage gain, i.e., $M > M^*$, and so s^* should be decreased to compensate for this gain.

The reason why β' cannot be corrected perfectly is as follows. Decreasing s^* to a certain point where at the beginning of the falling edge dead-time, the inductor current is positive ($i_L \geq 0$), or the current i_L is slightly less than 0, still results in discontinuous conduction mode. If $i_L < 0$ always holds in the falling edge dead-time, after decreasing s^*, the current i_L is always negative over one cycle, which implies that λ is beyond its boundary and instead becomes part of region α'. Fig. 2.36 (e) (f) (g) (h) shows the waveforms, which are discussed in detail in Section 2.3.2.

2.3.1.7 Region ψ' (perfect correction)

In this region, $s = s^*$. It occurs when

$$\begin{cases} \lambda \leq 0, \\ \frac{1}{2} \leq s^* < \left(\frac{1}{2} + \tau\right). \end{cases} \tag{2.41}$$

The same description of C_{1n} in Section 2.2 applies here. Fig. 2.19 (d) shows the waveforms. The region ψ' achieves perfect correction intrinsically.

2.3.1.8 Summary

In summary, different results appear after the compensating rule is applied:

1. perfect correction: α, ψ, α and ψ';

2. imperfect correction: β (β_1, β_2, β_3 and β_4), ϕ, β' (β'_1, β'_2, β'_3 and β'_4) and ϕ'.

When $s^* = -\frac{1}{2}$ and $\lambda = 0$, the extra s that needs to be added to s^* for compensation, τ_a, can be any number between $-\tau$ and τ. This is because $s - \tau = s^* + \tau_a - \tau = -\frac{1}{2} + \tau_a - \tau < -\frac{1}{2}$, which suggests that the switch Q_1 is off all the time. As the output current is zero, the middle point voltage v_m is connected to ground either through Q_2 (when it is on) or the inductor and capacitor (when Q_2

is off), i.e., $v_{\mathrm{m}} \equiv 0$. The same applies for the point where $s^* = \frac{1}{2}$ and $\lambda = 0$. Fig. 2.3.1.8 summarises and compares the waveforms of regions.

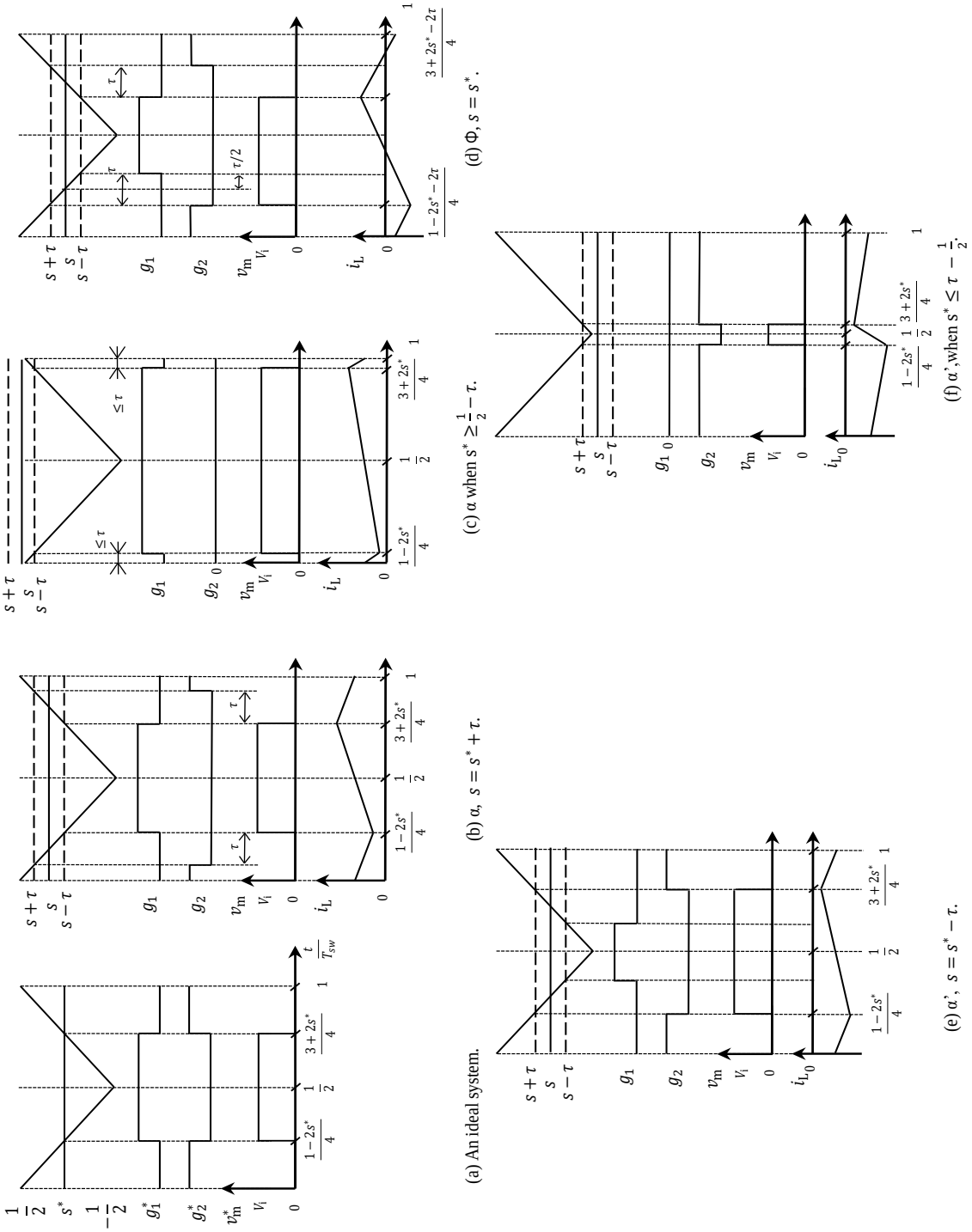


Figure 2.26: Waveforms of gate signals and middle point voltage (a) in an ideal system; (b)(c)(d)(e)(f) in a compensated system. Perfect correction is achieved in (b), (c), (e) and (f); Imperfect correction is achieved in (d).

2.3.2 Sub-regions of β and β'

As aforementioned, the instantaneous voltage error Δv cannot always be zero in β. Therefore, achieving imperfect correction becomes the goal. Four operating modes can occur after the compensation. Fig. 2.27 plots τ_a for λ and s^*.

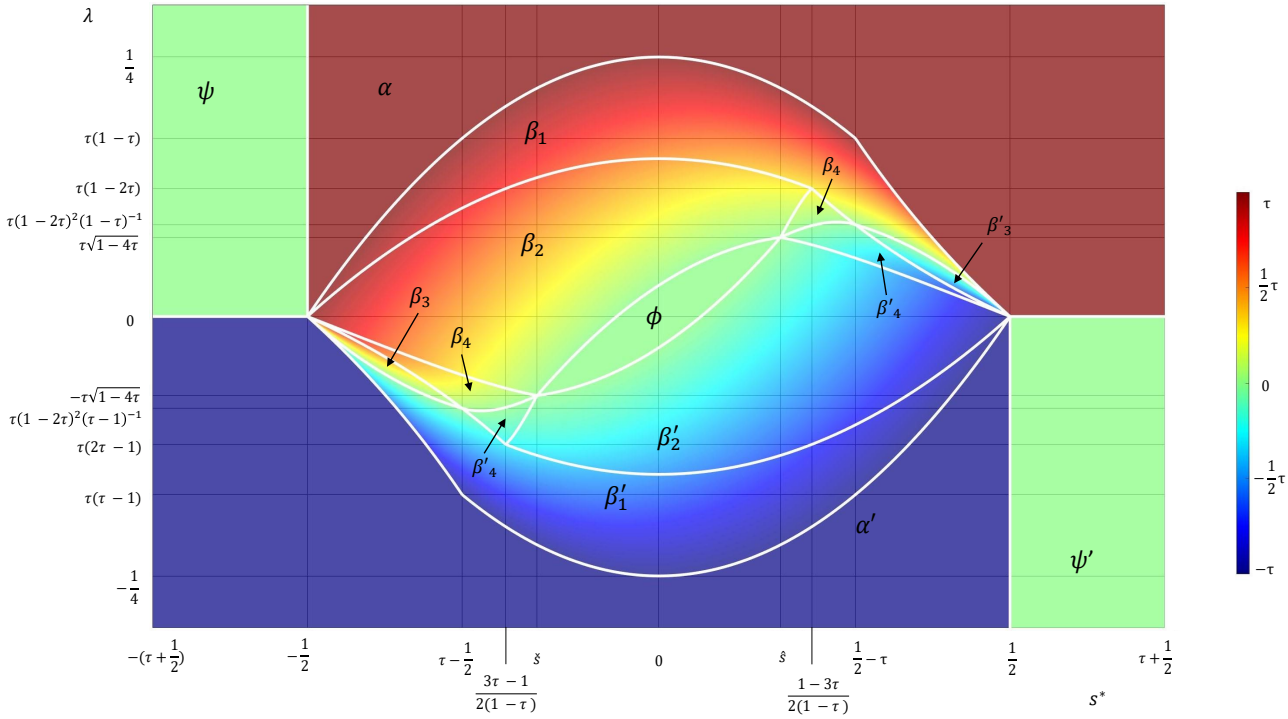


Figure 2.27: τ_a, the amount that should be added to s^* to compensate voltage error, as a function of λ and s^*. In α, $s = s^* + \tau$. In ϕ and ψ, $s = s^*$. In β, τ_a varies between 0 and τ. Boundaries among different regions, as shown in Fig. 2.22, are marked in white curves. In this diagram, $\tau = 0.22$.

2.3.2.1 Region β_1

Fig. 2.28 shows the waveforms of this region. This situation occurs when any of the following three inequality sets is satisfied:

$$\begin{cases} \lambda_{1p} \le \lambda < \lambda_{1p,max}, \\ -\frac{1}{2} \le s^* < \frac{1-3\tau}{2(1-\tau)}. \end{cases} \tag{2.42}$$

$$\begin{cases} \lambda_{5d} \le \lambda < \lambda_{1p,max}, \\ \frac{1-3\tau}{2(1-\tau)} \le s^* < \frac{1}{2} - \tau. \end{cases} \tag{2.43}$$

$$\begin{cases} \lambda_{0\mathrm{p}} \leq \lambda < \lambda_{2\mathrm{p}}, \\ \frac{1}{2} - \tau \leq s^* \leq \frac{1}{2}. \end{cases} \tag{2.44}$$

where

$$\lambda_{1\mathrm{p,max}}(s^*) = \left(\frac{1}{2} + s^*\right)\left(\frac{1}{2} - s^*\right), \tag{2.45}$$

$$\lambda_{1\mathrm{p}}(s^*) = (1-\tau)^2\left(\frac{1}{2} + s^*\right)\left(\frac{1}{2} - s^*\right), \tag{2.46}$$

$$\lambda_{5\mathrm{d}}(s^*) = \frac{(1-2\tau)^2(1-2s^*)}{2s^*+1}, \tag{2.47}$$

$$\lambda_{2\mathrm{p}}(s^*) = \frac{(1-\tau)^2(1-2s^*)}{2s^*+1}, \tag{2.48}$$

$$\lambda_{0\mathrm{p}}(s^*) = \frac{(1-2s^*)(1+2s^*-2\tau)^2}{8s^*+4}. \tag{2.49}$$

The time periods τ_0 and τ_a can be expressed as:

$$\tau_0 = 1 - \sqrt{\frac{4\lambda}{(1+2s^*)(1-2s^*)}}, \tag{2.50}$$

$$\tau_\mathrm{a} = \tau - \tau_0(s^* + \frac{1}{2}). \tag{2.51}$$

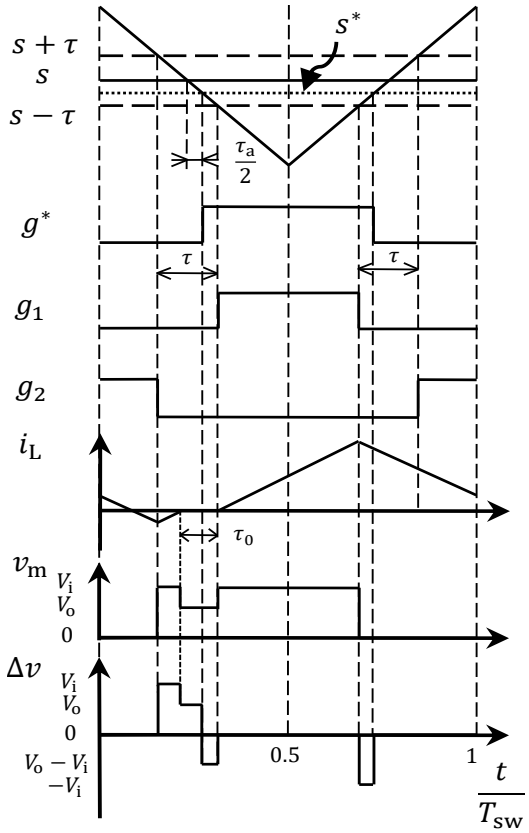


Figure 2.28: Waveforms of the region β_1.

2.3.2.2 Region β_2

Fig. 2.29 shows the waveforms of this region. This situation occurs when any of the following three inequality sets is satisfied:

$$\begin{cases} \lambda_{3b} \leq \lambda < \lambda_{1p}, \\ -\frac{1}{2} \leq s^* < \check{s}. \end{cases} \tag{2.52}$$

$$\begin{cases} \lambda_{1p,min} \leq \lambda < \lambda_{1p}, \\ \check{s} \leq s^* < \hat{s}. \end{cases} \tag{2.53}$$

$$\begin{cases} \lambda_{3b} \leq \lambda < \lambda_{1p}, \\ \hat{s} \leq s^* < \frac{1-3\tau}{2(1-\tau)}. \end{cases} \tag{2.54}$$

where

$$\lambda_{3b}(s^*) = \frac{2s^*+1}{2s^*-1}\left(1-\frac{2\tau}{1-2s^*}\right)\left(1-2\tau-\frac{2\tau}{1-2s^*}\right), \tag{2.55}$$

$$\lambda_{1p,min}(s^*) = \left(\frac{1}{2}-s^*\right)\left(s^*+\frac{1}{2}-2\tau\right), \tag{2.56}$$

The time periods τ_0 and τ_a can be expressed as:

$$\tau_0 = \frac{2s^*-2\tau+2\delta-1}{2s^*-3}, \tag{2.57}$$

$$\tau_a = \left(\frac{1}{2}-s^*\right)\tau_0, \tag{2.58}$$

where

$$\delta = \sqrt{\frac{\lambda(3-2s^*)}{2s^*-1}+(1-\tau)^2}. \tag{2.59}$$

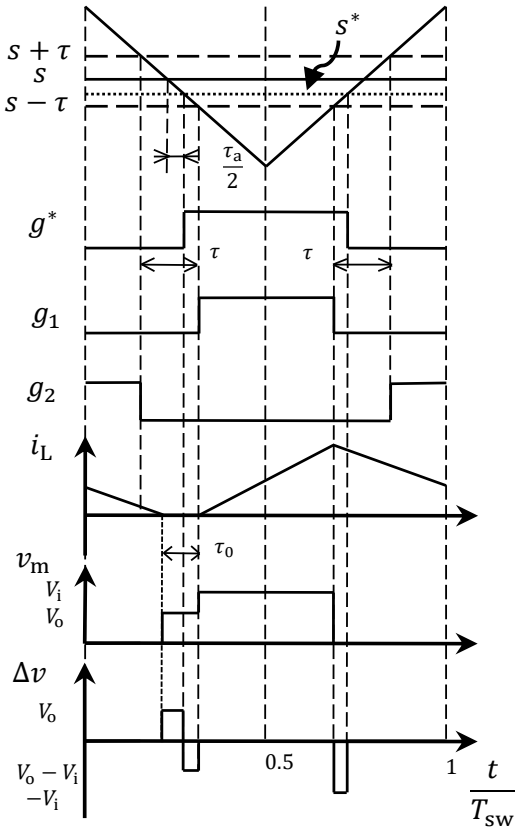


Figure 2.29: Waveforms of the region β_2.

2.3.2.3 Region β_3

Fig. 2.30 shows the waveforms of this region. This situation occurs when the following inequality set is satisfied:

$$\begin{cases} \lambda_{0\mathrm{n}} \leq \lambda < \lambda_{5\mathrm{b}}, \\ -\frac{1}{2} \leq s^* < \tau - \frac{1}{2}. \end{cases} \tag{2.60}$$

where

$$\lambda_{5\mathrm{b}}(s^*) = \frac{(2s^*+1)(1-2\tau)^2}{2s^*-1}, \tag{2.61}$$

$$\lambda_{0\mathrm{n}}(s^*) = \frac{(2s^*+1)(1-2s^*-2\tau)^2}{8s^*-4}. \tag{2.62}$$

The time periods τ_0 and τ_a can be expressed as:

$$\tau_0 = 1 - \sqrt{\frac{-4\lambda}{(1+2s^*)(1-2s^*)}}, \tag{2.63}$$

$$\tau_\mathrm{a} = \left(\frac{1}{2} - s^*\right)\tau_0 - \tau. \tag{2.64}$$

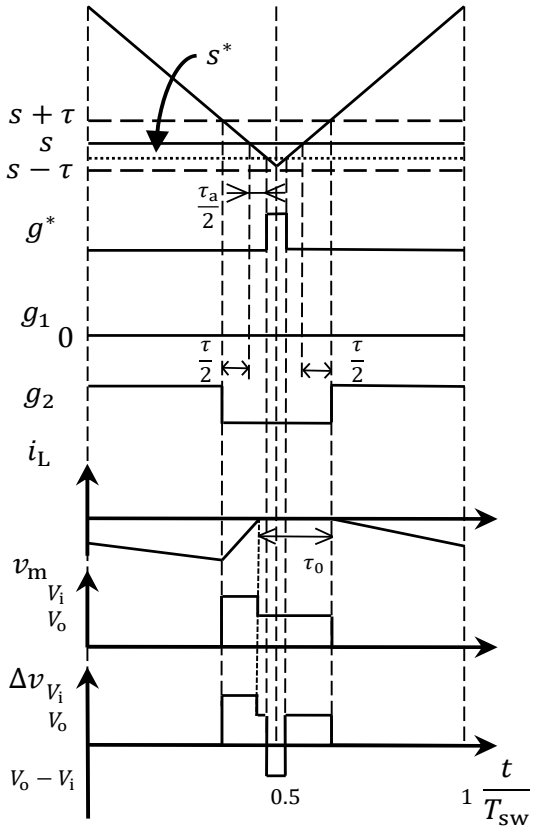


Figure 2.30: Waveforms of the region β_3.

2.3.2.4 Region β_4

Fig. 2.31 shows the waveforms of this region. This situation occurs when any of the following four inequality sets is satisfied:

$$\begin{cases} \lambda_{5\mathrm{b}} \leq \lambda < \lambda_{3\mathrm{b}}, \\ -\frac{1}{2} \leq s^* < \tau - \frac{1}{2}. \end{cases} \tag{2.65}$$

$$\begin{cases} \lambda_{\mathrm{b}} \leq \lambda < \lambda_{3\mathrm{b}}, \\ \tau - \frac{1}{2} \leq s^* < \check{s}. \end{cases} \tag{2.66}$$

$$\begin{cases} \lambda_{\mathrm{b}} \leq \lambda < \lambda_{3\mathrm{b}}, \\ \hat{s} \leq s^* < \frac{1-3\tau}{2(1-\tau)}. \end{cases} \tag{2.67}$$

$$\begin{cases} \lambda_{\mathrm{b}} \leq \lambda < \lambda_{5\mathrm{d}}, \\ \frac{1-3\tau}{2(1-\tau)} \leq s^* < \frac{1}{2} - \tau. \end{cases} \tag{2.68}$$

where

$$\lambda_{\mathrm{b}}(s^*) = \frac{-4\tau s^* \left(-4s^{*2} + 1 - 2\tau\right)}{\left(2s^* + 1\right)\left(2s^* - 1\right)}, \tag{2.69}$$

The time period when i_{L} remians zero during the rising edge dead-time, τ_{01}, and during the falling edge dead-time, τ_{02}, as well as τ_{a} can be expressed as:

$$\tau_{01} = \frac{\left(2s^* + 1\right)^2 (2\tau - 1) + 4s^* + 2 - 4\tau - 4\delta}{8s^*}, \tag{2.70}$$

$$\tau_{02} = -\frac{\left(2s^* - 1\right)^2 \tau_{01}}{\left(2s^* + 1\right)^2} + 1 - \frac{2}{2s^* + 1} + \frac{4\tau}{\left(2s^* + 1\right)^2}, \tag{2.71}$$

$$\tau_{\mathrm{a}} = \tau_{01} - \left(s^* + \frac{1}{2}\right)\left(\tau_{01} + \tau_{02}\right), \tag{2.72}$$

where

$$\delta = \sqrt{\left(s^* + \frac{1}{2}\right)^4 (2\tau - 1)^2 - \frac{4\lambda s^* \left(s^* + \frac{1}{2}\right)^3}{1 - 2s^*}}. \tag{2.73}$$

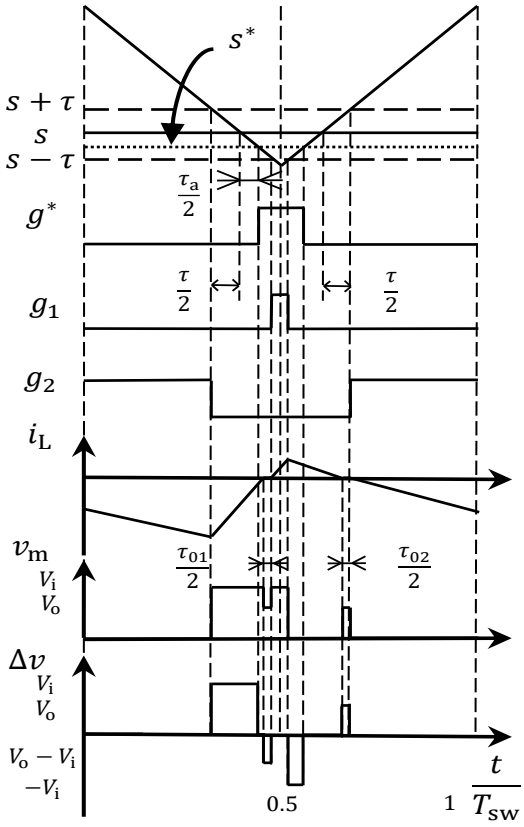


Figure 2.31: Waveforms of the region β_4.

2.3.2.5 Region β_1'

Fig. 2.32 shows the waveforms of this region. This situation occurs when any of the following three inequality sets is satisfied:

$$\begin{cases} \lambda_{1n,\min} \leq \lambda < \lambda_{1n}, \\ \frac{3\tau-1}{2(1-\tau)} \leq s^* < \frac{1}{2}. \end{cases} \tag{2.74}$$

$$\begin{cases} \lambda_{1n,\min} \leq \lambda < \lambda_{5b}, \\ \frac{3\tau-1}{2(1-\tau)} \leq s^* < \tau - \frac{1}{2}. \end{cases} \tag{2.75}$$

$$\begin{cases} \lambda_{2n} \leq \lambda < \lambda_{0n}, \\ \tau - \frac{1}{2} \leq s^* \leq -\frac{1}{2}. \end{cases} \tag{2.76}$$

where

$$\lambda_{1n,\min}(s^*) = \left(s^* + \frac{1}{2}\right)\left(s^* - \frac{1}{2}\right), \tag{2.77}$$

$$\lambda_{1n}(s^*) = (1-\tau)^2\left(\frac{1}{2} + s^*\right)\left(s^* - \frac{1}{2}\right), \tag{2.78}$$

$$\lambda_{5b}(s^*) = \frac{(1-2\tau)^2(2s^*+1)}{2s^*-1}, \tag{2.79}$$

$$\lambda_{2n}(S^*) = \frac{(1-\tau)^2(2s^*+1)}{2s^*-1}, \tag{2.80}$$

$$\lambda_{0n}(s^*) = \frac{(2s^*+1)(1-2s^*-2\tau)^2}{8s^*-4}. \tag{2.81}$$

The time periods τ_0 and τ_a can be expressed as:

$$\tau_0 = 1 - \sqrt{\frac{-4\lambda}{(1+2s^*)(1-2s^*)}}, \tag{2.82}$$

$$\tau_a = \tau - \tau_0\left(\frac{1}{2} - s^*\right). \tag{2.83}$$

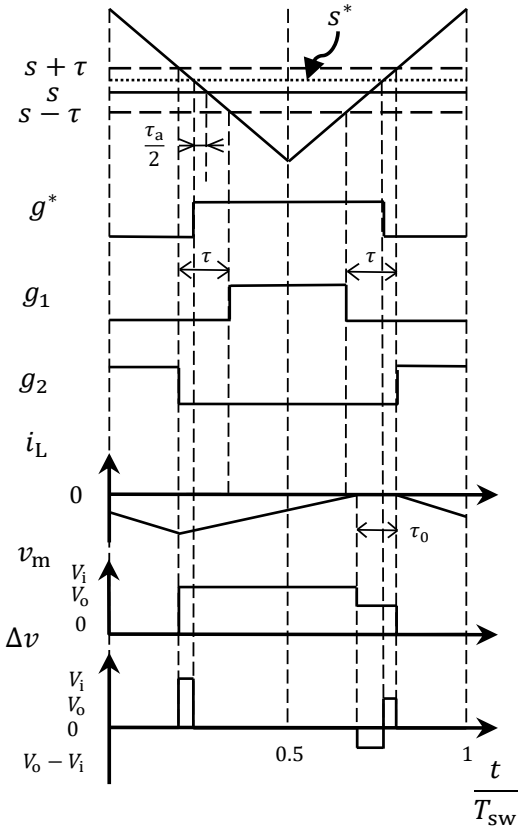


Figure 2.32: Waveforms of the region β_1'.

2.3.2.6 Region β_2'

Fig. 2.33 shows the waveforms of this region. This situation occurs when any of the following three inequality sets is satisfied:

$$\begin{cases} \lambda_{1n} \leq \lambda < \lambda_{2b}, \\ \hat{s} \leq s^* < \frac{1}{2}. \end{cases} \tag{2.84}$$

$$\begin{cases} \lambda_{1n} \leq \lambda < \lambda_{1n,\,max}, \\ \check{s} \leq s^* < \hat{s}. \end{cases} \tag{2.85}$$

$$\begin{cases} \lambda_{1n} \leq \lambda < \lambda_{2b}, \\ \frac{3\tau-1}{2(1-\tau)} \leq s^* < \check{s}. \end{cases} \tag{2.86}$$

where

$$\lambda_{2b}(s^*) = \frac{1-2s^*}{2s^*+1}\left(1-\frac{2\tau}{2s^*+1}\right)\left(1-2\tau-\frac{2\tau}{2s^*+1}\right), \tag{2.87}$$

$$\lambda_{1n,max}(s^*) = \left(s^*+\frac{1}{2}\right)\left(s^*-\frac{1}{2}+2\tau\right), \tag{2.88}$$

The time periods τ_0 and τ_a can be expressed as:

$$\tau_0 = \frac{2s^*+2\tau-2\delta+1}{2s^*+3}, \tag{2.89}$$

$$\tau_a = \left(\frac{1}{2}+s^*\right)\tau_0, \tag{2.90}$$

where

$$\delta = \sqrt{\frac{\lambda(3+2s^*)}{2s^*+1}+(1-\tau)^2}. \tag{2.91}$$

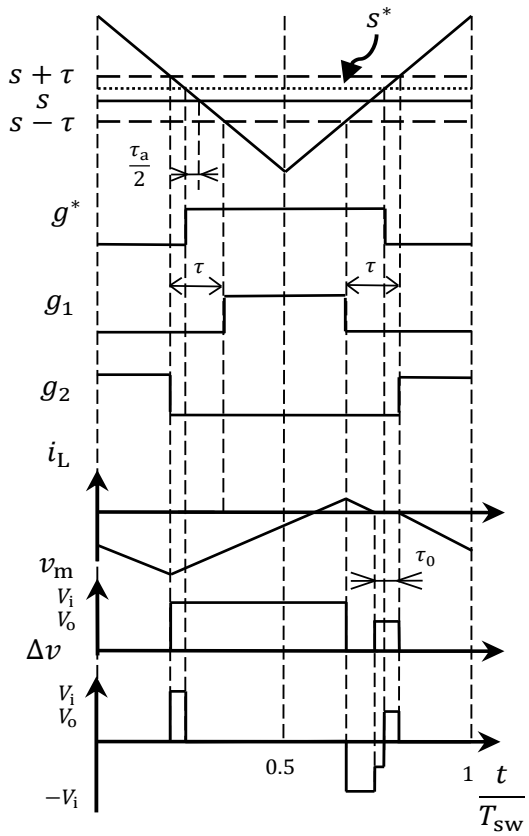


Figure 2.33: Waveforms of the region β_2'.

2.3.2.7 Region β_3'

Fig. 2.34 shows the waveforms of this region. This situation occurs when the following inequality set is satisfied:

$$\begin{cases} \lambda_{5\mathrm{d}} \leq \lambda < \lambda_{0\mathrm{p}}, \\ \frac{1}{2} - \tau \leq s^* < \frac{1}{2}. \end{cases} \tag{2.92}$$

where

$$\lambda_{5\mathrm{d}}(s^*) = \frac{(1-2s^*)(1-2\tau)^2}{2s^*+1}, \tag{2.93}$$

$$\lambda_{0\mathrm{p}}(s^*) = \frac{(1-2s^*)(1+2s^*-2\tau)^2}{8s^*+4}. \tag{2.94}$$

The time periods τ_0 and τ_a can be expressed as:

$$\tau_0 = 1 - \sqrt{\frac{4\lambda}{(1+2s^*)(1-2s^*)}}, \tag{2.95}$$

$$\tau_\mathrm{a} = \left(\frac{1}{2} + s^*\right)\tau_0 - \tau. \tag{2.96}$$

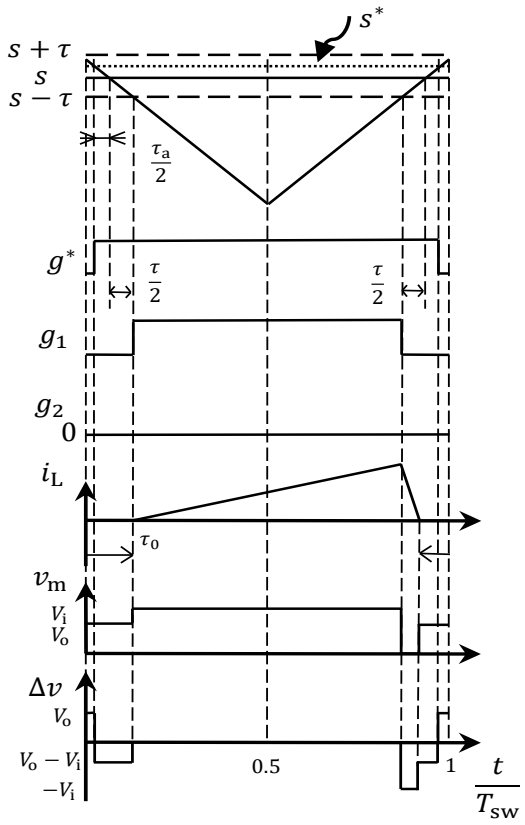


Figure 2.34: Waveforms of the region β_3'.

2.3.2.8 Region β_4'

Fig. 2.35 shows the waveforms of this region. This situation occurs when any of the following four inequality sets is satisfied:

$$\begin{cases} \lambda_{2\mathrm{b}} \leq \lambda < \lambda_{5\mathrm{d}}, \\ \frac{1}{2} - \tau \leq s^* < \frac{1}{2}. \end{cases} \tag{2.97}$$

$$\begin{cases} \lambda_{2\mathrm{b}} \leq \lambda < \lambda_{\mathrm{b}}, \\ \hat{s} \leq s^* < \frac{1}{2} - \tau. \end{cases} \tag{2.98}$$

$$\begin{cases} \lambda_{2\mathrm{b}} \leq \lambda < \lambda_{\mathrm{b}}, \\ \frac{3\tau-1}{2(1-\tau)} \leq s^* < \check{s}. \end{cases} \tag{2.99}$$

$$\begin{cases} \lambda_{5\mathrm{b}} \leq \lambda < \lambda_{\mathrm{b}}, \\ \tau - \frac{1}{2} \leq s^* < \frac{3\tau-1}{2(1-\tau)}. \end{cases} \tag{2.100}$$

The time period when i_{L} remians zero during the rising edge dead-time, τ_{01}, and during the falling edge dead-time, τ_{02}, as well as τ_{a} are expressed as:

$$\tau_{01} = \frac{\left(1-2s^*\right)^2(2\tau-1) - 4s^* + 2 - 4\tau - 4\delta}{-8s^*}, \tag{2.101}$$

$$\tau_{02} = -\frac{\left(2s^*+1\right)^2\tau_{01}}{\left(1-2s^*\right)^2} + 1 - \frac{2}{1-2s^*} + \frac{4\tau}{\left(1-2s^*\right)^2}, \tag{2.102}$$

$$\tau_{\mathrm{a}} = \tau_{01} - \left(\frac{1}{2} - s^*\right)\left(\tau_{01} + \tau_{02}\right), \tag{2.103}$$

where

$$\delta = \sqrt{\left(\frac{1}{2} - s^*\right)^4 (2\tau-1)^2 - \frac{4\lambda s^* \left(\frac{1}{2} - s^*\right)^3}{1+2s^*}}. \tag{2.104}$$

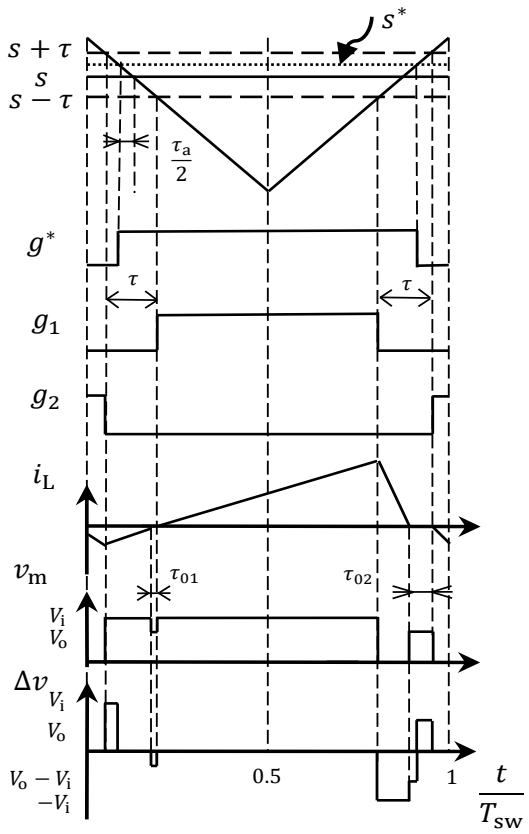


Figure 2.35: Waveforms of the region β_4'.

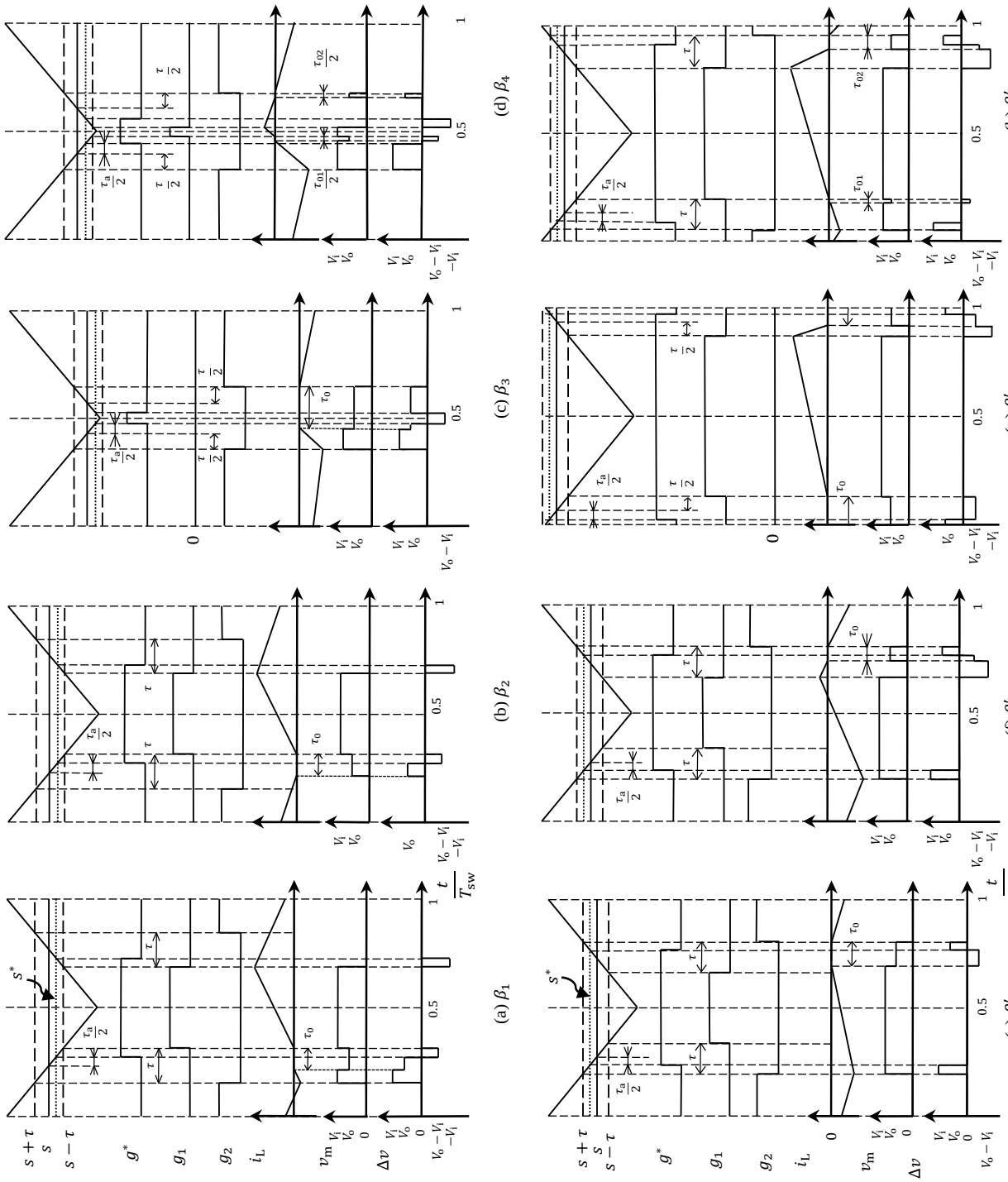


Figure 2.36: (a)-(d) Four sub-regions of β with imperfect correction result. (e)-(h) Four sub-regions of β' with imperfect correction result.

2.3.3 Compensation algorithm

Given I_0 and s^*, the compensation algorithm in Fig. 2.37 generates s that produces $V_\mathrm{o} \equiv V_\mathrm{o}^*$. The inequalities to determine whether a point (s^*, λ) belong to $\alpha, \beta, \psi, \phi$ or α', β', ψ' are:

$$\begin{cases} 0 \le \lambda, \\ -\left(\frac{1}{2} + \tau\right) \le s^* < -\frac{1}{2}. \end{cases} \tag{2.105}$$

$$\begin{cases} \lambda_{0\mathrm{n}} \le \lambda, \\ -\frac{1}{2} \le s^* < \tau - \frac{1}{2}. \end{cases} \tag{2.106}$$

$$\begin{cases} \lambda_\mathrm{b} \le \lambda, \\ \tau - \frac{1}{2} \le s^* < \check{s}. \end{cases} \tag{2.107}$$

$$\begin{cases} \lambda_{1\mathrm{n,max}} \le \lambda, \\ \check{s} \le s^* < \hat{s}. \end{cases} \tag{2.108}$$

$$\begin{cases} \lambda_\mathrm{b} \le \lambda, \\ \hat{s} \le s^* < \frac{1}{2} - \tau. \end{cases} \tag{2.109}$$

$$\begin{cases} \lambda_{0\mathrm{p}} \le \lambda, \\ \frac{1}{2} - \tau \le s^* < \frac{1}{2}. \end{cases} \tag{2.110}$$

$$\begin{cases} 0 \le \lambda, \\ \frac{1}{2} \le s^* \le \tau + \frac{1}{2}. \end{cases} \tag{2.111}$$

If any of inequalities holds, the point belongs to $\alpha, \beta, \psi, \phi$; otherwise, it belongs to α', β', ψ'.

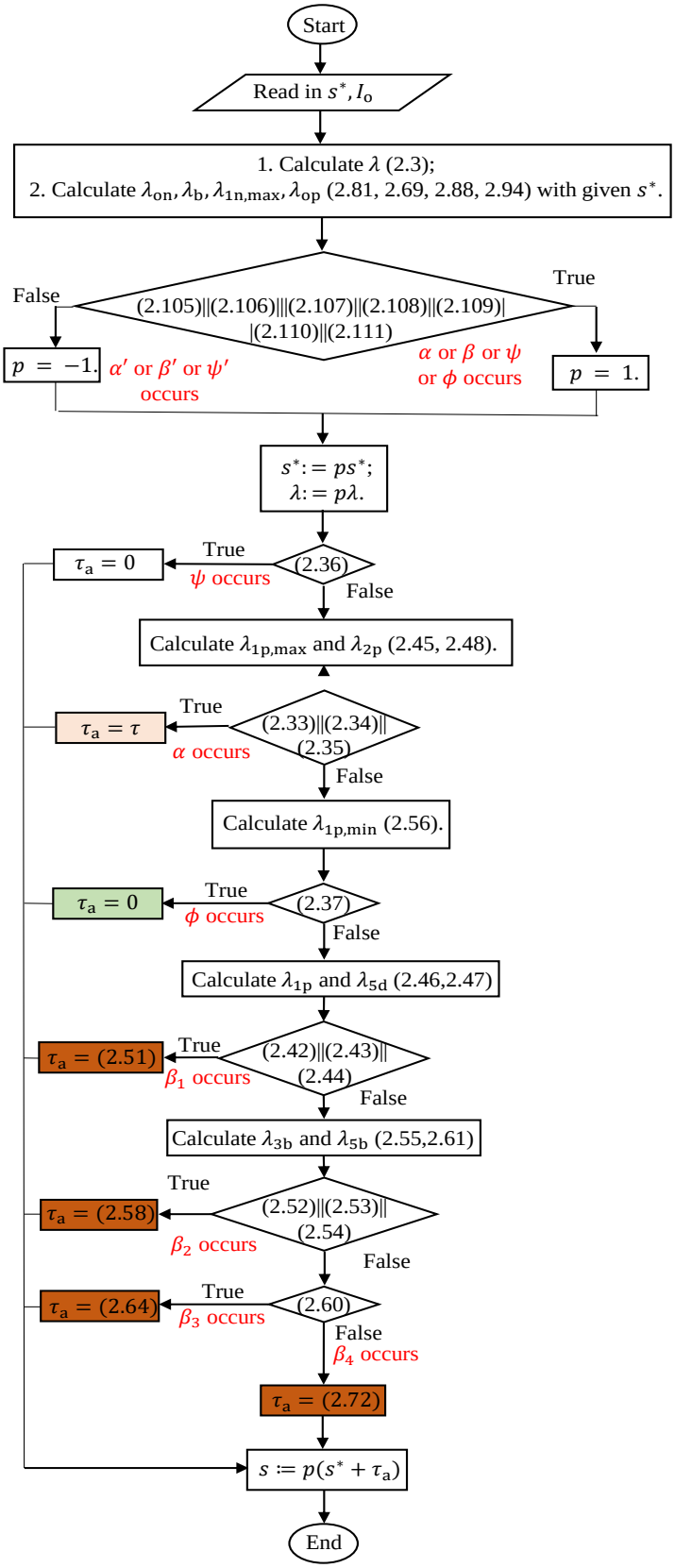


Figure 2.37: An algorithm that produces the compensating rule and evaluates the results of the compensation. Colours correspond to the regions in Fig. 2.22. Equations used to find the boundaries are marked in brackets. || represents the Boolean OR operator.

2.4 Comparison with conventional compensation

Fig. 2.38 shows the variation of regions' areas with the change of τ.

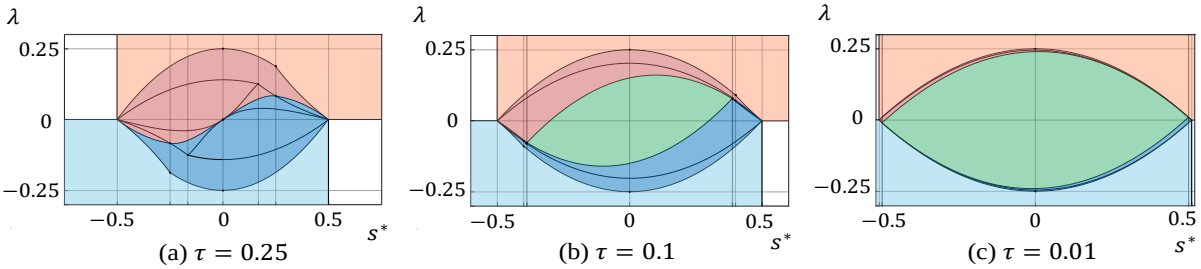


Figure 2.38: Variation of areas of regions when τ changes. With the decrease of τ, areas of β and β' shrink; the area of ϕ increases.

In the extreme case when $\tau = 0.25$, region ϕ disappears; regions β and β' become dominant around the zero-crossings. When τ becomes small, for example $\tau = 0.01$, areas of β and β' are negligible compared with that of ϕ. In such a situation, this compensation method is in agreement with the three-level ACM, i.e., near the zero-crossing where $-\lambda_{\text{th}} \leq \lambda \leq \lambda_{\text{th}}$, $\tau_{\text{a}} = 0$; in the positive half where $\lambda \geq \lambda_{\text{th}}$, $\tau_{\text{a}} = \tau$; in the negative half where $\lambda \leq -\lambda_{\text{th}}$, $\tau_{\text{a}} = -\tau$.

The threshold current, I_{th}, is the ripple current for a given D of an ideal system. The normalised threshold current is denoted as λ_{th}. Because the dead-time distortion has not been completely understood, no agreement on the equation of I_{th} is shown in the literature. In study [50], $I_{\text{th}} = \frac{V_{\text{i}} T_{\text{sw}}}{4L}$. In study [51], $I_{\text{th}} = \frac{D(1-D)V_{\text{i}}}{2f_{\text{sw}}L}$, and the author states it is difficult to select a suitable I_{th}. Fig. 2.38 (c) clearly shows that, the boundary I_{th}, which determines which compensation rule to use in conventional ACMs, is the curve between the region α and ϕ: $\lambda_{\text{1p,max}}$ (2.45) and $\lambda_{\text{1p,min}}$ (2.56), as shown in Fig. 2.22. Because τ is small, these two curves overlap, such that:

$$\lambda_{\text{th}} = \lambda_{\text{o,1p}} = \lambda_{\text{o,0p}} = (\frac{1}{2} + s)(\frac{1}{2} - s). \tag{2.112}$$

Assume $s = D - \frac{1}{2}$, then the expression of λ_{th} and I_{th} becomes:

$$\begin{cases} \lambda_{\text{th}} = D(1-D), \\ I_{\text{th}} = \frac{\lambda_{\text{th}} V_{\text{i}} T_{\text{sw}}}{2L} = \frac{D(1-D)V_{\text{i}}}{2f_{\text{sw}}L}, \end{cases} \tag{2.113}$$

which agrees with the equation of I_{th} in the study [51].

Based on the relationship between s and D as shown in Fig. 2.3, the amount of s that is added to s^* for compensation, τ_{a}, in the three conventional compensation methods is expressed in the notations used in this thesis. Fig. 2.39, 2.41 and 2.40 compare the τ_{a} of the proposed compensation method in this thesis, three-level ACM, linear ACM, and two-level ACM, with $\tau = 0.25$, $\tau = 0.1$ and $\tau = 0.01$ respectively.

When τ is large, for example, $\tau = 0.25$, this proposed compensation method is in agreement with the linear ACM, as shown in Fig. 2.39. When τ is small, for example, $\tau = 0.01$, this proposed compensation method is in agreement with the 3-level ACM, as shown in Fig. 2.41.

2.5 Conclusions

Based on the results and discussions presented in this chapter, the key conclusions are the following:

1. The duty cycle D cannot describe all the possible cases when the dead-time distortion is considered. The input reference signal, s, is used for the analysis in this thesis. A complete analysis of the dead-time distortion is presented, with two assumptions: (i) all the components are ideal; (ii) small ripple approximation is made such that V_{o} can be considered constant over one cycle. Four operating modes are first identified. The full map with $s \in [-(0.5+\tau), (0.5+\tau)]$ is demonstrated. The equations to find the conversion ratio, M, are provided.

2. Based on the analysis of the dead-time distortion, an accurate model of the compensating voltage near the current zero-crossings is proposed, and the compensation results are demonstrated in detail. The results reveal that the proposed compensation rule can remove the average voltage error for all s^* and I_{o} so that $V_{\mathrm{o}} \equiv V_{\mathrm{o}}^*$, i.e., $\langle \Delta v \rangle \equiv 0$. However, the removal of the instantaneous voltage error cannot be guaranteed, i.e., $\Delta v \not\equiv 0$ under some conditions. When $\lambda \geq 0.25$ or $\lambda \leq -0.25$, for all s^*, dead-time distortion can be completely eliminated such that the compensated system behaves exactly

the same as that of an ideal system, i.e., $\Delta v \equiv 0$; When $\lambda \in [-0.25, 0.25]$, it cannot guarantee that the instantaneous voltage error is always zero ($\Delta v \not\equiv 0$).

3. Using the compensation method of Fig. 2.37 ensures $V_{\mathrm{o}} \equiv V_{\mathrm{o}}^{*}$. However, the rules are complex. In practice, if τ is very large, the linear ACM is a reasonable approximation. If τ is very small, the three-level ACM is a reasonable approximation. The equation to find I_{th}, which is uncertain in the literature, is presented.

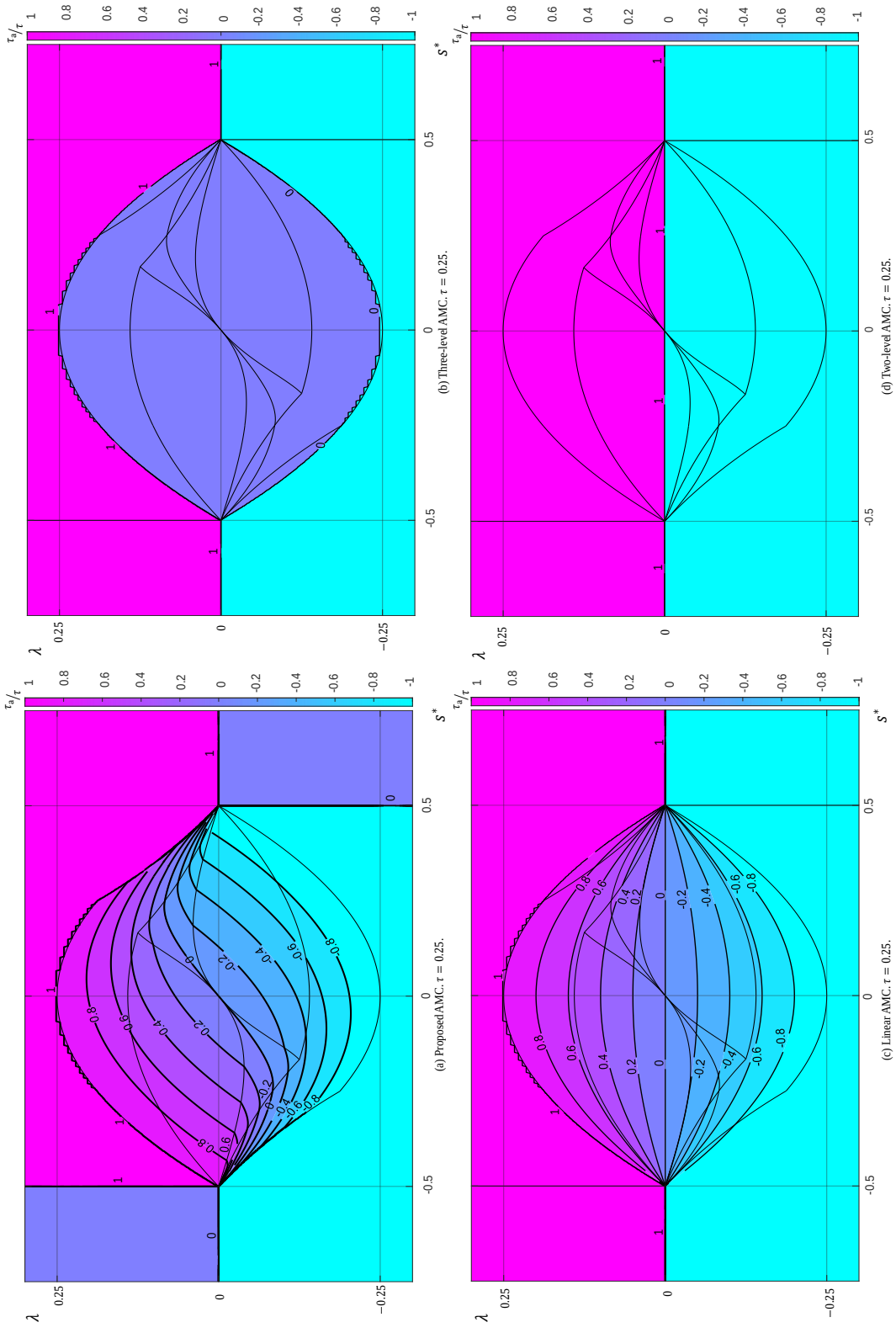


Figure 2.39: Comparison of the proposed compensation method, three-level, linear ACM and two-level ACM with $\tau = 0.25$.

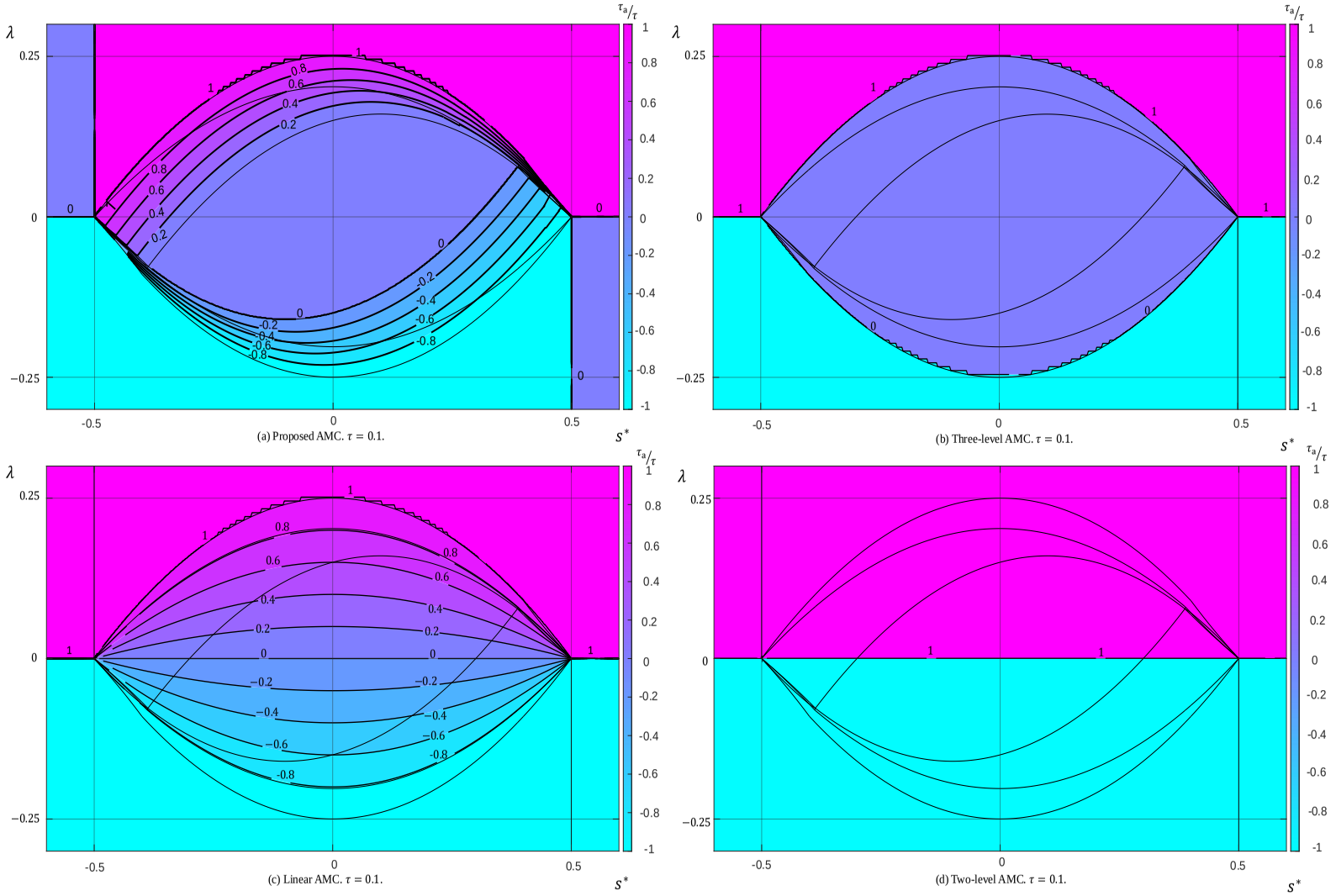


Figure 2.40: Comparison of the proposed compensation method, three-level, linear ACM and two-level ACM with $\tau = 0.1$.

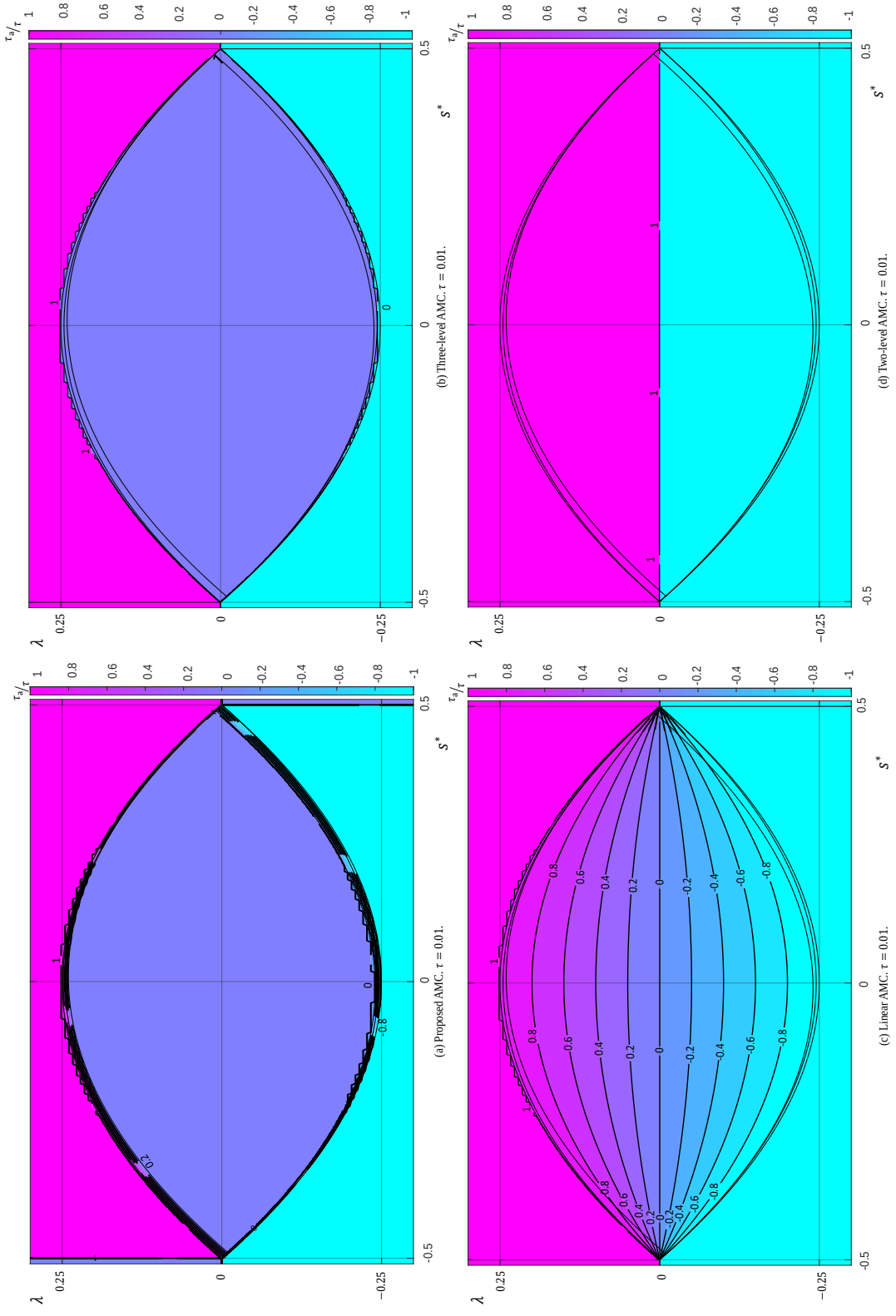


Figure 2.41: Comparison of the proposed compensation method, three-level, linear ACM and two-level ACM with $\tau = 0.01$. In (a), $\frac{\tau_a}{\tau}$ varies from 0 to 1 from ϕ to α; $\frac{\tau_a}{\tau}$ varies from -1 to 0 from α' to ϕ.

3
Experimental Validation

This chapter validates the analysis of the dead-time distortion of the half-bridge model in Chapter 2 and demonstrates its accuracy through experimental results. The compensation method, which is mathematically derived from the half-bridge model, is also verified. A comparison of the three widely used compensation methods and the proposed one is demonstrated.

3.1 Experimental Setup

Fig. 3.1 shows the circuit diagram and the setup block diagram. Fig. 3.2 shows a photo of the PCB used in this experiment. This experiment uses a GaN half-birdge. This is because the theoretical analysis in Chapter 2 is based on an assumption that all components are ideal, i.e., switches have fast rising and falling edges. GaN FETs behave closely to ideal components.

3.1.1 Power Circuit

An EPC23104 chip integrates two 80 V, 15 A GaN FETs, bootstrap circuitry, gate drivers, and an input logic interface in a half-bridge configuration. The Development Board EPC90152, which contains the EPC23104 chip, is used. Two gate signals

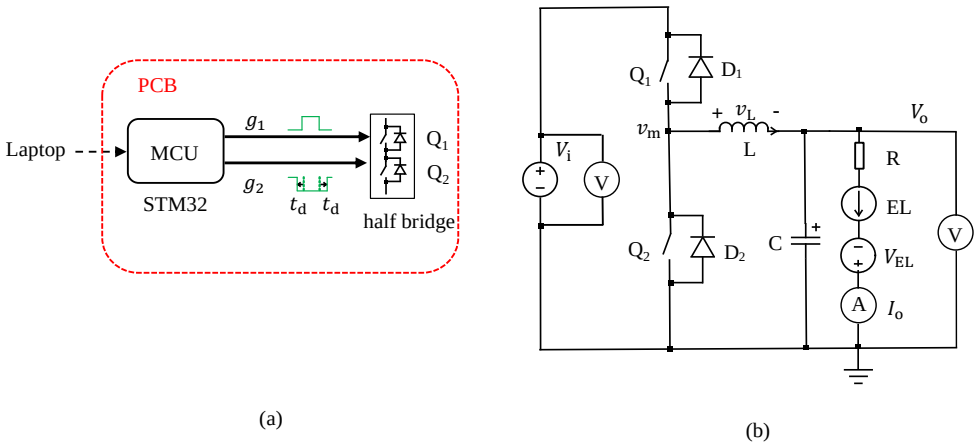


Figure 3.1: (a) Block diagram of the experimental setup. (b) Circuit diagram of the half-bridge, with an electronic load (EL) and digital multimeters.

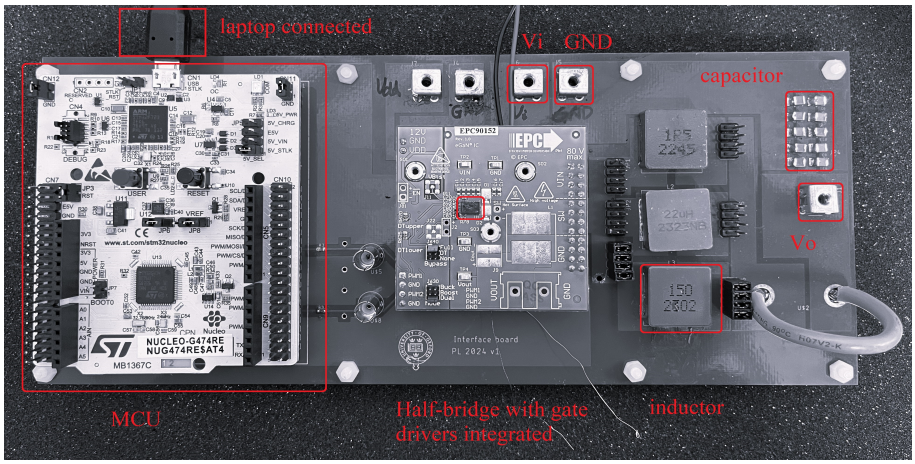


Figure 3.2: Photo of the PCB.

are inputs to this development board. They connect to the EPC23104 input logic interface. Other circuits included in this development board are not activated.

Fig. 3.3 shows the simplified schematic of the bootstrap circuit in the EPC90152. A bootstrap capacitor, C_{boot}, drives the high-side GaN FET, Q_1. When M_{PO1} is on, the bootstrap capacitor C_{boot} connects the gate and source of Q_1, through R_{boot}. Therefore, the voltage across C_{boot}, V_{boot}, is applied to v_{gs}, which turns Q_1 on. In this process, the bootstrap capacitor C_{boot} discharges by charging the gate-source capacitor of Q_1, and dissipating heat in R_{boot}. A bootstrap FET, Q_{SB}, connects the bias voltage supply, V_{cc}, and the bootstrap capacitor C_{boot}. It is driven synchronously with the low-side GaN FET, Q_2. During the on period of Q_1, it

is off. When the transistor Q_2 is on, the transistor Q_{SB} is also on such that V_{cc} charges C_{boot}, which compensates the energy that C_{boot} loses when it turns on Q_1. Because C_{boot} is only charged during the off period of Q_1, it may not charge up appropriately when this off period is very short. In such a case, the voltage across C_{boot}, V_{boot}, keeps decreasing and eventually is not sufficient to turn on Q_1. This limits the maximum on period Q_1 can have. This can occur in this experiment when s is large. To avoid such a situation, an isolated DC-DC converter, RSO-1205SZ, is connected in parallel with C_{boot}. It provides 5 V across the bootstrap capacitor and so guarantees that the transistor Q_1 can be turned on when its off period is very short. It is attached to the back of the development board (see Fig. 3.4). No external output capacitor is added to this DC-DC converter.

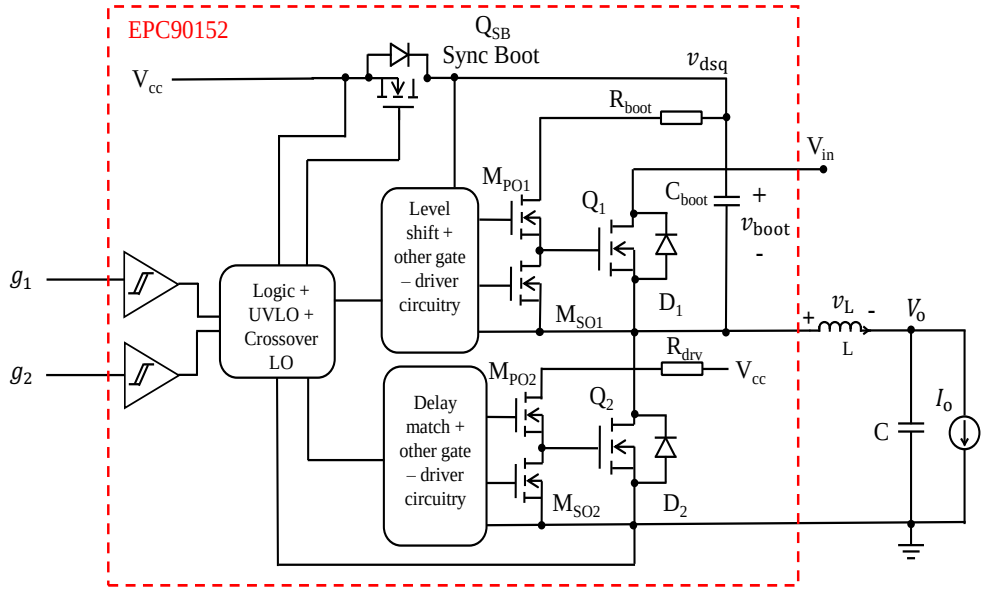


Figure 3.3: Simplified boostrap circuits of EPC90152. The voltage V_{cc} is generated from V_{dd} in EPC90152. This figure is reproduced from [88, 89].

An LC low-pass filter connects to the switch node. The load is an electronic load, EA-EL 3160-60, which operates in the constant current mode as a current sink.

Fig. 3.5 shows the general circuit diagram of an electronic load in the constant current mode. Transistors arranged in parallel simulate the behaviour of a variable resistor. When a reference current is set, a reference voltage, equal to the multiplication of the reference current and the shunt resistance, $V_{ref} = I_{ref}R_{shunt}$, is

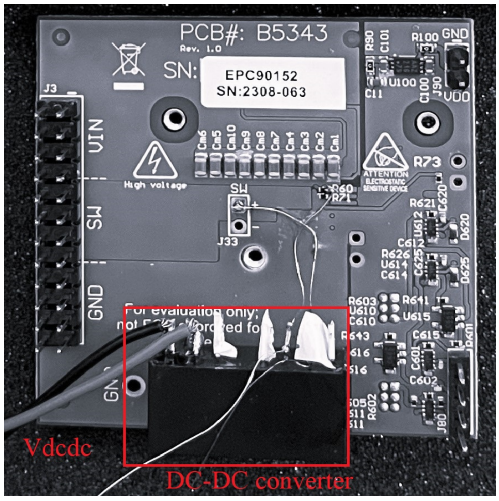


Figure 3.4: An isolated DC-DC converter is attached to the back of the EPC90152. It provides 5 V to the boot capacitor. Two cables provide its input voltage, V_{dcdc}.

applied to one input of an amplifier. The input current flows into the electronic load, through transistors, the shunt resistor and out of the electronic load. The voltage across the shunt resistor, $V_{\mathrm{shunt}} = I_{\mathrm{shunt}} R_{\mathrm{shunt}}$, is fed into the other input of the amplifier, which compares that voltage with the reference voltage to regulate the current flow through the transistors accordingly. Due to the shunt resistor and transistors, a minimum amount of voltage across the electronic load is required to provide a specific current. When s is small, the voltage across the electronic load is so low that the maximum I_{o} that can be drawn is limited [90]. Therefore, an additional voltage source, V_{EL}, is added to ensure the expected I_{o} can be provided by the electronic load, as shown in Fig. 3.1 (b).

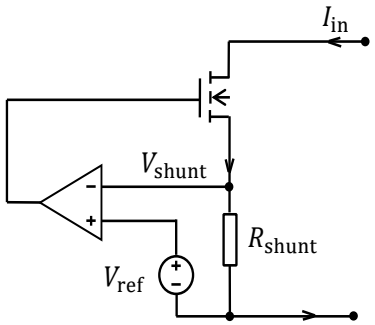


Figure 3.5: A circuit diagram of an electronic load. It is reproduced from [91].

The power supplies, EA-PS 2342-10 B, provide the input voltage V_{i}, the gate

drive input supply in the EPC90152, V_{dd}, the input voltage of the DC-DC converter V_{dcdc}, and the voltage across the electronic load V_{EL}. The PC powers the MCU via USB. Table 3.1 shows the specifications related to this power circuit.

Table 3.1: Key parameters in this experiment.

parameters	value
V_{i}	48 V
I_{o}	[0, 8.5 A]
f_{sw}	50 kHz
τ	0.1
L	17 μH
C	80 μF
R	1 Ω
V_{EL}	8.5 V
V_{dd}	12 V
V_{dcdc}	12 V

3.1.2 Gate Signal

A PC communicates with the MCU digitally. The MCU generates gate signals, which are directly fed into the half-bridge. A STM32 Nucleo-64 board with the STM32G474RE MCU generates g_1 and g_2, which are applied directly to the power circuit. A high-resolution timer peripheral (HRTIM) enables a time resolution of 368 ps ($f_{\mathrm{clk}} = 170$ MHz $\times$ 16) at $f_{\mathrm{sw}} = 50$ kHz [92]. The greatest possible error caused by the smallest duty cycle adjustment increment available, i.e., PWM resolution, is

$$\frac{T_{\mathrm{clk}}}{2T_{\mathrm{sw}}} = \frac{f_{\mathrm{sw}}}{2f_{\mathrm{clk}}} = \frac{50\text{ kHz}}{2 \times 170 \times 16\text{ MHz}} = 0.0009\%, \tag{3.1}$$

which is negligible.

This MCU has a dead-time manager. It generates a complementary signal of the target signal and then delays the rising edges of both. For cases where $s \in [(\tau - 0.5), (0.5 - \tau)]$, this manager is activated such that the PC only sends commands, in binary digits, that are related to the on and off time instants of the high-side gate signal without dead-time inserted, to the MCU. In cases where $s < (\tau - 0.5)$ or $s > (0.5 - \tau)$, one of the gate signals remains logic low always, i.e.,

a gate signal does not have any rising edge. The dead-time manager is inactivated in these cases. The PC only sends commands related to the gate signal that has rising and falling edges, with dead-time inserted, to the MCU. The MCU then generates the gate signal accordingly. The other gate signal, which is always logic low, is generated by the MCU. Fig. 3.6 shows this process.

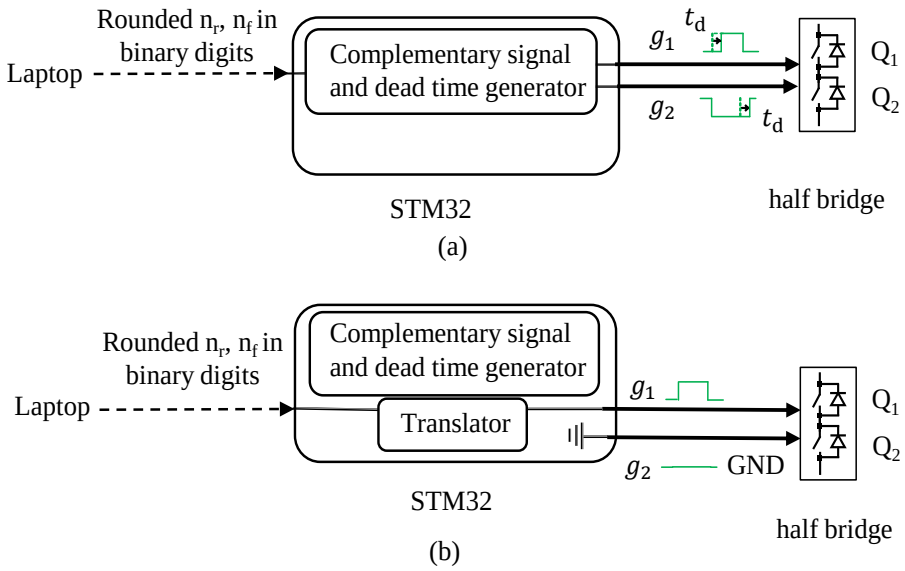


Figure 3.6: Generation of gate signals. (a) Use an existing block to produce a complementary signal and insert dead-time. (b) This block is inactivated in extreme cases where $s < (\tau - 0.5)$ or $s > (0.5 - \tau)$, when one of the gate signals always remains logic low. A translator generates g_1 based on the received binary digits.

The on and off timing information of the gate signals is pre-coded in the PC. The PC sends this information to the MCU in binary format. The number of MCU clocks per switching period is calculated by:

$$N_{\text{clk}} = \frac{T_{\text{sw}}}{T_{\text{clk}}} = \frac{f_{\text{clk}}}{f_{\text{sw}}}. \tag{3.2}$$

For a given s and τ, the time instants of the rising and falling edge of a gate signal are described in the number of clocks, n_{r} and n_{f} respectively, assuming the clock counts zero at the beginning of the switching period and N_{clk} at the end. When $s \in [(\tau - 0.5), (0.5 - \tau)]$, without dead-time insertion, the expressions of n_{r} and n_{f} are:

$$\begin{cases} n_{\text{r}} = 0.5(0.5 - s)N_{\text{clk}}, \\ n_{\text{f}} = 0.5(1.5 + s)N_{\text{clk}}. \end{cases} \tag{3.3}$$

Based on the value of s, the numbers of clocks n_r and n_f may be fractional, which cannot be implemented in the MCU. Therefore, these two numbers n_r and n_f must be rounded to integers. Four combinations are possible as shown in Table 3.2. The error, Δs, caused by this rounding for each combination is calculated, as shown in Table 3.2. The combination with the least absolute value of Δs is selected. The rounded n_r and n_f are then transmitted to the MCU in binary format by the PC, via UART at the baud rate of 115200 bits per second. The MCU receives these binary numbers and produces gate signals accordingly.

Table 3.2: All the possible combinations of rounding n_r and n_f into integers.

Combination	Δs
(a) $\lfloor n_\mathrm{r} \rfloor$, $\lceil n_\mathrm{f} \rceil$	$n_\mathrm{r} - \lfloor n_\mathrm{r} \rfloor + \lceil n_\mathrm{f} \rceil - n_\mathrm{f}$
(b) $\lfloor n_\mathrm{r} \rfloor$, $\lfloor n_\mathrm{f} \rfloor$	$n_\mathrm{r} - \lfloor n_\mathrm{r} \rfloor - \lceil n_\mathrm{f} - \lfloor n_\mathrm{f} \rfloor \rceil$
(c) $\lceil n_\mathrm{r} \rceil$, $\lceil n_\mathrm{f} \rceil$	$-\lceil \lceil n_\mathrm{r} \rceil - n_\mathrm{r} \rceil + \lceil n_\mathrm{f} \rceil - n_\mathrm{f}$
(d) $\lceil n_\mathrm{r} \rceil$, $\lfloor n_\mathrm{f} \rfloor$	$-\lceil \lceil n_\mathrm{r} \rceil - n_\mathrm{r} \rceil - \lceil n_\mathrm{f} - \lfloor n_\mathrm{f} \rfloor \rceil$

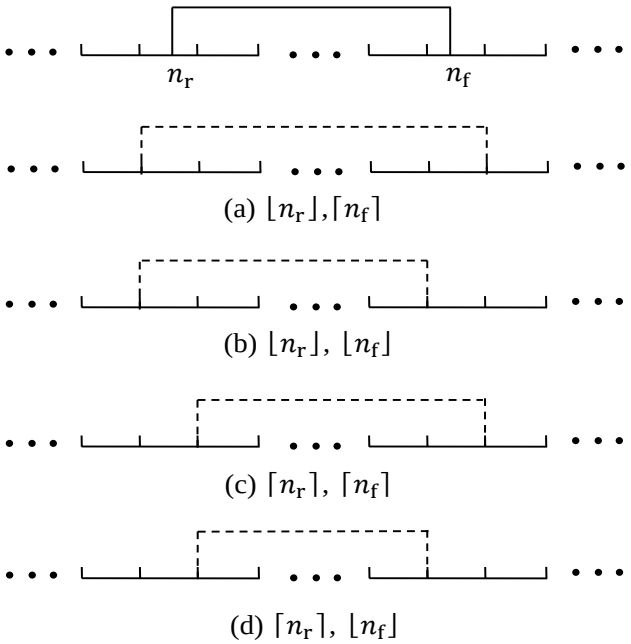


Figure 3.7: Combinations to round n_r and n_f into integers. The deviation Δs caused by each combination is listed in Table 3.2.

When $s \in [-(\tau + 0.5), (\tau - 0.5)]$, the gate signal g_1 is always zero ($g_1 \equiv 0$). The expressions of n_r and n_f of g_2 with dead-time insertion are:

$$\begin{cases} n_{\mathrm{r}} = [0.75 + 0.5(s+\tau)]N_{\mathrm{clk}}, \\ n_{\mathrm{f}} = 0.5(0.5 - \tau - s)N_{\mathrm{clk}}. \end{cases} \tag{3.4}$$

When $s \in [(0.5-\tau), (\tau+0.5)]$, the gate signal g_2 is always zero ($g_2 \equiv 0$). The expressions of n_{r} and n_{f} of g_1 with dead-time insertion are:

$$\begin{cases} n_{\mathrm{r}} = 0.5(0.5 + \tau - s)N_{\mathrm{clk}}, \\ n_{\mathrm{f}} = [0.75 + 0.5(s-\tau)]N_{\mathrm{clk}}. \end{cases} \tag{3.5}$$

Same to the situation aforementioned, n_{r} and n_{f} are rounded into integers that lead to the least absolute value of Δs, and then these integers are sent to the MCU via binary digits from the PC.

Fig. 3.8 shows an example of gate signals generated in this way. They are measured at the output of the MCU.

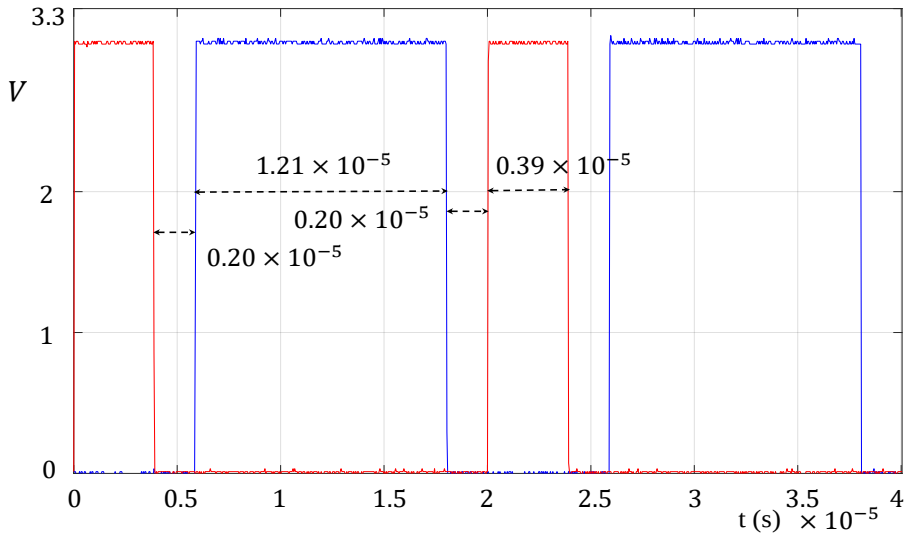


Figure 3.8: An example of measured gate waveforms. The blue curve is g_1. The red curve is g_2. They are fed into EPC90152 directly. $s = 0.2066$.

3.1.3 Measurement

Two digital multimeters, Keithley DMM6500, measure V_{o} and I_{o} respectively. A Keithley Model 2000 digital multimeter measures V_{i}. Table 3.3 shows the specifications related to the measurement [93, 94].

Table 3.3: Settings of digital multimeters. The Model 2000 is set so to balance its accuracy and reading speed.

setting \ meter	DMM6500	Model 2000
NPLC	10	10
Filter type	Repeating	Moving
Filter count	100	10

The maximum errors of measurements due to the accuracy of digital multimeters, in V_o, I_o, and V_i respectively, are [93, 94]:

$$\delta v_\mathrm{o} = 48 \times 0.005\% + 100 \times 0.0006\% = 0.003\ V, \tag{3.6}$$

$$\delta i_\mathrm{o} = 10 \times 0.25\% + 10 \times 0.025 = 0.0275\ A, \tag{3.7}$$

$$\delta v_\mathrm{i} = 48 \times 45 \times 10^{-6} + 100 \times 6 \times 10^{-6} = 0.00276\ V. \tag{3.8}$$

Errors due to the limitation of the measurement, the maximum errors of measurement, δv_o, δi_o and δv_i, can build up and lead to a combined error that affects the accuracy of M_meas and M_thry. Partial differentiation is used to estimate this combined error [95].

The error in the measured conversion ratio, $M_\mathrm{meas} = \frac{v_\mathrm{o}}{v_\mathrm{i}}$, resulting from δv_o and δv_i, is expressed as:

$$\delta M_\mathrm{meas}(v_\mathrm{o}, v_\mathrm{i}) = \frac{\partial M_\mathrm{meas}}{\partial v_\mathrm{o}} \delta v_\mathrm{o} + \frac{\partial M_\mathrm{meas}}{\partial v_\mathrm{i}} \delta v_\mathrm{i} \leq 6.25 \times 10^{-5}. \tag{3.9}$$

Similarly, the error in the theoretical conversion ratio, M_thry, which is derived from equations in Section 2.2 chapter 2 based on measured i_o and measured v_i, is expressed as:

$$\delta M_\mathrm{thry}(i_\mathrm{o}, v_\mathrm{i}) = \frac{\partial M_\mathrm{thry}}{\partial i_\mathrm{o}} \delta i_\mathrm{o} + \frac{\partial M_\mathrm{thry}}{\partial v_\mathrm{i}} \delta v_\mathrm{i}. \tag{3.10}$$

The maximum value of this error for each operating mode is listed in Table 3.4.

Table 3.4: The maximum error of M_{thry} due to the accuracy of the multimeters.

Operating Mode	$\delta M_{\text{thry}} \leq x$
C_{np}	$x = 1.53 \times 10^{-3}$
$D_{2\text{p}}$	$x = 1.20 \times 10^{-3}$
$D_{1\text{p}}$	$x = 1.09 \times 10^{-3}$
$D_{1\text{n}}$	$x = 1.20 \times 10^{-3}$
$C_{0\text{p}}$, C_{p}, C_0	$x = 0$

The precision of s impacts the precision of g_1 and g_2. As the implementation hardly affects the precision of the PWM, as shown in (3.1), the reference signal s is as precise as 0.0009%. For convenience, four significant figures of s are presented in the following discussion. The number of significant figures for V_{i}, I_{o} (λ), and ΔM depends on the accuracy of the digital meters, as shown in (3.6), (3.7), (3.8), (3.9), (3.10) and Table 3.4.

3.2 Results

The range of s, $s \in [-(\tau+0.5), (\tau+0.5))$ and the range of λ, $\lambda \in [0, 0.3]$, are divided into small steps, generating an array of s values and an array of λ values. These two arrays create a meshed grid. Each dot on this grid represents an operating case with parameters of s and λ.

An experiment of 15,500 cases is run in the range of $s \in [-(\tau+0.5), (\tau+0.5))$, $\lambda \in [0, 0.3]$. For each case, digital multimeters collect readings of V_{o}, I_{o}, and V_{i}, and send them to a PC automatically. Due to the symmetry (see Section 2.2 chapter 2), the measurement of the half where $\lambda < 0$ is not repeated.

3.2.1 Half-bridge Model

The difference between M_{thry} and M_{meas}, ΔM, are found by:

$$\Delta M = M_{\text{meas}} - M_{\text{thry}}. \tag{3.11}$$

Its absolute value, $|\Delta M|$, is shown in Fig. 3.9.

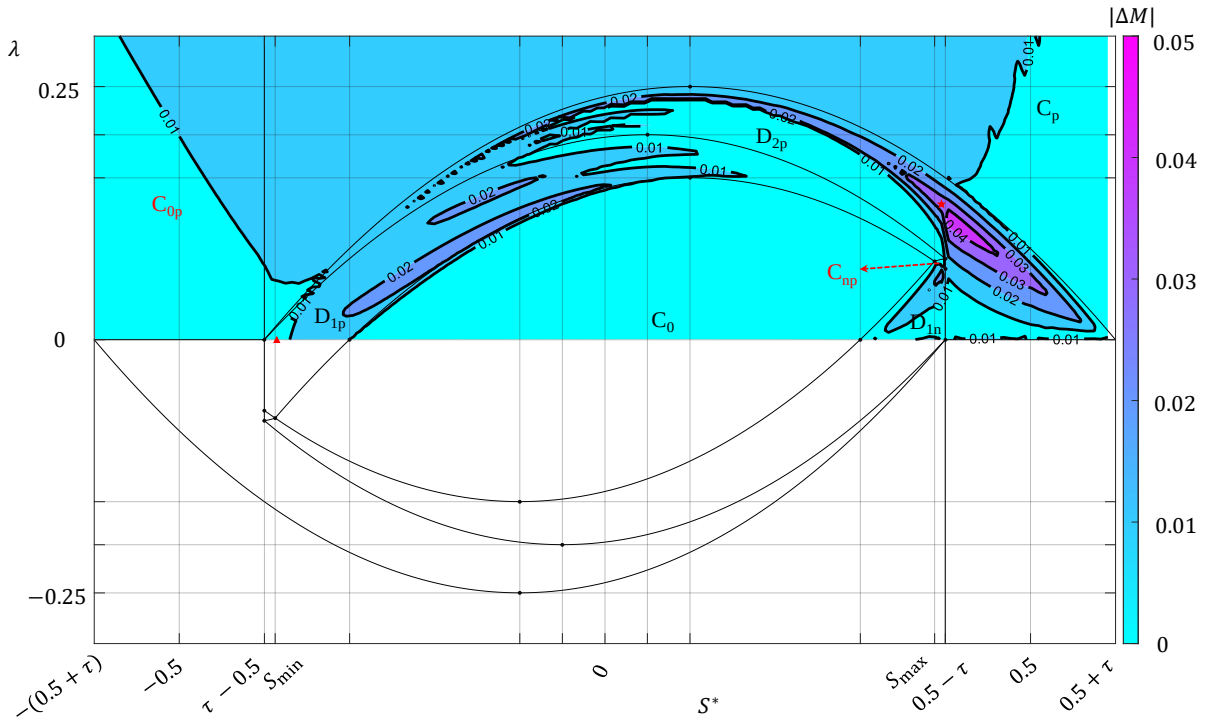


Figure 3.9: Values of $|\Delta M|$ at $\lambda \geq 0$. The boundaries are divisions of operating modes with $\tau = 0.1$. $|\Delta M| \leq 0.05$. Case I is marked in a red triangle in D_{1p}. Case II is marked in a red star in D_{2p}.

The cases near $s^* = (0.5 + \tau)$ are not run. In these cases, the transistor Q_1 is on, and the transistor Q_2 is always off, i.e., the half-bridge directly connects V_i to V_o.

Compared with Fig. 2.20, Fig. 3.9 shows the accuracy of the half-bridge model proposed in Chapter 2. These equations from Section 2.2 predict the average output voltage from various operating modes to within a few percent. The newly identified regions, C_{0p} and C_{np}, are accurate with an error of less than 0.02. A group of cases that are located in D_{2p} have an error between 0.03 and 0.05. Apart from this group, other operating modes are accurate within an error of less than 0.03. This error, ΔM, represents the ratio of the voltage difference between the measured output voltage and the theoretical output voltage over the measured input voltage.

The waveforms of the two cases are presented as follows. Case I has a low discrepancy where $|\Delta M| = 0.005$. The voltage v_m and the current i_L are well predicted by the theoretical analysis in Chapter 2. It is marked as a red triangle in D_{1p} where $s = -0.3834$, $\lambda = 0$ ($I_o = 0$), $V_{in} = 48.048$ V (see Fig. 3.9). Case II has a large discrepancy where $|\Delta M| = 0.035$. A big deviation from the theory

occurs on the rising edge of v_{m}. It is marked as a red star in $\mathrm{D_{2p}}$ where $s = 0.3956$, $\lambda = 0.13$ ($I_{\mathrm{o}} = 3.69$ A), $V_{\mathrm{in}} = 47.870$ V (see Fig. 3.9). The waveforms in this thesis are measured with an oscilloscope, Keysight DSOX2024A. The sample rate is 1 Gbits, and 1250 samples are captured. Voltage probes are TOKOGAWA 701939 Passive Probes. The current probe is Agilent N2783b.

Fig. 3.10 shows Case I. A small discrepancy exists between the measured waveforms, in red, and the theoretical ones, in blue. This is mainly due to the switching-node capacitance, c_{sw}, as discussed in Section 1.6.2. The following explanation is summarised in Fig. 3.11.

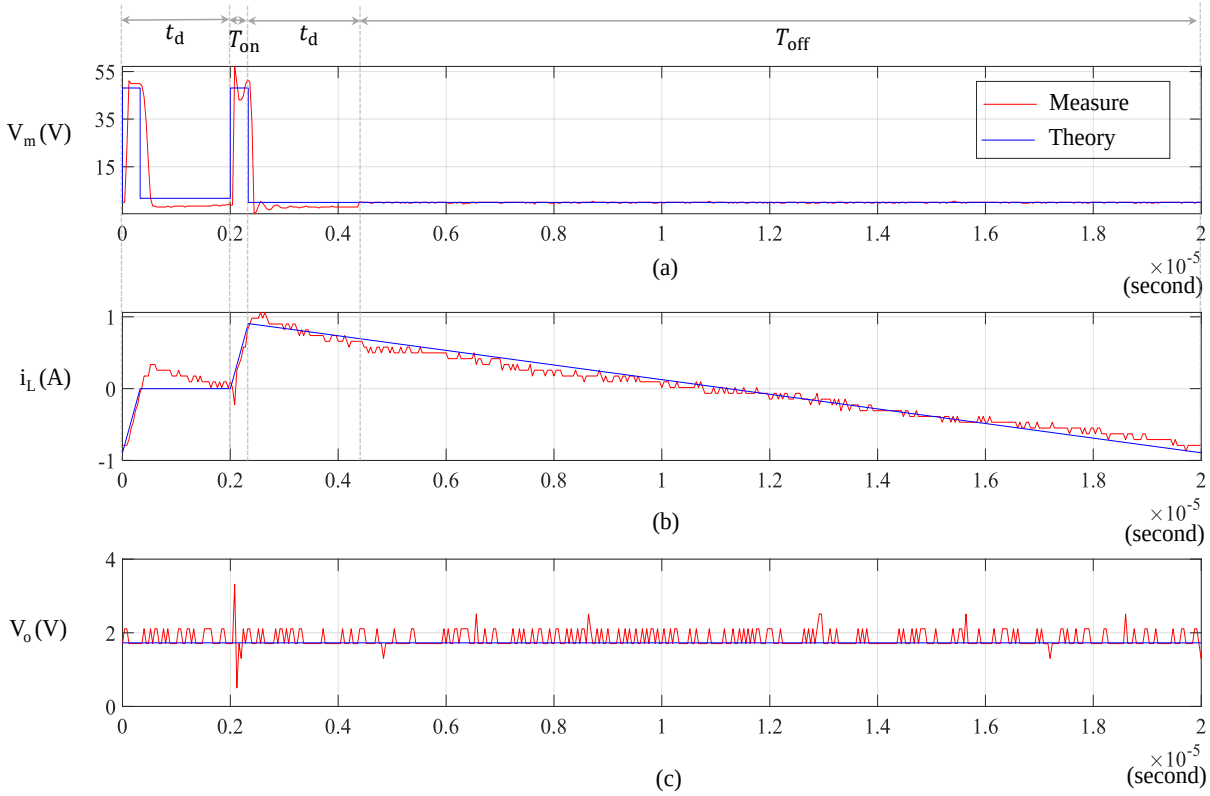
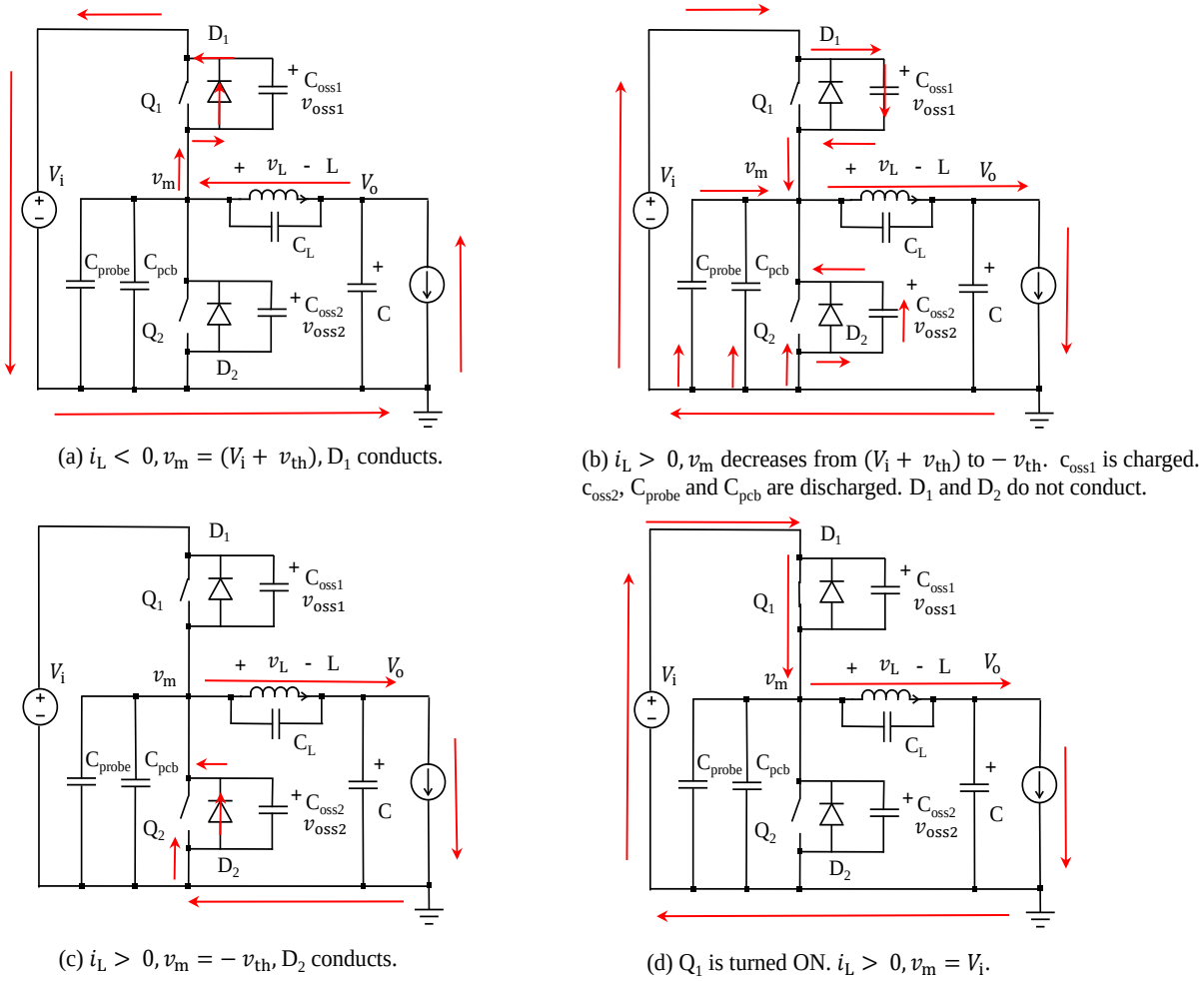


Figure 3.10: Waveforms of Case I. $|\Delta M| = 0.005$. (a) middle-point voltage. (b) inductor current. (c) output voltage. $\mathrm{t_d} = 2$ μs, $\mathrm{T_{on}} = 0.33$ μs, $\mathrm{T_{off}} = 15.67$ μs.

In the rising-edge dead-time, the inductor current i_{L} starts as negative, flowing into the power supply via $\mathrm{D_1}$ and so $v_{\mathrm{m}} = V_{\mathrm{i}}$. The inductor current i_{L} decreases in magnitude until it becomes zero. In the Model 1, after the current $i_{\mathrm{L}} = 0$, the middle point voltage equals the output voltage ($v_{\mathrm{m}} = V_{\mathrm{o}}$) until the transistor $\mathrm{Q_1}$ is turned on, as shown in the blue curves. However, in practice, the switching node



(a) $i_L < 0, v_m = (V_i + v_{th})$, D_1 conducts.

(b) $i_L > 0$, v_m decreases from $(V_i + v_{th})$ to $-v_{th}$. c_{oss1} is charged. c_{oss2}, C_{probe} and C_{pcb} are discharged. D_1 and D_2 do not conduct.

(c) $i_L > 0, v_m = -v_{th}$, D_2 conducts.

(d) Q_1 is turned ON. $i_L > 0, v_m = V_i$.

Figure 3.11: Charging and discharging c_{sw} during the rising-edge dead-time of Case I (see Fig. 3.10). Red arrows indicate the flow of i_L.

capacitance c_{sw} exists. When $i_L < 0$, the voltage across c_{oss1} is zero. The voltages across c_{oss2}, C_{pcb} and C_{probe} are the middle point voltage, which equals the input voltage ($v_m = V_i$). At the instant when $i_L = 0$, $v_m = V_i$, and so the inductor current i_L starts to increase in the positive direction, flowing into the electronic load via the inductor L. It charges and discharges c_{oss1}, c_{oss2}, C_{PCB}, and C_{probe}. Diodes D_1 and D_2 are blocked. The middle point voltage v_m decreases from V_i. When the middle point voltage equals the output voltage ($v_m = V_o$), the inductor current i_L reaches its maximum magnitude in the positive direction during this dead-time. After the middle point voltage becomes smaller than the output voltage ($v_m < V_o$), the inductor current i_L decreases. Capacitors c_{oss2}, C_{PCB}, and C_{probe} keep discharging until the middle point voltage v_m, which is the v_{ds} of Q_2, is less than V_{th}. At that

time, the diode D_2 conducts and supports i_L freewheeling.

In the falling-edge dead-time, the inducotr current i_L is negative ($i_L > 0$). In the half-bridge model, the inductor current i_L freewheels through D_2. In practice, the current i_L discharges c_{oss2}, C_{PCB}, and C_{probe}, and charges c_{oss1} first, then freewheels through D_2 after the middle point voltage becomes smaller than the threshhold voltage ($v_m \leq -V_{th}$). As the current i_L has a large magnitude at the beginning of the falling-edge dead-time, this charging and discharging process occurs fast. Therefore, there is not much difference between the measured waveform and that derived from the theory.

Fig. 3.12 shows Case II. There is a great discrepancy between the measurement and the theory after the inductor current becomes zero ($i_{\mathrm{L}} = 0$) in the rising-edge dead-time. In the Model 1, the middle-point voltage equals the output voltage ($v_{\mathrm{m}} = V_{\mathrm{o}}$) until the transistor Q_1 is on. In practice, the inductor current i_{L} increases in the negative direction and the middle-point voltage v_{m} increases gradually, i.e., the current i_{L} charges c_{sw}.

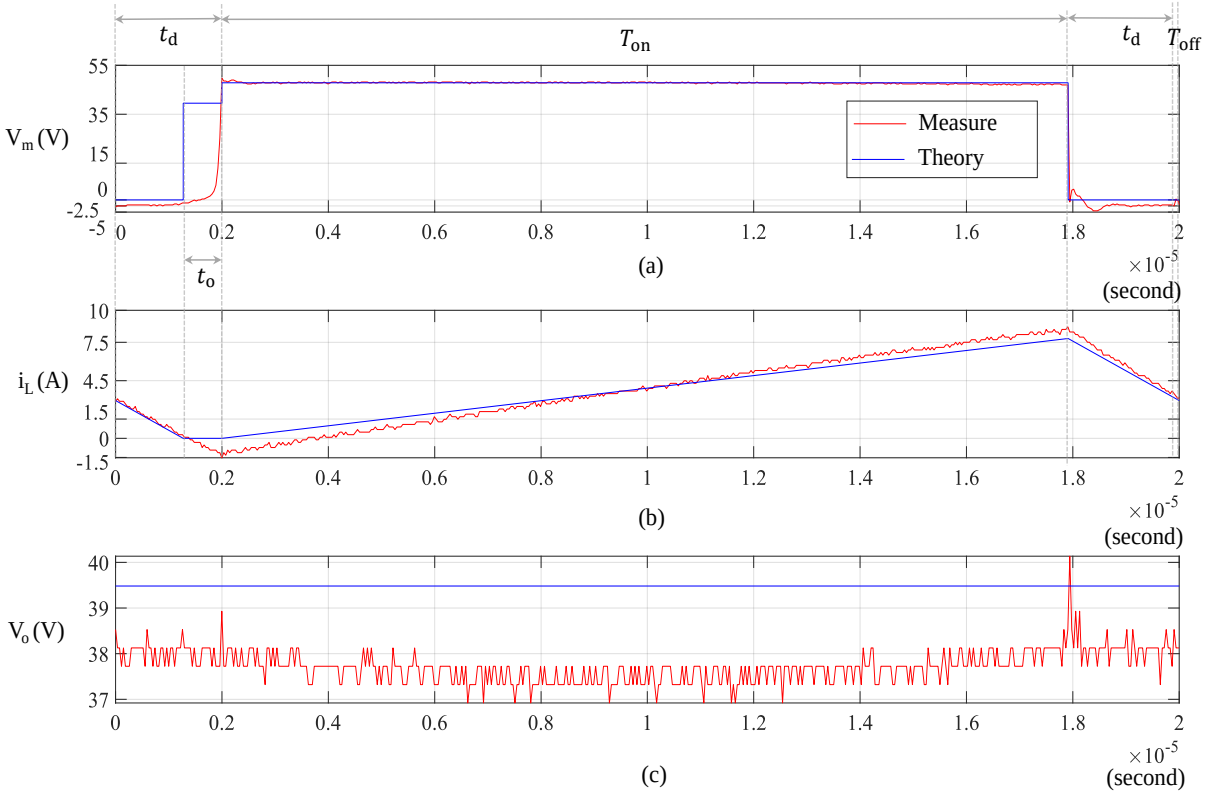


Figure 3.12: Waveforms of Case II. $|\Delta M| = 0.035$. (a) middle-point voltage. (b) inductor current. (c) output voltage. $\mathrm{t_d} = 2\ \mu$s, $\mathrm{T_{on}} = 15.9\ \mu$s, $\mathrm{T_{off}} = 0.1\ \mu$s. $t_{\mathrm{o}} = 0.7\,\mu$s.

Based on (1.19), during the rising-edge dead-time, the charging period can be divided into small slots against v_{m}. For each slot, the middle point voltage v_{m} varies from v_{m1} to v_{m2}. The switching node capacitor c_{sw} is approximated accordingly. Fig. 3.13 (b) and (c) approximate the variation of c_{sw} against v_{m} from Fig. 3.10 and 3.12, respectively. The intervals of v_{m} to estimate c_{sw} are selected based on how linearly v_{m} varies over the period, and so for each interval, the capacitor c_{sw} is regarded as a fixed value. Mostly $c_{\mathrm{oss1}} = c_{\mathrm{oss2}} = c_{\mathrm{oss}}$. Fig. 3.13 (a) plots $2c_{\mathrm{oss}}$ where the output capacitor c_{oss} is the output capacitance of one GaN FET in the EPC23104 chip.

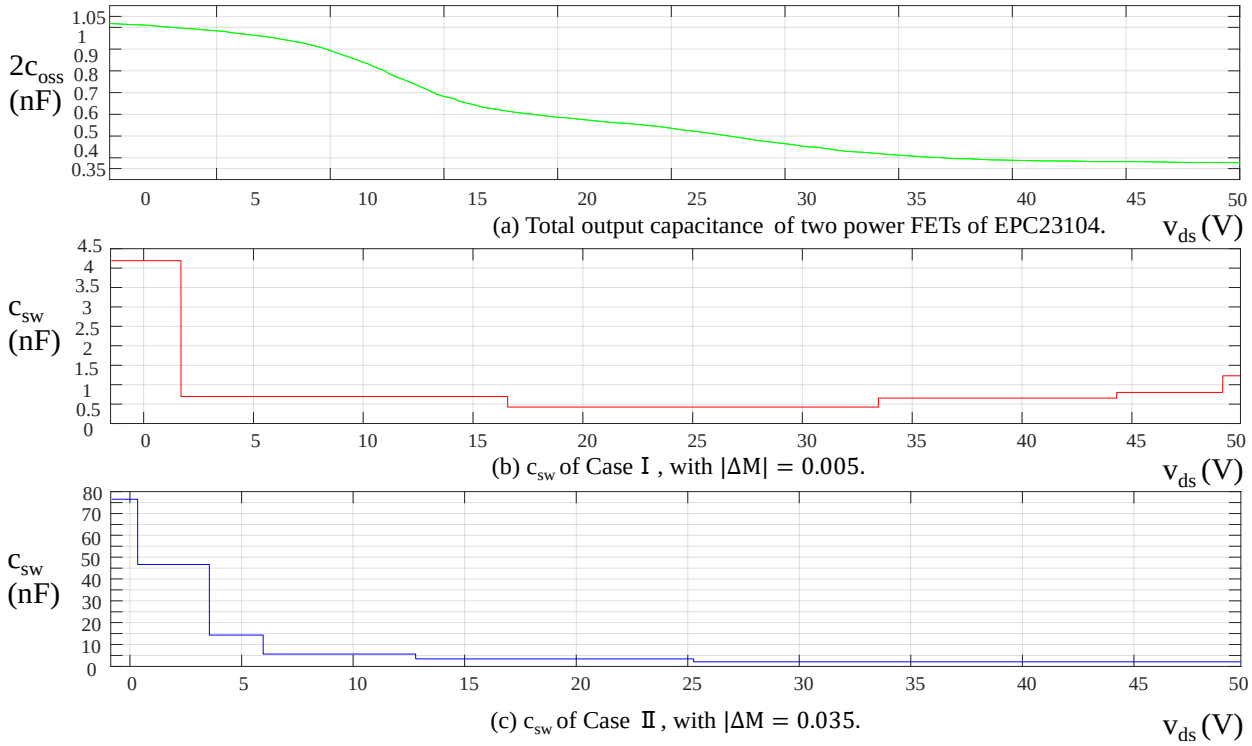


Figure 3.13: The output capacitor c_{oss} in (a) is the output capacitance of one GaN FET in the EPC23104 chip [75]. The switching node capacitors c_{sw} in (b) (c) are approximated by (1.19).

The switching node capacitor $c_{\rm sw}$ from Case II is much larger than that from Case I, and that $2c_{\rm oss}$ from the datasheet. Therefore, it takes a longer time period for $i_{\rm L}$ to charge this unexpectedly large $c_{\rm sw}$. During this charging period, $v_{\rm m}$ increases very slowly. Therefore, a voltage loss is identified in the rising-edge dead-time, compared with $V_{\rm o}$ derived from the theory. This loss leads to $|\Delta M| \geq 0.03$. From Fig. 3.12, $|\Delta M|$ is estimated as:

$$\Delta M = -\frac{\Delta V_{\rm o}}{V_{\rm i}} = -\frac{V_{\rm othry} t_{\rm o}}{T_{\rm sw} V_{\rm i}} = -\frac{39.668 \times 0.728 \times 10^{-6}}{2 \times 10^{-5} \times 47.870} = -0.0302, \tag{3.12}$$

where

$V_{\rm othry}$: the output voltage derived from the theory based on $V_{\rm i}$, λ, s and τ.

$t_{\rm o}$: the time period when $v_{\rm m} = V_{\rm o}$ ($i_{\rm L} = 0$) during the dead-time in theory. When the inductor current $i_{\rm L}$ is small, the switching node capacitor $c_{\rm sw}$ makes a big difference to the voltage-time product, and so a big discrepancy appears in $V_{\rm o}$.

Another discrepancy caused by the voltage drop during the SCRC, $V_{\rm bd}$, over the rest period of the dead-time, is estimated as:

$$\Delta M_{\rm bd} = -\frac{V_{\rm bd}(2t_{\rm d} - t_{\rm o})}{T_{\rm sw} V_{\rm i}} = -\frac{2.5 \times (2 - 0.728) \times 10^{-6}}{2 \times 10^{-5} \times 47.870} = -0.003. \tag{3.13}$$

As $\Delta M + \Delta M_{\rm bd} = -0.0332$, it illustrates that (i) this large $c_{\rm sw}$ dominantly contributes to $|\Delta M| = 0.035$. (ii) the voltage drop across transistors during the dead-time, $V_{\rm bd}$, also affects $|\Delta M|$.

Based on the discussion in Section 1.6.2, contributors to $c_{\rm sw}$ are estimated. Table 3.5 lists these contributors in this experiment. An impedance analyser, PSM1735 N4LN, is used to measure $C_{\rm L} = 38$ pF. The prepreg, FR370HR, is used in the PCB designed by EPC. The switching node capacitor $c_{\rm sw}$ measured from Case II is much larger than the sum of these parasitic capacitors listed here.

This large $c_{\rm sw}$ explains why $|\Delta M| \geq 0.03$ for the small group of cases in $\rm D_{2p}$ in Fig. 3.9. Errors where $0 < |\Delta M| < 0.03$ are caused by the impact of $c_{\rm sw}$ and the voltage drop across the transistors during SCRC. Chapter 4 presents simulations of Case I and Case II in Models 2 and 3, where the switching-node capacitance and SCRC are considered. The simulation results are compared with the measured

Table 3.5: Contributors to c_{sw}. The column of Q (nC) lists the charges that are stored in that capacitor when v_{m} changes from 0 to 48 V.

Contributors	C (pF)	Q (nC)
c_{oss}	170 - 510	8 - 24
C_{L}	38	2
C_{pcb}	60	3
C_{probe}	10.5 [96]	0.5

ones to explore the impact of c_{sw} and V_{bd} on $|\Delta M|$. Section 4.3 discusses the potential contributors to this large c_{sw}.

3.2.2 Discussion 1: Compensation Method

Fig. 3.14 shows the accuracy of the proposed compensation method based on Model 1. Assume that an ideal system generates the same conversion ratio as that of an uncompensated system: $M_{\mathrm{ideal}} = M_{\mathrm{meas}}$. Its input, s_{ideal}, is found, based on how gate signals are generated, as shown in Fig. 2.1. When $M_{\mathrm{meas}} \geq 1$ or $M_{\mathrm{meas}} \leq 0$, s_{ideal} does not have a unique value. Such cases are therefore excluded here, which limits the range of s_{ideal} to [-0.5, 0.5]. The difference between the input to the uncompensated system, s, and that of this ideal system, s_{ideal}, is denoted as τ_{ameas}:

$$\tau_{\mathrm{ameas}} = s - s_{\mathrm{ideal}}. \tag{3.14}$$

It is the additional amount of s that needs to be added to an uncompensated system so that the same results of an ideal system can be achieved, i.e., the average voltage error caused by the dead-time is removed. Fig. 3.14 (a) demonstrates τ_{ameas} found in this way based on the experimental results.

Fig. 2.27 demonstrates the amount of s should be added for compensation, τ_{a}. It is derived based on Model 1. Fig. 3.14 (b) zooms in Fig. 2.27 and shows the half with $\lambda \geq 0$, $\tau = 0.1$. The pattern of τ_{ameas} is similar to that of τ_{a}.

Near the right-hand side in $\mathrm{D}_{2\mathrm{p}}$, which is highlighted by a dotted red rectangle in Fig. 3.14 (a), the bands where $\tau_{\mathrm{a}} \in [0.02, 0.08]$, $\tau_{\mathrm{ameas}} = 0.1$. That is due to the large c_{sw} aforementioned, which leads to a large voltage loss during the

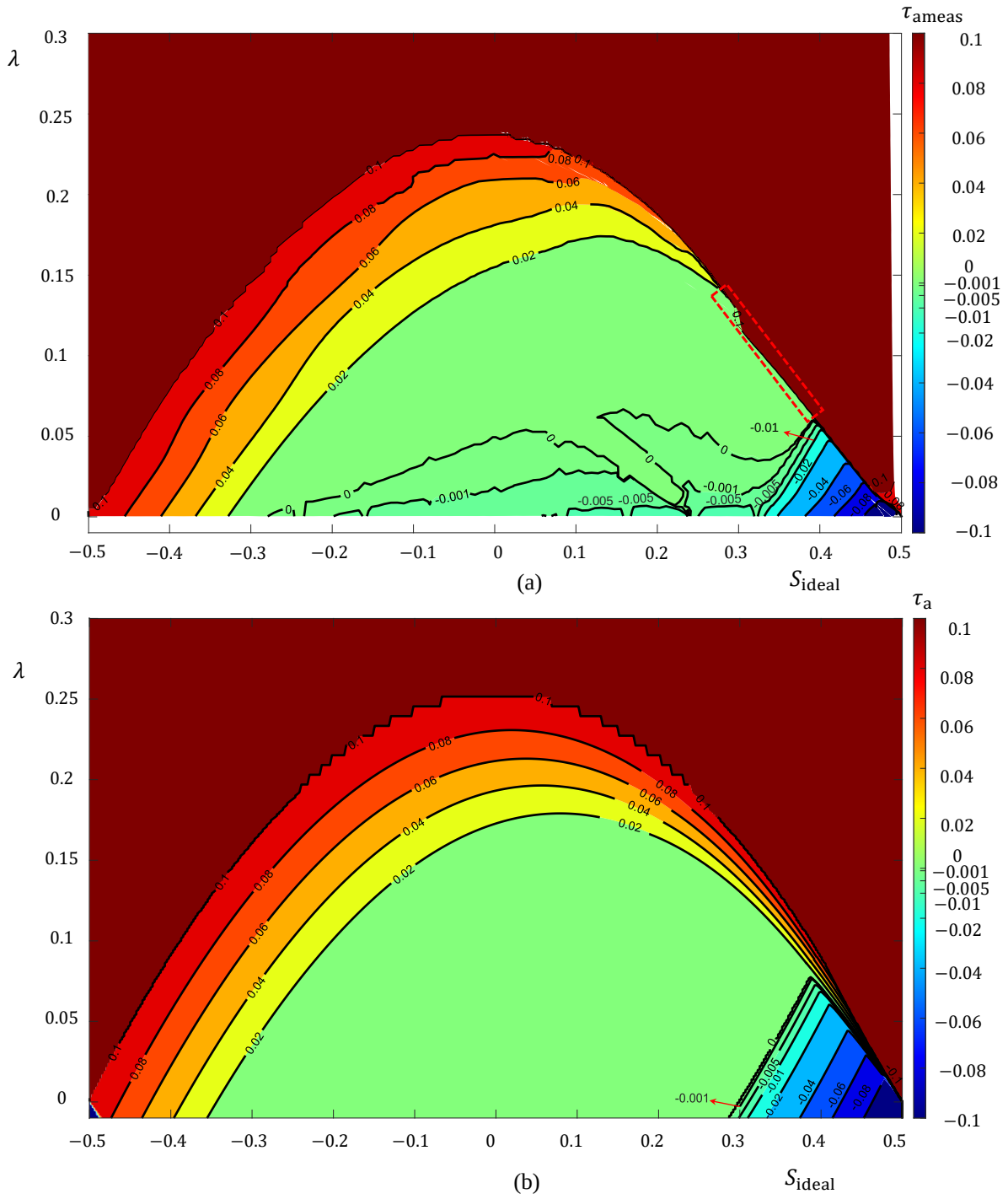


Figure 3.14: The amount that should be added to s of an uncompensated system such that the voltage error caused by t_d is removed. (a) The difference τ_{ameas} are found through experimental data. Cases, where unique s_{ideal} cannot be found, are excluded. Therefore, the x-axis ranges from -0.5 to 0.5, and NaN appears near $s_{ideal} = \pm 0.5$. (b) The value of τ_a is calculated via the proposed compensation method.

dead-time, and so the difference τ_{ameas} should be greater than the theory to compensate for this loss in V_{o}.

3.2.3 Discussion 2: Comparison with Conventional Methods

The three widely-used compensation methods, two-level ACM, three-level ACM and linear ACM, add τ_{a} to s^* to generate a new s_{n}, where $s_{\text{n}} = s^* + \tau_{\text{a}}$. The new reference signal s_{n} is then fed into the half-bridge to compensate for voltage errors, as aforementioned in Section 1.7. In the experiment, each operating case has s^* and λ. Based on each compensation method, the value of τ_{a} is found, so the new reference signal s_{n} can be calculated. Based on the measured M from the experiment, interpolation is applied to find the conversion ratio of a compensated system, M_{comp}, for a given s^* and λ, with a particular compensation method.

Interpolation is a technique to estimate unknown data points based on a pattern demonstrated by existing data points. As the conversion ratio of a compensated system M_{comp} is a function of two variables, s_{n} and λ, a two-dimensional interpolation is required. The bilinear interpolation is used here [97]. For any given s_{n} and λ, a rectangular grid of operating cases that are run in the experiment, $\text{A}_{\text{i,j}}$, $\text{A}_{\text{i+1, j}}$, $\text{A}_{\text{i,j+1}}$, $\text{A}_{\text{i+1,j+1}}$, is identified as shown in Fig. 3.15, where:

$$\begin{cases} s_{\text{i}} \leq s_{\text{n}} \leq s_{\text{i}+1}, \\ \lambda_{\text{j}} \leq \lambda \leq \lambda_{\text{j}+1}. \end{cases} \tag{3.15}$$

The normalized coordinate that s_{n} and λ locate in the grid are denoted as u and v respectively:

$$\begin{cases} u = \frac{s_{\text{n}} - s_{\text{i}}}{s_{\text{i}+1} - s_{\text{i}}}, \\ \\ v = \frac{\lambda - \lambda_{\text{j}}}{\lambda_{\text{j}+1} - \lambda_{\text{j}}}. \end{cases} \tag{3.16}$$

Therefore, the expression of M_{comp} is:

$$M_{\text{comp}} = M_{\text{i,j}}(1-u)(1-v) + M_{\text{i+1,j}}u(1-v) + M_{\text{i,j}+1}(1-u)v + M_{\text{i+1,j}+1}uv. \tag{3.17}$$

The difference between the interpolated conversion ratio with compensation implemented, M_{comp}, and the conversion ratio of an ideal system, M_{ideal}, is expressed

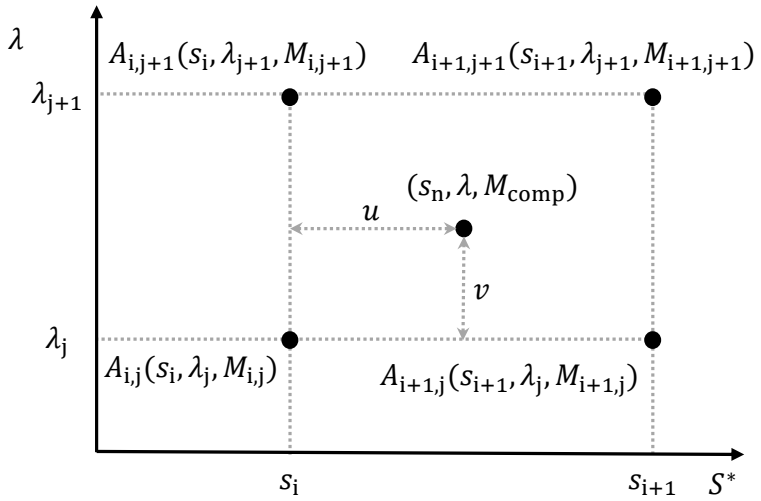


Figure 3.15: Bilinear interpolation to estimate M_{comp}.

as $\Delta = M_{\text{comp}} - M_{\text{ideal}}$. Fig. 3.16 (a) shows the normalised voltage error, the difference between M_{meas} and M_{thry}, caused by t_{d}. Fig. 3.16 (b)-(e) demonstrates Δ after the compensation.

As illustrated in Fig. 3.16 (a), insertion of t_{d} leads to a maximum voltage error of τ. This maximum voltage error is more likely to occur when λ is large ($\lambda > 0.24$ in Fig. 3.16 (a)). When λ is near zero, there is a region in which the insertion does not cause any errors. Between regions with the maximum and minimum voltage errors, the error increases from 0 to τ gradually as λ increases. Compared with Fig. 3.16 (a), all the compensation methods reduce the maximum error ($\tau = 0.1$) in the region with a large λ to a number less than 0.02. With the two-level ACM, the region with a minimum voltage error of 0 now increases the error between 0.08 and 0.10. The three-level ACM keeps the minimum voltage error equal to zero in the region when λ is near zero. However, it leaves part of the region with an error equal to 0.10. The linear ACM increases most of the voltage errors between 0 and 0.10. The proposed compensation method can limit errors to 0.03 across the whole map. As shown in Fig. 3.16, when $\tau = 0.1$, the 3-level ACM is closest to the proposed compensation method. This is also demonstrated in Fig. 2.40.

3.3 Conclusions

Based on the results and discussions presented in this chapter, the key conclusions are the following:

1. The half-bridge model (Model 1) predicts the average output voltage to within a few percent. Most cases have an error that is less than 0.03. These errors are caused by (a) voltage drop of the transistors during the SCRC; (b) capacitance at the switching point, which is mainly due to the output capacitance of transistors. A large c_{sw} is observed in the experiment, which leads to errors within [0.03, 0.05] in a small group of cases in $\mathrm{D}_{2\mathrm{p}}$.

2. The proposed compensation method is validated. In this method, an additional amount, τ_{a}, is added to s^*, to compensate for the voltage error. The value of τ_{a} is derived from the theory and then compared to τ_{ameas}, which comes from the experimental results. The comparison shows that the regions α, β, and ϕ, as well as the boundaries between them, have a similar pattern to the theoretical one.

3. The proposed compensation method reduces errors caused by t_{d} to 0.03 across all the operating modes. Three conventional compensation methods, namely two-level AMC, three-level AMC and linear AMC, all reduce the maximum errors from 0.02 to 0.10. However, all these methods increase errors in other regions. The maximum error after these compensation methods remains 0.10 ($\tau = 0.1$).

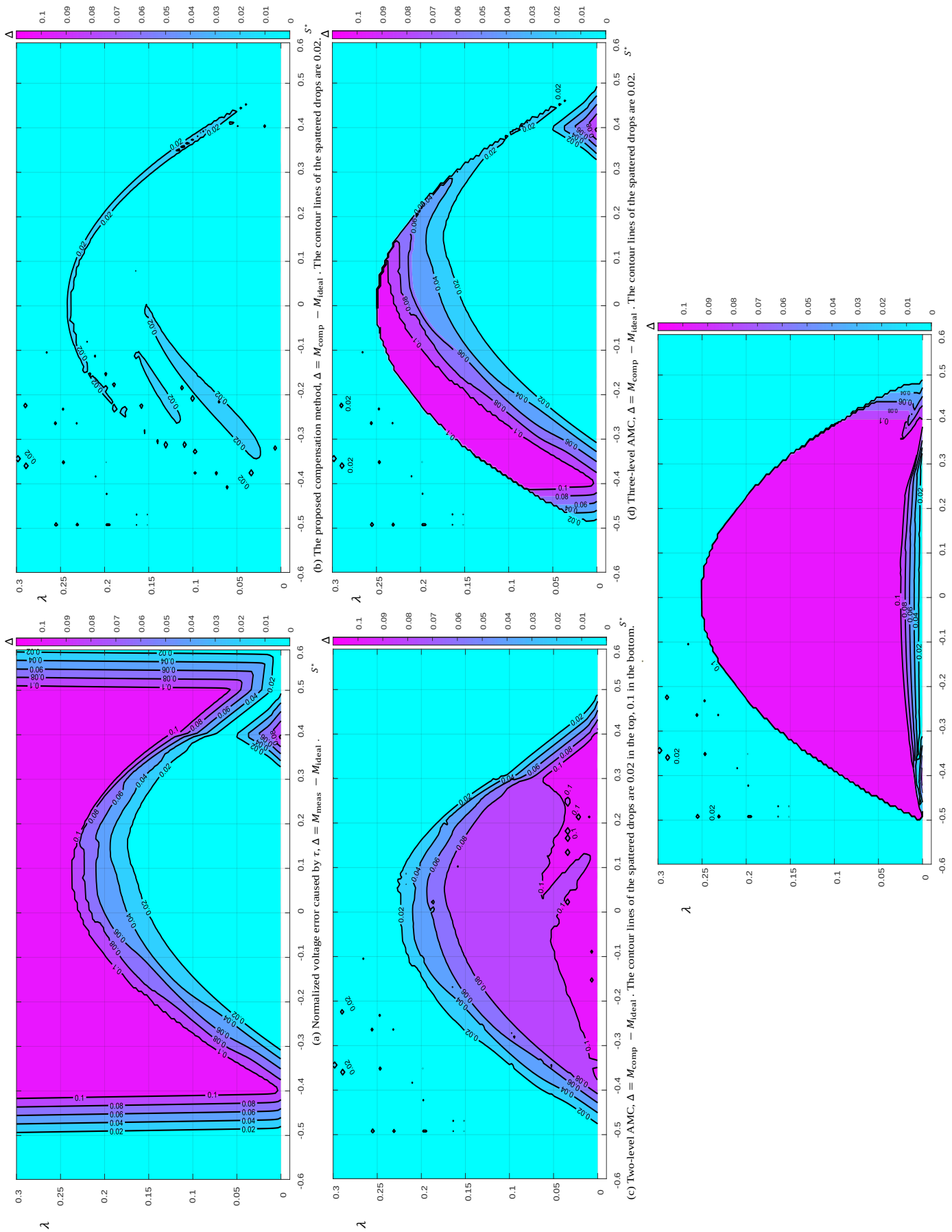


Figure 3.16: The difference between the conversion ratio of a compensated system and that of an ideal system.

(a) Normalized voltage error caused by τ, $\Delta = M_{\text{meas}} - M_{\text{ideal}}$.

(b) The proposed compensation method, $\Delta = M_{\text{comp}} - M_{\text{ideal}}$. The contour lines of the spattered drops are 0.02.

(c) Two-level AMC, $\Delta = M_{\text{comp}} - M_{\text{ideal}}$. The contour lines of the spattered drops are 0.02 in the top, 0.1 in the bottom.

(d) Three-level AMC, $\Delta = M_{\text{comp}} - M_{\text{ideal}}$. The contour lines of the spattered drops are 0.02.

(e) Linear AMC, $\Delta = M_{\text{comp}} - M_{\text{ideal}}$. The contour lines of the spattered drops are 0.02.

4

Half-bridge models with switching-node capacitance and self-commutated reverse conduction

Chapter 4 investigates the impact of the switching node capacitor c_{sw} and self-commutated reverse conduction (SCRC) on the output voltage of a half-bridge. A half-bridge model with fixed output capacitors of C_{oss} (Model 2), and a half-bridge model with variable c_{oss} (Model 3), are investigated. The impact of SCRC is considered in both models. As discussed in Section 1.6.2.1, the SCRC impact is modelled as a diode in parallel with the transistor. This diode has a source-to-drain voltage that equals the value of the threshold voltage, v_{th}, during the dead-time. The simulation results of these two models are demonstrated. A comparison of the simulation results, the measured results and the theoretical results is demonstrated. Contributors of the large c_{sw} that is observed in the experiment are explored. Model 4, which considers the bootstrap capacitor from the gate drive circuitry, is proposed and simulated.

4.1 A half-bridge model with fixed equivalent output capacitance and self-commutated reverse conduction

Fig. 3.13 (a) illustrates that the output capacitance of transistors is a function of $v_{\rm ds}$. To better understand the impact caused by $c_{\rm oss}$ during the dead-time, a fixed equivalent capacitor, $C_{\rm oss}$, which takes the same amount of time as $c_{\rm oss}$ to charge $v_{\rm ds}$ from 0 to $V_{\rm i}$, is included in the half-bridge model to represent $c_{\rm oss}$ [98]. This section investigates the impact of $c_{\rm oss}$ by modelling it with a fixed equivalent capacitor $C_{\rm oss}$.

Fig. 4.1 (a) shows a half-bridge with $C_{\rm oss}$. Fig. 4.1 (b) shows the simplified equivalent circuit of this half-bridge during the dead-time. The switches $\rm Q_1$ and $\rm Q_2$ are the same power transistors in most half-bridge configurations, and so $C_{\rm oss1} = C_{\rm coss2} = C_{\rm oss}$. The state space model (SSM) of this equivalent circuit in Fig. 4.1 (b) is:

$$\begin{cases} \frac{{\rm d}i_{\rm L}}{{\rm d}t} = \frac{1}{L}(v_{\rm m} - V_{\rm o} - Ri_{\rm L}), \\ \frac{{\rm d}v_{\rm m}}{{\rm d}t} = \frac{-i_{\rm L}}{2C_{\rm oss}+C_{\rm L}+C_{\rm pcb}+C_{\rm probe}}. \end{cases} \tag{4.1}$$

This is a second-order homogeneous differential equation, where $i_{\rm L}$ and $v_{\rm m}$ are sinusoidal equations with the frequency $f_{\rm m}$:

$$f_{\rm m} = \frac{\omega_{\rm m}}{2\pi} = \frac{1}{2\pi\sqrt{L(2C_{\rm oss} + C_{\rm L} + C_{\rm pcb} + C_{\rm probe})}}. \tag{4.2}$$

The expressions of $v_{\rm m}$ and $i_{\rm L}$ are:

$$\begin{cases} i_{\rm L} = e^{\alpha t}(A\cos\omega t + B\sin\omega t), \\ v_{\rm m} = L\dfrac{{\rm d}i_{\rm L}}{{\rm d}t} + V_{\rm o} + Ri_{\rm L} \\ \quad = e^{\alpha t}[(\alpha AL + B\omega L + RA)\cos\omega t + (\alpha BL - \omega AL + RB)\sin\omega t] + V_{\rm o}, \end{cases} \tag{4.3}$$

where

$$\begin{cases} \omega = \sqrt{\frac{1}{L(2C_{\rm oss}+C_{\rm L}+C_{\rm pcb}+C_{\rm probe})} - \frac{R^2}{4L^2}}, \\ \alpha = \frac{-R}{2L}. \end{cases} \tag{4.4}$$

4. Half-bridge models with switching-node capacitance and self-commutated reverse conduction

Constants A and B are determined by initial conditions. Assume at $t = 0$, $i_{\mathrm{L}} = i_{\mathrm{L0}}$, $v_{\mathrm{m}} = v_{\mathrm{m0}}$:

$$\begin{cases} A = i_{\mathrm{L0}}, \\ B = \frac{v_{\mathrm{m0}} - V_{\mathrm{o}} - R i_{\mathrm{L0}} - \alpha i_{\mathrm{L0}} L}{L\omega}. \end{cases} \tag{4.5}$$

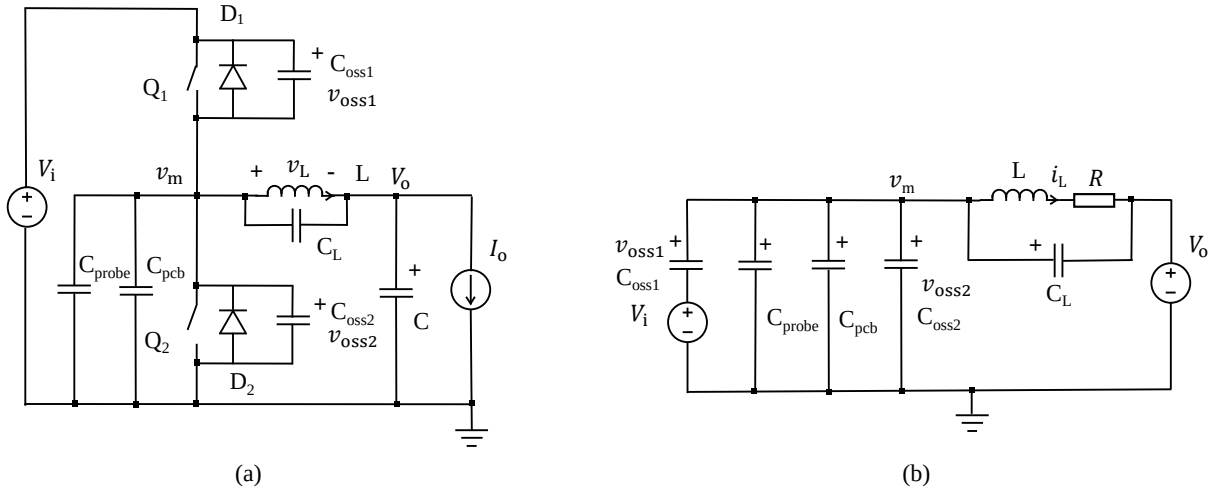


Figure 4.1: (a) The Model 2, a half-bridge model with fixed C_{oss}. This figure is the same as Fig. 1.16, apart from the fact that C_{oss} has a fixed value. (b) A simplified equivalent circuit of (a). Note that a resistor R is included in the SSM to present the decrease of voltage and current amplitude over time.

Based on this equation, the output capacitor C_{oss} can be calculated by finding f_{m}. Fig. 4.2 shows the gate signals that are fed directly into the half-bridge, which is used in the experiment, to measure f_{m}. The rising-edge dead-time is set as 3τ such that a sufficient amount of time is guaranteed to see the oscillation of v_{m}. Fig. 4.3 shows the measured waveforms with the oscilloscope, using the same setting as that in Chapter 3. Three periods of oscillation are captured. The averaged $f_{\mathrm{m}} = 588$ kHz. The inductor used for this particular measurement is $L = 107\,\mu$H. The impedance analyzer, PSM1735 N4LN, measures $C_{\mathrm{L}} = 45$ pF. Therefore, $C_{\mathrm{oss}} = 284$ pF. As the output capacitor C_{oss} is independent from the inductor, the fact that $C_{\mathrm{oss}} = 284$ pF holds for $L = 17\mu$H in the experiment described in Chapter 3. During the dead-time, the source-to-drain voltage of the transistor is approximated 2.3 V ($v_{\mathrm{bd}} \approx 2.3$ V), which is measured by the oscilloscope.

The charging and discharging of C_{oss} during the dead-time impacts the behaviour of v_{m} and i_{L}. Cases where C_{oss} charges or discharges during the dead-time are

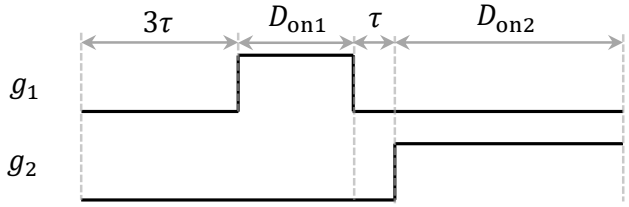


Figure 4.2: Gate signals to the half-bridge in Fig. 4.1 (a). The dead-time manager in the MCU is not activated, and so g_1 and g_2 shown here are applied directly to the half-bridge chip EPC23104. $\tau = 0.1$, $D_{\text{on1}} = 0.2$, $D_{\text{on2}} = 0.4$. $f_{\text{sw}} = 50$ kHz.

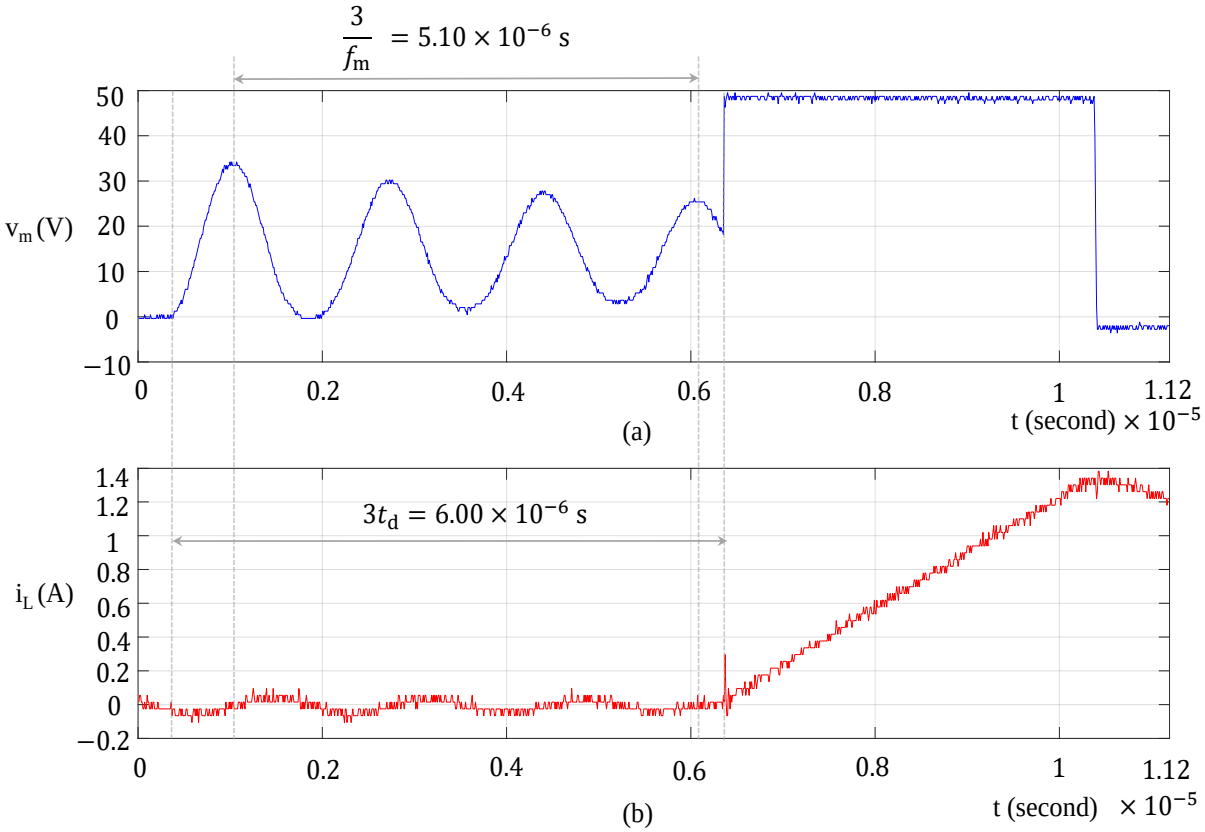


Figure 4.3: Waveforms of v_{m} and i_{L} when the gate signals are the ones in Fig. 4.2. Oscillations occur in the rising-edge dead-time.

divided into two categories. Each category has two situations. Two transistors exist in a half-bridge, Q_1 and Q_2. The symbol Q refers to one of the switches; The other switch is $\overline{Q}$. The output capacitor of one switch is C_{oss}; the capacitor of the other switch is $\overline{C_{\text{oss}}}$. The middle point voltage v_{m} only has two voltage levels when a switch is on, either 0 or V_{i}. The symbol V_{m} refers to one voltage level. The other voltage level is $\overline{V_{\text{m}}}$.

Category #1

4. Half-bridge models with switching-node capacitance and self-commutated reverse conduction

In this category, the direction of i_{L} changes at the beginning of the dead-time. When a transistor, Q, is on, the inductor current i_{L} flows through Q. $v_{\mathrm{m}} = V_{\mathrm{m}}$, where $V_{\mathrm{m}} \in \{V_{\mathrm{i}}, 0\}$. At the beginning of the dead-time, the current i_{L} transitions and flows into the body diode of the other transistor, $\overline{Q}$. Therefore, the current i_{L} charges the output capacitance of Q, and discharges the output capacitance of $\overline{Q}$, $\overline{C_{\mathrm{oss}}}$, until $v_{\mathrm{m}} = \overline{V_{\mathrm{m}}} - v_{\mathrm{bd}}$. Based on (4.1), the time it takes for v_{m} to change from V_{m} to $(\overline{V_{\mathrm{m}}} - v_{\mathrm{bd}})$, t_{c}, is calculated.

- **Situation #1**

If $t_{\mathrm{c}} < t_{\mathrm{d}}$, at the end of t_{c}, the middle point voltage v_{m} becomes $(\overline{V_{\mathrm{m}}} - v_{\mathrm{bd}})$. During the time period of t_{c}, the voltage v_{m} and the current i_{L} oscillate. Then, the current i_{L} flows through the body diode of $\overline{Q}$.

- **Situation #2**

If $t_{\mathrm{c}} \geq t_{\mathrm{d}}$, the voltage v_{m} cannot become $(\overline{V_{\mathrm{m}}} - v_{\mathrm{bd}})$. The current i_{L} charges C_{oss} and discharges $\overline{C_{\mathrm{oss}}}$ until the end of the dead-time. Oscillation in v_{m} and i_{L} are observed.

Category #2

In this category, the direction of i_{L} does not change at the beginning of the dead-time. When a transistor, Q, is on, the current i_{L} flows through Q. $v_{\mathrm{m}} = V_{\mathrm{m}}$, where $V_{\mathrm{m}} \in \{V_{\mathrm{i}}, 0\}$. At the beginning of the dead-time, the current i_{L} flows through the body diode of Q. During the dead-time, the current i_{L} becomes zero at a time instant, t_{o}. Then i_{L} charges C_{oss} and discharge $\overline{C_{\mathrm{oss}}}$ until $v_{\mathrm{m}} = \overline{V_{\mathrm{m}}} - v_{\mathrm{bd}}$. Based on (4.1), the time it takes for v_{m} to change from V_{m} to $(\overline{V_{\mathrm{m}}} - v_{\mathrm{bd}})$, t_{c}, is calculated.

- **Situation #1**

If $t_{\mathrm{c}} < (t_{\mathrm{d}} - t_{\mathrm{o}})$, at the end of t_{c}, the middle point voltage v_{m} becomes $(\overline{V_{\mathrm{m}}} - v_{\mathrm{bd}})$. During the time period of t_{c}, the voltage v_{m} and the current i_{L} oscillate. Then, the current i_{L} flows through the body diode of $\overline{Q}$.

- **Situation #2**

If $t_{\mathrm{c}} \geq (t_{\mathrm{d}} - t_{\mathrm{o}})$, the voltage v_{m} cannot become $(\overline{V_{\mathrm{m}}} - v_{\mathrm{bd}})$. The current i_{L} charges C_{oss} and discharges $\overline{C_{\mathrm{oss}}}$ until the end of the dead-time. Oscillation in v_{m} and i_{L} are observed.

Based on these categories, the exact waveforms of v_{m} and i_{L} during the dead-time with fixed C_{oss} can be calculated analytically. Fig. 4.4 shows an algorithm to find these waveforms.

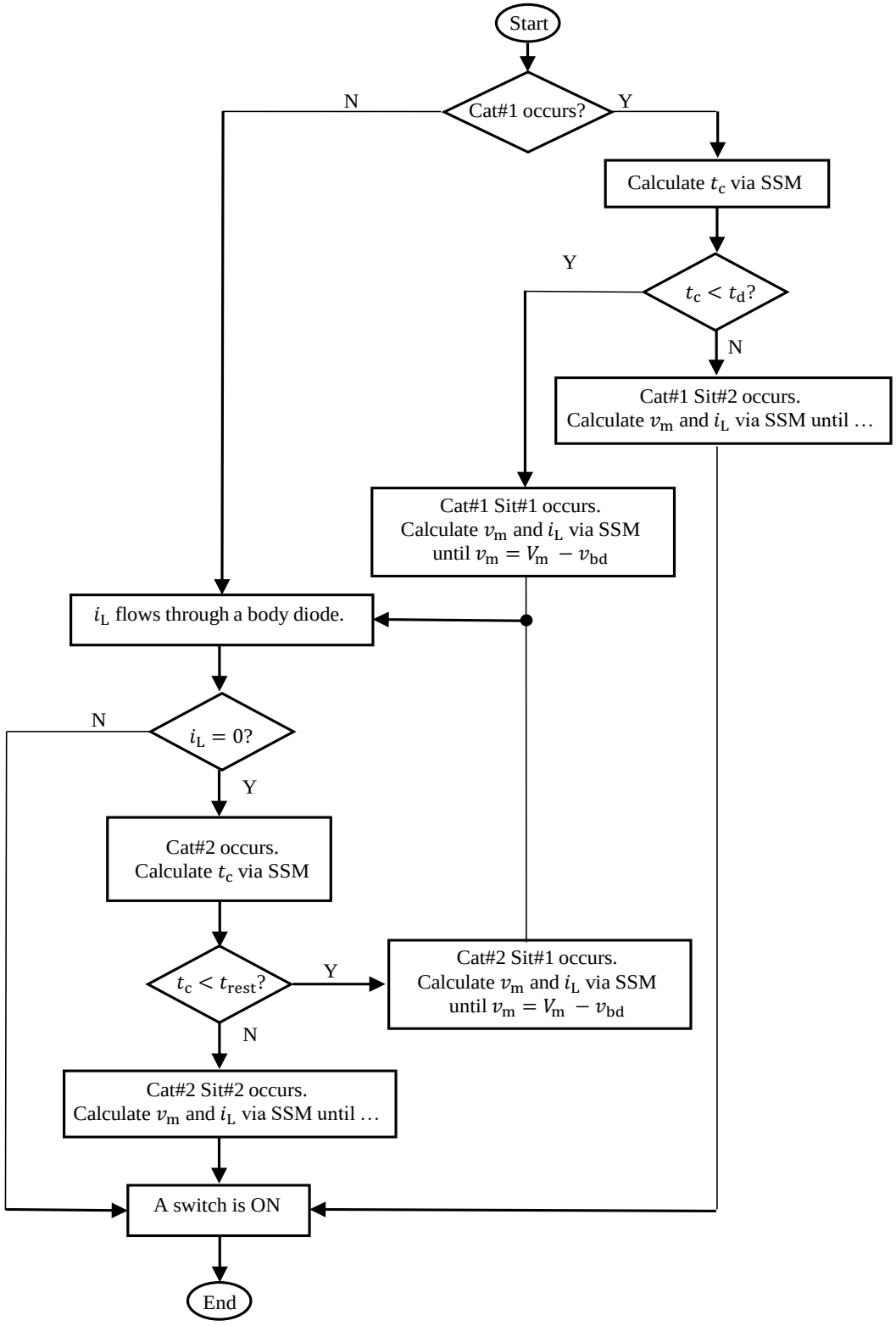


Figure 4.4: An algorithm to find the exact waveforms of v_m and i_L during the dead-time in the Model 2 as shown in Fig. 4.1. SSM is described by (4.1). The symbol t_rest refers to the rest of the dead-time.

The same 15,500 cases measured in the experiment in Chapter 3 are simulated. The half-bridge circuit in Fig. 4.1 (a) is built in the PLECS (Version 4.7.3, blockset), as shown in Fig. A.1 Appendix A. Table 4.1 lists the key parameters. The source-to-drain voltage of power FETs during the dead-time, v_{bd}, is modelled as the forward voltage of diode $\mathrm{D_1}$ and $\mathrm{D_2}$, assuming the source-to-drain voltage is fixed. The number of switching cycles that are simulated is $\mathrm{N_{sim}}$. The sampling time is $\mathrm{T_s}$. The mean value of the simulated output voltage is V_{o}. It is sampled during the last switching cycle. Appendix A presents more details on this simulation.

Table 4.1: Key specifications in the simulation of the Model 2.

parameters	value
f_{sw}	50 kHz
τ	0.1
L	17 μH
C	80 μF
$\mathrm{C_{pcb}}$ || $\mathrm{C_{probe}}$	70.5 pF
$\mathrm{C_L}$	38 pF
v_{bd}	2.3 V
$\mathrm{N_{sim}}$	350
$\mathrm{T_s}$	4×10^{-8} s

The difference between the simulated conversion ratio, M_{sim}, and the measured one, M_{meas}, is:

$$\Delta M = M_{\mathrm{meas}} - M_{\mathrm{sim}}. \tag{4.6}$$

Fig. 4.5 shows its absolute value, $|\Delta M|$.

Compared with the results of the Model 1 in Fig. 3.9, in $\mathrm{C_p}$ and $\mathrm{C_{0p}}$, cases with $|\Delta M| \in [0.01, 0.02]$ in the Model 1 have $|\Delta M| \leq 0.01$ in the Model 2. Almost half cases in $\mathrm{D_p}$ have $|\Delta M| \in [0.01, 0.03]$ in the Model 1. Model 2 has $|\Delta M| \leq 0.02$, and cases with these errors are restricted to a much smaller area. Operating modes $\mathrm{C_0}$ and $\mathrm{C_{np}}$ have $|\Delta M| \leq 0.01$ in both models. The operating mode $\mathrm{D_{1n}}$ has more areas where $|\Delta M| \in [0.01, 0.03]$. In the operating mode $\mathrm{D_{2p}}$, a small group of cases with $|\Delta M| \in [0.03, 0.05]$ still exists. Other areas, apart from this group, have $|\Delta M| \leq 0.02$, and cases with these errors are also restricted to a much smaller area.

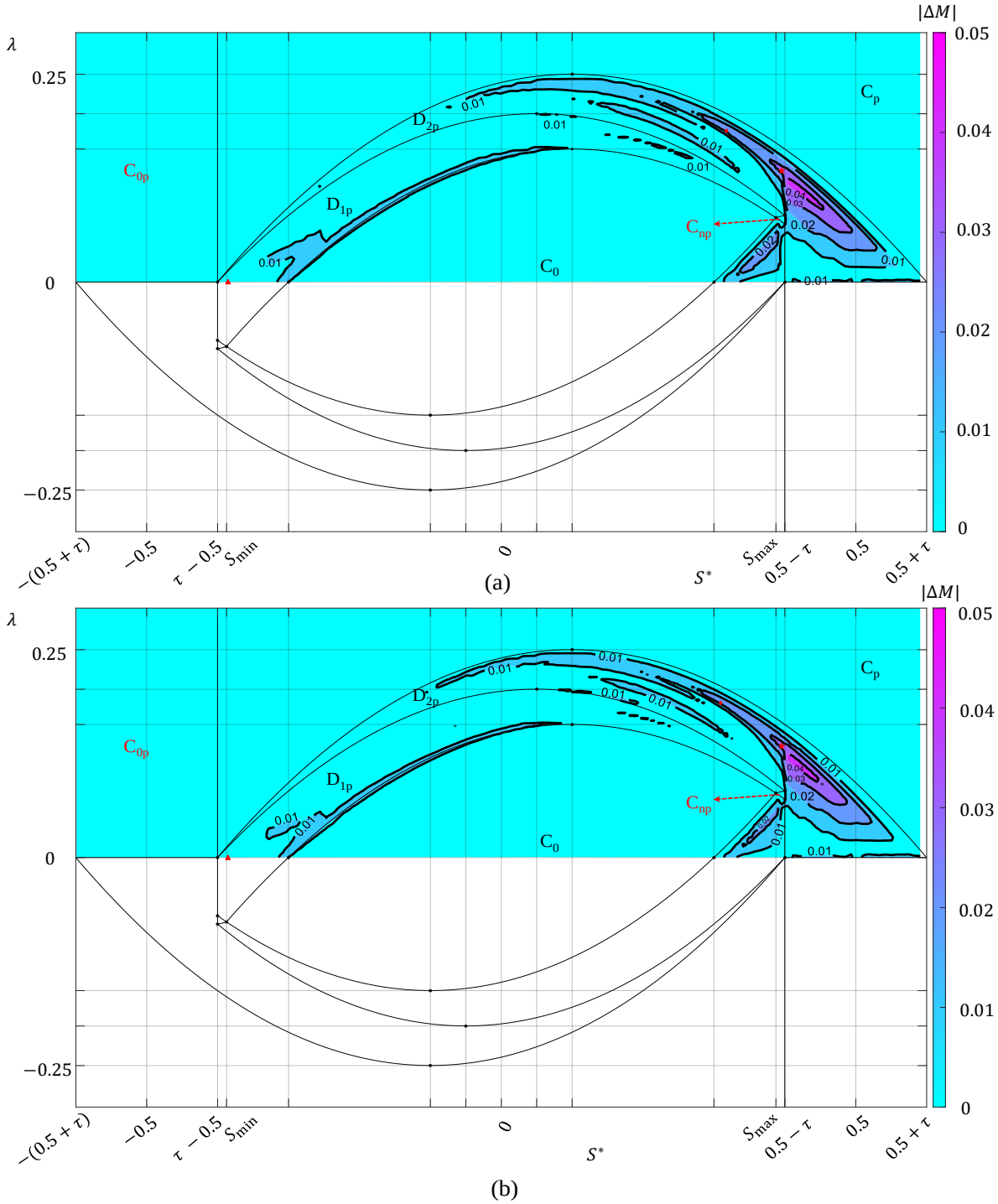


Figure 4.5: The same 15500 cases measured in the experiment are simulated. Case I and Case II are highlighted. Case III is highlighted as a red square in D_{2p}. Table 4.1 shows the parameters. (a) Simulation of Model 2. $C_{oss} = 284$ pF.(b) Simulation of Model 3. c_{oss} varies based on the piecewise function in Fig. 4.6.

4.2 A half-bridge model with variable output capacitance and self-commutated reverse conduction

The simulated results of Model 2, shown in Fig. 4.5 (a), illustrate that adding fixed parasitic capacitors and a fixed voltage drop during the dead-time to Model 1 can reduce $|\Delta M|$. In most cases where $|\Delta M| \leq 0.03$ in Model 1, $|\Delta M| \leq 0.02$ in Model 2. Model 3 approximates c_{oss} as a function of v_{ds}, and investigates the impact of a variable c_{oss} on the output voltage of a half-bridge.

The same half-bridge is built in the PLECS as that in Fig. A.1. The same method is used to generate gate signals as described in Section 4.1. The same cases measured in the experiment are simulated.

Fig. 3.13 (a) shows the variation of c_{oss} against v_{ds}. That curve is divided into 8 intervals based on the range of v_{ds}, as shown in Fig. 4.6. Values of c_{oss1}

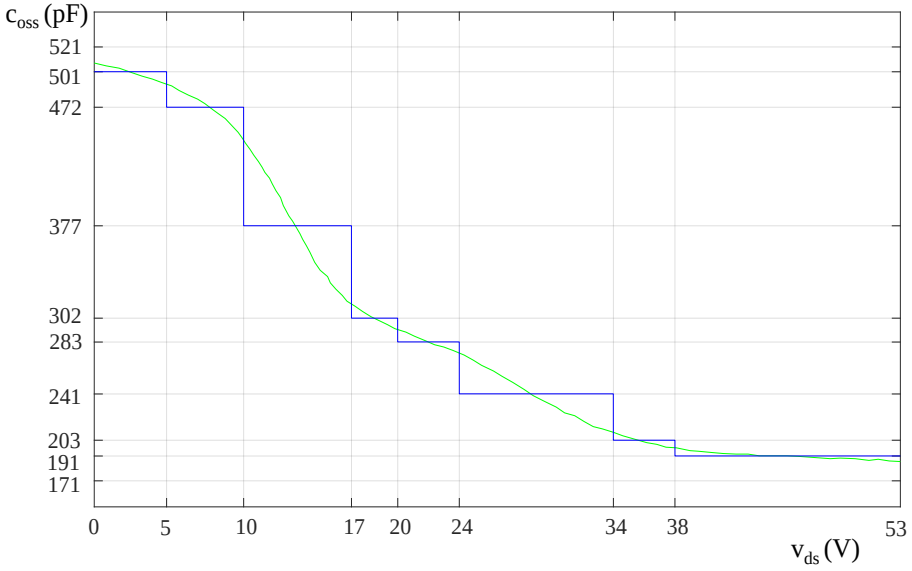


Figure 4.6: Variation of c_{oss} as a function of v_{ds}. The green one is the c_{oss} of each power FET of EPC23104, same as Fig. 3.13 (a). It is divided into 8 intervals based on the range of v_{ds}, as shown in the blue one. This piecewise function is implemented in PLECS to find the value of c_{oss1} and c_{oss2} in this simulation.

and c_{oss2} are found based on the value of their v_{ds} according to their relationship described by this piecewise function. Fig. 4.5 (b) demonstrates $|\Delta M|$ in this simulation with variable c_{oss} (see (4.6)).

4. Half-bridge models with switching-node capacitance and self-commutated reverse conduction

Compared with Fig. 4.5 (a), no significant differences are demonstrated after the output capacitor c_{oss} is changed from a fixed value to a variable that is a function of v_{ds}.

Fig. 4.7 shows waveforms of Case I in the simulation of Model 3. A comparison among the waveforms derived from the theory of Model 1 (blue curve), waveforms measured in the experiment (red curve), waveforms simulated in Model 2(black curve) and waveforms simulated in Model 3 (green curve) is demonstrated. The green and black curves almost overlap in Fig. 4.7 (a) (c). The sampling discretion observed in the measurement is due to the quantisation of the 8-bit ADC of the oscilloscope. For example, the discretion in the waveform of V_o is roughly 0.2 V. The scope of the ADC is $0.2 \times 2^8 = 51.2$ V. This is the voltage range that this oscilloscope captures, which is slightly larger than the input voltage $V_i = 48$ V.

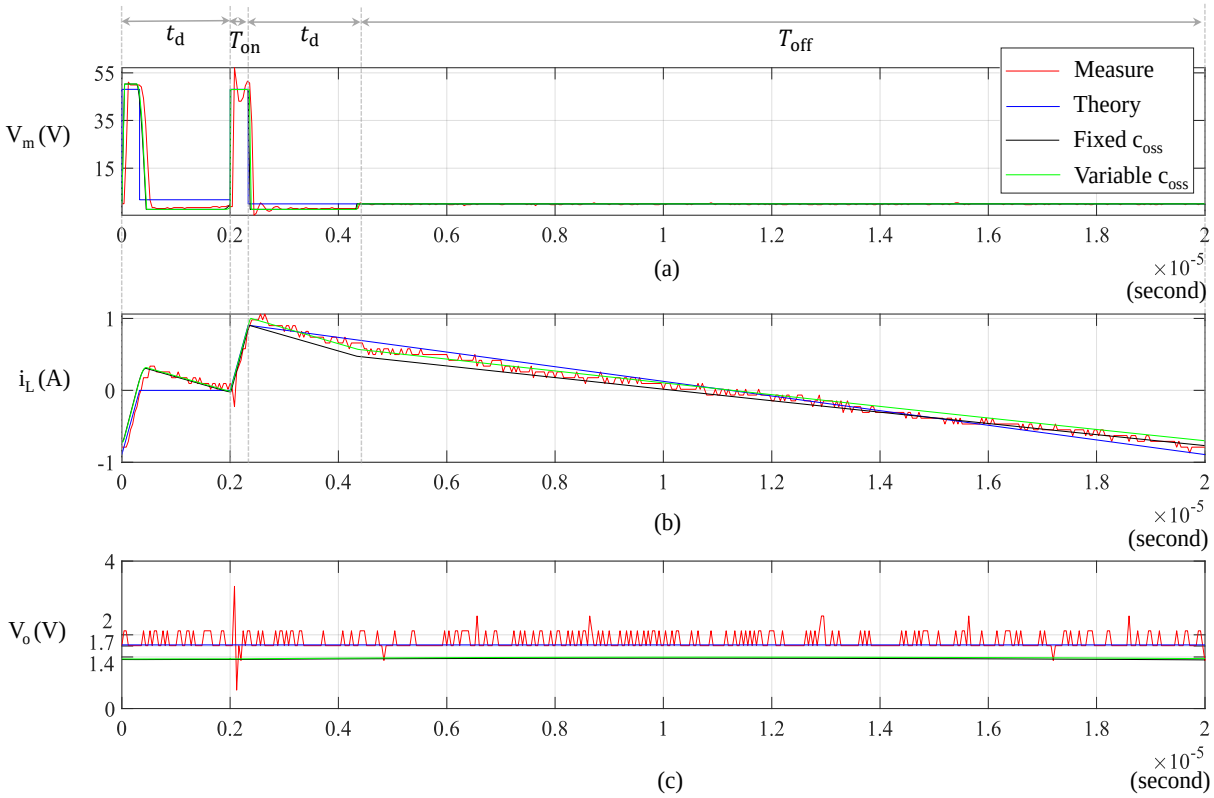


Figure 4.7: Waveforms of Case I in Model 3 simulation. (a) middle-point voltage. (b) inductor current. (c) output voltage. $t_d = 2$ μs, $T_{on} = 0.33$ μs, $T_{off} = 15.67$ μs. Fig. 3.10 only shows the measured and theoretical waveforms of the same case.

Similarly, Fig. 4.8 shows waveforms of Case II. The green and black curves almost

overlap in Fig. 4.8 (a) (c) also. The large c_{sw}, which causes $|\Delta M| \geq 0.03$ in $\mathrm{D_{2p}}$, does not come from c_{oss} or the voltage drop across the transistor during the dead-time.

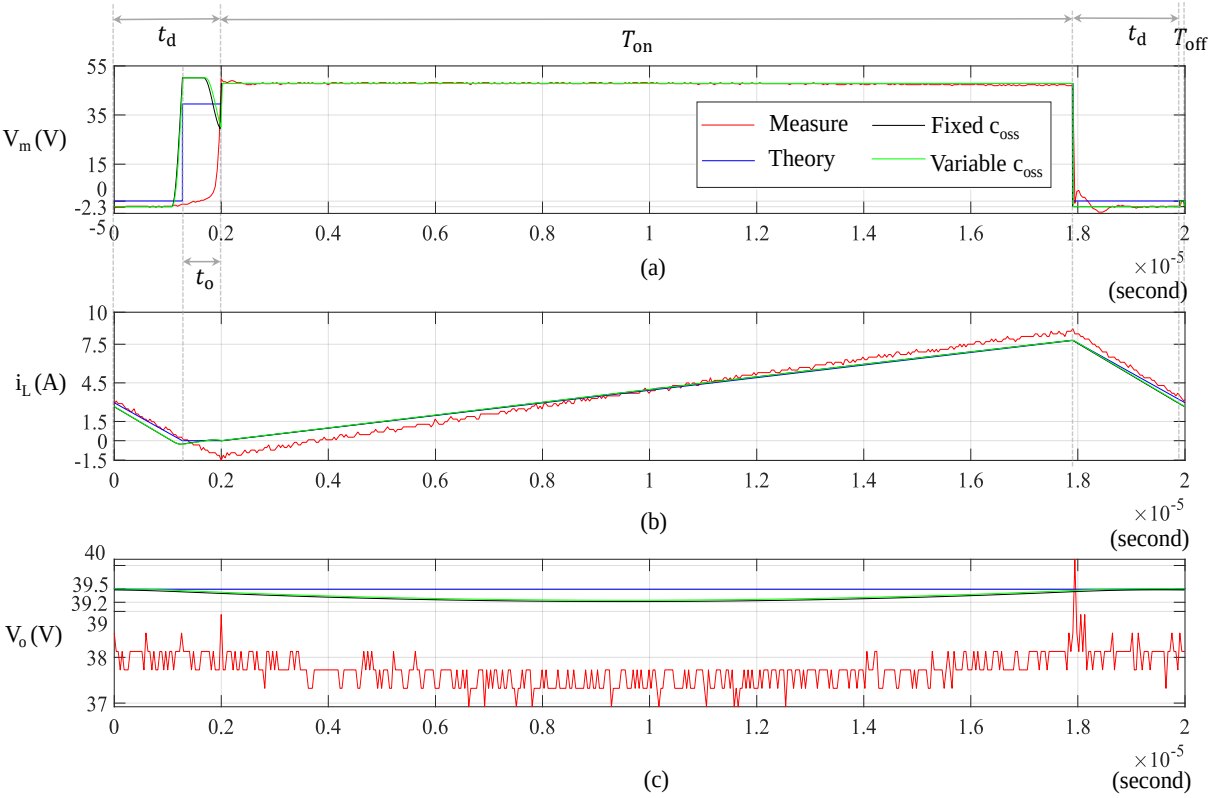


Figure 4.8: Waveforms of Case II in Model 3. (a) middle-point voltage. (b) inductor current. (c) output voltage. $\mathrm{t_d} = 2\ \mu$s, $\mathrm{T_{on}} = 15.9\ \mu$s, $\mathrm{T_{off}} = 0.1\ \mu$s. Fig. 3.12 only shows the measured and theoretical waveforms of the same case.

4.3 Investigation of the bootstrap capacitor

Fig. 4.5 illustrates that the parasitic capacitors in the power circuit of the half-bridge, including c_{oss}, C_{L}, C_{pcb} and C_{probe}, are not the dominant contributor to the switching capacitance that leads to $|\Delta M| \geq 0.03$ in the region in $\text{D}_{2\text{p}}$. Fig. 3.13 (c) shows that the switching node capacitor c_{sw} are as large as 76 nF when the middle point voltage v_{m} is near zero, which outweighs the parasitic capacitance in the power circuit.

Apart from the capacitors from the power circuit, capacitors from the gate driver circuit may also contribute to c_{sw}. Fig. 3.3 shows the simplified bootstrap circuit of the half-bridge. The capacitors that connect to the switching points include C_{boot} and output capacitors of the transistors in the bootstrap circuitry. The output capacitance of transistors in the bootstrap circuitry is not the dominant contributor to the large switching capacitance because its value is completely negligible compared with the total parasitic capacitor from the power circuit. Therefore, the hypothesis is that the bootstrap capacitor, C_{boot}, contributes to this large c_{sw}. In the rest of this section, an investigation of the validation of this hypothesis from literature review, experimental measurement and simulation is illustrated.

4.3.1 Study review

The EPC23104 chip uses a GaN FET as the synchronous bootstrap FET, Q_{SB} [89]. Few publications report this similar phenomenon in this synchronous bootstrap structure. Only a study [99] points out that the bootstrap capacitor C_{boot} charges and discharges during the dead-time. The operation of this gate drive is explained as follows. A level-shift circuit switches Q_{SB} as shown in Fig. 4.9. The source of Q_{SB} connects to V_{cc}, and the drain connects to C_{boot}. The level-shift, consisting of D_{ls} and C_{ls}, steps up the gate signal of Q_2, g_2, and so the voltage applied to the gate of Q_{SB} is: $v_{\text{gls}} = V_{\text{g2}} + V_{\text{cc}} - V_{\text{f}}$, where V_{f} is the forward voltage of D_{ls}, V_{g2} is the voltage value of g_2. When the transistor Q_2 is on (g_2 is logic high), $v_{\text{gls}} > v_{\text{dsq}}$. The transistor Q_{SB} self-commutates which enables V_{cc} charge C_{boot}. To have C_{boot} charged by V_{cc}, two

inequalities have to be satisfied: (i) the source-to-drain voltage of Q_{SB}, V_{sdsb}; (ii) v_{gls}:

$$\begin{cases} v_{dsq} \leq V_{cc} - V_{sdsb}, \\ v_{dsq} \leq v_{gls} = V_{g2} + V_{cc} - V_f. \end{cases} \tag{4.7}$$

When Q_2 is off (g_2 is logic low), the gate voltage, $v_{gls} = V_{cc} - V_f$, is less than the source voltage, V_{cc}. Therefore, the transistor Q_{SB} cannot conduct the current from the drain to its source. The capacitor C_{boot} cannot discharge through Q_{SB}.

Study [99] employs three diodes as D_{ls} with $i_L > 0$. These diodes have $V_f = 0.3, 0.7, 1.2$ V respectively. The current through the bootstrap capacitor i_{boot}, v_{boot}, and v_m are measured, as shown in Fig. 4.10. When Q_1 is on, the capacitor C_{boot} discharges. At the falling-edge dead-time, around 5-10 ns in Fig. 4.10, the current i_L flows through D_2 and so the middle point voltage v_m becomes negative. The voltage at the drain terminal of Q_{SB}, v_{dsq}, decreases: $v_{dsq} = V_{boot} - |v_m|$. The gate voltage becomes $v_{gls} = V_{cc} - V_f$. When $v_{gls} > v_{dsq}$, the transistor Q_{SB} conducts and v_{CC} charges C_{boot}. A negative spike occurs at the end of the dead-time. The author explains that when _m transitions from negative to zero, the current i_{boot} flows through the C_{oss} of Q_{SB}.

When Q_2 is on, around 10 - 52 ns in Fig. 4.10, the gate voltage becomes greater than the voltage at the drain terminal ($v_{gls} = V_{g2} + V_{cc} - V_f > v_{dsq}$). Therefore, the power supply V_{cc} charges C_{boot}. The maximum value of v_{dsq} is v_{gls}. Therefore, the greater V_f is, the smaller v_{dqs} becomes at the steady state.

At the rising-edge dead-time, around 52 - 60 ns in Fig. 4.10, the voltage v_m becomes negative. When V_f equals 1.2 V, the gate voltage v_{gls} is relatively smaller than the circuit with other diodes. Therefore, the transistor Q_{SB} does not conduct in the circuit with a forward voltage drop of 1.2 V in the diode. A similar negative spike in i_{boot} occurs for all the diodes. The same explanation for the spikes in the falling-edge dead-time is given.

Study [99] does not validate the hypothesis as it cannot explain why c_{sw} is as large as 76 nF in the experiment. Because the output capacitor c_{oss} of Q_{SB} is much smaller than the c_{oss} of power GaN FET Q_1 and Q_2. Therefore, the total capacitance from the gate side, i.e., the output capacitor c_{oss} of Q_{SB} in series

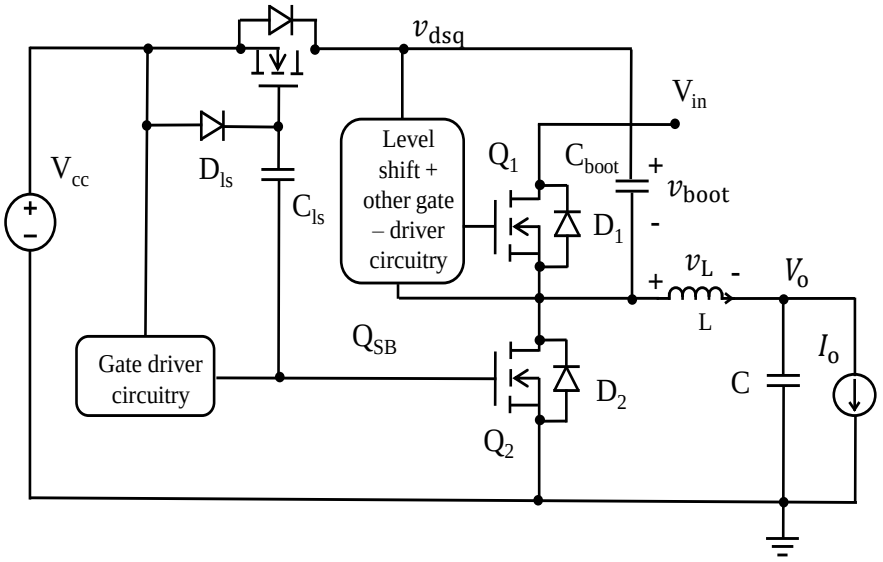


Figure 4.9: A simplified bootstrap circuit with a level-shift to switch a GaN synchronous bootstrap FET. This figure is reproduced from [99].

with C_{boot}, is much smaller than the capacitance from the power circuit. For example, the output capacitor c_{oss} of EPC2038 is 1.6 pF [100]. It can neither explain why this large c_{sw} only occurs in a certain group of cases in $\text{D}_{1\text{p}}$ instead of a general issue that every case has.

4.3.2 Experimental measurement

Fig. 4.11 shows the measured waveforms of v_{m}, v_{dsb}, v_{boot} and i_{L} of Case III, with $s = 0.3093$, $\lambda = 0.19$ ($I_{\text{o}} = 5.24$ A), $V_{\text{in}} = 47.89$ V, highlighted in Fig. 4.5 with a red square. Fig. 4.12 shows the waveforms of the same case without the DC-DC converter attached to C_{boot}. This large c_{sw} is observed in both figures. It illustrates that the DC-DC converter does not cause this large c_{sw}. A similar map with a group of cases where $|\Delta M| \geq 0.03$ in $\text{D}_{2\text{p}}$ as that in Fig. 3.9 is observed when the converter is removed.

As shown in Fig. 4.11, v_{boot} varies very little over a switching cycle. Based on the measured waveforms, V_{boot} increases 0.7 V over 2×10^{-7} s during the rising edge of the dead-time. It suggests that the average current is 0.3 A for a 100 nF capacitor. However, the average of i_{L} over that period is greater than 0.3 A.

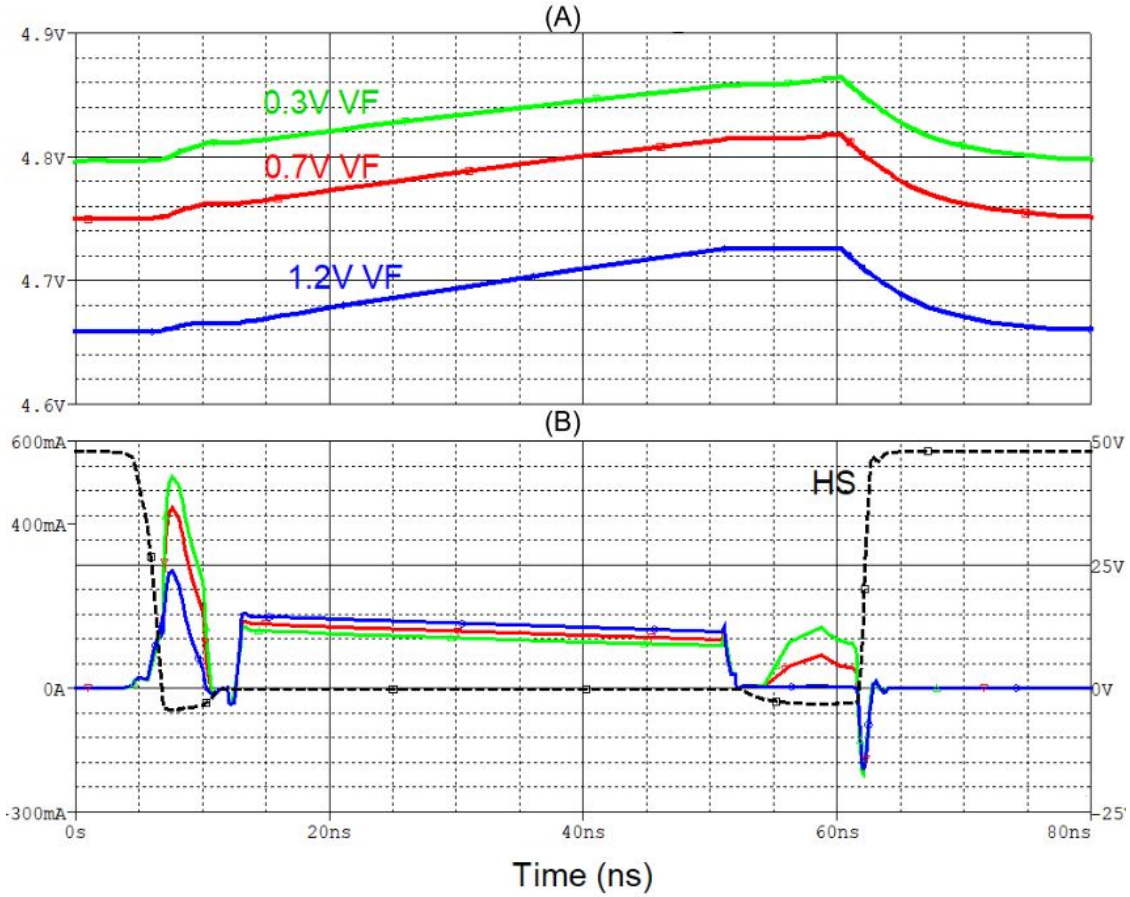


Figure 4.10: Captured waveforms of v_{boot}, i_{boot} and v_{m}. $i_{\text{L}} > 0$. (A) Waveforms of v_{boot} with three didoes with different V_{f} as D_{ls}. (B) Waveforms of i_{boot} (coloured) and v_{m} (dashed-balck). This figure comes from [99].

This experimental measurement does not support the argument that the bootstrap capacitor C_{boot} is the unknown contributor to c_{sw}. Also note that the voltage probe is not precise enough to capture such small variations, so these plots do not disclose useful information about whether the bootstrap capacitor C_{boot} charges and discharges during the dead-time and whether it contributes to c_{sw}.

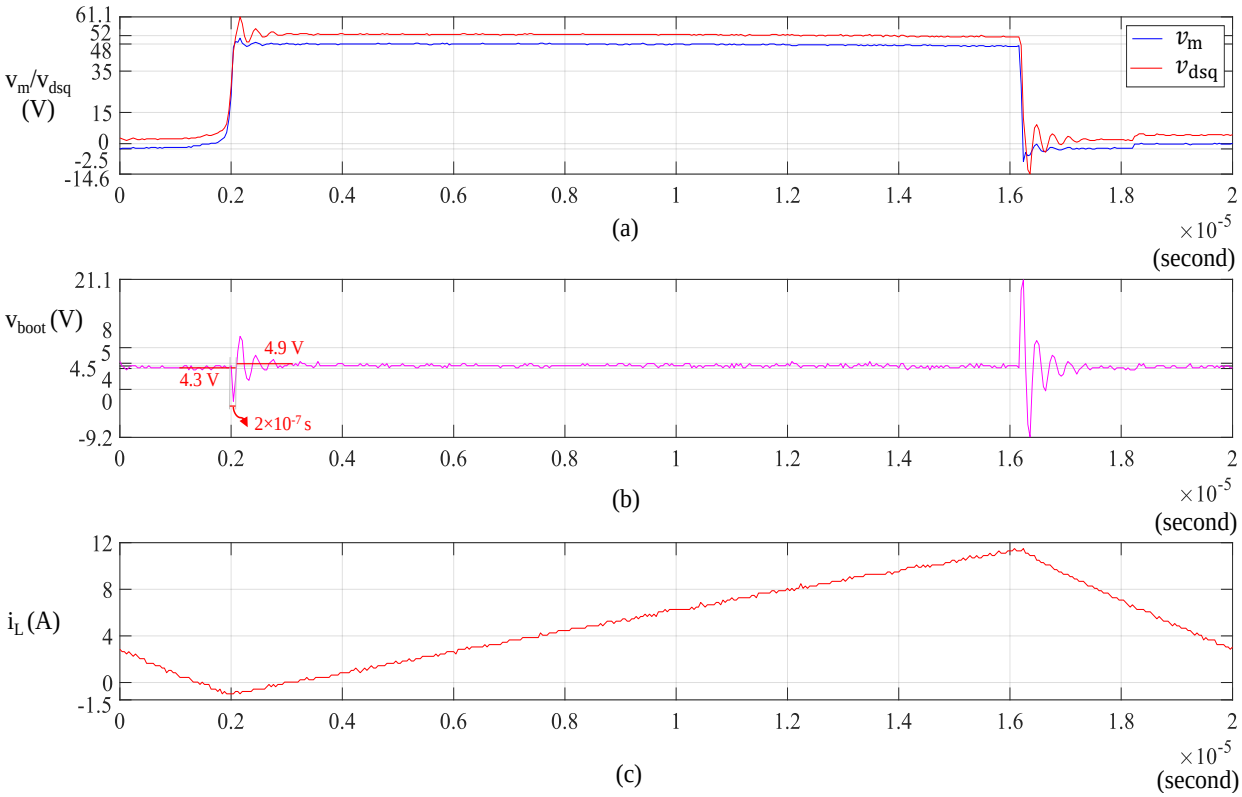


Figure 4.11: Waveforms of Case III, that is highlighted in red square in D_{2p} in Fig.4.5, with the DC-DC converter attached. $s = 0.3093$, $\lambda = 0.19$, $V_{in} = 47.89$ V. (a) Middle-point voltage (v_m) and the drain voltage of Q_{SB} (v_{dsq}). (b) The voltage across C_{boot}. It is obtained by subtracting v_m from v_{dsq}: $v_{boot} = v_{dsq} - v_m$. (c) inductor current.

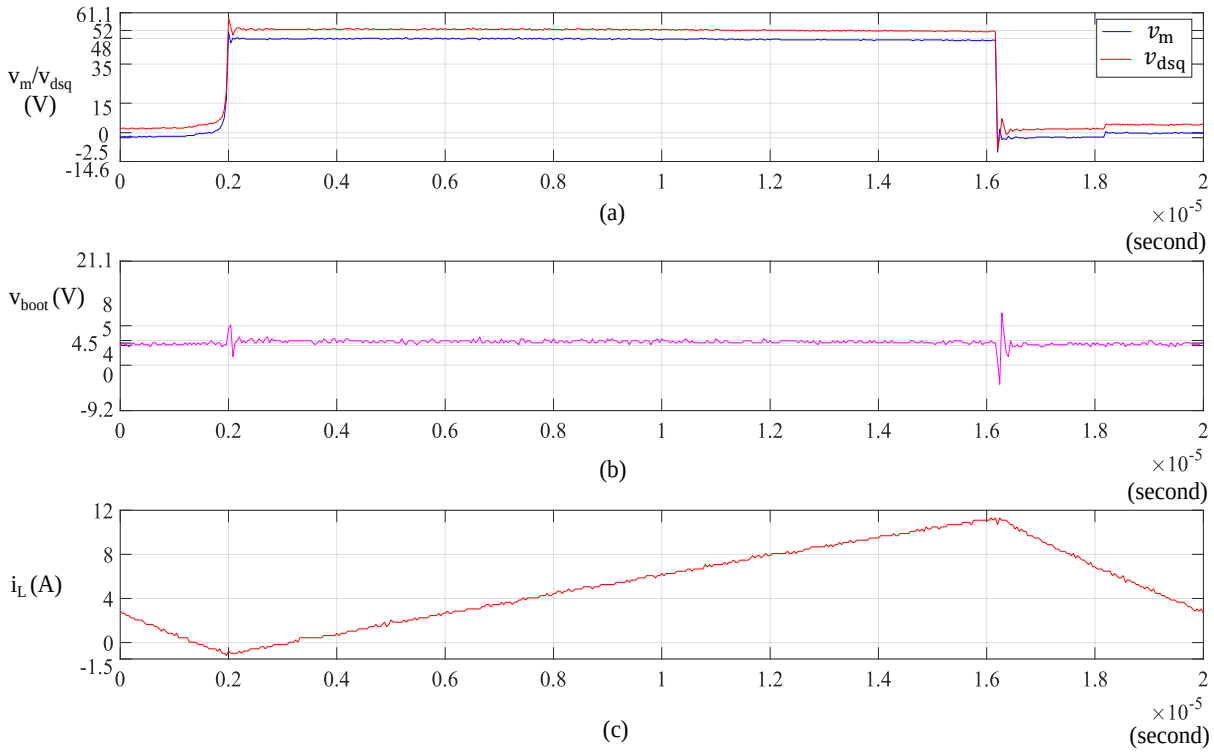


Figure 4.12: Waveforms of Case III, without the DC-DC converter attached. The voltage across the bootstrap capacitor v_{boot} is obtained by subtracting v_{m} from v_{dsq}: $v_{\text{boot}} = v_{\text{dsq}} - v_{\text{m}}$. Waveforms are similar to those in Fig. 4.10 when the DC-DC converter is attached.

4. Half-bridge models with switching-node capacitance and self-commutated reverse conduction

4.3.3 Simulation

To further explore the behaviour of C_{boot} during the dead-time, Case III is simulated with the LTspice model provided by EPC Co. in LTspice Version 17.1.8 [101]. The simulation circuit is based on Fig. 3.1 and the schematic of the EPC90125 [102]. Details are in Appendix B.

Fig. 4.13 shows the waveforms of v_{boot}, i_{boot} and v_{m}. The measured v_{boot} and v_{m} are also plotted as a comparison. The simulation does not demonstrate unexpectedly large c_{sw}.

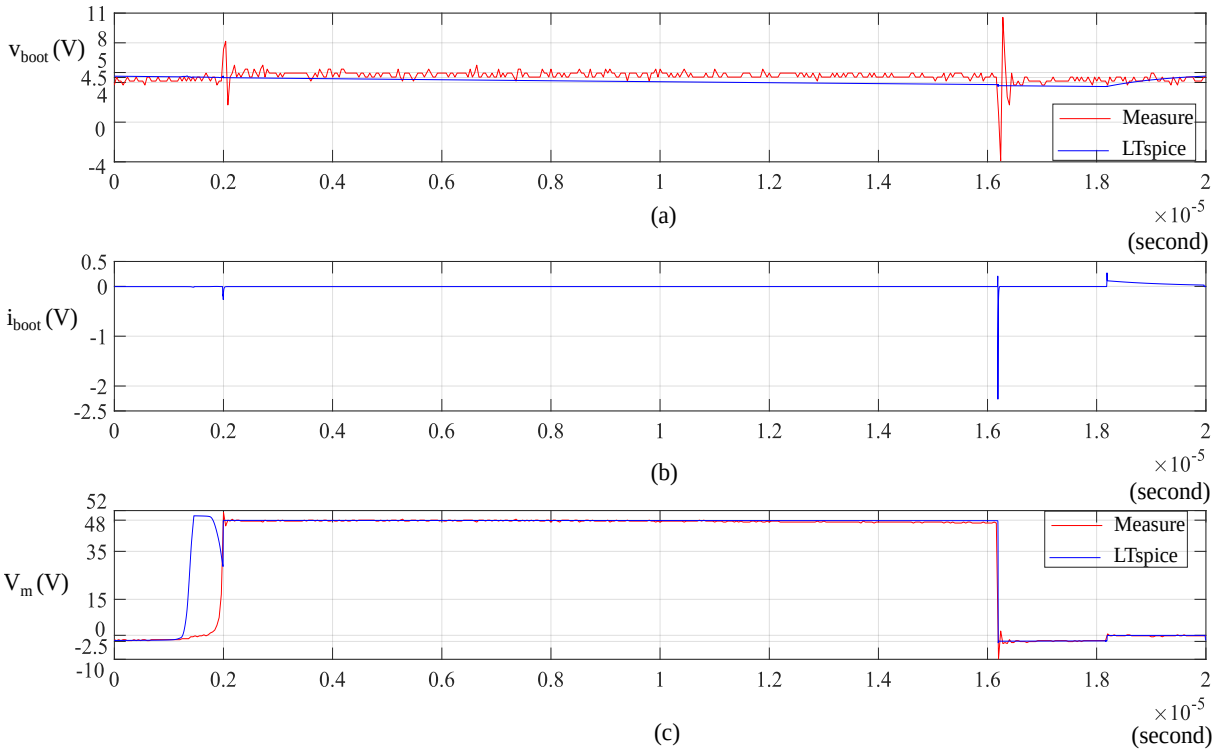


Figure 4.13: Simulated waveforms of Case III without the DC-DC converter (see Fig. 4.12) in LTspice. Fig. B.1 shows the simulation circuit. (a) Simulated v_{boot} in blue. The red one is the same waveform of v_{boot} in Fig. 4.12 (b). (b) Simulated i_{boot}. (c) Simulated v_{m} in blue. The red one is the same waveform of v_{m} in Fig. 4.12 (a).

Fig. 4.14 compares the waveforms of v_{m}, i_{L} and v_{o} in Case III that are (i) derived from Model 1 in the theory (see Chapter 2); (ii) measured from the experiment without the DC-DC converter; (iii) simulated in LTspice; (iv) simulated in PLECS in Model 2. As it shows, the simulated results from LTspice and PLECS are close to each other. The large c_{sw} is only observed in the measured waveforms.

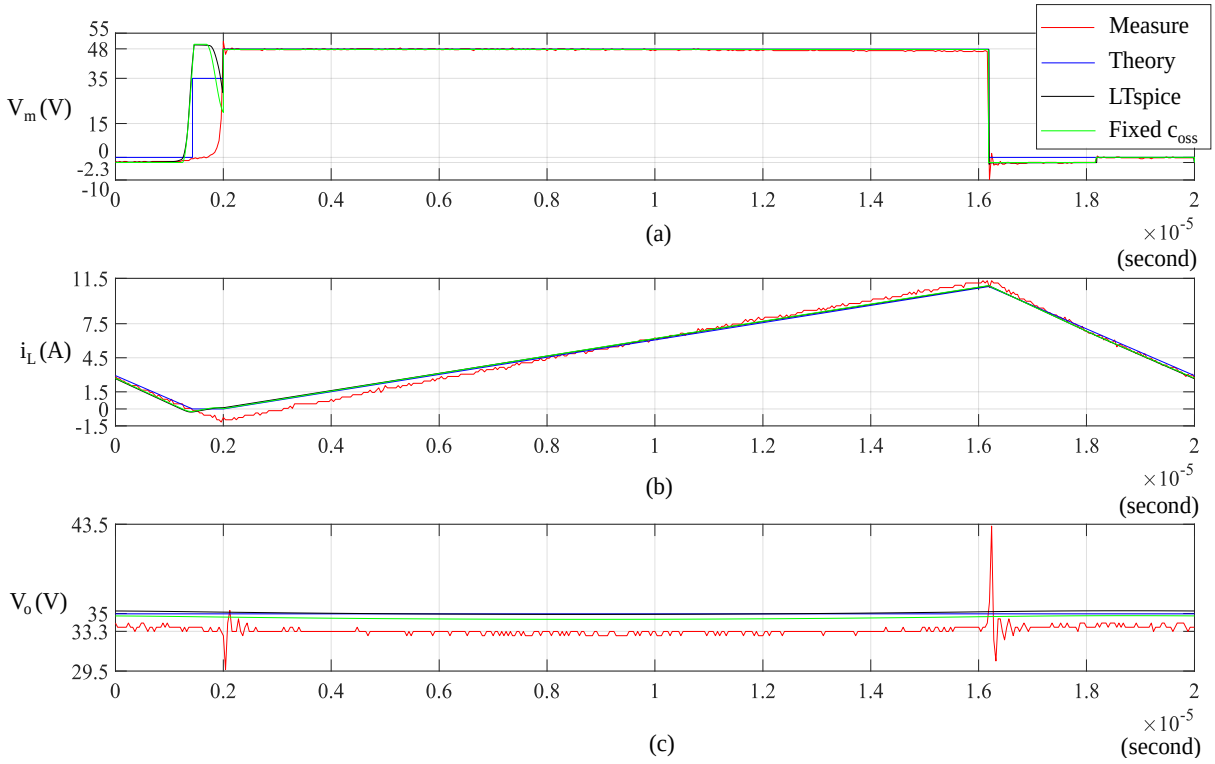


Figure 4.14: Waveforms of Case III, without the DC-DC converter. Measured waveforms are in red. Waveforms that are theoretically derived from Model 1 are in blue. Simulated waveforms from LTspice are in black. Simulated waveforms in Model 2 are in green. (a) Middle-point voltage. (b) Inductor current. (c) Output voltage.

4. Half-bridge models with switching-node capacitance and self-commutated reverse conduction

An external capacitor, C_{unk} = 100 nF, is added to the Model 2, where the output capacitor C_{oss} is constant, as shown in Fig. C.1, Appendix C. Case III is simulated. Waveforms from this simulation and measurement are compared in Fig. 4.15. These simulated waveforms match those measured at the rising-edge dead-time. However, in the falling-edge dead-time, the simulated v_m decreases slowly compared with the measured ones, which indicates that the capacitor C_{unk} disappears somehow. Case I is simulated in this circuit with C_{unk}. Fig. 4.16 compares the simulated waveforms with the measured ones. As it shows, they differ a lot. Compared with Fig. 3.10, the unexpectedly large c_{sw} does not appear in this case.

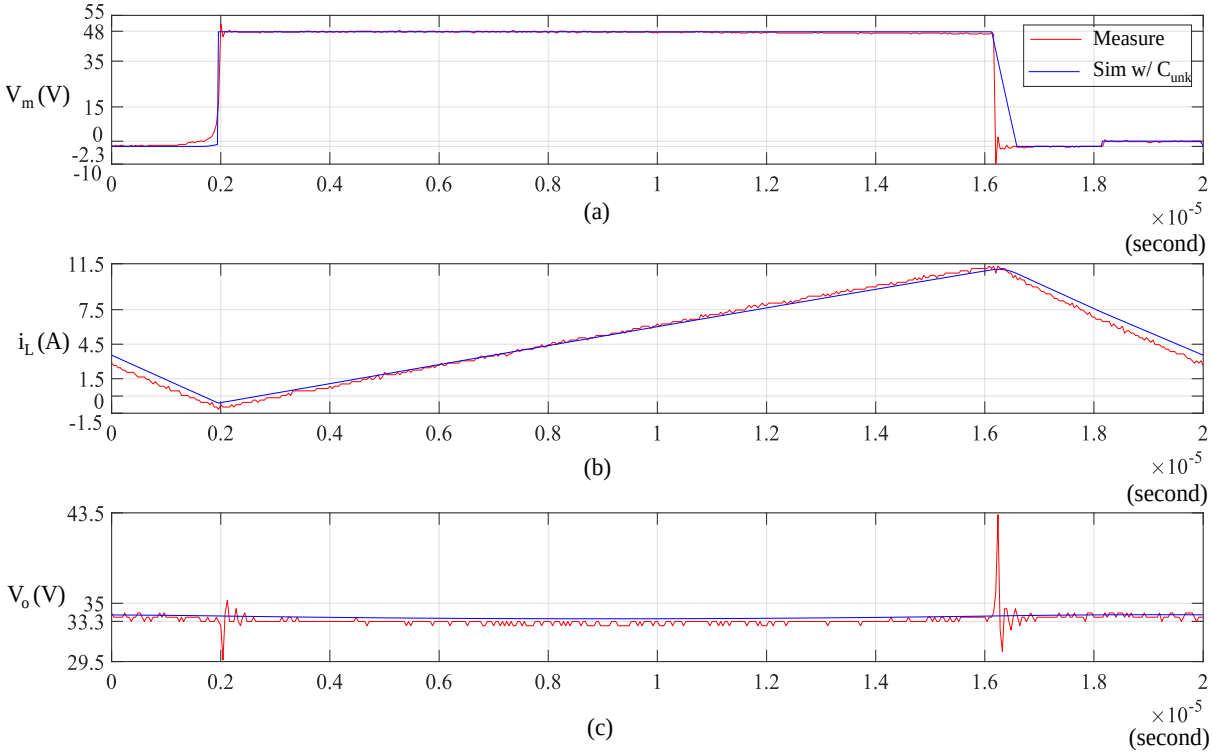


Figure 4.15: A comparison of measured waveforms of Case III without the DC-DC converter, and its simulated waveforms from the circuit in Fig. C.1 with C_{unk} = 100 nF. C_{oss} = 284 pF. (a) Middle-point voltage. (b) Inductor current. (c) Output voltage.

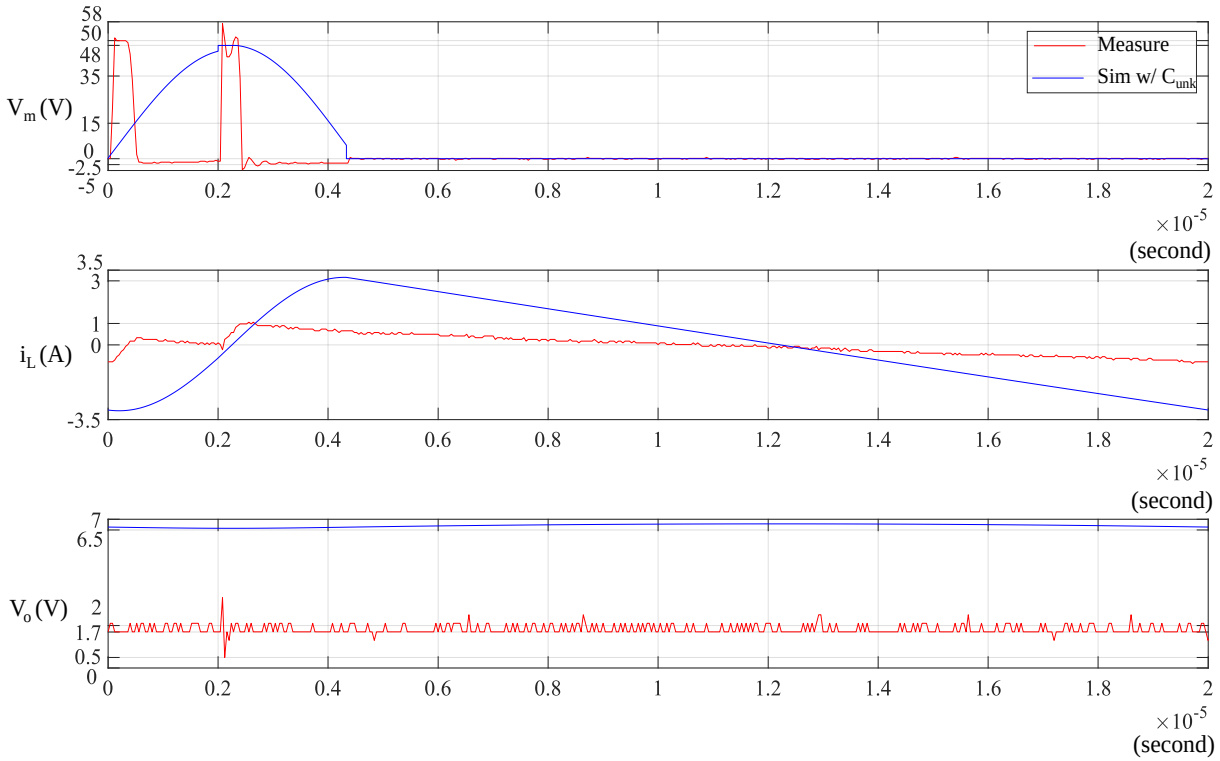


Figure 4.16: A comparison of measured waveforms of Case I, and its simulated waveforms from the circuit shown in Fig. C.1 with C_{unk} = 100 nF. C_{oss} = 284 pF. The simulated waveforms without C_{unk} in Fig. 4.7 match the measured waveforms much better than the ones here. (a) Middle-point voltage. (b) Inductor current. (c) Output voltage.

4. Half-bridge models with switching-node capacitance and self-commutated reverse conduction

Table4.2 compares errors of Case III and I in different models.

Table 4.2: Comparison of errors, $\Delta M = |M_{\text{sim}} - M_{\text{meas}}|$ for Case III and I in four models. In Model 1, $M_{\text{sim}} = M_{\text{thry}}$.

Model	Case III	Case I
1	0.029	0.005 (see Fig. 3.10)
2	0.023	0.003 (see Fig. 4.8)
3	0.023	0.003 (see Fig. 4.8)
4	0.004 (see Fig. 4.15)	0.107 (see Fig. 4.16)

4.3.4 Conclution

The hypothsis that the bootstrap capacitor C_{boot} cuases the large c_{sw} is proposed because

- the bootstrap capacitor C_{boot} is the only capacitor that connects to the switching point, apart from the output capacitors of transistors in the gate drive;
- $\text{C}_{\text{boot}} = 100$ nF and $c_{\text{sw}} \approx 76$ nF.

However, no validation is identified from the literature review, experimental measurements or simulation. It is possible that, for some unknown reason, the transistor Q_{SB} is turned on at the rising-edge of dead-time, and the inductor current i_{L} charges C_{boot} through Q_{SB}. This causes $|\Delta M| > 0.03$ in a specific region in D_{2p}. In other situations, the transistor Q_{SB} is off. This issue is left open for future exploration.

4.4 Conclusions

Based on the results and discussions presented in this chapter, the key conclusions are the following:

1. Model 2 includes C_{oss} with a fixed value, and the impact of SCRC, which is modelled as a diode in parallel with a transistor with a voltage drop of v_{th}. Four situations are identified based on whether i_{L} changes its direction (i)

at the beginning of the dead-time; (ii) during the dead-time. An analytical equation is developed to find i_{L} and v_{m}. An algorithm that considers the reiteration of the four situations is proposed. An analytical solution to find i_{L} and v_{m} during the dead-time is presented. Simulated results of Model 2 are demonstrated and compared with the experimental results. Model 2 reduces errors to 0.02 in most cases.

2. Model 3 includes a variable value of c_{oss}, which is a function of v_{ds}. similar results to those obtained with a fixed C_{oss} are observed.

3. A hypothesis that the bootstrap capacitor C_{boot} from the bootstrap circuit causes large c_{sw} is proposed. An investigation from literature review, experimental measurements and simulation is demonstrated. No validation of this hypothesis is identified.

5 Contributions and future studies

Throughout this thesis, a theoretical analysis of dead-time distortion, a proposed compensation method, along with experiments, is demonstrated to answer the research questions posed in Section 1.8. This chapter summarises the key contributions and presents avenues for future research within the topic of dead-time distortion.

5.1 Contributions

Presentation of a thorough analysis of the dead-time distortion for all the possible cases.

Because the switching frequency is much larger than the fundamental frequency, the output is approximated as a DC output over several consecutive switching cycles in SMPAs. All the possible continuous and discontinuous conduction modes caused by the current ripple on the inductor current in a half-bridge are identified through a thorough analysis. This analysis is conducted based on a half-bridge model (Model 1) with two assumptions: (i) ideal components; (ii) the small ripple approximation. The input signal, s, which describes all the cases, is used. There are eleven distinct operating modes, of which four are new. The analytical solutions of DC conversion ratios in Model 1 are presented, which are polynomial equations. Experimental results demonstrate that this model predicts the average output voltage to within a

few percent. The extensive data collected in the experiment illustrate that most cases have a deviation of less than 0.03 from the prediction of Model 1.

An accurate method of the compensating voltage near the zero-crossings is proposed.

This compensation method is proposed based on the thorough analysis of the dead-time distortion. The mathematical analysis shows that for all s and I_{o}, dead-time distortion can be removed, i.e., $V_{\mathrm{o}} \equiv V_{\mathrm{o}}^{*}$ always holds with the proposed compensating rule applied. When $\lambda \geq 0.25$ or $\lambda \leq -0.25$, for all s, dead-time distortion can be completely eliminated such that the compensated system behaves exactly the same as that of an ideal system, i.e., $\Delta v(t) \equiv 0$. When $\lambda \in [-0.25, 0.25]$, it cannot guarantee that the instantaneous voltage error is always zero ($\Delta v(t) \not\equiv 0$). This compensation method is validated by the experiment.

A comparison of this compensation method and three widely-used conventional ones is demonstrated.

Three widely-used conventional compensation methods, namely three-level ACM, two-level ACM and linear ACM, are compared with the proposed one. When τ is large, the proposed compensation rules agree with the linear ACM; when τ is small, the proposed compensation rules agree with the three-level ACM. The bilinear interpolation is deployed, based on the collected dataset, to find the compensated results of these compensation methods. It demonstrates that all the compensation methods reduce the maximum deviation from an ideal system, from 0.02 to 0.10, where $\tau = 0.1$. The proposed one reduces the deviation to 0.03 across all the operating modes. The three conventional ones increase errors in other regions. The maximum error after these compensation methods remains 0.10.

The impact of c_{sw} and SCRC to the dead-time distortion is investigated.

Two half-bridge models, Models 2 and 3, that consider c_{sw} and SCRC are proposed. Although an increased layer of complexity results in higher accuracy, computational

efforts also increase, and only numerical solutions are available. Model 2 includes C_{oss} with a fixed value. A state space model of the Model 2 during the dead-time is presented. The analytical equations to calculate v_{m} and i_{L} based on this state space model are presented, assuming initial values of v_{m} and i_{L} are known. Four situations are identified based on whether i_{L} changes its direction (i) at the beginning of the dead-time, (ii) during the dead-time. An algorithm that considers the reiteration of the four situations is provided to find the numerical solution of V_{o} of Model 2. Model 3 includes c_{oss} of a variable value as a function of v_{ds}. Simulated results of Models 2 and 3 are presented and compared to the measured ones. Model 2 further reduces errors compared to Model 1. Simulated results of Model 3 are very similar to those of Model 2.

The potential impact of the bootstrap capacitor from the gate drive is discussed.

A hypothesis that C_{boot} from the bootstrap circuit causes the large c_{sw} is proposed. The reason is that the bootstrap capacitor is the only capacitor connecting to the switching point with a similar value to that of the large c_{sw}. Few studies notice the charge and discharge of C_{boot} during the dead-time, except [99]. However, its conclusions cannot explain the large c_{sw} observed in the experiment. Waveforms related to the bootstrap capacitor are measured, which do not show whether the bootstrap capacitor is charged during the dead-time. The LTspice model of EPC23104 is simulated. This large c_{sw} is not observed. Model 4, which includes a capacitor of 100 nF to mimic the bootstrap capacitor, does not provide good agreement all the time with the measured waveforms. This issue is left for open discussion.

5.2 Discussion

Implementation of the proposed compensation to feedforward control
This study identifies voltage errors caused by dead-time distortion and proposes compensation rules to minimise its impact. The proposed compensation could be

integrated into a feedforward control, where the output current I_o and the inductor L are pre-known or predictable. Fig. 5.1 shows an example.

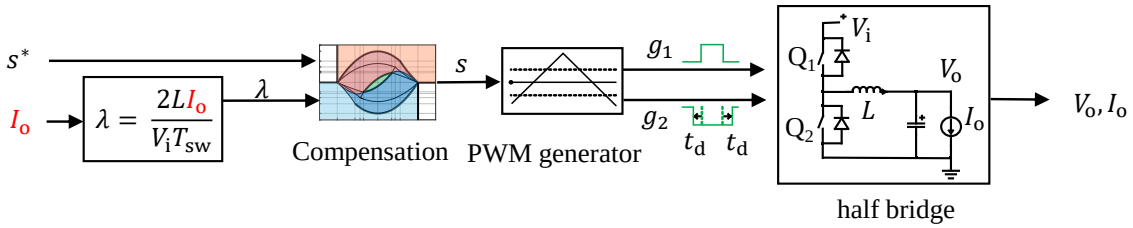


Figure 5.1: An example to implement the proposed compensation method into a feedforward control. The output current I_o at each switching cycle is either known or predictable.

In practice, the output current, I_o, and the filter inductor, L, may be unknown. The inductance may also vary with temperature. The implementation of this compensation needs the knowledge of L and I_o. To find L, the middle point voltage v_m, the output voltage V_o and the inductor current i_L are measured during a period from t_1 to t_2 when one transistor is ON and the other is OFF:

$$L = \frac{(v_m - V_o)(t_2 - t_1)}{i_L(t_2) - i_L(t_1)}. \tag{5.1}$$

The inductor current, i_L, could be measured. Based on that, the output current I_o could be calculated by:

$$I_o = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_L \, dt. \tag{5.2}$$

The normalised current, λ, is then found from the calculated L and I_o. The assumption that $f_{sw} >> f_m$ must hold, such that L and I_o are approximated as constant over two adjacent switching cycles. The accuracy of the measurements affects the results, particularly at the boundaries between different regions, as discussed in detail in Section 5.4. Fig. 5.2 shows an example where I_o and L are calculated from measurements and then fed back to the input.

Feedback control is used to reduce the dead-time impact on the output voltage. It compares the measured V_o with the expected output voltage, V_o^*, to generate an error signal. The controller then adjusts the duty cycle based on the error signal to compensate for the voltage loss or gain in V_o caused by dead-time. The

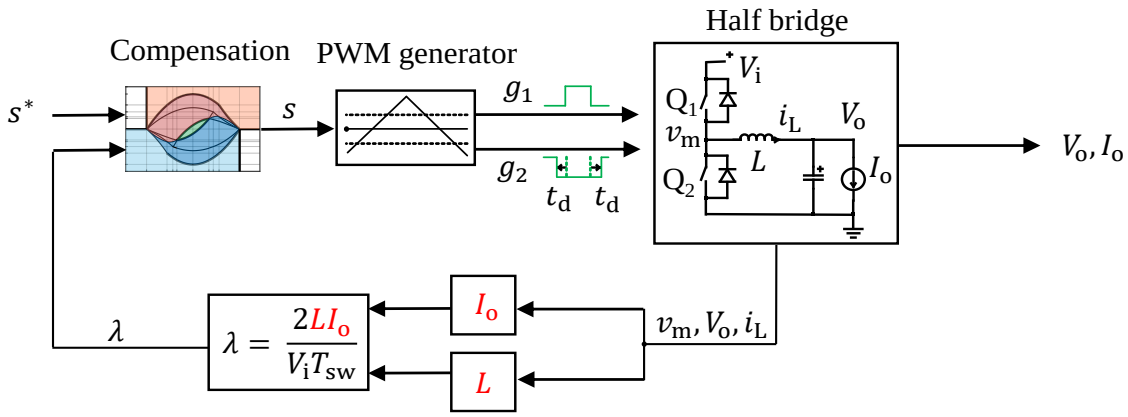


Figure 5.2: An example to implement the proposed compensation method when L and I_o are unknown. Measurements of v_m, V_o and i_L are taken to find L and I_o, as in (5.1) and (5.2). that $f_{sw} >> f_m$ must hold here.

bandwidth required for the feedback loop is proportional to f_{sw}. When f_{sw} is very high, the bandwidth becomes very high, which makes it hard for controllers to respond. A high f_{sw} results in a large τ, where transistional operating modes during the dead-time play a dominant role in the distortion in V_o. The complete analysis of these operating modes in this thesis enables an accurate prediction of the outputs, such that a feedforward control can minimise the dead-time distortion before V_o is impacted at a high f_{sw}.

Implementation of the dead-time analysis to model predictive control

Model predictive control is a control strategy. It uses a systematic model to predict future states and controlled variables over a finite prediction horizon for all the possible control actions, using the current state as the initial state. A cost function which captures controlled variables evaluates each predicted result. The best control action is then selected as the one that minimises the cost function. Finite Control Set Model Predictive Control (FCS-MPC) is commonly used in power electronics. The controller selects the switching states of transistors to minimise the cost function from a finite number of switching states, and directly manipulates the switch positions of the semiconductors. It is a completely different modulating method from PWM to operate power electronics. The insertion of

dead-time is still essential when two switches alternate in a half-bridge using FCS-MPC. Instead of using the term switching period T_{sw}, the sampling period, T_{s}, is used. The proposed compensation method, which is based on the PWM modulating method, is no longer valid. Similarly, the derivation of actual conversion ratios in chapter 2 no longer holds. However, all the possible operating modes during the dead-time, which are identified in this thesis, still occur in the dead-time in FCS-MPC, if the two assumptions hold: (i) the output voltage V_{o} is constant over a sampling period; (ii) ideal components.

Fig. 5.3 shows the key paramters in the k^{th} sampling period, where u represents the switching state. Two switching states are available, i.e., $u \in \{1, 0\}$: when the high-side switch is on, and the low-side switch is off, $u = 1$, $v_{\mathrm{m}} = uV_{\mathrm{i}} = V_{\mathrm{i}}$. When the low-side switch is on, and the high-side switch is off, $u = 0$, $v_{\mathrm{m}} = uV_{\mathrm{i}} = 0$. During the dead-time, the value v_{m} depends on (i) the direction of i_{L}; (ii) whether i_{L} drops to zero, as discussed in chapter 2. If the switching state remains the same as the one in the previous sampling period, dead time is not needed. Table 5.1 enumerates all the possible cases that could occur during a sampling period T_{s}. During the dead-time, the mathematical model of the half-bridge, as shown in Fig. 1.8 (a) is: $\frac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t} = \frac{1}{L}(v_{\mathrm{m}} - V_{\mathrm{o}})$, where the value of v_{m} has to be determined for each case listed in the table. The output voltage, V_{o}, is found with the knowledge of i_{L}. If the self-commutated reverse conduction and a fixed output capacitance are considered, as model 2, equation (4.2) models the behaviour of v_{m} and i_{L} during the dead-time.

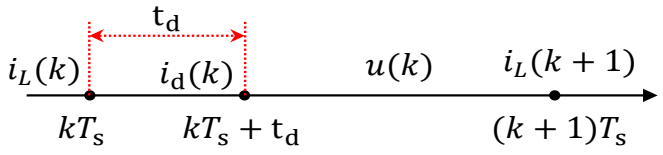


Figure 5.3: The k^{th} sampling period in FCS-MPC.

Extension of this analysis to an H-bridge The dead-time distortion and proposed compensation are based on a hld-bridge. They can be easily extended to

Table 5.1: Enumeration of all possible cases over one T_s. ✗: don't-care. The 4^{th} column indicates whether t_d is needed. The 6^{th} column implies whether i_L drops to zero during the dead-time or not.

u(k-1)	u(k)	i(k) direction	t_d?	Conduction Mode
1	1	✗	✗	CCM
1	0	1	✓	DCM CCM
1	0	-1	✓	DCM CCM
0	0	✗	✗	CCM
0	1	1	✓	DCM CCM
0	1	-1	✓	DCM CCM

an H-bridge when the two assumptions hold: (i) the output voltage V_o is constant over a switching cycle. (ii) Components are ideal.

Fig. 5.4 shows an example of an H-bridge where the analysis presented in this thesis is applicable. Gate signals of Q_1 and Q_2 in an ideal system are denoted as g_1^* and g_2^* respectively. Gate signals of Q_1, Q_2, Q_3 and Q_4 are marked as g_1, g_2, g_3, and g_4 respectively. When Q_1 and Q_2 are on, the middle point voltage v_m equals to V_i. When Q_3 and Q_4 are on, v_m equals to $-V_i$. During the dead-time, if i_L is positive, it flows through the inductor, the load, D_3, the power supply, and D_2. Therefore, the middle point voltage v_m equals to $-V_i$, and the inductor current i_L decreases. If the current i_L drops to zero during the dead-time, the voltage across the inductor L becomes zero, and the voltage across the capacitor C remains the same as before. Therefore, the middle point voltage v_m becomes V_o until two switches are on. Similarly, during the dead-time, if i_L is negative, it flows through the inductor, D_1, the power supply, D_2, and the load. The middle point voltage v_m equals to V_i, and the inductor current i_L decreases. If the current i_L drops to zero during the dead-time, the middle point voltage v_m becomes V_o until two switches are on.

Fig. 5.5 shows an example where i_L drops to zero during the dead-time. The same analysis is applied to this H-bridge, and similar conclusions are drawn. The only difference in the analysis and the conclusions is that, the middle point voltage

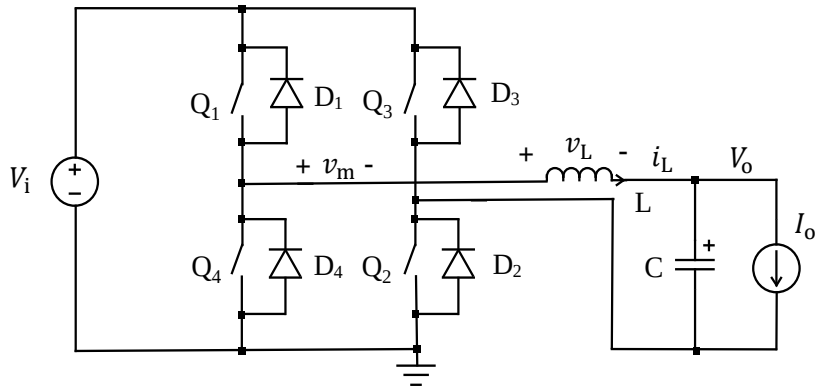


Figure 5.4: A circuit diagram of an H-bridge. The analysis of dead-time distortion and proposed compensation presented in this thesis applies to this H-bridge when V_o is constant over the switching cycle, and components are ideal.

v_m varies from 0 to V_i in a half-bridge in Fig. 1.8 While v_m in this H-bridge varies from $-V_i$ to V_i. Therefore, the output voltage V_o in the H-bridge doubles the amplitude and has a DC offset of V_i compared to V_o in the half-bridge. This H-bridge is commonly used in an isolated format where a transformer is included between the middle point of the H-Bridge and the LC filter. Considering the transformer is an ideal component, the same analysis discussed in this paragraph applies to that isolated format.

Fig. 5.6 shows a circuit of another widely-used H-bridge. Compared with the half-bridge in Fig. 1.8 (a), the LC filter is removed. The load, an inductor in series with a resistor, is directly connected between the middle points. The output voltage, V_o, is the middle voltage v_m. The output current i_o is the inductor current i_L. The current i_L is often the controlled variable instead of v_o. The equations of the actual conversion ratios and proposed compensation cannot be used in this H-bridge because the assumption in V_o is not held. However, the same analysis method applies to this H-bridge. The same operating modes still exist during the dead-time. Equations to find i_L and boundaries among these operating modes can be derived with the same method. The difference in the analysis is that i_L varies exponentially with time.

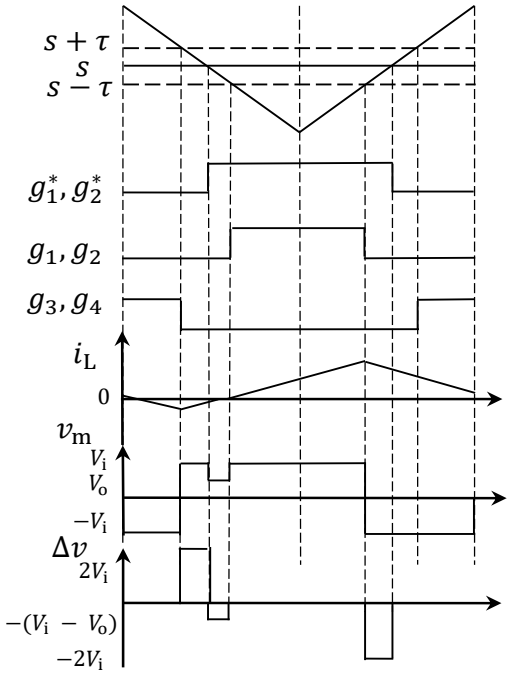


Figure 5.5: An example of waveforms of the H-bridge in Fig. 5.4. Waveforms have the same shape as those in a half-bridge, but the voltage waveforms of v_m and V_o double the amplitudes and have an offset of $-V_i$.

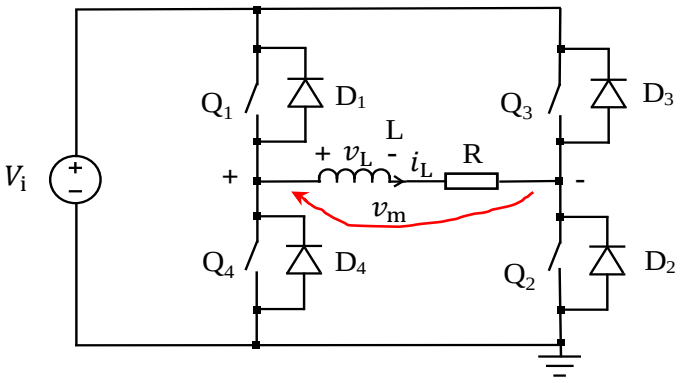


Figure 5.6: Another circuit diagram of an H-bridge. The LC filter is removed. Often, the variable of interest is the current through the inductance and the resistor instead of the output voltage.

5.3 Limitaion

This study is a fundamental scientific research that fills theoretical gaps in the dead-time field. The theoretical analysis in Chapter 2 is based on three assumpotions:

1. The half-bridge operates in a quasi-static situation, i.e., $f_{sw} >> f_o$, where f_o is the fundamental frequency.

2. Components are ideal.

3. Current measurement is accurate.

These three assumptions constrain the application of this analysis: When τ is large, transitional operating modes become dominant, as shown in Fig. 2.39, and the proposed compensation rules are more effective, as shown in Fig. 2.38. As the dead-time t_d is intrinsically set by semiconductor transistors, this analysis becomes more interesting when f_sw is large. However, on the one hand, a large f_sw increases $\frac{f_\mathrm{sw}}{f_\mathrm{o}}$. At a boundary value of f_sw, assumption 1 is not held. On the other hand, parasitic capacitors, c_sw, start to play a more significant role in the output distortion at a large f_sw such that components can no longer be approximated as ideal as stated in assumption 2. What's more, accurate measurements of I_o become difficult at a large f_sw, which could break assumption 3. To leverage this theory and the compensation rules, the boundary value of f_sw for given semiconductor transistors with a fixed t_d should be considered such that these three assumptions hold.

Models 2 and 3 consider the impact of c_sw, which identifies the voltage errors more accurately compared with model 1 at a large f_sw. However, both models are too complex to describe the voltage errors analytically. Therefore, an analytical investigation of the compensation rules for these two models is not conducted. The application of models 2 and 3 is constrained to numerical identification of the voltage errors.

5.4 Future studies

Extension of the proposed analysis to DC-AC conversion

This investigation is based on the quasi-static situation of a DC-DC half-bridge with a fixed output voltage (synchronous buck converter), instead of general situations including amplification of both DC and AC signals. The reason is that when the switching frequency (f_sw) is much higher than the fundamental frequency (f_o), a DC-AC inverter is often approximated as a DC-DC converter over several

consecutive switching periods. However, the ultimate goal is to implement the proposed compensation method to DC-AC inverters.

To implement this study to a DC-AC inverter, which generates a sinusoidal AC output, a lookup table of s^* is first produced. Assume that a DC output is approximated over M switching periods. This lookup table is then modified such that s^* is the same over M switching periods. The output current is measured at the beginning of every block of M switching periods. Based on s^*, λ, and τ, a new s is found based on the proposed compensation method. Gate signals, based on s, are then produced and applied to the DC-AC inverter.

However, many details would need to be considered in this implementation. For example, this proposed compensation method relies on the measurement of the output current (the same as the three conventional ones). The accuracy of the current measurement affects the generation of the new s. A big impact may occur near the boundaries among different regions. A study that investigates the relationship between the accuracy of the current measurement in practice and the compensated result would be conducted. Another example is that, based on the measured current, a new s is calculated and then used to generate gate signals. The computational efforts in this online calculation limit the complexity of the model. Models with more layers of complexity, such as Models 2 and 3, may require a fast numerical solver to identify s. A lookup table could replace the online calculation. However, it is important to consider whether errors accumulated over time would make the lookup table obsolete. Information about the load should also be known in advance.

Optimisation of the design of a half-bridge based SMPA subject to the practical impact of the dead-time distortion compensation

As discussed in Section 1.4.1, there is a trade-off among the dead-time (t_d), switching frequency (f_sw, or switching period $T_\mathrm{sw} = \frac{1}{f_\mathrm{sw}}$), THD and the low-pass filter (cut-off frequency f_c, and order o). After the implementation of the dead-time compensation to a DC-AC conversion, the spectrum of the output voltage can be obtained to investigate this trade-off in detail. This balance can help to optimise the design

flow of a half-bridge-based SMPA. For example, for a compensated system with a given THD, how to determine the value of f_{sw} to relax the requirement of the low-pass filter, so that a compact design is available. A DC-AC inverter can be implemented to validate the design flow.

Investigation of how the gate driver circuitry, along with the dead-time, impacts the distortion in the average output

A large c_{sw} is observed in the experiment (see Chapter 3), which leads to errors within [0.03, 0.05] in a small group of cases in models 1,2 and 3. A hypothesis that C_{boot} from the bootstrap circuit causes the large c_{sw} is proposed. However, no sufficient evidence has been found. To identify the voltage error caused by the dead-time more accurately, it is important to investigate (i) What are potential components that may lead to this large c_{sw}. (ii) How these components, along with the dead-time, result in distortion in the average output. (iii) How much distortion is caused due to the coupling impact of these components and dead-time. An understanding of these questions could further improve half-bridge models at the expense of increased complexity and computational efforts. Although not reported in this thesis, I performed the same experiment using a similar half-bridge chip with an integrated gate driver (LMG5200 [103]). A similar large switching capacitance is also observed. This suggests that C_{unk} may be a common feature across many or all bootstrap drivers. See Appendix D if interested.

Investigation of artificial neural network-based correction techniques for dead-time distortion

An Artificial Neural Network (ANN) is a computational model that recognises patterns among inputs and outputs from data. It consists of interconnected elements called neurons, organised in a structure with three layers: input layer, hidden layer and output layer. The interconnection between the input and hidden layer is described by the hidden neuron activation function, f_{h}. The interconnection between the hidden and output layer is described by the hidden neuron activation

function, f_o. The root cause of the large c_{sw} observed in the experiment is unclear. Analytical solutions in models 2 and 3 are hard to find due to the reiteration of situations and the non-linearity of c_{oss}, respectively. Instead of exploring the dominant contributor of the large c_{sw} and the analytical solutions of complex models, an ANN, which solves complex non-linear problems, could be developed to identify the actual conversion ratio M for a given input set in a half-bridge. Based on this ANN, the reference signal s, which compensates distortions in the half-bridge to obtain a specific M, can be searched. Fig. 5.7 shows an example of the structure of an ANN to achieve this goal. The input vector x includes six signals which are directly available from a half-bridge, including s, I_o, t_d, V_i, L, and f_{sw}. A hidden layer with n neurons is shown. The output signal is the conversion ratio M, which is denoted as y in this ANN. Experimental data, which scans the map shown in Fig. 3.9 and lists the output for each input vector, are used to train the ANN to optimise its weights and bias [104]. This ANN-based compensation technique avoids further exploration of the unknown c_{sw} and calculating analytical solutions of complex models. It also corrects distortion caused by other factors. However, the ANN trained by data collected from one half-bridge may not function well in other half-bridges if unknown factors exist. Apart from that, many details need to be considered. For example, how many hidden layers and how many neurons in each layer are needed to predict the output accurately? Which activation function should be selected in the design? What training pattern fits this problem best?

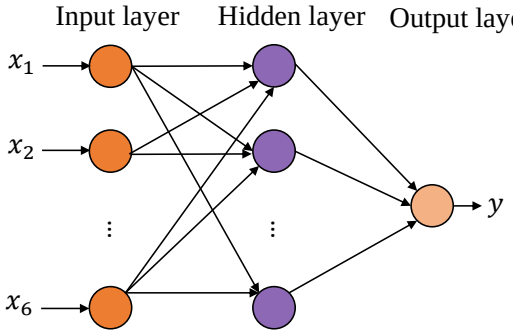


Figure 5.7: An example of a structure of an ANN to compensate for distortion.

Appendices

A

PLECS simulation of the Model 2

Fig. A.1 shows the simulation circuit of Model 2 in PLECS, as discussed in Section 4.1. Fig. 4.5 (a) is plotted based on the data simulated in this circuit.

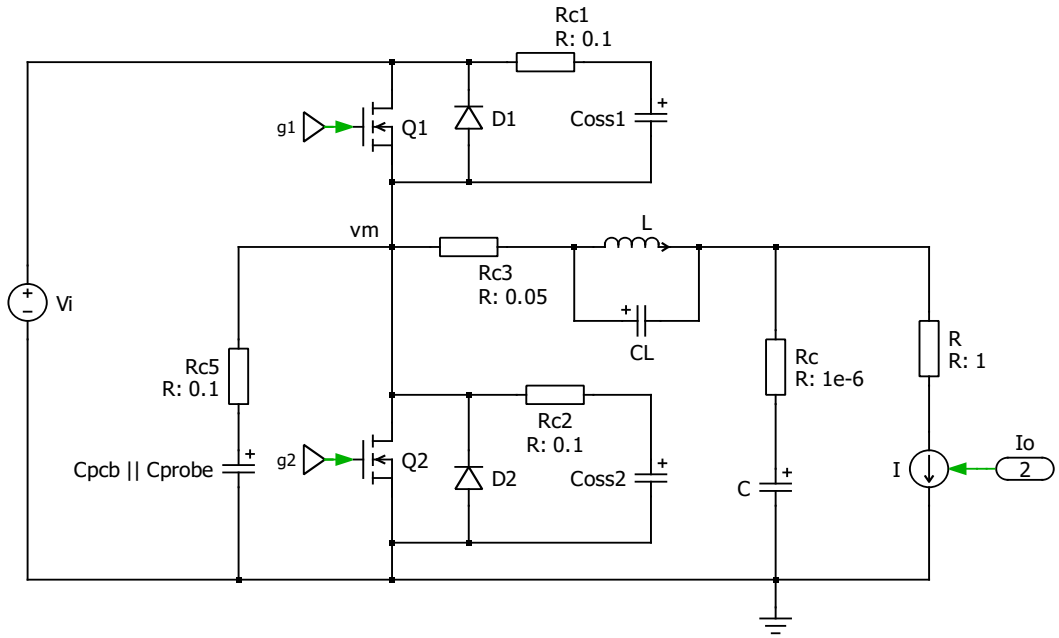


Figure A.1: The circuit simulated in PLECS with fixed C_{oss} (Model 2).

As aforementioned in Section 3.1.2, the dead-time manager in the MCU generates a complementary signal of a target signal, and then delays the rising edges of both. It is activated when $s \in [(\tau - 0.5), (0.5 - \tau)]$. When $s < (\tau - 0.5)$ or $s > (0.5 - \tau)$, one of the gate signals always remains logic low, so this dead-time manager is inactivated.

This behaviour of the dead-time manager is modelled by the 'Turn-on delay' block and the logic gate 'NOT' block in the PLECS. The 'Turn-on delay' block delays the rising edge of its input signal. When $s \in [(\tau - 0.5), (0.5 - \tau)]$, a gate signal without dead-time inserted is generated in the Simulink (Version 10.7, R2023a). Gate signals g_1 and g_2 with dead-time inserted are then generated accordingly by the 'Turn-on delay' and logic gate 'NOT' in the PLECS, as shown in Fig.A.2 (a). When $s < (\tau - 0.5)$ or $s > (0.5 - \tau)$, the gate signal that has rising and falling edges is generated in the Simulink, with dead-time inserted. It is then fed into the transistor. The gate signal for the other switch is always 0, as shown in Fig. A.2 (b).

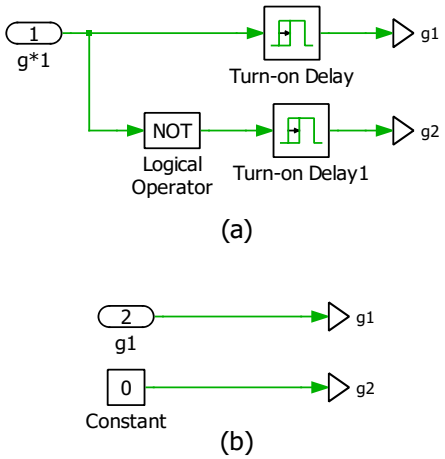


Figure A.2: Generation of gate signals in PLECS. (a) 'Turn-on delay' block and logic gate 'NOT' block model the behaviour of the dead-time manager in the MCU (see Fig. 3.6 (a)). When $s \in [(\tau - 0.5), (0.5 - \tau)]$, gate signals g_1 and g_2 are produced this way. (b) In extreme cases where $s < (\tau - 0.5)$ or $s > (0.5 - \tau)$, the dead-time manager is inactivated as one of the gate signals remains logic low always (see Fig. 3.6 (b)).

For each case, the time instants of the rising and falling edge of a gate signal in terms of the number of MCU clocks over one switching period, n_r and n_f, are found by the same way as described in Section 3.1.2, using the same script in Matlab Version 9.14 (R2023a). The time instants of the rising and falling edge in a switching period, t_on and t_off, are calculated as:

$$\begin{cases} t_\mathrm{on} = \frac{n_\mathrm{r} T_\mathrm{sw}}{N_\mathrm{clk}}, \\ t_\mathrm{off} = \frac{n_\mathrm{f} T_\mathrm{sw}}{N_\mathrm{clk}}. \end{cases} \tag{A.1}$$

At the j$^{\text{th}}$ (j $>$ 1) switching period, the time instants of the rising edge and the falling edge of the gate signal are:

$$\begin{cases} T_{\text{on}}(\text{j}) = T_{\text{on}}(\text{j - 1}) + T_{\text{sw}}, \\ T_{\text{off}}(\text{j}) = T_{\text{off}}(\text{j - 1}) + T_{\text{sw}}, \end{cases} \tag{A.2}$$

where $T_{\text{on}}(1) = t_{\text{on}}$, $T_{\text{off}}(1) = t_{\text{off}}$. A clock in the Simulink is compared to T_{on} and T_{off} to generate the gate signal, as shown in Fig. A.3.

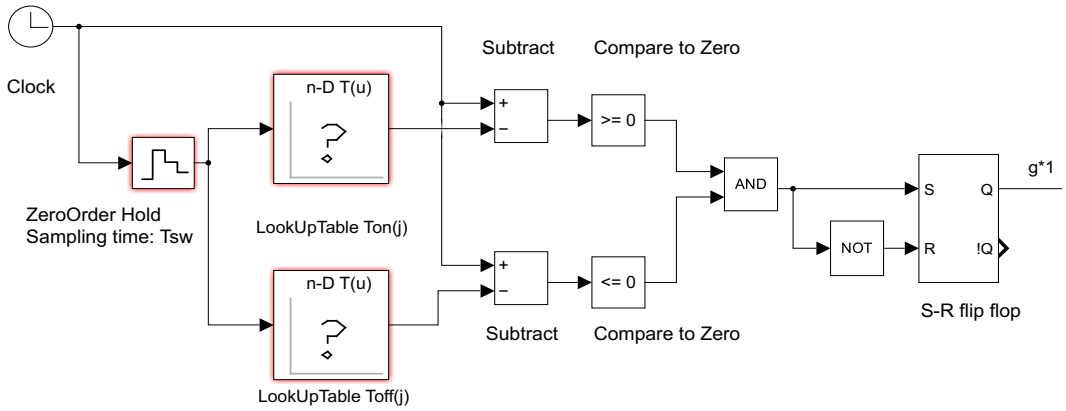


Figure A.3: Generation of g_1^* in Simulink. The gate signal $g_1^*$is then fed into PLECS as shown in Fig. A.2. One LookUpTable records $T_{\text{on}}(j)$, the other one records $T_{\text{off}}(j)$ (see (A.2)).

B

LTspice simulation of Case III

Fig. B.1 shows the LTspice circuit of Case III, as discussed in Section 4.3.

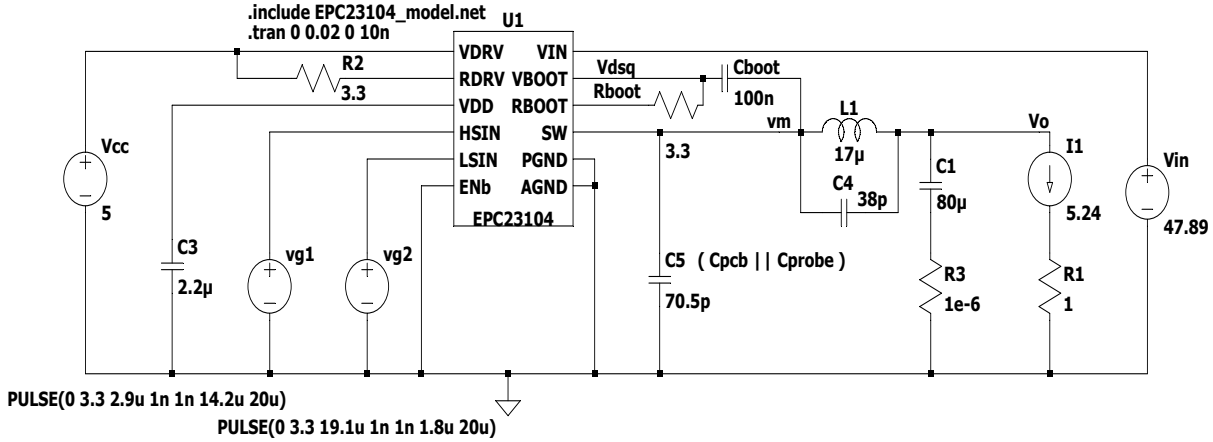


Figure B.1: The circuit simulated in LTspice. The EPC23104 module is provided by EPC Co.[101]. The gate drive part is set up based on [88]. The power circuit is set up based on the parameters used in the experiment (see Table 3.1).

C

PLECS simulation of Model 4

Fig. C.1 shows the PLECS circuit of the Model 4, as discussed in Section 4.3.

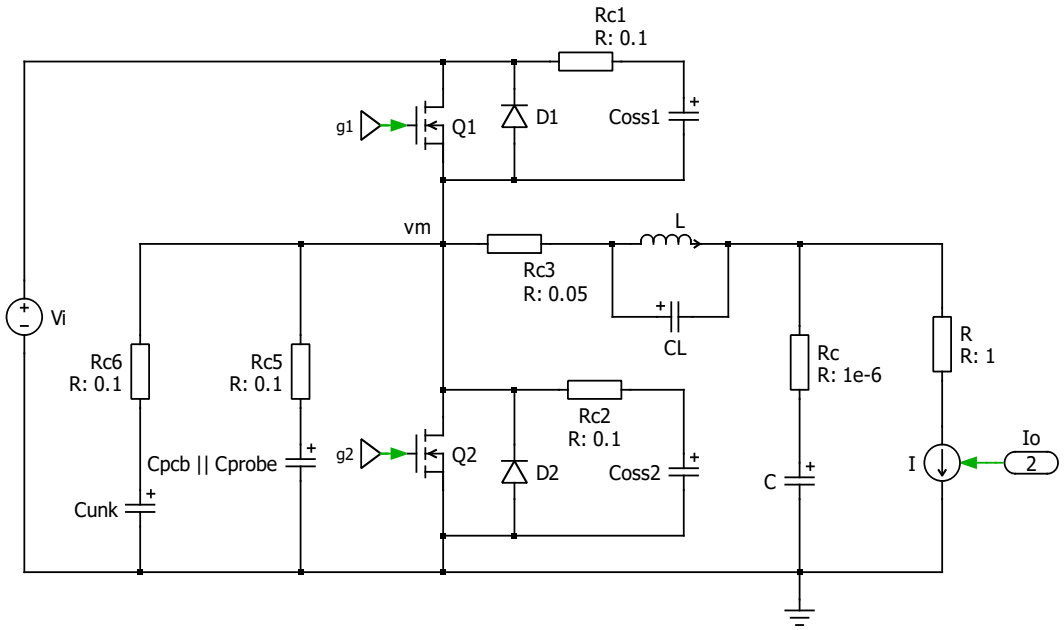


Figure C.1: The circuit simulated in PLECS. An external capacitor C_{unk} = 100 nF is included in the previous circuit shown in Fig. A.1. C_{oss} = 284 pF. Parameters are the same as those in Table 4.1.

D

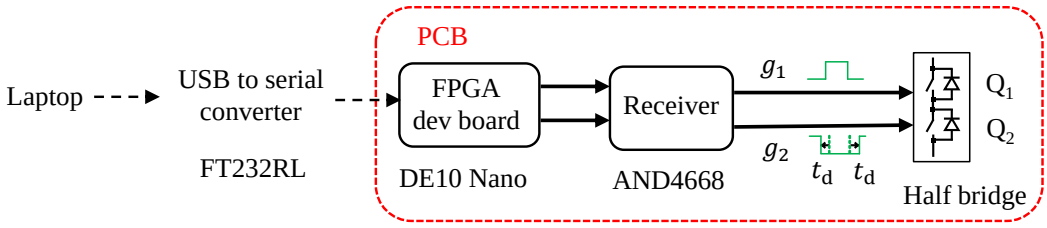
Waveforms collected by LMG5200

As mentioned in Chapter 4, prior to the experiment shown in Chapter 3, a preliminary experiment using LMG5200 [103] was conducted. LMG5200 integrates two GaN FETs into a half-bridge configuration. Similar to the chip EPC90152 shown in Chapter 3, LMG5200 also integrates a booststrap circuit as a gate driver. Some cases with $f_{\mathrm{sw}} = 50$ kHz and $f_{\mathrm{sw}} = 2$ MHz are scanned. The unknown capacitor, observed in Chapter 3, is also noticed in some measured cases. The PCB with LMG5200 was fabricated in 2019 for a different target. This preliminary experiment was conducted in 2023. LMG5200 is relatively old then. This PCB is not well designed with some flying wires. Therefore, I did not investigate the limited result collected here or measure the contributors of c_{sw}. Instead, I planned the experiment shown in Chapter 3. This appendix is presented as supplementary material for readers who are interested.

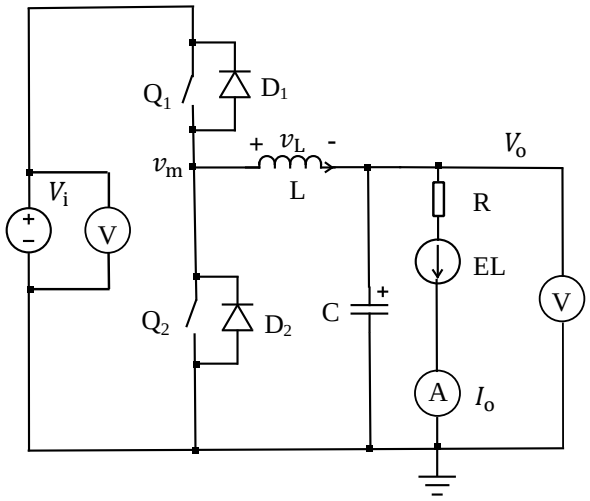
D.1 Circuit Setup

Fig. D.1 shows the set-up block diagram and the circuit diagram. Fig. D.2 shows a photo of the PCB. Cases with extreme s are not scanned. Therefore, no DC-DC converter is attached to the bootstrap capacitor. No power supply is attached to

the electronic load. The measurement and the method to generate gate signals are the same as those shown in Chapter 3.



(a)



(b)

Figure D.1: (a) Block diagram of the experimental set-up. (2) Circuit diagram of the half-bridge with digital multimeters.

D.2 Waveforms

Fig. D.3 compares the measured and theretical waveforms of a case where $f_{sw} = 50$ KHz, $s = 0.3837$, $\lambda = 0.13$ ($I_o = 1.62$ A), $V_i = 48.04$ V. Table 4.1 lists the parameters. Fig. D.4 shows the c_{sw} calculated based on (1.19), where a large c_{sw} is observed.

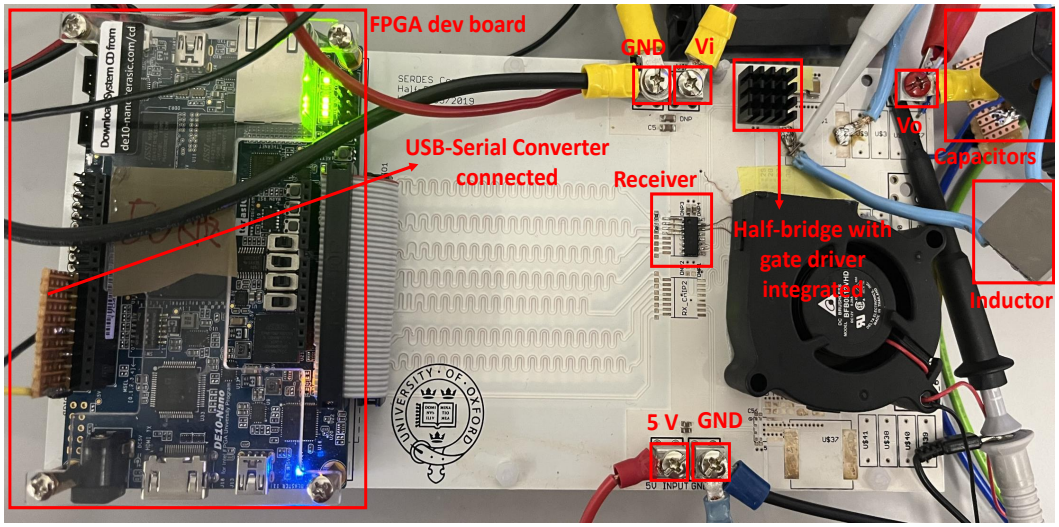


Figure D.2: A photo of this experimental setup.

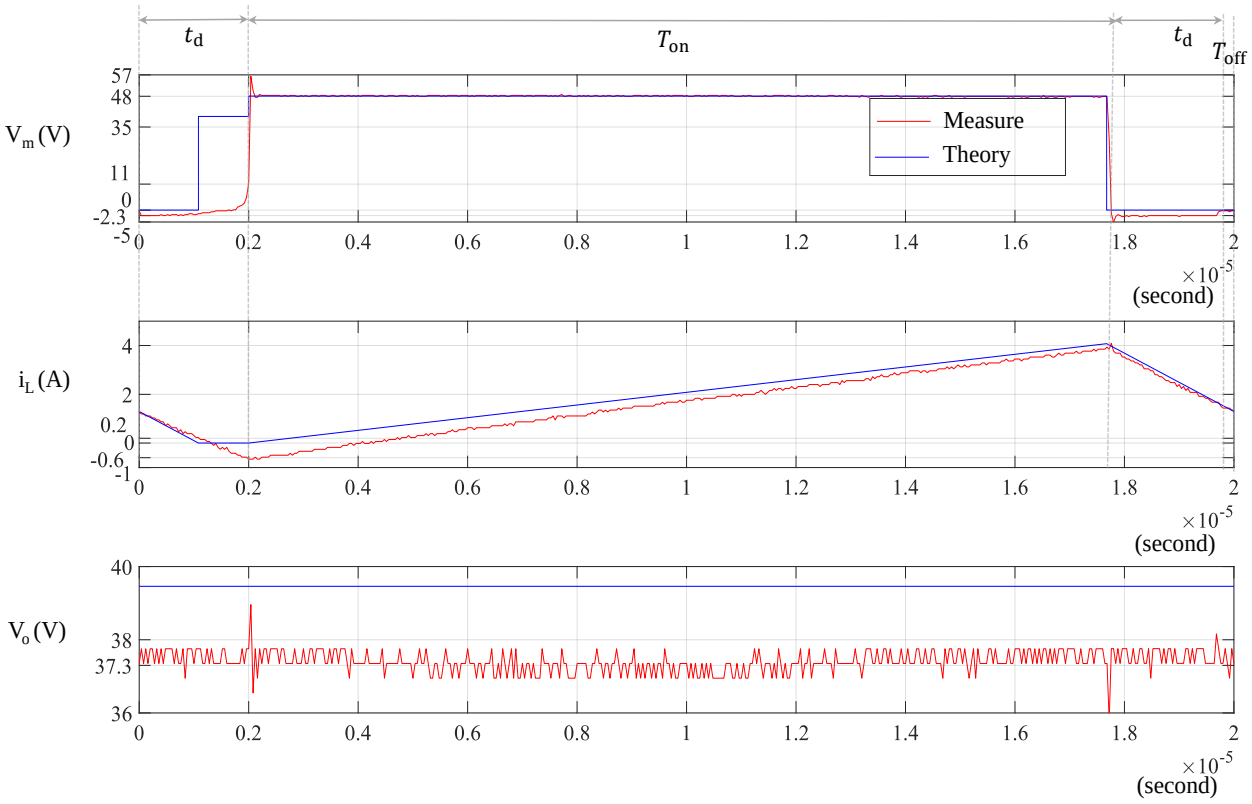


Figure D.3: Waveforms of a case with $f_{sw} = 50$ kHz. (a) middle-point voltage. (b) inductor current. (c) output voltage. $t_d = 2$ μs, $T_{on} = 15.7$ μs, $T_{off} = 0.3$ μs.

Table D.1: Key parameters in the case in Fig. D.3.

parameters	value
V_{i}	48 V
f_{sw}	50 kHz
τ	0.1
L	33 μH
R	1 Ω

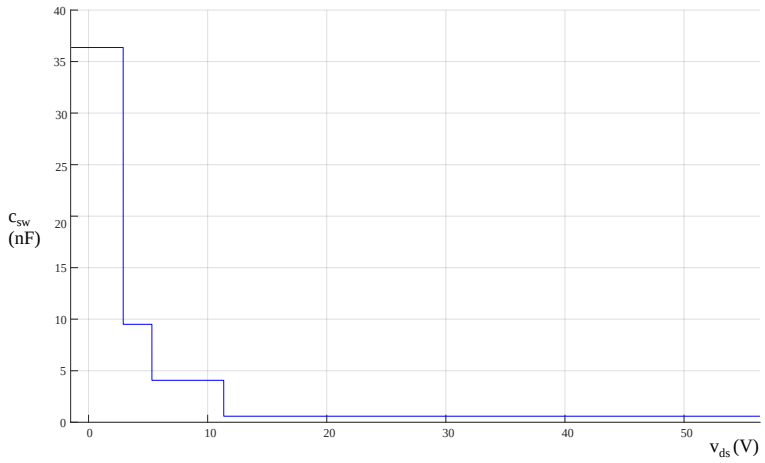


Figure D.4: Variation of c_{sw} for the case with f_{sw} as shown in Fig. D.3.

D. Waveforms collected by LMG5200

Fig. D.5 compares the measured and theretical waveforms of a case where $f_{sw} = 2$ MHz, $s = -0.0620$, $\lambda = 0.17$ ($I_o = 1.29$ A), $V_i = 48.03$ V. Table D.2 lists the parameters. Fig. D.6 shows the c_{sw} calculated based on (1.19). The large c_{sw} is not observed. The parasitic c_{sw} that i_L has to charge and discharge during the rising-edge dead-time leads to the deviation between the measured and theoretical waveform. It indicates that when f_{sw} is large enough, the impact of the c_{sw} affects V_o heavily.

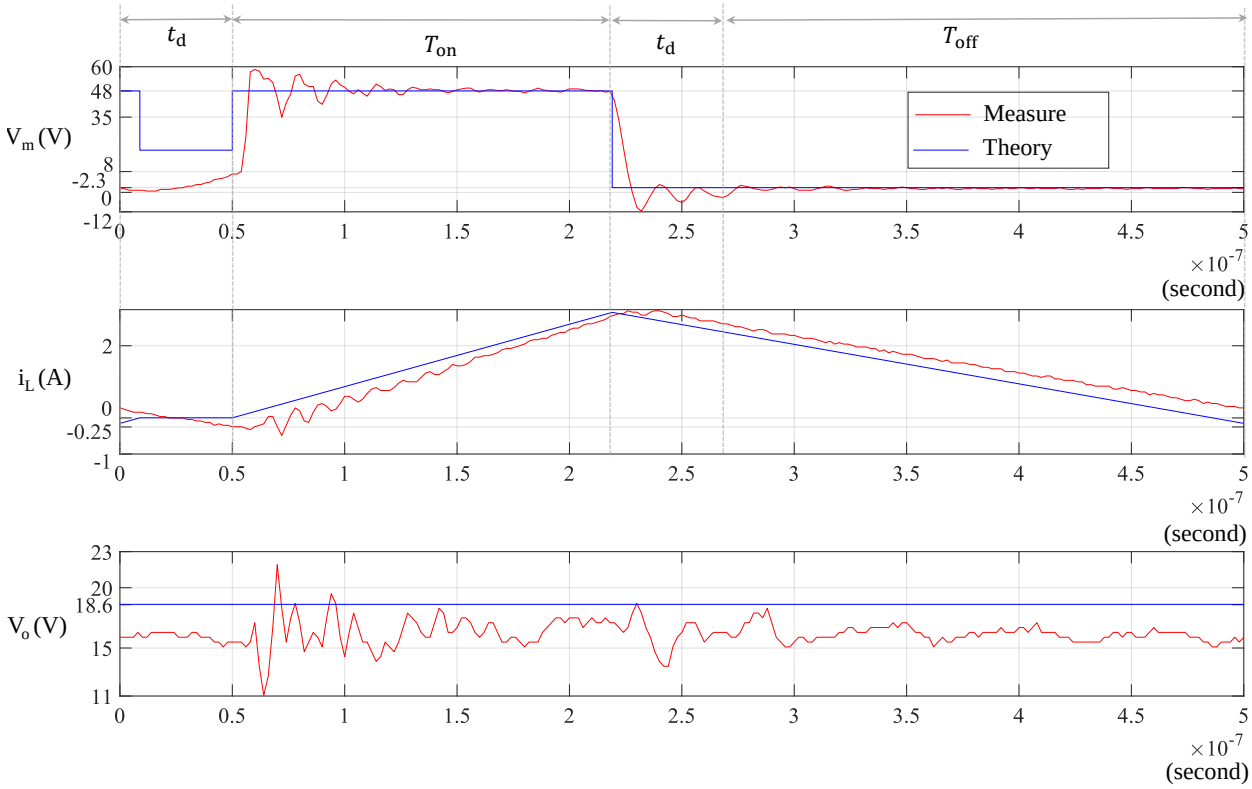


Figure D.5: Waveforms of a case with $f_{sw} = 2$ MHz. (a) middle-point voltage. (b) inductor current. (c) output voltage. $t_d = 50$ ns, $T_{on} = 169$ ns, $T_{off} = 231$ ns.

Table D.2: Key parameters in a case shown in Fig. D.5.

parameters	value
V_i	48 V
f_{sw}	2 MHz
τ	0.1
L	1.7 μH
R	1 Ω

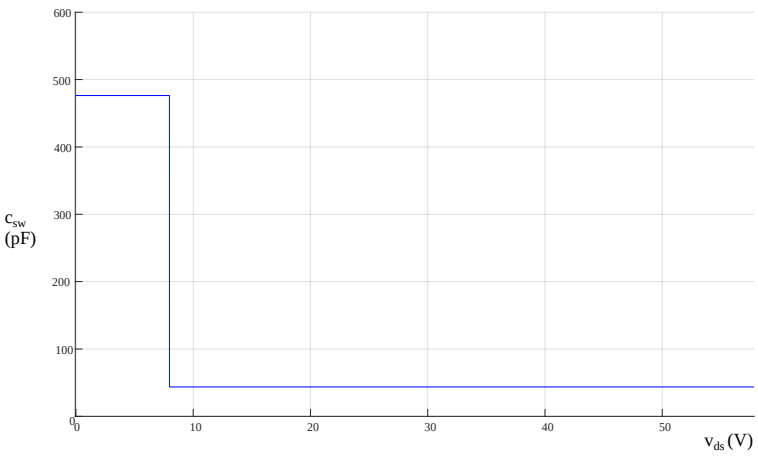


Figure D.6: Variation of c_{sw} for the case with f_{sw} as shown in Fig. D.5.

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