Integrating Logarithmic Wide Dynamic Range CMOS Image Sensors

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Abstract

Complementary Metal Oxide Semiconductor (CMOS) image sensors are widely used in many applications such as consumer electronics, automotive and security. One of the key requirements in today's imaging applications is the ability to capture natural scenes faithfully; a feature known as wide dynamic range (WDR). Current digital image sensors have a linear response that results in saturation and loss of details. Conventional CMOS image sensors with a logarithmic response attempt to address the limited dynamic range of the linear digital image sensors by exploiting the subthreshold operation of a transistor in a pixel. This results in CMOS pixels that are able to capture light intensities of more than six decades (120 dB). However, the approach comes at the expense of high fixed pattern noise (FPN) and slow response.

The work presented in this thesis describes a five all nMOS transistor (5T) pixel architecture that aims to achieve wide dynamic range. This feature is obtained using a time-varying reference voltage that is applied to one of the transistors of the pixel. The reference voltage varies in a logarithmic fashion in order to modulate the effective integration time of the pixel. This allows the pixel to avoid saturation; hence extending the dynamic range. In addition, the slope of the reference voltage that can be adjusted means the pixel response is adaptive and can be more robust towards temporal noise. To have a well-controlled pixel response, the pixel non-ideal effects such as source follower gain, body effect and subthreshold effect are characterised and included as an improved model to the reference voltage.

Measurement results from fabricated chips using UMC 180 nm technology are presented and analysed. A dynamic range of 80 dB with a logarithmic response of 600 mV/decade has been achieved. This is a significant improvement in comparison to that of conventional logarithmic pixel response (60 mV/decade). An analysis of the effect of chip variations that causes FPN has been conducted and correction methods that can reduce the illumination error to less than 2% have been proposed. In addition, the first experimental study comparing different dynamic range extension methods has been performed. In the study, a method to control the response of a WDR approach using a stepped voltage that has achieved a dynamic range of up to 120 dB is also presented. The result of the study leads to a modification to the reference voltage that allows an implementation of an analogue circuit to generate the reference voltage.

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Chapter 1

Introduction

Solid state image sensors have gained mass adoption in a variety of applications including leisure, scientific research, manufacturing, security and automotive [1]. This trend is driven by the high demand to acquire visual data due to increased ability to process and extract meaningful information from the visual object. In addition, since the last two decades, complementary metal oxide semiconductor (CMOS) image sensor technology has become more mature and therefore offers competitive advantages against charge couple device (CCD) technology in the field of solid stage imaging. In particular, the development of active pixel sensor (APS) that uses existing CMOS technology has emerged as a substitute to CCD as a result of comparable noise, quantum efficiency and dynamic range performances at a much lower power and increased functionality [2]. Furthermore, CMOS image sensors can offer true imaging systems, integrating timing control, data conversion and signal processing on a single chip.

However, one of the main challenges common to standard CMOS and CCD imagers, is its inability to capture a wide range of light intensities available in nature. This ability is referred as dynamic range and measured in decibels (dB). Natural scenes have dynamic range of more than 160 dB [3]. On the contrary, conventional CMOS and CCD image sensors have a dynamic range of 40-70 dB [4]. The limited

dynamic range of the sensors means that the acquired image will suffer from loss of details and will either be under or overexposed. In some critical applications such as automotive, the limited dynamic range is not tolerable. In addition to the wide dynamic range, the quality of the reproduced image is also an important factor. The conventional approach to extend dynamic range using CMOS imagers that have logarithmic response can achieve a dynamic range of up to six decades [5]. However, they suffer significantly from spatial noise known as fixed pattern noise (FPN) that results in images with salt and pepper features [6]. Until this day, the effort to design wide dynamic range imagers with high-quality images remains a great challenge.

1.1 Thesis motivation and organisation

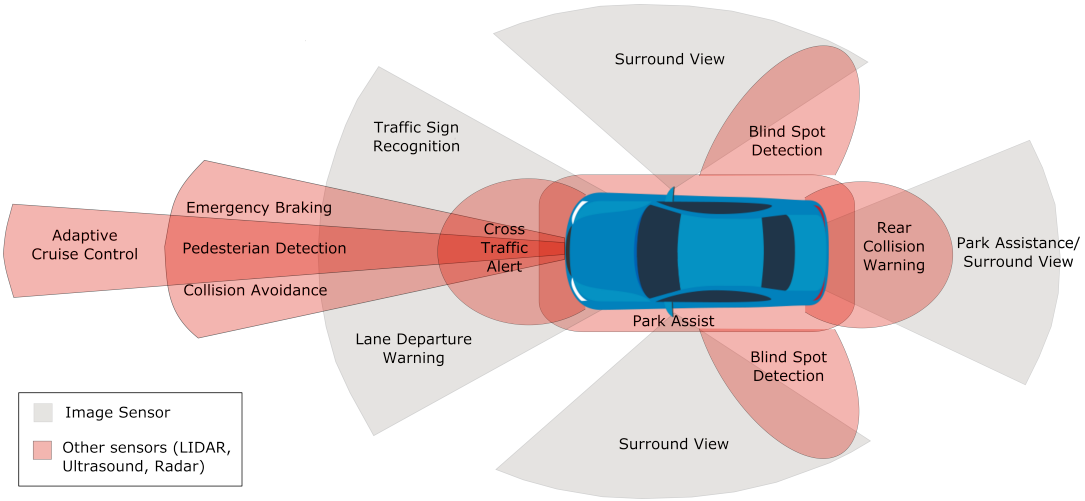


Figure 1.1: Examples of ADAS applications that use image sensors and other type of sensors for automotive vision in a fully autonomous car [7].

The wide range of light intensities encountered when imaging real-world scenes mean that a capability to acquire wide dynamic range scenes, is an important characteristic of future imagers. In addition, this capability must be achieved without sacrificing the quality of the acquired images. One major market demand for such imagers is in automotive industry. Automakers utilise image sensors extensively in

cars as part of automotive imaging solutions for Advanced Driver Assistance Systems (ADAS). The goals of ADAS are to make the driving experience safer and more enjoyable [7, 8]. Continuous research and development in automotive imaging has been undertaken to improve ADAS applications. This progress will accelerate the advent of autonomous driving [9, 10]. Figure 1.1 shows examples of ADAS applications using image sensors in an autonomous vehicle which include traffic sign recognition, park assistance, lane departure warning and surround view [7, 11]. In each of these applications, wide dynamic range capability is required in order to capture all image information in environments with varying light and harsh lighting conditions. For example at night, driving environments can be very dark while facing bright lights from illuminated and reflecting traffic signs and light sources from oncoming headlights. The dynamic range can easily exceed 100 dB in such environments. The industry standard for dynamic range set by major automotive image sensor manufacturers is at 120 dB [11, 12, 13, 14]. This is equivalent to a luminance ratio of 10^6. Common situations when wide dynamic range ability is required include:

- in environments with strong background lighting for example where an object is positioned in front of a bright light source such as sunlight
- during abrupt change of light conditions for example when entering/exiting tunnel and when pulling in/out from garage
- at night with varying light conditions and harsh lighting from headlights

To understand the impact of limited dynamic range cameras to automotive imaging, Figure 1.2 depicts a common driving situation in a tunnel with bright sunlight. Figure 1.2a and Figure 1.2b show under and overexposed scenes acquired using short and long time exposure respectively. In Figure 1.2a two cars can be seen and insufficient exposure in dark areas in the tunnel is observed. However in Figure 1.2b, only one car can be clearly seen with a complete image saturation at the end of the tunnel

(a) Underexposed scene acquired using short exposure time.

(b) Overexposed scene acquired using long exposure time.

(c) WDR image resulting from fused images adapted from [15].

Figure 1.2: Impact of underexposed and overexposed images due to limited dynamic range of imager and image correction using multiple exposure image fusion method.

while having sufficient exposure in dark areas inside the tunnel. The loss of image details at the end of the tunnel might cause safety risk and can not be compromised. One method to overcome the limited dynamic range of the camera is to fuse multiple exposure images to render a wide dynamic range image as shown in Figure 1.2c. This method is popular among some of the leading industrial players [16, 17][1] and academic research groups [18, 19]. However, this multiple capture approach requires on-chip memory, high speed read out and additional column circuitry. In addition it requires post-processing to merge and compress the images [19]. Furthermore, to have high quality images, more than two images are required to prevent a large sensitivity drop in signal to noise ratio (SNR) at the expense of higher memory and read out speed requirements. To meet all the demanding requirements, manufacturers leverage on specialised CMOS process such as 3D IC technology to accommodate high number of parallel readout circuits [17]. However this advantage comes with an increased cost.

The multiple capture approach does not solve the limited ability of imagers to capture highly contrast scenes. On the contrary, it only synthesises multiple captured images of limited dynamic range to produce wide dynamic range images. To address this issue, non-linear methods have been proposed in order to extend the dynamic range of CMOS imagers. Chou and co-workers have proposed imagers based

[1] ON Semiconductor (Aptina) and Omnivision account for 66% of the total market share of automotive image sensors [10]

on a linear-logarithmic (lin-log) response with an achieved dynamic range of up to 143 dB [20]. The method offers a tunable response that can control the transition point between the linear and the logarithmic responses. However, the main drawback of this method is that the range extension obtained at the high illumination region has a low sensitivity of only 55 mV/decade. This is because the response of the logarithmic region is based on conventional logarithmic pixels [5]. The response of the conventional logarithmic pixels is dependent on transistor parameters [21]. Using a similar method, Bae and co-workers have proposed imagers with a linear-linear-logarithmic response [22]. The additional linear response means the low sensitivity of the logarithmic region occupies a narrower region restricted at the very high illumination. However, this approach does not completely improve the low sensitivity response which can lead to a low SNR.

To avoid the low sensitivity response, methods using additional capacitors in pixel architectures have been proposed by a research group led by Sugawa [23, 24]. The connections to the additional capacitors are switched on to accommodate extra photoconverted charges at high illumination. Using these methods, responses with a dynamic range of more than 130 dB have been recorded. However, the wide dynamic range is achieved at the expense of a significant SNR drop of up to 20 dB due to the capacitor switching. Furthermore, adding capacitors increases pixel area which can lead to pixels with low fill factor.

Each method proposed previously achieves wide dynamic range at the cost of either low sensitivity response, drop in SNR or additional post-processing. The work presented in this thesis aims to propose a wide dynamic range imager that can produce high-quality images on a standard CMOS process. Using a standard CMOS process provides a cost-efficient solution to the limited dynamic range problem and benefits the academic community that does not have access to highly specialised CMOS image sensor process.

The thesis is organised as follows. In the remaining sections of Chapter 1, the background of CMOS imaging system and its performance metrics will be presented. Furthermore, different schemes of extending dynamic range will be reviewed. The reviews provide a background understanding when each of the schemes will be used later in a comparative study in Chapter 4. Then in Chapter 2, a wide dynamic range pixel is proposed. In particular, the dynamic range extension method relies on a logarithmic reference voltage V_{ref} that integrates pixel parameters to produce a well-controlled response. Subsequently, in Chapter 3, results of a prototype imager based on the proposed design are presented. In addition, a method to remove fixed pattern noise performed on the prototype imager is presented. In Chapter 4, a comparative study is conducted on different schemes of dynamic range extension on a single chip. Furthermore, a method to acquire a well-controlled response from well capacity adjusting scheme is proposed. Next, in Chapter 5, a modified V_{ref} based on linear approximation is proposed. This subsequently leads to a proposed design to generate V_{ref} and a prototype imager design. Finally, in Chapter 6, conclusions from the work presented are drawn and future work is suggested.

1.2 CMOS imagers

Using a standard CMOS technology process means that CMOS imagers can integrate analogue and digital processing on a single chip and take advantage of the technology scaling. In addition, much research and development has been invested to improve imaging performance of CMOS processes such as silicon processing, colour filter array, microlens integration and miniaturisation which lead to a camera on chip design [25]. As a result, CMOS imagers offer comparable image quality to that of CCD imagers. Early CMOS imagers adopted passive pixel sensor (PPS) architecture which is limited to only one transistor and a photodetector in the pixel. This is due to the large feature

sizes of the available CMOS technologies. The limited functionality means that PPS is vulnerable to noise and has low readout speed [4]. These issues are addressed by the introduction of active pixel sensor (APS) that integrates an amplifier in each pixel, thus overcome the drawbacks of PPS [2].

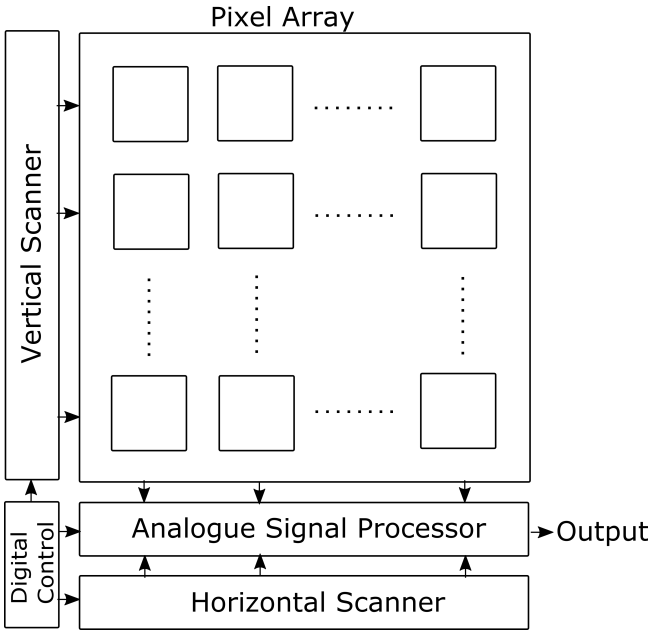


Figure 1.3: Conventional CMOS image sensor architecture.

A standard architecture of a CMOS imager is shown in Figure 1.3. The imager consists of an array of identical pixels, each having a photodetector and a minimum of three transistors. The most common photodetector used in CMOS image sensor is a p-n junction photodiode. The vertical and horizontal scanners are used for addressing the pixels' row and columns respectively. Each pixel is read out through an analogue signal processor block. Depending on a specific design, this block mainly consists of amplifiers to buffer the output voltage and may include switched capacitors and analogue to digital converter (ADC). The digital control block controls the timing of the scanners and the operation of the pixel array.

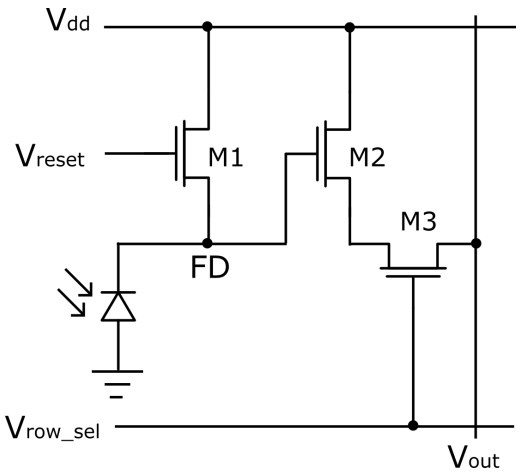


Figure 1.4: A standard three transistor pixel operating in a linear mode response.

1.2.1 3T active pixel sensor

Active pixel sensor (APS) is a standard three transistor pixel shown in Figure 1.4. Transistor $M1$ is used to reset the photodiode, $M2$ is a source follower to isolate the pixel's capacitance at floating diffusion node (FD) from column capacitance and $M3$ is a switch connected to a column current source to access to the pixel column line.

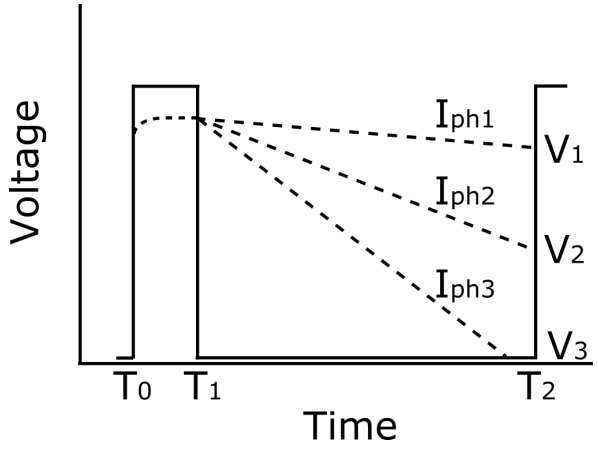


Figure 1.5: Transient responses of three different photocurrent on the standard pixel where T0 to T1, is reset period and T1 to T2, is integration period.

The pixel operation is demonstrated in Figure 1.5. It begins with a reset pulse when V_{reset} is set high to V_{dd}, resetting the photodiode. $M1$ becomes active and conducts a current which is generated by the photodiode. When this happens, parasitic

capacitance at FD is charged up to a certain voltage. Since $M1$ is an n-type transistor, this voltage at FD is equal to V_{dd}-$V_{th,M1}$. The parasitic capacitance consists of parasitic capacitances of the photodiode, transistor $M1$ and $M2$ connected to the node. When V_{reset} is dropped to gnd, $M1$ stops conducting and therefore the node connecting the photodiode and the gate of $M2$ is left floating. When this happens, photogenerated current starts to discharge capacitance at FD. The period when the discharge takes place is termed as the integration period. The discharge rate of the capacitance at FD is proportional to the light intensity illuminated at the photodiode. Therefore, the light intensity can be measured from the voltage change during the integration period. The voltage at FD can be expressed as:

$$V_{FD} = V_{reset} - \frac{I_{ph}.t_{int}}{C_{fd}} \tag{1.1}$$

where I_{ph} is the photogenerated current, t_{int} is the integration time and C_{fd} is the floating diffusion capacitance.

For a low photocurrent I_{ph1}, the pixel's capacitance will be discharged at a low rate until the end of the integration time. The pixel output voltage change which is V_{reset}-V_1 will be in proportion to the light intensity illuminated. However for a high photocurrent, I_{ph3}, the capacitance will be discharged at a high rate until it's fully discharged before the end of the integration time. This means the pixel has reached saturation and it would be impossible to measure the light intensity from V_{fd}.

1.3 Performance metrics

Several key metrics are used in order to assess the performance of CMOS imagers. In this section, relevant performance metrics when designing a wide dynamic range imager will be reviewed.

1.3.1 Pixel size and fill factor

High resolution is an important factor for high-performance imagers. This is possible by virtue of CMOS technology scaling. As a result, a pixel as small as 1.12 μm [26] has been proposed. In addition, several design methods have been adopted to reduce the size of a pixel. The methods include using minimum number and dimension of transistors. Other method includes employing $nMOS$ only transistors to avoid additional n-Well and implementing shared pixels architecture [27]. These are methods that are within the control of pixel designers.

The size of the pixel also defines the pixel's fill factor which is another important metric. The fill factor is a ratio of the pixel's photosensitive area to the total pixel size. This ratio can be expressed as:

$$Fill factor(\%) = \frac{A_{pd}}{A_{pixel}} \times 100 \tag{1.2}$$

Additional transistors may be included to perform pre-processing on the pixel level or increase other aspects of the pixel performance. However, adding transistors means reducing silicon area of the photodiode and therefore decreasing the fill factor. The fill factor can also be understood as the spatial sensitivity of the pixel. If all the illuminated light is directed to the photodiode, the pixel has a maximum spatial sensitivity. However, due to non-photosensitive components present in the pixel, some portion of the light is lost. With the advance of the CMOS image sensor process, solutions such as 3D stacked image sensors and microlenses to address this issue are employed at a higher cost [1, 28].

1.3.2 Dynamic range

The ability of an imager to capture natural scenes that have both bright and dark exposures can be measured by dynamic range. Natural scenes have a contrast of up

Condition	Illuminance (lux)
Clear night sky	0.001
Quarter moon	0.01
Full moon	0.1
Late twilight	1
Twilight	10
Heavy overcast	100
Overcast sky	1,000
Full daylight	10,000
Direct sunlight	100,000

Table 1.1: Light intensity in real world scenes [3].

to 1:10^8 as recorded in Table 1.1. The dynamic range of a pixel is a ratio between the maximum detectable light intensity before saturation to minimum detectable light intensity. The highest light intensity that can be captured is determined by the maximum photo-generated charge accumulated by a well capacity of a pixel. The functions of the well capacity are to collect the electron charge and convert it to a voltage level. The well capacity collects the charge during a specific time when the pixel is in integration mode. At the end of the integration time, the voltage level corresponds to the amount of the collected charge is read out. If the well capacity is full, any additional charge is overflowed and the pixel is known to be in saturation. When the pixel is saturated, any additional charges become indistinguishable and this limits the maximum light intensity that can be detected.

On the other hand, the smallest detectable signal of the pixel is set by the amount of background noise present during dark which is known as dark current. The major contribution of the dark current is due to thermally generated leakage current of the photodiode. When the pixel is exposed to light, the lowest light intensity that can be detected with the presence of the dark current defines the minimum detectable light intensity. The dynamic range can be defined in dB as [29]:

$$DR = 20 \log \frac{N_{FW}}{n_{floor}} \tag{1.3}$$

where N_{FW} is the full well capacity level and n_{floor} is the root mean square (rms) noise floor level measured in electrons or volts.

1.4 CMOS imager non-idealities

The key metrics presented previously are design specifications that are well under the control of circuit designers. However, CMOS imagers are also affected by technology related non-idealities that limit their performance. These non-idealities are dark current, fixed pattern noise and temporal noise. The sources of these non-idealities need to be understood in order to perform necessary corrections.

1.4.1 Dark current

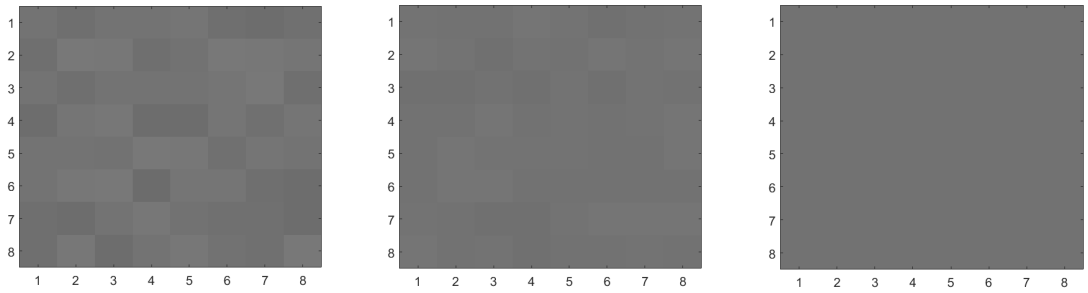
In an ideal case, the output of the pixel only corresponds to the photo-generated current in order to measure the intensity of the incident light. However, it has been demonstrated that there is an additional current contributed by the leakage current of the photodiode [30, 31]. The impact of this leakage current becomes more prominent at low light conditions when it dominates the total current. The leakage current is known as dark current due to its presence in the absence of incident light. The origins of dark current can be divided into three sources which are owed to thermally generated charge in the depletion region, injection-diffusion current at the edges of the depletion region and surface defects at n+ diffusion field oxide interface due to stress during trench formation [32, 31].

1.4.2 Fixed pattern noise

High spatial resolution of CMOS imagers leads to small pixel size design. However, implementing pixels using devices with minimum size means the performance of the pixel response becomes more susceptible to device mismatches and process parameter variations. These variations lead to pixel response non-uniformity which is time independent. In particular, each pixel responds slightly differently to the same light incident resulting in a salt-and-pepper pattern. This characteristic is known as fixed pattern noise (FPN).

The effect of FPN can be categorised into two components which are Dark Signal Non-Uniformity (DSNU) and Photoresponse Non-Uniformity (PRNU) [4]. The first component is pixel-to-pixel variations that arise irrespective of light conditions. These variations are caused by different values of dark current and device parameters such as threshold voltage. On the other hand, PRNU is illumination dependent. For instance, one major source of PRNU is caused by variations of photodiode conversion gain that is dependent on the photodiode area. In addition, device mismatches can lead to different values of buffer gain in each pixel as well as current biases at the column level. The contributions of both DSNU and PRNU can be modelled as offset (additive) and gain (multiplicative) FPN [33].

Unfortunately, there is no standard unit used to measure FPN. For example, some units used to quantify FPN include percentage of root mean square over total output swing [34], lowest significant bits [35], mV [36] and percentage of a logarithmic decade [37]. If no information about photoresponse or imaging system used, it would make comparing FPN values difficult. In addition, all the listed units are used to measure FPN in relation to the pixel output. However, the effect of FPN from a user's experience is more meaningful and also needs to be considered. In particular, human visual system perceives the effect of FPN in terms of differences of intensity levels between pixels in an image. When the intensity levels exceed the minimum contrast threshold,



(a) Image with 5% error (b) Image with 2% error (c) Original image

Figure 1.6: Effect of FPN on an image by 5% and 2% illumination error from the original image.

then the effect of FPN becomes apparent. Choubey and Collins have proposed percentage contrast threshold as a unit to measure FPN [38]. It quantifies the difference of illumination from the ideal value. An image is considered of high quality when its illumination error is less than 2% [39]. To quantify the error qualitatively, the effect of illumination error for 5% and 2% of an 8x8 pixel array on a uniform scene are shown in Figure 1.6. The figures show a notable difference between the images with 5% and 2% error. However the image with 2% has less apparent errors such that it is used as a standard level to be considered as of high quality.

1.4.3 Temporal noise

CMOS imagers also suffer from temporal noise which is time-dependent fluctuations in signal levels. The temporal noise can be divided into three sources which are reset noise, 1/f noise and shot noise. At low illumination, reset noise is identified as the major contribution of the temporal noise. However, at high illumination, photon shot noise is dominant [40]. Reset noise is due to voltage uncertainty on pixel's capacitance during reset. It is essentially a thermal noise originated from random thermal motions of electrons in resistive elements [41]. During reset, the thermal noise is sampled on the pixel's capacitance. The total noise voltage across the capacitor can be expressed

as [42]:

$$V_n^2 = \frac{kT}{C} \tag{1.4}$$

where k is the Boltzmann's constant, T is the temperature in Kelvin and C is the pixel's capacitance. The expression above makes reset noise also known as kTC noise. Tian and co-workers have demonstrated that the reset noise can be reduced by half, by using a soft reset technique [40]. This happens when the pixel's floating diffusion is reset to V_{DD}-V_{th}. In addition, reset noise can be removed effectively using correlated double sampling (CDS) [43].

The second source is the 1/f noise. It originates from fluctuations in the conductivity due to carrier traps in semiconductors which capture and release carriers in a random manner [44]. 1/f noise contributes to the overall noise at different pixel operation. For example, during integration, 1/f noise causes fluctuations in photodiode dark current. However, this is relatively small in comparison to the photodiode shot noise. Furthermore, during readout, source follower and row select transistors generate 1/f noise [45]. From a circuit designer's perspective, 1/f noise can be reduced by increasing the channel length of the transistors or reducing the bias current.

Shot noise is caused by the fact that flow of individual photon or electron is discrete and not continuous. The noise can be contributed by photo-generated current and dark current. The average number of particles and error is governed by Poisson statistics [46, 47].

1.5 Dynamic range extension methods

Previously, the operation of the standard APS presented has shown that it suffers from saturation at high light intensity. This limits the ability of the imager to produce high-quality images. Many approaches have been proposed to extend the dynamic

range of imagers. This section aims to review relevant methods that will be the basis of a proposed method of extending the dynamic range. In addition, operations of these different methods will be used in Chapter 4 to compare the performance of each method on a single pixel.

1.5.1 Logarithmic pixel

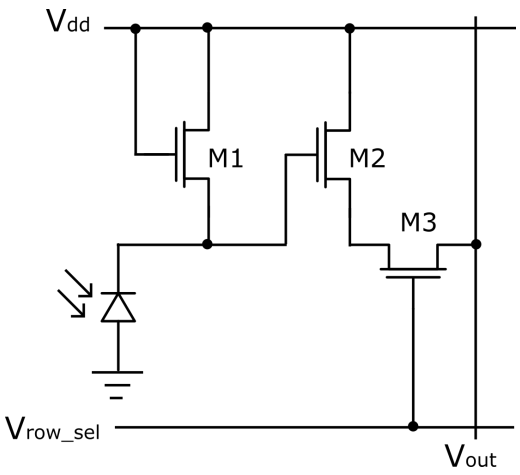


Figure 1.7: A standard three transistor logarithmic pixel.

The logarithmic pixel based upon subthreshold operation of an $nMOS$ transistor, is able to capture light intensities of more than six decades [5]. A logarithmic pixel is shown in Figure 1.7. The pixel is similar to the APS except that the gate and the drain of $M1$ are shorted. A logarithmic output is produced when the load transistor $M1$ operates in weak inversion which has a logarithmic relationship between the source of $M1$ and its drain current. The relationship can be expressed as [48]:

$$V_{S,M1} = V_{DD} - V_{th,M1} - nV_T \cdot \ln(I_{ph}/I_O) \tag{1.5}$$

where I_O and n are process dependant parameters such that I_O is the reverse saturation current, V_T is the thermal voltage kT/q, where k is the Boltzmann constant, T is the absolute temperature and q is the electronic charge.

Equation 1.5 shows that the voltage at the source of $M1$, $V_{S,M1}$ is determined by the intensity of the photocurrent. In addition, the response which is independent of integration time means that the pixel is in continuous operation; therefore the pixels can be accessed at a random time. The advantage of the pixel design is its simplicity of pixel operation and architecture. In particular, the pixel which only requires three transistors means it has a pixel size and a fill factor comparable to that of APS. Furthermore, the logarithmic response means the linear integration of light intensities is compressed over a wide dynamic range; hence relaxes the requirement for data read out.

However, one major disadvantage of the pixel is, it is very susceptible to FPN. This is due to its dependence on the threshold voltage, V_{th}. Furthermore, at low illuminations, the pixel suffers from a long settling time [49]. In addition, n and V_T parameters determine the slope of the response. A typical value for the response sensitivity is at approximately 60 mV/decade. The low value means that the response is also highly susceptible to temporal noise. Lai and co-workers have proposed PNP BJT in place of the photodiode in order to increase the sensitivity of the response [50]. This is achieved by exploiting the high gain of BJT which can amplify the photocurrent and hence the output swing. However, using BJT in each pixel introduces another source of FPN.

The continuous operation of logarithmic pixels means simple FPN correction through correlated double sampling (CDS) is not viable. However, several alternative methods have been proposed which include using calibration circuits [34, 21] and modelling each pixel response [39, 51]. The former approach sacrifices the pixel area to accommodate additional transistors, hence reducing the optical performance. The latter approach requires additional memory to store the modelled parameters of each pixel.

1.5.2 Linear-logarithmic (lin-log) pixel

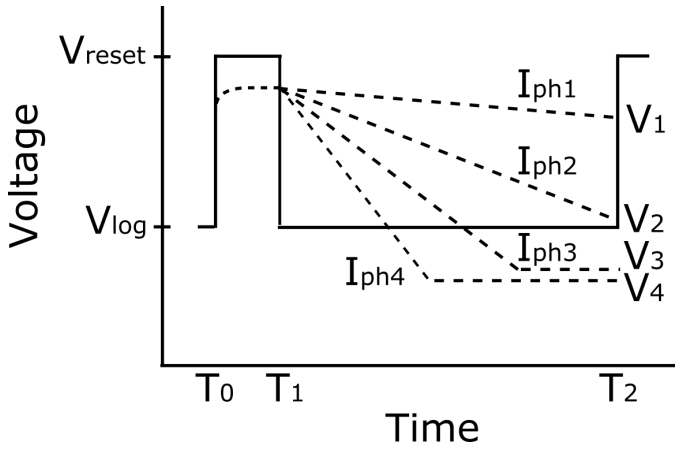


Figure 1.8: A reset signal to generate lin-log response on a standard 3T pixel which shows V_{reset} and V_{log} as an intermediary voltage level [52].

Linear-logarithmic (lin-log) pixel was proposed in order to address the challenges faced by the logarithmic pixel. In particular, a long settling time is required for the logarithmic pixel at low light conditions. This results in artefacts when acquiring images. Lin-log pixel offers a sensitive response at low light intensities by having a linear response. In addition, the response is coupled with a logarithmic response at high light intensities to avoid saturation. To achieve the lin-log response, pixel architectures using three and four transistors have been proposed. The former method was first proposed by Wany and co-workers using standard APS architecture [52]. The reset signal is modified such that after raised high during reset, the voltage drops to an intermediary voltage, V_{log}, as shown in Figure 1.8. This voltage level sets as a threshold for a transition between linear and logarithmic responses. More specifically, for low photocurrent, the pixel will be discharged until the end of integration period without arriving at the corresponding threshold level set by V_{log}. The response is therefore linear. However, for high photocurrent, the pixel will be discharged at a higher rate. This means the response will arrive at the corresponding threshold level of V_{log}-$V_{th,N1}$ before the end of the integration period. The pixel response is therefore logarithmic governed by relationship expressed in Equation 1.5 similar to

the logarithmic pixel. The method, however, requires additional peripheral circuitry in order to generate the reset signal.

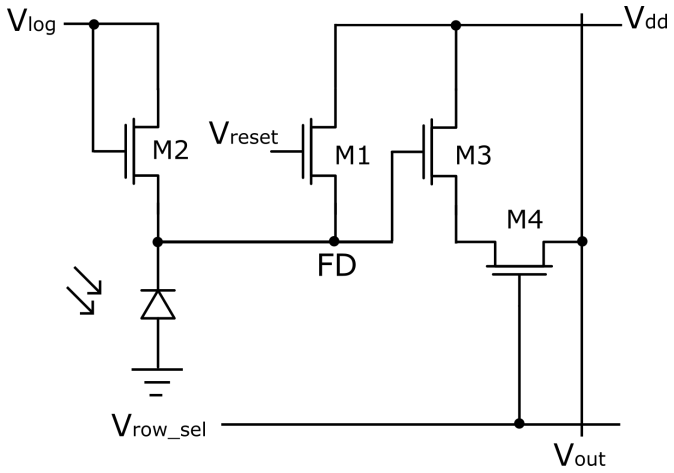


Figure 1.9: Linear-logarithmic pixel using four transistors [49].

A lin-log pixel that does not require additional peripheral circuitry to generate the reset signal has been proposed by Choubey and co-workers as shown in Figure 1.9. The pixel operates on the same principles as the former approach. The difference is an additional transistor $M2$ has its gate and drain shorted to V_{log}. In addition, V_{reset} is a pulse signal similar to that of the standard 3T linear APS. However, the pixel fill factor is slightly reduced on account of the additional transistor.

Although the lin-log pixel solves the long settling time issue by having a linear response at low light illuminations, it still encounters the same issue of low sensitivity at high illuminations due to the subthreshold logarithmic response. In addition, lin-log pixel also experiences high FPN. Methods to reduce FPN that have been proposed include modelling the pixel response [49] and using double sampling [20, 53].

1.5.3 Well capacity adjusting pixel

The maximum amount of photo-generated charge that can be stored in a pixel is determined by its well capacity. Beyond this amount, the well capacity becomes saturated and charge then spills to the diffusion layer. This can be avoided if the well

capacity is increased. One approach that has been proposed is by adding a lateral overflow capacitor in each pixel to integrate the overflowed charge [54]. Using the photodiode to store charges at low light and the additional capacitor to cater for the spilled charges, the pixel maintains its sensitivity at low light intensities while increasing the dynamic range at high light intensities. Furthermore, similar approach has been extended to a column level capacitor [23]. However, both approaches require extra space for the additional capacitor.

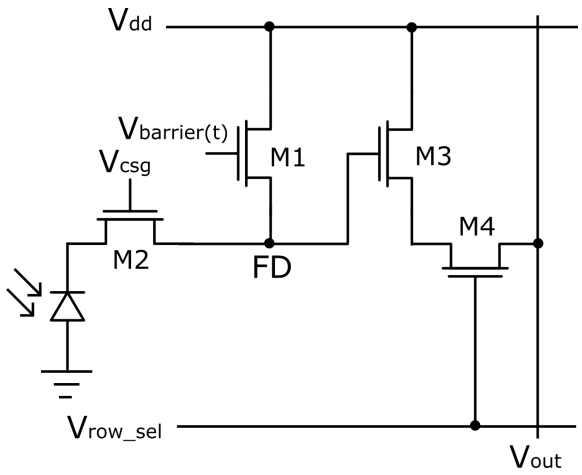


Figure 1.10: A four transistor well capacity adjusting pixel with $M1$ transistor as a barrier gate to control the rate of charge flowing from FD to V_{dd} [55].

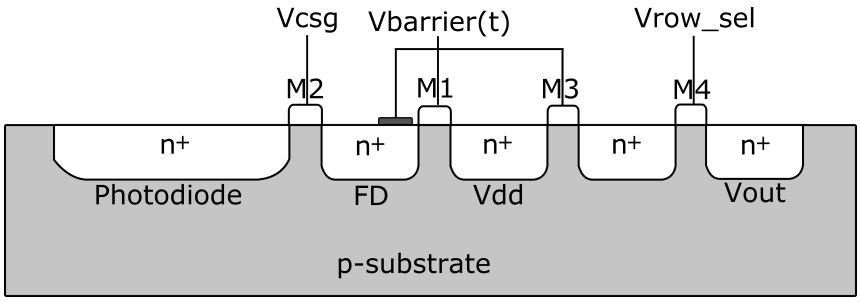
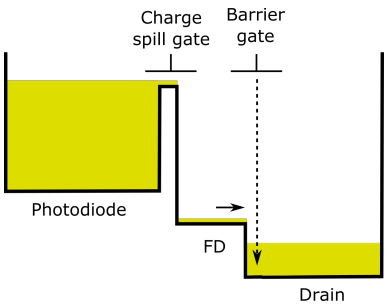


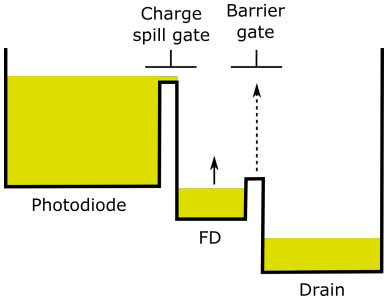
Figure 1.11: A cross sectional view of the four transistor well capacity adjusting pixel from Figure 1.10 [55].

A different approach has been proposed in order to control the effective well capacity of a pixel without adding a capacitor. For example, Decker and co-workers have proposed a 4T pixel as shown in Figure 1.10 where $M1$ is used to control well

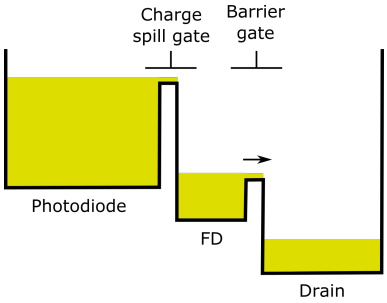
capacity barrier level, $M2$ is to pin the photodiode voltage in order to increase the pixel's low light sensitivity [55]. A cross sectional view of the pixel is depicted in Figure 1.11 for a clearer outlook of the operation of the pixel. The effective well capacity (FD) can be controlled by the gate barrier ($M1$). For example, the barrier level can be adjusted to set different maximum capacity throughout the integration period using a multiple stepped reset signal $V_{barrier(t)}$.



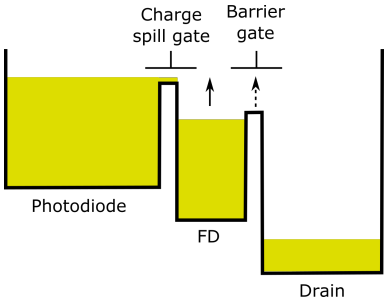
(a) Reset operation when all the charges at FD are transferred to drain



(b) Low light condition: as barrier level is increased at a specific potential, charges are collected at FD



(c) Mid light condition: charges exceeding the barrier level overflow to drain



(d) High light condition: barier is raised to the next level to store more charges to avoid overflow

Figure 1.12: Operation of the well capacity adjusting pixel by controlling the barrier voltage.

The operation of the pixel is shown in Figure 1.12. In Figure 1.12a, the pixel begins with a reset where the gate barrier is lowered. This allows remaining charges in FD from previous exposure to be flushed to the drain (V_{dd}). Then in Figure 1.12b, integration starts and the barrier voltage is raised slightly allowing charges from the photodiode to be transferred and accumulated in FD. Assuming a case for a low light condition, the charges are read out at the end of the integration period. In

Figure 1.12c for a mid-light condition, some of the charges are overflowed and spill into the drain. At this particular light intensity, the spilling of the charges means the pixel response is less sensitive. However, spilling some of the charges is performed in order to allocate some capacity in the well and accumulate charges in a high light illumination; thus avoiding saturation. In Figure 1.12d, in a high light condition, the maximum amount of charge is accumulated in FD as the gate barrier is raised. A larger amount of charges can be accumulated due to the previous charge spilling at the mid light condition. Therefore the dynamic range is extended. This can be achieved when proper selections of number and value of barrier levels are made. However, the main challenge of this approach is its sensitivity drop at its SNR response on account of spilling the charges in mid light intensity [56].

1.5.4 Integrating logarithmic pixel

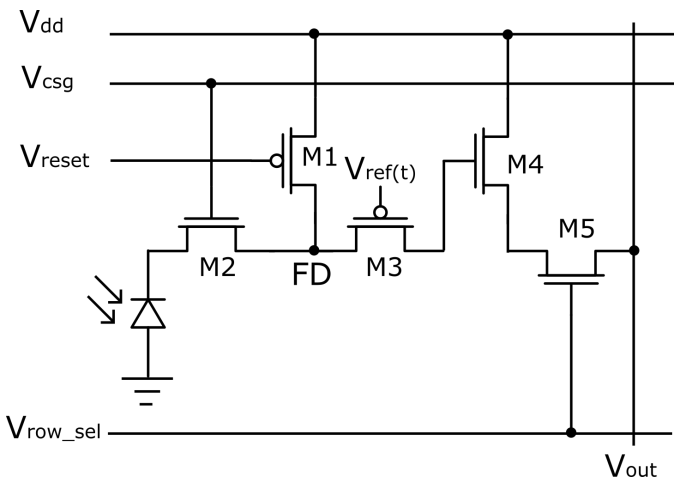


Figure 1.13: A five transistor pixel with a continuous time varying reset voltage $V_{ref}(t)$ to generate an integrating logarithmic response [57].

The integrating logarithmic pixel extends the approach presented in the gate barrier adjusting pixel. In particular, the gate barrier is changing continuously in logarithmic fashion in time instead of discretely at specific times during the integration period. When this happens, the gate barrier changes in a way that adjusts the effec-

tive integration time (i.e. when the pixel integrates linearly) according to the light intensity. More specifically, if a shorter integration time is allocated to the high light condition, then pixel saturation can be avoided. This, in turn, extends the dynamic range. The main advantage of this approach is the associated SNR drops can be avoided. Das and Collins have proposed a five transistor pixel employing a continuous reference voltage $V_{ref}(t)$ to control the gate barrier as shown in Figure 1.13 [58]. $V_{ref}(t)$ is expressed as:

$$V_{ref}(t) = V_{reset} + V_{th} - S \cdot \log_e \left(\frac{I_{ph}(t)}{I_{ref}} \right) \tag{1.6}$$

where S is a logarithmic slope, $I_{ph}(t)$ is photocurrent and I_{ref} is a reference current. The effective integration time is integrated into I_{ph} as a function of time. A dynamic range up to 100 dB has been demonstrated using this approach [59]. The advantage of this approach is the slope of the pixel response can be defined by the user, unlike the standard logarithmic pixel which is dependent on the transistor parameters. However, the proposed integrating logarithmic scheme requires a pixel architecture that uses two $pMOS$ transistors. Employing $pMOS$ in a pixel design means additional space is required for the n-Well. This requirement reduces the pixel fill factor. Using the same principle, Shimonomura and co-workers have proposed a pixel with integrating logarithmic response using all $nMOS$ transistors [60]. However, the $V_{ref}(t)$ model proposed by the group excludes important pixel parameters such as source follower gain and body effect. These parameters are important in order to achieve a well-controlled pixel response. In addition, the application for the pixel was aimed at silicon retina which means, large pixel size was used to perform other functionalities; requiring a total of 87 transistors. The pixel size is 87 x 87 μm^2 with a fill factor of 8.5%.

1.6 Summary

Increasing market demand for high-performance imagers has caused a technological shift in digital imaging from predominantly based on CCD to CMOS for the last two decades. CMOS image sensors offer features such as low power, miniaturised, low cost and the ability to integrate with analogue and digital systems that makes a camera on chip possible. In addition, critical imaging applications such as automotive and security require a specific feature namely wide dynamic range capability. Standard CMOS imagers are unable to capture natural scene faithfully and are limited to 40-60 dB of dynamic range. Furthermore, existing wide dynamic range imagers suffer from either high FPN or sensitivity drops at its SNR. This results in unacceptable illumination error. The work in this thesis attempts to propose a wide dynamic range CMOS imager that can produce high-quality images. To do this, several relevant wide dynamic range methods have been reviewed. The review has examined advantages and disadvantages of each method. From the review, a wide dynamic range imager based on an integrating logarithmic method seems quite promising; in particular, its ability to control the response of the pixel. This method will be the basis of a newly proposed imager with some improvements.

Chapter 2

Integrating logarithmic WDR pixel

2.1 Introduction

In the previous chapter, different approaches to extending the dynamic range of a pixel have been described. One approach, in particular, the integrating logarithmic mode is observed to offer advantages such as the ability to control pixel slope response, maintaining low-light sensitivity, requiring only a few transistors and providing a high signal to noise ratio. The approach extends the dynamic range by controlling the effective integration time. This means that for a high photocurrent, saturation can be avoided by reducing the effective integration time. This chapter proposes an integrating logarithmic pixel that can achieve a wide dynamic range. In particular, a continuously varying reference voltage, $V_{ref}(t)$ is proposed to avoid pixel saturation. First, a new pixel configuration and its operation will be presented. Then a $V_{ref}(t)$ model to control the pixel will be described. An improvement to the initial model will be proposed in order to achieve a well-controlled pixel response. Finally, the adaptability of $V_{ref}(t)$ to control pixel response will be presented.

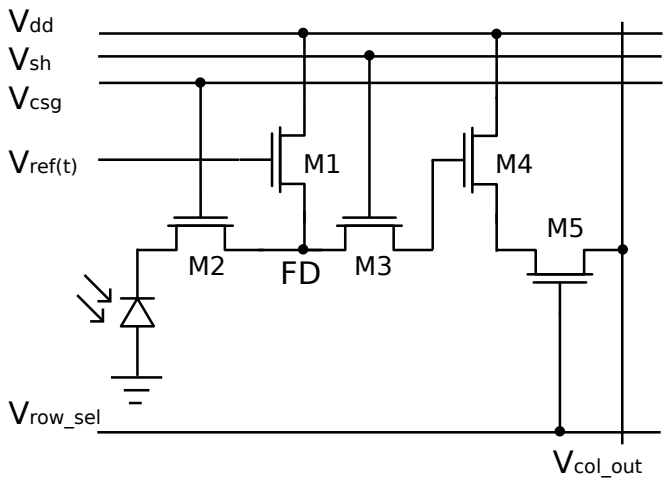


Figure 2.1: Proposed 5 transistor pixel including 2 additional transistors M2 used for an improved low light sensitivity and M3 for a global shutter feature.

2.2 5T pixel

In order to extend the dynamic range of a pixel, an integrating logarithmic scheme aimed at a pixel configuration shown in Figure 2.1 is used. The most important device in the pixel is transistor $M1$. The gate of $M1$ is connected to a continuously varying voltage $V_{ref}(t)$ to control the effective integration time. Furthermore, the source of $M1$ is connected to a floating diffusion (FD) node where its voltage, (V_{FD}), determines the voltage of the pixel. In particular, V_{FD} changes according to charging and discharging activities of parasitic capacitances, C_{FD}, controlled by $V_{ref}(t)$. C_{FD} consists of parasitic capacitances associated with transistors $M1$, $M2$ and $M3$. Transistors $M2$ and $M3$ are additional transistors to the standard 3T pixel. In particular, $M2$ is placed laterally to separate the large photodiode capacitance from C_{FD} by biasing its gate voltage slightly above its V_{th}. Separating the large photodiode capacitance means the effective capacitance of the pixel is reduced which leads to an increased sensitivity at low light conditions [57]. Then $M3$ is placed between FD node and the input of the source follower $M4$ where it can be used as a switch to offer a global shutter feature for a snapshot imaging [61, 62]. In a standard single pixel operation, this feature is turned off by simply applying a constant V_{dd} at the gate of

$M3$. Finally, $M4$ is a source follower to isolate C_{FD} from column capacitance and $M5$ is a switch connected to a column current source to access to the pixel column line.

The pixel operation begins with a reset period when $V_{ref}(t)$ is set high to V_{dd}. In the pixel implementation, $nMOS$ is used as the reset transistor. Using $nMOS$ means during the reset period when both the drain and gate voltages are held at V_{dd}, the maximum voltage applied to FD node is V_{dd}-$V_{th,M1}$. This leads to a decreased output range of the pixel. Then during the integration period, $V_{ref}(t)$ slowly decreases until the end of integration time arriving at a particular voltage. As this happens, C_{FD} is discharged at a rate restrained by $V_{ref}(t)$ due to the fact that V_{FD}=$V_{ref}(t)$-V_{th}. V_{FD} will keep tracking $V_{ref}(t)$ until at a time t, when the discharging current is unable to discharge C_{FD} as quickly as the rate of change of $V_{ref}(t)$. When this happens, $M1$ will stop conducting as $V_{ref}(t)$-V_{FD} is less than its $V_{th,M1}$. The pixel capacitance C_{FD} is then linearly discharged until the end of the integration time. For a high photocurrent, the time t where linear discharge begins is much later during the integration period as opposed to a low photocurrent. This means high photocurrent has a shorter linear integration period, hence saturation can be avoided.

2.3 Reference voltage, $V_{ref}(t)$

A continuously varying reference voltage $V_{ref}(t)$ that is applied to the gate of $M1$ needs to be defined to achieve a wide dynamic range pixel response. In particular, $V_{ref}(t)$ needs to be designed to achieve a pixel response that depends upon the logarithm of the photocurrent. A continuously varying voltage $V_{ref}(t)$ that creates a logarithmic response has been proposed by Shimonomura and co-workers [60]. However, the $V_{ref}(t)$ does not take into account pixel parameters that can affect the slope of the pixel response. A study by Das and co-workers [63] has demonstrated that in

order to obtain a well-controlled pixel response, pixel parameters such as the source follower gain and the body effect need to be considered. To measure how much the pixel parameters will affect the slope of the pixel response, the original $V_{ref}(t)$ model first needs to be studied. The $V_{ref}(t)$ is defined as [60]:

$$V_{ref}(t) = \alpha + \beta \log(T_{int} - t) \tag{2.1}$$

for $t = 0$ to t=$[(w-1)/w]T_{int}$ where

$$\alpha = V_{max} - \frac{V_{max} - V_{min}}{\log(w)} \log(T_{int}) \tag{2.2}$$

$$\beta = \frac{V_{max} - V_{min}}{\log(w)} \tag{2.3}$$

where T_{int} is the integration time, $\log(w)$ is the desired dynamic range, V_{max} and V_{min} are the maximum and the minimum voltages of $V_{ref}(t)$. Equations 2.1, 2.2 and 2.3 can be rearranged and simplified to be:

$$V_{ref}(t) = V_{max} - \beta \log(\frac{T_{int}}{T_{int} - t}) \tag{2.4}$$

Equation 2.4 indicates that at a time zero, $V_{ref}(t)$ starts at a reset level determined by V_{max} before slowly decreases logarithmically as time progresses. The rate of the decrease is controlled by β. Alternatively, β can be considered as the slope of the logarithmic change. To generate $V_{ref}(t)$, values for the reset level, the targeted dynamic range and the slope of the pixel response need to be selected. The value for the reset level is 3.3 V, the dynamic range is six decades and the slope of pixel response is 350 mV/decade. The slope of the pixel response can be defined by a user that is constrained by the pixel's output swing and dynamic range. $V_{ref}(t)$ was generated in Matlab with an integration time of 20 ms. In addition, a reset period of

5 ms and a readout period of 2 ms were added before and after the integration period to simulate an actual pixel response.

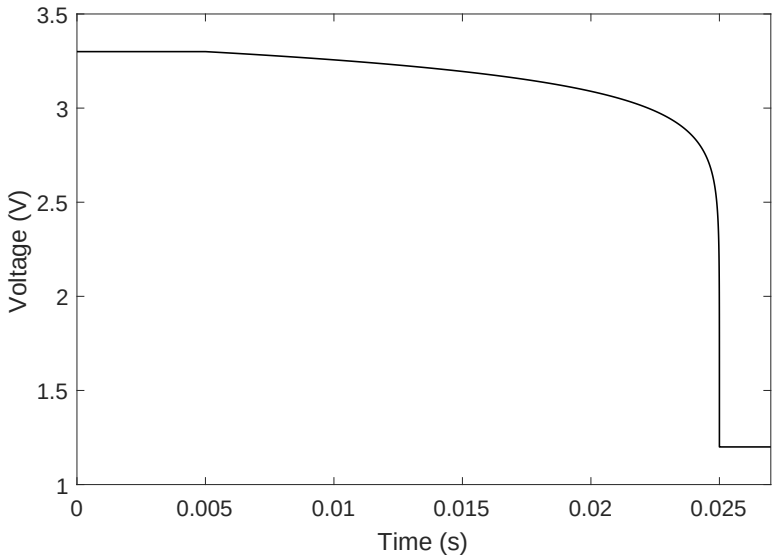


Figure 2.2: $V_{ref}(t)$ model from Equation 2.4 generated using Matlab with a slope of 350 mV/decade and integration time of 20 ms.

Figure 2.2 shows $V_{ref}(t)$ with an integration time of 20 ms and a slope value of 350 mV/decade. The figure shows that as $V_{ref}(t)$ decreases, the rate of change of $V_{ref}(t)$ increases logarithmically towards the end of the integration period. $V_{ref}(t)$ is then, used as an input to the gate of $M1$ in the pixel. The 5T pixel was simulated in Cadence Spectre using UMC 180 nm 3.3V technology process. All the transistors *M1* to *M5* are sized using the minimum geometry (240nm/340nm) to maximise the pixels fill factor. The output of the pixel is connected to a column bus biased by a current source transistor which has a dimension of (2μm/1μm). The pixel was simulated with photocurrent ranging from 0.1 fA to 1 nA. The output values of the pixel are shown in Figure 2.3.

The figure shows a simulated pixel response which was aimed at a slope of 350 mV/decade. The pixel response covered up to 7 decades of dynamic range. A closer inspection reveals that the pixel response has a linear region at low photocurrent

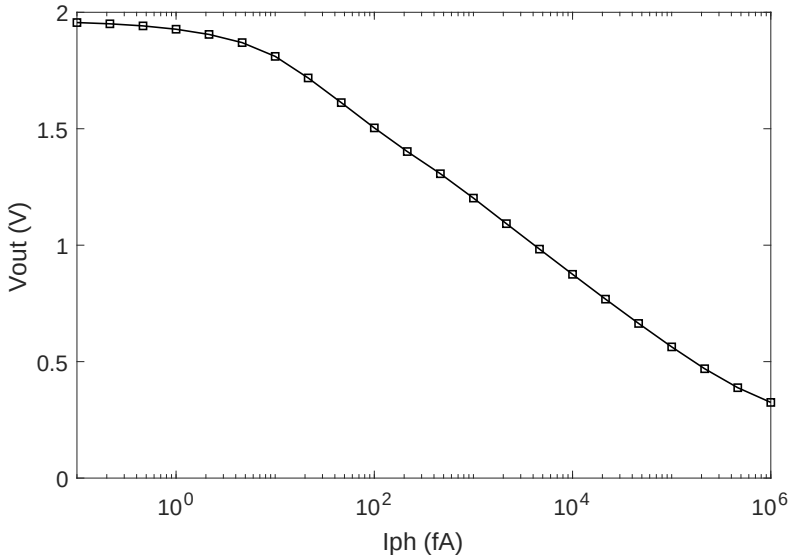


Figure 2.3: Pixel response aimed at 350 mV/decade achieving 315 mV/decade due to non-ideal effects.

below approximately 2 fA. Photocurrent in this region integrates linearly at the start of the integration period and fails to track the logarithmic change of $V_{ref}(t)$. After the linear region, the pixel response falls at a higher slope for more than 5 decades of the dynamic range. The response is logarithmic and the slope of the response is expected to be 350 mV/decade as defined in $V_{ref}(t)$ previously. To measure the slope of the pixel response, two values of the photocurrent and their corresponding voltage values are selected from the logarithmic region where the slope can be defined as:

$$Slope = \left| \frac{V_{ph2} - V_{ph1}}{\log(I_{ph2}) - \log(I_{ph1})} \right| \tag{2.5}$$

Using two values from the logarithmic region in Equation 2.5 produces a slope of 315 mV/decade. This value is equivalent to 10 % error from the targeted slope of 350 mV/decade. The error is expected when the pixels parameters are not taken into account in $V_{ref}(t)$ equation. Therefore, pixel parameters such as the subthreshold slope, source follower gain and body effect need to be extracted and taken into account. When these parameters are considered, the slope of the pixel response is

expected to match the value defined in $V_{ref}(t)$.

2.4 Parameter extraction

In the previous section, a reference voltage model $V_{ref}(t)$ to generate a wide dynamic range pixel response has been explored. However, the slope of the pixel response obtained has 10% error from the targeted value. The $V_{ref}(t)$ model does not consider pixel parameters that affect the slope of the pixel response. These parameters are source follower gain, subthreshold slope and body effect. In order to study the effect of these parameters, the parameters need to be extracted and then included in the original $V_{ref}(t)$ model.

2.4.1 Source follower gain and offset

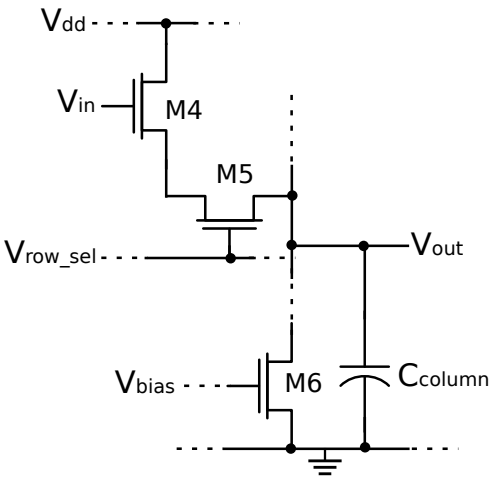


Figure 2.4: Schematic of the input and the output of the pixel's source follower.

Figure 2.4 shows the readout stage of the pixel. The gate of $M4$ is connected to the floating diffusion node in the original pixel. However, in order to analyse the source follower, the gate is connected to an external voltage source V_{in}. The drain of $M4$ is connected to V_{dd} and its source is connected to a column bus through the transistor $M5$. The column bus is biased by a current source transistor $M6$. The

source follower configuration means that the source of $M4$ is able to track any voltage change at its gate due to having a high input impedance and low output impedance. In particular, the source follower acts as a voltage buffer separating the pixel from a large column capacitance at the output node. In addition, the column bus has a large capacitance, C_{column} at a typical value of 1 pF. During the pixel operation, this capacitance will be charged and discharged accordingly. In order to determine the appropriate bias current at the column, the times required to charge and discharge the capacitance have to be faster than the sampling rate of the data acquisition systems to be used. To measure the charge and discharge time, V_{in} is sourced with a pulsed voltage and the source current is biased at 2 μA with a current mirror. When selecting the current value, a trade-off between high current, which leads to a faster charging and discharging activity with a large pixel output range was considered. The output of the pixel is shown in Figure 2.5. This figure shows that during charging, the voltage rises exponentially and takes about 200 ns to charge C_{column}. In comparison discharging time decreases linearly and takes about 1 μs.

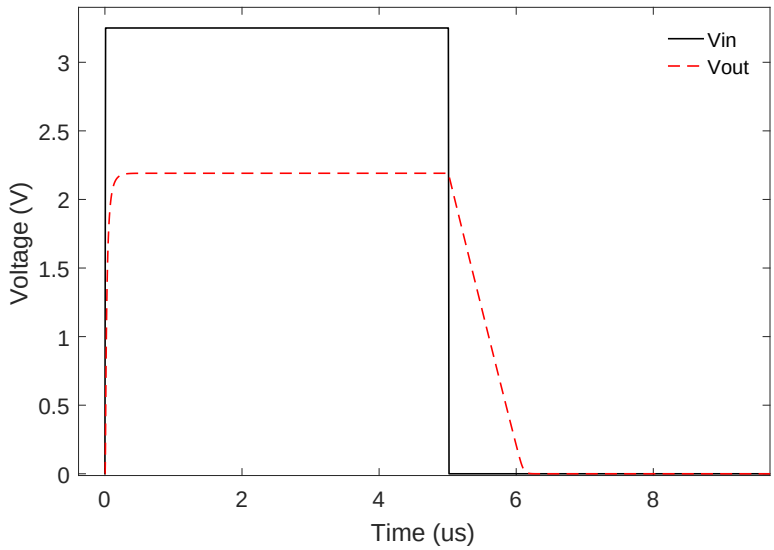


Figure 2.5: Transient response of the column capacitance during charge and discharge operation.

Having a source follower in the pixel means that its non-unity gain will affect the slope of the pixel response. However, in Equation 2.4, the source follower gain was not considered. To measure the source follower gain, first the saturation region of M_4 is determined. This can be done by sourcing V_{in} with a ramp voltage varying from 0 V to 3.3 V. The result is shown in Figure 2.6 which illustrates that the saturation region begins approximately at 1 V. At this region, the drain-source current stays approximately at 2 μA and increases slightly due to a channel length modulation effect. In addition, the saturation region determines the operating region of the source follower input.

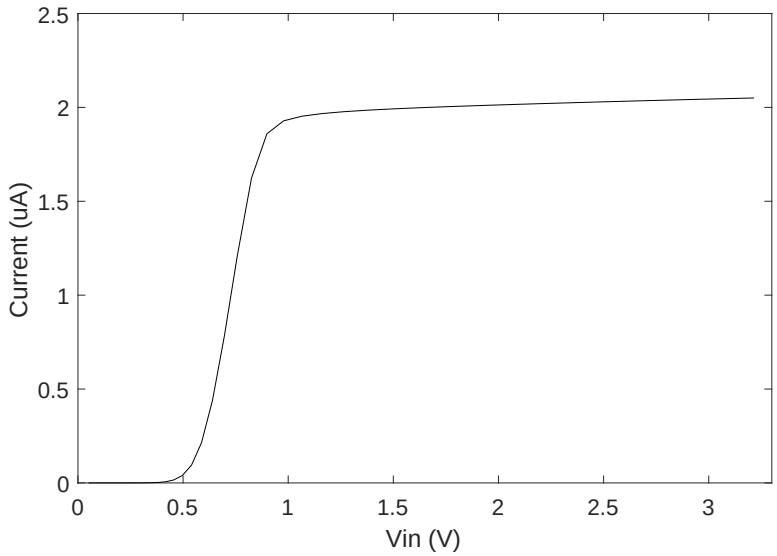


Figure 2.6: Bias current at the pixel column to determine the pixel operation region.

Figure 2.7 shows pixel output response as V_{in} is varied from 1 V to 3.3 V. The output voltage ranges from 200 mV to 2.1 V which is equivalent to 1.9 V range. Furthermore, the output voltage can be linearly fitted so that the source follower gain and offset can be characterised as:

$$V_{out} = 0.88V_{in} - 0.68 \tag{2.6}$$

Equation 2.6 shows that the slope of the source follower is 0.88 V/V. In addition,

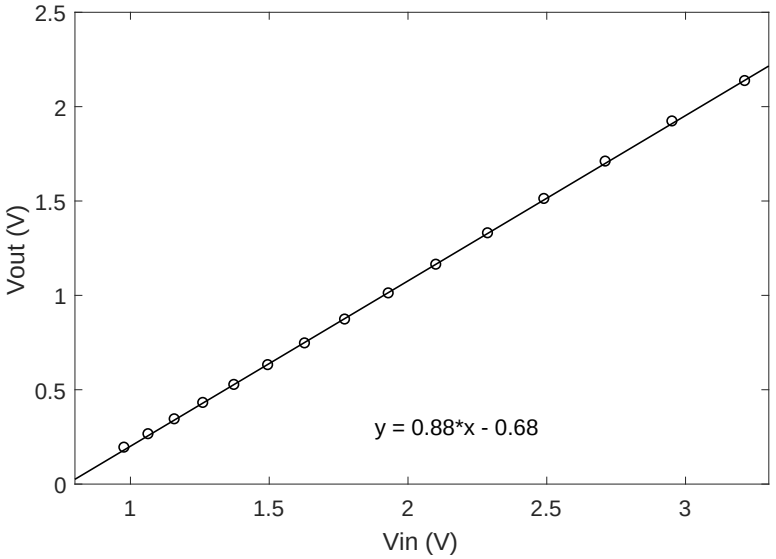


Figure 2.7: Input output voltage of source follower transistor.

the output voltage is shifted down by 0.68 V from the input voltage. All parameters of the source follower are summarised in Table 2.1. The source follower slope therefore needs to be included into $V_{ref}(t)$ by accounting for a higher slope such that:

$$\beta'' = \frac{\beta'}{SFgain} \tag{2.7}$$

Parameter	Value
Input Range	1V-3.3V
Output Range	0.2V-2.1V
Gain	0.88V/V
Offset	-0.68V
Bias Current	2μV

Table 2.1: Source follower parameters.

2.4.2 Voltage subthreshold slope

The V_{reset} in the reference voltage sets the reset level of the pixel during the reset period. For a $pMOS$ reset transistor, the reset level can be raised up to V_{dd}. However,

the main disadvantage of using $pMOS$ is the large area required to form a separated n-Well inside the pixel. This requirement makes $nMOS$ a preferred transistor for the reset device. Using $nMOS$ for reset operation means that the pixel value during reset is less than V_{reset} and it is also dependent on the photocurrent. In addition, the range of photocurrent available in natural scenes, which is limited to small values means that the reset transistor $M1$ is operating in weak inversion. The photocurrent, therefore, can be approximated as [6]:

$$I_{ph} = I_o e^{\frac{Vg - Vs - V_{th,M1}}{nV_t}} \tag{2.8}$$

where V_g is the gate voltage, V_s is the source voltage, $V_{th,M1}$ is the threshold voltage. Parameters I_o and n are process dependent with I_o also dependent on the size of $M1$. The voltage V_t is the thermal voltage kT/q. From Equation 2.8, the effect of varying photocurrent on the source voltage V_s, which is also known as V_{FD} in the pixel is:

$$V_{FD} = V_{g,M1} - V_{th,M1} - nV_t \ln(\frac{I_{ph}}{I_o}) \tag{2.9}$$

Equation 2.9 shows that the pixel's reset level is dependent on the logarithm of the photocurrent. For example, a high photocurrent is expected to have a lower reset value than a low photocurrent. The decrease of the reset value as photocurrent increases is equivalent to a subthreshold slope in a standard logarithmic pixel. The effect from the subthreshold slope is an additional slope of approximately 60 mV/decade from the expected slope. To account for this effect, the subthreshold slope needs to be subtracted from the slope defined in $V_{ref}(t)$ such that:

$$\beta' = \beta - V_{subth-drop} \tag{2.10}$$

To measure the effect of varying the photocurrent on the pixel response, a DC voltage of 3.3 V is sourced to the gate of *M1*. The photocurrent is varied from 1 fA

to 1 nA and V_{FD} is recorded after 50 ms at each photocurrent. The simulation result is depicted in Figure 2.8.

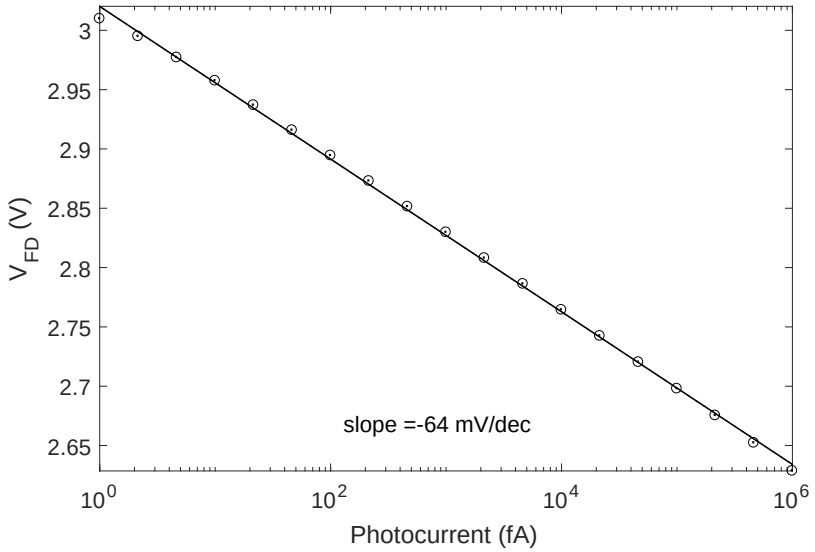


Figure 2.8: Subthreshold slope measured at V_{FD} node.

The figure shows that V_{FD} decreases when photocurrent is increased as expected. In addition, the slope of the pixel response is -64 mV/decade. The impact of this subthreshold slope will cause a slope error on the final pixel response from the defined slope parameters in $V_{ref}(t)$. The value of the subthreshold slope, therefore, is accounted as defined in Equation 2.10.

2.4.3 Body effect

The original $V_{ref}(t)$ in Equation 2.4 does not consider the threshold voltage of transistor $M1$. Furthermore, applying $V_{ref}(t)$ on the transistor M1 means its response is dependent on the transistor's parameters. One of the non-ideal parameters that needs to be considered is the body effect. The effect occurs due to the body of $M1$ tied to the *gnd* rather than its source. When this happens, the body effect causes the threshold voltage to vary in proportion to $V_{ref}(t)$ variation. One way to avoid this effect is by employing a $pMOS$ transistor as the reset transistor [64]. A $pMOS$

will allow a connection between the bulk in a separated n-well and the source, hence avoiding the body effect. However, having a separated well means extra space is required. An $nMOS$ transistor is therefore preferred and its body effect needs to be characterised. The relationship between a transistor's threshold voltage with respect to its bulk is defined as [65]:

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) \tag{2.11}$$

where V_{TH0} is the threshold voltage when V_{SB} is zero and γ is the body effect coefficient and ϕ_F is the Fermi potential.

Equation 2.11 shows that V_{SB} has a square-root relationship with respect to V_{TH}. V_{SB} increases as a result of the potential difference between the source and the bulk grows and therefore the threshold voltage is expected to increase. This effect will impact the effective voltage of $V_{ref}(t)$ applied on the floating diffusion node. To measure this effect on the pixel, $V_{ref}(t)$ was sourced with a DC voltage varied from 0.9 V to 3.3 V with 0.2 V increment. At each voltage increment, V_{FD} was recorded after 20 ms. Then, the gate-source voltage difference,V_{gs} is measured by subtracting V_{FD} from $V_{ref}(t)$.

The simulation result in Figure 2.9 shows that when $V_{ref}(t)$ increases, $V_{ref} - V_{FD}$ also increases as expected instead of being constant due to the body effect. Although the effect is not perfectly linear, the body effect can be linearly fitted in order to simplify the $V_{ref}(t)$ model such that:

$$V_{th,M1} = \sigma V_{ref} + \gamma \tag{2.12}$$

where σ is the slope of the threshold voltage variation of $M1$ with respect to $V_{ref}(t)$ and γ is the threshold voltage of $M1$ when $V_{ref}(t)$ is zero. The body effect is therefore characterised as:

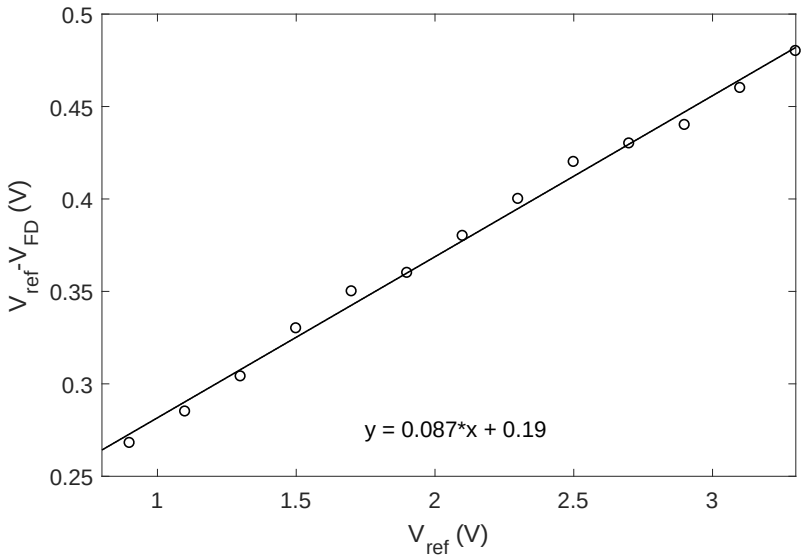


Figure 2.9: Body effect of the reset transistor.

$$V_{th,M1} = 0.087 \times V_{ref} + 0.19 \tag{2.13}$$

2.5 Pixel response

Previously, it was observed in Figure 2.3 that the current $V_{ref}(t)$ model has failed to produce a pixel response at the desired slope. The $V_{ref}(t)$ model needs to consider non-ideal pixel parameters such as source follower gain, body effect and subthreshold slope. When these parameters are considered, a well-controlled pixel response is expected to be achieved. Equation 2.4, therefore, is modified to include the pixel parameters in Equation 2.7, 2.10 and 2.12 such that:

$$V_{ref}(t) = V'_{max} - \beta'' \log(\frac{T_{int}}{T_{int} - t}) \tag{2.14}$$

where

$$V'_{max} = \frac{V_{max} + \gamma}{(1 - \sigma)} \quad \text{and} \quad \beta'' = \frac{\beta'}{(1 - \sigma)} \tag{2.15}$$

where V'_{max} is a scaled reset voltage, β" is a scaled slope of pixel response, σ and γ are body effect parameters.

2.5.1 Effect of extracted pixel parameters

All the pixel parameters extracted such as the source follower gain, the body effect and subthreshold slope are shown in Table 2.2. In addition, Table 2.3 shows user-defined parameters such as targeted pixel response slope, reset level and integration period. Both sets of parameters have been used in Equation 2.14 to generate $V_{ref}(t)$ using Matlab. The result of $V_{ref}(t)$ generated in Matlab can be observed from Figure 2.10. In addition, original $V_{ref}(t)$ without the extracted parameters is also depicted in the figure for a comparison.

Extracted Pixel Parameter	Function	Value
Vsubth_drop	Slope of voltage drop at Reset level	64 mV/dec
SFgain	Source follower gain	0.88 V/V
α	Slope of threshold voltage variation of M1 with $V_{ref}(t)$	0.087 V/V
β	Threshold voltage of M1 for reference voltage at $V_{ref}(t)$=0	0.19 V

Table 2.2: Pixel parameters extracted from Cadence to be included in $V_{ref}(t)$ generation.

User Defined Parameters	Function	Value
V_{max}	Reset level	3.3 V
Slope	Slope of pixel response	350 mV/decade
T_{int}	Integration time	20 ms

Table 2.3: User defined parameter values to be included in $V_{ref}(t)$ generation.

Figure 2.10 shows that $V_{ref}(t)$ with the pixel parameter terms is slightly different from the $V_{ref}(t)$ without the pixel parameter terms. In particular, $V_{ref}(t)$ with the

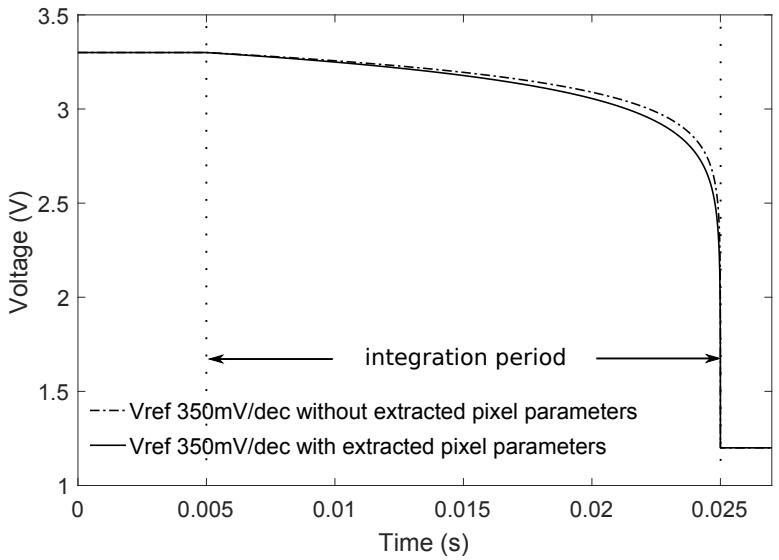


Figure 2.10: Comparison of pixel transient response using $V_{ref}(t)$ with and without extracted pixel parameters.

pixel parameter terms bends slightly downward which means it has a higher rate of change. This difference is expected when the effective slope value is larger which results in a higher rate of change. The effect of the slight difference of $V_{ref}(t)$ with the pixel parameter terms is expected to produce a more accurate slope of the pixel response.

The modified $V_{ref}(t)$ was applied to the pixel and its pixel response was simulated using Cadence. The simulation was done for photocurrent ranged between 0.1 fA to 2 nA and the pixel responses generated from $V_{ref}(t)$ with and without the pixel parameters are shown in Figure 2.11. This figure shows that both pixel responses cover seven decades of dynamic range without saturation. In addition, the output voltage range extends more than 1.7 V. The figure shows that when the photocurrent is low, at a range between 0.1 fA to 2 fA, both pixel responses have a linear response similar to that of a linear pixel. The photocurrents at this range are too small to discharge the pixel's capacitance within the specified integration period. However, when the photocurrent is at approximately 10 fA, both pixel responses start to have a

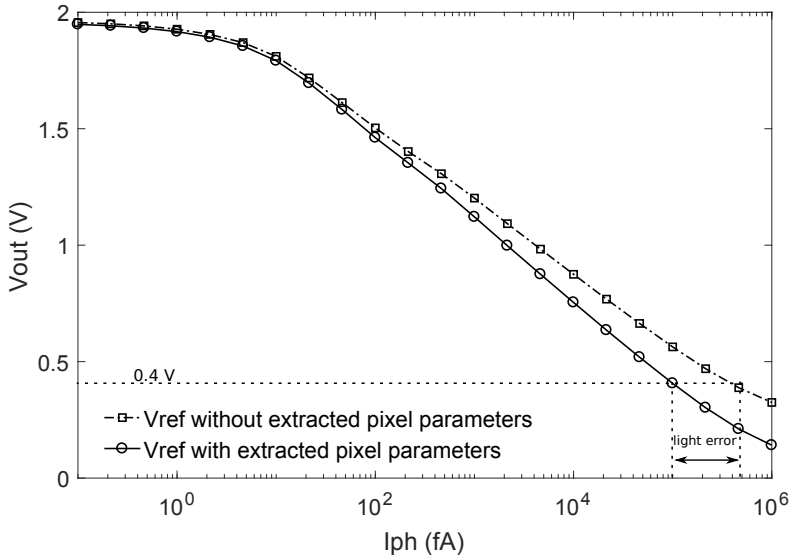


Figure 2.11: Comparison of pixel response using $V_{ref}(t)$ with and without extracted pixel parameters. An example of the effect of the slope error with pixel output at 0.4 V causing light error up to 60%.

logarithmic response with each at a different slope. The slopes of both pixel responses are recorded in Table 2.4. The pixel response generated from $V_{ref}(t)$ without the pixel parameters has a slope response of -315 mV/decade which is 10% error from the targeted slope of -350 mV/decade. When this error is not corrected, it will produce up to 60% of illumination error. For example, based on Figure 2.11, a pixel output value at 0.4 V which is supposed to translate to 100 pA will result in 400 pA because of the slope error. In contrast, the pixel response generated from $V_{ref}(t)$ with pixel parameters produces a slope of -353 mV/dec which equals to 0.5 % error from the targeted slope. In conclusion, it has been demonstrated that the pixel response is dependent on the parameters such as the source follower gain, body effect and subthreshold slope.

2.5.2 Control of $V_{ref}(t)$ slope

The integrating logarithmic approach allows the user to select a desired value for the slope pixel response. The value selection usually depends on the voltage output range

Parameter	Measured Slope	Error
Slope of pixel response of $V_{ref}(t)$ without extracted pixel parameters	-315 mV/dec	10%
Slope of pixel response of $V_{ref}(t)$ with extracted pixel parameters	-353 mV/dec	0.5%

Table 2.4: Comparison of $V_{ref}(t)$ with and without extracted pixel parameters for $V_{ref}(t)$ aiming for -350 mV/dec response.

of the pixel and the dynamic range desired. First, the voltage output range is determined mainly by the power supply voltage and the pixel reset voltage. Furthermore, the dynamic range is selected by the user, according to the specific imaging situation. For example, an application that requires high light sensitivity and robustness towards noise would prioritise the high value of the slope of a pixel response over the wide dynamic range and vice versa. This feature gives the user a flexibility to use the pixel based on the desired application.

To demonstrate the flexibility of the integrating logarithmic approach, additional $V_{ref}(t)$ with slope values of 300 mV/dec, 400 mV/dec and 600 mV/dec have been generated. All other values such as integration time and reset level remained the same. Next, each $V_{ref}(t)$ was used on the pixel with the same range of photocurrent from 0.1 fA to 1 nA.

Parameter (mV/dec)	Measured Slope (mV/dec)	Error (%)
$V_{ref}(t)$ with slope of 300	-304 mV/dec	1.3
$V_{ref}(t)$ with slope of 350	-353 mV/dec	0.86
$V_{ref}(t)$ with slope of 400	-399 mV/dec	0.25
$V_{ref}(t)$ with slope of 600	-601 mV/dec	0.17

Table 2.5: Pixel response slope control at three different values.

The pixel response from each $V_{ref}(t)$ and the previously simulated pixel response are depicted in Figure 2.12. This figure shows pixel responses with four different slopes as expected. In particular, the pixel response which has a slope value of 300

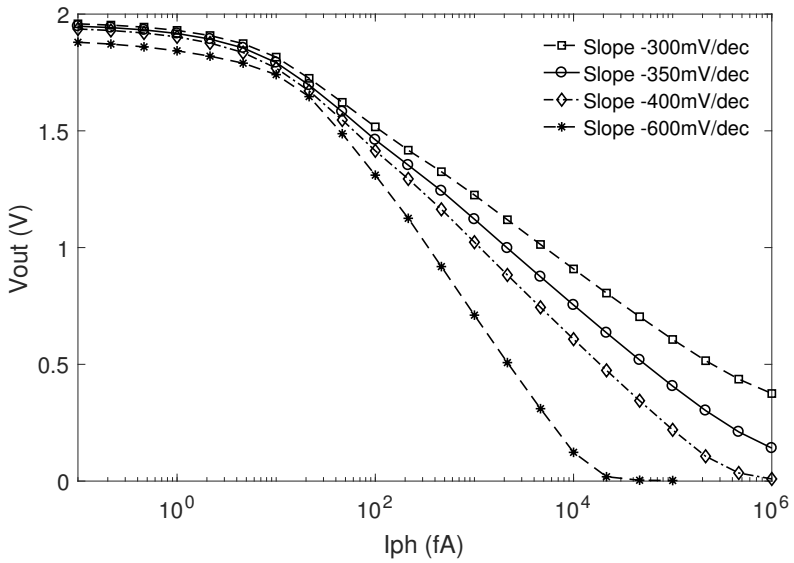


Figure 2.12: Comparison of pixel response using $V_{ref}(t)$ with slopes aimed at 300mV/dec, 350mV/dec, 400mV/dec and 600mV/dec.

mV/dec yields a pixel response with a slope of 304 mV/dec. This slight deviation is equal to 1.3 % error from the expected slope value. The pixel response covers about 1.6 V output range without any saturation. The remaining voltage range of about 400 mV before reaching *gnd* means the dynamic range can further be extended well beyond 1 nA. This feature can be useful for an application intended for a dynamic range of more than 7 decades. In comparison, the pixel response which is aimed at 400 mV/dec covers less than 7 decades of dynamic range before saturation. This is evident from the flat regions nearing the *gnd* at approximately 500 pA and 15 pA respectively. Furthermore, the pixel response yields a slope of 399 mV/dec which is equivalent to 0.25 % from the expected value. Finally, the pixel response that is aimed at 600 mV/dec results in a response of 601 mV/dec. The response covers up to four decades of dynamic range before saturation. Although the dynamic range is limited, the higher slope value is expected to produce higher quality images with better SNR. The results of all the responses are summarised in Table 2.5. In conclusion, the results from Figure 2.12 illustrate that it is possible to control the pixel response from the

modified $V_{ref}(t)$ with minimum error. The modified $V_{ref}(t)$ takes into account the pixel's non-idealities in order to achieve a well-controlled pixel response.

2.6 Summary

A wide dynamic range pixel based on continuously varying reference voltage $V_{ref}(t)$ has been proposed. From the simulation results, a well-controlled pixel response has been demonstrated for a dynamic range of up to 140 dB. In particular, slope errors of less than 1.3% have been demonstrated at three different slope values. Furthermore, an adaptive $V_{ref}(t)$ model means that slope value higher than the conventional logarithmic pixel can be selected. This is an important aspect that can improve the response sensitivity and be more robust to noise. The well-controlled response is possible when the pixel parameters are included into the $V_{ref}(t)$ model. These parameters are source follower gain, subthreshold slope and body effect. From the simulation results, test pixels need to be designed and fabricated. Then, pixel characterisation needs to be performed in order to generate $V_{ref}(t)$. Subsequently, the test pixels need to be measured to confirm that pixel response can be accurately controlled by $V_{ref}(t)$ model.

Chapter 3

Measurement results

3.1 Introduction

Simulation results demonstrated in the previous chapter are quite promising. In particular, the pixel photoresponse has achieved the targeted slope defined in the $V_{ref}(t)$ model. The ability to control the photoresponse is possible when the non-ideal parameters were taken into account. In order to demonstrate the pixel's functionality in the real world, an imager chip prototype containing test pixels is required. This is done through a layout design which then will be fabricated. This chapter first describes the layout design of the pixel. Then the experimental setup for the chip, measurements for pixel characterisation and photoresponse are presented. Finally, photoresponses from test pixels of different chips are measured in order to perform fixed pattern noise (FPN) correction.

3.2 5T Pixel layout

The chip prototype consisting of test pixels was fabricated in 180 nm 1P6M MM Process by United Microelectronics Corporation (UMC). The layout of a 2x1 test pixels is shown in Figure 3.1. Mirroring two pixels together means that the area of

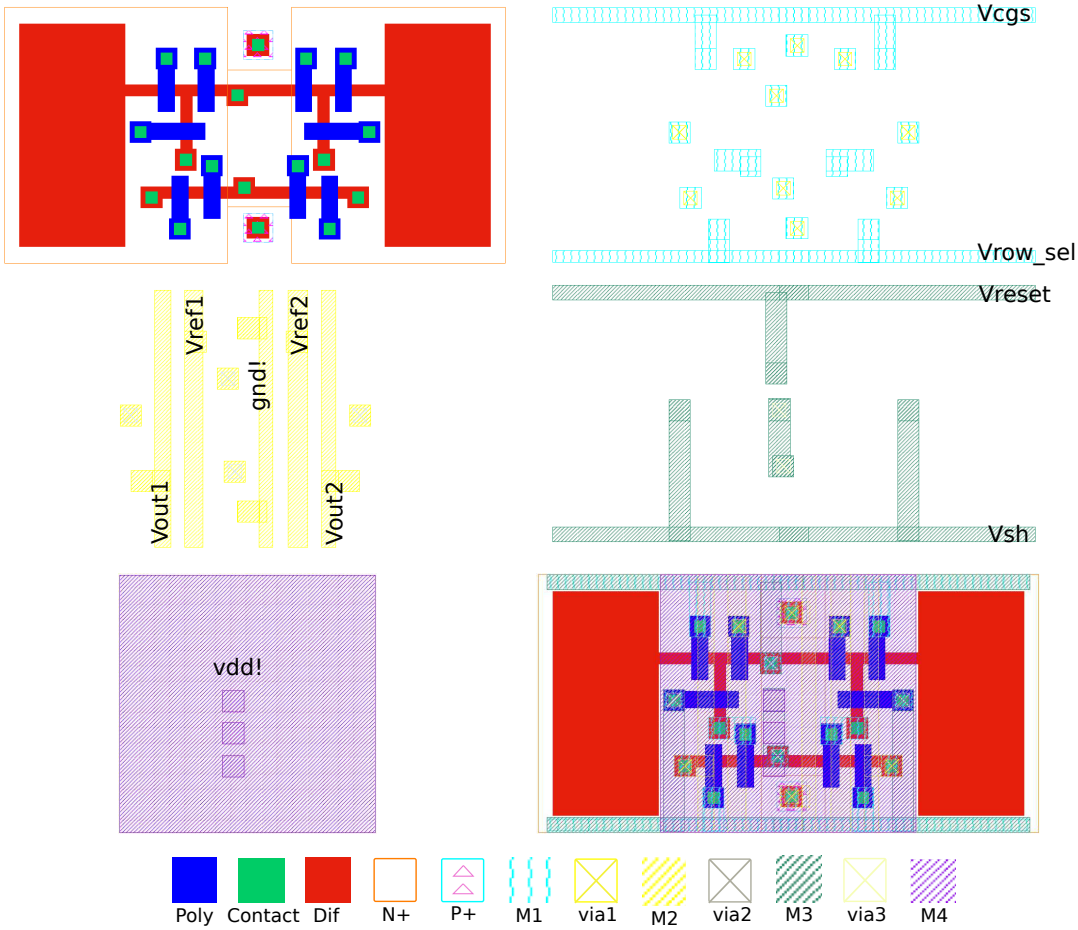


Figure 3.1: Layout of tiled 2x1 5T pixel using UMC 180 nm process to optimise the photosensitive area. Metal 1-3 are used for routing while Metal 4 is used as an optical shield.

the pixel circuitry can be minimised by sharing common signals and grouping the pixel circuitry in the middle. This approach leads to an increase photodiode area; hence the pixel's fill factor. The photodiodes are of N+/P substrate type photodiode located at the left and right of the pixels. Metal 1 to metal 4 are used to route the pixel signals. In particular, metal 4 is used to provide V_{dd} and optical shielding to the pixel circuitry [66]. Metal 5 and 6 which have low sheet resistance are reserved for top-level routing. All the transistors have minimum dimensions of 240 nm/ 340 nm in a pixel size of 5 μm x 5 μm each which leads to a fill factor of 34%.

3.3 Experimental setup

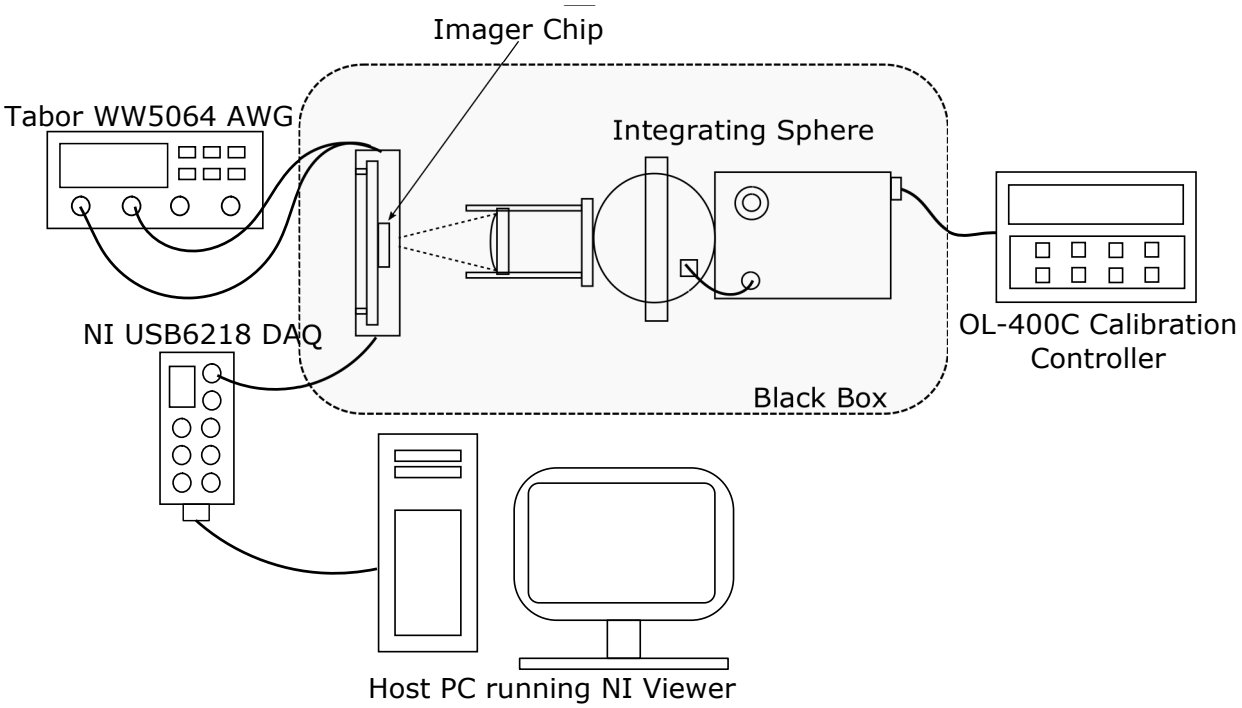


Figure 3.2: Experimental setup for the test pixels characterisation conducted in a light controlled environment.

The experimental setup for the test pixels is illustrated in Figure 3.2. The setup consists of an imager chip, a test board, a light source, a lens and a lens mount, apertures, integrating sphere, light an arbitrary waveform generator (AWG) and a data acquisition system (DAQ) connected to a host PC. The test board holding the imager chip is housed inside an aluminum casing. To provide signal connections to the imager chip, the casing is attached with BNC sockets. The imager chip is illuminated with a high-intensity light source through the integrating sphere to provide a homogenous light distribution. In addition, a photodetector is mounted on the integrating sphere wall to measure the luminance of the light source accurately. In order to reduce optical interference, the setup is placed inside a black box. Outside of the black box, an OL 400C Series Digital Controller is used to control the light source as well as to provide a light measurement from the photodetector. Furthermore, a Tabor

WW5064 series AWG is used to provide necessary input signals to the imager chip. This includes a Matlab generated $V_{ref}(t)$ text file which is fed into the AWG for the signal generation. The AWG provides 4 channels of high-speed signal generator up to 50 MS/s with a 16 bit resolution. The output of the pixel is measured with an NI USB connected 6218 DAQ with an aggregate multichannel sampling rate of 250 kHz. The DAQ offers an analog-to-digital conversion of 16 bit at a full-scale range of ± 5 V with an absolute accuracy of 150 μV. In addition, the DAQ system is connected to a host PC running NI Data Viewer for data collection. The whole experiment process was conducted in a dark room to further avoid any optical interference.

3.4 Parameter extraction

Previously, simulation results have shown that when the pixel's non-ideal effects are taken into account, a well-controlled photoresponse can be obtained. Therefore the parameters of the test pixels such as the source follower gain, subthreshold slope and body effect need to be measured. The parameters can then be used to generate a $V_{ref}(t)$ signal to control the test pixels.

3.4.1 Source follower gain

In order to characterise the source follower, a test pixel with signal assignments illustrated in Figure 3.3 was used. In this pixel, the gate of transistor $M1$, $M3$ and $M5$ are connected to V_{dd}. In addition, the gate of transistor $M2$ is grounded and the gate of transistor $M6$ is connected to a current mirror (not shown in the diagram) with 2 μA of drain-source current. Previously during the circuit simulation, when only the readout stage of the pixel was used, an input voltage $V_{sf,in}$ could be connected directly to the gate of the source follower $M4$. However, when the parameter needs to be extracted from the test pixel, $V_{sf,in}$ has to be connected to the drain of

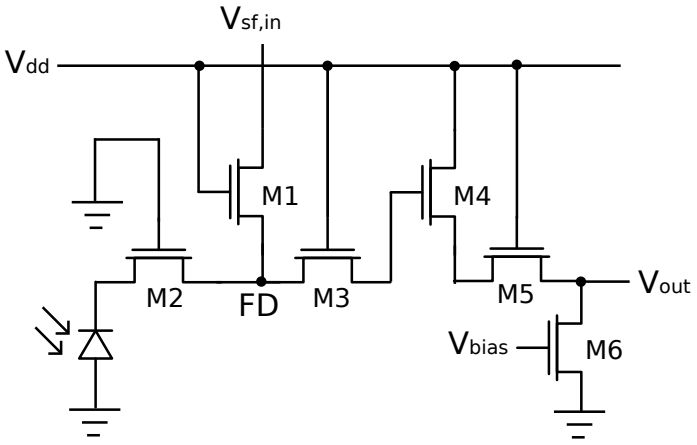


Figure 3.3: Test pixel showing signal assignments for source follower characterisation.

transistor $M1$. Both transistors $M1$ and $M3$ function as $nMOS$ switches during this measurement. One clear disadvantage of an $nMOS$ switch is the output of the switch is slightly less than V_{dd} due to the threshold voltage drop. This will reduce the linear output region of the pixel. However, for the purpose of extracting the gain and the offset of the source follower, this effect can be neglected.

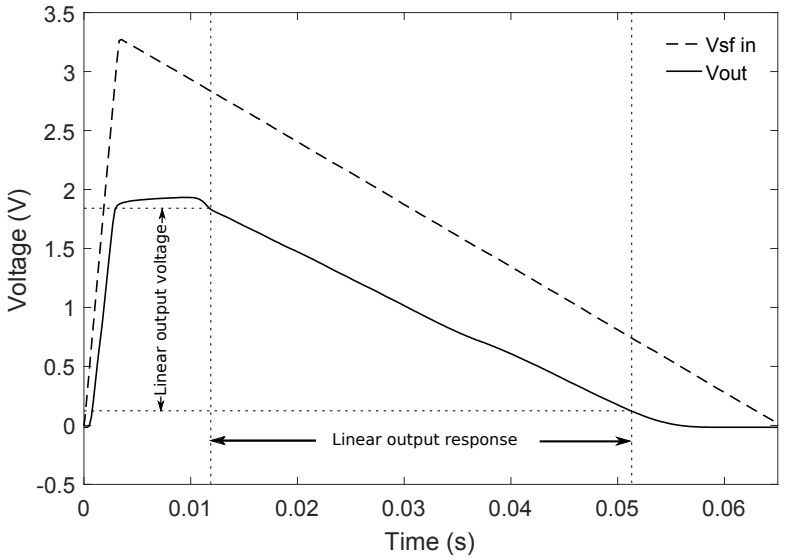


Figure 3.4: Input output response of the source follower transistor at the linear range.

In order to characterise the source follower, $V_{sf,in}$ was ramped slowly from 3.3 V to 0 V. The output of the pixel was measured and is shown in Figure 3.4. The figure

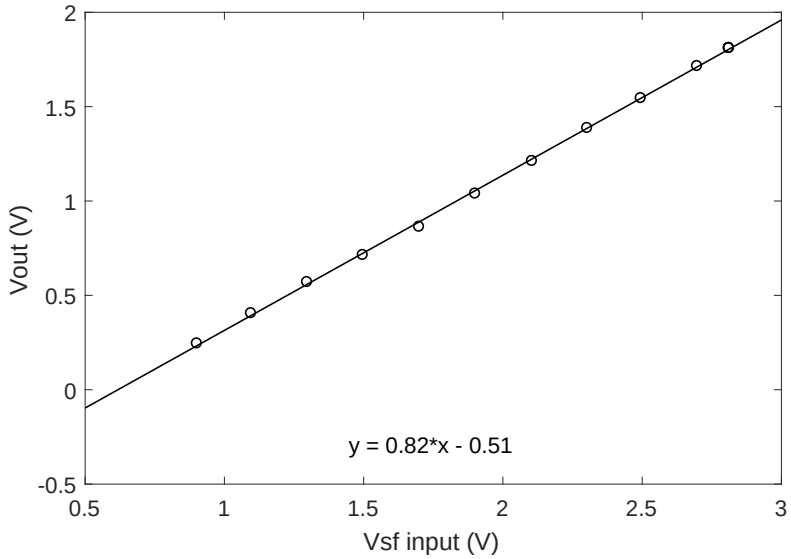


Figure 3.5: Input output response of the source follower transistor at the linear range.

shows that the output is slightly clipped as anticipated due to the use of $nMOS$ switches. The linear output ranges from 150 mV to 1.8 V which corresponds to an input voltage of 0.8 V to 2.8 V. This linear region of input and output is shown in Figure 3.5 to determine the gain and offset of the source follower. The output response can be fitted linearly and is given as:

$$V_{out} = 0.82V_{in} - 0.51 \tag{3.1}$$

The source follower parameters are summarised in Table 3.1

Parameter	Value
Input Range	0.8 V - 2.8 V
Output Range	0.15 V - 1.8 V
Gain	0.82 V/V
Offset	-0.51 V

Table 3.1: Measured parameters of the source follower transistor.

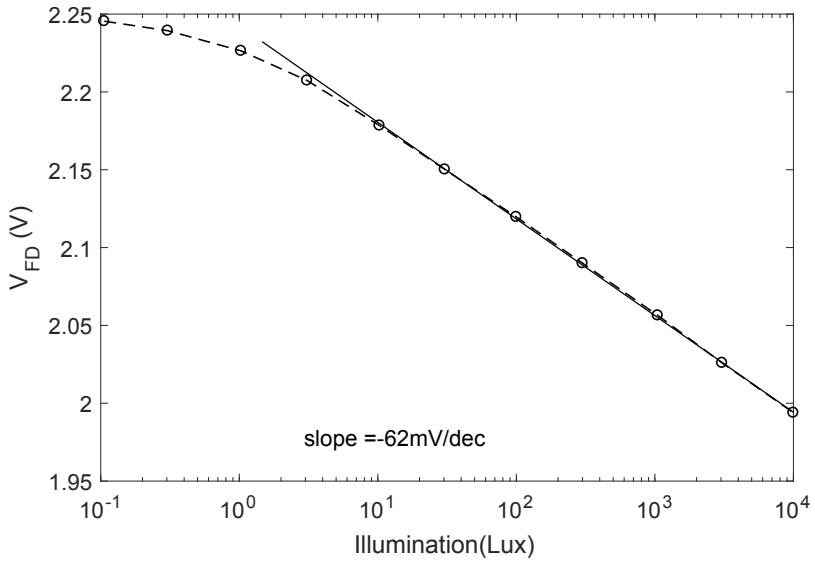


Figure 3.6: Measured subthreshold slope of the pixel.

3.4.2 Subthreshold slope

In order to measure the subthreshold slope, a 3 V DC signal which represents a reset level was applied to the gate of transistor $M1$. Other signals were sourced with similar values during a normal pixel operation. For example, referring to Figure 2.1, V_{cgs} was sourced at 0.5 V while V_{sh} and V_{row_sel} were sourced at 3.3 V. Then the output of the pixel was measured after a period of 20 ms which corresponds to integration period. Each measurement was done at 11 light levels ranging from 0.1 lux to 10 klux.

The $V_{ref}(t)$ equation includes the subthreshold slope parameter measured at the FD node. The FD node could be measured directly during simulation. However, during experiment, the FD node was measured indirectly at the pixel output. When measuring indirectly at the pixel output, one aspect that needs to be considered is the contribution of the source follower gain and offset. This contribution needs to be factored in when determining the value of the subthreshold slope at FD node. Figure 3.6 shows the voltage response at FD node across different illuminations after the source follower contribution measured previously has been taken into account. As expected, at the very low light region, the response is not logarithmic due to the

dark current domination of the photocurrent. This means increasing the light level has a little effect on the overall photocurrent. This effect disappears at a light level from approximately 10 lux where the response starts to become logarithmic. The subthreshold slope is therefore measured at the log region and observed to be at -62 mV/decade. This value is then used to generate $V_{ref}(t)$.

3.4.3 Body effect

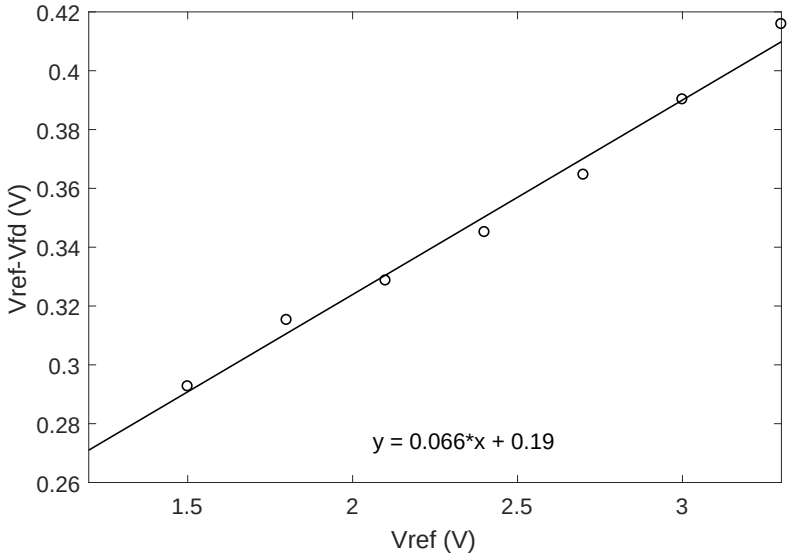


Figure 3.7: Measured body effect of transistor M1 from the pixel.

Another important parameter that needs to be measured is the body effect of the transistor $M1$. To measure the body effect of the pixel, the gate of $M1$ was sourced with DC voltages from 1.5 V to 3.3 V with 200 mV increment. During the measurement, the light intensity was set at 100 lux. Then, at each voltage level, the output of the pixel was measured after 20 ms. The measured values were affected by the source follower slope and offset. Therefore, the source follower parameters expressed in Equation 3.1 were factored in to determine the voltage values at FD node, V_{FD}. The voltage difference between the gate and the source of $M1$ (V_{ref}-V_{fd}) with respect to the input (V_{ref}) is shown in Figure 3.7 to determine the impact of

body effect towards the pixel operation. As expected, the threshold voltage of $M1$ varies with the input voltage. From the figure, the relationship between V_{ref} and the threshold voltage of $M1$ can be fitted linearly and can be expressed as:

$$V_{th,M1} = 0.066 \times V_{ref} + 0.19 \tag{3.2}$$

3.5 Pixel response

Extracted Pixel Parameter	Function	Value
Vsubth_drop	Slope of voltage drop at Reset level	62 mV/dec
SFgain	Source follower gain	0.82 V/V
α	Slope of threshold voltage variation of M1 with Vref(t)	0.066 V/V
β	Threshold voltage of M1 for reference voltage at Vref(t)=0	0.19 V
V_{max}	Reset level	3 V
Slope	Slope of photoresponse	-600 mV/decade
T_{int}	Integration time	20 ms

Table 3.2: Pixel parameters used for $V_{ref}(t)$ generation.

Extracted parameters and values shown in Table 3.2 are used to generate $V_{ref}(t)$ using an arbitrary wave generator. A slope of -600 mV/decade is selected based on an estimation of the pixel output range and the illumination range available. The main consideration when selecting the slope value is to maximise the output swing within the range of the available illumination. From the initial experiment setup, the maximum illumination of the light source is 10 klux.

The generated $V_{ref}(t)$ is shown in Figure 3.8. In addition, transient responses of the pixel for light levels at 100 lux, 1 klux and 10 klux are also demonstrated. During the reset period, the difference between $V_{ref}(t)$ and the pixel output is mainly due to the threshold voltage drop of $M1$ and $M4$. In addition, in the case of a high light

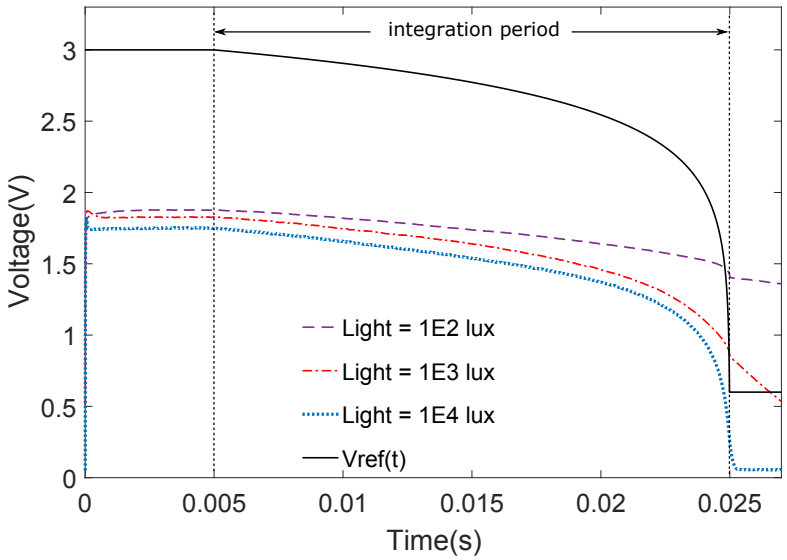


Figure 3.8: Generated $V_{ref}(t)$ and measured transient response of the test pixel at three different light levels for one cycle.

level for example at 10 klux, the reset voltage level is slightly lower than that of 100 lux. The reset voltage level is determined by the amount of photocurrent as defined in Equation 2.9 previously.

During the integration period, the pixel discharges logarithmically attempting to track the rate of change of $V_{ref}(t)$. For a light level at 100 lux, a relatively low photocurrent generated tracks $V_{ref}(t)$ rate of change until at a time t. At this time, the pixel has reached its maximum discharge rate set by the photocurrent. When this happens, the pixel is linearly discharged until the end of the integration period. However, for a light level at 10 klux, a relatively high photocurrent generated means, a higher rate of change can be afforded by the pixel. As a result, the time t when the light level is at 10 klux, is much later than that of 100 lux. The pixel is, therefore, able to track $V_{ref}(t)$ at a higher rate of change.

The output of the pixel was measured at multiple light levels from 1 lux to 10 klux. At each light level, pixel response for 20 cycles was recorded. Then, the values at the end of the integration time of each cycle were averaged in order to reduce

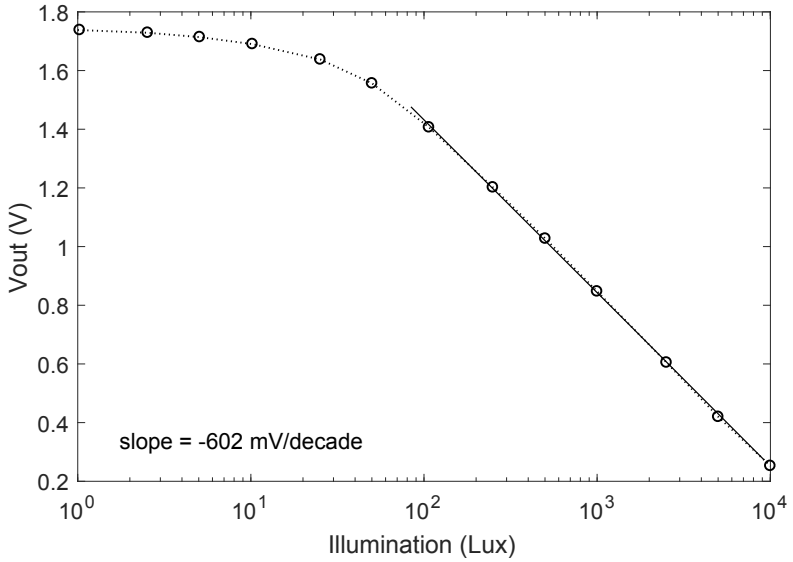


Figure 3.9: Measured photoresponse for $V_{ref}(t)$ with slope of -600 mV/decade covering four decades of dynamic range.

the impact of temporal noise. The measured values are shown in Figure 3.9. The result confirms the logarithmic response as expected. Furthermore, a dynamic range of 80 dB (10^4) has been achieved from the pixel response. From the total dynamic range, the logarithmic region is slightly more than 40 dB. In addition, the slope of the photoresponse was estimated to be -602 mV/decade which is less than 0.35% error from the targeted slope of 600 mv/decade. Although the error is slightly higher than the recorded error from the simulation at 0.17%, (Table 2.5), it is not very significant. More importantly, the measured result shows that the $V_{ref}(t)$ model is able to achieve a well-controlled photoresponse. In particular, in a case where the pixel output range or illumination range is different, the target slope of $V_{ref}(t)$ can be adjusted accordingly with very small error.

3.6 Fixed pattern noise correction

Unlike temporal noise, FPN is time independent and constitutes a more dominant source of noise in an image sensor. The sources of FPN can be classified into offset

(additive) FPN and gain (multiplicative) FPN. In particular, the difference between these two types of FPN is owed to its dependence on light intensity. For example, offset FPN is relatively constant throughout a range of light intensities in contrast to gain FPN.

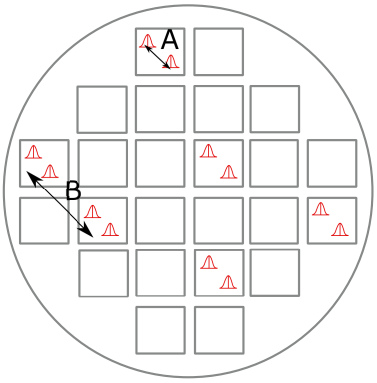


Figure 3.10: Drawn image depicting a wafer with intra-chip (within chip) and inter-chip (chip to chip) variations.

Previous studies have focused on FPN correction of intra-chip variations [67, 59]. In this study, the difference of photoresponses obtained from different chips (inter-chip variations) of a same wafer are studied and correction methods are then proposed. Figure 3.10 illustrates an image of a wafer showing the difference of intra-chip and inter-chip variations. The photoresponses across chips are expected to demonstrate FPN due to variations originated during the manufacturing process such as lithographic variations, random dopant fluctuation, oxide thickness non-uniformity and many others [68, 69]. These variations are beyond the control of circuit designers and the FPN resulted from the variations needs to be corrected.

To study the effect of FPN on photoresponses from different chips, four chips containing a test pixel were chosen randomly out of eight chips available. A $V_{ref}(t)$ generated from extracted parameter values of Chip 1 was used for all other chips. Then photoresponse of each chip was characterised individually. When measuring pixel response at each light level, 20 output readings were averaged out to minimise

variations due to temporal noise.

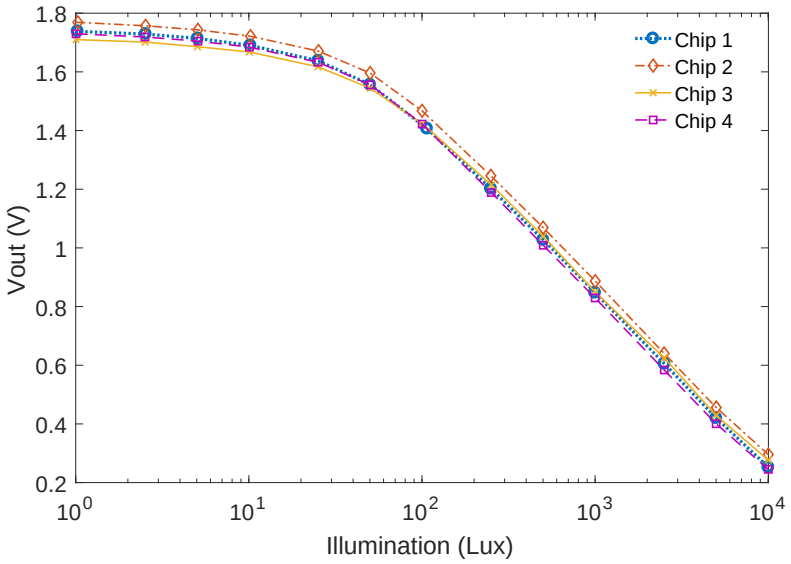


Figure 3.11: Photoresponses of test pixels from four different chips showing FPN with gain and offset components.

Figure 3.11 shows photoresponses of four different pixels demonstrating the effect of the inter-chip variations. A closer observation confirms the presence of the two sources of FPN as expected. At low light levels from 1 lux to 25 lux, each photoresponse tracks each other by relatively constant offsets. The voltage variations between the four chips at 1 lux and 25 lux are 59 mV and 55 mV respectively. However, at higher light levels from 100 lux to 10 klux, each pixel output decreases at a different slope as light level increases. In particular, it is visible that photoresponse of Chip 3 has a lower slope than that of Chip 4 with slopes of 602 mV/decade and 607 mv/decade respectively. The slopes and the start values of all the photoresponses are recorded in Table 3.3. From these observations, it can be concluded that offset FPN dominates at a low light region while gain FPN dominates at a high light region.

The variations in the photoresponses are expected when the $V_{ref}(t)$ extracted from Chip 1 was applied to other chips. The significance of the variations is demonstrated when the photoresponses parameters are compared in Table 3.3. When comparing

Chip	Start value (V)	Slope (mV/dec)
Chip 1	1.738	602
Chip 2	1.769	608
Chip 3	1.71	602
Chip 4	1.73	607

Table 3.3: Measured parameters of photoresponses from 4 different chips showing voltage at 1 lux and slope of the logarithmic region.

peak to peak value of two different pixel responses, the variations will degrade the quality of an image produced up to 10% if not corrected. Therefore, a corrective measure to reduce the FPN is necessary.

3.6.1 Offset FPN correction

The presence of two uncorrelated FPN components which are the offset and the gain FPN suggests that it is possible to remove each component individually [33]. A simple yet effective way to remove offset FPN is by using a correlated double sampling (CDS) method. When using CDS, the pixel is sampled during reset and after the integration time. The difference between these two samples has been demonstrated previously [70, 50, 71] to remove the threshold voltages of $M1$ and $M4$ which are the main contribution of the offset FPN. Ignoring temporal noise contribution, a CDS operation can be described as the difference of $V_{1,reset}$ and $V_{2,read}$ such that:

$$V_{1,reset} = (V_{reset} - V_{th,M1}) \times SFgain - V_{th,M4} \tag{3.3}$$

$$V_{2,read} = (V_{reset} - V_{th,M1} - i_{ph} \times t_{int}/C_{fd}) \times SFGain - V_{th,M4} \tag{3.4}$$

where $V_{1,reset}$ is the pixel output during reset operation, $V_{2,read}$ is the pixel output at the end of integration time and SFgain is the source follower gain and the difference of the two signals eliminates the offset FPN component is equal to:

$$V_{CDS} = V_{1,reset} - V_{2,read} = (i_{ph} \times t_{int}/C_{fd}) \times SFGain \tag{3.5}$$

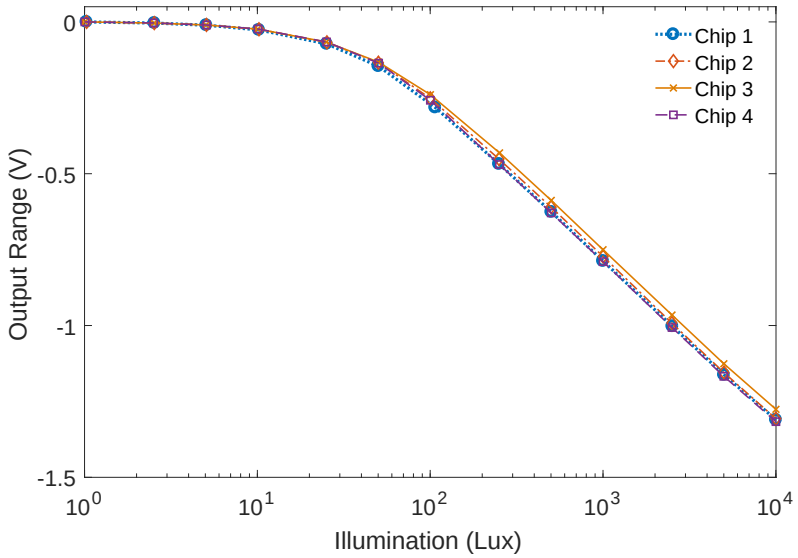


Figure 3.12: Double sampled photoresponses of test pixels from four different chips showing the offset FPN is significantly reduced.

The result of the double sampled photoresponses in Figure 3.12 shows that at a low light region from 1 lux to 20 lux, the pixel responses appear to be identical for all chips demonstrating that the offset FPN has been significantly removed as expected. However, at high light levels, the double sampling technique does not cause any significant change to the pixel response variability. The remaining FPN means an additional step needs to be taken in order to produce a high-quality image output. Furthermore, the significance of this variation to the quality of an image needs to be measured.

3.6.2 Gain FPN correction using single response model

An ideal case to correct the gain FPN is by having a single response curve whose parameters can be used to estimate all the light levels for every pixel within an acceptable margin of error. In particular, for a high-quality image, these estimated

light levels should fall within 2% from the corresponding light responses of every pixel [21, 72]. A simple approach to produce a single response curve is to fit an individual model to all the pixel responses in Figure 3.12. Then, parameters of all the models that characterise the responses can be extracted and the mean values for each parameter can be obtained. Finally, to produce the single response curve, the mean value of the parameters can be used to estimate the light levels.

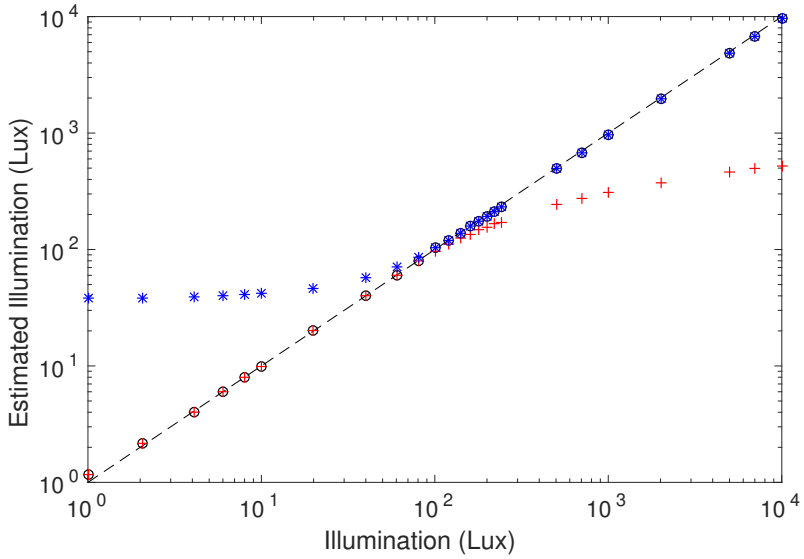


Figure 3.13: Modelled linear and log regions from extracted parameters of Chip 1. '+' is the estimated low light linear model fit for measured light responses at low light region. '*' is the estimated high light log model fit for measured light responses at high light region. 'o' is the estimates of the light responses by selecting either linear or log regions with transition at 100 lux.

Using a similar method proposed by Das and co-worker [59], the responses of one of the pixels has been estimated with a combination of linear and logarithmic fit. In particular, from the results obtained in Figure 3.12, a linear response has been estimated using the third and the sixth data points and a logarithmic response has been estimated using the eight and the thirteenth data points. The selection of these points was made using visual inspection based on the maximum likelihood for the data points to fall either into linear or logarithmic region. Figure 3.13 shows a comparison between known illuminations from the measurements and the estimated

illuminations of pixel response of Chip 1 using a combination of estimates from linear and logarithmic responses. The linear response is shown to fit the pixel response at low light levels before the response diverges and saturates at the maximum of the integration period. In contrast, the logarithmic response fits the pixel response at high light levels from 100 lux. Final estimated illuminations (marked in 'o') therefore are chosen using a combination of these two responses in order to estimate the pixel response. The same method was applied to the response of pixels from other chips. The pixel parameters extracted to estimate the photoresponse for all the four chips are recorded in Table 3.4. Then the mean value of each parameter (Table 3.5) is used to generate a single reference curve.

Chip	Linear Slope (mV/lux)	Linear Constant (mV)	Log Slope (mV/decade)	Log Constant (mV)
Chip 1	-2.7	-7	-527	-352
Chip 2	-2.8	-7.1	-532	-363
Chip 3	-2.7	-7.9	-528	-339
Chip 4	-2.7	-6.7	-531	-377

Table 3.4: Extracted parameters from pixel responses of all four chips to generate estimated response for FPN correction.

	Linear Slope (mV/lux)	Linear Constant (mV)	Log Slope (mV/decade)	Log Constant (mV)
Mean value	-2.73	-7.18	-529.5	-357.8

Table 3.5: Mean value of extracted parameters from pixel responses of all four chips to generate the single response curve.

The accuracy of the estimates produced using parameters extracted from the single curve response needs to be verified against the response of pixels from different chips. The aim is to study if a single curve response is a sufficient representation of all pixel

responses. In addition, the FPN residue of the pixel response variation from the estimated illumination is expected to be low enough imperceptible to human vision. The percentage illumination error of each pixel with respect to the single response curve can be defined as:

$$\%I_{error} = \frac{|\ \overline{I_{est}} - I_i\ |}{I_i} \times 100 \tag{3.6}$$

where I_{est} is a vector of estimated illuminations from the single curve and I_i is a vector of the measured illuminations of chip i.

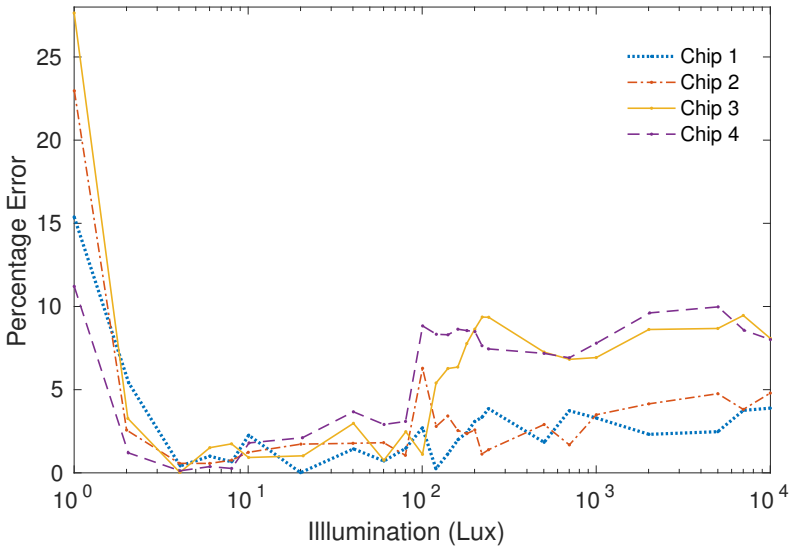


Figure 3.14: Percentage light error of four test pixels from the mean output response as a universal linear log fitted model.

Figure 3.14 shows the percentage illumination error of each pixel response from the estimated illuminations of a single curve response. It is apparent that two different regions exist demonstrating linear logarithmic curve fit performed previously. At the very low light region, the errors for all chips are higher than 10% from the estimated illumination. These errors are due to the unavoidable quantisation noise introduced by the ADC which has a significant effect on the very low light conditions. Illumination error as high as 10% due to quantisation noise at the low light levels has been recorded

previously [59]. With the exception of the quantisation noise present at the very low light levels, the percentage error obtained at low light region is less than 4%. The result highlights that although the previous CDS method removed the offset FPN significantly, it is not sufficient to reduce the error to less than 2%. Furthermore, the percentage error at the high light region demonstrates that the estimates from a single curve response are insufficient to estimate the illuminations from each pixel response to the acceptable range.

3.6.3 Gain FPN correction using multiple response models

The previous study showed that the estimated illuminations from a single curve response are unable to approximate the illuminations of each pixel response to 2% or less, in particular at the high light region. This result suggests that a better alternative to a single curve response which was obtained from the mean of pixel response of different chips is to use individual curve response extracted from each chip. To have an individual curve response means that each chip will need to be characterised individually in order to have estimates of its response for FPN correction.

Parameters extracted from each chip in Table 3.4 are used to estimate illuminations of pixel response. Then the accuracy of the estimates is assessed as shown in Figure 3.15. The figure shows that the percentage error from 5 lux up to the maximum illumination measured is below 2% except in the middle of the illumination range which corresponds to the transition between linear-logarithmic region estimate. The result suggests that the response of each pixel needs to be modelled individually to obtain lower percentage error. However, the arbitrary choice when determining the transition between the two estimates of linear logarithmic region leads to high percentage error in the middle of the illumination spectrum. One way for a user to avoid having to choose between the two estimates at the transition point is by averaging near the transition region where the illumination in the middle region

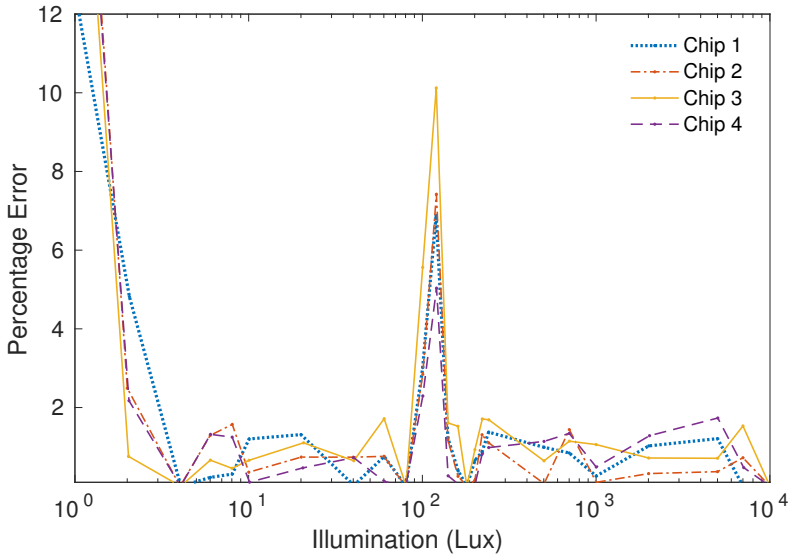


Figure 3.15: Percentage light error of four test pixels from each output response as linear log fitted model with a high error at transition region.

can be estimated such that [59]:

$$I_{est} = ((1 - w) \times I_{lin,est}) + (w \times I_{log,est}) \tag{3.7}$$

where $I_{lin,est}$ is the linear estimate of the illumination while $I_{log,est}$ is the logarithmic estimate of the illumination. w is a weight variable when averaging as the pixel response is shifting from a linear to logarithmic response. The averaging region near the transition point where the weight needs to be applied is found to be between 90 lux and 120 lux. The weight, therefore, can be defined as:

$$w = \frac{\log(I_{avg}) - \log(90)}{\log(120) - \log(90)} \tag{3.8}$$

By using the averaging method between the two estimates, the estimated illumination is expected to have a better approximation to the pixel response. The result of this method is demonstrated in Figure 3.16 which shows that the spiked error has been reduced significantly. The advantage comes at the cost of a more sophisticated approach than requiring only pixel parameters to estimate the pixel response. This

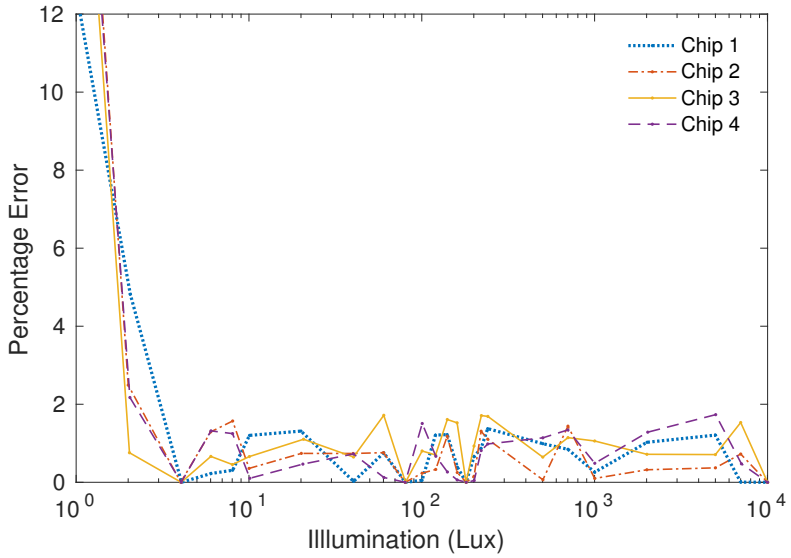


Figure 3.16: Percentage light error of four test pixels from each output response as linear log fitted model with an averaged transition regions.

means that the estimated values from the averaging method need to be included in the two estimates. A simple solution to perform the proposed FPN correction is by using a look-up table (LUT) which can be implemented on an FPGA. Therefore a direct conversion is possible from a list of illuminations represented by voltages as the inputs to the estimated illuminations as the corrected FPN outputs. In particular, in a case of a 10 bit image sensor, the illumination range from 1 lux to 10 klux is divided equally between 1 and 1024 as input values whose outputs are the estimated illuminations that have already been FPN corrected.

3.7 Summary

5T test pixels have been laid out and fabricated acquiring an area of 5 μm per pitch. The fill factor obtained is 34% per pixel. Details of the experimental setup that was used to characterise and measure the pixels have been presented. Then, parameter values extracted from pixel characterisation were included in a $V_{ref}(t)$ model which was generated by an arbitrary wave generator. Pixel response of up to 80 dB has been

achieved. In addition, the slope of the response obtained is -602 mV/decade which is less than 1% from the targeted slope. This result demonstrates a well-controlled photoresponse from the $V_{ref}(t)$ model. Furthermore, additional pixel responses from three different chips have been measured to study the impact of inter-chip FPN. To reduce FPN, two-step correction procedures have been performed. In particular, first, CDS method was used to reduce the offset FPN. Then, the remaining FPN which is the gain component has been reduced using linear and logarithmic fits. When fitting the pixel responses, a universal fitting model has failed to reduce illumination error to less than 2%. Therefore, each pixel response has been fitted individually. In addition, the transition point between the linear and log fit that demonstrates a high error has been corrected using a weighted average method. As a result, the FPN has been reduced to less than 2%.

Chapter 4

A comparison of modes of operation

4.1 Introduction

Previously in Chapter 3, it was demonstrated that the 5T pixel can achieve dynamic range extension by using an integrating logarithmic mode. This method is performed by controlling the pixel's discharge rate through an external signal referred to $V_{ref}(t)$. The ability to control the pixel response through $V_{ref}(t)$ means that other types of dynamic range extension mode can also be performed on the pixel. This offers an opportunity to conduct a comparative study of different modes. Previous comparative studies have only reviewed different modes using quantitative models and simulations [73, 74, 56]. In these studies, different pixel configurations were adopted in order to perform each extension mode. When using different configurations, each pixel will have different parameter values, for example, its well capacity, noise levels such as offset FPN, output range and other parameters. Therefore, in the study presented in this chapter, the same pixel is used exclusively and the performance of each mode is assessed experimentally. Different modes of operation are achieved by controlling

$V_{ref}(t)$.

In this chapter, a study of different modes of dynamic range extension is presented. The performance of each mode is assessed using performance metrics such as dynamic range, sensitivity and percentage error in the estimated illumination. When defining each metric, the standard linear mode is used as a benchmark. Therefore, the performance of the linear mode is first reviewed. Then dynamic range extension modes such as logarithmic, linear-logarithmic and multiple stepped reset modes are investigated subsequently. Finally, the results of integrating logarithmic mode demonstrated in the previous chapter are brought together in a discussion of mode comparisons. All the results presented in this chapter were measured on the same pixel with an integration time of 20 ms except for the logarithmic mode that operates in continuous mode. The experimental setup and conditions used, were described in the previous chapter.

4.2 Linear mode

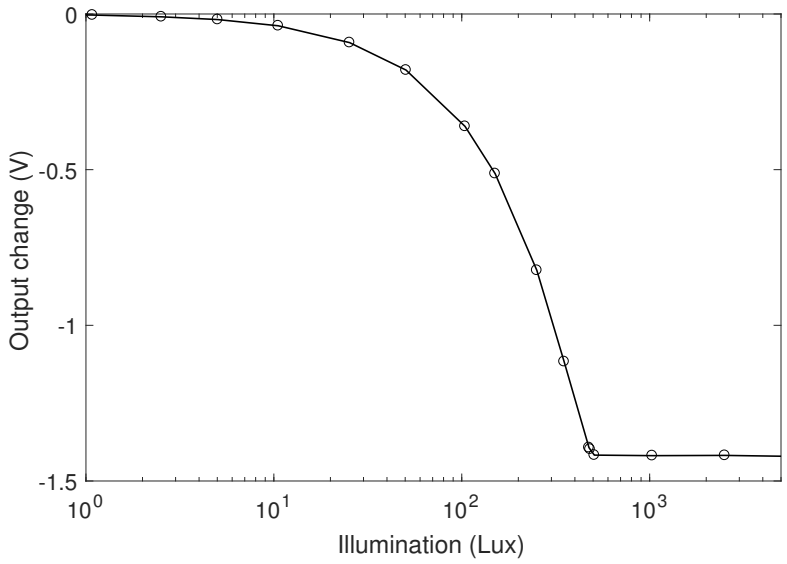


Figure 4.1: Linear mode pixel response on the 5T pixel.

The linear mode was performed on the 5T pixel and its response was measured at illumination from 1 to 10000 lux. The pixel response in Figure 4.1 shows that the dynamic range of this mode is approximately 54 dB with an output range of 1.4 V. To confirm the response of the pixel and further study its performance, the pixel response is fitted with linear models as shown in Figure 4.2. The figure shows that the pixel response can be divided into two linear regions. The second region is not of interest because it is in saturation. The linear fit to the region of interest (Region 1 in Figure 4.2) is observed to overlap the measured data as expected. However, a closer inspection shows that the response slightly departs from the expected linear fit at 475 lux. The reason for this is due to the smaller bias current as the pixel output approaches the maximum output range. When this happens, the drain voltage of the current source transistor is decreased and the transistor is out of saturation.

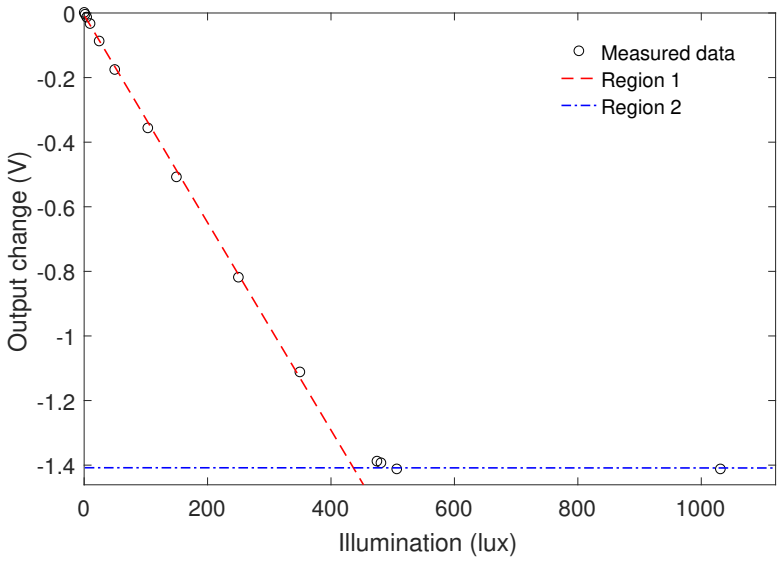


Figure 4.2: Linear mode response with linear x-axis showing that it can be fitted to two linear regions with the second being at saturation.

The sensitivity of a linear response across the illumination spectrum can be determined by [56]:

$$Sensitivity = \frac{\mathrm{d}V_{pix}}{\mathrm{d}I_{ph}} = \frac{\mathrm{d}}{\mathrm{d}I_{ph}}\left(\frac{I_{ph}t_{int}}{C_{fd}}\right) = \frac{t_{int}}{C_{fd}} \tag{4.1}$$

Parameters from the modelled linear response can be used to study the pixel sensitivity. Figure 4.3 shows the pixel sensitivity is constant at about 3.2 mV/lux. This value corresponds to the slope of the linear model fitted onto the response previously.

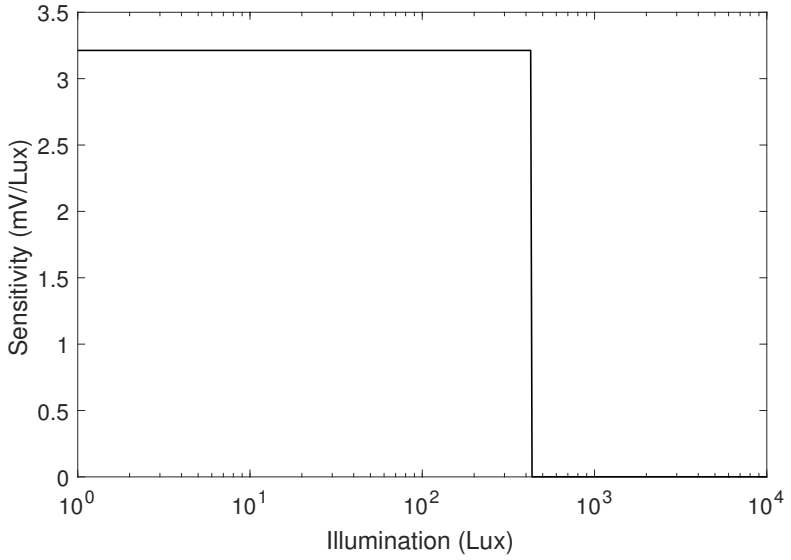


Figure 4.3: Linear response sensitivity showing drops to zero indicates pixel saturation and limited dynamic range.

Percentage illumination error (as described in Chapter 1) is an important metric and conveys a more meaningful measurement than the usual SNR metric because the metric captures the experience of an end user. The real illumination fitted from the measured illumination can be defined as:

$$I_{real} = \frac{LSB}{Sensitivity} \tag{4.2}$$

where LSB is the smallest detectable voltage. For example, a pixel with an output range of 1.4 V with a 10-bit ADC has an LSB of 1.4 mV. Then the real illumination is measured against the estimated illumination falling onto the pixel to get the

percentage illumination error such that:

$$\%I_{error} = \frac{I_{real} \times 100}{I_{est}} \tag{4.3}$$

Figure 4.4 shows the percentage illumination error for the linear mode response. The horizontal line denotes the 2% threshold line. This figure shows that the error varies from 20 % down to less than 0.1 %. The high error in the low illumination region shows that it is highly susceptible to temporal noise. In addition, the illumination error is observed to decrease and cross the threshold line at 11 lux. The decreasing error is the most obvious feature of the figure. In particular, the error is large at low light levels, but decreases as the light level increases until it becomes less than 2% when the illumination is at 11 lux.

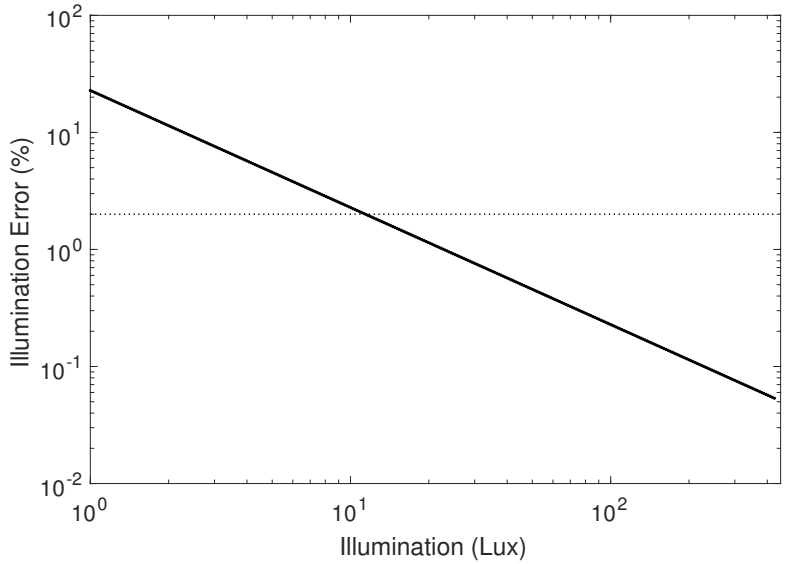


Figure 4.4: Percentage illumination error of the linear response.

4.3 Logarithmic mode

The linear mode suffers from pixel saturation at high illuminations. Furthermore, having a linear relationship between illumination and pixel output means that a

large volume of data needs to be captured when extending the dynamic range. For example, an imager with six decades of dynamic range requires an ADC with at least 20-bit precision to produce high-quality images. A logarithmic imager overcomes this challenge by compressing the data during image capture. This, in turn, relaxes the demanding requirement for subsequent data processing.

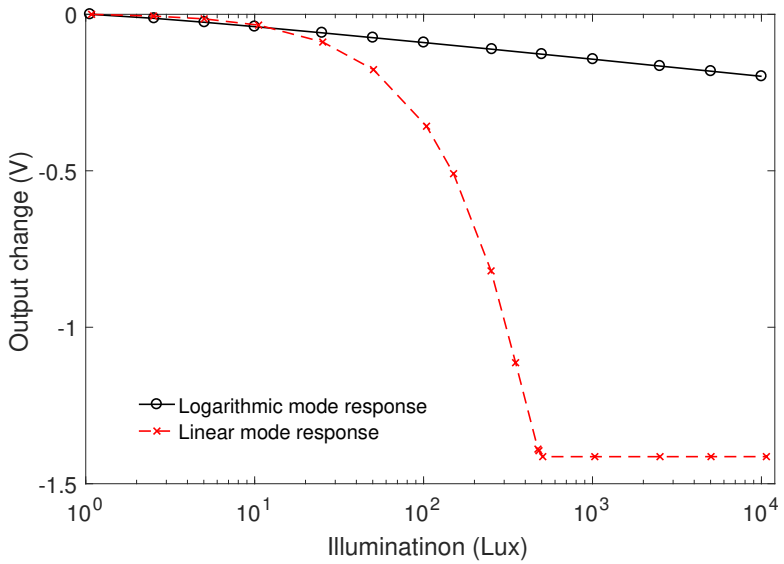


Figure 4.5: Subthreshold logarithmic response showing wide dynamic range is achieved in comparison to linear response.

The logarithmic mode operation can be obtained when both the gate and the drain of the reset transistor remain high. The available illumination from the natural scene falling onto an imager typically generates photocurrent less than 1 nA. This means that the photocurrent flowing through the reset transistor maintains the operation in a subthreshold mode. When this happens, the source of the reset transistor has a logarithmic relationship with respect to the photocurrent which can be approximated as [6]:

$$V_{pix} = V_{S,M1} = V_{G,M1} - V_{th,M1} - nV_t \ln\left(\frac{I_{ph} + I_d}{I_{O,M1}}\right) \tag{4.4}$$

where $V_{S,M1}$, $V_{G,M1}$ and $V_{th,M1}$ are the source, gate and threshold voltage of $M1$ in

Figure 2.1, I_{ph} is the photocurrent and I_d is the pixel dark current, parameters I_O and n are process dependent with I_O is dependent on the transistor dimension, V_t is the thermal voltage kT/q.

The logarithmic mode operation was performed on the 5T pixel by connecting both the gate and the drain of $M1$ to V_{dd}. The output of the pixel was measured across the available illumination range. The measured pixel response of the logarithmic mode is shown in Figure 4.5 with a linear response is also depicted as a reference. The logarithmic response covers four decades of dynamic range in a range of approximately 200 mV. The remaining output range available means that the logarithmic photoresponse is able to cover an additional dynamic range.

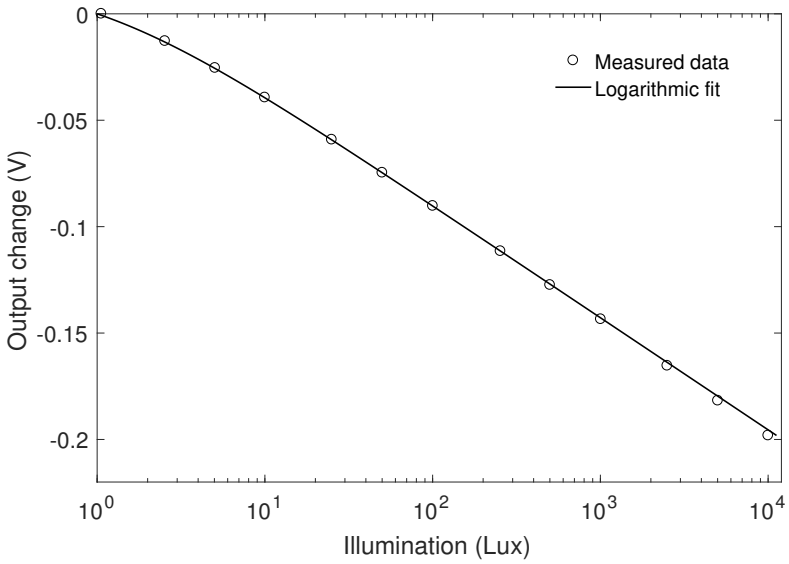


Figure 4.6: Modelled logarithmic photoresponse showing a slight deviation from a logarithmic response at low light levels due to dark current domination.

The sensitivity and the illumination error of the pixel response can be studied by first modelling the response. The presence of the dark current and its effect on the response that is modelled based on Equation 4.4 is shown in Figure 4.6. The impact of the dark current can be seen from the fitted model which has a slight bent curve at very low illumination region. This confirms that the response is dominated

by the presence of dark current at the very low illumination region [75]. When the illumination is increased, I_{ph} gets higher than I_d and the pixel will respond to the increasing illumination with a slope determined by nV_t. The slope of the logarithmic response is measured at 53 mV/decade.

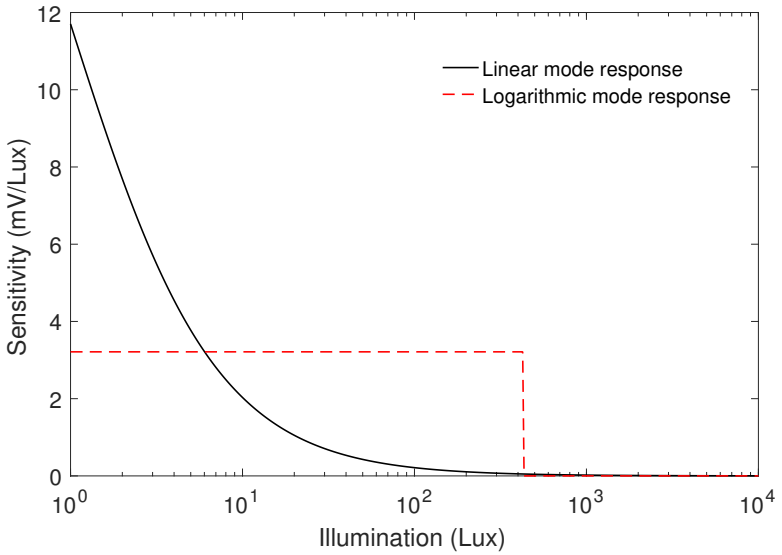


Figure 4.7: Sensitivity of the logarithmic response showing a rapid decrease as illumination increases.

The sensitivity of an ideal case of a logarithmic response can be estimated such that:

$$Sensitivity = \frac{\mathrm{d}V_{pix}}{\mathrm{d}I_{ds}} = \frac{\mathrm{d}}{\mathrm{d}I_{ds}} \frac{nkT}{q} \ln\left(\frac{I_{ds}}{I_{O,M1}}\right) = \frac{nkT}{qI_{ds}} \tag{4.5}$$

where $I_{ds} = I_{ph} + I_d$. I_{ph} and I_d are photocurrent and dark current respectively. The equation shows that the sensitivity decreases as the illumination increases. Furthermore, the sensitivity is fixed by the transistor's parameter nkT. Figure 4.7 shows the sensitivity of the logarithmic response plotted against the linear response as a reference. The sensitivity of the logarithmic response is higher than the linear mode due to the logarithmic relationship between photocurrent and the pixel output as expected. This can be clearly observed in Figure 4.8. The highest sensitivity reaches

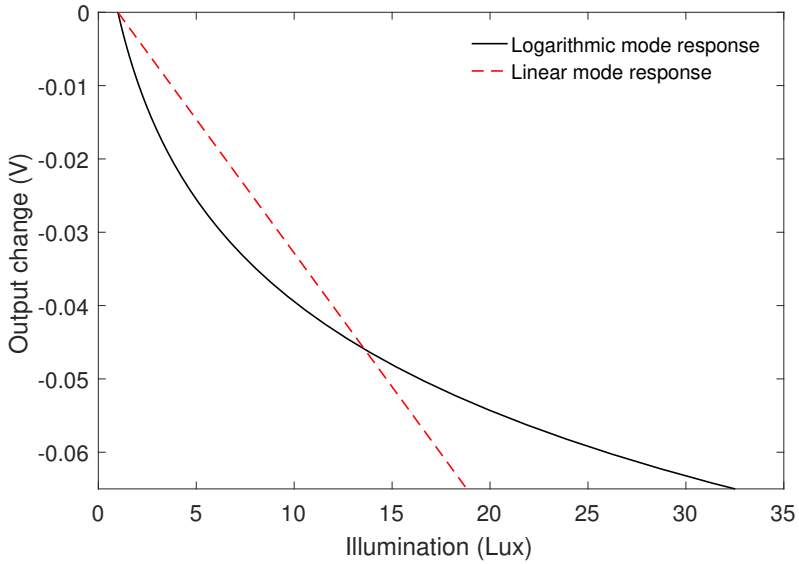


Figure 4.8: Modelled logarithic response at dark response showing a higher sensitivity compared to linear response at very low illumination.

11 mV/lux. Although the sensitivity is higher, the logarithmic mode suffers from slow transient response at low illuminations due to the small photocurrent [29, 76]. As the illumination increases, the sensitivity drops rapidly below the sensitivity of the linear response at 6.5 lux. This makes the logarithmic mode highly susceptible to temporal noise.

The impact of the sensitivity to the image quality can be studied from the percentage illumination error shown in Figure 4.9. The figure shows that for the logarithmic response, the percentage light error is higher than 2% throughout the illumination spectrum. This demonstrates that the dynamic range extension gained comes at the cost of reduced image quality. One way to reduce the error is by employing a higher precision ADC. However, this approach results to an increased volume of data which counters the aim of compressing the captured data.

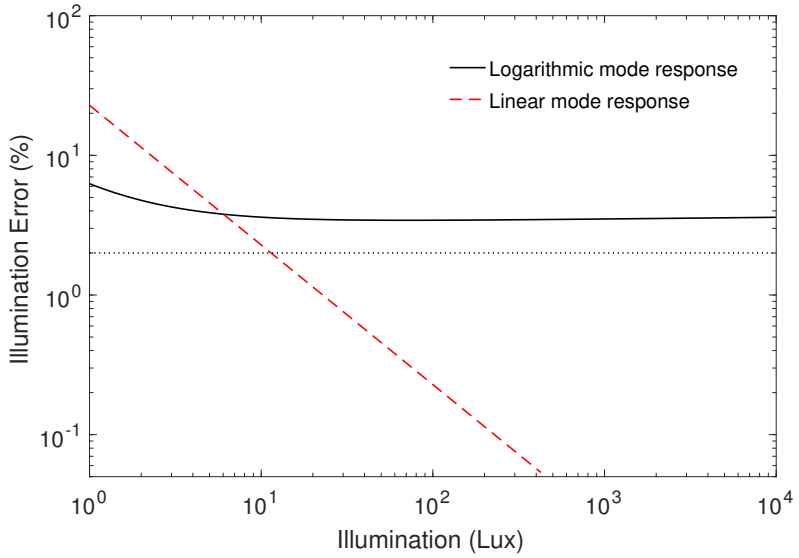


Figure 4.9: Logarithmic response showing it has a wide dynamic range covering four decades at a cost of percentange light error higher than 2% threshold level.

4.4 Linear-logarithmic mode

It was demonstrated earlier that the linear response covers up to 54 dB of dynamic range. In contrast, the logarithmic mode demonstrated a dynamic range of up to 80 dB at the expense of reduced image quality. The linear-logarithmic mode aims to offer the advantages of both approaches by preserving the linear response at low to mid region and logarithmic response at high region across the illumination spectrum.

To generate a linear-logarithmic mode with the 5T pixel, a reference voltage, V_{ref} similar to the reset signal of a linear mode is sourced to the gate of the reset transistor M1. The only difference is the voltage is held at an intermediary voltage V_{log} after reset instead of dropped to ground [52]. The response of the pixel will depend on V_{log} which can be defined as [53]:

$$V_{pix} = \begin{cases} V_{dd} - \frac{t_{int} I_{ph}}{C_{pix}} & V_{pix} > V_{log} \\ V_{log} - V_{th} - nV_T \ln(\frac{I_{ds}}{Io}) & V_{pix} \leq V_{log} \end{cases} \tag{4.6}$$

where the V_{log} is a user-defined voltage whose value needs to be higher than the

threshold voltages of M_1 and M_4, $Vth_{M1} + Vth_{M4}$ (Figure 2.1).

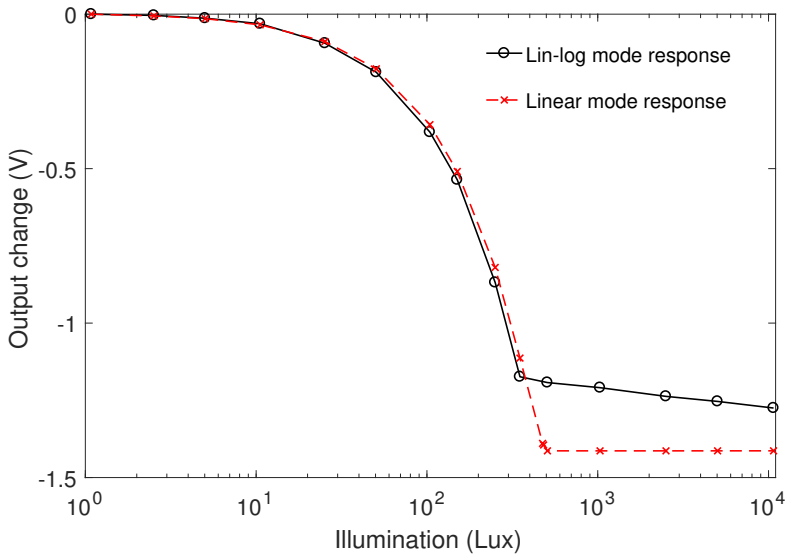


Figure 4.10: Linear-logarithmic mode pixel response showing saturation is avoided at high illuminations.

The pixel response can be understood when analysed at low and high illuminations. At low illuminations, the generated photocurrent will discharge the pixel capacitance until the end of the integration time similar to the linear mode response. However, at high illuminations the generated photocurrent will discharge the pixel capacitance at a higher rate. When the voltage of the pixel capacitance V_{pix} equals to V_{log}, the load transistor M_1 starts to supply current that balances the photocurrent until the end of the integration time. The pixel response, therefore, can be related to the logarithm of the photocurrent as referred in Equation 4.6.

The pixel response of the linear-logarithmic mode when V_{log}=1.2 V and t_{int}=20 ms is shown in Figure 4.10. The linear response is also shown for a reference. The pixel response of the linear-logarithmic mode shows that the linear mode for about 51 dB. The slight difference between the two responses at low illuminations is contributed by the effect of the parasitic capacitance of $M1$ during reset. This happens when the reset signal is raised from V_{log} to V_{reset} for the linear-logarithmic mode as opposed to

gnd to V_{reset} for the linear mode at the start of each frame. When the pixel response is observed at high illuminations, a logarithmic response is demonstrated as expected. A dynamic range extension of 29 dB is demonstrated by the results in Figure 4.10.

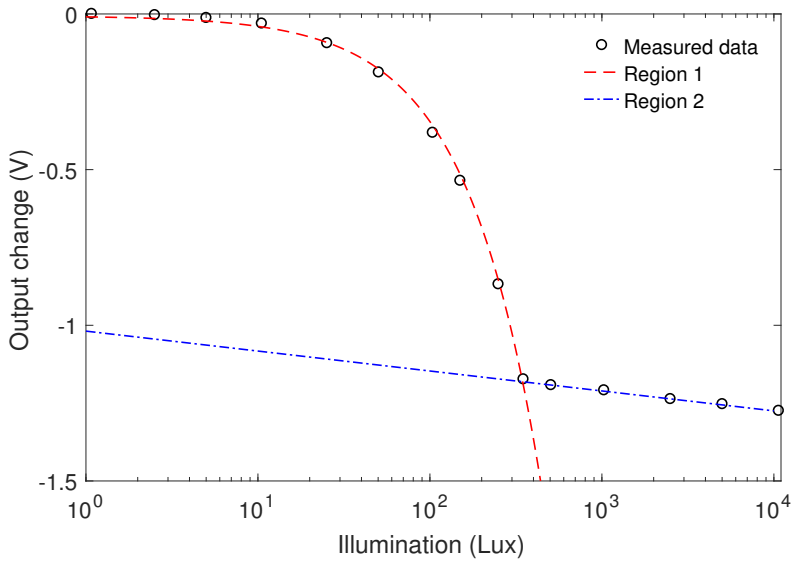


Figure 4.11: Modelled linear-log photoresponse using linear and log fits in Region 1 and Region 2 respectively.

Slope (mV/lux)	Linear Constant (mV)	Log Slope (mV/decade)	Log Constant (V)
-3.3	-5.9	-64	-1.27

Table 4.1: Extracted parameters from the modelled linear-logarithmic response.

The pixel response is then modelled using linear and logarithmic fits at the corresponding regions as depicted in Figure 4.11. The parameters used for modelling the linear and logarithmic regions are recorded in Table 4.1. The sensitivity of the pixel response can be divided into linear and logarithmic operations. From Equation 4.6 the sensitivity is equal to:

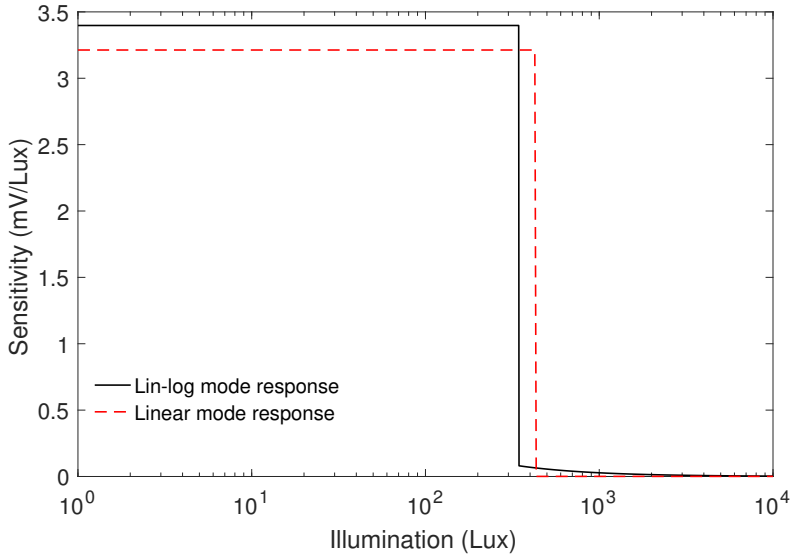


Figure 4.12: Sensitivity of linear-logarithmic response in comparison to linear response.

$$Sensitivity = \frac{\mathrm{d}V_{pix}}{\mathrm{d}I_{ds}} = \begin{cases} \frac{t_{int}}{C_{pix}} & V_{pix} > V_{log} \\ \frac{nkT}{qI_{ds}} & V_{pix} \leq V_{log} \end{cases} \tag{4.7}$$

The sensitivity of the mode is shown in Figure 4.12. A linear response is also shown as a comparison. The figure shows that the linear-logarithmic response has a sensitivity of 3.4 mV/lux at low illuminations which is slightly higher than that of the linear response. However, the sensitivity difference is very small with less than 0.2 mV/lux. When the operation is switched from linear to logarithmic to avoid saturation at high illumination range, the sensitivity drops by several orders of magnitude to 0.08 mV/lux. By combining the linear and the logarithmic operations, the sensitivity at low illuminations and the dynamic range extension are achieved.

A closer examination of the linear-logarithmic mode performance can be observed from the percentage illumination error. The impact of the dynamic range extension using logarithmic operation can be observed in Figure 4.13. The percentage illumination error during linear operation of the linear-logarithmic mode is similar to the

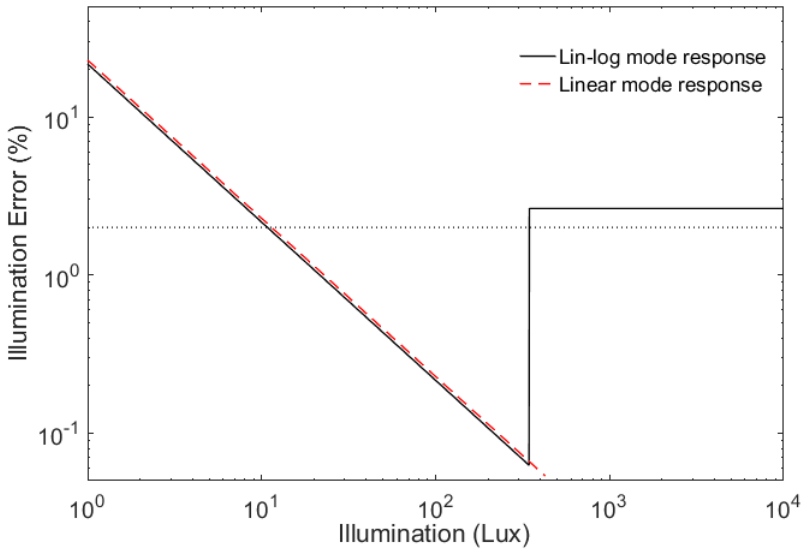


Figure 4.13: Percentage illumination error of linear-logarithmic response.

conventional linear mode. However, when the operation is switched to the logarithmic operation, the percentage light error rises above the threshold level. This means that although the dynamic range is extended, the high illumination region is susceptible to temporal noise.

4.5 Multiple reset mode

The multiple reset mode is a dynamic range extension mode based on the well capacity adjusting scheme. This mode is attractive due to its simplicity and adaptivity. However, a well-known issue of this approach is its SNR dips due to the transitions at the reset signal [73]. The dips cause severe image degradation despite achieving wide dynamic range. If a proper method is used in determining the number of steps, the reset voltage levels and the time interval of the reset level transitions, this effect can be significantly minimised.

A few studies using multiple stepped reset have been published in the past[14, 55, ?]. However, there is no clear method of choosing the stepped reset parameters. The

results are pixel responses that are not well controlled and difficult to model [14, 77]. In addition, parameters such as number of steps, voltage level and transition time have to be carefully determined in order to produce high-quality images. A starting point to choose these parameters is by adopting the $V_{ref}(t)$ model of the integrating logarithmic mode [78]. In particular, the voltage of $V_{ref}(t)$ used in this mode can be divided into equal parts of voltage according to the number of steps required. As a result, voltage levels and transition times can be identified. This can be a simple method to generate a well-controlled pixel response.

In this section, first, a brief explanation of the multiple reset mode operation is presented. Then a method of generating a three stepped reset signal is introduced. Next, the pixel response and its performance is discussed. Finally, dynamic range extension of up to six decades and its performance are presented.

4.5.1 Three stepped reset

The advantage of the multiple stepped reset mode can be understood by considering a gate voltage of the reset transistor which has two intermediate values between the original maximum and minimum $V_{ref}(t)$ values. If the photocurrent is small, then the pixel will discharge slowly and the pixel remains isolated from V_{dd}. However, if the photocurrent is larger, the pixel will discharge at a higher rate to a voltage value lower than the gate voltage of the reset transistor. When the voltage difference is large enough, then the reset transistor will supply the photocurrent and the pixel voltage will remain constant. This condition remains until the gate voltage drops to a lower value. The pixel will discharge again until the end of integration time. The operation, therefore, reduces the effective integration time of the larger photocurrent and saturation can be avoided. The photoresponse will be a piece-wise linear response.

To generate a stepped reset voltage, the $V_{ref}(t)$ model is used. An equal voltage strategy is performed in order to divide the voltage into multiple steps. In particular,

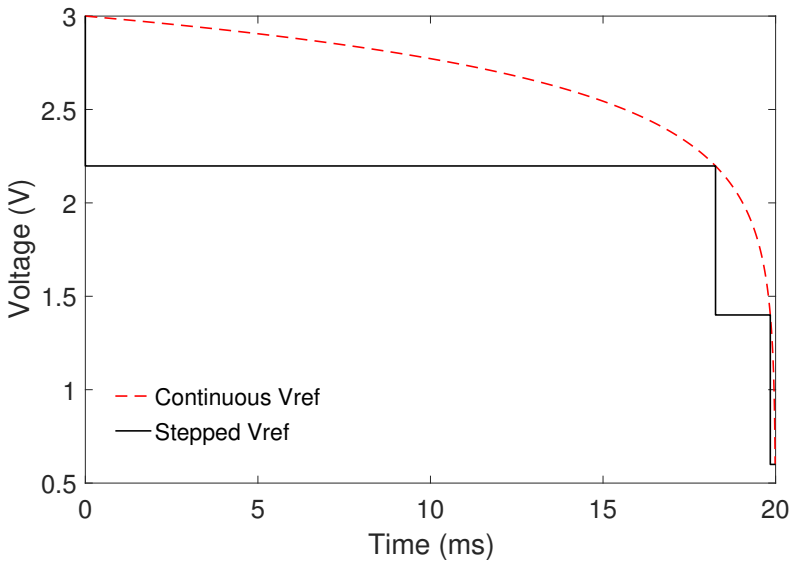


Figure 4.14: Three stepped reset signal generated from the integrating logarithmic $V_{ref}(t)$

the voltage range of $V_{ref}(t)$ is divided into three regions equally corresponding to three steps. As a result of this division, voltage levels and the transition times can be determined. The choice of the number of steps needs to be considered based on the trade off between potential SNR dips and circuit complexity. Higher number of steps can avoid large SNR dips at the expense of more complex circuitry. Figure 4.14 shows a stepped reset voltage generated from the continuous reset voltage (integrating logarithmic $V_{ref}(t)$) calculated using Equation 2.4 and pixel parameter values from Table 3.2 for a case of three stepped voltage. By dividing into multiple regions, the parameter values of the regions for the voltage level and step duration for each region can be obtained and are recorded in Table 4.2. The corresponding time durations for each region identified are 18.26 ms, 1.59 ms and 150 μs for Region 1, 2 and 3 respectively. The relationship between the pixel output and the photocurrent can be approximated as:

$$V_{pix}(I_{ph}) = \begin{cases} V_{reset} - \frac{t_{int} I_{ph}}{C_{pix}} & I_{ph} < I_{1,2} \\ V_1 - \frac{(t_{int} - t_1) I_{ph}}{C_{pix}} & I_{1,2} < I_{ph} < I_{2,3} \\ V_2 - \frac{(t_{int} - t_2) I_{ph}}{C_{pix}} & I_{ph} > I_{2,3} \end{cases} \tag{4.8}$$

where parameters V_1, V_2, t_1, t_2 are voltage levels and time transition for each region. $I_{1,2}$ and $I_{2,3}$ are the photocurrents that fall on the pixel whose pixel responses are at the transition points.

Region	Voltage Level (V)	Time (ms)
Region 1	2.2 (V_1)	18.26 (t_1)
Region 2	1.4 (V_2)	19.85 (t_2)
Region 3	0.6 (V_3)	20 (t_{int})

Table 4.2: Extracted parameters from the modelled logarithmic response.

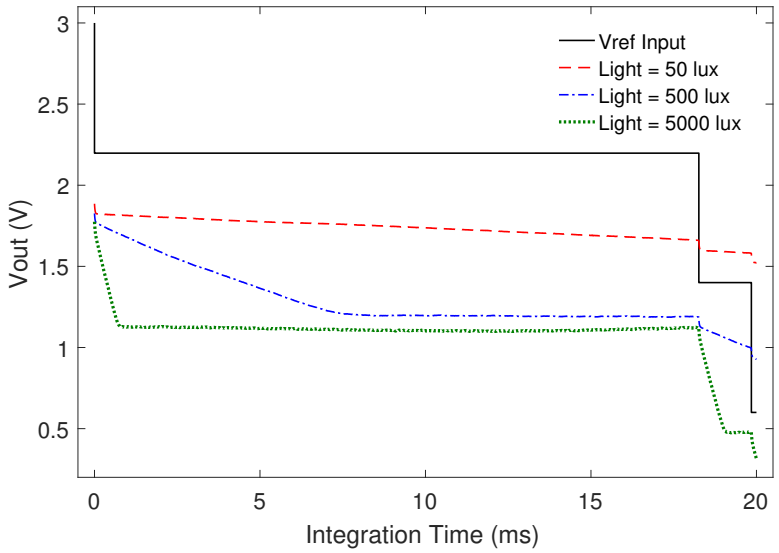


Figure 4.15: Measured transient response of three stepped reset mode at 50 lux, 500 lux and 5000 lux.

An experiment was conducted to evaluate the performance of the multiple reset mode using the three stepped reset on the 5T pixel. The pixel response to different

illumination levels is demonstrated in Figure 4.15. As expected the stepped reset level controls the effective integration time depending on the illumination level. In particular, for a low illumination level at 50 lux, the photocurrent discharges the pixel throughout the integration period. However, for higher illumination levels at 500 lux and 5 klux, the photocurrents discharge the pixel until particular voltage levels controlled by the stepped reset voltage level are reached. The pixel is discharged again when the stepped reset drops to a lower voltage value. The period of the subsequent discharge process that reaches to the end of integration time is the effective integration period. One non-ideal feature that is apparent in the response is a slight voltage drop when the stepped reset voltage changes to a lower value. This occurs due to the parasitic capacitance between the gate and source node of the reset transistor. However, the effect is relatively small and the response of the pixel will be determined by the photocurrent.

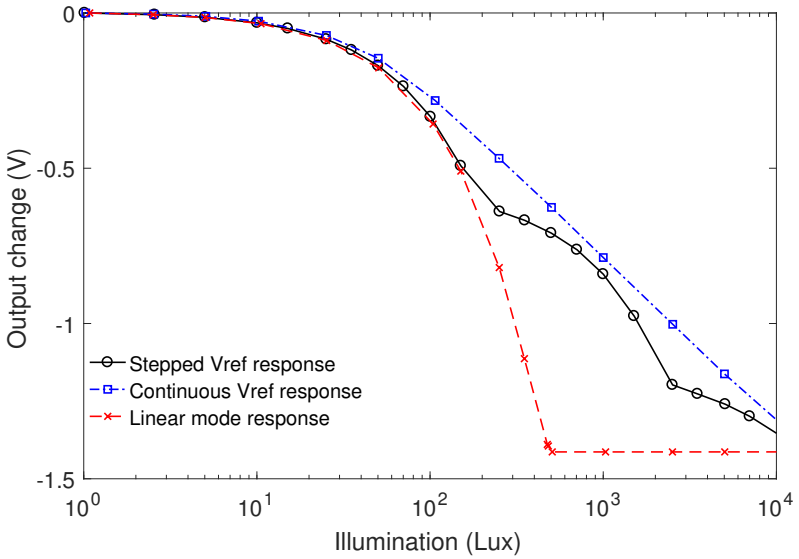


Figure 4.16: Three stepped reset mode photoresponse aiming for four decades of dynamic range.

The response of the pixel using stepped reset mode to different illumination levels for an integration period of 20 ms is shown in Figure 4.16. Responses from the

linear mode and the continuous $V_{ref}(t)$ are also included for comparison. The response shows three distinguishable curves corresponding to the three voltage levels of the stepped reset signal. In addition, the curves are approximate to the continuous $V_{ref}(t)$ response extending its dynamic range as expected. The response alignment is due to the use of the continuous $V_{ref}(t)$ to generate the three stepped reset $V_{ref}(t)$. In addition, this means that the stepped reset response can be controlled by the reset signal adapted from the reference voltage, $V_{ref}(t)$ developed for the integrating logarithmic mode.

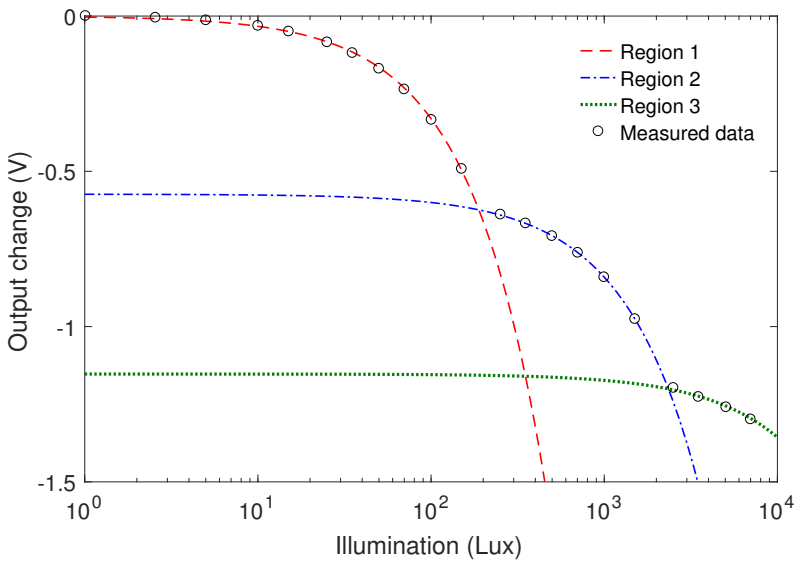


Figure 4.17: Response of the pixel showing it can be fitted to three linear regions.

The previous transient response of the pixel, demonstrated that the pixel is discharged linearly, similar to the conventional linear pixel. However the difference is for high photocurrent is that sometimes, the pixel voltage is held at a certain voltage. This suggests linear fits can be modelled to the pixel response to further investigate its performance. Figure 4.17 shows the pixel response which is fitted using three linear models. The parameters of the models are recorded in Table 4.3. The values of the slope show a reduction of approximately one order of magnitude from the preceding region as expected due to different duration of each step. This change means the

sensitivity of the response is reduced at each curve. From Equation 4.8 of the pixel response, the sensitivity of the response can be estimated such that:

$$Sensitivity = \frac{\mathrm{d}V_{pix}}{\mathrm{d}I_{ph}} = \begin{cases} \frac{t_{int}}{C_{pix}} & Region1 \\ \frac{(t_{int}-t_1)}{C_{pix}} & Region2 \\ \frac{(t_{int}-t_2)}{C_{pix}} & Region3 \end{cases} \tag{4.9}$$

Region	Offset (V)	Slope (V/lux)	Minimum Voltage (V)
Region 1	0.000	-3.4x10^{-3}	-0.574
Region 2	-0.574	-2.67x10^{-4}	-1.153
Region 3	-1.153	-2.04x10^{-5}	-1.5

Table 4.3: Extracted parameters from the modelled linear-logarithmic response.

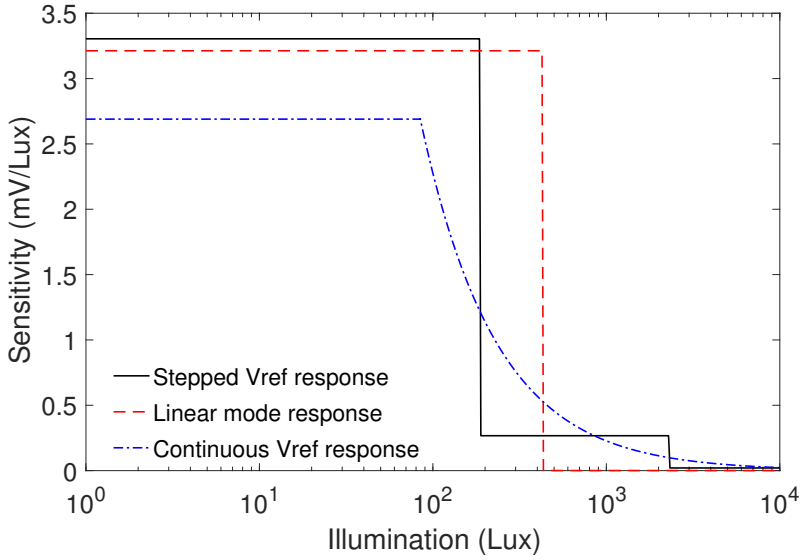


Figure 4.18: Sensitivity of the three stepped reset mode showing a comparable sensitivity to the linear response and higher than the integrating logarithmic response at low light levels.

The parameters of the fitted linear models are used to study the sensitivity of the response as shown in Figure 4.18. In addition, sensitivity plots modelled from measured data of linear mode and continuous $V_{ref}(t)$ responses are also shown for

comparison. The parameters of the continuous $V_{ref}(t)$ response used are from the previously modelled response for Chip 1 in Table 3.4. The sensitivity of the stepped $V_{ref}(t)$ response demonstrates sudden drops in the pixel sensitivity in relation to the logarithmic increase of illumination. In particular, the difference of the sensitivity at very low and high illumination is relatively high from -3.4x10^{-3} V/lux to -2.04x10^{-5} V/lux. At low illuminations from 1-190 lux, the stepped response has a better sensitivity in comparison to the continuous response whose sensitivity is at -2.7 mV/lux. This demonstrates that although the stepped $V_{ref}(t)$ is based from the continuous $V_{ref}(t)$, it has a better sensitivity at low illuminations due to the sudden drops in the stepped $V_{ref}(t)$.

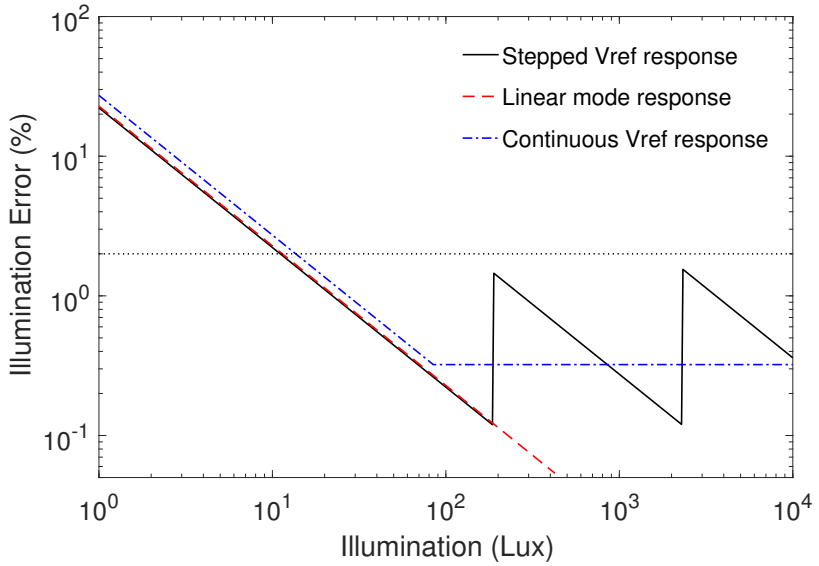


Figure 4.19: Percentage illumination error of three stepped reset mode showing peaks under 2% due to decreased sensitivities.

The impact of the sudden drops in the sensitivity can be measured from the illumination error. Figure 4.19 shows the percentage illumination error of the response which demonstrates the presence of small peaks as a result of the sensitivity drop. While the maximum peaks are still below the error threshold level, the peaks can exceed the threshold level, if $V_{ref}(t)$ parameters such as time, voltage and number

of steps are not selected appropriately. This aspect will be investigated in the next section. In addition, unlike the stepped $V_{ref}(t)$ response, the absence of peaks from the continuous response highlights the advantage of continuous $V_{ref}(t)$.

4.5.2 Eight stepped reset

Previous result demonstrated that the three stepped reset signal is sufficient to achieve high-quality images for four decades of dynamic range. In addition, one of the parameters that a user has to decide when generating the reset signal is the number of steps. It is expected that a higher number of steps will result in a pixel response which resembles the continuous response more closely. However, this advantage comes at a cost of higher circuit complexities when generating the $V_{ref}(t)$. When covering a dynamic range of more than four decades while having the same pixel output range, a higher number of steps is expected to minimise the illumination error. To investigate how the number of steps affect the image quality, a three stepped reset signal and eight stepped reset signal aiming at a pixel response of six decades range were performed. The choice of eight for the number of steps was based on previously reported studies [55, 78]. In addition, the equal voltage strategy previously used in generating the three stepped reset voltage was adopted in order to divide the number of steps and obtain the voltage levels and the transition times.

The limiting factor in the experiment is the maximum brightness of the light source. However, the effect of higher light levels on a pixel operating with an integration of 20 ms can be replicated by increasing the integration time. Results from integration times of 20 ms, 200 ms and 2 s have therefore been combined to produce six decades of dynamic range [78]. To account for the different integration time, the corresponding illuminations of the responses have been multiplied by a factor of 1, 10 and 100 respectively. When the pixel responses are plotted together, a single response with an effective dynamic range of six decades can be produced.

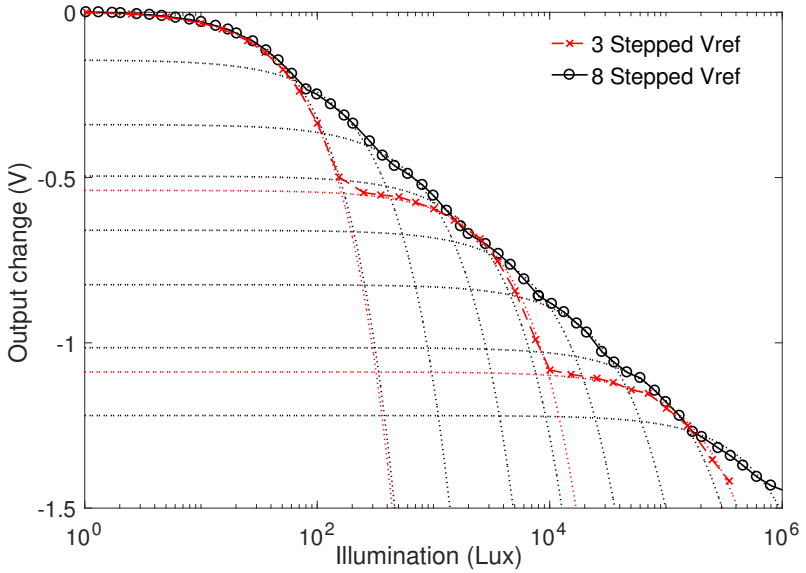


Figure 4.20: Three and eight stepped reset mode photoresponse aiming for six decades of dynamic range.

Figure 4.20 shows pixel responses of three stepped reset and eight stepped reset covering six decades of dynamic range. The measured responses were fitted linearly with three and eight linear regions respectively. The eight stepped response has a nearly straight logarithmic response as expected. However, for the three stepped response, a closer observation reveals that the response is not ideal. In particular, the nearly horizontal lines present at the start of each curve. The impact of this feature can be assessed from the percentage illumination error.

The percentage light error from the estimated light falling into the pixel for both three and eight stepped responses are shown in Figure 4.21. For the three stepped response, the peaks due to the reset voltage drops are more than 7% which are higher than the acceptable threshold level. However, for the eight stepped response, the peaks due to the reset voltage drop is well below the threshold level of 2%. This confirms that when extending the dynamic range, the number of steps, need to be considered appropriately. In particular, the three stepped response can only cover four decades of dynamic range if 2% of accuracy is demanded. When the dynamic

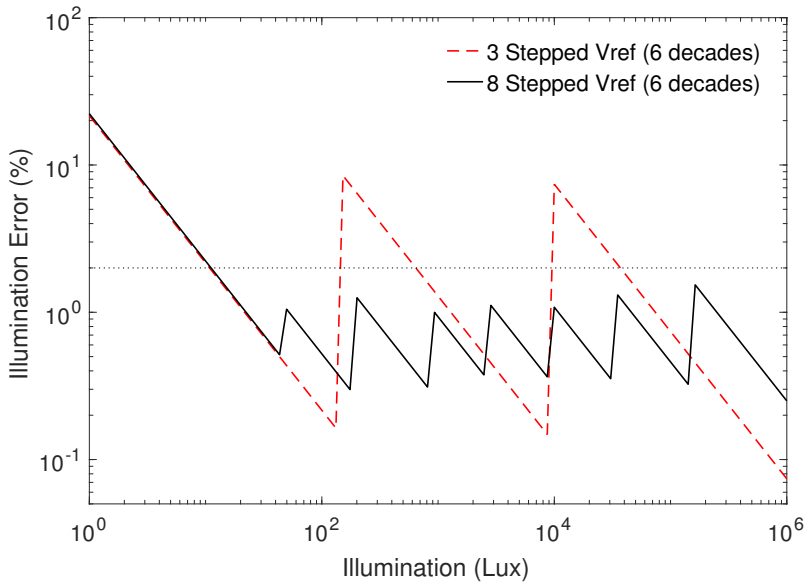


Figure 4.21: Percentage error showing that for response of six decades of dynamic range, eight stepped reset V_{ref} is required in order to have an error of less than 2% while three stepped reset V_{ref} yields peaks of more than 2%.

range is extended to six decades, eight stepped response is required to achieve similar accuracy.

4.6 Comparison of modes

The dynamic range of an imager can be extended by increasing its sensitivity of minimum detectable photocurrent at low illuminations or maximum detectable photocurrent before saturation. This particular study is only focused on extending the dynamic range at high illuminations. The 5T pixel architecture offers the opportunity to implement most of the proposed modes of dynamic range extension. In particular, the 5T pixel was operated in different modes by controlling the reference voltage $V_{ref}(t)$. This approach is advantageous since all the modes were measured from a single pixel using the same technology and experiment conditions.

The metrics that have been used to study the performance of different modes are the dynamic range, low light sensitivity and the illumination error. These metrics

serve as a basis to properly understand the tradeoffs of each mode. In addition, the advantages and drawbacks of implementing each mode will also be reviewed. Summary of the performance of all the modes is recorded in Table 4.4.

Mode	DR (dB)	Dark Sensitivity (mV/lux)	Sensitivity (mV/lux)	Illumination Error at Extended DR (%)
Linear	54	3.2	0-3.2	$> 2\%$
Logarithmic	> 80	< 11	0.002-11	$> 2\%$
Linear-log	51 (linear) + >29 (log)	3.4	0.003-3.4	$> 2\%$
Integrating log	> 80	2.7	0.02-2.7	$< 2\%$
Multiple reset	> 80	3.3	0.02-3.3	$< 2\%$

Table 4.4: Summary of the performance for different DR extension modes.

The minimum pixel requirement to perform linear mode needs only three transistors. This offers a great advantage in terms of spatial resolution and increased of fill factor. Furthermore, the sensitivity of the mode is constant throughout the detectable illumination at 3.2 mV/lux. The sensitivity can be increased by extending the integration time at the cost of lower frame rate. However, the main drawback of the linear mode is its limited dynamic range at 54 dB. In addition, percentage illumination error ranges from more than 10% to below 2%. This error serves as a reference when comparing to other modes. The control of the linear mode is relatively simple by generating a reset signal. The reset operation can be achieved through hard or soft reset which offers tradeoffs between temporal noise and transient response at low illuminations. In particular, the hard reset is when the gate voltage is raised higher than V_{dd}; improves the slow transient response at low illuminations that causes image lag. This is due to the incomplete charge transfer. However, hard reset comes at a cost of nkT/C noise value double than that of the soft reset [40]. The reset noise can be significantly reduced by correlated double sampling (CDS). For this purpose,

additional peripheral circuitry for the pixel array is needed in addition to ADC for data conversion. These few requirements suggest that the power consumption for this mode is relatively low.

The logarithmic mode was first proposed in order to overcome the limited dynamic range suffered by the linear mode. Through this mode, the wide dynamic range can be achieved in a small signal swing [5]. The measurement result has demonstrated a dynamic range of 80 dB with a potential of a higher dynamic range given the pixel output swing available. The mode is also most sensitive at very low illumination with a value up to 11 mV/lux. This is due to the fact that the pixel has a logarithmic relationship with the photocurrent. However, the sensitivity drops significantly as illumination increases compared to linear mode sensitivity which remains relatively constant at low illuminations. The reduced sensitivity at a logarithmic rate makes the pixel very susceptible to temporal noise. This leads to illumination error that is above 2% throughout the measured illumination. It is well known that the mode has a very slow transient response at low illuminations due to its operation in the subthreshold region [49]. However, this effect is not captured in the plot since the measurements had been done when the responses had reached steady state. Another drawback of this mode is its dependence on the transistor parameters nkT and V_{th}. V_{th} in particular contributes to high FPN. Due to continuous operation of logarithmic operation, conventional CDS operation is not applicable to reduce FPN. Therefore, various calibration schemes have been proposed to address this issue. However, most of the schemes require additional transistors which result in reduced fill factor [37, 6, 21]. The high FPN residual with wide dynamic range makes logarithmic mode very attractive for applications where the aesthetic of an image is not of concern such as machine vision.

The lin-log mode that requires a simple $V_{ref}(t)$ can achieve advantages offered by both linear and logarithmic modes. In particular, the low light sensitivity compa-

rable to the linear mode and the dynamic range extension at high illuminations is obtained. Experimental results have been presented which show that the measured linear response ranges up to 51 dB and the logarithmic extension is 29 dB. The logarithmic extension can potentially increase given the available output swing. However, the sensitivity at which the dynamic range is extended drops significantly from 3.4 mV/lux to below 0.08 mV/lux. This value of 0.08 mV/lux is at the same range to that of logarithmic mode due to the same response. For this reason, the percentage illumination error rises higher than 2% when the response changes from linear to logarithmic. The signal that controls the change of response from linear to logarithmic is the intermediary voltage V_{log}. This signal requirement suggests that additional peripheral circuitry is required when compared to circuit implementation of logarithmic mode. Similar to logarithmic mode, this mode suffers from FPN [38]; in particular, at the illumination region with a logarithmic response. A scheme that has been proposed to remove FPN requires additional transistors [20]. Furthermore, despite the overall FPN reduction, FPN at the transition point still remains un-addressed [38].

Integrating logarithmic mode was proposed in order to offer an improved logarithmic response. Unlike the other logarithmic mode, the sensitivity of the integrating logarithmic response can be adaptable and is not fixed to the transistor parameter and the operating temperature, nkT. At low illuminations, the dark response was observed to have slightly lower performance than the linear mode and the sensitivity is measured at 2.7 mV/lux. The sensitivity measured at high illuminations is still higher when comparing to logarithmic and lin-log responses. Hence, better quality images are expected at high illuminations. This aspect is confirmed when plotting the illumination error which shows that the error is below 2% throughout the high illumination region. The main drawback of this mode is its high FPN. This is due to its response that is dependent on the threshold voltage of the reset transistor. A CDS procedure has been shown to significantly overcome the offset FPN. However, a

more sophisticated procedure is required to suppress the effect of gain FPN as shown in Chapter 3 [59]. One primary challenge of this mode is generating $V_{ref}(t)$ which requires very accurate logarithmic amplifiers [27]. This in turn increases the power consumption and area requirement. In conclusion, the integrating logarithmic mode offers a superior image performance than the previous three modes. However this advantage comes at the cost of complex circuitry and additional power consumption. The challenging $V_{ref}(t)$ requirement means that its tradeoff with image performance needs to be carefully considered.

The multiple stepped reset that had been performed was generated from $V_{ref}(t)$ of the integrating logarithmic mode. As a result, the multiple reset response is a linear response approximation to the integrating logarithmic response. Two different stepped resets have been performed and measured. In particular, a three stepped reset for four decades of dynamic range and an eight stepped reset for six decades of dynamic range have been generated. Both operations demonstrate dark responses that are comparable to that of linear mode. This aspect is confirmed when the sensitivity of the responses were both measured at 3.3 mV/lux. However, in the case of three stepped reset, the sudden drops of sensitivity are observed from 3.3 mV/lux to 0.27 mV/lux and subsequently to 0.02 mV/lux. Despite of the drops, the sensitivity levels are still higher in comparison to the logarithmic mode and lin-log mode. This means that the drops are not very significant. The impact of the sensitivity drops can be ignored when measuring the percentage illumination error. The peak error is less than 2% for three stepped response covering four decades of dynamic range. However, when it is aimed at six decades of dynamic range a higher number of steps is required to better approximate the integrating logarithmic response. In particular, a minimum number of eight steps is required to demonstrate a response with error less than 2%. This mode that is based on the integrating logarithmic mode means that the FPN is expected to be similar. This also indicates that a similar FPN correction

schemes can be applied. Furthermore, when generating $V_{ref}(t)$, accurate analogue circuitry with precise timing controls are required to generate the reset signal. In addition when driving the row frame array, the reset signal requires high current to pull down the row capacitance at a fraction of time. This operation suggests that it consumes a lot of power.

4.7 Summary

This chapter reviewed different dynamic range extension modes that can be performed on the 5T pixel. More specifically, the response of the modes such as linear, logarithmic, lin-log, integrating logarithmic and multiple stepped reset have been measured. The response of linear mode has been used as a reference when comparing the performance of other responses. All the responses, except logarithmic response highlight constant sensitivity for the dark response. In contrast, logarithmic response which achieves high sensitivity at very dark region degrades significantly. This suggests that linear response at low illuminations is preferable. However, integrating logarithmic response and multiple stepped resets are desirable at high illuminations due to its high sensitivity when compared to the logarithmic response of logarithmic and lin-log modes. Furthermore, the challenges of implementing each mode were also reviewed. In summary, modes that demonstrate low illumination error while achieving wide dynamic range require demanding additional circuitry that leads to high power consumption. This tradeoff needs to be considered when choosing a suitable mode.

Chapter 5

Piecewise linear $V_{ref}(t)$ CMOS imager

5.1 Introduction

In the previous chapter, the responses of pixels to five different reference voltages were compared. From the five responses, the multiple stepped resets and the integrating logarithmic were observed to demonstrate low illumination error and a wide dynamic range. The $V_{ref}(t)$ used to obtain the two responses were generated off-chip using a waveform generator. A potential implementation to generate $V_{ref}(t)$ in the same substrate as the imager, needs to be explored to have a truly integrated image sensor. In this chapter, a study to explore viable implementations of $V_{ref}(t)$ signal generation is described. In particular, for multiple stepped reset mode, a $V_{ref}(t)$ signal generator based on multiplexers is reviewed. Then for the integrating logarithmic mode, a $V_{ref}(t)$ signal generator based on logarithmic amplifiers is studied. As a result of the study, a new $V_{ref}(t)$ model based on piecewise linear is proposed. The new $V_{ref}(t)$ allows a possible implementation of a $V_{ref}(t)$ signal generator alongside a 2D array. Finally, a chip implementation of a 2D imager comprising a $V_{ref}(t)$ generator and

pixel array is presented.

5.1.1 Multiple stepped reset $V_{ref}(t)$

To generate the multiple stepped reset $V_{ref}(t)$, voltage and timing specifications of $V_{ref}(t)$ are first required. These values were obtained using $V_{ref}(t)$ model in Equation 2.14 with parameter values listed previously in Table 2.2 and Table 2.3. Furthermore, based on the comparative study conducted in Chapter 4 on multiple stepped resets, it was demonstrated that a $V_{ref}(t)$ with eight segments is required to achieve illumination error below 2% for six decades of illumination. Therefore, Table 5.1 shows the voltage and timing required for an eight stepped reset $V_{ref}(t)$ generated for an integration period of 20 ms with a logarithmic slope of 350 mV/dec.

Step	1	2	3	4	5	6	7	8
Voltage	3.035 V	2.772 V	2.512 V	2.489 V	1.986 V	1.723 V	1.463 V	1.2 V
Duration	15.5 ms	3.5 ms	773 μs	177 μs	40 μs	9 μs	2 μs	440 ns

Table 5.1: Voltage and time requirement for eight stepped reset $V_{ref}(t)$.

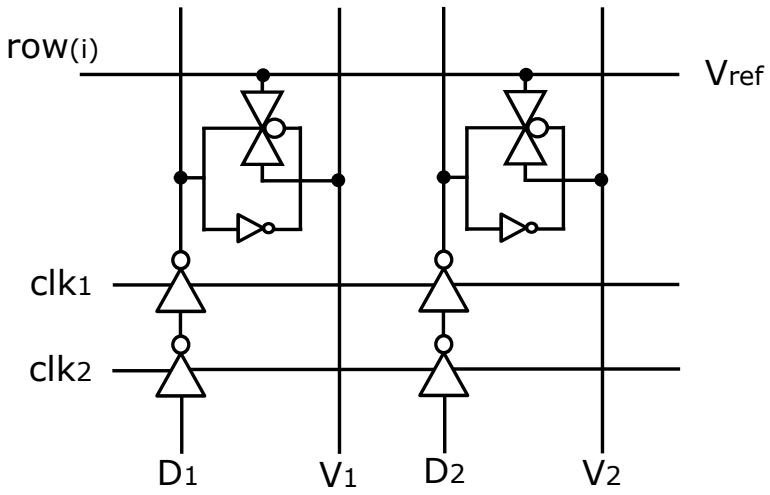


Figure 5.1: An example of a two stepped reset $V_{ref}(t)$ signal generator for one row [55]. The two voltage levels are defined by V_1 and V_2.

Decker and co-workers have proposed a multiple stepped reset signal generator

which can be implemented using a multiplexer for each row of pixels [55]. Figure 5.1 shows an example of a two stepped reset $V_{ref}(t)$ signal generator which can be extended to eight steps. The output of the multiplexer is a $V_{ref}(t)$ whose inputs correspond to different voltage levels. Only one voltage level V_n is connected to $V_{ref}(t)$ at any time. The voltage selection is controlled by the digital signals D_n. For example, when D_1 is high, $V_{ref}(t)$ is connected to V_1 when clk_1 is high. In a case of eight steps, a three bit controller can be used as a decoder to enable one input out of eight input voltage levels to be connected to the output. When implementing the signal generator in an array, the $V_{ref}(t)$ signal needs to be delayed to allow sufficient time for the row read out. Therefore, the signals controlling the decoder need to have proper timing considerations so that the $V_{ref}(t)$ generated is staggered in time between rows. To achieve this, an array of digital shift register can be used as delay blocks when passing down the three bit signals [77]. However, one main challenge of generating the multiple reset $V_{ref}(t)$ is the sharp voltage transition required, in particular at the last reset step. The last reset step has the shortest time duration which lasts about 440 ns. The transition time at this step can be estimated to be a tenth of this value. Furthermore, the accuracy of the last step affects the pixel response in particular at the high illumination region. When a pixel array is scaled up for a large pixel array, the row capacitance multiplies and the value can be between 1 to 5 pF. The current required to drive a 5 pf capacitance through a 263 mV voltage change in 40 ns can amount up to tens of micro amperes per row for one step. This current requirement could be significantly reduced if the voltage changed more slowly and this might be a closer approximation to the continuous $V_{ref}(t)$

5.1.2 Integrating logarithmic mode

Another possible mode to achieve wide dynamic range response that has low illumination error is the integrating logarithmic mode [58, 27]. The logarithmic characteristic

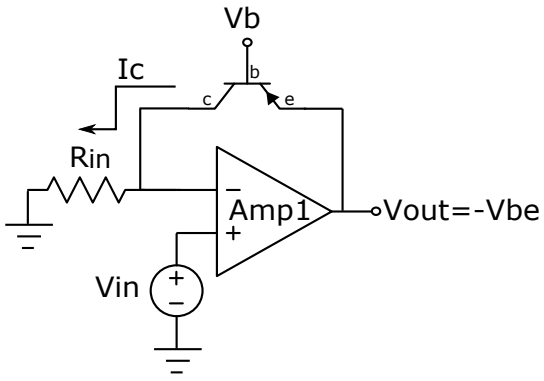


Figure 5.2: A logarithmic amplifier using a BJT at the feedback loop.

of $V_{ref}(t)$ can be generated using a logarithmic amplifier [79]. A simple logarithmic amplifier is depicted in Figure 5.2 which consists of an op-amp and a Bipolar Junction Transistor (BJT) in its feedback loop. The non-linearity of BJT means its characteristic can be exploited to produce a logarithmic voltage output. Furthermore, a lateral BJT can be formed by a MOS transistor and has been demonstrated to be compatible with any bulk CMOS technology [80]. Assuming the op-amp is ideal, the voltage across the input resistor R_{in} is equal to V_{in} due to zero input offset voltage. The collector current I_c, therefore, can be set by V_{in}. When the BJT is connected in a negative feedback, the output of the amplifier determines the emitter voltage in order to keep the current through BJT equal to I_c. The collector current and the output of the op-amp can be expressed as [81]:

$$I_C = I_S e^{\frac{V_{be}}{V_T}} = \frac{V_{in}}{R_{in}} \tag{5.1}$$

Therefore

$$V_{out} = -V_T \ln\left(\frac{I_C}{I_S}\right) = -V_T \ln\left(\frac{V_{in}}{R_{in} I_S}\right) \tag{5.2}$$

where I_C is the collector current, I_S is the reverse saturation current and V_T is the thermal voltage. Equation 5.2 shows that V_{out} can be controlled by selecting the value of V_{in} and R_{in}. However this equation is dependent on I_S which is also temperature

dependent [82].

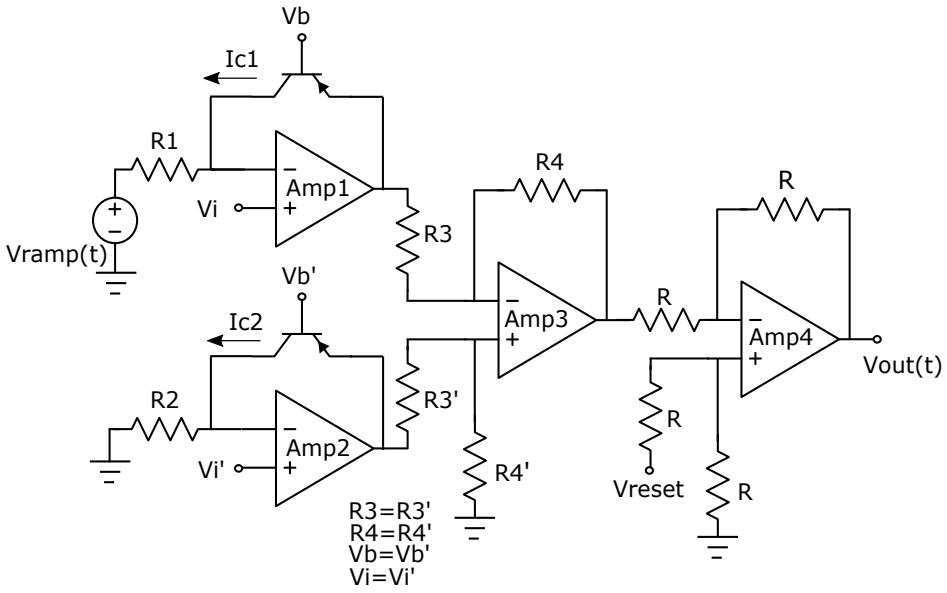


Figure 5.3: Multi-stage amplifiers to generate $V_{ref}(t)$ for integrating logarithmic response [27].

To remove I_S a partially temperature compensated logarithmic amplifier has been proposed previously as shown in Figure 5.3. These multi-stage amplifiers are based on the simple logarithmic amplifier with a slope value that can be defined by users. A second logarithmic amplifier $Amp2$ is included in order to cancel out I_s. The cancellation is achieved through a differential amplifier which is performed by $Amp3$. Furthermore, resistor $R3$ and $R4$ can be used to set the slope of V_{out}. Finally, $Amp4$ sets the reset level which provides an offset to $V_{ref}(t)$ level. The output of this multi-stage amplifier can be expressed as:

$$V_{out} = V_{reset} - \frac{R4}{R3} V_T \ln\left(\frac{I_{c2}}{I_{c1}(t)}\right) \tag{5.3}$$

The degree of logarithmic compression as shown in Equation 5.3 is determined by the current ratio $I_{c2}/I_{c1}(t)$. $V_{ref}(t)$ has a rapid rate of change in particular towards the end of the integration period. For a $V_{ref}(t)$ with a slope of 350 mV/dec aimed for six decades of dynamic range, the highest rate is up to 1 V/μs. The advantage

of this circuit is the rapid change of $V_{ref}(t)$ can be generated from a slow ramped voltage, $V_{ramp}(t)$. For example, a $V_{ramp}(t)$ for an integration period of 20 ms and 1 V of voltage change means the rate of change is 50 μV/μs. However, the main challenge of implementing the multi-stage log amplifiers arises when employing a rolling shutter system for a prospective 2D imager. In particular, four amplifiers, two lateral BJT's and several resistors need to be fit in every row within the pixel pitch that has been designed which is 5 μm. Therefore this approach is not practical on the basis of area limitation imposed by the pixel. In addition, the use of BJT introduces an additional source of FPN through V_T and I_S parameters.

5.2 Piecewise linear (PWL) approximated $V_{ref}(t)$

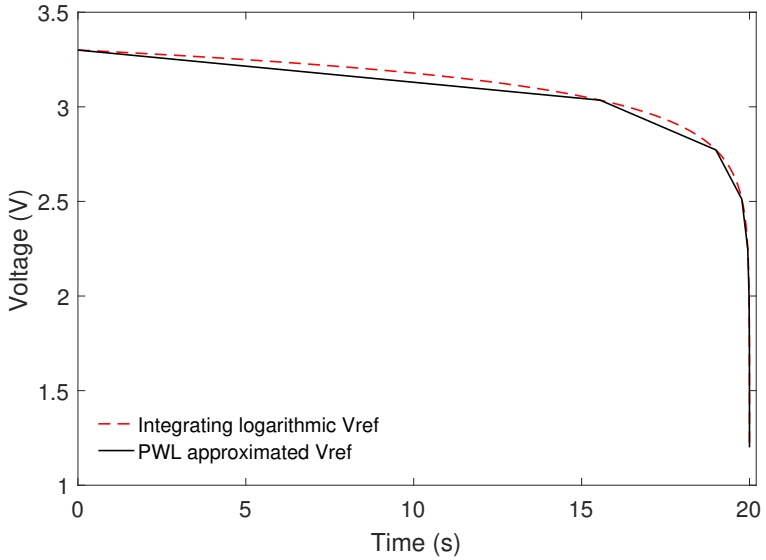


Figure 5.4: A PWL based $V_{ref}(t)$ generated from the original $V_{ref}(t)$ using eight segments for a slope of 350 mV/decade.

The previous section explored different designs of $V_{ref}(t)$ generation that would produce an adaptive logarithmic response. The challenges associated with previous designs such as the area requirement and power consumption make the designs impractical for array implementation in a rolling shutter system. In this section, a

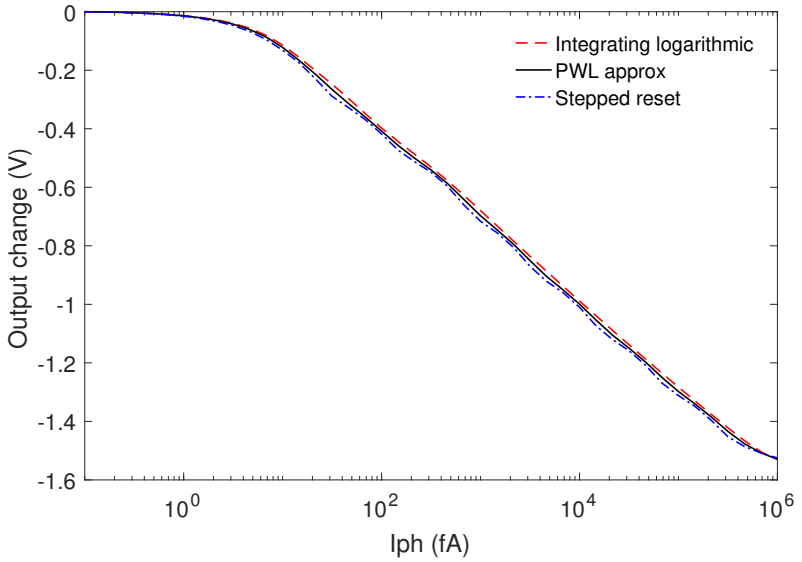
pseudo integrating logarithmic $V_{ref}(t)$ by way of piecewise linear (PWL) approximation is proposed. In particular, the voltage range of the original $V_{ref}(t)$ model is divided into eight segments equally. The segments are then connected by straight lines with various linear slopes. A clear advantage of this approach is that it does not require a rapid transition as in the case of multiple stepped reset $V_{ref}(t)$. In contrast, the gradual voltage change of $V_{ref}(t)$ means that it can be generated using multiple current sinks. In addition, as a result of the voltage approximation, a high precision requirement of purely logarithmic $V_{ref}(t)$ by way of logarithmic amplifiers is no longer necessary.

A PWL based $V_{ref}(t)$ with a slope of 350 mV/dec, 20 ms integration time and V_{reset} of 3.3 V has been generated as shown in Figure 5.4. The parameters of the $V_{ref}(t)$ are recorded in Table 5.2. The most critical specification of $V_{ref}(t)$ is the last segment which requires the fastest transition time. The value of this change at 572 mV/μs is lower at approximately half and one order of magnitude less than that of integrating logarithmic $V_{ref}(t)$ and multiple stepped reset $V_{ref}(t)$ respectively. This reduces the current requirement for the $V_{ref}(t)$ generator.

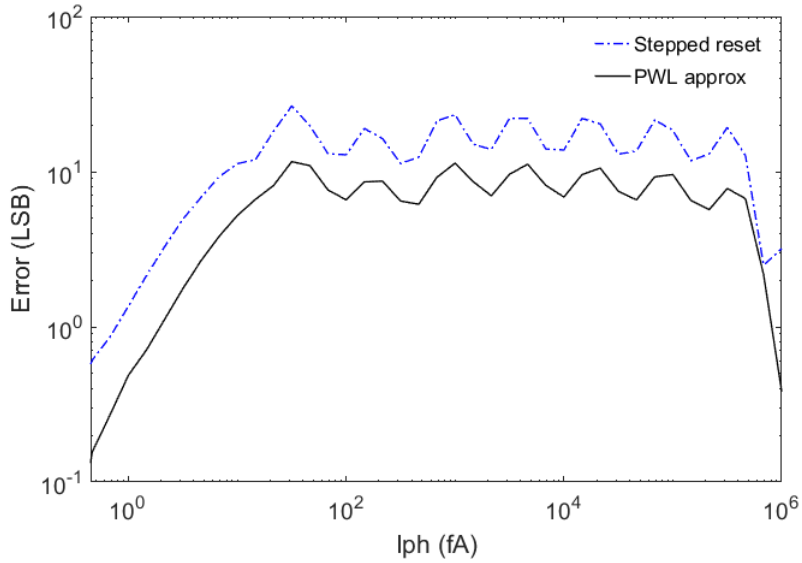
Segment	Start Voltage	End Voltage	Duration	Discharge Rate
1	3.30 V	3.04 V	15.5 ms	-17 μV/μs
2	3.04 V	2.77 V	3.5 ms	-76 μV/μs
3	2.77 V	2.51 V	773 μs	-337 μV/μs
4	2.51 V	2.49 V	177 μs	-2 mV/μs
5	2.49 V	1.99 V	40 μs	-7 mV/μs
6	1.99 V	1.72 V	9 μs	-29 mV/μs
7	1.72 V	1.46 V	2 μs	-130 mV/μs
8	1.46 V	1.20 V	440 ns	-572 mV/μs

Table 5.2: Parameter for PWL based $V_{ref}(t)$ extracted from the original $V_{ref}(t)$ generated in Figure 5.4.

The PWL based $V_{ref}(t)$ is fed to a test pixel and simulated in Cadence. Figure 5.5a shows the simulated response of the PWL $V_{ref}(t)$ for photocurrent from 0.1 fA to 1 nA covering seven decades of dynamic range. For comparison, the multiple stepped reset



(a) Pixel response after CDS of the eight segmented PWL based $V_{ref}(t)$ in comparison to the integrating logarithmic $V_{ref}(t)$ and eight stepped $V_{ref}(t)$.



(b) Error from the integrating logarithmic response in LSB

Figure 5.5: Pixel responses of the eight segmented PWL based $V_{ref}(t)$ in comparison to multiple stepped and integrating logarithmic responses.

$V_{ref}(t)$ and the integrating logarithmic $V_{ref}(t)$ responses are also depicted. The results show that the PWL approximated response falls in between the multiple stepped reset response and the integrating logarithmic response as expected. This suggests that the illumination error of the PWL response is comparable to the other two responses. Furthermore, the differences of multiple stepped reset and PWL based $V_{ref}(t)$ pixel responses from the ideal integrating logarithmic $V_{ref}(t)$ response are shown in Figure 5.5b. This difference is measured in term of LSB error assuming a 10 bit ADC is used covering the output range available. The error of the PWL based $V_{ref}(t)$ is less than 10 LSB throughout the spectrum of the photocurrent. In addition, the error is observed to be 5 to 10 LSB lower than that of the stepped reset $V_{ref}(t)$. This is expected since the PWL based $V_{ref}(t)$ has a gradual change in comparison to the multiple stepped reset $V_{ref}(t)$.

5.2.1 PWL $V_{ref}(t)$ generation

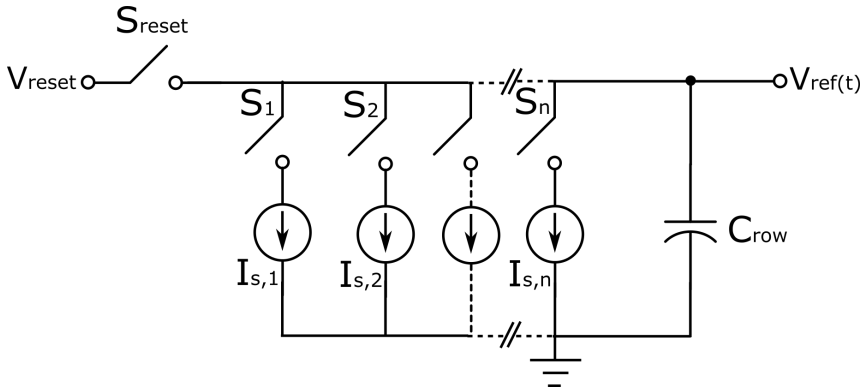


Figure 5.6: Simplified $V_{ref}(t)$ generator based on multiple current sinks.

A simple way to generate the PWL $V_{ref}(t)$ is using multiple current sinks. The current sinks can be used to discharge the pixel's row capacitance as shown in Figure 5.6. Each current sink has a different value corresponding to the discharge rate of each segment of $V_{ref}(t)$. Only one current sink is connected to discharge the row capacitance at one time. This operation is controlled by the switches which are

connected to a digital block. The discharge of the row capacitance is performed after the row capacitance has initially been charged to a reset voltage. Once the last current sink has finished discharging the row capacitance, then the readout process begins.

5.2.2 Row capacitance

In order to generate the current sinks, the row capacitance of the pixels needs to be estimated. Then the corresponding values of the current sinks can be determined. The capacitance is formed by parasitic capacitances associated with the gate of the reset transistor of each pixel in a row.

The row capacitance is the cumulative value of each pixel's parasitic capacitance. The capacitance value for each pixel is dependent on the size of the reset transistor. Due to the minimum size of the reset transistor used, a typical value is very small and is usually less than 1 fF. The value of the row capacitance can be estimated using a transient simulation. More specifically, if a reference current is used to discharge the reset voltage of a row of pixels, the row capacitance can then be estimated from the voltage change after a period of time. Since the row capacitance tends to be very small, a reference capacitance is added in parallel to make the estimation.

To estimate the value of the parasitic capacitance at the gate of the reset transistor, a few rows containing a different number of pixels were simulated. Figure 5.7 shows the result of the discharge rate of the reset voltage on rows containing 128 pixels, 512 pixels and 1024 pixels respectively. The reference current and capacitance used were 100 pA and 1 pF. The parasitic capacitance per pixel obtained from the results is estimated to be between 0.2 - 0.25 fF. In order to obtain the discharge rates specified previously in Table 5.2, the small value of the capacitance means that the value of the current sink required will also be very small (in fA range). This poses a challenge when generating the small current. One way to address the challenge is to create a large pixel array for example 1000 pixels per row. However, this is dependent on the

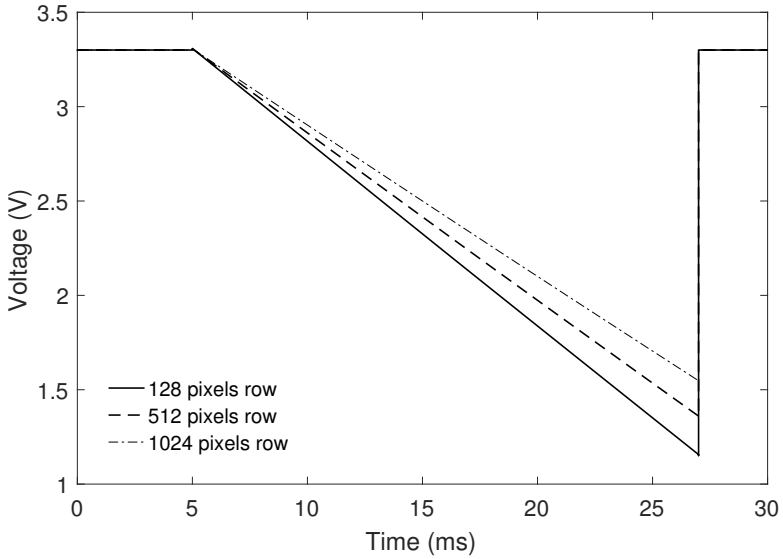


Figure 5.7: Transient response of rows with 128 pixels, 512 pixels and 1024 pixels when the reference current discharging the row and reference capacitance.

silicon area available for the image sensor. Alternatively, an additional capacitance can be added at each row to increase the overall value of the row capacitance such that the total row capacitance is:

$$C_{row} = \sum_{i}^{N} (C_{gd,M1,i} + C_{gs,M1,i}) + C_{ref} \tag{5.4}$$

where N is the total number of pixels in a row, $C_{gd,M1,i}$ is the gate-drain capacitance of transistor $M1$, $C_{gs,M1,i}$ is the gate-source capacitance of transistor $M1$ and C_{ref} is the added capacitance.

In a chip implementation using UMC 180 nm technology, a (MIM) type capacitor is available and has been chosen for the row capacitance. The MIM capacitor is formed between Metal 5 and 6. The MIM capacitor which is formed by metal layers offers the advantage as optical shields to peripheral circuits of an image sensor. Its flexibility to be inserted between metal layers means no additional silicon area is necessary for the capacitor. In addition, its distance from the substrate reduces the substrate coupling effect and makes it suitable for high precision applications [83].

5.2.3 Current sink $V_{ref}(t)$ generator

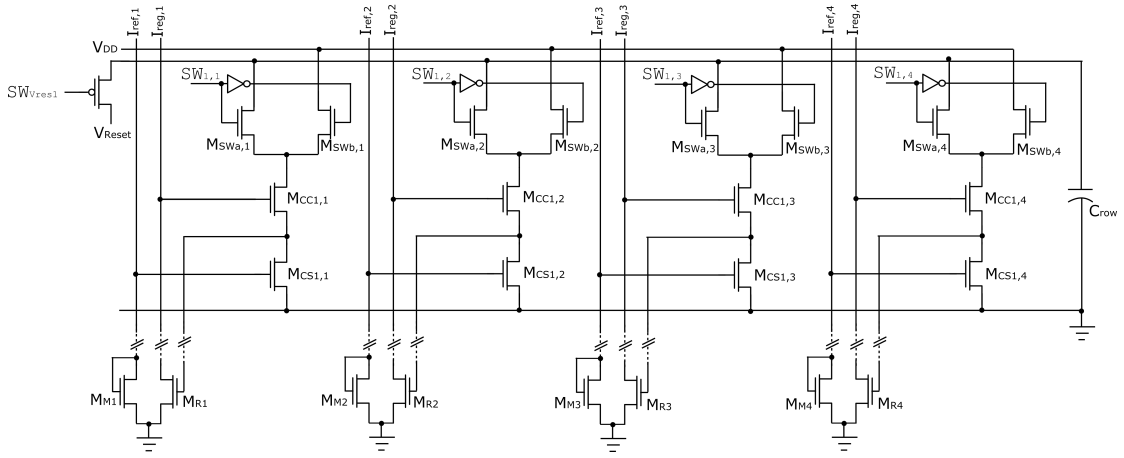


Figure 5.8: Proposed $V_{ref}(t)$ generator using multiple regulated current sinks for four current sinks in 1 row operation.

The small pixel pitch of 5 μm available means that the designs of row circuitries including the current sink have to be simple to satisfy the area requirement. In addition, the current sink needs to provide a stable current covering a wide output swing. Figure 5.8 shows a proposed multiple current sink architecture to generate a four segmented $V_{ref}(t)$. In each unit of the current sink architecture, a differential pair is used. It consists of transistors M_{SWa} and M_{SWb} which operate as switches to sink current either from the charged row capacitance C_{row} or the power source. In addition, regulated cascode current mirrors have been chosen in order to provide a constant current over the $V_{ref}(t)$ range. This is achieved through negative feedback of the shared transistor M_{Rn} which increases the output resistance and the output swing [44]. The minimum voltage of $V_{ref}(t)$ at 1.2 V, is sufficiently high to maintain both transistors M_{CC} and M_{CS} in saturation. All the transistors have been sized to 1.5μm/1μm to satisfy the pitch size. Furthermore, I_{ref} and I_{reg} are set to be equal and the currents are mirrored at the array level and sourced externally off-chip. The ability to control the current values in order to change $V_{ref}(t)$ is an important aspect when testing a prototyped imager. Once the intended pixel response has been

confirmed through an optical test, an ideal design for the current sink is to use on-chip current references to generate the required currents.

A simulated $V_{ref}(t)$ was generated using the proposed $V_{ref}(t)$ generator with a 25 MHz clock controlling the switching of the $V_{ref}(t)$ generator. The input values of the generator such as current and timing specifications are listed in Table 5.3. These requirements are extracted from the $V_{ref}(t)$ parameter values recorded previously in Table 2.2 and 2.3. The current sink generated $V_{ref}(t)$, as well as Matlab generated $V_{ref}(t)$, are shown in Figure 5.9a. A close inspection reveals that the two $V_{ref}(t)$s are not exactly the same. In particular, the voltage knee points are different because of slightly different current values and the time resolution of the clock used. These result in discharge rates that are different from the ideal Matlab model.

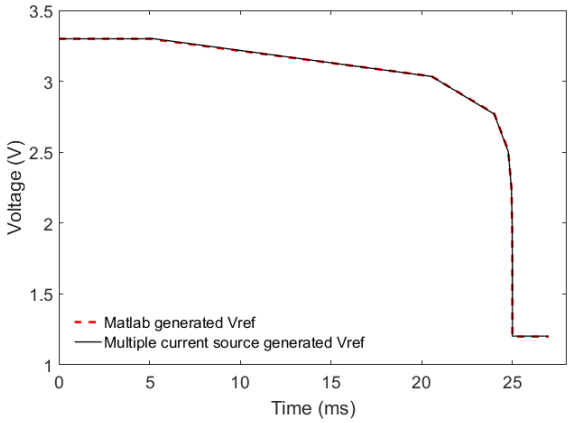
The impact of the generated $V_{ref}(t)$ can be analysed further in the pixel responses and response error in Figure 5.9b and 5.9c respectively. The difference of the response generated by the two models demonstrate errors less than 4 LSB throughout the six decades of dynamic range.

Segment	1	2	3	4	5	6	7	8
I_{ref}, I_{reg}	18 pA	82 pA	360 pA	2 nA	7 nA	32 nA	140 nA	620 nA
Duration	15.5 ms	3.5 ms	773 μs	177 μs	40 μs	9 μs	2 μs	440 ns

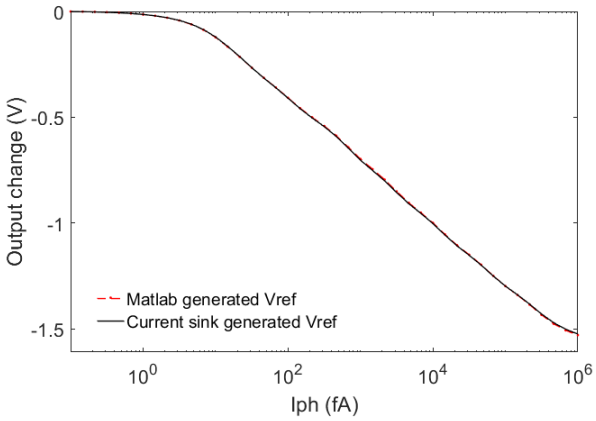
Table 5.3: Current and time requirement for eight stepped reset $V_{ref}(t)$ with V_{reset} = 3.3 V, slope = -350 mV/dec, C_{row} = 1 pF.

5.3 CMOS imaging array

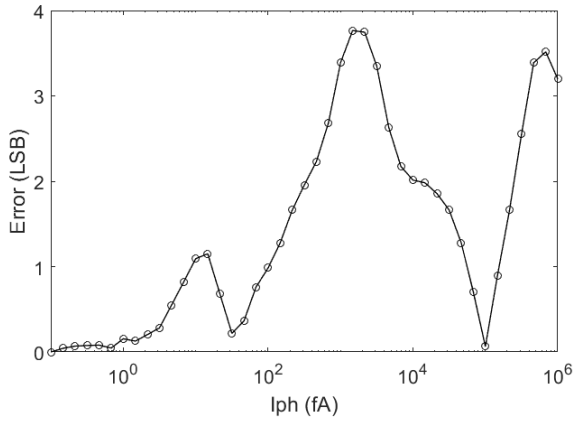
The design of the proposed current sink $V_{ref}(t)$ generator has been demonstrated. In addition, its operation on a test pixel has been simulated. The generator design is extended to operate on a 2D pixel array. In particular, to implement in an array, shift registers are used at each segment of current sink in order to control the timing



(a) $V_{ref}(t)$ comparison



(b) Output change comparison



(c) LSB error of the current sink generated $V_{ref}(t)$ response from the Matlab $V_{ref}(t)$ response

Figure 5.9: Comparison between Matlab (ideal) and current sink generated $V_{ref}(t)$ and pixel responses of the two $V_{ref}(t)$s simulated in Cadence. Error between the two responses measured in LSB.

signals appropriately. Furthermore, other peripheral circuits are also needed such as scanners and readout stage. This section presents the details of these circuits.

5.3.1 Row and column scanners

Scanners are used in imagers for row and column addressing of a pixel array during read out. The scanner architecture consists of a chain of flip-flops which functions as shift registers. In particular, the flip-flop used is a master-slave positive edge triggered as shown in Figure 5.10. The use of the flip-flop reduces the complexity of the required control signals in contrast to other types of scanner such as decoder based scanner. More specifically, in a rolling shutter system, the $V_{ref}(t)$ signal generated is cascaded down the rows. Therefore, the duration of the pixel operation needs to be staggered between the rows in order to allow sufficient time for the readout of each pixel. The layout of the pixel pitch size of 5 μm means a tight signal routing is required. This was achieved using M1 to M4 layers available. Furthermore, the spatial constraint of the pitch means minimum gate length of the transistors were used for nMOS and pMOS. The layout of the register shown in Figure 5.11 has a dimension of 47 μm x 5 μm. As the registers were designed using thin oxide transistors, level up shifters were implemented to raise the digital voltage of 1.8 V to 3.3 V used in analogue blocks. In addition, to avoid potential clock skew issues, the clock signals clk and $\overline{clk}$ are non-overlapping signals.

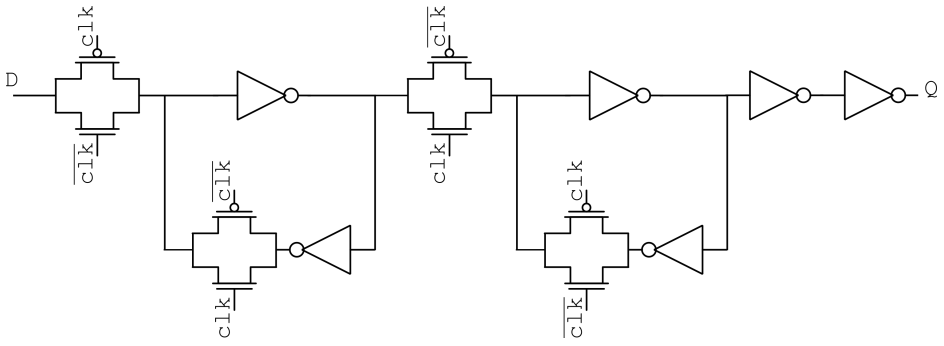


Figure 5.10: Circuit of a shift register used in scanner.

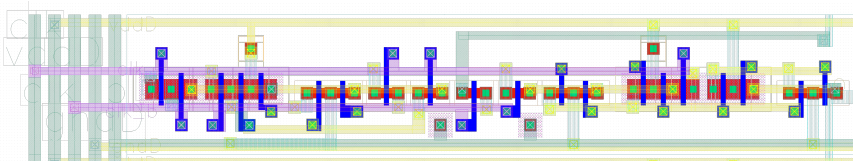


Figure 5.11: Layout of a shift register used in scanner.

During the readout operation, a single pixel is selected by `ROW_SELECT` and `COL_SELECT` signals. As the pixel selection reaches the end of each row, the `COL_SELECT` signal needs to be looped through to the start of a subsequent row. To avoid sending a column pulse signal after the end of each row, a simple column loop control circuit is designed as shown in Figure 5.12. The `COL_SELECT` is a pulse sent at the start of a frame readout operation. The `FR_ACTIVE` signal indicates the duration when readout is active throughout the entire array to enable the last pixel selection of each row `SR_OUT<LAST>` to loop through the process. The output of the circuit is connected to the first column scanner.

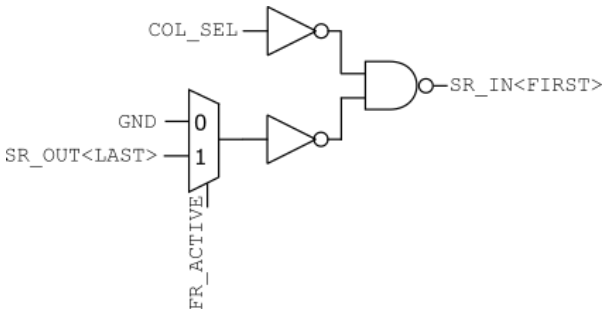


Figure 5.12: Column loop control.

5.3.2 Vref generator circuits

Previously a current sink based $V_{ref}(t)$ generator was presented in section 5.2.3. When implementing the $V_{ref}(t)$ generator on a 2D array, the timing requirement for the switches activating each segment of current sink needs to be considered. In particular, during the readout operation, the time delay between each row is one row clock cycle (256 μs). However the duration required for some $V_{ref}(t)$ segments are less than one

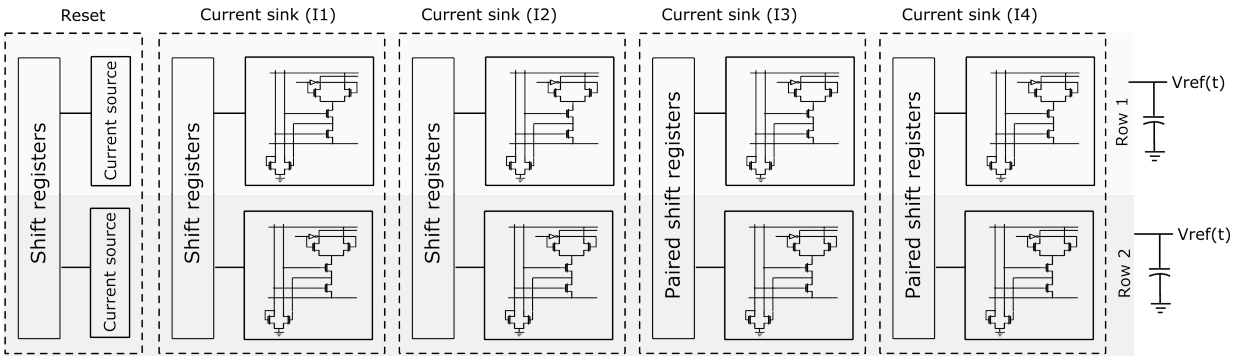


Figure 5.13: Block diagram of four segmented $V_{ref}(t)$ generator for two rows. The architecture consists of three main blocks; reset block, current sink with single shift registers block and current sink with paired shift register block.

row clock cycle as recorded in Table 5.3. Therefore the architecture needs to address the timing constraints.

Figure 5.13 shows a proposed architecture of the $V_{ref}(t)$ generator for $V_{ref}(t)$ with four segments aimed for two rows. The architecture can be grouped into three main blocks; a reset block, current sink with single shift register block and current sink with paired shift register block. The output of each $V_{ref}(t)$ generator is connected to a row capacitance and a pixel row. The current source in the reset block consists of a *pMOS* transistor for the initial pixel reset operation. The paired shift register architectures are implemented for $V_{ref}(t)$ segments whose duration are less than the duration of the row clock cycle used. In the case of the architecture in the figure, current sink blocks of three (I3) and four (I4) use paired shift registers.

Figure 5.14 shows the timing diagram of the $V_{ref}(t)$ generator operation. An example of operation for four segmented $V_{ref}(t)$ generator for two rows of pixel is used in the diagram. The different discharge rate and duration required by each segment of $V_{ref}(t)$ are controlled by digital signals `SW`. These signals activate each current sink block of the $V_{ref}(t)$ generator. In the 2D array, the signals are cascaded down through each shift register. The most important aspect of the timing control is to sequence the operation of reset, integration and read out at each row accordingly. In particular, `SW` signals to the subsequent row have to be exactly after one `CLK_ROW`

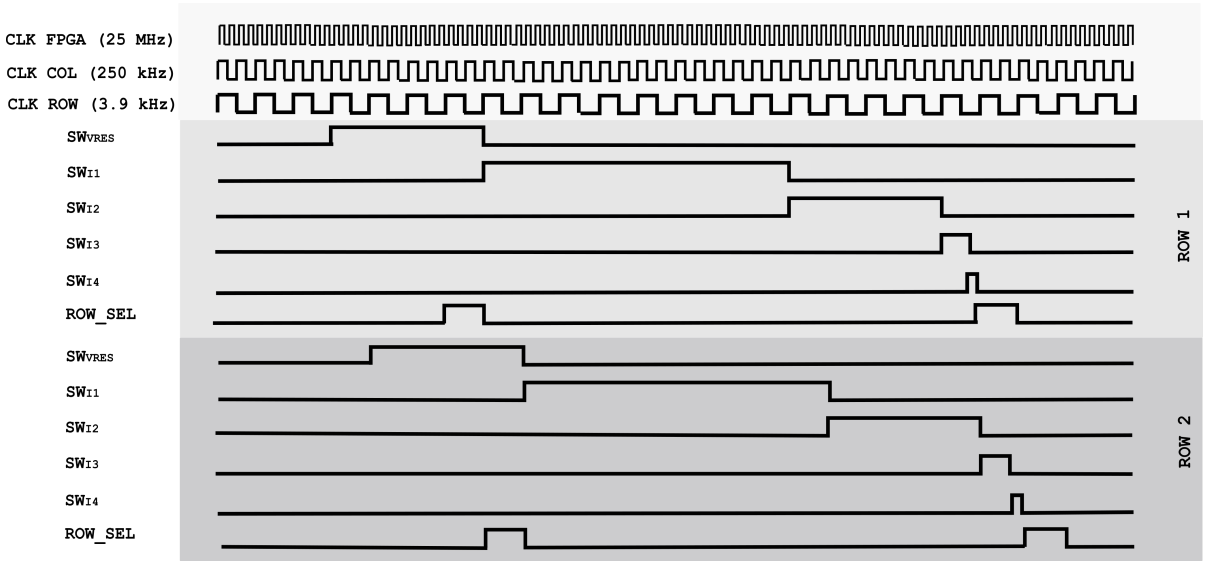


Figure 5.14: Timing diagram of $V_{ref}(t)$ generator showing switching signals for each segment. The signals are cascaded to the subsequent row.

cycle. This requirement can be achieved using the shift registers for $V_{ref}(t)$ segments that have a duration longer than one CLK_ROW cycle.

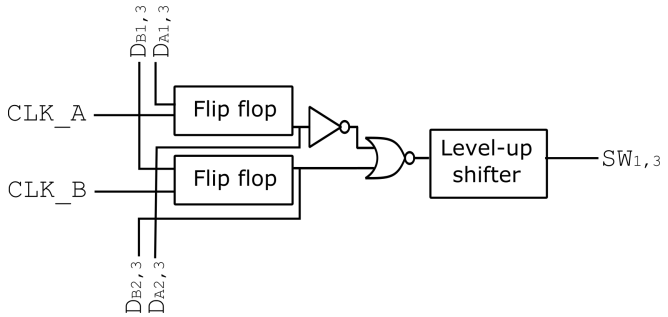


Figure 5.15: Paired shift registers for switch signal generation that has duration less than one row clock cycle.

However, for $V_{ref}(t)$ segments that have durations less than CLK_ROW cycle, paired shift register blocks are implemented to generate pulses shorter than CLK_ROW cycle. Figure 5.15 shows the digital circuits of the paired shift registers in one row. Two clock signals CLK_A and CLK_B of the same frequency as CLK_ROW are fed to the flip-flops respectively. Both of the clock signals are referenced to CLK_FPGA. The difference is, CLK_B is delayed relative to CLK_A. The duration of the delay corresponds to the duration of the $V_{ref}(t)$ segments. The timing diagram of the operation is shown in

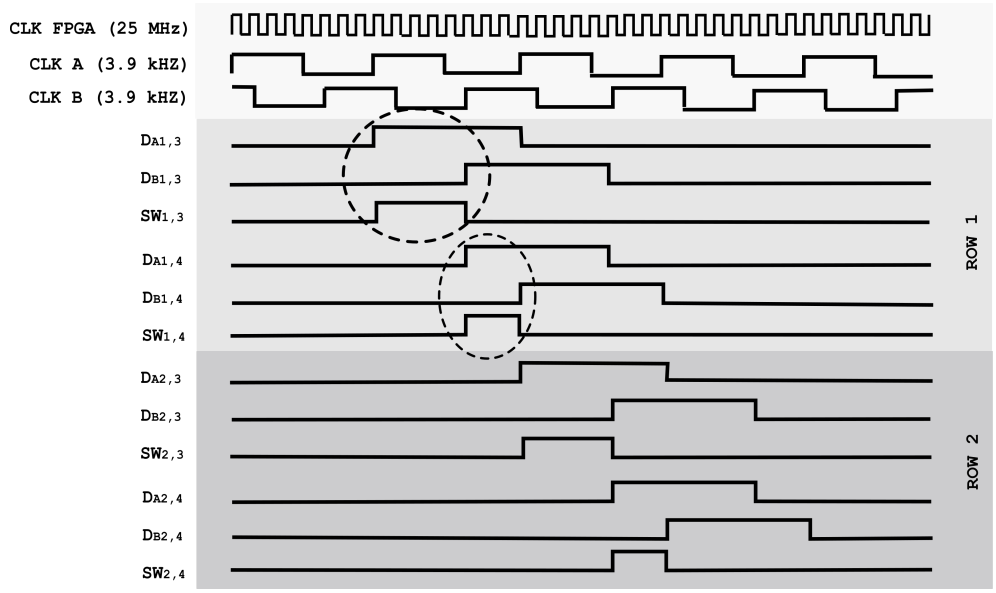


Figure 5.16: Timing diagram of $V_{ref}(t)$ generator showing switching signals of the paired shift registers for segments that have duration less than one row clock cycle.

Figure 5.16. The SW signals are generated with the start and end at the positive edges of the two clocks (circled in Figure 5.16). This way pulses shorter than CLK_ROW can be generated while still maintaining one CLK_ROW cycle delay to the subsequent row. One implication of using this approach is that the duration of each segment of $V_{ref}(t)$ signal needs to be adjusted according to the timing resolution of CLK_ROW and CLK_FPGA.

The $V_{ref}(t)$ generator presented was for an example of four segmented $V_{ref}(t)$. In the final 2D imager implementation, an eight segmented $V_{ref}(t)$ generator has been designed to meet the specifications in Table 5.3.

5.3.3 Read out circuits

The values of all pixels are obtained through the column and the array readout stages. The schematic of the readout stage is shown in Figure 5.17. The column readout stage consists of a column current source M_{CCs}, a transmission gate TX, a storage capacitor C_S, a source follower M_{CSf} and a column select M_{CRs}. All the output columns are

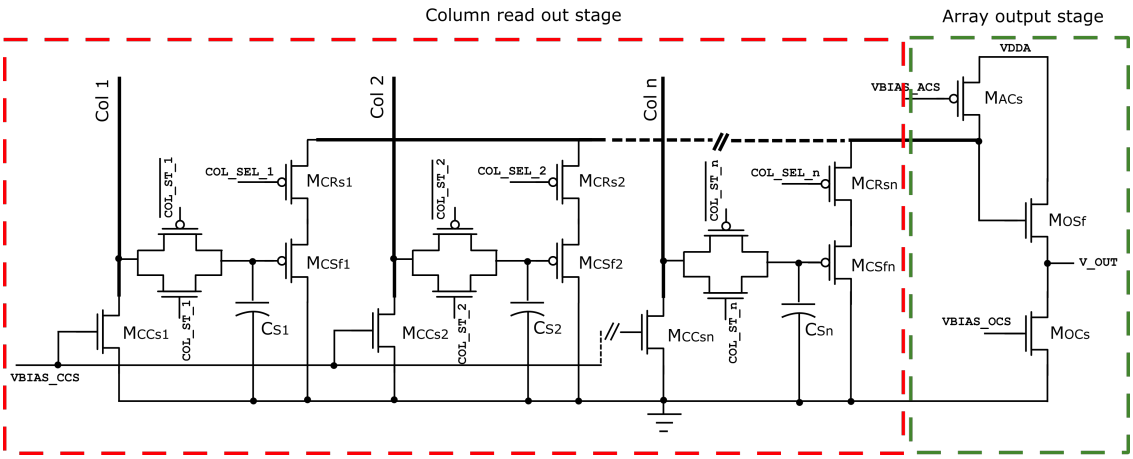


Figure 5.17: Read out circuits consist of column and array stages with one analogue output channel.

Component	Function	Dimension/Value
M_{CCs}	Column current source	5/10 μm/μm
TX	Transmission gates	0.36/0.34 (nMOS), 0.72/0.34 (pMOS) μm/μm
C_S	Storage capacitor	550 fF
M_{CSf}	Column source follower	10/0.5 (μm/μm)
M_{CRs}	Column select	24/1 (μm/μm)
M_{OSf}	Array current source	50/5 (μm/μm)
M_{OCs}	Output source follower	40/1 (μm/μm)
M_{OCs}	Output current source	25/10 (μm/μm)

Table 5.4: Dimensions and value of the components used in the read out stage.

connected to a single array current source M_{ACs}. The value of each pixel is then read from a single analogue output channel through a source follower M_{OSf}. The dimensions of the transistors and capacitor used are shown in Table 5.4. To perform a true CDS, each pixel is sampled twice when `ROW_SEL` is active. The reset values of all pixels are sampled first then followed by the integrated values as shown previously in Figure 5.14. More specifically, in the array operation, the reset values of each pixel in the first row are sampled in the storage capacitor. Then each reset value is read individually in a period of one row clock cycle. This operation is then performed on the subsequent row in the next row clock cycle. During this time the pixels in the

first row are integrating concurrently. The process continues until it reaches the last row. While reading the reset values of the last row, the pixels in the first row are still integrating. The second sampling process of the integrated values of the first row starts right after the pixels in the integration period of the first row ends. The method is possible when the integration time (20 ms) is sufficiently long to cover the duration of sampling and reading the reset values of all pixels. The total readout time of the array is given as:

$$Readout_{total} = (T_{int}) + (\texttt{CLK\_ROW}_{period} \times Number_{row}) \tag{5.5}$$

For an array of 64 x 64 pixels with an integration time of 20 ms and `CLK_ROW` period of 256 μs, the total readout time is 36.4 ms. A more ideal way to perform CDS is by having two column based storage capacitors measuring each pixel's reset and integrated values respectively. In addition, a column differential amplifier is required to perform the subtraction. However, the CDS strategy that is aimed at the chip is to perform the subtraction externally. The strategy avoids the need of second storage capacitor and the differential amplifier. Furthermore, this simplifies the readout circuit and reduces any additional risk for the prototyped chip.

5.3.4 Chip layout

A prototyped imager consists of the proposed $V_{ref}(t)$ generator with MIM capacitors and a 64 x 64 pixel array was fabricated in UMC mini-ASIC 180 nm, 1P6M, 1.8V/3.3V CMOS process. The total size of the chip is 1525 μm x 1525 μm as shown in the chip layout in Figure 5.18. In addition to the 2D pixel array, a single row of $V_{ref}(t)$ generator connected to a row of 64 pixels is also implemented for characterising the generator and the pixels. The analogue and digital I/O pads used were from Faraday Technology, UMC's third-party library provider. Within the available silicon area,

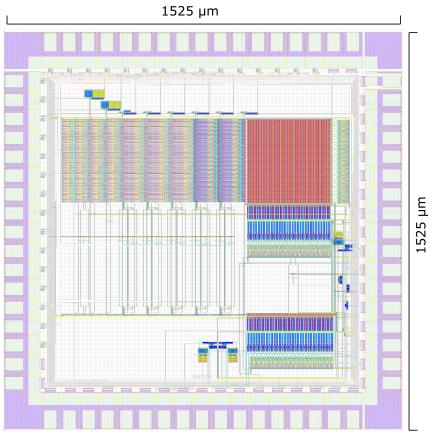


Figure 5.18: Chip layout of the prototyped imager using UMC 180 μm CMOS process.

the majority of the space is occupied by the $V_{ref}(t)$ generator with a dimension of 700 μm x 320 μm. The horizontal space acquired by the $V_{ref}(t)$ generator allows the pixel array of up to 64 x 64 pixels. Therefore the $V_{ref}(t)$ generator is as wide as 64 pixels, where 64 is small compared to a typical pixel array. The same 5T pixel layout presented earlier in Figure 3.1 was used to form the pixel array. In addition to $V_{ref}(t)$ generator, the peripheral circuits for the imager include pixel scanners and imager readout circuits. The topology and dimension of these circuits are shown in Figure 5.19.

5.4 Impact of pixel variations to $V_{ref}(t)$ parameters

The design of a 2D imager has been presented. Responses from each pixel in the imager are expected to vary which causes FPN. The study so far has only focused on the response from a single test pixel. In addition, it has been demonstrated in Equation 2.14 that $V_{ref}(t)$ is dependent on V_{th} which is the major source of FPN. This FPN contribution needs to be considered when determining $V_{ref}(t)$ parameters. To study the impact of the generated $V_{ref}(t)$ towards FPN, responses of 1000 pixels can be performed using Monte Carlo analysis. A proper selection of $V_{ref}(t)$ parameter values required for the $V_{ref}(t)$ generator such as V_{reset} and the slope value are expected

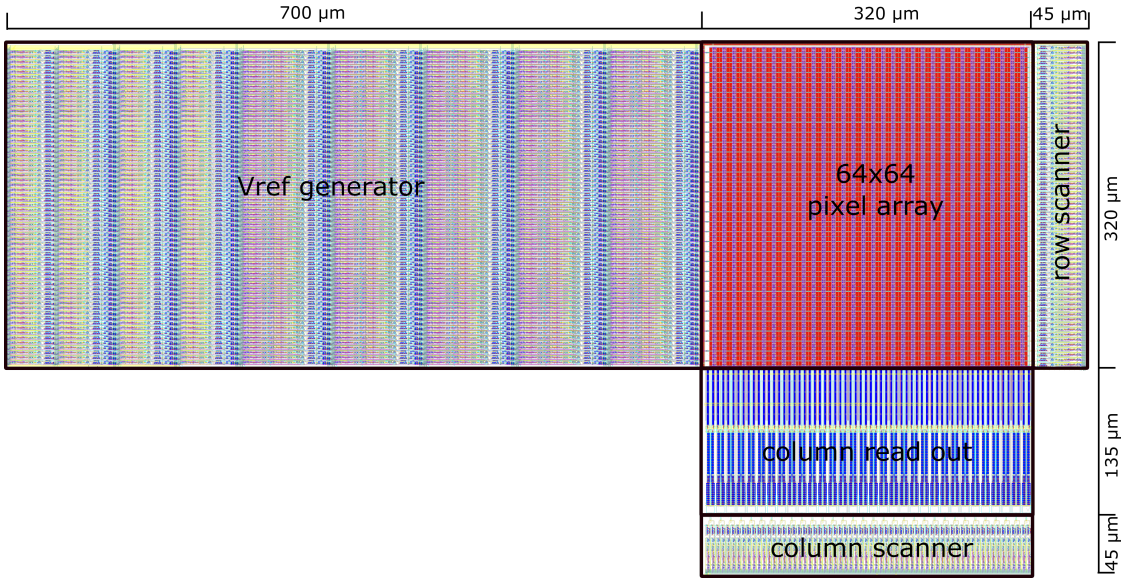
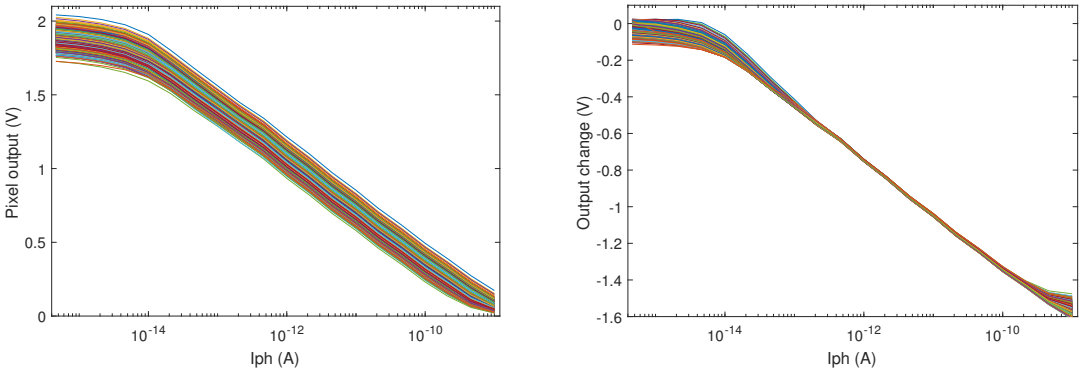


Figure 5.19: Layout of the 2D imager consists of 8 segmented $V_{ref}(t)$ generator, 64 x 64 pixels, row scanners, column scanners and column readout.

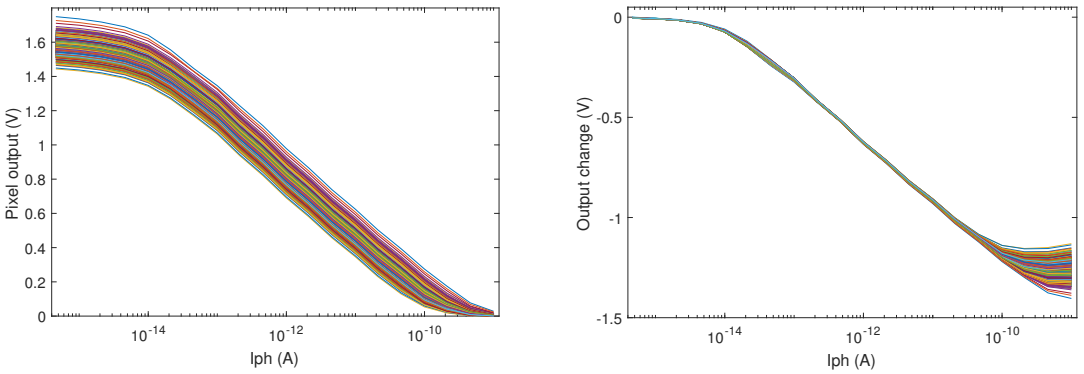
to minimise the impact of FPN after performing CDS. In this study, pixel responses of three $V_{ref}(t)$ signals of different V_{reset} and slope values are simulated.

Pixel responses of the first $V_{ref}(t)$ for before and after CDS are depicted in Figure 5.20a and Figure 5.20b respectively. As shown in Figure 5.20a, the pixel responses in particular at the low photocurrent of 0.5 fA, have outputs which vary by approximately 300 mV. In addition, at high photocurrent, some of the responses are observed to have saturated. The pixel response after CDS shown in Figure 5.20b demonstrates that the CDS method is not effective to minimise the response variation in particular at low and high photocurrent. The effectiveness of CDS means the major contribution of the offset FPN originated from V_{th} is removed. This is possible when V_{th} value is properly preserved during reset and readout operation. However, further investigation showed that at low photocurrent, the voltage at the floating diffusion node, V_{FD} overshoots during reset due to the effect of parasitic capacitances. In particular, the FD node is connected to the gate of the reset transistor through an overlap capacitor. When $V_{ref}(t)$ changes from low to high at reset (V_{reset} set to 3.3 V) after the previous cycle, V_{FD} departs from the expected value of V_{reset}-V_{th}. The effect is more evident



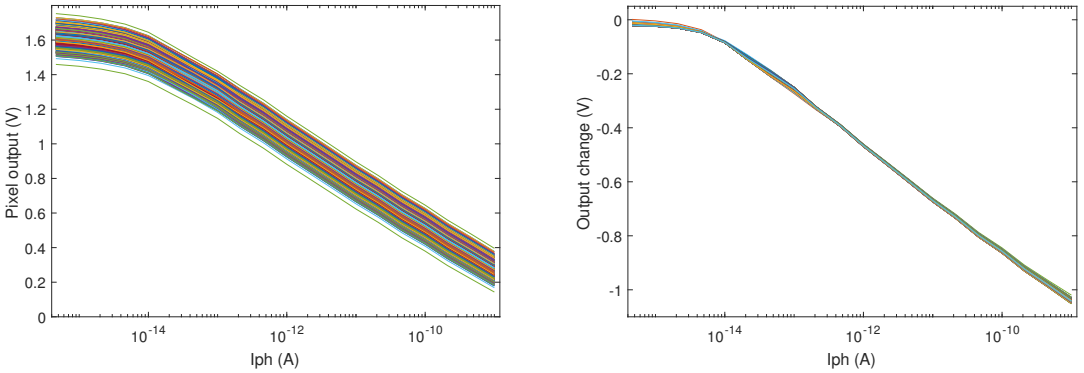
(a) Pixel output (b) Output change after CDS

Figure 5.20: Simulated response of 1000 pixels for V_{reset} = 3.3 V and slope = -350 mV/dec.



(a) Pixel output (b) Output change after CDS

Figure 5.21: Simulated response of 1000 pixels for V_{reset} = 3.0 V and slope = -350 mV/dec.



(a) Pixel output (b) Output change after CDS

Figure 5.22: Simulated response of 1000 pixels for V_{reset} = 3.0 V and slope = -250 mV/dec.

at low photocurrent primarily, due to the fact that it takes a longer time for the photocurrent to discharge the pixel. This means that the pixel response is not fully settled within the duration of the reset period. On the other hand, at high photocurrent, the high residual FPN is observed due to the responses that have saturated. When a response saturates, the V_{th} value which is the major source of offset FPN is no longer preserved. Therefore the CDS method is not effective.

In order to reduce the effect of overshoots during the reset transition, V_{reset} is set to 3 V. When V_{reset} is reduced, the potential difference of V_{FD} before and after reset is decreased. However, one adverse effect of this approach is the pixel output swing is now reduced. The impact of this change can be seen from Figure 5.21b. In particular, at low photocurrent, the residual FPN is now decreased marked by the reduced thickness of the response variations. However, the FPN at high photocurrent becomes worse on account of more pixel responses have saturated when the slope is unchanged. This is expected and can be observed by the increased thickness of the pixel response after CDS.

To avoid saturation at high photocurrent, the slope value is reduced to -250 mV/dec to provide enough output swing covering the photocurrent range without any saturated pixel response. V_{reset} is maintained at 3 V. The pixel responses in Figure 5.22a shows that no single response is saturated at high illumination. This is confirmed in Figure 5.22b which shows that the responses after CDS with minimum FPN residuals at less than 10 mV. However, as a result of reducing the slope, the output swing of the response is about 1 V.

In conclusion, $V_{ref}(t)$ is dependent on V_{th} which is known to be a source of FPN that can be minimised by CDS. However, the simulated results show that FPN can be effectively minimised when $V_{ref}(t)$ parameters are carefully selected. The $V_{ref}(t)$ generator that has been proposed is adaptable. In particular, the PWL segments of $V_{ref}(t)$ can be controlled to account for the needs of different value of $V_{ref}(t)$

parameters such as V_{reset} and slope value.

5.5 Summary

The chapter first reviewed different methods to generate $V_{ref}(t)$. $V_{ref}(t)$ models that have been considered are based on multiple stepped reset $V_{ref}(t)$ and integrating logarithmic $V_{ref}(t)$. However, the requirements to generate $V_{ref}(t)$ based on the models are either impractical for area requirement or inefficient in term of power consumption. Therefore, a new $V_{ref}(t)$ model has been proposed which is based on piece-wise linear (PWL) $V_{ref}(t)$. The PWL based $V_{ref}(t)$ has demonstrated a pixel response up to 120 dB comparable to the other two models. In addition, the most critical aspect of $V_{ref}(t)$ which is the rapid discharge rate at the last segment is relaxed at least by half to 0.6 V/μs. This reduces the complexity and the current requirement when generating $V_{ref}(t)$ in particular for a large pixel array.

Using the PWL $V_{ref}(t)$ model, a $V_{ref}(t)$ generator based on multiple current sinks is proposed. The design of the $V_{ref}(t)$ generator for a rolling shutter system means the $V_{ref}(t)$ generator needs to be implemented at every row and meets the constraint of the pixel pitch. More importantly, the $V_{ref}(t)$ generator design needs to be adaptive in order to account for pixel variations when performing FPN correction. In particular, for the first prototyped imager, the ability to change the value of V_{reset} and the slope value of $V_{ref}(t)$ parameters have been shown to impact FPN correction.

A 2D imager has been fabricated on 180 nm mini-ASIC process. The imager system consists of a 64 x 64 pixel array, $V_{ref}(t)$ generator and imager peripheral circuits such as scanners and read out. In addition, a single row of $V_{ref}(t)$ generator and 1 x 64 pixels are implemented for characterisation purposes. A study focussing on the impact of the pixel variations on the $V_{ref}(t)$ parameters has been presented. However, the analysis is limited to the accuracy of the simulation models. In particular, the

simulation performed in Cadence lacks in accurate models to simulate a pixel such as dark current, photodiode conversion gain and photodiode capacitance. Therefore, further work is required to test the chip and confirm the response of the imager.

Chapter 6

Conclusions and future work

The ability to faithfully capture a wide range of light intensities is an important figure of merit for CMOS image sensors. For example, some critical applications such as automotive imaging demands a dynamic range of up to 120 dB without any loss of details [14, 84]. Standard CMOS image sensors have a dynamic range between 40 to 60 dB [4]. Previously, several methods have been proposed in order to extend the dynamic range of CMOS imagers. The methods include multiple exposures [18, 19], logarithmic response [5], a combination of linear and logarithmic (lin-log) responses [85], schemes relying upon threshold comparisons [86, 87] and well capacity adjustment [55, 54]. However, there are drawbacks associated with each method. For example, multiple exposure schemes require post-processing to merge and compress images. In addition, synthesising multiple images with various integration time causes signal drops with respect to noise. Both the logarithmic and lin-log responses suffer from high spatial noise. In particular, the lin-log response suffers from high error at the transition of linear and logarithmic response [49]. The threshold comparing schemes require an in pixel comparator which means that photosensitive area is reduced to accommodate more transistors. Finally, the well capacity adjusting schemes achieve wide dynamic range at the expense of significant drops of sensitivity

on the photoresponse [24]. Each method proposed previously achieves wide dynamic range at the cost of either higher noise, reduced photosensitive area or additional post-processing.

The work described in this dissertation has presented an improved model of continuous time-varying reference voltage $V_{ref}(t)$ to extend the dynamic range of a pixel. This is achieved when $V_{ref}(t)$ is used to control the effective integration time. The effective integration time is the period when the pixel integrates linearly. When a short effective integration time is allocated to a light incident with high intensity, saturation can be avoided and hence the dynamic range is extended. To control the effective integration time, the improved $V_{ref}(t)$ model is a logarithmic function with an increasing rate (dV/dt) that controls the discharge rate of the pixel. The discharge rate of the pixel, therefore, can be restrained for a high light intensity to a time t controlled by $V_{ref}(t)$. From this time t, the pixel is discharged linearly until the end of the integration time. The effective integration time is therefore reduced for high light intensity to avoid saturation.

One main advantage of the logarithmic response is the wide dynamic range can be compressed, hence reducing the complexities of readout circuitries. In addition, the proposed $V_{ref}(t)$ model has demonstrated slope controllability. The slope of the standard logarithmic pixel is dictated by process parameters with a slope at approximately 60 mV/decade. However the $V_{ref}(t)$ model allows users to control the degree in which the effective integration time is compressed according to the intensity of light. This degree defines the slope of the photoresponse.

$V_{ref}(t)$ model has been simulated on a 5T pixel. It has been demonstrated that in order to control the slope of the response, the $V_{ref}(t)$ model needs to account for non-ideal second-order effects of the pixel. These include the source follower gain, the subthreshold slope and the body effect. When these parameters are extracted and included in the model, the slope accuracy has been improved from 10% to 0.5%

of slope error. In addition, response with different slopes of 300, 350, 400 and 600 mV/decades have been simulated with an error of less than 2%. The results show a high degree of control of the slope response. More importantly, a dynamic range of more than six decades has been achieved.

To verify pixel response of the proposed $V_{ref}(t)$ model, 5T test pixels have been laid out and fabricated in 180 nm process. The pixel has a pitch of 5 μm with a fill factor of 34%. Experiments performed on the test pixel have been conducted in a controlled dark chamber. During the experiments, $V_{ref}(t)$ was generated externally using an arbitrary waveform generator. In addition, the light source that was used during the experiments, has a maximum light intensity that is restricted to four decades of dynamic range. The limited light intensity means the slope of the response can be increased in order to optimise the pixel output swing.

The pixel was first characterised to measure parameters that are required in $V_{ref}(t)$ model. The measured values of the parameters were used to generate $V_{ref}(t)$ with a slope of 600 mV/decade. The slope of the $V_{ref}(t)$ response has been measured at 602 mV/decade. The slope error which equals to less than 0.5% means, the response can be well controlled using the $V_{ref}(t)$ model. Furthermore, the dynamic range for the $V_{ref}(t)$ has been extended up to 80 dB. The limited illumination of the light source used during experiment means, the potential of the proposed method ideally up to 120 dB could not be fully demonstrated.

The effect of process variation has been measured between four different chips. The pixel responses exhibit gain and offset FPN as expected. In the case of offset FPN, it has been reduced significantly using CDS. For the gain FPN, the measured responses have been fitted using the mean value of four linear-logarithmic fitted models as a universal response curve. However when measuring the illumination error, the method has failed to obtain less than 10% error. As a result, each response has been fitted individually. In addition, a weighted average method has been used in order to reduce

the error at the transition point between the linear-logarithmic response. Using these strategies, the illumination error for all the four responses have been reduced to less than 2%.

A study investigating the performance of different approaches to extending dynamic range has been conducted. The need arises due to the fact that current comparative studies have only been performed in simulations. The study presented in Chapter 4, therefore, will be the first experimental study of different WDR approaches on a single pixel. The architecture of 5T pixel allows different modes of WDR to be performed by controlling the gate voltage of the reset transistor. The modes include logarithmic, linear-logarithmic, integrating logarithmic and multiple stepped reset. In addition, an approach to control the response of a multiple stepped reset mode based on integrating logarithmic $V_{ref}(t)$ has been proposed. For each approach, the photoresponse, sensitivity and illumination error have been analysed. Furthermore, the advantages and disadvantages of each approach based on the performance and the circuitry requirements have been reviewed. A dynamic range of 80 dB has been demonstrated by all the WDR modes. In addition, the results have demonstrated that integrating logarithmic and multiple stepped resets are both promising approaches. In particular, the two modes recorded illumination error of less than 2% at mid and high light intensity.

A further study has been conducted on a multiple stepped reset approach investigating the number of steps required when the dynamic range is extended from 80 dB to 120 dB. Responses with integration time of 20 ms, 200 ms and 2 s that achieved a similar effect when increasing the light intensity were performed. The results have demonstrated that eight steps are required for the multiple stepped reset approach in order to achieve the same quality as three steps when extending the dynamic range to 120 dB. In summary, the chapter has presented measured responses of different WDR approaches on a single pixel. These results serve as a basis for WDR mode

selection for CMOS imaging array implementation.

The results from the comparative study have concluded that both the integrating logarithmic and multiple stepped reset approaches can achieve high-quality images. Furthermore, in order to implement an imaging array, a circuit to generate $V_{ref}(t)$ that can perform either of the WDR approaches needs to be considered. Therefore a study to explore possible implementations of $V_{ref}(t)$ generator has been performed. Both WDR approaches have challenges in meeting either the pixel pitch or low power requirement. A PWL based $V_{ref}(t)$ has been proposed that can achieve a comparable response to those of the integrating logarithmic and the multiple stepped reset. In addition, the main advantage of this approach is the PWL based $V_{ref}(t)$ can be generated from a simple current sink array with controlled timing signals. A 64 x 64 2D CMOS image sensor was fabricated in 180 nm, 3.3V, 1P6M, mini-ASIC process. The size of the imager is 1.525 mm x 1.525 mm. In addition to the pixel array, an eight segment PWL $V_{ref}(t)$ generator occupying 700 μm x 5 μm for a single row has been laid out. Furthermore, readout circuits for the imager with a single output channel have been designed. A study simulating the performance of the imager has been conducted to explore the effect of $V_{ref}(t)$ parameter value selections such as V_{reset} and the slope towards the effect of pixel variations. The results have demonstrated that the values of V_{reset} and the slope have been reduced to 3 V and 250 mV/decade respectively in order to effectively remove the offset FPN component when performing CDS. The residual offset FPN has been reduced from 300 mV to 10 mV. The promising result from the simulated responses means that ensuing works on measuring the chip imager need to be conducted in the future.

6.1 Future work

The imaging array described in Chapter 5 has been fabricated. A series of measurements need to be conducted. For this purpose, an experimental setup similar to the one described in Section 3.3 will be used. In addition, a test board that has current varying capability has been assembled. More specifically, a row of trimming potentiometers are used to control the value of each current bias. Furthermore, for a very low current requirement, an accurate source meter Keithley 2636B will be used. The switching of the $V_{ref}(t)$ generator and timing signals controlling the row and column scanners need to be generated. To do this, Zynq 7000 FPGA board will be used. Once the signals have been generated, a list of experiments that need to be performed are as follows:

1. **Pixel response measurements**

   The first experiment that should be conducted is to measure parameter values required in $V_{ref}(t)$ equation. In particular, measurements for source follower gain, subthreshold slope and body effect parameters need to be performed. After these parameters have been determined, an optimum value of slope should be set on $V_{ref}(t)$ equation, aiming at more than 80 dB of dynamic range. When all the values of $V_{ref}(t)$ have been set, two PWL based $V_{ref}(t)$ signals can be generated. The first $V_{ref}(t)$ should be generated externally using an arbitrary wave generator (WW5064) and the second one should be generated internally using the $V_{ref}(t)$ generator. When generating internally, bias current to each current sink element in the $V_{ref}(t)$ generator can be tuned individually using trimming potentiometers. The manual tuning should be performed to compensate for the expected variants of the potentiometer values and mismatch of the transistors in the $V_{ref}(t)$ generator from the ideal values. Once the two $V_{ref}(t)$ signals are matched, pixel response from each $V_{ref}(t)$ can be measured and com-

pared. The previous measurements should be repeated with a single row of 64 pixels. The aim is to get the average values of the parameters to produce a universal $V_{ref}(t)$ model. Using the universal $V_{ref}(t)$ model, $V_{ref}(t)$ signal can be generated per row feeding into the 64 x 64 pixel array. The response of each pixel can be measured and the expected variations will need to be corrected.

2. **FPN Correction**

   The variations of the pixel responses can be corrected using the previous method described in Section 3.6. In a case where a distinct divergence of pixel responses from the mean value exists for example due to saturation, the user-defined $V_{ref}(t)$ parameters such as V_{reset} and *slope* need to be adjusted in order to reduce the illumination error as explained in Section 5.4. Furthermore, all responses will be modelled individually and the parameters need to be recorded in order to perform FPN correction. The illumination errors for all the responses are expected to be less than 2%. If this is achieved, the same measurements can be conducted on other chip imagers to study the effect of FPN across different chips. The universal $V_{ref}(t)$ model will be used when measuring other chips. Therefore pixel responses from other chips are expected to be similar to the first chip. However, if this is not the case due to high process variations, pixel characterisation need to be repeated on each chip. Therefore a unique $V_{ref}(t)$ model is needed for each chip imager.

6.1.1 Gamma correction

The focus of the study in this dissertation has been on acquiring wide dynamic range images. A subsequent challenge after acquiring the image is to display the image on a monitor. The method of dynamic range extension described in Chapter 2 achieves two objectives. First is capturing a wide range of illuminance and second is compressing the acquired information in a logarithmic term. However, the response demonstrated

a lower gain at the low light region in contrast to the mid and high region. This can result in low contrast value and loss of details. Generally, an image processing technique referred to as tone mapping is applied to wide dynamic range images to display on standard monitors. Standard monitors typically have a limited dynamic range of 8 bits. Gamma correction is a form of tone mapping technique that is widely used to improve the quality of images [88]. It controls the overall brightness of captured images by applying a non-linear mapping of light intensity from input to output. In particular, when the images are displayed on monitors, gamma correction is applied to compensate for the non-linear response of the monitors [89]. The non-linear luminance of the monitors can be expressed as:

$$f(x) = x^{\gamma} \tag{6.1}$$

where x is the normalised input voltage such that $x \in [0, 1]$ and γ is a gamma coefficient. The value of gamma is determined experimentally and the most commonly used value is 2.2 [90]. To compensate for the non-linear response of the monitors, the ideal gamma correction can be expressed as:

$$f^{-1}(x) = x^{\frac{1}{\gamma}} \tag{6.2}$$

The outputs of the functions in Equations 6.1 and 6.2 are depicted in Figure 6.1. The figure demonstrates the effect of the gamma correction function (in Red), when it is applied in order to compensate for the non-linear response of monitors (in Green). The result for a linear line (in Blue) is an increased contrast value in particular at the low light regions.

The effect of gamma correction can be assessed perceptually from Figure 6.2. The gamma correction has been performed on a grayscale image in Matlab. The difference between the two images before and after applying the function is clearly visible at the

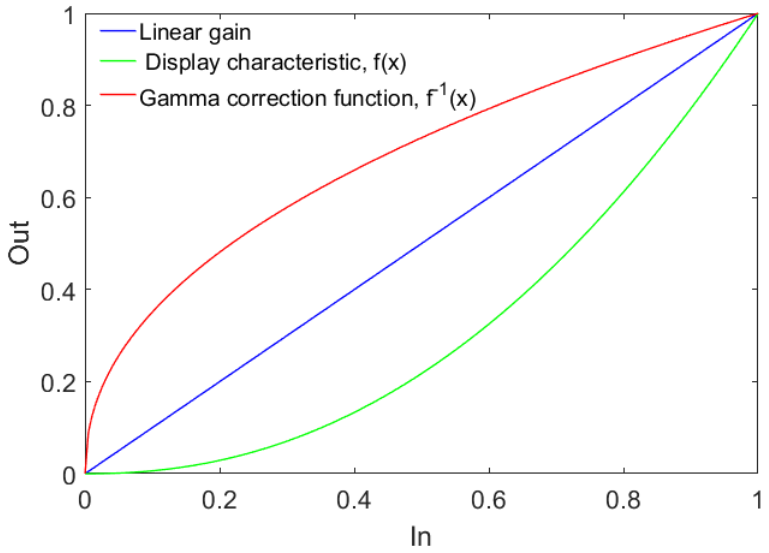


Figure 6.1: Gamma and inverse gamma correction function using $\gamma = 2.2$ and a linear gain.

vicinity of the gate in particular at the top. Figure 6.2b has a stark contrast value at low light highlighting the details of the image.

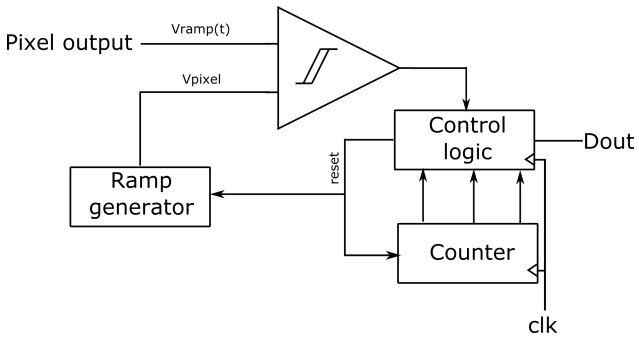
6.1.1.1 ADC architecture

Different methods performing gamma correction have been proposed in digital and analogue domains. In the former case, the methods include using a direct lookup table [91] or a dedicated FPGA [92, 93, 94]. The gamma correction is performed on a quantised image after conversion stage. The main advantage of this approach is its flexibility to choose arbitrary gamma values. However, the main disadvantage is the performance is limited by the ADC. In particular, the ADC quantisation error is amplified after performing gamma correction mainly at the low light region. One way to reduce the error is by using a higher resolution ADC. However, this comes at the expense of high memory resources, area and power consumption. In the latter case, few implementations in the analogue domain using ADC have been proposed. More specifically, gamma correction is performed using non-linear inputs to the ADC achieving data conversion at the same time. Methods to generate the non-linear input

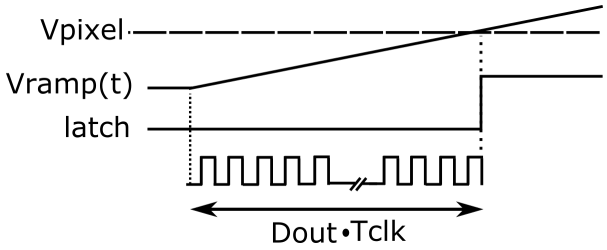
(a) Original grayscale image

(b) Gamma correction function applied to the image showing a bright adjustment at the original dark scene.

Figure 6.2: Gamma corrected image using $\gamma = 2.2$ to a grayscale image.



(a) A standard single slope linear ramp ADC.



(b) Timing diagram of a ramp ADC

Figure 6.3: A block diagram and a timing diagram for a standard single slope linear ramp ADC.

include using ramp generator [95], logarithmic counter [96] and voltage controlled oscillator [90]. The ADC architecture that has been proposed is a single-slope ramp ADC shown in Figure 6.3a. The ADC which mainly consists of a comparator means that it requires a relatively simple column circuit that can be fit in a narrow pixel pitch. Furthermore the low complexity column circuit guarantees uniformity between columns and can minimise the column FPN. However, the main potential source of the column FPN is from the comparator's offset which can be reduced by auto-zeroing method. The operation of the ADC depicted in Figure 6.3b begins with a reset period before the counter starts counting. When the pixel output value matches with the value of the ramp voltage, the comparator latches a signal signalling the end of the counting process. The final count determines the value of the pixel.

To perform gamma correction, a reference voltage $V_{ref}(t)$ of the gamma function needs to be generated as an input to the comparator. One way to achieve this is by first interpolating the $V_{ref}(t)$ using piecewise linear. Jeong and co-workers

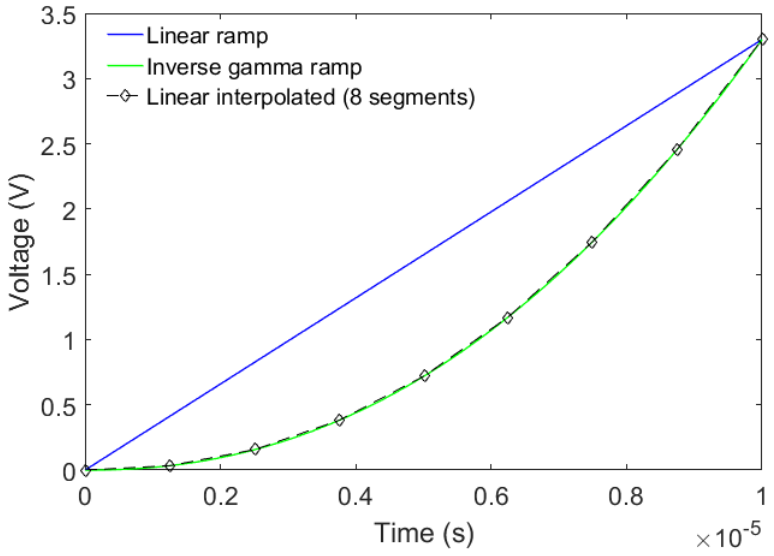


Figure 6.4: Non-linear ramp signal to the comparator aimed for gamma corrected ramp ADC. The signal is linear interpolated to eight segments.

have demonstrated this method successfully using an FPGA [92]. Using a similar approach, Kim and co-workers have achieved better image quality when modelling the gamma function using 8 sections as opposed to 4 sections [96]. The main advantage of approximating the $V_{ref}(t)$ is, the circuit architecture proposed in Section 5.2 can be employed with a few adjustments. An example of a $V_{ref}(t)$ required for the ADC is shown in Figure 6.4 where the $V_{ref}(t)$ is divided into 8 segments with a total time of 10 μs. By integrating the gamma correction in the ADC, a fully integrated image sensor can be obtained.

6.1.2 Increased frame-rate imager

In the previous imaging array design, the expected time required to read a single frame of the proposed imaging array during experiment is determined by the pixel integration time and the array read out time as in Equation 5.5. This leads to a total frame time of 36.4 ms or a readout time of 8.9 μs per pixel. The long frame time is due to two main reasons. First, the long integration time of 20 ms is important

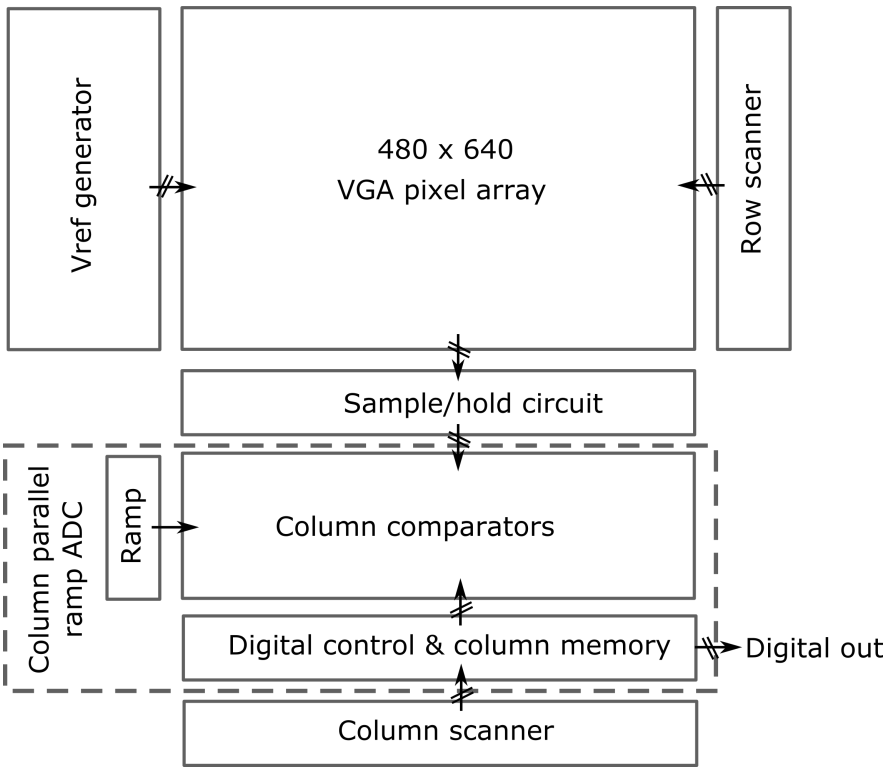


Figure 6.5: Block diagram of CMOS WDR image sensor architecture of a VGA array size with column parallel gamma correction ramp ADC.

in order to allow sufficient time for the pixel to integrate in low light condition that can be measured in a case of 10 bit ADC. Second, the measurement is limited by the speed of the external data converter used during experiment at a sampling rate of 250 kHz. This is the cost of not having an integrated ADC in the proposed imaging array which potentially can be the focus of the future study.

The opportunity to integrate the proposed ADC in the future work can increase the imaging array speed. In particular, a column parallel ADC architecture can be adopted as shown in Figure 6.5 where each column will have a ramp ADC that can perform gamma correction. A 10 bit ADC requires $2^{10} = 1024$ clock cycles to complete the data conversion. For an ADC with a clock rate of 100 MHz, the conversion time is equal to:

$$T_{ADC} = \frac{1}{100\ \text{MHz}} \times 1024 = 10.24\ \mu\text{s} \tag{6.3}$$

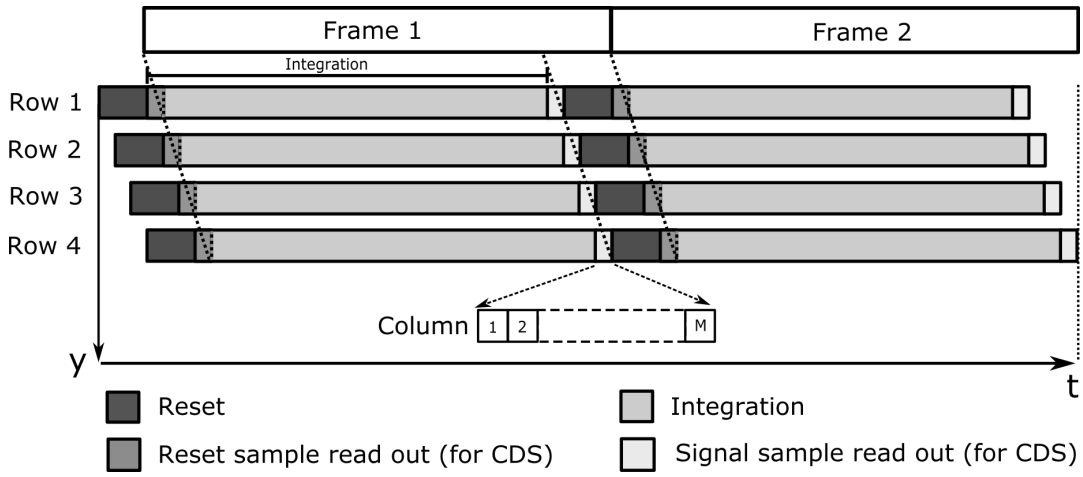


Figure 6.6: Timing diaram of a column parallel signal processing readout.

The imager readout is performed in a pipelined manner in which, each row may perform different pixel operations at the same time as shown in Figure 6.6. In order to perform CDS, two samples are read out; first at the start of the integration period and second at the end of the integration period. These two operations of the current row need to be independent from other rows in order to maintain continuous read out operation and to prevent data overwrite. Subsequently, all pixels in the row are read out for each column. Using the same clock rate aimed at a VGA size array, the read out time for a row is equivalent to 6.4 μs. Then, the total frame can be determined as:

$$\begin{aligned} T_{Frame} &= T_{int} + (T_{ADC} + T_{Row\_readout}) \times Number_{row} \\ &= 20 \text{ ms} + (10.24\,\mu\text{s} + 6.4\,\mu\text{s}) \times 480 \approx 28 \text{ ms} \end{aligned} \tag{6.4}$$

The frame time above results in a readout time of 92 ns per pixel and frame rate of 35 fps which is slightly higher than the standard video rate of 30 fps. In future applications where higher frame rate is critical, a study can be focused on the impact of a shorter integration time which is currently the major component of the frame time. The current integration time of 20 ms has achieved 80 dB and potentially up to

120 dB of the dynamic range. However, reducing the integration time can affect the pixel sensitivity at low light condition. In particular, if the integration time is reduced by half, the dynamic range at the low light region will be reduced by approximately 6 dB when having the same ADC resolution. To compensate for this effect, the impact of having higher ADC resolution and higher gamma value in the proposed ADC to improve the imager's performance needs to be studied.

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