

Design of an on-chip integrated 230 GHz dual-polarization balanced SIS receiver for multi-pixel array applications

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ABSTRACT

We report the design of a 230 GHz dual-polarization (2-pol) balanced Superconductor-Insulator-Superconductor (SIS) receiver that can be easily extended for large array applications. We achieve this by integrating all of the required radio frequency (RF) and local oscillator (LO) components on-chip using planar superconducting circuit technology, therefore simplifying the architecture of the receiver block substantially. One major feature of our design is the planar LO injection scheme, which couples the LO with a single on-chip antenna and distributes the LO power via a series of microstrip couplers to the balanced mixers of each polarization of each pixel. In this paper, we describe in detail the design and layout of the individual planar circuit components of our receiver, as well as how they are integrated to form a full receiver. We then conclude the paper with the design of a 2-pixel array demonstrator, illustrating how the balanced SIS mixer and the LO distribution network can be extended to form an even larger array.

Keywords: Heterodyne Receiver, Superconductor-Insulator-Superconductor Mixer, Balanced Mixer, Dual-Polarization Receiver, Focal Plane Array, Polarimeter

1. INTRODUCTION

The advancement of our knowledge in the past few decades with regards to the Far Infrared (FIR) spectroscopic Universe in the 100 GHz to 1 THz range, including the direct imaging of the black holes,^{1,2} would not be possible without the SIS mixer technology. Most of these SIS receivers deployed at existing millimetre (mm) and sub-mm observatories are constructed from two separate singly-polarised receivers mounted together to form a single-pixel receiver. In such receiver, the two polarization states are traditionally split using a wire grid^{3,4} or a waveguide orthomode transducer (OMT)^{5,6} and fed into the two single-polarization receivers, to recover the polarization information and the full strength of the astronomical signal. Consequently, the design of the receivers is bulky and complicated, making it difficult to scale to large focal-plane arrays. Moreover, to further improve the receiver sensitivity by eliminating the LO noise via the balanced mode operation,⁷ two separate mixers embedded within a large waveguide network are required for each polarization, as well as a sophisticated LO injection scheme. This further adds to the complexity of the mechanical construction, even for a single-pixel receiver.

In this paper, we aim to substantially simplify the architecture of a mm-wave 2-pol balanced SIS receiver so that it can be easily extended to form a large array. We achieve this by replacing all of the mechanical waveguide structures of the receiver with planar circuit components, which can be fabricated on a single receiver chip. This allows us to relax the requirements and reduce the complexity of the receiver block design, with only pockets and holes milled to host the receiver chip and subsequent intermediate frequency (IF) and DC biasing components.⁸ This approach, however, requires careful integration of planar on-chip circuit components to minimise losses, which is now possible with modern electromagnetic software packages and powerful computing resources. In the following, we shall describe in detail the electromagnetic designs of each of these important components and how they can be integrated to form a full receiver chip.

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2. ARRAY RECEIVER CONCEPT

Before we discuss the designs of the individual circuit components, we first present an overview concept of our balanced 2-pol array receiver in this section. Fig. 1(a) shows an idealised schematic of a 16-pixel balanced 2-pol array, employing a single planar 4-probe antenna for coupling the LO power into the array. The same 4-probe antenna will also be deployed for each RF pixel, acting as the planar OMT to split the polarization states of the incoming signal. Each of these 4-probe antennas, including the LO antenna, will be connected directly to the output of a drilled feedhorn,^{9–11} removing the need for a rectangular-to-circular waveguide transition that is difficult to machine at high frequency. This, therefore, allows for the design of a very simple array block requiring only backshorts and drilled feedhorns, as shown in Fig. 1(b), repeated throughout the array.

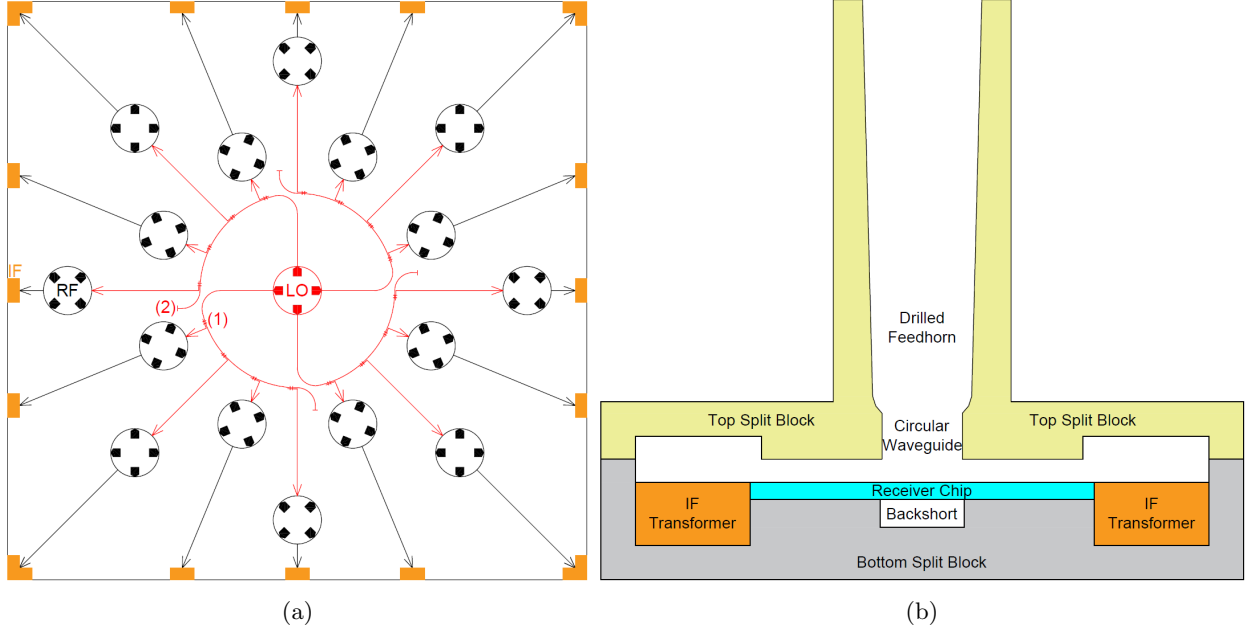


Figure 1: A 16-pixel 2-pol on-chip receiver concept. (a) Illustration of the full array receiver chip. The LO is coupled into the on-chip LO distribution network via a 4-probe antenna (red) and distributed to the individual RF pixels (black) with microstrip couplers (1) before it is terminated (2). The down-converted IF signals from both polarizations are guided to the IF transformer at the IF bonding pads near the edge of the receiver chip (orange). (b) Cross-section drawing of the 2-part split-block.

The array chip is configured to be symmetric for each quadrant, with the LO antenna at the centre and the RF pixels extended radially outward. Each of the LO antenna probes couples a quarter of the incident LO power to each quadrant. In this example, we have four RF pixels in each quadrant, hence the LO power from each LO probe is further distributed to these four pixels via a series of microstrip couplers, coupling a small portion of the LO power to ‘pump’ the SIS mixers. This radial arrangement around the central LO antenna also allows for even spacing between the RF pixels and enough margins to route the IF signal to the edge of the receiver chip for wire bonding. It is worthwhile noting that this particular array arrangement is facilitated by the availability of substrate technology accessible to us, which in our case would be a thinned quartz wafer. Therefore, such an array design can be further simplified and improved, allowing for a more compact and arbitrary pixel arrangement, using a more versatile substrate such as the silicon-on-insulator (SoI) substrate.

It is obvious that the construction of such a 16-pixel array is ambitious at this stage. Therefore we aim to start with a 2-pixel demonstrator. In the following sections, we focus on the schematic layout of the 2-pixel demonstrator and describe in detail the LO distribution mechanism, the separation of the RF polarisations paths, the mixer circuit, and the overall balanced 2-pol receiver circuitry. Finally, we conclude the paper by presenting the full 2-pixel balanced 2-pol receiver design along with the predicted performance and the accommodating receiver block design.

3. SCHEMATIC OF THE BALANCED 2-PIXEL ARRAY DEMONSTRATOR

Fig. 2 shows the schematic of the 2-pixel demonstrator array. The LO power is coupled from a two-probe antenna (instead of 4-probe antenna since we only have 2 RF pixels here) and is distributed to each polarization branch of each pixel with a set of two microstrip couplers. The RF signal of each pixel is coupled on-chip via a 4-probe OMT, where each polarization state (hereafter Pol. 1 and Pol. 2) is fed from a set of opposing probes. As shown in Fig. 2, the layout of both pixels and all the polarization branches are identical from there onwards.

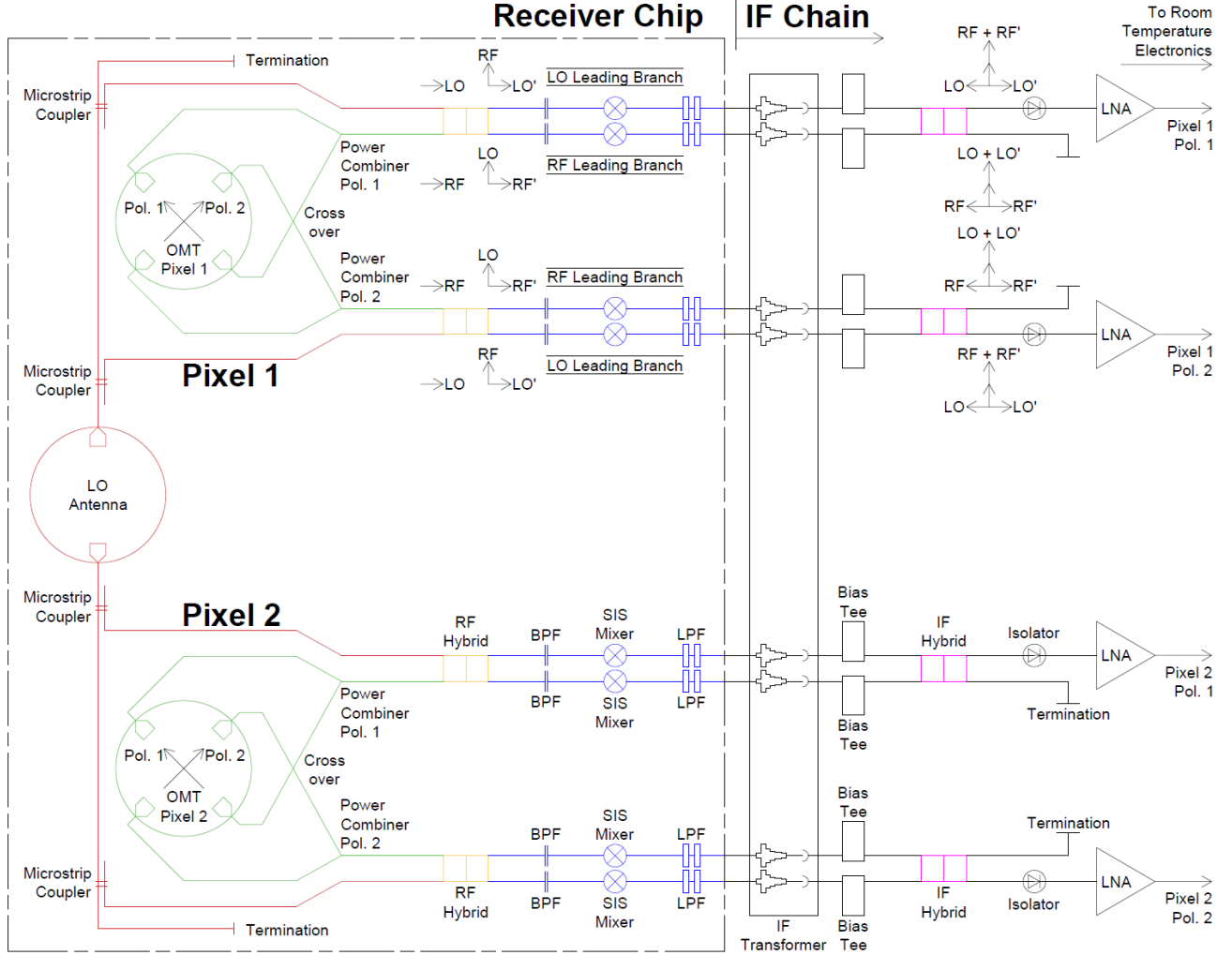


Figure 2: The schematic of the 2-pixel receiver. Components on the receiver chip are shown within the dashed rectangle, including the LO distribution network shown in red and the 2-pol RF receiver network of each pixel shown in green. The RF hybrids, coloured orange, combine the RF and LO signals before feeding to the mixer circuits shown in blue. The RF hybrid introduces a 90° phase difference between the RF and the LO signals, indicated by the vector diagram shown in Pixel 1 branches. The IF hybrid, coloured pink, introduces a similar 90° phase difference to separate out the down-converted IF and the LO noise component into two separate ports, hence the balanced operation mode.

Focusing on the Pol.1 branch of Pixel1: The signals of the OMT probe sets are routed via a crossover to the planar power combiner, where the output powers from both probes are recombined. The combined RF and the LO power from the top microstrip coupler are then fed into an RF quadrature hybrid. This hybrid splits the power of both, the RF and the LO signals, equally between its outputs. The output ports are connected to two identical mixer circuits comprising a bandpass filter (BPF), an SIS mixer circuit and a lowpass filter

(LPP). The down-converted IF outputs from these mixers are then fed to an IF quadrature hybrid via a series of IF transformers for impedance matching and bias-tees for DC-biasing the mixers. The output ports of the IF hybrids that contains the IF signal is then connected to the IF amplification chains for further processing.

3.1 Balanced Operation

One notes immediately that this configuration of feeding the RF and LO power to the two mixer branches via a set of RF and IF quadrature hybrid is in effect a balanced scheme. Similarly, focusing on the Pol. 1 branch of Pixel 1, the RF hybrid introduces a 90° phase shift between the RF and the LO tones, including the LO noise. As a result, the hybrid output for the top mixer branch indicated as ‘LO Leading Branch’ in Fig. 2 contains an RF/LO signal pair where the LO is leading the RF tone by 90° , as shown in the vector diagram in the figure. Likewise, the ‘RF Leading Branch’ has an RF/LO pair where the RF is leading the LO by 90° . This phase difference between the RF and LO tones remains unchanged during the mixing process. Once processed by the SIS mixers, the down-converted IF signals are fed via the IF transformers and bias-tees to an IF quadrature hybrid. Following the vector diagram of the IF hybrid, we see now that the top IF branch contains both the RF signals, which are in-phase, while the LO pair is 180° out-of-phase, hence cancelling out each other. Similarly, the LO pairs recombined in-phase at the bottom IF branch, which now contains all the residual LO and the corresponding noise contribution, hence can be terminated with a matched load, allowing for a LO-noise-free operation of the receiver.

In this 2-pixel example, the remaining LO power from the 2-probe antenna is terminated with an RF load. As the LO power needed to ‘pump’ an SIS mixer is relatively low, this terminated port, in fact, still contains quite a lot of LO power. This microstrip branch can therefore be used to ‘pump’ a subsequent array of SIS pixels, all with the same layout as the configuration of the pixel diagram shown earlier except for a minor alteration to the microstrip couplers (see later Sec. 4.1.2), hence the flexibility of this scheme to form a large array.

4. DESIGN OF THE FRONT-END RECEIVER CHIP

Fig. 2 shows the full receiver circuit diagram of the entire 2-pixel demonstrator, including both the front-end receiver chip, which contains all the high-frequency components, as well as the back-end IF signal chain. Since the microwave components required to form the IF chain can be purchased commercially, in the remaining of this paper, we shall focus only on the design of the front-end receiver chip.

We chose to demonstrate the feasibility of the array chip in the frequency range of 190–290 GHz, the low-band of the wideband Submillimetre Array (wSMA),¹² which also coincides with many other receiver bands of other telescopes such as Band 6 of the Atacama Large Millimetre/sub-millimetre Array (ALMA),¹³ Band 3 of the Northern Extended Millimeter Array (NOEMA)⁴ and the Receiver A (RxA) of the James Clerk Maxwell Telescope (JCMT).¹⁴ All of the front-end components of the receiver chip share several common features. All the planar circuit components are formed using three separate layers, a 400 nm Niobium (Nb) ground plane and a 400 nm top Nb wiring plane, sandwiching a 400 nm thick silicon monoxide (SiO) dielectric layer. The superconducting planar circuit is supported with a 50 μm thick quartz substrate. We also ensure that none of the circuit features has a dimension smaller than 3 μm to ease the fabrication process and improve the fabrication yield. Our mixers were designed based on the standard Nb/Al-AlO_x/Nb tunnel junction with a normal resistance of 20 $\Omega \mu\text{m}^2$ and geometric capacitance of 80 fF/ μm^2 , in which all the tunnel junctions are 1.5 μm^2 in size.

We designed and optimised the layout of our receiver chip using the commercially available Ansys® high frequency structure simulator (HFSS). However, it is not feasible to model the entire receiver chip in HFSS due to its large electrical size, spanning several tens of wavelength across the entire chip with features micron in size. From the discussion above and Fig. 2, it is clear that the circuit of the receiver chip can be grouped into three major parts: 1) The LO distribution network, 2) the 2-pol RF paths, and 3) the mixer circuit. Therefore, we split the 3D model of the receiver chip into three parts accordingly to speed up the simulations and better understand the behaviour of individual components without adding too much complexity. The overall performance of the full chip is then simulated by concatenating the scattering parameters of these three main parts following the circuit depicted in Fig. 2 using Ansys® Circuit Designer package.

4.1 LO Distribution Network

The most novel feature of our array chip design is the on-chip LO distribution network, feeding the LO from the planar 2-probe antenna to each polarization branch of all pixels of the array. This allows for a compact and easy-to-control LO power distribution design using planar circuit technology, replacing the complicated waveguide structures and thus simplifying the receiver design. Our LO distribution network comprises two main components: the 2-probe antenna and the microstrip couplers, interconnected with microstrips lines.

4.1.1 Two-Probe Antenna

The 2-probe antenna shown in Fig. 3(a) is basically one polarization probe-set of the 4-probe OMT used in the RF pixels. The 2-probe antenna is mounted directly underneath a drilled three-section flare-angle smooth-walled feedhorn^{9,10} that couples the free-space signal into the TE_{11} mode of the circular waveguide hosting the antenna. By aligning the probe set along the E-field direction of the TE_{11} mode, each of the probe would pick up one half of the incident LO power, and split evenly between the two output microstrips.

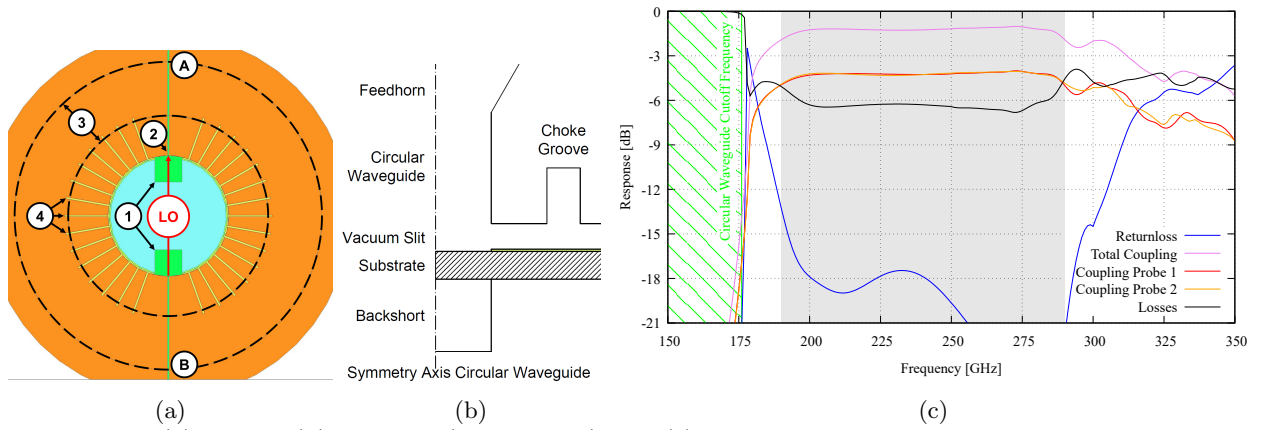


Figure 3: The (a) layout, (b) sideview (not-to-scale) and (c) predicted performance of the two-probe antenna. The probes (1) couple the TE_{11} mode from the circular waveguide via an intermediate microstrip impedance transformer (2) into microstrips (A) and (B). Losses through the vacuum slit above the chip are reduced by the choke groove shown with dashed lines (3), and the serrations in the ground plane (4) to prevent parallel-plate waveguide resonances in the ‘ring’ area between the choke groove and the circular waveguide. In the layout (a), the width of the microstrips and the serrations are artificially widened for clarity.

The probes are placed approximately a quarter-wavelength from the backshort section underneath the quartz substrate to improve the coupling into the microstrips connected to the probes. As the array chip is mounted along the split-plane of the receiver block, it is inevitable to mill a slightly deeper recess to avoid the planar circuit on top of the chip touching the receiver block and subsequently electrically shorting the circuit. This 50 μm wide vacuum slit above the chip and the 50 μm thick quartz substrate itself, however, provide a pathway for the LO energy to escape into both of these structures via parallel-plate waveguide modes instead of coupling in the microstrips. It is possible to reduce this leakage through the quartz by utilising a thinner substrate, but it is technically not feasible to polish a quartz chip thinner than 50 μm without risking the rigidity of the substrate. However, the losses through the vacuum slit can be reduced by employing a circular quarter-wavelength deep groove forming a choke structure at a quarter wavelength from the edge of the circular waveguide, as shown in Fig. 3(b). Using this method, we successfully improve the LO power coupling, but unfortunately, the introduction of the choke structure also induces unwanted resonances in the parallel-plate waveguide ‘ring’ area between the choke and the circular waveguide. Therefore, we further introduce a series of serrations in the ground plane around this ‘ring’ area to suppress these resonances.

As shown in Fig. 3(c), with the combination of the choke and serrations, as well as a single-section impedance transformer to bridge the impedance between the probe and the microstrip (for subsequent lower characteristic impedance connections), we managed to improve the total coupling from the circular waveguide to the set

of microstrips to approximately -1.3 dB. The return loss is better than -18 dB across the entire designated bandwidth. More importantly, the power coupling between the two probes is identical and flat across the entire band, ensuring that the LO power is distributed evenly between the two RF pixels. It can be noted from the plot that the loss through the substrate and the vacuum slit is still rather high at -6 dB. As mentioned earlier, this is possible to improve using a membrane technology to further thinning down the substrate, but unfortunately this technology is unavailable to us at the moment. Hence, we believe that the current performance is the best one could achieve using the standard quartz substrate technology.

4.1.2 Microstrip Coupler

As only a small portion of the LO power coupled from the 2-probe antenna needs to be injected into the SIS mixers, we utilise a series of planar microstrip couplers to route approximately -10 dB of the LO power to each polarization branch of each pixel. As shown in Fig. 4(a), our microstrip coupler is similar to the conventional design, where two adjacent microstrips are fabricated close to each other to allow for the fringing field lines to cross over between the two microstrips, with the fourth unused port terminated with a quarter-wavelength radial stub. However, as the field lines in a microstrip are strongly confined between the wiring and the ground plane, it is not feasible to increase the coupling level without too narrow a gap between the two microstrips or to transition into another type of transmission line topology. Following the design presented by Tan et al.,¹⁵ we employ a pair of slot openings in the ground plane underneath the microstrip pair to promote the field line crossover and therefore increase the coupling. This feature is important as the coupling level can be controlled precisely by altering the length and width of the slot openings. In our case, after the first coupler, the width of these slots in the subsequent coupler is widened accordingly to achieve the same power coupling as the first coupler, ensuring all the mixer branches are ‘pumped’ at a similar level. This simple design also allows us to employ the same coupler layout for a larger array since they can be cascaded in series easily and yield the same LO coupling for all pixels by simply controlling the slot dimensions.

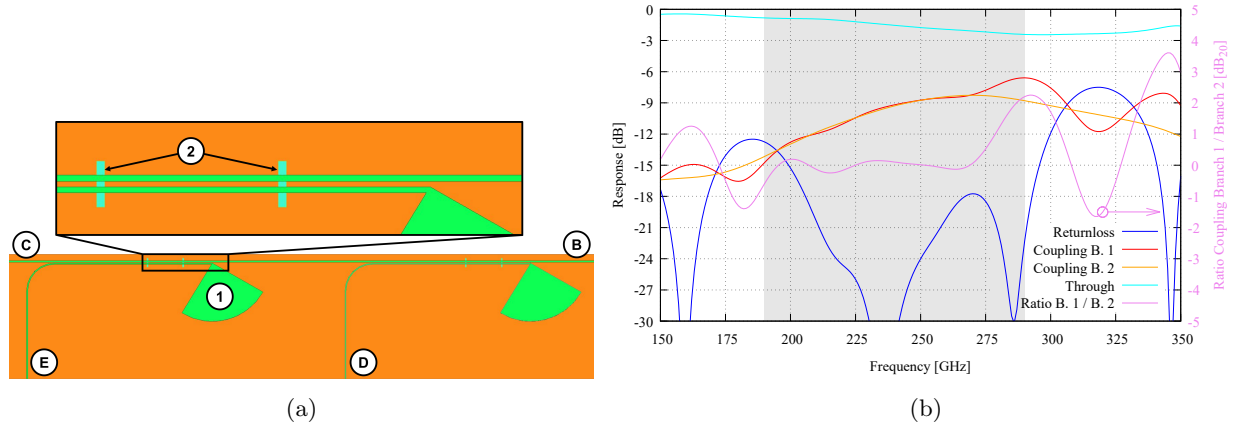


Figure 4: (a) The layout of the microstrip coupler, showing the main microstrip line, fed from the LO antenna (B) to (C), where more microstrip couplers can be connected or terminated. The LO power from (B) is coupled to (D) and (E) for subsequent connection to the two polarization branches of a pixel. The fourth port is terminated with a radial stub (1). The slot openings in the microstrip ground plane (2) improve the LO power coupling from (B) into each branch (D) and (E). (b) The predicted performance of the -10 dB microstrip coupler.

Using HFSS to optimise the performance of the microstrip coupler in the designated frequency range from 210–270 GHz, we successfully achieve an identical power coupling between -12 to -8 dB from the output of the probe to both polarization branches of one of the RF pixel of our 2-pixel demonstrator, as shown in Fig. 4(b). Again, the return loss performance is better than -18 dB across the band, and the coupling difference between the two couplers is less than 0.3 dB throughout. Although the coupling level is lower at the lower frequency ends, due to the nature of the fringing fields being less tightly confined in the dielectric layer at shorter wavelength, this effect has less impact on our application since the LO power can be adjusted while switching the LO frequency during observation. Therefore, the mixer can still be ‘pumped’ at a similar level over the full frequency bandwidth.

As explained earlier, even after a set of microstrip couplers, more than -3 dB of LO power remains in the main line. Thus, additional microstrip couplers can be cascaded to ‘pump’ subsequent pixels in a larger array.

4.2 Polarised RF Signal Coupling Network

The RF power coupling path of our receiver chip comprising mainly a 4-probe OMT antenna, a crossover and two power combiners, is shown in Fig. 5(a). The main objective of this network is to couple the polarised signal from the circular waveguide and split the two orthogonal states before feeding them separately into two individual branches for subsequent connection. The design of the 4-probe OMT is largely similar to the one described in Sec. 4.1.1, except now we incorporate another set of probes to form the 4-probe OMT. The crossover design has also been described in detail in Wenninger et al.,⁸ hence in the following, we shall only briefly summarise the design of the OMT and the crossover and focus mainly on the design of the power combiner.

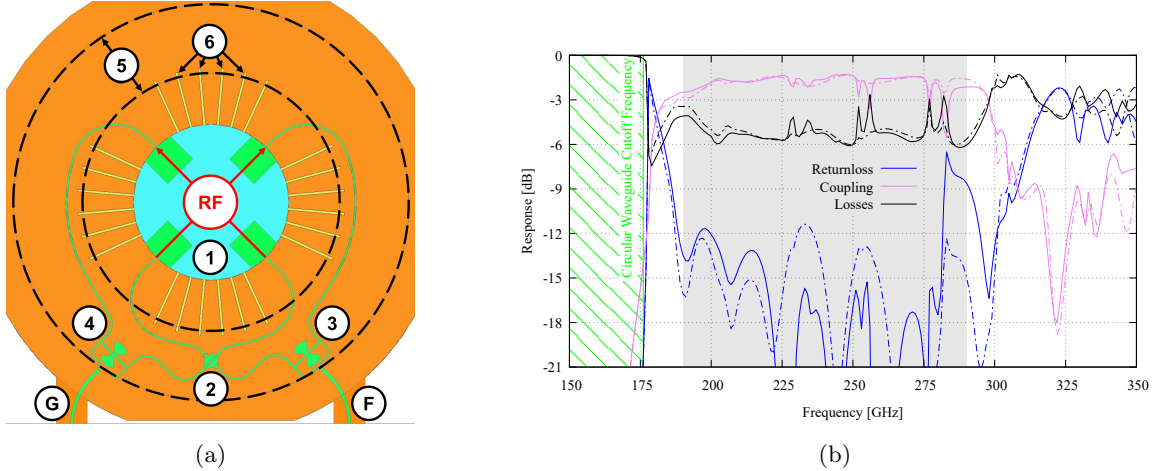
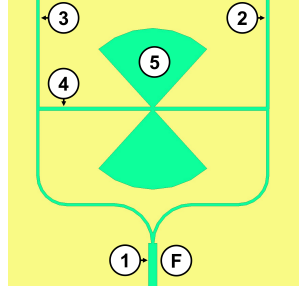


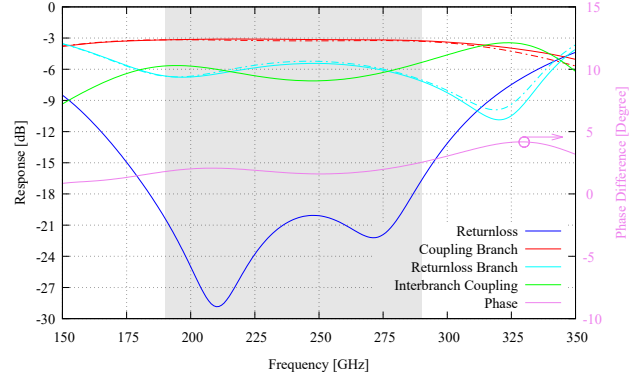
Figure 5: (a) The layout of the OMT-to-power-combiner circuit. The four-probe OMT (1) couples both polarisation states from the circular waveguide with two sets of opposing probes. The signal of a probe set is then routed via the crossover (2) to the power combiners (3) & (4) for Pol. 1 and Pol. 2 states respectively. The recombined signal power at (F) and (G) would be fed to the subsequent mixer circuits. Similar to the LO antenna, the OMT features a choke groove (5) and serrations in the ground plane (6). The width of the microstrips and the serrations are artificially widened for clarity. (b) The predicted performance of the OMT-to-power-combiner circuit. The response of Pol. 1 is shown with solid lines and Pol. 2 with dash-dotted lines.

The OMT couples the two TE_{11} polarization states from the circular waveguide into microstrips via two pairs of opposing probe sets. Similarly to the LO antenna, the incident power of a polarization state splits evenly between the opposing probes, hence needs to be routed to the same location on the chip for recombination. This routing, however, leads unavoidably to the need for a crossover. The detailed design of our crossover can be found in Wenninger et al.,⁸ which based on the layout shown in Abbosh et al.¹⁶ and Tan et. al.¹⁷ In principle, the cross-over is achieved by transition one of the microstrips into a coplanar waveguide (CPW) in the ground plane via a set of broadside couplers to avoid physical contact with the other microstrip trace. In order to further minimise cross-talk between the two transmission lines, the top microstrip trace is further enhanced with two ‘ground patches’ forming a quasi-grounded CPW structure in the wiring layer.

After routing the output power from the probe set to the proximate locations on the chip, the RF power from each probe set is recombined using the planar power combiner shown in Fig. 6(a). The design of a planar power combiner is challenging with the standard photolithography fabrication process we utilised here, as it is difficult to fabricate a planar power absorbing component to replace the resistor in a conventional Wilkinson power combiner without complicating the fabrication process. It is possible to terminate this power absorbing port, transforming a 4-port Wilkinson power combiner into a 3-port device, but it is well known that it is not possible to match the impedance of all ports in a lossless 3-port device. In this case, we opt to match only the power combining output port with an equal -3 dB in-phase coupling from the two input ports while leaving the return losses and the coupling between the two input ports fixed at approximately -6 dB.



(a)



(b)

Figure 6: (a) The layout of the power combiner. The matched combined port (1) is fed by two branches (2) and (3), which are interconnected with a microstrip (4) and two radial stubs (5). (b) The predicted performance of the combiner. The responses of the individual branches are shown as solid and dash-dotted lines.

For the termination of the power absorbing port, we introduce a back-to-back radial stub structure with a microstrip connecting the two input ports. These radial stubs act, in effect, as a quasi-lossy component to radiate away the power imbalance between the two input ports, hence slightly improving the combiner's performance. As shown in Fig. 6(b), with this method, we successfully achieve a uniform -3 dB coupling from the two input ports to the combined output port across the required band, with the phase difference close to 0° throughout the band. The return loss performance of the combined port is well below -20 dB as well. The only downside here is the -6 dB return loss of the input ports and the power coupling between these two ports at a similar level. However, it is worth noting that this combiner is very simple to design and does ease the fabrication process significantly, as the structure can be fabricated using the same material as the other circuit components, using just the microstrip topology.

4.2.1 Performance of the Integrated Polarised RF Signal Coupling Network

Once the individual circuit components are optimised, we integrate them within the HFSS environment to form the entire RF signal coupling network. This network guides each polarised RF signal to be combined with the LO power from the LO distribution network before feeding to the subsequent mixer circuits. As the planar power combiner we utilised here is an in-phase power combiner, while the phase difference between the two probes from the probe-set of each polarisation branch is 180° out of phase, we need to ensure that the lengths of the two microstrip lines that connect the outputs of the probes to the inputs of the combiner are differed by 180° to compensate for the 180° phase difference. In our design, those microstrips guided through the crossover are a half-wavelength shorter than their counterpart without the crossover. These microstrips also feature several sections of quarter-wavelength impedance transformers to match the output impedance of the probes to the input impedance of the power combiner.

We should emphasise that the simplest way to combine a 180° out-of-phase signal pair is, in fact, a 180° hybrid, where the two signals combine at the 'difference' port. However, this would require an efficient way to terminate the 'sum' port of the hybrid, such as the use of another mixer circuit biased above the gap voltage acting as a matched load.^{18,19} It is obvious that this method complicates the array chip design substantially, requiring six mixer branches now instead of four, and consequently making the chip unnecessarily larger due to the additional bonding pads for biasing these 'terminating' junction loads.

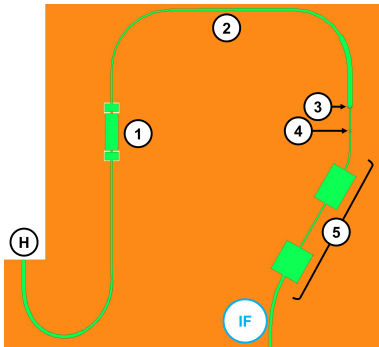
Referring back to Fig. 5(b), where we show the simulated responses of the RF signal coupling network, we see that the overall performance of the network is good. The power coupling from the OMT to the output of the power combiner stays near the -1.8 dB level. The return loss of the entire network remains below -10 dB across the band for both polarization states, except for the very high-frequency end of the band for Pol. 1. The total loss in the network is about -5 dB, again dominated mainly by the energy loss of the OMT antenna through the quartz substrate and the vacuum slit, similar to the case of the LO antenna. More importantly, we see that

the behaviour for both polarization branches remains largely identical throughout the band, preventing any bias during observations with the receiver.

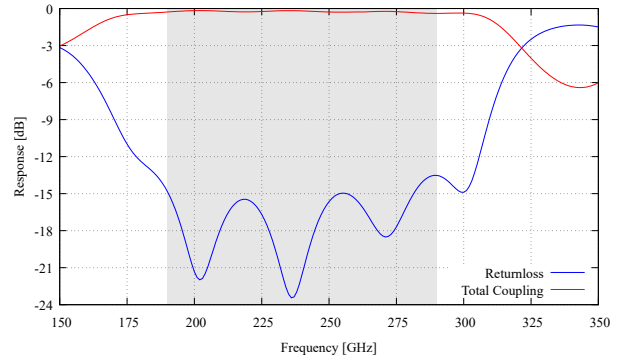
However, it is evident from the plot that there are unexpected resonance features within the network. Curiously, Pol. 1 appears to have a more repeated resonance structure than the other. The causes of this, together with the unexpected higher return loss for Pol. 1 at the high-frequency end, are still under investigation. We suspect this could be due to the high return losses from the input ports of the power combiner, reflecting -6 dB of power back to the OMT probes which subsequently coupled via the OMT to the other branches and setting up unwanted standing wave within the system. It could also be caused by the imperfect impedance matching between the individual components, particularly at the broadside couplers of the crossover. However, we do not rule out that the issue could simply be caused by the irregular meshing by HFSS due to the large electrical model of the network. Therefore, further investigations are required to identify the root cause of these unexpected effects by carefully tracing the energy flows between all the components forming the RF signal coupling network.

4.3 Mixer Circuit

The final major component of the array chip is the mixer circuit shown in Fig. 7(a), comprising the DC and IF blocking BPF, the SIS tuner circuit and the RF-chokes acting as LPF for the IF chain. The design of this mixer circuit is largely similar to the one reported earlier.⁸ Hence we shall only briefly describe the individual components making up the mixer. The main function of the BPF before the mixer tuner circuit is to prevent IF signals from coupling into the RF and LO network, which would affect the IF output power. Furthermore, the BPF also allows for independent biasing of each mixer circuit branch by physically disconnecting the microstrip such that the top metallisation layer of the subsequent components is not in direct electrical contact with the remaining circuit components prior to the BPF. This is achieved by using a pair of broadside couplers to transform the microstrip into a CPW in the ground plane and back into a microstrip, hence physically breaking the microstrip, similar to the crossover shown earlier.



(a)



(b)

Figure 7: (a) The layout of the mixer circuit. The RF and LO signals fed from (H) couple through the BPF (1) and an impedance transformer (2) to the twin-junction mixer, comprising a first (3) SIS junction, a short intermediate microstrip and a second (4) SIS junction. The twin-junction is followed by a LPF (5) to prevent RF power leakage into the IF circuit. (b) The simulated performance of the mixer circuit.

For tuning out the unwanted junction capacitance, which would otherwise short the tunnel junction, we employ the commonly used twin-junction tuner method.²⁰ Here, the two SIS junctions are separated by a short microstrip, transforming the complex reactance of one junction into the conjugate of the counterpart, therefore cancelling out the junction capacitance and presenting a full resistive load to the incoming RF and LO signals. To further improve power coupling to the SIS junctions, a series of high-low impedance chokes are employed to form a LPF, allowing only the down-converted IF signal to propagate through for further amplification. As shown in Fig. 7(b), we successfully achieve a total coupling from the input port of the mixer circuit to the twin-junctions better than -0.4 dB throughout the designated bandwidth, with a return loss less than -15 dB across.

5. DESIGN OF THE INTEGRATED 2-PIXEL ARRAY CHIP

As shown in Fig. 2, the three main sub-circuits, the LO distribution network, the RF signal coupling network and the mixer circuits, are integrated via a series of quadrature hybrids to form the entire 2-pixel array receiver chip. The design of the hybrid is pretty straightforward, and has been described in detail previously,⁸ where we cascade two conventionally used branch-line quadrature hybrids in series to broaden the operational bandwidth as shown in Fig. 8(a).

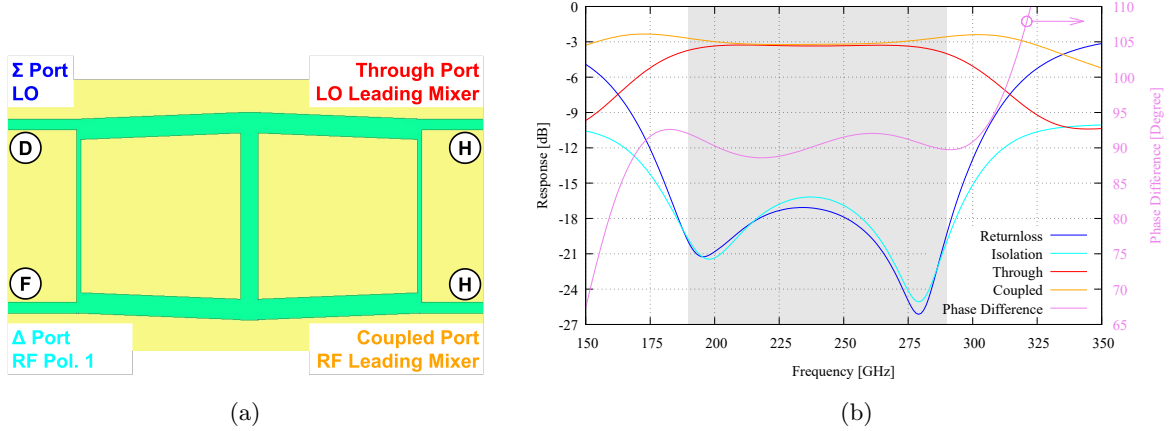


Figure 8: (a) The layout of the two-section branch-line 90° hybrid. The labels in the figure show the conventional used port names of hybrids, as well as the connection reference to other circuits with reference to Pol.1 branch of Pixel 1. (b) The simulated performance of the quadrature hybrid. The colour code of the performance corresponds to a signal applied at the Σ port.

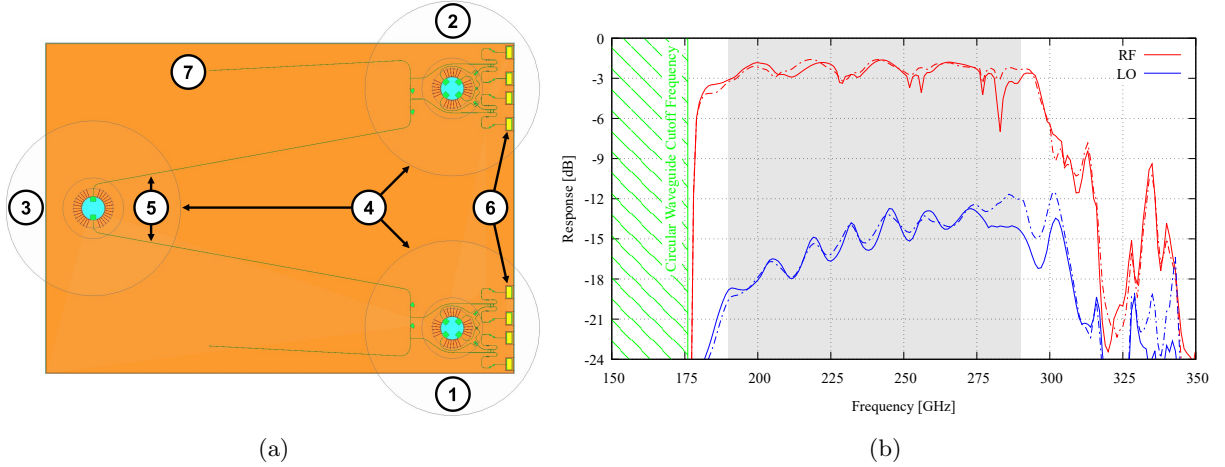


Figure 9: (a) The layout of the full receiver chip. Pixel 1 (1) and Pixel 2 (2) are identical, comprising the polarised RF signal coupling network, the hybrids and mixer circuits for each polarization. The microstrip couplers are placed to the left of the OMTs of the RF pixels to couple the LO power from the LO antenna (3). The spacing between the LO antenna and the RF pixels is mainly dictated by the aperture of the feedhorns (4), resulting in long microstrips (5) connecting the LO antenna and the microstrip couplers. The IF bonding pads (6) are at the right-side edge of the chip. The location of the bonding pads for the ground and the termination of the remaining LO power (7) is to be finalised. (b) The predicted performance of the full 2-pixel array chip, showing the total RF and LO power coupling from the circular waveguides to the SIS mixers of Pixel 1. The responses of both pixels are identical, where Pol. 1 performance is shown with solid lines, and Pol. 2 with dash-dotted lines.

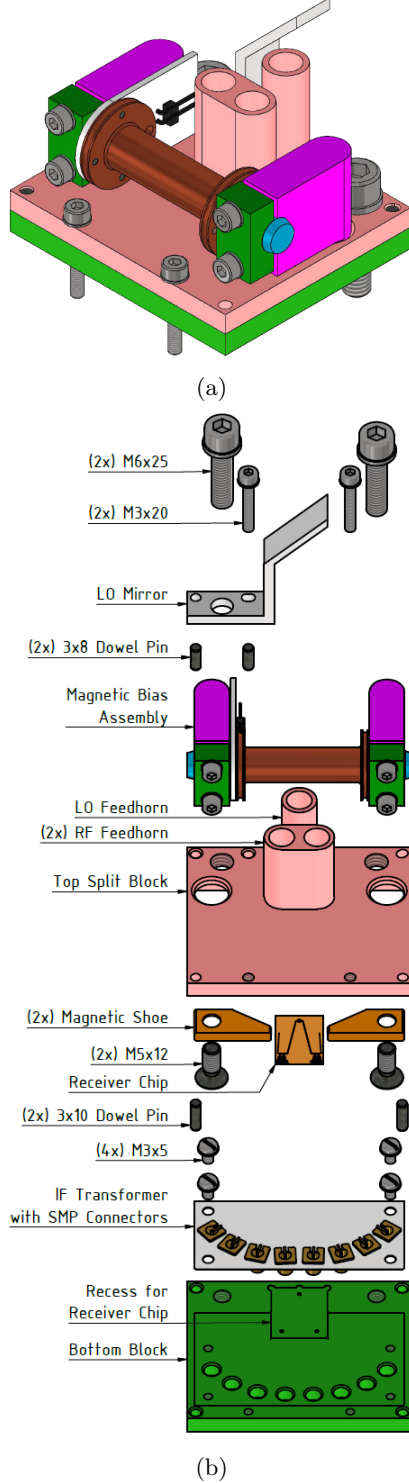


Figure 10: The (a) assembled receiver block and (b) exploded view with all required components.

As the layout of the integrated LO-RF-mixer circuit is identical for both pixels and both polarization branches, we shall focus only on Pol. 1 of Pixel 1. The two input ports of the RF hybrid are connected to the LO distribution network and the RF coupling network, resulting in an equal distribution of RF and LO power to the two output ports, which are subsequently connected to two identical mixer circuit branches. In our design, the LO and RF signals are applied to the Σ and Δ ports of the hybrid shown in Fig. 8(a). The simulated performance of our RF hybrid is shown in Fig. 8(b). As expected, we successfully achieve equal and flat -3 dB coupling from the input ports to the ‘through’ and ‘coupled’ output ports. The return losses for both input ports and the isolation between the two input ports are well below -15 dB across the band. The phase difference between the two output ports remains close to 90° throughout the band, with a $\pm 3^\circ$ variation. However, it is well-acknowledged that the performance of a balanced SIS mixer is relatively tolerant to the phase difference variation,^{18,21} therefore we expect a good performance of the array chip design presented here.

Fig. 9 shows the full array receiver chip layout, mapping the design schematic shown in Fig. 2. The size of the chip is measured at $13.8 \times 19.6 \times 0.05$ mm, primarily constrained by the size of the feedhorns’ aperture. Although the entire RF circuit network for a single pixel, including the mixer circuits, could be fit within an area of 4.6 mm by 3.8 mm, but we need to separate the two RF OMTs by about 10 mm to accommodate the feedhorn aperture with a diameter of $\varnothing 7.3$ mm. The LO antenna is centred 15 mm away from the RF pixels to allow for additional optical components to guide the LO power to the mixer block.

Nevertheless, this relatively small receiver chip allows us to design a compact receiver block, measuring only $64.0 \times 55.0 \times 34.4$ mm in size, as shown in Fig. 10(a). This receiver block can be easily machined using two-part split-block technology, along with the assembly to apply magnetic field across the SIS junctions, the IF transformers, and IF connectors for connections to the bias-tees and the IF hybrid. As can be seen from the exploded view shown in Fig. 10(b), this split block design simplifies dramatically the fabrication of the array block. It requires only milled recesses for the RF chip and IF board, and holes for various connectors, in comparison to traditional array designs that are often populated with a large waveguide network throughout the block.

As explained earlier, the overall performance of our full receiver array chip is simulated by concatenating the scattering parameters of the three main sub-circuits together with the RF hybrids, using Ansys[®] Circuit Designer package. Fig. 9(b) shows the RF and the LO coupling responses for one of the pixel (the response are identical for both pixels). It is clear that the simulated performances are very similar for the two polarization branches. The RF signal couples on average -2.5 dB from the circular waveguide into the SIS junctions with approximately -19 dB to -13 dB of LO power across the band, sufficient to pump the mixer array with our existing LO source.²² If the LO coupling level is too low, we can easily alter the design of the

microstrip coupler to improve the coupling e.g., increasing the coupling level of the microstrip coupler by 4 dB to increase the overall LO power coupling from the waveguide to the mixer to a level between -15 dB and -9 dB. This modification requires only a replacement of one photo-fabrication mask (the ground plane).

Another potential improvement upon the current design is flattening of the standing wave structure shown in the performance of our array receiver chip. This can be seen clearly in Fig. 9(b), where both the LO and RF power coupling level, as well as the return losses, are undulating at about ± 1 dB level. The root cause for the existence of the standing wave is unclear and requires further investigation. We suspect that it is caused by the imperfect impedance matching between the different circuit components and/or by the -6 dB return loss and coupling between the branches of the power combiner. The prior issue could be resolved by re-optimising the impedance transformers deployed at different stages. At the moment of writing, we are also improving the performance of the power combiner using a different methodology, hoping to reduce the return loss of the input ports. However, it is worth noting that because we cascade these sub-circuits to form the full-chip model, a small artificial impedance miscalculation in HFSS could also cause these coupling level undulations. This is because an accurately calculated port impedance of the sub-circuits requires a high number of meshing passes in HFSS, which inevitably increases the model size and results in an impractically long simulation run.

6. CONCLUSION

We have described the design of a 2-pixel 230 GHz dual-polarisation balanced SIS mixer array. We replaced the RF and LO circuit components traditionally comprising various waveguide structures with planar on-chip circuits, therefore allowing for miniaturisation of the array block design and easing the construction of a large array. We described in detail the electromagnetic design of the various components forming the full receiver chip, as well as presented their predicted performance. Finally, we integrated all these optimised circuit components to form the full-chip model and discuss the overall performance of the 2-pixel receiver array. We showed that we could achieve good and uniform coupling for both pixels in both polarization states, demonstrating the feasibility of constructing such a 2-pixel array with planar on-chip technology. Although we have achieved reasonable performance, there is still potential for improvements, such as improving the return loss performance of the power combiner and minimising the coupling undulations of the receiver chip. Nevertheless, we demonstrated that our approach of extending the array size via planar on-chip technologies is achievable without sacrificing the bandwidth performance of the array.

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