Field Emission from Porous Silicon

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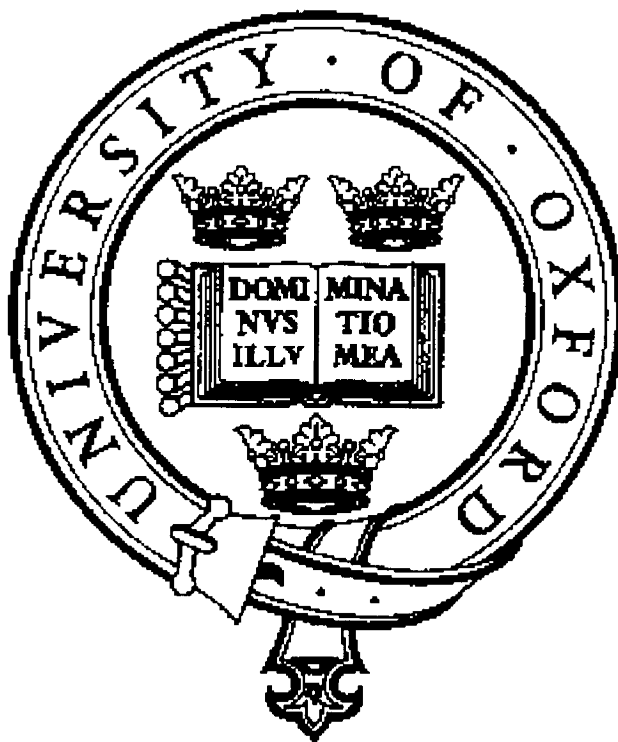
Trinity Term 1997



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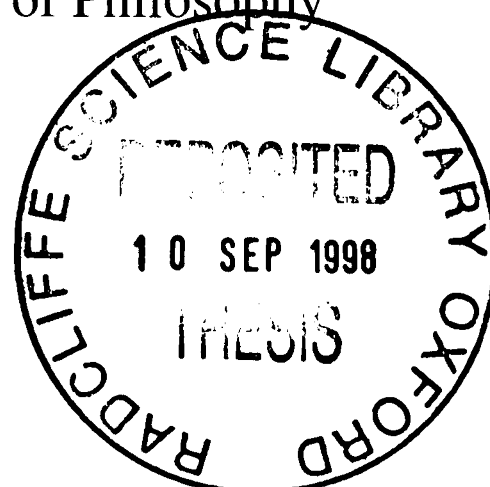

ABSTRACT

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Vacuum microelectronic (VME) devices are of interest for the development of flat-screen displays and microwave devices. In many cases, their operation depends on the field emission of electrons from micron-sized cathodes (semiconductor or metal), into a vacuum. Major challenges to be met before these devices can be fully exploited include obtaining - low operating voltages, high maximum emission currents, uniform emission characteristics, and long-term emission stability.

The research in this thesis concerns the production of silicon field emitters and the improvement of their emission properties by the process of anodisation. Anodisation was carried out for short times, in order to form a very thin layer of porous silicon (PS) at the surface of both p and p^+-type silicon emitters. The aim in doing this was to form a high density of asperities over the surface of the emitters. It was the intention that these asperities, rather than the "macroscopic" apex of the emitter, would control emission. This was the first work of its kind to be carried out.

Transmission electron microscopy was used to characterise the morphology of p and p^+-type silicon emitters before and after anodisation. Both the structure and arrangement of the surface fibrils, the thickness of the PS layers at the apex and nature of PS cross-sections were studied. The morphology was correlated to subsequent field emission measurements.

Field emission characteristics, before and after anodisation, were obtained using a scanning electron microscope adapted for field emission measurements, and a field emission microscope. Extensive measurements showed that, following anodisation, there was substantial improvement in emission behaviour. After anodisation, the following was found to be true:

i) The starting voltage was reduced by up to 50% (with p^+-type PS emitters exhibiting a greater reduction in starting voltage than p-type PS emitters).
ii) Number of emitting tips per array was increased.
iii) Higher maximum currents (up to 3 times higher) were obtained before tips underwent destruction.
iv) The resistive effect of the PS layer at the apex was important in determining the maximum current obtained from a tip.

In addition, both field emission and field ion microscopy were used to identify the emission source following anodisation. It was shown that individual fibrils on the emission surface caused an increase in field enhancement over a flat plane, leading to emission at lower voltage.

Overall, porous silicon appears to be a very promising material for field emission displays.

Preface

This thesis reports work conducted by the author during the period October 1992 to September 1997 in the Department of Materials, University of Oxford. No part of this work has been previously submitted for a degree at this or any other University. Where the work of others has been mentioned, it has been referenced and acknowledged.

Some of the work reported in this thesis has already been published in the following papers:

1) E.C.Boswell and P.R.Wilshaw, 'Emission Characteristics and Morphology of Wet Etched Cathodes in P-Type Silicon', J. *Vac. Sci. Technol.* (1993), **B 11(2),** 412
2) P.R.Wilshaw and E.C.Boswell, 'Field Emission from Pyramidal Cathodes Covered in Porous Silicon', *J. Vac. Sci. Technol.* (1994), **B 12(2),** 662
3) E.Boswell, T.Y.Seong and P.R.Wilshaw, 'Studies of Porous Silicon Field Emitters', *J. Vac. Sci. Technol.* (1995), **B 13(2),** 437
4) E.C.Boswell, M.Huang, G.D.W.Smith and P.R.Wilshaw, 'Characterization of Porous Silicon Field Emitter Properties', *J. Vac. Sci. Technol.* (1996), **B 14(3),** 1
5) E.C.Boswell, S.E.Huq, M.Huang, P.D.Prewett and P.R.Wilshaw, 'Polycrystalline Silicon Field Emitters', *J. Vac. Sci. Technol.* (1996), **B 14(3),** 1
6) S.E.Pullen, M.Huang, S.E.Huq, E.C.Boswell, P.D.Prewett, G.D.W.Smith and P.R.Wilshaw, 'Enhanced Field Emission from Polysilicon Emitters Using Porous Silicon', *presented at 9th International Vacuum Microelectronics Conference in St. Petersburg, Russia (1996)*

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Appendix - Background Theory for Field Ionization and Field Emission Microscopy

Chapter 1 - Introduction

1.1 Background

In recent years, there has been a dramatic increase in technological interest in the area of vacuum microelectronics (VME), a category of electron devices which exploit the mechanism of electron field emission into a vacuum. This thesis describes research carried out to improve the emission characteristics of silicon VME devices.

1.2 Basic Structure of Devices

VME devices are based on traditional thermionic-based vacuum devices, such as that shown in Figure 1.1a. Shoulders (1961) designed the first VME device and Spindt (1968) built the first functioning device, using the basic structure shown in Figure 1.1b. VME devices most commonly use sharp tips (cathodes) to enhance locally the applied electric field, allowing field emission to occur at low voltages, by electron tunnelling through a potential barrier. The process of field emission and the parameters affecting it are discussed in detail in Chapter 2.

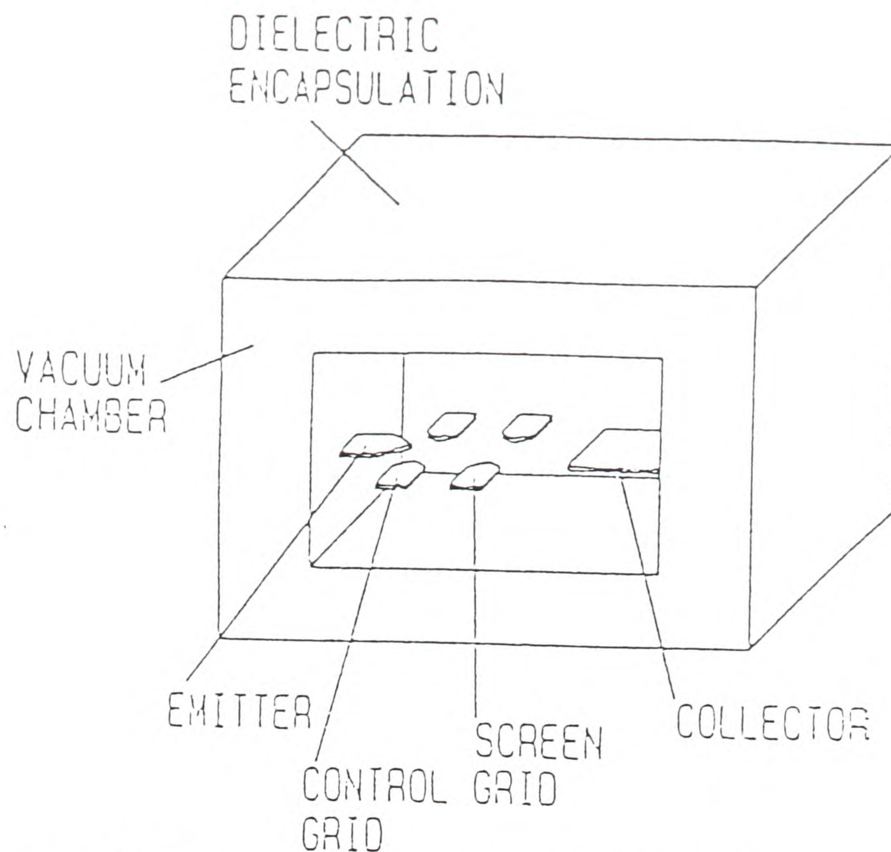
In a VME device, an electric field is applied to the tip of an emitter, using a gate placed typically a few microns away. Electrons are collected using an anode placed just beyond the gate, see Figure 1.1b. The cathodes themselves are only a few microns in dimension, typically being conical/pyramidal in geometry and having tip radii of nanometre dimensions. VME devices contain either individual cathodes, or arrays of cathodes (typically 25,000 tips per mm^2), depending on the application.

1.3 Applications

Potential uses for VME technology are described in detail by Spindt & Brodie (1992), Ianazzo (1992) and Busta (1992). The main applications are summarised below:

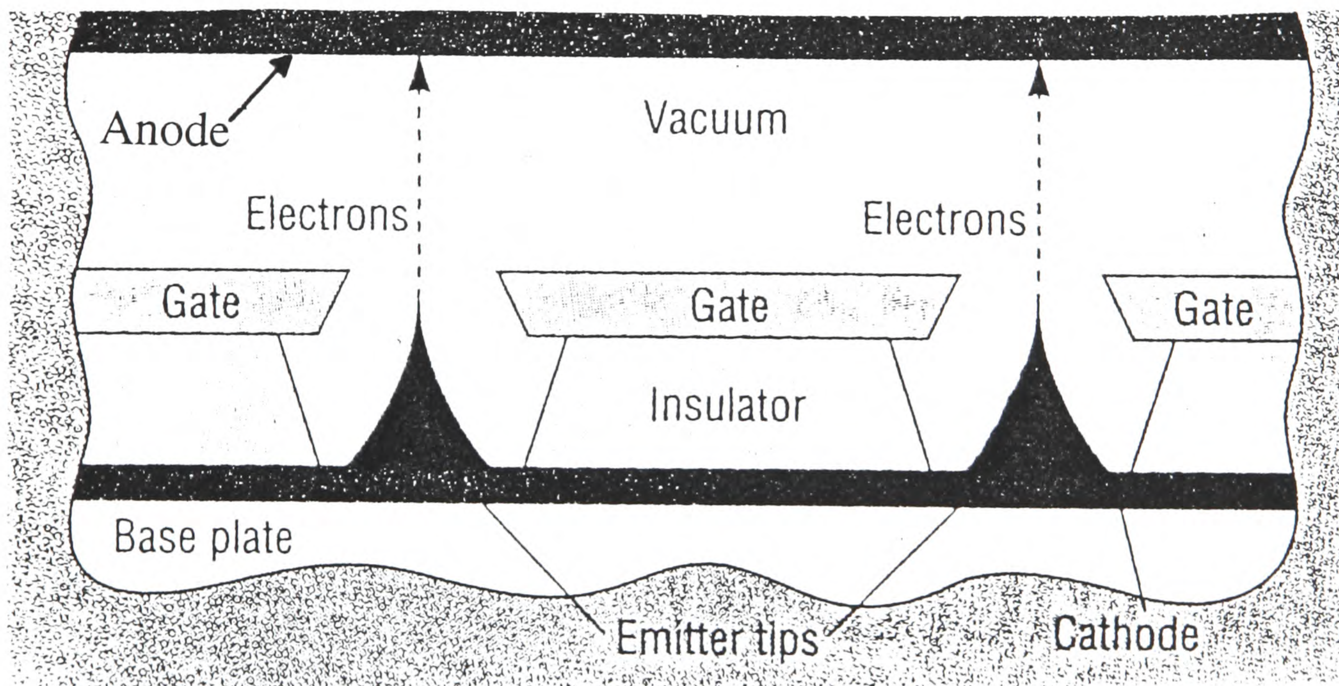
a) Flat Panel Field Emission Displays

A diagram of a field emission display (FED) is shown in Figure 1.2. An FED is a mini version of a cathode ray tube (CRT), in that a phosphor screen lights up when excited by a source of



(Ref: H.H.Busta, *J. Micromech. Microeng.*, **2** (1992), 43)

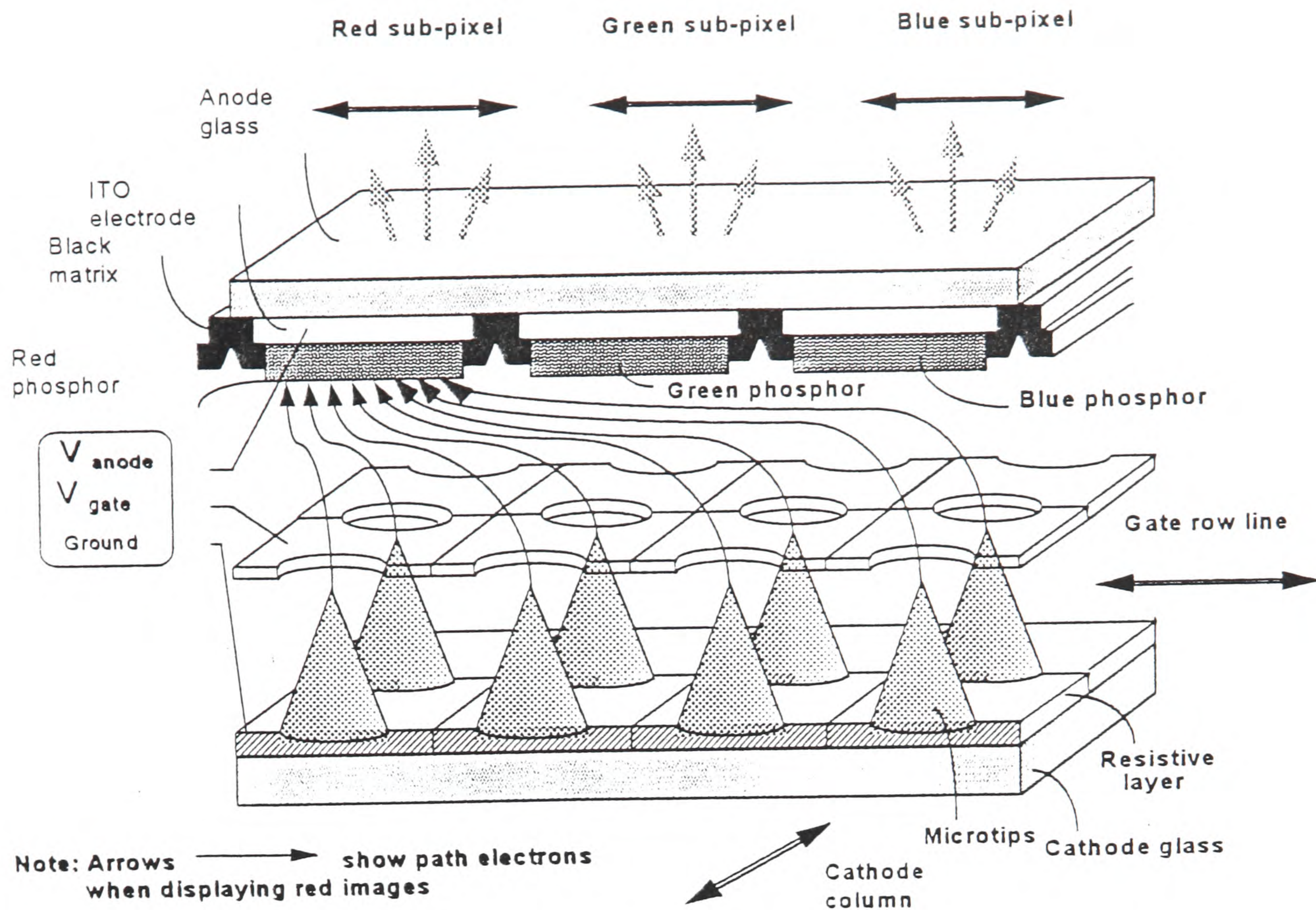
a) Basic Structure of Traditional Lateral Vacuum Device
This figure shows the structure of a traditional thermionic-based vacuum device. The design of vacuum microelectronic (VME) devices is based on this basic structure - i.e. there is an emitter cathode, a control grid and a collector anode. However, VME devices are based on field emission (rather than thermionic emission) from sharp semiconductor/metal emitters. VME devices operate at much lower voltages than for thermionic devices.



(Ref: P.H.Holloway, J.Sebastian, T.Trottier, H.Swart and R.O.Petersen, *Solid State Technology*, **Aug.** (1995), 47)

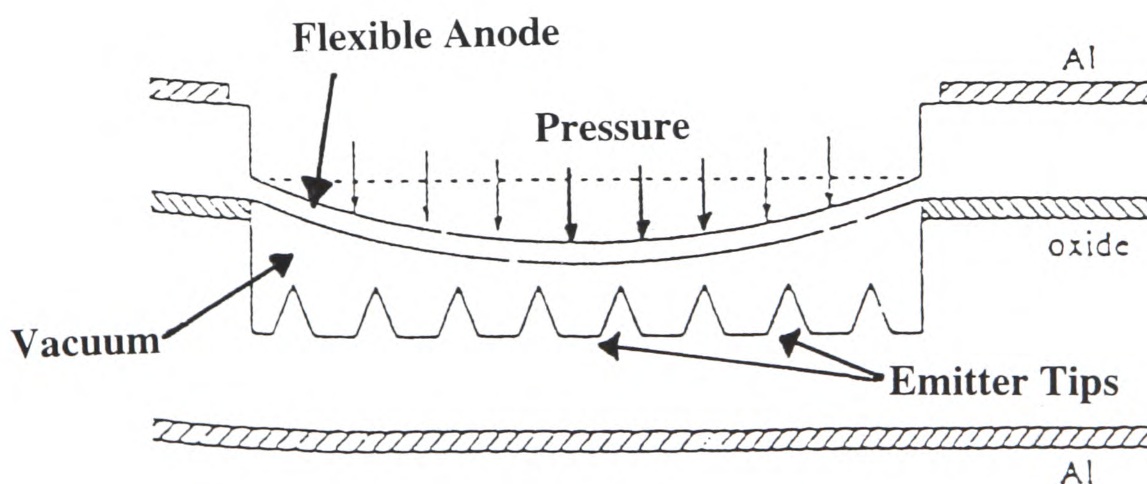
b) Typical Structure of Vacuum Microelectronic Device
In a VME device, an electric field is applied to the tip of an emitter using a gate placed a few microns away. The tips themselves are only a few microns high, are typically conical/pyramidal in geometry and have tip radii of nanometre tolerances. Field emission current is collected by an anode positioned above the gate. The entire device operates within a vacuum. VME devices can exist as individual cathodes, or as arrays of cathodes.

Figure 1.1 - Basic Structure of Vacuum Microelectronic Device



(Ref: Internal report by Pixel International, France)

Figure 1.2 - Diagram of Field Emission Display (FED)
A field emission display is a mini version of a cathode ray tube (CRT). Instead of simply collecting the field emission current, the anode is a phosphor screen which illuminates when hit by electrons. In an FED, there are thousands of emitting tips at every pixel. The entire display is very thin compared to a conventional CRT display.



(Ref: H.H.Busta, *J. Micromech. Microeng.*, **2** (1992), 43)

Figure 1.3 - Diagram of VME Pressure Sensor
Vacuum microelectronic devices can be used to produce pressure sensors. In this type of device, the anode is flexible and will deflect when the pressure changes. When the anode deflects, the emitter-anode separation will change and hence affect the emission current collected. This is in turn will lead to a change in the sensor reading.

electrons. However, whereas CRTs produce an electron beam by thermionic emission (where electrons escape over a potential barrier), FEDs operate by the tunnelling of electrons through a potential barrier. In addition, there are thousands of emitting tips at each pixel of an FED, each directing a static, unfocused electron beam onto a tiny part of the display. In a CRT, there are only three electron guns - one single electron gun for each colour scans across the entire screen. Due to the difference in these arrangements, FEDs are much thinner than conventional CRTs.

There are many applications for flat panel displays, see Holland *et al.* (1987), Ghis *et al.* (1991) and Wilson (1994). Examples are listed below:

i) Consumer Electronics Displays - Portable computers, wrist watches, virtual reality headsets, camcorders, video telephones, multimedia displays, pressure-sensitive flat displays (which can be operated with pens), flat wall-hung televisions and digital cameras.

ii) Military applications - High definition table-top displays, helmet-mounted and "head-up" displays, and advanced navigational systems.

The advantages of FEDs versus competitor flat panel technologies are summarised in Table 1.1. The market for flat panel displays is expected to be worth $50 billion a year by the year 2000, see McKie (1994) and Hewson (1994). In the US, the development of flat panel displays is regarded as so important that the government has spent $1 billion helping US companies to develop flat panel displays, see Bradsher (1994) and Manners (1994). Many companies, including Coloray, Micron Technology, Motorola, Silicon Video (backed by Compaq, Hewlett-Packard and Lawrence-Livermore Laboratories), Texas Instruments, Raytheon and SI Diamond, have announced plans to manufacture FEDs in the US. In France in 1993, Pixel demonstrated a 6-inch colour FED (256x256 pixels) and opened a pilot manufacturing plant, see Wilson (1993) and Ferranti (1994). Pixel have licensed this technology to Texas Instruments, Raytheon and Futaba. It is believed that many Japanese, Korean and Taiwanese companies are also actively developing FED technology.

Advantage	Details
Reduced Thickness	Field emission displays (FEDs) are thinner than cathode ray tubes (CRTs) - FEDs can be as thin as 2.4mm.
High Brightness	FEDs have similar brightness to CRTs (~200cd/m^2), but are brighter than LCDs (~60cd/m^2). Another advantage versus LCDs is that FEDs do not require back-lighting.
Viewing Angle	FEDs have excellent viewing angles of ~180°C. This is much greater than for LCDs.
Low Power Consumption	FEDs use much less power than CRTS and competitor flat panel technologies. For example, the power consumption of a 10-inch LCD is ~4W. However, the power consumption of a similar-sized FED is estimated to be only ~1W.
Simple Manufacturing Process	Production of FEDs should be easier than for LCDs, where a large proportion of displays have to be scrapped during production (due to the complex manufacturing procedure for the thin film transistors needed to address the pixels). Standard equipment presently used in the semiconductor industry can be used to fabricate FEDs.
Wide Operating Temperature Range	LCDs can only operate within the range 0°C to 50°C, whereas the temperature range for FEDs is much wider. The extended operating range of an FED would be useful for military, aeronautical and space applications.
High Speed Response Time	In applications such as videos, AMLCDs switch quite slowly, causing a smearing effect. However, FEDs do not have such problems - FEDs have a response time of <2μs.
Low Weight	It is important that flat panel displays are light so that they are easily portable. FEDs are much lighter than CRTs, as a large protective vacuum casing is not required. They are also approximately one third lighter than LCDs.

Although there are competing technologies for the flat panel market, such as liquid crystal displays (LCDs), plasma displays, ferroelectric crystal displays and electroluminescent displays (see Werner (1993), Browning (1995) and Rodgers (1995)), FEDs have characteristics which are potentially superior in some respects. The advantages of FEDs versus cathode ray tubes (CRTs) and competitor flat screen technology are summarised in this table.

Table 1.1 Advantages of Field Emission Displays versus CRTs and Competitor Flat Screen Technology

b) Ultra-High Frequency Devices

Vacuum microelectronics has also been used to develop ultra high frequency (UHF) devices, used for power sources, microwave amplifiers and beam deflection devices, see Devyatkov *et al.* (1989), Orvis *et al.* (1989), Spindt *et al.* (1993), Cha-Mei Tang (1994), Kodis *et al.* (1996) and Spindt *et al.* (1996). Applications are discussed in detail by Gray (1967) and Brodie & Spindt (1979). Advantages of these devices are summarised in Table 1.2.

c) Pressure Sensors

Figure 1.3 shows a diagram of a VME pressure sensor. In such a sensor, the anode is flexible and will deflect when the pressure changes. When the anode deflects, the emission current collected will change, which in turn alters the sensor reading. Lee *et al.* (1991) discuss this application in detail.

1.4 Major Challenges

There are several challenges which must be met before VME devices can be fully exploited. These include the following:

a) Operation at Low Voltage

FEDs need to be able to operate at low voltage (~20V), in order that they can be controlled by currently-available integrated circuits.

b) Maximum Emission Currents

The tip should be as robust as possible, in order to prevent regions of the display failing. Therefore, the maximum field emission currents which can be obtained from each tip prior to self-destruction, should be as high as possible.

c) Uniformity from Tip to Tip

Arrays should exhibit uniform characteristics from tip to tip, in order to prevent differences in the levels of brightness across the display. To obtain this uniformity of emission, the tip geometry across the array needs to be as uniform as possible. This is very difficult to achieve.

Fast Transport	Electron transport through a vacuum is much faster than charge carrier transport in any solid (even GaAs or InP), as it is not limited by interactions with the lattice and because power is not dissipated in the vacuum. Therefore, high frequency devices up to 1THz are probably possible. VME devices could replace solid-state devices for certain high frequency applications.
Resistance to Temperature and Radiation	Compared to solid-state semiconductor devices, operation of VME devices is much less affected by temperature or radiation. Useful performance should be possible up to temperatures of 500°C, which is presently impossible for solid-state devices, see Cade & Lee (1990). Also, resistance of these devices to radiation damage is expected to be up to four orders of magnitude higher than for solid state devices, Orvis (1989). Radiation resistance could be useful in aeronautical, space, military and hospital applications.

Table 1.2 Advantages of VME Devices versus Solid-State Devices for Microwave Device Applications

d) Emission Stability

In order for working devices to have reasonable lifetimes, the emitter needs to run for a long time (tens of thousands of hours) without being poisoned by species within the vacuum. Emission fluctuations should be small enough not to limit device performance. In addition, the cathode should be resistant to ion bombardment and reaction with residual gases.

1.5 Aims of Research Described in this Thesis

The overall aim of the research described in this thesis has been to investigate a way of lowering the starting voltage of emitters and increase the tip to tip uniformity. Instead of fashioning a single very sharp emitting point at the apex of each cathode, the cathode itself has been treated in such a way as to cover it with a high density of naturally occurring very sharp asperities. The intention in doing this has been to allow the emission to be controlled by these asperities, rather than by the "macroscopic" apex of the emitter. In order to achieve this, a thin layer of porous silicon (PS) has been formed on the surface of silicon FEAs, using a process called anodisation. PS has a sponge-like or coral-type structure, depending on the anodisation conditions. It is composed of an interconnected network of nanometre scale silicon ligaments enclosing pores. An anodised surface contains a very high density of sharp asperities, each of which could act as a source of field emission.

The effect of anodisation on silicon FEAs was initially investigated during the course of a Part II project (Boswell 1992). Both lower starting voltages and higher maximum currents were observed following anodisation. During that project there was not sufficient time to study the effect in detail, but these early results were promising enough to merit further investigation. In the present work, the capability of the experimental apparatus and specimen preparation techniques first had to be studied and improved versus the Part II studies, in order to improve reproducibility. After these changes had been made, a wider and more detailed study was carried out, and the effect of changing the silicon dopant type and the anodisation parameters was investigated.

The work described in this thesis was the first of its kind to be reported. Since the initial publication of these results, other researchers have also studied field emission from anodised structures. However, their work (discusses in Chapter 2 and Chapter 7) has been limited, and they have not succesfully identified the cause for the improvement in emission characteristics following anodisation.

1.6 - Experimental Techniques

In this work, several experimental techniques were used to study PS:

1) Field emission from silicon FEAs (before and after anodisation) was studied using an adapted scanning electron microscope (SEM).

2) The morphology of silicon emitter tips (before and after anodisation) was studied using transmission electron microscopy (TEM).

3) Field emission from single silicon tips (before and after anodisation) was studied using field emission microscopy (FEM). In conjunction with field ion microscopy (FIM), the source of the improved emission characteristics was also identified.

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Chapter 2 - Field Emission and Vacuum Microelectronics

This chapter is a survey of the field emission literature relevant to the current project. Sections 2.1-2.3 describe the theory of field emission of electrons from metals. Section 2.4 describes how field emission from semiconductors differs versus field emission from metals. Section 2.5 describes the effect which adsorbates have on emission from both metals and semiconductors. Section 2.6 discusses the typical causes of field emission instability, ways in which stability can be improved, and techniques which can be used to protect emitters from premature self-destruction. Section 2.7 briefly describes the manufacturing techniques typically used to lower the operating voltage of vacuum microelectronic (VME) devices. Finally, Section 2.8 outlines further the aims of this thesis and reviews related investigations of field emission from porous silicon reported by other researchers.

2.1 Field Emission from Metals

2.1.1 Potential Energy Diagram

Field emission occurs by tunnelling of electrons through a potential barrier. In vacuum microelectronic (VME) devices, this barrier occurs at the solid/vacuum interface at the tip surface. The height of the barrier at zero applied field is determined by the work function (ϕ). Energy equivalent to ϕ needs to be applied in order for an electron to escape from the top of the Fermi level in the material. The shape of the barrier and its resultant height, when the applied field $F \neq 0$, are dependent on the following:

a) Applied Field (F)

As the field is increased, the barrier to tunnelling is lowered. A force equivalent to -eF will act on the electron, acting to pull it out of the material.

b) Image Force

The image force is a result of the attraction between an escaped electron (situated at a distance x from the surface), and the surface which it has just left. The image force experienced by an electron escaping from a flat metal surface, is given by the following equation:

$$\text{Image Force} = \frac{e^2}{4x^2} \quad \text{(eq.2.1)}$$

where e=charge on an electron; x = distance of electron from the surface (see Gomer (1961)).

Overall, the potential energy of an electron can be described by the following equation (see Figure 2.1):

$$V(x) = E_f + \phi - \frac{e^2}{4x} - eFx \quad \text{for } x > x_c \quad \text{(eq. 2.2)}$$

$$V(x) = 0 \quad \text{for } x < x_c \quad \text{(eq.2.3)}$$

where F=applied field; ϕ=work function; E_f=Fermi energy level.

When the barrier is thin enough, electrons will tunnel through it. This distinguishes field emission from thermionic emission, where electrons must obtain enough thermal energy to hop over a potential barrier. For thermionic emission, temperatures >>1000°C are often required, whereas field emission (sometimes termed "cold" emission) may occur at any temperature.

2.1.2 Equations Governing Field Emission from Metals

Fowler & Nordheim (1928) developed the equation which describes field emission from metals (see also Good & Müller (1956)). The equation was obtained by taking the product of the flux of electrons arriving at the potential barrier and the probability of barrier penetration.

a) Flux of Electrons

To calculate the flux of electrons, N(E,T), arriving at the barrier, Fermi-Dirac statistics were assumed for the energy distribution of electrons in a metal. The total emission current is assumed to be entirely dominated by electrons with energies very close to the Fermi level, E_f.

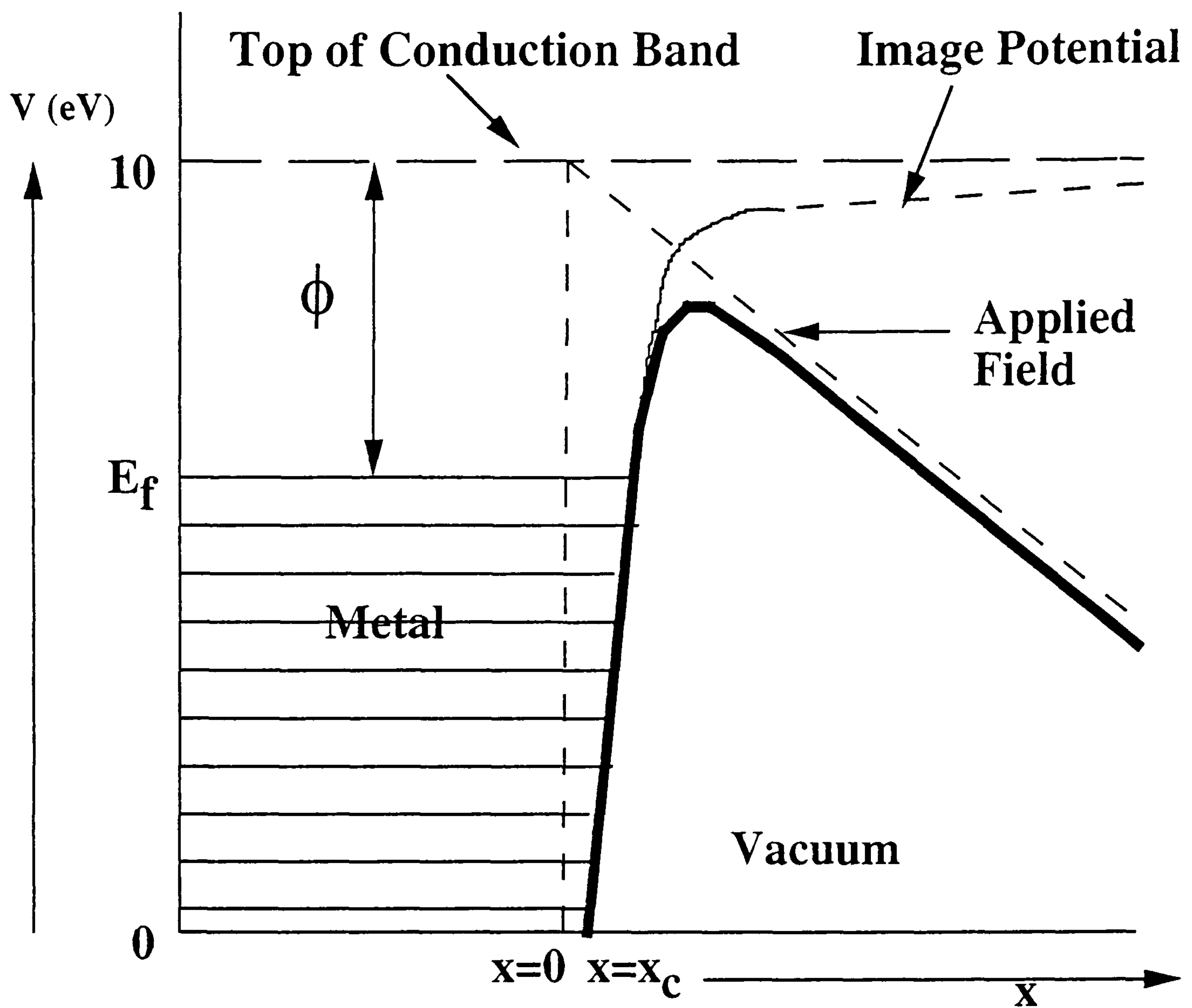


Figure 2.1 - Example of Surface Potential Seen by an Electron in a Field Emission Experiment

Actual potential barrier at a metal surface is determined by the contribution of the applied field and by the image potential.

E_f = Fermi level

ϕ = work function of metal surface

x = distance of electron from metal surface

V = potential energy of electron

x_c = point at which $V(x_c) = 0$

b) Transmission Coefficient

The fraction of electrons penetrating the barrier is defined by the transmission coefficient, D(E,V). The Wentzel-Kramers-Brillouin (WKB) approximation to the Schrödinger equation solution is used.

To calculate the emission current from the flux of electrons and the transmission coefficient, integration is carried out over all electron energies as follows:

$$J(V,T) = e\int_0^{\infty} N(E,T)D(E,V)dE$$

(eq. 2.4)

where N(E,T) = flux of electrons (supply function); D(E,V) = transmission coefficient of electrons through the barrier; e=charge on an electron.

The resulting Fowler-Nordheim (FN) equation relates the current density (J) at a temperature of 0K, to the applied electric field (F) for a metal of work function (ϕ), see Spindt & Brodie (1992). The FN equation is as follows:

$$J(0) = \frac{e^2F^2}{8\pi h\phi t^2(y)} \exp\left[\frac{4(2m)^{\frac{1}{2}}\phi^{\frac{3}{2}}}{3heF} f(y)\right]$$

$$= \frac{A(F)^2}{\phi t^2(y)} \exp\frac{-B\phi^{\frac{3}{2}}f(y)}{F} A/cm^2$$

(eq.2.5)

where: F=applied electric field; $y = (e^3F)^{1/2}/\phi$; $A=1.537x10^{-6}$ and $B=6.83x10^7$; ϕ=work function; e=electron charge; m=electron mass; h=Planck's constant. f(y) and t(y) are the Nordheim elliptic functions and are available as computed values, see Good & Müller (1956). f(y) and t(y) are slowly varying functions of the variable y. Within the range of most experiments, these values are $t^2(y) \sim 1.1$ and $f(y) \sim 0.95-y^2$, see Spindt *et al.* (1976).

2.2 - Extraction of Parameters from Experimental Data Using the Fowler-Nordheim Equation

a) The electric field (F) can be re-written as (see Schroder *et al.* (1974):

$$F=\frac{\beta V}{d} \qquad \text{(eq.2.6)}$$

where V= voltage applied between anode and emitter, d = anode-to-emitter spacing and β = field enhancement factor which is defined as:

$$\beta=\frac{kh}{r} \qquad \text{(eq.2.7)}$$

where h=emitter height, r=tip radius, k=constant depending on tip geometry. k~3 for a typical pyramidal emitter used in VME devices.

b) In addition, the current density (J) can be re-written as:

$$J=\frac{I}{\alpha} \qquad \text{(eq.2.8)}$$

where I=total current obtained from a tip and α=emitting area of tip.

c) The Fowler-Nordheim equation can therefore be re-written as follows:

$$J=\frac{I}{\alpha}=\frac{A(\beta V)^2}{1.1\phi}\exp\left(\frac{-B\phi^{\frac{3}{2}}f(y)}{\beta V}\right) \quad A/cm^2 \qquad \text{(eq.2.9)}$$

This in turn can be re-written to give a more simplified expression for the experimentally measured emission current, as follows:

$$I=J\alpha=aV^2\exp\left(\frac{-b}{V}\right) \qquad \text{(eq. 2.10).}$$

$$\text{where } a=\frac{1.397\text{x}10^{-6}\alpha\beta^2}{\phi}\exp\left(\frac{9.89}{\phi^{\frac{1}{2}}}\right) \qquad \text{(eq.2.11)}$$

$$\text{and } b=\frac{6.488\text{x}10^{7}\phi^{\frac{3}{2}}}{\beta} \qquad \text{(eq.2.12)}$$

Field emission data is usually displayed on a Fowler-Nordheim plot, which is a plot of $\ln\left(\frac{I}{V^2}\right)$ versus $\frac{1}{V}$. The FN equation is therefore rewritten as follows:

$$\ln\left(\frac{I}{V^2}\right) = -\frac{b}{V} + \ln(a) \qquad \text{(eq.2.13)}$$

For the values of electric field typically applied during field emission (10^6-10^7Vcm^{-1}), an FN plot is a straight line with a slope of value -b, and an intercept of ln(a).

2.2.1 Extraction of Work Function From Experimental Data

In principle it should be possible to extract the work function from the slope of the FN plot, using eq. 2.12. However, the Fowler-Nordheim equation contains two unknown variables - ϕ and F. Therefore, one of these variables has to be guessed/estimated in order to find the other variable. As a result, an absolute value for the work function cannot be obtained, as the absolute value of the electric field at the emitter plane cannot be obtained with sufficient accuracy, due to the following reasons:

i) The normally assumed triangular barrier may be incorrect for sharp tips.

ii) Adsorbate atoms/protuberances are likely to be present on the tip surface.

However, if the total energy distribution (TED) from an emitter can be measured (in addition to the field emission I-V characteristics), a more accurate value of ϕ can be obtained. Young (1959) derived the following equation for the TED:

$$J(\varepsilon) = J(0)\exp\frac{\left[\frac{\varepsilon}{d}\right]}{d\left(1+\exp\left[\frac{\varepsilon}{kT}\right]\right)} \qquad \text{(eq. 2.14)}$$

where ε=E-E_f; d= $\frac{0.975F}{\phi^{\frac{1}{2}}t(y)}$; k=Boltzmann's constant; and T=temperature in K.

This relationship contains the same unknowns, but is independent of the Fowler-Nordheim equation. Using both equations will allow ϕ to be calculated.

2.2.2 Extraction of Emitting Area and Field Enhancement Factor from Experimental Data

The emission area (α) and field enhancement factor (β), can be extracted from FN plots, see Stern *et al.* (1929). However, the slope and intercept of the FN plot must first be obtained. If the field emission distribution cannot be obtained, a value for the work function (ϕ) must be assumed. Equation 2.12 can then be used to calculate the value of β, which can be used in equation 2.11 to calculate the emission area (α).

Another method can be used to obtain a more accurate value of the emitting area. This method does not require the work function (ϕ) to be assumed. It uses an additional expression developed by Van Oostrom (1962) and Charbonnier & Martin (1962) (from equations 2.11 and 2.12), as follows:

$$ab^2 = (5.96\text{x}10^9)\alpha\phi^2 \exp\left(\frac{9.89}{\phi^{\frac{1}{2}}}\right) \qquad \text{(eq.2.15)}$$

Within the typical range of work function values (3.4-11.6eV), the value of $\phi^2 \exp\left[\frac{9.89}{\phi^{\frac{1}{2}}}\right]$ can be approximated to 2250. Substituting this value into eqn. 2.15 and using the following equation allows the emitting area to be estimated to ±10%:

$$\alpha = \frac{ab^2}{1.34\text{x}10^{13}}\text{cm}^2 \qquad \text{(eq.2.16)}$$

2.3 Validity of the Fowler-Nordheim Equation for Metals

2.3.1 Blunt Tips (Radii >5nm)

For blunt tips with radii >5nm, the tunnelling electrons essentially see a flat conducting surface (within the distance < 0.5nm, in which the classical image force for a planar surface is appreciable). Therefore a straight line FN plot is obtained within the moderate current regime, see Good & Müller (1956). Young & Müller (1959) used measurements of the energy of field emitted electrons to verify the relationship between current and voltage as

defined by the FN equation. However, they found that the FN equation could not be relied upon for an estimate of the emitted current density. Possible reasons for this include:

a) Emission may have occurred from microprotrusions on the tip surface.

b) Emission may have occurred from tips covered with work-function modifying adsorbates. In addition, adsorbates may modify the degree of transparency of the potential barrier and will therefore affect the transmission coefficient.

c) Space-charge effects (at high current densities only), where emitted electrons screen the tip from the applied field, can affect emission.

2.3.2 Sharp Tips (Radii <5nm)

In the literature, doubt has been cast over the validity of the application of the FN equation to very sharp field emitters. Niedermann *et al.* (1990), have shown that for metal tips subject to high electron fields, emission will occur at fields much lower than predicted by the FN equation, and that the FN plots will not be straight. Cutler *et al.* (1993a) have shown that this is because the FN equation was derived using the planar model for the tunnelling barrier, see Good & Müller (1956). For the planar model, only electrons at the Fermi energy contribute to current. However, newer models predict that for sharp tips, electron emission will occur from up to 2eV below the Fermi level, see Kirkpatrick *et al.* (1992), He *et al.* (1991a&b), Cutler *et al.* (1993b), and Jensen & Zaidman (1994). Therefore, use of the planar model can lead to incorrect estimations of the emission area of a tip.

2.4 Field Emission from Semiconductors versus Metals

The physics of the field emission process from semiconductors is more complicated than for metals. The general features of field emission from semiconductors are described by Gofman *et al.* (1957), Asaro (1958), Fischer (1960 & 62), Gadzuk (1970), Busch & Fischer (1963), Arthur (1965), Gadzuk & Plummer (1973) & Modinos (1967). The main differences versus emission from metals are outlined in the following sections.

2.4.1 Emission from Conduction Band, Valence Band and Surface States

In a semiconductor, emission may occur from several different sources:

a) Emission from Conduction Band

For a semiconductor, the energy required to promote an electron from the bottom of the conduction band to the vacuum level is called the electron affinity χ. For highly doped n-type semiconductors, χ is analogous to the work function (ϕ) of a metal. Figure 2.2 shows the band diagram of a typical n-type semiconductor emitter. At the surface, x=0. x_c is determined by the point at which V(x) = 0 and which typically lies 3-4 atomic layers below the surface, due to re-arrangement of the surface atoms.

In a metal, the Fermi level lies within the conduction band. However, in a semiconductor the Fermi level lies within the band gap and so the conduction band must bend in order for emission to occur. The Fermi level is normally close to the conduction band, see Figure 2.2. When a field is applied, the bottom of the conduction band will dip below the Fermi level. When this occurs, a pool of electrons will collect in this depression, from which emission can occur. This electron pool will screen the field from the rest of the semiconductor. For a p-type emitter, a similar effect is observed. However, a depletion region will also form next to the surface pool of electrons. This is demonstrated in Figure 2.3, see Baskin *et al.* (1971).

b) Emission from Valence Band

If the field is high enough, tunnelling can also occur from the top of the valence band. The effective work function in this case will be higher than for emission from the conduction band. It will be given by the following equation:

$$\chi_{valence} = \chi + E_g \qquad \text{(eq. 2.17)}$$

where χ = electron affinity for emission from the bottom of the conduction band; and E_g = band gap. It should be noted that as the field will be higher than normal, the image force term will also have changed.

c) Emission from Surface States

Field emission can also occur from ionized surface states. Surface states will trap electrons when an external electric field is applied. Electrons are expelled into the vacuum from these states. The energy levels of surface states lie within the band gap, see Baskin *et al.* (1977).

Evidence of emission from all three sources has been observed by studying field emission distributions obtained from semiconductors.

2.4.2 Internal Voltage Drop and Current Saturation

So far, it has been assumed that the position of the Fermi level remains constant (zero current approximation). However, if current is emitted from p-type semiconductors, the position of the Fermi level will change. This effect causes p-type semiconductors to exhibit non-linear Fowler-Nordheim plots, see Figure 2.4. This behaviour has been studied in detail by many researchers, see Apker & Taft (1952), Arthur (1965), Neumann (1968), Fursey & Egorov (1969), Baskin *et al.* (1972), Baskin *et al.* (1977), and Schroder *et al.* (1974).

It has been found that FN plots obtained from p-type semiconductors exhibit four distinct stages, as described in the following sections:

a) Region I

At low fields, the Fowler-Nordheim equation is obeyed. There is a sufficient concentration of electrons in the conduction band, and the emission current is limited only by the probability of electron tunnelling at the surface.

b) Region II

At a particular value of applied field, the electron concentration in the surface inversion layer drops abruptly. Field penetration causes a depletion region to expand into the semiconductor. This causes the current to be limited by the electron supply, rather than by the transparency of the barrier. Within this region, the current will be almost independent of the applied voltage. The following also applies:

- The value of the current in the saturation region will depend strongly on changes which affect the density of free carriers (i.e. conductivity). Figure 2.5 shows that as the temperature and illumination are increased, the saturation current will increase and the length of the saturation region will decrease. In the saturation region, current is generated at the surface, rather than in the bulk, see Schroder *et al.* (1974) and Arthur (1965). Therefore, treatments affecting the surface concentration of electrons will affect the emission current. The effect that different treatments have on emission are summarised in Table 2.1.

- For metals, the field enhancement (β) depends only on the geometry of the emitter and is independent of the applied voltage. However, for semiconductors undergoing current saturation, the tip surface is no longer an equi-potential surface. Schroder *et al.* (1974) found that during current saturation, β is much lower and is very insensitive to tip radius. This causes the current to increase at a much slower rate than previously. The field emission image steadily contracts as the applied voltage is increased, due to contraction of the Fermi level. The degree to which β is reduced can be measured by measuring the relative changes in the dimensions of the field emission pattern, before and after field penetration, see Fursey & Egorov (1969).

Arguments still exist within the literature, as to whether silicon emitters actually do undergo saturation. For example, Gray *et al.* (1986) and Makhov (1989) reported that silicon emitters undergo saturation at a few microamperes; whereas Marcus *et al.* (1990) could not obtain saturation even at 20μA. The difference in these results are most likely due to:

i) Differences in the cleanliness of different samples.

ii) Differences in temperature/illumination between samples

iii) Differences in geometry/cone angle between samples

iv) Differences in the doping levels between samples

vi) Difference in the impurity levels between samples.

Emission Region	Treatment	Effect
Region II - Plateau Region	1) Temperature	Baskin *et al.* (1971) showed that the saturation current (j^{lim}) for a p-type emitter depends on temperature according to the following equation, where ε_g = band gap: $\frac{d(\ln j^{lim.})}{d(1/kT)} \approx -\frac{\varepsilon_g}{2}$
	2) Illumination	Current in plateau region increases with illumination.
	3) Substrate Doping	The higher the substrate resistivity, the longer the current plateau.
	4) Treatments affecting bulk concentration of electrons.	Such treatments have little effect on the current in the plateau region.
	5) Treatments affecting surface concentration of electrons:	Such treatments have a pronounced effect on emission, see Fursey & Ivanov (1967), Fursey & Egorov (1969) and Lewis & Fischer (1974).
	- Baking at 300°C (in vacuum).	The current was found to be two orders of magnitude higher following this treatment (see above).
	- Heating above 450°C (in (vacuum).	After this treatment, emission was no longer light sensitive. This effect is believed to be due to irreversible surface changes along the shank of the emitter, as the original behaviour could be restored by removal of <10nm of the emitter surface using an HF-HNO_3 etch. This was probably due to inward diffusion of impurities during heating, producing a surface "channel" layer along the emitter shank. Such a layer could increase the surface leakage current and could provide defect centres which could initiate breakdown, Chynoweth & Pearson (1958).
	- HF Dipping	Emitters not treated with HF exhibited linear FN plots, Sawada *et al.* (1994); whereas emitters treated with HF exhibited current saturation. This difference is attributed to a difference in the concentration of surface states, which prior to HF dipping would have screened the emitter and prevented current saturation. Higher current values were obtained from the tips which had not been cleaned with HF.
Region III Avalanche - Breakdown	1) Temperature	Current still sensitive to temperature, Arthur (1965).
	2) Illumination	Current still sensitive to illumination, Arthur (1965).
	3) Substrate Doping	Critical field for avalanche breakdown increases with increasing impurity content, see Grove (1967) and Thomas & Nathanson (1972).
	4) Thermal treatments	Critical field considerably reduced for tips heated between 500K - 700K due to formation of conductive surface layer, Arthur (1965).

Table 2.1 Treatments Affecting Current Obtained from P-Type Silicon During Stage II and Stage III emission

c) Region III

As the field is increased, a point will be reached where the current will rise sharply, due to carrier multiplication produced by avalanching in the depletion region. At this point, the surface charge will increase and β will increase in value. Energy distributions obtained from tips operating in this region are very broad, suggesting that heating (by inelastic scattering) of electrons by up to several eV occurs.

d) Region IV

With further increases in applied voltage, the rapidly increasing current will again be limited by the probability of electron tunnelling.

2.4.3 Adaption of Fowler-Nordheim Equation for Semiconductors

Stratton (1955, 1962 and 1964) derived equations for field emission from silicon, taking into account contributions from the valence band, surface states and the conduction band. However, this calculation was based on the zero current approximation, which is not correct for most values of applied field. Since then, Baskin *et al.* (1971), Jensen & Ganguly (1993), and Jensen & Ganguly (1995) have derived equations which do not assume the zero current approximation. Their models correctly predict the occurrence of the current saturation effects described in Section 2.42.

2.5 Effect of Adsorbate Layers on Emission from Semiconductors and Metals

It is important to consider the effect of adsorbates on field emission from semiconductors and metals. Adsorbates cannot be easily removed from the surfaces of most working FEA devices. Even if this were possible, UHV conditions cannot be maintained in packaged devices and so re-contamination is likely to occur. Adsorbates can influence emission in the following ways:

a) Increase in Work Function

Adsorbates affect the work function (ϕ) of emitters - ϕ can increase due to polarisation of the adsorbate by the applied field (F). The field causes an induced dipole αF, where α=polarizability of the adsorbate. The electron affinity then becomes:

$$\chi_{ad} = \chi + \lambda F \qquad \text{(eq. 2.18)}$$

λ = factor containing the polarizability and adsorbate coverage; χ = electron affinity of clean surface.

An example is described by Spindt *et al.* (1991), who found that when the operating pressure for metal tips was increased from 10^{-9} torr to 10^{-5} torr, the emission current dropped drastically to a value ~20 times lower than at 10^{-9} torr, see Figure 2.6. This is thought to be due to adsorption of gas molecules. However, emission was restored after the pressure was reduced back to 10^{-9} torr. The restoration of emission is thought to have been due to desorption of the adsorbates which caused the initial increase in work function. Busta (1992) describes similar results for silicon tips.

b) Tunnelling Resonance for Thin Layers

Adsorbates act as discrete atomic potentials lying outside the emitter, see Duke & Alferieff (1967), Gadzuk (1970), Modinos (1970), Johnston (1991), and Yang *et al.* (1991). They can cause a perturbation of the tunnelling electrons by wave-mechanical interference effects. At certain adsorbate layer thicknesses, a resonance effect will occur. In this case, the emission current will be higher than if no adsorbate were present. The electronic levels of the adsorbate lying within the conduction band or valence band can provide windows of enhanced electron tunnelling, which appear as additional peaks in the field emission distribution. Figure 2.7 demonstrates resonant tunnelling using an energy band diagram. However, anti-resonance effects can also be observed, dependng on the adsorbate thickness. In such cases, the probability of barrier transmission will drop and the emission current will decrease. The effects of resonance and anti-resonance will be most pronounced on smooth tips.

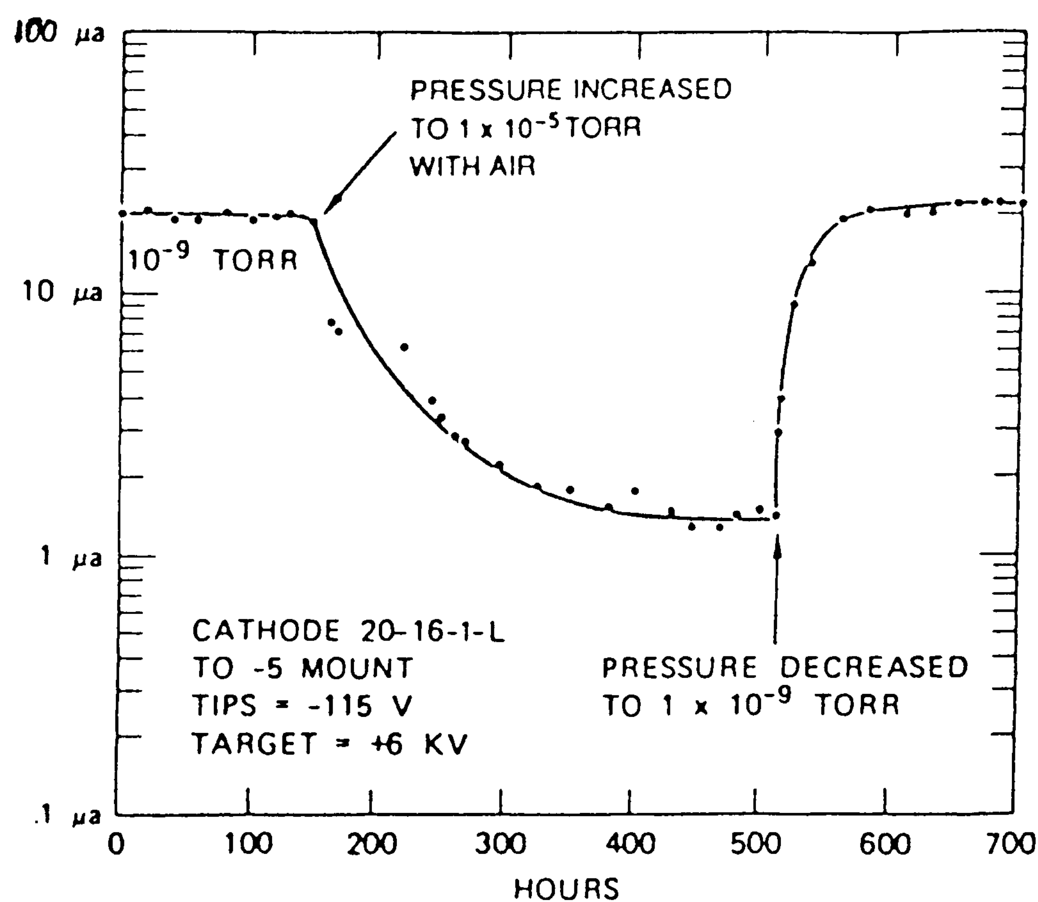
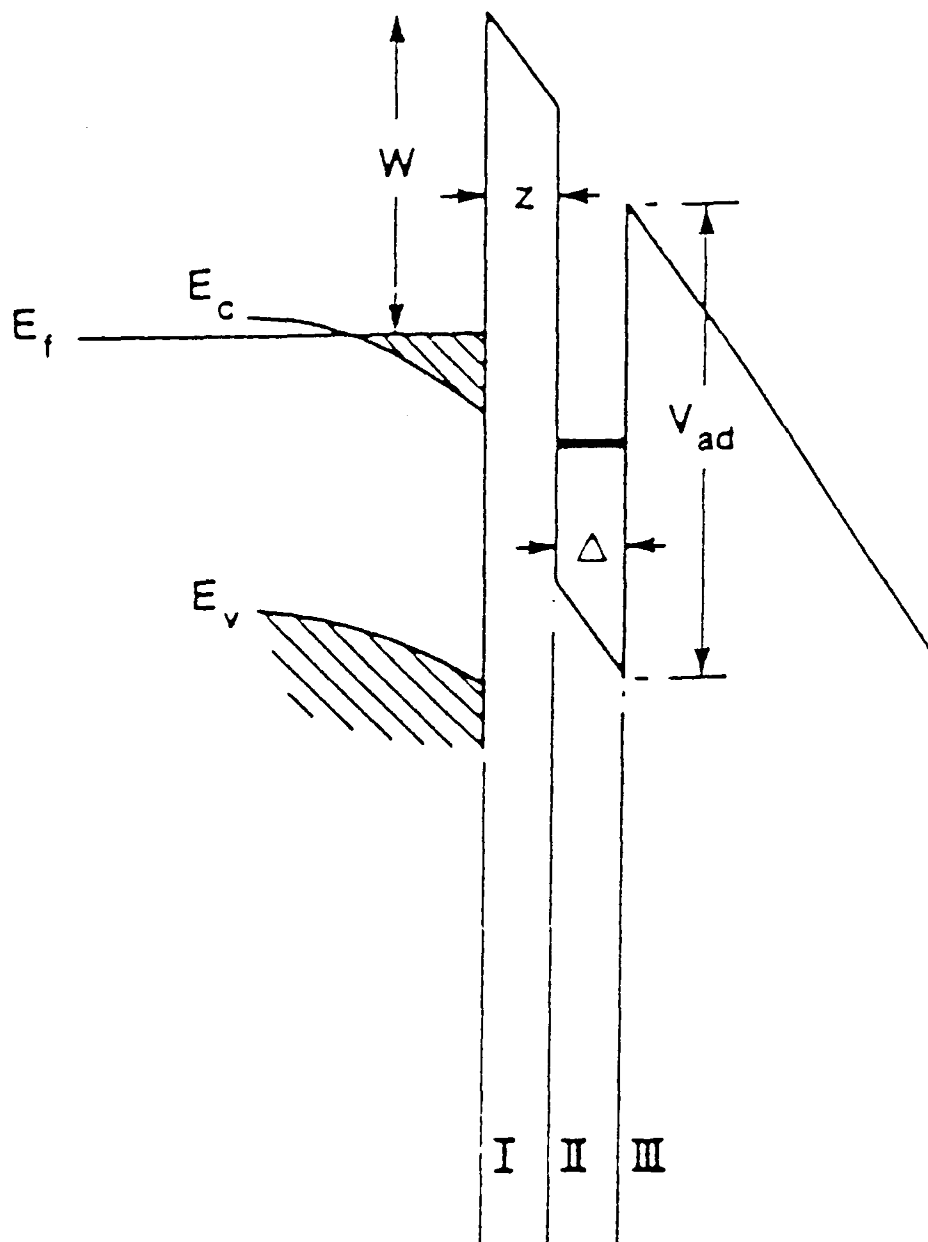


Figure 2.6 - Diagram Showing Effect of Pressure on Emission from Metal Tips

This graph shows the emission current obtained from a molybdenum emitter when the operating pressure was increased from 10^{-9} torr to 10^{-5} torr. The emission current dropped drastically (by almost 20-fold) over several hundred hours, but was restored quickly after the pressure was reduced back to 10^{-9} torr. The initial decrease in current is thought to have been due to adsorption of gas molecules.

(Ref: C.A.Spindt, C.E.Holland, A.Rosengreen and I.Brodie, *IEEE Trans. Electron Devices*, **ED-38** (1991), 2355)



(Ref: R.Johnston, *J. Phys.: Condens. Matter.*, **3** (1991), S187)

Figure 2.7 - Field Emission from Silicon Through an Adsorbate Layer
This figure shows the surface band structure and tunnelling potential for an adsorbate monolayer on silicon. The well of depth V_{ad}, at a distance z from the surface, models the potential due to the adsorbate layer. The width of the adsorbate is Δ.The field in the regions I, II and III can have three independent values. Band bending gives an effective work function of W.

If the energy level in the well is aligned with one of the substrate bands, resonant tunnelling to the vacuum will occur. The energy level in the well is determined by the properties of the atomic species and the surface, but also by the high fields and current densities involved in field emission. This enhanced tunnelling appears as additional peaks in the field emission distribution.

2.6 Emission Stability and Lifetimes

2.6.1 Emission Noise

Instability is defined as the current fluctuation divided by the average current within a certain time period. Emission instability needs to be reduced as far as possible for operating devices. Recent studies of noise/emission stability have been reported by Spindt (1976), Kirton & Urens (1989), Brodie (1989), Bakhtizin *et al.* (1991), Bakhtizin *et al.* (1993), Tringedes *et al.* (1993), Busta *et al.* (1994), Bintz & McGruer (1994), Py & Baptist (1994) and Li *et al.* (1996). In general, instability can be divided into five main components described in the following sections. These components are superimposed to give the total instability.

a) Surface Diffusion

Diffusion of adsorbates and "loose" substrate atoms across surfaces will cause fluctuations in the emission current. Current fluctuations are directly related to the diffusion coefficients of species and to tip temperature. Surface migration is particularly important for more weakly bonded adsorbates such as molecular H_2O.

b) Pulse Instability

Pulse instability is likely to be due to arc discharge. This type of noise consists of pulses ~ 10^{-9}-10^{-6} seconds in duration. The height of these pulses is approximately the same as for the average current. Arc discharges have enough energy to destroy emitting tips, see Browning *et al.* (1992) and McGruer *et al.* (1993). Arc discharge can be caused by:

i) A high gas concentration near the highest voltage point on a tip. This may be due to the presence of residual gas in the vacuum chamber, or to the field enhanced evaporation of contamination. Meassick *et al.* (1994) show that failure rates due to arc discharge, increase exponentially with emission current and pressure, Zeitoun-Fakiris & Juttner (1991).

ii) An imbalance between the surface tension force and the Taylor electric force, can change the radius of emitting tips. This imbalance can make the tip smaller and smaller until arc discharge occurs. (This only occurs if high tip temperature permits surface diffusion.)

c) Bistable

Bistable pulses are due to dipole switching of chemisorbed impurities on the silicon surface, see Busta (1994) and Greene & Daneshvar (1994). The height of bistable pulses are ~1 tenth of the average current and last only a few seconds. Migration of bulk impurities to the surface and migration of surface impurities (such as oxide) can increase the occurrence of bi-stable pulses.

d) Wavy

Wavy noise is probably due to a periodical change in either work function or tip geometry, due to slow changes in adsorption, desorption, diffusion and migration of impurities and tip heating. This type of instability occurs over a period of several minutes and represents a gentle change in emission current with time.

e) Unidirectional

Unidirectional noise can be positive (i.e. causes current increase) or negative (i.e. causes current decrease). The tip forming process is positive and will cause tip sharpening, and hence a gradual increase in emission current, see Busta (1994). Again, this is due to a balance of the Taylor force and surface tension force. This type of instability causes change over a few hours or days and is a measure of long-term stability. Negative processes can be caused by slight contamination of the vacuum system. In the worst cases, emission current will totally disappear and in order to regain emission, the voltage would have to be increased, see Li *et al.* (1996).

2.6.2 Improvement in Emission Stability

a) Reduction in Pressure Level

From the previous sections it is clear that if the pressure of the operating vacuum could be reduced, the level of noise observed would be reduced. For pressures of ~10^{-8} torr, Busta *et al.* (1994) found that current fluctuations lay in the range 20-200%.

b) Removal of Adsorbates from Emission Surfaces

From the previous sections, it is also clear that removing contamination should also decrease the level of noise observed. There are several methods to achieve this:

i) HF Dipping - Contamination can be removed from the surface of silicon samples by using an HF dip (5% solution). However, although this treatment may remove gross oxide contamination, the resulting surface may still not be completely clean silicon. Johnston & Miller (1992) have shown this by studying field emission distributions (FEDs) obtained from samples before and after HF treatment, see Figure 2.8.

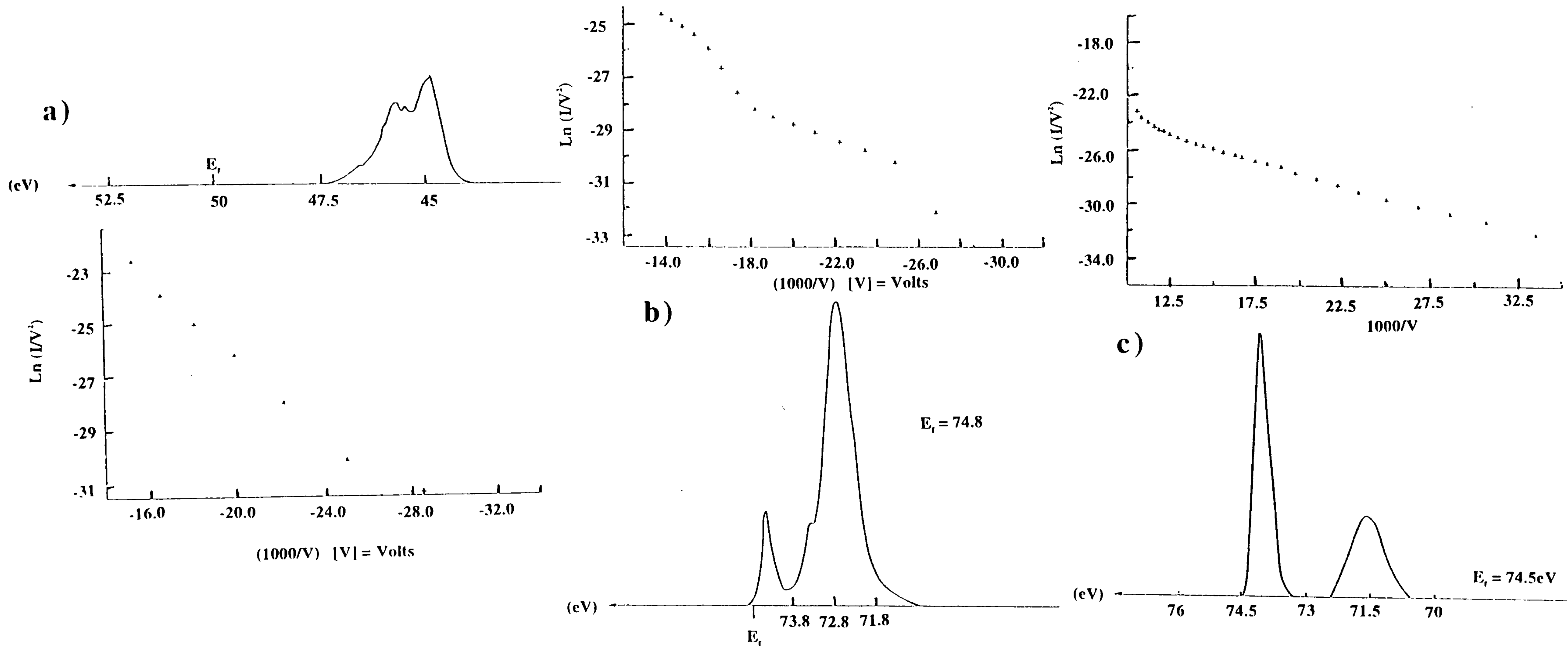
ii) Argon Ion Bombardment - Johnston & Miller (1992) also investigated the effect of low-energy (500eV) argon ion bombardment, in-situ within UHV apparatus. Ion bombardment gave atomic cleanliness, but cleaning tips in this way caused blunting of the emitter tip.

iii) Hydrogen Plasmas - A hydrogen plasma operates by bombarding the emitter surface with hydrogen ions. This technique has been used to clean the surface of molybdenum emitters, see Schwoebel & Spindt (1993a,b), Sokolich *et al.* (1993) and Itoh (1993). These ions 'knock off' adsorbate atoms. However, because hydrogen ions are very light, they do not alter the surface morphology of the emitter (unlike argon ion bombardment).

iv) Heating - In some systems, oxygen/oxides can be desorbed below the melting point of the emitter (e.g. tungsten), see Dyke & Dolan (1956). However, for some materials, this may not be possible.

2.6.3 Tip Protection

Typically, field emitters fail due to sudden increases in current, which cause the tip to over-heat and self-destruct. Such problems are particularly acute when the vacuum conditions are poor. However, emitters (either individual tips or an array of tips) can be protected from sudden current bursts by using a series resistor. Any sudden increase in current, will cause an increase in voltage to occur. However, if a resistor is placed in series with an emitter, the



(Ref: R.Johnston and A.J.Miller, *Surface Science*, **266** (1992), 155)

Figure 2.8 - Effect of HF Cleaning and Ion Bombardment on Emission from Silicon Tips
a) This shows the field emission energy spectrum and Fowler-Nordheim plot from an untreated silicon emitter.
b) Fowler-Nordheim plot and field emission energy spectrum from a tip on which chemical cleaning with HF has not been successful - not all the oxide layer has been removed. The spectrum shows two peaks - one near the Fermi level and one ~1eV below the Fermi level.
c) Fowler-Nordheim plot and field emission energy spectrum from tip b) on which ion bombardment has been carried out. The emission peak at the Fermi level is now much stronger than at lower energy, indicating that the tip is cleaner. The thickness of the oxide layer has been reduced, but the spectrum is still not characteristic of a clean tip. The position of the peaks is consistent with emission from the valence and conduction bands - low energy band emission is enhanced by contamination. Further ion bombardment would be required to obtain a clean spectrum.

voltage will be dropped across the resistor rather than across the emitter. Values of resistors typically used are in the tens of megaohms range.

For FEAs, an alternative to using a series resistor is to include a resistive layer at the base of the emitters. Resistive layers have been used in flat panel displays designed by LETI, see Baptist (1993), Borel *et al.* (1990), Meyer (1993) and Levine *et al.* (1995). A diagram of an FEA with a resistive layer is shown in Figure 2.9. Testing at LETI has shown that if no resistive layer was used during operation, 1-10% of tips underwent self-destruction. However, if a resistive layer was incorporated into the FEA, zero tips underwent self-destruction during operation, see Levine (1996).

LETI found that tips protected by lateral resistors were extremely robust. Even after exposure to air, a high voltage could be applied to such FEAs (without carrying out bake-out), without causing them to self-destruct. However, for FEAs not protected by a resistive layer, a very slow and gradual increase in grid voltage was necessary to activate them, in order to prevent destructive arcs occurring.

2.7 Techniques to Reduce Operating Voltage of VME Devices

SiO_2 breakdown occurs at ~$4x10^6$ V/cm and Si_3N_4 breakdown occurs at ~10^7 V/cm (see Spindt (1991)). To allow compatibility with other electronic components, and to prevent breakdown of the gate insulation the operating voltage of FEAs should be kept in the range 10-50V. However, in order to achieve field emission, the local field at the tip must lie within the range 10^7-10^8 V/cm. Starting voltages can be reduced by either:

1) Designing FEAs so that the local field at the tip is as high as possible.

2) Constructing emitters from materials having low work functions.

2.7.1 Techniques to Increase Field at Emitter Tip

a) Decreasing the Emitter-Anode separation

Decreasing the emitter-anode separation will increase the local field at the emitter tip. Hence the operating voltage required to obtain a particular current could be reduced. The emitter-

anode separation depends on the limits of microelectronic fabrication. Recent advances in gating technology have allowed this separation to be decreased down to sub-micron levels. Bozler *et al.* (1994) reported gate-to-tip separations of ~0.08μm and tip to tip separations of ~0.32μm. This produced a current of ~1nA per tip at a gate voltage of 25V. Although these researchers obtained a low starting voltage, costly lithography processes were required to reduce the dimensions of the FEA. Prior to that, gate-tip spacings were typically ~0.4μm or greater.

b) Increasing the Field Enhancement Factor of Tips

Following Equation 2.7, the aim in manufacturing devices has been to increase the value of β, by increasing the tip height and decreasing the tip radius.

i) Improving Tip Geometry - Typical manufacturing techniques used to produce FEAs result in the formation of cone/pyramid-shaped tips. However, some researchers have formed unusual geometries in an attempt to increase β. For example, Yadon *et al.* (1995) formed tips having higher aspect ratios than the typical cone/pyramid geometry, by forming columns 0.7μm in height and 0.4μm in diameter with a pyramidal-shaped cone at the top.

ii) Tip Sharpening - Tip sharpening can be carried out once FEAs have been produced, in order to reduce the starting voltage further. Techniques to sharpen tips (and also to improve tip-to-tip emission uniformity) include oxidation sharpening, see Marcus *et al.* (1990); ion bombardment, see Schwoebel & Spindt (1993a); and tip forming. Oxidation sharpening is the most widely used technique for sharpening silicon FEAs, although in some cases a high temperature oxidation step may not be possible. Ion bombardment and tip forming are less controllable than oxidation sharpening and are difficult to apply gated FEAs, as they could damage the device.

2.7.2 Techniques to Decrease Emitter Work Function

In order to lower the operating voltage by a factor of ten or more, surfaces with work functions in the range 1-3 eV must be used. Layers of highly electropositive materials (e.g.

barium, thorium and caesium, immobilised by electronegative species e.g. oxygen or fluorine) have been adsorbed onto tips, see Sanford *et al.* (1989), Macauley *et al.* (1992), Bozler (1994), Santos & MacDonald (1993) and Macauley (1993). Unfortunately, most low work function materials are highly chemically reactive and must to be prepared in the vacuum in which they will be operating. In addition, this vacuum must be devoid of chemically reactive species. To date, the lifetime of such coated devices is reported to be very short, even under UHV conditions. This is thought to be due to poisoning of the low work function layer, which occurs relatively quickly.

Recently, much work has been reported on field emission from diamond FEAs (typically produced by chemical vapour deposition (CVD)). Diamond is a negative electron affinity material. For such materials, electrons in the conduction band will be emitted at very low voltage. However, only n-type diamond should behave in this manner. This is because p-type diamond should not have electrons in the conduction band, as the Fermi level for this material lies ~5eV below the vacuum level (band gap of diamond is very large being ~5.5eV). Unfortunately, whereas p-type doped diamond is relatively easy to produce, there is currently no effective method by which to dope n-type diamond. Curiously, low emission voltages and high current densities have been observed from both undoped and p-type doped diamond films, see Wang *et al.* (1991), Xu *et al.* (1993), Liu *et al.* (1994), Hong & Aslam (1995) and Zhu *et al.* (1996). The mechanism of emission is not understood. It is possible that defect states in sufficient concentrations can form bands with energy gaps close to the conduction band edge, see Cutler *et al.* (1996). It is thought that hydrogen-termination of surfaces may enhance emission from diamond.

2.8 Thesis Aims - Field Emission from Porous Silicon

2.8.1 Background

As outlined in Chapter 1, in this thesis a different approach has been taken in order to lower the starting voltage and increase the uniformity of emission from silicon FEAs. Anodisation has been carried out in order to form a high density of sharp emission sites at the apex of each tip within an array. The intention in doing this has been that emission should be

controlled by these asperities, rather than by the underlying apex. Therefore, emission should occur at lower voltages without the need for additional treatments, such as oxidation.

The original idea for anodising emitters came from examining a schematic diagram of porous silicon published by Canham *et al.* (1992), see Figure 2.10. In this diagram, the PS fibrils were found to be very similar in geometry and shape to the "ideal" field emitter suggested by Utsumi (1991), see Figure 2.11. In this work, it was decided to investigate emission from anodised tips, rather than from anodised flat substrates. This was because field screening would be expected to occur between neighbouring fibrils on a flat substrate. Initial tests confirmed that emission could not be obtained from a flat anodised silicon substrate.

2.8.2 Previous Research from Flat Porous Silicon Layers

However, researchers at Texas A&M University investigated emission from oxidised anodised flat substrates (p^+ type and n-type), see Yue *et al.* (1990), Smith *et al.* (1993) and Pang *et al.* (1993). These samples had been vacuum baked at 135°C for 30 minutes and subsequently oxidised at 900°C for 15 minutes in dry oxygen. By evaporating a metal layer on top of the oxidised layer (to act as a gate), a sustained diode current of ~$20 Acm^{-2}$ was collected using a bias voltage of ~10V. A diagram of their device is shown in Figure 2.12. The authors claim that the oxidation treatment insulated the metal layer from the underlying bulk silicon. However, it seems probable that electrical breakdown could have occurred and that the reported low voltage "emission" may have been a result of leakage through the oxide layer. Assuming that true field emission did occur, the authors suggest two reasons for why emission was obtained at low voltage:

i) Extremely sharp tips were formed at the PS/bulk silicon interface. The researchers believe that these points emitted electrons at very low voltages.

ii) Emission could have occurred from sharp PS fibrils.

Although the authors present SEM images of the surface in plan-view, they do not present any cross-sectional SEM/TEM studies of the PS/bulk interface. Therefore, there is no evidence to show that there were sharp points on the interface, which were a potential source of low-voltage emission. The authors do not present any data to show that emission did not occur from the surface fibrils, which seems a more obvious source of emission than from the rough interface. Also, very few samples appear to have been examined and little attempt has been made to investigate the relationship between the pore morphology, PS layer thickness and field emission properties.

2.8.3 Emission from Anodised Emitters

Although other researchers had previously investigated the effect of micro-protrusions formed on tips, e.g. Atlan *et al.* (1992) and Binh & Garcia (1992), anodisation of emitter tips had not been investigated. Anodisation is a simple way to form a high density of sharp points at the emitter surface. The work described in this thesis was the first to investigate emission from anodised emitters. However, since the start of the work for this thesis, some researchers have also reported studies of anodised emitters (both gated and ungated). In Chapter 7, the results reported by other researchers is summarised in detail and compared to the results reported in this thesis.

2.8.4 Aims of Thesis in Relation to Work Reported by Other Researchers

There are several shortcomings in the work reported by other researchers. As work for this thesis has progressed, investigation has therefore been aimed at:

1) Thoroughly investigating the effect which anodisation has on the field emission properties of silicon FEAs. Other researchers have only investigated a very small number of samples and most have not properly compared emission before and after anodisation.

2) Optimisation of the field emission properties by changing the PS layer thickness and initial substrate doping. Little attempt at this has been reported by other researchers.

3) Investigation of the actual morphology of the anodised tip surface using transmission electron microscopy (TEM), and relation of the PS morphology to the field emission properties. Other researchers who have investigated emission from anodised tips have not published any studies of the morphology of the anodised tip.

4) Identify the true source of field emission and the cause for the decrease in starting voltage, following anodisation. Other researchers have stated that the operating voltage was reduced due to either an increase in field enhancement or a decrease in work function. However, they have not proved that either caused the reduction in starting voltage, and they have not shown whether emission occurred from the sharp interface or the surface fibrils. Field emission and field ion microscope studies

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Chapter 3 - Background to Porous Silicon

3.1 Introduction

As outlined previously, the aim of this work has been to improve the field emission properties of silicon emitters, by forming a high density of asperities at their apex. This aim has been achieved by anodisation, an electrochemical etching process by which a layer of porous silicon (PS) is formed at the surface of bulk silicon. During this process, material is selectively removed from bulk silicon to form a sponge-like silicon structure. PS structures were first reported by Uhlir (1956) and then Turner (1958). However, most extensive research into PS has occurred within the last few years. In particular, research has been aimed at understanding the ability of certain types of PS to photoluminesce efficiently at room temperature.

This chapter describes the following:

1) The electrochemical anodisation process used to produce PS.
2) How experimental variables of anodisation process affect the PS morphology.
3) The electrical and electronic properties of PS layers.

3.2 Electrochemical Anodisation

3.2.1 Electrochemistry

In order to anodised a silicon wafer, it must be made the anode of a cell filled with electrolyte (usually an HF/ethanol solution). During anodisation, holes at the silicon/electrolyte interface weaken the Si-Si bonds, allowing them to be attacked by F^- ions. Hydrogen gas is evolved from the silicon surface during this reaction. Ethanol in the electrolyte reduces the surface tension, allowing H_2 gas to escape from the surface, thereby improving the homogeneity of the resulting layer, see Bomchil *et al.* (1984).

The electrochemistry of anodisation is described in detail by Uhlir (1956), Turner (1958), Memming & Swandt (1966), Unagami (1980), Zhang *et al.* (1989) and Gaspard *et al.*

(1989). Exact details of the fabrication process used in this work, and the problems associated with it, are outlined in Chapter 6.

3.2.2 Importance of Holes to Anodisation Process

A large concentration of holes must be available in order for the anodisation reaction to occur, see Lehmann & Gosele (1990). If a silicon atom is removed from an atomically flat surface by the interfacial reaction, an atomic size dip remains. A large number of these dips is naturally formed across the semiconductor surface, due to the presence of either surface defects or impurities. These dips change the electric field distribution, so that hole (h^+) transfer occurs preferentially at such locations. A series of hole-rich and hole-depleted regions are thus formed across the semiconductor surface. Hole-rich regions are eaten away to form pores, leaving behind hole-depleted silicon wires. Anodisation of p-type silicon can be carried out without illumination, as holes are the majority carriers. However, in n-type silicon, holes are the minority carriers. Therefore, n-type silicon requires illumination in order to generate sufficient concentrations of holes, see Searson & Macauley (1992).

3.2.3 Anodisation Under Non-Standard Conditions

PS can also be formed using non-HF-based electrolytes, see Jung *et al.* (1993). In addition, semiconductors other than silicon, e.g. gallium arsenide, may be anodised. Beale *et al.* (1985) believe that a porous film can be formed if the following conditions are satisfied:

i) The material is a semiconductor, so that depletion widths have suitable dimensions.
ii) Fermi level of semiconductor is pinned mid-gap at the semiconductor-electrolyte interface.
iii) Electrolyte attacks the semiconductor only when a current is passed.
iv) Electrochemical reaction products are soluble in electrolyte.
v) Electrolyte is capable of carrying required current density.

Stain etching can also cause the formation of PS, without the application of a current. However, this process is very slow. Stain etching occurs when an HF-HNO_3 electrolyte is

dropped on to a silicon surface, see K.H.Beckmann (1965), Kidder *et al.* (1992) and Steckl *et al.* (1993).

3.2.4 Current-Voltage Plots

A typical current-voltage plot taken during anodisation is shown in Figure 3.1a. Below point A (which depends on the substrate type), selective dissolution occurs and PS is formed. Increasing the current past point A leads to electropolishing. If the HF concentration is very high, this transition point is not so well defined and the region of pore formation can be extended to higher current densities, without electropolishing occurring, see Figure 3.1b.

3.3. Effect of Variables on PS Morphology

Many different experimental techniques have been used in the literature to study the dependence of PS morphology on several variables. These techniques and the information which they supply are summarised in Table 3.1.

3.3.1 Dependence of Morphology on Substrate Type & Doping

The way in which pores grow is highly dependent on substrate doping, see Beale *et al.* (1985) and Searson *et al.* (1992). Three main types of PS structure are obtained from different silicon substrates:

i) Microporous PS with pore widths 3-10nm

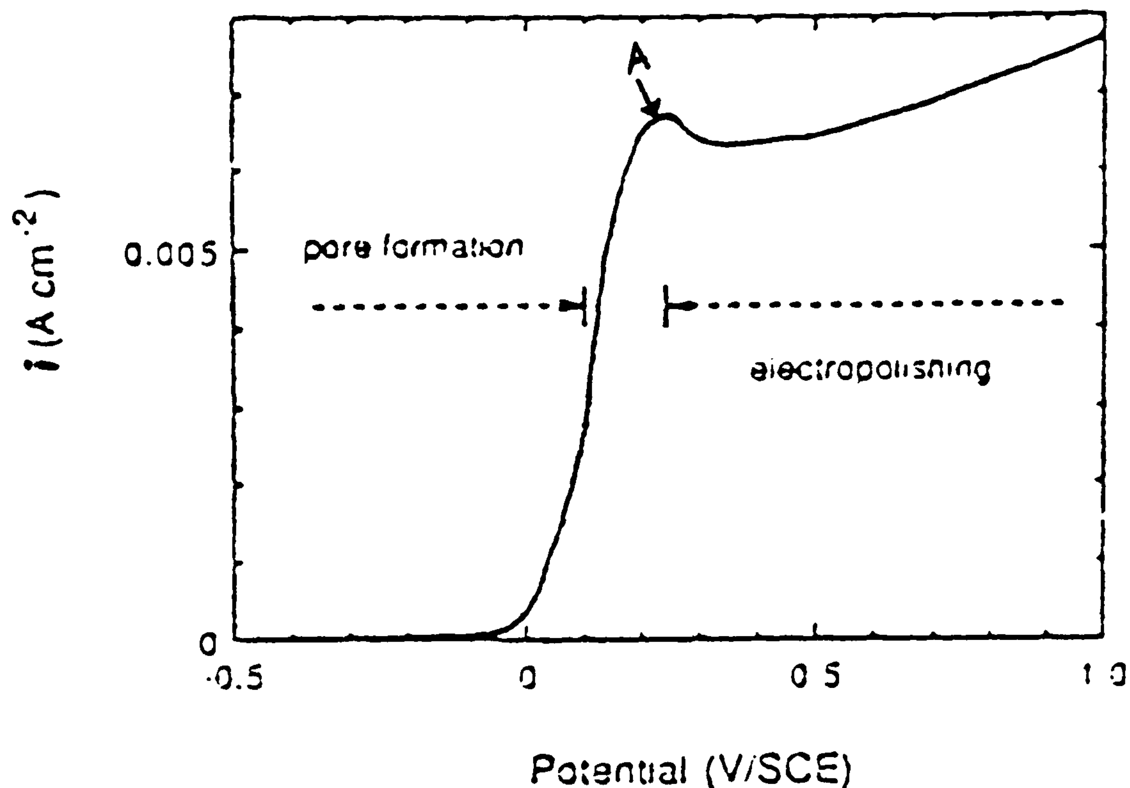
ii) Mesoporous PS with pore size 10-100nm

iii)Macroporous PS with pore size 100-1000nm

The schematic diagram in Figure 3.2 demonstrates these three types of structure in n, p and p^+-type silicon.

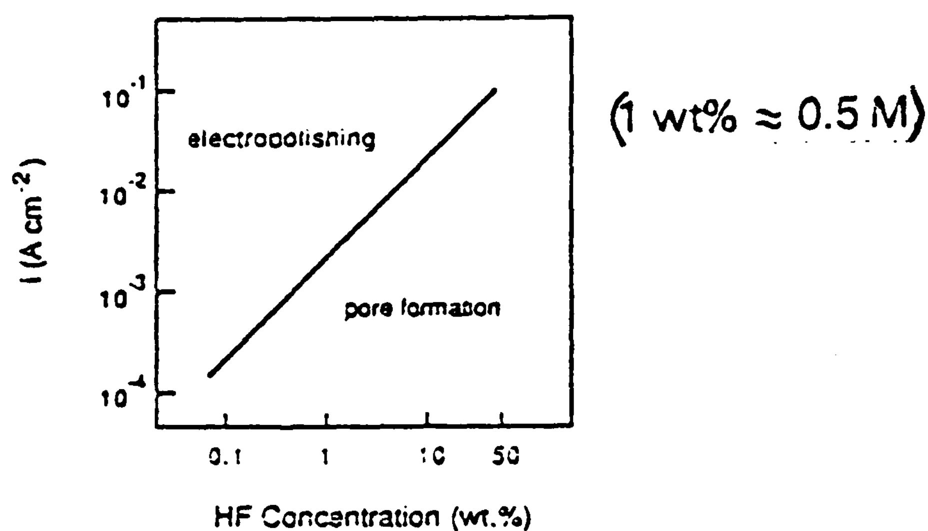
a) P-Type Porous Silicon (Non-degenerate) - Microporous

Beale *et al.* (1985) found that all nondegenerate p-type PS exhibits a pore structure which is non-directional, consisting of random but interconnected voids. The type of morphology is microporous, and the porosity of these films lies in the range 40-60%.



a) Plot of Current versus Voltage During Anodisation

If the voltage is lower in value than at point A, selective dissolution occurs and porous silicon is formed. However, if the voltage is increased past the value at point A, electropolishing will occur.



b) Plot of Current versus HF Concentration

This plot shows that if the HF concentration of the electrolyte is very high, the region of pore formation can be extended to higher current densities wihout electropolishing occurring.

(Ref: P.C.Searson and J.M.Macauley, *Nanotechnology*, **3** (1992), 188)

Figure 3.1 - Plots of Current versus Voltage and Current versus HF Concentration Showing Regimes of Porous Silicon Formation and Electropolishing

Experimental Technique	Information Obtained from This Technique
1) Transmission Electron Microscopy (TEM)	Commonly used to determine pore size and distribution, see Beale *et al.* (1985), Tsao *et al.* (1987), Chuang *et al.* (1989), Sugiyama & Nittono (1990), Cullis *et al.* (1992) and Macauley *et al.* (1992). Care must be taken when comparing structures reported by the various researchers, as the particular TEM specimen preparation techniques used will influence the PS structure observed. For example, ion beam thinning can introduce amorphous phases not present after anodisation; and TEM samples formed by scraping PS layers off the substrate can damage the fragile structure.
2) Scanning Electron Microscopy (SEM)	Similar information can be obtained to TEM, but this technique is less destructive method of examination. However, the technique is limited to examination of coarser PS morphologies, see Cullis *et al.* (1992). P-type PS structures are not easily resolved using SEM, as they are so fine.
3) Adsorption Isotherms	Used to measure the surface to volume ratio of PS films, see Herino *et al.* (1987).
4) Gravimetric Analysis	Used to investigate how pores nucleate and propagate. Very simple method involving accurate weight measurement during anodisation, see Brumhead *et al.* (1993).
5) Capacitance Measurements	Used to examine changes in the internal surface area of PS during anodisation, see Peter *et al.* (1995).
6) Scanning Tunnelling Microscopy (STM)	Used to examine the degree of surface roughness of PS layers, see Amisola *et al.* (1992), Parkhutik *et al.* (1993), Enachescu *et al.* (1994) and von Behren *et al.* (1995).
7) X-Ray Topographic Techniques	Used to determine crystallite size, mis-orientation and the high degree of strain present in PS materials, see Barla *et al.* (1984).
8) Raman and Infrared Spectroscopy	Used to investigate porosity, crystallite size and oxidation of PS films, see Munder *et al.* (1992), Gregora *et al.* (1994), Naundon *et al.* (1994) and Pickering *et al.* (1984).

Table 3.1 Experimental Techniques Typically Used for Studying Porous Silicon

This type of morphology is believed to form for the following reasons. In order for pore growth to occur, charge must cross the Schottky barrier (i.e. the semiconductor-electrolyte interface at pore tip) by the process of thermionic emission. For thermionic emission, the barrier height (not barrier width) is important. As the pore tip radii are very small, image forces will significantly lower the barrier height, thereby causing current to flow preferentially at the pore tip. As the pore grows rapidly, its radius increases and the image forces are quickly reduced, thereby slowing down pore growth to produce small pores. At this point, other pores begin to grow. Any perturbations due to impurities, doping density fluctuations, the presence of H_2 bubbles, or the etching process can lead to lowering of the barrier, and therefore pore growth. As a result, a highly porous structure is formed.

b) P^+-Type Porous Silicon (Degenerate) - MesoPorous

Compared to p-type PS, p^+-type PS is highly anisotropic, see Beale *et al.* (1985) and Berbezier & Halimaoui (1993). This material exhibits long voids running perpendicular to the silicon surface, separated by silicon rods. These rods are ~10nm in diameter and follow the [100] direction. There is much side branching, with small buds forming on the sides of pores. The PS porosity lies in the range 30-80%.

This type of morphology is believed to form because current flow in highly doped silicon occurs by tunnelling (either direct or Zener), rather than by thermionic emission. Therefore, the barrier width (not barrier height) is important. The barrier width depends on the width of the depletion region, with tunnelling being possible for barriers <80Å. At the pore tips, the electric field is enhanced, thus causing a reduction in the depletion layer width. However, the depletion regions are widest at the pore edges, see Figure 3.3. In addition, if the depletion regions of adjacent pores overlap, the depletion layer width increases. This further reduces the current density in that region, preventing the pores growing any closer. Therefore maximum current flow will occur at the pore tip and little current will flow between pores. This effect results in the formation of columnar pores.

c) N and N^+-Type Porous Silicon

The morphologies of n and n^+-type PS depend strongly on illumination. However, as this material has not been studied in this thesis, detailed descriptions will not be given. Macroporous PS is formed if anodisation is carried out without strong illumination, see Albu-Yaron *et al.* (1993), Searson *et al.* (1992) and Chuang *et al.* (1989). However, if illuminated, n / n^+ PS morphologies are similar to those formed on p / p^+-type silicon of corresponding resistivity, see Lehmann & Gosele (1992).

3.3.2 Dependence of Porosity on HF Concentration and Current Density

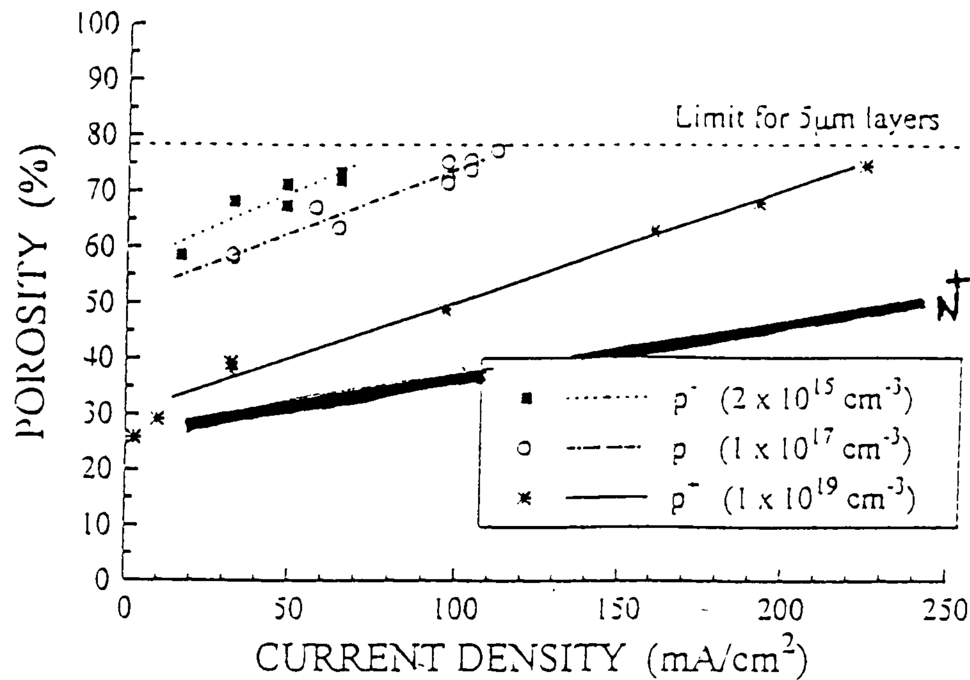
The substrate doping has the strongest influence on PS morphology. However, other variables, including current density and HF concentration also affect pore size and hence porosity. (Note that pore size is dependent on increasing film porosity.) Figure 3.4 explains the concept of porosity, showing an idealised view of the partial dissolution of silicon during pore formation, see Canham (1990). Beale *et al.* (1985) have performed detailed examination of the effect of HF concentration and current density on p-type silicon, for wafers of different resistivity. The results are shown in Table 3.2 and the main points are summarised below.

a) Porosity Increases with Increasing Current Density

The PS material will always act to minimise the voltage drop at the interface. The voltage dropped at the interface is minimised if the current is distributed over a larger interfacial area. The interfacial area will increase if the number of pore tips at the interface is increased. If the current density is increased, the voltage drop will also increase. Therefore, the PS will act to minimise this increase by growing more pores, thereby increasing the porosity of the material. Figure 3.5 demonstrates this effect for p and p^+-type PS, see Frohnhoff *et al.* (1995).

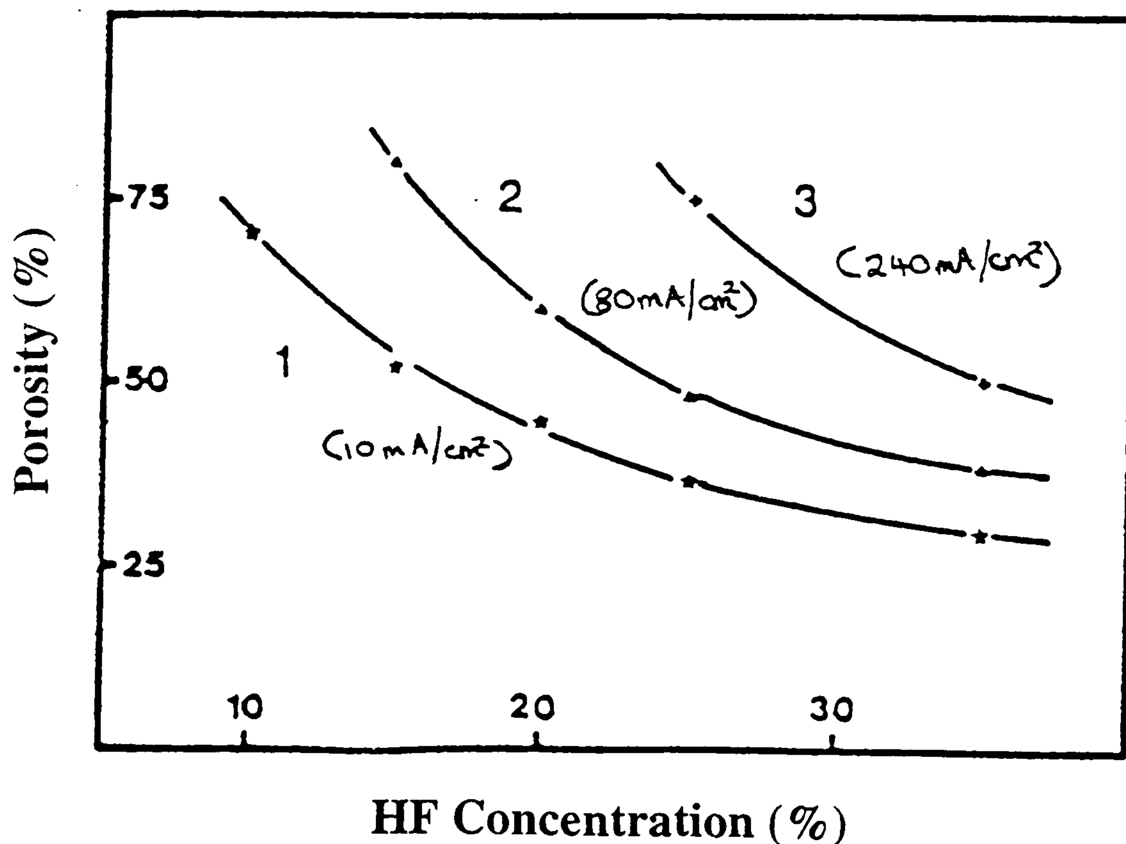
b) Porosity Increases with Decreasing HF Concentration

Decreasing the HF concentration leads to an increase in the interfacial impedance. This increase in impedance causes an increase in the voltage dropped across the interface. The PS material acts to minimise this increase, and so causes an increase in the number of pores at



(Ref: S.Frohnhoff, M.G.Berger, M.Thonissen, C.Dieker, L.Vesean, H.Munder and H.Luth, *Thin Solid Films*, 255 (1995), 59)

Figure 3.5 - Dependence of Porosity on Current Density Applied During Anodisation for Different Substrate Doping Levels
This graph demonstrates results reported in the literature, showing the dependence of porosity on applied current density.



(Ref: R.Herino, G.Bomchil, K.Barla and C.Bertrand, *J. Electrochem. Soc.: Solid State Science & Technology*, B4 (8) (1987), 1994)

Figure 3.6 - Dependence of Porosity on HF Concentration of Electrolyte
This graph demonstrates the dependence of porosity on the HF concentration in the electrolyte, for p^+-type silicon.

Substrate was heavily P-doped silicon (resistivity of 0.01Ωcm). Porosity was measured using a gravimetric technique.

the interface, thereby causing an increase in porosity. Figure 3.6 demonstrates this effect for p^+ type silicon, see Herino *et al.* (1987).

The values of porosity shown in Table 3.2 lie in the range 20-79%. Intact PS layers of higher porosity are difficult to obtain. It is thought they are under great strain and break up during evaporation of the electrolyte. However, Canham *et al.* (1994) believe they have obtained intact layers with porosities up to 95%, by using supercritical drying to preserve very high porosity films.

3.4 Post-Anodisation Procedures

Several procedures result in thinning of the PS structure after anodisation has taken place, see Canham (1990) and Bsiesy *et al.* (1991). Examples are described below:

a) Open-circuit etching - The PS structure is immersed in HF in the dark for several hours. The PS structure is thinned by chemical dissolution.

b) Anodic oxidation - The PS sample is immersed in an HCL or KNO_3 solution and the PS structure is thinned by oxidation, see Halimaoui *et al.* (1991).

3.5 Oxidation and Contamination of Porous Silicon Films

Canham *et al.* (1991) carried out secondary ion mass spectroscopy (SIMS) analysis on PS layers and found that they contained a high level of impurities. Jung *et al.* (1993) found very high concentrations of H, C, O and F ($>>10^{20}cm^{-3}$), in addition to N ($\sim10^{19}cm^{-3}$). H and F are believed to be introduced during the anodisation process, while C and O are introduced over time. It has been found that extended storage in air at room temperature converts the hydrogen passivated surface to a contaminated native oxide. The PS skeleton is thought to undergo gradual oxidation over time. Even small amounts of oxidation can produce large stresses and lead to cracking of the layer, particularly in high porosity PS. One of the reasons for the adsorption of such a large number of impurities is the large surface area ($>500m^2cm^{-3}$ for 55% porosity microporous p-type PS). Oxygen levels in microporous films were found to be greater than in mesoporous films, presumably due to the larger surface area.

3.6 Electrical Properties Of Porous Silicon

3.6.1 Resistivity versus Bulk Silicon

For both micro- and mesoporous silicon, resistivity is several orders of magnitude higher than for bulk silicon. Two and three terminal measurements of n-type and p-type PS films (while still attached to their substrates), and also four terminal measurements of films (removed from the substrate) were made by Beale *et al.* (1985), Unagami (1980) and Bilenko *et al.* (1983). High values of resistivity ($>10^5$ Ωcm) were achieved each time.

3.6.2 Models for Conduction in Porous Silicon

Beale *et al.* (1985), Lehmann *et al.* (1995) and Simmons *et al.* (1995) believe the decrease in conductivity (following anodisation) results from a depletion of carriers in the PS layer due to the small dimensions of its skeleton, which are well below the depletion layer width. They propose that the Fermi level is pinned by surface states on the internal surface. Measured carrier concentration levels are only $\sim 10^{19}cm^{-3}$ at the Fermi level and so are consistent with this theory, see Ben-Chorin *et al.* (1993).

3.6.3 Microporous versus Mesoporous

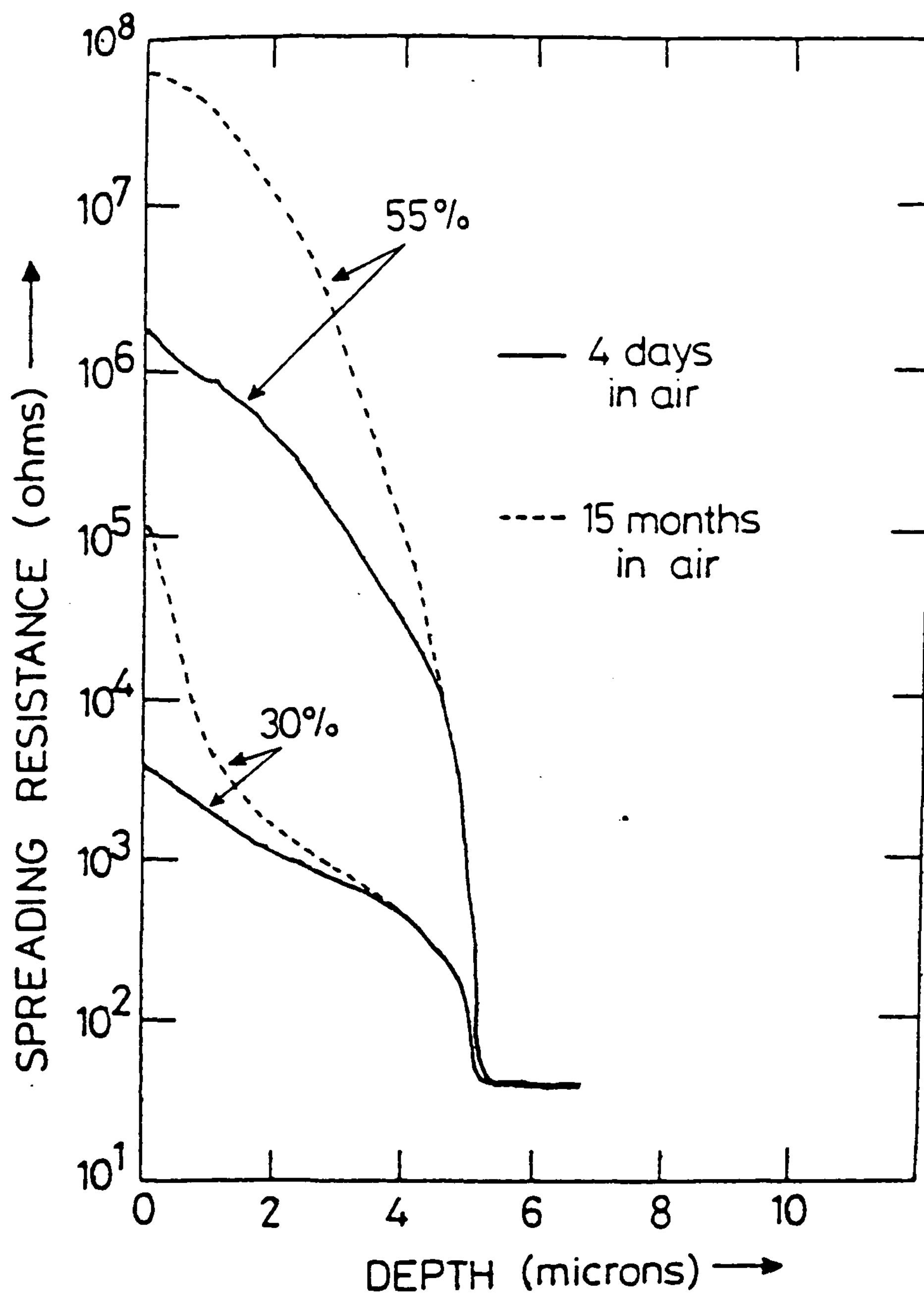
Microporous PS is the most resistive of the different PS structures. The resistivity of mesoporous PS is in the range $\sim 10^5$-10^9Ωcm, compared to the resistivity of microporous PS, which is in the range $\sim 10^8$-10^{11}Ωcm, see Sculz (1993). This is probably due to the fact that the dimensions of the structure are larger, and so regions of the material will not be depleted.

3.6.4 Effect of Oxidation and Gaseous Treatments on Resistivity

The conductivity of PS can be altered by certain treatments:

a) Oxidation - Increases resistance of the PS film, due to the formation of an insulating layer on the PS surface. This effect is demonstrated in Figure 3.7.

b) Gases/Liquids - Ben-Chorin *et al.* (1994) observed that for microporous PS, an increase in conductivity of several orders of magnitude occurred on exposure to polar gases and



Variation in resistivity of two mesoporous layers in n^+ substrates as a result of extended storage in air. The gravimetrically determined porosities of the freshly anodized layers are indicated.

(Ref: L.T.Canham, M.R.Houlton, W.Y.Leong, C.Pickering and J.M.Keen, *J. Appl. Phys.*, **70 (1)** (1991), 422)

Figure 3.7 - Graph Demonstrating Increase in Resistance of Porous Silicon as Oxidation Occurred
This graphs shows that the resistance of the porous silicon layer increased with time, due to oxidation of the layer following extended storage in air. These results are for n^+-type porous silicon - the effect would be expected to be more marked for p-type silicon.

liquids such as water and ethanol. Lehmann *et al.* (1995) explain this effect as a screening of the surface traps by polar species.

3.7 Quantum Confinement in Porous Silicon

3.7.1 Quantum Size Effects

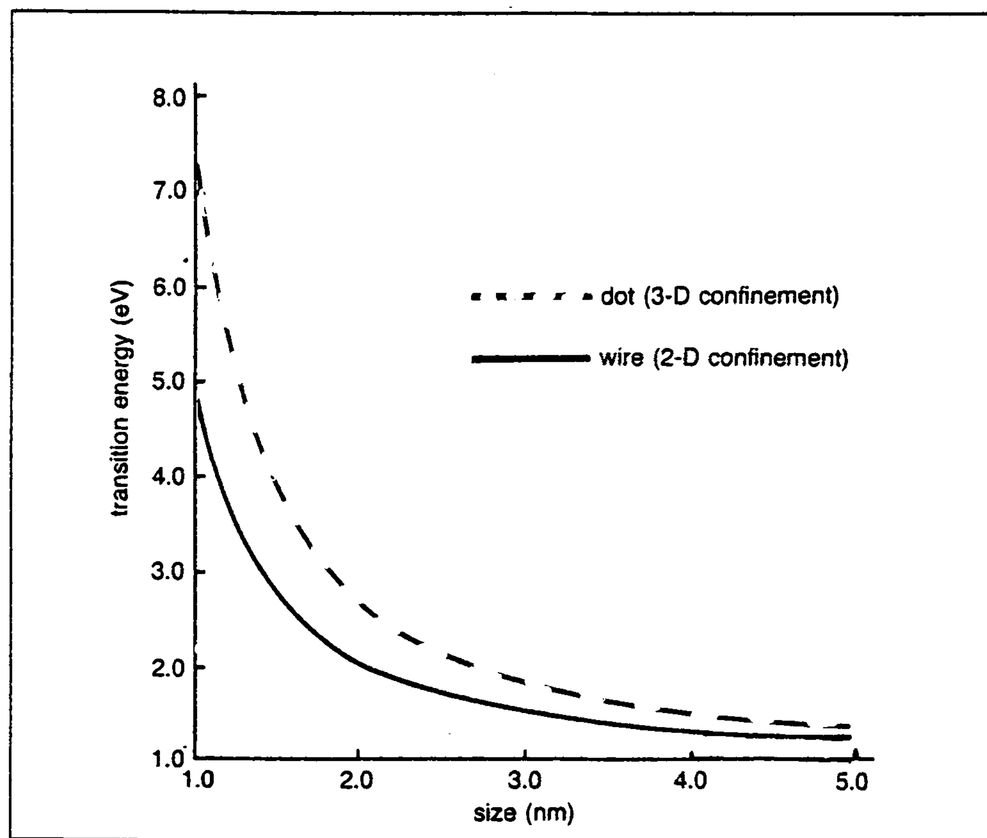
Quantum size effects are observed when structures become smaller than the Bohr radius of the free exciton (which is ~5nm in silicon). Structures <5nm are commonly found in p-type PS structures and so quantum effects should exist in this material. If quantum confinement occurs, the bandgap will be changed. The bandgap of bulk silicon is ~1.1eV. Canham (1992) report calculations of the effect of quantum confinement on silicon particles and wires using simple particle-in-the-box and effective mass theory. The results are shown in Figure 3.8, showing that for both quantum dots and quantum wires, the bandgap can treble within the particle size range 1-5nm. An increase in the bandgap width should affect the field emission properties of an anodised silicon tip, because an increase in bandgap will cause a change in electron affinity.

3.7.2 Evidence for Quantum Confinement in Porous Silicon

a) Efficient Luminescence

Luminescence from bulk silicon occurs at a wavelength of 1.12eV in the infrared region. However, efficient luminescence occurs from p-type PS in the energy range 1.4-2.2 eV (from red to green in the visible spectrum), see Bsiesy (1991), Halimaoui *et al.* (1991), Ren & Dow (1992), Read *et al.* (1992) and Steigmeier *et al.* (1992). This luminescence corresponds to a crystallite size between 2.5 and 4.5nm, which is known to occur in p-type PS structures. The origin of improved luminescence is therefore believed to be the fine p-type PS morphology. Luminescence is not observed from p^+-type PS. The reason for this is believed to be the crystallite size within p^+-type PS is usually not small enough to cause quantum confinement.

Alternative explanations for photoluminescence have been put forward. These include surface passivation and the presence of Si-H_x compounds (see Jung *et al.* (1993) for a comprehensive discussion of the possible mechanisms). However, it is now widely believed that the photoluminescence is caused by the fine PS morphology.



(Ref: L.Canham, *Physics World*, **5(3)** (1992), 41)

Figure 3.8 - Diagram Demonstrating Relationship Between Bandgap and Crystallite Size

This graph shows the relationship between bandgap and crystallite size for 2-D (quantum wire) and 3-D (quantum dot) confinement. The plots were calculated using simple particle-in-the-box and effective mass theory. It can be seen that for both quantum wires and quantum dots, the bandgap can treble within the particle size range 1-5nm.

Luminescence from bulk silicon occurs at a wavelength of 1.12eV. However, luminescence from p-type porous silicon has been reported to be in the range 1.4-2.2eV. According to the plot above, this would correspond to a crystallite size in the range 2.5nm and 4.5nm. TEM studies have shown that this crystallite size is known to occur within p-type PS structures.

b) Blue Shift

Canham (1990) carried out an HF open-circuit etch for several hours. This resulted in thinning of the PS structure, increasing the porosity to 80%. This subsequently led to an increase in bandgap, blue shift in the emitted light, and a dramatic increase in luminescent intensity, see Figure 3.9. Anodic oxidation, which results in thinning of the PS structure, also produced a blue shift, see Figure 3.10. These effects are attributed to a reduction in the size of PS quantum structures, and are further evidence that room temperature luminescence is a result of quantum confinement only.

3.8 - Concluding Remarks

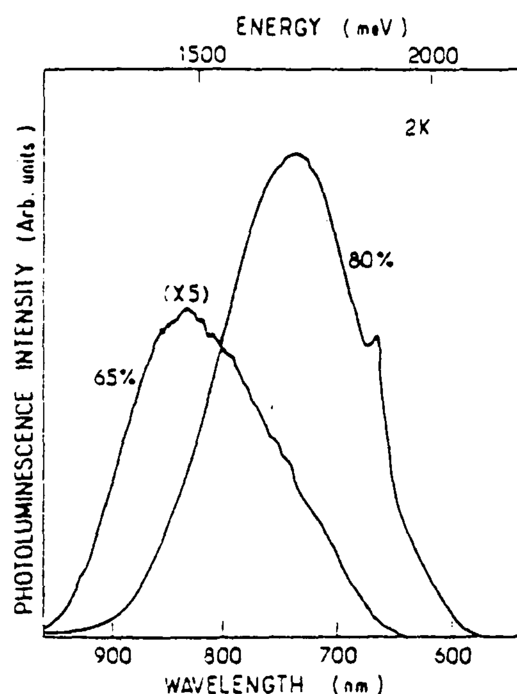
In summary, the main differences between bulk and porous silicon are as follows:

1) The structure of porous silicon is completely different - it contains pores in the range 3-1000nm wide, depending on initial substrate doping, applied current density and HF concentration.

2) Porous silicon is highly resistive.

3) Porous silicon has a very high surface area, which is easily oxidised.

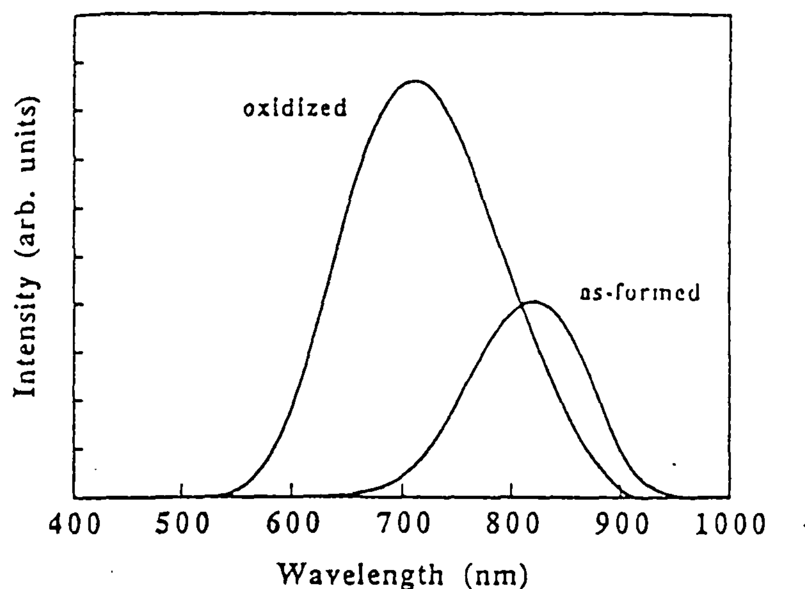
4) Depending on initial substrate doping, quantum confinement can occur in porous silicon, leading to a widening of the silicon bandgap.



2 K photoluminescence spectra of 20-μm-thick porous Si samples with porosity 65% and 80%. The intensity of the 65% sample spectrum is multiplied by a factor of 5. The excitation was provided by the 0.5 W 4579 Å line of an argon laser.

(Ref: M.Vocs, P.Uzon, C.Delalande, G.Bastard and A.Halimaoui, *Appl. Phys. Lett.*, **61(10)** (1992), 1213)

Figure 3. 9 - Effect of Open-Circuit Etching on Photo-Luminescence
Open-circuit etching was carried out by placing the anodised substrate in HF for several hours. This resulted in thinning of the porous silicon structure, increasing porosity from 65% to 80%. This led to an increase in bandgap, giving rise to a blue shift in the light emitted and a dramatic increase in phtoluminescent intensity.



Comparison of the room temperature PL spectra of two identical % porosity porous layers, as formed and after electrochemical oxidation

(Ref: R.Herino, S.Billat, A.Bsiesy, F.Gaspard, M.Ligeon and I.Mihalcescu, *Appl. Phys. Lett.*, **61 (10)** (1992))

Figure 3. 10 - Effect of Anodic Electrochemical Oxidation on Photo-Luminescence
Electrochemical oxidation also resulted in thinning of the porous silicon structure. This also gave rise to a blue shift in the light emitted and an increase in the photoluminescent intensity. The results shown in Figure 3.10 and Figure 3.11 are further evidence that room temperature phtoto-luminescence is a result of quantum confinement only.

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Chapter 4
Development of SEM for Field Emission Measurements

4.1 Introduction

A Philips 505 scanning electron microscope (SEM) was adapted to enable field emission tests to be carried out. The main reasons for choosing the SEM were as follows:

a) It was believed that the vacuum required for field emission measurements ($\sim 10^{-7}$ torr) was achievable inside the SEM.

b) A probe could be attached to a micromanipulator arm already fitted to the microscope, thus allowing a voltage to be applied to individual tips.

c) The SEM primary beam deflection system allowed the position of the probe relative to individual emitters to be monitored.

4.2 Adaptations Made to SEM for Field Emission Testing

In order to allow field emission measurements to be carried out, adaptations were made to the SEM. These included the following:

a) A new probe, capable of carrying a high voltage, was constructed.

b) This probe was connected through the wall of the SEM to a high voltage supply.

c) A computer was interfaced to the high voltage supply, in order to control the voltage applied by the probe.

d) A computer program was written to measure and record the field emission current.

Figure 4.1 shows a flow diagram of the adapted 505 SEM and the equipment required to run it. The important aspects of the microscope are summarised in Table 4.1. The initial adaptations were made during the course of a Part II undergraduate project, see Boswell (1992). However, during the course of the work for the present thesis, it was necessary to improve the vacuum system. Following this improvement, it was also necessary to study the following parameters affecting field emission measurements in detail:

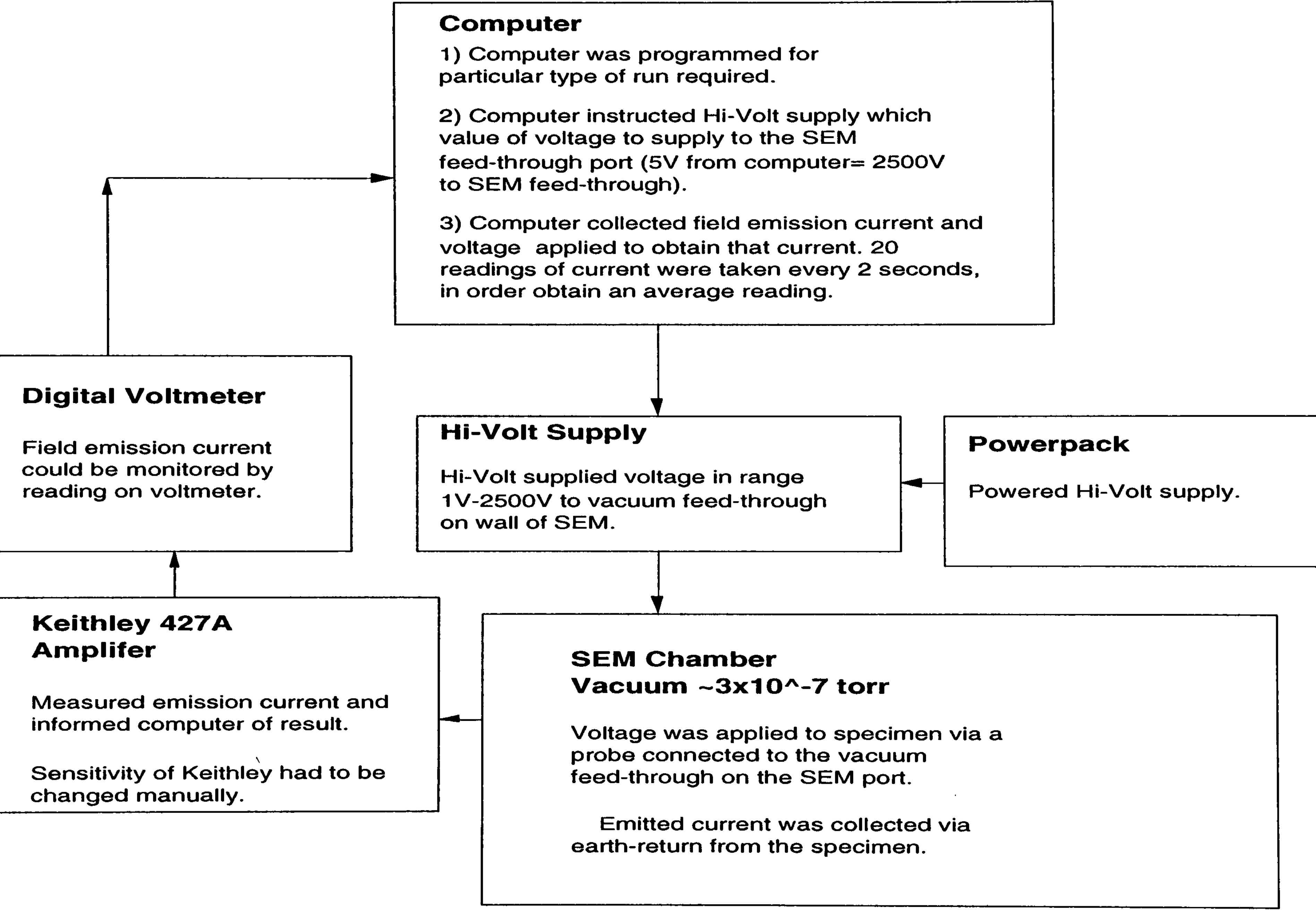


Figure 4.1 - Flow Diagram of Adapted 505 SEM and Equipment Required to Run It

Aspect of Microscope	Experimental Details
Specimen/ Specimen Mounting	Specimens were secured to a specimen stub (see Figure 4.2), which was slid onto a cold stage inside the microscope. The temperature of the cold stage could be lowered to 70K by adding liquid nitrogen to the cold trap.
Probe and Micromanipulator	A probe was constructed so that high voltages could be applied to individual emitters, see Figure 4.3.
In-Line Series Resistors	A 0.67MΩ resistor was placed between the probe and the high voltage vacuum feed-through. The role of this resistor was to protect the probe, in case it made contact with the specimen during field emission. If there was a surge in current, the accompanying increase in voltage was dropped across the resistor, rather than the probe. Figure 4.4 shows the effect if a resistor was not used.
High Voltage Supply	The high voltage supply consisted of a step-up transformer (Hivolt type) connected to a standard power pack. The exact voltage applied by the Hivolt pack was controlled by a computer, via an analogue/digital PCB Lab card.
Current Measurement	The field emission current was measured via the earth return from the specimen using a Keithley 427A amplifier, see Figure 4.1..Unfortunately, if the current rose past the Keithley overload protection level for a particular current setting, the computer program stopped the voltage ramping run. The sensitivity of this Keithley amplifier had to be changed manually. Therefore, if a tip did not self destruct at the maximum voltage applied, the run had to be repeated in order to obtain the highest value of emission current at destruction.
Computer	In order to allow the computer to control the applied voltage, a computer program was written in Quickbasic. This read and recorded the field emission current collected. The programme asked the operator at what value to start and finish ramping the voltage (between 1 and 2500V); and the voltage step to be used (usually 10V steps). The computer made 20 current readings every 2 seconds, in order to calculate an average value. Averaging decreased the effect of noise on the measured field emission current. The time taken to ramp up the voltage from 10V to 2500V in 10V steps, was ~2 minutes.

Table 4.1 Important Experimental Details of 505 SEM Adapted for Field Emission Testing

a) The reproducibility of emission from plain silicon emitters.

b) The accuracy with which the probe could be positioned above emitters.

c) The effect of changing the value of the resistor held in series with the probe.

Results from these studies are described in this chapter.

4.3 Improvement of Vacuum System

At the start of this project, the achievable vacuum inside the SEM was believed to be in the 10^{-7} torr range, assuming that the cold trap was regularly refilled with liquid nitrogen. Two different ion gauges had originally been used to check this vacuum level. However, field emission data collected in the SEM exhibited high levels of noise, and the starting voltage (defined as the applied voltage required to obtain an emission current of 1nA) varied greatly from tip to tip. Several researchers had reported that they obtained acceptable, reproducible field emission data at vacuum levels of $\sim 10^{-7}$ torr, i.e. at a similar vacuum believed to exist in the SEM, Tringedes (1993). Therefore, such poor emission data was unexpected.

Approximately 18 months into the project, it was discovered that the two ion gauges originally used to test the vacuum were faulty, and that the quality of the vacuum in the 505 SEM was, in fact, only 10^{-6}-10^{-5} torr - i.e. <u>at least</u> an order of magnitude worse than originally believed. It was thought that this poor vacuum was partly caused by leaks in the microscope. In order to detect and eliminate any leaks, the entire vacuum chamber had to be stripped. It was also decided to replace the old pumping system (an Edwards diffusion pump backed up with a rotary pump) with a turbo-molecular pump. After these procedures had been carried out, the final vacuum achieved was $\sim 3 \times 10^{-7}$ torr (as checked by a new ion gauge).

Prior to investigating the effect of anodisation on silicon FEAs, field emission from plain silicon emitters was studied in the improved vacuum, in order to check that the problems of emission noise had been substantially reduced. <u>All data collected in the poor vacuum</u>

was discarded and all anodisation experiments were repeated. All data from the anodised samples described in this thesis was obtained in the improved vacuum. The following sections demonstrate how the emission properties were improved following overhaul of the vacuum system.

4.3.1 Reduction in Emission Noise Following Improvement of Vacuum

Field emission noise was evaluated by applying a constant voltage to the probe, which was kept at a fixed distance from the emitter. The current was monitored using a digital voltmeter, see Figure 4.1. Current fluctuations over the course of a few seconds (at different current levels), a few minutes and over a period of ~90 minutes were studied in the improved vacuums and compared to the results obtained in the poor vacuum. For each test/sample examined and described in this chapter, ~20 separate tips were tested in order to ensure reproducibility.

Noise measurements were taken from two types of emitters:

i) P-type silicon emitters

ii) P-type silicon emitters coated with an evaporated layer of Au/Pd were investigated

It is known that field emission instabilities can be caused by fluctuations in the work function of an emitting site. In the case of silicon tips, most increases in work function are due to the formation of a thin surface oxide layer. An Au/Pd layer would not be expected to form such an oxide layer. Therefore, it was thought that emission from silicon tips with a Au/Pd layer evaporated onto them, would be more stable than emission from silicon tips.

a) Short-Term Noise (~1 second) After Vacuum Improvement

Table 4.2 summarises short-term noise (i.e. rapid changes in the emission current over a time <1 second) observed for silicon emitters, before and after improvement of the vacuum. Data obtained from Au/Pd coated tips was similar to that obtained from silicon tips.

- This data shows that short-term noise levels dropped by ~10 times after the vacuum was improved.

- In both vacuums, the noise levels were found to increase with the value of the current. This may have been due to desorption of adsorbates from the emitter surface, as emission caused heating of the tip. Other researchers have also seen this effect, see Section 2.6.1.

b) Medium-Term Noise (over ~1 minute) After Vacuum Improvement

For both silicon and Au/Pd coated emitters, emission was initially set at a current value (I_{start}) of ~0.02μA. The amplitude of current deviation ($\Delta I = |I - I_{start}|$) was estimated from the digital voltmeter readings.

In the poor vacuum, the emission current switched between high and low values several times over the course of ~1 minute. This type of noise is similar to the bistable noise discussed in Section 2.6.1. The maximum ΔI for a silicon tip was ~ 0.2μA, i.e. ~10 times I_{start}. The maximum ΔI for a Au/Pd coated tip was ~1.5μA, which is ~100 times I_{start}, i.e. much larger than for plain silicon tips.

For emission in the improved vacuum, sudden current switching between low and high current values was not observed for either silicon or Au/Pd coated emitters. This indicated that the degree of contamination had been reduced.

c) Longer-Term Noise (over ~90 minutes) After Vacuum Improvement

The initial current was set at a value of ~0.2μA and the probe-sample separation was kept constant. In the poor vacuum, the current obtained from a silicon tip dropped to zero over a period of ~20 minutes. As the emission current dropped, so did the degree of noise observed. Over the following 70 minutes, no emission was observed at all. In order to obtain ~0.2μA from the same emitter again, the voltage had to be increased from 1000V to 1200V. However even at this higher voltage, the emission current eventually decreased. The voltage then had to be increased to 2000V to regain a current of ~0.2μA. Other researchers have observed similar behaviour when testing in contaminated measuring systems (see Section 2.6.1). They attribute the affect to high work function species

adsorbing onto the emitter surface. The same mechanism could explain the results obtained here.

The emission current obtained from Au/Pd coated tips behaved differently - the value did not drop to zero at any time over a 90 minute period. In fact, for one tip, the current increased up to 80μA at one point and the fluctuations increased with current. These results are completely different to those obtained from silicon, where an increase in work function probably occurred with time. It appears that the work function of Au/Pd coated surfaces did not increase with time. Therefore, there is some advantage to covering silicon FEAs with Au/Pd. However, emission from Au/Pd coated tips was still extremely noisy. A possible explanation for the rise in current and increase in fluctuations is as follows. The electric field at the tip may have caused the transient formation of nanoscale protuberances at the metal emission surface. The formation of such protuberances is not well understood. However, it is thought that high local current densities cause tip heating. Heating will cause desorption from the tip surface, thereby increasing the current fluctuations. Heating could also cause field-induced build-up by preferential surface diffusion towards the highest field regions. The protuberances could therefore grow until local heating/sputtering became excessive. The protuberances could suddenly undergo self-destruction, causing large peaks in the emission current, as was observed in this work. (Protuberances would be expected to be present anyway on a surface onto which metal has been evaporated, due to the polycrystalline nature of the layer. These protuberances could have grown.)

In the improved vacuum, the field emission current obtained from both silicon and Au/Pd-coated tips did not decrease to zero, but remained at a similar value throughout the 90 minute period.

d) Summary

It is clear that improving the vacuum level reduced the level of emission noise observed. It was important for the noise to be substantially reduced, prior to carrying out the anodisation experiments.

4.3.2 Comparison Fowler-Nordheim Plots in Poor & Improved Vacuum

The large degree of noise observed in the poor vacuum at constant voltage had a detrimental effect on the Fowler-Nordheim (FN) and current-voltage (IV) plots obtained. In the poor vacuum, the computer was programmed to average the current 20 times per second, in an attempt to reduce the level of noise observed in the field emission data. However, noise was still evident in the FN plots. Figure 4.5 shows FN and IV plots collected in the poor vacuum. Examples of FN and IV plots collected in the improved vacuum are shown in Figure 4.6. In general, two different types of plots were observed.

a) Approximately Linear Fowler-Nordheim Plot

This type of plot (Figure 4.6, Tip 1) was not truely linear.

b) Typical Three-Stage P-Type Fowler-Nordheim Plot

The second type of plot (Figure 4.6, Tip 2) consisted of three stages. This behaviour is typical of emission from p-type semiconductors, see Section 2.4.4.

In the plots obtained in the improved vacuum, noise is not evident to the same extent as in the poor vacuum. However, if the surfaces had been contaminate free, truely linear FN plots or typical 3-stage emission plots should have been observed. However, this was not the case. Johnston & Miller (1992) obtained plots which were non-linear. By studying the field emission energy distributions (FEDs), they showed that an oxide layer was present at the surface. In the present work, it is highly likely that an oxide layer was present at the surface, as the specimen was exposed to air after fabrication and the SEM was not UHV. The presence of an oxide layer would explain the non-linear FN plots. It should also be noted that the oxide layer will affect the calculated values of emitting area and render estimates inaccurate, so care should be taken when analysisng these parameters.

c) Summary

In summary, the improvement in vacuum improved the FN plots obtained. However, the situation was still not perfect as the emission surfaces were not completely clean.

4.3.3 Improvement in Reproducibility Following Vacuum Improvement

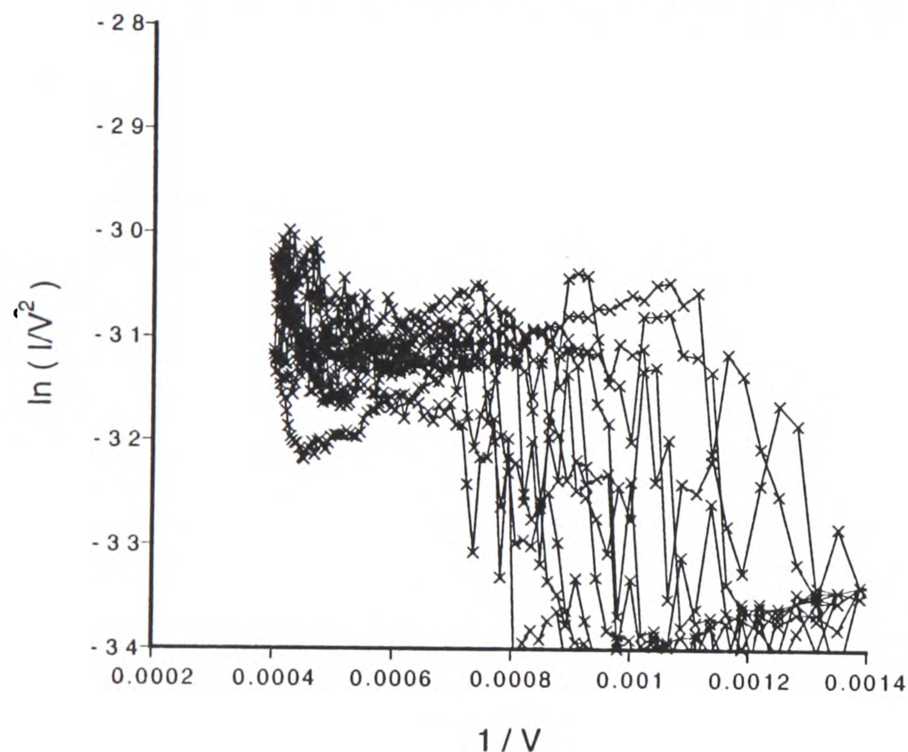
In addition to affecting the emission noise, the contaminated vacuum meant that field emission runs taken from one tip could not be reproduced. This section demonstrates how reproducibility was greatly improved following the improvement in vacuum.

a) Repeated Up-Down Runs

The computer was programmed to ramp the voltage up and then down again. Figure 4.7 and Figure 4.8 show several up-down runs, obtained in quick succession in both the poor and improved vacuums. For the runs obtained in the poor vacuum, the up and down runs do not follow the same paths. This gives the appearance of a hysteresis loop. Loops obtained from different tips exhibited varying degrees of hysteresis and the shape of the hysteresis loops varied between tips. As the maximum current was increased, the size of the hysteresis loop became more accentuated. This suggests that as the voltage was increased, the tip became blunter. A possible cause of blunting is tip sputtering. If tip sputtering occurred, this would have increased as the voltage increased. Therefore, the hysteresis would have increased as the tip was ran to higher current values, as was observed here.

In the poor vacuum, an interesting effect was observed when the temperature of the sample was decreased to 100K, by cooling the specimen stage with liquid nitrogen. Hysteresis plots obtained from the same tip before and after cooling are shown in Figure 4.9. The degree of noise within the higher current region decreased on cooling. However, the degree of hysteresis was only slightly reduced. This suggests that general emission noise was linked to surface diffusion; whereas hysteresis was linked to a desorption/sputtering effect. Diffusion is typically decreased by lowering the temperature, whereas desorption/sputtering is not affected.

In the improved vacuum, a small amount of hysteresis was observed for the first loop, see Figure 4.8. However, subsequent plots showed hardly any hysteresis, even in the high



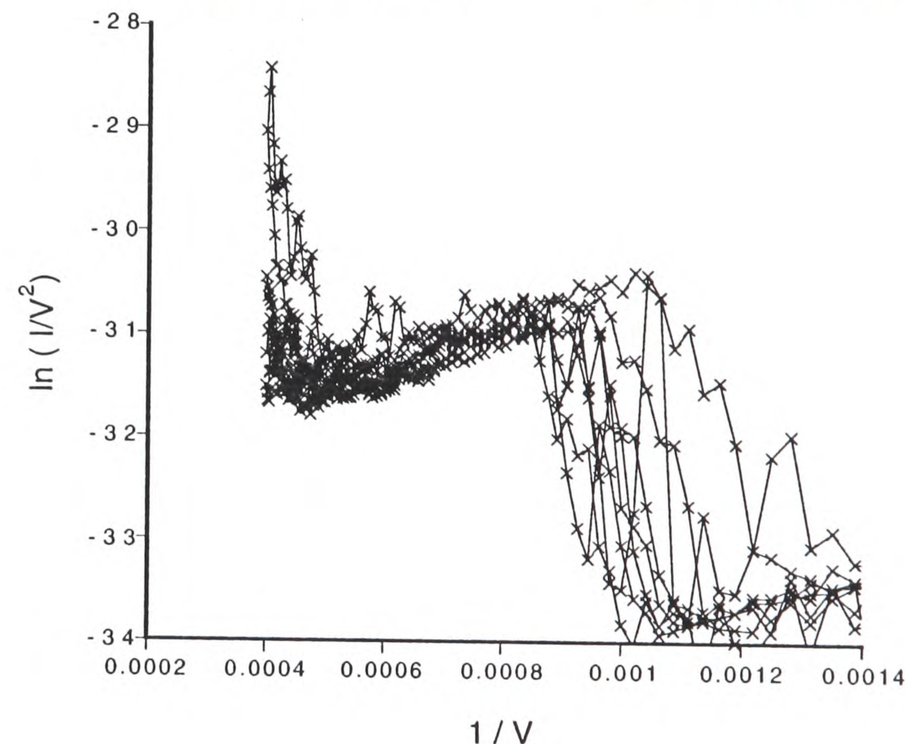


Figure 4.9 - Up-Down Hysterisis Plots Obtained from Silicon Tips in Poor Vacuum, Before and After Cooling the Sample to 100K
Hysterisis plots were obtained from the same tip before and after cooling to 100K. Although cooling reduced the degree of current fluctuations observed within the higher current region, the degree of hysterisis was only slightly reduced. Therefore, cooling the samples would not have been sufficient to reduce the overall noise observed - the vacuum system still needed to be improved to obtain reproducible results.

These results suggests that the current fluctuations were linked to surface diffusion, whereas the hysterisis was linked to a desorption/sputtering effect.

current range (10^{-5}A). This was a great improvement over the situation in the poor vacuum.

b) Successive Repeat Up-Runs

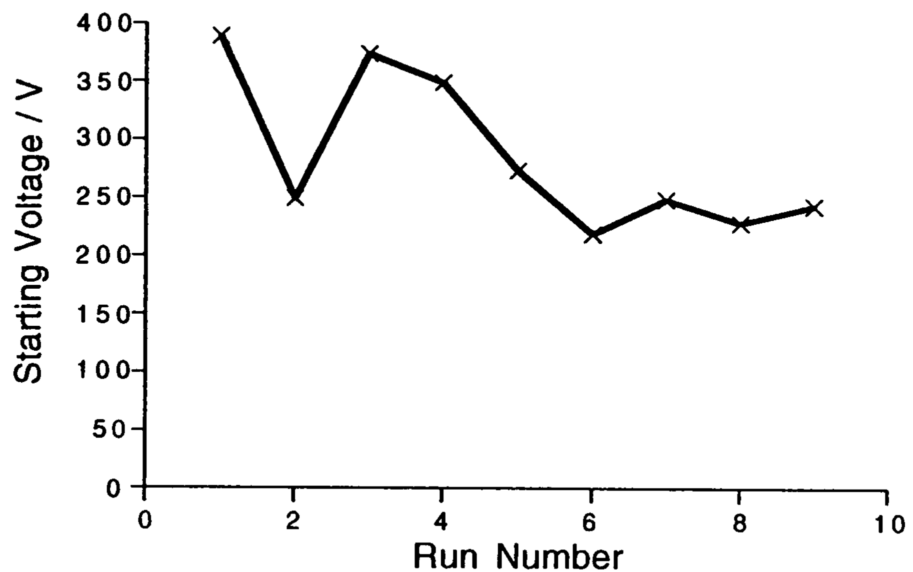
In this test, the voltage was increased to a certain value and then dropped to zero (instead of ramping the voltage down gradually). Field emission runs were taken from the same emitter several times and the probe-sample separation was kept constant. Emission runs were obtained from the same emitter in quick succession, with ~1 minute being left between each run. The starting voltage and slope/intercept of the FN plot were recorded for each run and compared. The following trends were observed:

i) Starting Voltage - Starting voltage was plotted versus run number, for emitters tested in the poor and improved vacuum, see Figure 4.10.

- In the poor vacuum, there was a large drop in starting voltage following the first run. This was probably due to desorption from the tip surface. Starting voltages measured for subsequent runs fluctuated from run to run. In general, the starting voltage decreased by up to 50% between the 1st and 9th run.
- In the improved vacuum, little variation in starting voltage was observed between runs. The largest drop in starting voltage was observed between the first and second run (probably due to some desorption of adsorbates). However, this drop was much less than that observed in the poor vacuum. The drop in starting voltage between 1st and 15th run was only 5-15%. This indicates that reproducibility of starting voltage was much better in the improved vacuum.

ii) FN Plots - Figure 4.11 and 4.12 shows successive FN runs obtained in the poor and improved vacuum.

- In the poor vacuum, the second plot was shifted to the right of the first plot, corresponding to a decrease in starting voltage. Subsequent plots were positioned either to the left or to the right along the axis. Differences in the shape, gradient and intercept of the FN plot were also observed from run to run.



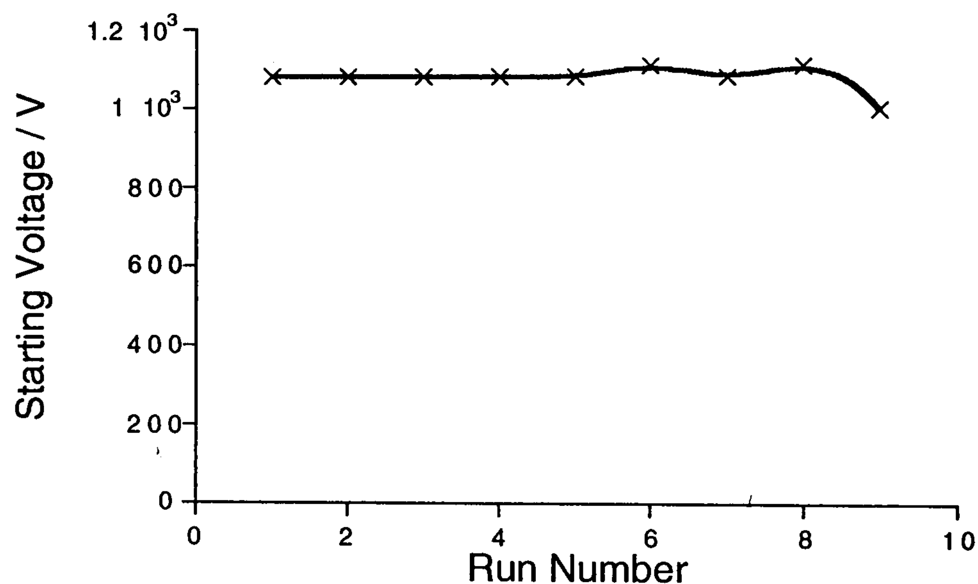
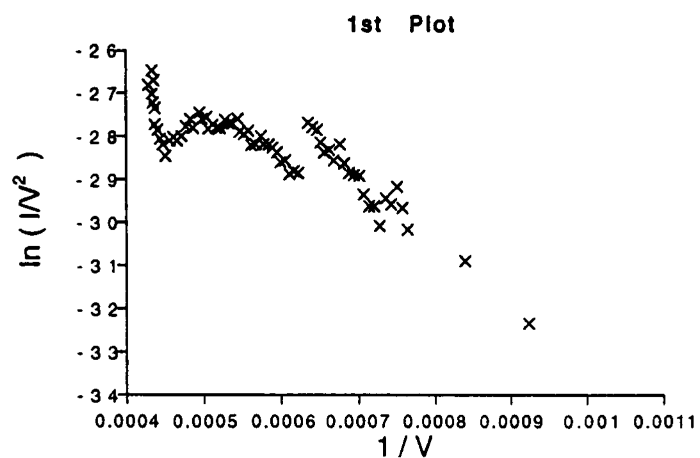
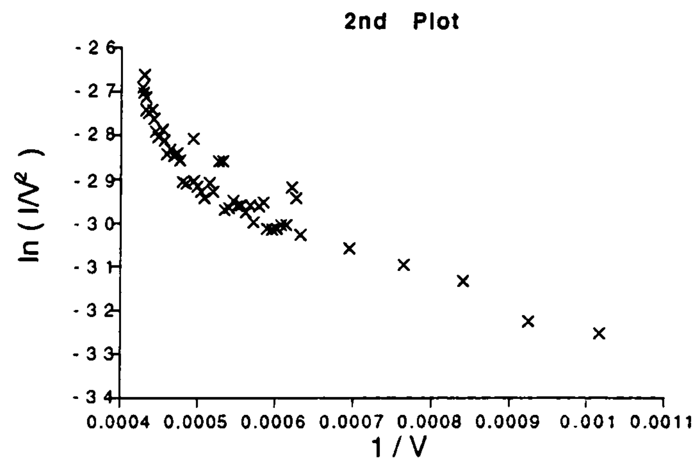
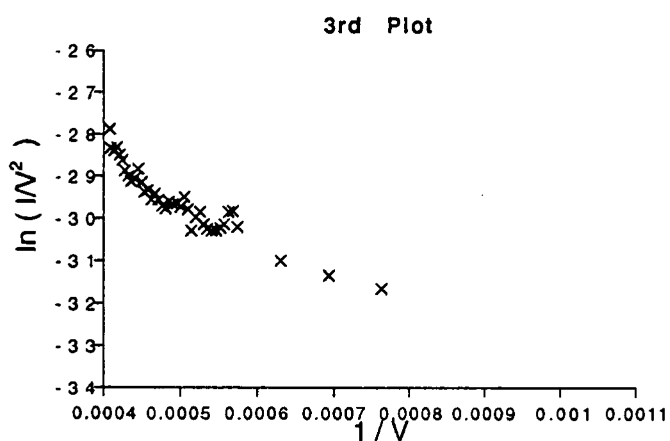
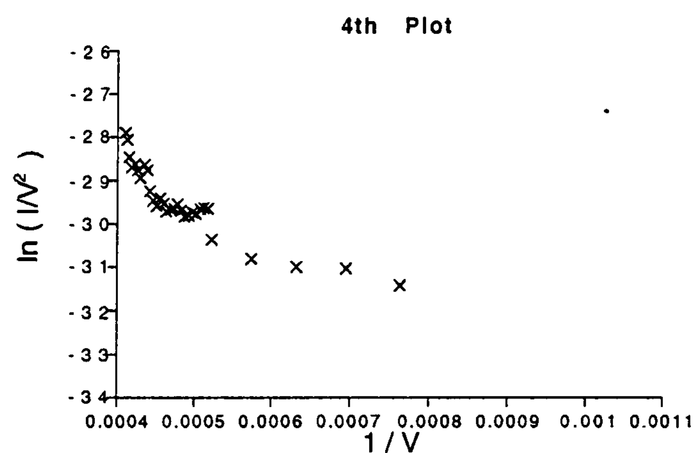


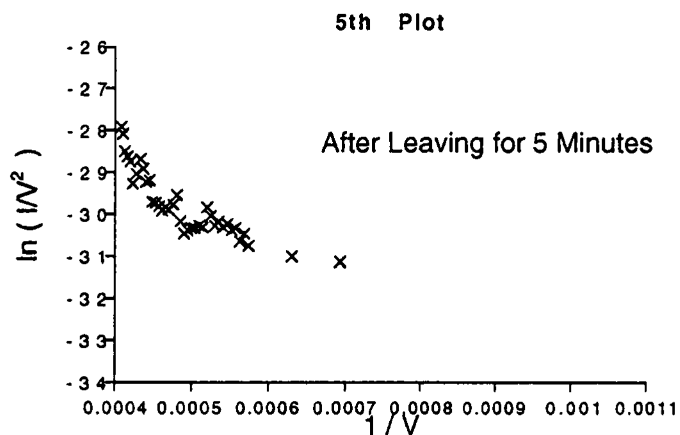
Figure 4.10 - Plots of Starting Voltage versus Run Number in both the Poor and Improved Vacuum Systems
This figure shows starting voltage plotted versus run number, for emitters examined in both the poor and improved vacuum systems. It is clear from these plots, that reproducibility was much better following improvement of the vacuum system. When several runs were obtained from a particular tip, the starting voltage from run to run was very similar - the starting voltage dropped by only ~5-15% between the first and 9th runs. When this experiment was carried out in the poor vacuum system, there was a large drop in starting voltage following the first run and subsequent runs fluctuated - in general, the starting voltage decreased by ~50% between the 1st and 9th run.

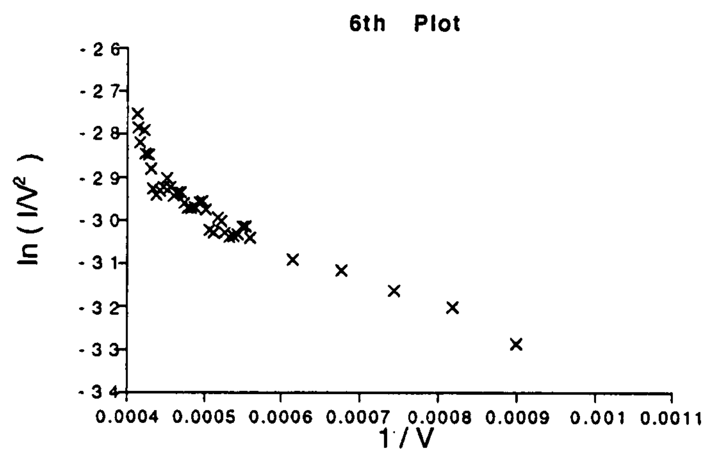


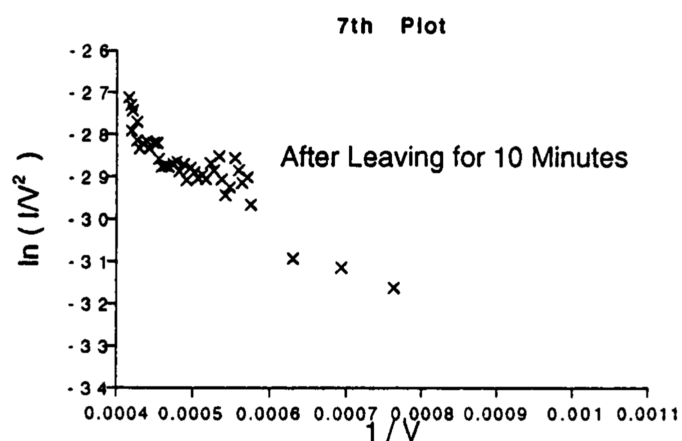












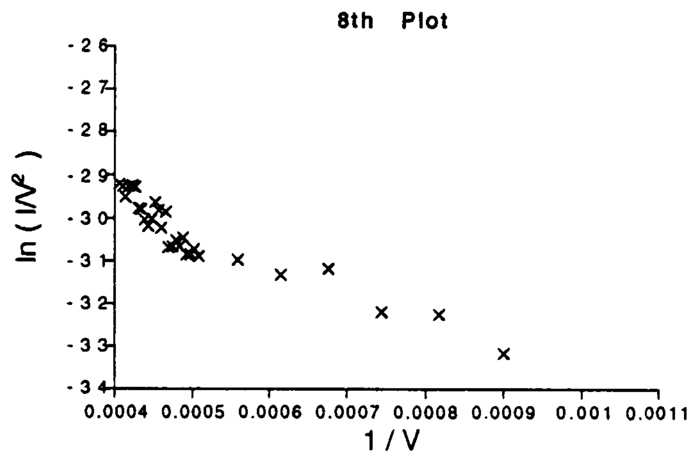


Figure 4.12 - All Eight Plots from Emitter Shown in Figure 4.11b) in Improved Vacuum
All 8 plots were obtained from the same emitter - all 8 plots are very similar. After leaving for 10 minutes, there was a slight difference in the plot, but this was much improved versus the situation in the poor vacuum.

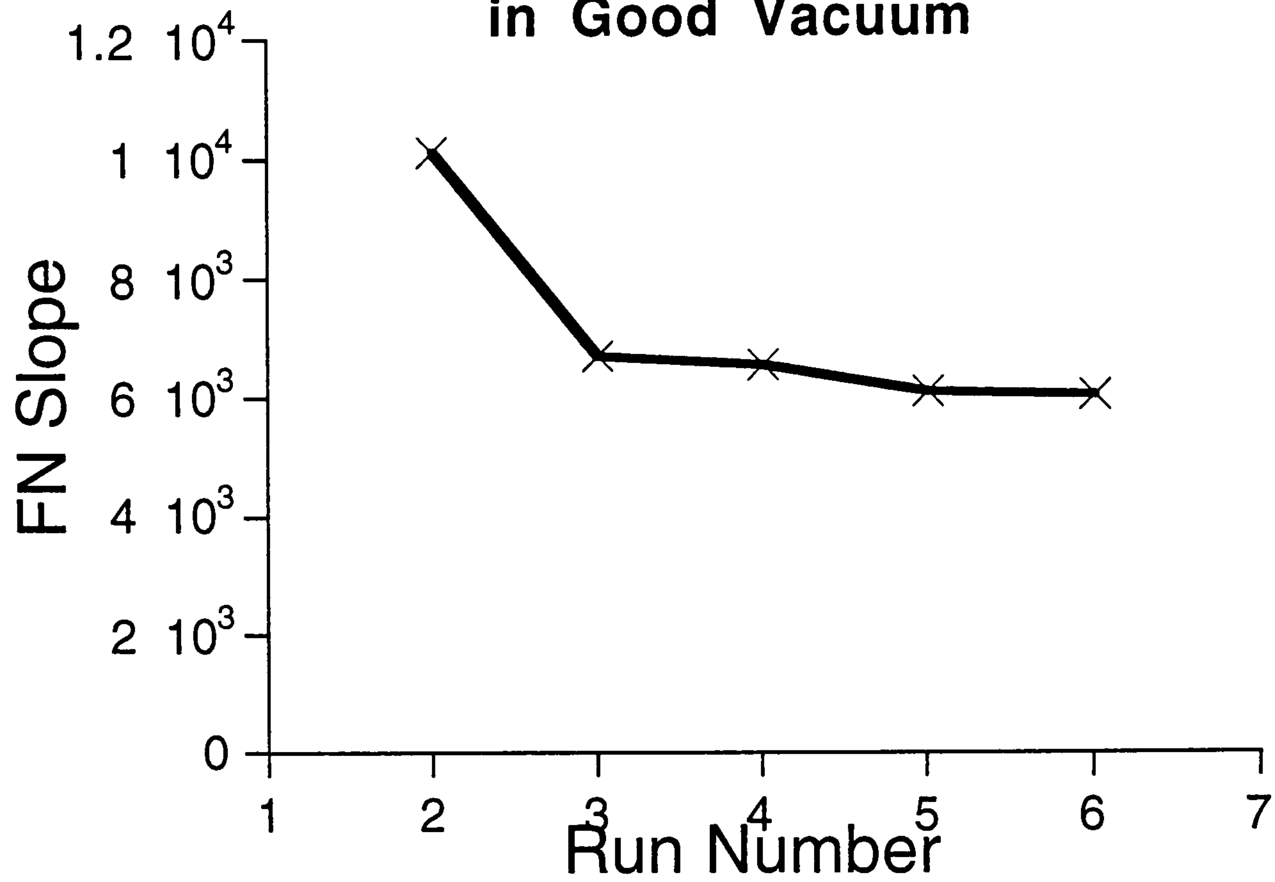
- In the improved vacuum, the reproducibility of plots from run to run was much better. However, the first plot was still slightly noisier than for subsequent runs. This was probably due to the presence of adsorbates/protrusions at the beginning of the first run. These adsorbates may have been evaporated off as the current increased, and therefore did not affect subsequent runs. All plots obtained from the same tip were similar in shape. The middle four plots from this series of runs are superimposed on top of each other, emphasising the similarity between them, see Figure 4.11b.
- Between some runs, emitters were left for up to half an hour before carrying out the next run (see Figure 4.12 - 5th and 6th plots). The difference in the shape of the plots before and after these time periods had elapsed was small. Therefore, this is a large improvement compared to the situation in the poor vacuum, where a change in FN plot was observed even if tips were left for only 30 seconds.

iii) Slope and Intercept of FN Plot- In the improved vacuum, the FN slope and intercept were calculated. Figure 4.13 shows these values plotted versus run number for one emitter. The value of FN slope for the first run was normally higher than for subsequent runs, but the values for subsequent runs were very similar. This may be connected with the small decrease in starting voltage observed after the first run, attributed to minor desorption.

iv) Maximum Current - Figure 4.14 shows a plot of the maximum current obtained at 2500V plotted versus run number, for one tip in the improved vacuum. This value dropped for each subsequent plot. It is not known why this occurred, as the starting voltage did not change much between runs and hence little tip blunting/work function increase can have occurred between runs.

4.3.4 Minor Influence of Ramping Rate on Emission Characteristics in Improved Vacuum

In the poor vacuum, the rate at which the voltage was stepped up affected the data collected. Therefore, the rate of data collection in the improved vacuum was investigated, to ensure that this effect had been reduced.



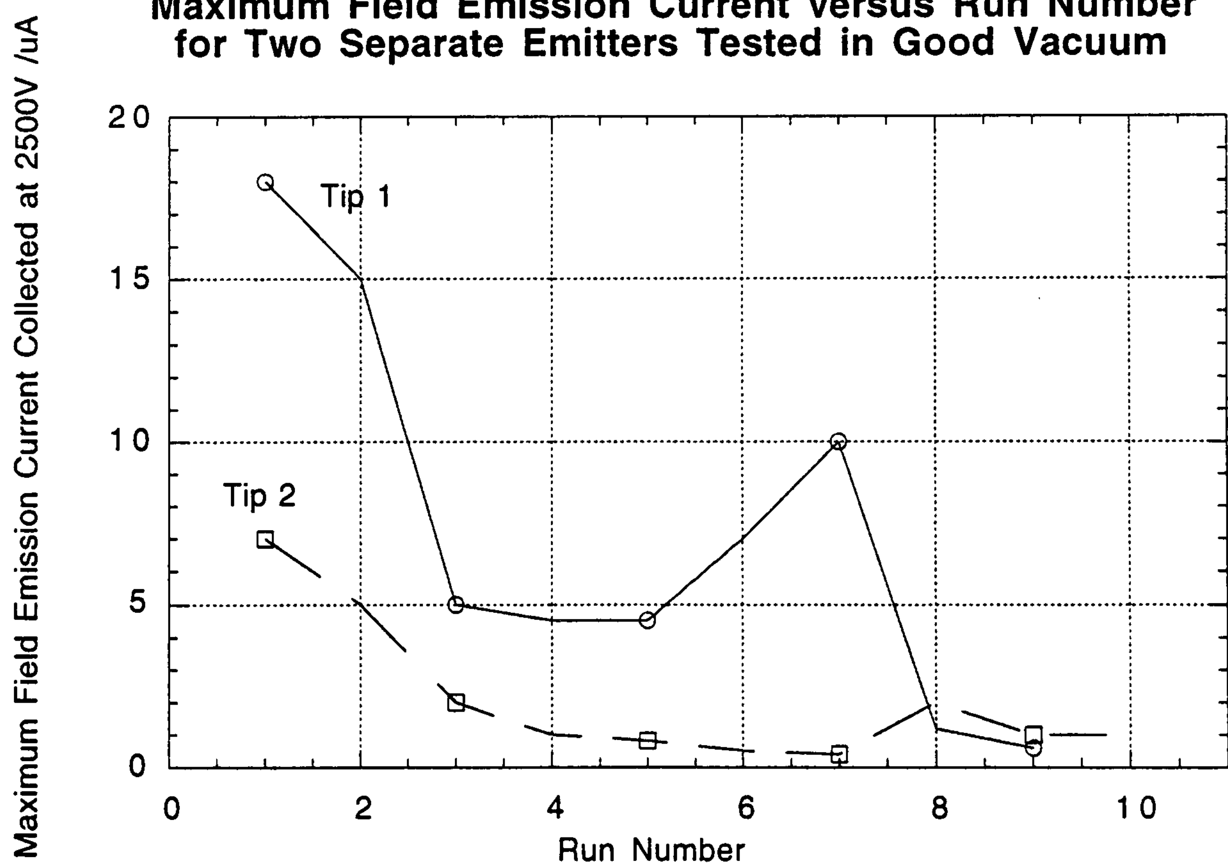


Figure 4.13 and Figure 4.14

a) Poor Vacuum

In the poor vacuum, data collected at a low ramping rate (e.g. 2V per second) was noisier than data collected at a faster ramping rate (e.g. 30V per second). Therefore, in order to reduce the amount of noise in the data, the tips were ramped at a higher rate. However, one disadvantage of increasing the ramp rate was that the tips appeared to destruct at a lower current level. This is probably because they did not have time to become 'seasoned', and so were unstable. Also, the shape of FN plots obtained from the same tip was different for different voltage ramping rates.

b) Improved Vacuum

In the improved vacuum, this situation was much better. One tip has been chosen to demonstrate this - see Figure 4.15. Eight plots were taken in total from this tip, using increments varying from 10V to 100V. These results show that in the improved vacuum, the voltage step had little effect on the emission characteristics. The shape of the FN plots taken at different voltage steps were very similar. This was a large improvement over the situation observed in the poor vacuum.

4.3.5 Summary

Emission in the overhauled vacuum system was much improved, but was still not ideal. This was probably because although the microscope was less contaminated, the samples were already coated with oxide layers prior to entering the vacuum chamber.

4.4 Cleanliness of Sample

4.4.1 HF Cleaning of Samples before Entering Vacuum

In the poor vacuum, cleaning the sample with buffered HF before placing into the adapted SEM did not improve the emission noise. In the improved vacuum, cleaning with HF appeared to make no difference to the emission noise either.

For a sample stored in air for several weeks, the first emission run occurred at a starting voltage ~50% higher than for subsequent runs, in either vacuum. This was probably due to

removal of an oxide layer during the first field emission run, which caused a drop in starting voltage for all subsequent plots. Similar behaviour was observed by King *et al.* (1994). However, if samples were cleaned in HF after storing in air for several weeks, the mean starting voltage was lowered to that of freshly etched tips. It was believed that dipping the sample in an HF solution removed the oxide layer, decreasing the emitter work function, see Makhov (1989).

For this reason, anodised samples were placed into the 505 microscope immediately after etching and/or anodisation. Non-anodised silicon samples which were not placed into the microscope immediately after etching, were always given an HF dip prior to insertion in the microscope. Anodised silicon could not be given an HF dip, as this disrupted the PS layer (see Chapter 6).

4.4.2 Hydrogen-Plasma Cleaning

While the vacuum was still poor, attempts were made to clean the sample surface in-situ, using a hydrogen plasma. This method has been used by other researchers to clean molybdenum tips, see Section 2.6.1. It was thought that the same treatment would have a similar effect on silicon tips. However, it was found that the emission noise level did not decrease after the plasma treatment was carried out. Therefore, the use of the hydrogen plasma was dis-continued. It is thought that the vacuum at the time was too poor to work properly. This treatment may work in the improved vacuum, but there was not sufficient time to investigate this further.

4.5 Accuracy of Probe Positioning

The probe-emitter separation is an extremely important parameter in field emission experiments. This is because the field at the tip is determined by the voltage applied by the probe and by the probe-emitter separation. It is therefore crucial to know the extent to which the emitter-probe separation varies both from tip to tip and from sample to sample.

In this work, major issues with the probe included the following:

a) Mechanical Stability

A tap on the bench outside the microscope caused the probe to oscillate (this could be seen on the SEM screen). If the probe oscillated during emission, the field at the emitter tip also oscillated, and caused the emission current to change.

b) Attraction to Surface

As a voltage was applied to the probe, it was attracted down towards the specimen surface. Therefore, the emitter-probe separation at an applied voltage of 10V and at 2500V were not the same.

c) Exact Probe-Emitter Separation Not Known

In this work, the external micromanipulator control wheels were used to position the sharp tungsten probe tip close to the specimen. Final, more accurate positioning of the probe relative to individual emitters, was carried out using the x,y,z control on the SEM specimen stage. Unfortunately, in the adapted SEM, the probe-emitter separation could not be observed in all three dimensions. Using the normal configuration, the vertical probe-emitter separation could not be measured. Although the specimen could be mounted vertically, the lateral probe-emitter separation was then unknown.

These issues were cause for some concern. Therefore, the configuration used in the adapted SEM was investigated in more detail. Both computer modelling and field emission tests were carried out - the results are outlined in the following sections.

4.5.1 Computer Modelling - Dependence of Starting Voltage on Emitter-Probe Separation

In the literature, modelling of an FEA with an extended planar anode has been widely reported, see van Veen (1994), Mackie *et al.* (1994), Nicolaescu (1994) and Hong *et al.* (1994). However in an experimental configuration, such as exists inside the adapted SEM, the probe diameter has similar dimensions to the emitter-probe separation (and to the dimensions of the emitter). Thus the probe can no longer be assumed to be an infinite

conducting plane and the situation has to be modelled differently. To understand the influence of emitter-probe distance on field emission inside the 505 SEM, computer modelling of the dependence of field emission on tip-probe separation was carried out in collaboration with Dr. Dan Nicolaescu, Institute of Electronic Engineering, Romania.

a)Assumptions

Computer modelling was carried out using the configuration and assumptions shown in Figure 4.16.

b)Variables Altered

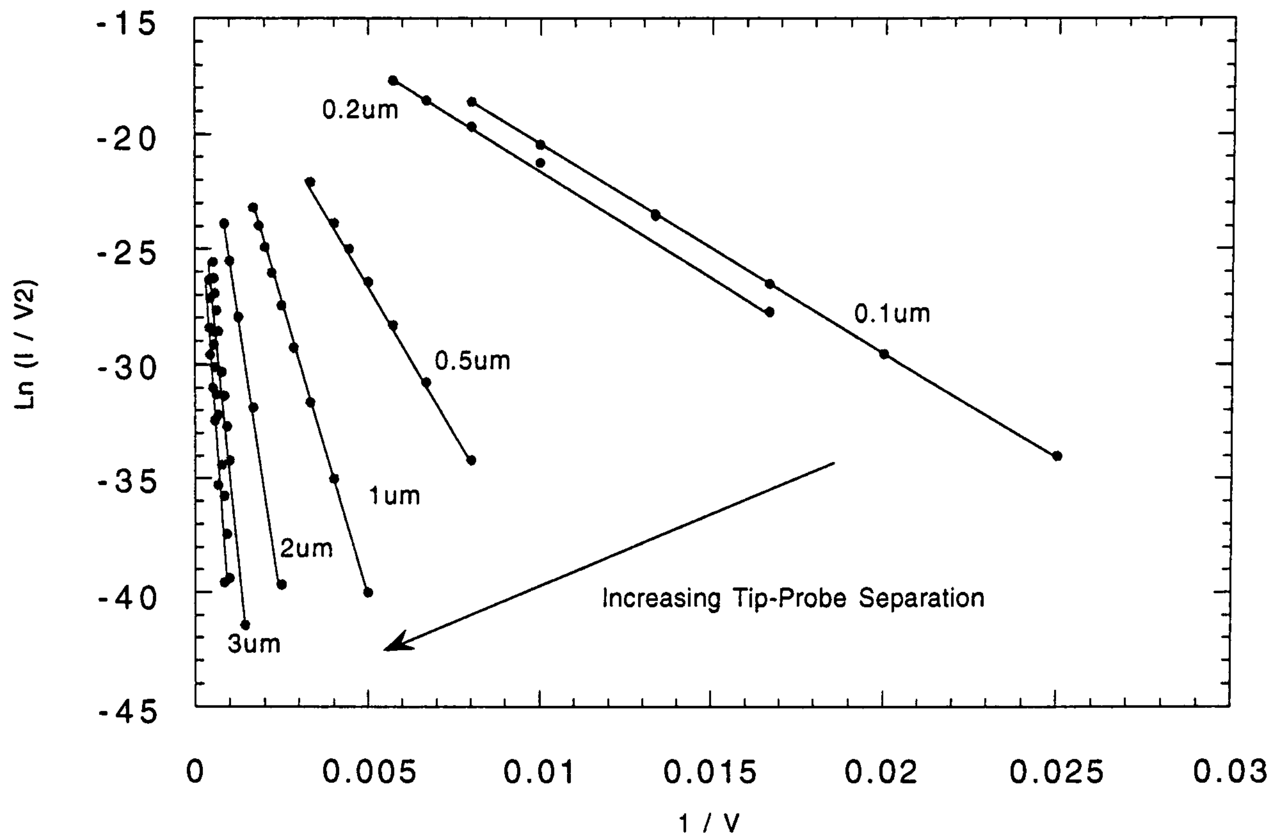
Variables which were changed were the probe-emitter separation and the half angle of the emitter. Values of probe-emitter separation used were 0.1, 0.2, 0.5, 1, 2 and 5μm. Only modelling results for an emitter half angle 80° (corresponding to a typical 4 sided pyramid) are presented here.

c)Results

The modelling results (both FN plots and IV plots) are presented in Figure 4.17a-c. The FN plot shifted to the left along the x-axis as the probe-emitter separation increased, corresponding to emission at higher and higher voltage. The voltage required to obtain $2x10^{-6}$ A (defined as starting voltage here), and the value of FN slope, were recorded for each emitter-probe separation. These values were plotted versus emitter-probe separation, see Figure 4.18a and 4.18b.

d) Conclusion

For emitters of the geometry tested in this experimental apparatus, the starting voltage depended strongly on tip-probe separation - if the probe was positioned 1μm away from the tip instead of 2μm, the starting voltage was halved. Therefore, it was very important that positioning of the probe in the adapted SEM was carried out as accurately as possible.



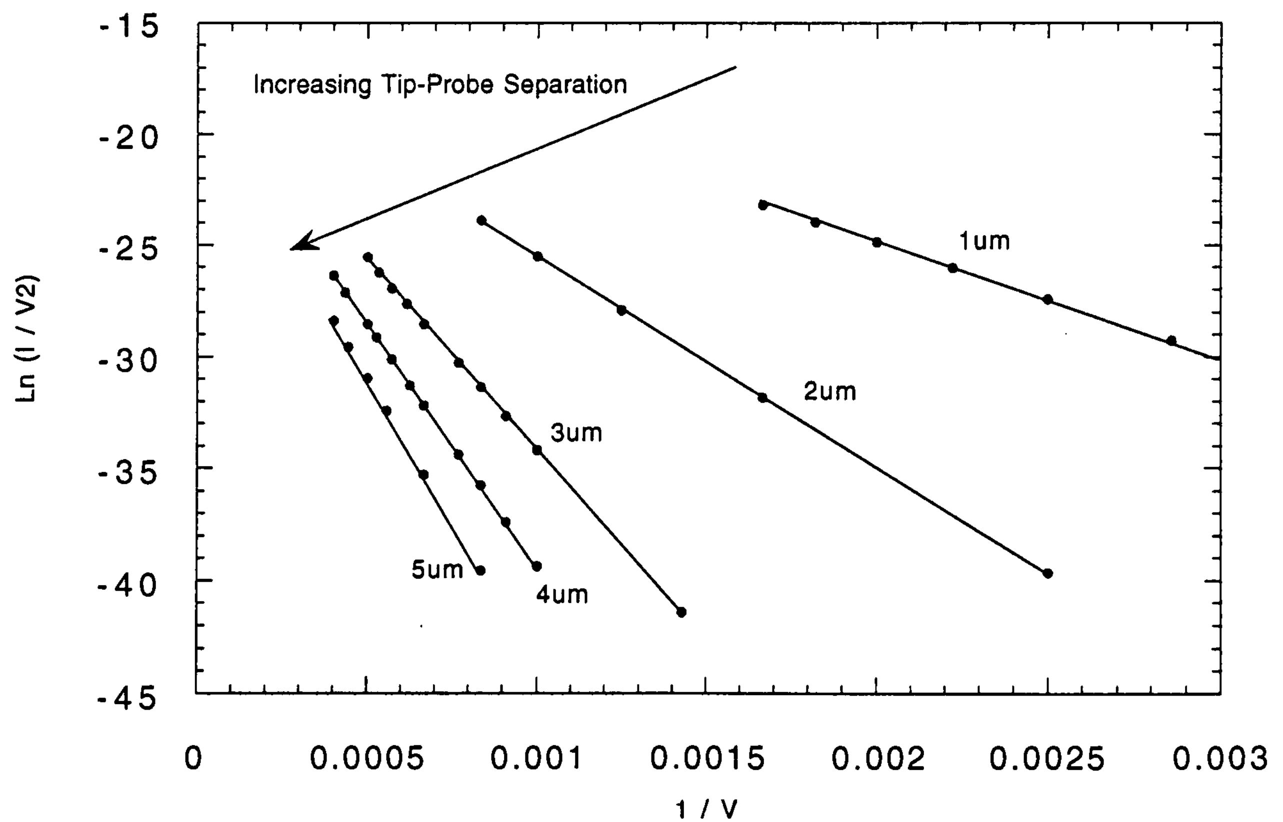
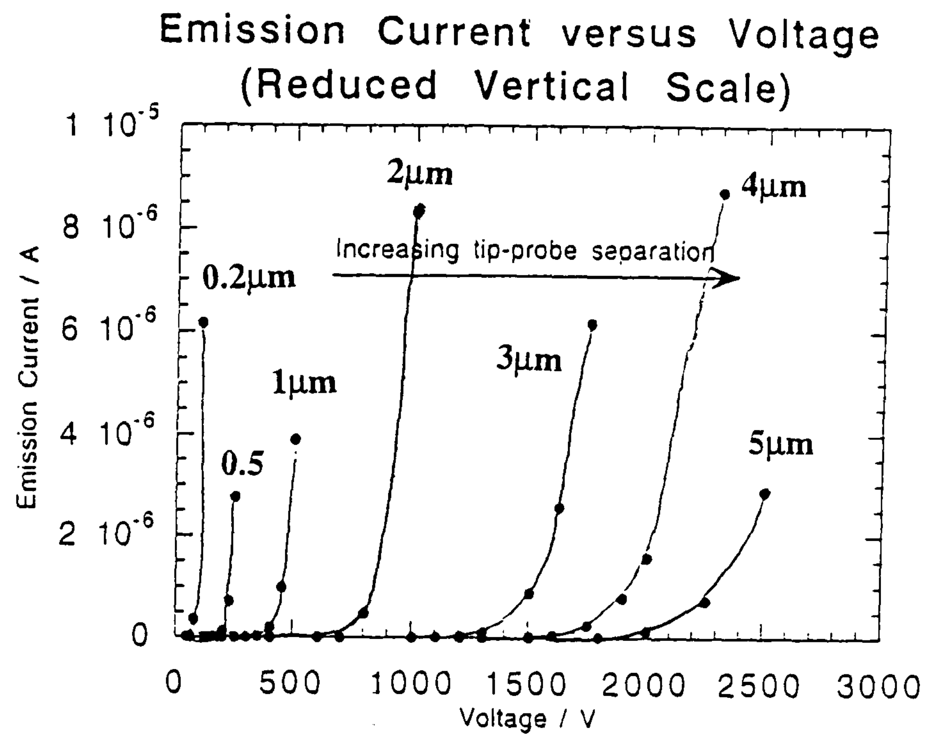
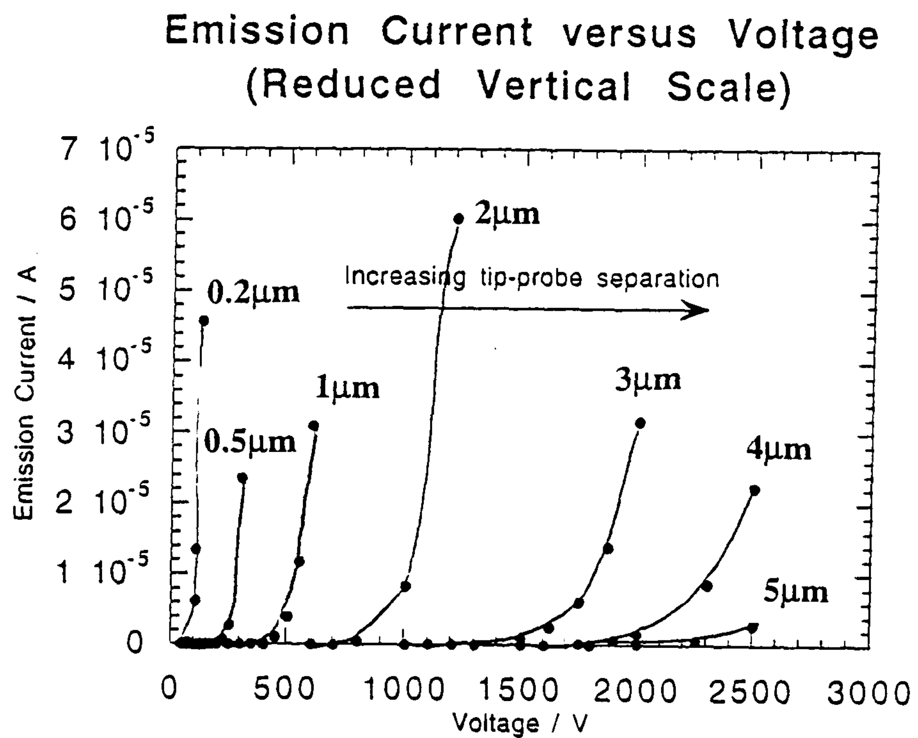


Figure 4.17a & b - Results from Computer Modelling of Tip-Probe Separation Fowler-Nordheim Plots (80° tip only)





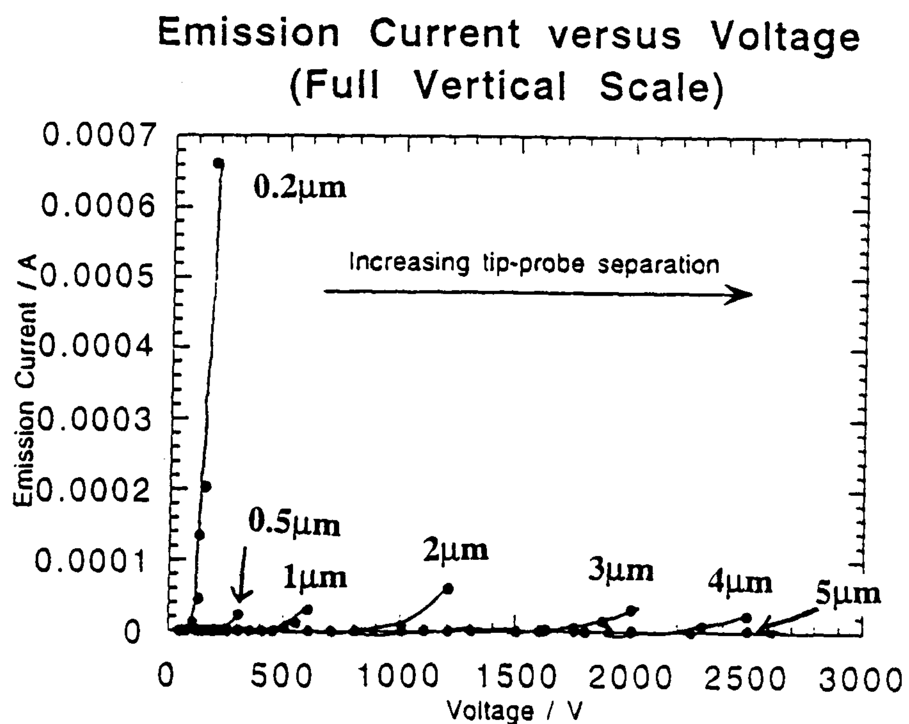
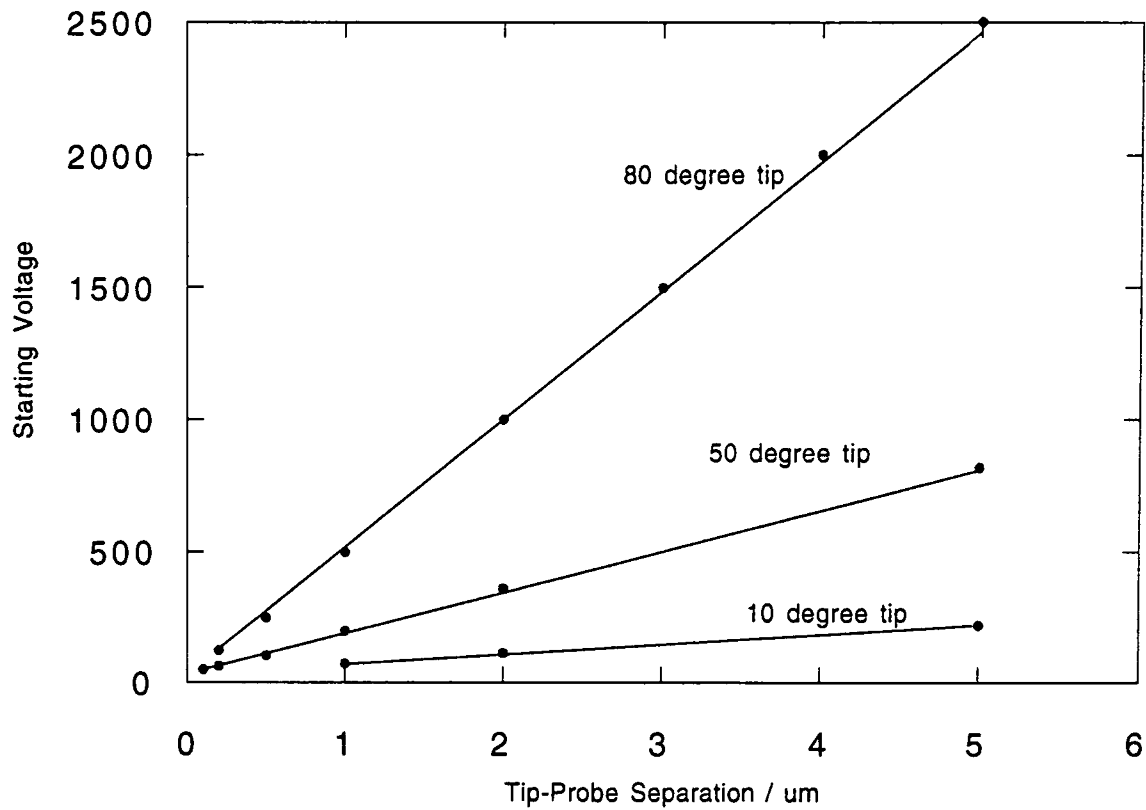


Figure 4.17c) - Current-Voltage Characteristics from Computer Modelling (for 80° tip only)

a) Starting Voltage versus Tip-Probe Separation (Starting Voltage is defined as Voltage Required to Obtain $2x10^{-6}A$)



b) Calculated Value of Fowler-Nordheim Slope versus Tip-Probe Separation

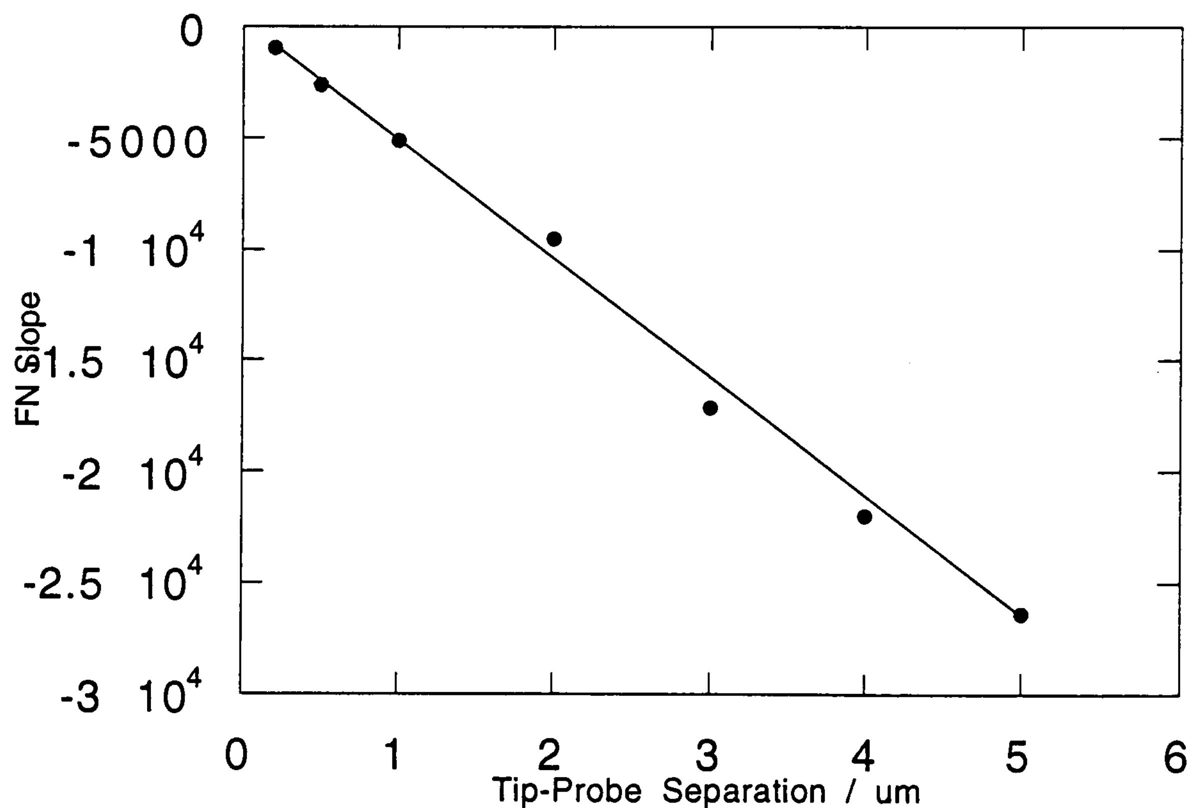


Figure 4.18 - Modelling Results Showing Starting Voltage (10°, 50° and 80° tips) and Fowler-Nordheim Plotted versus Tip-Probe Separation (80° tip only)

4.5.2 Linear Dependence of Starting Voltage on Vertical and Lateral Tip-Probe Separation

An experiment was carried out in order to check that the starting voltage increased linearly as the emitter-probe separation was increased. The separation was increased by the same increment each time, by using the micrometer attached to the cold stage. The starting voltage was recorded for each incremental increase.

a) Vertical Separation

Unfortunately, the initial emitter-probe separation was not known. Therefore, it was not possible to plot the starting voltage versus the exact emitter-probe separation. Therefore, starting voltage was plotted versus the incremental increase instead, see Figure 4.19. The plot is not truely linear. Also, the starting voltage did not double as the tip separation doubled. This suggests that there was some movement of the cold stage in a lateral direction, at the same time it was moved in a vertical direction.

b) Lateral Separation

In addition, the dependence of emission current on the lateral emitter-probe separation was investigated. The lateral emitter-probe separation could be approximated from the SEM image. A plot of emission current versus separation is shown in Figure 4.20. The current dropped off rapidly within ~1μm of the centre of the tip. It is clear that not only positioning in the vertical direction, but also positioning in the lateral direction was important.

4.5.3 Variation in Emitter-Probe Separation from Tip to Tip

The accuracy with which the probe could be re-positioned above the same tip a number of times was investigated. This was carried out in order to give an indication of the accuracy with which the tip-probe separation could be kept constant, from tip to tip across an array and from sample to sample. To maintain a similar probe-emitter separation, the routine summarised in Figure 4.22 was carried out for each new emitter examined.

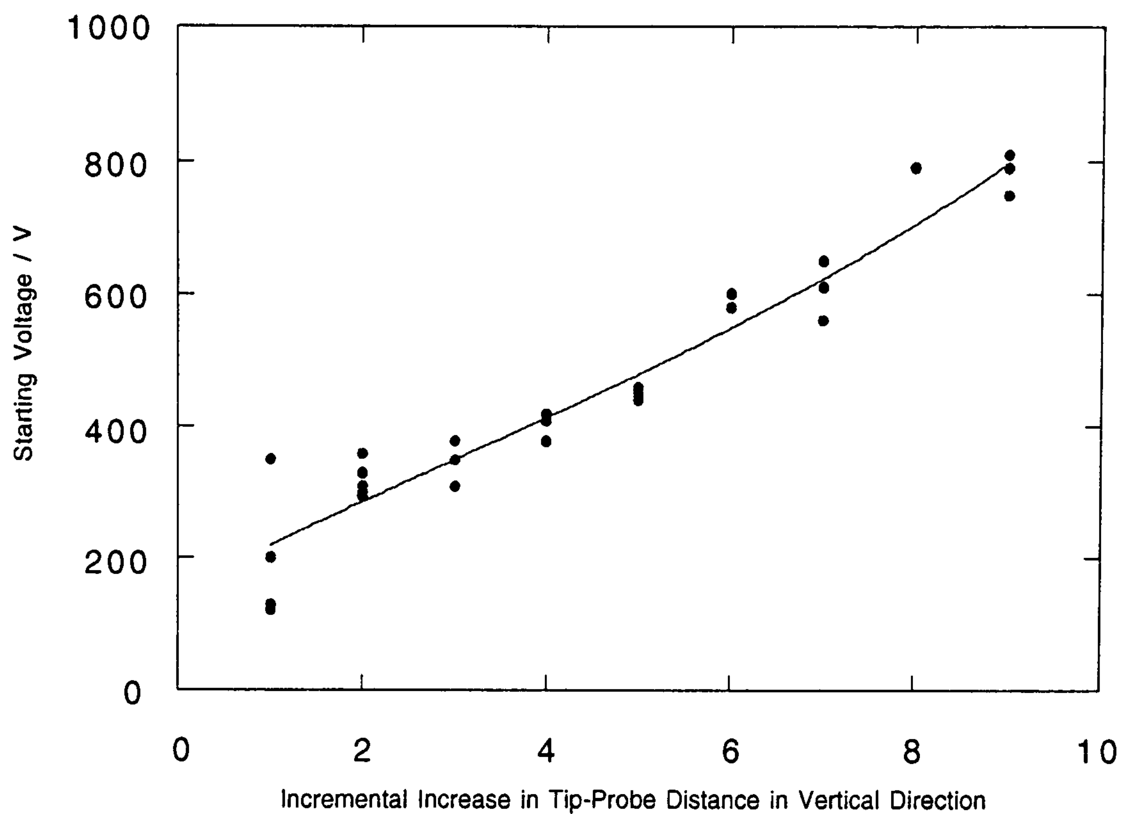


Figure 4.19 - Dependence of Starting Voltage on Incremental Tip-Probe Separation Measured Experimentally
Data was obtained by measuring the starting voltage as the tip-probe separation was increased. This plot shows that the dependence of starting voltage on tip-probe separation is not truely linear. It suggests that when the cold stage was moved, there was some lateral movement of the stage at the same time as vertical movement.

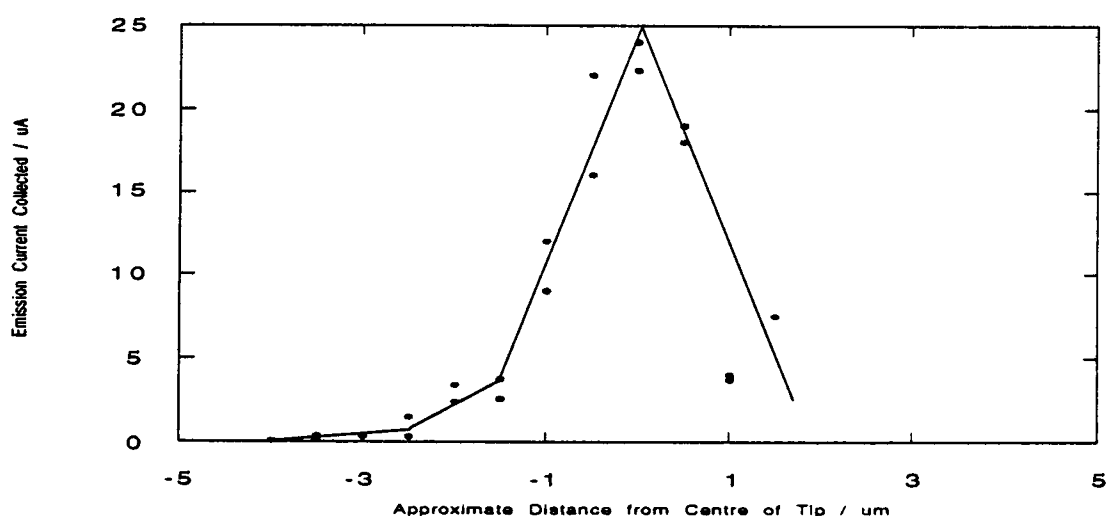
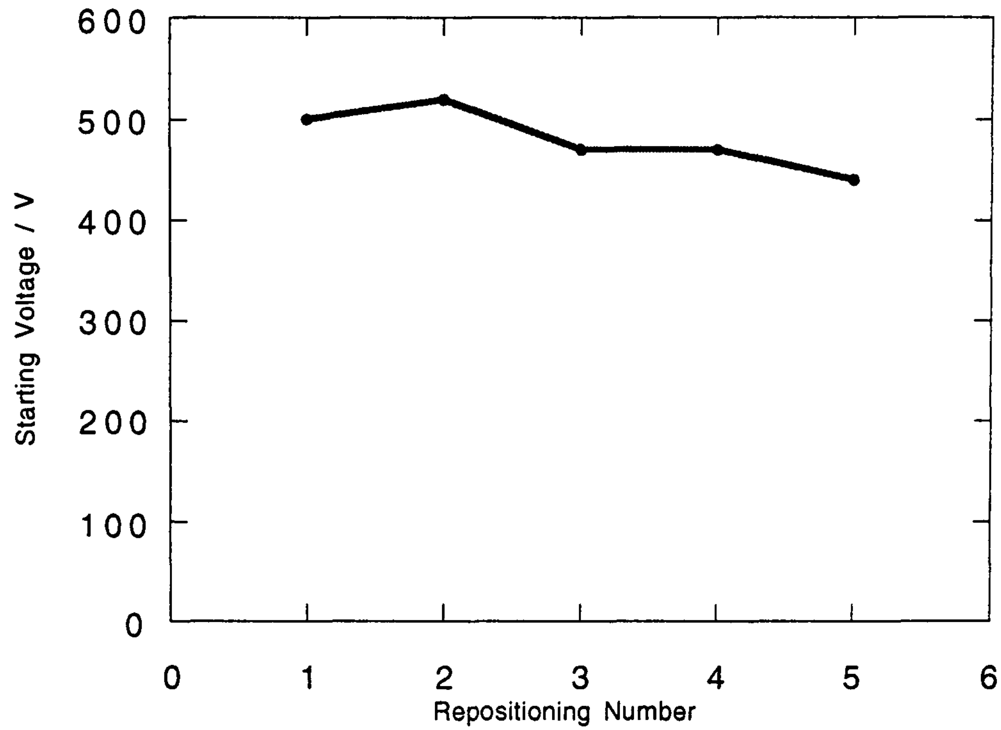


Figure 4.20 - Starting Voltage Plotted versus Incremental Increase in Tip-Probe Separation
Data for this plot was obtained by keeping the voltage on the probe the same, moving the probe and reading the emission current off a digital voltmeter. This plot shows that positioning of the probe in a lateral direction was important, in addition to positioning in the vertical direction.



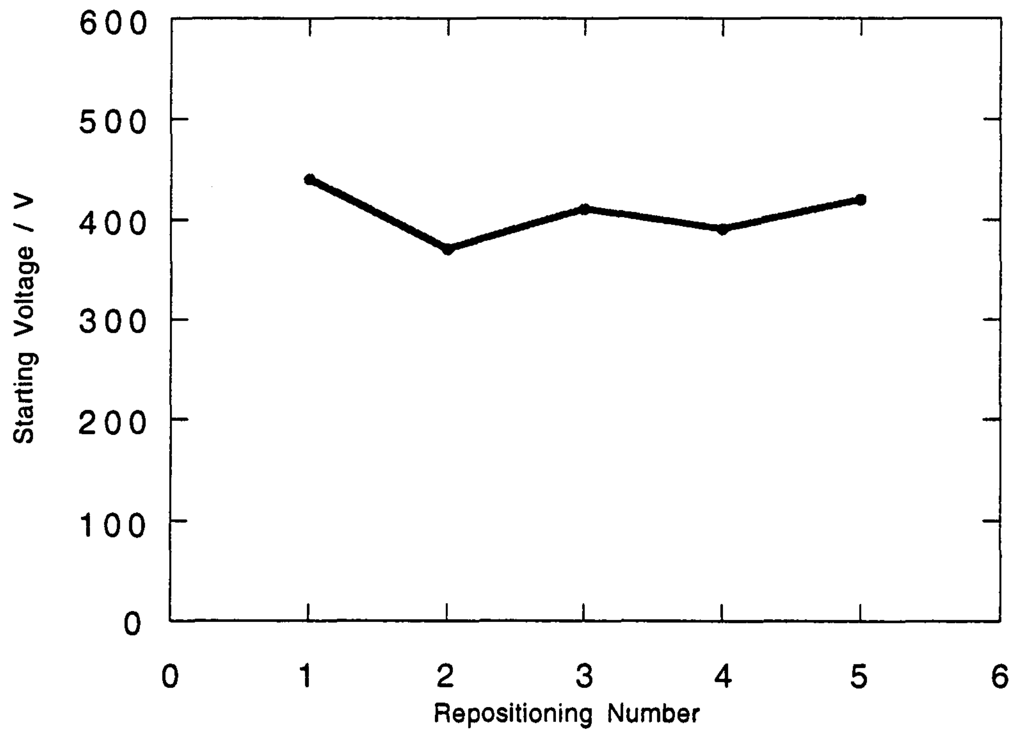


Figure 4.21 - Starting Voltage versus Number of Times that Probe has been Repositioned

To obtain data for this plot, the probe was re-positioned above the same tip a number of times, using the routine shown in Figure 4.22. After each re-positioning, the starting voltage was taken. The intention of these tests was to give a measure of the accuracy with which the probe could be positioned from tip to tip across an array.

1) The emitter to be tested was selected.

2) The probe was placed in contact with an immediate neighbour, causing a reading on a digital voltmeter (DVM) attached to the specimen earth.

3) The probe was moved so that contact with the neighbour was just lost, i.e. the probe-emitter separation was as small as possible. This was confirmed by simultaneously watching the probe, which would vibrate slightly on losing contact with the tip. As the probe lost contact with the tip, the DVM reading dropped to zero.

4) The probe was then moved above the emitter selected to be examined and field emission tests were carried out.

This routine was carried out in order to keep the tip-probe separation as constant as possible, from tip to tip and from sample to sample.

Figure 4.22 Routine Carried out to Position Probe Above Emitters

Figure 4.21 shows a typical plot of starting voltage versus run number. The first starting voltage was at 500V, dropping to 440V for the fifth starting voltage, i.e. ~12% less than for the first starting voltage. Therefore, even when this routine was used, there was still error when attempting to re-position the probe over the same tip.

4.5.4 Summary

In summary, computer modelling and testing has shown that for emitters of the geometry tested in this experimental apparatus, the probe is very sensitive to emitter-probe separation. In order to maintain as similar a separation as possible, from emitter to emitter, the same procedure has been used each time the probe is positioned above a tip. However, testing also showed that even if this routine was used, there was some variation in probe-separation when repositioning above the same tip, or when testing across an array.

4.6 Effect of Series Resistance on Field Emission Data

As outlined in Chapter 2 (Section 2.6.3), a resistor placed in series with an emitter should protect it from premature self-destruction. The effect of series resistance on the maximum emission current was investigated here. In the poor vacuum, a silicon FEA was examined with the following values of resistor in series with the probe - 0Ω, 1kΩ, 10kΩ, 100kΩ, 1M Ω, 10MΩ (in poor vacuum). To change the resistor value over, the microscope had to be re-opened. A plot of maximum field emission current versus series resistor value, is shown in Figure 4.23. This shows that the resistor value had a significant effect on the maximum emission current collected in the poor vacuum.

In the improved vacuum, an external 20MΩ resistor could be added to the external high-voltage lead adjoined to the probe. Therefore, one particular tip could be tested with different values of series resistor, without re-exposing the FEA to air. With the 20MΩ resistor in series, a particular emitter was selected and a field emission run was carried out. The resistor was then removed, so that only a 0.67MΩ resistor was left in series. A second field emission run was then taken. The I-V plots from one emitter are shown in Figure 4.24. For the first run (with a 20.67MΩ resistor in series), 30μA was obtained from the

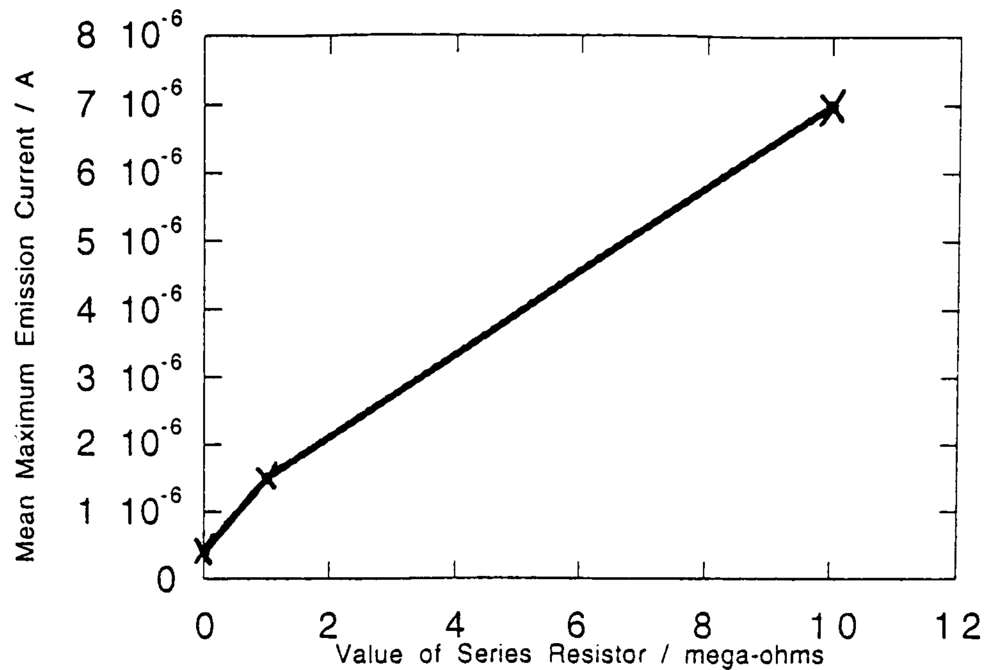


Figure 4.23 - Plot of Maximum Emission Current versus Series Resistor in Parallel with Probe (Poor Vacuum)
This plot shows that in the poor vacuum, the value of the series resistor had a large effect on the maximum emission current.

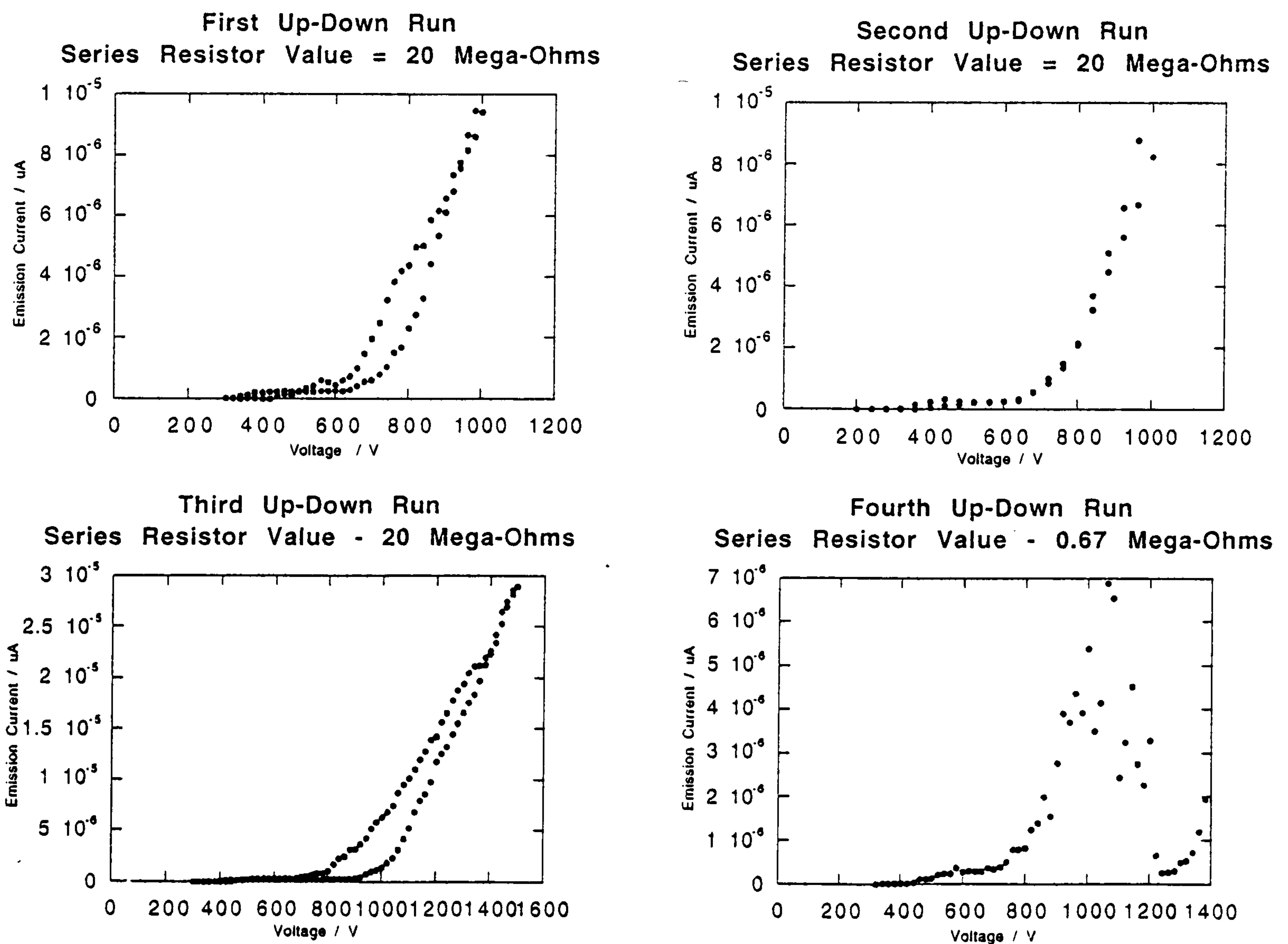


Figure 4.24 - IV Plots Obtained Using Variable Resistance in Series with Probe (Improved Vacuum System)
This figure shows that when a large resistance was placed in series with the emitter, the tip was protected - an emission current up to 30μA was obtained. However, when this resistor was removed the emitter blew at 7μA.

emitter. However, when the resistor was reduced to 0.67MΩ, the tip blew at ~1μA. Each time a tip was examined after the series resistance was reduced to 0.67MΩ, the tip blew before reaching the current achieved with a 20.67MΩ resistance in series. However, if the 20.67MΩ resistor was left in series, the tip did not blow.

The results from both experiments confirm that the value of maximum emission current were influenced by the series resistor value. Therefore, the same resistor value was used in all experiments. Otherwise, it would not have been possible to compare the results from samples examined with different resistors in series.

4.7 Overall Summary

The reproducibility of the results obtained in the adapted SEM were improved since this work began. However, the system was not perfect for field emission studies of ungated FEAs. The main issues were:

- The exact probe-sample separation could not be measured, and this separation still varied slightly from emitter to emitter. Also, the probe was not as stable as desired.
- The samples were not clean on entering the vacuum and it was not possible to clean them in-situ. (However, one 'advantage' is that the vacuum is close to the vacuum that may exist in a working device. Therefore, testing was more realistic, than testing carried out under ultra-high vacuum conditions.)

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Chapter 5 - Preparation of Uniform Silicon Field Emitter Arrays

This chapter describes the methods used to fabricate single crystal silicon field emitter arrays (FEAs). The fabrication of polycrystalline silicon FEAs is also briefly described. The main steps carried out in order to fabricate silicon FEAs were:

1) Oxidation of the flat silicon substrate
2) Photolithography to pattern the oxide layer, to form square oxide masks.
3) Chemical wet etching beneath the oxide masks to form silicon emitters.

These steps will be described in detail in the following sections.

Although the basic processes are similar to those used during the course of the Part II project, the resulting structures have been studied in more detail during the present work, in an attempt to obtain the most uniform FEAs possible, with the equipment available.

5.1 Step I: Oxidation of Wafers

The silicon samples were placed at the hottest zone of a tube-furnace. Before entering the furnace, oxygen was bubbled through cold water, in order to 'wet' it. Ellipsometer measurements indicated that 0.17μm of thermal oxide was formed on the silicon surface if a sample was left in the furnace for 5 hours at a temperature of 950°C.

Process Issues Included the Following:

a) Before oxidation, samples were cleaned and dried. However, additional dust deposited onto the specimen surface from the furnace walls, causing non-uniformities in the oxide layer.
b) The hot zone of the furnace tube was non-uniform. This caused variations in the oxide thickness, from sample to sample (as well as across samples), manifested as variations in the oxide colour.

5.2 Step II: Contact Photo-Lithography

Photo-lithography was used to form an array of oxide masks lying on the top surface of the silicon substrate. Figure 5.1 outlines the individual steps and experimental details of the

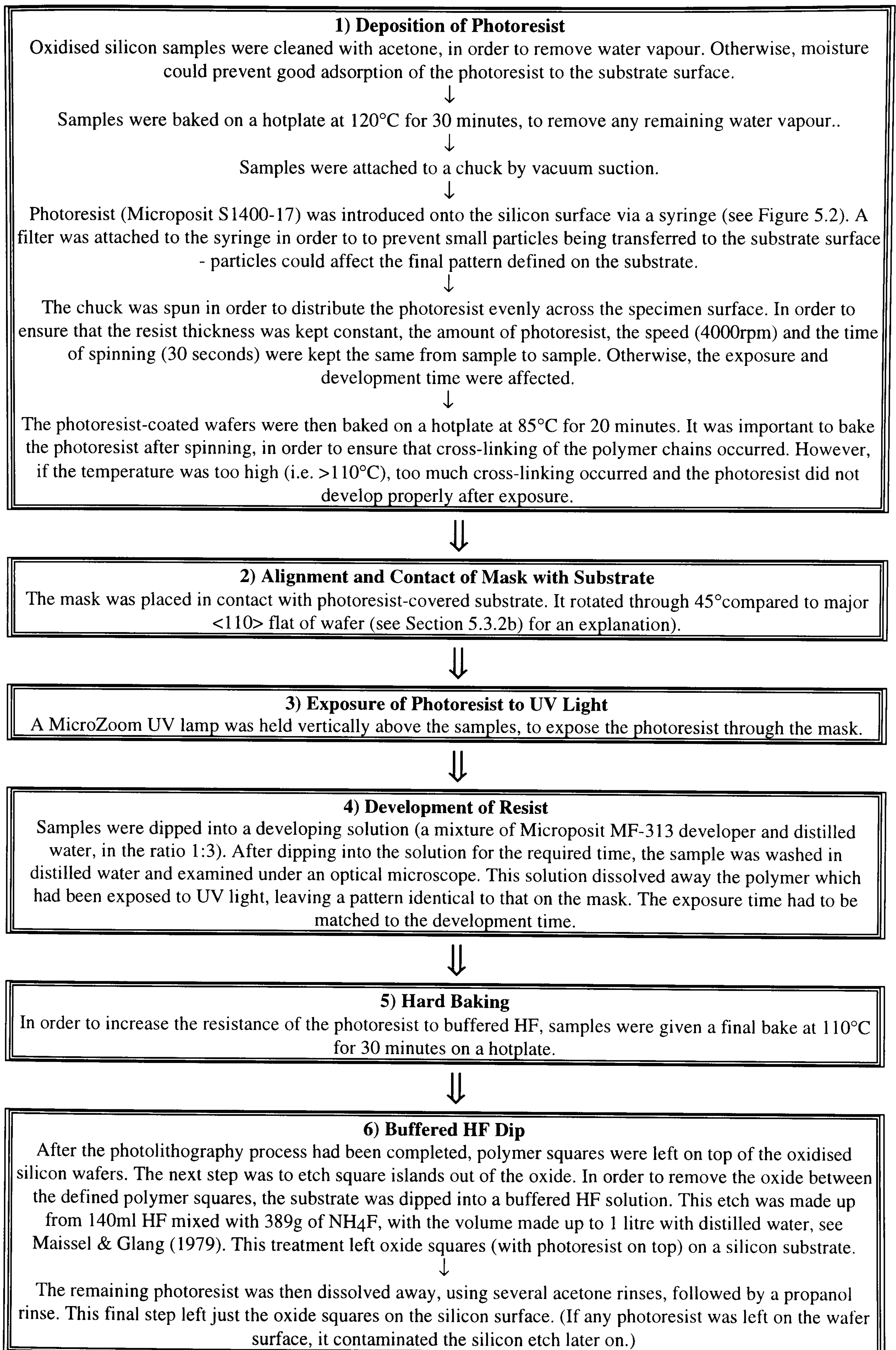


Figure 5.1 Photolithography Process

photo-lithography process. First, photo-sensitive polymer (photo-resist) was spun onto the oxidised silicon surface, see Figure 5.2. It was then exposed to ultra-violet (UV) light shone through a mask. The exposed photoresist was then developed, leaving a polymer copy of the mask pattern on the top surface of the oxidised substrate. The oxide between the photoresist squares was removed using a buffered HF dip. The remaining photoresist was then removed using acetone. This left square oxide masks on the top silicon surface.

A positive resist process was used. In this process, regions of photoresist exposed to light were preferentially dissolved away using a developing solution, as demonstrated in Figure 5.3. The glass mask through which UV light was shone, was 4 inches wide. In this work, the mask was patterned with squares of side 5μm by 5μm and 15μm spacing, and was a light-field mask. When used in conjunction with a positive resist process, a pattern of squares was defined in the resist, see Figure 5.3.

Process Issues Included:

a) **Mask/Substrate Contact** - The mask had to make even physical contact with the silicon wafer during exposure to UV light. Otherwise, vibration of the chuck occurred, causing an irregular pattern to be defined on the substrate due to poor contact. Unfortunately, a good contact was sometimes difficult to achieve. This was because the wafer sections did not cover all the air holes on the chuck surface (original wafers were too large and had to be cut down for processing).

b) **Balance of Exposure and Development Times** - There were fluctuations in the ideal exposure time from session to session, over the course of several months. This was due to changes in the intensity of the UV lamp. An increase in lamp intensity reduced the ideal development time. Development time had to be matched to the correct exposure time. Therefore, if the exposure time changed, the ideal development time also changed. Keeping the sample in the developing solution longer than the ideal time, resulted in either partial or complete removal of the photoresist squares, in addition to the unwanted photoresist.

c) **Imperfect Replication of Mask Pattern** - It was difficult to replicate the mask pattern exactly. Perfect squares were rarely obtained. SEM studies presented in Section 5.3 show that even if resist 'squares' appeared to have equal sides under the optical microscope, examination at higher magnification in an SEM often showed that one side of the 'square' was longer than the other. Unfortunately, when the etching process was carried out, these sub-micron scale differences caused variations in the tip geometry across the sample, see Section 5.3.

5.3 Etching of Silicon to Form Tips

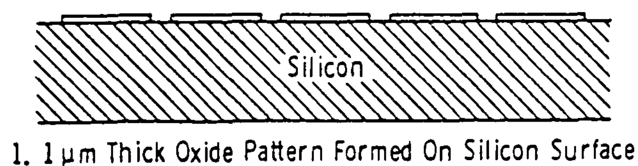
The etching process used to form silicon tips is demonstrated in Figure 5.4 and the experimental details are summarised in Figure 5.5. Figures 5.6a-e shows optical micrographs of FEAs at different stages of etching. The intersection of the underlying silicon tip and the oxide mask decreased as the etch time increased. At the point at which the oxide masks dropped off, tips were thought to be ~2.5μm high.

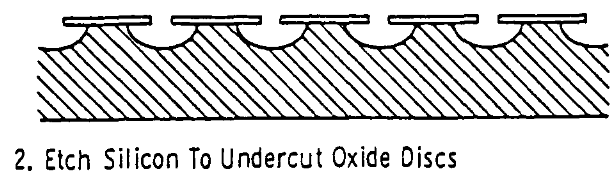
The aim was to obtain the most uniform FEA possible, with the apparatus available. In order to do this, TEM analysis was carried out to check the morphology of the tips produced. A high resolution x4000 JEOL JEM transmission electron microscope was used and operated at 400kV. A LaB_6 filament provided an electron beam with high brightness and low energy spread. This microscope was chosen because selected area images could be obtained at very high resolution, using a CCD camera and TV screen to help focus the microscope image.

Figure 5.7 summarises the steps required to prepare FEA samples for TEM analysis. In order to identify the etching conditions which produced the most uniform starting voltage from tip to tip, field emission measurements from FEAs etched to three different stages were investigated in the SEM. The results are summarised in the following sections.

5.3.1 Flat-Topped Tips (Etch Stopped with all Masks Still in Place)

These sets of samples were removed from the etch while the silicon tips were still in contact with their oxide masks. This corresponded to the situation shown in the optical micrograph





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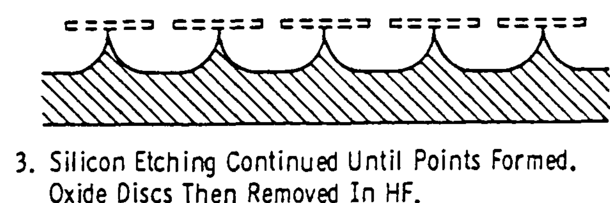
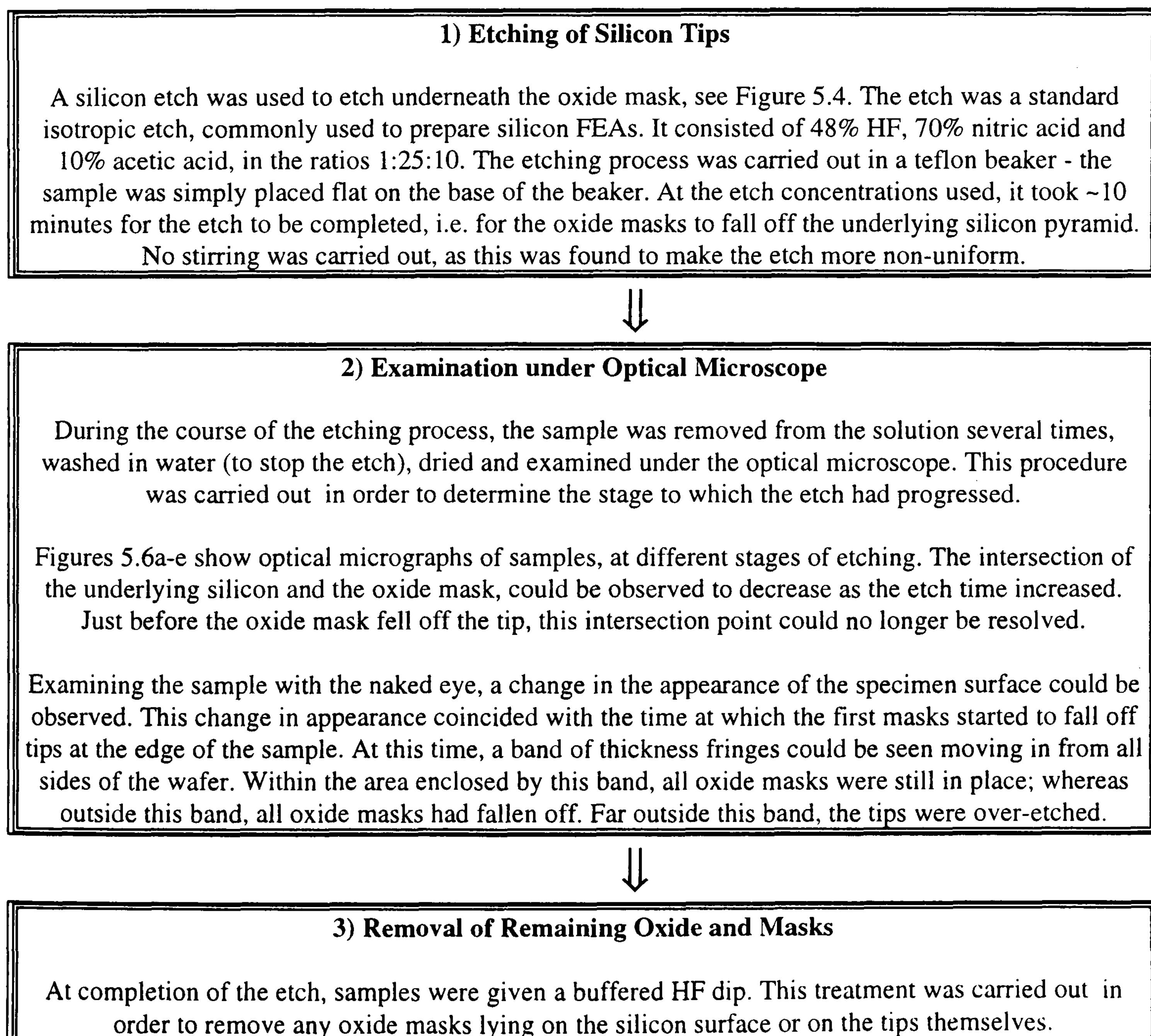


Figure 5.4 - Schematic Diagram of Etching Process Used to Produce Silicon Tips



1) Etching of Silicon Tips

A silicon etch was used to etch underneath the oxide mask, see Figure 5.4. The etch was a standard isotropic etch, commonly used to prepare silicon FEAs. It consisted of 48% HF, 70% nitric acid and 10% acetic acid, in the ratios 1:25:10. The etching process was carried out in a teflon beaker - the sample was simply placed flat on the base of the beaker. At the etch concentrations used, it took ~10 minutes for the etch to be completed, i.e. for the oxide masks to fall off the underlying silicon pyramid. No stirring was carried out, as this was found to make the etch more non-uniform.

⇓

2) Examination under Optical Microscope

During the course of the etching process, the sample was removed from the solution several times, washed in water (to stop the etch), dried and examined under the optical microscope. This procedure was carried out in order to determine the stage to which the etch had progressed.

Figures 5.6a-e show optical micrographs of samples, at different stages of etching. The intersection of the underlying silicon and the oxide mask, could be observed to decrease as the etch time increased. Just before the oxide mask fell off the tip, this intersection point could no longer be resolved.

Examining the sample with the naked eye, a change in the appearance of the specimen surface could be observed. This change in appearance coincided with the time at which the first masks started to fall off tips at the edge of the sample. At this time, a band of thickness fringes could be seen moving in from all sides of the wafer. Within the area enclosed by this band, all oxide masks were still in place; whereas outside this band, all oxide masks had fallen off. Far outside this band, the tips were over-etched.

⇓

3) Removal of Remaining Oxide and Masks

At completion of the etch, samples were given a buffered HF dip. This treatment was carried out in order to remove any oxide masks lying on the silicon surface or on the tips themselves.

Figure 5.5 Silicon Etching Process Used to Produce Tips

in Figure 5.6d. The oxide mask was then removed using a buffered HF dip. Figure 5.8 shows SEM and TEM images of emitters, before and after the mask fell off. Figure 5.9 shows TEM images of flat-topped emitters having an apex ~0.5μm wide. These images show that in the apex region the tips were near-vertical. Figure 5.10 shows high magnification images of the tip corners - the radius at each corner is ~5nm, i.e. very sharp. The etch is not quite isotropic - an isotropic etch would have been expected to produce a more curved profile similar to that shown in Figure 5.4. Other researchers have obtained similar geometries by etching silicon in the same solution, see Thomas *et al.* (1974), Ravi *et al.* (1991) and Hariz *et al.* (1995).

The etch rate varied over the specimen surface. Figure 5.11 shows images of emitters observed at different parts of the wafer. Tip 1 was from the centre of the wafer, the width of the apex being ~200nm; whereas Tip 3 was from the edge of the wafer, the width of the apex being only ~10nm. These images indicate that the etch rate at the wafer edge was faster than in the centre.

5.3.2 Tips Etched Until Masks at Very Edge Fell Off (i.e. Slightly Over-Etched - Masks in Centre of Sample Still in Place)

These sets of samples were etched until the masks at the edge of the sample had fallen off. TEM studies showed that the uniformity of tip geometry across the array was poor for the following reasons:

a) Non-Uniform Etch

The etch rate was non-uniform across the sample. Figure 5.12b) shows an array of tips etched until the masks at the edge of the sample had just fallen off. Whereas some emitters had formed points, others were still under-etched and were flat topped. This sample was much less uniform than the under-etched flat-topped samples shown in Figure 5.12a). Similar problems of non-uniformity were observed by Thomas *et al.* (1974), although they found that rotating the sample during etching improved the etch uniformity. In this work agitation during etching was investigated, but appeared to decrease the tip to tip uniformity further.

b) Differences in Morphology - Wedges versus Points

Previous experiments during the Part II project had shown that tips with edges lying along the <100> direction consistently etched to form a point-like apex, see Boswell (1992) and Boswell & Wilshaw (1993); whereas tips with edges lying along the <110> direction (i.e. parallel to the flat of the wafer) consistently formed a wedge-like apex, even though the base of each emitter was originally square. Figure 5.13 shows SEM images of both a point and wedge-like tip formed on a wafer aligned along the <100> direction. The difference was attributed to a crystallographic dependence of the etch, although the etch was supposed to be isotropic. Clearly, a point-like apex was preferred to a wedge-like apex. Therefore, in order to obtain point-like apexes, subsequent wafers were rotated through 45° so that the edges of squares were approximately aligned along the <100> direction. (A crystallographic effect of this etch was observed by Thomas *et al.* (1974). They found that knife-edged emitters were obtained on a (110) wafer, but that sharp pyramids were formed on (100) and (111) wafers. The authors found that although these knife-edged emitters were very sharp, emission was poor and uneven.)

Unfortunately, in the work for the present thesis, it was found that even if the sample was aligned along the <100> direction, both wedge and point-like apexes were formed during etching. The formation of wedges is now thought to have been due to the limitations of the photolithography process, see Figure 5.13c). Figure 5.14 and 5.15 show SEM micrographs of point-like and ridge-like apexes respectively. Figure 5.14a) shows that the side parallel to the direction of the ridge is actually ~500nm longer than the other side. The ridge itself was ~500nm long. The sides of the emitters shown in Figure 5.15 (having point-like apexes), were equal. Figure 5.16 demonstrates the formation of emitters having wedge-like apexes. As the emitters (such as tips 1&2) were etched, their masks fell off and they became over-etched (see tip 3), eventually forming a wedge-like apex (see tip 4). It was possible to tell that these emitters were ridges because the thickness fringe pattern indicates that the tips are very thin in the direction perpendicular to the paper, and because the apex was very electron transparent.

The formation of ridge-like apexes versus point-like apexes were also reported by other researchers, and also appear to have been caused by problems with the accuracy of the optical lithography process. Ravi *et al.* (1991) found it was almost impossible to prevent the formation of wedges with either wet or dry etching. In addition, Marcus *et al.* (1991) found that the separation of the two parallel edges of a nominal 10μm square masking pad could vary by ±0.1μm, and that this variation dominated the resulting tip morphology. To prevent this problem, the authors suggested a switch to a more precise type of lithography, e.g. electron beam/X-ray lithography. In the current work, this was not possible.

c) Determination of End Point

Even if the etch rate had been uniform, determining the end-point of the etch would still have been difficult. The aim was to remove the sample from the etch just at the moment that the oxide masks fell off. However, this was difficult due to the following reasons:

i) It was easy to miss this end-point and over-etch the tips. The smallest object resolvable under the optical microscope was ~500nm. However, the dimensions of the apex just before the oxide mask fell off would have been much smaller than this. As the etch rate changed from sample to sample, it was not possible to work out the exact etch time and re-apply this to other samples. Therefore, the progress of the etch on removal from the solution was different from sample to sample.

ii) It was possible for the etch to eat away the silicon, at a distance below the point of contact with the mask, see Figure 5.17. If this occurred, the overall emitter height was then lower than neighbouring tips.

iii) When the contact area between the silicon and mask was very small, it was noticed that the drying process could blow off the masks. This is believed to be because the mechanical stability was reduced. This may have occurred during checking of the etch progress, resulting in tips having different morphology compared to neighbouring tips.

5.3.3 Very Over-Etched Tips (Etched Until All Masks Across Sample Fell Off)

For some samples, etching was carried out until all masks across the wafer had fallen off. Table 5.1 summarises the morphology and tip radius of 14 randomly chosen emitters examined on one sample. From these 14 tips, 5 had a wedge-like apex and the tip radii varied within the range 10-35nm. In this case, examination showed that for all tips, the vertical part of the apex had been etched away. Tip morphology varied from neighbour to neighbour. Figure 5.18a shows three neighbouring emitters from such a sample, the middle emitter having a wedge-like apex. In addition, Figure 5.18b shows a tip (tip 2) which appears to be a sharp point. However, closer examination shows that the tip was actually a wedge. Figure 5.19 shows higher magnification images of such a tip, which has been tilted to show the ridge. Figure 5.20 shows six neighbouring tips, each having a different morphology, to further emphasise the non-uniformity from tip to tip.

5.3.4 Comparison of Field Emission Properties

The field emission properties of FEAs (20 tips tested/FEA) produced by etching for different times were examined using the adapted SEM. The results are summarised in Table 5.2 and Graph 5.1. It is clear from these tables, that the lowest starting voltages were obtained from under-etched (flat-topped) tips; whereas the highest starting voltages were obtained from over-etched (point/wedge-like) tips. The values of starting voltage for over-etched tips was almost twice that of flat-topped under-etched tips. The standard deviation and range of starting voltage for flat-topped emitters were much lower than for over-etched emitters.

It is thought that flat-topped under-etched emitters had the lowest starting voltage because the aspect ratio was high, (due to very sharp corners ~5nm in radius and near vertical sides in the apex region). The values of FN slope in Table 5.2 indicate that the field enhancement was higher than for other samples. In addition, the flat top had 4 corners from which emission could occur. For over-etched tips, the vertical sides had been etched away and the tip radii were not as sharp. Therefore, the aspect ratio would have been lower. In addition, there was only one point from which emission could occur.

Tip Number	Type	Radius
1	Point	10nm
2	Point	10nm
3	Point	17nm
4	Point	30nm
5	Wedge	20nm
6	Point	10nm
7	Point	20nm
8	Point	35nm
9	Point	20nm
10	Point	20nm
11	Wedge	10nm
12	Wedge	10nm
13	Wedge	10nm
14	Wedge	10nm

Tips were examined by TEM, and were randomly selected from the array.

Table 5.1 Tip Type and Radius Observed on As-Etched Silicon Array

Parameter	Sample Number	Starting Voltage	Maximum Current	FN slope (m)	FN intercept (c)
Mean Value	1) Flat-Topped Emitter (Ref: F)	507V	30μA	-5897	-18.0
	2) Slightly Over-Etched (Ref: Ne)	560V	9.7μA	-6710	-18.5
	3) Over-Etched (Ref: E)	690V	6 μA	-11255	-14.6
	4) Very Over-Etched (Ref: Fred)	971V	16μA	-17782	-20.3
Spread of Values	1) Flat-Topped Emitter (Ref: F)	420V-600V (i.e. 180V range)	0.5μA-80μA	(-2084)-(-7512)	(-10.4)-(-24.7)
	2) Slightly Over-Etched (Ref: Ne)	325V-980V (i.e. 655V range)	0.7 μA -27 μA	(-1360)-(-19740)	(-4.2)-(-26.5)
	3) Over-Etched (Ref: E)	400V-1100V (i.e. 700V range)	0.5 μA-22 μA	(-3530)-(-23701)	(-2.6)-(-19.1)
	4) Very Over-Etched (Ref: Fred)	570V-1700V (i.e. 1130V range)	6μA-30μA	(-9867)-(-44207)	(-5.5)-(-24.6)
Median Value	1) Flat-Topped Emitter (Ref: F)	500V	14μA	-6845	-17.5
	2) Slightly Over-Etched (Ref: Ne)	550V	8 μA	-6015	-20.3
	3) Over-Etched (Ref: E)	630V	5 μA	-11559	-15.6
	4) Very Over-Etched (Ref: Fred)	918V	15μA	-12382	-23.3
Standard Deviation	1) Flat-Topped Emitter (Ref: F)	±60V (±12%)	±31μA (±100%)	±1972 (±34%)	±3.7 (±21%)
	2) Slightly Over-Etched (Ref: Ne)	±148V (±26%)	±15μA (±78%)	±2153 (±64%)	±5 (±27%)
	3) Over-Etched (Ref: E)	±243V (±35%)	±6μA (±100%)	±5502 (±55%)	±4.4 (±28%)
	4) Very Over-Etched (Ref: Fred)	±350V (±35%)	±6μA (±36%)	±12989 (±68%)	±6.5 (±40%)

Sample 1) TEM showed sample contained only flat-topped emitters

Sample 2) TEM showed that sample contained mostly flat-topped emitters, but also some over-etched emitters where the mask had fallen off.

Sample 3) TEM showed that sample contained both flat-topped and over-etched emitters

Sample 4) TEM showed that sample contained only over-etched emitters

Main points from this table are that the lowest starting voltage and smallest range of values was obtained from flat-topped over-etched emitters. The values of FN slope indicate that flat-topped emitters had a higher and more uniform aspect ratio than the other samples.

20 tips examined per FEA

Table 5.2: Summary of Data Obtained from P-Type Silicon FEAs Etched for Different Times

For tips etched until the first masks fell off, there was a mixture of under-etched and over-etched tips across the sample. This would be expected to result in a wider range of starting voltage than for under-etched tips, where all emitters across the array had the same geometry. As a result, the standard deviation for over-etched FEAs was ~twice that for under-etched tips, and the range was much greater.

The plots of Fowler-Nordheim slope and intercept also indicate that flat-topped emitters have higher field enhancement than for over-etched emitters. This table shows that the emission current obtained from flat-topped emitters was slightly lower than for over-etched emitters. This may be due to the difference in thermal stability between sharp and blunt emitters.

5.3.5 Overall Summary

Summarising, it was clear that the lowest and most uniform emission was obtained from under-etched flat-topped FEAs. The aspect ratio of the emitter and the tip radius from emitter to emitter, were more uniform than for FEAs etched until the masks dropped off.

5.4 Oxidation Sharpening

Oxidation sharpening has been used extensively throughout the literature, in order to obtain atomically sharp silicon tips and wedges, see Marcus *et al.* (1990) and Liu *et al.* (1991). It is reported that this treatment led to a decrease in the operating voltage of FEAs, and to an improvement in tip to tip uniformity. Oxidation sharpening is believed to improve tip uniformity for the following reason. During oxidation, stress builds up at regions of high curvature (e.g. at the apex of an emitter), due to the volume difference of silicon dioxide with respect to silicon, see Marcus *et al.* (1982). However, this stress cannot be relieved at temperatures <1050°C. Kao *et al.* (1987) have shown that this stress build-up leads to an increase in the activation barrier for oxidation, thereby suppressing the reaction and slowing down the oxidation rate. Therefore when one tip becomes sharp, it will not sharpen any further. However, blunter tips will continue to sharpen, until all tips in an array have similar radii.

In the literature, oxidation sharpening was carried out with and without the oxide mask in place, and was reported to produce similar results. In this work, both methods of oxidation sharpening were investigated. The tube-furnace, described in Section 5.1.1, was used to carry out the oxidation process.

5.4.1 Oxidation Sharpening of Tips with Mask Removed

This type of oxidation has been used by Marcus *et al.* (1990), Liu *et al.* (1991), Ravi *et al.* (1991), Trujillo & Hunt (1991), Marcus *et al.* (1991) and Lee *et al.* (1989). Etching was carried out until the first oxide masks at the sample edge fell off. The remaining masks in the centre were removed using a buffered HF dip prior to oxidation.

a) Single Oxidation

Figure 5.21 shows TEM images of neighbouring tips oxidised for 65 minutes at 1000°C. The oxide layer was left in place during examination - it was ~70-90nm thick. The geometry of the underlying silicon tip still varied dramatically from tip to tip, even after this treatment was carried out.

b) Multiple Oxidation Treatments

It was thought that several oxidation treatments would improve the reproducibility of the emitters. Therefore, further oxidation treatments were carried out (each treatment lasting 4 hours at 950°C). Figures 5.22-5.25 show TEM images of emitters oxidised up to seven times. The main results are summarised below:

- Emitters with both point-like and wedge-like apexes were sharpened significantly, tip radii being ~2-3nm following oxidation, compared with up to 35nm for as-etched tips (see Table 5.1).
- However, oxidation did not appear to improve the tip to tip uniformity. Three distinct tip morphologies were still observed, even after seven oxidation treatments:

  i) Emitters with point-like apexes.

  ii) Emitters with edge-like apexes - with ridges parallel to plain of photograph.

  iii) Emitters with edge-like apexes - with ridges perpendicular to plain of photograph.

Similar results were obtained by Ravi *et al* (1991), see Figure 5.26.

c) Field Emission Measurements

The starting voltage of tips which underwent oxidation sharpening 1, 5 and 7 times were recorded and the results are summarised in Table 5.3. It can be seen that the starting voltages were not reduced compared to as-etched FEAs, and there was no improvement in emission uniformity compared to as-etched FEAs.

d) Summary

In this work, it has been shown that oxidation did not improve the emission uniformity or tip to tip geometry of over-etched FEAs. Many researchers have reported that oxidation did improve tip uniformity. It is possible that they had access to better lithography and more uniform etching facilities, in order to obtain more reproducible FEAs, prior to oxidation sharpening.

5.4.2 Oxidation Sharpening with Mask in Place

Some researchers carried out oxidation sharpening by oxidising while the mask was still in contact with the silicon tip, see McGruer *et al.* (1991), Urayama *et al.* (1993) and Liu *et al.* (1992). In this part of the work, oxidation with masks in place was also investigated. The results are discussed below.

a) TEM Studies

Oxidation was carried out at 1000°C for 2 hours. TEM images of the resulting emitters, are shown in Figures 5.27a-f. The thermal oxide layer was not removed prior to examination and was ~200nm thick. [Note: In order to obtain TEM images of the silicon tip still covered in an oxide layer, it was necessary to tilt the specimen to a major pole and concentrate the beam down onto the apex region. Otherwise, the silicon inside was only a faint shadow and could not be easily imaged.] The shape of the underlying silicon tip varied from neighbour to neighbour. This difference is attributed to either a difference in the etch rate prior to oxidation, or to the inaccuracy of the photolithography process used to define the mask.

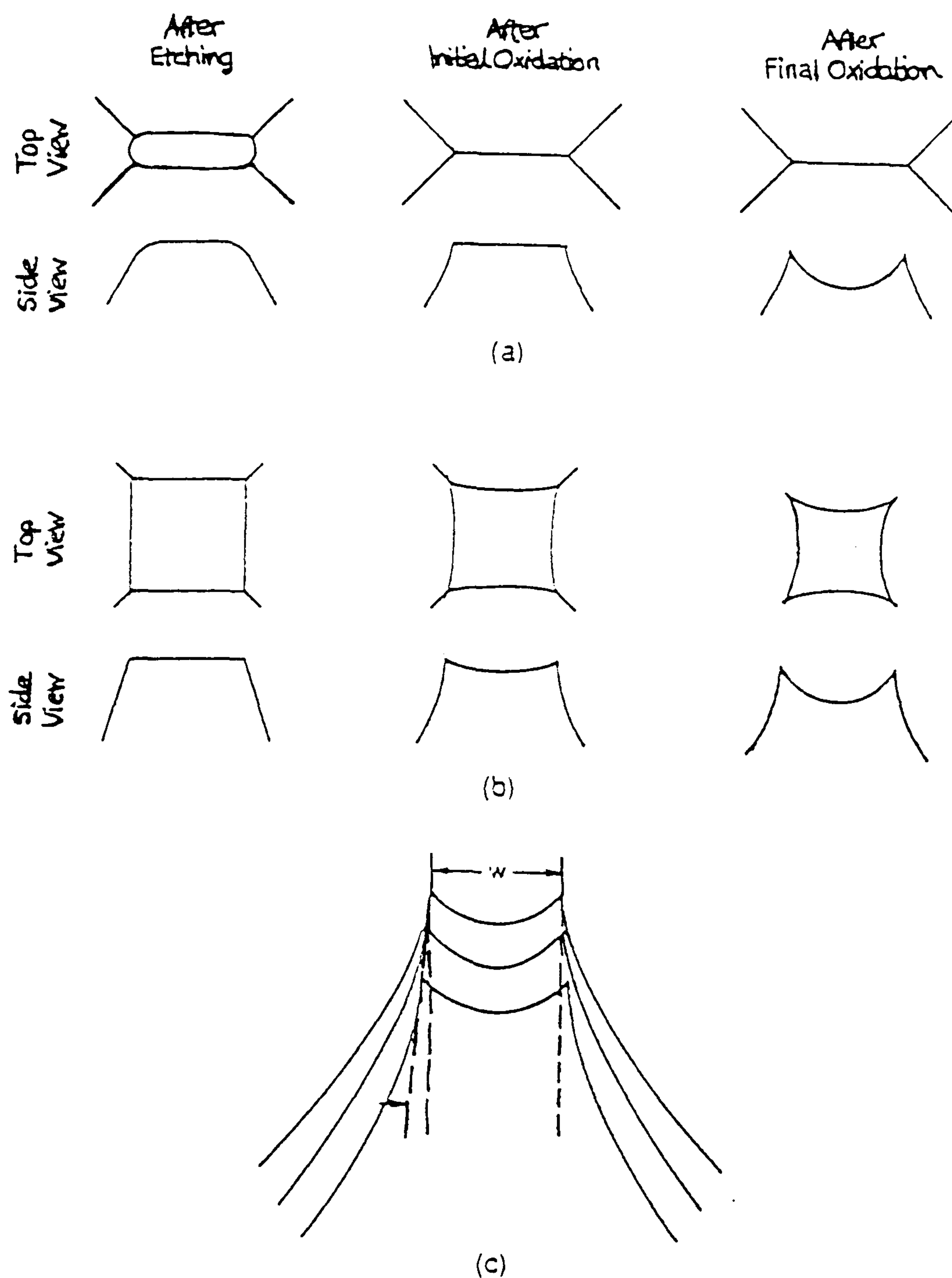


Figure 5.26 - Similar Results Obtained by Ravi *et al.* (1991)
Ravi et al. (1991) also found that wedge-like apexes remained wedges, even after several oxidation treatments were carried out.

a) Shows top and side view of emitter with rectangular cross-section before and after two oxidations.

b) Similar illustration for emitter with square-top geometry before and after two oxidations.

c) Side view of emitter after successive oxidations, showing increasing separation of two or four atomically sharpened tips.

(Ref: T.S.Ravi, R.B.Marcus and D.Liu, *J. Vac. Sci. Technol. B*, **9(6)** (1991) 1733)

Parameter	Sample Number	Starting Voltage	Maximum Current	FN slope (m)	FN intercept (c)
Mean Value	1) 1 Oxidation of over-etched emitter	1140V	20μA	-21272	-11.6
	2) 1 Oxidation of over-etched emitter	1432V	n/a	n/a	n/a
	3) 7 Oxidations of over-etched emitter	1450V	3.3μA	n/a	n/a
	4) 7 Oxidations of over-etched emitter	1309V	1.8μA	n/a	n/a
	5) 1 Oxidation with oxide mask still in place	450V	11 μA	-5489	-18.6
Spread of Values	1) 1 Oxidation of over-etched emitter	300V-1900V (i.e. 1600V range)	4μA-50μA	(-4456)-(-47387)	(-4.9)-(-22.3)
	2) 1 Oxidation of over-etched emitter	800V-2000V (i.e. 1200V range)	n/a	n/a	n/a
	3) 7 Oxidations of over-etched emitter	700V-2224V (i.e. 1524V range)	0.2μA-9μA	n/a	n/a
	4) 7 Oxidations of over-etched emitter	600V-2000V (i.e. 1400V range)	0.02μA-5.6μA	n/a	n/a
	5) 1 Oxidation with oxide mask still in place	313V-672V (i.e. 360V range)	1.3 μA - 37 μA	(-1825)-(-10324)	(12.0)-(-23.5)
Median Value	1) 1 Oxidation of over-etched emitter	1090V	15μA	-20531	-14.3
	2) 1 Oxidation of over-etched emitter	1380V	n/a	n/a	n/a
	3) 7 Oxidations of over-etched emitter	1500V	2μA	n/a	n/a
	4) 7 Oxidations of over-etched emitter	1405V	1.5μA	n/a	n/a
	5) 1 Oxidation with oxide mask still in place	425V	10 μA	-5271	-18.6
Standard Deviation	1) 1 Oxidation of over-etched emitter	±402V (±35%)	±14μA (±70%)	±12062 (±57%)	±8.1 (±70%)
	2) 1 Oxidation of over-etched emitter	±392V (±27%)	n/a	n/a	n/a
	3) 7 Oxidations of over-etched emitter	±494V (±34%)	±3μA (±91%)	n/a	n/a
	4) 7 Oxidations of over-etched emitter	±480V (±37%)	±1.7μA (±95%)	n/a	n/a
	5) 1 Oxidation with oxide mask still in place	±95V (±21%)	±9μA (±90%)	±2868 (±52%)	±3.7 (±16%)

(n/a = not calculated.) These results show that oxidation with the oxide mask still in place produced lower starting voltage, with a lower range of values, than for emitters oxidised with the masks removed. Although the starting voltage was lower than for flat-topped emitters, the range of starting voltage values was higher.

Table 5.3: Summary of Data Obtained from Oxidation-Sharpened Emitter Arrays (20 tips examined per FEA)

The tip shown in 5.27e has the ideal tip geometry. An image of such a tip following removal of the oxide layer, is shown in Figure 5.28. However, most of the tips did not have this geometry. It would be expected that had oxidation had been continued, all tips would have oxidised to produce this morphology. Therefore, longer oxidation times were carried out to see if all the tips in the array would eventually be similar in geometry. However, this was not found to be the case. This was believed to be for the following reasons:

- It was difficult to match the etch time with the correct oxidation time.
- Errors in the photolithography process caused differences in the width of the flat-top and so oxidation still produced some wedge-like apexes.

If sufficient time had been available, it may have been possible to eventually optimise these conditions to produce an array of sharp points.

b) Field Emission Measurements

Results are summarised in Table 5.3 and Graphs 5.2 & 5.3. The mean starting voltage for these samples were the lowest obtained and were slightly lower than for flat-topped emitters. However, the range of starting values was larger than observed for flat-topped emitters.

c) Summary

Oxidation sharpening with the oxide masks kept in place produced tips which had the lowest starting voltages of any of the emitter geometries tested. However, TEM studies showed that the uniformity of the apex geometry from tip to tip was still non-uniform. However, oxidation with the masks still in place was more promising than oxidation without the mask in place. If more time had been available, it may have been possible to optimise the processing to obtain very sharp points across the array.

5.5 Overall Summary - Obtaining Most Reproducible Emitters

For this work, it was decided to use flat-topped emitters as the basic arrays on which to investigate the process of anodisation (although the flat-topped geometry is unusual and would probably not be used in a working device). This decision was made for the following reasons:

i) The uniformity of the tip morphology across the array and from sample to sample was better for flat-topped emitters than for any of the other FEA geometries produced (even emitters oxidised with masks in place).

ii) The starting voltage for flat-topped emitters were lower than for emitters etched for longer times.

iii) The spread of starting voltage values and standard deviation for flat-topped emitters were lower than for emitters etched for longer times. The range of values was also much lower than for emitters oxidised with their masks in place.

5.6 Development of Polysilicon Emitters

In addition to single crystal FEAs, polycrystalline silicon FEAs were also investigated. Much research has been reported in the area of single crystal silicon field emitter technology. However, it would be expensive to manufacture large area displays from single crystal silicon wafers, which are at present limited to a size of 12 inches. Therefore, there are significant advantages to be gained if emitters could be manufactured from polycrystalline silicon deposited onto a glass substrate.

Although several researchers have produced polysilicon emitters, see Busta *et al.* (1993), Aslam *et al.* (1993) and Mei *et al.* (1993), little comparison has been made between the field emission characteristics of single crystal and polycrystalline silicon emitters. Furthermore, TEM examination of the actual structure of the polysilicon emitter tip has not been described.

Polysilicon FEAs reported in the literature were produced by evaporating polysilicon using a Spindt-like process, rather than forming them by polysilicon layer deposition and then etching. In the present work, wet etching was used to form polysilicon emitters. The tip morphologies were examined in the TEM. In addition, the field emission characteristics of polycrystalline and single crystal silicon were compared, in order to find out if there was any difference in the performance of the two materials.

The formation of polysilicon layers on silicon wafers was carried out at GEC. The process is summarised in Figure 5.29. A 0.7μm thick layer of polysilicon was formed on top of a single crystal substrate.

5.6.1 TEM and Field Emission Studies of Polysilicon Tips

The polysilicon wet etched emitters were formed by etching until the majority of oxide masks had fallen off, as in Section 5.3.3.

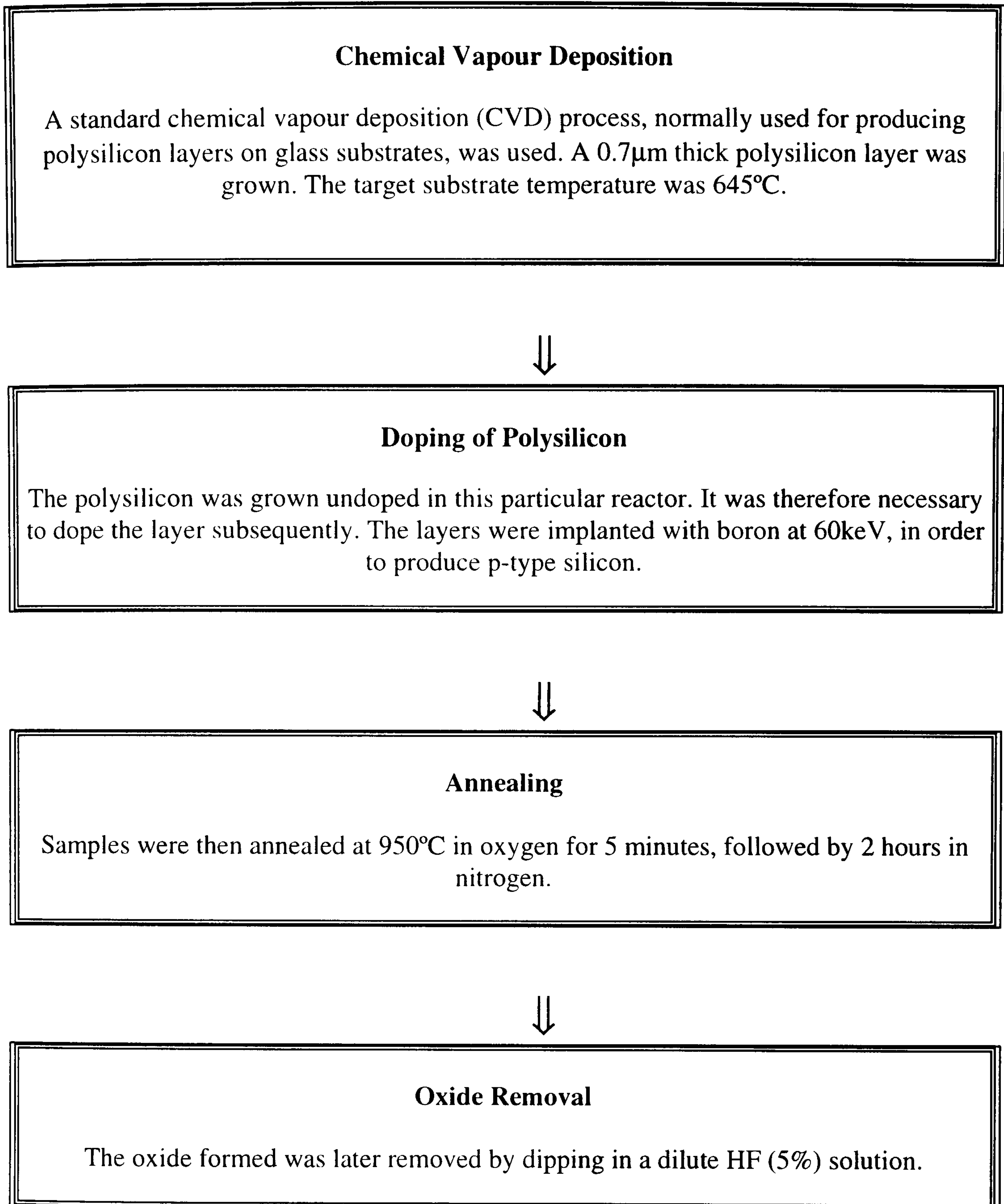
a) TEM Examination

Figure 5.30 shows micrographs of typical polycrystalline emitters. A polysilicon cone lies on top of a single crystal silicon emitter, which has near vertical sides. This image shows that the polysilicon etched in a different manner to the single crystal silicon. The emitters are very sharp, being ~5nm in radius. Many individual grains can be seen within each polysilicon cone, varying in size from 10 to 100nm. At the base of all cones is a layer of very small grains. These were the original nucleation sites for the growth of the polysilicon layer. This base layer is ~30nm thick. Within the polysilicon cone itself, the individual grains run in a vertical direction.

The height of the polysilicon cone depended on the etch time. Figure 5.29a) shows a tip from which the oxide mask is about to drop off. It is ~400nm tall. If the tip was etched until the mask fell off, the cone would become shorter (see Figure 5.29b) & 5.29d)), while maintaining the same base width. Eventually, if etching was continued, only a few grains of polysilicon were left sitting on top of the underlying single crystal silicon emitter. Several emitters formed double tips, due to the presence of two separate protruding grains at the apex, see Figure 5.31. This is the result of inhomogeneous etching of the polysilicon grains.

b) Field Emission Studies

Field emission characterisation was carried out using the adapted SEM. Table 5.4 summarises the results obtained. Distributions are shown in Figure 5.32. The polysilicon emitters were compared to single crystal silicon emitters which had been oxidised with their



(Processing was carried out by Southhampton University.)

The layer of polysilicon deposited was very thin (0.7µm), as the production of a thicker layer would have been very time consuming. Since both the single crystal substrate and polysilicon layer were etched during the same process step, this allowed comparison of the etching of the two materials to be made.

Figure 5.29 Summary of Fabrication of Polysilicon Wafers

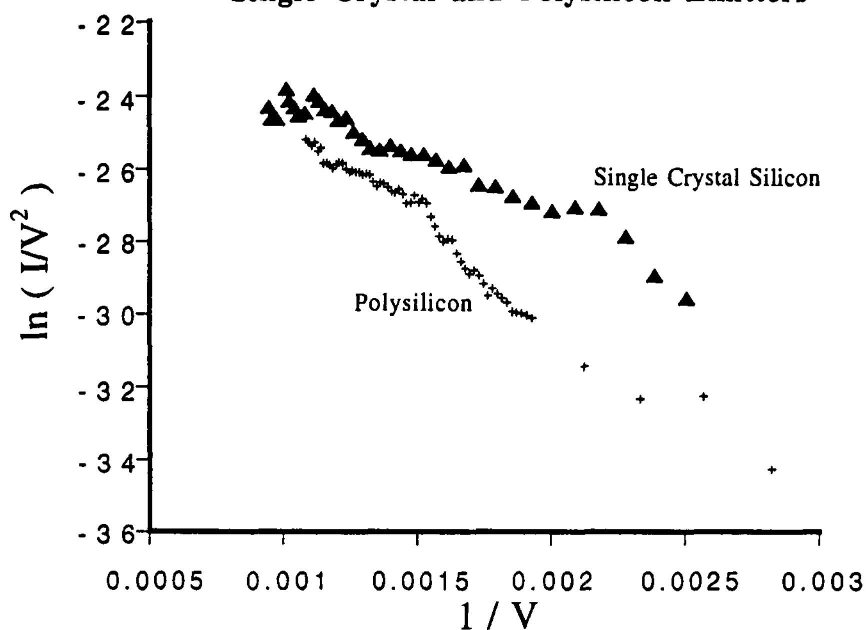
	Polysilicon Emitters	**Single Crystal Silicon (Oxidised with Masks in Place)**
Mean Starting Voltage **Median Starting Voltage** **Range** **Standard Deviation**	497V 500V 219V-941V ±190V (±38%)	450V 425V 313V-672V ±95V (±21%)
Mean Maximum Current **Median Maximum Current** **Range** **Standard Deviation**	24μA 8μA 0.6μA-100μA ±37μA (±154%)	11μA 10μA 1.3μA-37μA ±31μA (±100%)
Mean FN Slope **Median FN slope** **Range** **Standard Deviation**	-6759 -5412 (-889)-(-21905) ±5861 (±87%)	-5489 -5271 (-1825)-(-10324) ±2868 (±58%)
Mean FN Intercept **Median FN Intercept** **Range** **Standard Deviation**	-19.2 -21.2 (-3.6)-(-26.2) ±5.7 (±29%)	-18.6 -18.6 (-12.0)-(-23.5) ±3.7 (±16%)

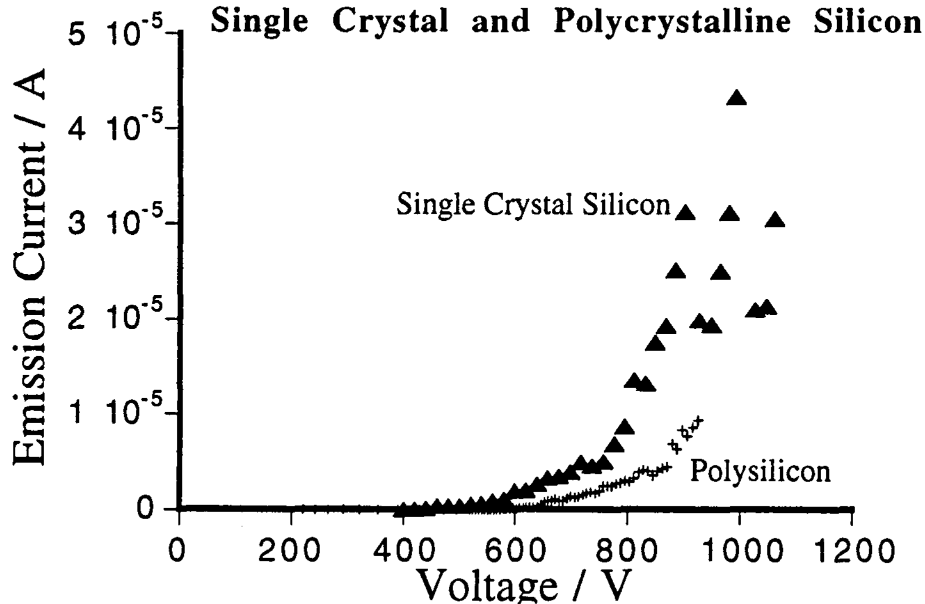
The results obtained from polysilicon emitters were compared to results obtained from single crystal emitters oxidised with their masks still in place - such emitters were more similar in geometry to the polysilicon emitters, than for flat-topped emitters.

The results show that the emission currents obtained from both polysilicon and single crystal silicon were very similar. However, the values of starting voltage and Fowler-Nordheim slope lie over a greater range than for single crystal silicon emitters. This may be due to the fact that some polysilcion emitters had single tips at the apex, while other emitters had double tips at the apex. This depended on the polysilicon grain structure at the very apex of the tip.

(20 tips examined per FEA)

Table 5.4 Comparison of Field Emission Parameters from P-Type Single Crystal, and P-Type Polysilicon Tips





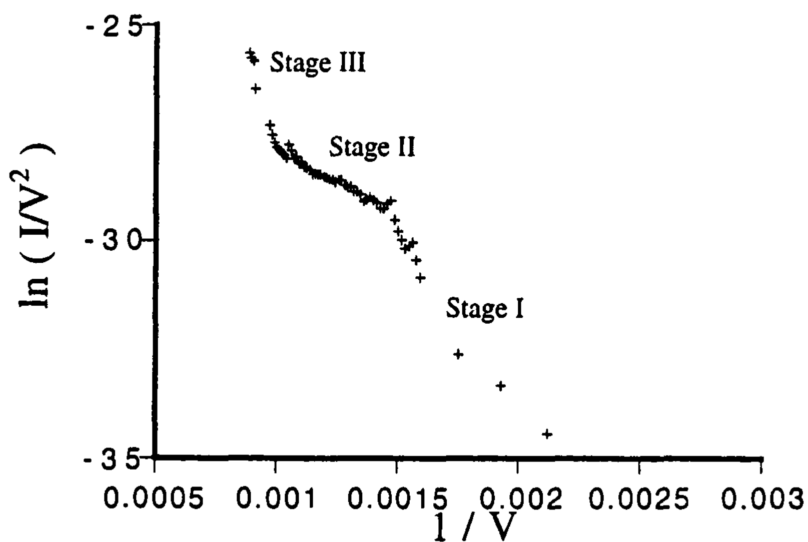


Figure 5.33 - Fowler-Nordheim and Current-Voltage Plots from Polysilicon
a) and b) compare FN and I-V plots for a polysilicon emitter and a single crystal silicon emitter which had similar starting voltage. In general, there did not appear to be any difference in the shape of plots between the two samples. c) shows a 3-stage plot obtained from a polysilicon emitter. This shows that doping of the polysilicon layer to form p-type material was successful.

masks in place, as these were closer in apex geometry than the flat-topped emitters. Apart from a few tips, which exhibited very large maximum emission currents, the maximum emission current obtained from both single crystal and polysilicon emitters was very similar. The starting voltages of the single crystal emitters were slightly lower, probably because these tips were very sharp. In addition, the range of starting voltage values for polysilicon FEAs was greater than for single crystal silicon FEAs. This may have been due to variation in the tip morphology across the array, which varied between single and multiple points, depending on the polysilicon grain structure at the tip.

A comparison of plots obtained from a polysilicon tip and a single crystal tip are shown in Figure 5.33a) & b). In general, there was no difference in the nature of the plots. Many polysilicon tips exhibited typical 3 stage p-type-like behaviour, see Figure 5.33c). This indicates that doping of the polysilicon layer had successfully formed p-type silicon.

5.6.2 Summary

Polycrystalline silicon emitter arrays could easily be formed using a wet etch process. Polysilicon field emitters fabricated by a wet etching route showed their field emission characteristics to be very similar to those of single crystal silicon emitters, although the starting voltage values were more scattered.

Chapter 5 - References

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Chapter 6 - TEM Studies of Porous Silicon

6.1 Introduction

This chapter discusses transmission electron microscope (TEM) studies of:

a) Cross-sections of p and p^+-type porous silicon (PS)

b) Anodised p and p^+-type silicon FEAs

In particular, TEM investigations were carried out in order to:

i) Check that cross-sections of the PS produced in this work matched PS structures reported in the literature, produced under similar conditions.

ii) Check that anodisation did not cause blunting of the silicon tip apex.

iii) Study the structure and arrangement of fibrils at the anodised tip apex, for different substrate dopings.

iv) Investigate the PS morphology and layer thickness at the anodised apex and on a flat plane, for a range of anodisation conditions.

v) Investigate the nature of the PS/bulk silicon interface at the anodised tip apex.

vi) Examine the nature of the anodised tip apex after various treatments, such as oxidation and HF dipping, had been carried out.

6.2 Anodisation - Formation of Porous Silicon Layers

6.2.1 Electrochemical Cell

In the literature, three main types of cell have been used to produce PS layers on semiconductor wafers. Table 6.1 describes these cells and lists the advantages/disadvantages of each. After initial testing, samples reported in this thesis were produced using the second type of single electrochemical cell described in Table 6.1b and shown in Figure 6.1.

6.2.2 Computer Control

Anodisation was controlled by a Hewlett-Packard computer attached to a power pack, via a lock-in amplifier. This allowed a constant current to be maintained for a known time. Very thin layers could be formed in this way - the shortest time that anodisation could accurately be applied was ~0.1 seconds. Current densities could be applied in the range 10-400mAcm^{-2}.

Type of Cell	Description of Apparatus	Advantages/Disadvantages
a) Single Cell - Type I	A silicon wafer was simply dipped into the electrolyte held in a beaker, see Figure 6.1a. In this case, electrical contact was made via a crocodile clip at the top of the wafer. After anodisation was completed, the wafer was removed. PS was formed on both the back and front of the wafer. **This type of cell was used initially in this work. However, it was replaced with the Type II cell described below, due to serious problems with uniformity and reproducibility.**	**Advantage** - This method was very quick to use and allowed for a quick turnover of specimens. **Disadvantage** - The uniformity of the PS layer was poor (indicated by the uneven distribution of thickness fringes).
b) Single Cell - Type II	This cell consisted of a teflon beaker with a hole in the bottom, see Figure 6.1b. The wafer to be anodised was clamped over this hole, forming a water-tight seal. The electrolyte was then poured into the beaker. With this cell, only the front side of the wafer was exposed to the HF solution. A metal contact was made to the back of the silicon wafer. **This type of cell was used for all the samples reported in this thesis.**	**Advantage** - This cell produced much more uniform layers than the Type I single cell. **Disadvantage** - The turnover of specimens was quite slow, as the entire beaker had to be emptied of HF and the sample unclamped before anodising the next sample.
c) Two Cell	The silicon wafer to be anodised would be used to separate the 2 half cells. A Pt electrode would be held in each cell. Contact with the back side of the wafer would be made via the electrolyte and current would flow from one half of the cell to the other through the wafer. **This type of cell was not tried in this work, due to the expense of building such a system. However, it is likely that this type of cell would be used in any industrial-scale process.**	**Advantage** - This method is reported to produce the most uniform layers, due to the electrolytic contact. **Disadvantage** - It is more expensive to fabricate than the other cells.

Table 6.1 Different Types of Electrochemical Cell Typically Used for Anodisation of Silicon Wafers

6.2.3 Process Details

The process steps which had to be carried out in order to anodise silicon wafers are outlined in Table 6.2. The process could be used to anodise both FEAs and flat substrates.

6.2.4 Sample Appearance After Anodisation

Only the region which had been exposed to the electrolyte was anodised, see Figure 6.2a. After formation of a PS layer, this region became brightly coloured. Thickness fringes could be observed within this coloured region. The fringes could be used to give some indication of the uniformity of the PS layer. The spacing of these thickness fringes indicated that the layers were most uniform at the centre of the wafer. Examination under the optical microscope after drying showed the sample surface had become rough, see Figure 6.2b-d.

6.3 Preparation of TEM Samples

i) Anodised FEAs - TEM specimens of anodised FEAs were prepared in the same way as plain silicon FEA TEM specimens, see Chapter 5.

ii) Cross-Sections - Samples of porous silicon cross-sections for TEM analysis were prepared from flat anodised substrates using the steps outlined in Table 6.3.

6.4 Cross-Sections of Porous Silicon

Cross-sections were studied, in order to check that the structures produced were similar to those reported in the literature.

6.4.1 Difference Between Morphology of P and P^+-Type Porous Silicon

Thick PS layers were formed on flat pieces of p-type and p^+-type silicon, using the anodisation conditions shown in Table 6.4.

a) P-Type Porous Silicon

Figure 6.3a-c shows micrographs of p-type PS cross-sections. Main results were:

- The micrograph in Figure 6.3a shows that p-type PS appears "mottled" - it has a very fine sponge-like structure, with pores ~1-2nm in diameter (micrograph taken with

Process Step	Details	Issues/Important Points
1) Formation of ohmic contact on back of wafer.	Electrical contact to the back of the wafer was made by roughening the wafer with sandpaper, to break the oxide layer. The back of the wafer was then covered with a uniform layer of conductive paint.	It was important that a good contact was made. Samples having poor contacts formed uneven PS layers.
2) Wafer clamped to cell.	The wafer (~1 inch square) was placed over the hole in the bottom of the teflon beaker. A piece of aluminium foil was placed in direct contact with the back of the wafer. This was clamped in place, see Figure 6.1. The contact between the wafer and the teflon beaker had to be water-tight, in order to prevent HF leaking through.	Care had to be taken not to crush/scrape the tips when clamping the sample in place. If the wafer was clamped too hard, the wafer cracked and HF flooded out.
3) Electrolyte	Once the beaker was water-tight, the beaker was filled with electrolyte. An electrolyte of 48% HF and ethanol in the ratio 1:1 was used.	Care had to be taken not to spill HF.
4) Electrical contact made to power supply.	A crocodile clip was attached to the aluminium foil making contact with the back of the silicon wafer. This was attached to the +ve terminal of the power supply. A platinum electrode was placed over the edge of the teflon beaker, so that it dipped into the electrolyte. A crocodile clip attached to this electrode made contact with the -ve terminal of the power supply.	n/a
5) Current Applied	The computer was programmed to apply a certain current for a given amount of time. During anodisation, hydrogen bubbles were produced which escaped from the top of the cell.	If the contact was very poor, the required current density could not be obtained, and non-uniform layers were formed. The illumination conditions were kept as uniform as possible from sample to sample, as light influence the formation of PS.
6) Electrolyte Removed	After anodisation, the electrode and crocodile clips were detached from the cell. The electrolyte was poured out of the cell. Methanol was then introduced into the container to remove the HF from the anodised silicon surface.	Care had to be taken not to spill HF, and not to crush the emitter tips when removing from the cell.
7) Drying	The specimen was blown dry with oxygen gas.	It was important to completely dry the surface. Drops left on the PS surface caused discolouration of the uniform film.

Table 6.2 Process Steps for Anodisation of Silicon Wafers

Process Step	Experimental Details
Step 1	The flat anodised sample was covered with a drop of methanol. If the sample was not wetted, the PS layer would break up and disperse in the air.
Step 2	A lacey carbon film grid was then taken and touched onto the substrate. It was dragged gently across the substrate surface. This transferred fragments of PS to the TEM grid.
Step 3	The grid was then placed face up on filter paper to dry. The fragments were attached to the grid by capillary action.
Step 4	When placed in the microscope, the grid was inserted so that the fragments were supported by the grid.

Table 6.3 Preparation of Porous Silicon Cross-Sections for TEM Analysis

image in focus). Figure 6.3b shows a micrograph of the same area, but taken with the image under-focused. The structure appears coarser and pores are more easily resolved. Underfocusing is commonly used in the examination of finely structured PS, see Beale *et al.* (1985).

- The micrograph in Figure 6.3d, demonstrates the fragility of p-type PS - this piece has torn and split following separation from the silicon substrate.

b) P^+-Type Porous Silicon

Micrographs of p^+-type PS are shown in Figure 6.4.

- In contrast to p-type PS, individual p^+ fibrils could be imaged easily. The p^+ fibrils are larger and more widely spaced, see Figure 6.4a. The p^+-type PS structure (perpendicular to substrate) is much more open and directional than for p-type PS. Pores run vertically and continuously from the top to the bottom of the flake. There is much side branching, giving the appearance of a dendritic structure.

- The fibrils are ~5-10nm thick with sideways separation being ~20-50nm. Figure 6.4b shows a single fibril standing proud from the rest of the material.

- The PS structure parallel to the substrate is different - Figure 6.4c shows a plan view micrograph looking down the pores. The PS has a honeycomb structure which has an average pore diameter of ~20-50nm.

Overall, the p and p^+-type PS structures produced in this study correlate well with PS formed under similar conditions by other researchers, e.g. Beale *et al.* (1985), Searson & Macauley (1992) and Berbezier & Halimaoui (1993). Reasons for the difference in morphology between p and p^+-type PS are outlined in Chapter 3.

6.4.2 Dependence of PS Morphology and Layer Thickness on Applied Current Density

In order to measure the film thickness formed at a particular value of anodisation current density, heterogeneous layered structures were formed on p and p^+-type silicon substrates. The layered structures were formed by alternating the anodisation current between low and high values, using the values shown in Table 6.5. A similar study was carried out by Frohnhoff *et al.* (1995). Results are as follows:

- As the current density increased, the porosity of p and p^+-type PS increased. Micrographs of the p-type PS heterostructure are shown in Figure 6.5b). The p^+-type PS heterostructure is shown in Figure 6.5a). The lighter bands in the micrographs correspond to PS formed at the higher values of current density. The darker bands correspond to PS formed at the lower values of current density. The darker bands have a more compact, denser structure.

- The higher the current density, the higher the rate of PS formation. Figure 6.6 shows a plot of PS formation rate versus anodisation current, for both p and p^+-type material. This data is also summarised in Table 6.6. The PS thickness at different anodisation times can be estimated from this data.

6.4.3 Crystallinity of Porous Silicon Layers

a) P-Type

Figure 6.3e) shows a diffraction pattern taken from a p-type PS sample (1 day old). It consists of thick, diffuse rings, with very faint diffraction spots superimposed on top. The diffuse rings are characteristic of amorphous material, indicating that much of the p-type PS was amorphous.

b) P^+-Type

Figure 6.4f) shows a diffraction pattern taken from a p^+-type PS sample (1 day old). The spots are much more intense and well-defined than for the p-type PS sample. There are no

diffuse surrounding rings, as was the case for p-type material. This indicates that the p^+-type PS was much more crystalline, being closer in structure to the original substrate than to the p-type material. In addition, TEM micrographs of p^+-type PS show lattice imaging, further evidence of the crystalline nature of the p^+-type PS fibrils.

These results are consistent with those obtained by other researchers.

The diffraction spots from p-type and p^+-type PS are significantly streaked. Streaking of diffraction spots has been reported by many other researchers, e.g. Cullis *et al.* (1992) and Berbezier & Halimaoui (1993). Streaking is believed to be caused by the presence of narrow quantum sized structures, which can give rise to broadening of the Ewald sphere (due to the uncertainty principle). P-type PS would certainly be expected to undergo quantum confinement, as it has a very fine structure.

6.4.4 Ageing/Oxidation of Porous Silicon Samples

Diffraction patterns were taken from p-type and p^+-type PS samples left in a dessicator for ~1 year.

a) P-Type

Figure 6.3f) shows that the pattern contains diffuse amorphous rings, but no diffraction spots. This implies that the p-type PS material underwent almost complete oxidation during that time, leaving no crystalline material.

b) P^+-Type

There is no difference between a freshly anodised sample and a 1 year old sample, suggesting that p^+-type PS did not undergo oxidation to the same degree as p-type PS. As discussed in Chapter 3, this is probably due to the fact that p^+-type PS has a smaller surface area than p-type PS.

Beale *et al.* (1985) also found that aged PS gave rise to amorphous rings, consistent with oxidation. Oxidation could be deleterious to the lifetime of a field emission device. The effect which oxidation has on field emission from p-type PS-covered emitters is discussed in Chapter 7.

6.4.5 Sharp P^+-Type Porous Silicon/Bulk Silicon Interface

A few intact sections of p^+-type PS were found to be still attached to the underlying bulk silicon substrate, see Figure 6.7a. It was therefore possible to study the PS/bulk silicon interface region containing the pore ends. Figure 6.7b, c and d show high magnification images of this region. The ends of the pores are ~5-10nm in radius and are curved. The residual silicon between the pores has formed sharp silicon points. These sharp points are potential field emission sites, as the electric field at them would be enhanced compared to the field at a flat interface.

6.5 Morphology of Anodised Tip Apex

The morphology of anodised emitter tips has never been reported in the literature previously. PS layers of different thickness were formed on p-type and p^+-type silicon FEAs, using the anodisation conditions shown in Table 6.7. Both flat-topped FEAs (see Section 5.3.1) and over-etched FEAs (see Section 5.3.3) were examined after anodisation.

Figure 6.8 shows micrographs of p-type PS-covered apexes, and Figure 6.9 shows micrographs of the p^+-type PS-covered apexes. Comparing and contrasting these two materials, the main results were as follows:

- Anodisation does not blunt the tip apex of p or p^+-type silicon tips.

- The entire tip surface is made rough by the anodisation process. It is covered with asperities - see the low magnification micrographs in Figures 6.8a and 6.9a. Prior to anodisation, only a few asperities were present at the tip apex, see Chapter 5.

- After anodisation, p-type silicon emitters have asperities ~1-4nm high (and of similar width) at their apex. Anodised p^+-type tips exhibit much larger fibrils, ~5-10nm high and ~5nm thick. Figure 6.9c shows three equally spaced neighbouring fibrils standing proud of the emitter surface (marked A, B and C on the micrograph).

- The density of p-type PS fibrils is higher than for p^+-type PS fibrils.

- Individual p-type pores do not appear to grow in any direction. However, p^+-type silicon pores are highly directional, running perpendicular to the surface of the emitter.

6.6 Structure of Silicon Core

On closer examination of the micrographs shown in Section 6.5, a shadow could be seen within the PS layer. When samples were rotated to a major crystallographic pole (typically [001]) and bright-field diffraction mode was used, the contrast was improved. (Rotating to a major crystallographic pole was achieved by taking a diffraction pattern from the cleaved side of the sample where there was no PS present). Under these conditions, the shadow that had appeared within the tip structure was clearly resolved as a core. The core could be observed more clearly if the electron beam was condensed down to a small spot, in order to increase its intensity.

6.6.1 Comparison of Core Geometry for P and P^+-Type PS-Covered Emitters

a) P-Type

Micrographs of the core of a p-type emitter anodised for 30 seconds are shown in Figure 6.10. The core has quite a different geometry to the outline of the original tip. The aspect ratio of the core is much higher than that of the original tip - the core is only ~10-20nm thick, but is up to 200nm in length. In the region close to the apex, the core has almost vertical sides. Further down the emitter, the core runs parallel to the {111} faces. A schematic diagram of the core is shown in Figure 6.11.

b) P^+-Type

A core was also observed for p^+-type samples anodised for 10 seconds. However, the p^+-type core has a completely different geometry to the p-type core. Figure 6.12 shows bright and dark field images of p^+-type tips, anodised for 10 seconds. The PS layer is ~400nm thick at the apex. In fact, the formation rate appears to be greater at the apex than up the emitter sides, where only 300nm was formed. This is the inverse of the situation observed for anodised p-type tips, where the PS thickness up the emitter sides is much thicker than at the apex. The p^+-type silicon core has a lower aspect ratio than the original tip.

6.6.2 P-Type PS-Covered Core

The p-type core, which exhibited greater enhancement over the original tip geometry, is discussed in more detail below:

a) Core Dimensions

The cores of a large number of anodised p-type silicon tips, examined across several similar samples, were studied in both bright and dark field imaging mode, see Figure 6.13. Most of the cores were very similar in geometry to that shown in Figure 6.10. However, some emitter cores (shown in Figure 6.13) had unusual geometries and were thicker. However, all cores had much higher aspect ratios compared to those before anodisation. Even emitters which were originally blunt, developed a high aspect ratio core following anodisation, see Figure 6.14.

b) Diffraction information

A diffraction pattern taken from the core and the surrounding PS region are shown in Figure 6.14. The results are:

- Diffraction patterns taken from an area which contained only PS and no core, showed only an amorphous pattern, see Figure 6.14c. No diffraction spots were observed.

- When a diffraction pattern was taken from a region which did contain a section of the core, silicon diffraction spots were found to be superimposed on the amorphous ring pattern of the PS layer. This indicated that the core was crystalline.

- Some tips were found to have had their apex crushed, leaving the silicon core exposed at the tip surface, see Figure 6.14. A diffraction pattern taken from this exposed core region show distinct spots with no amorphous rings, see Figure 6.14d. This confirmed that the core was crystalline.

c) Nature of Core for Flat-Topped Emitters

Flat-topped tips (i.e. those formed by stopping the etch before the oxide masks fell off) were discussed in Chapter 5, and were used for the field emission studies of PS-covered tips described in Chapter 7. Therefore, anodisation of flat-topped tips was also investigated. Figure 6.15 shows a flat-topped emitter which has been anodised for 30 seconds. Results were as follows:

- Results for flat-topped emitters are similar to those obtained for point-like emitters, i.e. there is a high aspect core having a vertical section in the region of the apex.

- However, the core is wider than for point-like emitters. This is due to the difference in starting geometry.

- As for point-like emitters, it can be seen that the thickness of PS on the vertical sides of the apex is much thinner than on the {111} planes.

- At the corner of the flat top, the PS is ~25-35nm thick. This is slightly thicker than for tips which have a point-like apex.

d) Unusual Appearance of Core

For some point-like emitters, the core appears to be constricted to a very fine wire. For such cores, it is difficult to determine whether the silicon at the very apex is actually physically attached to the rest of the core, see Figure 6.16a. In order to investigate this further, dark field micrographs of the same tip were taken using 3 different diffraction spots, see Figure 6.16b,c and d. It can be seen that bright and dark reflections occur at different positions within the core, when different diffraction spots are selected. This suggests that sections of the core are lying at different orientations to other sections. The cores of the flat-topped emitters show a similar effect - see Figures 6.17a and b, along with the bright field image in Figure 6.17c. Possible explanations for this effect are discussed below:

i) The core could be polycrystalline - Although the core appears to be polycrystalline, the emitters were originally fabricated from single crystal silicon. Therefore they should not be polycrystalline.

ii) The core could have broken up under stress existing within the oxidised PS structure - The sample was 1 year old and it has already been shown that p-type PS undergoes oxidation within a few weeks. Stress build-up could have been caused by oxidation of the surrounding PS, which would have a larger volume than fresh PS. If the core had cracked under the stresses caused by oxidation of the PS layer surrounding it, different segments could then be left lying at slightly different crystallographic orientations. Segments lying at different orientations would thus reflect the electron beam differently, as if the core consisted of separate crystals. It is possible that pore ends acted as crack propagation sites, once the stress had started to build. In fact, close examination of the diffraction patterns does show that at each spot, there is a second spot very close to it. If part of the core lay slightly out of place, a second diffraction pattern would be generated. This would be superimposed on the main diffraction pattern, giving an effect similar to that observed in this work.

6.7 Porous Silicon / Bulk Silicon Interface

The PS/bulk silicon interfaces of p and p^+-type anodised tips have been studied. Figure 6.18 show high magnification images of these interfaces (tips are still covered with PS). Results are as follows:

- The interfaces (for both p and p^+-type PS) contain sharp point-like structures, with roughness on a scale of ~10nm.

- The p^+-type PS interface was harder to image because the PS layer was so thick. The best images of the p^+-type PS interface were observed in cross-section, see Section 6.4.5.

A rough PS/bulk silicon interface was also observed by Berbezier & Halimaoui (1993). They observed a roughness of the order ~6nm for p^+-type PS and of the order 3nm for p-type PS.

6.8 Variation In PS Layer Thickness with Anodisation Time

P and p^+-type tips were anodised for the times shown in Table 6.7. The thickness of the PS layer at the apex was measured. It is important to know the PS layer thickness at the tip apex for the following reasons:

i) PS is a very resistive material and so a PS layer formed at the apex of an emitter tip could potentially cause resistive heating to occur during field emission. Such heating could subsequently lead to premature destruction of the tip. Resistive heating would be expected to depend on the PS layer thickness.

ii) As described in Chapter 2, certain researchers have placed resistors in series with tips, in order to protect them from short current bursts. A resistive PS layer on the surface of a tip apex may act in a similar way to a series resistor. The extent to which any resistive protection occurs, would be expected to depend on the thickness of the PS layer.

Micrographs of emitters anodised for times other than those shown already, are shown in Figure 6.19 (p-type) and Figure 6.20 (p^+-type). For each anodisation time, the thickness of the PS layer at the apex (A on schematic diagram in Figure 6.11), and on the {111} planes (B on same diagram) have been recorded in Tables 6.8 and 6.9. In addition, for p and p^+-type tips, a graph of PS thickness at both the apex and on the {111} planes has been plotted versus the anodisation time - see Figures 6.21a and 6.21b. Main results were as follows:

6.8.1 P-Type Porous Silicon-Covered Tips

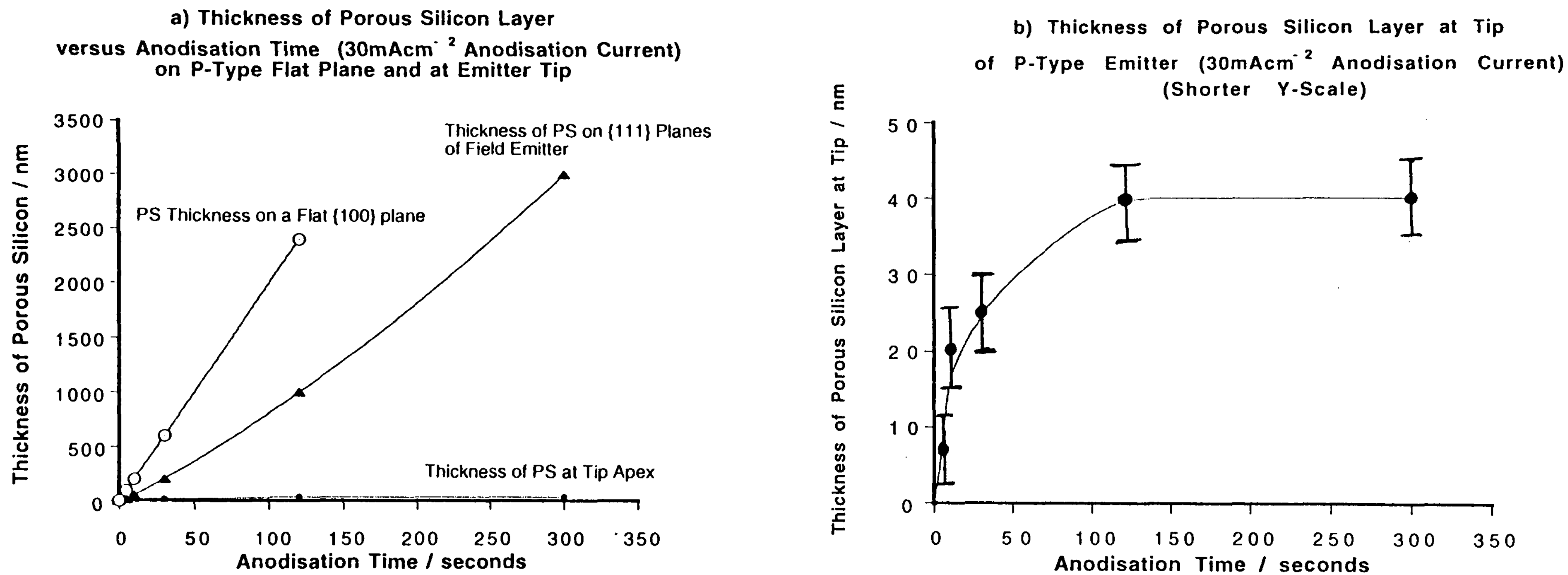
- For all anodisation times, the PS layer at the apex is much thinner than on the {111} planes. As the anodisation time increases, this difference increases. The increase in thickness at the apex is negligible compared to the change in thickness on the {111} planes. After ~120 second anodisation, the PS layer at the apex does not appear to grow any thicker.

- For samples anodised for 120 seconds, the geometry of the silicon core is completely different to the geometry of the original tip. The core is vertically sided and reaches almost to the base of the emitter. The overall geometry is 'bullet-like' (see Figure 6.19f) & 6.19g)). The core is much longer than for samples anodised for 30 seconds and the PS layer on the {111} planes is much thicker, being ~1μm (compared to 0.15μm formed on 30 seconds samples).

- Tips anodised for 300 seconds had a structure very similar to that observed for the 120 seconds samples, and the thickness of porous silicon on the emitter sides were very similar.

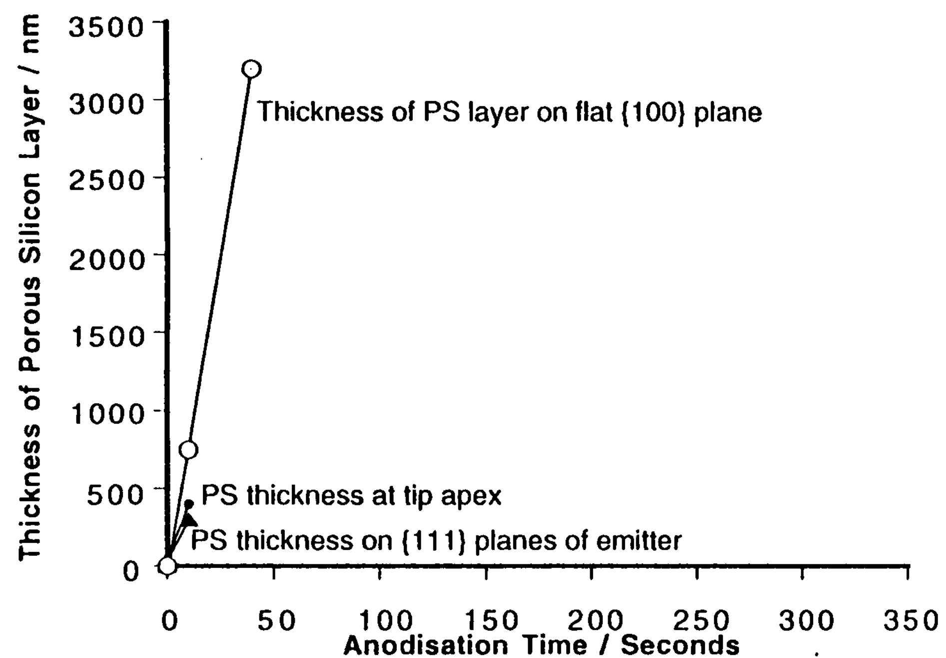
6.8.2 P^+-Type Porous Silicon

Even for a very short anodisation time of 0.25 seconds, a PS layer ~40nm thick was formed (see Figure 6.20b)). On a flat substrate, a layer ~20nm thick would be expected to form in this time. Therefore, anodisation of p^+-type PS appears to occur faster at the emitter apex,



Accuracy of measurement of PS thickness at emitter apex, from TEM micrograph, is believed to be ±5nm (as it was sometimes difficult to identify the exact position of the PS/bulk silicon interface).

Figure 6.21a - Thickness of Porous Silicon Layer at Emitter Apex versus at Flat Plane - P-Type Silicon
- These plots show that the PS layer at the emitter apex is much thinner than on either the {111} planes or on a flat plane.
- The plot also shows that after ~120 second anodisation time, the p-type PS layer thickness did not increase any further.



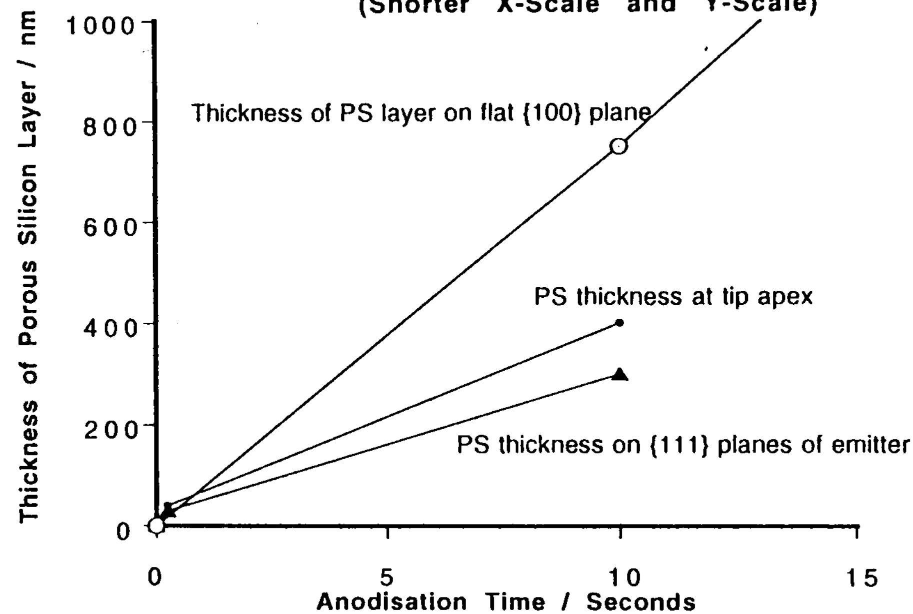


Figure 6.21b - Thickness of Porous Silicon Layer at Emitter Apex versus at Flat Plane - P+-Type Silicon
- This plot shows that at the tip apex, a PS layer formed much faster than at the apex of a p-type PS emitter.
- The plot also shows that the PS layer thickness was proportional to anodisation time, unlike the situation at a p-type apex.

than on a flat plane. This is the reverse of the situation observed for p-type PS, where the PS rate of formation was lower at the apex than on a flat plane. The thickness of the PS layer at the tip apex is proportional to anodisation time, unlike the case for p-type PS.

6.8.3 Summary

Summarising, the main results from this section are:

- The PS morphology at the tip apex did not change with anodisation time.
- For both p^+ and p-type silicon emitters, continuous PS layers were formed on tips, even for very short anodisation times. This may be important for producing anodised devices. The gate insulation may be eaten away by long anodisation times. Therefore, the time that a gated field emission device is kept immersed in HF should be minimised as much as possible.
- A rough PS/bulk silicon interface was identified for all samples, whatever the PS layer thickness.
- At the tip apex, p^+-type PS layers were much thicker than p-type PS layers, for a given anodisation time. For example, a p^+-type silicon tip anodised for 0.25 seconds formed a layer ~40nm thick at the apex; whereas p-type tips had to be anodised for 120 seconds in order to form a PS layer of the same thickness.
- At the tip apex, the thickness of p-type PS layers was not proportional to anodisation time, whereas the thickness of p^+-type PS layers was proportional to anodisation time.

6.9 Oxidation And HF Treatments on Porous Silicon

The following treatments were also investigated:

6.9.1 PS-Covered Samples Dipped into HF solution

Figure 6.22a shows an image of a p-type PS tip which was dipped into buffered HF, one day after anodisation (originally anodised for 30 seconds at a current density of $30mAcm^{-2}$). Some of the PS layer has been removed, but some remains adhered to the silicon core. However, it was found that samples left in air for several months, before carrying out this

HF treatment, were almost completely stripped of PS, (similar to tip shown in Figure 6.22b). This is thought to be due to oxidation of the PS layer, which was then readily removed by the HF.

6.9.2 PS-Covered Samples Oxidised and then Dipped into Buffered HF

Fresh p and p^+-type PS-covered samples were oxidised at 900°C for 30 seconds and then dipped into buffered HF. The following observations were made:

- The p-type PS layer was completely removed from all the tips examined, see Figure 6.22b.

- The p^+ PS layer was still in place following this treatment and the morphology had not changed.

6.9.3 Structures Left Behind Following Removal of P-Type Porous Silicon Layer

The main results are described below:

- **High Aspect Ratio Core** - The thin (~5nm) p-type core (formed when tips were anodised for 30 seconds) was found to be intact after PS removal, see Figure 6.22. This result is important because it shows that the core is continuous. It also shows that it was possible to remove the PS layer without damaging the fragile core inside.

- **Indication of stress break-up of wider cores** - For wedge-shaped tips (originally anodised for 30 seconds), the cores are quite different to the cores observed while the PS layer was still in place. Figure 6.22c) and 6.22d) show images of double-peaked tips - two silicon rods are standing vertically, in the position where the sides of the silicon cores used to be. Between the two rods, there is some debris. In Section 6.6.2d, it was suggested that thicker silicon cores may have cracked under stress in the oxidised PS layer. The TEM images after removal of the PS layer indicate that this may have

occurred. During the HF dip, the mis-oriented silicon grains could have broken apart and floated away. This would have resulted in total removal of the core centre, leaving behind two silicon rods, as has been observed here.

- **Bullet-shaped cores** - Following removal of the PS layer, tips originally anodised for 120 seconds have a very unusual geometry. The tips, which were originally pyramid-shaped, have become 'bullet'-shaped - see Figure 6.23. In these images, almost the entire emitter height could be imaged - the cores had near vertical sides right down to the emitter base.

- **Rough core** - For all anodisation times, the core surface is rough, see Figure 6.24.

6.10 Discussion

6.10.1 Potential Sources for Field Emission

After anodisation, both p-type and p^+-type emitters exhibited the following:

1) A large density of surface asperities were present at the apex.
2) Sharp points were present at the PS/bulk silicon interface

In addition, anodised p-type emitters exhibited:

3) A sharp core which had an enhanced aspect ratio, compared to the original tip geometry.

Emission could originate at any of these three sites, as they all have the potential to locally enhance the applied field.

6.10.2 Possible Applications to Micro-Machining

The difference in core geometry between p and p^+-type PS-covered tips is interesting in itself. PS is presently being developed for use as a micromachining technique, by several researchers, see Smith *et al.* (1991) and Steiner & Lang (1995). In addition, Kim *et al.*

(1995) used PS as a sacrificial layer, to produce gated FEAs. The fact that p and p^+-type silicon behave differently when anodised, could affect the type of silicon substrate chosen for certain micromachining applications.

Anodisation of p-type FEAs, followed by HF dipping, could be used to produce more uniform arrays of tips. This is because the geometry of the core does not appear to depend on the starting geometry of the tip. At present, processes such as oxidation sharpening at high temperature are typically used to sharpen tips and increase their uniformity, see Chapter 5. It may not be possible to give all devices a high temperature treatment. Anodisation could be used as a low temperature alternative to oxidation sharpening.

6.10.3 Possible Reason for Formation of Sharp Cores

The reason for the formation of sharp cores is not clear. One theory that could explain the difference in anodisation behaviour between the p and p^+-type tips is as follows. When the PS layer is formed, the etch front is preceded by a depletion region. During anodisation, depletion regions are formed ahead of the etch front. If the two depletion regions from opposite sides of the emitter meet during anodisation, then it may not be possible for PS to form in the overlapping region, as very few holes are available. The depletion region would be expected to be larger in the case of p-type silicon as it is less heavily doped. Therefore overlapping of depletion regions would be expected to occur to a greater degree than for p^+-type silicon. The high aspect ratio core may be a region which was depleted of holes during the anodisation process, and so could not be anodised further. This core geometry may not have formed within p^+-type silicon tips, because depletion of holes did not occur due to the high conductivity of the material.

Core formation is unlikely to be due to any crystallographic effect. This is because PS layers formed on low doped p-type silicon are randomly oriented, see Harsanyi & Habermeier (1987) and Chuang *et al.* (1989). The p-type PS etch rate is found to be isotropic, depending only on the availability of holes at the silicon/electrolyte interface, see Steiner & Lang (1995).

Nakajima *et al.* (1993) reported an effect which appears to be related to the results obtained here. They observed thread-like features ~5-10nm wide and ~400nm long, originating at sharp points on a flat anodised p-type silicon substrate of similar doping to that used here (10Ωcm). These threads were spaced between 0.5μm-2μm apart and their orientation lay in the direction of growth of the PS. Micrographs taken in both bright and dark field showed that the threads consisted of linked micro-crystals. Diffraction patterns contained double spots showing that the atomic planes of these microcrystals lay in almost the same direction, but were slightly rotated relative to each other. However, the authors did not suggest how this effect occurred.

Further investigations should be carried out to investigate why p-type FEAs formed sharp cores when anodised. Suggestions for experiments which could be carried out include:

1) Strongly illuminating the surface of p-type FEAs during the anodisation process. It has been suggested that the sharp cores developed due to the formation of depletion regions (depleted of holes), which were not present to the same extent during anodisation of p^+-type silicon. If this theory was correct, strong illumination would decrease the size of depletion regions and hence alter the geometry of the silicon core.

2) Anodisation of n and n^+-type emitters may also further understanding of this effect, as such emitters would have lower concentrations of holes. If this theory was correct, these structures should form a core similar to p-type silicon when anodised.

6.11 Anodisation of Polycrystalline Silicon Emitters

Anodisation of the p-type polycystalline silicon emitters described in Section 5.6 was investigated briefly, but the images are not shown here. Studies indicated that the structure formed was of a different thickness to the PS formed on the single crystal silicon. As tips in working devices are likely to be fabricated from polysilicon, future work should investigate anodisation of these polysilicon FEAs in more detail. Studies should check that the morphology and layer thickness are similar, and that the silicon core structure is similar.

Chapter 6 - References

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Chapter 7 Field Emission from Porous Silicon Covered Arrays

7.1 Introduction

The aim of the work described in this chapter was as follows:

1)To investigate the effect of anodisation (i.e. the formation of a porous silicon (PS) layer) on the field emission properties of silicon field emitter arrays (FEAs).

2)To understand how, following anodisation, any improvements in the field emission properties depended on the type of PS morphology and the PS layer thickness. This information was required in order to understand the origin of any improvements in field emission properties following anodisation, and the factors influencing the degree of improvement observed.

3) To investigate the effects of ageing and treatment by a buffered HF dip, on the emission characteristics of porous silicon.

This chapter is arranged as follows:

Section 7.2 - Effect of anodisation on p and p^+-type silicon FEAs

Section 7.3 - Effect of thermal oxidation of anodised FEAs and removal of the PS layer

Section 7.4 - Discussion of results described in Sections 7.2 and 7.3

Section 7.5 - Comparison of these results to similar work reported by other researchers

Section 7.6 - Effect of ageing and HF treatment of aged samples

Section 7.7 - Overall conclusions for this chapter

7.2 Effect of Anodisation on P and P^+-Type Silicon Field Emitter Arrays

This section describes the field emission properties of both p and p^+-type FEAs anodised for a range of times. Their field emission properties have been compared to those of non-anodised emitters having the same substrate doping.

All results reported in this chapter were collected in the adapted SEM under the improved vacuum. At the start of the work for this thesis, many anodised samples were examined before it was realised that the vacuum conditions inside the adapted SEM and the reproducibility of the

geometry of the non-anodised silicon FEAs were very poor (see Chapters 4 and 5). These factors had to be improved before useful studies could be carried out. Therefore, the results obtained at the start of the work for this thesis have not been included here. All experiments were repeated once the vacuum system and sample preparation techniques had been improved. Experimental details are summarised in Table 7.0.

7.2.1 Field Emission from Anodised P-Type Field Emission Arrays

P-type FEAs were anodised using the conditions shown in Table 7.1, for times in the range 5-300 seconds. The number of samples and the number of tips examined on each sample, for each anodisation time, are also summarised in Table 7.1. For p-type silicon, two separate sets of samples were examined. For the first set, 20 tips were examined per sample. For the second set, 10 tips were examined per sample. (For each anodisation time, a new FEA had to be prepared; the two different sets of samples were prepared several weeks apart.) Data from both sets of samples are shown here, to give an indication of the reproducibility of the results. The field emission data obtained from anodised p-type FEAs is summarised in Tables 7.2-7.10. The main results are outlined in the following sections.

a) Proportion of Tips Tested which Emitted

The proportion of tips tested which emitted within the voltage range which could be applied in the adapted SEM was found to increase following anodisation. On average, only 80% of non-anodised tips tested actually emitted, whereas all anodised tips which were tested emitted.

b) Starting Voltage Reduction

During the brief study carried out during the course of the Part II project, the starting voltage for p-type FEAs was found to be reduced by ~25% following anodisation for 30 seconds. However, due to the poor vacuum and the poor reproducibility of sample preparation, it was necessary to confirm these results. It was also important to investigate whether anodisation time and PS morphology affected the starting voltage.

In all cases, the starting voltage was taken as being the voltage required to obtain 1nA of current. Figures 7.1 shows distributions of starting voltage for each anodisation time. Table 7.12

1) Specimen Preparation of Anodised Emitters	The FEAs used in these experiments were flat-topped (see Chapter 5 for reasons). Samples were always cleaved from the centre of the anodised sample, as the PS layers were most uniform at this point on the wafer (see Chapter 6).
2) Preparation of Non-Anodised Emitters	The FEAs used here were also flat-topped. Note that prior to examination, non-anodised silicon FEAs were dipped into the same anodisation solution, but no current density was applied. This step was carried out in order to check that the formation of a PS layer (and not the effect of the electrolyte) was responsible for the results obtained from anodised FEAs.
3) Series Resistor	All emitters were examined with a $0.67M\Omega$ resistor held in series with the probe. The effect of the voltage dropped across the series resistor has been removed from the data presented here.
4) Multiple Runs	As discussed in Chapter 4, the first field emission run from an emitter was slightly noisier than for the second run (even in the improved vacuum), probably due to desorption of adsorbates. Therefore, wherever possible, only data from second runs was analysed.
5) Specimen Examination	Ideally, exactly the same samples (and even exactly the same tips) would have been examined before and after anodisation. However, it was difficult to do this for the following reasons: The samples had to be cut down to a section ~5mm by 5mm square, in order to fit onto the specimen stub for examination in the adapted SEM. However, specimens which had already been examined in the SEM were then too small to cover the opening at the base of the anodisation cell. For this reason, the standard anodisation cell could not be used to form PS layers. Initially, anodisation of SEM samples was attempted by sticking them onto larger pieces of silicon which did cover the hole at the base of the electrochemical cell (see Figure 6.1b). In addition, anodisation was also attempted by simply dipping the small SEM samples into the electrolyte held in a normal beaker (see Figure 6.1a). However, in both cases, poor quality, uneven PS layers were formed. (If time had allowed, it may have been possible to build anodisation apparatus designed specifically to anodise small specimens.) For this reason it was decided that the same samples would not be examined before and after anodisation. Instead, for each set of conditions to be tested, several samples (prepared in a similar way) were examined, in order to check the reproducibility of the results obtained. To allow a proper statistical comparison, a similar number of tips were examined before and after anodisation.

Table 7.0 - Summary of Experimental Details for Investigation of Anodised FEAs in Adapted SEM

Anodisation Time (Seconds)	Sample Codes	Number of Tips Examined
0	1, 2	20, 10
5	A, B	20, 9
10	C	21
30	D, E	21, 11
90	F, G	21, 10
300	H, I	20, 12

P-type FEAs (10Ωcm resistivity) were anodised using the electrochemical cell described in Chapter 5. The same anodisation conditions were used for all samples. The electrolyte consisted of 48% HF:ethanol in the concentrations 50:50. An anodisation current of 30mAcm^{-2} was used. Anodisation times are listed in the table above.

All results were obtained in the improved vacuum system of the adapted SEM. Although numerous samples were also examined before the vacuum system had been improved (see Chapter 4), the results could not be relied upon and so are not included here.

(Tables 7.2-7.10 on the following pages aummarise the data obtained from these samples before and after anodisation.)

Table 7.1 Summary of Anodised and Non-Anodised P-Type Samples Examined

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	FN slope (m)	FN intercept (c)	Voltage to obtain 0.1μA	Voltage to obtain 1μA	Voltage to obtain 10μA
Mean Value	Before	500V	13μA	875V	-9360	-12.9	560V	655V	830V
	After	335V (33%drop)	19μA (46%increase)	615V (30%drop)	-2150 (77%drop)	-18.8 (more -ve)	335V (40%drop)	470V (27%drop)	580V (30%drop)
Spread of Values	Before	300V-670V	2μA-40μA	550V-1150V	(-2675)-(-17270)	(-9.33)-(-21.76)	460V-780V	425V-1000V	520V-1150V
	After	200V-500V	5μA-60μA	310V-920V	(-500)-(-4830)	(-3.6)-(-23.7)	210V-520V	260V-730V	320V-870V
Median Value	Before	500V	10μA	850V	-8860	-14.05	540V	620V	800V
	After	325V	15μA	630V	-2170	-20.9	325V	450V	605V
Standard Deviation (+ Coefficient of Variation)	Before	±80V (±16%)	±10μA (±77%)	±195V (±22%)	±4370 (±47%)	±7.8 (±60%)	±95V (±17%)	±155V (±24%)	±225V (±27%)
	After	±90V (6%)	±15μA (±79%)	±170V (±27%)	±1180 (±55%)	±5.0 (±27%)	±110V (±32%)	±140V (±30%)	±140V (±24%)

20 separate tips examined both before and after anodisation

Table 7.2: Summary of Data Obtained from P-Type Silicon Field Emitter Arrays Before and After Anodisation for 5 Seconds - Sample A

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	FN slope (m)	FN intercept (c)	Voltage to obtain 0.1μA	Voltage to obtain 1μA	Voltage to obtain 10μA
Mean Value	Before	510V	30μA	1110V	-5900	-18.0	555V	810V	1060V
	After	340V (33%drop)	50μA (67%increase)	670V (40%drop)	-2775 (47%drop)	-20.4 (more -ve)	375V (33%drop)	500V (39%drop)	620V (43%drop)
Spread of Values (Range)	Before	420V-600V	0.5μA-80μA	850V-1430V	(-2085)-(-7510)	(-10.4)-(-24.7)	450V-700V	600V-1100V	800V-1420V
	After	240V-500V	10μA-75μA	475V-900V	(-460)-(-5860)	(-10.0)-(-26.6)	260V-540V	360V-670V	450V-900V
Median Value	Before	500V	14μA	1000V	-6845	-17.5	550V	840V	1000V
	After	300V	55μA	700V	-1340	-22	380V	430V	610V
Standard Deviation	Before	±60V (±12%)	±31μA (±103%)	±210V (±19%)	±1970 (±33%)	±3.7 (±20%)	±80V (±14%)	±165V (±21%)	±280V (±27%)
(+ Coefficient of Variation)	After	±85V (±25%)	±20μA (±40%)	±135V (±20%)	±2280 (±82%)	±6.4 (±31%)	±85V (±22%)	±120V (±23%)	±140V (±23%)

10 separate tips examined both before and after anodisation

Table 7.3 Before and After 5 Second Anodisation of P-Type FEA - Sample B

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	FN slope (m)	FN intercept (c)	Voltage to obtain 0.1μA	Voltage to obtain 1μA	Voltage to obtain 10μA
Mean Value	Before	500V	13μA	875V	-9360	-12.9	560V	655V	830V
	After	315V (37%drop)	16μA (23%increase)	635V (27%drop)	-3575 (62%drop)	-18.4 (more -ve)	340V (40%drop)	455V (31%drop)	655V (21%drop)
Spread of Values	Before	300V-670V	2μA-40μA	550V-1150V	(-2675)-(-17270)	(-9.33)-(-21.76)	460V-780V	425V-1000V	520V-1150V
	After	170V-500V	1μA-43μA	250V-1000V	(-895)-(-7950)	(-11)-(-23.3)	180V-570V	230V-770V	400V-900V
Median Value	Before	500V	10μA	850V	-8855	-14.05	540V	620V	800V
	After	290V	12μA	665V	-3740	-20.6	345V	450V	685V
Standard Deviation (+ Coefficient of Variation)	Before	±80V (±16%)	±10μA (±77%)	±195V (±22%)	±4370 (±47%)	±7.8 (±60%)	±95V (±17%)	±155V (±24%)	±225V (±27%)
	After	±90V (±29%)	±12μA (±75%)	±180V (±28%)	±1750 (±49%)	±4.0 (±22%)	±95V (±28%)	±120V (±26%)	±145V (±22%)

20 separate tips examined both before and after anodisation

Table 7.4 Before and After 10 Second Anodisation of P-Type FEA - Sample C

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	FN slope (m)	FN intercept (c)	Voltage to obtain 1µA	Voltage to obtain 10µA
Mean Value	Before	500V	13µA	875V	-9360	-12.9	655V	830V
	After	340V (32%drop)	18µA (38%increase)	740V (16%drop)	-3510 (64%drop)	-21.3 (more -ve)	570V (13%drop)	670V (20%drop)
Spread of Values	Before	300V-670V	2µA-40µA	550V-1150V	(-2675)-(-17270)	(-9.3)-(-21.8)	425V-1000V	520V-1150V
	After	214V-505V	0.6µA-80µA	400V-1100V	(-470)-(-6900)	(-7.7)-(-30.3)	325V-800V	380V-900V
Median Value	Before	500V	10µA	850V	-8855	-14.05	620V	800V
	After	345V	8µA	779V	-2785	-23.9	550V	695V
Standard Deviation (+ Coefficient of Variation)	Before	±80V (±16%)	±10µA (±77%)	±195V (±22%)	±4370 (±47%)	±7.8 (±60%)	±155V (±24%)	±225V (±27%)
	After	±30V (±9%)	±22µA (±122%)	±185V (±25%)	±2445 (±70%)	±6.0 (±28%)	±30V (±5%)	±165V (±25%)

20 separate tips examined both before and after anodisation

Table 7.5 Before and After 30 Second Anodisation of P-Type FEA - Sample D

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	FN slope (m)	FN intercept (c)	Voltage to obtain 0.1μA	Voltage to obtain 1μA	Voltage to obtain 10μA
Mean Value	Before	510V	30μA	1110V	-5900	-18.0	555V	810V	1060V
	After	355V (31%drop)	33μA (10%increase)	665V (40%drop)	-2830 (52%drop)	-20.7 (more -ve)	410V (27%drop)	510V (37%drop)	610V (43%drop)
Spread of Values	Before	420V-600V	0.5μA-80μA	850V-1430V	(-2085)-(-7510)	(-10.4)-(-24.7)	450V-700V	600V-1100V	800V-1420V
	After	190V-540V	6.3μA-90μA	400V-1100V	(-875)-(-6180)	(-8.7)-(-26.8)	205V-585V	285V-700V	380V-860V
Median Value	Before	500V	14μA	1000V	-6845	-17.5	550V	840V	1000V
	After	370V	25μA	600V	-2265	-22.0	375V	470V	550V
Standard Deviation (+ Coefficient of Variation)	Before	±60V (±12%)	±31μA (±103%)	±210V (±19%)	±1970 (±33%)	±3.7 (±20%)	80V (±14%)	±165V (±21%)	±280V (±27%)
	After	±100V (±29%)	±27μA (±82%)	±205V (±31%)	±1980 (±70%)	±5.9 (±28%)	±140V (±34%)	±130V (±26%)	±150V (±24%)

10 separate tips examined both before and after anodisation

Table 7.6 Before and After 30 Second Anodisation P-Type FEA - Sample E

Parameter	**Sample Number**	**Starting Voltage**	**Maximum Current**	**Maximum Voltage**	**Voltage to obtain 0.1μA**	**Voltage to obtain 1μA**
Mean Value	Before	500V	13μA	875V	560V	655V
	After	360V (29%drop)	2.9μA (78%drop)	620V (29%drop)	370V (34%drop)	550V (18%drop)
Spread of Values	Before	300V-670V	2μA-40μA	550V-1150V	500V-750V	400V-900V
	After	290V-500V	0.7μA-14μA	450V-750V	210V-450V	360V-650V
Median Value	Before	500V	10μA	850V	565V	700V
	After	355V	2.4μA	635V	370V	530V
Standard Deviation	Before	±80V (±16%)	±10μA (±77%)	±195V (±22%)	±80V (±14%)	±130V (±20%)
(+ Coefficient of Variation)	After	±50V (±14%)	±2.8μA (±96%)	±90V (±14%)	±55V (±5%)	±70V (±25%)

20 separate tips examined both before and after anodisation

Note that emission from samples anodised for times > 30 seconds was extremely noisy. Although estimates for the starting voltage have been given, the emission began and then stopped several times before rising properly. Therefore, values for the Fowler-Nordheim slope and intercept have not been calculated (for samples anodised for longer than 30 seconds) as emission was too noisy.

Table 7.7 Before and After 90 Second Anodisation of P-Type FEA - Samples F

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	Voltage to obtain 0.1μA	Voltage to obtain 1μA
Mean Value	Before	510V	30μA	1110V	555V	810V
	After	425V (17%drop)	1.3μA (96%drop)	765V (31%drop)	600V (11%higher)	815V (same)
Spread of Values	Before	420V-600V	0.5μA-80μA	850V-1430V	450V-700V	600V-1100V
	After	240V-500V	0.2μA-3.2μA	580V-1400V	420V-800V	600V-1400V
Median Value	Before	500V	14μA	1000V	550V	840V
	After	300V	1.1μA	690V	575V	730V
Standard Deviation (+ Coefficient of Variation)	Before	±60V (±12%)	±31μA (±103%)	±210V (±19%)	±80V (±14%)	±165V (±21%)
	After	±85V (±25%)	±1μA (±23%)	±240V (±31%)	±105V (±18%)	±295V (±36%)

10 separate tips examined before and after anodisation

Table 7.8 Before and After 90 Second Anodisation of P-Type FEA - Sample G

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	Voltage to obtain 0.1μA	Voltage to obtain 1μA
Mean Value	Before	500V	13μA	875V	560V	655V
	After	395V (21%drop)	1.4μA (78%drop)	600V (31%drop)	430V (34%drop)	575V (13%drop)
Spread of Values	Before	300V-670V	2μA-40μA	550V-1150V	500V-750V	400V-900V
	After	220V-700V	0.01μA-4μA	380V-900V	240V-790V	390V-750V
Median Value	Before	500V	10μA	850V	565V	700V
	After	370V	1.2μA	570V	410V	540V
Standard Deviation (+ Coefficient of Variation)	Before	±80V (±16%)	±10μA (±77%)	±195V (±22%)	±80V (±14%)	±130V (±20%)
	After	±120V (±30%)	±1μA (±71%)	±160V (±26%)	±130V (±30%)	±110V (±19%)

20 separate tips examined both before and after anodisation

Table 7.9 Before and After 300 Second Anodisation of P-Type FEA - Sample H

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	Voltage to obtain 0.1μA	Voltage to obtain 1μA
Mean Value	Before	510V	30μA	1110V	555V	810V
	After	410V (20%drop)	3μA (90%drop)	625V (44%drop)	395V (29%drop)	615V (24%drop)
Spread of Values	Before	420V-600V	0.5μA-80μA	850V-1430V	450V-700V	600V-1100V
	After	250V-660V	0.6μA-11μA	345V-875V	275V-540V	370V-800V
Median Value	Before	500V	14μA	1000V	550V	840V
	After	355V	1.9μA	625V	375V	610V
Standard Deviation (+ Coefficient of Variation)	Before	±60V (±12%)	±31μA (±103%)	±210V (±19%)	±80V (±14%)	±165V (±21%)
	After	±135V (±33%)	±3.2μA (±100%)	±150V (±24%)	±85V (±21%)	±120V (±20%)

10 separate tips examined before and after anodisation

Table 7.10 Before and After 300 Second Anodisation of P-Type FEA - Sample I

summarises the starting voltage, the percentage reduction in starting voltage and the range of values/standard deviation obtained for each anodisation time. In addition, Figure 7.2 shows starting voltage and percentage reduction in starting voltage plotted versus both anodisation time and plotted versus PS layer thickness at the tip apex (as determined by TEM analysis - see Chapter 6). Note that the error bars added to these plots assume an accuracy of ±15% of the measured value of starting voltage. The main results are summarised below:

i) The mean starting voltage was reduced by up to 37% following anodisation. The mean starting voltage prior to anodisation was ~500V versus ~314V following for a 10 second anodisation. The lowest starting voltage from an anodised tip was 170V, whereas the lowest starting voltage for a non-anodised emitter was ~300V. These reductions in starting voltage is greater than the 25% reduction recorded during the Part II project.

ii) There was relatively good consistency between the two sets of samples - similar results were obtained from both sets of samples.

iii) The starting voltage for samples anodised for times in the range 5-30 seconds (where the PS layer at the apex was in the range 14nm-25nm thick) were very similar. However, the starting voltage for anodisation times <30 seconds, increased slightly with increasing anodisation time and hence increasing PS layer thickness. For samples anodised for 90 and 300 seconds (where the PS layer at the tip apex of these samples was ~50nm thick), the starting voltage was higher - there was only 17% reduction versus non-anodised silicon.

iv) The spread of values and the values of standard deviation before and after anodisation were similar, within the limits determined by the experimental accuracy of the adapted SEM.

c) Voltage Required to Obtain Higher Current Values and Rate of Increase of Current with Voltage

In addition to the starting voltage, the mean voltages required to obtain current values of 0.1, 1 and 10μA were plotted versus current for all anodisation times, see Figure 7.3. The results are summarised in Table 7.13. The main points are outlined below:

Specimen Type	Approximate % Tips Emitting / Array
Prior to Anodisation	~80% of tips tested emitted
After Anodisation	100% of tips tested emitted

Table 7.11 Proportion of P-Type and P^+-Type Tips Tested which Emitted Before and After Anodisation

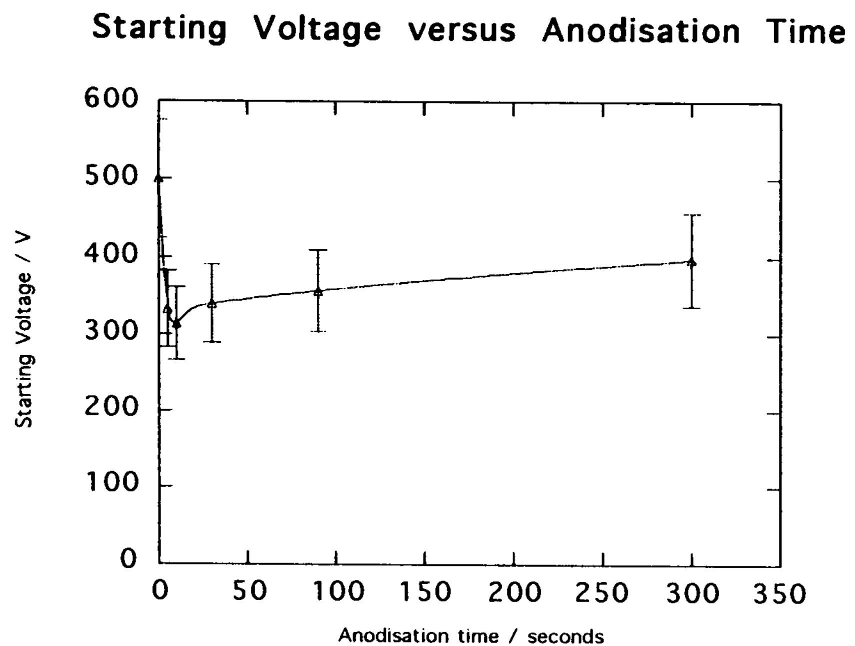
Anodisation Time / Seconds	Porous Silicon Layer Thickness / nm	Starting Voltage	Range & Standard Deviation	Reduction in Starting Voltage
0	0	500V	300V-670V (370V range) ± 80V	n/a
5	14	335V	200V-500V (300V range) ± 85V	33%
10	20	315V	170V-500V (330V range) ± 95V	37%
30	25	340V	215V-505V (290V range) ± 30V	32%
90	50	355V	290V-500V (210V range) ± 50V	29%
300	50	395V	220V-700V (480V range) ± 120V	21%

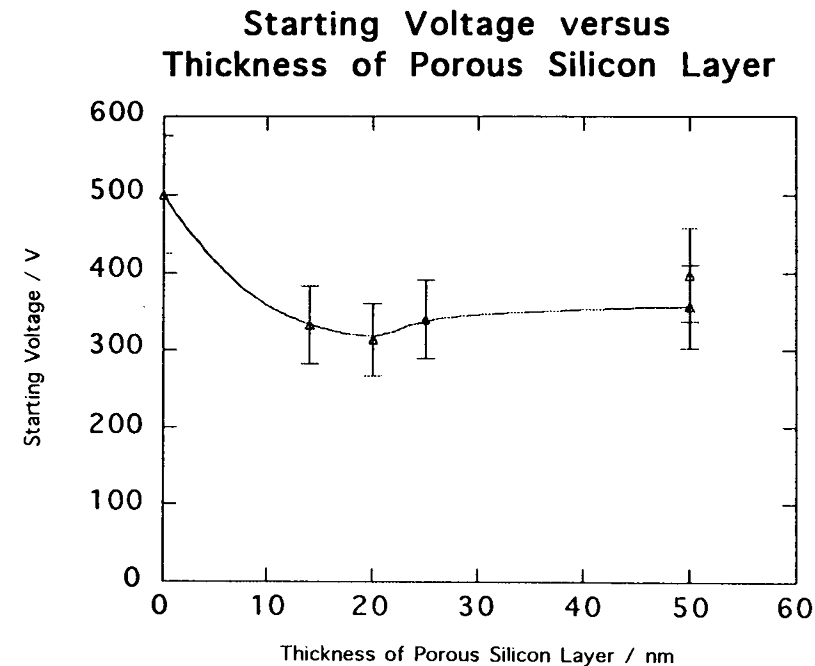
20 tips Examined per Sample

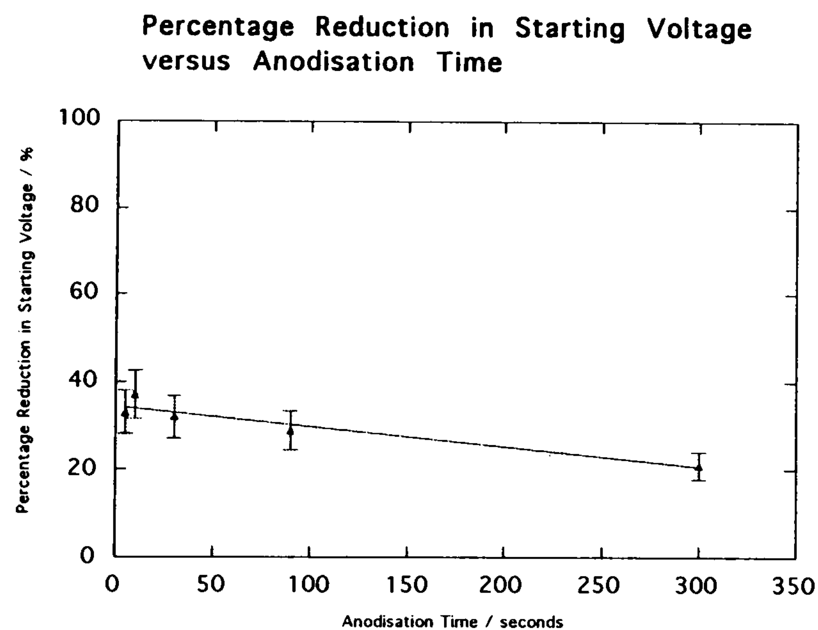
Anodisation Time / Seconds	Porous Silicon Layer Thickness / nm	Starting Voltage	Range & Standard Deviation	Reduction in Starting Voltage
0	0	510V	420V-600V (180V range) ± 60V	n/a
5	14	340V	240V-500V (260V range) ±85V	33%
30	25	355V	190V-540V (350V range) ± 100V	31%
90	50	425V	240V-500V (260V range) ± 85V	17%
300	50	410V	250V-660V (410V range) ± 135V	20%

10 tips Examined per Sample

Table 7.12 Reduction in Starting Voltage for Each Anodisation Time







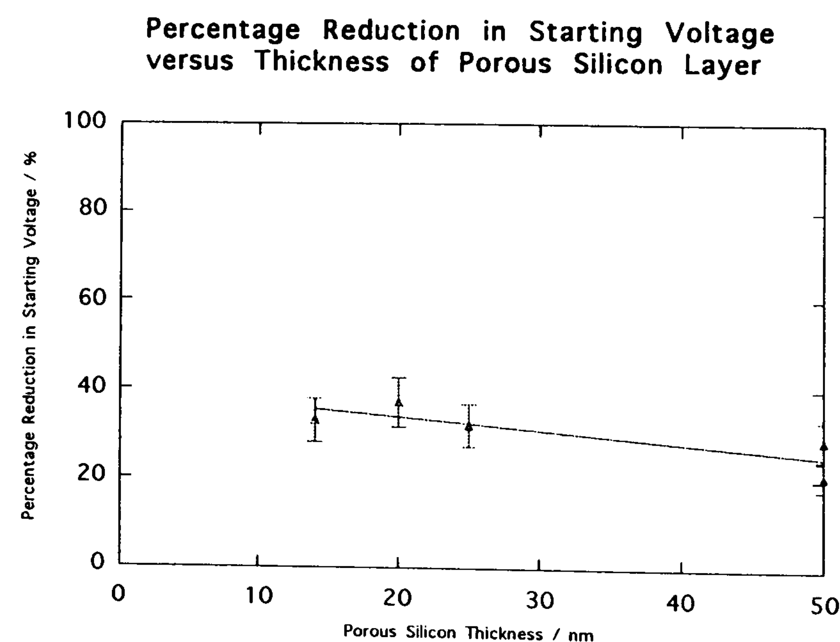
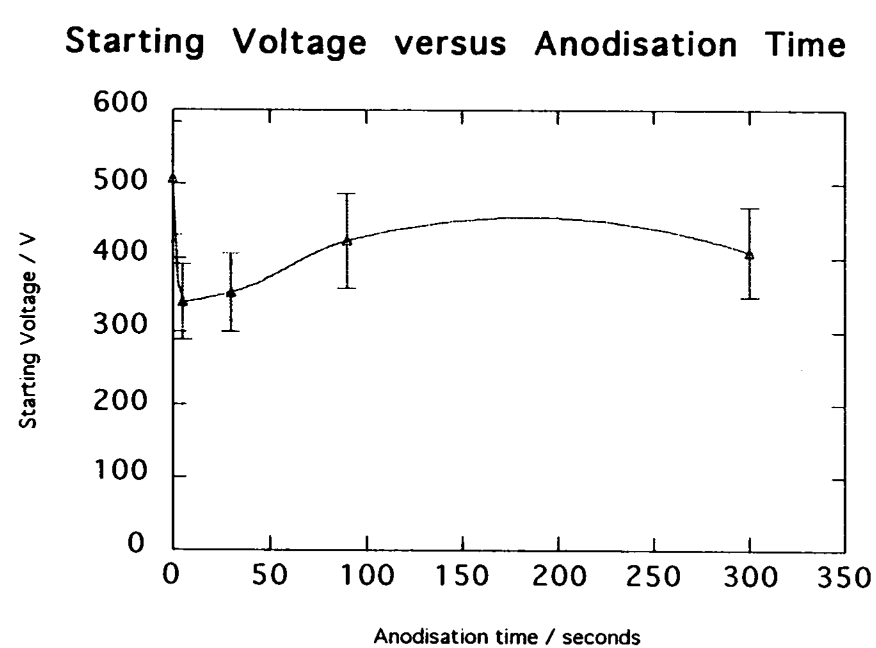
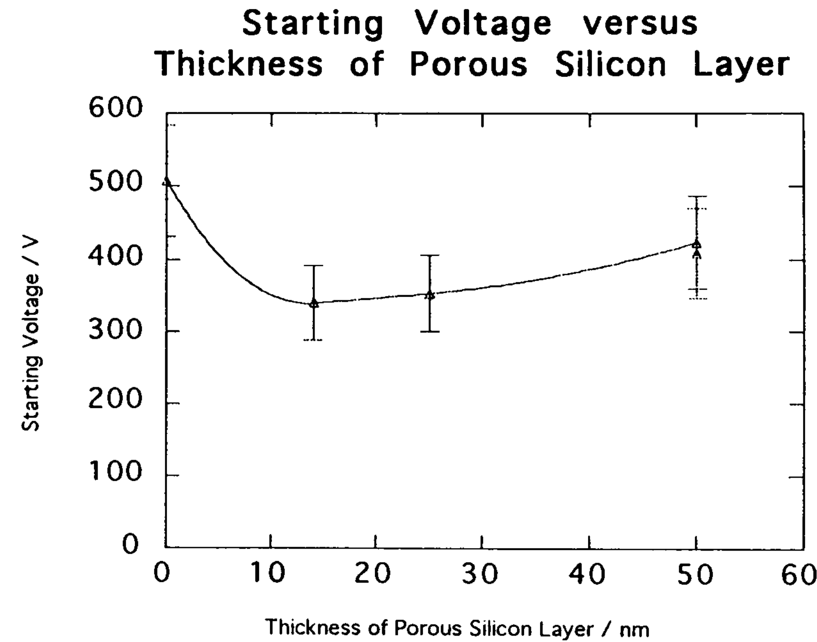
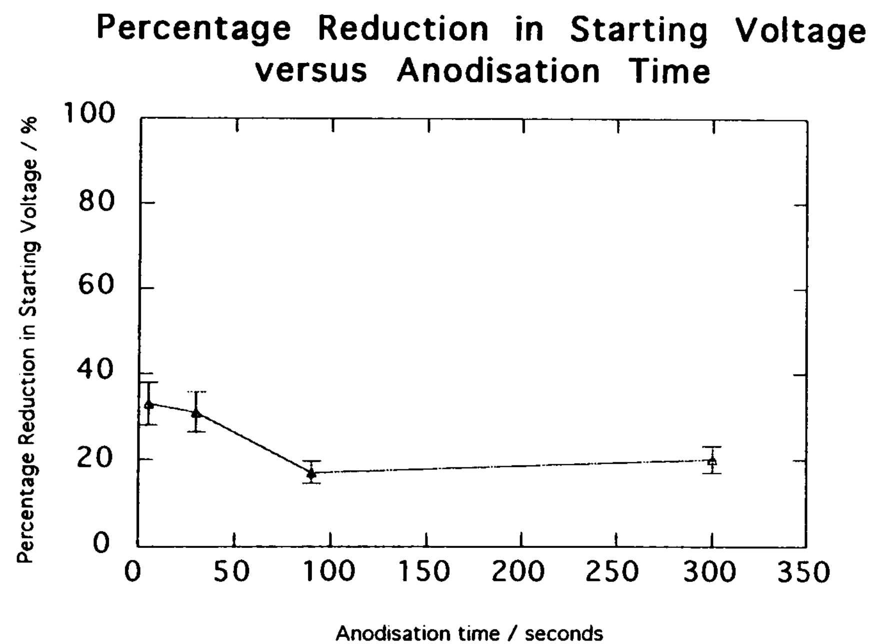


Figure 7.2a - Starting Voltage and Percentage Drop in Starting Voltage versus Anodisation and Thickness of Porous Layer ≈20 tips per sample







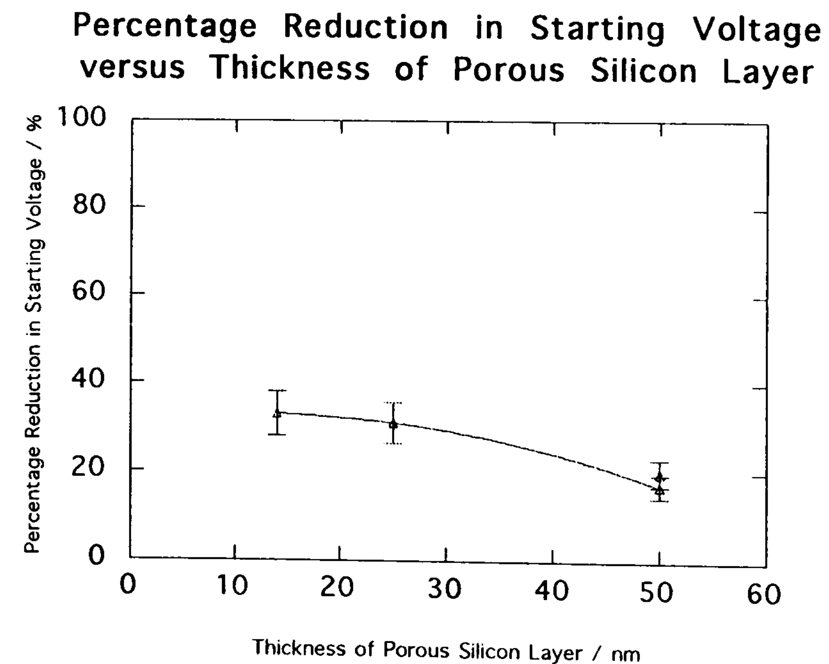


Figure 7.2b - Starting Voltage and Percentage Drop in Starting Voltage versus Anodisation and Thickness of Porous Layer ≈10 tips per sample

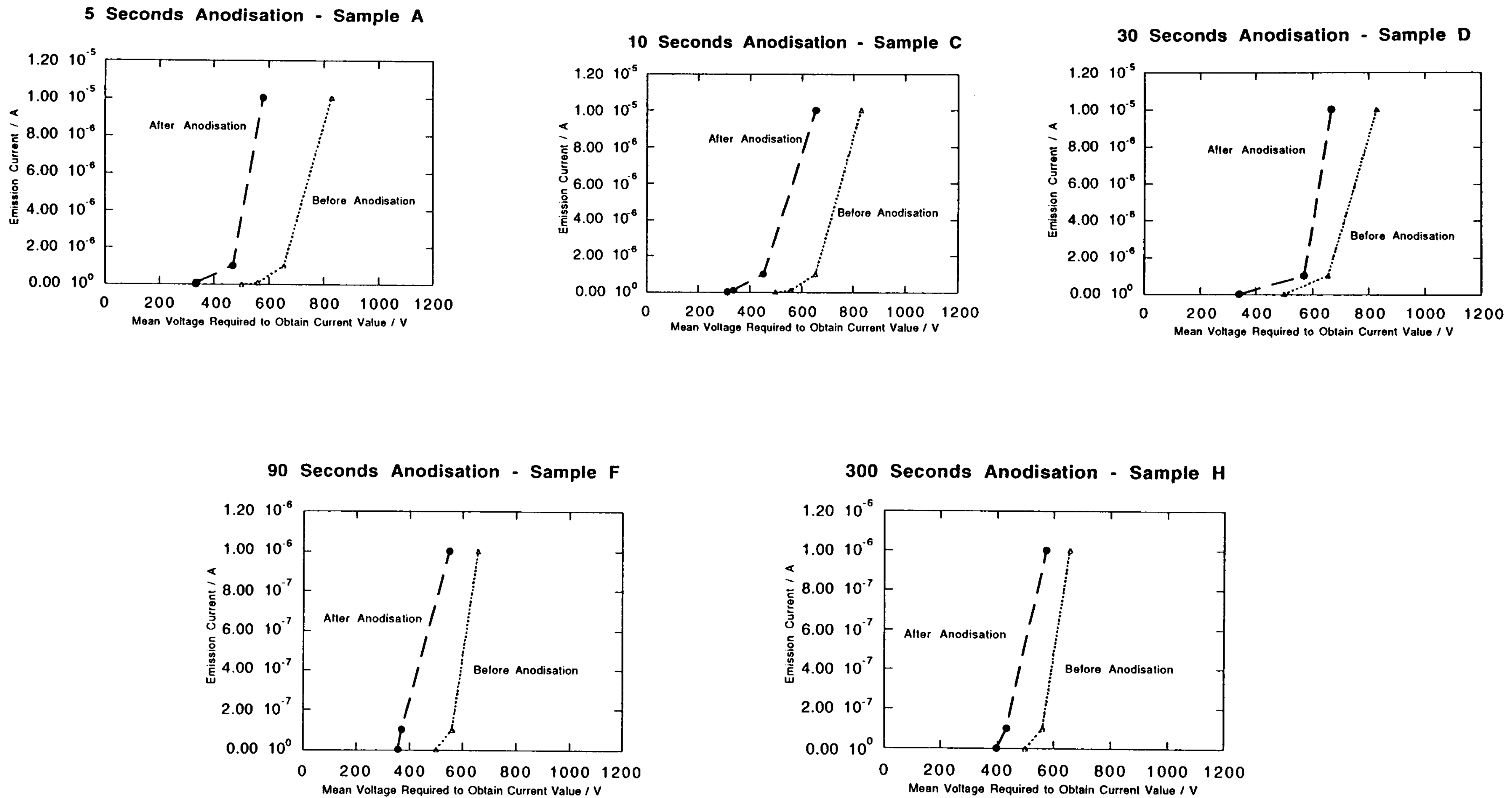
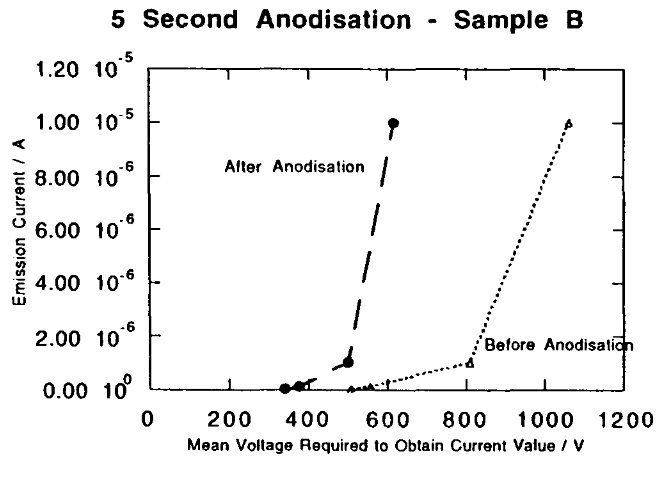
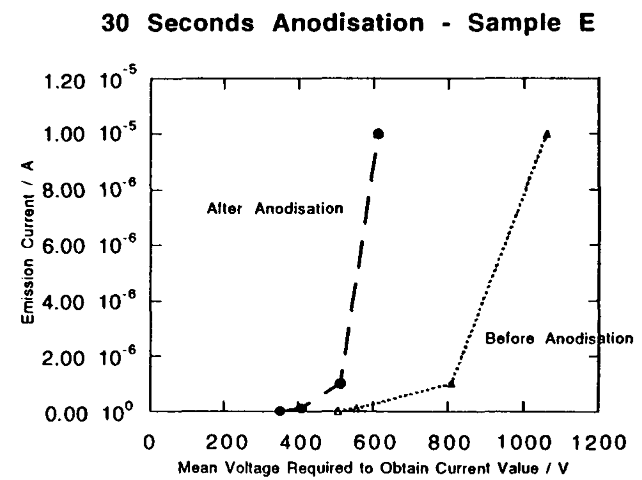
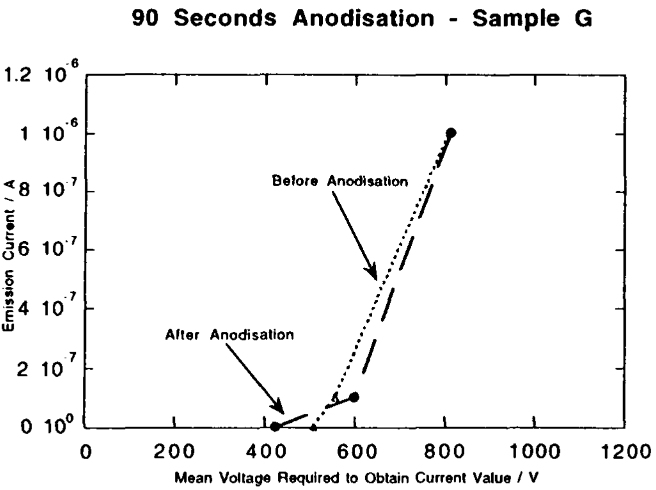


Figure 7.3a - Mean Voltage Required to Obtain Certain Current Values ≈20 tips per sample examined







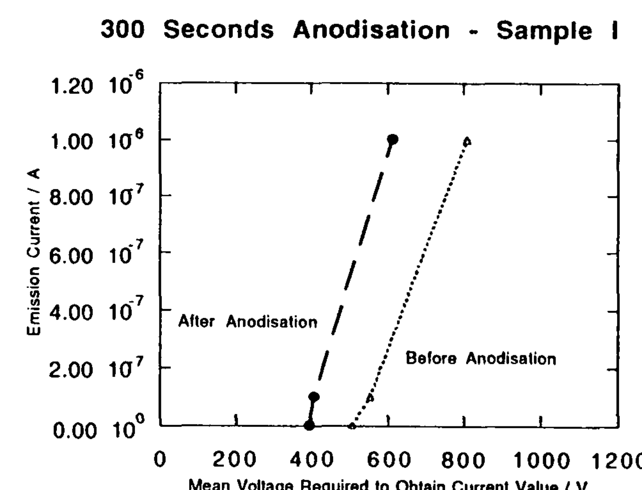


Figure 7.3b - Mean Voltage Required to Obtain Certain Current Values ≈10 tips per sample examined

Anodisation Time / Seconds	Porous Silicon Layer Thickness / nm	Voltage Required to Obtain 0.1μA + % Reduction	Voltage Required to Obtain 1μA + % Reduction	Voltage Required to Obtain 10μA + % Reduction
0	0	560V	655V	830V
5	14	335V 40% drop	470V 27% drop	580V 30% drop
10	20	335V 40% drop	455V 31% drop	655V 21% drop
30	25	n/a	570V 13% drop	670V 20% drop
90	50	370V 34%, drop	550V 18% drop	n/a (tip blew before)
300	50	430V 34% drop	575V 13% drop	n/a (tip blew before)

20 tips examined per sample

Anodisation Time / Seconds	Porous Silicon Layer Thickness / nm	Voltage Required to Obtain 0.1μA + % Reduction	Voltage Required to Obtain 1μA + % Reduction	Voltage Required to Obtain 10μA + % Reduction
0	0	555V	810V	1060V
5	14	375V 33% drop	500V 39% drop	620V 43% drop
30	25	410V 27% drop	515V 37% drop	615V 43% drop
90	50	600V 11% increase	810V No change	n/a (tip blew before)
300	50	395V 29% drop	615V 24% drop	n/a (tip blew before)

10 tips examined per sample

Table 7.13 Reduction in Voltage Required to Obtain Given Current Values

i) The mean voltages required to obtain current values >1nA, were also significantly reduced following anodisation. The mean values for non-anodised emitters have been added for comparison. For example, for one sample anodised for 5 seconds, 10μA was obtained at 580V; whereas for a non-anodised sample, 10μA was obtained at a much higher voltage of 830V. This represents a drop of 48% in the voltage required to obtain 10μA.

ii) A similar result was observed for all anodisation times. However, the difference before and after anodisation, appeared to decrease as the anodisation time increased. For example, for an anodisation time of 5 seconds, only 469V was required to obtain 1μA, versus 656V for non-anodised silicon. However, for an anodisation time of 300 seconds, 573V was required to obtain 1μA.

iii) Similar results were obtained from both sets of samples.

In addition, the rate of increase of current with voltage (dI/dV) (i.e. slope of I-V curve) for individual plots was calculated before and after anodisation. The value of dI/dV was calculated at different current levels - in the range 0.1μA-1μA and in the range 1μA-10μA. The results are summarised in Table 7.14. The main results were as follows:

i) The mean value of dI/dV was ~3 times higher for anodised tips than for non-anodised tips, for each current level (for anodisation times in the range 5-30 seconds.)

d) Nature of the Fowler-Nordheim (FN) Plot

The nature of the Fowler-Nordheim plots were compared for plain and anodised emitters. In addition, the current value at the start of the plateau region and the length of the plateau region (for those emitters exhibiting typical p-type emission) were compared. The results are summarised in Table 7.15. The main points are outlined below:

i) For both anodised and non-anodised samples, the majority of tips exhibited typical p-type 3-stage emission (see Chapter 2).

Anodisation Time	**Mean Value of dI/dV for currents in range 0.1μA-1μA**	**Mean Value of dI/dV for currents in range 1μA-10μA**
0	0.003 μA/V	0.03 μA/V
5	0.01 μA/V	0.1 μA/V
10	0.009 μA/V	0.1 μA/V
30	0.01 μA/V	0.1 μA/V
90	0.005 μA/V	0.04 μA/V
300	0.004 μA/V	0.01 μA/V

Note that: 1) Following anodisation, rate of increase of current with voltage (dI/dV) increases.
2) dI/dV decreases as the anodisation time increases.

Table 7.14 Rate of Increase of Current with Voltage

Sample	**Current Value at Start of Stage II Plateau Region**	**Mean Length of Plateau Region**
Non-Anodised	0.2μA	300V (Range: 250V-650V)
Anodised for 5 seconds	0.2μA	90V (Range: 25V-130V)

Similar data was obtained for all anodisation times.
Note that: 1) Current value at start of and during plateau was similar before and after anodisation
2) The length of the plateau was much shorter following anodisation.

Table 7.15 Comparison of Fowler-Nordheim Plots

ii) The Stage II plateau began at approximately the same current value (i.e. ~0.2μA) for both anodised and non-anodised samples.

iii) For anodised emitters, the plateau region was on average one third of the length of the plateau region for non-anodised emitters.

e) Maximum Current Obtained Prior to Destruction of Emitter

During the early tests carried out during the Part II thesis, it was found that the maximum emission current obtained prior to tip destruction increased by up to 10 times following anodisation. However, these results needed to be confirmed.

The maximum field emission current collected prior to destructive failure of the emitter, was recorded for each anodisation time. Distributions of maximum current for each anodisation time are shown in Figure 7.4, and the results are summarised in Table 7.16. Figure 7.5 shows mean maximum current plotted versus both anodisation time and PS layer thickness. In addition, the proportion of tips blowing below a certain current level was calculated. Figure 7.5 also shows the percentage of tips which underwent self-destruction at currents <5μA plotted versus the anodisation time and PS layer thickness at the tip apex. These results are summarised in Table 7.17. The main points are summarised below:

i) Maximum Current Increased Slightly For Very Thin Porous Silicon Layers

For thin PS layers, there was an increase in maximum current versus non-anodised FEAs. However, there was variation between samples. For one sample anodised for 5 seconds (PS layer thickness of 14nm at tip apex), the maximum current was 3.9 times higher than before anodisation; whereas a second sample also anodised for 5 seconds only exhibited a 1.5 times increase following anodisation. However, for both these samples, 0% of tips blew at current levels <5μA; whereas at least 25% of non-anodised tips blew at current values <5μA. However, the increase in emission current following anodisation was lower than observed during the Part II project and during the early stages of the work carried out for this thesis. In those cases, the current was found to be ~10 times greater following anodisation. However, those samples were

Anodisation Time / Seconds	Porous Silicon Layer Thickness / nm	Mean Maximum Current	Current (after anodisation)/ current (before anodisation)
0	0	10 μA	n/a
5	14	15μA	1.5
10	20	12μA	1.2
30	25	8μA	0.8
90	50	2.4μA	0.24
300	50	1.2μA	0.1

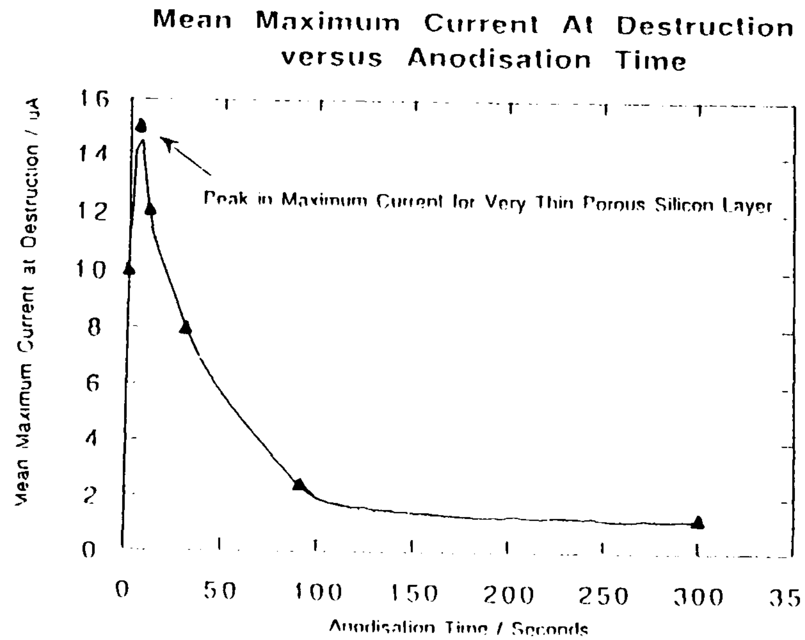
20 tips examined per sample

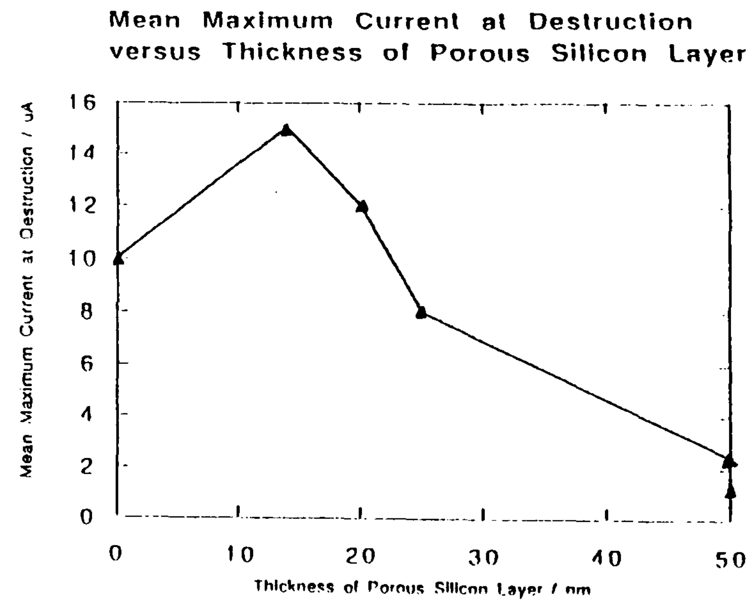
Anodisation Time / Seconds	Porous Silicon Layer Thickness / nm	Mean Maximum Current	Current (after anodisation)/ current (before anodisation)
0	0	14 μA	n/a
5	14	55μA	3.9
30	25	25μA	1.8
90	50	1.1μA	0.08
300	50	1.9μA	0.1

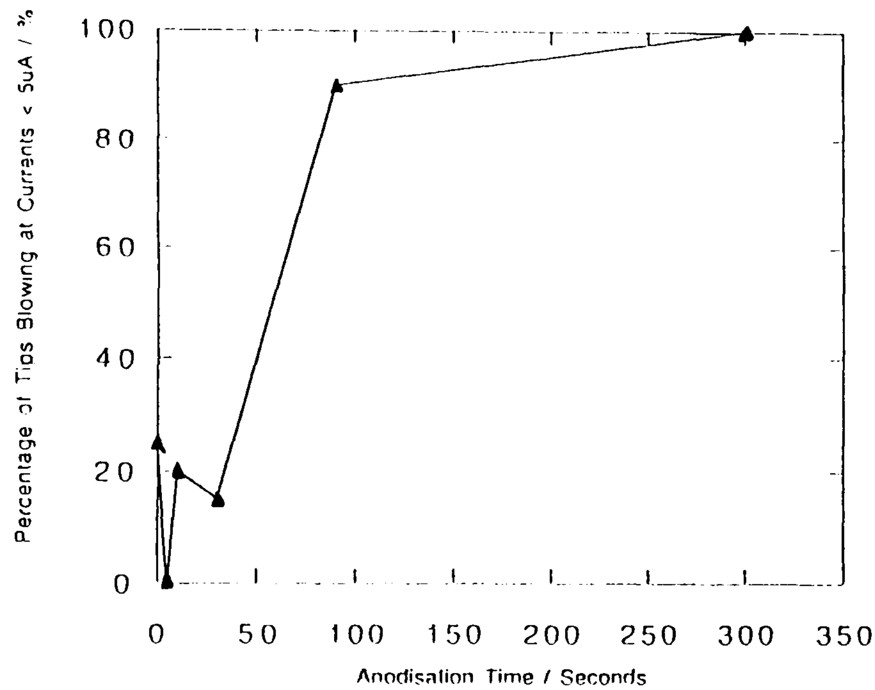
10 tips per sample

Note that: 1) There is some increase in maximum current following anodisation.
2) The maximum current decreased as the anodisation time increased.

Table 7.16 Maximum Emission Currents for Each Anodisation Time







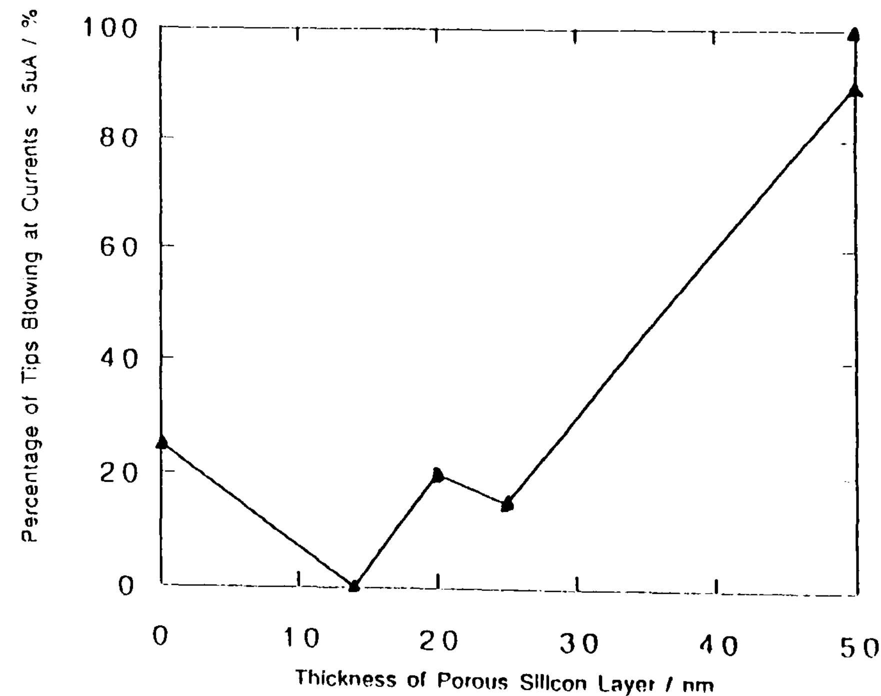
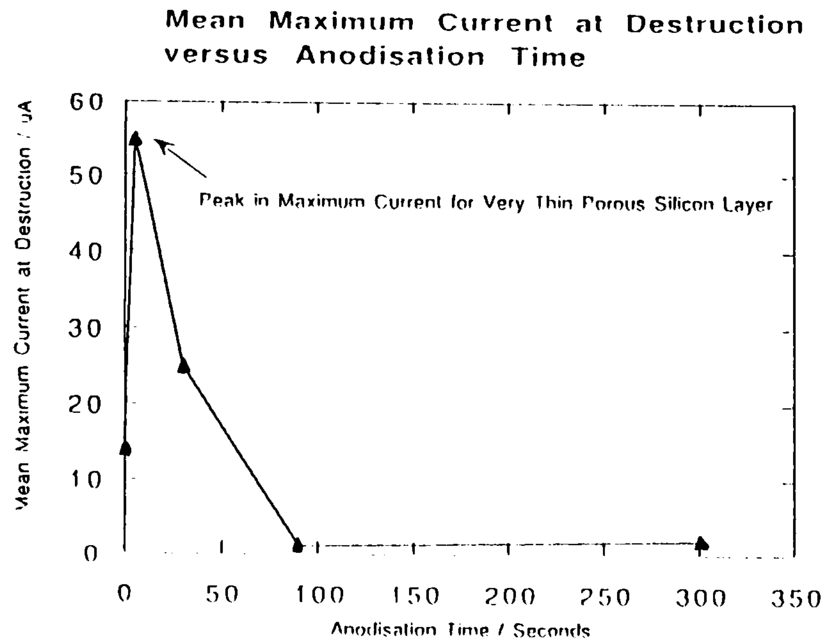
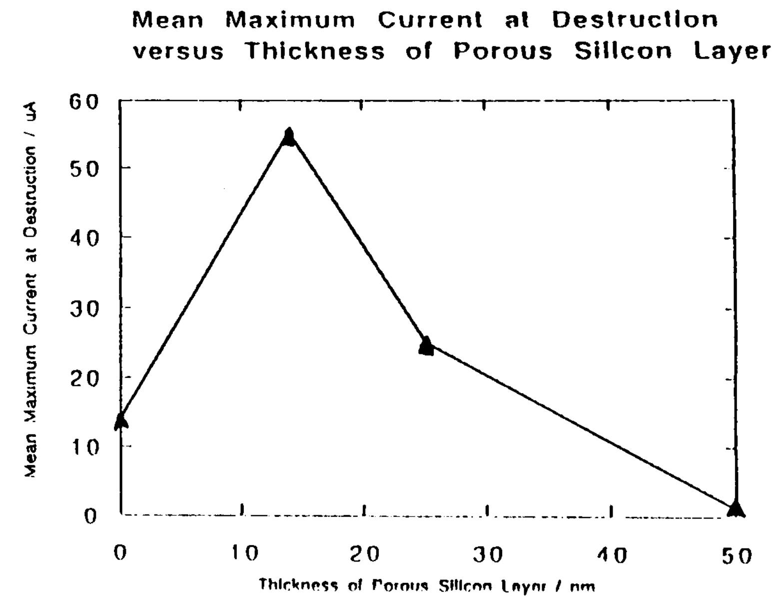
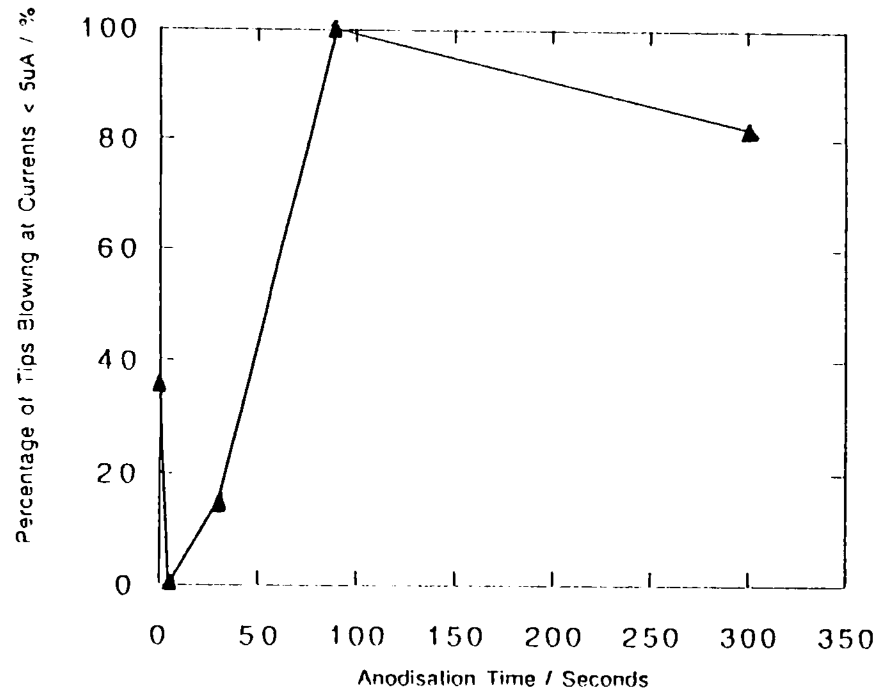


Figure 7.5a - Mean Maximum Emission Current and Percentage Tips Blowing at Currents <5μA versus Anodisation Time and versus Thickness of Porous Silicon Layer
≈20 tips per sample examined







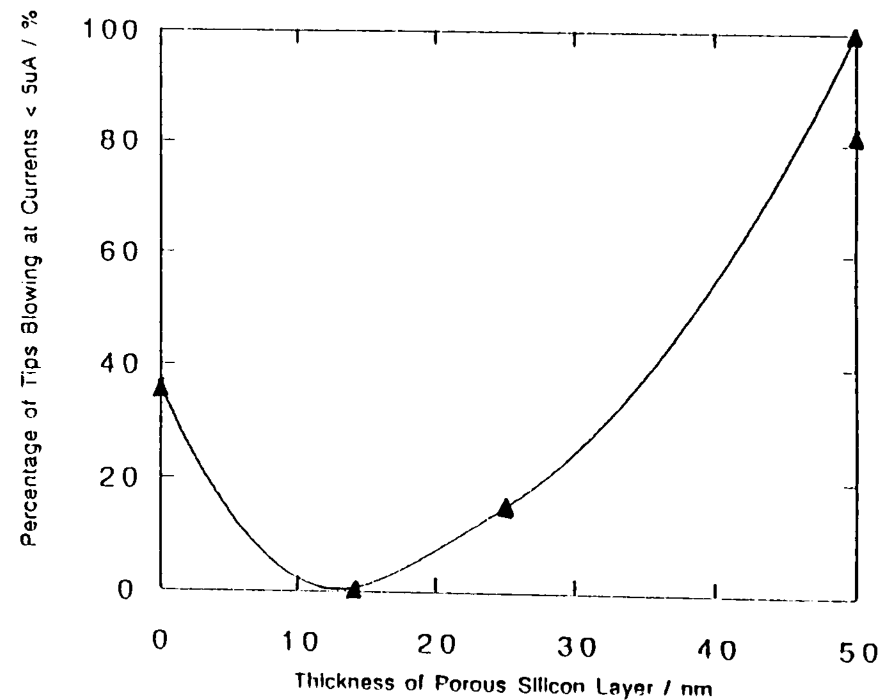


Figure 7.5b - Mean Maximum Emission Current and Percentage Tips Blowing at Currents <5μA versus Anodisation Time and versus Thickness of Porous Silicon Layer
≈10 tips per sample examined

Anodisation Time / Seconds	Thickness of Porous Silicon Layer / nm	% Tips blowing <5μA
0	0	25%
5	14	0%
10	20	20%
30	25	15%
90	50	90%
300	50	100%

20 tips per sample

Anodisation Time / Seconds	Thickness of Porous Silicon Layer / nm	% Tips blowing <5μA
0	0	36%
5	14	0%
30	25	0%
90	50	100%
300	50	82%

10 tips per sample

Table 7.17 Percentage of Tips Blowing at Currents <5μA

examined in a poor vacuum, using a less uniform FEA which had a different basic apex morphology (tips were over-etched versus square-topped under-etched emitters). These differences could have significantly affected the maximum emission current recorded.

ii) Maximum Current Decreased As Porous Silicon Layer Thickness Decreased

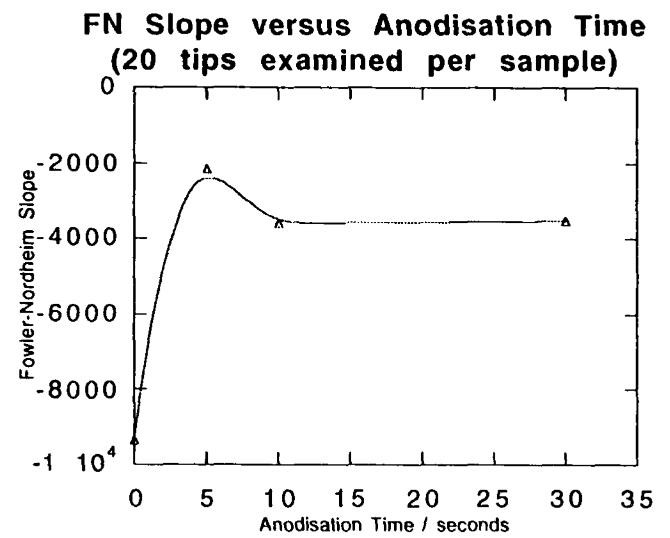
The maximum current obtained prior to self-destruction peaked at an anodisation time of 5 seconds (PS layer thickness of 14nm at tip apex). For longer anodisation times, the maximum current decreased. Plots of maximum emission current versus actual PS layer thickness (rather than versus anodisation time) show that after peaking at a PS layer thickness of 14nm, the maximum current obtained decreased with increasing PS layer thickness at the tip apex (as observed in TEM). In addition, the proportion of tips blowing at current values $<5\mu A$ increased with anodisation time (after dropping to zero for anodisation times of 5 seconds). For samples anodised for 90 and 300 seconds, the maximum current obtained before destruction was up to 10 times lower following anodisation, and the proportion of tips blowing at currents $<5\mu A$ was 100% - i.e. much greater than for non-anodised tips.

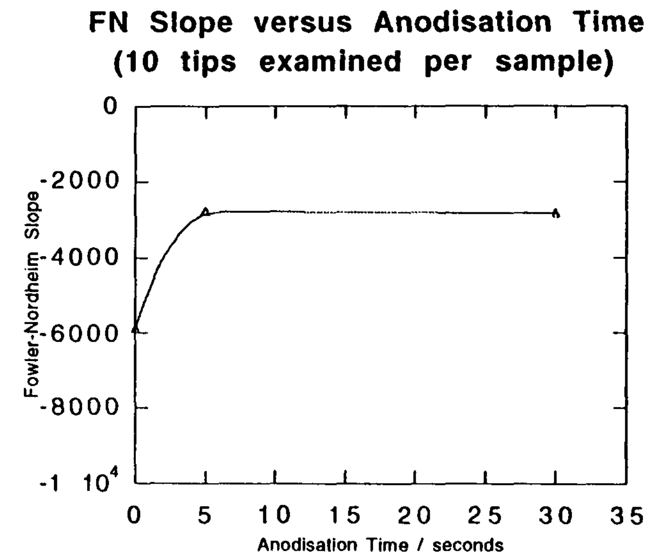
f) Slope and Intercept of Fowler-Nordheim Plot and Calculations of Field Enhancement Factor, Emission Areas and Radii

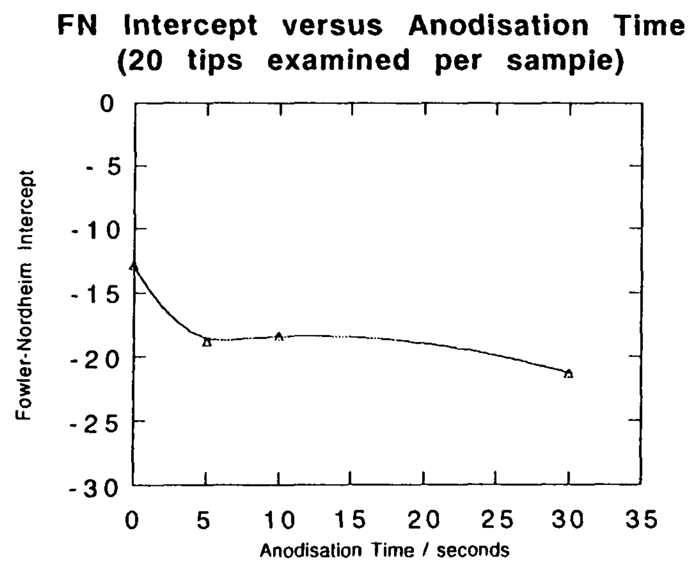
i) Calculation of Slope and Intercept

If the slope and intercept of an FN plot can be obtained, the field enhancement factor (β), emission area (α) and emitting tip radius (r) can be calculated (if a value for the work function is known or assumed). Distributions of slope and intercept before and after anodisation are shown in Figure 7.6. Figure 7.7 shows FN slope and intercept plotted versus anodisation time. The slope and intercept of FN plots obtained from samples anodised for times in the range 5-30 seconds are summarised in Table 7.18. Note that for FN plots which did not contain enough data points, or where Stage I Fowler-Nordheim emission could not be clearly identified, calculation of the FN slope and intercept were not attempted. For samples anodised for 90 and 300 seconds, the FN plots were very noisy - therefore, the slope and intercept were not calculated for those samples either.

The main results are outlined below - both sets of samples show similar results:







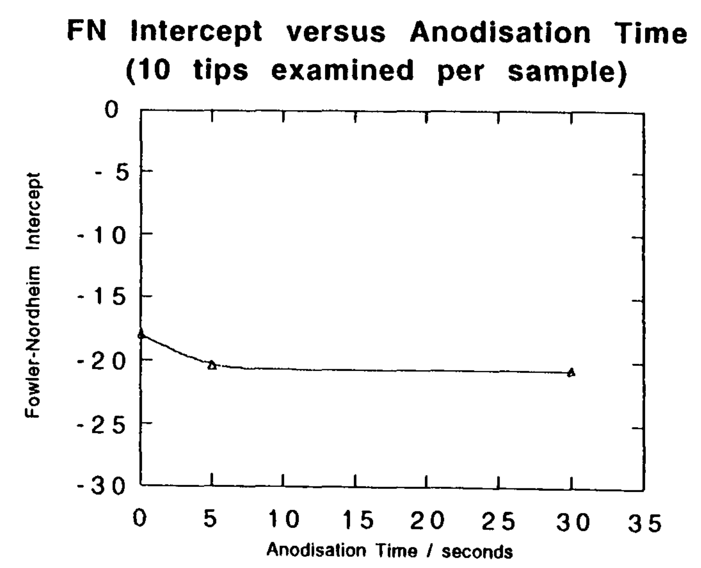


Figure 7.7 - Fowler-Nordheim Slope and Intercept plotted versus Anodisation Time

Anodisation Time / Seconds	FN Slope	FN Slope (Before Anodisation) / FN Slope (After Anodisation)	FN Intercept After Anodisation
0	-9360	n/a	-12.9
5	-2150	4.4	-18.8
10	-3575	2.6	-18.4
30	-3510	2.7	-21.3

20 tips per sample

Anodisation Time / Seconds	FN Slope	FN Slope (Before Anodisation) / FN Slope (After Anodisation)	FN Intercept After Anodisation
0	-5897	n/a	-18.0
5	-2776	2.1	-20.4
30	-2830	2.1	-20.7

10 tips per sample

Note that: 1) Following anodisation, the FN slope decreased.
2) Following anodisation, the FN intercept became more negative.

Table 7.18 Fowler-Nordheim Slope and Intercept Before and After Anodisation (for Different Anodisation Times)

1) The values obtained from anodised samples were 2-4 times lower in value than those obtained from non-anodised tips.

2) The values of slope and intercept did not depend strongly on the anodisation time.

3) The value of the intercept became more negative following anodisation. Distributions of intercept showed that following anodisation, the majority of values were within the range (-25) to (-20); whereas prior to anodisation, the majority of values lie within the range (-15) to (-10).

Both results indicate that emission from anodised tips occurred from sites which were sharper than for non-anodised tips. In order to obtain further information about the nature of the emission sites, the field enhancement factor and emitting tip radius needed to be calculated. (However, it should be noted that the absolute values of slope and intercept would have been influenced by the fact that the vacuum system in which these results were taken was not UHV and that the tip surface will not have been adsorbate free. In particular, calculated values of the emission area will have been affected by contamination.)

ii) Calculation of Field Enhancement Factor

The field enhancement factor could be calculated from the FN slope using equation 2.12 from Chapter 2:

$$b = 6.488\text{x}10^{7}\,\frac{\phi^{\frac{3}{2}}}{\beta}$$

where b = -(FN slope); and ϕ (work function) = 4.5eV.

Using this equation, the field enhancement factor was calculated for different anodisation times - these values are summarised in Table 7.19. (Values for anodisation times of 90 or 300 seconds were not calculated, as the FN plots were too noisy and so the values of slope and intercept could not be calculated.) Distributions of field enhancement factor for different anodisation times are shown in Figure 7.8. A plot of field enhancement factor versus anodisation time is shown in Figure 7.9. The main results were as follows:

a) 5 Second Anodisation - Sample A

Value	Sample	Field Enhancement Factor (β)	Emission Area (α) / cm^2	Tip Radius (r) calculated from α / cm	Tip Radius (r) calculated from β / cm
Mean	a) Before b) After	8.7×10^{4} 4.2×10^{5}	1×10^{-8} 5.5×10^{-13}	2.3×10^{-5} 1.6×10^{-7}	5×10^{-6} 1.2×10^{-6}
Range	a) Before b) After	$3.6 \times 10^{4} - 2.3 \times 10^{5}$ $1.3 \times 10^{5} - 1.2 \times 10^{6}$	$2.3 \times 10^{-15} - 1 \times 10^{-7}$ $2.2 \times 10^{-17} - 9.3 \times 10^{-12}$	$2.7 \times 10^{-8} - 1.8 \times 10^{-4}$ $2.6 \times 10^{-9} - 1.7 \times 10^{-6}$	$1.4 \times 10^{-6} - 9.2 \times 10^{-6}$ $2.6 \times 10^{-7} - 2.6 \times 10^{-6}$
Median	a) Before b) After	7.4×10^{4} 2.8×10^{5}	1.9×10^{-11} 3.4×10^{-16}	2.3×10^{-6} 1×10^{-8}	4.7×10^{-6} 1.2×10^{-6}
Standard Deviation	a) Before b) After	$\pm 5.7 \times 10^{4}$ (±66%) $\pm 3 \times 10^{5}$ (±71%)	$\pm 3.6 \times 10^{-12}$ (±0.04%) $\pm 2.2 \times 10^{-12}$ (±400%)	$\pm 5.5 \times 10^{-5}$ (±240%) $\pm 3.4 \times 10^{-7}$ (±213%)	$\pm 2.3 \times 10^{-6}$ (±46%) $\pm 6.3 \times 10^{-7}$ (±52%)

b) 5 Second Anodisation - Sample B

Value	Sample	Field Enhancement Factor (β)	Emission Area (α) / cm^2	Tip Radius (r) calculated from α / cm	Tip Radius (r) calculated from β / cm
Mean	a) Before b) After	1.3×10^{5} 4.8×10^{5}	3.6×10^{-11} 3×10^{-11}	1.3×10^{-6} 1.6×10^{-6}	3.2×10^{-6} 1.6×10^{-6}
Range	a) Before b) After	$8 \times 10^{4} - 2.9 \times 10^{5}$ $1.5 \times 10^{4} - 1.3 \times 10^{6}$	$1.7 \times 10^{-17} - 3.9 \times 10^{-10}$ $2.2 \times 10^{-19} - 1.8 \times 10^{-10}$	$2.3 \times 10^{-9} - 1.1 \times 10^{-5}$ $2.7 \times 10^{-10} - 7.6 \times 10$	$1.1 \times 10^{-6} - 4.1 \times 10^{-6}$ $2.7 \times 10^{-10} - 7.7 \times 10^{-6}$
Median	a) Before b) After	9×10^{5} 4.6×10^{5}	2.9×10^{-13} 4.6×10^{-17}	3×10^{-7} 3.9×10^{-9}	3.6×10^{-6} 1.9×10^{-6}
Standard Deviation	a) Before b) After	6.5×10^{4} (±50%) 4.6×10^{5} (±96%)	1.2×10^{-10} (±334%) 6.5×10^{-11} (±217%)	3.3×10^{-6} (±254%) 2.8×10^{-6} (±175%)	1×10^{-6} (±31%) 6.8×10^{-7} (±42%)

Table 7.19 Calculated Values of Field Enhancement Factor, Emission Area and Tip Radius (Continued Overleaf)

c) 10 Second Anodisation - Sample C

Value	Sample	Field Enhancement Factor (β)	Emission Area (α) / cm^2	Tip Radius (r) calculated from α / cm	Tip Radius (r) calculated from β / cm
Mean	a) Before b) After	8.7×10^4 2.2×10^5	1×10^{-8} 1.5×10^{-11}	2.3×10^{-5} 1.1×10^{-6}	5×10^{-6} 2.1×10^{-6}
Range	a) Before b) After	$3.6 \times 10^4 - 2.3 \times 10^5$ $7.8 \times 10^4 - 7.0 \times 10^5$	$2.3 \times 10^{-15} - 1 \times 10^{-7}$ $3.6 \times 10^{-17} - 9.9 \times 10^{-11}$	$2.6 \times 10^{-9} - 1.7 \times 10^{-6}$ $3.3 \times 10^{-9} - 5.6 \times 10^{-6}$	$1.4 \times 10^{-6} - 9.2 \times 10^{-6}$ $4.8 \times 10^{-7} - 4.2 \times 10^{-6}$
Median	a) Before b) After	7.4×10^4 1.7×10^5	1.9×10^{-11} 4.6×10^{-15}	2.3×10^{-6} 3.8×10^{-8}	4.7×10^{-6} 2.2×10^{-6}
Standard Deviation	a) Before b) After	5.7×10^4 (±66%) 1.6×10^5 (±138%)	3.6×10^{-12} (±0.04%) 2.9×10^{-11} (±193%)	5.5×10^{-5} (±239%) 1.9×10^{-6} (±172%)	2.3×10^{-6} (±46%) 1.1×10^{-6} (±52%)

d) 30 Second Anodisation - Sample D

Value	Sample	Field Enhancement Factor (β)	Emission Area (α) / cm^2	Tip Radius (r) calculated from α / cm	Tip Radius (r) calculated from β / cm
Mean	a) Before b) After	8.7×10^4 3.4×10^5	1×10^{-8} 3.3×10^{-10}	2.3×10^{-5} 2.8×10^{-6}	5×10^{-6} 1.9×10^{-6}
Range	a) Before b) After	$3.6 \times 10^4 - 2.3 \times 10^5$ $7.4 \times 10^4 - 1.3 \times 10^6$	$2.3 \times 10^{-15} - 1 \times 10^{-7}$ $3 \times 10^{-21} - 6.5 \times 10^{-9}$	$2.6 \times 10^{-9} - 1.7 \times 10^{-6}$ $3.2 \times 10^{-11} - 4.6 \times 10^{-5}$	$1.4 \times 10^{-6} - 9.2 \times 10^{-6}$ $2.5 \times 10^{-7} - 4.5 \times 10^{-6}$
Median	a) Before b) After	7.4×10^4 2.2×10^5	1.9×10^{-11} 7.8×10^{-17}	2.3×10^{-6} 5×10^{-9}	4.7×10^{-6} 1.5×10^{-6}
Standard Deviation	a) Before b) After	5.7×10^4 (±66%) 3.6×10^5 (±106%)	3.6×10^{-12} (±0.04%) 1.5×10^{-9} (±455%)	5.5×10^{-5} (±239%) 1×10^{-5} (±357%)	2.3×10^{-6} (±46%) 1.3×10^{-6} (±68%)

Table 7.19 Calculated Values of Field Enhancement Factor, Emission Area and Tip Radius (Continued from previous page and continued Overleaf)

e) 30 Second Anodisation - Sample E

Value	Sample	Field Enhancement Factor (β)	Emission Area (α) / cm^2	Tip Radius (r) calculated from α / cm	Tip Radius (r) calculated from β / cm
Mean	a) Before b) After	1.3×10^5 3.5×10^5	3.6×10^{-11} 1.6×10^{-10}	1.3×10^6 2.6×10^{-6}	3.2×10^{-6} 1.5×10^{-6}
Range	a) Before b) After	$8 \times 10^4 - 2.9 \times 10^5$ $1 \times 10^5 - 7 \times 10^5$	$1.7 \times 10^{-17} - 3.9 \times 10^{-10}$ $6.4 \times 10^{-19} - 1.3 \times 10^{-9}$	$2.3 \times 10^{-9} - 1.1 \times 10^{-5}$ $4.5 \times 10^{-10} - 2 \times 10^{-5}$	$1.1 \times 10^{-6} - 4.1 \times 10^{-6}$ $4.7 \times 10^{-7} - 3.3 \times 10^{-6}$
Median	a) Before b) After	9×10^5 3×10^5	2.9×10^{-13} 2.5×10^{-16}	3×10^{-7} 8.6×10^{-9}	3.6×10^{-6} 1.2×10^{-6}
Standard Deviation	a) Before b) After	6.5×10^4 (±50%) 2.3×10^5 (±66%)	1.2×10^{-10} (±334%) 4.6×10^{-10} (±288%)	3.3×10^{-6} (±254%) 7×10^{-6} (±269%)	1×10^{-6} (±31%) 1×10^{-6} (±67%)

Anodisation Time / Seconds	Ratio of Mean Field Enhancement Factors Before and After Anodisation $\beta_{after\ anodisation} / \beta_{before\ anodisation}$
5	4.8
5	3.7
10	2.5
30	3.9
30	2.7

It is clear that: 1) Following anodisation, field enhancement occurs.
2) Following anodisation, the radius of the emitting area is smaller.
3) More reliable values of tip radius are obtained by calculating from β rather than from the emission area α.

Table 7.19 Calculated Values of Field Enhancement Factor, Emission Area and Tip Radius (Continued from previous two pages)

1) Following anodisation, the mean field enhancement factor increased by 2-5 times.

2) The values of field enhancement for samples anodised for 5 seconds was greater than for samples anodised for longer times.

iii) Calculation of Emitting Radius

The radius of the emitting tip (r) was calculated using two different methods:

1) The radius could be calculated from the tip emitting area α using the equation $\alpha=2\pi r^2$. The emitting area α was calculated from the FN slope and intercept using the following equation (see Chapter 2):

$$\alpha = \frac{ab^2}{1.34x10^{13}} cm^2$$

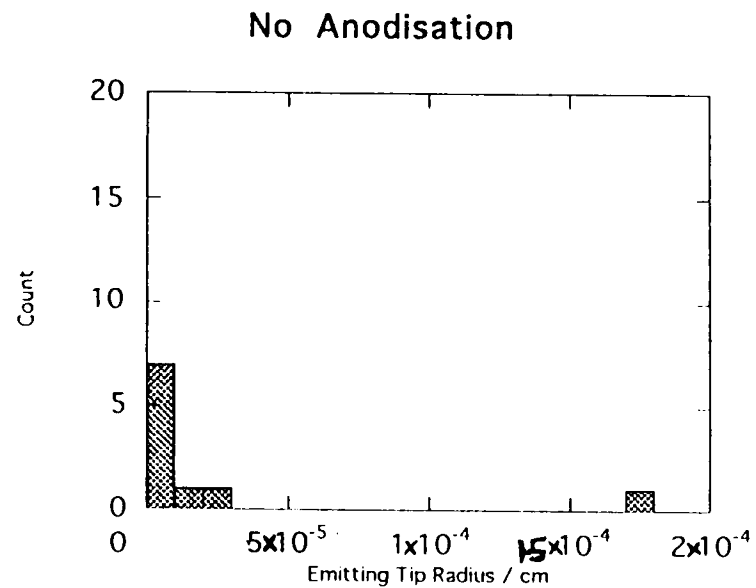
where ln (a) = intercept of Fowler-Nordheim plot; b = slope of Fowler-Nordheim plot.

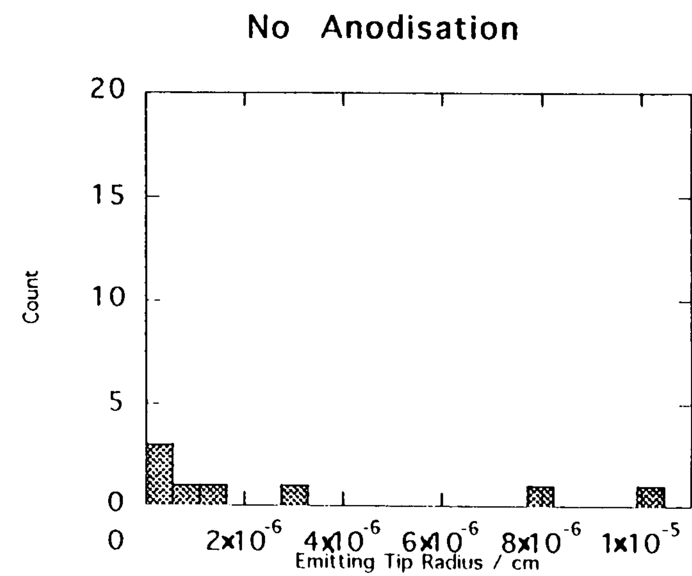
2) The radius could also be calculated from the calculated value field enhancement factor β only. For this method, the equation $\beta=\frac{1}{kr}$ was used, where k~3.

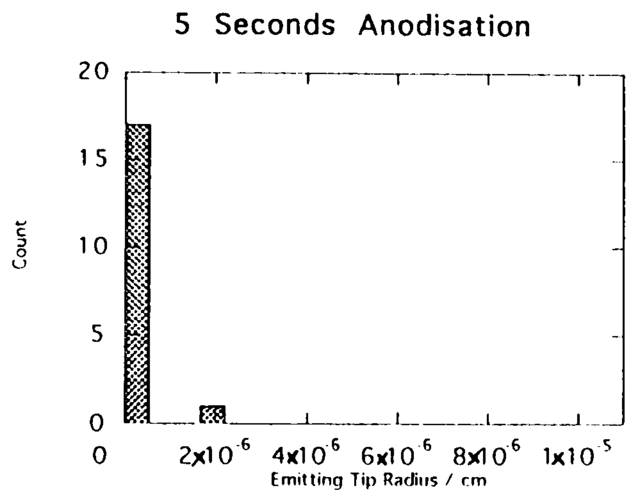
In theory, if the tip surface was completely clean, the values calculated from both methods should have matched. However, under non-UHV conditions, the calculations will have been influenced by contamination. The results from both calculations are summarised in Table 7.19. Distributions of tip radius (calculated from both α and β) are shown in Figure 7.10. Plots of tip radius (calculated from both α and β) versus anodisation time are shown in Figure 7.11.

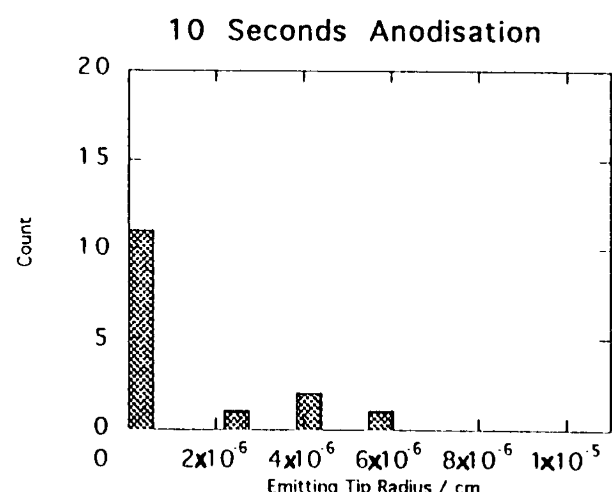
The main results were as follows:

1) For both calculations, the tip radii were smaller following anodisation (assuming no change in ϕ). The radius (calculated from β) was 2-4 times smaller following anodisation. These results indicate that emission occurred from smaller sites on the tip surface following anodisation.









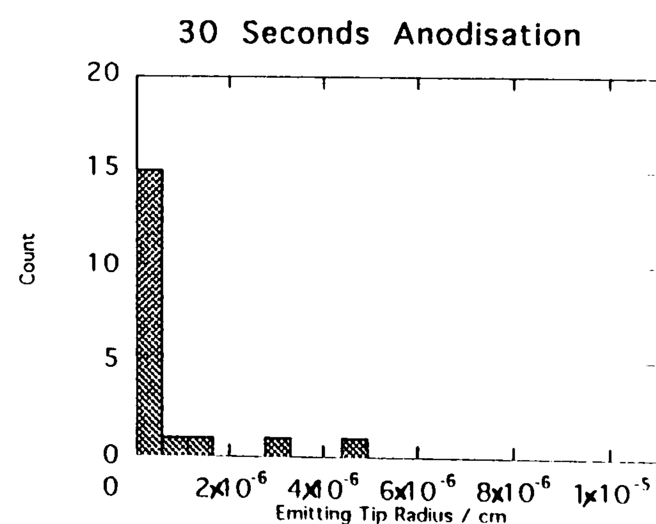
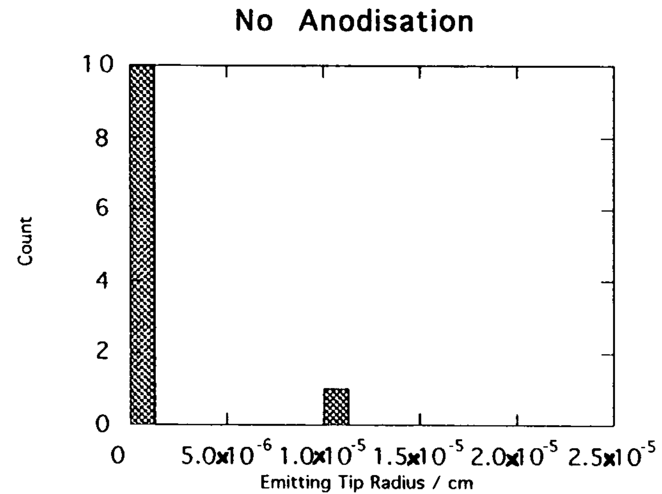
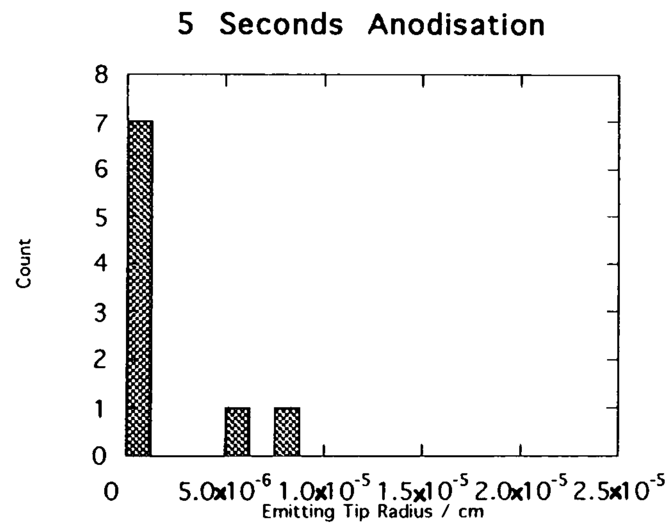


Figure 7.10a - Distribution of Value of Tip Radius (Calculated from Emission Area) for different Anodisation Times
≈20 tips per sample





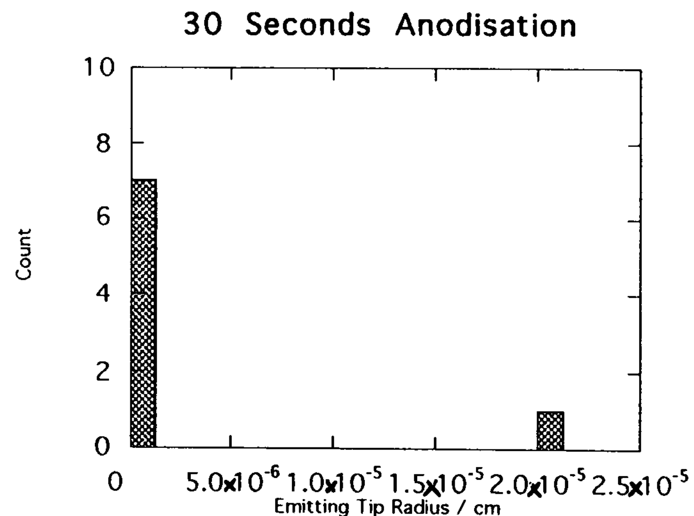


Figure 7.10b - Distribution of Value of Tip Radius (Calculated from Emission Area) for Different Anodisation Times
≈10 tips per sample

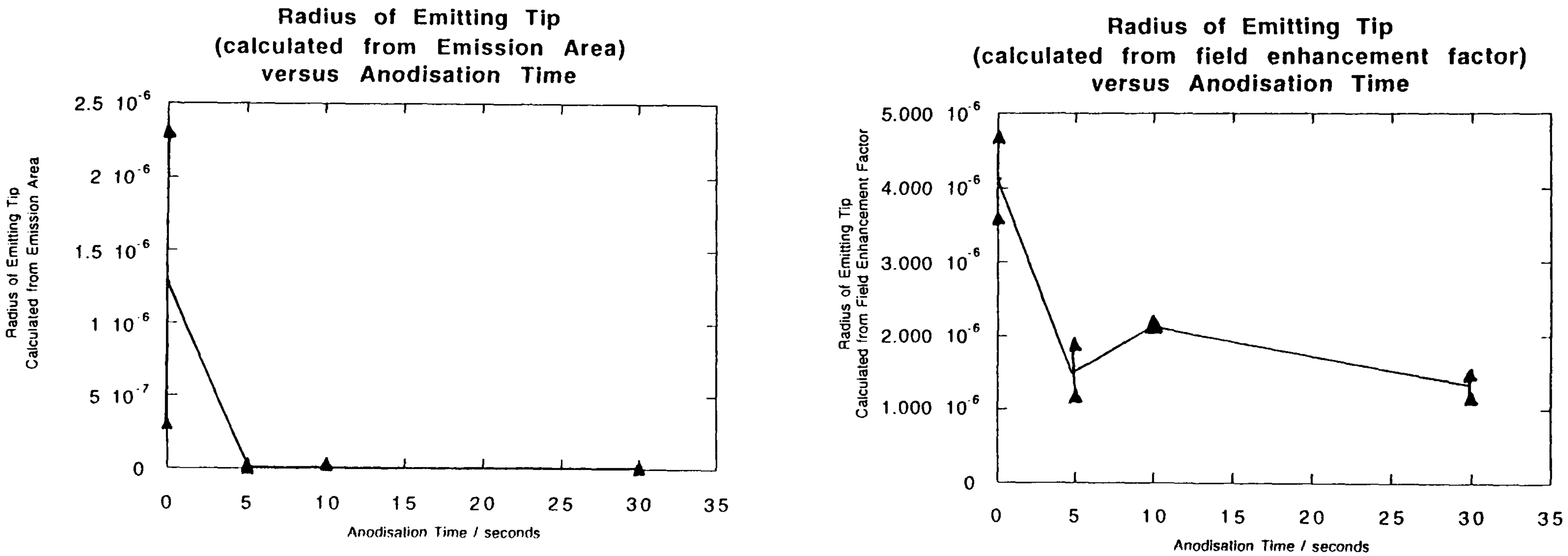


Figure 7.11 - Radius of Emitting Tip (Calculated from Field Enhancement Factor) and Radius of Emitting Tip (Calculated from Emission Area) plotted versus Anodisation Time

Data from both sets of data presented here

Clearly, both plots indicate the tip radius was much smaller following anodisation.

2) The values of tip radius calculated from α and from β were inconsistent. The values calculated from α were ~100 times smaller than the values calculated from β. Also, the difference after anodisation was greater for values calculated from α (the radius being ~10-100 times smaller after anodisation), than indicated from the values calculated from β (i.e. 2-4 times smaller after anodisation). In addition, values for tip radii calculated from α exhibited more scatter than for values calculated from β. Some of values for tip radius calculated from α (for anodised emitters) suggest that the tip was physically smaller than the dimensions of one atom, which clearly cannot be the case. These inconsistencies may have been caused by tip contamination.

h) Specific Examples of Plots Before and After Anodisation

Typical FN and IV plots obtained from individual emitters are shown in Figure 7.12. The key data for each tip is summarised in Table 7.20.

7.2.2 Field Emission from Anodised P+-Type Field Emission Arrays

As it was possible that emission originated at the porous silicon surface, it was important to examine the effect of changing the PS fibril morphology. As TEM had shown (see Chapter 6) that the p^+-type silicon PS morphology at the tip apex was much coarser than for p-type PS, field emission from anodised p^+-type silicon FEAs was investigated. An anodisation current of $100mAcm^{-2}$ was used. All other anodisation and experimental conditions were the same as for p-type FEAs. Table 7.21 summarises the p^+-type samples investigated. Table 7.22-7.26 summarise the data obtained from these samples.

a) Starting Voltage

Distributions of starting voltages for different anodisation times, are shown in Figure 7.13. The mean values of starting voltage, percentage reduction and range of values/standard deviation are summarised in Table 7.27. Plots of starting voltages and percentage reduction in mean starting voltage, versus both anodisation time, and versus PS layer thickness are shown in Figure 7.14. The main points are as follows:

i) As for p-type FEAs, there was a large reduction in starting voltage following anodisation.

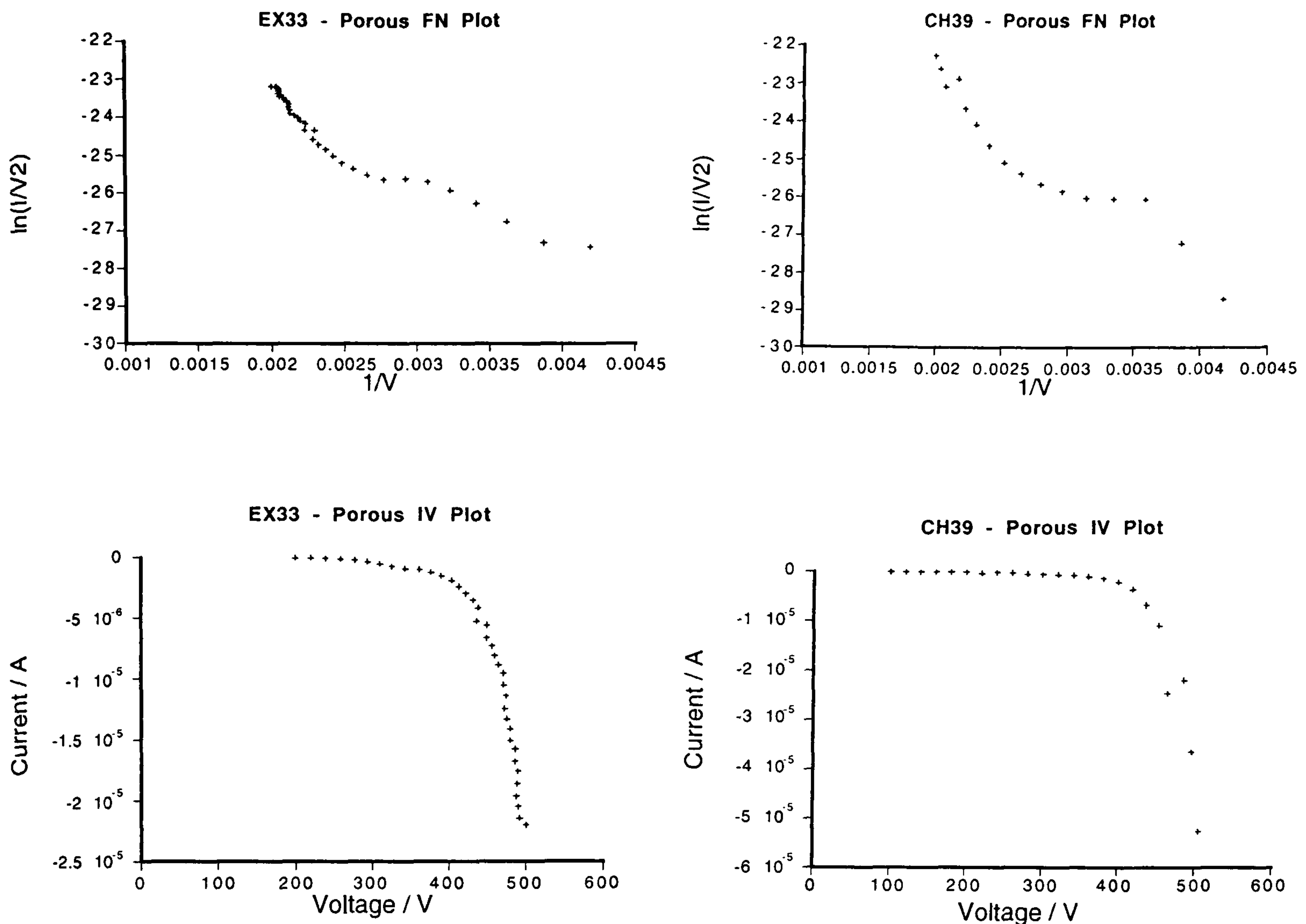


Figure 7.12 - Examples of Fowler-Nordheim and Current-Voltage plots collected from FEAs anodised for 5 Seconds Showing Results from 2 Tips with Lowest Starting Voltages

Emitter Name	ex33 (porous)	ch39 (porous)
Starting Voltage	200V	240V
Maximum Current	23μA	55μA
Maximum Voltage	485V	510V
F-N slope	-2067	-4478
F-N intercept	-19.3	-10.0
Length of Plateau	45V	30V
dI/dV at destruction	0.35 μA/V	0.65μA/V

This table summarises the key data for the plots shown in Figure 7.12. Both tips have low starting voltages. None of the non-anodised tips had such low starting voltages. The best performing tip was CH39, which produced ~60μA at ~500V. Both tips exhibit a short Stage II plateau, typical of p-type silicon emission.

Table 7.20 - Summary Table for P-Type Silicon Emitters (Anodised for 5 Seconds) Showing Lowest Starting Voltages

Anodisation Time / seconds	Sample Codes	Number of Tips Examined
0	I	16
0.25	J, K, L	15, 15, 10
3.5	M	10
10	N	11

Resistivity of the p+-type silicon wafers used to fabricate the FEAs was 0.01Ωcm.

The results obtained from these samples are summarised on Tables 7.22-7.26.

Table 7.21 Summary of Anodised and Non-Anodised P^+-Type Silicon Samples Examined

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	FN slope (m)	FN intercept (c)	Voltage to obtain 0.1µA	Voltage to obtain 1µA	Voltage to obtain 10µA
Mean Value	Before	505V	23µA	760V	-13935	-3.9	570V	600V	670V
	After	260V (49%drop)	15.6µA (14% drop)	425V (38%drop)	-4790 (66%drop)	-17.6 (more -ve)	375V (33%drop)	400V (23%drop)	450V (18%drop)
Spread of Values	Before	300V-700V	5µA-80µA	420V-1200V	(-2405)-(-29325)	(30.5)-(-23.9)	370V-820V	350V-910V	420V-1100V
	After	160V-375V	0.01µA-80µA	170V-700V	(-645)-(-14715)	(-11.2)-(-25.2)	210V-480V	310V-580V	405V-500V
Median Value	Before	520V	17µA	750V	-12890	-9.0	550V	570V	620V
	After	300V	7.5µA	700V	-3670	-18.2	330V	380V	450V
Standard Deviation (+ Coefficient of Variation)	Before	±120V (±24%)	±20µA (±17%)	±190V (±25%)	±9170 (±66%)	±18.3 (±470%)	155V (±29%)	±165V (±27%)	±190V (±28%)
	After	±85V (±25%)	±20µA (±40%)	±135V (±20%)	±3830 (±21%)	4.3 (±24%)	±75V (±22%)	±90V (±22%)	±45V (±10%)

Table 7.22 - Before and After 0.25 Second Anodisation of P^+-Type Silicon - Sample J

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	FN slope (m)	FN intercept (c)	Voltage to obtain 0.1μA	Voltage to obtain 1μA	Voltage to obtain 10μA
Mean Value	Before	505V	23μA	760V	-13935	-3.9	570V	600V	670V
	After	320V (37%drop)	10μA (43% drop)	455V (40%drop)	-4415 (68%drop)	-13.4 (more -ve)	360V (27%drop)	370V (38%drop)	455V (32%drop)
Spread of Values	Before	300V-700V	5μA-80μA	420V-1200V	(-2405)-(-29325)	(30.5)-(-23.9)	370V-820V	350V-910V	420V-1100V
	After	195V-430V	0.45μA-45μA	280V-630V	(-930)-(-8525)	(-2.3)-(-27)	220V-475V	240V-500V	380V-530V
Median Value	Before	520V	17μA	750V	-12890	-9.0	550V	570V	620V
	After	300V	5μA	450V	-5010	-10.9	330V	380V	460V
Standard Deviation (+ Coefficient of Variation)	Before	±120V (±24%)	±20μA (±17%)	±190V (±25%)	±9170 (±66%)	±18.3 (±470%)	155V (±29%)	±165V (±27%)	±190V (±28%)
	After	±70V (±22%)	±12μA (±120%)	±110V (±24%)	±2235 (±50%)	±8.8 (±35%)	±75V (±21%)	±90V (±25%)	±70V (±15%)

Table 7.23 - 0.25 Second Anodisation of P^+-Type Silicon - Sample K

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	FN slope (m)	FN intercept (c)	Voltage to obtain 0.1μA	Voltage to obtain 1μA	Voltage to obtain 10μA
Mean Value	Before	505V	23μA	760V	-13935	-3.9	570V	600V	670V
	After	265V (48%drop)	53μA 230% increase)	445V (42%drop)	-7400 (47%drop)	-11.5 (more -ve)	270V (43%drop)	315V (48%drop)	375V (44%drop)
Spread of Values	Before	300V-700V	5μA-80μA	420V-1200V	(-2405)-(-29325)	(30.5)-(-23.9)	370V-820V	350V-910V	420V-1100V
	After	160V-500V	17μA-110μA	250V-800V	(-705)-(-17385)	(-1.4)-(-25.1)	195V-330V	190V-560V	225V-740V
Median Value	Before	520V	17μA	750V	-12890	-9	550V	570V	620V
	After	260V	62μA	440V	-6710	-8.7	275V	310V	355V
Standard Deviation (+ Coefficient of Variation)	Before	±120V (±24%)	±20μA (±17%)	±190V (±25%)	±9170 (±66%)	±18.3 (±470%)	155V (±29%)	±165V (±27%)	±190V (±28%)
	After	±95V (±36%)	±34μA (±64%)	±150V (±33%)	±5190 (±70%)	±8.7 (±25%)	±60V (±22%)	±120V (±38%)	±160V (±43%)

Table 7.24- 0.25 Second Anodisation of P^+-Type Silicon - Sample L

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	Voltage to obtain 0.1μA	Voltage to obtain 1μA	Voltage to obtain 10μA
Mean Value	Before	505V	23μA	760V	570V	600V	670V
	After	335V (33%drop)	0.1μA (large drop)	545V (29%drop)	520V (9%drop)	n/a	n/a
Spread of Values	Before	300V-700V	5μA-80μA	420V-1200V	370V-820V	350V-910V	420V-1100V
	After	100V-600V	0.08μA-0.18μA	210V-940V	220V-850V	n/a	n/a
Median Value	Before	520V	17μA	750V	550V	570V	620V
	After	325V	0.1μA	550V	480V	n/a	n/a
Standard Deviation (+ Coefficient of Variation)	Before	±120V (±24%)	±20μA (±17%)	±190V (±25%)	155V (±29%)	±165V (±27%)	±190V (±28%)
	After	±160V (±48%)	±0.03μA (±30%)	±235V (±43%)	±235V (±45%)	n/a	n/a

Table 7.25 - 3.5 Second Anodisation of P^+-Type Silicon - Sample M

Parameter	Sample Number	Starting Voltage	Maximum Current	Maximum Voltage	Voltage to obtain 0.1μA
Mean Value	Before	505V	23μA	760V	570V
	After	360V (28%drop)	0.9μA (large drop)	580V (24%drop)	450V (21%drop)
Spread of Values	Before	300V-700V	5μA-80μA	420V-1200V	370V-820V
	After	260V-400V	0.35μA-3.2μA	330V-900V	315V-750V
Median Value	Before	520V	17μA	750V	550V
	After	370V	0.6μA	610V	430V
Standard Deviation (+ Coefficient of Variation)	Before	±120V (±24%)	±20μA (±17%)	±190V (±25%)	155V (±29%)
	After	±45V (±13%)	±0.9μA (±100%)	±190V (±33%)	±120V (±26%)

Table 7.26 - 10 Second Anodisation of P^+-Type Silicon - Sample N

Anodisation Time / Seconds	Porous Silicon Layer Thickness / nm	Starting Voltage	Range & Standard Deviation	Reduction in Starting Voltage
0	0	505V	300V-700V (400V range) ± 120V	n/a
0.25	40	260V	160V-375V (215V range) ± 85V	49%
		320V	195V-430V (235V range) ± 70V	37%
		265V	160V-500V (340V range) ± 95V	48%
3.5	125	335V	200V-600V (400V range) ± 160V	33%
10	400	425V	260V-400V (140V range) ± 45V	28%

Note that:
1) Following anodisation, the starting voltages were reduced.
2) The values of starting voltage obtained from anodised p^+-type silicon tips were much lower than obtained from anodised p-type silicon tips.
3) Following anodisation, the range of values of starting voltage was lower.
3) The starting voltage increased slightly with anodisation time.

Table 7.27 Starting Voltages for Different Anodisation Times

ii) The reduction in starting voltage was greater than for anodised p-type samples. For samples anodised for 0.25 seconds, the starting voltage was reduced by up to 49%; whereas the greatest reduction in starting voltage for an anodised p-type sample (anodised for 10 seconds) was 37%. Absolute values of starting voltage were lower for anodised p^+-type FEAs, than for anodised p-type FEAs. For example, the lowest mean value for a p^+-type tip was 258V (0.25 second anodisation) versus 328V for a p-type tip (10 second anodisation). The lowest recorded starting voltage for an anodised p^+-type tip was 160V which is similar to the lowest value recorded for a p-type FEA (170V).

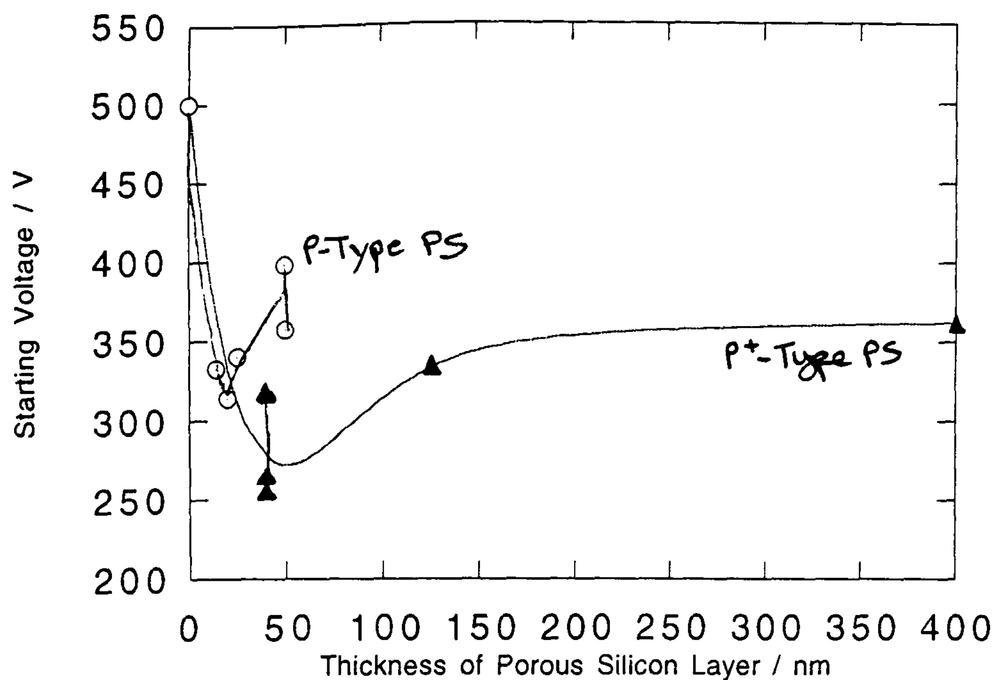
iii) The starting voltage increased with anodisation time - the starting voltage for 10 seconds anodisation was 423V, which is 60% higher than the value obtained for an anodisation time of 0.25 seconds. A similar increase in starting voltage was also observed for p-type FEAs. A plot comparing both p-type and p^+-type anodised FEAs is shown in Figure 7.15. These plots show that for both p and p^+-type PS, the starting voltage increased slightly with porous silicon thickness. However, comparing the two different materials, a p^+-type tip covered with a PS layer of 400nm had a similar starting voltage to a p-type tip covered with a PS layer of 40nm. The plot of anodisation time versus starting voltage in Figure 7.15 shows that FEAs with lower anodisation time appear to have lower starting voltages.

iv) Following anodisation, the standard deviation was lower. Also, for most samples, the range of values of starting voltage was less following anodisation. For example, for 0.25 seconds anodisation, the range of values was only 200V versus 400V prior to anodisation. The range of values for p-type FEAs were similar before and after anodisation.

b) Voltage Required to Obtain Higher Current Values and Rate of Increase of Current with Voltage

The mean voltages required to obtain current values of 0.1, 1 and 10μA were plotted versus current for all anodisation times, see Figure 7.16. These values are summarised in Table 7.28. Following anodisation, a large drop was observed in the mean voltage required to obtain 0.1, 1μA and 10μA. For example, only 400V-450V was required to obtain 10μA from a p^+-type sample (0.25 second anodisation); whereas 575V was required to obtain a similar current from a

Starting Voltage versus Porous Silicon Thickness - Comparison of P-Type and P^+-Type Porous Silicon



Starting Voltage versus Anodisation Time - Comparison of P-Type versus P^+-type Porous Silicon

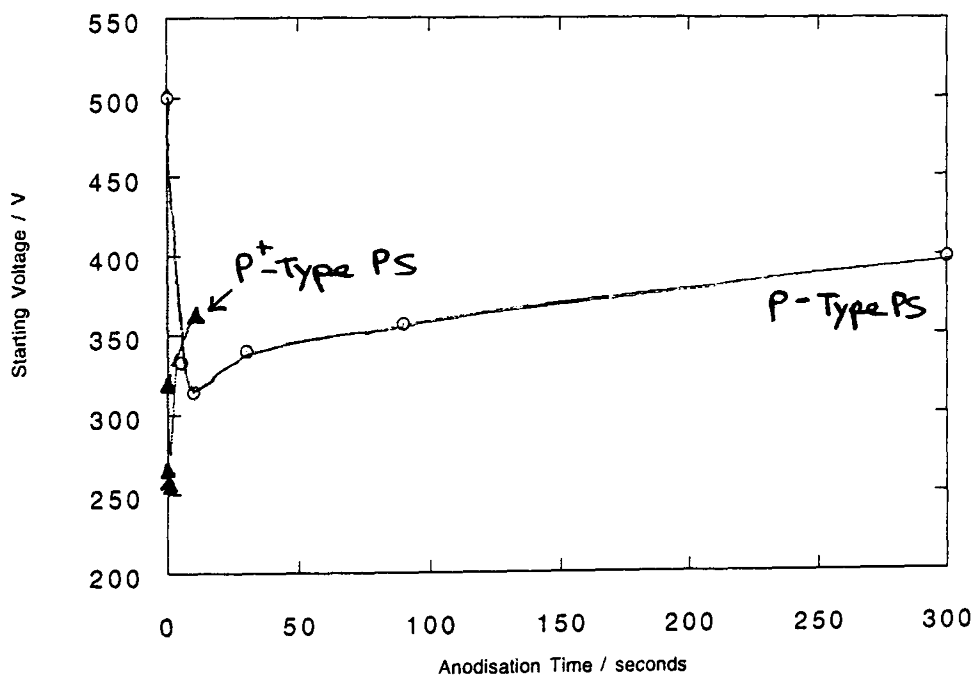


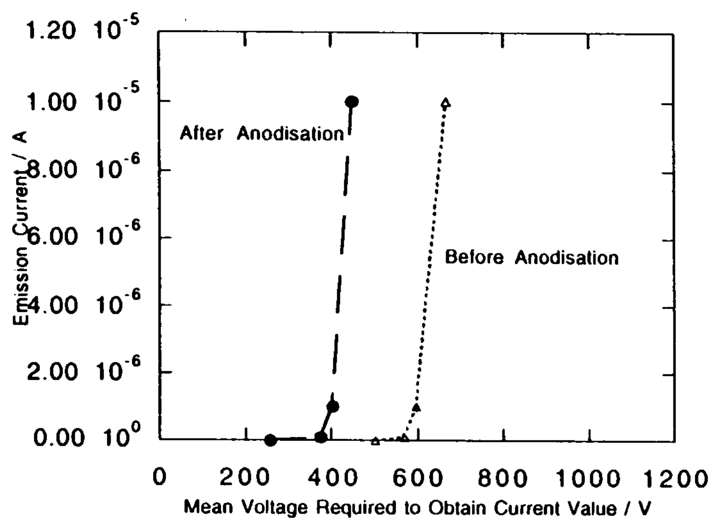
Figure 7.15 - Comparison of Starting Voltages for P-Type and P^+-Type Silicon Following Anodisation

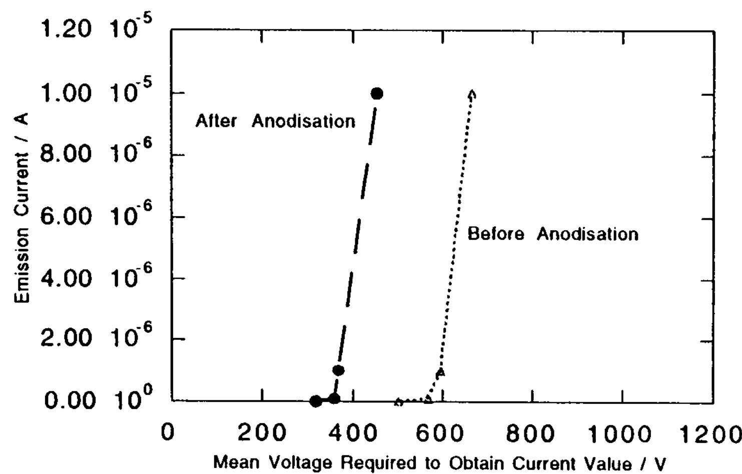
Note the following:

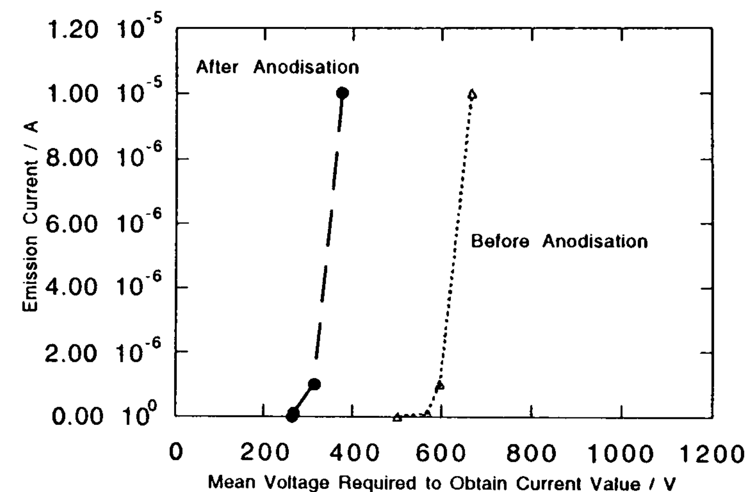
1) These plots emphasise the fact that the starting voltage obtained from p^+-type porous silicon were lower than from p-type porous silicon.

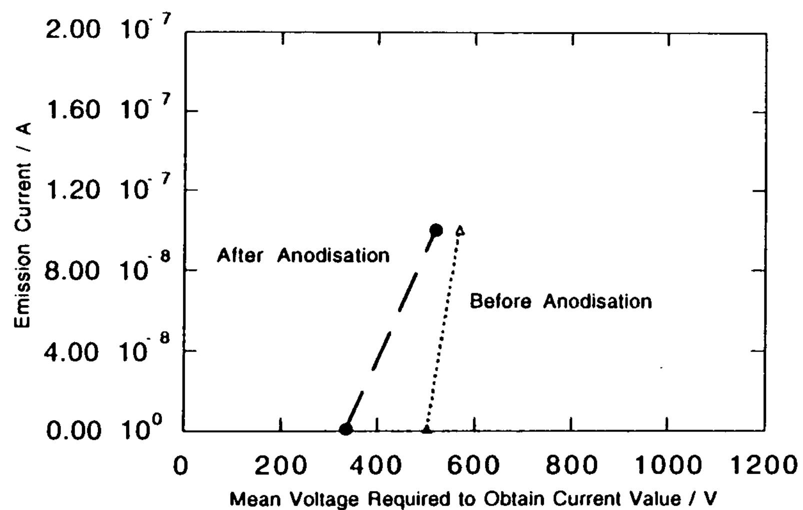
2) For both p-type and p^+-type porous silicon, there is some increase in starting voltage as the thickness of the layer increased. However, anodised p^+-type emitters with thick PS layers (400nm) still had much lower starting voltages than p-type emitters with much thinner PS layers (40nm).

3) The plot of starting voltage versus anodisation time suggests that FEAs anodised for the shortest anodisation times (p+-type PS) had the lowest starting voltages. This could suggest that the etch affected the emitting sites if the sample was left in the etch for too long.









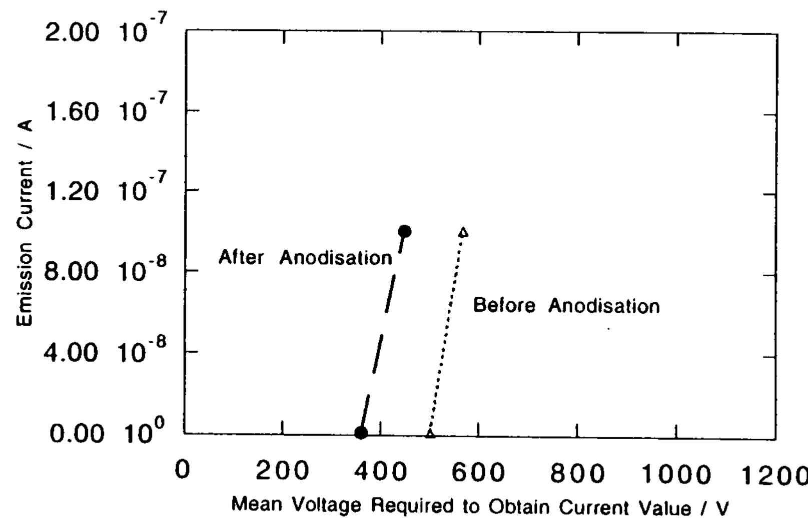
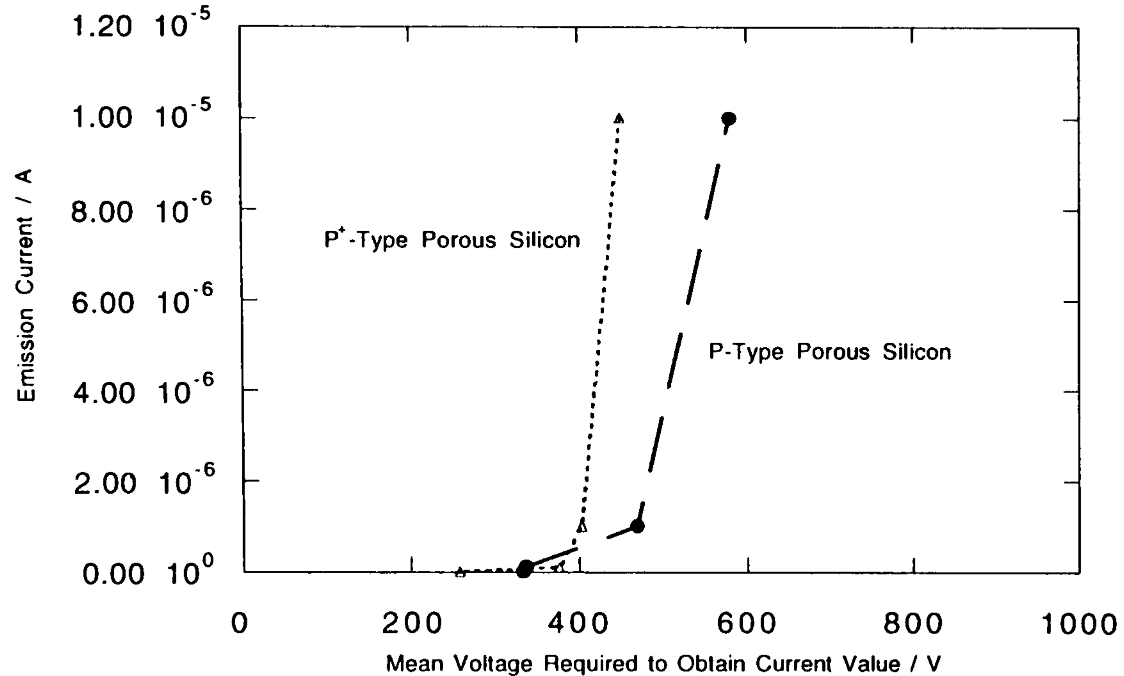


Figure 7.16a - Mean Voltage Required to Obtain Certain Current Values - P+-Type Silicon



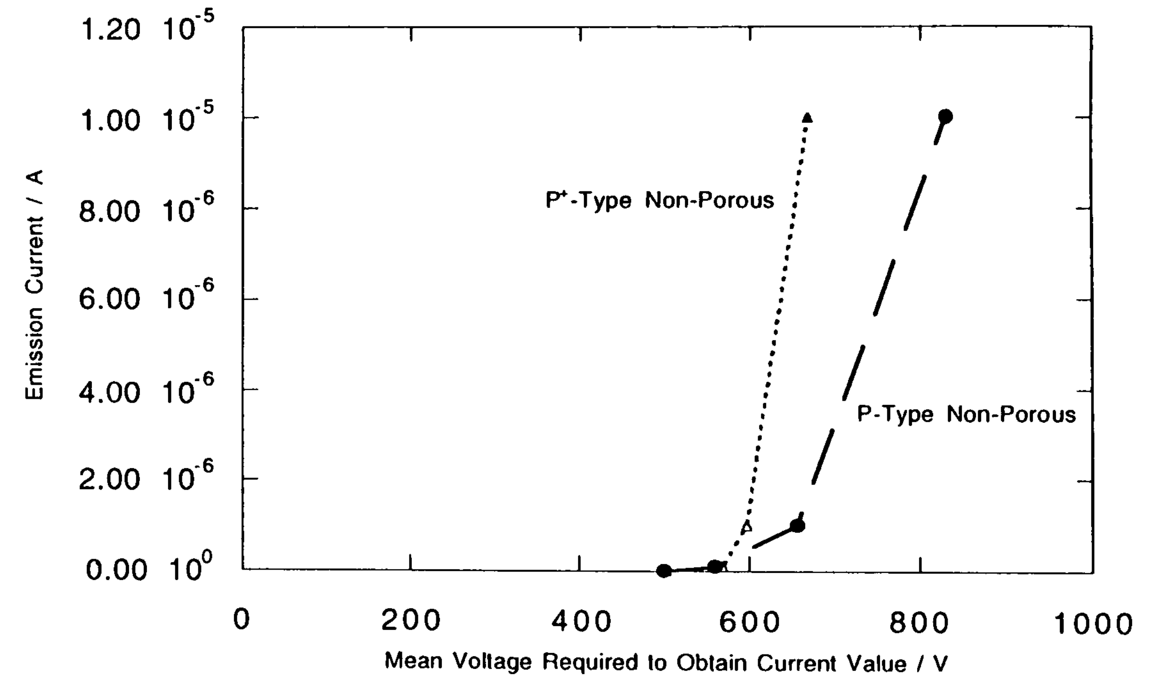


Figure 7.16b - Comparison of Mean Voltage Required to Obtain Certain Current Values - Anodised P-Type Silicon versus Anodised P+-Type Silicon and Non-Anodised P-Type Silicon versus Non-Anodised P+-Type Silicon

These plots show that for p^+-type porous silicon, current rose faster with voltage than for p-type porous silicon (this was also the case when comparing these samples prior to anodisation).

Anodisation Time / Seconds	Porous Silicon Layer Thickness / nm	Voltage Required to Obtain 0.1μA + % Reduction	Voltage Required to Obtain 1μA + % Reduction	Voltage Required to Obtain 10μA + % Reduction
0.25	40	375V (33% drop)	405V (23% drop)	450V (18% drop)
		360V (27% drop)	370V (38% drop)	455V (32% drop)
		270V (43% drop)	315V (48% drop)	375V (44% drop)
3.5	125	520V (9% drop)	n/a	n/a
10	400	450V (21% drop)	n/a	n/a

n/a - the emitter blew before this current level was reached

Table 7.28 Reduction in Voltage Required to Obtain Given Current Values

Anodisation Time	Mean Value of dI/dV for currents in range 0.1μA-1μA	Mean Value of dI/dV for currents in range 1μA-10μA
0	0.03 μA/V	0.1 μA/V
0.25	0.02 μA/V	0.7 μA/V
	0.04 μA/V	1.5 μA/V
	0.04 μA/V	2 μA/V
3.5	0.003 μA/V	0.005 μA/V
10	0.001 μA/V	0.007 μA/V

Note that:
1) In the higher current range, dI/dV was much greater following anodisation.
2) In the higher current range, dI/dV was much greater for anodised p^+-type silicon tips than for anodised p-type silicon tips.
3) dI/dV decreased with increasing anodisation time.

Table 7.29 Rate of Increase of Current with Voltage

p-type sample (5 second anodisation). A plot comparing p-type and p^+-type anodised FEAs is also shown in Figure 7.16.

In addition, the rate of increase of current with voltage (dI/dV) was calculated before and after anodisation. The results are summarised in Table 7.29. dI/dV for anodised p^+-type silicon was greater than for non-anodised p^+-type silicon. For some tips, the value was as high as 1.5μA/V. The highest value for p-type silicon tips was 0.1μA/V. However, the rate of increase decreased substantially as the anodisation time was increased. For 3.5 and 10 second anodisation times, dI/dV was much lower than for the non-anodised samples.

c) Nature of Fowler-Nordheim Plots

i) Typical three-stage emission, as observed for most p-type silicon tips, was rarely observed for p^+-type silicon tips, either before or after anodisation. When three-stage emission was observed, the length of the Stage II plateau was very short, being <50V on average. This is much smaller than the values observed for p-type FEAs.

ii) The plots obtained from p^+-type FEAs (both before and after anodisation) were more noisy than for p-type tips (either before or after anodisation).

d) Maximum Emission Current Prior to Destruction

Distributions of maximum current for each anodisation time are shown in Figure 7.17. Table 7.30 summarises the current values obtained for each anodisation time. Figure 7.18 shows maximum current plotted versus both anodisation time and versus PS layer thickness. The percentage of tips blowing at current levels <5μA is summarised in Table 7.31. The percentage of tips blowing at current levels <5μA was also plotted versus both anodisation time and PS layer thickness, see Figure 7.19. The main results are summarised below:

i) After anodisation, the maximum emission current was approximately halved for a 0.25 second anodisation. This is different to p-type FEAs, where the emission current increased by up to 3.5 times following anodisation, although it is possible that if a shorter anodisation time had been used, a similar result to p-type silicon would have been obtained.

Anodisation Time / Seconds	Porous Silicon Layer Thickness / nm	Mean Maximum Current	Current (after anodisation)/ current (before anodisation)
0	0	17µA	n/a
0.25 (shows results from 3 different specimens)	40	7.5µA 5µA 62µA	0.5 0.3 3.6
3.5	125	0.1µA	0.006
10	400	0.6µA	0.03

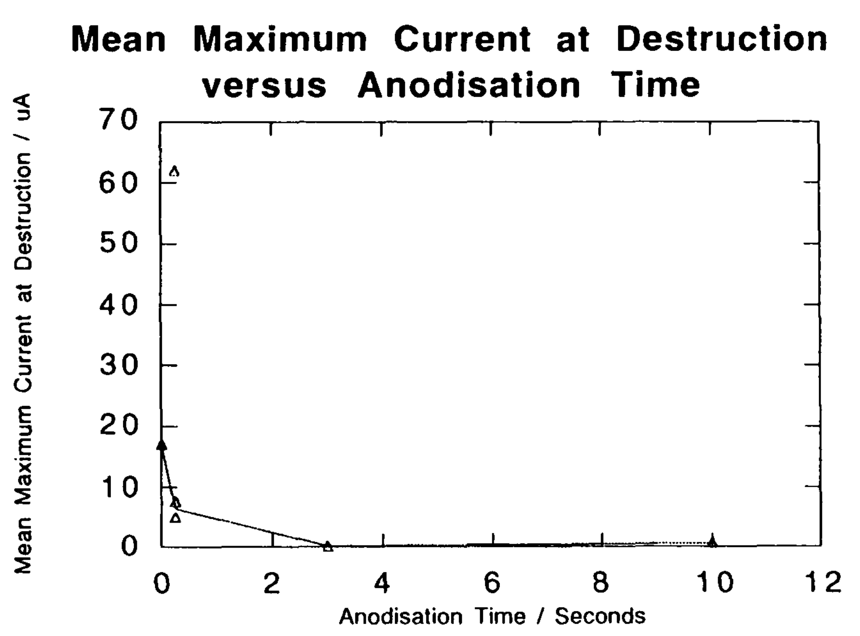
(Median values used instead of mean values due to large deviations in the values)

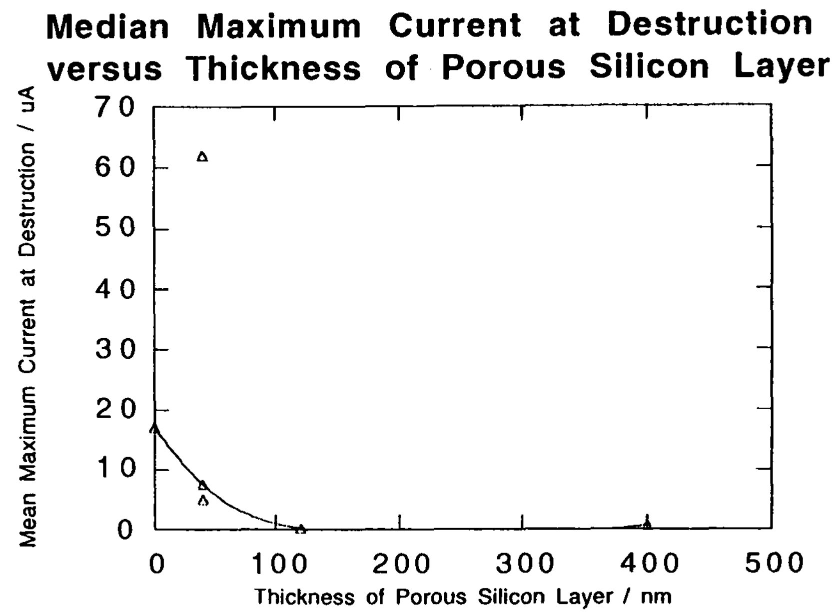
Note that:
1) Following anodisation, the maximum emission current dropped.
2) The maximum emission current decreased drastically as the anodisation time increased.

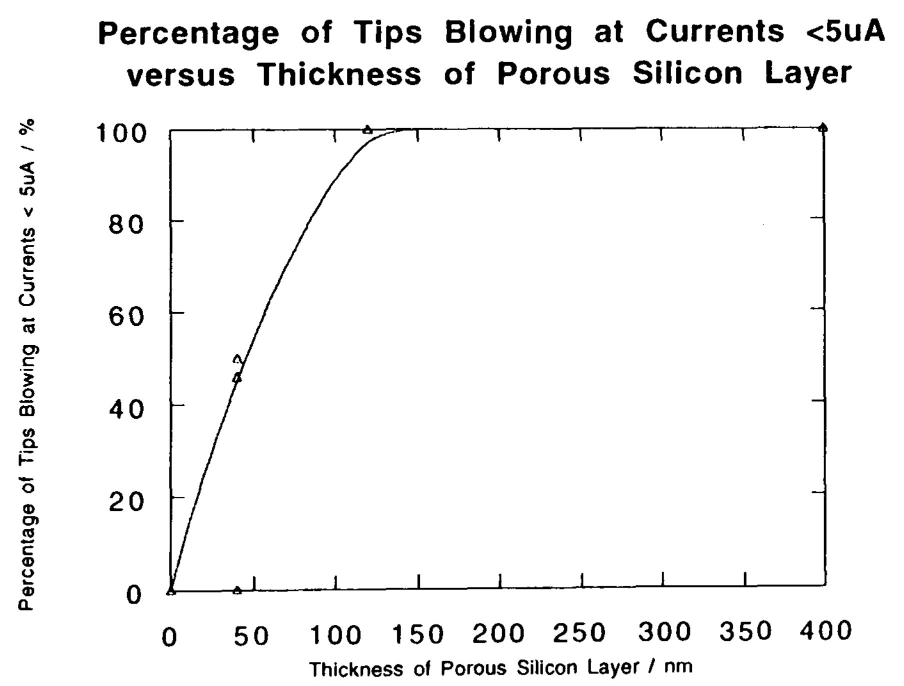
Table 7.30 Maximum Emission Currents for Each Anodisation Time

Anodisation Time / Seconds	Thickness of Porous Silicon Layer / nm	% Tips blowing <5µA
0	0	0%
0.25 (shows results from 3 different specimens)	40	46% 50% 0%
3.5	125	100%
10	400	100%

Table 7.31 Percentage of Tips Blowing at Currents <5µA







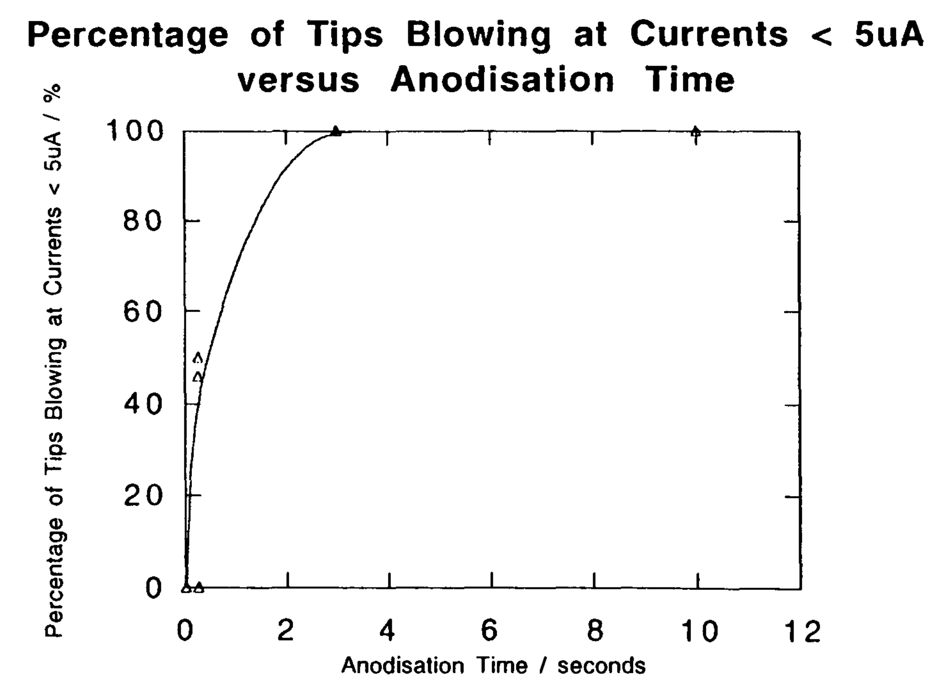
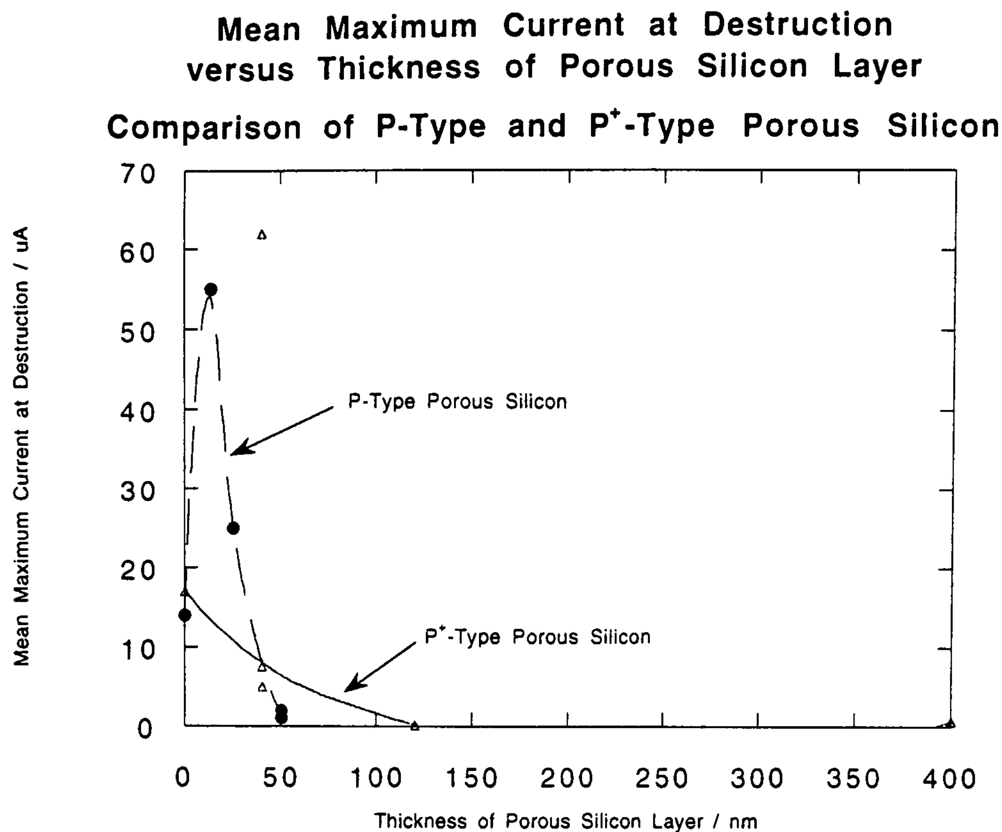


Figure 7.18 - Mean Maximum Emission Current and Percentage Tips versus Anodisation Time and versus Thickness of Porous Silicon Layer - P^+-Type Silicon



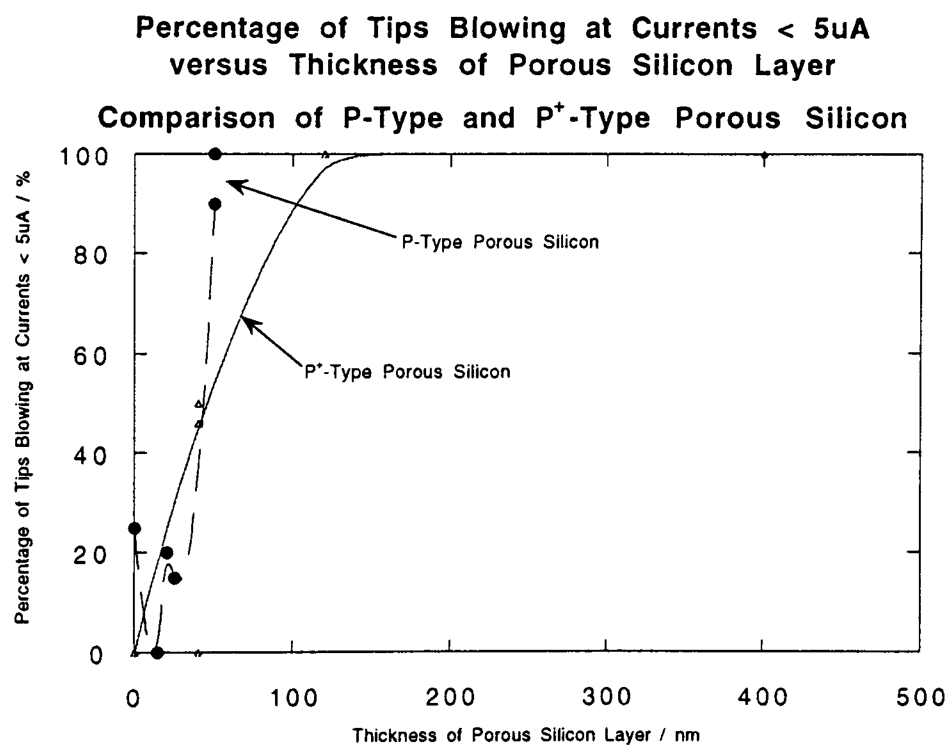


Figure 7.19 - Mean Maximum Emission Current and Percentage Tips Blowing at Currents <5μA - Comparison of P-Type and P+-Type Porous Silicon

Note the following:

1) These plots show that for p-type porous silicon, there was an increase in maximum emission current following anodisation. However, this did not occur for p+-type porous silicon.

2) These plots show that for both p-type and p+-type porous silicon, the maximum emission current decreased with the thickness of the porous silicon layer.

3) These plots also show that at the point where the data from p-type and p+-type porous silicon, both materials would have the same mean maximum emission current.

ii) As for anodised p-type FEAs, the maximum current decreased as the anodisation time and hence the thickness of the PS layer increased. As for p-type FEAs, the percentage of tips blowing <5μA increased drastically as the anodisation time increased.

iii) Comparing like with like (i.e. a 40nm layer of p-type PS to a 40nm layer of p^+-type PS), the mean current obtained from the p^+-type FEA was similar (looking at the point where the two plots meet) to the mean current obtained from the p-type FEA.

e) Slope and Intercept of the Fowler-Nordheim Plot and Calculations of Field Enhancement Factor, Emission Area and Emitting Tip Radii

i) Slope and Intercept

Distributions of the FN slope and intercept obtained before and after anodisation are shown in Figure 7.20 and are summarised in Table 7.32. Figure 7.21 shows both plotted versus anodisation time. The main points are summarised below:

i) For all anodisation times, the values of slope were less than for non-anodised silicon. All values for anodised FEAs were $< |-10{,}000|$, whereas values for non-anodised silicon were up to -40,000.

ii) The values of anodised p^+-type FEAs were greater than for anodised p-type FEAs, implying that the emitting sites were blunter.

iii) For all anodisation times, the mean intercept was much lower than for non-anodised silicon, also implying that the emitting sites were blunter.

ii) Calculation of Field Enhancement Factor

The values of field enhancement have been calculated in the same way as for p-type FEAs. Results are summarised in Table 7.33. Distributions of the calculated field enhancement factor are shown in Figure 7.22. The main results are outlined below:

i) The field enhancement factors were between 1.9 and 3.5 times higher following anodisation.

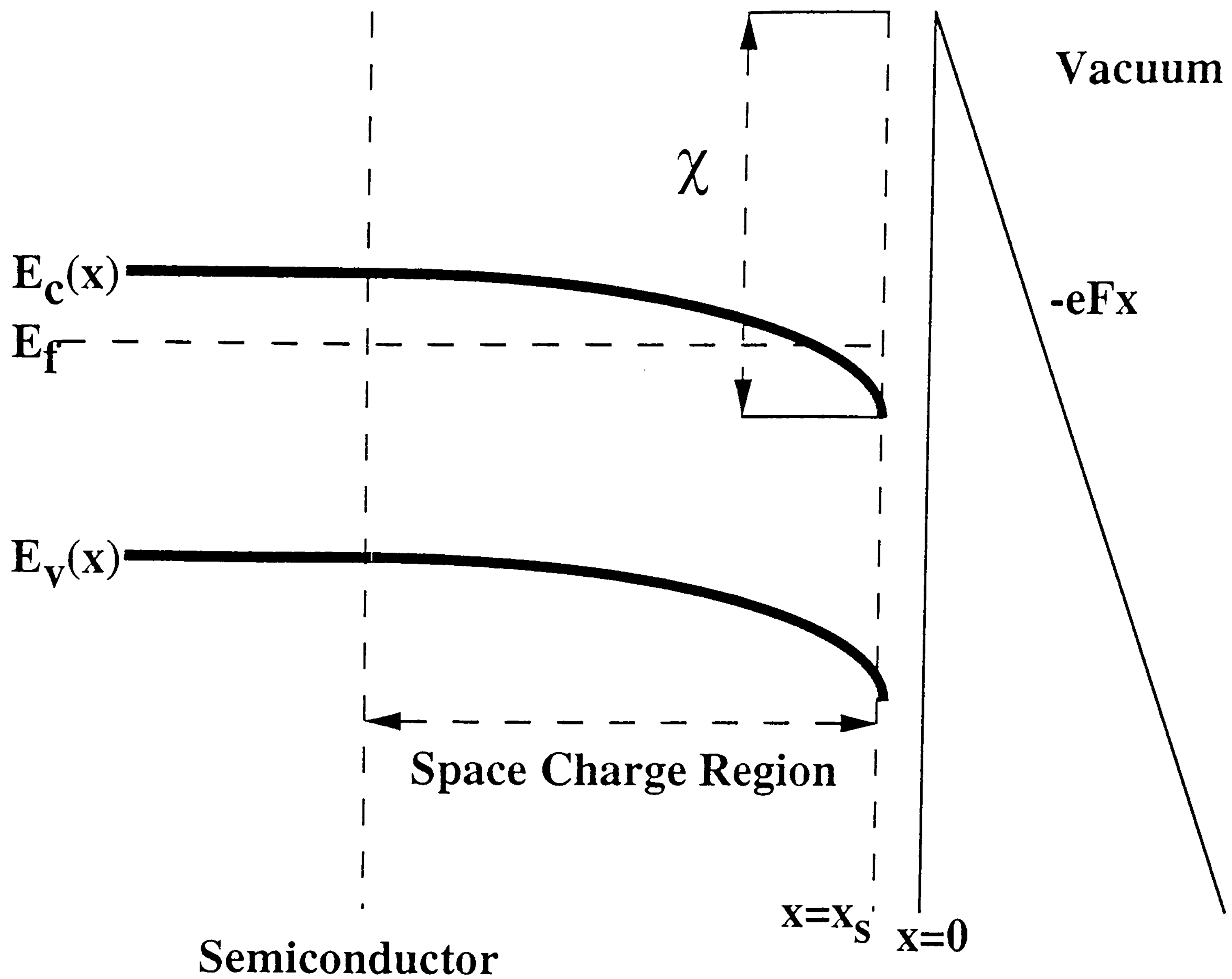


Figure 2.2 - Surface Potential Barrier at an N-Type Semiconductor Surface
Band bending must occur in order for emission to occur. When a field is applied, the bottom of the conduction band will dip below the Fermi level. A pool of electrons collects in this depression, from which emission can occur.

Ef = Fermi level; χ = electron affinity of the semiconductor; F = applied electric field
$E_C(x)$ = energy at bottom of conduction band; $E_V(x)$ = energy at top of valence band

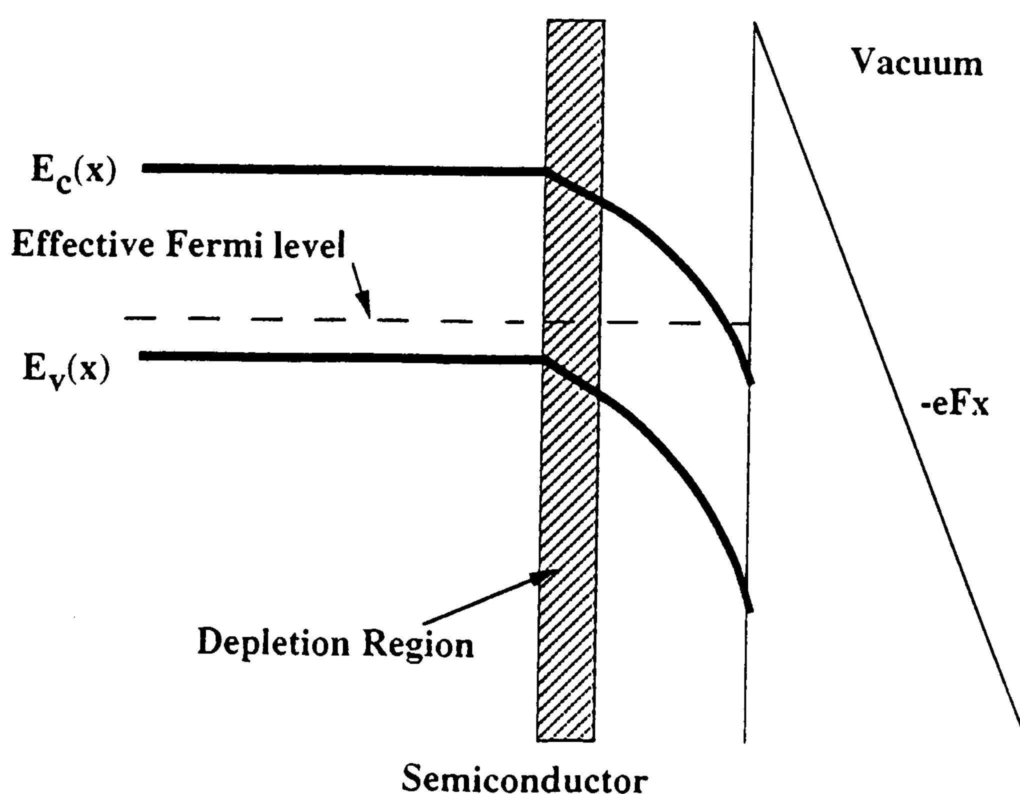


Figure 2.3 - Depletion Region Formation near P-Type Semiconductor Surface
Band bending is greater for a p-type semiconductor. In additon, a depletion region (depleted of both holes and electrons) forms next to the surface pool of electrons.

Anodisation Time / Seconds	FN Slope	FN Slope (Before Anodisation) / FN Slope (After Anodisation)	F-N Intercept After Anodisation
0	-13935	n/a	-3.9
0.25	-4795 -4415 -7400	2.9 3.2 1.9	-17.6 -13.4 -11.5

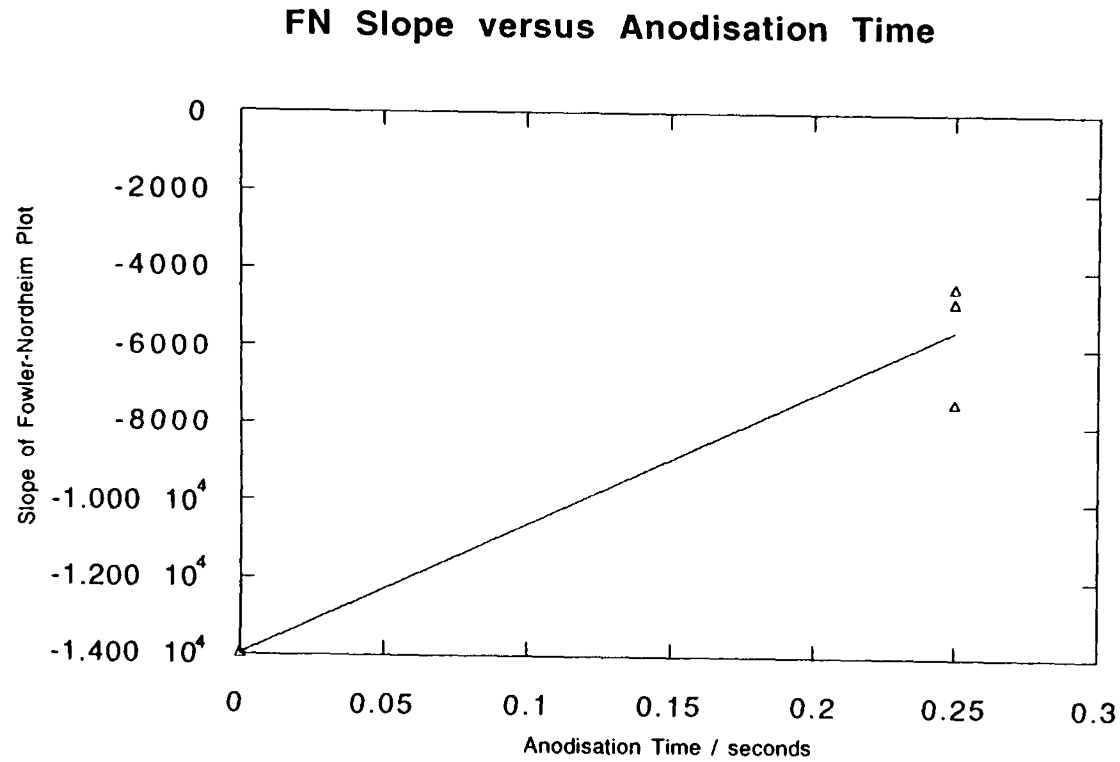
Values for samples anodised for 3.5 and 10 seconds were not included, as the FN plots were too noisy to take estimates of the slope and intercept.

Note that:

1) Following anodisation, the FN slope was much lower in value - a similar result as for anodised p-type silicon tips.

2) Following anodisation, the FN intercept was more negative - a similar result as found for anodised p-type silicon tips.

Table 7.32 FN Slope and Intercept Before and After Anodisation (for Different Anodisation Times)



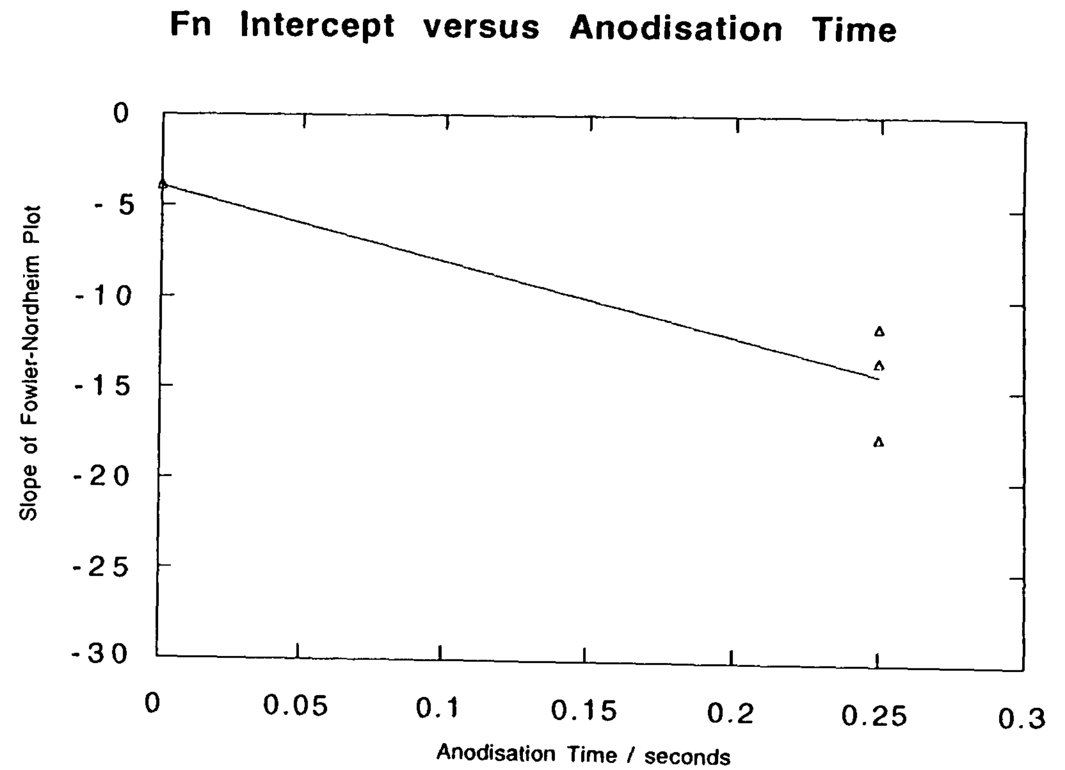


Figure 7.21 - Fowler-Nordheim Slope and Fowler-Nordheim Intercept plotted versus Anodisation Time - P+-Type Silicon

a) 0.25 Second Anodisation - Sample I

Value	Sample	Field Enhancement Factor (β)	Emission Area (α) / cm^2	Tip Radius (r) calculated from α / cm	Tip Radius (r) calculated from β / cm
Mean	a) Before	8.4×10^{4}	3.7×10^{-7}	1.3×10^{-4}	7.5×10^{-6}
	b) After	2.6×10^{5}	4.8×10^{-12}	7.2×10^{-7}	2.6×10^{-6}
Range	a) Before	$2.1 \times 10^{4} - 2.6 \times 10^{5}$	$1.8 \times 10^{-16} - 3.6 \times 10^{-6}$	$7.5 \times 10^{-9} - 1 \times 10^{-3}$	$1.3 \times 10^{-6} - 1.6 \times 10^{-5}$
	b) After	$4.2 \times 10^{4} - 9.6 \times 10^{5}$	$2.6 \times 10^{-18} - 3.3 \times 10^{-11}$	$9.2 \times 10^{-10} - 3.2 \times 10^{-6}$	$3.5 \times 10^{-7} - 7.9 \times 10^{-6}$
Median	a) Before	4.8×10^{4}	6.9×10^{-12}	1.1×10^{-6}	6.9×10^{-6}
	b) After	1.7×10^{5}	3.5×10^{-14}	1×10^{-7}	1.9×10^{-6}
Standard Deviation	a) Before	$\pm 7.8 \times 10^{4}$ ($\pm 93\%$)	$\pm 1.1 \times 10^{-6}$ ($\pm 297\%$)	$\pm 3.3 \times 10^{-4}$ ($\pm 254\%$)	$\pm 4.9 \times 10^{-6}$ ($\pm 65\%$)
	b) After	$\pm 2.6 \times 10^{5}$ ($\pm 100\%$)	$\pm 1.1 \times 10^{-11}$ ($\pm 229\%$)	$\pm 1 \times 10^{-6}$ ($\pm 139\%$)	$\pm 2 \times 10^{-6}$ ($\pm 77\%$)

b) 0.25 Second Anodisation - Sample J

Value	Sample	Field Enhancement Factor (β)	Emission Area (α) / cm^2	Tip Radius (r) calculated from α / cm	Tip Radius (r) calculated from β / cm
Mean	a) Before	8.4×10^{4}	3.7×10^{-7}	1.3×10^{-4}	7.5×10^{-6}
	b) After	2×10^{5}	4.2×10^{-8}	6.5×10^{-5}	2.3×10^{-6}
Range	a) Before	$2.1 \times 10^{4} - 2.6 \times 10^{5}$	$1.8 \times 10^{-16} - 3.6 \times 10^{-6}$	$7.5 \times 10^{-9} - 1 \times 10^{-3}$	$1.3 \times 10^{-6} - 1.6 \times 10^{-5}$
	b) After	$7.3 \times 10^{4} - 6.7 \times 10^{5}$	$3.3 \times 10^{-19} - 2 \times 10^{-7}$	$3.2 \times 10^{-10} - 2.5 \times 10^{-4}$	$5 \times 10^{-7} - 4.5 \times 10^{-6}$
Median	a) Before	4.8×10^{4}	6.9×10^{-12}	1.1×10^{-6}	6.9×10^{-6}
	b) After	1.2×10^{5}	9.5×10^{-11}	5.5×10^{-6}	2.7×10^{-6}
Standard Deviation	a) Before	$\pm 7.8 \times 10^{4}$ ($\pm 93\%$)	$\pm 1.1 \times 10^{-6}$ ($\pm 297\%$)	$\pm 3.3 \times 10^{-4}$ ($\pm 254\%$)	$\pm 4.9 \times 10^{-6}$ ($\pm 65\%$)
	b) After	$\pm 1.7 \times 10^{5}$ ($\pm 85\%$)	$\pm 7.5 \times 10^{-8}$ ($\pm 179\%$)	$\pm 9.9 \times 10^{-5}$ ($\pm 152\%$)	$\pm 1.2 \times 10^{-6}$ ($\pm 52\%$)

Table 7.33 Field Enhancement Factor, Emission Area and Tip Radii Calculated for P^{+}-Type Silicon (continued overleaf)

c) 0.25 Second Anodisation - Sample K

Value	Sample	Field Enhancement Factor (β)	Emission Area (α) / cm^2	Tip Radius (r) calculated from α / cm	Tip Radius (r) calculated from β / cm
Mean	a) Before b) After	8.4×10^{4} 1.9×10^{5}	3.7×10^{-7} 3.8×10^{-7}	1.3×10^{-4} 1.7×10^{-4}	7.5×10^{-6} 4×10^{-6}
Range	a) Before b) After	$2.1 \times 10^{4} - 2.6 \times 10^{5}$ $3.6 \times 10^{4} - 8.8 \times 10^{5}$	$1.8 \times 10^{-16} - 3.6 \times 10^{-6}$ $1.3 \times 10^{-18} - 2.3 \times 10^{-6}$	$7.5 \times 10^{-9} - 1 \times 10^{-3}$ $6.4 \times 10^{-10} - 8.5 \times 10^{-4}$	$1.3 \times 10^{-6} - 1.6 \times 10^{-5}$ $3.7 \times 10^{-7} - 9.3 \times 10^{-6}$
Median	a) Before b) After	4.8×10^{4} 9.3×10^{4}	6.9×10^{-12} 1.5×10^{-9}	1.1×10^{-6} 1.8×10^{-5}	6.9×10^{-6} 3.6×10^{-6}
Standard Deviation	a) Before b) After	$\pm 7.8 \times 10^{4}$ ($\pm$93%) $\pm 2.5 \times 10^{5}$ ($\pm$132%)	$\pm 1.1 \times 10^{-6}$ ($\pm$297%) $\pm 9.2 \times 10^{-7}$ ($\pm$242%)	$\pm 3.3 \times 10^{-4}$ ($\pm$254%) $\pm 3.3 \times 10^{-4}$ ($\pm$194%)	$\pm 4.9 \times 10^{-6}$ ($\pm$65%) $\pm 2.7 \times 10^{-6}$ ($\pm$67%)

Anodisation Time / Seconds	Ratio of Mean Field Enhancement Factors Before and After Anodisation $\beta_{after\ anodisation} / \beta_{before\ anodisation}$
0.25	3.5 2.5 1.9

Note that:

1) Following anodisation, significant field enhancement occurred - the values were similar to anodised p-type tips.
2) Following anodisation, the radius of the emitting area was smaller. This value was larger than for anodised p-type tips.
3) More reliable values of tip radius were obtained by calculating from β, rather than from the emission area α.

Table 7.33 Field Enhancement Factor, Emission Area and Tip Radii Calculated for P^+ Type Silicon (continued from previous page)

ii) The field enhancement following anodisation was slightly less than for p-type FEAs which were between 2 and 5 times higher following anodisation. Figure 7.23 shows plots of enhancement versus anodisation time. A a comparison of field enhancement factor for both p and p^+-type FEAs plotted versus anodisation time is shown in Figure 7.25a.

iii) Calculation of Tip Radius

As for p-type FEAs, the radius was calculated from both α and β. Results are also summarised in Table 7.33. Distributions of the calculated tip radius are shown in Figure 7.24. Results are as follows:

i) Following anodisation, the radius (calculated from β) was ~2-3 times smaller than the case prior to anodisation. As for p-type FEAs, the difference before and after anodisation was greater if the values of radius (calculated from α) were compared instead of the values calculate from β.

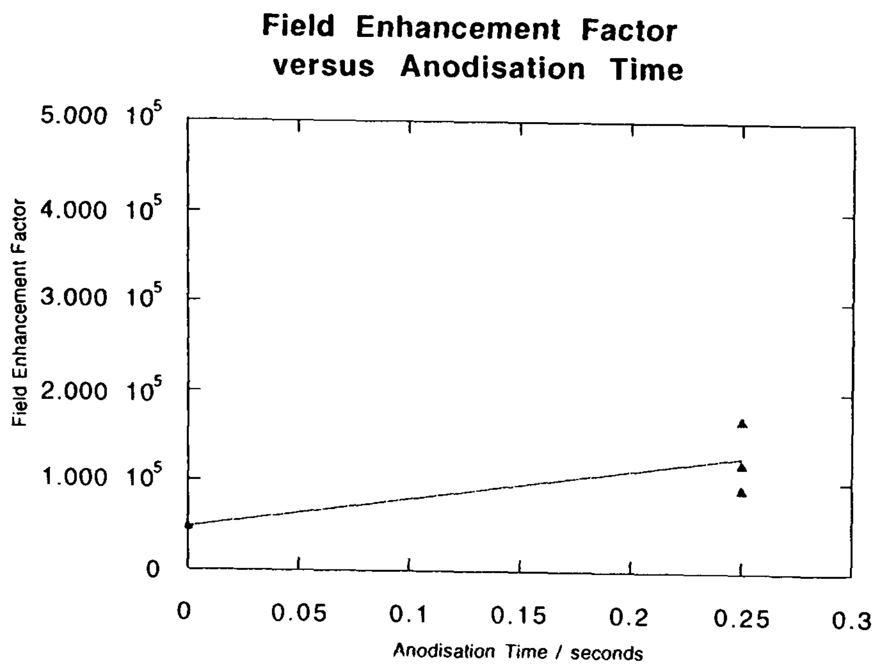
ii) Figure 7.25b shows a comparison of the radius (both methods) for p and p^+-type FEAs versus anodisation time. Comparing the values calculated from β, the values for p^+-type FEAs are slightly greater than for p-type FEAs. The values calculated from α show that the values for p^+-type FEAs were much greater than for p-type FEAs, by up to 4 orders of magnitude. This implies that emission from anodised p^+-type FEAs occurred from sites having much greater radius than for p-type FEAs.

f) Comparison Before and After Anodisation - Specific Examples

FN and IV plots plots obtained from individual anodised emitters are shown in Figure 7.26. Key data from each tip is summarised in Table 7.34.

7.3 Thermal Oxidation of Anodised FEAs and Removal of the PS Layer

Yue *et al.* (1990) reported obtaining emission from flat PS layers, both before and after oxidation. They claimed that in both cases, extremely sharp tips were formed at the PS/bulk silicon interface, which allowed electrons to be collected at very low voltages when an electric field was applied, see Chapter 2. Apparently, this caused oxidation of the PS layer only, not the



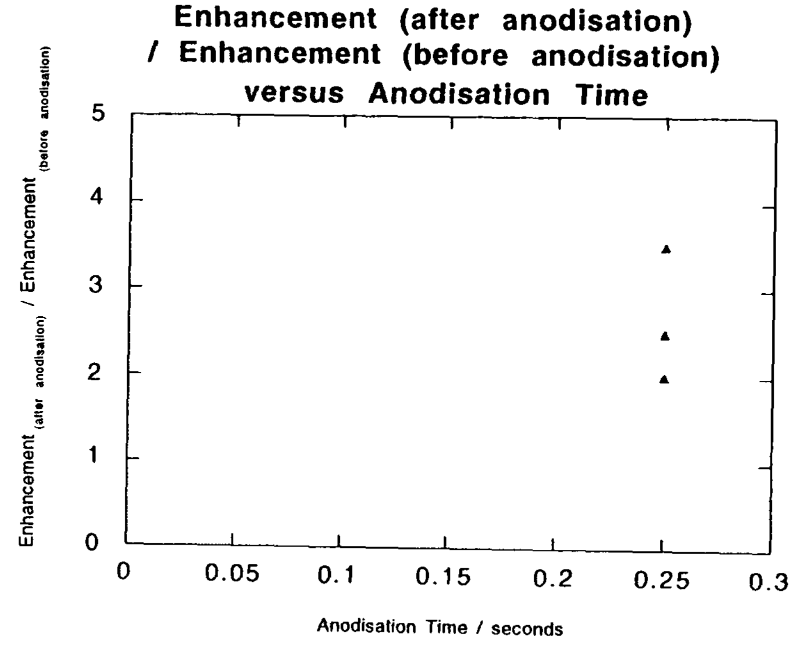


Figure 7.23 - Field Enhancement Factor versus Anodisation Time - P+-Type Silicon

Figure 7.25a

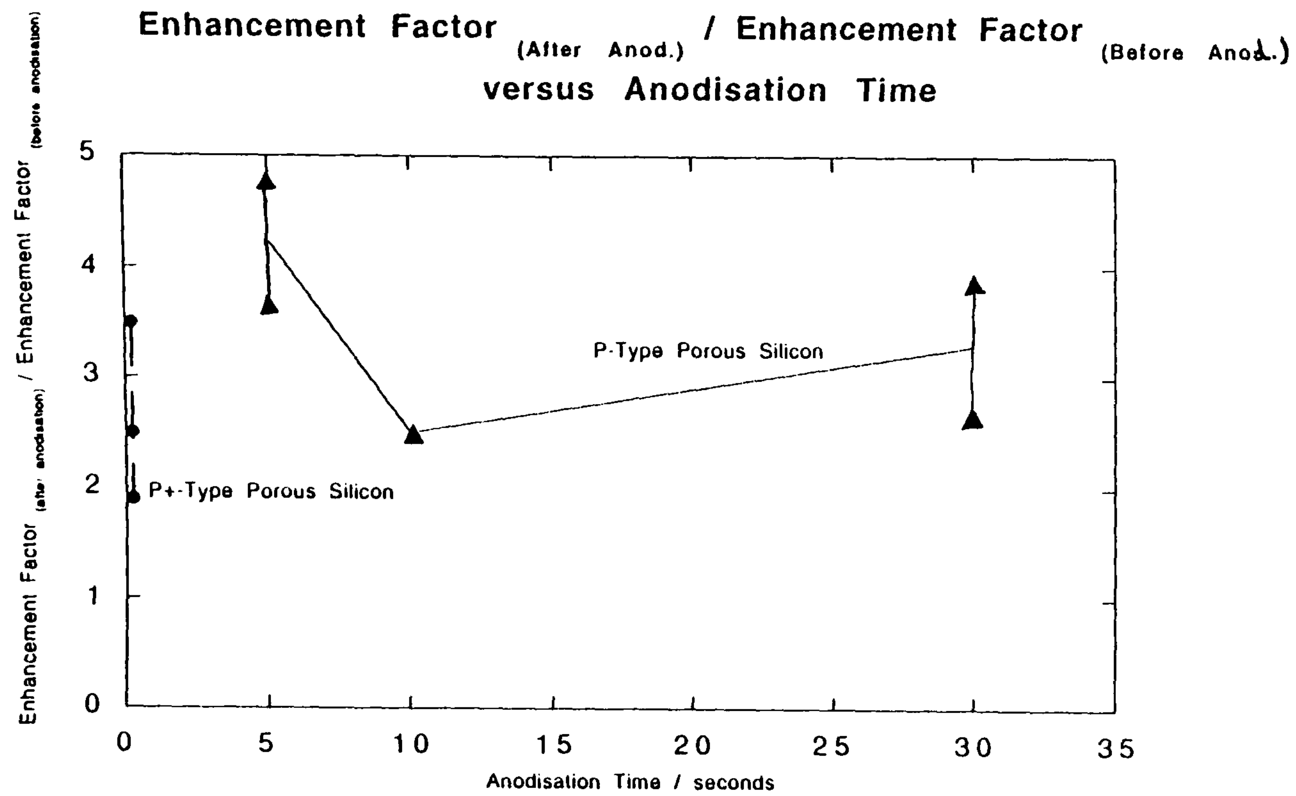


Figure 7.25b

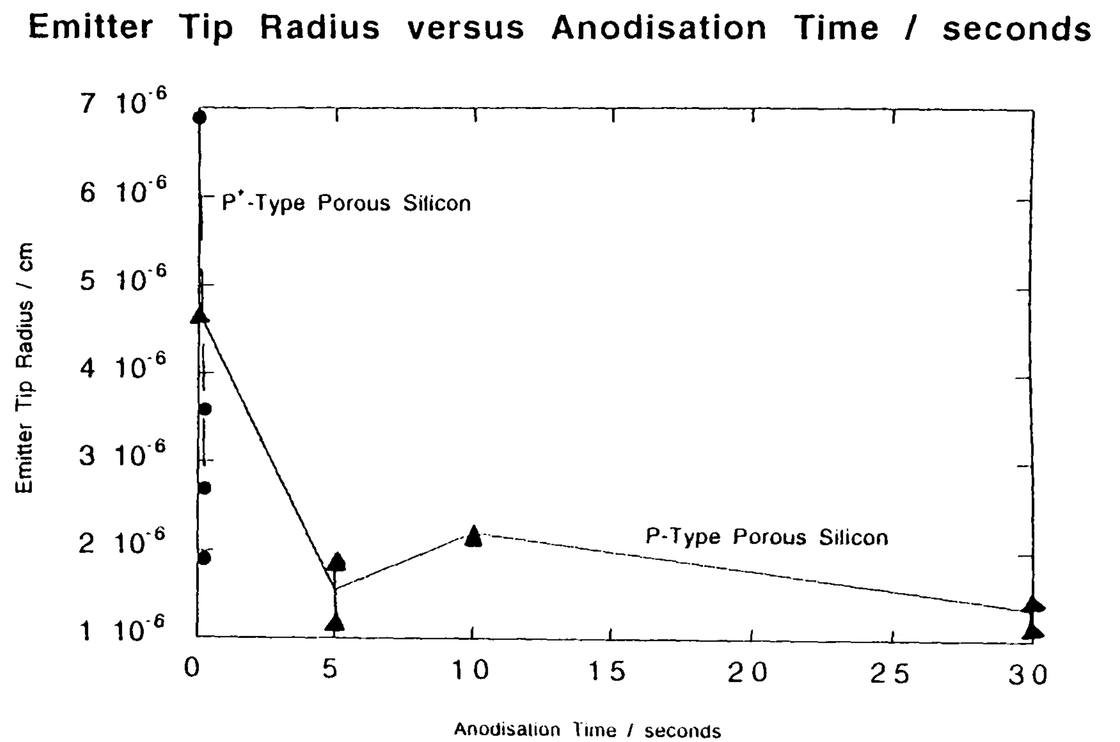


Figure 7.25 - Comparison of P-Type and P+-Type Anodised Silicon - Field Enhancement Factor and Tip Radius (Calculated from Enhancement Factor)

Note the following:

1) These plots indicate that field enhancement (over non-anodised state) were similar for p-type and p+-type porous silicon, although for the shortest anodisation time, p-type porous silicon exhibited slightly higher field enhancement.

2) These plots also indicate that the emitting tip radius for p-type porous silicon was smaller than for p^+-type porous silicon. If emission had occurred from the surface fibrils, this would be consistent with the fact that p-type fibrils were shown to be smaller than p^+-type fibrils (TEM studies in Chapter 6).

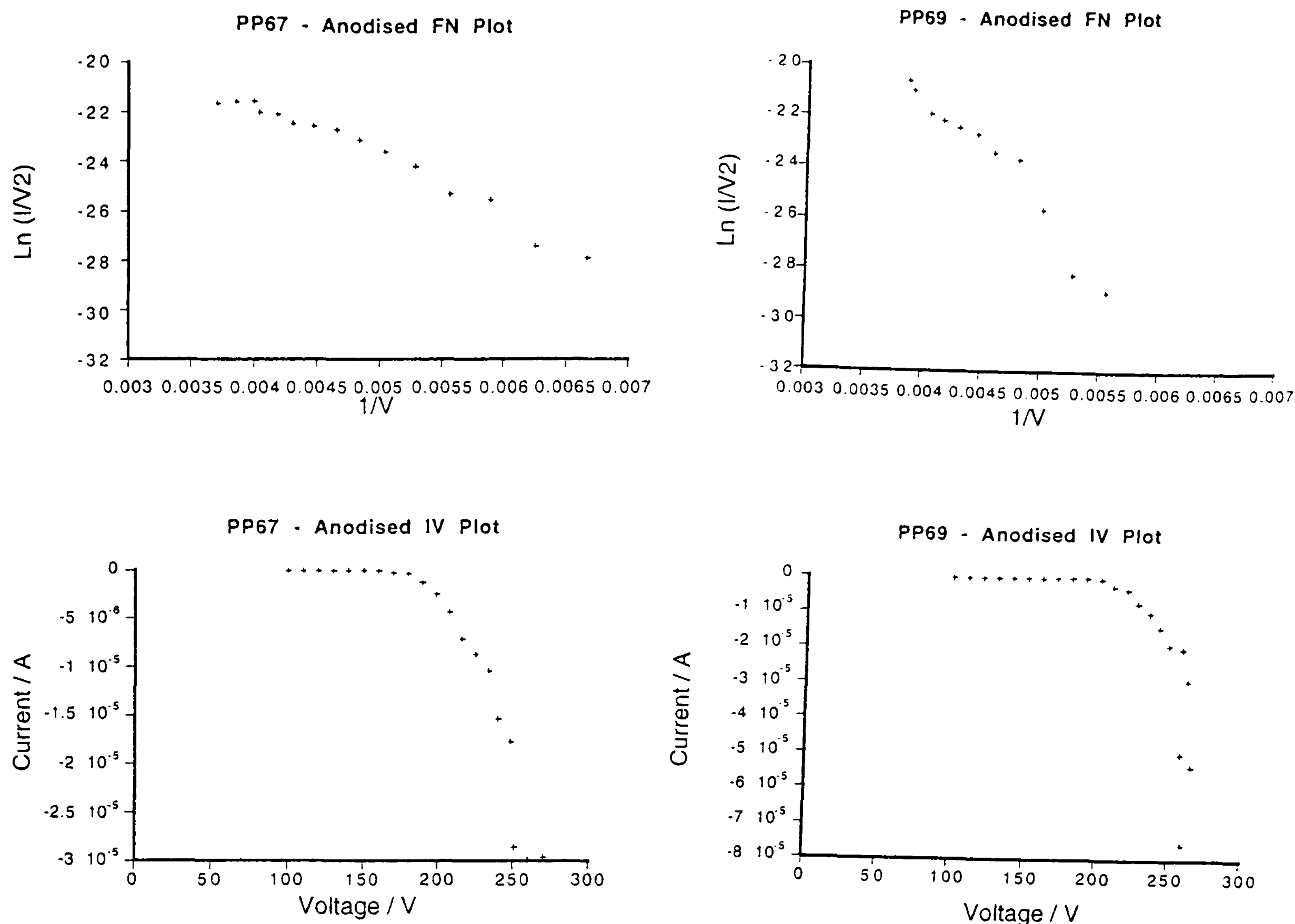


Figure 7.26 - Examples of Fowler-Nordheim and Current-Voltage plots Collected from P^+-type FEAs Anodised for 0.25 Seconds Showing Results from 2 Tips with Lowest Starting Voltages

Sample	pp67	pp69
Starting Voltage	160V	190V
Maximum Current	30 µA	75 µA
Maximum Voltage	250V	250V
F-N Slope	-7399	-6764
F-N Intercept	-1.2	8.2

Both tips show emission starting at very low voltages. High maximum currents were also obtained at very low voltages. Comparing these I-V plots to those obtained from p-type silicon emitters, the plots are much steeper. Comparing PP69 with the anodised p-type tip EX33 in Figure 7.12, both tips have the same starting voltage of 200V, but the p^+-type tip reached 20µA at 250V, whereas the p-type tip produced 20µA at 480V (i.e.at much higher voltage).

Table 7.34 - Summary Tables for Comparison Plots of Anodised Samples versus Non-Anodised Samples (continued overleaf)

underlying bulk silicon. They also claimed that oxidation sharpened these points, allowing emission to occur at even lower voltage.

In the present work, two experiments were carried out in order to investigate whether this bulk/PS interface was the true source of field emission for anodised emitters. Firstly, the effect of oxidation on anodised FEAs was investigated. Secondly, removal of the PS layer from anodised FEAs was investigated. (In both cases, there was only sufficient time available to study p-type FEAs.)

7.3.1 Thermal Oxidation of Anodised FEAs

Oxidation was carried out in order to investigate whether the same results were obtained as for Yue *et al.* (1990). If emission had improved following oxidation, this would have indicated that emission occurred at the bulk/PS interface. Anodised samples were oxidised in a furnace held at 950°C. Two different oxidation times were investigated - 1 minute and 20 minutes. Prior to oxidation, all samples had originally been anodised for 30 seconds. The field emission properties of oxidised anodised samples were compared to those of freshly anodised samples. The results obtained are summarised in Table 7.35. The main points are outlined below:

a) Starting Voltage

Distributions of starting voltage are shown in Figure 7.27. For a 1 minute oxidation, the mean starting voltage was 1070V which is nearly 3 times the value observed for a freshly anodised sample. For a 20 minute oxidation, the mean starting voltage was even higher, being ~1720V. These results are completely different to those obtained by Yue *et al.* (1990), where a lower starting voltage was observed following oxidation. Figure 7.28 shows starting voltage plotted versus oxidation time.

b) Maximum Emission Current

Distributions of emission current are also shown in Figure 7.27. For both a 1 minute and 20 minute oxidation, the maximum current obtained before destruction was only 1.2μA. Emission was very unstable. Figure 7.28 also shows maximum emission current plotted versus oxidation time.

	Starting Voltage / V	Maximum Current / µA
Before Treatment	333V	15µA
After 1 minutes oxidation (papoxid)	1070V	1.2µA
After 30 minutes oxidation (Tothinox)	1659V	2µA

It is clear that following oxidation of anodised p-type emitters, the starting voltage was drastically increased.

Table 7.35 Starting Voltage and Maximum Current Following Oxidation at 950°C

Sample Type	Starting Voltage for Freshly Anodised Samples / V	Starting Voltage / V after Oxidation and Removal of Porous Silicon	Mean Maximum Current for Freshly Anodised Samples	Maximum Current after Treatment
Sample originally anodised for 30 seconds (papoxhfthin)	333V	540V	15µA	3µA

It is clear that following removal of the PS layer (by oxidation and dipping into buffered HF), the starting voltage returned to a higher value which was similar (but slightly higher) to that obtained prior to anodisation.

Table 7.36: Anodised P-Type FEA Oxidised for 1 minute at 950°C and Dipped into Buffered HF to Remove Porous Silicon Layer

These results indicate that the nature of the emission from oxidised anodised FEAs was not the same as proposed by Yue *et al.* (1990).

7.3.2 Removal of Porous Silicon Layer

The effect of removing the PS layer from the anodised surface was investigated for the following reason. If emission had actually occurred from the interface between the bulk and porous silicon, it could be expected that removal of the PS layer should have enhanced the emission, as the interface would then have been fully exposed.

Samples were oxidised at 950°C for 1 minute. They were then dipped into a buffered HF solution for ~20 seconds. TEM examination carried out on samples treated in this way showed (see Chapter 6) that the PS layer was completely removed from the tips, leaving behind a rough surface (the original PS/bulk silicon interface). Samples which had been originally anodised for 30 seconds were given this treatment. The field emission results are summarised in Table 7.36. Distributions of starting voltage and maximum emission current after this treatment are shown in Figure 7.29. Figure 7.30 shows plots of starting voltage and maximum emission current after this treatment. The main points are outlined below:

i) After the PS layer was removed from the tip apex, the starting voltage increased dramatically (versus freshly anodised FEAs), returning to a value similar to that obtained from non-anodised silicon.

ii) The maximum emission current was reduced following removal of the PS layer.

It is therefore clear that removal of the PS layer was detrimental to the field emission properties. This indicates that the presence of the PS fibrils were necessary for the improvement in properties observed following anodisation.

7.4 Discussion of Results Described in Section 7.2 and 7.3

7.4.1 Possible Reasons for Increase in Proportion Tips Emitting

After anodisation was carried out, an improvement was seen in the number of cathodes emitting per sample. This was true for both p-type and p^+-type FEAs. This could be explained in terms of the presence of intentional and unintentional asperities, as follows. In the literature, it has been reported that only a small proportion of plain silicon and metal tips in an array will actually emit, see Goodhue *et al.* (1994). This is due to differences in tip radius across FEAs. It is possible that prior to anodisation, field emission only occurred from those tips containing randomly occurring unintentional asperities and that those without an asperity at the apex did not emit at all at the voltages applied. However, the process of anodisation used to form a PS layer on the tip surface, caused many asperities of similar shape and size to be formed at the tip apex. These intentionally formed asperities may have allowed field emission to occur from all tips at low voltage, and that as a consequence, the proportion of tips which field emitted was greater following anodisation.

7.4.2 Potential Explanations for Decrease in Starting Voltage

For both p-type and p^+-type silicon FEAs, the starting voltage was substantially reduced following anodisation. The largest decrease in starting voltage was observed for anodised p^+-type FEAs. This section discusses possible explanations for the reduction in starting voltage observed.

From the Fowler-Nordheim equation (see Section 2.1.2), it is clear that the following may have changed in order to cause the decrease in starting voltage, following anodisation:

a) The work function ϕ may have decreased.

b) The field enhancement factor β may have increased.

This section discusses which is more likely to be the case.

a) Possible Cause - Increase in Field Enhancement Factor

First, it is assumed that there was no change in the work function following anodisation. It will be assumed that the decrease in starting voltage was caused solely by an increase in the field

enhancement factor. An obvious source of field enhancement was the high concentration of small sharp fibrils present at the anodised tip surface, as observed by TEM analysis (Chapter 6). In order to assess whether the presence of these fibrils caused the decrease in starting voltage, the following points need to be considered:

i) Using computer modelling, could the theoretical improvement in field enhancement due to the presence of surface fibrils account for the actual improvement observed experimentally?

ii) Did emission appear to occur from points having smaller radius than before anodisation, which would be consistent with emission from porous silicon fibrils?

i) Theoretical Increase in Field Enhancement Due to Presence of Protrusions at Emitter Surface

Basic electrostatic theory predicts that a hemispherical protrusion on an infinite flat surface will cause a field enhancement of 3 times over that of the flat plane, see Miller *et al.* (1996). However, the situation at an anodised tip is more complicated than this and requires further analysis. Factors which complicate the situation include the following:

1) For a protrusion on a finite curved tip, the field enhancement factor will be slightly reduced versus a flat plane. Therefore the factor would lie in the range 1-3.

2) TEM studies showed that most of the protrusions at an anodised surface were not hemispherical in geometry (Chapter 6).

3) TEM studies showed that anodised silicon FEAs were covered with a high density of small asperities/protrusions. Where several neighbouring protrusions were present on a tip, field screening effects would be expected to have occurred. Screening would have caused a decrease in the expected field enhancement.

In order to create a better model for an anodised tip, fibril-covered emitter, work was carried out in collaboration with Nicolaescu & Filip (1996). The assumptions made in their modelling are

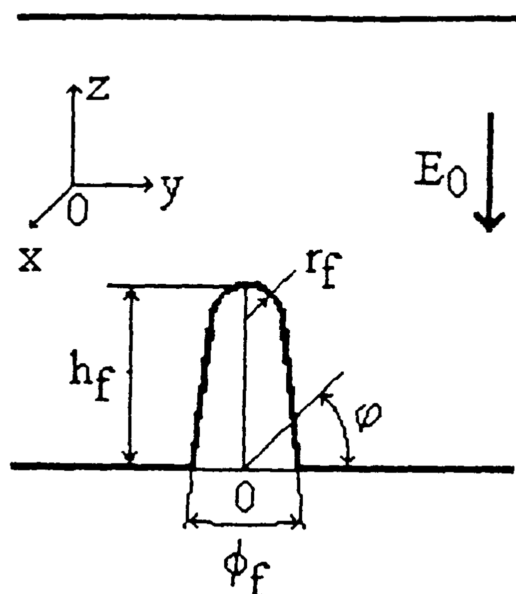
outlined in Figure 7.31. Using this model, a plot of field versus distance between neighbouring fibrils (for both the 5nm and 10nm high fibrils) was produced, see Figure 7.31c). The main results of this modelling are summarised below:

1) For the 5nm high fibril, it can be seen that at large fibril separations, the field at the surface is ~4 times higher than on a completely smooth surface. For a 10nm high fibril, the field at the surface is ~6.5 times higher than the field on a smooth surface.

2) As fibrils become more closely spaced, the field enhancement drops. For a 10nm high fibril, the field enhancement starts to decrease at fibril-fibril separations <80nm (i.e. 8 times the height of the tip). For a 5nm high bump, the field enhancement starts to decrease at a separation <30nm (i.e. 6 times the bump height).

The modelling showed that fibrils of similar size and separation to p^+-type silicon would have caused a field enhancement in the range 4-6 times. The field enhancement factors for p^+-type PS calculated from the experimental results lie in the range 2-3.5 times. Therefore this is encouraging, as the theoretical improvement can fully account for the experimental results. However, these experimentally determined values of field enhancement are lower than predicted by the modelling results. Possible explanations for why the experimental field enhancement was less than the value expected from computer modelling were as follows:

1) **Unintentional Asperities versus Intentional Asperities** - Even non-anodised emitters have asperities at their emission surface. Emission will occur preferentially at these unintentional asperities, thereby lowering the starting voltage. This assumption would be consistent with calculations of emission area presented in the literature, which indicate that emission occurs, in general, from areas which are much smaller than the total tip surface area, see Spindt *et al.* (1976). When tips are anodised, a high density of intentional rather than unintentional asperities are formed on the emitter surface. As the field enhancement due to intentional asperities will not be much higher than the value for unintentional asperities, the reduction in starting voltages could be smaller than expected.



a) Model of Fibril
h_f = height of fibril (5nm and 10nm)
r_f = radius of fibril (2nm)
ϕ_f = angle of fibril (10°)
ρ = half-distance between fibrils

Single fibril model (section in plane YZ)

(Ref: D.Nicolaescu, V.Filip and P.R.Wilshaw, *Appl. Surface Science*, **94/95** (1996), 79)

Figure 7.31 - Modelling of Theoretical Increase in Field Enhancement Due to Presence of Protrusions at Anodised Emitter Surface
The situation of a fibril-covered, anodised emitter has been modelled in conjunction with Dan Nicolaescu at the Research Institute for Electronic Componenets in Bucharest, Romania.

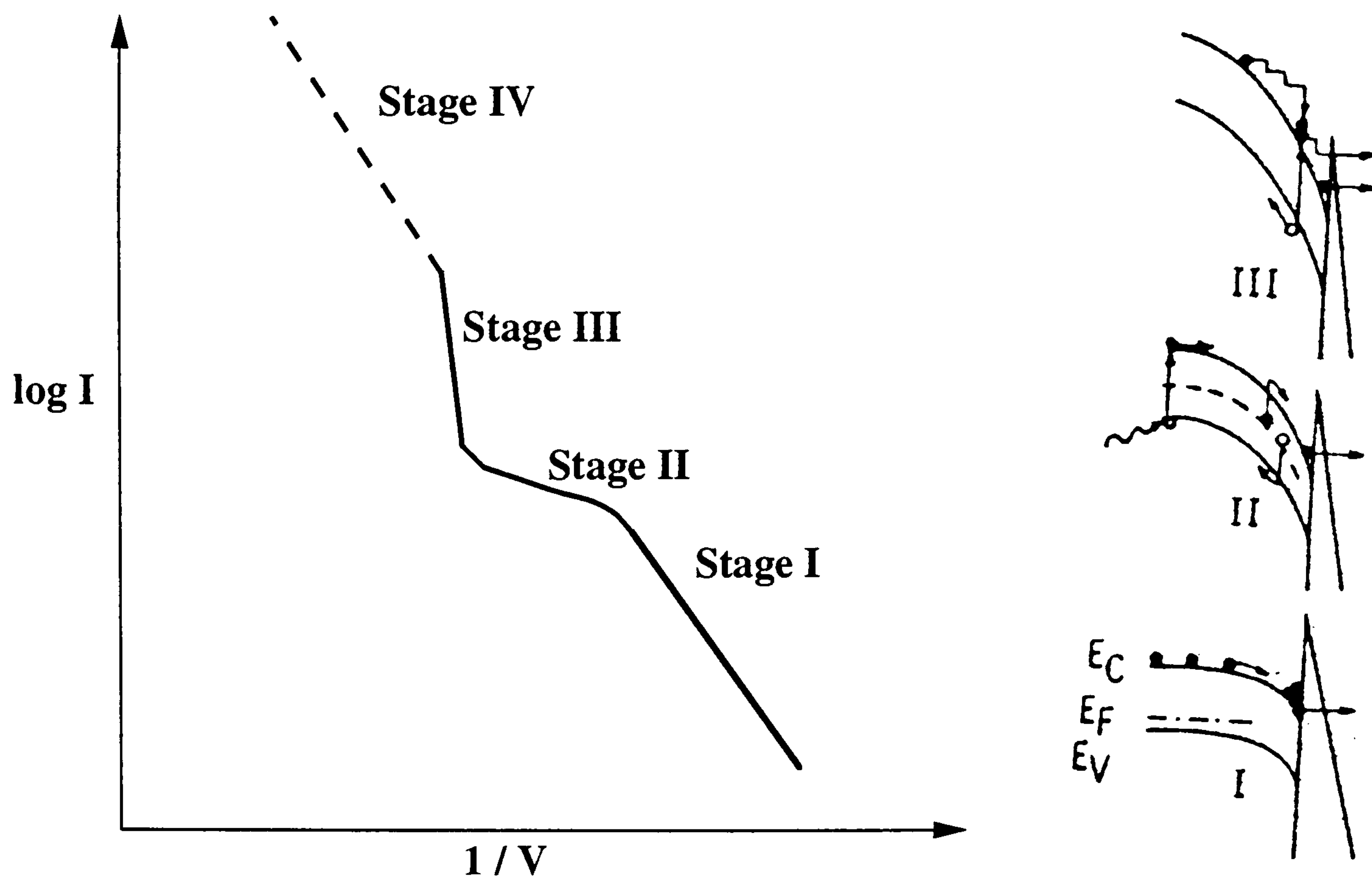
The emitters were considered as being part of a field emission microtriode. The assumptions made in this model are outlined below:

1) The protrusions which have been modelled had hemispherical ends ~2nm in radius and of height 5nm and 10nm. These protrusions were laid on top of smooth underlying emitters (1μm high with tip radius of 100nm). This arrangement is similar to the morphology of p^+-type PS-covered tips as observed in the TEM. However, this arrangement is coarser than the morphology of p-type FEAs - modelling of p-type PS could not be carried out.

2) The arrangement of the fibrils in the PS layer had to be approximated as a regular square array of identical fibrils. However, in reality, the fibrils in a PS layer did not have such a regular arrangement.

3) Band bending effects were not taken into account.

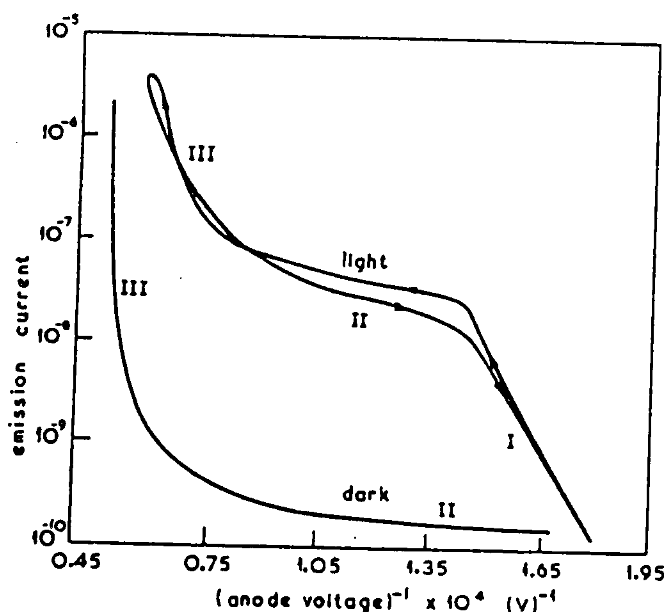
4) As long as the protrusion radius was at least one order of magnitude smaller than the underlying emitter, it was assumed that the field from the underlying emitter could be multiplied by the enhancement from the protrusion.



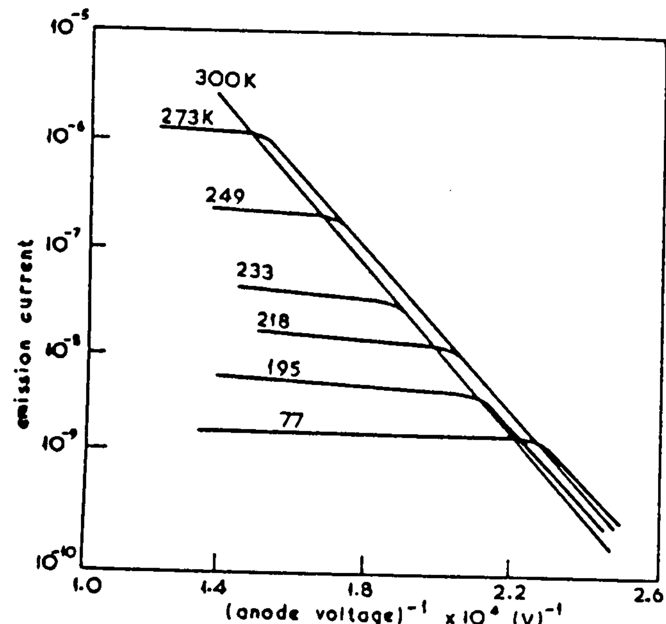
(Ref: D.Schroder, R.N.Thomas, J.Vine and H.C.Nathanson, *IEEE Transactions on Electron Devices*, **12** (1974), 785)

Figure 2.4 - Typical 3-Stage Non-Linear Fowler-Nordheim Plot Obtained from P-Type Silicon Emitters

Stage I - corresponds to emission where the Fowler-Nordheim characteristics are obeyed. Emission is only limited only by the probability of electron tunnelling.
Stage II - corresponds to the situation when field penetration has occurred, creating a depletion region. Current is limited by the electron supply.
Stage III - corresponds to the situation where field penetration is strong enough to cause impact ionization in the space-charge region, causing rapid increase in current to occur.
Stage IV - is not commonly observed, but should occur at high voltage when the rapidly increasing emission current is again limited by the barrier at the semiconductor surface.



a) Field-emitted current for a 40-Ω cm p-type Ge tip at 77K in the dark and with room lights.

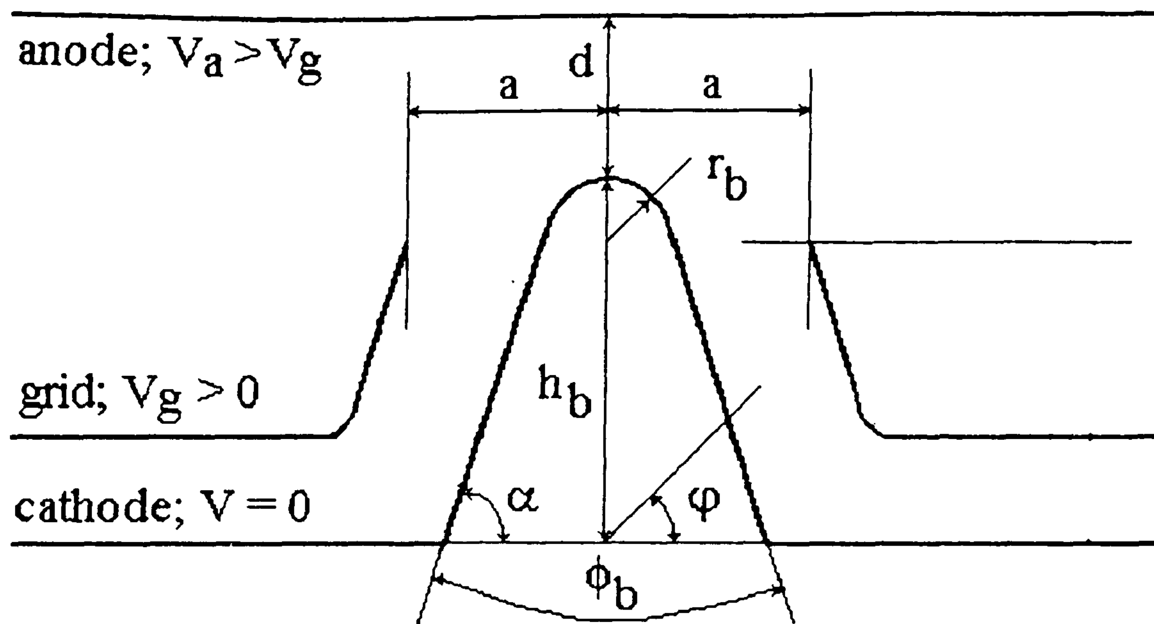


b) Field-emitted current for a 40-Ω cm p-type Ge tip at various temperatures in the dark.

(Ref: J.R.Arthur, *J. Appl. Phys.*, **36** (1965), 3221)

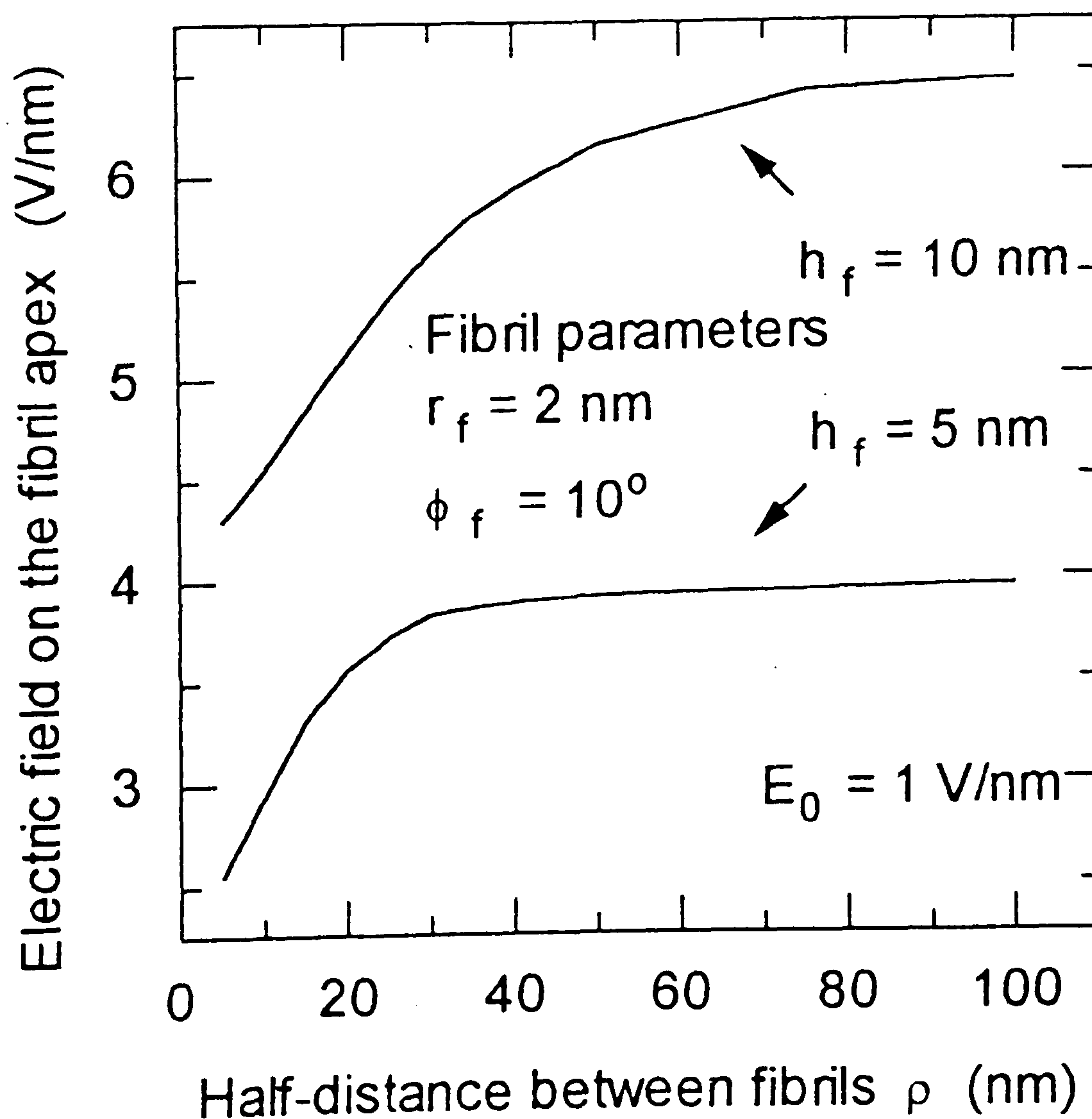
Figure 2.5 - Plots Showing that Typical P-Type Emission is Strongly Affected by Temperature and Illumination

As the temperature and illumination are increased, the saturation current in Stage II will increase, and the length of the saturation region will increase. These effects occur because the surface concentration of electrons is increased by carrying out these treatments.



b) Model of Emitter Triode Device

h_b = height of base emitter (1μm)
r_b = radius of base emitter (100nm)
$\varnothing_b$ = angle of base emitter (50°)



(Figure 7.31 Continued)

c) This graph shows the electric field at the apex of the fibril plotted versus the half-distance between the fibrils.

2) Field Penetration/Band Bending - As explained in Chapter 2, field penetration will occur when the electron supply diminishes. When penetration occurs, the volume of material from which field emission originates lies below the surface and this volume has a geometry which is blunter than the original tip shape, see Schroder *et al.* (1974). This leads to a decrease in the field enhancement factor.

3) Field Screening - This modelling shows that the distance between fibrils would have to be ~6-8 times the height of the fibril, in order for field screening to be prevented. However, fibrils separations were typically only 2-3 times greater than the fibril height.

ii) Calculated Values of Tip Radii (r)

For both p-type and p^+-type FEAs, the values of tip radius (calculated from both α and β) were smaller following anodisation. The decrease in emission area which occurred following anodisation could only have been caused by an increase in field enhancement factor. A reduction in work function alone could not have caused a lowering of the calculated emission area.

Both points discussed above support the proposition that the decrease in starting voltage following anodisation was caused by an increase in field enhancement.

b) Decrease in Work Function/Electron Affinity

The possibility that the decrease in starting voltage was due to a decrease in work function, rather than an increase in field enhancement factor, was also considered. A PS layer formed on a p-type silicon substrate will luminescence if exposed to a laser. It is believed that this is due to the dimensions of the PS structure, which are small enough to cause quantum confinement. The result of quantum confinement is that electrons have increased energy and will cause the bandgap to increase, see Chapter 2. This change will result in a decrease in the electron affinity relative to bulk silicon. It is thought that the total increase in the bandgap for p-type PS should be ~1eV (see Chapter 3). This should lead to a decrease in electron affinity of ~0.5eV. As the usual work function of silicon is ~4.5eV, the effective work function of luminescent PS could therefore be lowered to ~4eV.

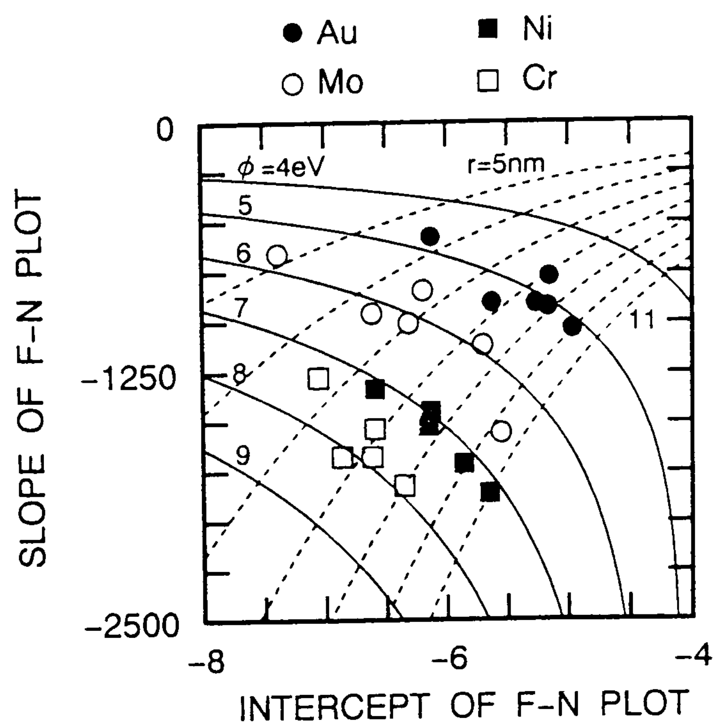
i) Evidence for Work Function Causing Decrease in Starting Voltage is as follows:

One method for distinguishing whether the decrease in starting voltage was caused by an increase in field enhancement or a decrease in work function, is to plot the FN slope versus the FN intercept. The use of this method has been reported in the literature by Ishikawa *et al.* (1993) and Mackie *et al.* (1994), see Figure 7.32. Their plots show that tips having the same field enhancement factor lie along one set of lines, while tips having the same work function lie along another set of lines. If a change in work function had occurred after anodisation, it would be expected that a plot of FN slope versus FN intercept would have shown points obtained before and after anodisation lying on different lines. For a decrease in work function, the line of points after anodisation would be expected to lie above the line of points before anodisation, as shown in Ishikawa (1993).

For the present work, FN slope was plotted versus FN intercept both before and after anodisation, for both p and p^+-type anodised emitters, see Figure 7.33 and Figure 7.34. Although there is much scatter, it can be seen that points before and after anodisation do sit along different lines, and that the lines along which the points appear to sit are equi-work function, rather than equi-radius lines. This indicates that there was some change in work function following anodisation. However, the two sets of data are close together and there is much scatter. If a reference plot had been obtained from a completely clean inert metal surface such as gold, it would have been possible to calculate the absolute difference in work function. Unfortunately, this was not possible as conditions inside the SEM were not UHV.

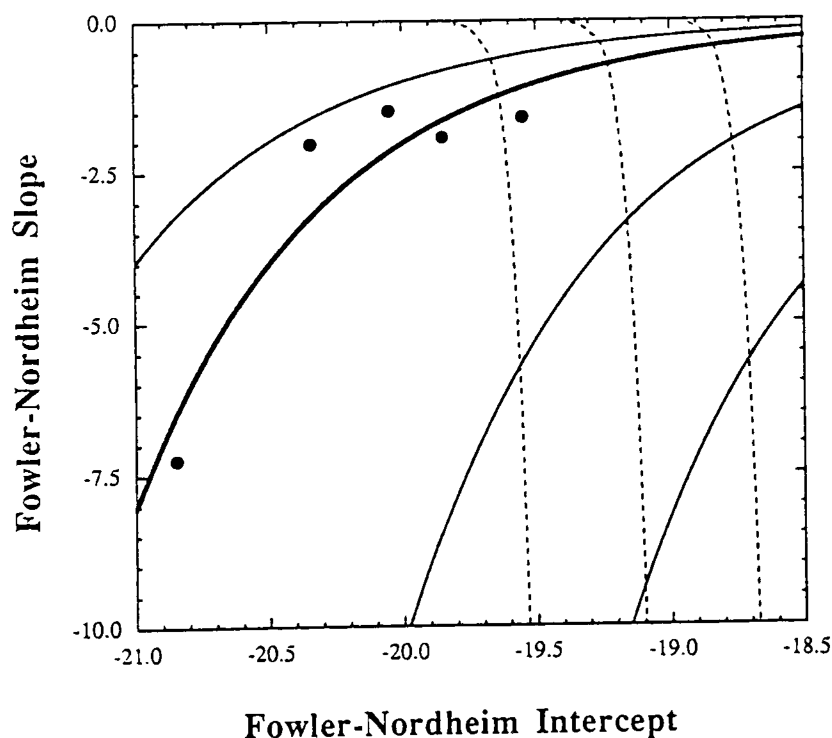
ii) Evidence Against Decrease in Work Function is as Follows:

1) Figure 7.35 shows a plot of field emission current density versus field, for three different values of the work function (4, 4.5 and 5eV; 4.5eV is assumed to be the work function of bulk silicon). It can be seen that a decrease in work function of 0.5eV results in a 25% decrease in the voltage required to obtain a given current density. A 25% drop in starting voltage is less than most results obtained from p-type PS (up to 37% reduction in starting voltage) and is much lower than the results obtained from p^+-type PS (up to 49% reduction in starting voltage). To match the experimental results, a 1eV decrease in the work function would be required. However, it is unlikely that this value could be achieved, even for p-type PS. Therefore, a



(Ref: J.Ishikawa, H.Tsuji, Y.Gotoh, T.Sasaki, T.Kaneko, M.Nagao and K.Inoue, *J. Vac. Sci. Technol. B*, **11(2)** (1993), 403)

a) Results Obtained by Ishikawa *et al.* (1993)
The solid curves indicate the equi-work function lines and the broken curves indicate the equi-apex radius lines.



(Ref: W.A.Mackie, R.L.Hartman, M.A.Anderson and P.R.Davies, *J. Vac. Sci. Technol. B*, **12(2)** (1994), 722)

b) Results obtained by Mackie *et al.* (1994)
(Families of curves for constant work function ø are shown by the dashed lines and for constant field enhancement factor β are shown by the solid lines.)

Figure 7.32 - Fowler-Nordheim Slope Plotted versus Fowler-Nordheim Intercept - Data Reported in the Literature
Tips which have the same field enhancement factor as each other lie along one horizontal line, while tips which have the same work function as each other lie along a perpendicular line.

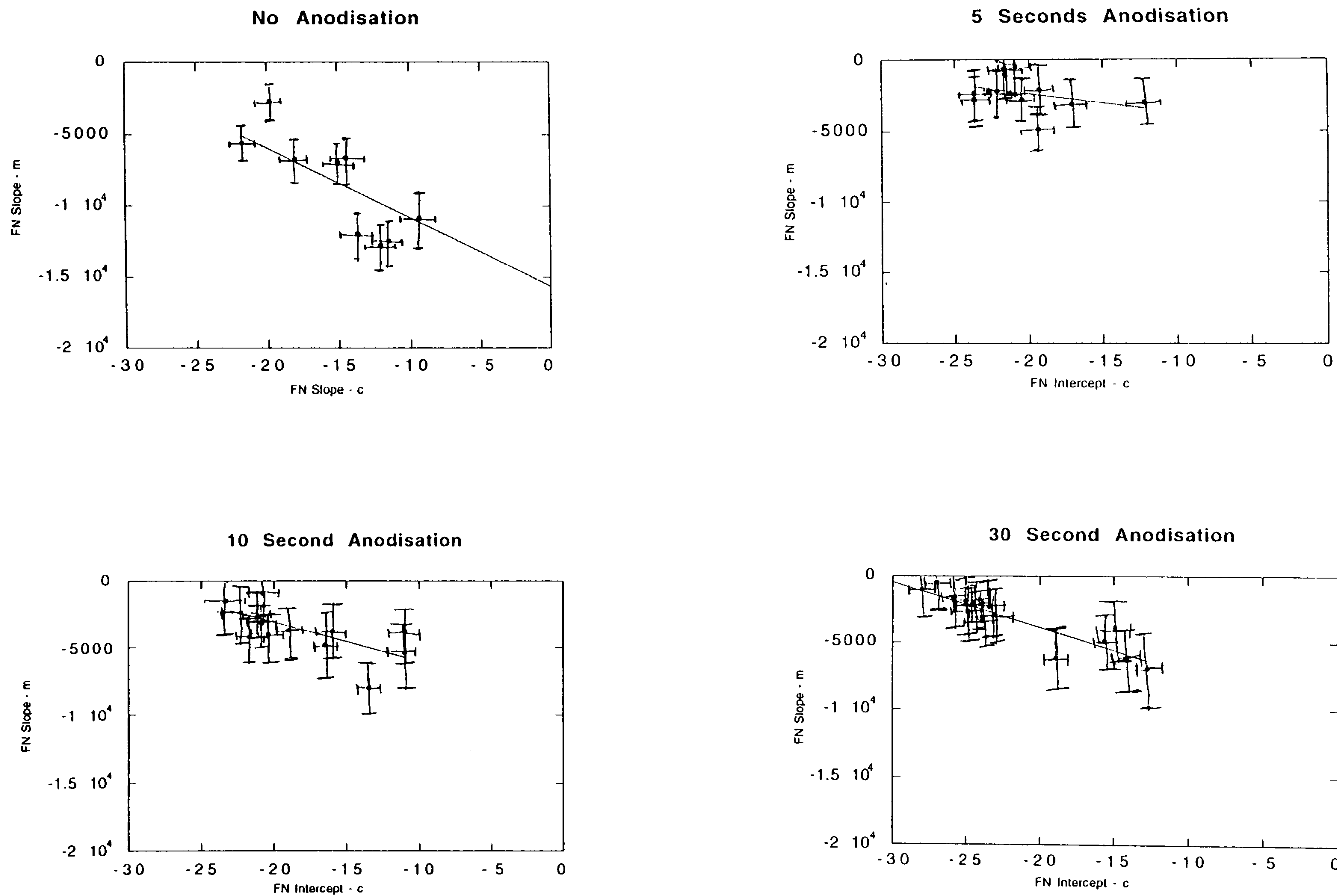
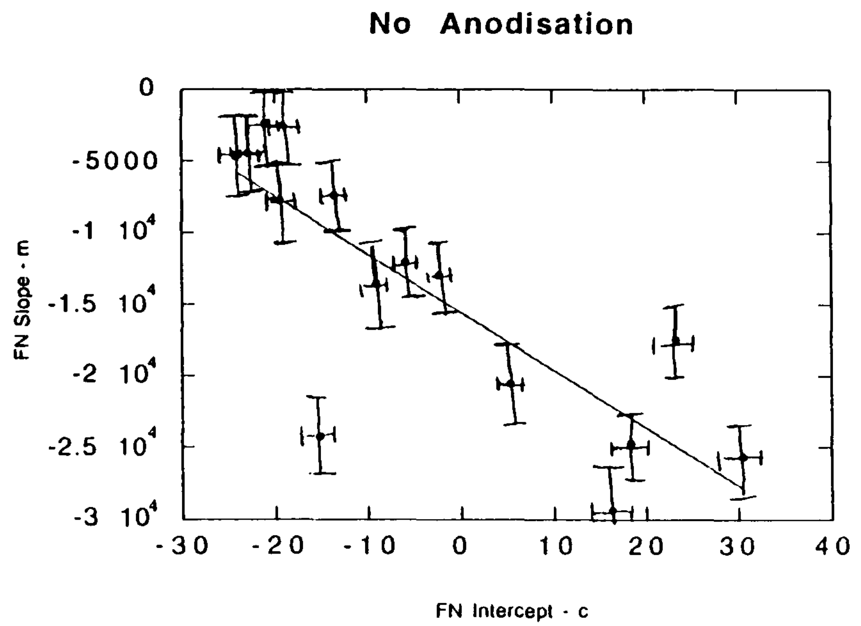
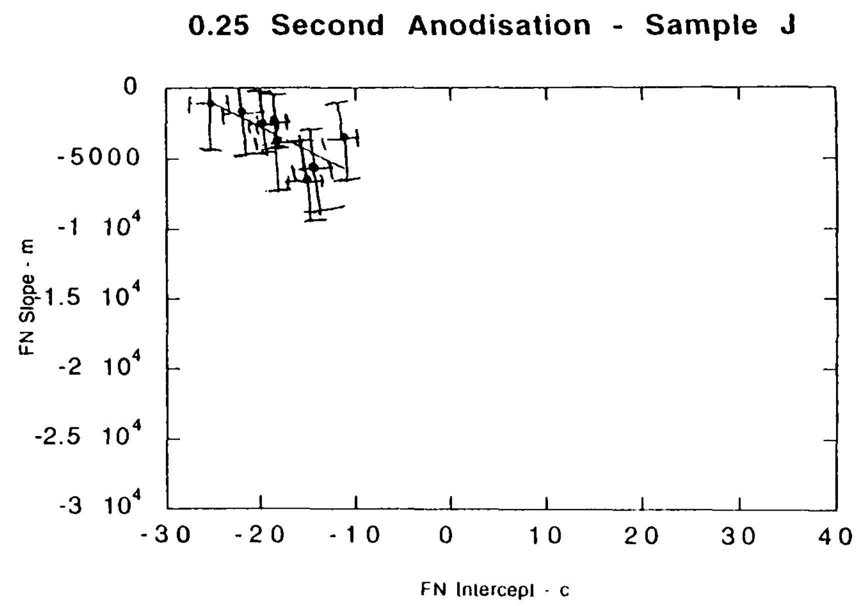
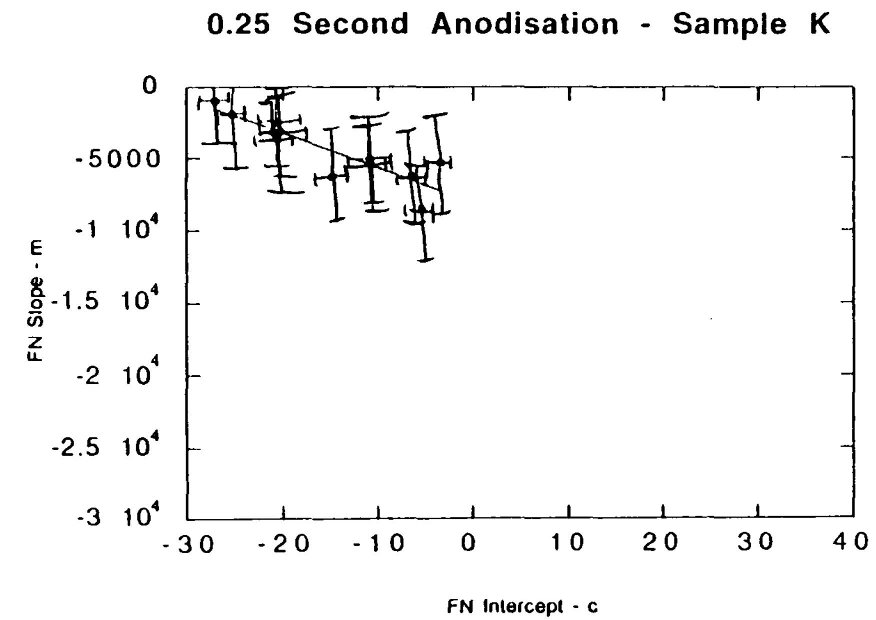


Figure 7.33 - Fowler-Nordheim Slope versus Fowler-Nordheim Intercept - P-Type Silicon
≈20 tips examined per sample







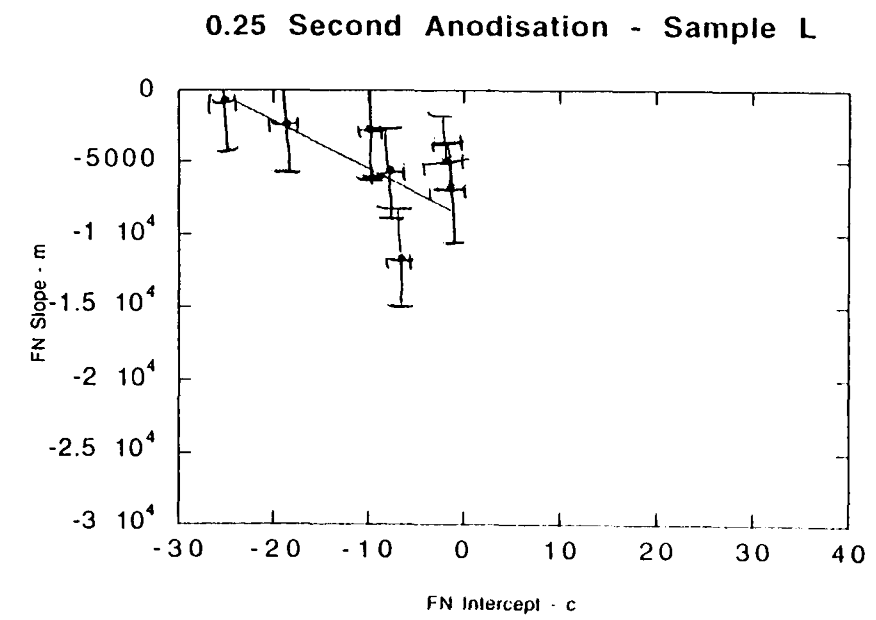


Figure 7.34 - Fowler-Nordheim Slope versus Fowler-Nordheim Intercept - P+-Type Silicon

decrease in work function could not fully account for the decrease in starting voltage observed experimentally.

2) Luminescence from anodised p^+-type samples is much weaker than for anodised p-type samples, see Chapter 3. This is believed to be because quantum confinement only occurs in p-type PS. Therefore, even if a decrease in work function caused the decrease in starting voltage for p-type PS, virtually no decrease in starting voltage would have been expected for p^+-type PS. However, the decrease in starting voltage observed for p^+-type PS was much larger than that observed for p-type PS. Therefore, it is unlikely that a decrease in the work function caused the reduction in starting voltage, for p^+-type PS at least.

3) Few measurements of the work function of PS have actually been reported. However, Bhoraskar *et al.* (1994) have measured the work function of PS, using the retarding field method (Rajopadhye and Bhoraskar (1986)). They report that the work function of PS was actually increased versus non-anodised silicon, and that it increased with anodisation current density.

c) Overall Summary

An increase in field enhancement factor could account for the decrease in starting voltage following anodisation; whereas, a decrease in work function is unlikely to have caused a decrease in starting voltage. However, it is possible that a combination of both an increase in the field enhancement and a decrease in the work function caused the decrease in starting voltage.

7.4.3 Possible Explanation for Why Anodised P^+-Type FEAs Exhibit Lower Starting Voltages than Anodised P-Type FEAs

Although the field enhancement factor for anodised p^+-type FEAs was similar (although slightly lower) to that obtained for anodised p-type FEAs, the starting voltage for anodised p^+-type FEAs was lower than for p-type FEAs. A plot of starting voltage versus field enhancement factor is shown in Figure 7.36. This shows that although p-type PS had higher field enhancement factor, p^+-type PS had the lowest starting voltage. Therefore, the lower starting voltage from p^+-type PS cannot have been caused by the fibrils having higher enhancement factor. A plot of starting

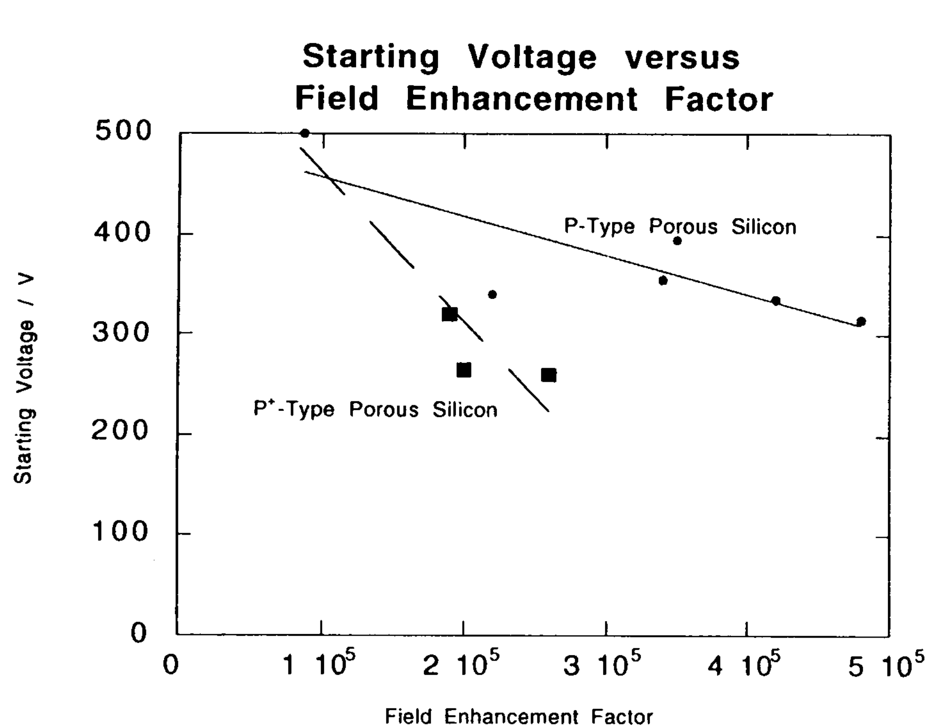


Figure 7.36
This shows that although the field enhancement factor for p-type porous silicon is slightly higher, it exhibits higher starting voltages than for p$^+$-type porous silicon.

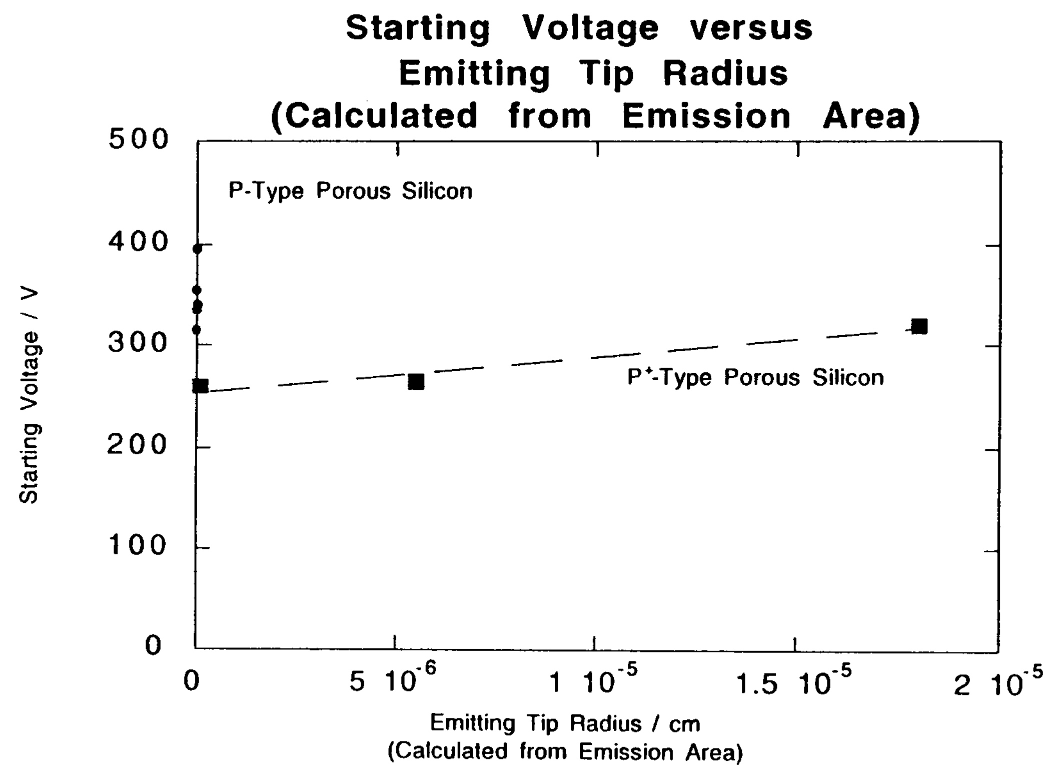


Figure 7.37
This shows that the low starting voltages exhibited by p$^+$-type porous silicon may have been due to the larger emitting radius.

Figure 7.36 and Figure 7.37 - Field Enhancement Factor Plotted versus Starting Voltage and versus Emitter Tip Radius

voltage versus tip radius is shown in Figure 7.37. This shows that the larger the apparent emitter tip radius (and therefore emitting area), the lower the starting voltage.

An explanation could be as follows. After anodisation, it is possible that the number of actual emitting sites (fibrils) was higher for p^+-type PS, than for p-type PS. Therefore, even though the p^+-type fibrils were less sharp and so produced less current at a given voltage, a tip containing many emitting fibrils (p^+-type PS) could have a higher overall current than for a tip containing a much smaller number of emitting fibrils (p-type PS). This could therefore account for the fact that anodised p^+-type FEAs exhibited lower starting voltages than for anodised p-type FEAs. In addition, the number of emitting fibrils would influence calculation of the radius of the individual emitting fibrils. The presence of many emitting fibrils at a p^+-type PS tip would have resulted in a larger apparent value of emitting radius for p^+-type PS fibrils than was actually the case. Therefore, the emitting radius for p^+-type PS fibrils could have been closer to p-type PS fibrils than has been reported in this chapter. As a result, the current obtained from a single p^+-type fibril at a given voltage may have been more similar to p-type PS fibril than originally believed. If this was true and the actual number of emitting fibrils at the surface of a porous p^+-type tip was higher than the number of emitting fibrils at the surface of for a porous p-type tip, the overall current from a porous p^+-type tip will have been higher than the overall current obtained from a porous p-type tip. Unfortunately, the exact number of separate emitting fibrils at the tips could not be determined in the adapted SEM.

This explanation could also be used to explain, to some extent, why the starting voltage was lower following anodisation of both p and p^+-type FEAs. Following anodisation, the number of emitting sites may have been much greater. Therefore, more current could be obtained at the same voltage and so the starting voltage (defined as voltage at which 1nA current was obtained) would appear to be lower following anodisation. However, the increase in the number of emitting sites per tip is unlikely to be a complete explanation for the decrease in starting voltage following anodisation. The calculations indicate that either an increase in field enhancement factor or work function lowering also occurred.

7.4.4 Possible Explanation for Increase in Starting Voltage with Anodisation Time

For both p and p^+-type FEAs, the starting voltage increased with anodisation time. P-type FEAs underwent the longest anodisation times and exhibited the highest starting voltages. One possible explanation is that for longer anodisation times, the radii of the PS fibrils was decreased by etching in the electrochemical solution. If the fibrils were reduced in radii, this would have decreased the overall emission area and so could have led to an increase in starting voltage. If this explanation holds, it is possible that if shorter anodisation times were used, the starting voltage could be lowered even further.

7.4.5 Alternative Source of Field Enhancement

Section 7.4.2 showed that an increase in field enhancement is likely to have caused the decrease in starting voltage following anodisation. It is possible that there was an alternative source of field enhancement to the fibrils at the emitter surface of an anodised tip caused the improvement. This alternative source was the interface between the PS layer and the underlying bulk silicon. As mentioned previously, Yue *et al.* (1990), investigated field emission from oxidised flat layers of PS and claimed that oxidation sharpened up the PS/silicon interface, allowing field emission to occur at very low voltage, from extremely sharp points sitting at the interface.

a) Evidence Indicating that Emission Occurred at Interface

i) TEM has shown that very sharp points existed the PS/bulk silicon e. These points were very similar in nature and size for both p and p^+-type PS, see Chapter 6.

ii) TEM also showed that the geometry of the bulk silicon underlying the p-type PS layer had a much higher aspect ratio than the original tip geometry.

iii) Starting voltage increased slightly with anodisation time. If emission had originated at the interface, the starting voltage would have been expected to increase, as the distance from the emission source increased.

iv) The calculated value of field enhancement for anodised p-type emitters was higher than for anodised p^+-type emitters. A sharp core was only observed for p-type emitters, whereas the p^+-type core was relatively blunt. If emission had occurred at the interface, the field enhancement factor for anodised p-type tips would therefore have been expected to be lower than for anodised p^+-type tips - the field enhancement factor was observed to be slightly lower following anodisation.

b) Evidence to Indicate that Emission did not Originate at Interface

When the PS layer was removed and the sharp core was completely exposed, the emission characteristics were similar to those obtained from non-anodised emitters. If emission had occurred from the interface, the starting voltage would have been expected to be lower (or at least unchanged) after removal of the PS layer. Therefore, the source of field enhancement is unlikely to have been the sharp PS/bulk silicon interface.

c) Summary

The evidence shows that is possible that the source of the field enhancement was the high density of sharp fibrils present at the sharp PS/bulk silicon core interface. However, it is more likely that emission originated at the PS fibrils. However, in order to confirm this, further studies were carried out in the field ion / field emission microscope - the results of these studies are described in Chapter 8.

7.4.6 Discussion of Maximum Field Emission Current Obtained Prior to Tip Destruction

Following anodisation, two competing factors affected the maximum current obtained before tip destruction occurred:

a) Increase in Maximum Current for Short Anodisation - For the thinnest p-type PS layers, the maximum current was found to be 1.5-3.5 times higher following anodisation. However, the maximum current obtained here was much lower than reported during the Part II studies (current up to 10 times higher following anodisation).

b)Decrease in Maximum Current as PS Layer Thickness Increased - For both p and p^+-type PS-covered emitters, a clear reduction was observed in the maximum current obtained at destruction, as the thickness of the PS layer was increased.

a) Possible Reason for Slight Increase in Maximum Current Following Anodisation

A well known method of protecting an FEA from destruction, and for increasing the uniformity from tip to tip, is to introduce a highly resistive layer beneath the individual cathodes, see Baptist *et al.* (1993). The tips are then protected from sudden increases in current (current bursts) by the resistive film, as the sudden increase in voltage will fall across the resistive layer rather than across the tip.

Values for the resistivity of PS have been obtained by some researchers and can be as high as $10^6\Omega$cm (depending on dopant type and formation conditions), see Chapter 3. It is therefore possible that a PS layer at the tip surface could act in a similar manner to a resistive layer such as that incorporated into devices by Baptist *et al.* (1993). Each p-type PS cathode could be considered to be composed of many nanoscale emitters, each of which is a single asperity, connected to an underlying substrate by a thin but highly resistive layer, namely the p-type PS. In this way, the current emitted from each fibril would be to some extent limited by the voltage drop produced by the current flowing through the underlying resistive layer. As the current would be limited, the emitting asperity would be less likely to destruct and so would reach a higher current before blowing. The longer an emitting asperity survived, the higher the probability that other asperities around it could emit. This in turn would lead to an increase in the emission current.

However, compared to early results obtained in the poorer vacuum, the increase in maximum emission current following anodisation, is less dramatic. These early results showed that there was a ten-fold increase following anodisation. A possible explanation for the difference in results is that the tip geometry used for these early experiments was different. During the early experiments, the tip geometry was a blunt, over-etched point or wedge; whereas sharp-cornered square-topped emitters were used for the experiments reported here. It is possible that

anodisation affects different tip geometries in different ways. It is possible that anodised relatively blunt emitters were more thermally stable than anodised sharp-cornered emitters, and so reached higher maximum currents prior to self-destruction. Further investigation should now be carried out on blunt anodised emitters (in the improved vacuum), to check whether the improvement in emission current following anodisation is larger for blunt emitters than for sharp emitters.

b) Possible Reason for Dependence of Maximum Emission Current on PS Layer Thickness

PS layers are highly resistive. Therefore, as the thickness of the PS layers increased, the total resistance of the layer should also have increased. It is possible that when the resistance of the layer reached a certain value, significant resistive heating occurred, which could have caused the layer to overheat and break down, causing the field emitter to undergo self-destruction. A planar resistive layer beneath an array of tips acts as a large heat sink to dissipate heat energy dissipated. However, in the case of the anodised tip, dissipated energy would have been confined to a very localised region with no escape and so heating would definitely have occurred. Following the peak in maximum current at very short anodisation times, the maximum emission current decreased as the PS layer thickness was increased. This relationship would support the theory that resistive heating occurred, as resistive heating is proportional to the square of the resistor value.

It is possible that if p^+-type PS thinner than 40nm and p-type PS thinner than 14nm had been investigated, higher emission currents could have been obtained. However, to produce much thinner layers (particularly for p^+-type PS) more accurate anodisation equipment would have been required.

7.5 Comparison to Similar Work Carried Out by Other Researchers

Since the start of this work, several other researchers have reported investigations into field emission from PS. This section compares the results reported in this thesis with the results obtained by other researchers.

7.5.1 Emission from anodised un-gated emitters

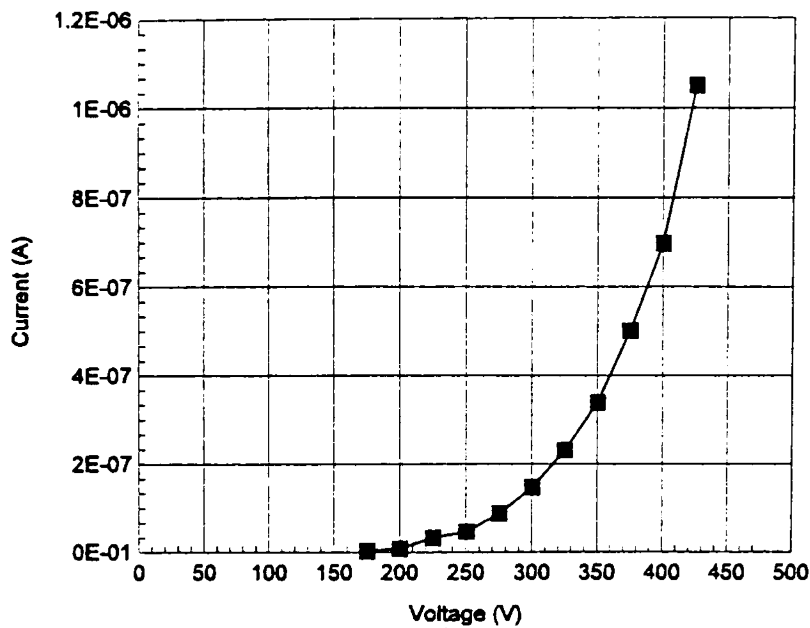
1) Jessing *et al.* (1996) formed a thin layer of PS on p^+-type silicon cones. They examined the field emission characteristics in a vacuum of 7×10^{-7} torr, using a system similar to that reported in this thesis. An example of a typical FN and IV plot obtained is shown in Figure 7.38. The main points are listed below:

i) After anodisation, the starting voltage (voltage required to obtain 1nA) was typically ~150V and 1μA was obtained at ~420V. These results are comparable to those reported in this thesis (from p^+-type FEAs), where the mean starting voltage could be as low as 160V (mean value ~250V) and 1μA was obtained at voltages in the range 320V-410V. It is encouraging that their results are so similar to ours.

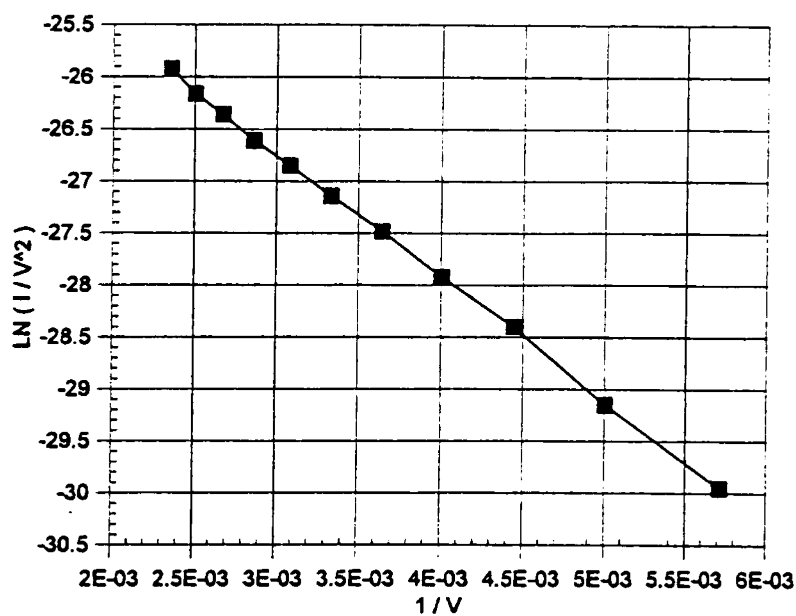
ii) Jessing *et al.* (1996) claim that the field emission characteristics of anodised tips were more reproducible and more stable than for non-anodised tips and that they were stable over extended periods of time. This is encouraging. In the present work, extensive stability tests were not carried out, due to problems with the apparatus. However, the stability of anodised tips was certainly no worse than from non-anodised tips. (The emission stability of anodised FEAs needs to be investigated as part of further work, but this cannot be done until a new measuring technique (other than adapted SEM) is devised or gated devices are developed.)

iii) Unfortunately, these researchers did not report the results obtained prior to anodisation. Therefore, no comparison could be made to show the extent of any improvement. Furthermore, the PS morphology at the anodised tip apex was not reported. Therefore, it was not known whether the fibril structure and PS layer thickness were truly comparable to the results reported in this thesis. No attempt to optimise the emission properties by varying the PS layer thicknesses or initial substrate doping was reported.

2) Evtukh *et al.* (1996) reported tests carried out on anodised non-gated n-type silicon emitters. They reported an improvement in the field emission properties, observing a 40% decrease in starting voltage. However, they did not report the morphology of the PS at the tip. As the emitters were manufactured from n-type silicon, the structure and thickness of their PS layer is



a) Current-Voltage Plot for an Anodised Silicon Cone



b) The corresponding Fowler-Nordheim plot

(Ref: J.R.Jessing, D.L.Parker and M.H.Weichold, *J. Vac. Sci. Technol. B*, **14(3)** (1996), 1899)

Figure 7.38 - Emission from Anodised Un-Gated Silicon Emitters - Results Obtained by Jessing *et al.* (1996)
The results shown here were obtained by Jessing *et al.* at the University of Texas A&M University. The samples were examined in a vacuum of 7×10^{-7} torr by positioning a small tungsten probe above the emitters - this testing equipment was similar to that used in the present work.

likely to have been different to that obtained from p-type silicon. They claim that the starting voltage was lowered due to the presence of fibrils at the emitting tip surface. However, they did not provide any evidence to support this theory.

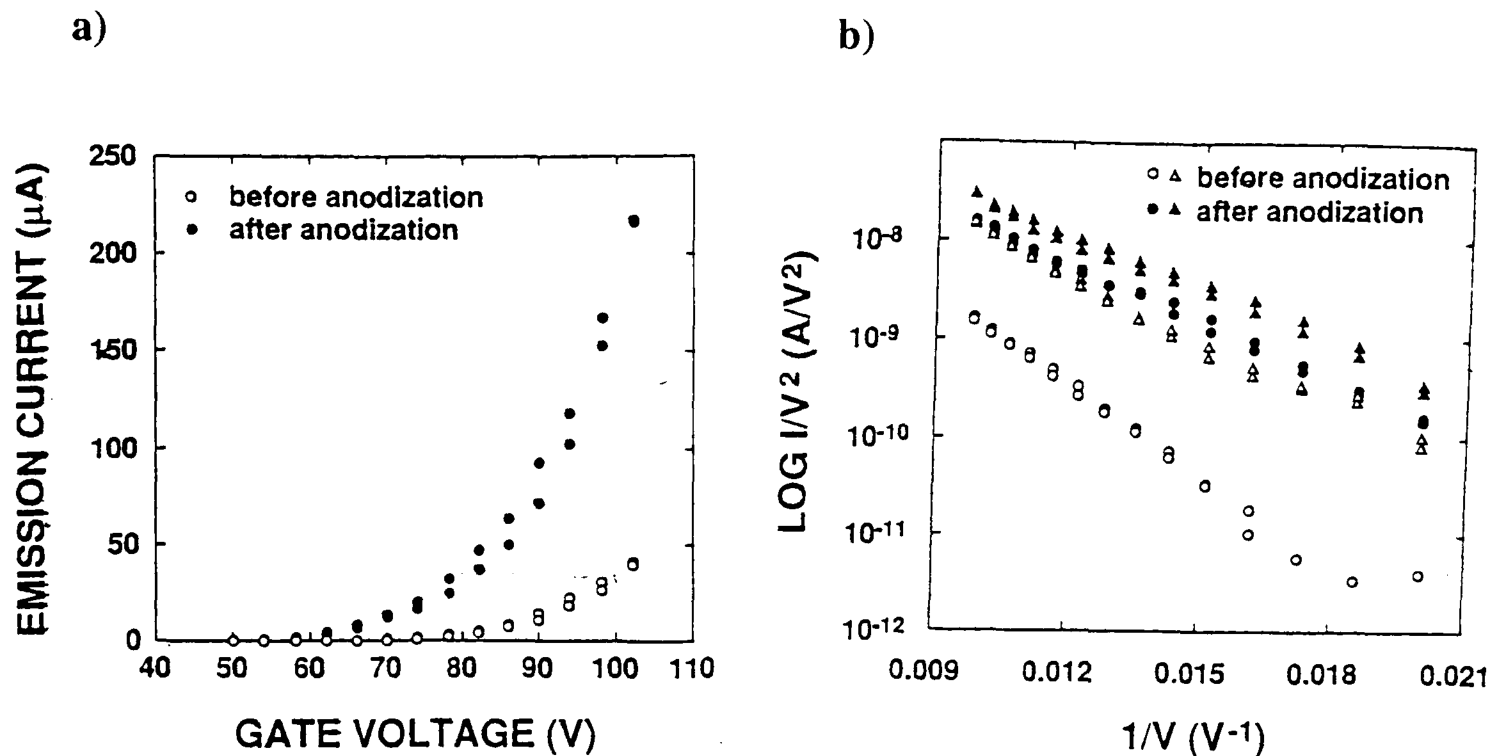
7.5.2 Emission from Anodised Gated Emitters

Takai *et al.* (1995) investigated field emission from gated arrays of silicon emitters. This work is particularly interesting, as the facilities to gate tips were not available during the present work. It was possible for these authors to anodise the gated FEAs because the insulator between the substrate and the gate was manufactured from SiO. SiO etches much more slowly than the SiO_2 which is typically used for insulation in gated devices. It is important that the insulator remains intact in order for the device to operate. In their work, n-type silicon (rather than p-type silicon) was anodised using a current density of $40mAcm^{-2}$, in a solution of HF:water:ethanol in the ratios 1:1:2. The samples had to be illuminated with an Ar laser during anodisation. Anodisation was carried out for times in the range 15-60 seconds. Tests were carried out under a vacuum of 10^{-10} torr. An example of a typical IV and FN plot are shown in Figure 7.39. The main results are outlined below:

i) Their work confirmed that the improvement in field emission following anodisation could be reproduced with gated arrays as well as ungated arrays.

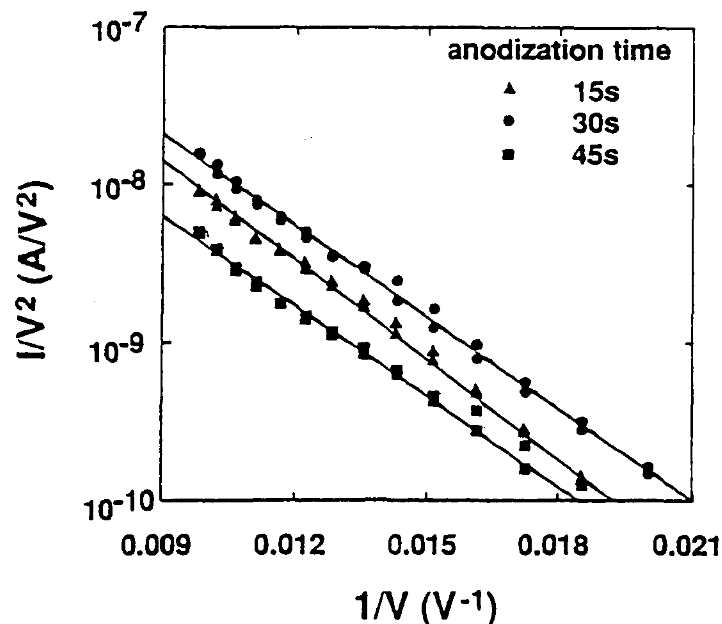
ii) The gate voltage required for emission was lowered by ~22% following anodisation. This is slightly lower than the results reported in this thesis for ungated p-type PS. However, a direct comparison cannot be made. This is because the FEAs were manufactured from n-type silicon, rather than from p-type silicon and therefore the PS fibril structure and PS layer thickness may have been different. Unfortunately, TEM studies following anodisation were not reported and so the morphology of the anodised apex was unknown.

iii) The current obtained at a given voltage was increased by a factor of 5 following anodisation. This was higher than observed during the course of this thesis, but was more similar to the results obtained in this work during early testing.



a) Emission Current as a Function of Gate Voltage for Field Emitter Arrays (FEAs) Before and After Tip Surface Anodisation

b) Fowler-Nordheim plots for silicon FEAs before and after tip surface anodisation



c) Fowler-Nordheim plots for Silicon FEAs after tip surface anodisation with three different anodisation times of 15, 30 and 45 seconds, corresponding to n-type porous silicon thicknesses of 235, 470 and 705nm.

(Ref: M.Takai, M.Yamashita, H.Willw, S.Yura, S.Horibata and M.Ototake, *J. Vac. Sci. Technol. B*, **13**(2) (1995), 441)

Figure 7.39 - Emission from Anodised Gated Silicon Emitters - Results Obtained by Takai *et al.* (1995)
The results shown here were obtained by Takai *et al.* (1995) at Osaka University, Japan and Mitsubishi Electric Corporation, Japan.

iv) The field emission properties were dependent on the PS layer thickness - emission was found to be degraded for anodisation times >30 seconds. This is similar to the results reported in this thesis.

Although mentioned briefly, no evidence was provided to identify what caused the decrease in starting voltage observed.

7.5.3 Emission from Flat Anodised Substrates

Yue *et al.* (1990) investigated the emission characteristics of flat anodised p^+-type silicon substrates. Anodisation was carried out at ~250mAcm^{-2} for 2 seconds, in order to form a PS layer ~0.4μm thick. As mentioned previously, flat PS layers which had been oxidised were also investigated. The authors claim that in both cases, extremely sharp tips were formed at the PS/bulk silicon interface, which allowed electrons to be collected at very low voltages. However, they also suggested that emission could have occurred from sharp PS fibrils. They did not prove which of these actually caused the decrease in starting voltage following anodisation.

7.5.4 Summary

It is encouraging that others have obtained similar results. The work carried out on gated FEAs is particularly encouraging and it is clear that this should be investigated further when the facilities for gating are available. Unfortunately, in the majority of cases, the actual morphology of the anodised tip surface has not been investigated. Therefore, it is difficult to compare between the results obtained by different authors. In particular, none of these researchers have thoroughly investigated the true source of field emission or the cause for the decrease in starting voltage following anodisation. Little attempt has been made to optimise the field emission properties by changing the PS layer thickness or the initial substrate doping.

7.6 Effect of Ageing and HF Dipping

7.6.1 Results from Aged FEAs

The effect of ageing on the field emission characteristics of p-type PS was investigated (there was not sufficient time to examine the ageing of anodised p^+-type FEAs). An FEA originally

anodised for 10 seconds, and which had already been characterised, was stored in a dessicator for a period of ~6 months. Its field emission properties were then re-characterised. Table 7.37 summarises the results obtained. The main points are summarised below:

a) Emission Current

Distributions of the maximum emission current after ageing are shown in Figure 7.40. There was little difference in the maximum emission current obtained from fresh and from aged samples. In fact, the value for aged samples was slightly higher than for fresh samples (being ~20μA versus 14μA for fresh samples). The proportion of tips blowing at current levels <5μA was similar, being ~20% for the freshly anodised and ~30% for the aged sample.

b) Starting Voltage and Voltage for Higher Current Values

The initial starting voltage was higher than for freshly anodised FEAs. However, the starting run could be lowered by carrying out a second run. The mean starting voltage on the first run was 570V, compared to 390V on the second run. The mean starting voltage for the freshly anodised sample (anodised for 10 seconds) was 330V. Therefore, the second run was higher than for fresh samples, but was still lower than for either fresh or aged non-anodised silicon. A comparison of current versus the mean voltage required to obtain a particular current, for freshly anodised, aged anodised and fresh non-anodised samples, are shown in Figure 7.41. The plot from the freshly anodised FEA and the second plot from aged samples are close.

7.6.2 Results from Aged and HF Dipped FEAs (1 Day Old and 6 Months Old)

The effect of HF dipping was investigated in order to determine whether this treatment restored the field emission characteristics of aged anodised FEAs. The emission characteristics of FEAs aged for different times and then dipped into buffered HF have been compared. Table 7.37 also summarises the results obtained from aged samples following HF dipping. Table 7.38 summarises the results obtained from freshly anodised PS which was given an HF dip only 1 day after anodisation. The results are plotted in Figure 7.42. The main results are outlined below:

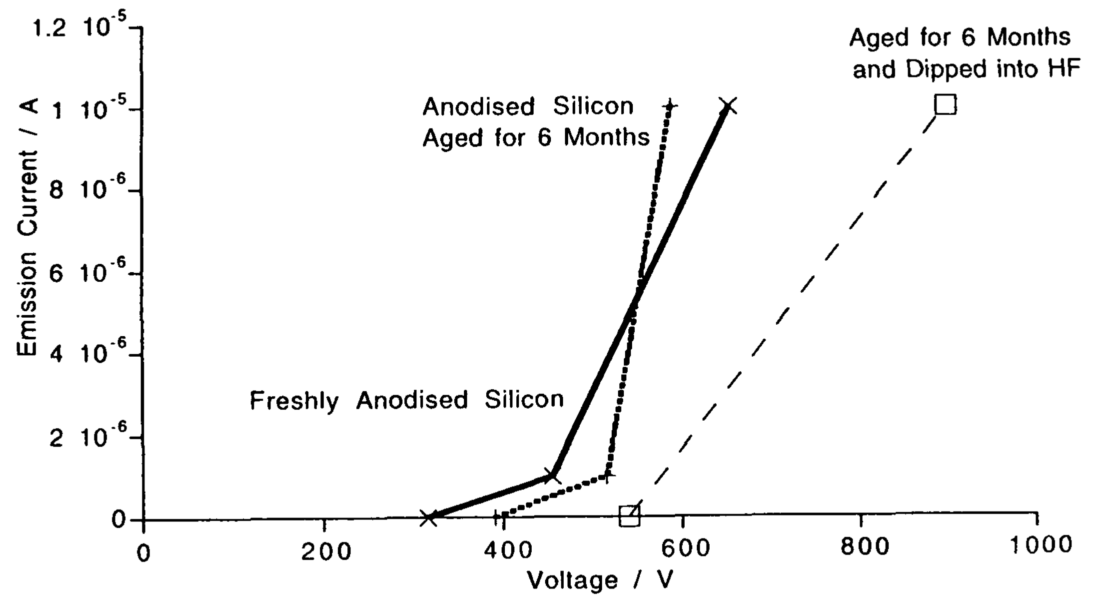
	Starting Voltage / V	**Maximum Current / μA**
Freshly Anodised Emitters	333V	19μA
Ageing for 6 Months in Dessicator	570V on first run 390V on second run	20μA
After Treatment of Aged Samples with HF	540V	17μA

Table 7.37: Starting Voltage for P-Type PS-Covered Sample Aged for Six Months

	Starting Voltage / V	**Maximum Current / μA**
Freshly Anodised Emitters	333V	19μA
After Treatment with HF	510V	15μA

Note that: 1) HF dipping did not restore the field emission properties of PS exposed to air for long periods.

Table 7.38: P-Type PS-Covered Sample 1 Day Old When Dipped into Buffered HF



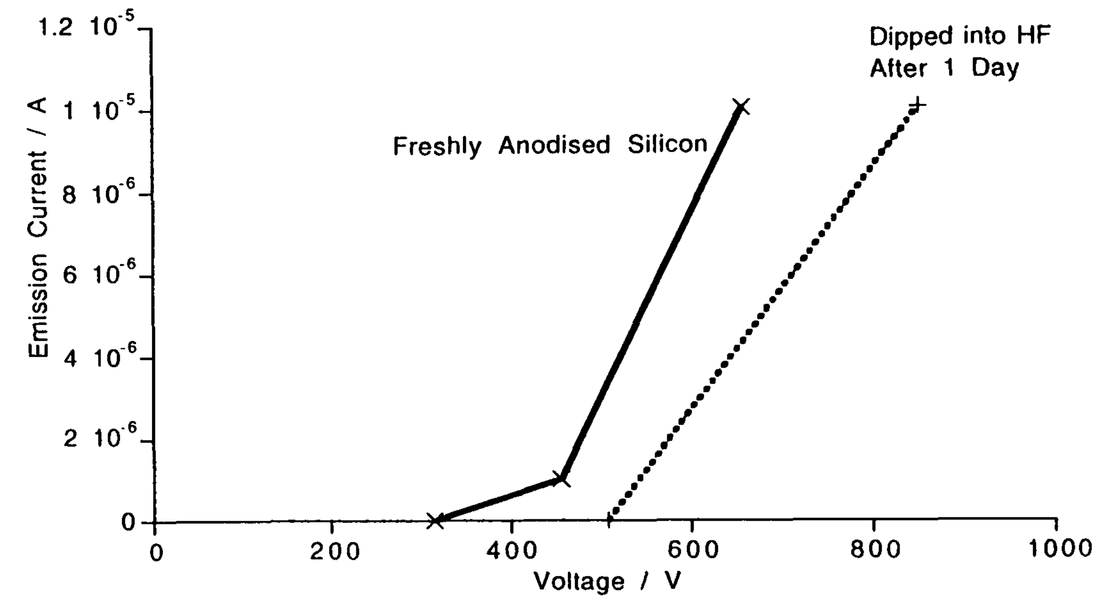


Figure 7.42 - Comparison of Current versus Voltage After Ageing and HF Dipping (For Porous Silicon Aged for 6 Months and Porous Silicon Only 1 Day Old)

a) For both the day-old and month-old samples, there was a drastic increase in the starting voltage, following HF dipping.

b) For both the day-old and month-old samples, the emission was very unstable following HF dipping. FN plots were very noisy following HF dipping, and lower emission currents were collected.

TEM examination (see Chapter 6) has shown that if the specimen was several weeks old, the PS layer could be completely removed by dipping into buffered HF, without an oxidation step. However, if the sample was only a couple of days old, some residual (but discontinuous) PS material was still left at the tip apex. The difference in the degree to which the PS layer was removed is believed to depend on the degree of oxidation of the PS layer, which depends on the time since anodisation. However, it is clear that even partial removal of the PS layer from the surface of FEAs seriously degraded the field emission properties of anodised FEAs. Therefore, HF dipping cannot be used to restore the low starting voltages of PS samples which have undergone ageing.

7.6.3 Discussion

Ageing caused an increase in the starting voltage of anodised FEAs. In Chapter 6, it was shown that the aged p-type PS samples had diffuse diffraction patterns, which implied that they were completely oxidised. Therefore, the increase in starting voltage relative to freshly anodised samples, was probably caused by the formation of an oxide layer. The starting voltage could be reduced again by carrying out a second run (either disruption of the oxide layer or tip sputtering occurred). However, an HF dip which is typically used to restore the characteristics of aged non-anodised FEAs, could clearly not be used to completely restore the emission properties of aged anodised emitters.

In a working device, the emitter should not be exposed to air. However, further work needs to be carried out to examine the stability of field emission properties with time, following storage under vacuum. Unfortunately, this was not possible using the apparatus available during the course of this project, due to the fact that the 505 SEM probe was too unstable. If long term

emission studies had been carried out over several weeks or months, stability would have been seriously affected by probe oscillations and creep of the specimen stage. In order to carry out such testing, a fixed probe and stage would have been needed.

7.7 Overall Summary of Results and Conclusions for Chapter 7

- The operating voltage of both p-type and p^+-type silicon FEAs was significantly reduced following anodisation. It is believed that this was due to the presence of sharp fibrils at the anodised surface, which caused field enhancement (rather than a decrease in work function). Further evidence for this is presented in Chapter 8. This is different to the explanation given by Yue *et al.* (1990), that operating voltage was lower due to emission from sharp points on the bulk silicon/porous silicon apex.

- The operating voltage of p^+-type silicon FEAs was lower than for p-type silicon FEAs. This is believed to be due to the fact that the emitting area (due to either larger surface fibrils or larger number fibrils emitting) were larger for p^+-type silicon FEAs than for p-type silicon FEAs.

- There was an increase in maximum emission current following anodisation, but this increase was relatively small. However, it is thought that the effect of anodisation on the maximum emission current may be related to the tip geometry - initial testing in the poor vacuum on blunt emitters had shown much higher increases in emission current following anodisation.

- The maximum emission current obtained from anodised PS emitters decreased as the thickness of the PS layer increased. It is believed that that the PS layer acted as a resistive layer, which broke down when it became too thick.

- Ageing significantly increased the starting voltage of anodised FEAs. A buffered HF dip could not be used to restore the emission characteristics prior to ageing (even for sample only 1 day old), as this resulted in partial or total removal of the PS layer.

7.8 - Suggestions for Further Work

Further work should be carried out in order to understand the characteristics of anodised FEAs fully. These include the following:

1) It should be checked whether the nature of the initial tip geometry influences the increase in maximum emission current following anodisation.

2) The anodisation equipment should be improved so that shorter anodisation times are possible. Emission from thinner PS layers may allow higher emission currents to be obtained.

3) The long-term stability of anodised FEAs versus non-anodised FEAs should be studied in detail, as it was not possible to examine stability with the equipment available in this work. In order to do this, a new measuring system allowing the probe-sample separation to remain constant (or development of gated devices) needs to be developed.

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Chapter 8 - Field Ion/Field Emission Microscopy of Anodised Silicon Tips

8.1 Introduction

Field ion and field emission microscopy (FIM/FEM) have been used to study the effect of anodisation on silicon field emitters. Although the effect of anodisation was also investigated using the adapted SEM (see Chapter 7), FIM/FEM studies have been used to confirm that:

i) Anodisation lowers the starting voltage of silicon emitters.

ii) The origin of field emission for anodised tips was the sharp surface fibrils.

The following points are discussed in this chapter:

i) Discussion of main advantages and disadvantages of carrying out experiments in the FIM/FEM, versus the adapted SEM.

ii) Basic operation of the field ion and field emission microscope.

iii) Production and anodisation of silicon FIM tips.

iv) Discussion of results from FIM/FEM and TEM studies, before and after anodisation.

8.2 Advantages/Disadvantages of Field Ion/Field Emission Microscopy

8.2.1 Main Advantages

- In addition to the measurement of field emission current, both field ion and field emission images of the surface could be observed. These images could provide important information about the surface of an emitter. Field ion microscopy is a technique that can be used to study in detail the overall symmetry of the tip end form and tip surface topography (the resolution limit of an FIM is 0.25nm). A FIM image is formed when gas molecules are ionised above prominent atoms on a tip surface held at positive polarity, and an image is formed when ions are attracted to a fluorescent screen. (A further explanation of both FIM and FEM imaging is given in Appendix 1.) Therefore, it should be possible to identify the presence of sharp points (such as porous silicon fibrils) by examining the FIM image. In addition, a field emission microscope can be formed by reversing the polarity of an FIM and removing residual gas. An image is formed when electrons are emitted from the tip surface and hit the fluorescent screen (the resolution

limit of an FEM is less than an FIM, being 2.5nm). In a FEM image, the sharpest conducting points on a tip surface should image first. Comparison of FIM and FEM images from the same tip allows the field emission characteristics to be directly related to the structure of the tip surface. From this comparison, it should be possible to identify the source of emission, thereby determining whether emission occurred from the sharpest points.

- In the FIM/FEM, the specimen-collector separation was known and was kept constant. Therefore, the applied field for a given applied voltage was identical before and after anodisation, and between samples. This was an improvement versus the adapted SEM, where the specimen-collector separation was unknown and could vary slightly before and after anodisation, and between examination of different samples. It was useful to be able to confirm the results obtained in the SEM using a known, fixed specimen-collector separation.

- Field evaporation could be used to smooth the tip surface prior to characterisation. Therefore, the morphology of the tip surface after field evaporation to a given voltage was known and smooth from tip to tip. This was an advantage versus the situation in the adapted SEM where the tip morphology before and after anodisation was unknown and was different from tip to tip.

- Field emission measurements could be obtained under UHV conditions ($\sim 10^{-11}$ torr). This allowed noise and re-contamination of the surface to be reduced, versus that observed in the adapted SEM.

8.2.2 Main Disadvantages

a) Experiments were much more time consuming than those carried out in the adapted SEM. This was because only one tip could be examined at a time. Therefore the number of experiments that could be carried out within the time available was limited.

b) Specimen preparation took much longer than for FEA samples.

c) FIM tips were much more likely to be destroyed during fabrication than for FEA samples.

8.3 Experimental Details

In order to examine the effect of anodisation on the field emission properties of individual silicon tips, and in order to identify the emission source, several steps had to be carried out. These steps are summarised in Figure 8.1.

8.3.1 Fabrication of P^+-Type Silicon FIM Tips

FIM tips were of very different geometry from the FEAs examined in the adapted SEM. FIM tips were typically ~1.5cm long and ~0.5mm square in cross-section. The individual steps required to manufacture silicon FIM tips are listed below:

1) Production of blanks by grinding.
2) Fast polishing to form tapered needle.
3) Slow polishing to produce vanishingly sharp tip.

The experimental details of these individual steps are outlined in Table 8.1. The equipment used to carry out both polishing steps is shown in Figure 8.2 and Figure 8.3.

8.3.2 FIM/FEM Apparatus

A VG FIM 100 atom probe (see Cerezo *et al.* (1984)) was used to carry out both the FIM and FEM analysis. The basic construction of a FEM/FIM is shown in Figure 8.4. The FIM 100 contained three chambers. The vacuum inside the main chamber was 1×10^{-11} torr (i.e. much better than in the SEM). Once a FIM tip sample had been prepared, the sample was inserted into the main chamber ready for FIM/FEM analysis. In order to reach the main chamber, the sample had to pass through both the airlock and the preparation chamber. The preparation chamber could be used to evaporate metals onto the FIM tip surface.

8.3.3 Anodisation of FIM Tips

The same electronic equipment was used to anodise silicon FIM tips, as was used to anodise silicon FEAs. However, FIM tips were anodised by dipping the end of the silicon FIM tip into the electrolyte which was contained in a beaker (similar arrangement to that used for tip polishing in Figure 8.2a).

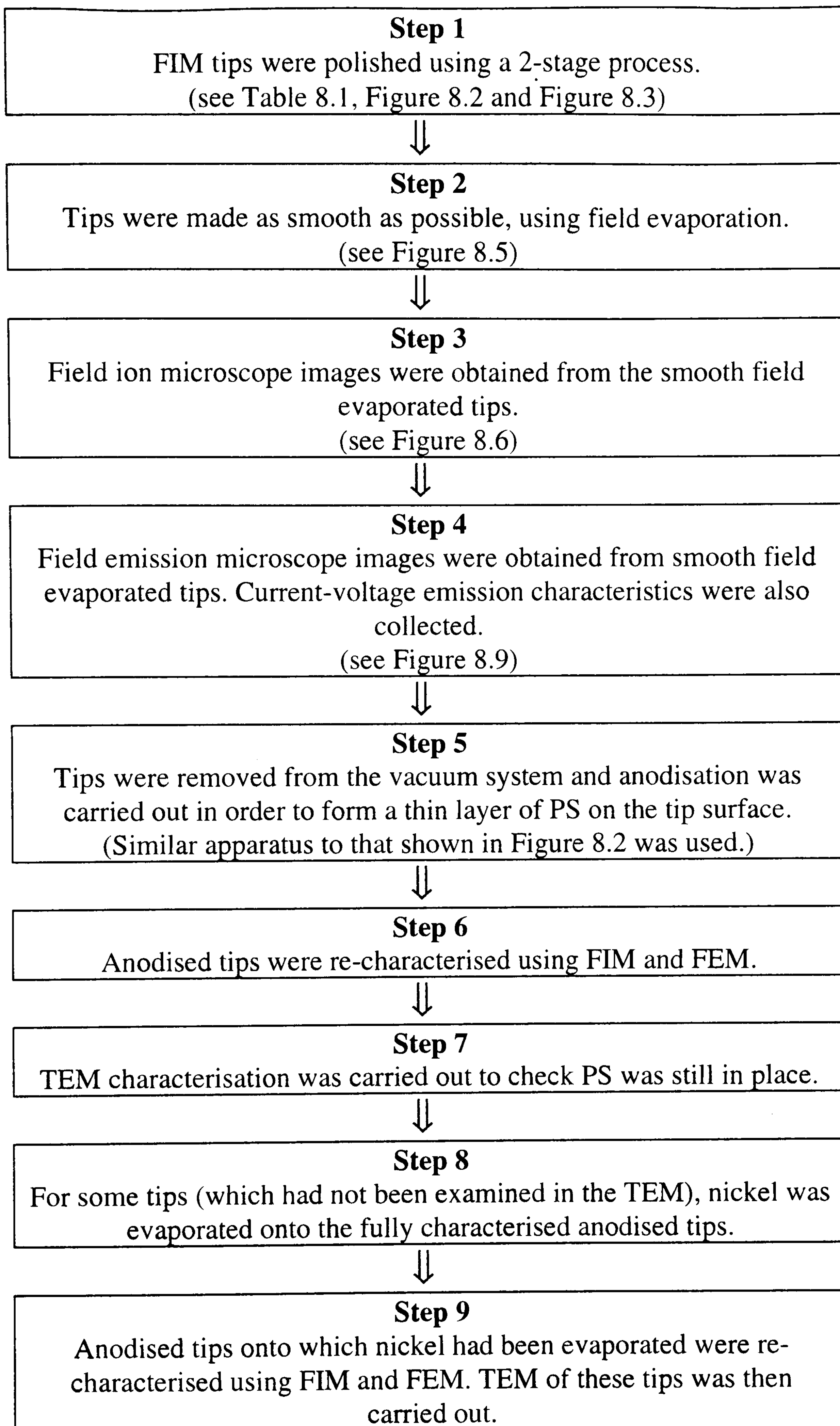
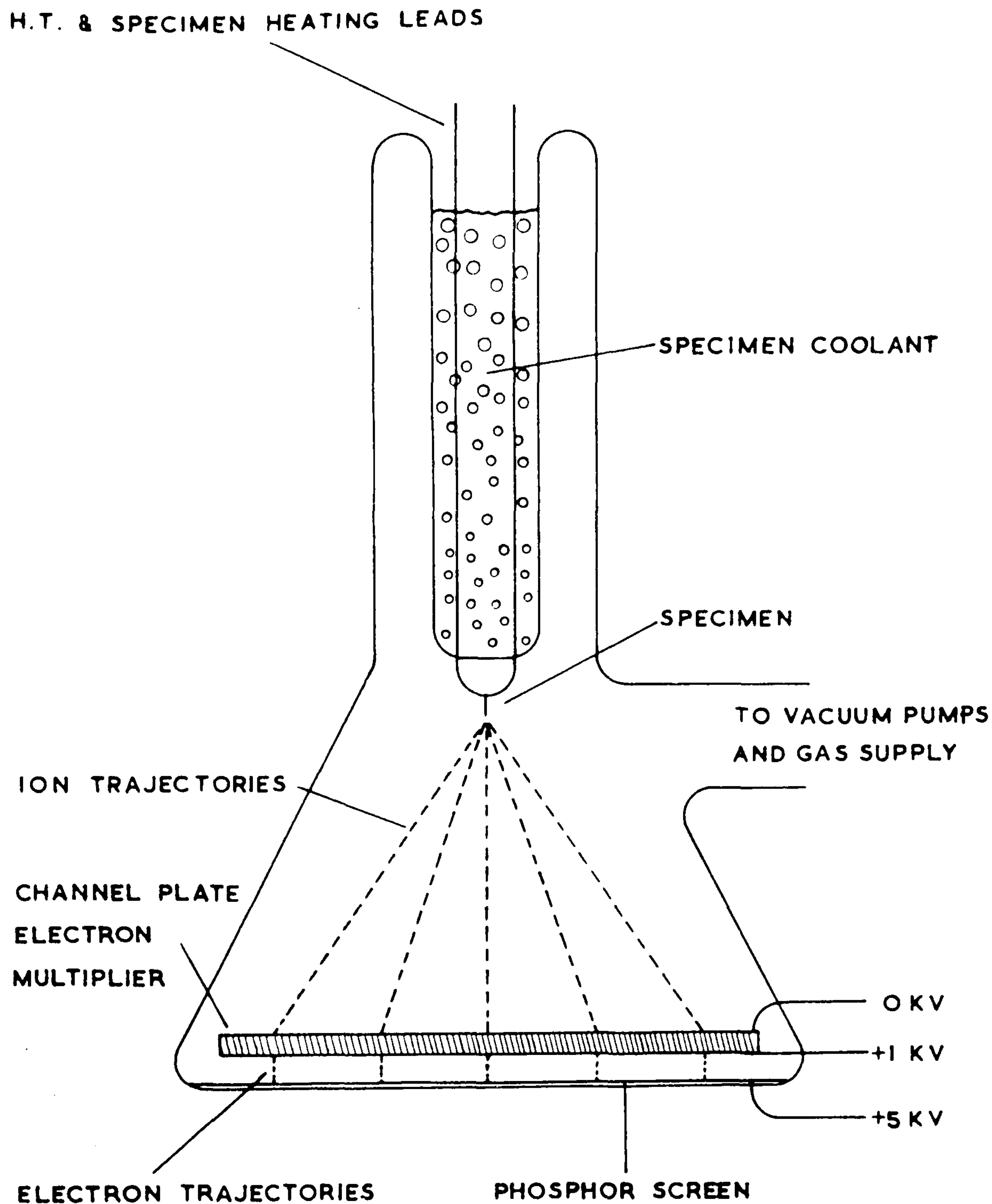


Figure 8.1 Steps Carried Out in Order to Investigate Effect of Anodisation on FIM tips, and to Identify the Source of Emission

Step	Details	Process Issues
1) Production of Blank Silicon Shafts	i) Uniform shafts of silicon ~1 inch long were cleaved from flat silicon wafers. ii) These shafts were ground on a polishing wheel. This was achieved by glueing the shafts of silicon wafer to a glass disc. iii) Grinding was carried out until the shaft was square in cross-section, with the two dimensions of the cross-section having values within ±10μm of each other (as measured by a micrometer).	1) It was found that shafts cut along the axis of the needle parallel to the [110] wafer edge formed apexes which were blade-shaped after the polishing stage. However, those cut at 45° to the [110] direction formed point-like apexes. 2) If the silicon shaft was not square, it was highly likely that a blade-shaped tip would be produced later on, during the final polishing stages.
2) Fast Polishing	i) The blank was immersed in fuming nitric acid, to clean it and to remove any organic material. This formed a thin oxide layer on the surface, which was removed by dipping the shaft into HF for ~10 seconds. ii) A gradually tapered needle was produced from the blank shaft, by electropolishing using the apparatus shown in Figure 8.2. The electrolyte solution was a solution of HNO_3: 40%HF:acetic acid in the ratios 43:42:5. This solution was floated on a denser inert liquid. A gold electrode was used. An a.c. voltage of ~8V was applied, and the tip was lowered in and out of the solution. This up and down movement was continued until the tip formed a neck, and the weight of the lower half became too heavy to be supported by the necked region and so broke in two. The voltage was switched off immediately when this occurred, to prevent tip blunting. iii) The silicon needle was then washed with water and ethanol.	
3) Slow Polishing	After fast polishing, the tip end was still not sharp enough to undergo field evaporation. Slow polishing was required in order to produce a very sharp tip. The apparatus used for this operation is shown in Figure 8.3. A small gold counter electrode loop filled with a drop of electrolyte (HNO_3:40%HF:acetic acid in the ratio 80:15:5) was placed on the specimen stage of a low power (x30) optical microscope, so that fine polishing of the tip could be observed. The specimen was held in a micromanipulator for accurate positioning and was moved until the tip of the silicon needle could be passed through the centre of the electrode ring, without hitting it. Controlled pulses of ~1 second duration were then applied to the tip, as it was moved rapidly in and out of the electrode. The electrolyte had to be regularly refreshed. The aim was to obtain a silicon tip which was vanishingly sharp under the optical microscope, at which stage the tip was sharp enough to undergo field evaporation. This polishing stage could also be used for repolishing tips which had flashed during the later field evaporation process.	1) The production of blade-shaped specimens was undesirable, because they were likely to 'flash' during the field evaporation process. Unfortunately it was quite common to produce a blade-shaped tip. 2) P^+-type tips required a higher voltage to polish than n-type tips. 3) The slow polishing stage was particularly difficult if the specimen was blade-shaped, because it tended to crumble before a sharp tip was formed.

Table 8.1 Processes Required for Production of Smooth Uniform Tips by Etching



(Ref: M.K.Miller & G.D.W.Smith, "Atom Probe Microanalysis: Principles and Applications to Materials Problems, (Materials Research Society, 1989)

Figure 8.4 - Basic Construction of Field-Ion / Field Emission Microscope

A field ion / field emission microscope consists of a vacuum tube with a needle-like specimen at one end mounted along its axis. Approximately 10cm away at the opposite end, is a fluorescent screen and a channel plate electron multiplier of ~7.5cm in diameter. The channel plate acts as an ion/electron image converter and intensifier. The specimen is mounted on an electrical insulator so that it can be taken up to a high voltage. It is kept at cryogenic temperatures, by mounting it on a 'cold-finger' cryostat.

For FIM studies, the specimen was made positive; whereas for FEM studies, the specimen was made negative.

Due to the voltage drop along the length of the FIM tip, and the low conductivity of p-type silicon (10Ωcm), it was not believed that a p-type FIM tip could be anodised at the tip end. For this reason, only p^+-type (0.01Ωcm) FIM tips were anodised. Calculation showed that only 1mA current needed to flow to the tip (if ~5mm of FIM tip was dipped into the electrolyte), in order to obtain a current density of $100mAcm^{-2}$, at the tip surface. This was due to the unusual geometry of FIM tips. However, one problem when anodising FIM tips, was that it was difficult to ensure that the same tip surface area came in contact with the electrolyte, from tip to tip. This must have caused variations in the value of applied current density from tip to tip. As the morphology and thickness of PS layers depend on the anodisation current density, this situation was not ideal.

8.4 TEM Examination of FIM Tips

A 200CX TEM microscope was used to examine the morphology of FIM tips before and after anodisation. After field evaporation, FIM tips were thin enough to allow electrons to pass straight through the tip end. No further sample preparation was necessary. However, a special attachment had to be used to hold the FIM tip in place, see Warren (1993). The FIM tip was held in place by a screw and the attachment was slipped into a bulk specimen holder, usually used for STEM work.

8.5 Characteristics of P^+-type Silicon Tips Before Anodisation

8.5.1 Field Evaporation and Field Ion Microscopy

Field evaporation in argon was carried out in order to produce a smooth tip surface. Field evaporation is a process by which prominent atoms are removed from a rough tip, leaving behind a smooth surface (see Appendix 1). The steps that had to be carried out in order to field evaporate a tip are outlined in Figure 8.5. Results from tips of different geometriy are summarised below:

a) Symmetrical Point-like Tips

At 7.7kV, symmetrical point-like tips produced a bright image on the screen. This image did not contain any detail - it appeared fogged out. However, on lowering the tip voltage slightly,

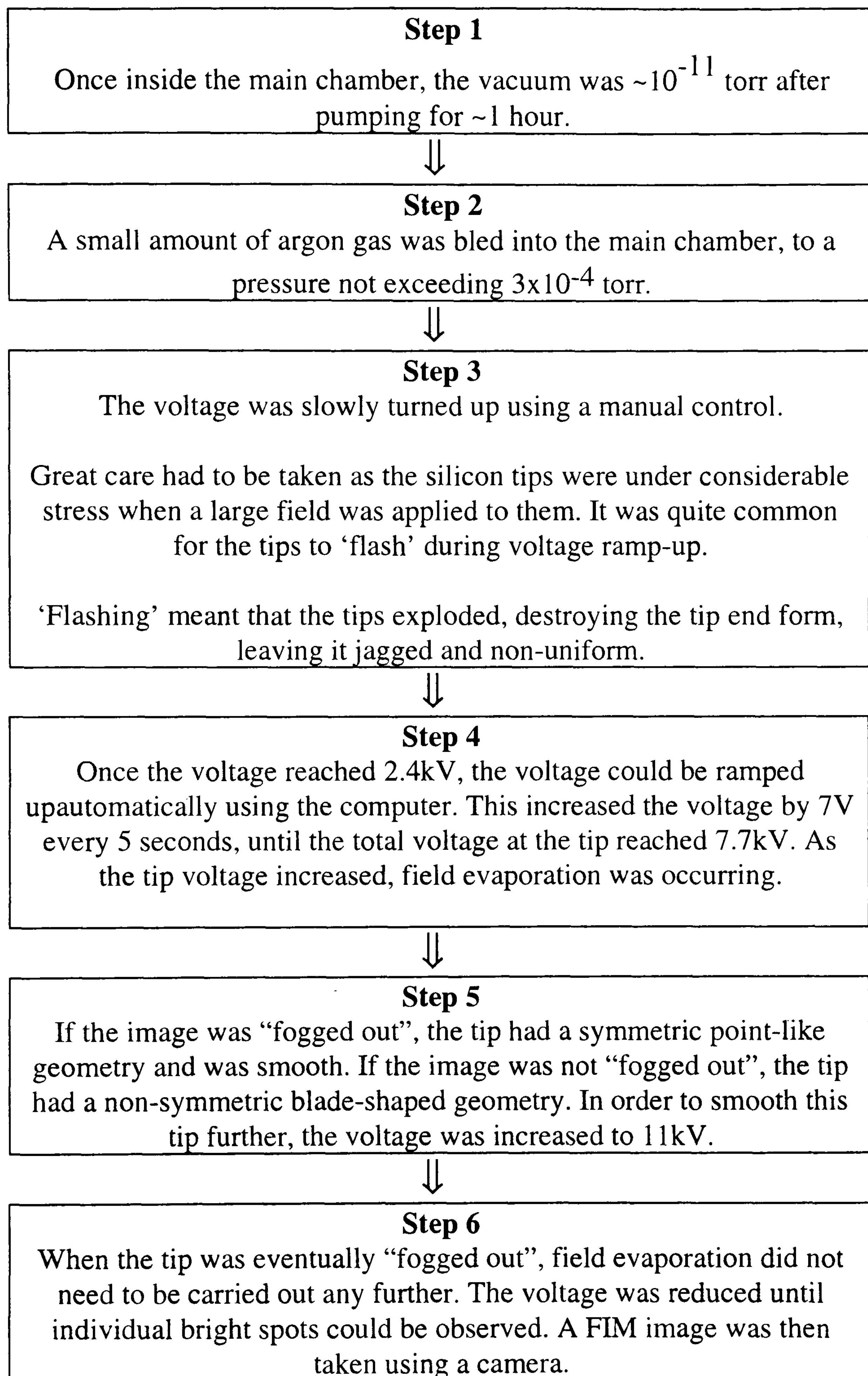


Figure 8.5 Process of Field Evaporation and Field Ion Imaging

the FIM image could be seen to contain a uniform distribution of small spots, see Figure 8.6a. All tips which were fogged out at 7.7kV produced images which were similar.

b) Non-Symmetric Blade-Shaped Tips

Some tips did not exhibit a fogged out image at 7.7kV. Instead, some detail could still be observed within the image. An example is shown in Figure 8.8a. The distribution of spots is less uniform, exhibiting streaks across the image. Such images were formed if the tip apex had a blade-shaped geometry, rather than a symmetric point-like geometry. However, subsequent field evaporation to 11kV usually improved the FIM image uniformity.

8.5.2 Transmission Electron Microscopy of FIM Specimens

TEM studies show that after simple electropolishing, the FIM tip end was non-uniform. However, field evaporation made the tip smooth and uniform.

a) Symmetrical Point-like Tips

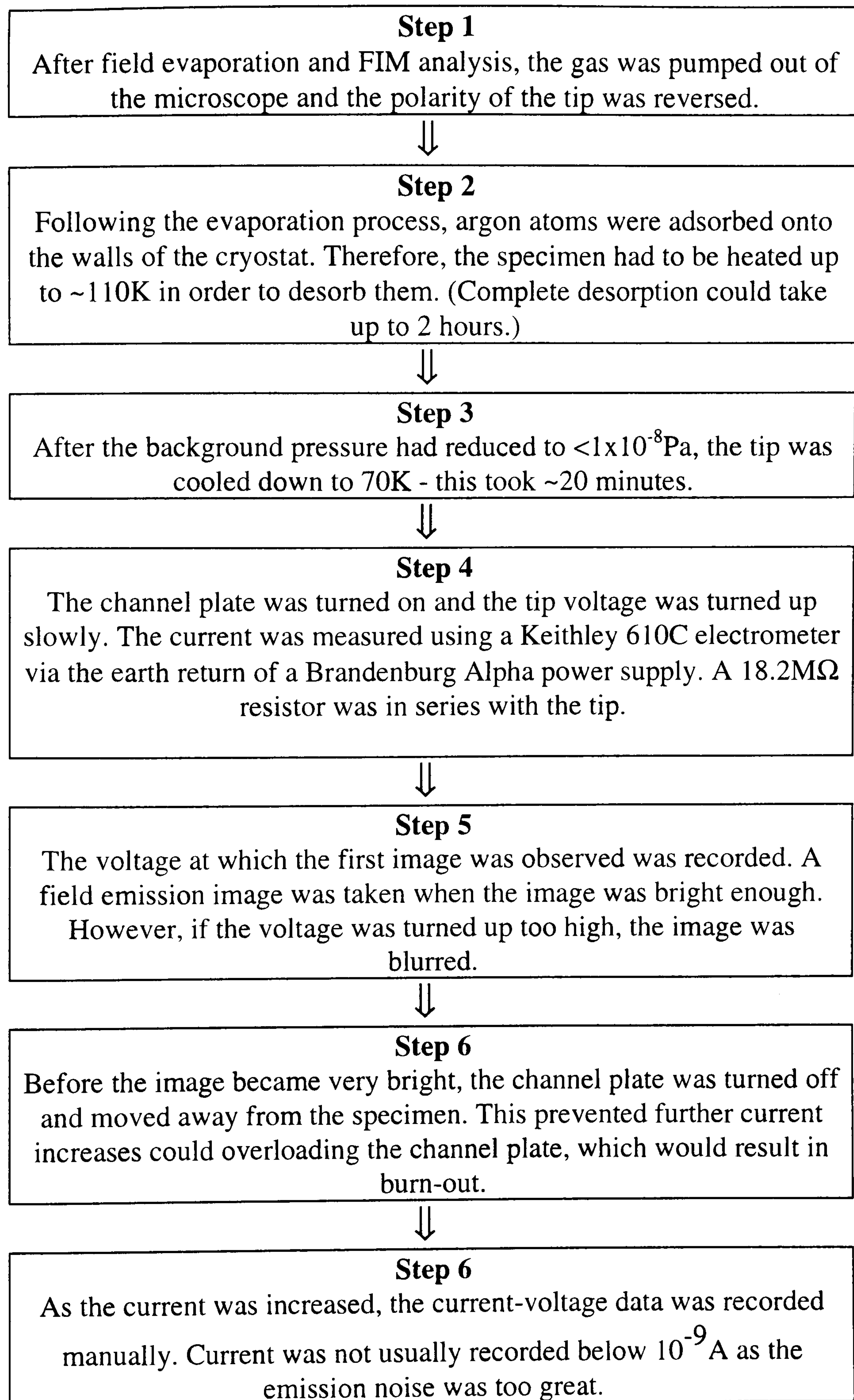
All tips which were fogged out at 7.7kV had tip radii similar to that shown in Figure 8.7 (i.e. ~100nm). The tip end is very smooth.

b) Non-Symmetric Blade-Shaped Tips

These tips had a wider range of tip radii and geometry. Figure 8.8d) and 8.8e) show TEM images of a tip which had to be ramped to 11kV, before the FIM image was totally fogged-out. In d), the tip is ~700nm in radius. However, when this tip was rotated through 90°, the tip radius was only 0.1µm, due to the blade-like geometry of these tips. Although the tips are not symmetrical, they are smooth.

8.5.3 Field Emission Microscopy

After complete removal of the Ar gas and reversal of the tip polarity, field emission microscope (FEM) images could be taken. The field emission characteristics of tips were recorded at 70K, under a pressure less than 1×10^{-11} torr. Figure 8.9 explains the process for FEM characterisation and explains how I-V measurements were collected. Figures 8.6b) and 8.6c) show FEM images taken at ~1kV, before and after emission. Note the uniform



(For further details, see King (1996).)

Figure 8.9 Process of Field Emission Imaging and Current-Voltage Characterisation

distribution of small spots. Figure 8.8c) shows a FEM image from a blade-shaped emitter - this image is less uniform.

8.5.4 Field Emission Characteristics

Emission was much more stable than in the adapted SEM. Fowler-Nordheim (FN) plots were obtained from a number of tips, following evaporation to a range of voltages. An analysis of the FN plots is summarised in Table 8.2.

a) Point-like Tips

For all tips fully fogged out at 7.7kV, starting voltage (defined as voltage required to obtain 10^{-9}A of current) was very similar from tip to tip. The mean starting voltage was 1.11kV. In addition, the slope and intercept of the FN plots were very similar from tip to tip. Calculation (using equation 2.16 in Chapter 2) showed that the mean emission radius was ~1.17×10^{-7}m. This value of radius was very similar to that observed during TEM examination of field-evaporated point-like tips.

b) Blade-Shaped Tips

Tips which were not fully fogged out at 7.7kV had higher starting voltages. The mean starting voltage for such tips was 1.62kV (i.e.~45% higher than for those fogged out at to 7.7kV), indicating that the tips were blunter. The mean FN slope was ~27% higher than for tips fully fogged out at 7.7kV, indicating that the field enhancement factor of these tips was lower. The calculated values of tip radii and FN slope were much more scattered than for tips fully fogged out at 7.7kV. However, all blade-shaped tips had smooth surfaces following field evaporation.

Ideally, it would have been preferable to use only uniform tips fully fogged out at 7.7kV during these experiments. However, in reality, tips evaporated to 11kV had to be used due to limitations of time and equipment.

a) Uniform Tips evaporated to 7.7kV

Tip Number	Starting Voltage (to collect 10^{-9}A)	Fowler-Nordheim Slope	Fowler-Nordheim Intercept	Estimated Emitting Radius
1(27/2/95)	1.12kV	-25,180	-12.530	1.23×10^{-7}m
2(21/2/95)	1.14kV	-24,840	-12.730	1.09×10^{-7}m
3(16/2/95)	1.12kV	-24,540	-12.730	1.08×10^{-7}m
4(28/10/94)	1.18kV	-26,280	-12.540	1.27×10^{-7}m
5(28/10/94)	1.16kV	-23,630	-12.510	1.17×10^{-7}m
6(20/10/94)	1.10kV	-24,990	-12.510	1.04×10^{-7}m
7(20/1/94)	1.00kV	-24,350	-12.510	1.11×10^{-7}m
8(16/9/94)	1.07kV	-24,110	-12.490	1.15×10^{-7}m
Mean Value	1.11kV	-24,740	-12.570	1.14×10^{-7}m $\pm0.07\times10^{-7}$m

b) Blade-Shaped Tips evaporated to 9kV

Tip Number	Starting Voltage (to collect 10^{-9}A)	Fowler-Nordheim Slope	Fowler-Nordheim Intercept	Estimated Emitting Radius
1(12/2/95)	1.43kV	-30,630	-13.740	0.82×10^{-7}m

c) Blade-Shaped Tips evaporated to 11kV

Tip Number	Starting Voltage (to collect 10^{-9}A)	Fowler-Nordheim Slope	Fowler-Nordheim Intercept	Estimated Emitting Radius
1 (16/3/95)	2.04kV	-32,940	-13.140	1.86×10^{-7}m
2 (3/5/95)	1.35kV	-19,820	-17.780	6.99×10^{-9}m
3 (18/5/95)	1.63kV	-31,790	-14.790	5.01×10^{-8}m
4 (16/6/95)	1.37kV	-34,920	-15.740	3.42×10^{-8}m
5 (16/6/95)	1.54kV	-19,200	-17.570	7.5×10^{-9}m
6 (22/6/95)	1.72kV	-37,210	-12.940	1.48×10^{-7}m
7 (14/8/95)	1.66kV	-37,180	-13.560	1.08×10^{-7}m
8 (12/11/94)	1.71kV	-36,220	-12.960	1.42×10^{-7}m
9 (28/10/94)	1.53kV	-34,910	-12.110	2.03×10^{-7}m
Mean Value	1.62kV	-31,580	-14.510	0.88×10^{-7}m $\pm0.72\times10^{-7}$m

d) Blade Shaped Tips Field Evaporated to 12kV

Tip Number	Starting Voltage (to collect 10^{-9}A)	Fowler-Nordheim Slope	Fowler-Nordheim Intercept	Estimated Emitting Radius
1(28/1/95)	1.67kV	-36,370	-13.420	1.34×10^{-7}m

e) Blade Shaped Tips Field Evaporated to 13kV

Tip Number	Starting Voltage (to collect 10^{-9}A)	Fowler-Nordheim Slope	Fowler-Nordheim Intercept	Estimated Emitting Radius
1(15/7/95)	1.73kV	-42,430	-12.240	2.39×10^{-7}m
2(7/10/94)	1.68kV	-39,740	-13.050	2.13×10^{-7}m

Table 8.2 - Summary of Field Emission Characteristics for P^+ Type Silicon FIM Tips Evaporated to Different Voltages

8.6 Characteristics of Silicon Tips Following Anodisation

After field evaporation and subsequent characterisation, tips were removed from the FIM/FEM vacuum system and a thin layer of PS was formed on the FIM tip surface by anodisation. The modified tips were then re-characterised in both FEM and FIM mode. The results are discussed below.

8.6.1 PS Morphology Following Anodisation

Figure 8.10 shows a TEM micrograph of an anodised FIM tip. TEM examination showed that it was possible to anodise a FIM tip without damaging the tip itself or altering its overall geometry. Table 8.3 summarises the TEM results from examining tips anodised for different times. In Table 8.4, the morphology of anodised FIM tips has been compared to the morphology of anodised FEA tips:

a) Similarities versus PS Morphology at Anodised P^+-Type FEA Tips

- There is a high density of fibrils at the tip surface, see Figure 8.11.
- The pores have a honeycomb structure.
- The PS morphology is not affected by anodisation time.
- A core can be observed within the PS layer. This core has approximately the same geometry as the original tip, but also depended on anodisation time, see Figure 8.12. Figure 8.12c) shows the silicon core protruding from the centre of the PS layer (which has been damaged). It can be seen that the core is rough (Figure 8.12d)).

b) Differences versus PS Morphology of Anodised P^+-Type FEA Tips

- The fibrils at the surface of anodised FIM tips have higher aspect ratios than the fibrils at the surface of anodised FEA tips - the fibrils are almost 10 times longer, see Table 8.4. While some fibrils stand vertically proud of the tip surface, others are bent over and lie across the tip surface.
- The average pore size for anodised FIM tips is twice that for anodised FEA tips, i.e. the structure is much more open, see Figure 8.11a).
- The PS layer at the tip apex is thicker than for FEA tips anodised for the same time, see Figure 8.12b).

Anodisation Time (Seconds)	**Applied Current**	**Porous Silicon Layer Thickness up Sides**	**Porous Silicon Layer Thickness at Tip**
0.5	1mA	0.1μm	1.0μm
1	2mA	2.5μm	5μm
2	1mA	0.6μm	2.0μm
5	1mA	5.0μm	not possible to measure
10	1mA	1.6μm	8μm

The results shown in this table suggest that the current density at the FIM tip surface was not identical from tip to tip (for same applied current), as the porous silicon thickness is not quite proportional to anodisation time. This is not surprising, as it was difficult to maintain the same tip surface area in contact with the electrolyte, from tip to tip.

Table 8.3 Thickness of Porous Silicon Layer at Anodised FIM Tip Surface (for Various Anodisation Times)

	Pore Width	**Fibril Width**	**Fibril Height**
At anodised FIM tip	30-50nm	~5nm	up to 100nm
At anodised FEA tip	~20nm	~5nm	5-10nm

Table 8.4 Comparison of Porous Silicon Morphology at Anodised FIM Tips and FEA Tips

- The PS layer is up to 5 times thicker at the tip than up the emitter sides, see Table 8.3. For anodised FEA tips, the PS layer was only slightly thicker than up the emitter sides.

8.6.2 Robustness of Porous Silicon Layers

The anodised FIM tips appeared to be more fragile than anodised FEA tips. The highest current obtained from anodised FIM tips (before destruction) was in general lower than obtained from anodised FEA tips. In fact, half the anodised FIM tips blew at emission currents lower than 1nA (regardless of anodisation time). When an anodised FIM tip blew, the PS layer was completely stripped away at the apex, leaving only the silicon core. However, there were traces of residual PS much further down the FIM tip shaft.

One possible reason that the anodised FIM tips blew at low current values could be due to the differences in the PS morphology between anodised FIM and FEA tips. This difference may have caused the PS formed on FIM tips to be less thermally stable.

8.6.3 Dependence of Stability on Porous Silicon Layer Thickness

Anodisation was carried out for both 0.25 seconds and for 5 seconds. Emission characteristics collected from tips anodised for these times are summarised in Table 8.5 and 8.6. The emission behaviour of tips anodised for these times was very different:

- Emission from tips anodised for 5 seconds was very unstable compared to samples anodised for only 0.25 seconds. The field emission current obtained from these tips was uncontrollable and increased, with very little increase in the applied voltage. A typical example is as follows. For one tip, a FIM spot appeared as the voltage was ramped up from zero. Suddenly at an applied voltage of 800V, the emission current jumped in value from 1nA to almost 100nA, without any corresponding increase in the applied voltage. The applied voltage had to be turned down quickly to 520V in order to prevent damage to the channel plate. However, the spot still had the same intensity as at 800V. Shortly afterwards, the tip failed without any further increase in the applied voltage. In contrast, field emission from tips anodised for only 0.25 seconds was controllable - there were no sudden increases in current, unless the voltage was increased.

Tip Number	Max I	Lowest voltage at which FIM image observed		Lowest voltage at which FEM image observed		Starting voltage (to obtain 10^{-9} A)		Fowler-Nordheim Plot Slope		Fowler-Nordheim Plot Intercept	
		Before	**After**	**Before**	**After**	**Before**	**After**	**Before**	**After**	**Before**	**After**
5/2/95	6μA	7kV	1.6kV	780V	470V (↓40%)	1670V	900V (↓46%)	-36,370	-14,950 (↓59%)	-14,950	-17.400
16/3/95	n/a	6.2kV	1.3kV	1100V	380V (↓66%)	1520V	1010V (↓33%)	-32,940	n/a	-13.140	n/a
18/5/95	not known	6.7kV	1.5kV	1160V	700V (↓40%)	1750V	not known	-31,790	not known	-14.790	not known
4/6/95	n/a	6kV	2kV	1100V	n/a	1480V	n/a	-34,920	n/a	-15.740	n/a
6/6/95	n/a	6.3kV	1.9kV	1130V	n/a	1510V	n/a	-35,100	n/a	-12.950	n/a
22/6/95	0.1μA @	6.5kV	2.3kV	1200V	650V (↓46%)	1700V	1300V (↓24%)	-37,210	-21,400 (↓33%)	-12.940	-18.07
15/7/95	n/a	7.6kV	2.5kV	1300V	660V (↓50%)	1850V	n/a	-42,430	n/a	-12.240	n/a
Mean Value	-	6.6kV	1.9kV (↓72%)	1110V	570V (↓48%)	1640V	1070V (↓35%)	-35,820	-18,170 (↓50%)	-13.820	-17.740

Before = Value prior to anodisation; After = Value after anodisation
n/a = tip blew before this value could be obtained
Max I = maximum current reached before FIM tip blew and was destroyed
@ = was not tested to destruction
↓ = decrease in value by x%, relative to value prior to anodisation

Table 8.5 Field Emission Results from Anodised P^+-Type Silicon FIM Tips Short Anodisation Time - 0.25 seconds at 1mA

Tip Number	Max I	Lowest voltage at which FIM image observed		Lowest voltage at which FEM image observed		Starting Voltage (to obtain 10^{-9}A)	
		Before	**After**	**Before**	**After**	**Before**	**After**
11/10/94	5μA	5.5kV	not known	800V	500V	1300V	980V
20/10/94	0.1μA	5.2kV	not known	1090V	560V (↓49%)	1200V	680V (↓32%)
20/10/94	0.2μA	6kV	not known	940V	460V (↓52%)	1000V	600V (↓4%)
3/12/94	0.1nA	5.5kV	not known	1050V	500V (↓53%)	1100V	n/a
16/2/95	n/a	5.4kV	2kV (↓63%)	830V	n/a	1200V	n/a
21/2/95	n/a	4.8kV	3.12kV (↓35%)	800V	n/a	1100V	n/a
Mean Value	-	5.4kV	2.56V (↓53%)	920V	510V (↓45%)	1150V	750V (↓35%)

Note: These tips were anodised for 5 seconds, i.e. 4 times longer than for the previous samples summarised in Table 8.5. Their emission was poor and very unstable - although they exhibited FIM images at lower voltages after anodisation, they typically blew when any attempt was made to extract a field emission current from them.

Before = Value prior to anodisation; After = Value after anodisation
n/a = tip blew before this value could be obtained
Max I = maximum current reached before FIM tip blew and was destroyed
↓ = decrease in value by x%, relative to value prior to anodisation

Table 8.6 Field Emission Results from Anodised P^{+} Type Silicon FIM Tips Much Longer Anodisation Time - 5 Seconds at 1mA

- Very few data points could be collected from tips anodised for 5 seconds, prior to failure. Therefore, the resulting Fowler-Nordheim and current-voltage plots were very irregular, see Figure 8.13. In contrast, field emission from tips anodised for ~0.25 seconds produced regular straight Fowler-Nordheim plots, see Figure 8.14.

The fact that thicker PS layers are less stable than thinner layers is similar to the results obtained in the adapted SEM. As suggested in Chapter 7, thicker PS layers would have higher resistance than thin PS layers. Field emission from these thicker layers may have caused overheating of the tip, resulting in thermal run-away.

8.6.4 Confirmation that Anodisation Lowered Starting Voltage

- The mean starting voltage for field emission from anodised emitters was ~35% lower than before anodisation.

- The first FEM image was obtained at a voltage ~48% lower following anodisation.

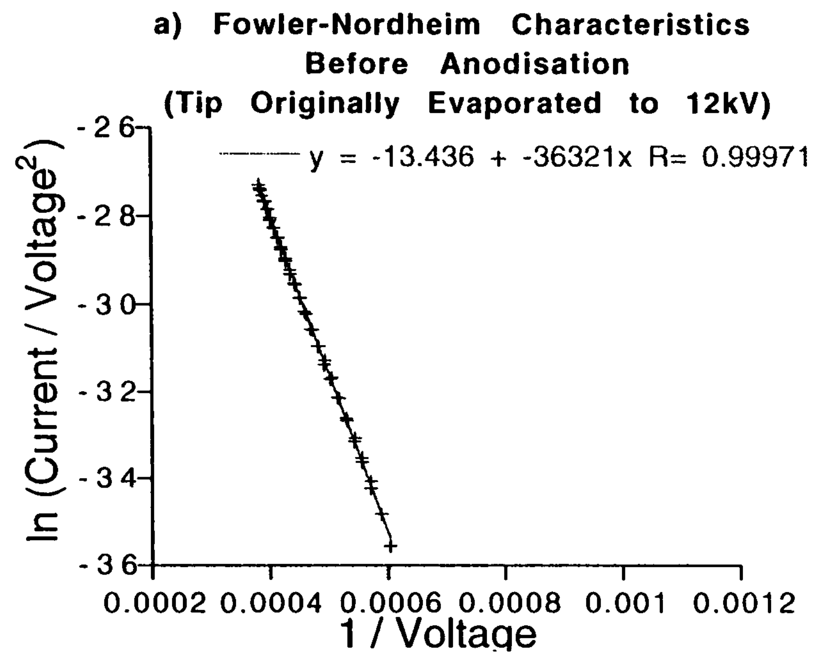
These results confirm the result obtained in the adapted SEM, that the starting voltage was found to be lowered by 30-60% (although the height of the fibrils was different).

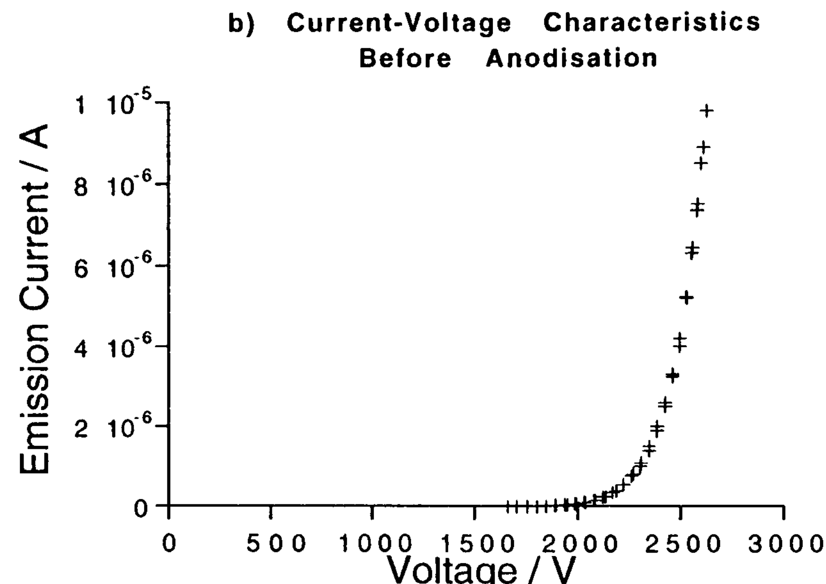
8.6.5 Evidence for Emission from Sharp Points of High Field Enhancement

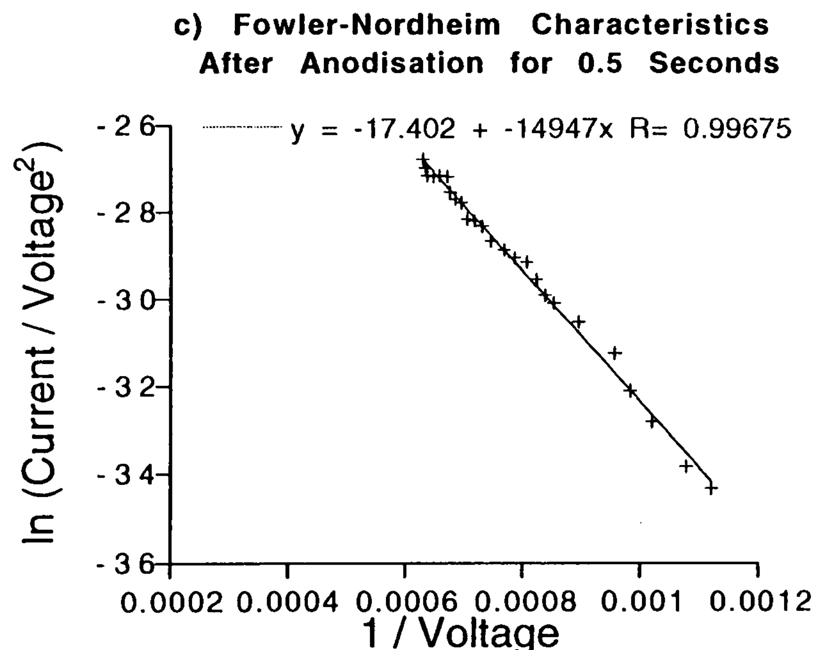
Examining the more stable data obtained from tips anodised for just 0.25 seconds (summarised in Table 9.4), and the FEM/FIM images from anodised tips shown in Figure 8.15, the main results were as follows:

- The first FIM image spots were obtained at a voltage ~72% lower than before anodisation. The FIM spots were also larger following anodisation. This suggests that very sharp points were present on the emitter surface, following anodisation.

- Size of FEM spots was larger following anodisation. If emission had occurred from sharp points of small radius on the emitter surface, it would be expected that larger FEM spots







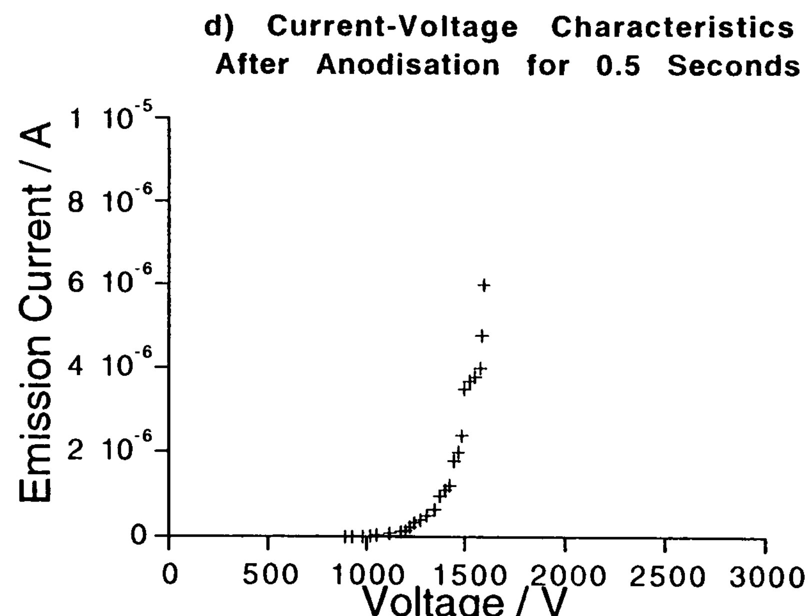


Figure 8.14 - Field Emission Before & After Anodisation for 0.25 Seconds (i.e. Formation of Thin Porous Silicon Layer on Tip Surface) (Corresponds to FEM image of Tip 2 Shown in Figure 8.15) - Note that for this thinner porous silicon layer, the Fowler-Nordheim plot is a straight line before and after anodisation, and emitter did not blow until it was within the μA range.

would have been produced. Therefore, these results indicate that after anodisation, emission occurred from small points.

- Following anodisation, the slopes of the Fowler-Nordheim plots were ~ 50% lower.

These results indicate that the emission voltage was lowered due to the presence of sharp points having high field enhancement. However, the experiments did not show whether these points were present at the tip surface, or whether they were at the sharp interface between the PS and bulk silicon.

8.7 Control Experiment

8.7.1 Aim of Experiment

The purpose of this experiment was to carry out a control experiment. In the control experiment, some tips were taken through the same procedure as for anodised tips, but when dipping into the electrolyte, no current was applied. This procedure was carried out in order to expose tips to the same chemicals as the anodised tips, but to prevent the formation of a surface PS layer. There was a concern that the decrease in starting voltage observed for anodised FIM tips was actually the result of a native oxide layer (formed when tips were removed from the vacuum to carry out anodisation, exposing them to air), rather being due to the presence of sharp PS fibrils at the tip surface. King *et al.* (1994) studied silicon tips which had been exposed to air, following field evaporation. They found that the irregularity of oxidised tips lowered the emission voltage by 50% compared to clean field evaporated silicon. The control experiment was carried out in order to eliminate the possibility that the decrease in starting voltage in this work was due to a rough oxide layer. If the non-anodised tips had displayed identical characteristics to those of the anodised tips, this would have been cause for concern.

8.7.2 Results

Five control tips were examined and the results are summarised in Table 8.7. The voltage at which FEM images were obtained did decrease after being dipped into the electrolyte. However, the emission characteristics were completely different from those obtained from

Sample Number	FEM before anodisation	FEM after anodisation	Starting Voltage before anodisation	Starting Voltage after anodisation	Maximum current obtained
1) 20/10/94	900V	280V (lowered by 69%)	1200V	n/a	10^{-10}A at 340V
2) 3/11/94	700V	640V (lowered by 9%)	1160V	n/a	$<10^{-10}$A at 720V
3) 3/11/94	1400V	480V (lowered by 66%)	1600V	n/a	$<10^{-10}$A at 800V
4) 12/11/94	1100V	750V (lowered by 32%)	1600V	1200V (-25%)	$<2\times10^{-8}$A at 1316V
5) 18/11/94	700V	700V (no change)	900V	1000V (+11%)	$<2\times10^{-8}$A at 1260V

n/a = tip blew before current reading could be taken

Table 8.7 Control Tips

Tips were given the same treatment as for anodised tips, but current was not applied when dipping into the anodisation solution. Therefore, no porous silicon was formed at the tip surface.

anodised tips. Emission from the control tips was extremely short-lived and virtually no emission current was obtained from these tips, prior to tip self-destruction occurring (no emission current $>10^{-8}$A was obtained). FEM images obtained from control tips were very unstable and non-localised - they appeared as "sheet-lightening", with spots continuously skipping over the channel plate. Anodised tips were much more stable than control tips and in addition, much higher currents could be extracted from these tips, before destruction.

8.7.3 Summary

The conclusion from the control experiments is that the emission characteristics of anodised FIM tips cannot be a result of oxidation during exposure to air only.

8.8 Identification of Surface Fibrils as Emission Source

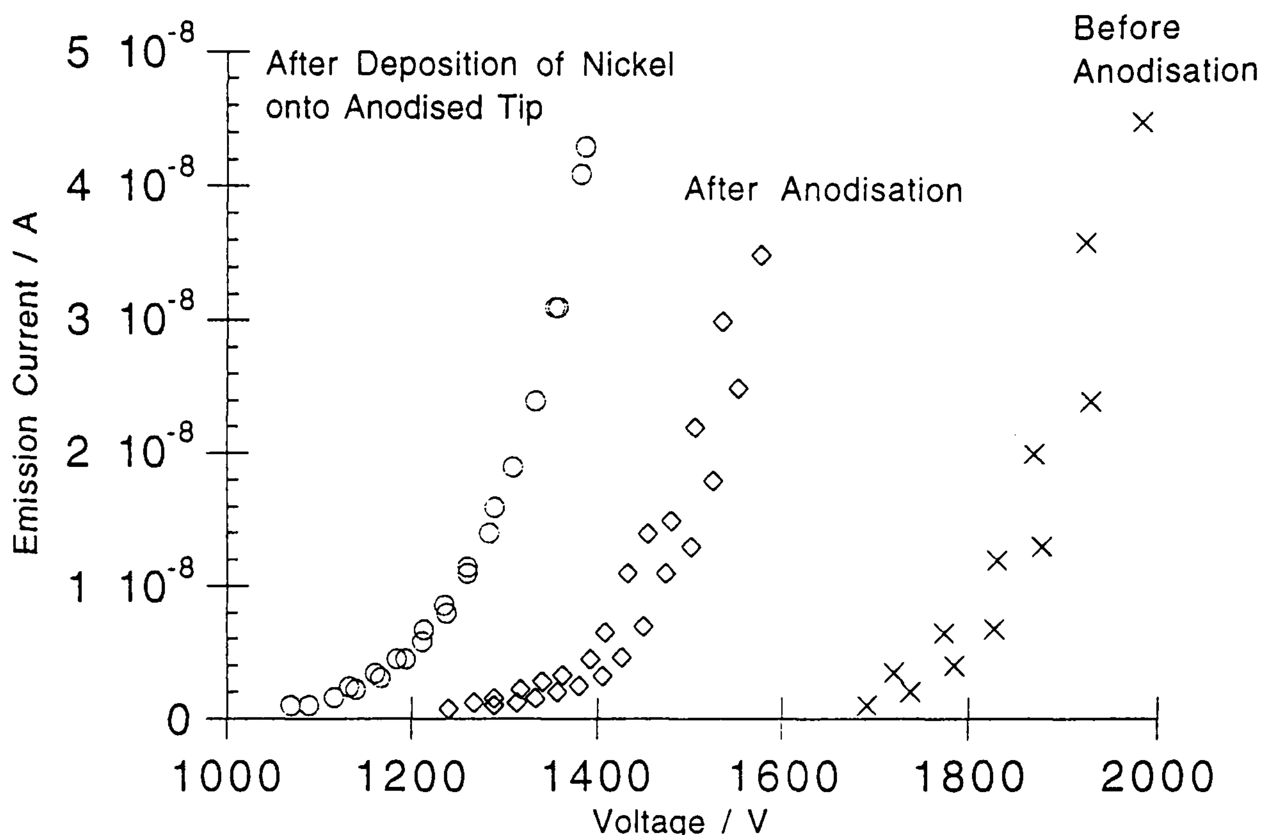
8.8.1 Emission from Anodised Surfaces - FIM/FEM Image Correlation

Figure 8.16 and Figure 8.17 show FIM and FEM images taken before and after anodisation for 0.25 seconds, respectively. Figure 8.20 shows a TEM image of the tip confirming that the PS layer was still intact following characterisation (and evaporation of nickel). Figure 8.17 shows that there is good correlation between the FIM and FEM image. The brightest spots in the FEM image correspond to the brightest spots in the FIM image.

Spots within a FIM image only originate at the tip surface. Therefore, as the FIM spots correlate well with the position of the FEM spots, it follows that the FEM spots must also have originated at the tip surface. If electron emission had occurred from the PS/bulk silicon interface located below the emitter surface instead, this correlation would not have been expected. Instead, the FEM spots might have been expected to be much more diffuse, due to scattering of the emitted electrons as they crossed the porous silicon layer. Therefore, these results indicate that field emission occurred from the surface of the PS layer and hence the PS fibrils, rather than elsewhere.

8.8.2 Correlation between FIM/FEM Images from Anodised Surfaces

A further experiment was carried out in order to confirm that the sharp surface fibrils were the source of emission. The idea behind this experiment was as follows. Assuming that field



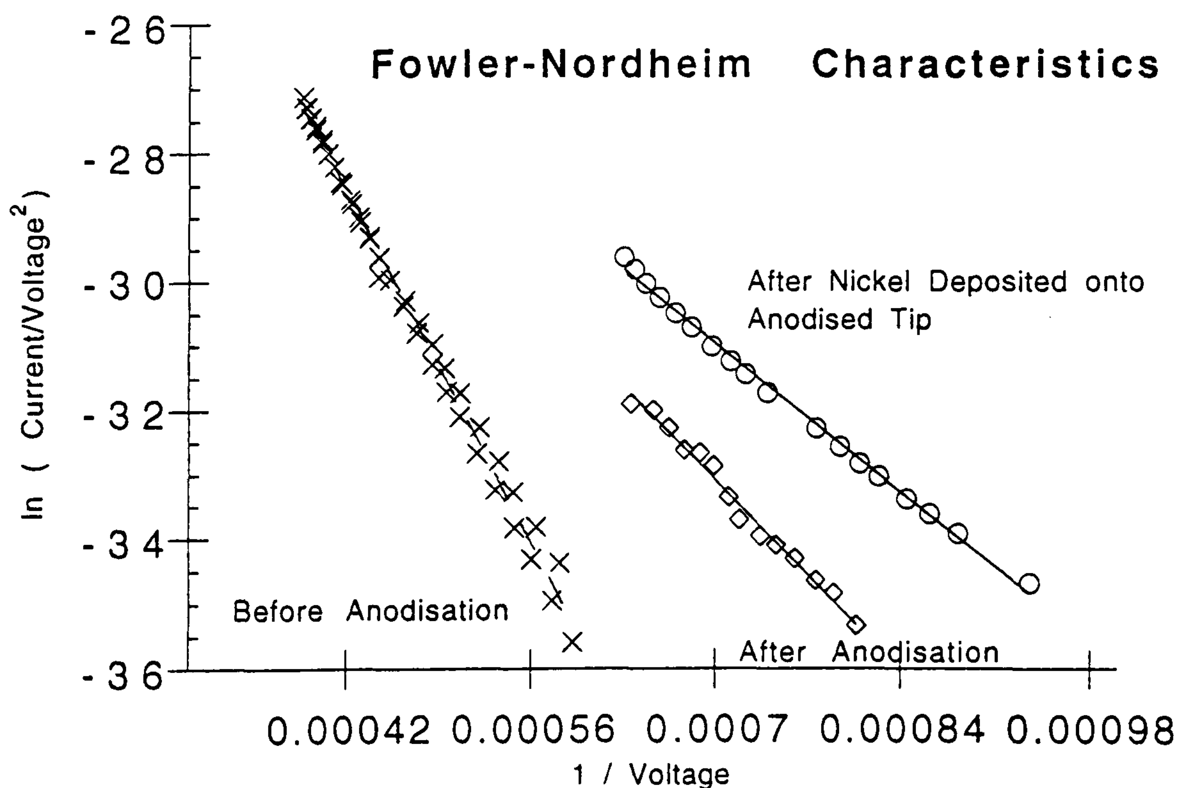


Figure 8.18 - Characteristics Before and After Anodisation and After Deposition of Nickel onto Anodised Tip (for Tip Used to Study Origin of Field Emission from Porous Silicon)

emission occurred at the PS surface fibrils, then if a thin metal layer was deposited onto a PS FIM tip, emission should still occur at the same points as prior to deposition. This should therefore give further proof that emission originated at the PS surface, rather than at the sharp PS/silicon interface.

This theory was tested by evaporating a thin layer of nickel onto the surface of an anodised tip (tip had already been characterised). Evaporation was carried out under UHV conditions in the microscope preparation chamber, using an electron beam heated evaporation source. After evaporation, the tip was re-characterised (FIM, FEM and I-V characterisation).

a) Correlation of FIM/FEM Images Before and After Nickel Deposition

The FEM and FIM images after deposition of nickel are shown in Figure 8.19. These images are very similar to the corresponding images of the tip obtained prior to nickel deposition, also see Figure 8.17. This indicates that after nickel was evaporated, emission still occurred from the same sites. If emission had occurred from a buried interface, the good correlation between the FIM and FEM images before nickel deposition and with FEM images before and after nickel deposition would not have been expected. Therefore it is concluded that the source of field emission from anodised emitters was the sharp surface fibrils present at the tip surface.

b) Comparison of Field Emission Data Before and After Nickel Deposition

Emission characteristics before and after nickel deposition are summarised in Table 8.8. Figure 8.18 compares the FN plots obtained before and after nickel deposition and before anodisation. The emission characteristics were similar to those obtained prior to nickel deposition, although some improvement in emission properties did occur. The starting voltage was ~15% lower than immediately after anodisation and the slope of the FN plot was lower by ~25%. These results suggest that either some sharpening of the emission sites occurred, or that the work function was lowered. (Note that if the work function was lowered after deposition of nickel onto the porous silicon layer (rather than an increase in enhancement factor), the work function of the porous silicon must have been higher than bulk silicon. This is because the work function of nickel is higher than bulk silicon.)

Tip Number	Max I	Starting voltage (to obtain 10^{-9} A)			Fowler-Nordheim Plot Slope			Fowler-Nordheim Plot Intercept		
		Plain	Porous	Nickel	Plain	Porous	Nickel	Plain	Porous	Nickel
1	n/a	1700V	1200V	1094V	3.8×10^4	2.1×10^4	1.6×10^4	-13	-18	-19.7
2	6μA	1741V	not taken	680V	3.1×10^4	not taken	0.47×10^4	-14.8	not taken	-23.5

Plain = Before Anodisation; Porous = After anodisation; Nickel = After deposition of nickel onto anodised silicon

n/a = not tested to destruction.

Tip no. 2 was not characterised between anodisation and nickel deposition.

(The starting voltage was ~15% lower than immediately after anodisation and the slope of the FN plot was lower by ~25%. These results suggest that either some sharpening of the emission sites occurred, or that the work function was lowered. Note that if the work function was lowered after deposition of nickel onto the porous silicon layer (rather than an increase in enhancement factor), the work function of the porous silicon must have been higher than bulk silicon. This is because the work function of nickel is higher than bulk silicon.)

Table 8.8 Characterisation of Anodised Tips After Deposition of Thin Nickel Layer

c) Confirmation of Presence of Nickel on Porous Silicon Surface

Figure 8.20 shows images of the tip after FIM/FEM characterisation and nickel evaporation. The presence of nickel on the porous silicon surface was confirmed by the FIM image, which exhibited small rings (similar to those obtained from a nickel FIM tip). In addition, TEM examination following characterisation showed the appearance of additional spots in a selected area diffraction pattern.

8.9 Summary of FIM/FEM Results

The main conclusions from this work are as follows:

i) For anodised emitters, the emission source was the sharp fibrils present at the anodised surface.

ii) Anodisation lowered the starting voltage of tips by 25-50%, confirming the results obtained in the adapted SEM.

iii)The stability of emission decreased as the PS layer thickness increased, confirming the results obtained in the adapted SEM.

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Chapter 9 - Conclusions and Suggestions for Further Work

9.1 Decrease in Operating Voltage Following Anodisation

9.1.1 Degree by Which Operating Voltage was Lowered

a) Studies in the adapted scanning electron microscope (SEM) showed that anodisation of p^+-type silicon FEAs led to a decrease in starting voltage of up to ~50% compared to before anodisation. Similar results were also observed in the field emission microscope (FEM).

b) The decrease in starting voltage for p^+-type FEAs was greater than for p-type FEAs, which exhibited a reduction in starting voltage of up to ~40% following anodisation.

These results are important because one of the major challenges in the development of vacuum microelectronic (VME) devices is to obtain field emission at the lowest possible voltage. These results agree with similar work carried out by other researchers who examined both anodised gated and ungated tips.

9.1.2 Source of Lower Operating Voltage Emission

a) Studies in the adapted SEM indicated that the reduction in operating voltage following anodisation was due to an increase in field enhancement, rather than a decrease in work function.

b) Transmission electron microscope (TEM) analysis showed that following anodisation, there were two possible causes for field enhancement:

i) The high density of very small, sharp fibrils present at the anodised surface.

ii) The rough, sharp interface between the PS layer and the underlying silicon.

c) Further studies in the adapted SEM and studies of FIM/FEM images showed that emission occurred from surface fibrils at the surface of anodised tips, which caused local enhancement of the applied electric field. This work is an advance on the work of other researchers, who have not identified why emission improved following anodisation. In

particular, this work indicates that the explanation proposed by Yue *et al.* (1990), that emission occurred from the rough PS/bulk silicon interface, is incorrect.

d) Studies in the adapted SEM showed that the greatest decrease in starting voltage was observed for anodised p^+-type silicon FEAs. This is believed to be due to the fact that p^+-type PS had a larger emission area, possibly due to the larger fibrils present at the emitter surface (as observed by TEM).

9.2 Maximum Emission Current

Two different effects appear to have influenced the maximum emission current obtained before destruction of emitters occurred. One effect acted to increase the maximum current, whereas the other effect acted to decrease the maximum current:

9.2.1 Increase in Maximum Emission Current for Very Thin Porous Silicon Layers

For very short anodisation times (i.e. for very thin porous silicon layers), the maximum emission current increased by up to three times the value obtained before anodisation. This is an important result, as another challenge in the development of VME devices is to obtain high currents at low voltages, and to prevent tips blowing at low current values. If the required current (~0.1μA per tip for displays) could be obtained at a low voltage, the tip would be less likely to experience ion bombardment which could destroy it. However, the effect was not as great as early results from blunter emitters had indicated (where maximum emission current was up to 10 times higher following anodisation).

The increase in maximum current was believed to be due to one or both of the following two effects:

1) The PS layer acted as a protective resistive layer, hence preventing tips blowing at lower current values.

2) There was an increase in the number of emitting sites, due to the presence of many fibrils at the emitting surface.

9.2.2 Maximum Emission Current Decrease with Increasing Resistance of Porous Silicon Layer

The higher the resistance of the PS layer, the lower the maximum current obtained prior to destruction of the tip. It is believed that this was due to resistive heating of the PS layer, which led to over-heating and subsequent tip self-destruction. Resistive heating would have increased with increasing PS layer thickness, and would thus have caused tips to self-destruct at lower current values.

9.2.3 Optimum Porous Silicon Layer Thickness

There may be an optimum PS layer thickness, at which point the maximum current is increased versus non-anodised silicon, but at which destructive resistive heating has not yet occurred. It is thought that if layers of PS even thinner than investigated here could be produced, an optimum thickness may be reached and hence higher maximum currents may be obtained.

9.3 Suggestions for Further Work

The work described in this thesis has advanced the understanding of how anodisation can be used as a simple treatment to improve the field emission properties of silicon FEAs. The investigations described in this thesis should be continued. Suggestions for further experiments and improvements to the existing equipment are described in the following sections.

9.3.1 Further Optimisation of Field Emission Properties

a) Investigation of Larger Range of Anodisation Conditions

i) For p and p^+-type silicon FEAs, a wider range of anodisation current densities should be investigated. In this work there was only sufficient time to investigate samples anodised with a current density of $30mAcm^{-2}$ for p-type silicon and $100mAcm^{-2}$ for p^+-type silicon.

ii) Studies of anodised n and n^+-type silicon emitters should also be investigated. The cross-sectional morphology of n and n^+-type PS has been found by other researchers to be very different from p and p^+-type PS (see Chapter 3). Therefore the morphology of the anodised tip is likely be different from p and p^+-type PS, and could potentially have even better emission characteristics.

b) Search for Optimum Porous Silicon Layer Thickness

Field emission from layers of PS which are thinner than those examined here should be investigated. An optimum thickness may exist where even higher emission currents than so far observed can be obtained.

9.3.2 Investigations into Long-Term Stability

Emission stability is an important parameter in the operation of a VME device. Studies in the adapted SEM and in the FEM showed that the stability of emission from silicon tips before and after anodisation was similar. However, it has not been possible to compare the long-term stability of emission from FEAs before and after anodisation. This is because the mechanical probe used in the adapted SEM was not stable over long periods of time (i.e. several hours) and would have drifted, thereby confusing any results taken. Also, for both the adapted SEM and the FIM/FEM, sufficient equipment time was not available. Such studies could be carried out in a FEM which has been specially designed and dedicated to examining gated FEAs; or alternatively in another piece of UHV equipment, such as the VME Surface Science System. However, such studies would also require the development of gated FEAs, as it would not be possible to apply a voltage to ungated emitters using these systems. This work has been started by Huang *et al.* (1997).

9.3.3 Development of Devices

a) Development of Anodised Polysilicon Emitters

FEAs for flat panel displays are likely to be manufactured from polysilicon evaporated onto glass, rather than from wafers of single crystal silicon. Therefore, investigations should also be carried out to ensure that polysilicon emitters undergo a similar improvement in emission

following anodisation, and that the PS morphology at the tip apex of an anodised polysilicon tip is similar to that at an anodised single crystal silicon tip. This work has been started by S.Pullen and M.Huang in the Department of Materials, Oxford (see Pullen *et al.* (1996)).

b) Increase in Emission Current and Stability

If the porous structure was metal rather than silicon, higher emission currents could be obtained. Conversion of the PS structure to porous tungsten has previously been carried out for flat PS layers, by flowing WF_6 gas through the structure, see Groenen *et al.* (1994). This treatment should be investigated for anodised FEAs.

References - Chapter 9

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Appendix - Background Theory for FIM and FEM

1) Field Ion Microscopy / Field Evaporation

The field ion microscope (FIM) was invented by Müller (1953). It can be used to image the surface protrusions at a tip.

a) Process of Image Formation

When a high voltage is applied to the needle-like tip, gas atoms become polarised and are drawn towards the tip, colliding with it. In the process of collision, they lose some of their kinetic energy and become trapped in the high field region. The atoms then "hop" along the surface, as they become thermally accommodated to the specimen temperature. At high enough field, the first gas atoms to reach the surface become adsorbed at the high field sites above prominent surface atoms. Subsequent atoms to arrive at the surface migrate across the surface of this field adsorbed layer, until they are ionized by quantum-mechanical tunnelling.

For ionization to occur, electrons from the gas atoms must tunnel through the surface potential barrier into the specimen, leaving positively charged gas ions on the surface. However, electrons can only tunnel if they have an empty state to fill. Therefore, there is a critical distance within which field ionization will not occur. Gomer (1961), Müller & Tsong (1969) and Miller & Smith (1989) give detailed treatments of the equations governing the field ionization process. Field ionization occurs preferentially above the most prominent atoms, due to a higher probability of tunnelling (as this critical distance is decreased) and an increased gas supply.

Following ionization, the gas ions are then repelled from the sample, and travel along radial paths towards the channel plate. On hitting the channel plate, secondary electrons are produced in the electron multiplier. Hence, a highly magnified, projected image of the tip surface is obtained on the fluorescent screen. The magnification of the image is determined by the ratio of the tip-to-screen distance to the tip-radius, and is ~1 million times. The maximum solid-angle viewed in a FIM image is 100-120°, depending on the

tip-to-screen distance. The resolution limit of the FIM is 0.25nm (higher than in the FEM), depending on specimen temperature and the image gas used.

Only the protruding atoms at the tip are imaged. The intersection of each atomic layer with the specimen surface forms a ring. On the surface of a crystalline material, the most prominent atoms lie at the edges and corner sites, corresponding to a series of concentric rings over a curved surface. Successive atomic terraces parallel to a particular crystallographic plane generate concentric rings in the image. This allows identification of major crystallographic directions. However, FIM images from semiconductors are less regular and fainter than for metals. This is due to the fact that field evaporation from high index regions is irregular, and leads to immediate surface reconstruction of the remaining atoms.

b) Field Evaporation - Obtaining Smooth Tips

In order to form a good FIM image, the tip should be smooth, and of cylindrical symmetry, rather than being blade-shaped. Smooth tips may be achieved by the process of field evaporation. Field evaporation occurs when high fields are applied to the tip. During field evaporation, surface atoms themselves (not just gas atoms) become positively charged and are removed from their atomic sites. Prominent atoms are removed, thereby smoothing out rough surfaces. Detailed accounts of field evaporation theory are given by Müller & Tsong (1969), McKinstry (1972), Miller & Smith (1989) and Forbes (1995). Field evaporation of semiconductors is less uniform than field evaporation of metals, for the reasons described previously.

2) Field Emission Microscopy

The field emission microscope (FEM) was invented by Müller (1937). A detailed description of the FEM and its various applications are given by Gomer (1961) and Swanson & Bell (1973).

a) Image Formation

To obtain a FEM image, the emitter is held at negative polarity. The actual field at the tip is:

$$F = V/kr \qquad (2)$$

where F=field at tip surface, V=voltage applied, r=radius of tip and k=field factor due to the fact that the emitter has a conical shrank (rather than being a sphere) - value is in range 4-7, with a usually quoted value of ~5. Adequate fields for electron emission should be obtained at 2-3kV, for a tip of radius 100nm.

Electrons travel approximately radially from the specimen surface, through the vacuum to the channel plate. On hitting the channel plate, they form a field emission image. The electrons closely follow the lines of force because they have very little energy after leaving the tip surface.

b) Magnification

When the tip has a hemispherical end form, the magnification of the microscope is given by:

$$M = x/\beta r \qquad (1)$$

where β is the image compression factor (β = 1.5-1.8), x is tip-screen distance and r is tip radius. Magnifications obtained typically lie in the range 10^5-10^6. The resolution of a FEM is ~2.5nm (i.e. 10 times lower than FIM). The resolution improves as the tip radius gets smaller ($\propto \frac{1}{\sqrt{r}}$) and is independent of the tip-screen distance. The resolution is mainly limited by the electron velocity at right angles to the emission direction.

c) Image Contrast

Local variations in the field, e.g. due to asperities, cause emission anisotropies and therefore provide image contrast. Such asperities, if conducting, will distort and compress the equipotentials in their vicinity. (A divergence of the lines of force also occurs which is equivalent to a lens effect.) The result is local field enhancement and increased emission. The electric field at a hemispherical bump is three times less than

the field at a flat surface (if the bump is on a curved surface, enhancement is slightly less). The magnification at an asperity, whose shape is approximated to that of a hemispherical bump of radius ρ, is given by:

$$M'/M = 1.1(r/\rho)^{1/2} \quad (3)$$

where M' = magnification from the hemispherical bump, M=magnification away from bump area and r = radius of underlying emitter. Work function differences on the specimen surface will also cause image contrast in the FEM, with regions of lower work function producing higher emission.

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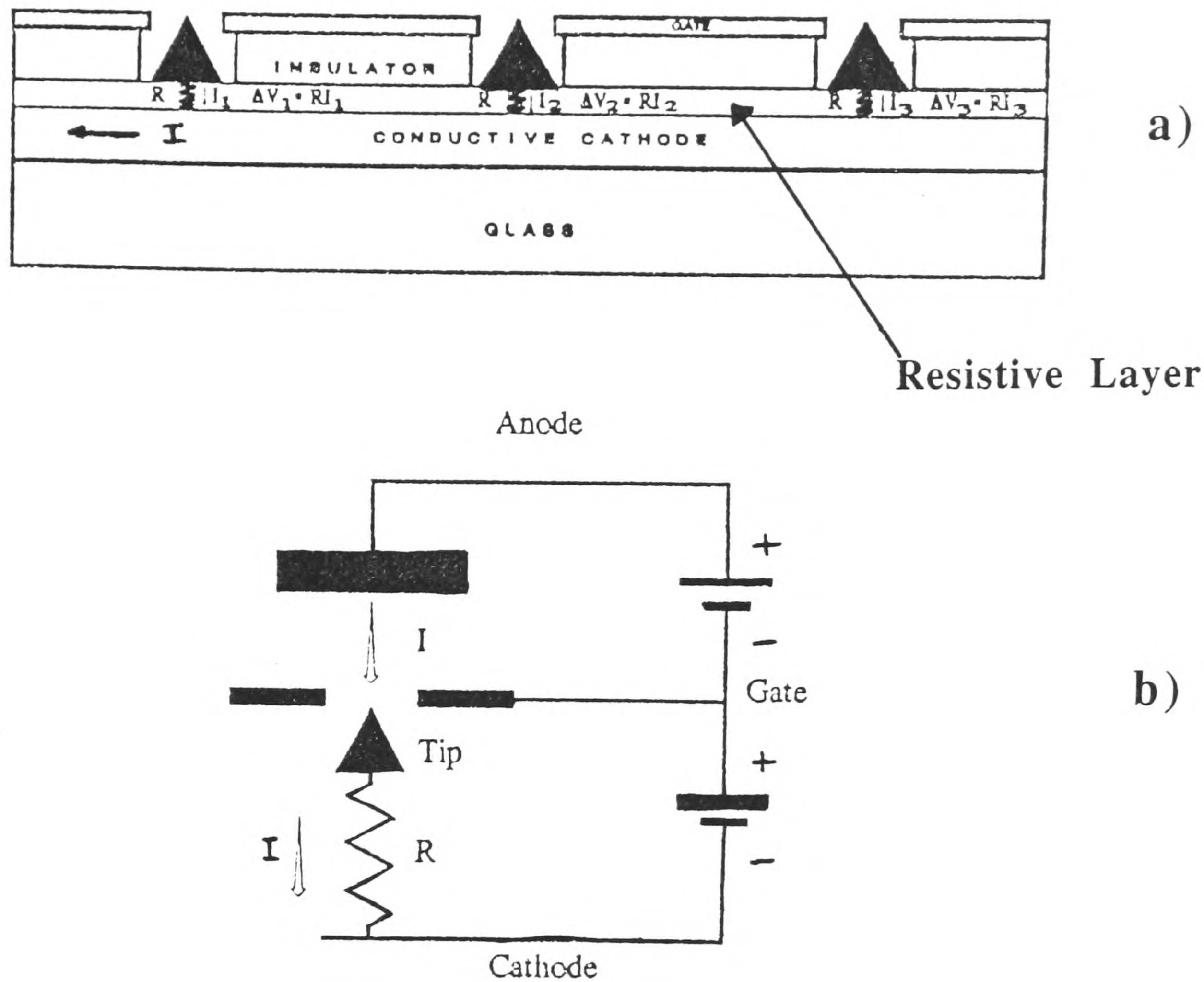
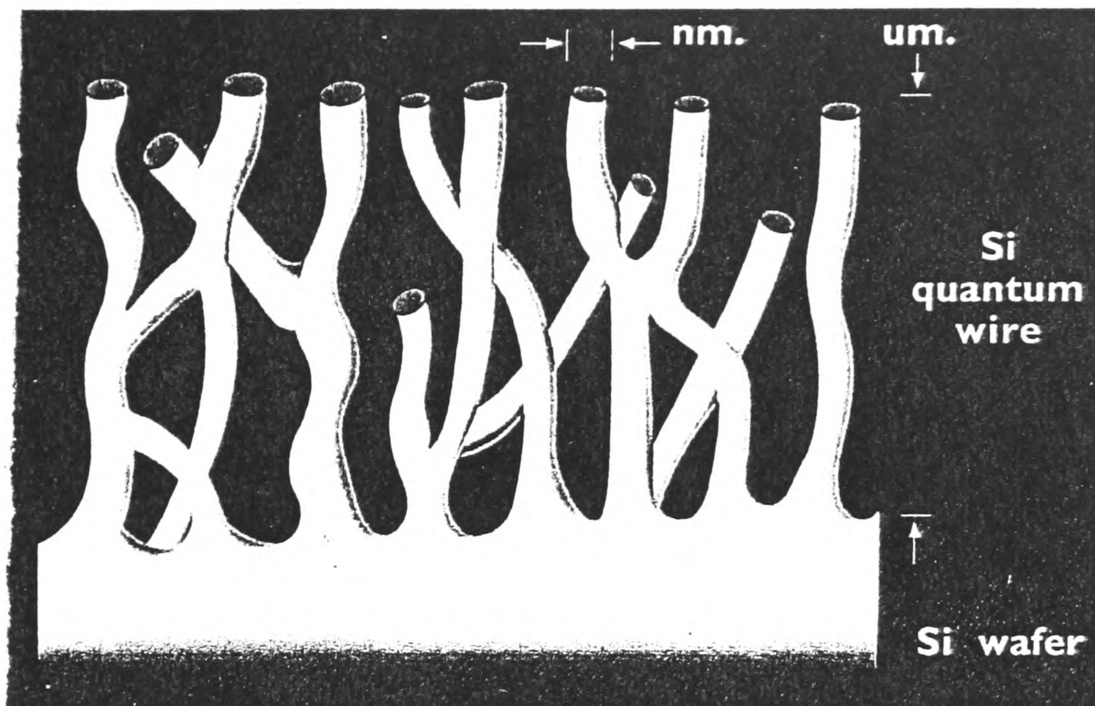


Figure 2.9 - Diagram Showing Incorporation of Resistive Layer into FEA Device for Protection

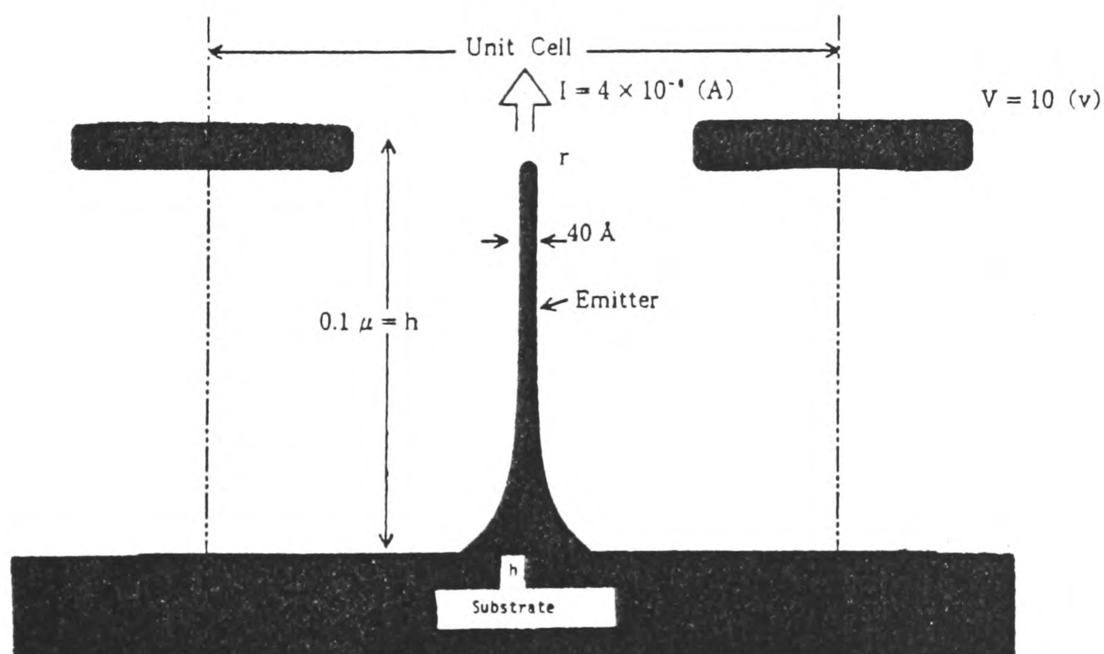
a) Shows a lateral resistive sheet lying right across the device, just below the emitters. This had the effect of acting as though a resistor was in series with each emitter tip as shown in Figure b).

(Ref: R.Baptist, *"Nanosources and Manipulation of Atoms Under High Fields and Temperatures: Applications"* edited by V.T.Binh, N.Garcia and K.Dransfeld, published by Kluwer Academic Publishers, Dordrecht (1993), 165)



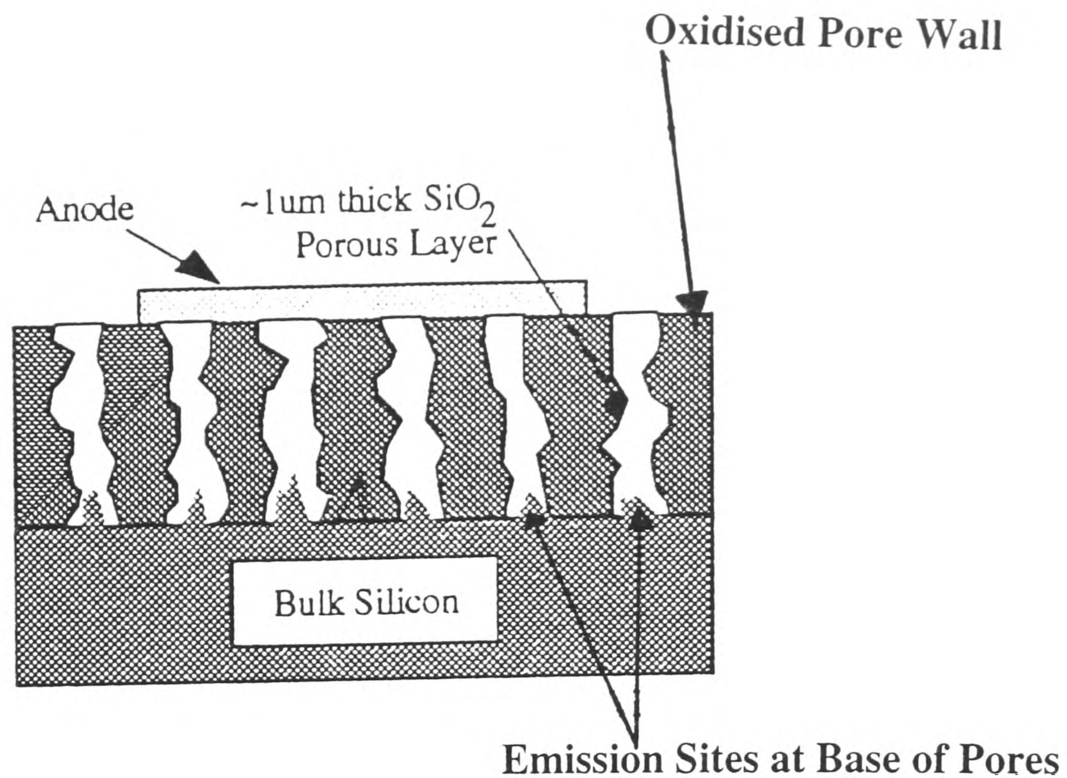
(Ref: L.Canham, *Physics World*, **5(3)** (1992), 41)

Figure 2.10 - Schematic Diagram of Porous Silicon
This shows a highly schematic diagram of porous silicon. In this diagram, the porous silicon fibrils were found to be very similar in geometry and shape to the "ideal" field emitter shown in Figure 2.11.

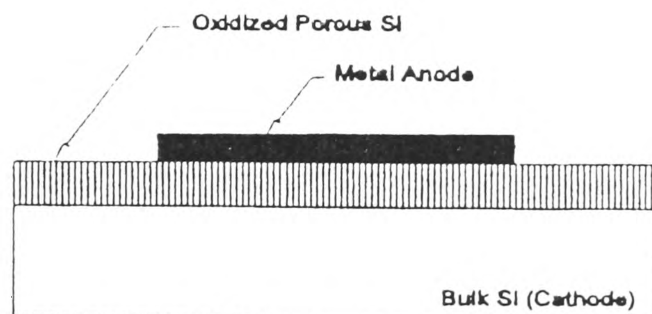


(Ref: T.Utsumi, IEEE Trans. Electron Devices, 38 (10) (1991), 2276)

Figure 2.11 - Geometry of "Ideal" Eiffel-Tower Field Emitter
This tip has the "ideal" geometry for a field emitter. It has a high aspect ratio (ratio of emitter height / emitter radius), giving it a low starting voltage. It also has a wide base (giving it an Eiffel-Tower geometry), giving it good thermal stability.



a) Microscopic Representation of a Cross-Section of an Oxidised Porous Silicon Field Emission Diode
A thin layer of porous silicon was oxidized to form an insulating layer. Metal was then evaporated over this layer (shadow-mask evaporation to form metal dots), sealing the micropores. This metal layer became the anode. The researchers believe that low voltage emission was possible because ultra-sharp silicon fibrils were formed at the base of the pores. They believe that stable emission occurred due to the high number of emission sites beneath the metal anode.

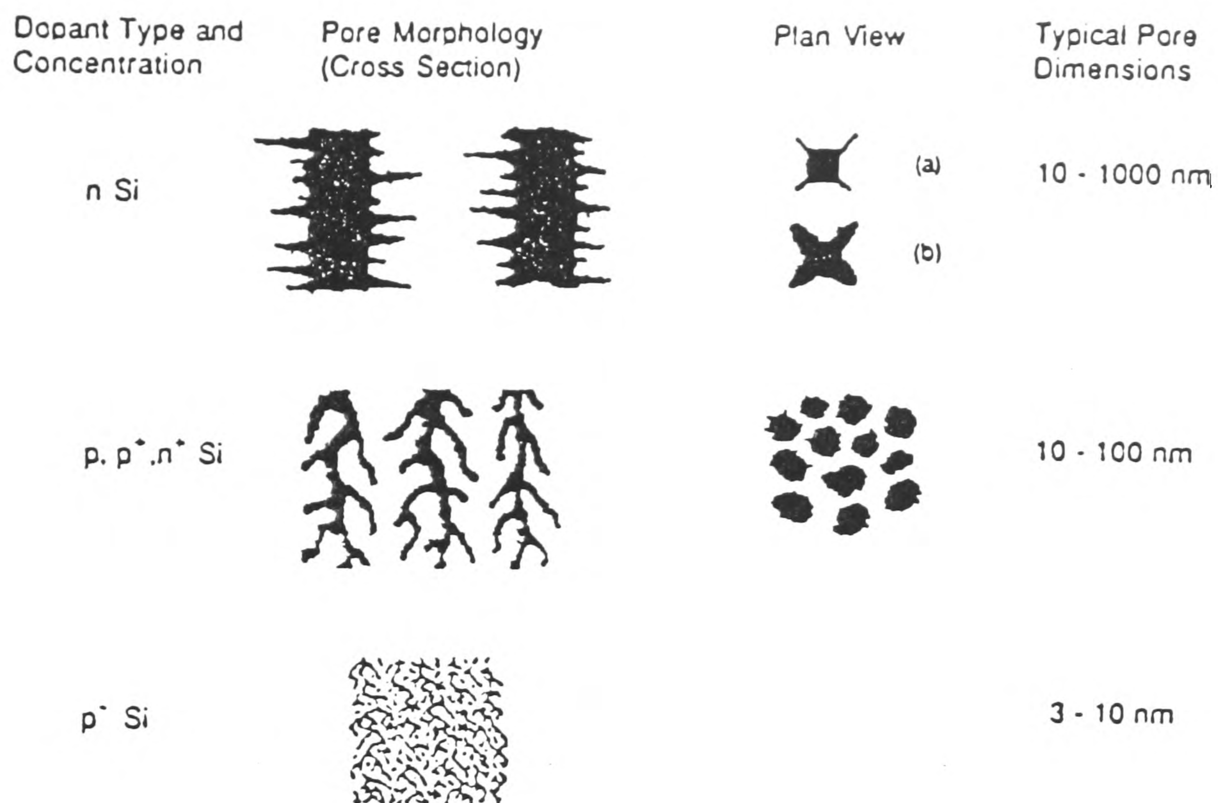


Cross-sectional representation of an OPSFED.

b) Cross-sectional representation of the device structure.

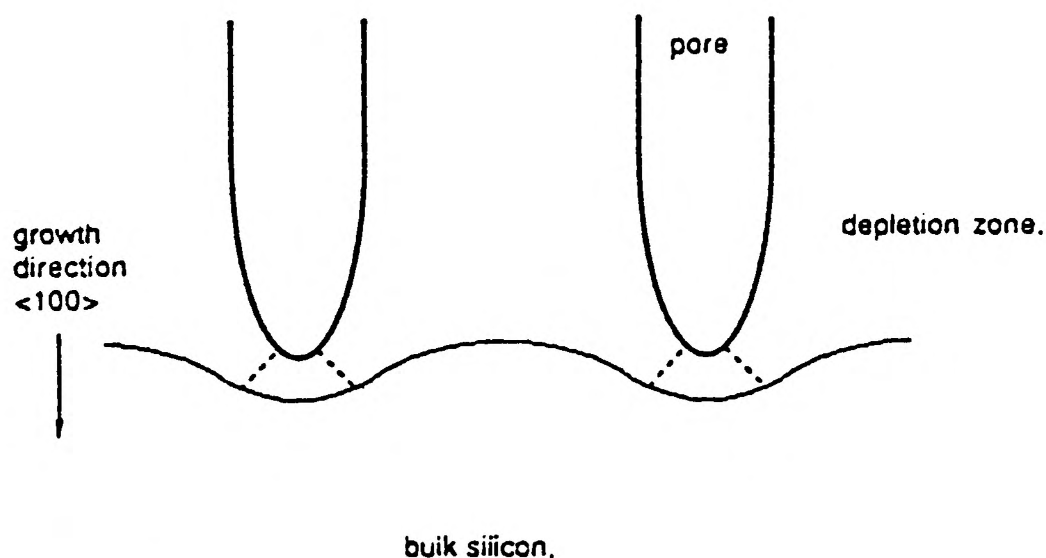
(Ref: J.R.Jessing, D.L.Parker and M.H.Weichold, *J. Vac. Sci. Technol. B*, **14(3)** (1996), 1899)

Figure 2.12 - Diagrams of Oxidised Porous Silicon Field Emission Diode
These diagrams show the flat porous silicon diode investigated by Jessing *et al.* at Texas A&M University, US.



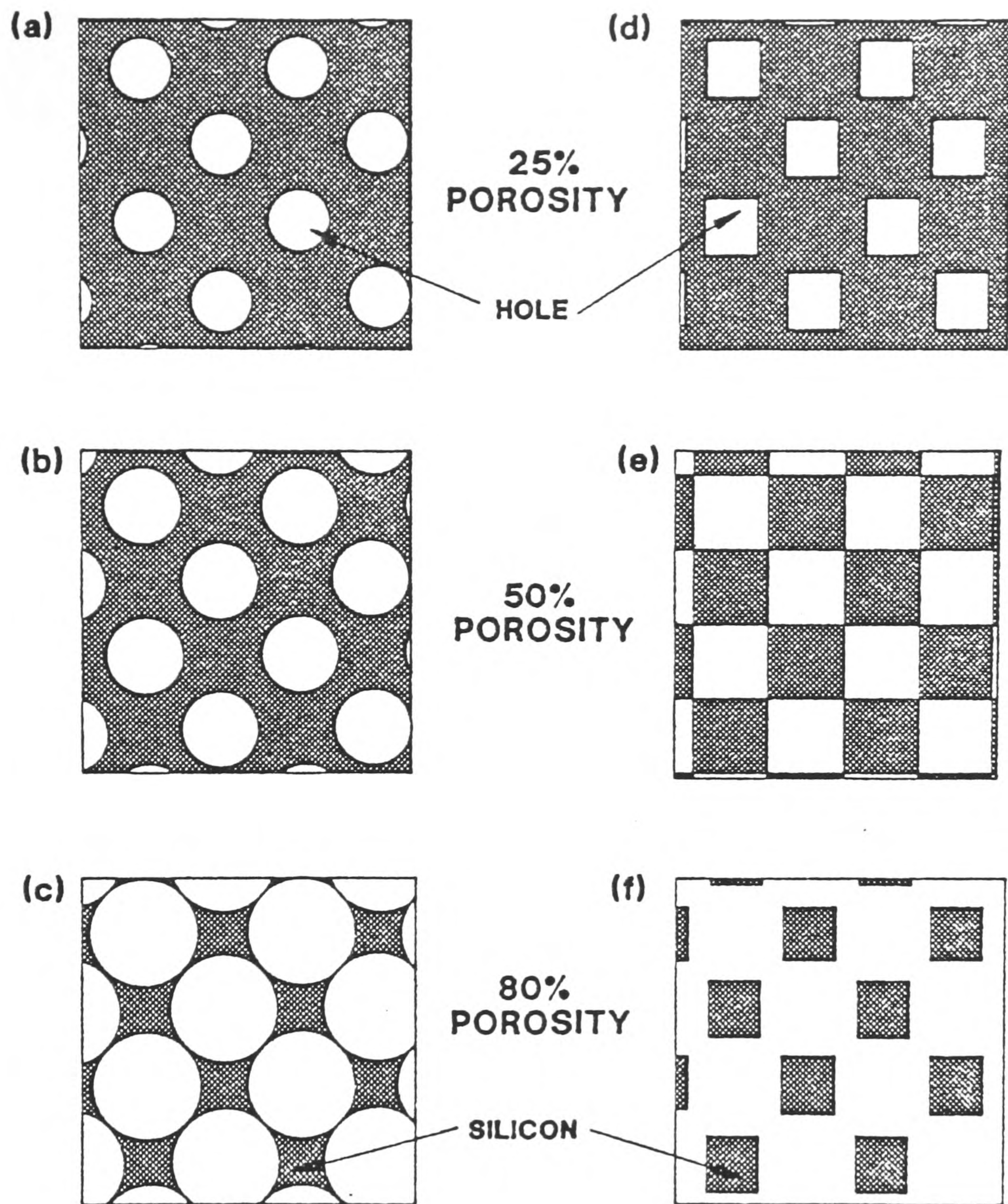
(Ref: P.C.Searson and J.M.Macauley, *Nanotechnology*, **3** (1992), 188)

Figure 3.2 - Schematic Diagram Demonstrating Three Main Types of Pore Structure
This diagram demonstrates the three different types of pore structure obtained by anodising different types of silicon substrate (p-type, p^+-type, n-type and n^+-type).



(Ref: (Ref: P.C.Searson and J.M.Macauley, *Nanotechnology*, **3** (1992), 188)

Figure 3.3 - Schematic Diagram Demonstrating Depletion Regions Formed During Anodisation of P^+-Type Silicon
During anodisation of p^+-type silicon, the depletion regions formed are widest at the pore edges than at the pore ends. As a result, the current density in the region between the pores is much lower than at the pore ends. The depletion regions of adjacent pores overlap, increasing the depletion layer width. This prevents the pores from growing any closer, whereas the pores will propogate at the tip ends. This results in the formation of columnar pores.



(Ref: L.T.Canham, *Appl. Phys. Lett.*, **57** (1990), 1046)

Figure 3.4 - Schematic Diagram Demonstrating Concept of Porosity
This figure shows an idealised view of the partial dissolution of silicon during pore formation. Note that for 50% porosity and above, the silicon wires become physically isolated from each other.

Silicon resitivity (Ωcm)	Current density (mA/cm2)	Porous Silicon Porosity / W%			
		20 % HF	30 % HF	40% HF	48% HF
0.01	**10**	40	30	28	23
	30	51	34	31	23
	100	79	45	40	29
0.1	**10**	55	46	38	37
	30	61	45	42	33
	100	77	58	28	41
1.0	**10**	60	50	49	40
	30	61	53	52	41
	100	a	64	54	52

a = samples crazed on removal from cell due to low density
The density of each PS film was determined from the weight loss on anodization (determined by gravimetric analysis), and the film depth was measured in an SEM.

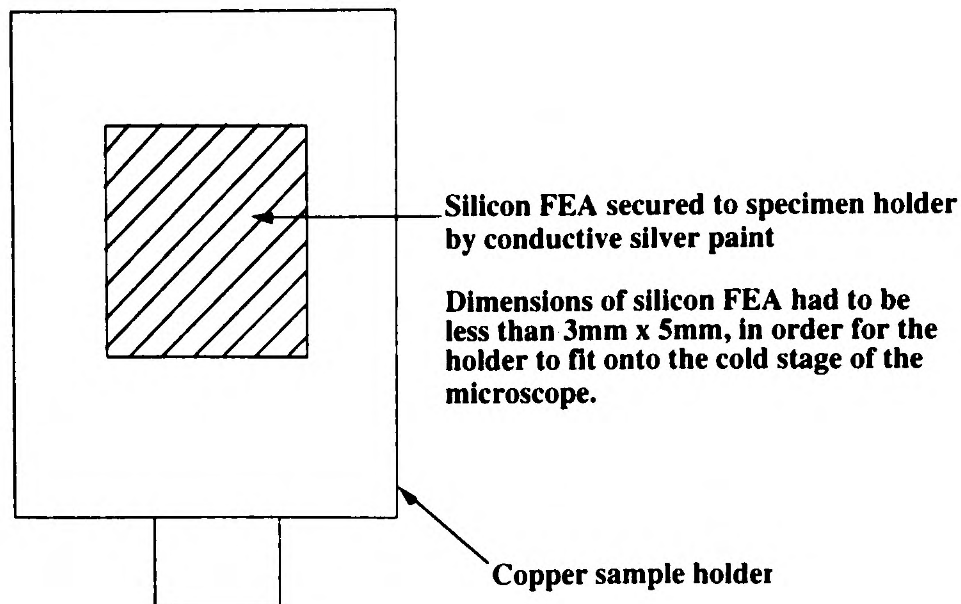
Table is taken from M.IJ.Beale, N.Chew, M.J.Uren, A.G.Cullis and J.D.Benjamin, *Appl. Phys. Lett.* **46** (1985) 1

The pore size increases with increasing film porosity:

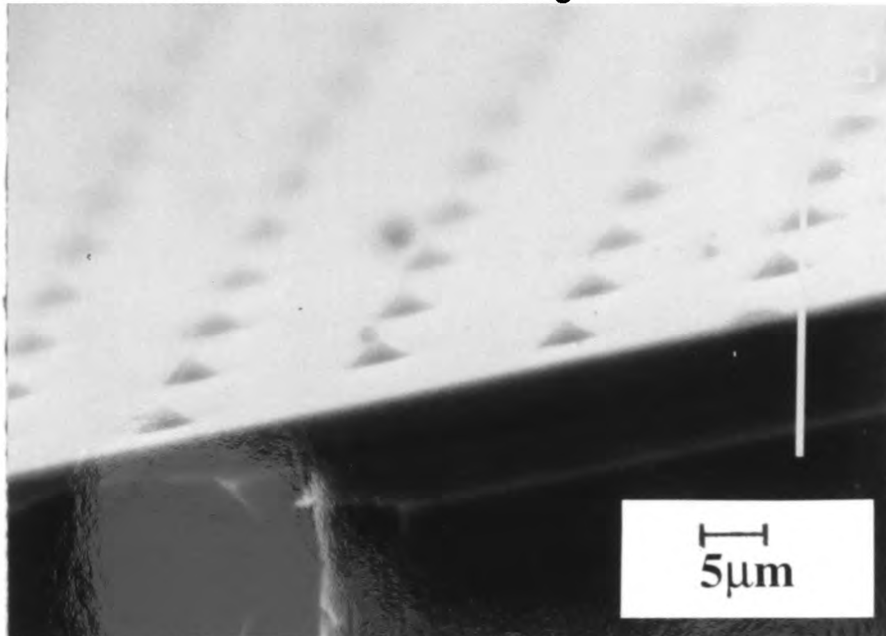
1Ωcm Resistivity Silicon - PS material of 36% porosity would have pore sizes ~2.5nm wide and PS material of 52% porosity, would have pore sizes of ~5nm wide. Material of 64% porosity is so open that it is very difficult to distinguish between separate pores.

0.01Ωm Resistivity Silicon - PS material of 31% porosity would have pores ~6nm wide, whereas material of 51% porosity PS would have pore ~12nm wide. 79% porosity PS is so open that it is difficult to identify individual pores.

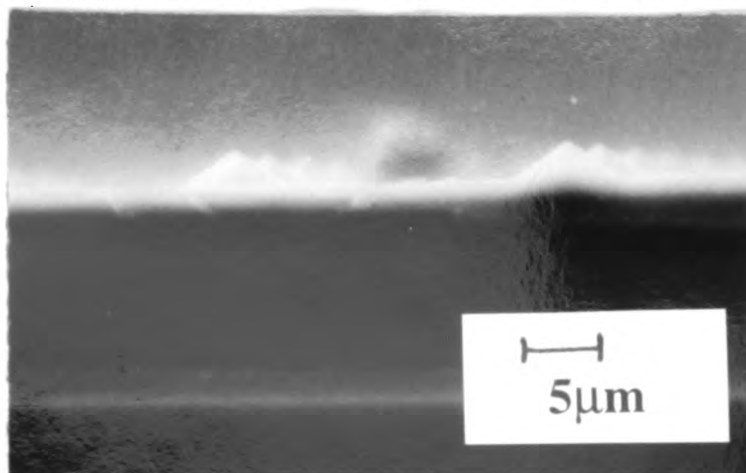
Table 3.2 - Porosity and Pore Size of P-type and P^+-Type Porous Silicon as Weight % of Bulk Silicon



a) Plan View Showing Silicon FEA array glue onto copper grid
Specimens were secured to the specimen stub with conductive paint. The specimen stub took a sample up to 3mm x 5mm in size. The stub slid onto a cold stage inside the microscope (see Fell (1992)). Normally, the sample was secured so that the substrate was flat and emitters protruded in a vertical direction., but the sample could also be secured so that the substrate stood on edge.



b) 505 SEM micrograph across a silicon field emitter array - sample lying horizontal
The sample was normally placed flat, so that the position of the probe in the x and y direction was known.



c) 505 SEM micrograph looking down rows of emitters - sample standing vertical
The sample could also be placed on its edge, so that the position in the x and z direction were known. It was much harder to position the probe if this configuration was used.

Figure 4.2 Specimen Mounting

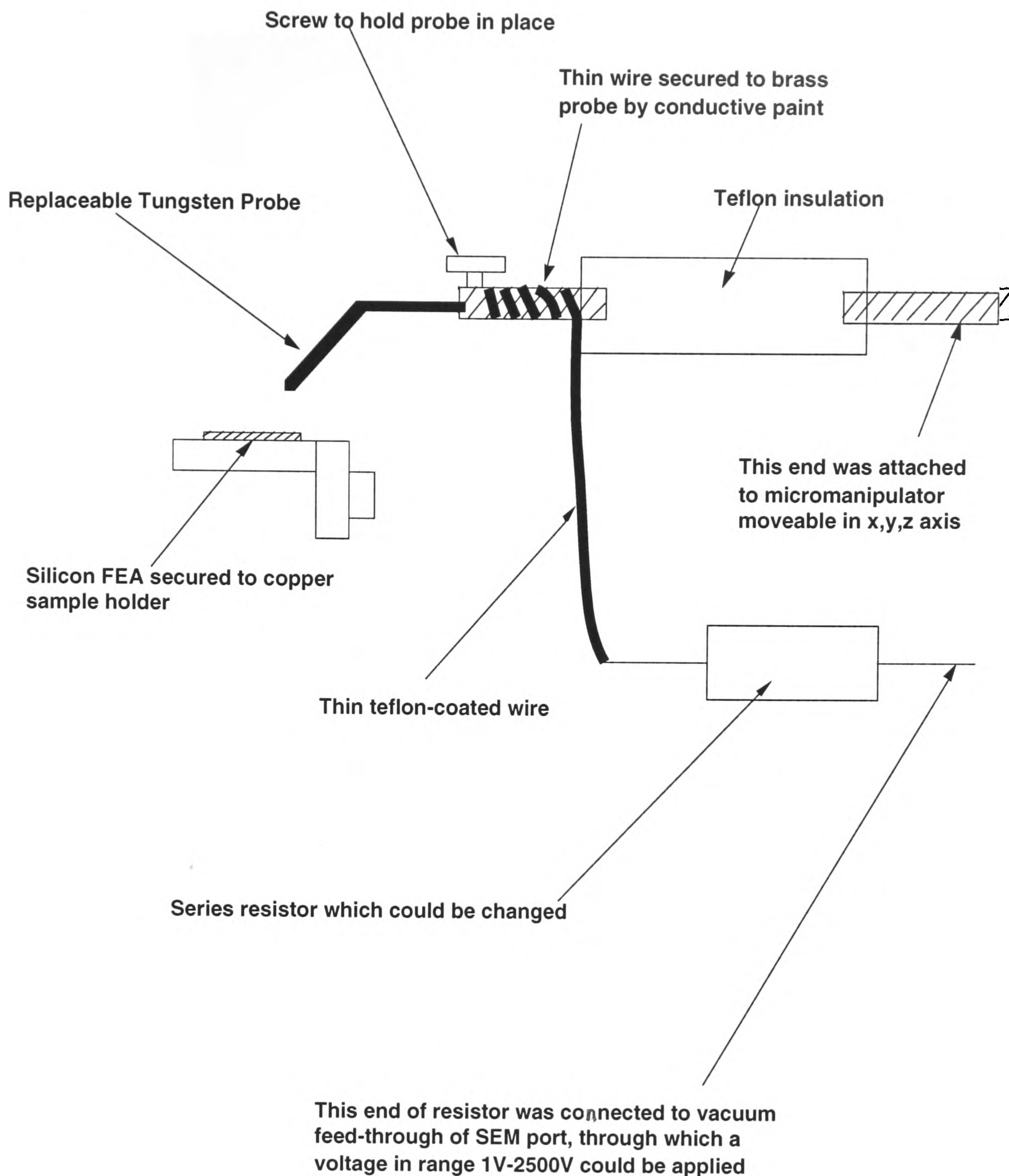
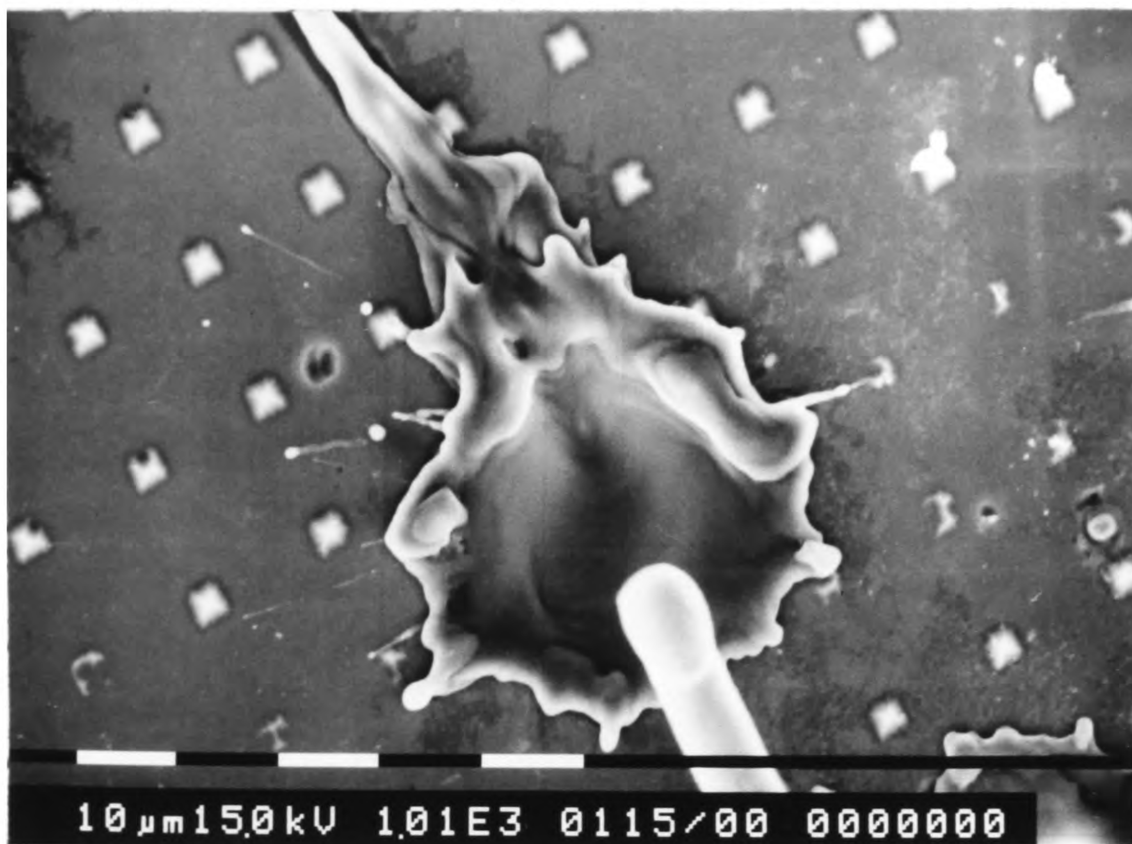


Figure 4.3 - Schematic Diagram of Probe

To ensure electrical insulation between the SEM wall and the probe end, the middle section of the probe was constructed from teflon. One end of the probe slotted into an existing micromanipulator arm inside the microscope, see Fell (1992). This probe could be moved in the x,y and z directions using external control wheels. The front part of the probe, which carried the high voltage, was constructed from brass. It was screwed into the teflon section and was joined, via a wire, to a high voltage feed-through connection on the wall of the SEM. On the outer wall of the SEM chamber, this high voltage connection was attached to a high voltage source, which could deliver a voltage in the range 1-2500V.

A small hole was drilled into the front brass section of the probe (i.e. the section carrying a high voltage). A fine tungsten wire was inserted into this hole and was held in place by a small screw. This wire was as thick as possible, in order to increase its stiffness. This wire was formed by electropolishing one end of a length of tungsten wire, using the same method used to electropolish silicon FIM tips, see Chapter 8. The electropolished wire end was small enough in diameter to be positioned above individual emitters. This wire was often bent or damaged during emission, which caused its diameter to increase. In this case it was replaced with a newly polished wire, in order to prevent neighbouring emitters from contributing to the emission current. Although replacing this tungsten probe was a simple procedure, the microscope had to be let up air thereby re-exposing the sample to air. Maintaining a 0.67MΩ resistor in series with the probe protected it from premature damage.

a) Resistor not placed in series with probe



b) Resistor placed in series with probe

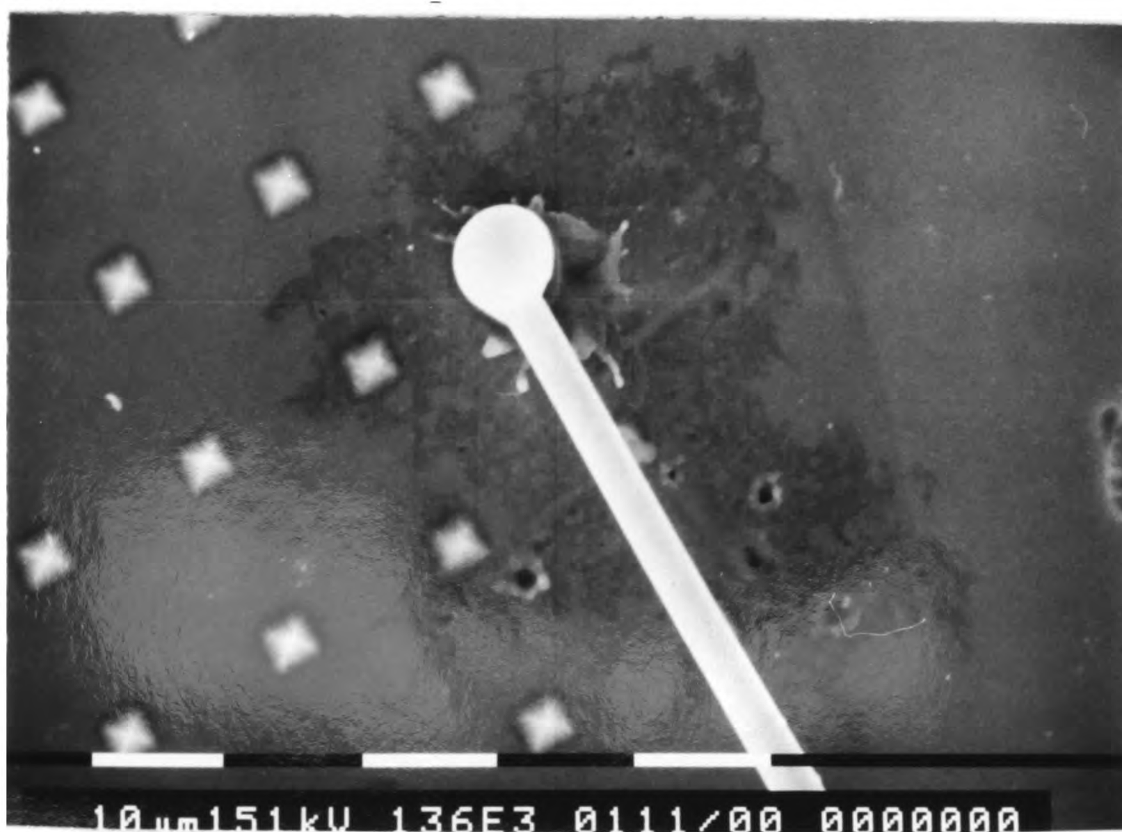


Figure 4.4 - Effect of Series Resistor

During the field emission testing described here, a 0.67MΩ resistor was placed between the probe and the high voltage vacuum feed-through. The role of this resistor was to protect the probe, in case it made contact with the specimen during field emission. If there was a surge in current, the accompanying increase in voltage was dropped across the resistor, rather than across the probe.

If a resistor was not placed in series with the probe and a voltage was still applied to the probe when it made contact with the specimen surface, both the probe and sample were melted. This could cause an increase in the radius of the probe. It was undesirable for the probe to become too large, as the emission current could then be collected from more than one tip in the array. The series resistor limited the damage to the probe, so that it did not have to changed too often. The value of the series resistor also affected the maximum current which could be obtained from each tip prior to self-destruction, see Section 4.6.

a) shows the damage caused to the sample if a resistor was not placed in series with the probe, versus **b)** which shows that the damage was reduced if a 0.67MΩ resistor was placed in series with the probe.

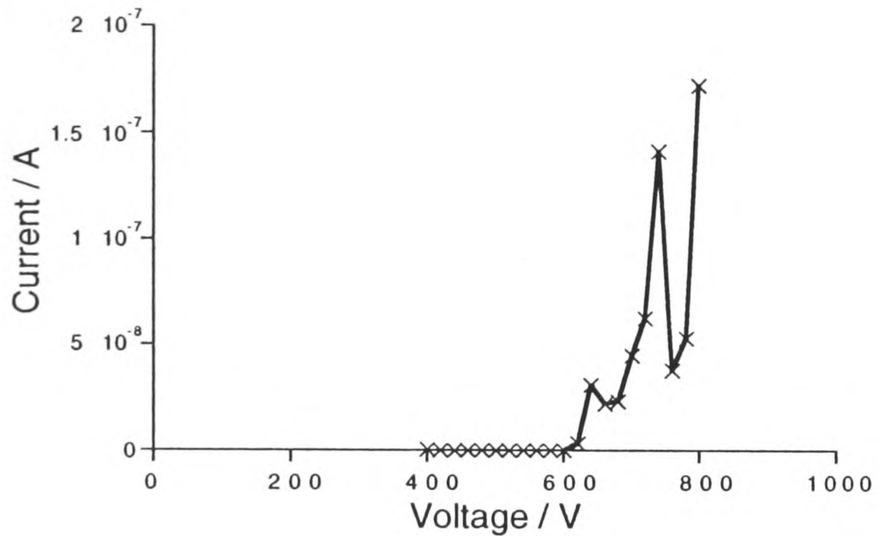
Field Emission Current Range / μA	Noise Levels In Poor Vacuum (Up to 10^{-5} torr)	Noise Levels in Improved Vacuum (Up to 2 x 10^{-7} torr)
0.5-10μA	200% or greater	10-30%
0.01-0.1μA	up to 100%	up to 10%
0.001μA	50%	up to 5%

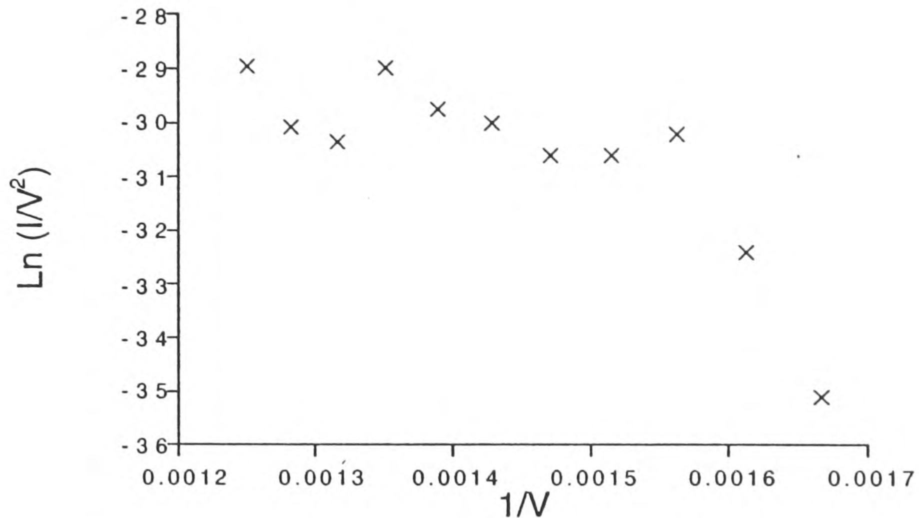
These readings were taken by observing the current fluctuation displayed on a digital voltmeter, while the probe was kept stationary above an emitter.

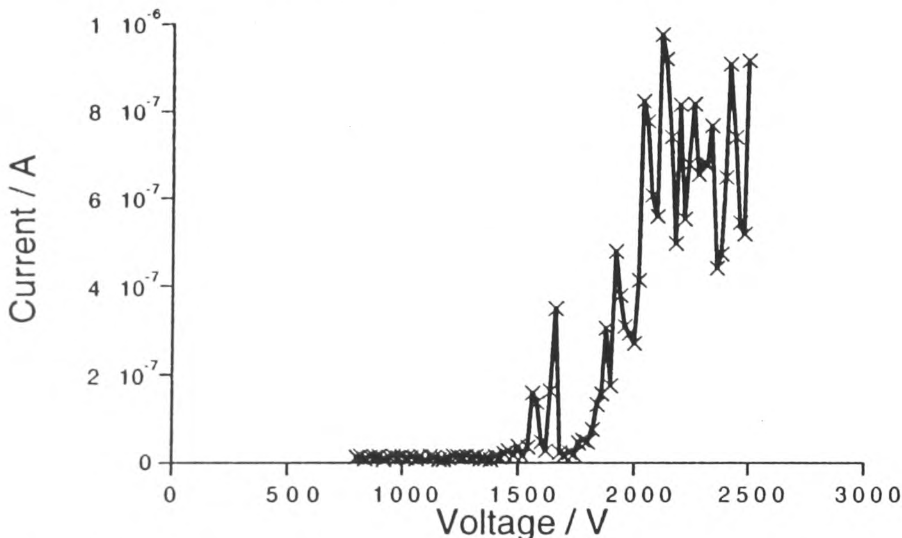
These results apply to both silicon emitters and silicon emitters onto which a thin layer of Au-Pd was evaporated.

This table shows that the noise in the poor vacuum was ~10 times greater than in the improved vacuum. Note also, that the noise increased with emission current - this has been observed by other researchers, see Chapter 2 (Section 2.6.1). This type of noise is likely to be due to adsorbates being cleaned off the emitter surface as the emission current increased.

Table 4.2: Comparison of Short-Term Noise Levels in Poor and Improved Vacuums Over time period up to 1 second for P-TypeSilicon and Au-Pd Coated Silicon Tips







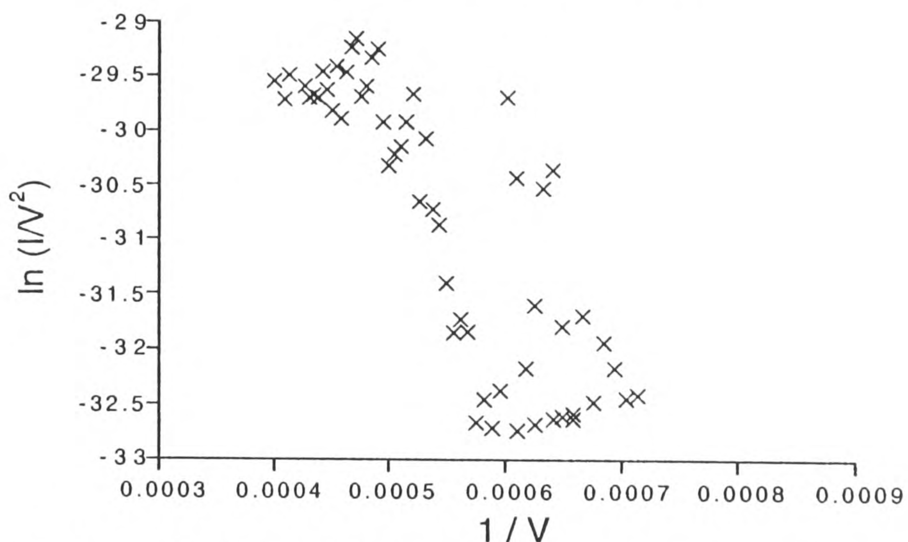
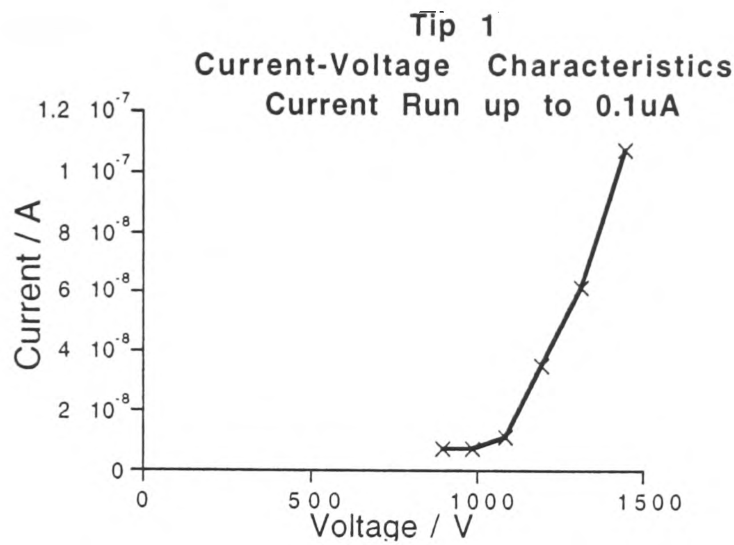
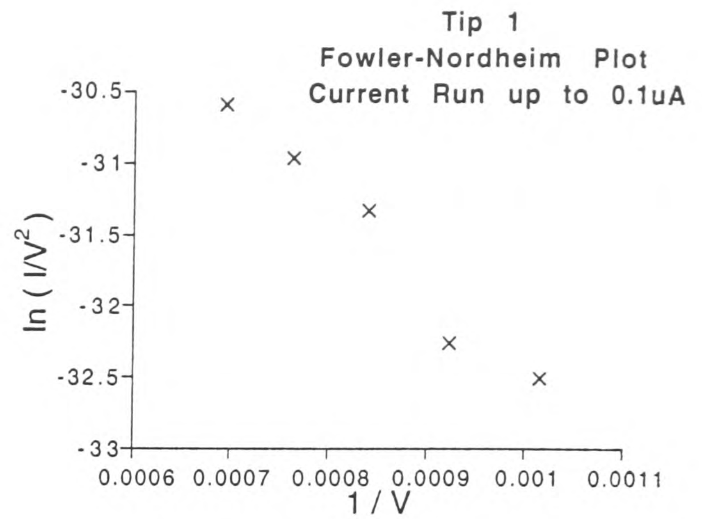
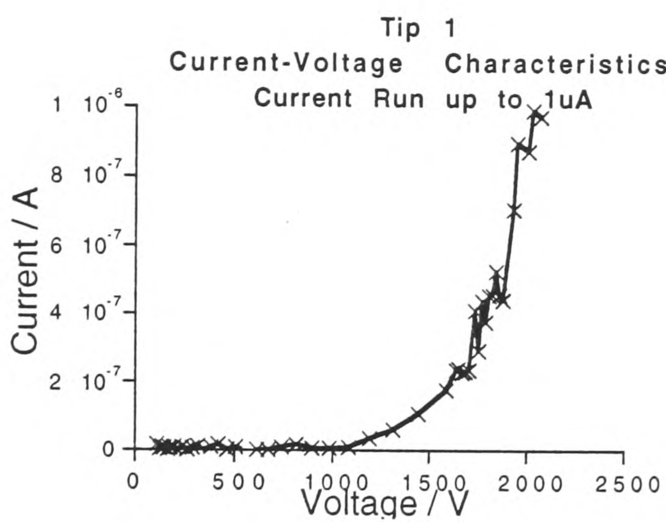
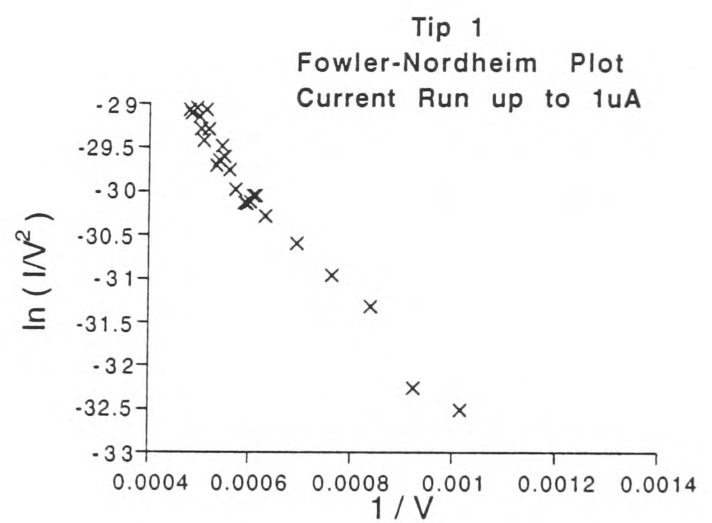


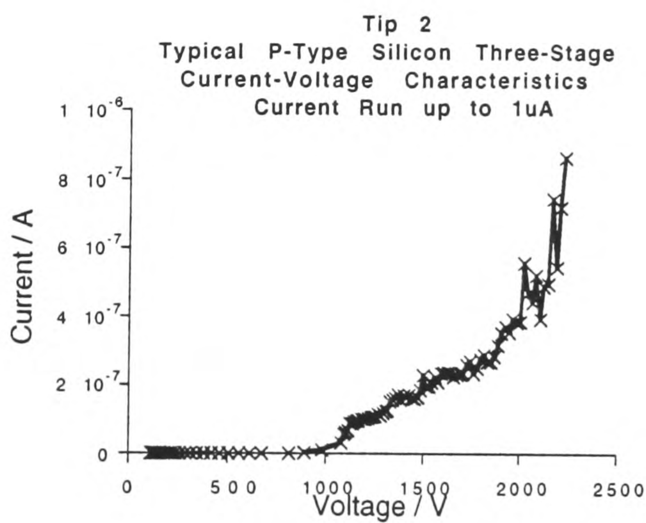
Figure 4.5 - Current-Voltage & Fowler-Nordheim Characteristics Obtained from Silicon Emitters in Poor Vacuum
This figure shows I-V and FN plots collected from 2 typical silicon emitters tested in the poor vacuum system. These figures show that the level of noise was high during current runs to both 0.1μA and to 1μA.











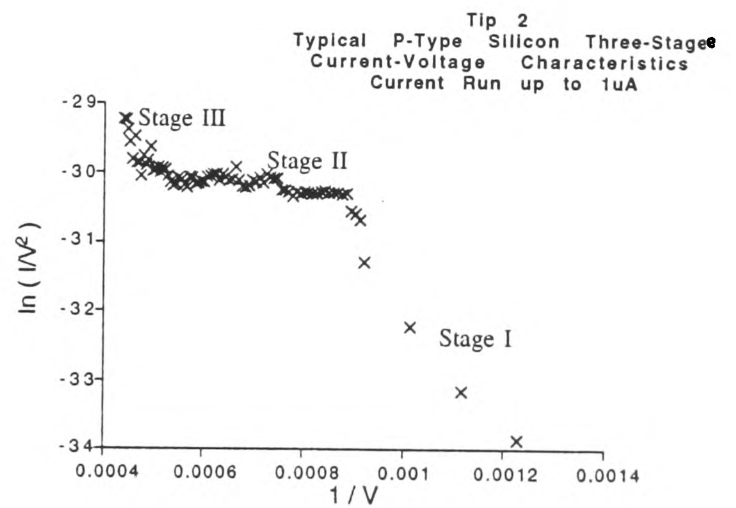


Figure 4.6 - Current-Voltage & Fowler-Nordheim Characteristics Obtained from Silicon Emitters in Good Vacuum

Comparing these FN and I-V plots with those shown in Figure 4.5, it is clear that current fluctuations were reduced following improvement of the vacuum system. However, the plots are not truely linear, probably due to oxide contamination.

Tip 2 shows FN and I-V plots from an emitter exhibiting typical p-type silicon three-stage emission.

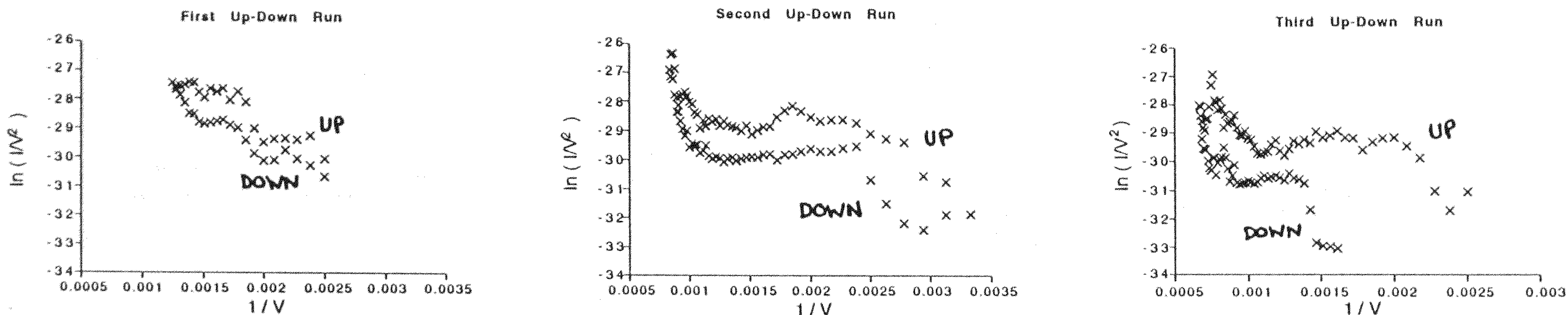


Figure 4.7 - Up-Down Hysterisis Plots Obtained in Poor Vacuum System
These plots were obtained by ramping the voltage up and then down again. Note that the up and down runs do not follow the same path, giving the appearance of a hysterisis loop. As the maximum current to which the tip was run was increased, the size of the loop became more accentuated. This suggests that as the voltage was increased, the tip became blunter. This may have been due to tip sputtering, which would have increased as the voltage was increased (as the tip was run to higher current values), thereby accentuating the effect.

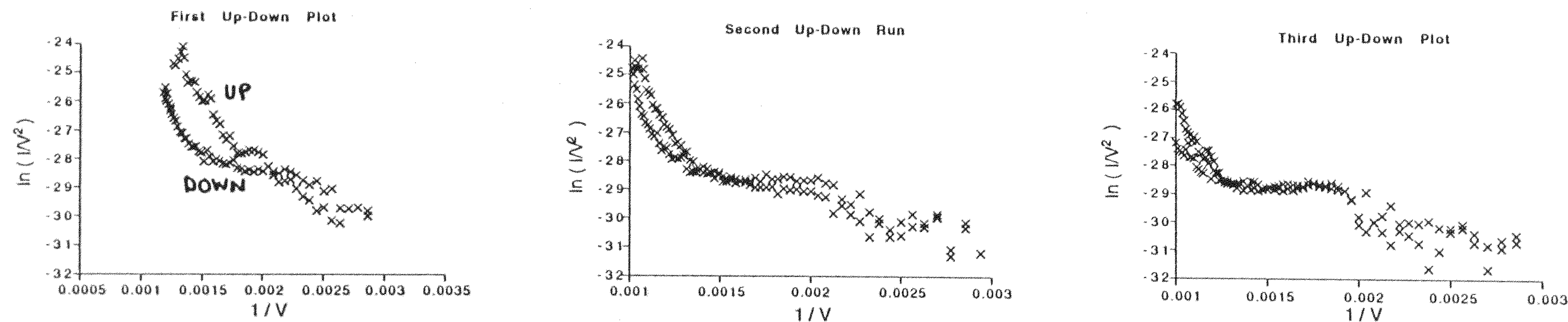


Figure 4.8 - Up-Down Hysterisis Plots Obtained in Good Vacuum System
In the improved vacuum, it is clear that the hysterisis effect was not as pronouced as in the poor vacuum system. In addition, the effect was not accentuated as the tip was run to higher current values - in fact, the effect decreased as the maximum current to which the tip was run was increased. The first plot exhibits a small amount of hysterisis (probably due to removal of adsorbates on first run-up plot), but this is much reduced for subsequent plots.

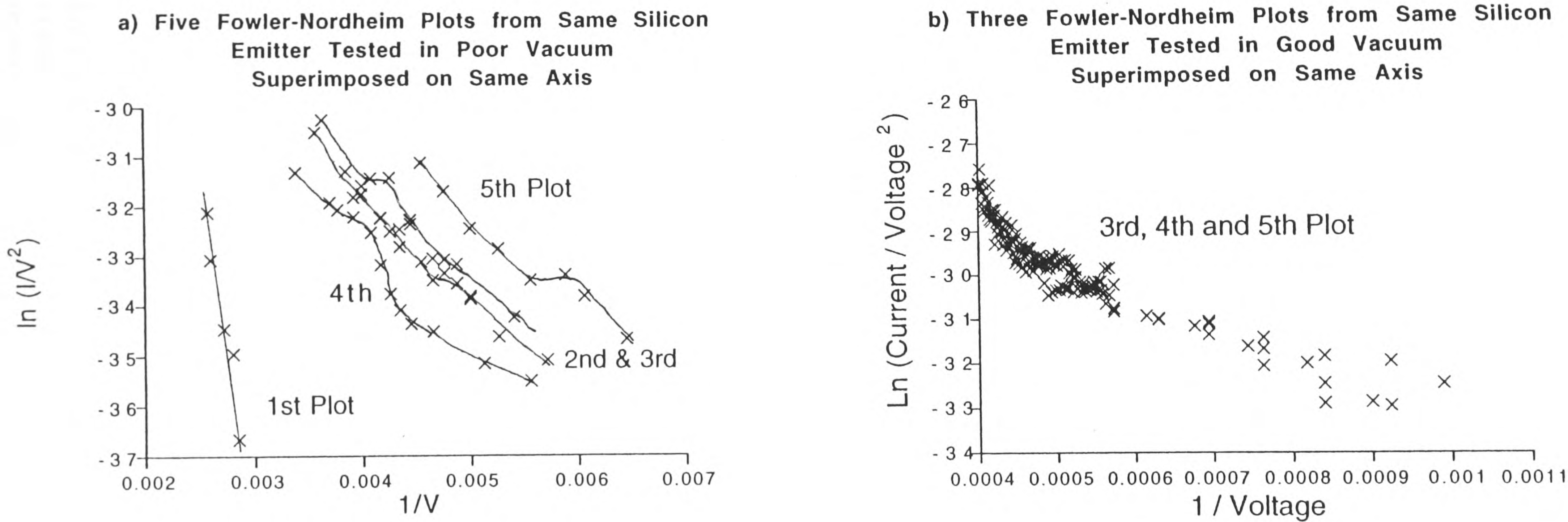


Figure 4.11 - Plots from Same Emitter Superimposed on Same Axis, for Both Poor and Good Vacuum

a) This figure shows that when successive runs were taken from the same tip in the poor vacuum, the second plot was shifted to the right of the first plot, corresponding to a decrease in starting voltage. Subsequent plots were positioned either to the left or to the right along the axis. Differences in the shape, slope and intercept of the FN plot were also observed from run to run.

b) In the good vacuum, the reproducibility from tip to tip was much improved. This plot shows 3 separate plots from the same emitter, supeimposed on each other. The plots shown here are very similar in position along the x-axis. All 8 plots taken from this tip are shown in Figure 4.12 (not superimposed).

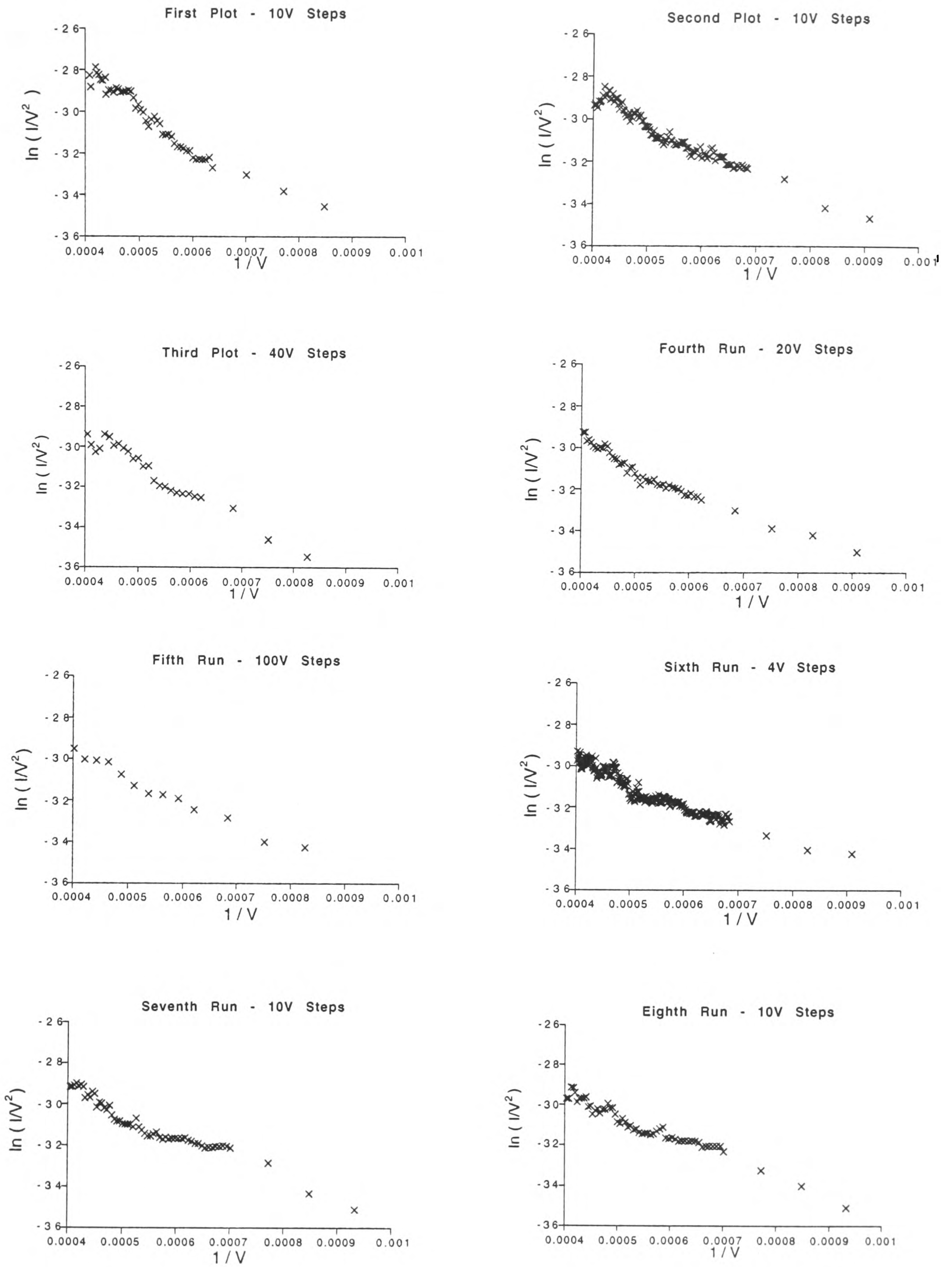


Figure 4.15 - Ramp Rates in Improved Vacuum
8 plots were taken from one tip, using different voltage steps (between 10V and 100V). Changing the ramping rate appeared to have little effect on the shape and position of the plots, unlike the situation in the poor vacuum.

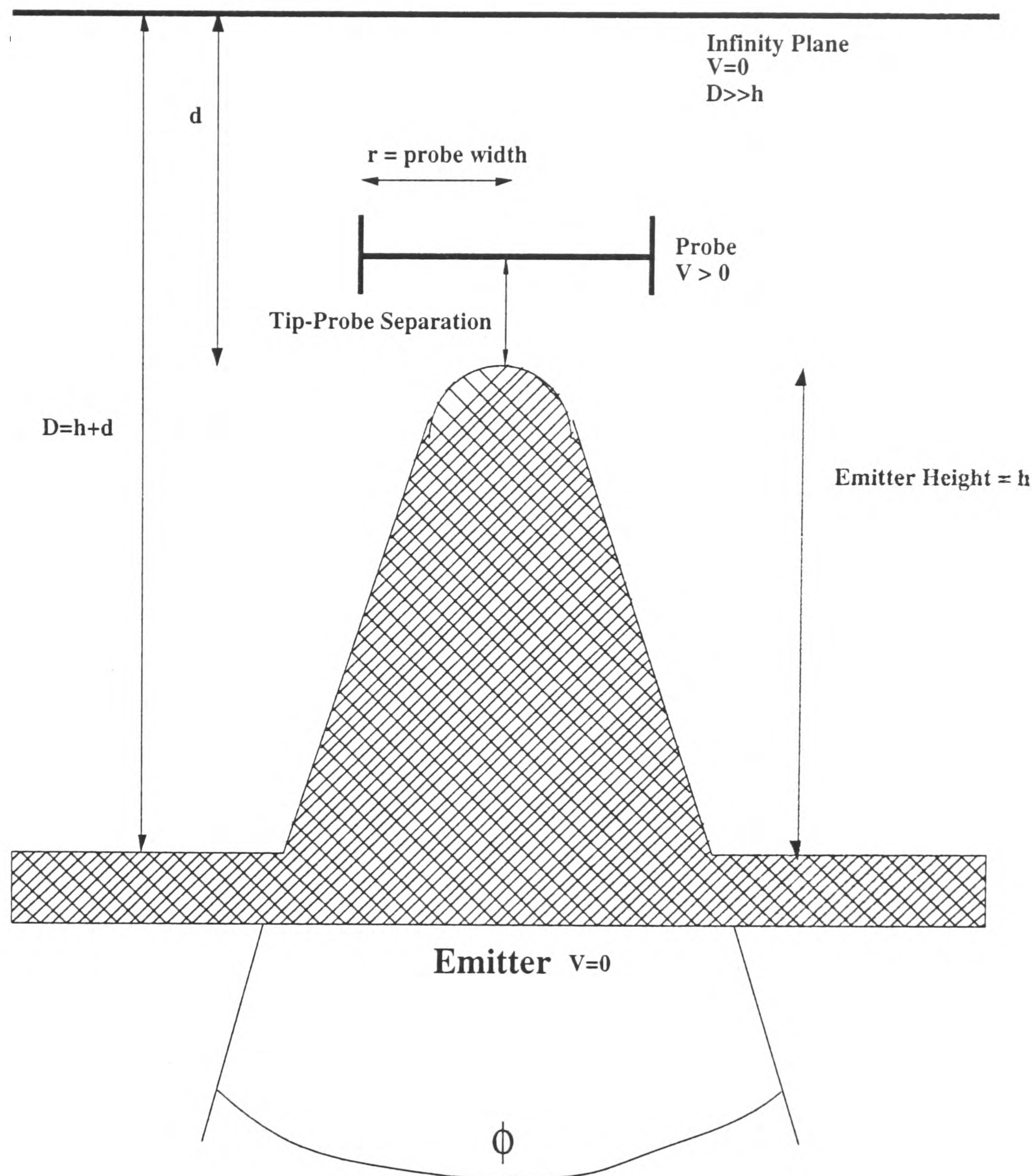


Figure 4.16 - Configuration of Tip-Probe Arrangement used by D.Nicolaescu for computer modelling of situation in 505 SEM
The following assumptions were made during modelling:

Tip angle = 80°, which is closest to geometry tested in 505 SEM (4 sided pyramid)
Work function = 4.5eV
Emitter radius = 5nm
Emitter height = 5μm
Probe width = 1μm (Initially, modelling was carried out with a probe width of both 1μm and 2μm. However, little difference was found between the 2 cases, so only results for 1μm separation are shown here.)

(Ref: D.Nicolaescu, *Private Communication,* (1996))

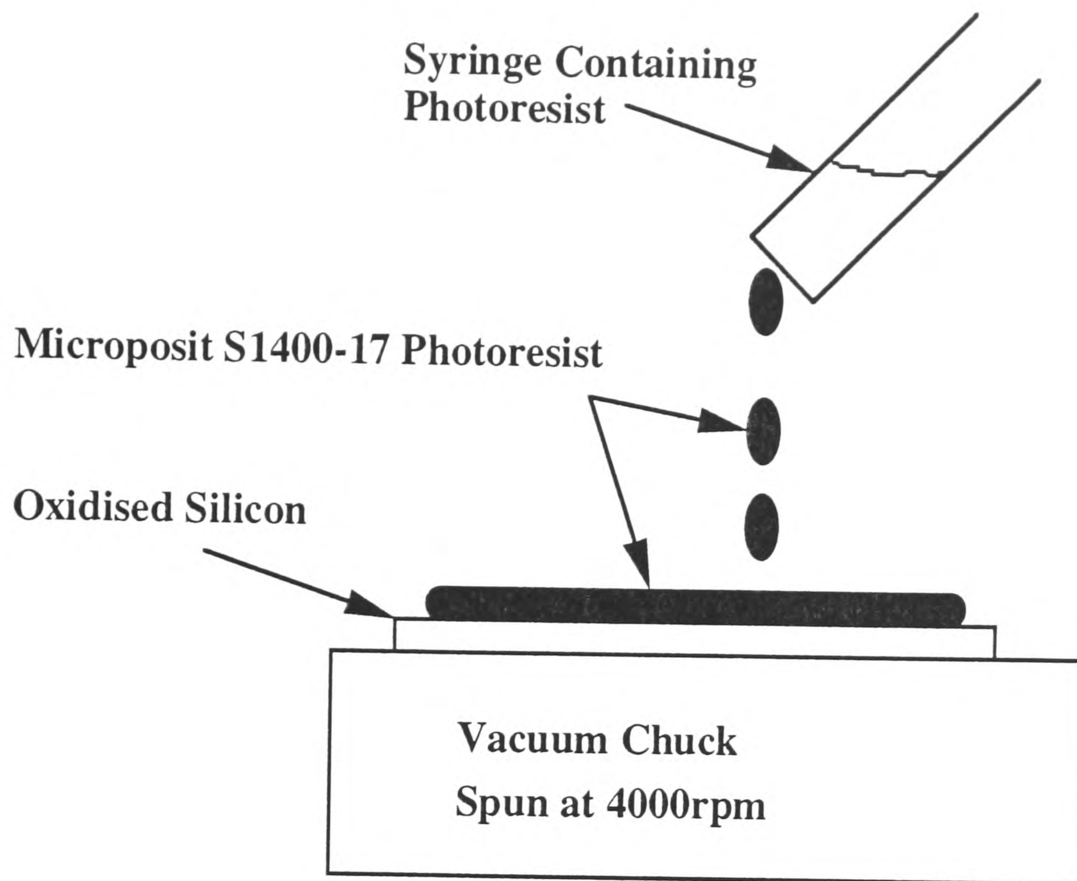


Figure 5.2 - Diagram Showing Spinning of Photo-Sensitive Polymer onto Silicon Surface

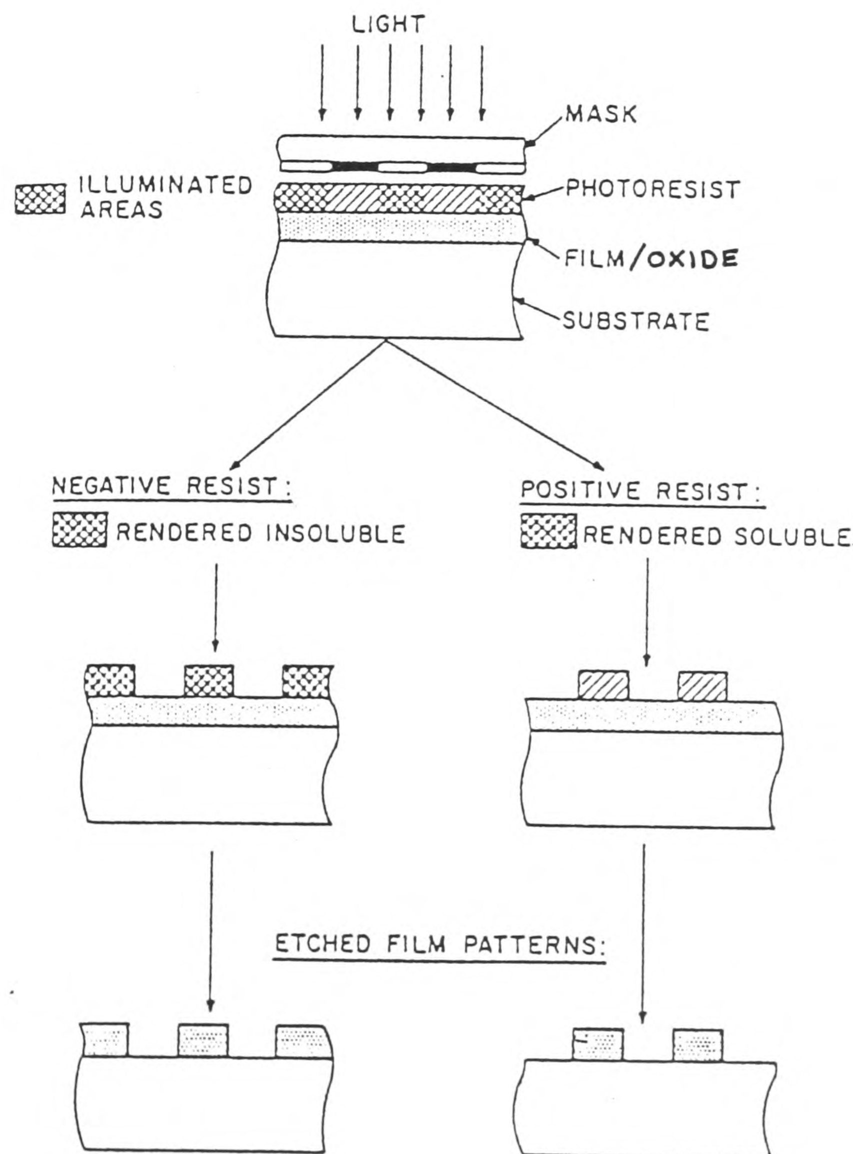
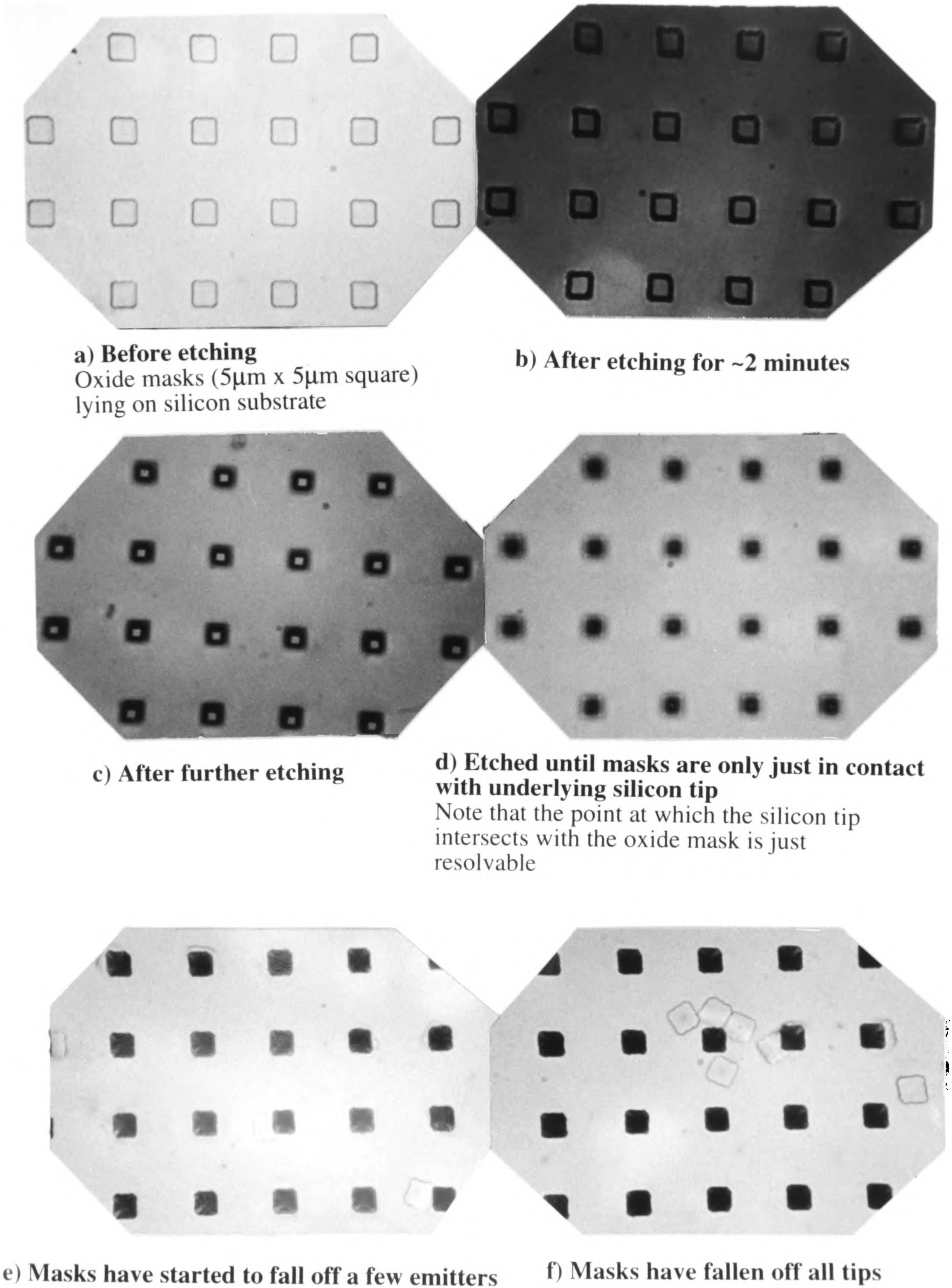


Figure 5.3 - Diagram Demonstrating Positive Resist Process and Difference versus Negative Resist Process



a) Before etching
Oxide masks (5µm x 5µm square) lying on silicon substrate

b) After etching for ~2 minutes

c) After further etching

d) Etched until masks are only just in contact with underlying silicon tip
Note that the point at which the silicon tip intersects with the oxide mask is just resolvable

e) Masks have started to fall off a few emitters

f) Masks have fallen off all tips

Figure 5.6 - Optical micrographs showing field emitter arrays at different stages of chemical wet etching process
Note that the intersection of the underlying silicon tip with the oxide mask, decreases as the etch time increases. At the point where the oxide masks fall off, the tips are believed to be ~2.5µm high.

1) Specimen Cleaving

Arrays of tips could be examined by cleaving a very small section from the larger substrate. This procedure was carried out using a diamond scribe and tweezers. Samples had to be <1mm square, in order to fit onto a TEM grid. However, it was difficult to obtain such a small sample intact - the tips were often crushed during cleaving, in which case a new sample had to be prepared.

2) Examination under Optical Microscope

The cleaved samples were then examined under the optical microscope, in order to to ensure that the majority of tips had not been crushed and that there was a large population of tips present on the upper surface. It was important to obtain a cleaved section which could stand vertically on its edge, as in Figure 5.7. When placed in the TEM, the electron beam had to be able to pass straight through the tips which were standing proud of the surface.

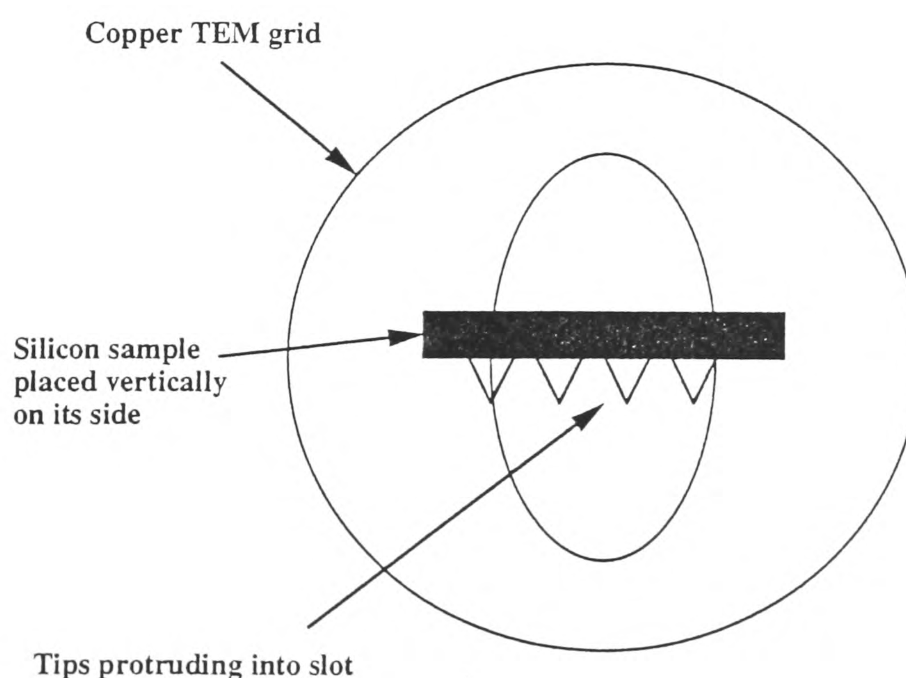
3) Sample Glued to TEM Grid

The cleaved sample was then stuck down onto a copper slit grid using super glue. The sample had to hang over the slit, so that the tips were visible to the electron beam - see the diagram below. If excess glue was placed on the copper grid, capillary action pulled the sample onto the glue, covering the tips with glue. Excess glue on the sample caused charging when examined in the TEM.

4) Insertion into TEM

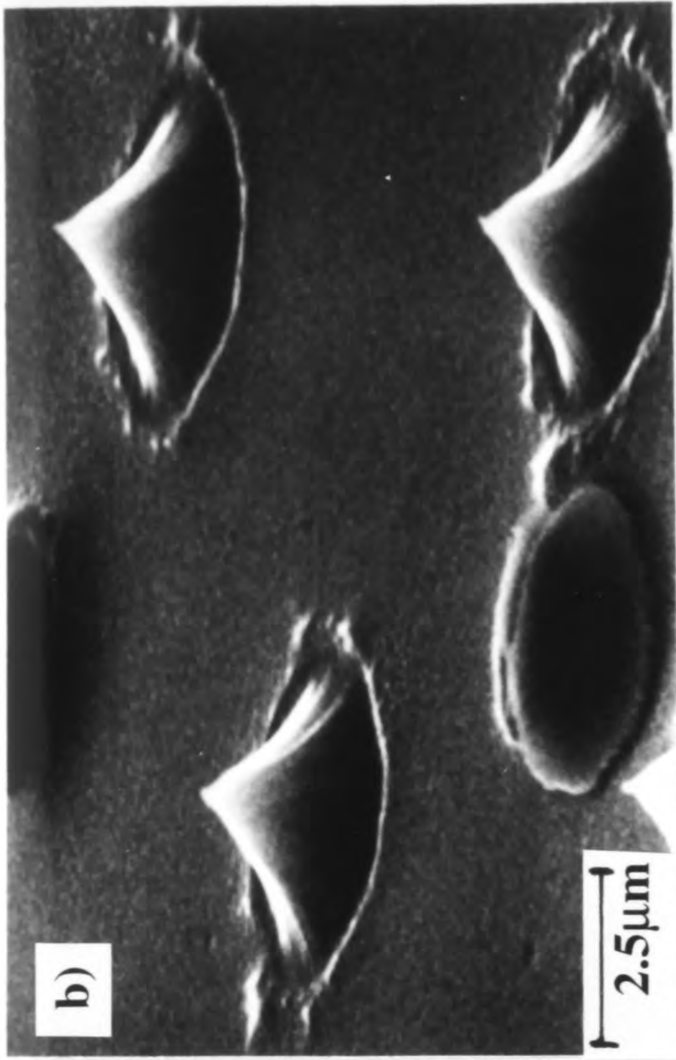
Prior to insertion into the TEM, the specimen was arranged in the holder so that the sample edge lay approximately parallel to the tilt axis of the holder. This allowed the specimen to be tilted to the maximum degree possible, thereby allowing examination of the greatest number of tips possible.

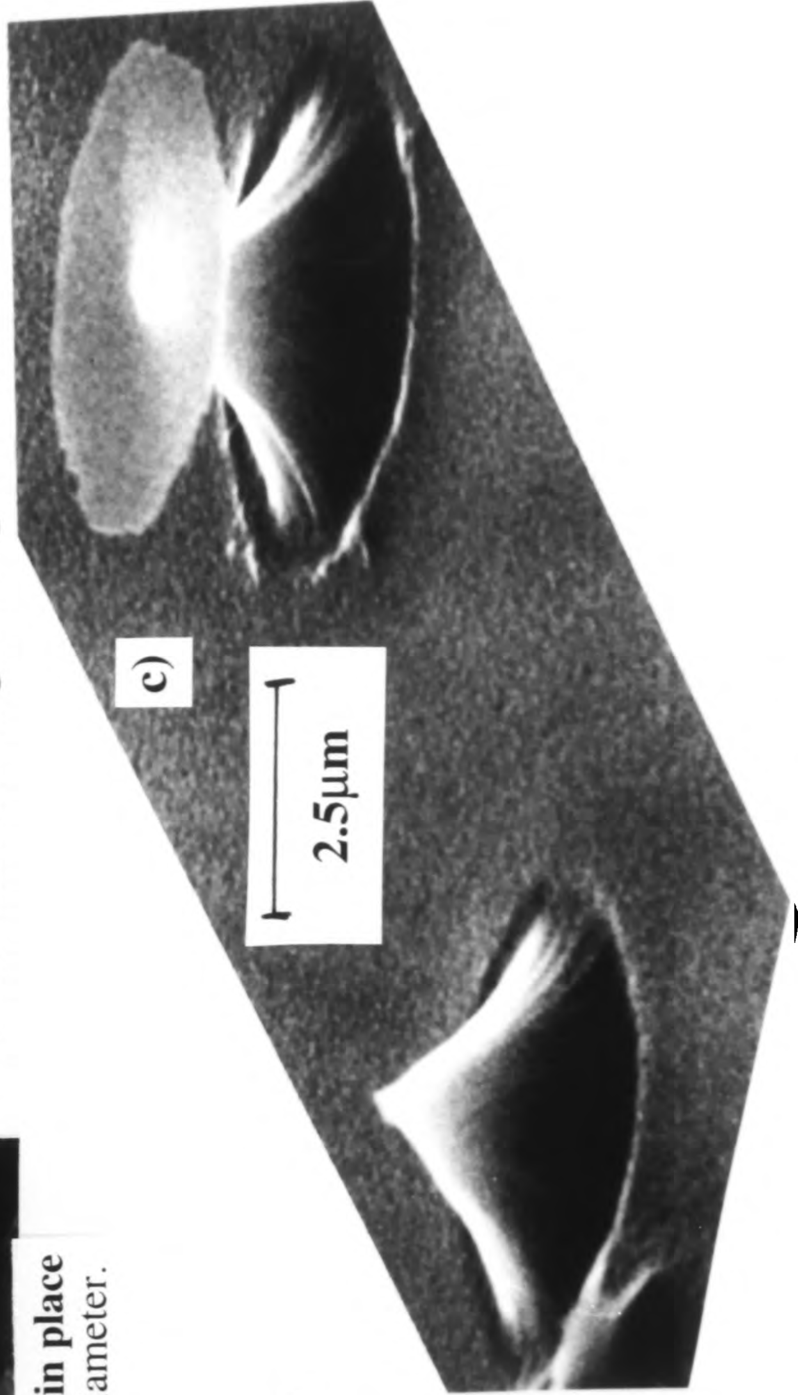
a) Outline of Steps Required to Prepare TEM Samples



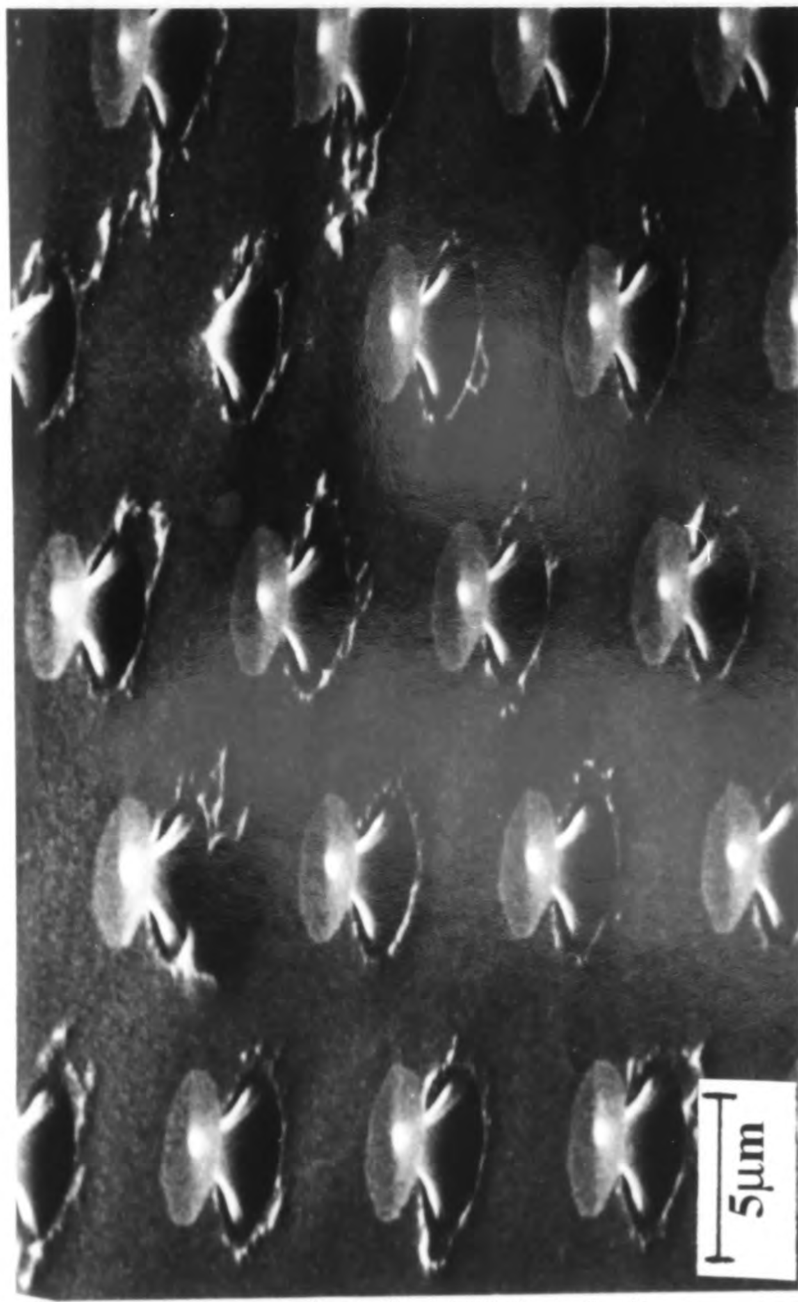
b) Diagram Showing How Specimen had to be Placed onto TEM Grid

Figure 5.7 Preparation of TEM Samples from Field Emission Arrays (FEAs)

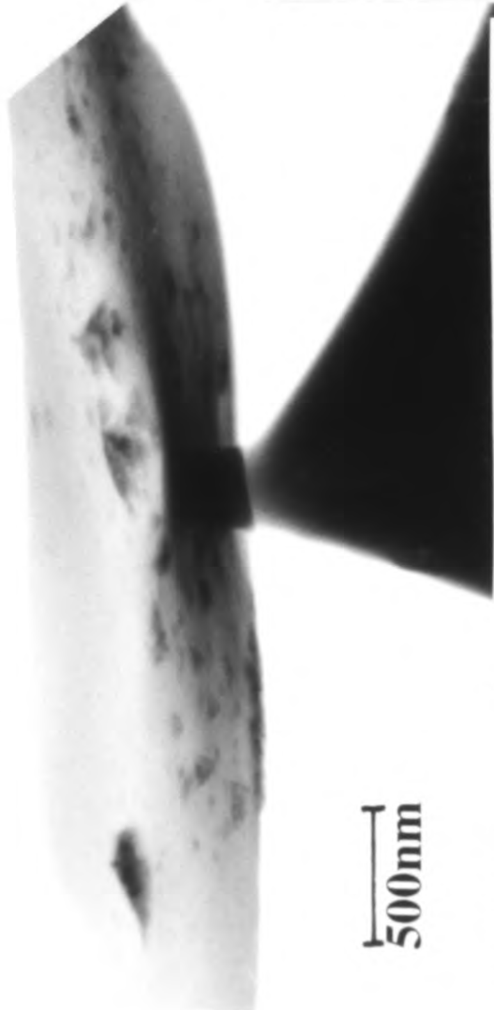




b) and c) SEM image of emitters with and without masks at higher magnification



a) SEM image of field emitter array - most masks still in place
Area of silicon tip still in contact with mask is ~1μm in diameter.

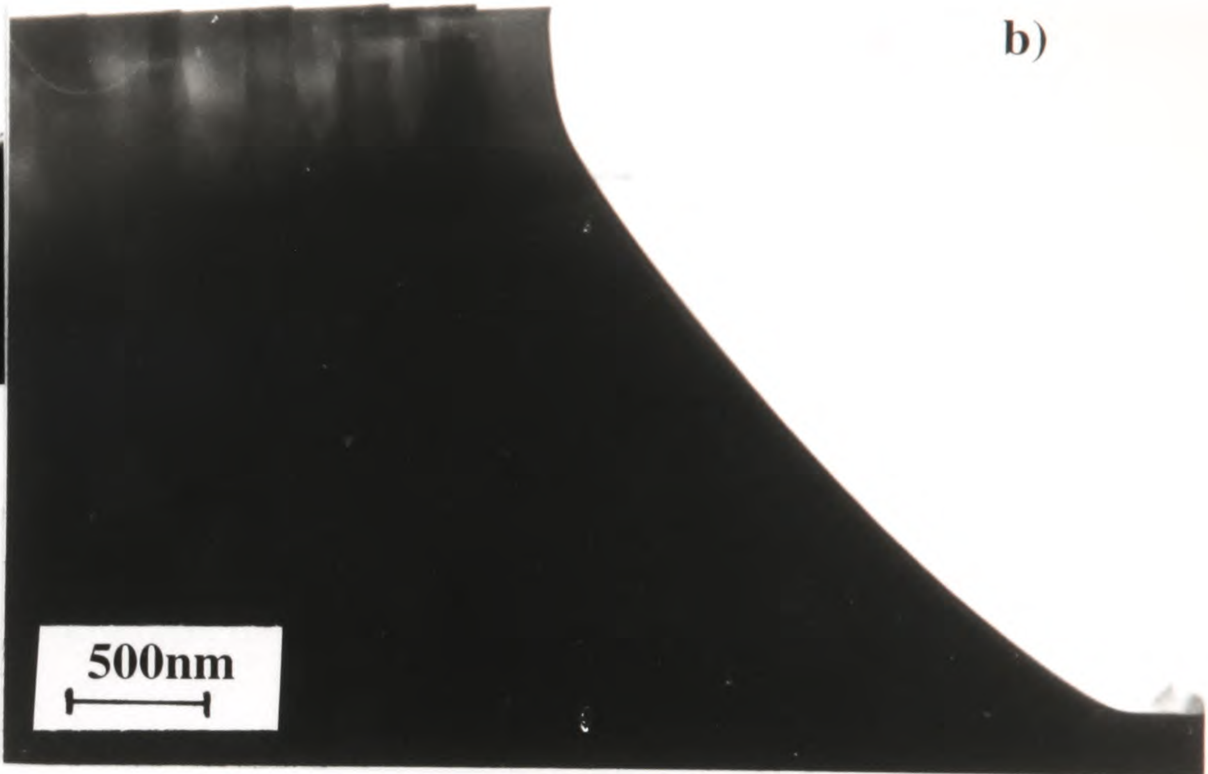


d) TEM image showing tip with mask still in place
Note that area of silicon in contact with oxide mask is much smaller than in previous images

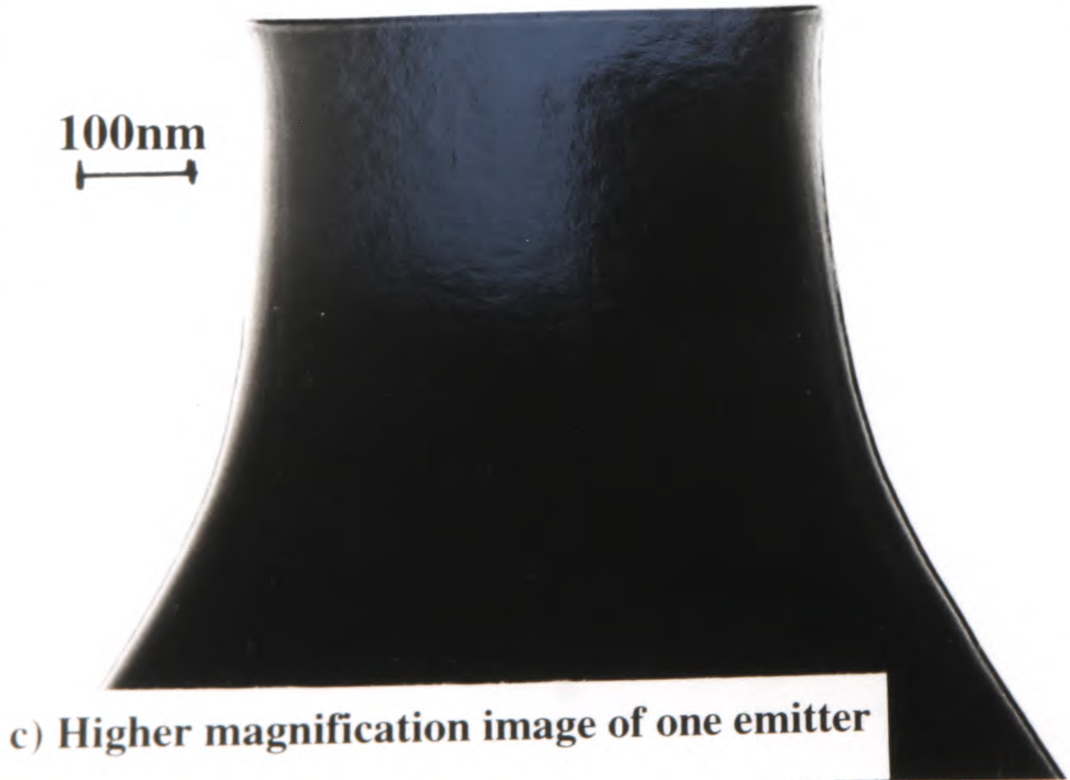
Figure 5.8 - SEM and TEM micrographs of emitters before and after the mask has fallen off
Note that in the SEM images, the masks used to produce the tips here were round, whereas only square masks were used for the work reported in this thesis.

5.9 - TEM images of flat-topped emitters

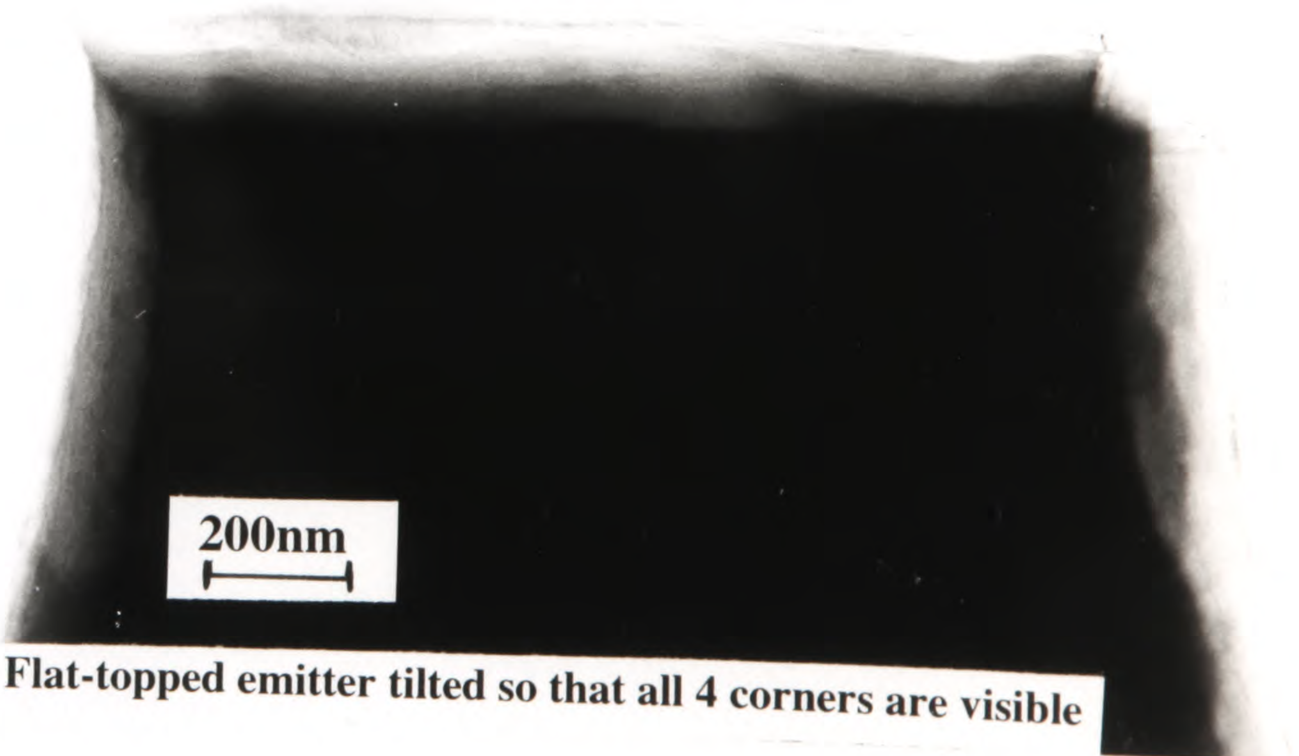
a) Low-magnification image of several flat-topped emitters
All tips have the same basic height and geometry.



b) Higher magnification of one emitter
Note the near-vertical sides in the region of the apex, versus sloping sides lower down the emitter.



c) Higher magnification image of one emitter



d) Flat-topped emitter tilted so that all 4 corners are visible

a) Image taken across top of flat-topped tip
Note that 2 opposite corners are very similar in geometry and radius

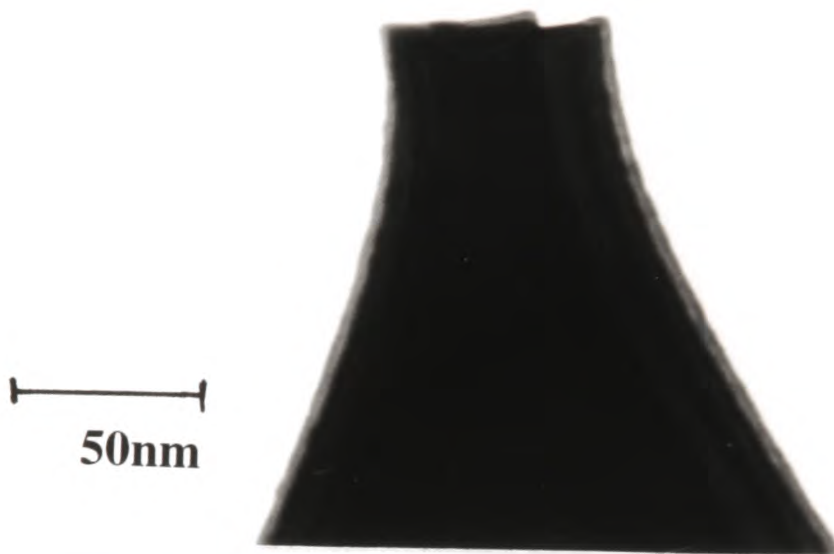
100nm

b) Higher magnification of one corner
Note that tip radius is ~5nm

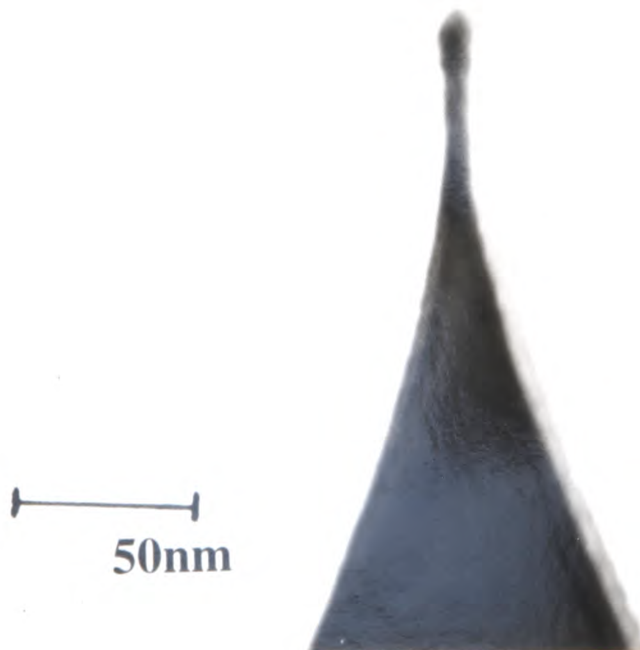
Note that the the radius and geometry of each of the 4 corners of this emitter were found to be very similar. This was also true from emitter to emitter.

Figure 5.10 - TEM micrographs showing sharp corners of flat-topped emitters

a) Tip 1 - Wide flat-topped emitter observed at centre of sample, where etch rate was the slowest (Top is ~0.2μm wide)



b) Tip 2 - Narrower flat-topped emitter observed closer to edge of sample, where etch rate was faster (Top is ~0.04μm wide)

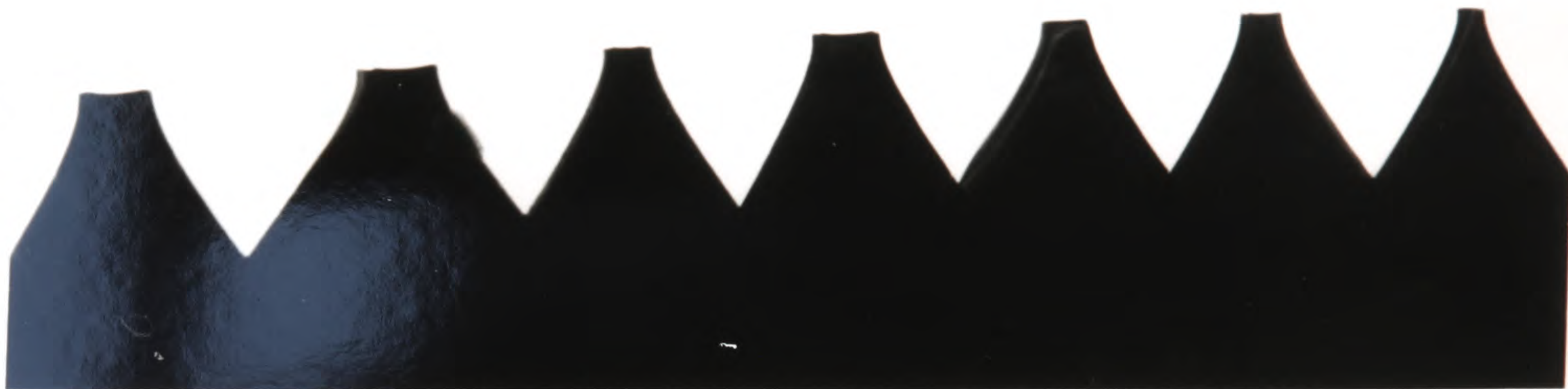


c) Tip 3 - Flat-topped emitter at edge of sample has been etched almost to a point
Note that this tip is close to the ideal tip geometry (Top is ~0.01μm wide)

Figure 5.11 - TEM micrographs of emitters observed at different positions of wafer
The difference in the width of the flat-topped emitters across the sample demonstrates the variation in etch rate across the sample.

a) Etching process stopped before any of the oxide masks from the array had fallen off

Note that the tip-to-tip uniformity is much better than for the FEA shown in **b)**. The height and overall geometry of all tips shown here is very similar from tip-to-tip. All tips have a near-vertical section at the tip apex.



b) Etching process stopped after most of the oxide masks from the array had fallen off

Note that the tip-to-tip uniformity is poor, demonstrating the difference in the etch rate from tip-to-tip, in addition to varying from the centre to the edge of the sample. Both the tip geometry and tip height vary from tip-to-tip. Some of the emitters are flat-topped (due to being under-etched), whereas some are point-like and others are quite blunt (due to over-etching). Some emitters are much lower in height due to over-etching.

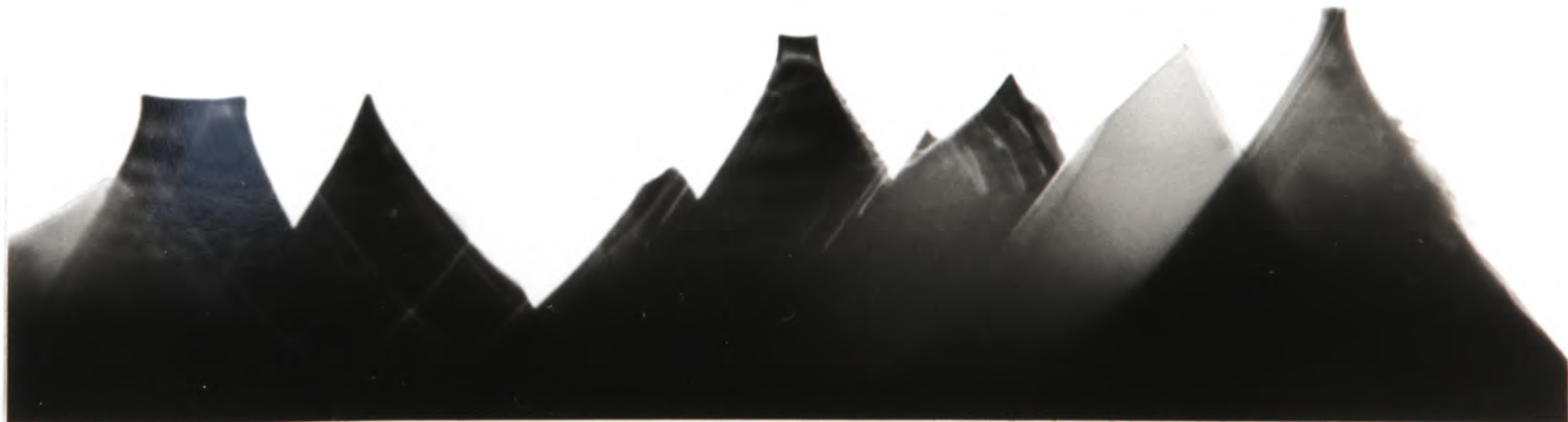


Figure 5.12 - TEM micrographs comparing tip-to-tip uniformity for an under-etched FEA and an FEA etched until the oxide masks have started to fall off

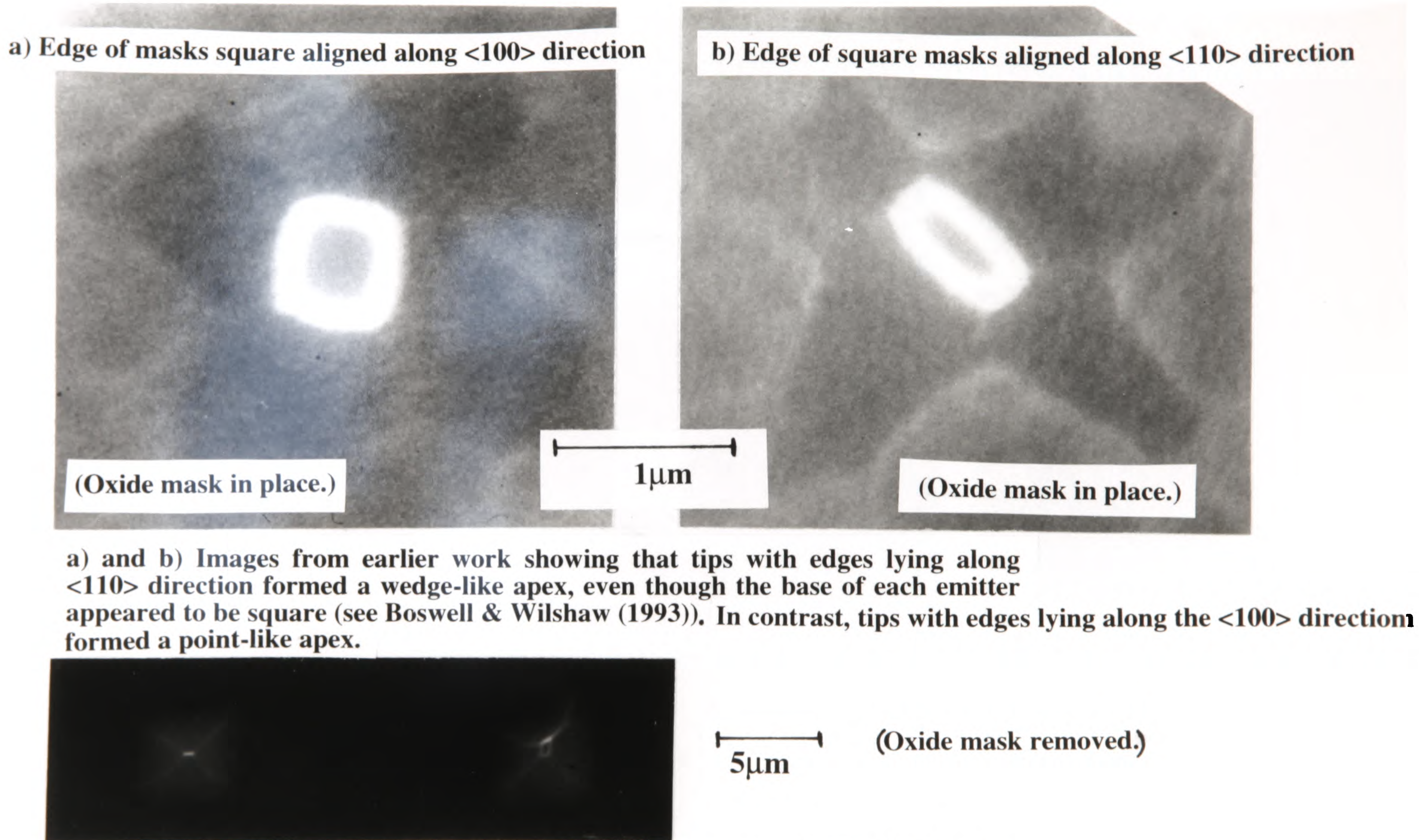
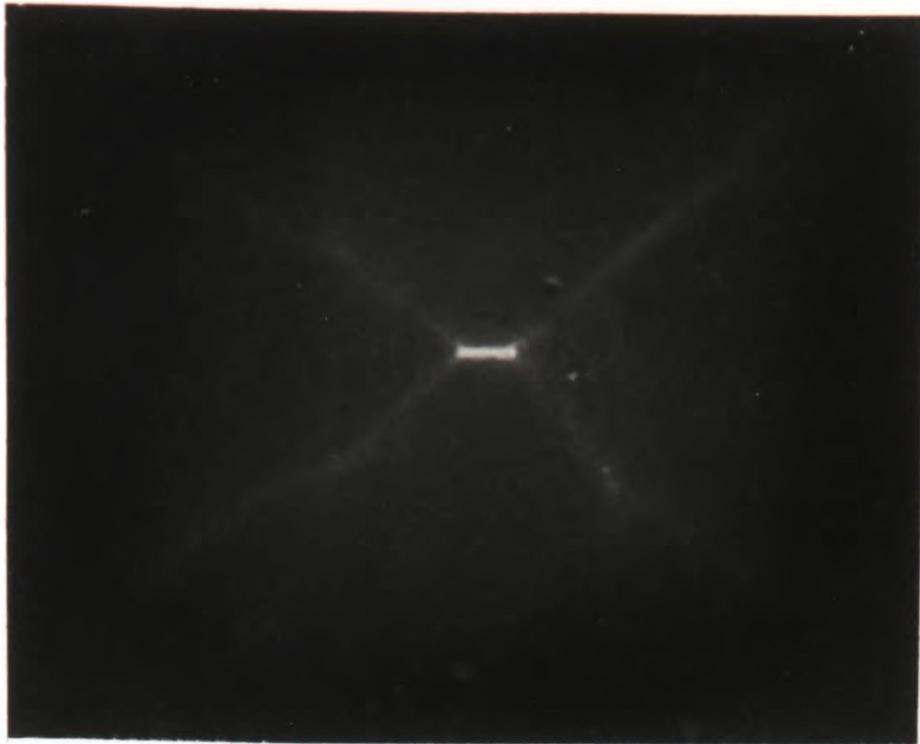
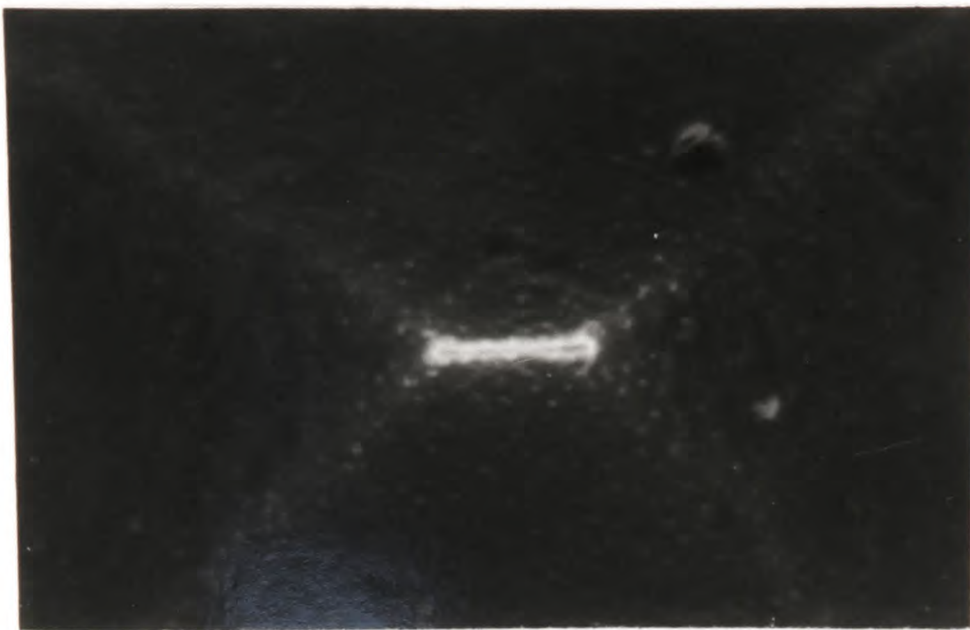


Figure 5.13 - SEM micrographs demonstrating both square and wedge-like apexes



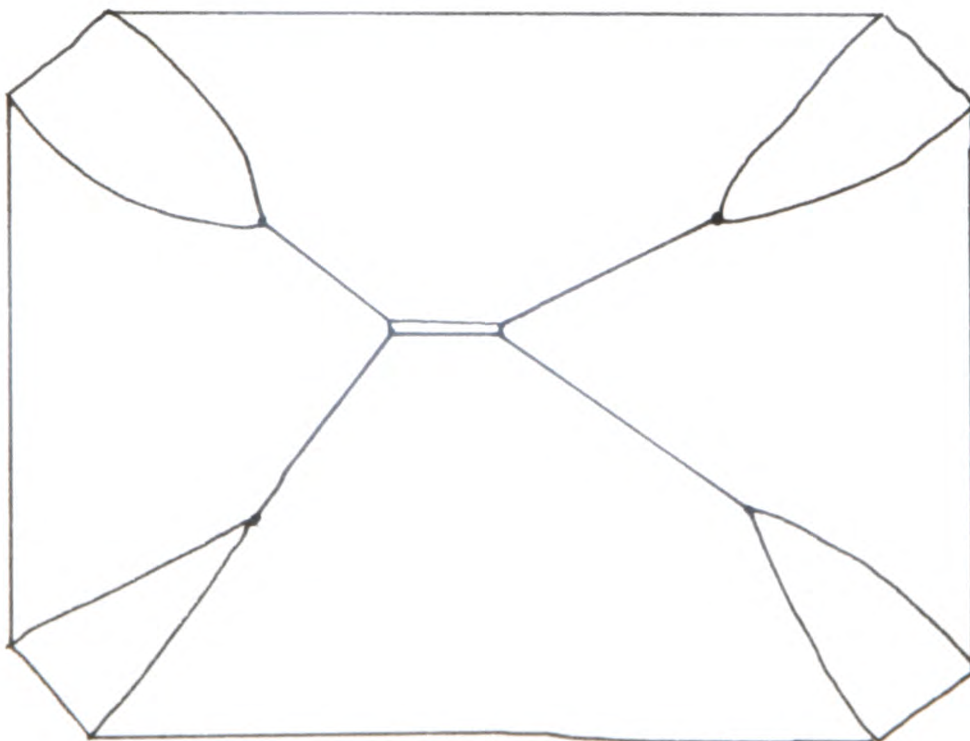
$1\mu m$

a) Image of one emitter showing overall emitter geometry



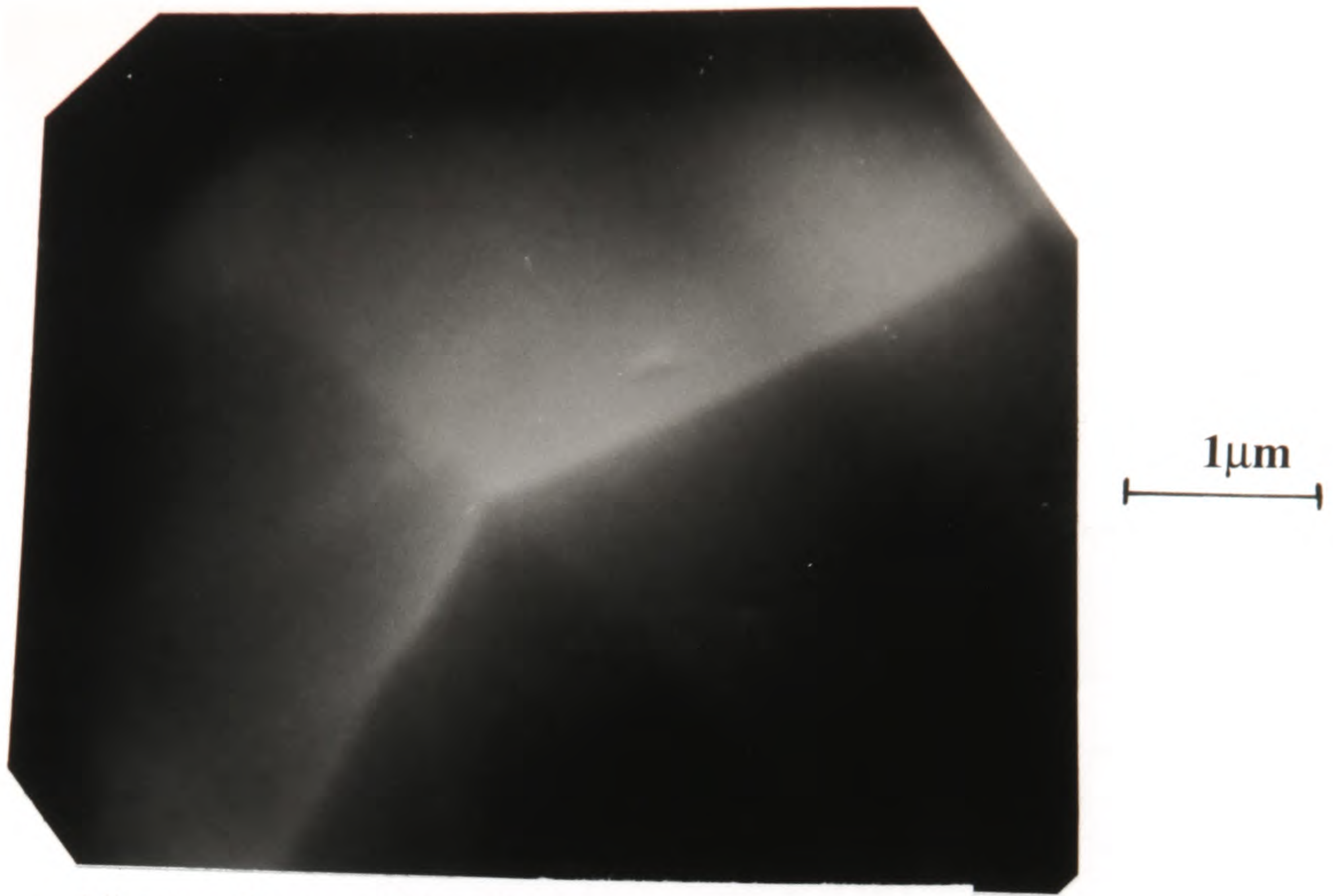
$0.5\mu m$

b) Higher magnification of wedge-like apex

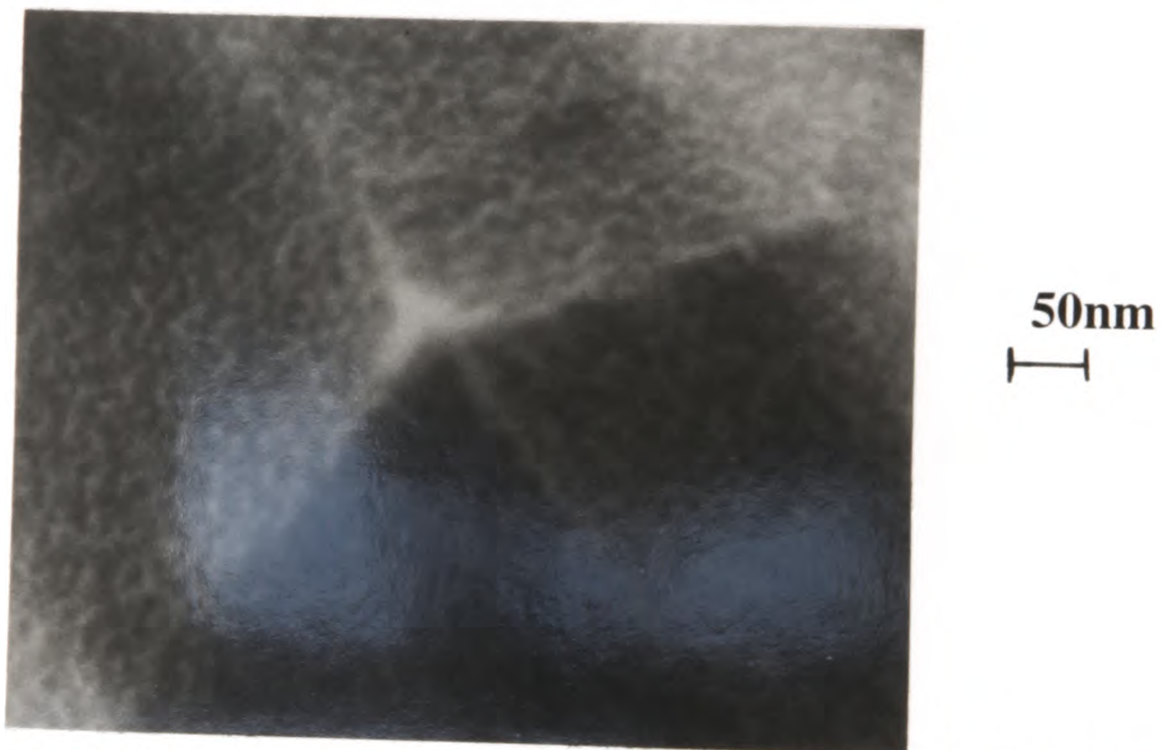


c) Schematic diagram demonstrating overall geometry of emitter

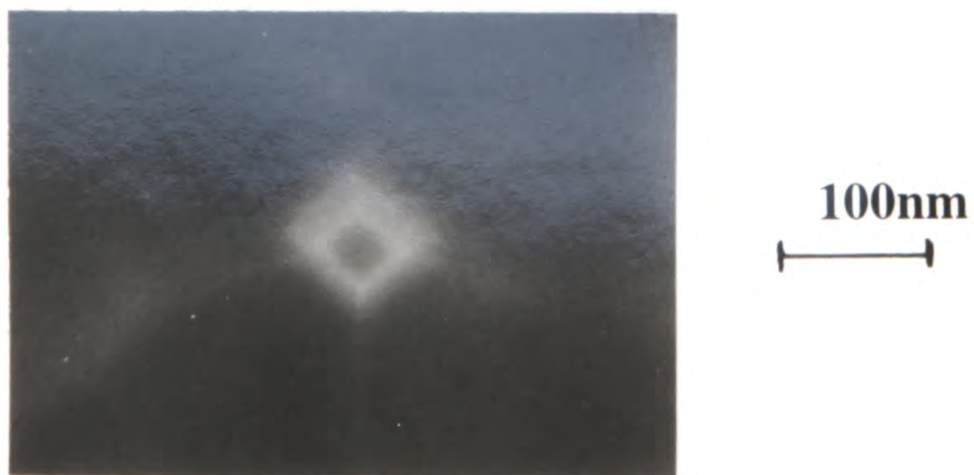
Figure 5.14 - SEM micrographs of wedge-shaped emitter apexes



a) Image of one emitter showing overall geometry



b) Higher magnification image of tip apex showing that it is a point



c) Image of point-like apex just before forming a point
(Oxide mask still in place.)

Figure 5.15 - SEM micrographs of point-like emitter apexes

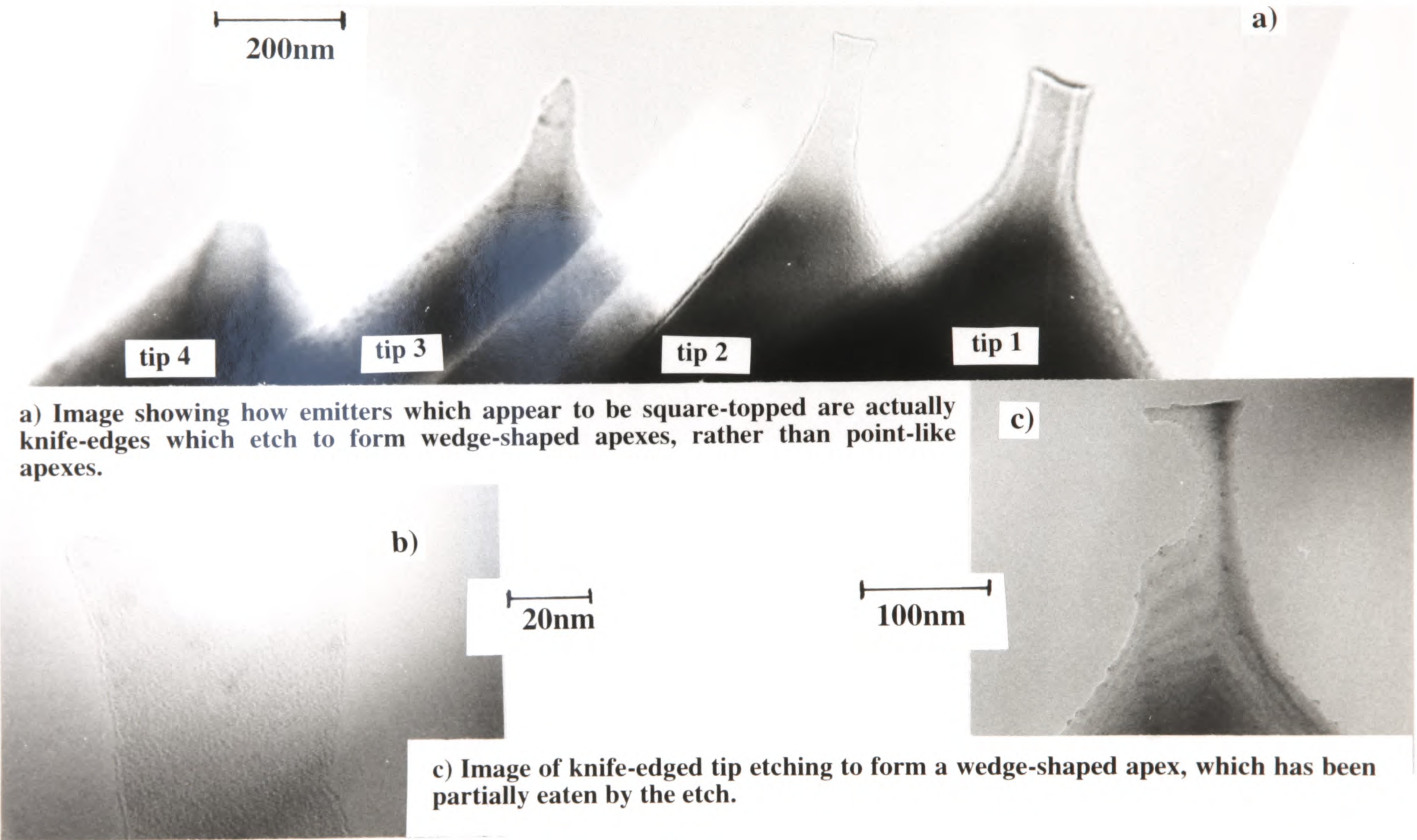


Figure 5.16 - TEM micrographs of formation of wedge-shaped emitters from knife-edged emitters

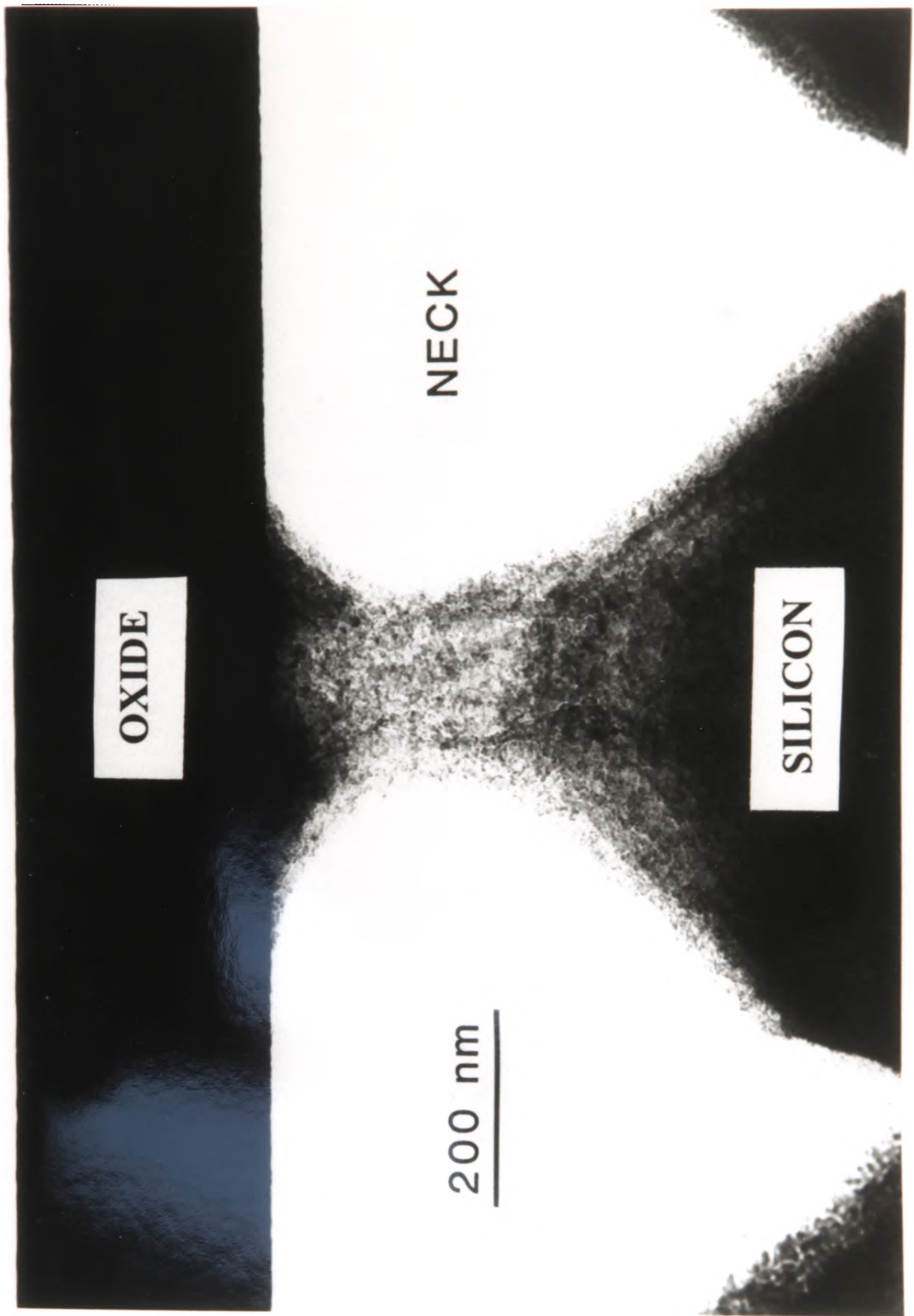


Figure 5.17 - TEM image of silicon tip being etched at a point beneath the point of contact of the tip with the oxide mask
Depending on the etch conditions, the silicon tip could be etched at a faster rate at a point just below the point at which the oxide mask made contact with the underlying tip, than at the point where it did make contact. If this occurred, the geometry of the resulting tip was slightly different to that obtained when the tip was etched at the exact point where the tip met the oxide mask.

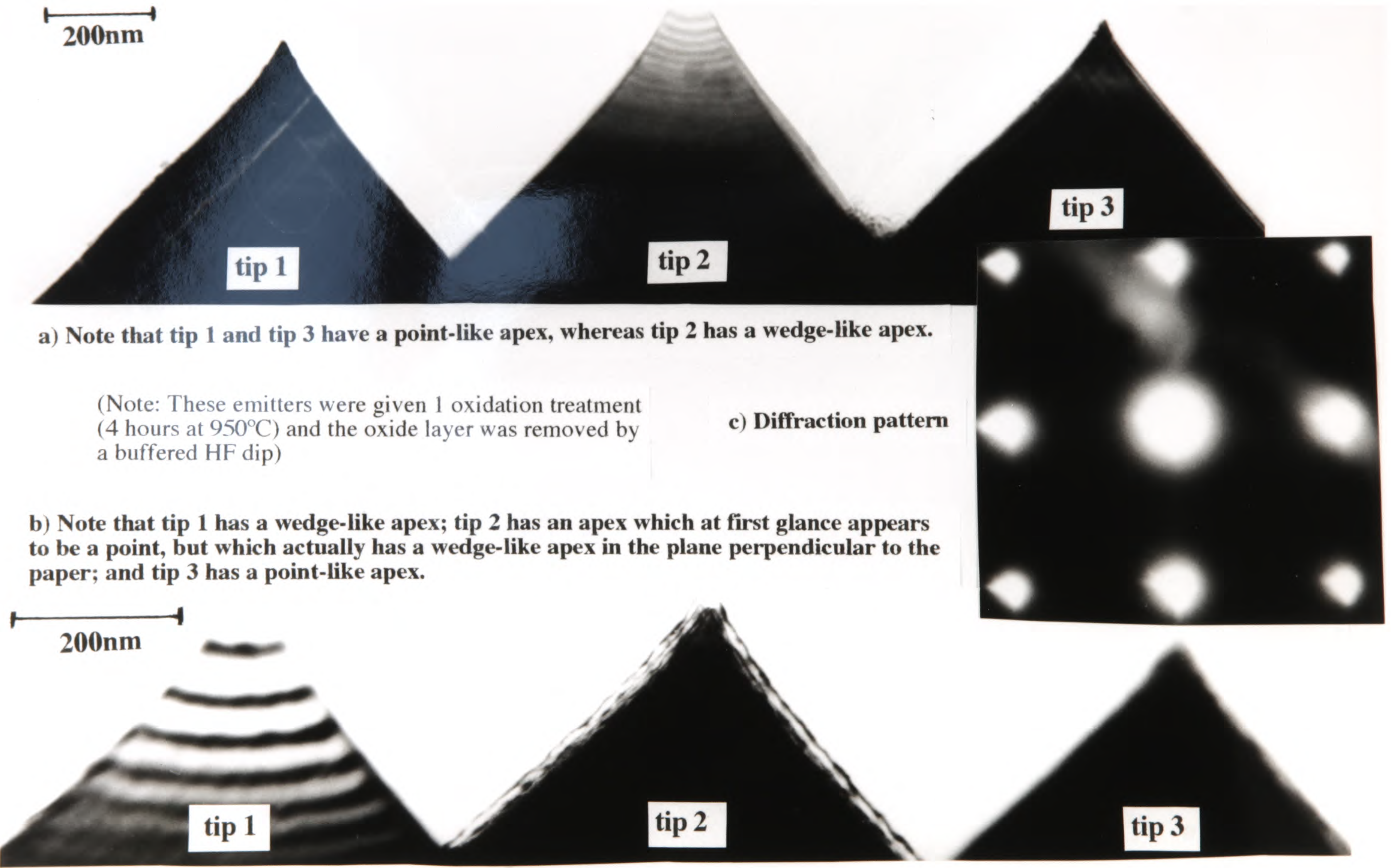
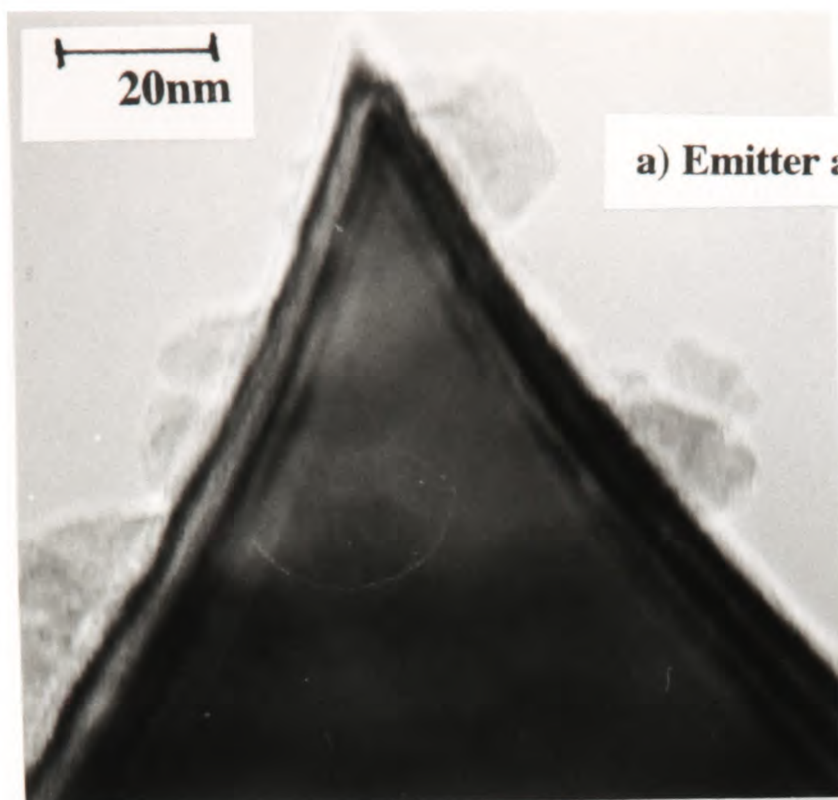
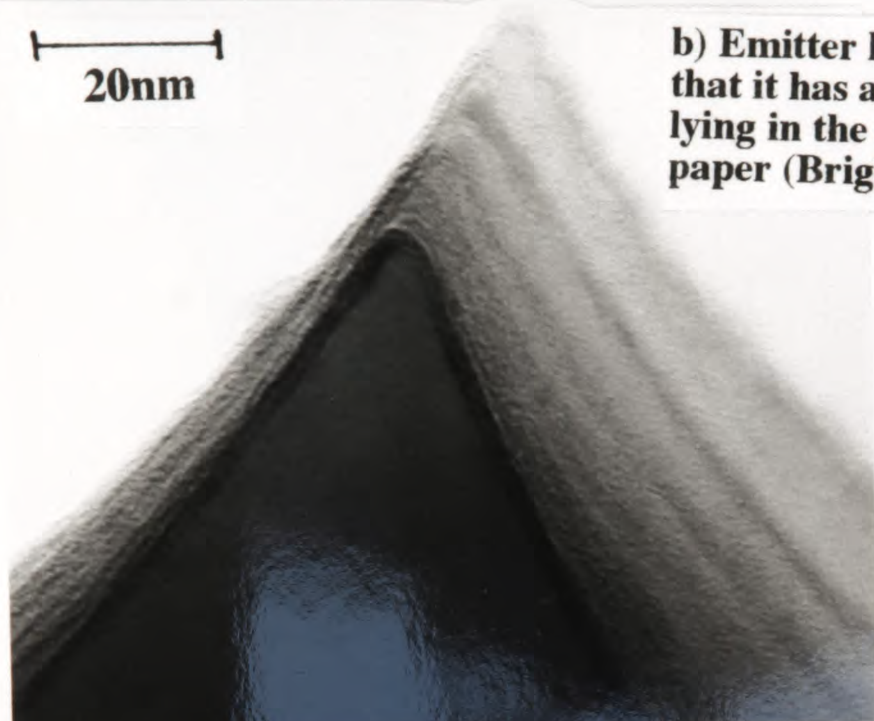


Figure 5.18 - TEM micrographs demonstrating how morphology of tip apex varied between being wedge-shaped and point-like, from neighbour to neighbour

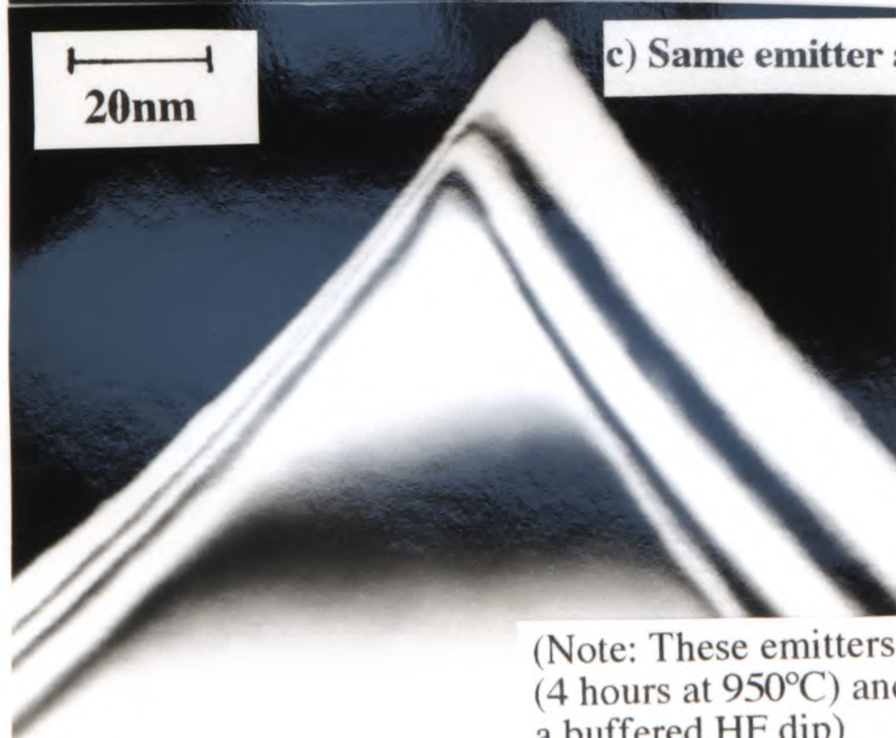


a) Emitter appears to have a point-like apex

(Diffraction pattern for a) was same as for diffraction pattern shown in Figure 5.18c.)



b) Emitter has been tilted and it is now clear that it has a wedge-like apex, with a ridge lying in the direction perpendicular to the paper (Bright-Field image)



c) Same emitter as in b), but Dark-Field image

(Note: These emitters were given 1 oxidation treatment (4 hours at 950°C) and the oxide layer was removed by a buffered HF dip)

Figure 5.19 - Higher magnification image of emitter which initially appears to have a point-like apex, but which actually has a wedge-like apex.
Note that tip is similar to tip 2 in Figure 5.18b.

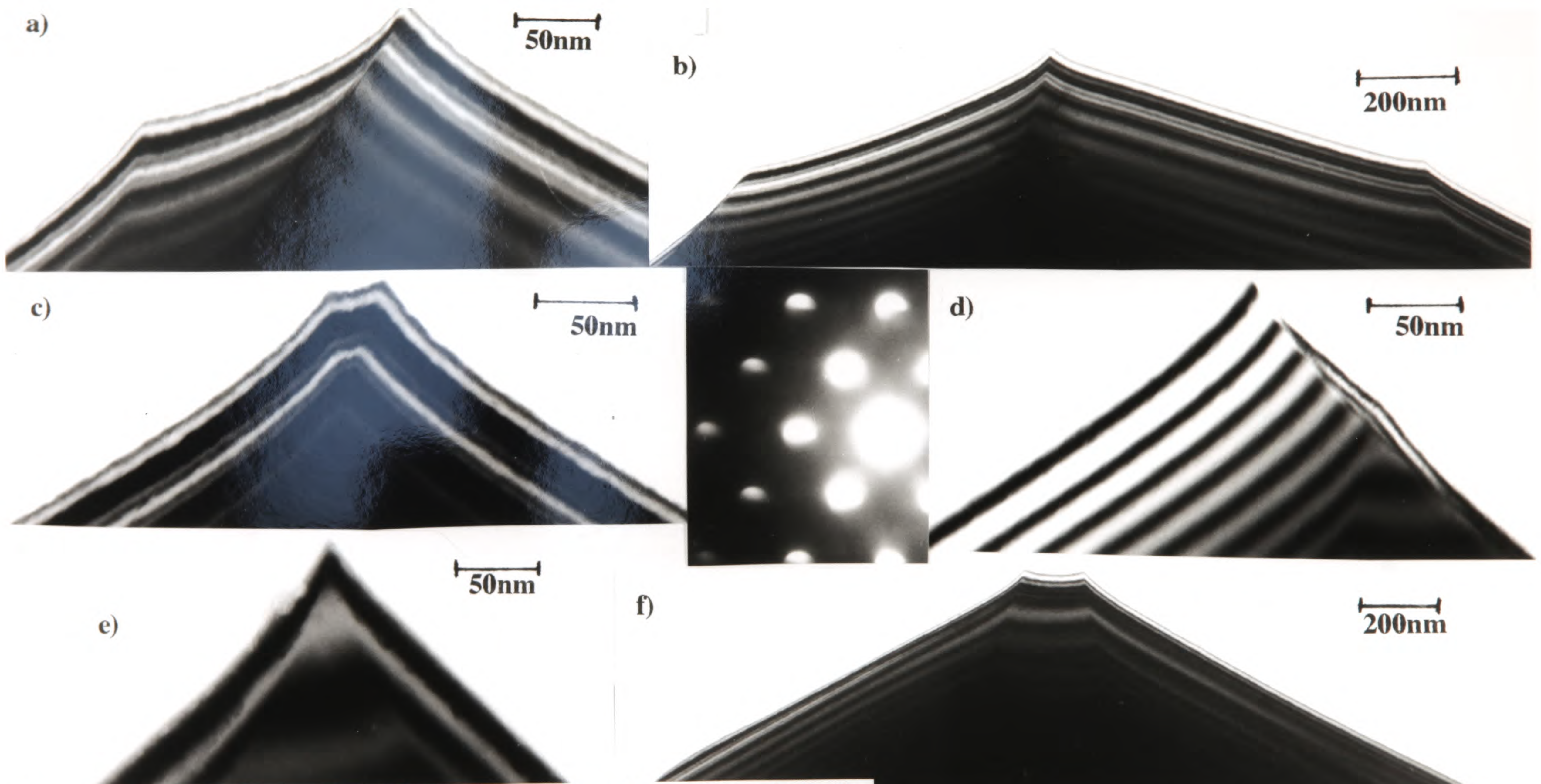
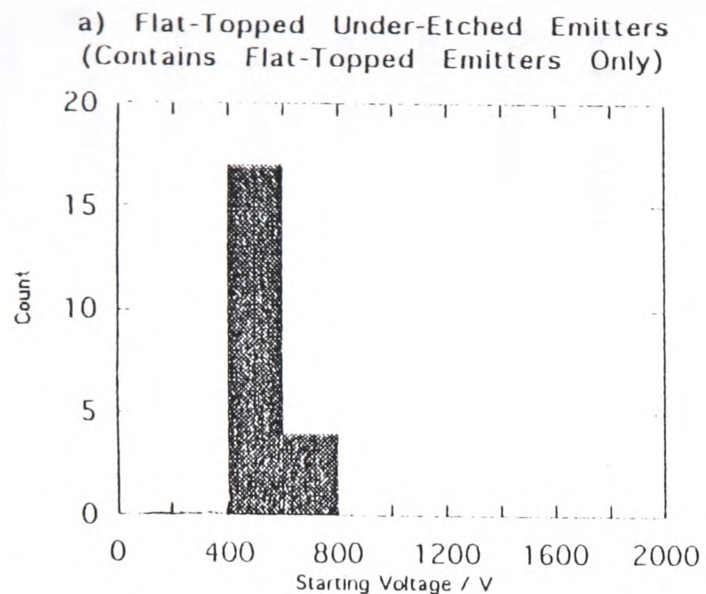
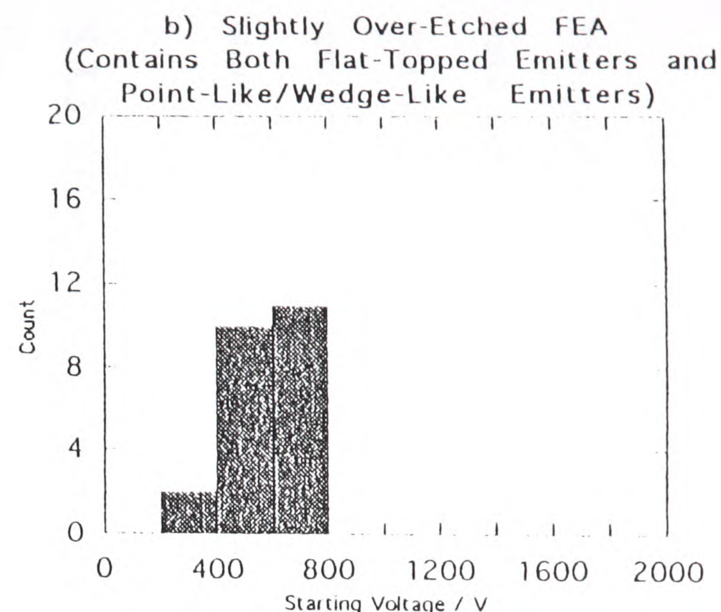
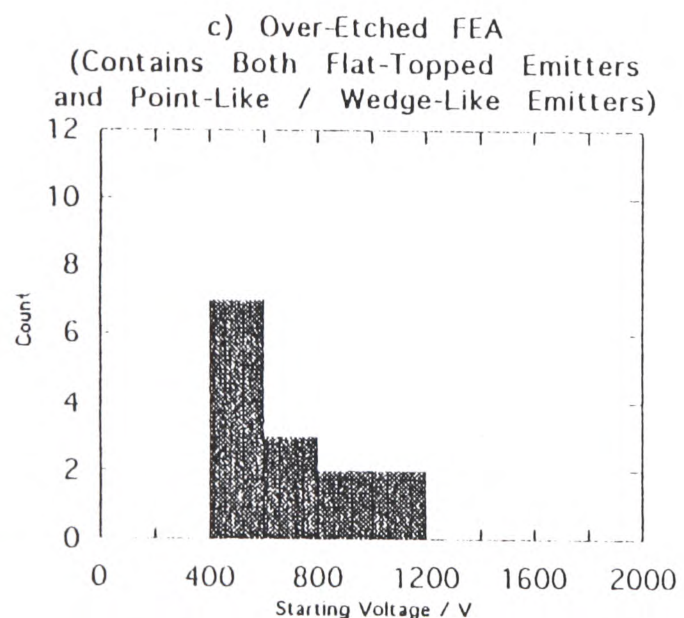


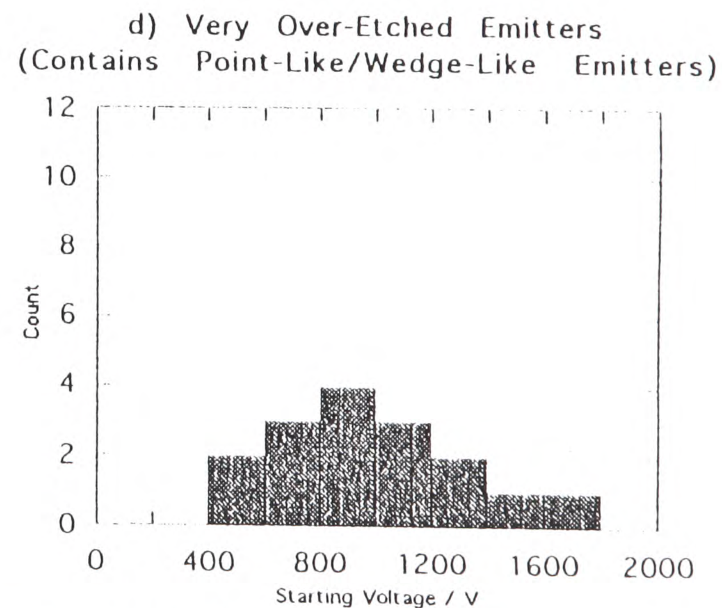
Figure 5.20 - TEM micrographs of 6 neighbouring over-etched tips demonstrating difference in tip morphology from tip-to-tip across the sample
Note that these images were taken with the sample aligned along a different crystallographic direction to that used for previous figures

(Note: These emitters were given 1 oxidation treatment (4 hours at 950°C) and the oxide layer was removed by a buffered HF dip)

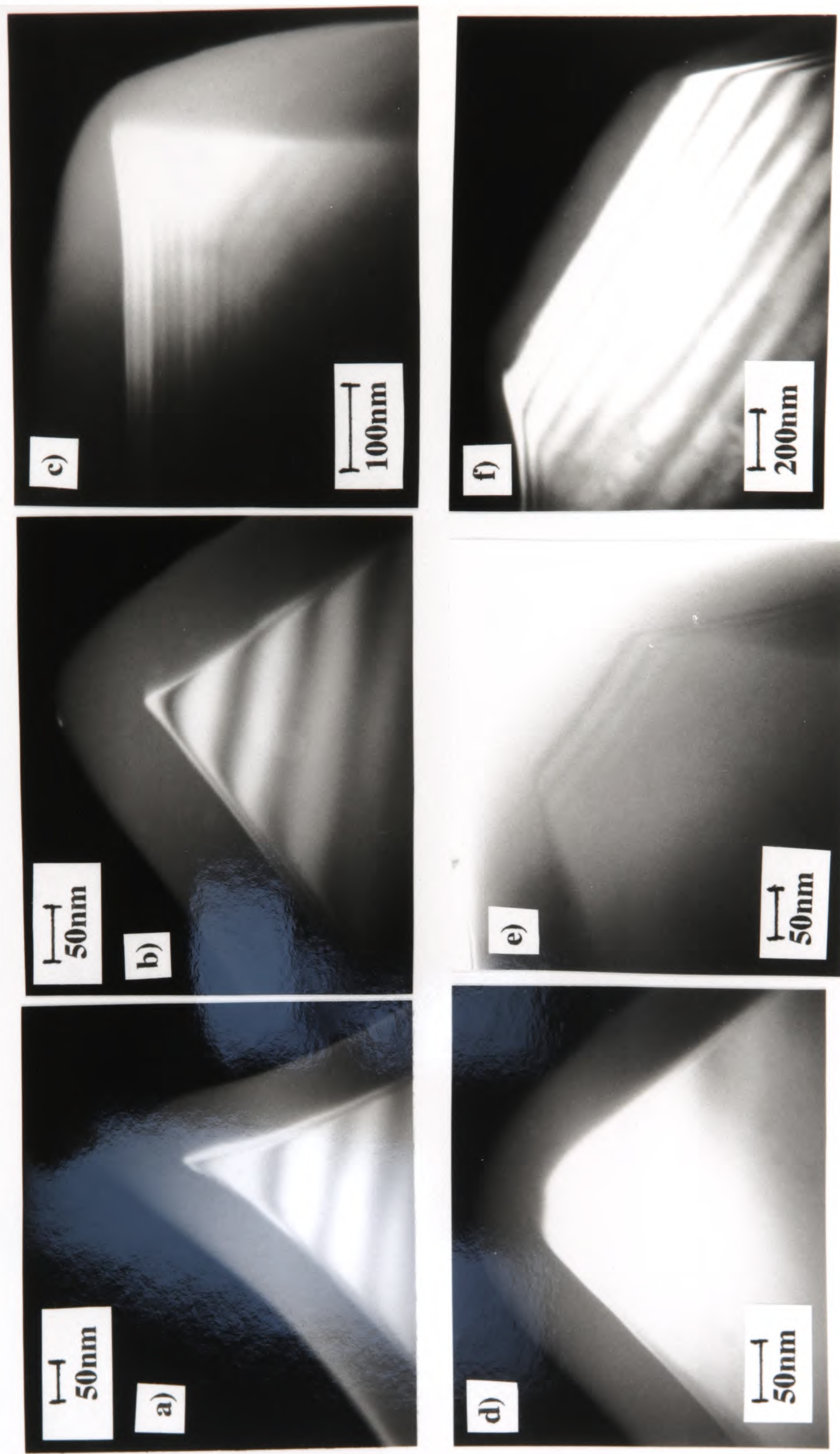






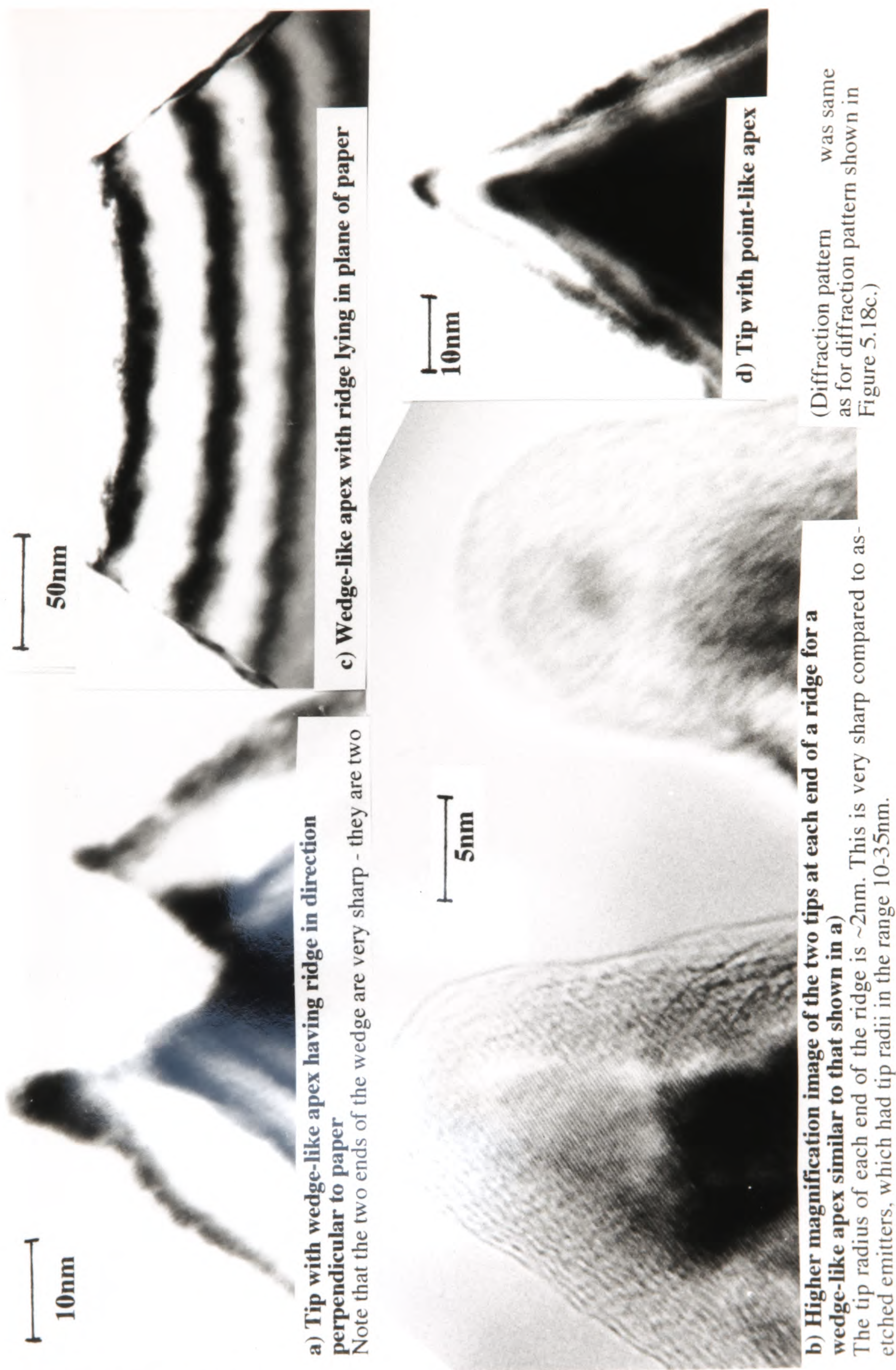


Graph 5.1 - Distributions of Starting Voltage for Field Emitter Arrays Etched for Different Times
Comparison of these distributions shows that the lowest mean starting voltage and the narrowest range of values was obtained from FEAs containing flat-topped emitters only. As the FEAs became slightly over-etched, the mean starting voltage and the range of values increased, leading to a decrease in uniformity. TEM studies showed that such FEAs contained a mixture of both flat-topped emitters and point-like/wedge-like emitters. The widest range of starting voltage was obtained from very over-etched emitters (TEM showed that these FEAs contained point-like/wedge-like emitters only - no flat-topped emitters were present).



(Diffraction pattern was same as for diffraction pattern shown in Figure 5.18c.)

Figure 5.21 - TEM images of neighbouring emitters which were oxidised for 65 minutes at 1000°C - Oxide masks were removed prior to oxidation
The oxide layer was left in place for TEM examination - it was ~70-90nm thick. It can be seen that the tip-to-tip uniformity is still poor. Although different point-like apexes appear to have become more similar to each other following oxidation, emitters with wedge-like apexes did not become point-like apexes following the oxidation treatment.



a) Tip with wedge-like apex having ridge in direction perpendicular to paper
Note that the two ends of the wedge are very sharp - they are two

b) Higher magnification image of the two tips at each end of a ridge for a wedge-like apex similar to that shown in a)
The tip radius of each end of the ridge is ~2nm. This is very sharp compared to as-etched emitters, which had tip radii in the range 10-35nm.

c) Wedge-like apex with ridge lying in plane of paper

d) Tip with point-like apex
(Diffraction pattern was same as for diffraction pattern shown in Figure 5.18c.)

Figure 5.22 - TEM micrographs of emitters which have been given 3 separate oxidation treatments (each oxidation at 950°C for 4 hours)
This figure demonstrates that even after 3 oxidations, there is still variation in the apex geometry from tip-to-tip - both wedge-like and point-like apexes were still observed.

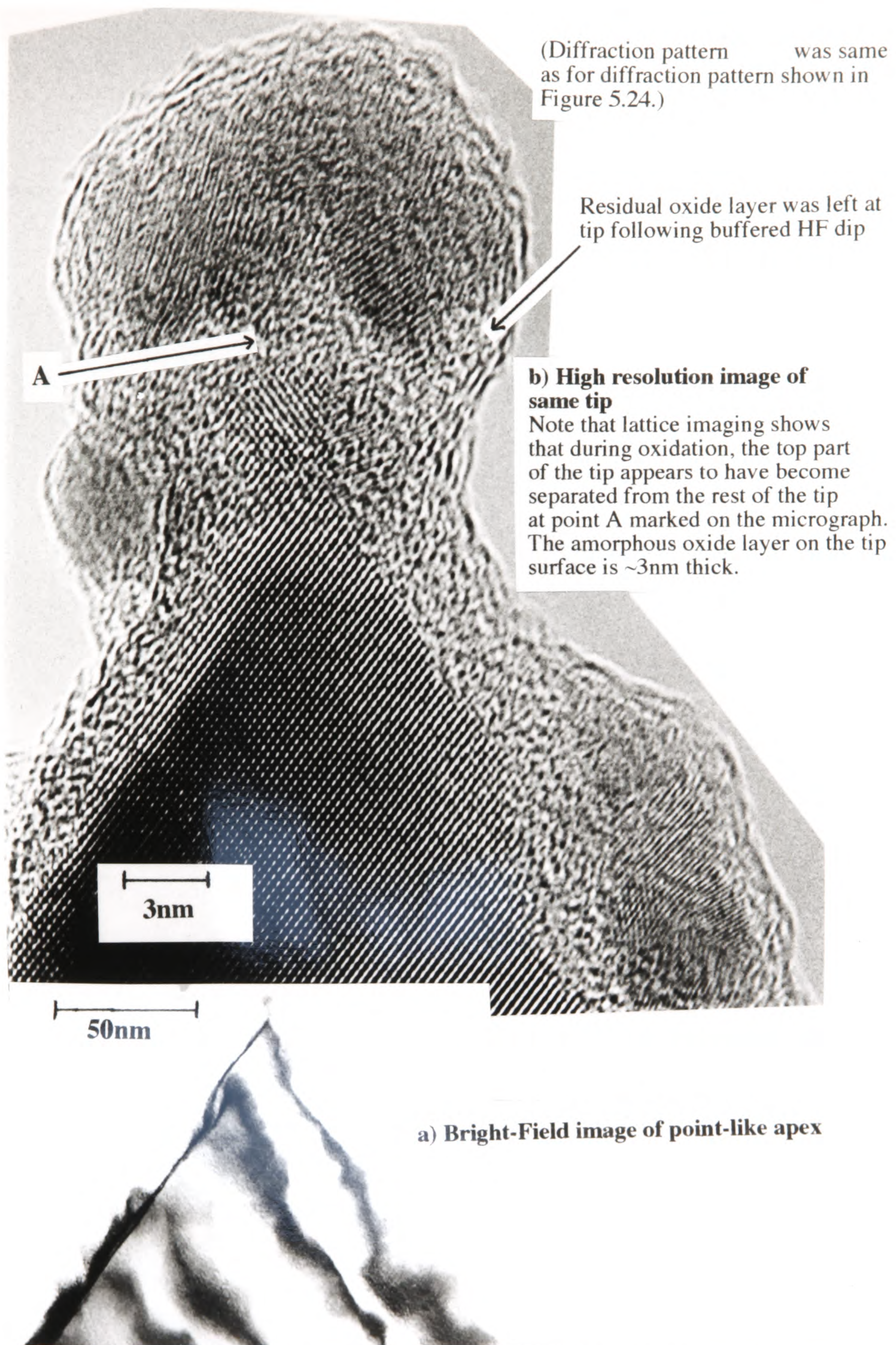
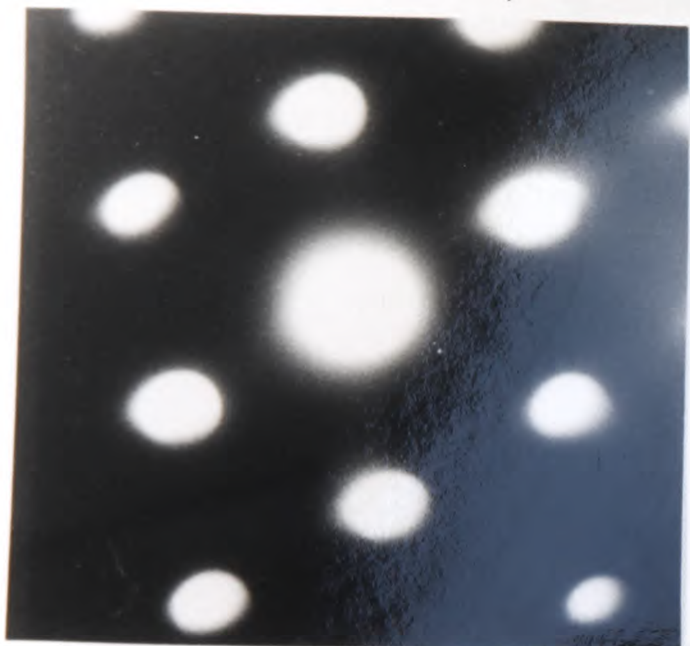


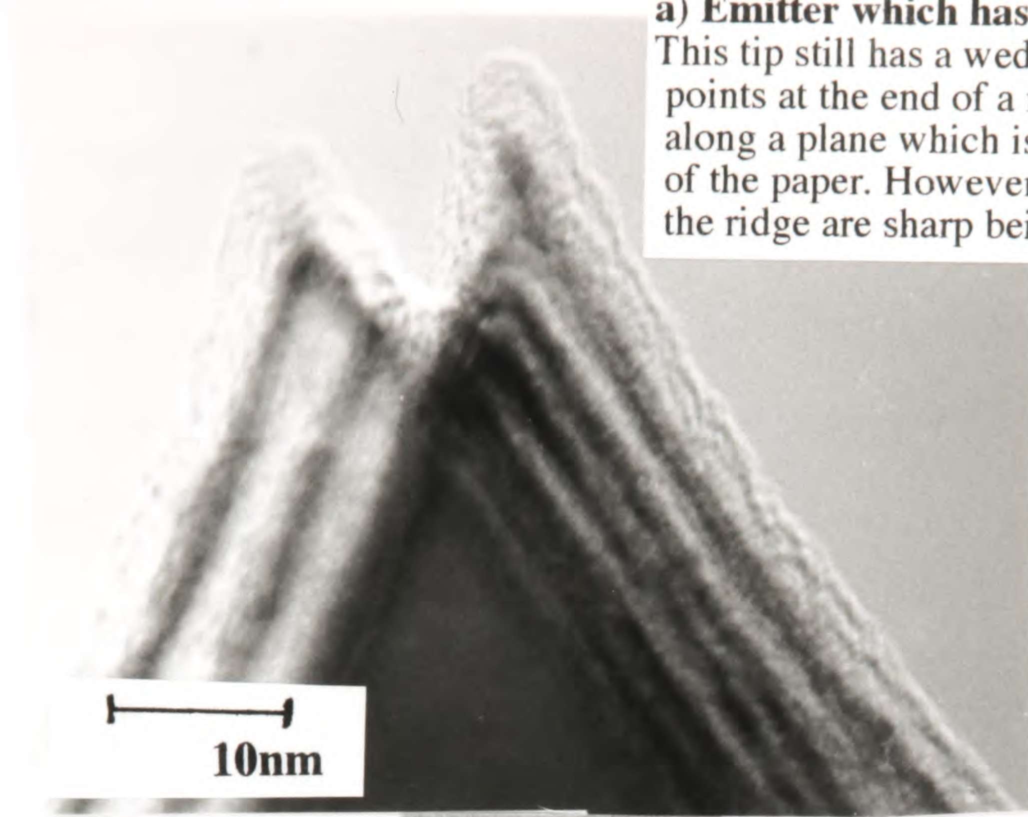
Figure 5.23 - 4 Oxidation Treatments: TEM micrographs of emitters with point-like apexes, which have been given 4 separate oxidation treatments (each oxidation at 950°C for 4 hours)
Note that some tips did have point-like apexes. The tip shown here is very sharp, being ~2nm in radius.



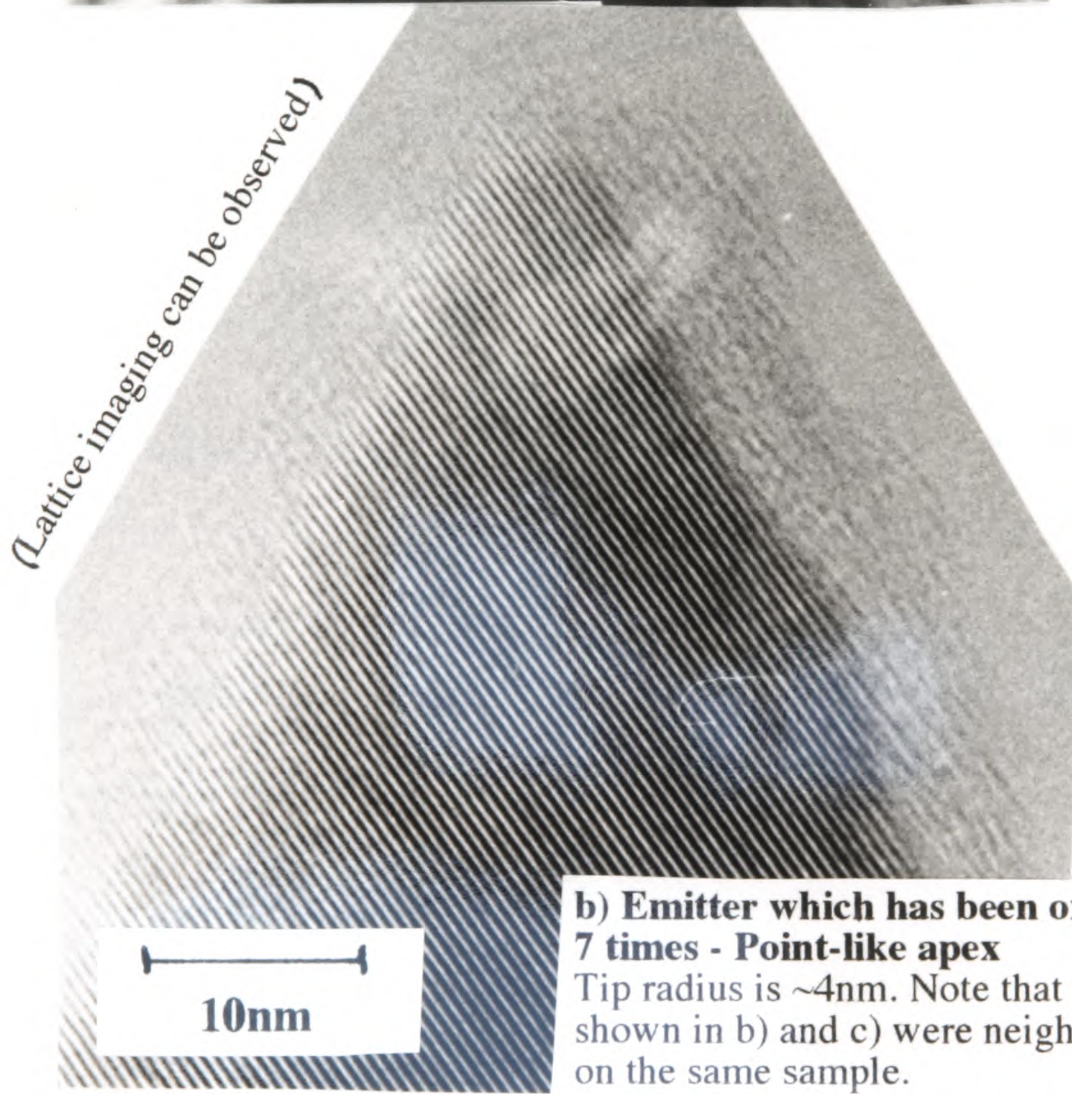
a) **Bright-Field image of wedge-like apex**

b) **High resolution image of same tip**

Figure 5.24 - 4 Oxidation Treatments: TEM micrographs of emitter with wedge-like apex , which have been given 4 separate oxidation treatments (each oxidation at 950°C for 4 hours)
Note the two tips at the end of the wedge-shaped apex still exists after 4 oxidation treatments - they have not formed a point-like apex. Note also that tips at each end of the wedge are very sharp.



a) Emitter which has been oxidised 5 times
This tip still has a wedge-like apex with 2 sharp points at the end of a ridge, with the ridge lying along a plane which is perpendicular to the plane of the paper. However, the tips at the each end of the ridge are sharp being ~1nm in radius.



b) Emitter which has been oxidised 7 times - Point-like apex
Tip radius is ~4nm. Note that the tips shown in b) and c) were neighbours on the same sample.

(Diffraction pattern was same as for diffraction pattern shown in Figure 5.18c.)

c) Emitter which has been oxidised 7 times - Wedge-like apex
Tip radius is ~5nm

Figure 5.25 - 5 and 7 Oxidation Treatments: TEM micrographs of emitters which have undergone 5 and 7 oxidation treatments (each oxidation at 950°C for 4 hours)
This figure shows that even after 5 and 7 oxidation treatments, there is still variation in the tip-to-tip morphology - there is still a mixture of point-like and wedge-like apexes. All emitters shown here were examined with the sample aligned along the same crystallographic direction as that shown in the diffraction pattern in Figure 5.18.

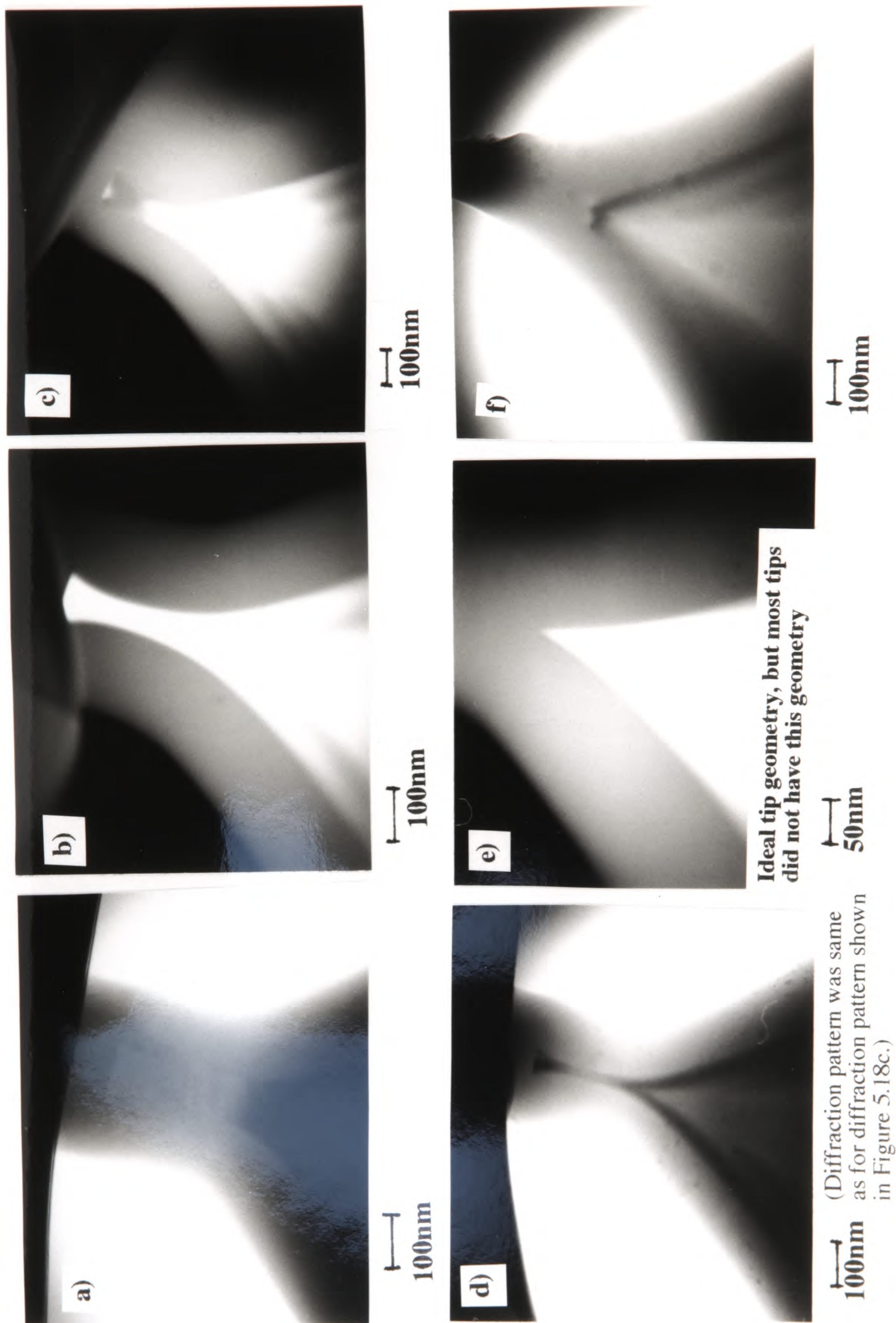
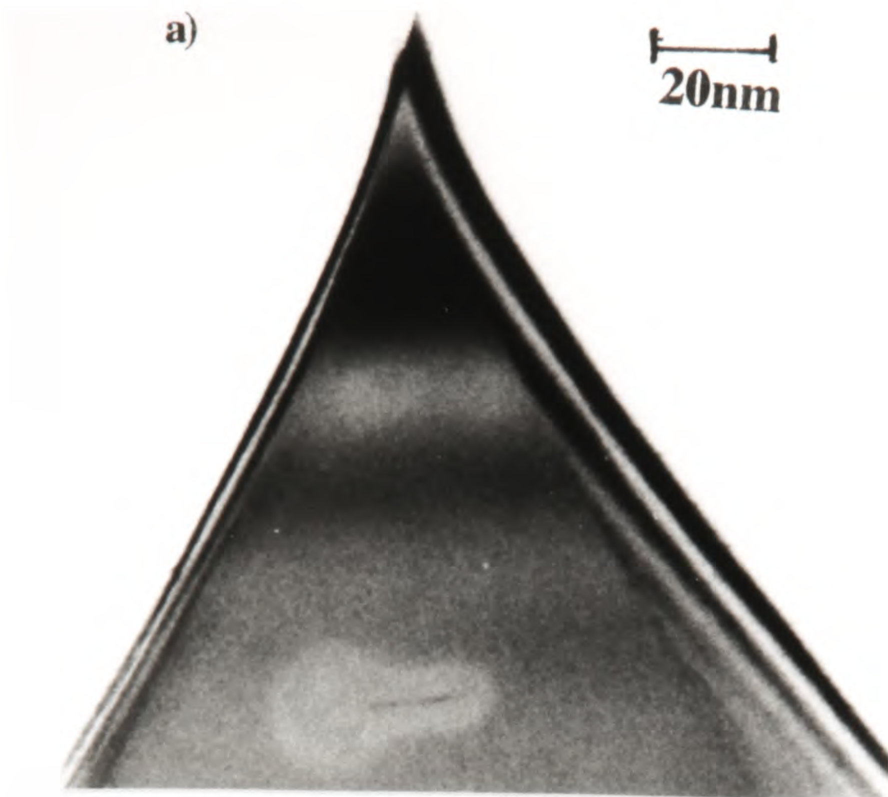
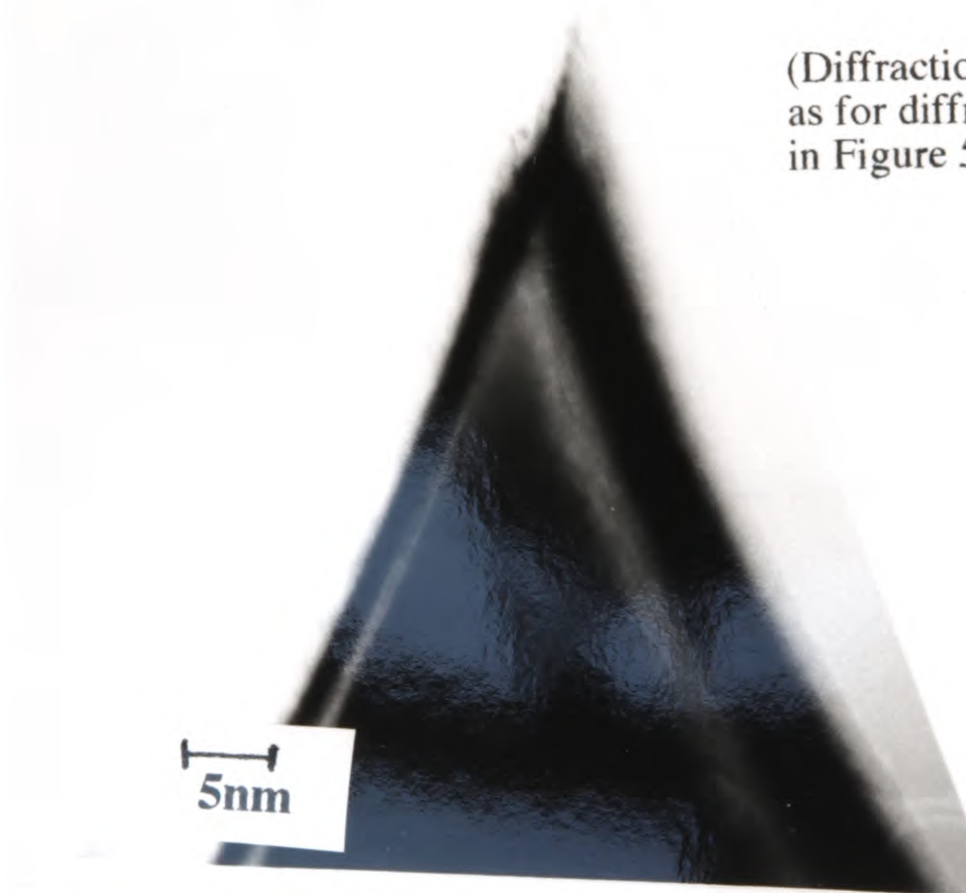


Figure 5.27 - TEM micrographs of neighbouring emitters on same sample which was oxidised at 1000°C for 2 hours with oxide masks still in place
Note that the thermal oxide and the original oxide masks was not removed prior to examination. Oxide layer was ~200nm thick. Morphology of the silicon tip within the oxide layer varies from tip-to-tip, due to differences in the starting geometry of the tips across the sample.

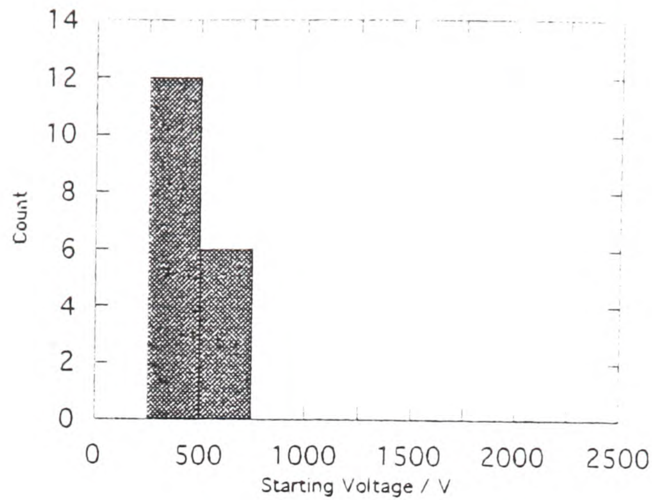


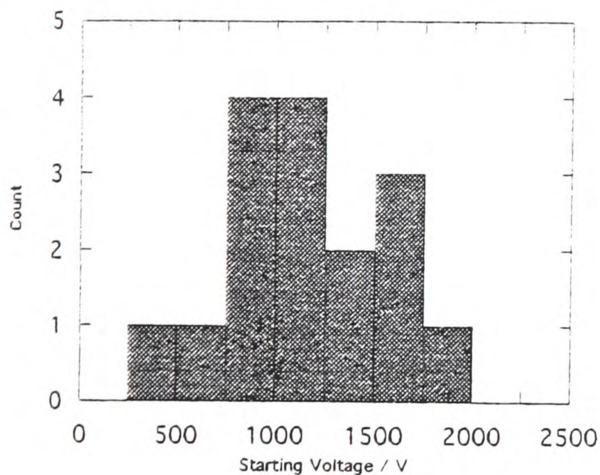
(Diffraction pattern was same as for diffraction pattern shown in Figure 5.18c.)

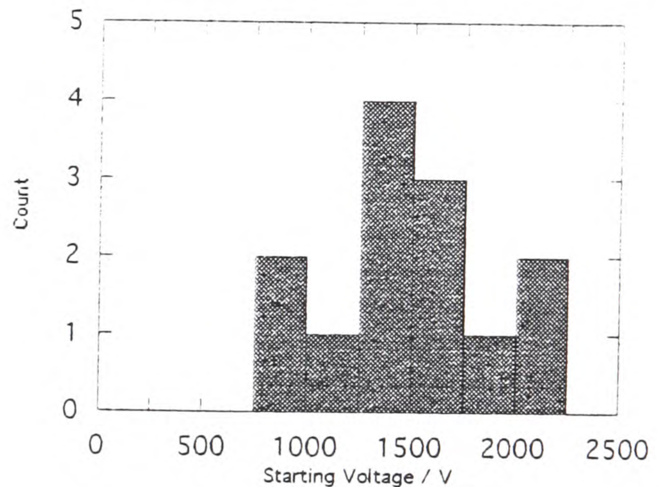


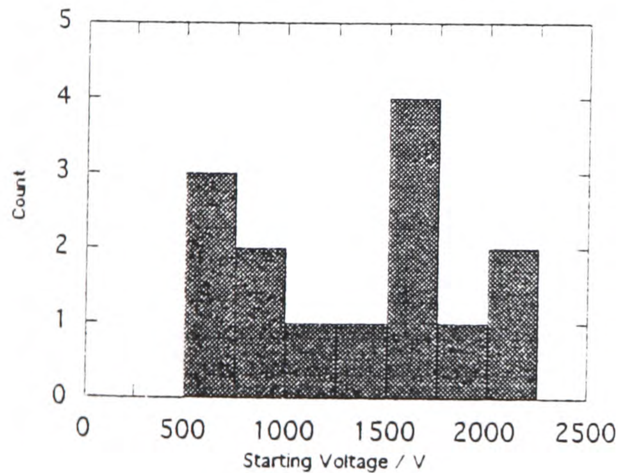
b) Same tip as a) but at higher magnification

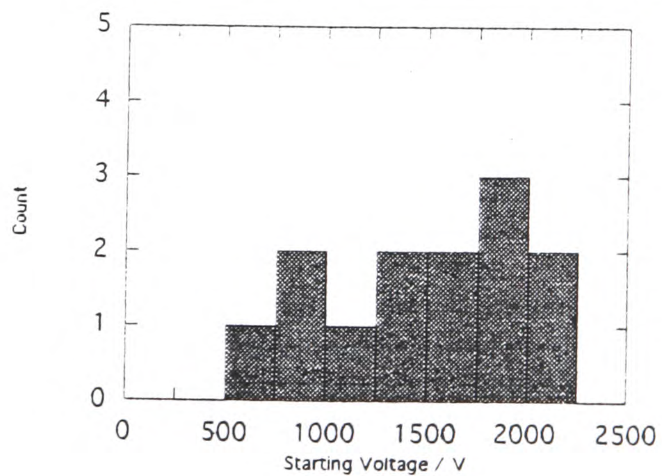
Figure 5.28 - TEM micrograph of tip such as that shown in Figure 5.27e, following removal of the oxide layer
The oxide layer and oxide mask were removed by dipping the sample into buffered HF (sample originally given same treatment as sample shown in Figure 5.27, i.e. oxidation at 1000°C for 2 hours). The tip is very sharp (being ~1nm in radius) and has a high aspect ratio. Ideally, this geometry of tip would have been replicated across the entire array. However, as shown in Figure 5.27, most tips did not have this geometry.





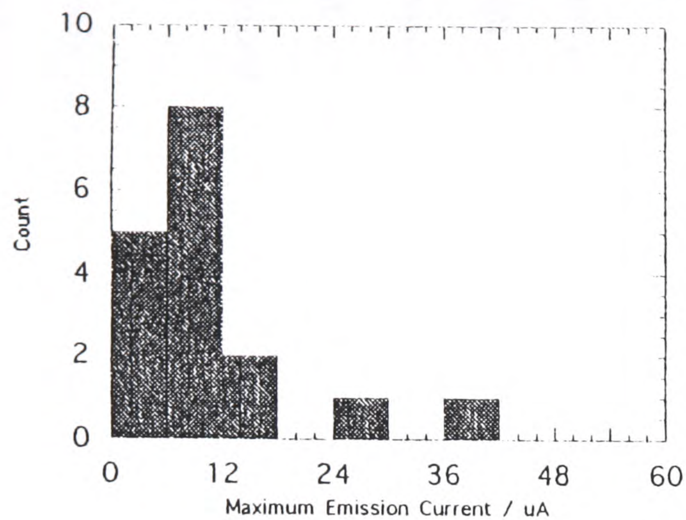


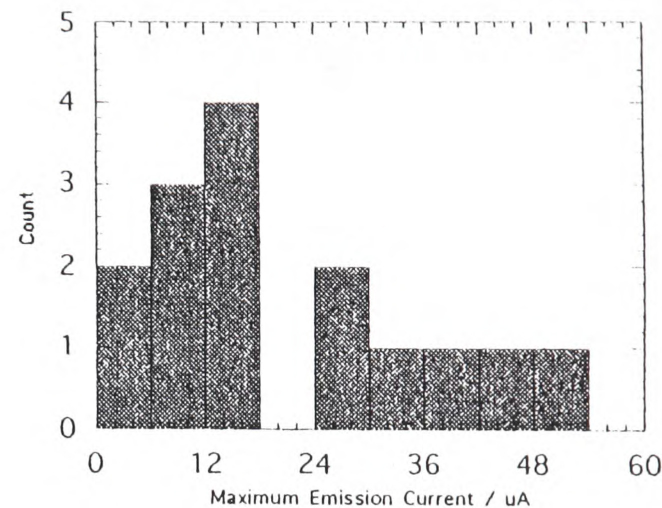


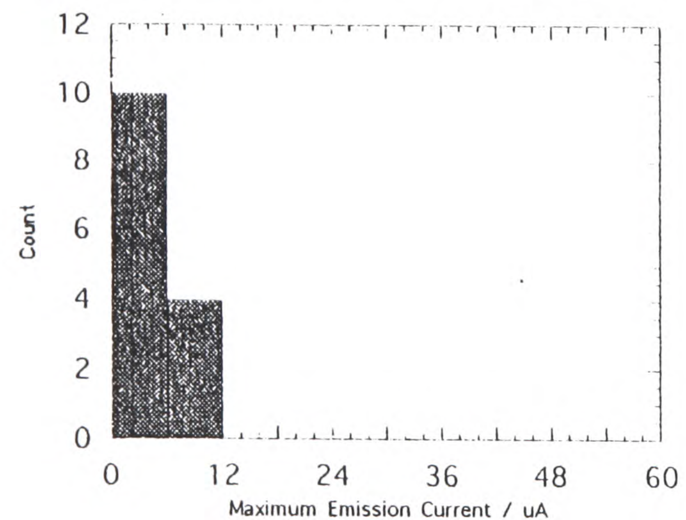


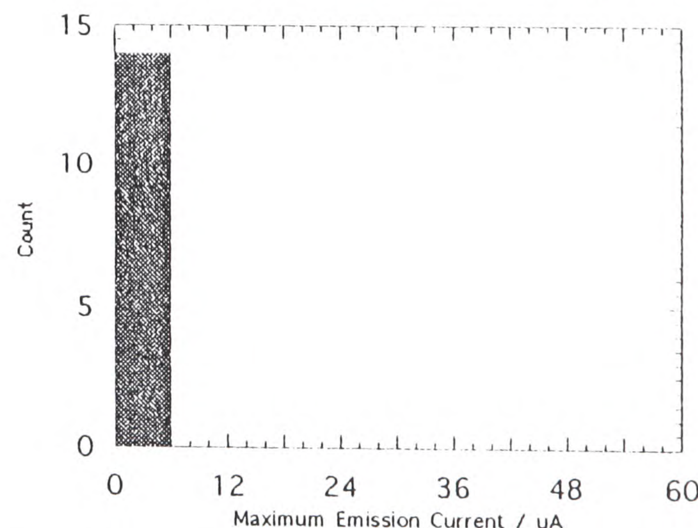
Graph 5.2 - Distributions of Starting Voltage for Oxidation-Sharpened Field Emitter Arrays

The distribution shown in a) was obtained from an FEA oxidised with the oxide masks still in place. This array exhibited the lowest mean starting voltage and the narrowest range of values. The other distributions were obtained from very over-etched FEAs which had then been oxidised up to 7 times. Oxidation in these cases did not reduce the mean starting voltage or decrease the range of values obtained.

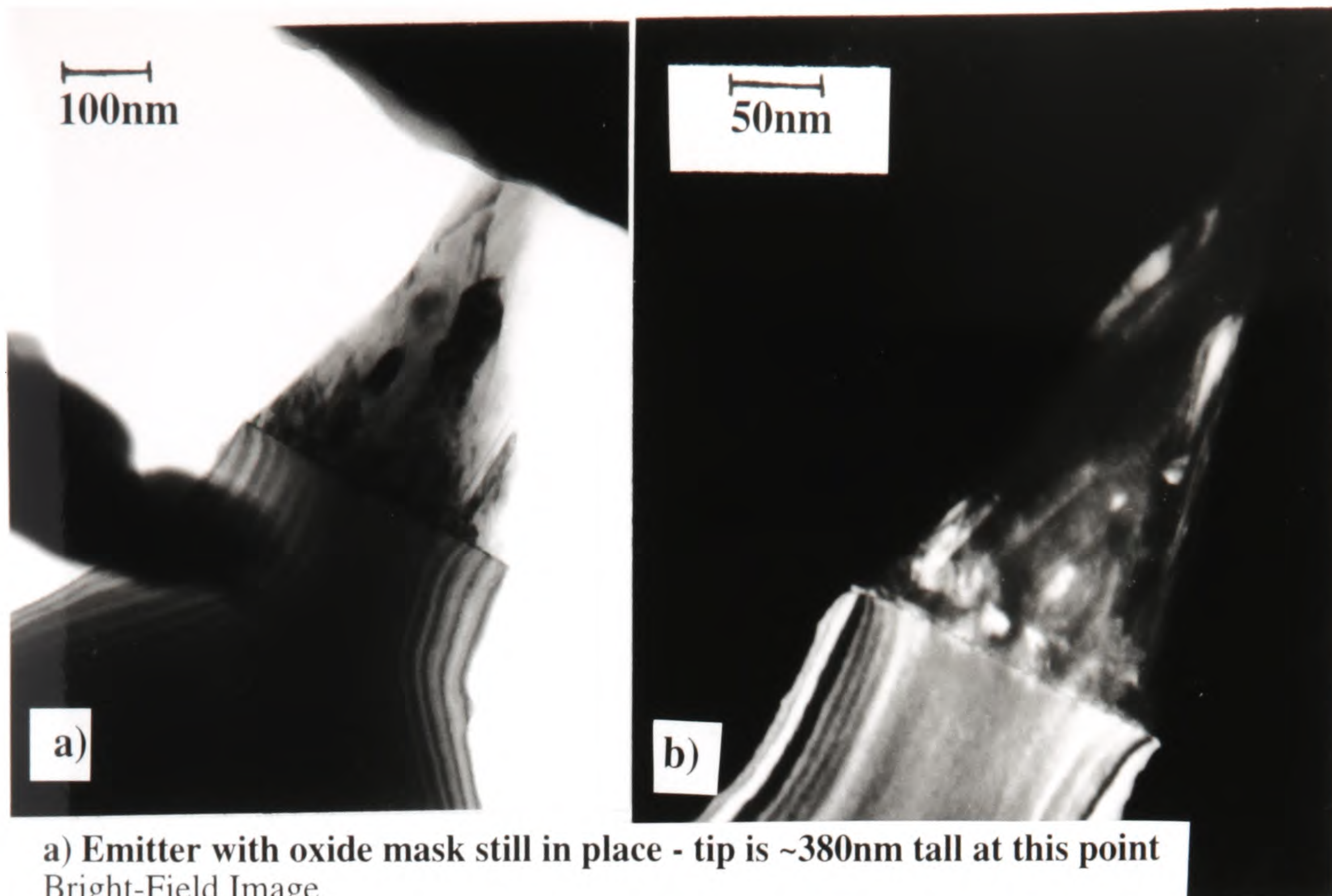






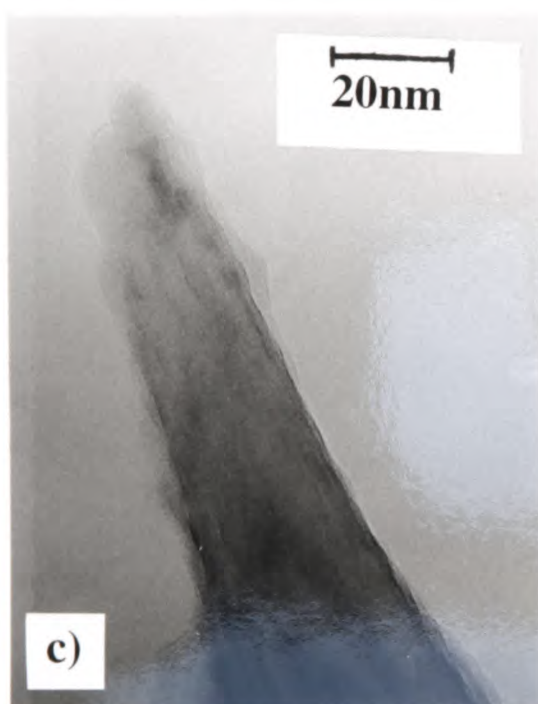


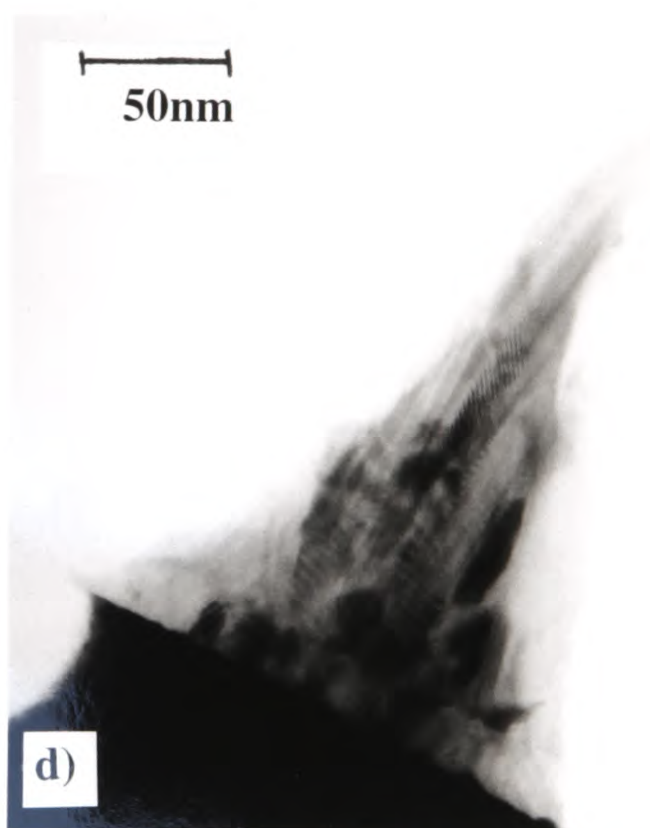
Graph 5.3 - Distributions of Maximum Emission Current for Oxidation-Sharpened Field Emitter Arrays
These distributions show that FEAs oxidised up to 7 times exhibited very low maximum emission currents prior to destruction, compared to the other samples. One possible explanation for this is that TEM for tips oxidised 7 times showed that the tip radii were very sharp. This may have made the tips less thermally stable at high emission currents, than prior to oxidation when the tips were blunter. The maximum current obtained from emitters oxidised with the mask in place were similar (although slightly lower in value) to those obtained from over-etched FEAs which had undergone 1 oxidation treatment.



a) Emitter with oxide mask still in place - tip is ~380nm tall at this point
Bright-Field Image

b) Emitter from which the oxide mask has just fallen off - tip is ~450nm tall at this point
Dark-Field Image

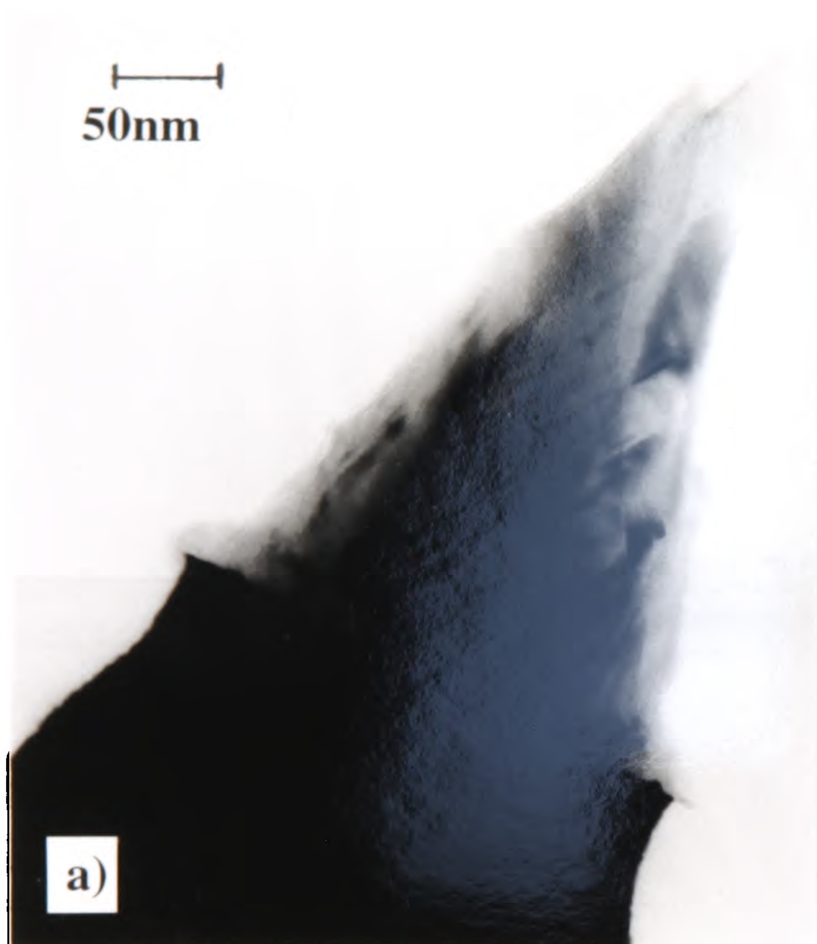


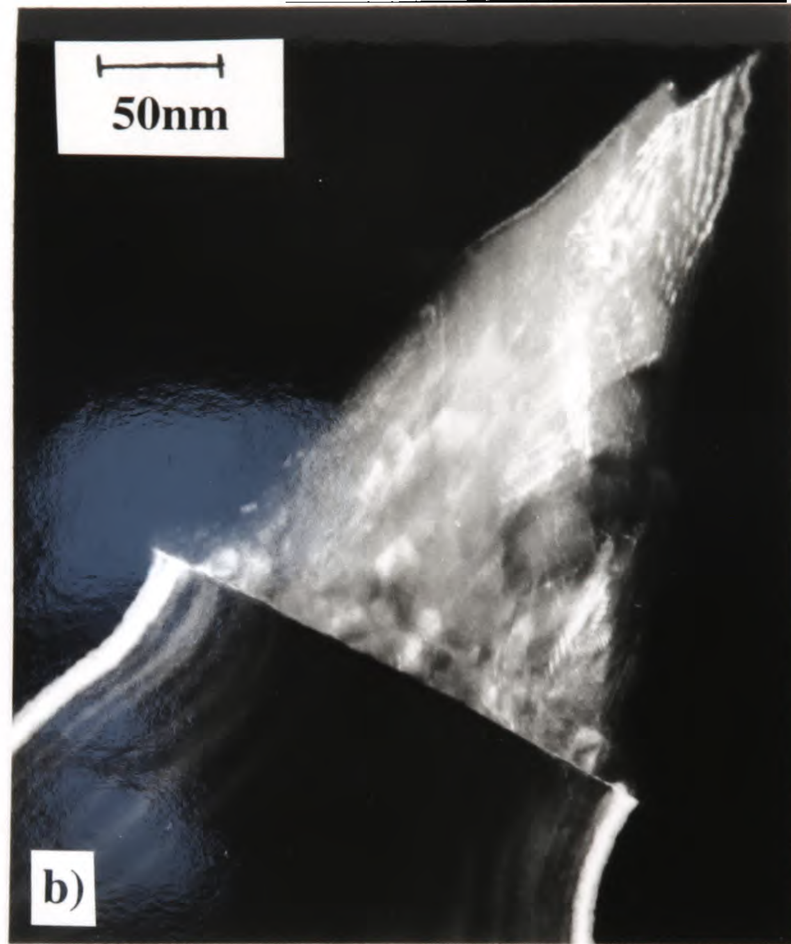


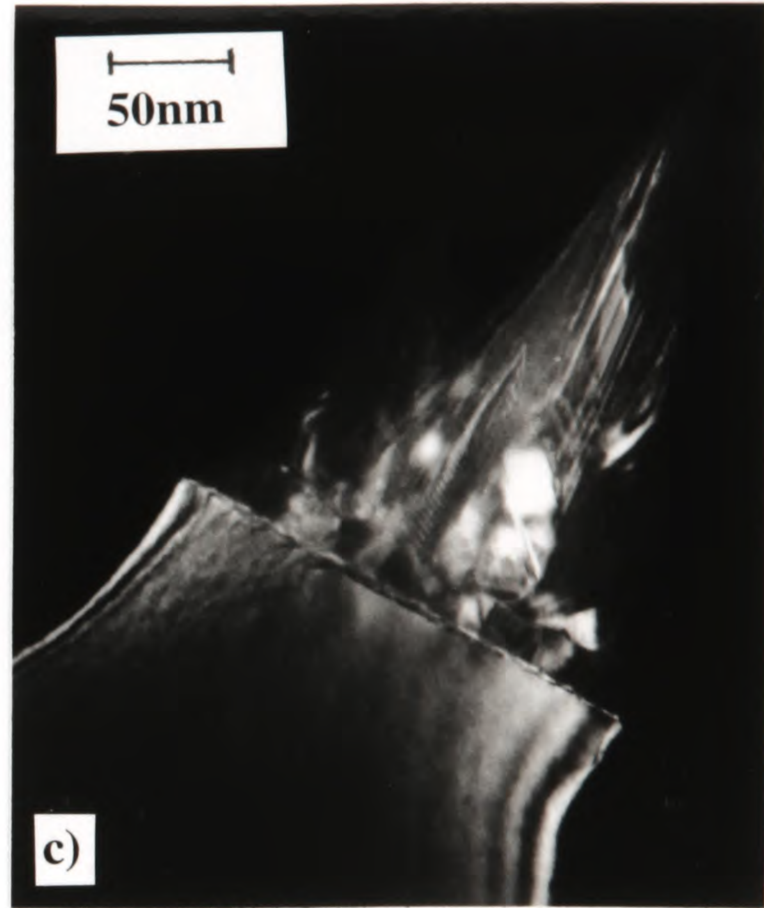
c) High magnification image of tip apex shown in b) - Emitter is ~10nm in radius
Bright-Field Image

d) Emitter which has been etched further than emitter shown in b) - tip is ~270nm tall at this point
Bright-Field Image

Figure 5.30 - TEM micrographs of typical polycrystalline emitters formed by wet-etching
These micrographs show that the polysilicon etched in a different manner to the single crystal silicon. Note that many individual grains can be seen within each polysilicon cone, varying in length from 10 to 100nm. At the base of the cones is a layer of very small grains - these were the original nucleation sites for growth of the polysilicon layer. This base layer is ~30nm thick. Within the polysilicon cones themselves, the individual grains lie in a vertical direction.







a) Bright-Field image of double-tipped emitter

c) Dark-Field image of different double-tipped emitter

b) Dark-Field image of double-tipped emitter shown in a)

Figure 5.31 - TEM micrographs of emitters which have formed double tips, due to the presence of two separate protruding grains at the apex
For uniformity, it would be better to have single tips, rather than double tips.

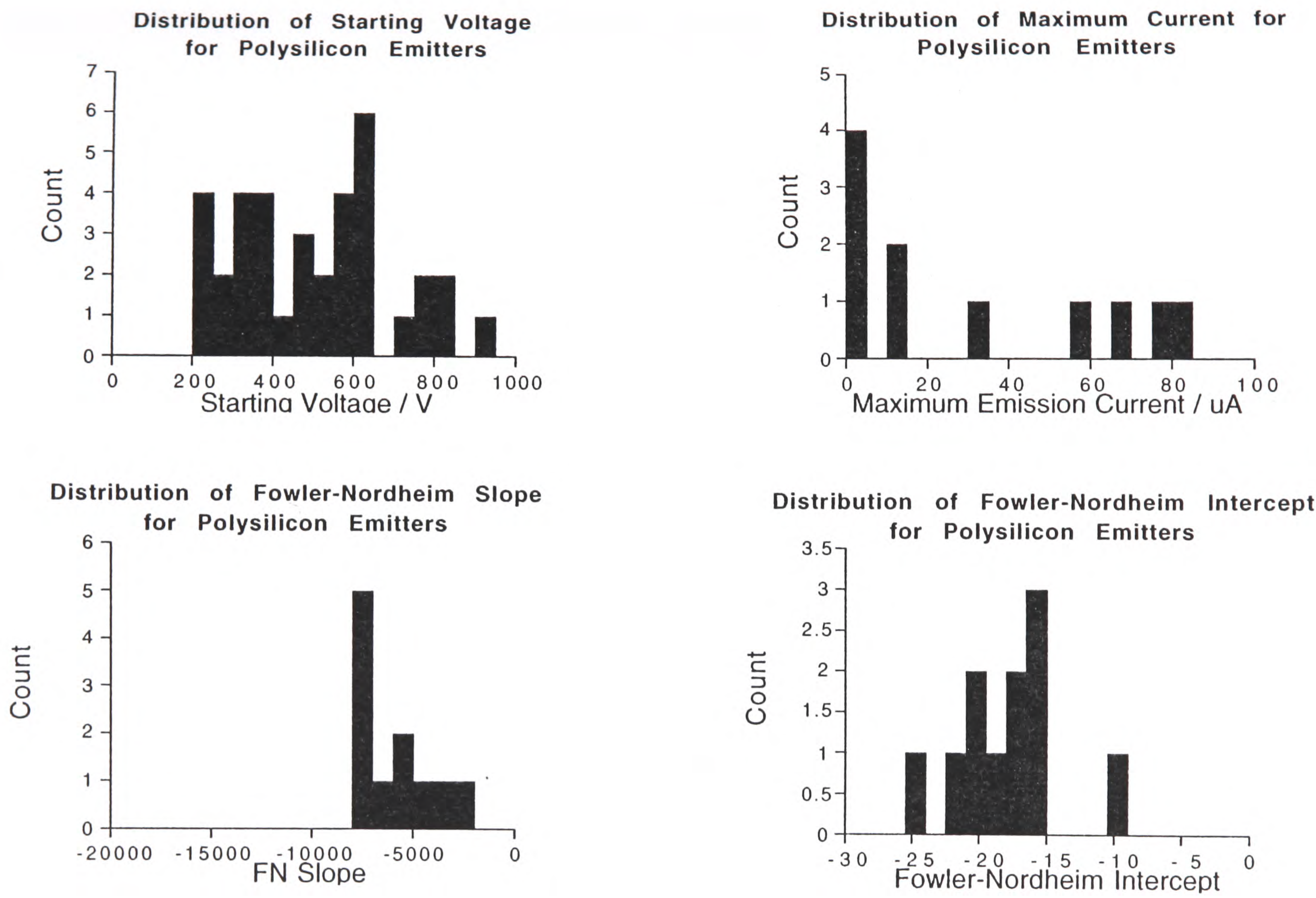
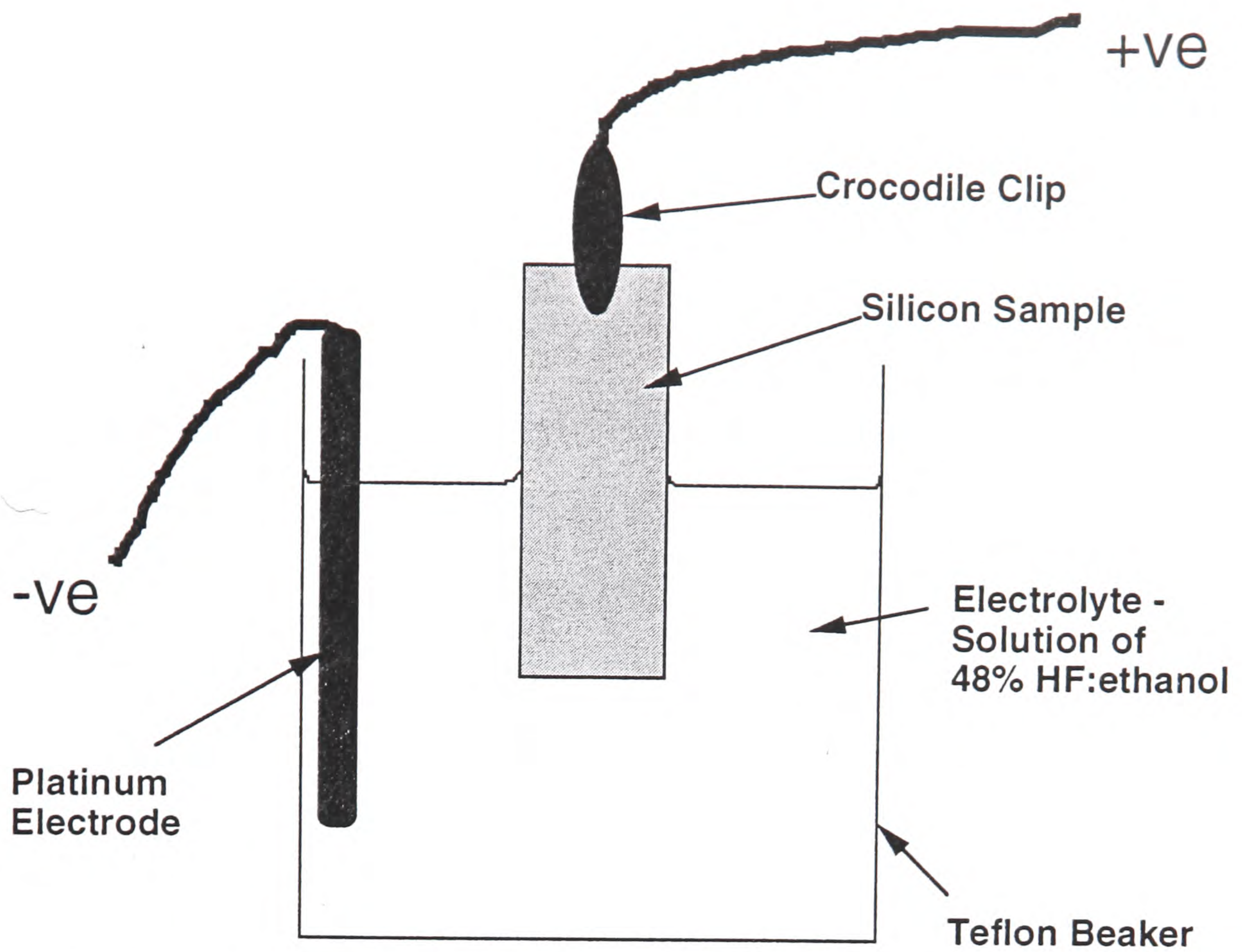
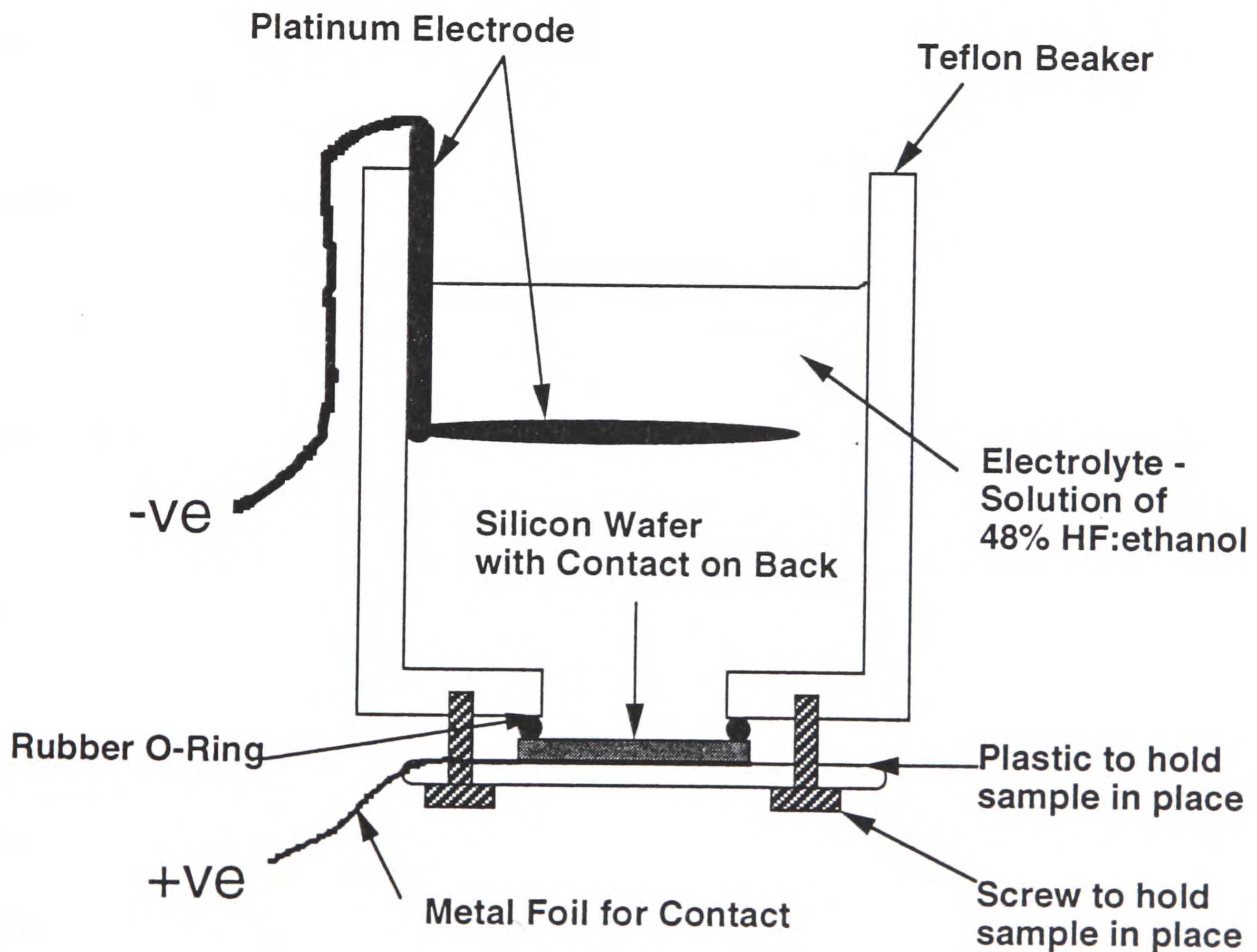


Figure 5.32 - Distributions of Key Parameters for Polysilicon
The mean values for each parameter (compared to single crystal emitters) are summarised in Table 5.4.

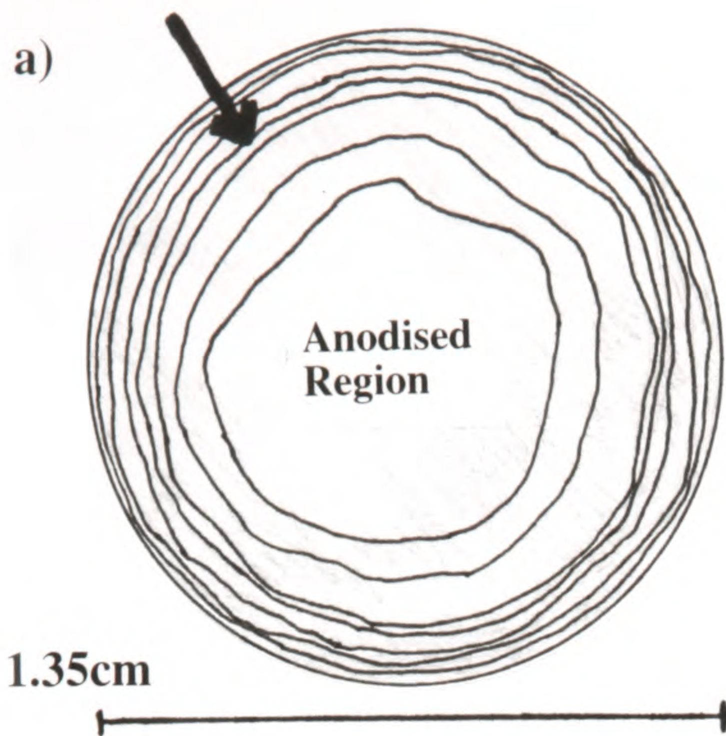


a) Single Cell (Type I) Anodisation Equipment

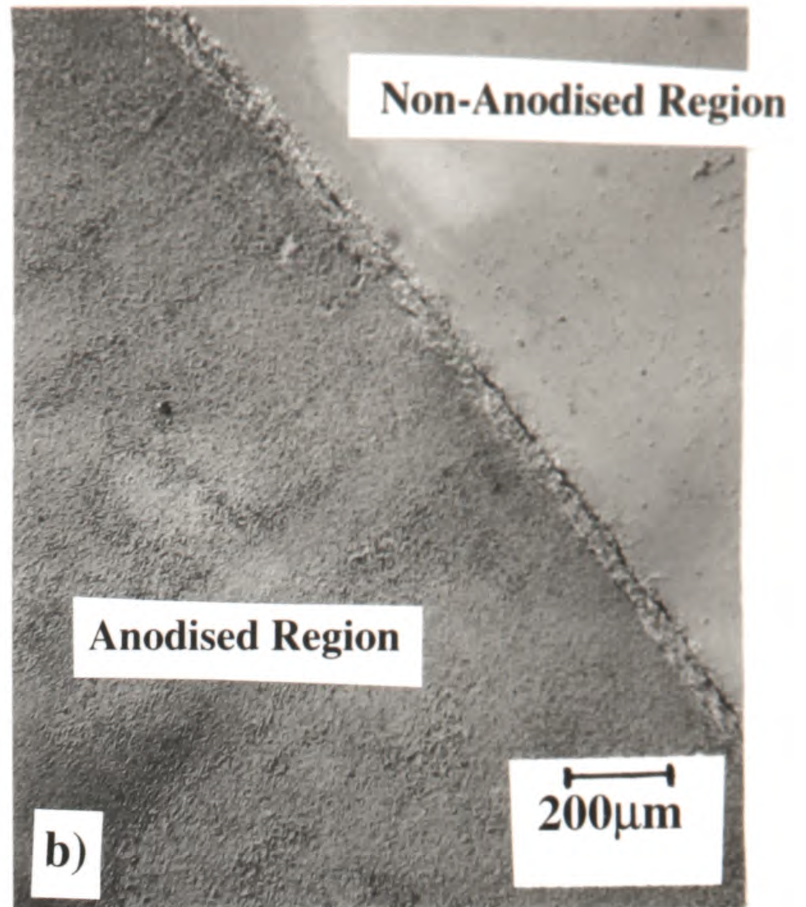


b) Single Cell (Type II) Anodisation Equipment

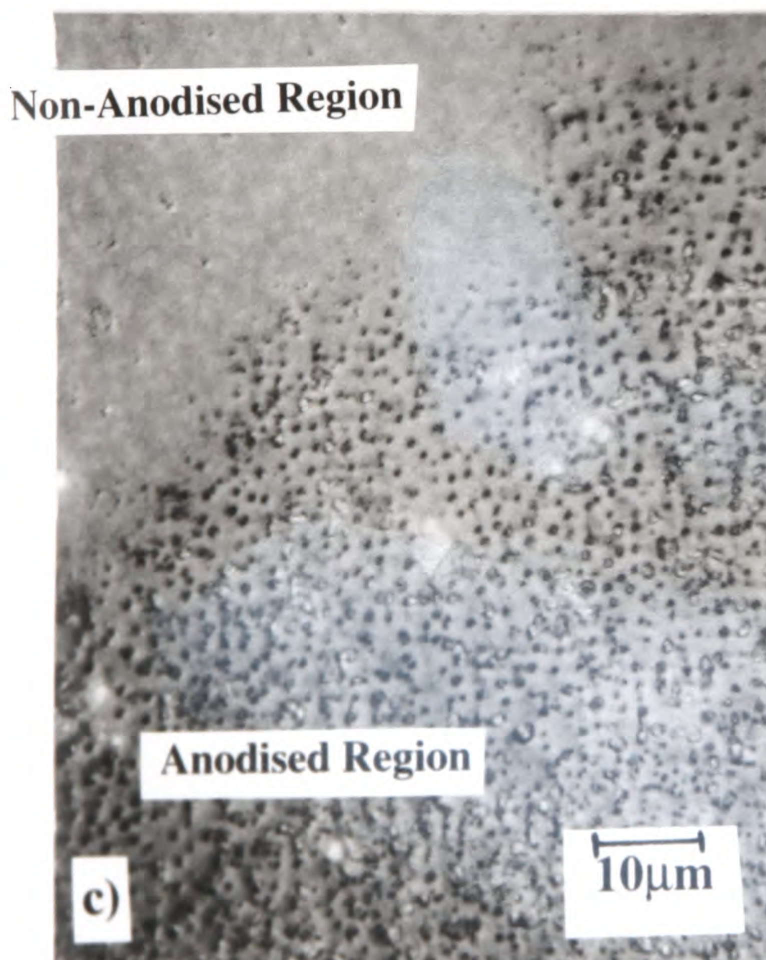
Figure 6.1 - Diagrams Showing Two Types of Electrochemical Cell Used to Anodise Silicon Wafers in This Work
The Type II cell produced much more uniform layers of porous silicon, than for the Type I cell.



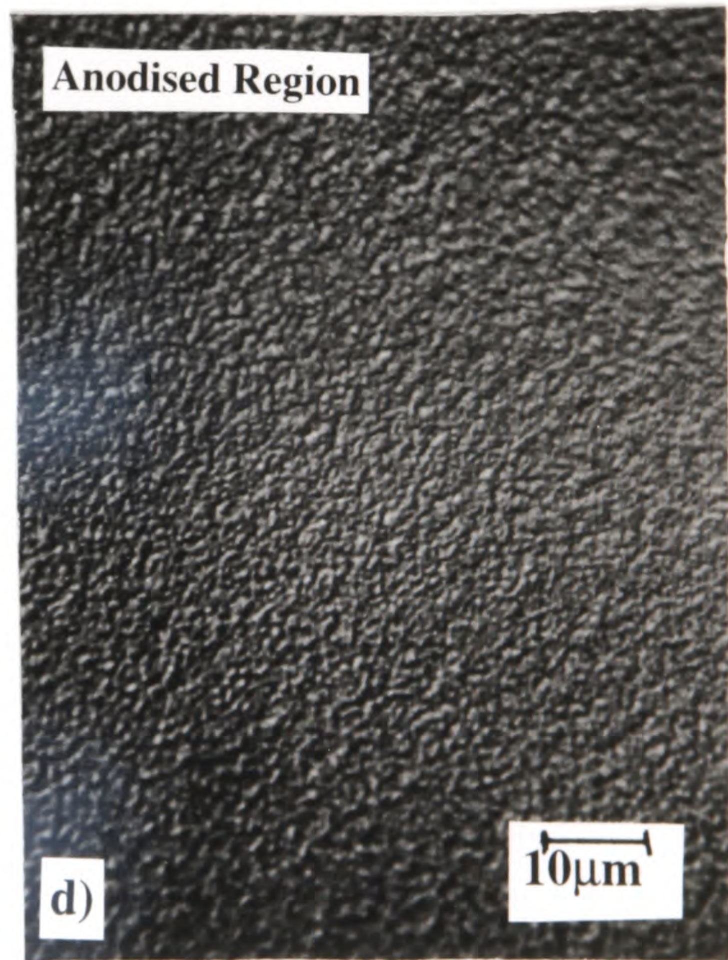
a) Schematic diagram demonstrating porous silicon and thickness fringes following anodisation
Diameter of anodised region is ~1.35cm.



b) Edge of porous silicon region
Note that the porous silicon region appears rough compared to the non-anodised region of the substrate.



c) Higher magnification of edge of porous silicon region



d) Higher magnification image of centre of porous silicon region

Figure 6.2 - Optical micrographs showing appearance of p-type silicon substrate exposed to electrolyte during anodisation - 30 seconds anodisation

(Anodisation current = 30mAcm^{-2})

Substrate Type	Current Density	Anodisation Time
P-Type	$30mAcm^{-2}$	5 minutes
P^+ Type	$100mAcm^{-2}$	5 minutes

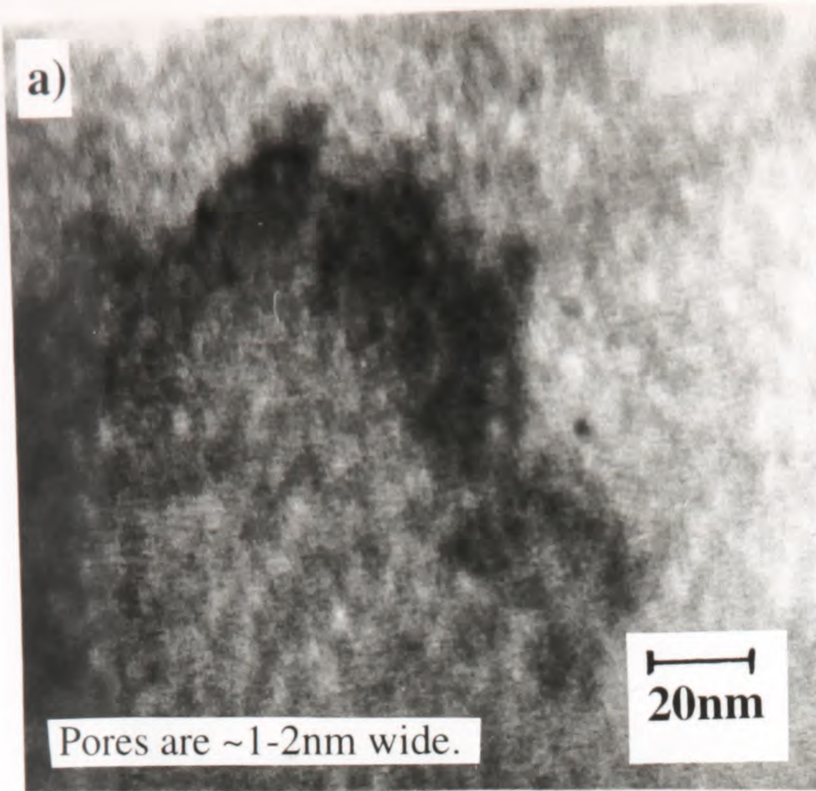
Electrolyte consisting of 48% HF:ethanol ratio 1:1 was used.

Table 6.4 Anodisation Conditions Used to Form Thick Porous Silicon Layers on P and P^+-Type Silicon Substrates

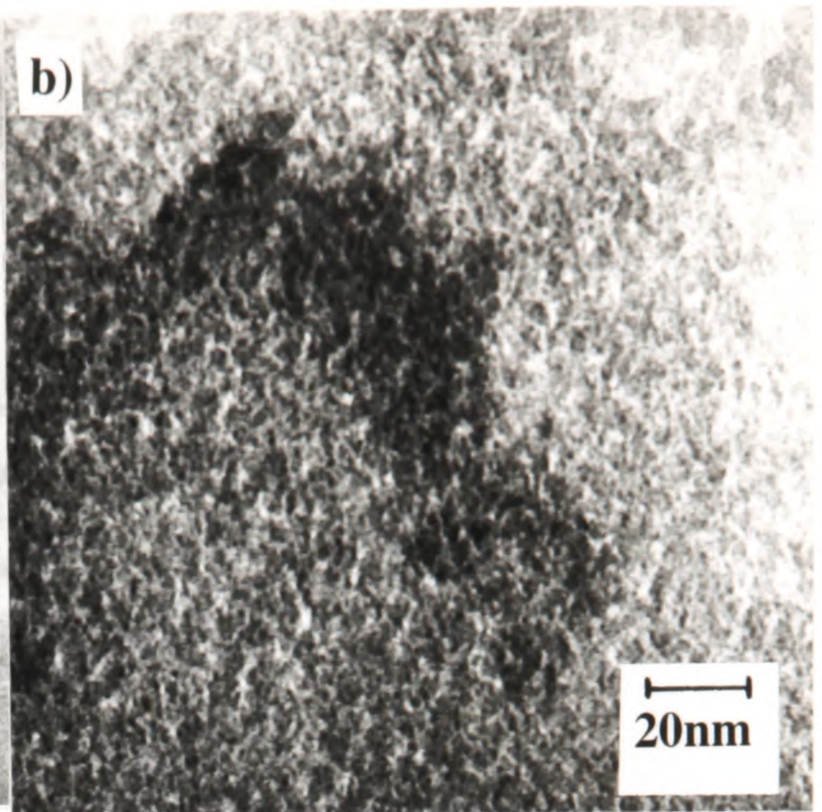
Substrate Type	Current Density	AnodisationTime
P-Type	$10mAcm^{-2}$ $120mAcm^{-2}$	1 second 2 seconds
P+ Type	$10mAcm^{-2}$ $250mAcm^{-2}$	1 second 2 seconds

For each substrate, the current density was cycled between the 2 given anodisation currents for the times shown. In total, 60 cycles were carried out, to form a layered structure.

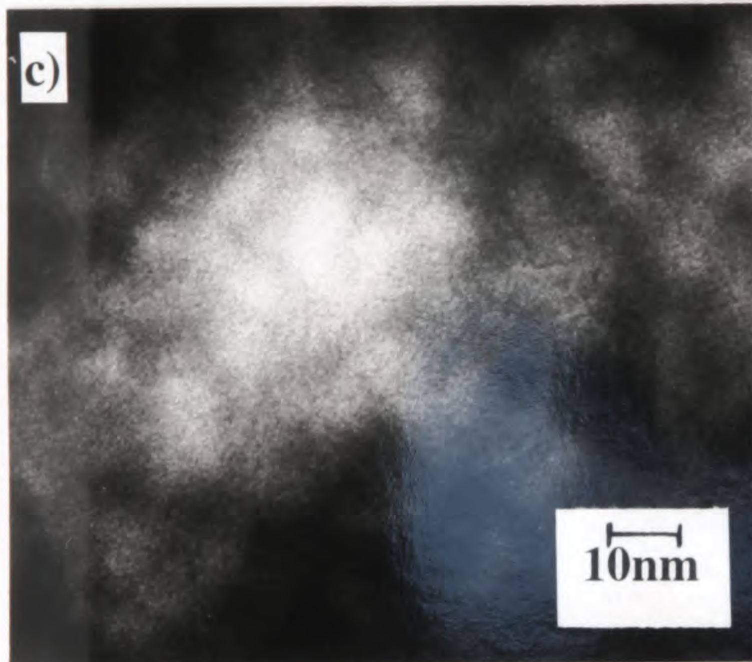
Table 6.5 Anodisation Conditions Used to Form Heterogeneous Layered Porous Silicon Structures on Flat Silicon Substrates



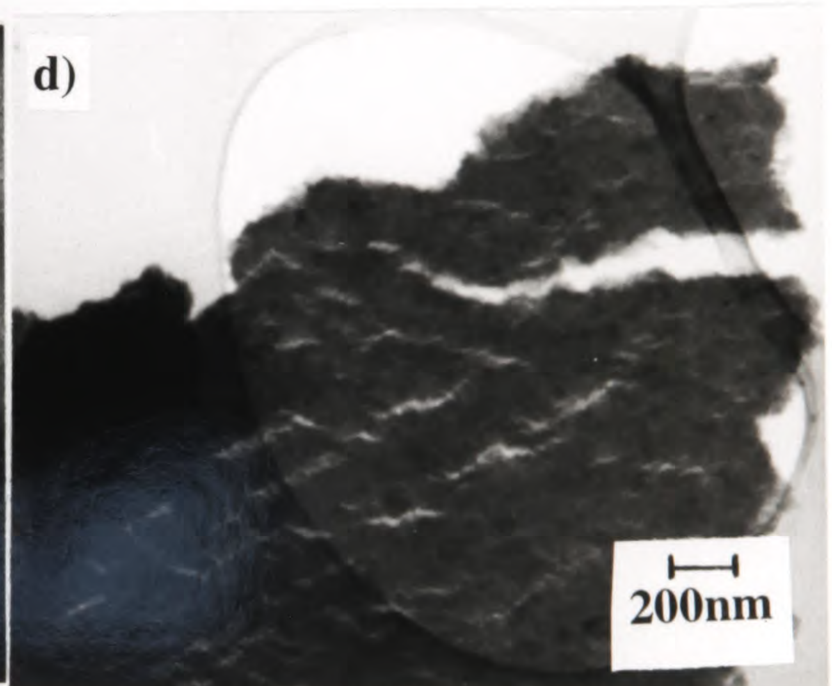
a) Image in-focus
Note fine mottled appearance of p-type porous silicon structure



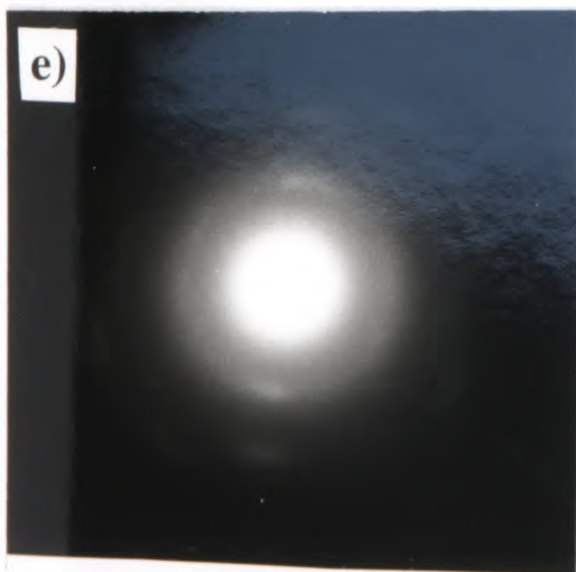
b) Image slightly under-focused
Note that it is easier to resolve the pores if the image is under-focused



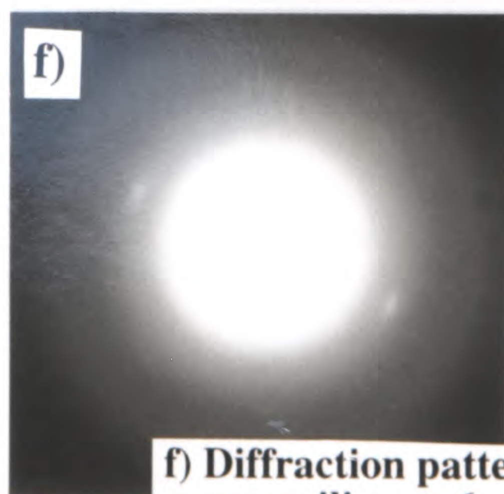
c) Higher magnification image



d) Micrograph showing fragile nature of porous silicon
The porous silicon has torn and split

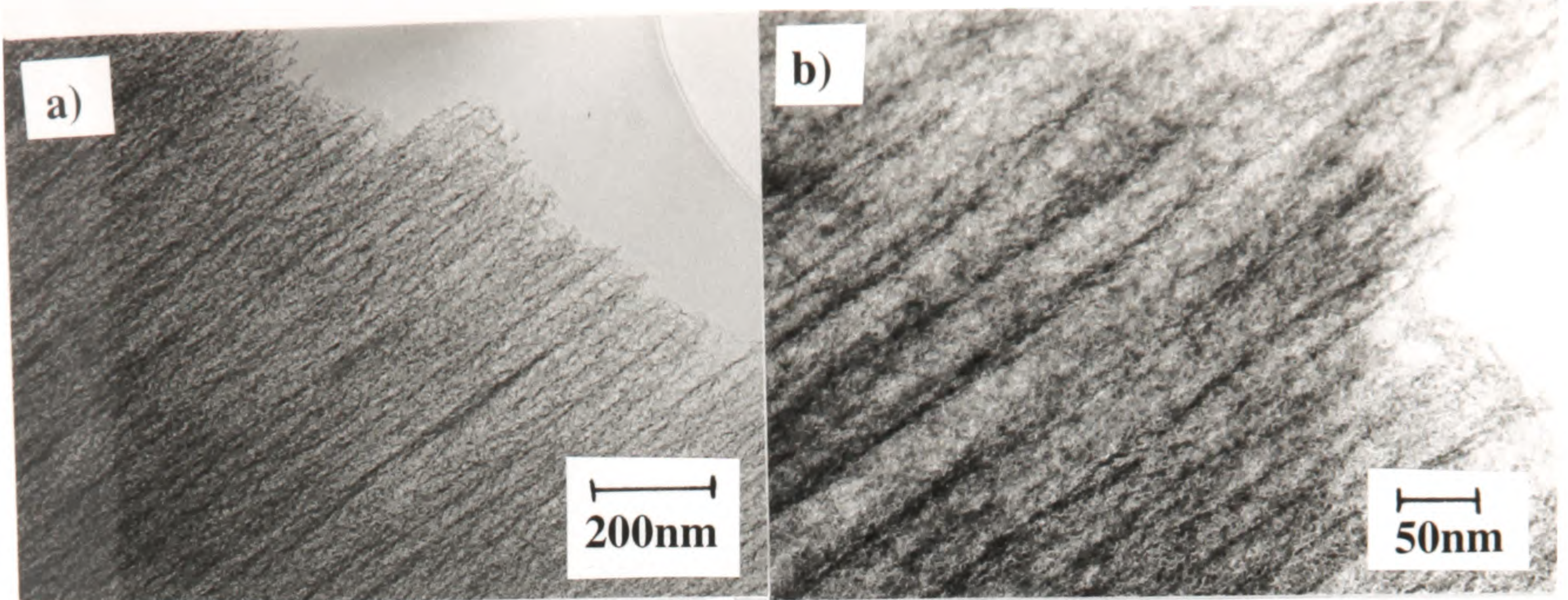


e) Diffraction pattern from p-type porous silicon - 1 day old
Note weak, streaked diffraction spots



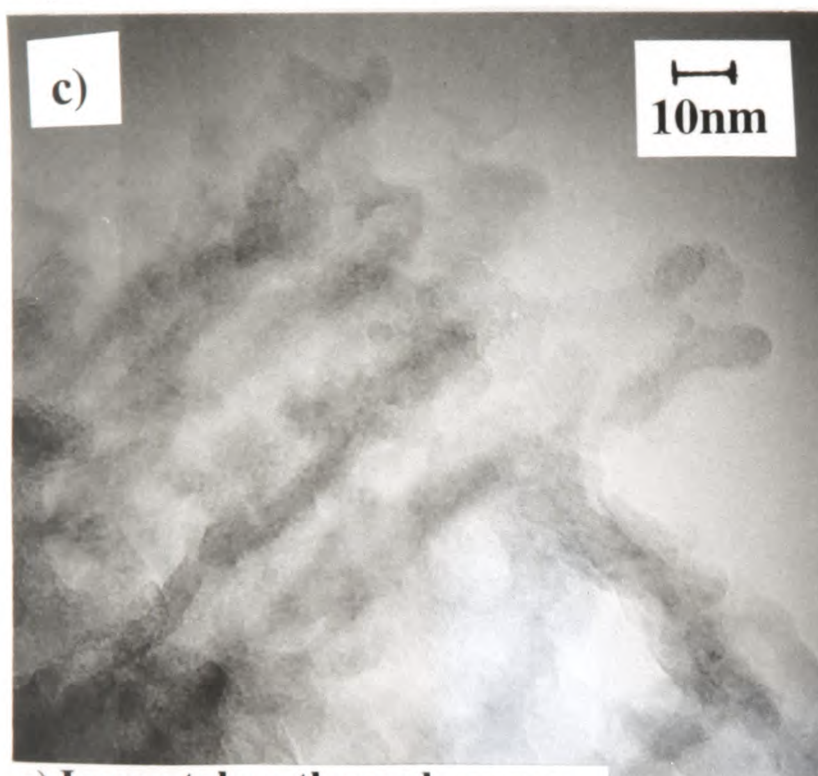
f) Diffraction pattern from p-type porous silicon - 6 months old
Note spots are almost invisible and pattern appears more amorphous

Figure 6.3 - TEM micrographs of cross-sections of p-type porous silicon (Anodisation current density = $30mAcm^{-2}$)

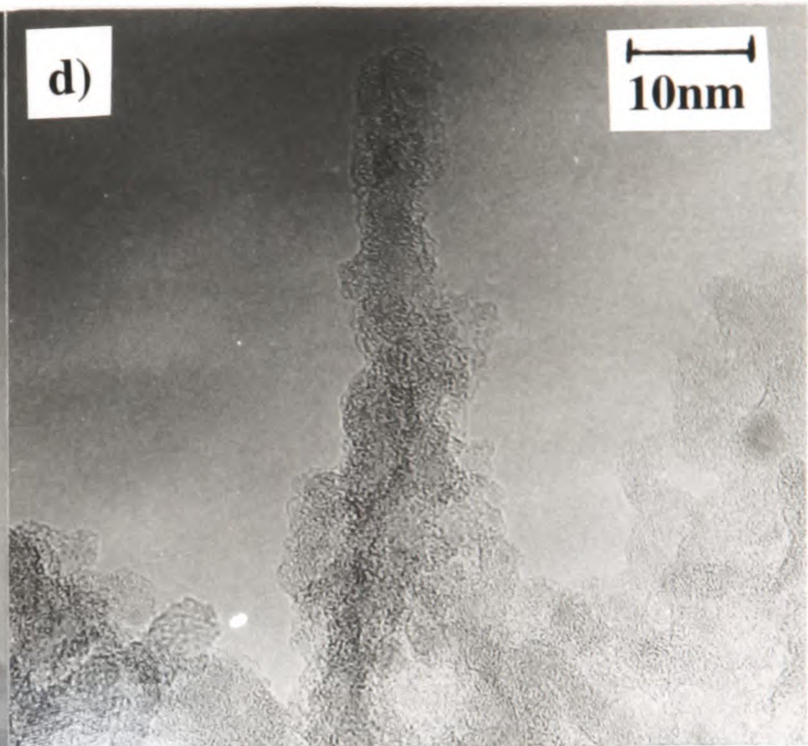


a) Image taken through pores
Note the p^+-type PS structure is much more open and directional than for p-type PS.

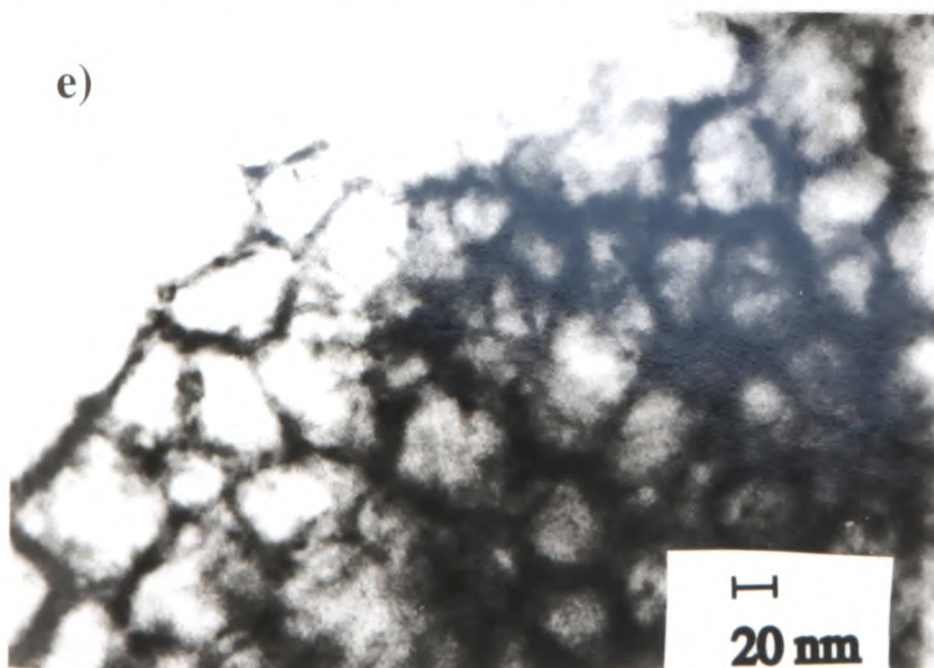
b) Image taken through pores - higher magnification
Pores are ~20nm-50nm wide



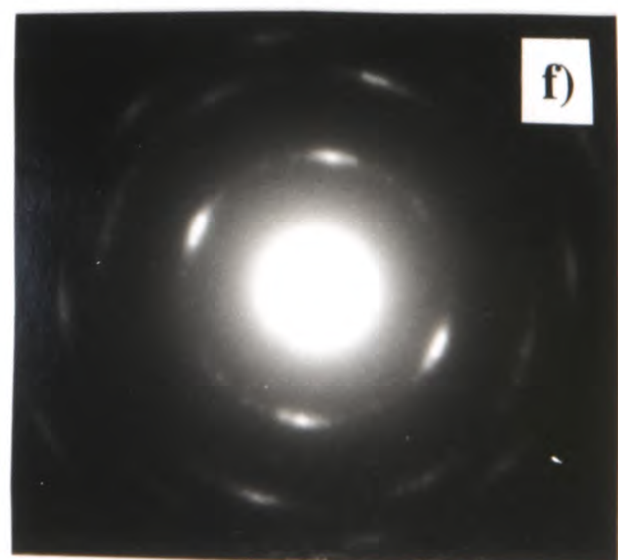
c) Image taken through pores - higher magnification
Individual fibrils are ~5nm thick



d) Single fibril standing proud of material
This particular fibril is ~50nm high

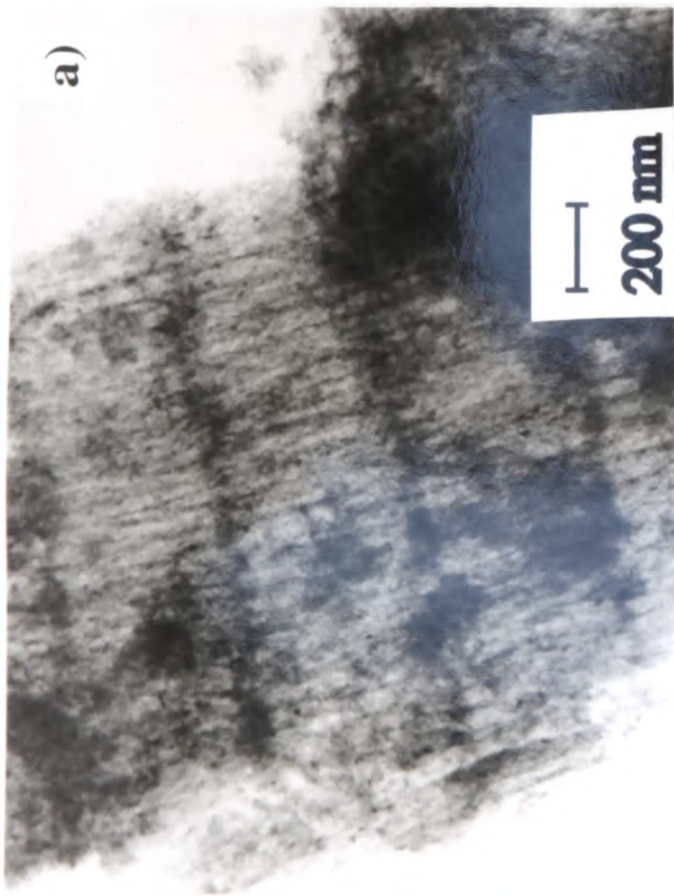


e) Plan-view images down pores
Pores are ~20-50nm wide

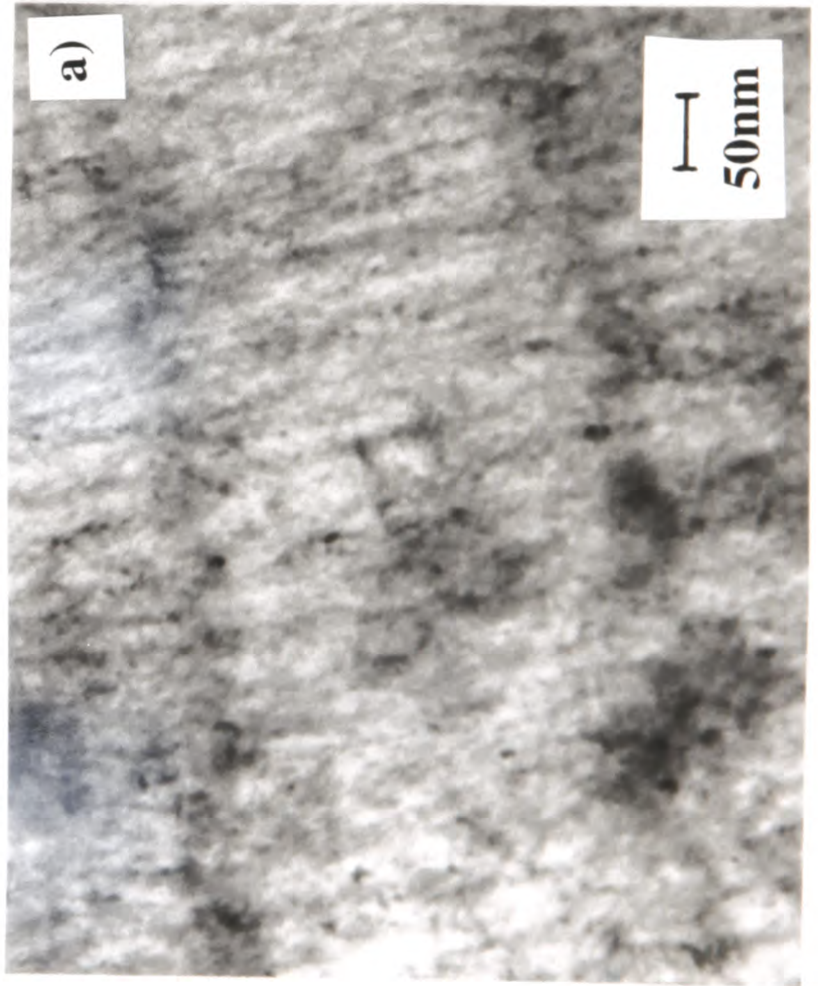


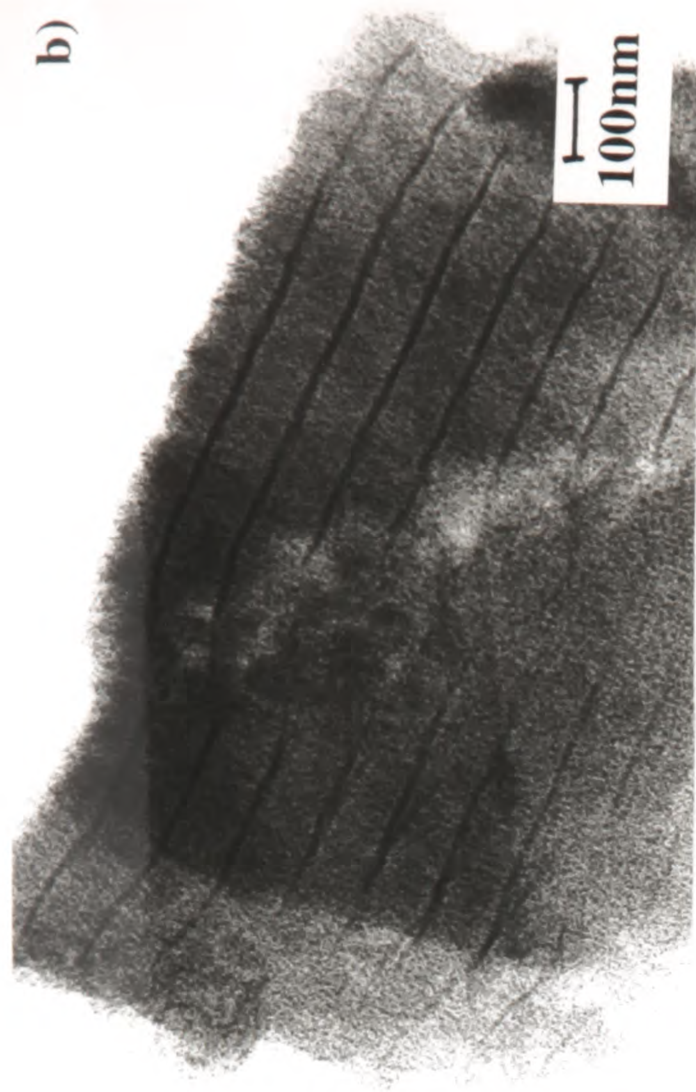
f) Diffraction Pattern
Note that diffraction spots are more distinct than for p-type PS, but are still streaked.

Figure 6.4 - TEM micrographs of cross-sections of p^+-type porous silicon (Anodisation current density = $100mAcm^{-2}$)



a) P^+-Type porous silicon heterostructure
Formed by alternating current density between $10mAcm^{-2}$ for 1 second and $250mAcm^{-2}$ for 2 seconds.





b) P-Type porous silicon heterostructure
Formed by alternating current density between $10mAcm^{-2}$ for 1 second and $120mAcm^{-2}$ for 2 seconds

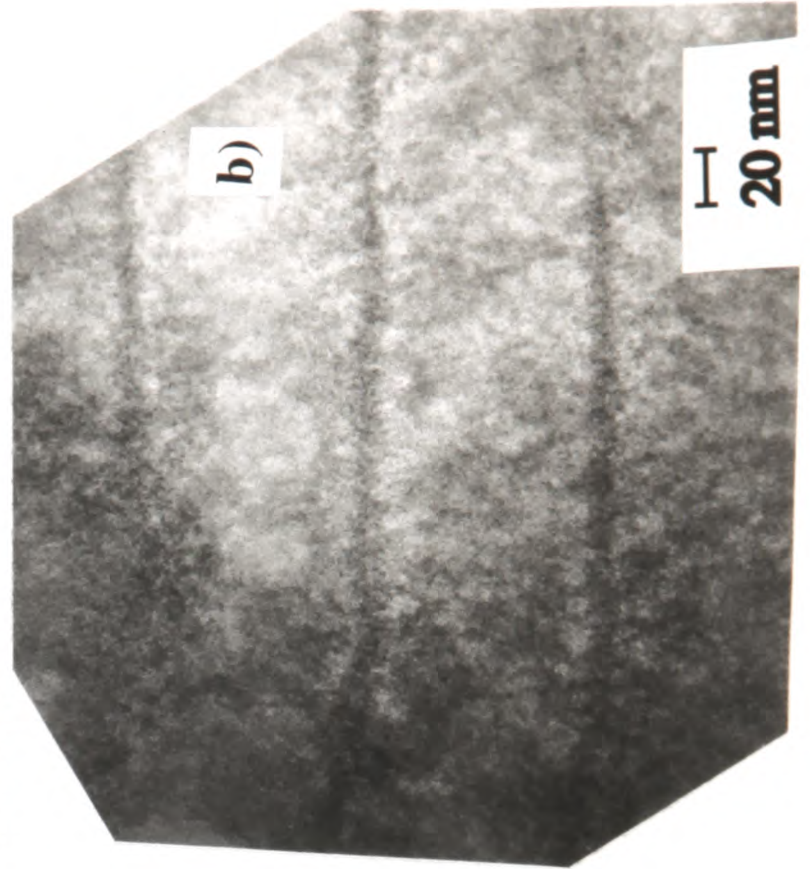


Figure 6.5 - TEM micrographs of p-type and p^+-type porous silicon heterostructures
Heterostructures were formed by alternating the anodisation current between low and hig values, in order to allow the film thickness formed at a particular value of anodisation currer to be measured. In each case, the darker bands correspond to porous silicon formed at th lower values of current density - they have a more compact, denser structure.

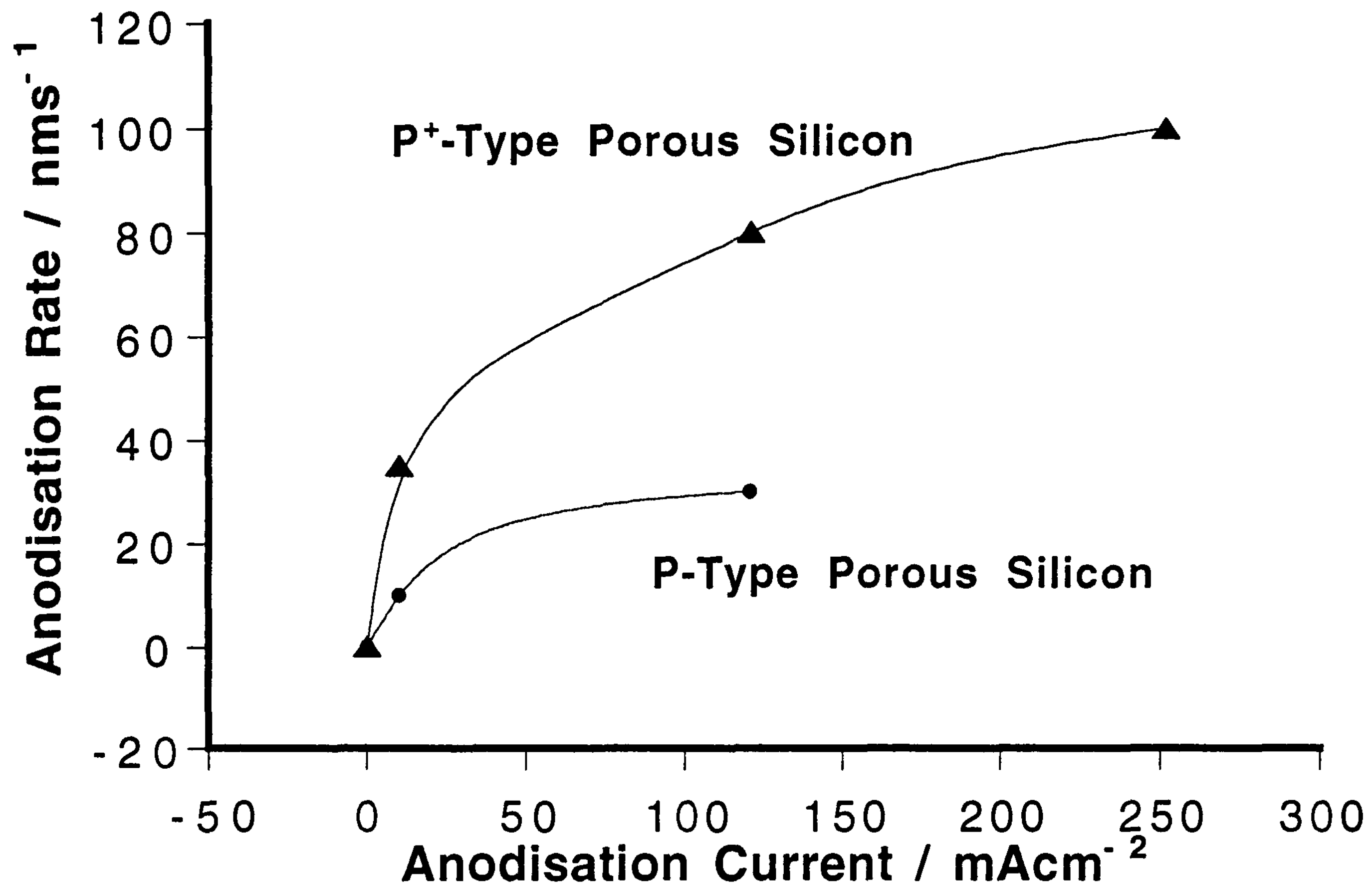
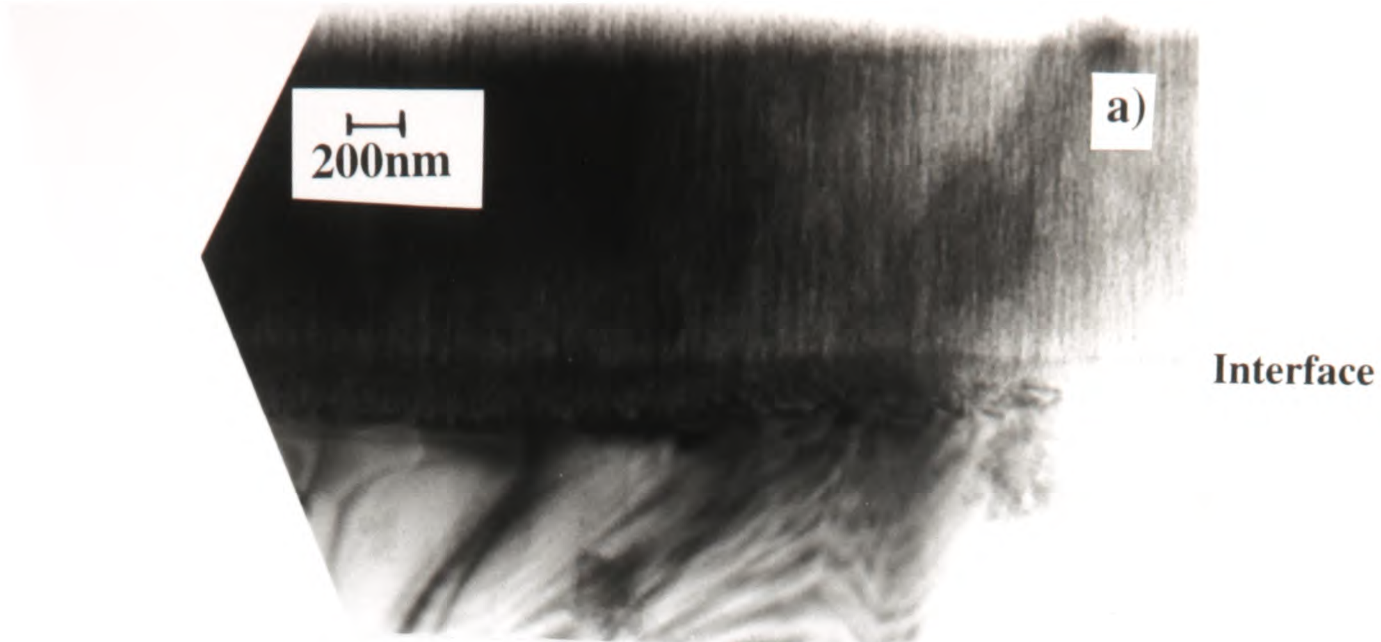


Figure 6.6 - Anodisation Rate on Flat Plane Plotted versus Anodisation Current for P-Type and P+-Type Silicon

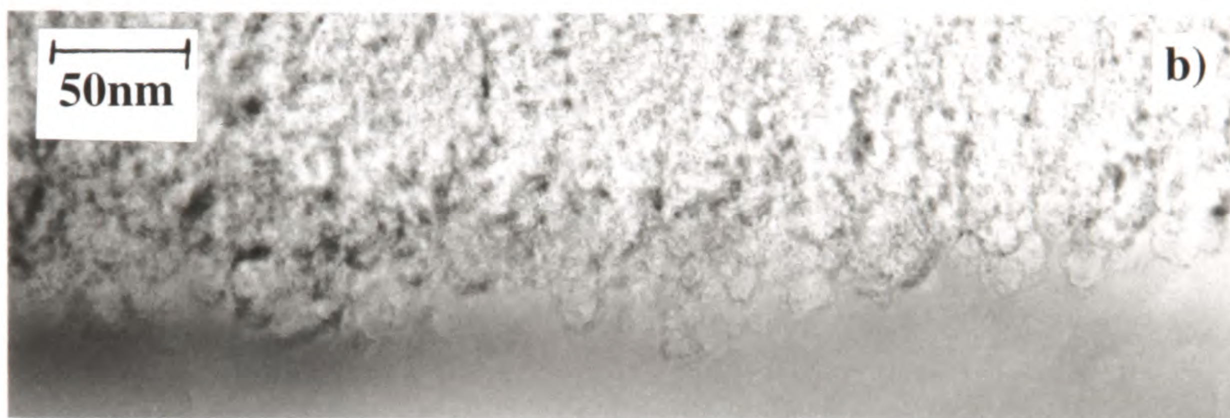
Data for this plot was obtained from studies of the heterostructures and the porous silicon layer still attached to the substrate.

Substrate Type	Current Density	Formation Rate nms^{-1}
P-Type	$10mA/cm^2$	$10nms^{-1}$
	$120mA/cm^2$	$30nms^{-1}$
P+ Type	$10mA/cm^2$	$35nms^{-1}$
	$120mA/cm^2$	$80nms^{-1}$
	$250mA/cm^2$	$100nms^{-1}$

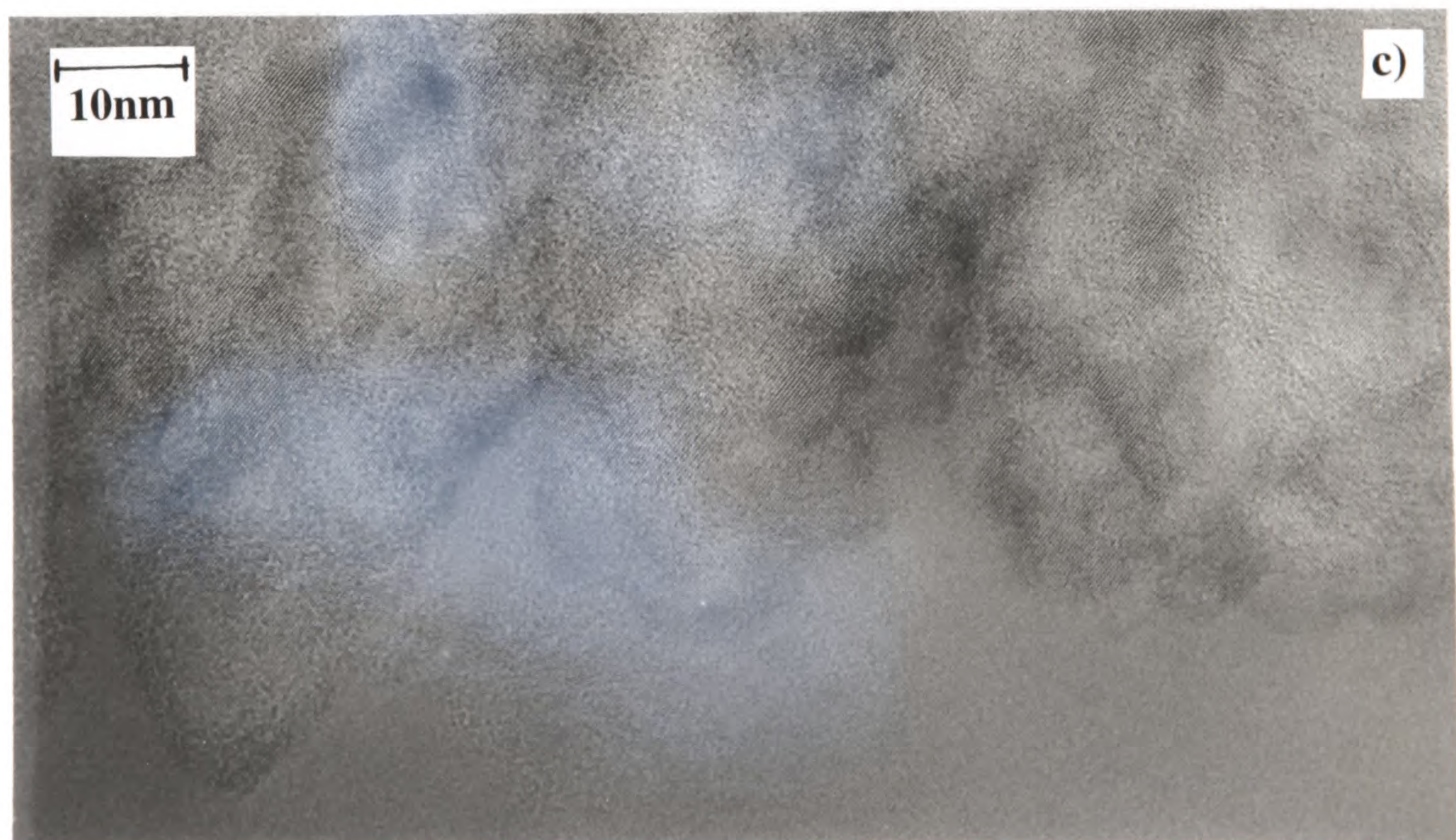
Table 6.6: Effect of Anodisation Current on Porous Silicon Layer Thickness on Flat Silicon Substrate



a) Porous silicon layer still attached to underlying substrate



b) Porous silicon / bulk silicon interface
Note the pore ends

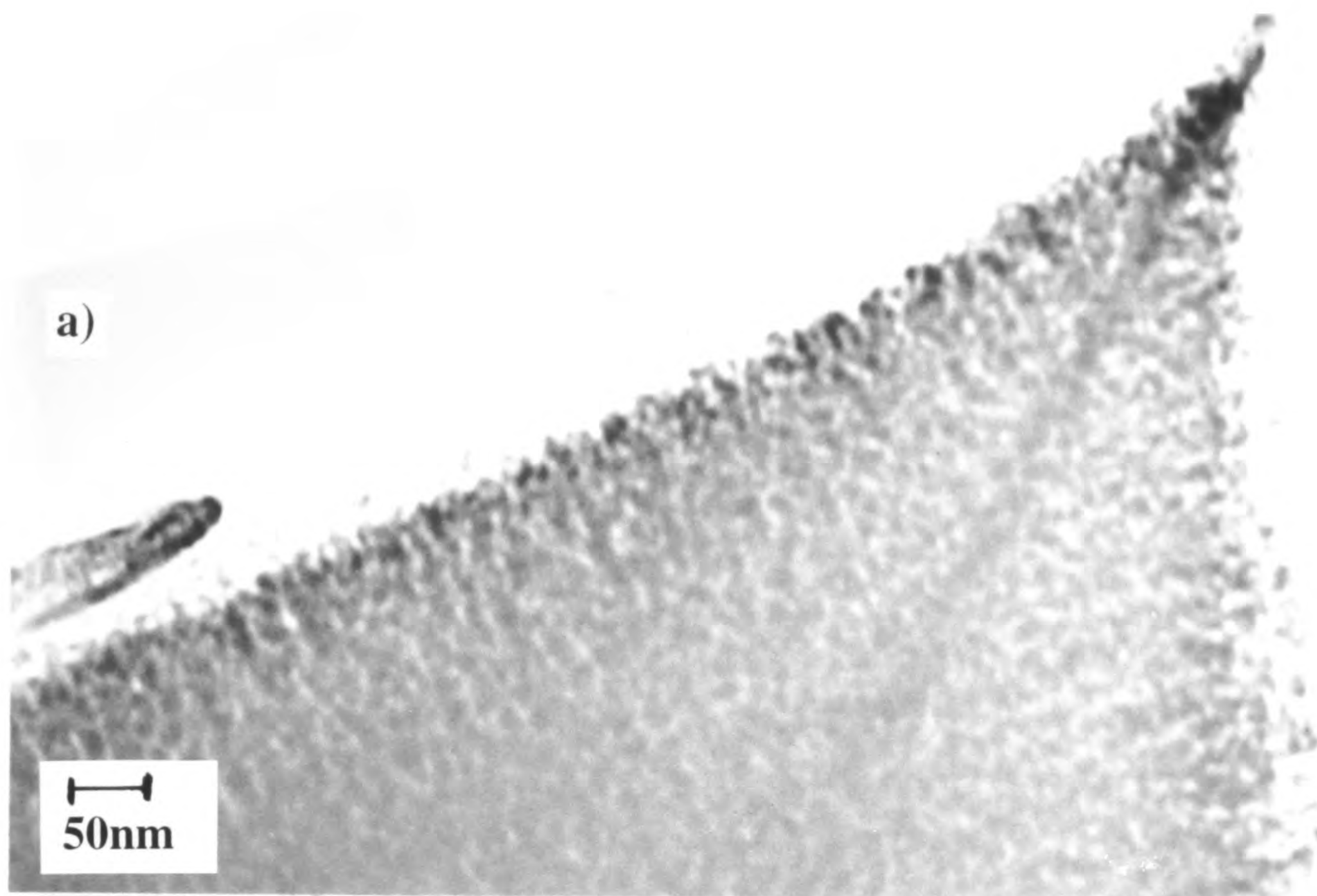


c) Higher magnification image of porous silicon / bulk silicon interface
Note the sharp points of silicon formed between the pore ends - these points could locally enhance an applied electric field.

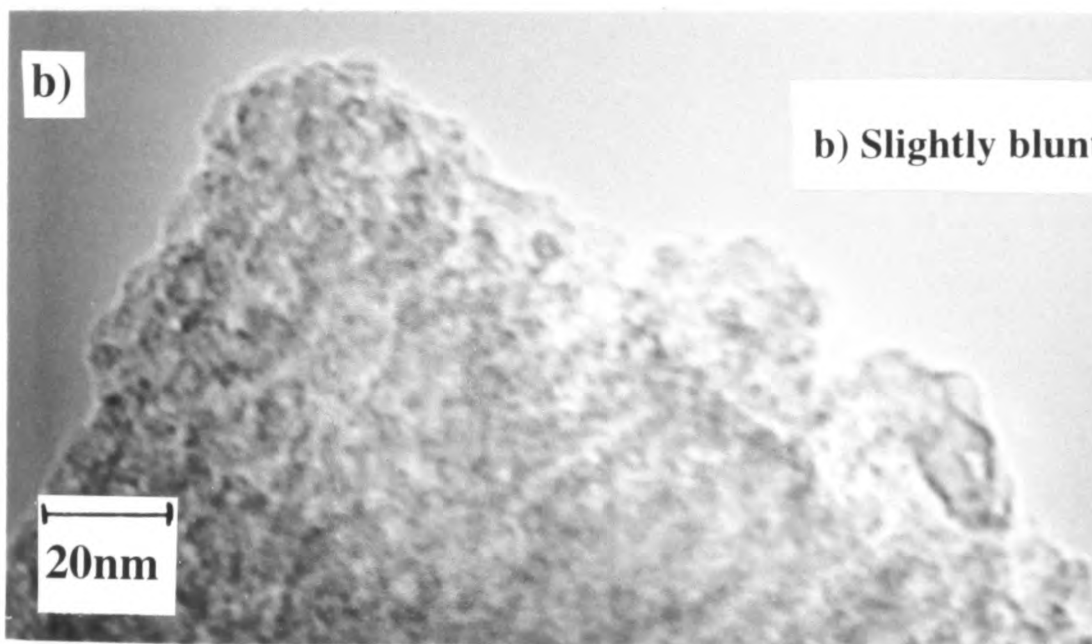
Figure 6.7 - TEM micrographs of p^+-type porous silicon / bulk silicon interface
(Anodisation at 100

Substrate Type	Current Density	Time / seconds
P-Type	$30mAcm^{-2}$	5 10 30 120 300
P+ Type	$100mAcm^{-2}$	0.25 3 10

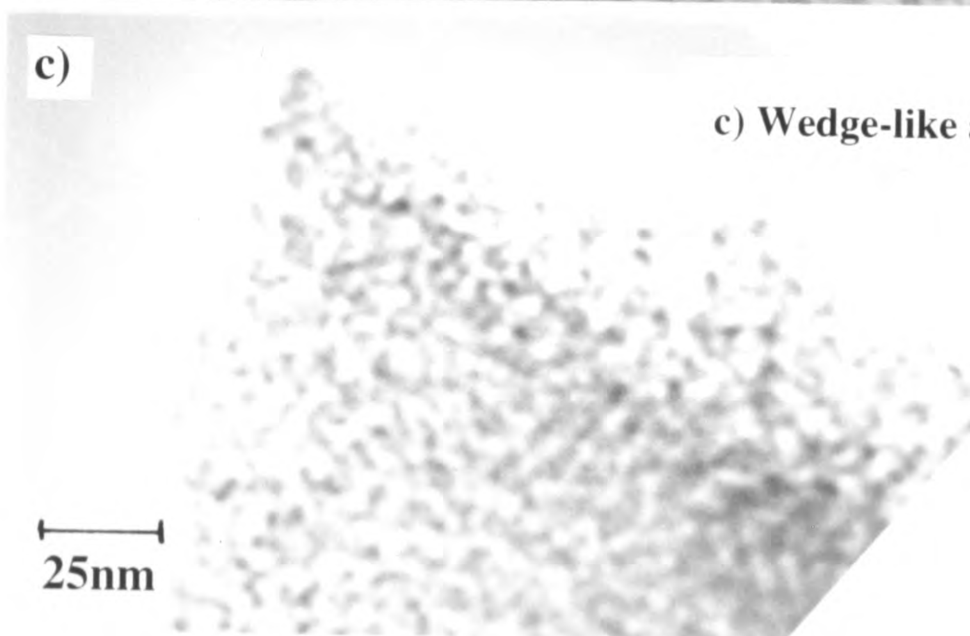
Table 6.7: Anodisation Conditions used to form PS Layers on Silicon Field Emitter Arrays (FEAs)



a) Sharp anodised emitter

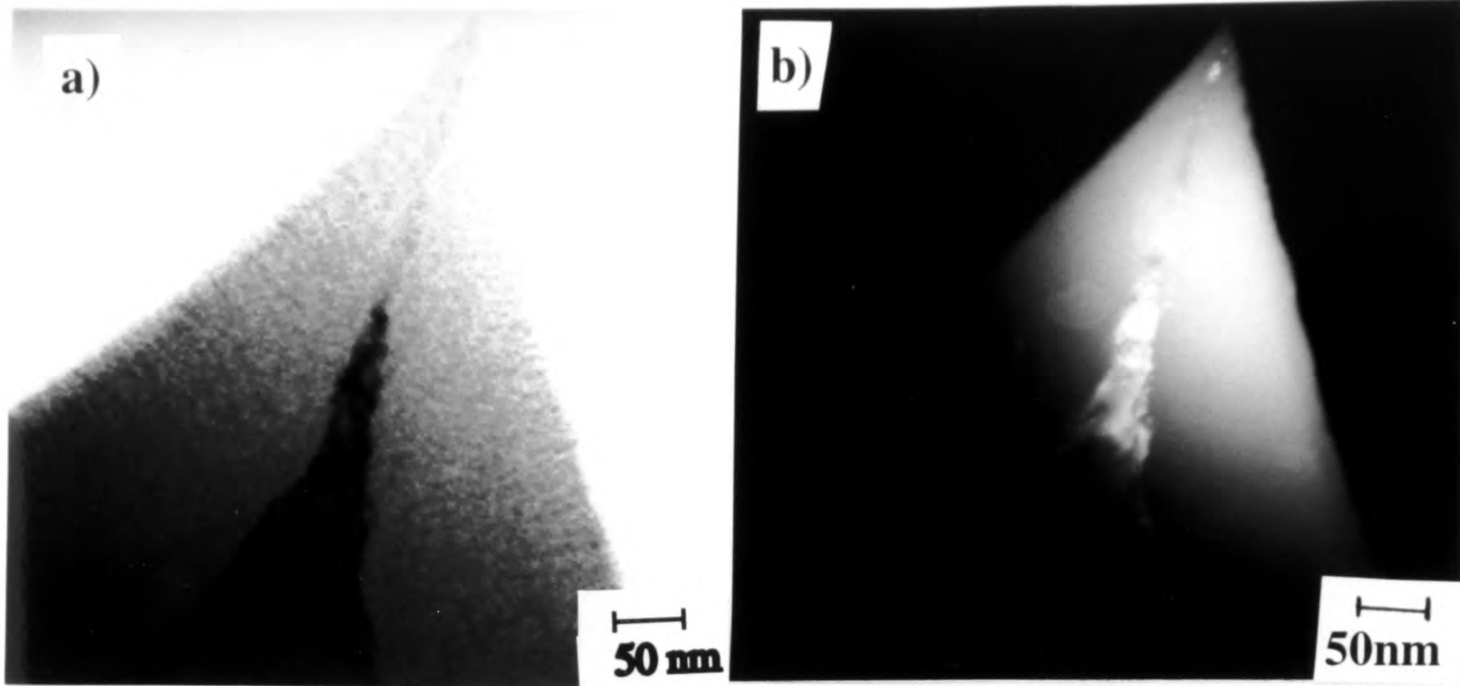


b) Slightly blunter anodised emitter



c) Wedge-like anodised emitter

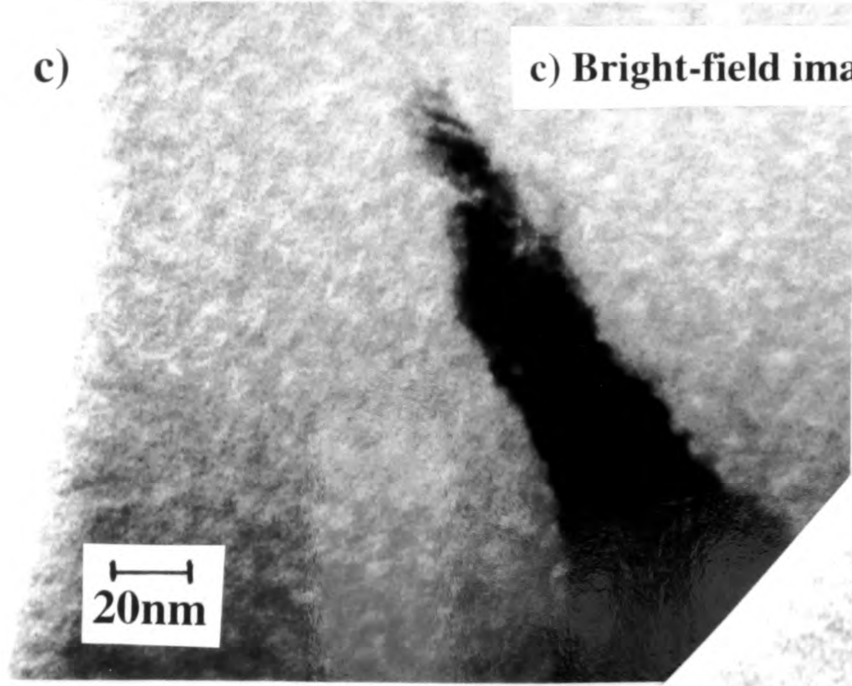
Figure 6.8 - TEM micrographs of several anodised p-type silicon field emitter apexes
These images show that the entire tip surface was made rough by the anodisation process - it is covered with asperities. Prior to anodisation, only a few asperities were found at the tip apex. Asperities are ~1-4nm high and of similar width. These emitters were anodised for 30 seconds using an anodisation current of $30mAcm^{-2}$.



a) Bright-field image of tip
Note that from this image, it is difficult to tell whether the silicon core is continuous to the tip end.

b) Dark-field image of tip
Note that the dark-field image shows that the silicon core is continuous to the tip end.

c) Bright-field image of core at higher magnification



Anodisation current = $30 mAcm^{-2}$

d) Bright-field image of core near to tip section
Note that the core in this image is almost vertical and is very thin - it is ~10nm thick and is ~200nm in length.

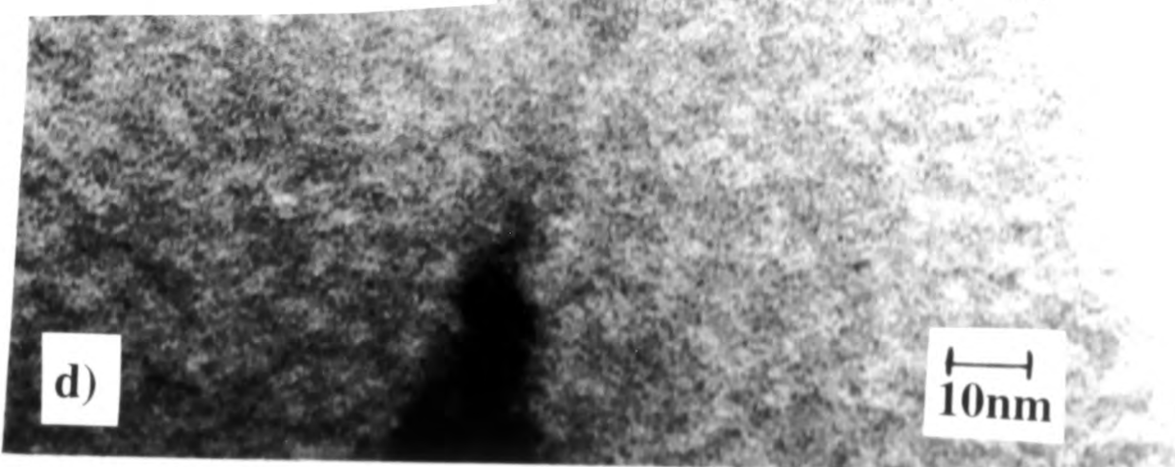
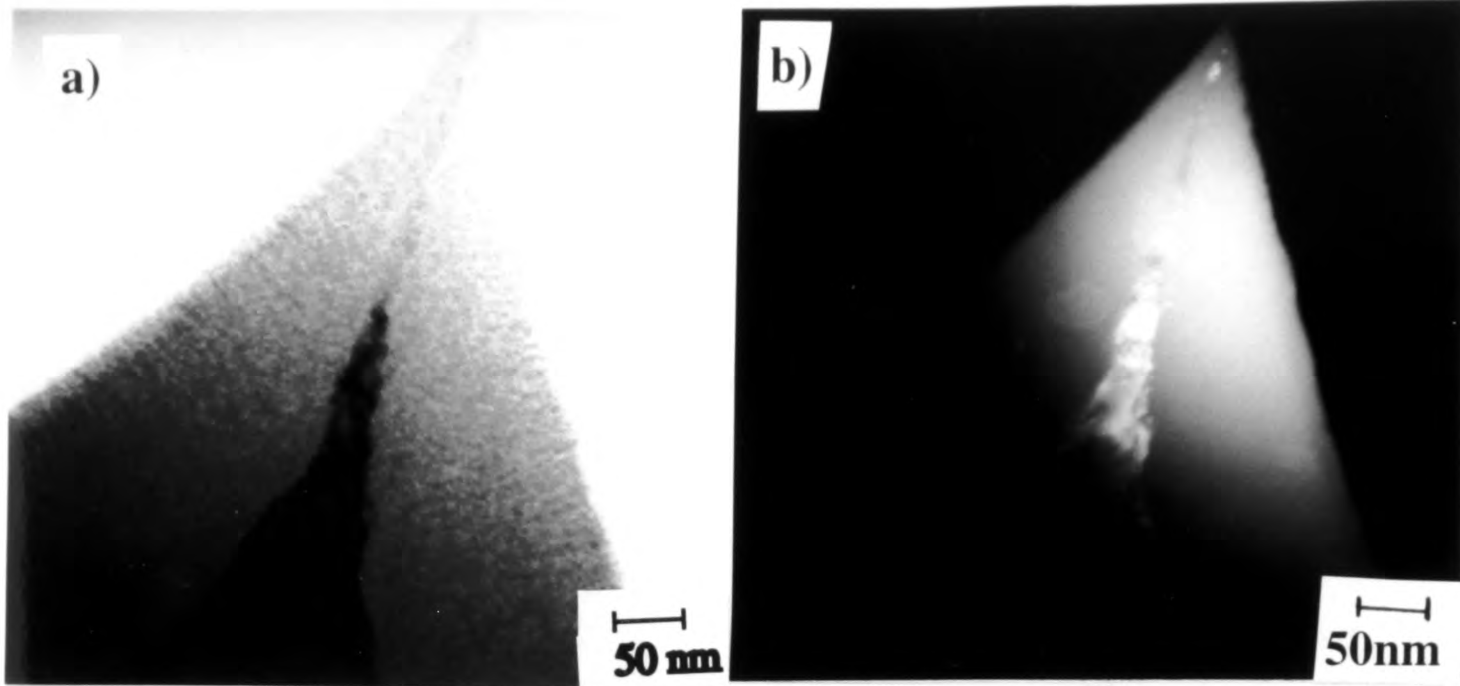
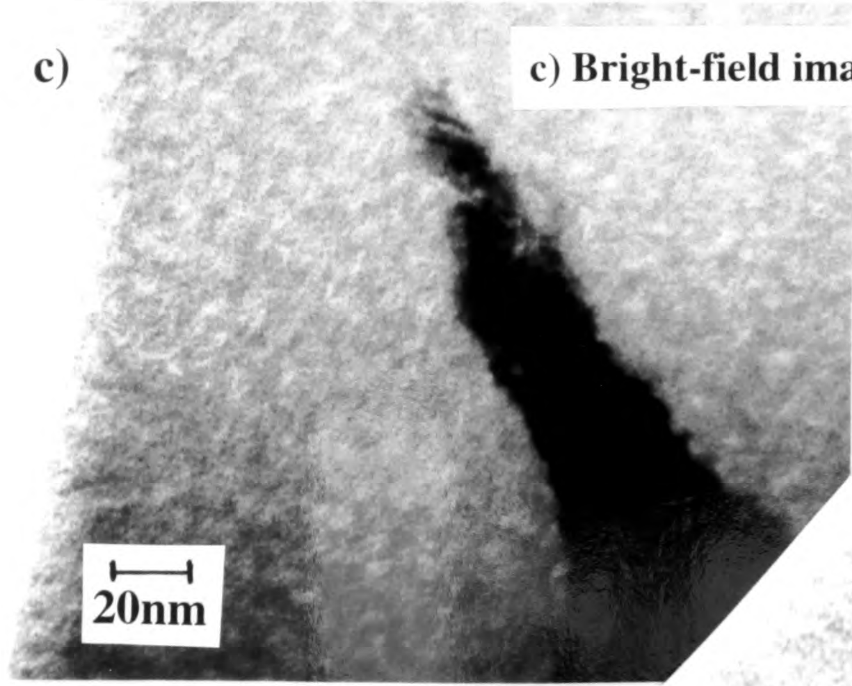


Figure 6.10 - TEM micrographs of core of p-type emitter anodised for 30 seconds
A dark silicon core can be resolved within the porous silicon layer of each tip. The geometry of each core is very different to the original geometry of the tip - the aspect ratio is much higher.



a) Bright-field image of tip
Note that from this image, it is difficult to tell whether the silicon core is continuous to the tip end.

b) Dark-field image of tip
Note that the dark-field image shows that the silicon core is continuous to the tip end.



c) Bright-field image of core at higher magnification

Anodisation current = 30mAcm^{-2}

d) Bright-field image of core near to tip section
Note that the core in this image is almost vertical and is very thin - it is ~10nm thick and is ~200nm in length.

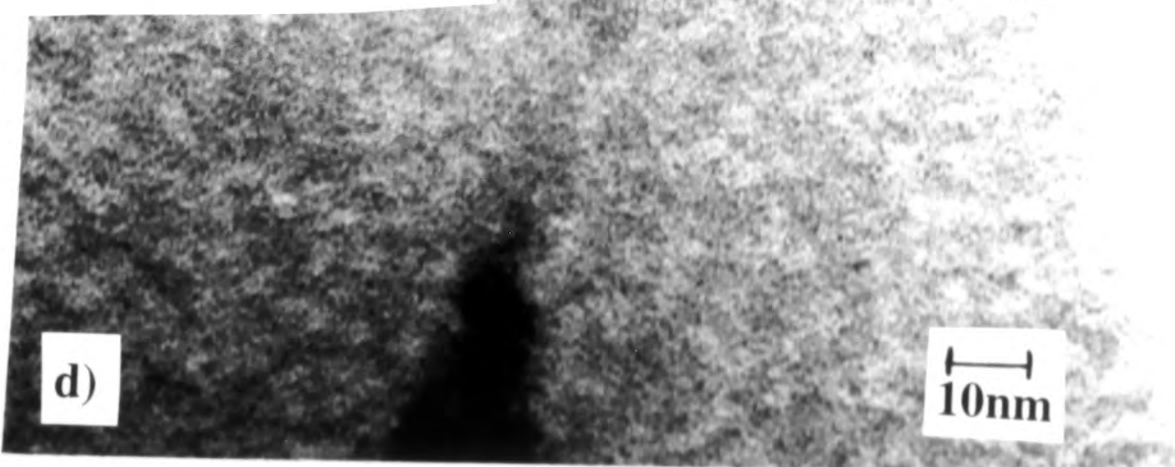
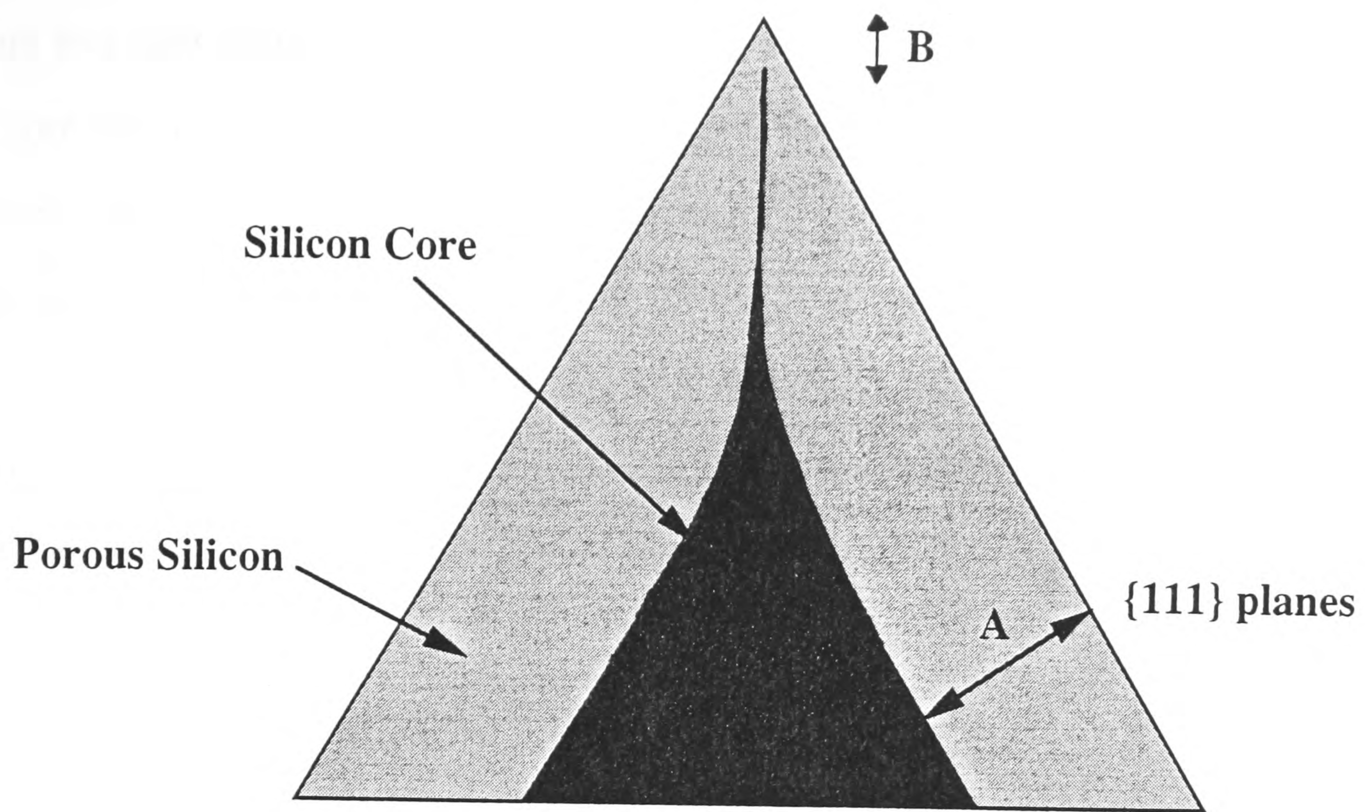
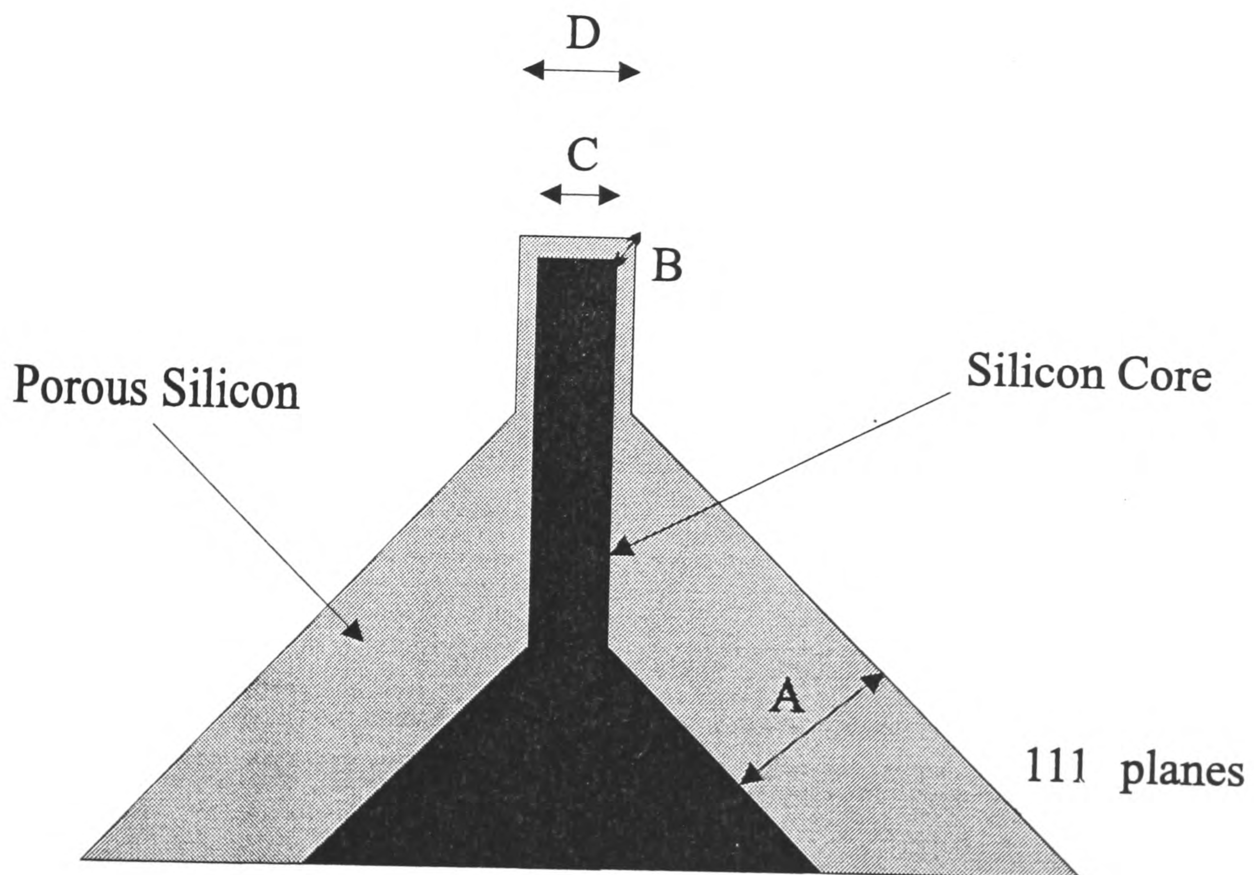


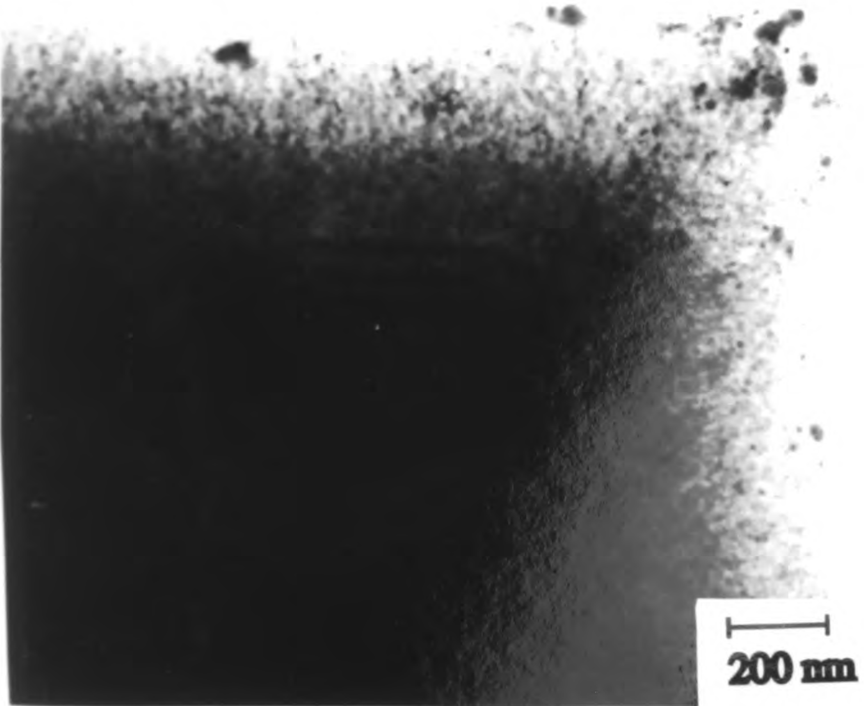
Figure 6.10 - TEM micrographs of core of p-type emitter anodised for 30 seconds
A dark silicon core can be resolved within the porous silicon layer of each tip. The geometry of each core is very different to the original geometry of the tip - the aspect ratio is much higher.



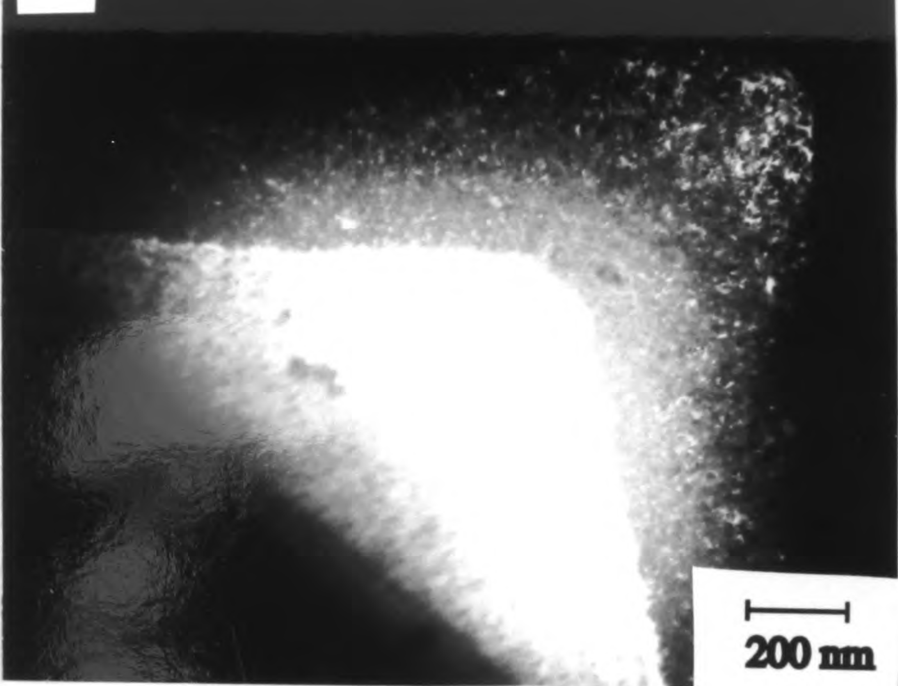
a) Sharp Emitter



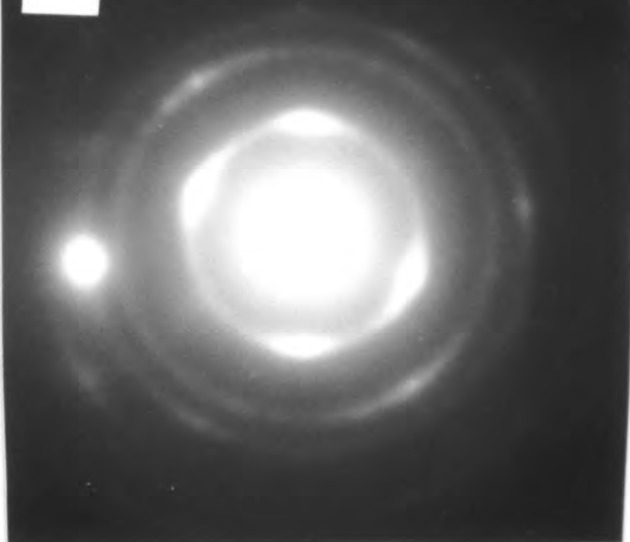
b) Flat-Topped Emitter



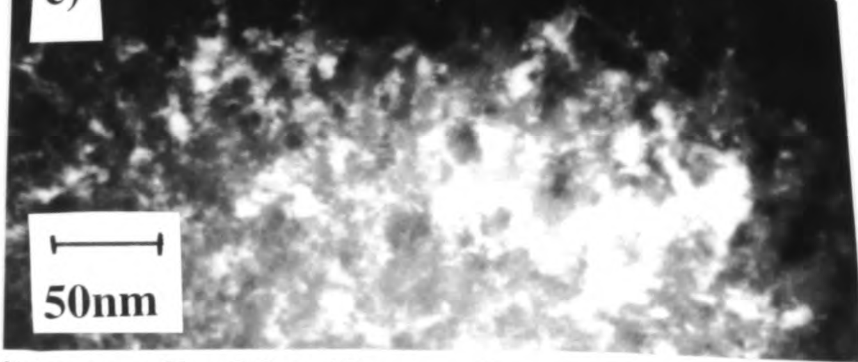
a) Bright-Field Image
The outline of the silicon core can just be observed



b) Dark-Field Image
The outline of the silicon core can be observed more easily in dark-field mode than in bright-field mode.



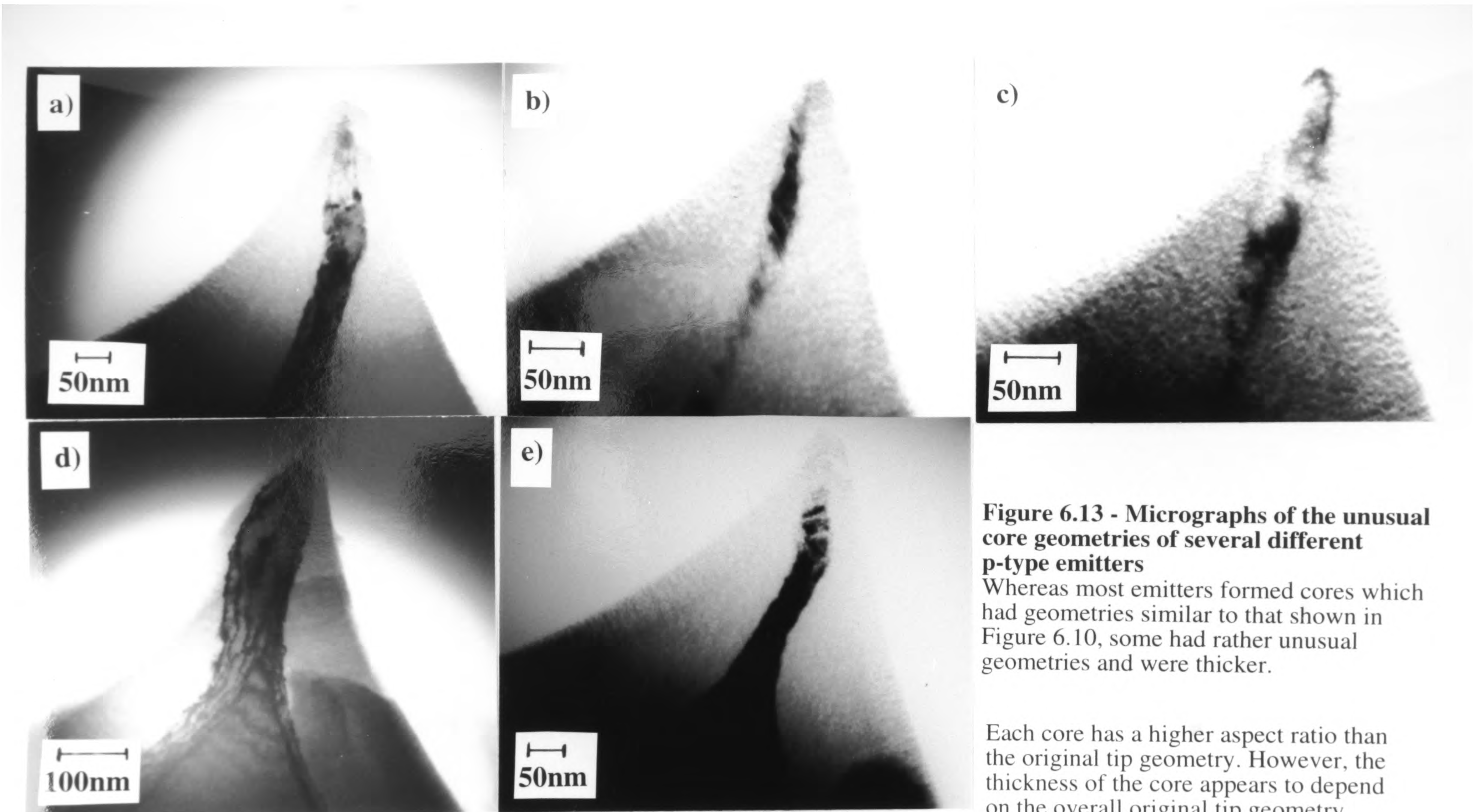
c) Diffraction pattern from anodised p^+-type silicon emitter



d) and e) Higher magnification images of bright and dark field images in a) and b)
Images were taken at edge of the emitter

igure 6.12 - TEM micrographs of core of p^+-type emitter anodised for 10 seconds
he geometry of the core of this anodised p^+-type emitter is very different to the geometry of ie core of the anodised p-type emitter shown in Figure 6.10. The porous silicon layer is hicker at the apex than down the emitter sides - in this case the layer is ~400nm thick at the ipex and ~300nm on the emitter sides. For anodised p-type emitters, the porous silicon layer it the apex was always much thinner than the layer on the emitter sides.

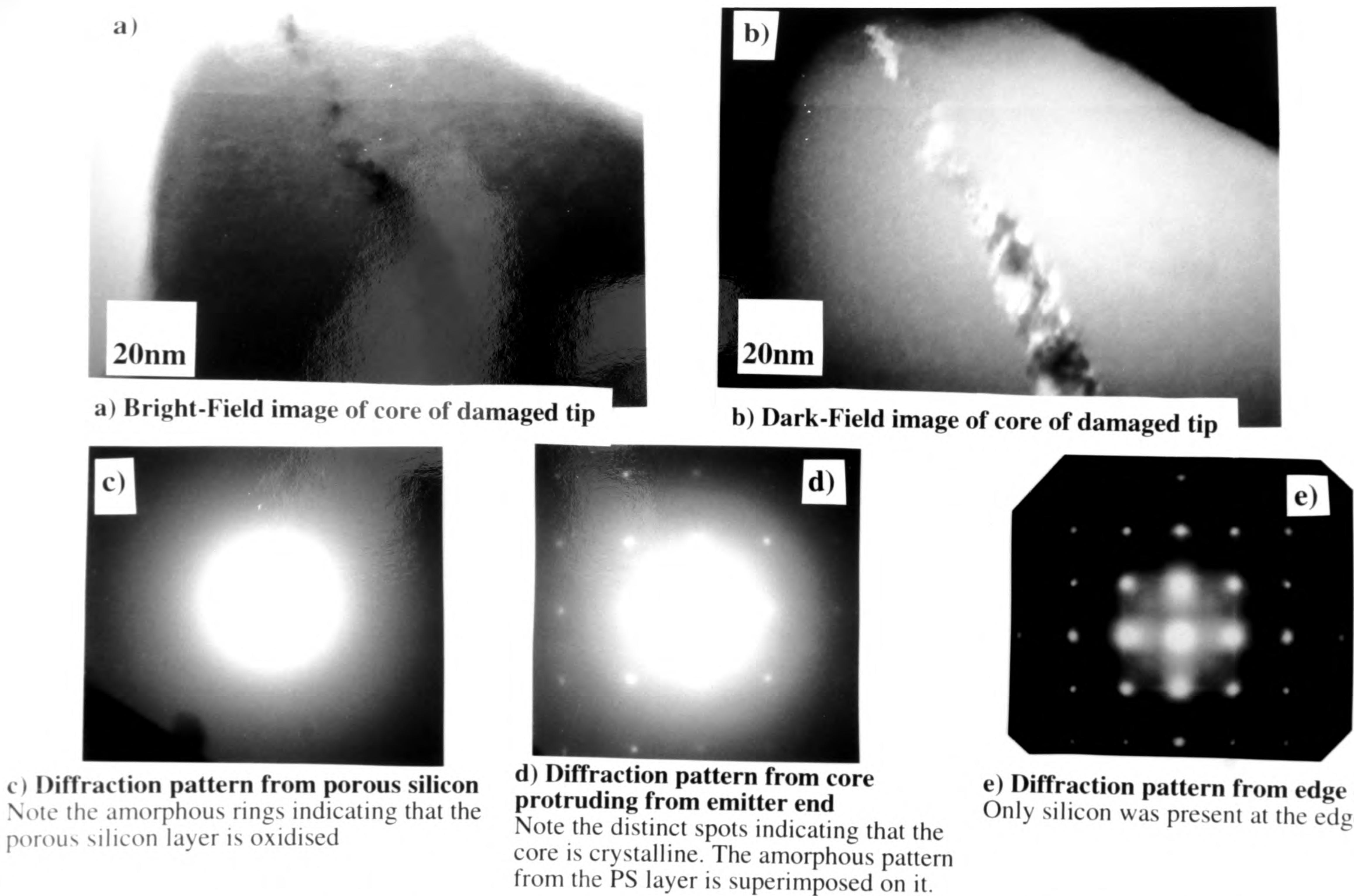
Anodisation at $100mAcm^{-2}$ for 10 seconds



(Anodisation at $30mAcm^{-2}$ for 30 seconds)

Figure 6.13 - Micrographs of the unusual core geometries of several different p-type emitters
Whereas most emitters formed cores which had geometries similar to that shown in Figure 6.10, some had rather unusual geometries and were thicker.

Each core has a higher aspect ratio than the original tip geometry. However, the thickness of the core appears to depend on the overall original tip geometry.



a) Bright-Field image of core of damaged tip

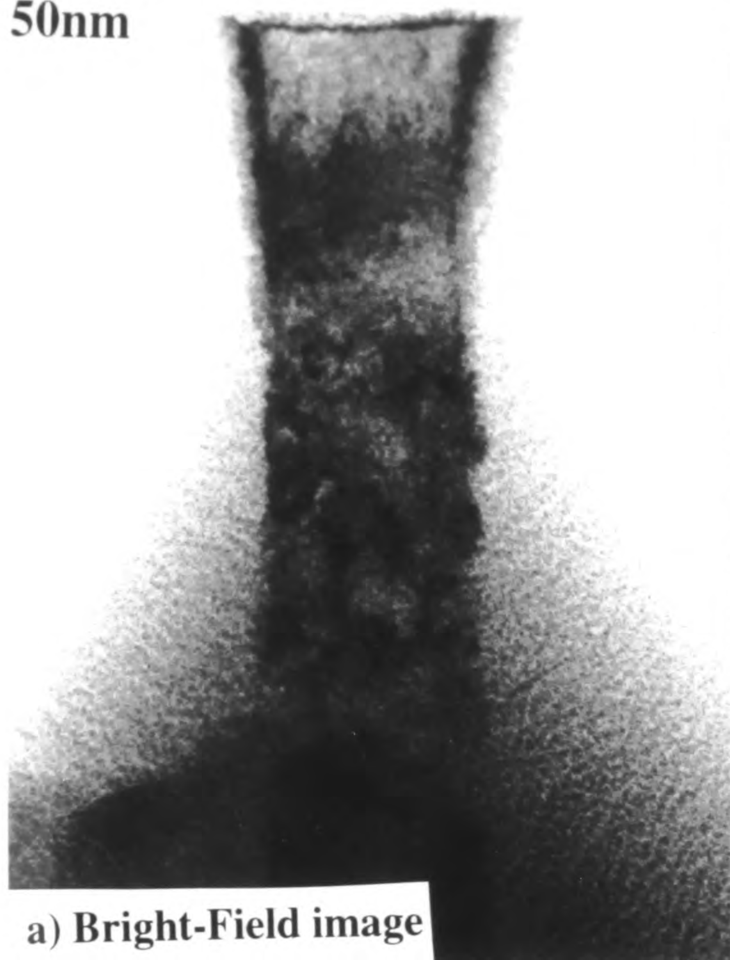
b) Dark-Field image of core of damaged tip

c) Diffraction pattern from porous silicon
Note the amorphous rings indicating that the porous silicon layer is oxidised

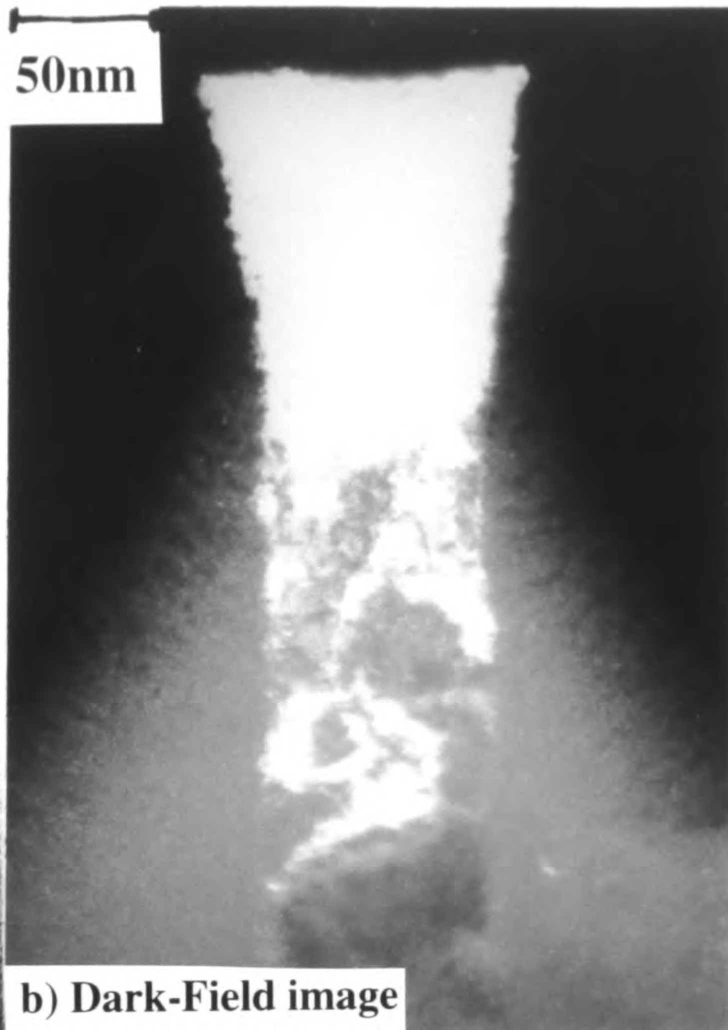
d) Diffraction pattern from core protruding from emitter end
Note the distinct spots indicating that the core is crystalline. The amorphous pattern from the PS layer is superimposed on it.

e) Diffraction pattern from edge of sample
Only silicon was present at the edge of the sample

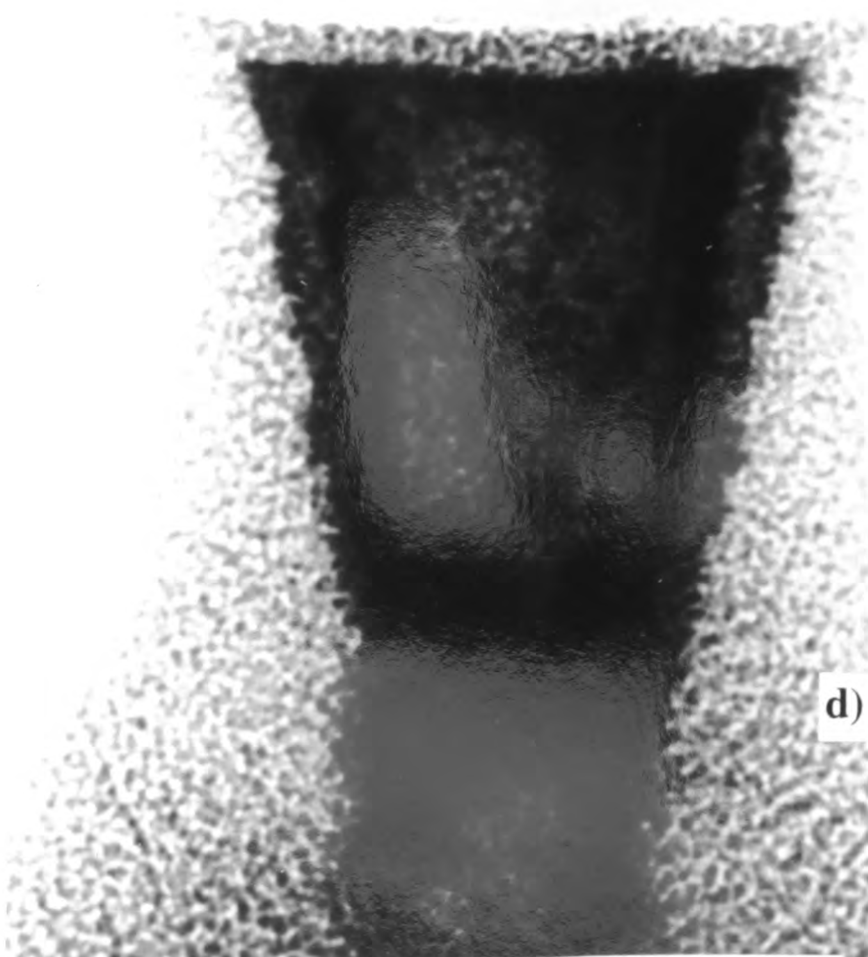
Figure 6.14 - Higher Magnification Images of Core Region of Damaged Tip and Information from Diffraction Patterns
A tip was found which had been slightly damaged prior to insertion into the TEM. The core was protruding slightly from the top of the tip, so diffraction patterns could easily be taken from the core.



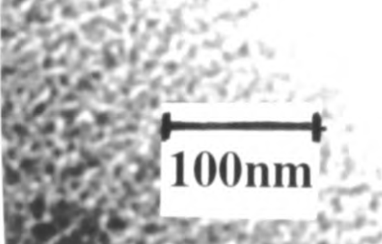
a) Bright-Field image



b) Dark-Field image

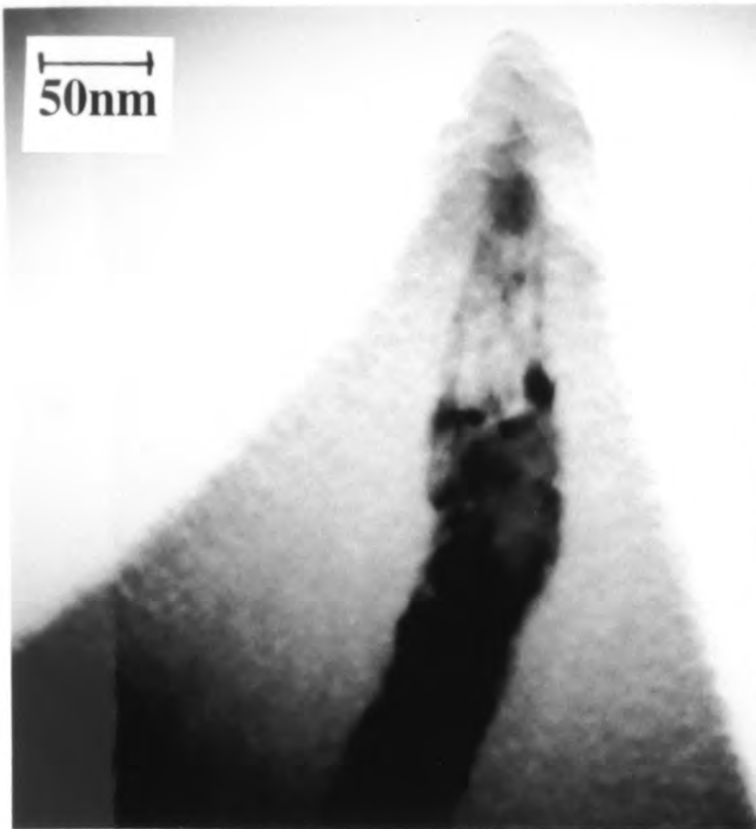


c) Higher magnification bright-field image
Note that this image is slightly under-focused. The thickness of the layer at the tip is slightly thicker than at the apex of point-like tips - it is ~35nm thick.

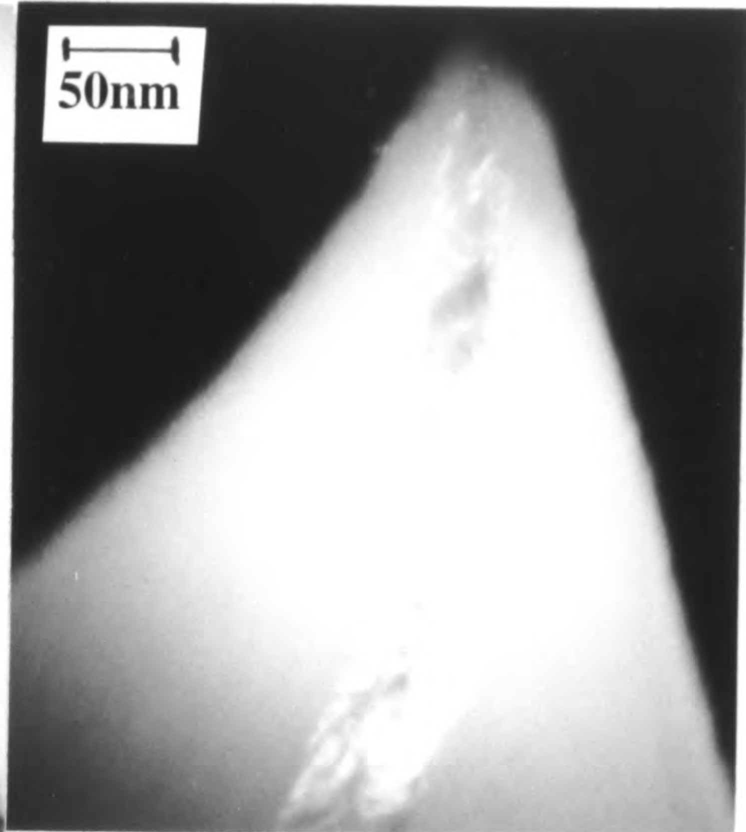


d) In-focus image at apex corner

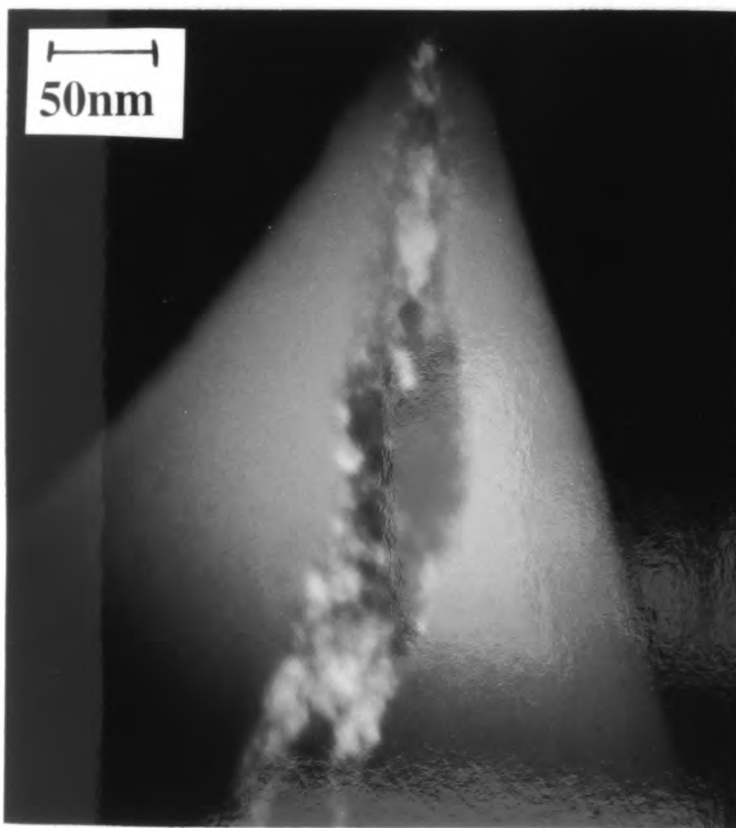
Figure 6.15 - TEM micrographs of anodised flat-topped p-type emitters anodised for 30 seconds
As for point-like p-type emitters, a high aspect ratio core was formed following anodisation. However, the core is much wider than for point-like emitters - it is 450nm wide, due to the difference in starting geometry. (Anodisation anodised at



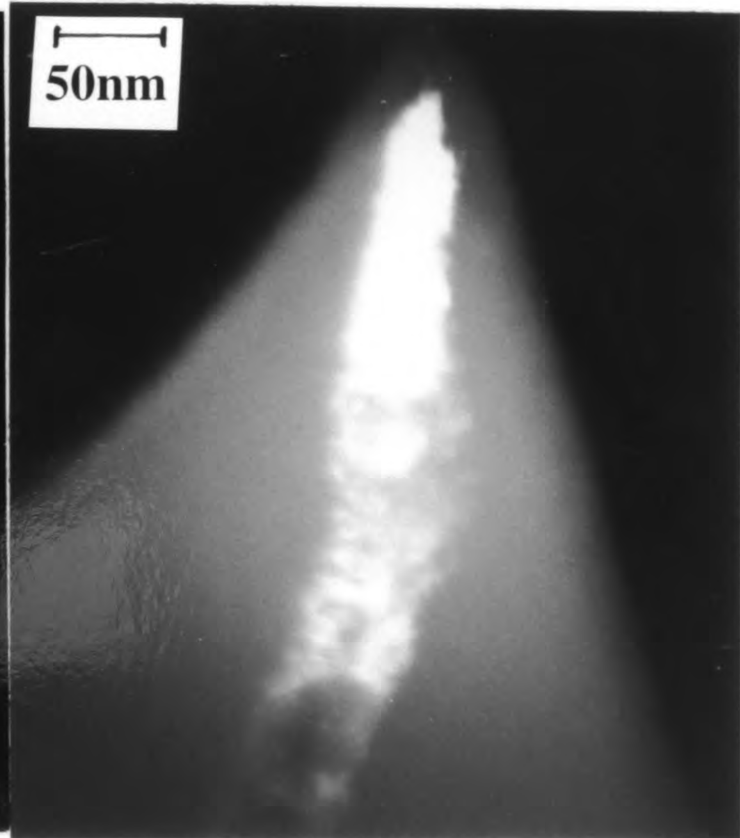
a) Bright-Field Image



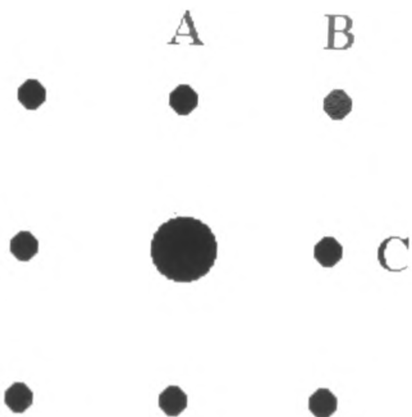
b) Dark-Field Image - Spot A



c) Dark-Field Image - Spot B



d) Dark-Field Image - Spot C



e) Diffraction Pattern

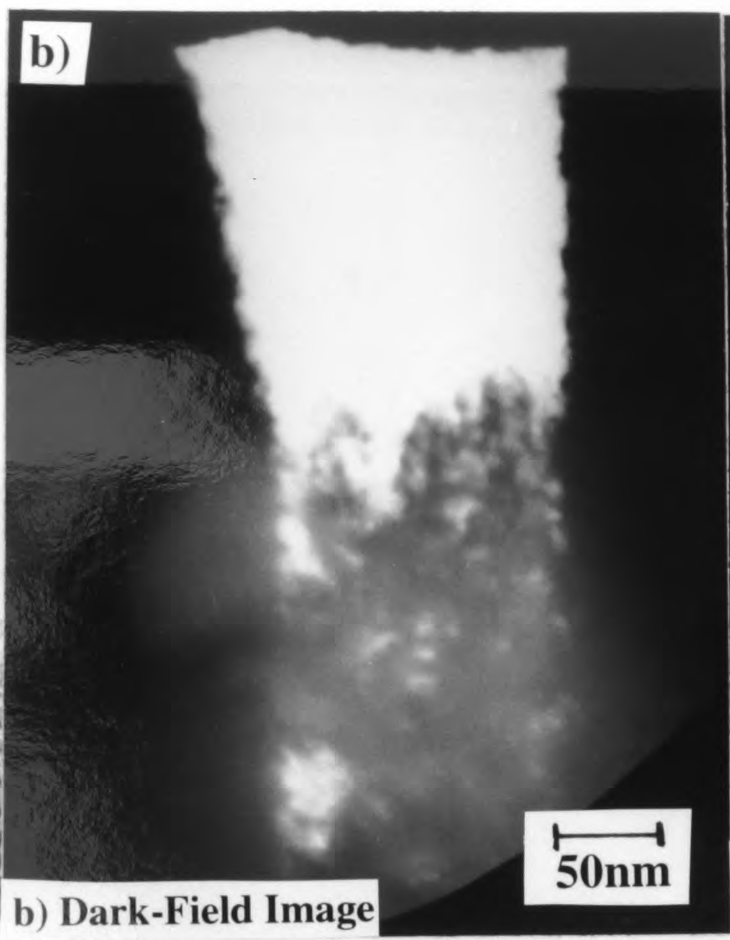
Pattern is that shown in Figure 6.14d

(Anodisation anodised at $30mAcm^{-2}$ for 30 seconds)

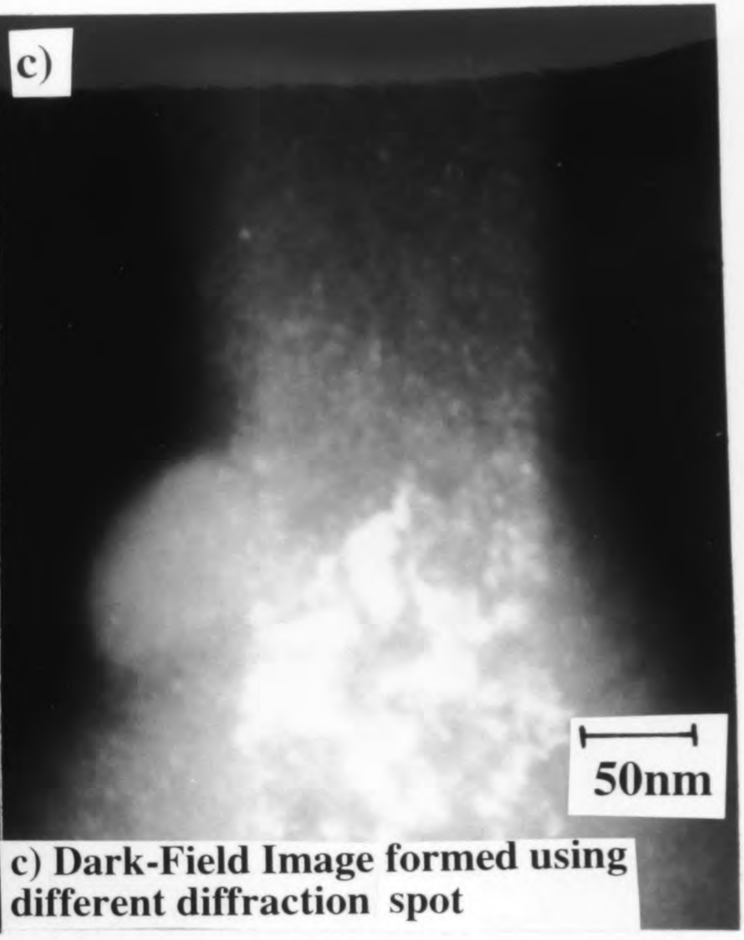
Figure 6.16 - TEM micrographs of a p-type anodised emitter imaged in bright-field and imaged in dark field using three different diffraction spots

It can be seen that bright and dark reflections occur at different positons of the core for the different dark-field images formed using the three different diffraction spots. This suggests that sections of the core are lying at different orientations to other sections.

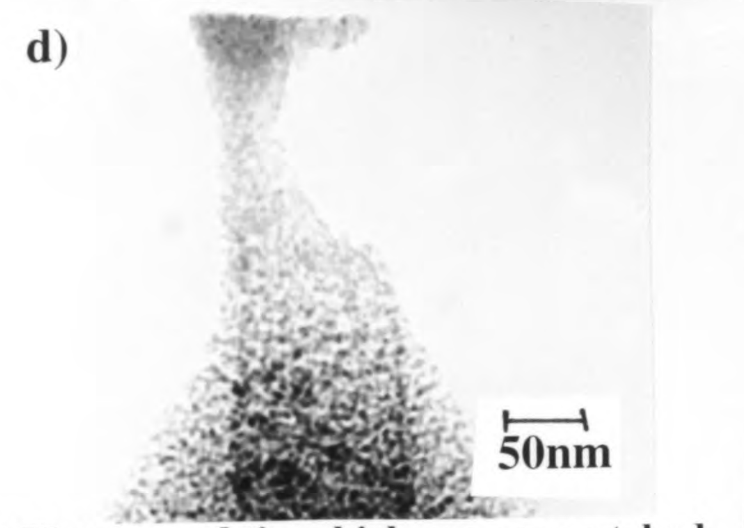
a) Bright-Field Image



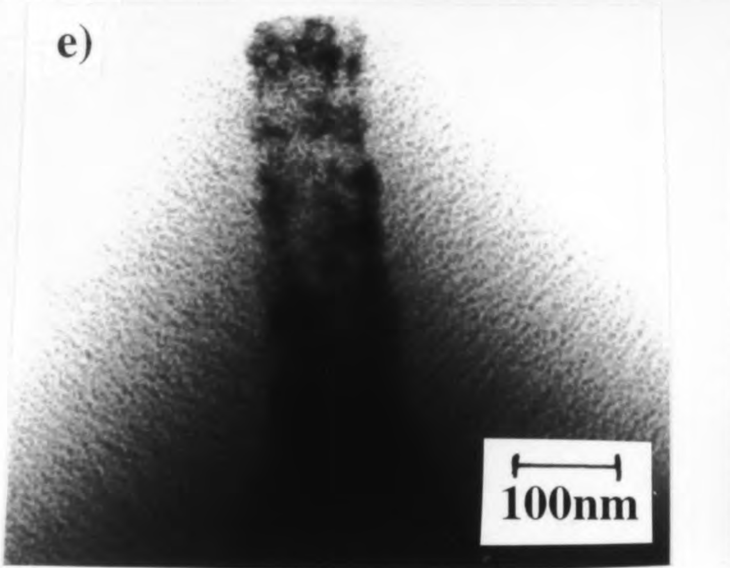
b) Dark-Field Image

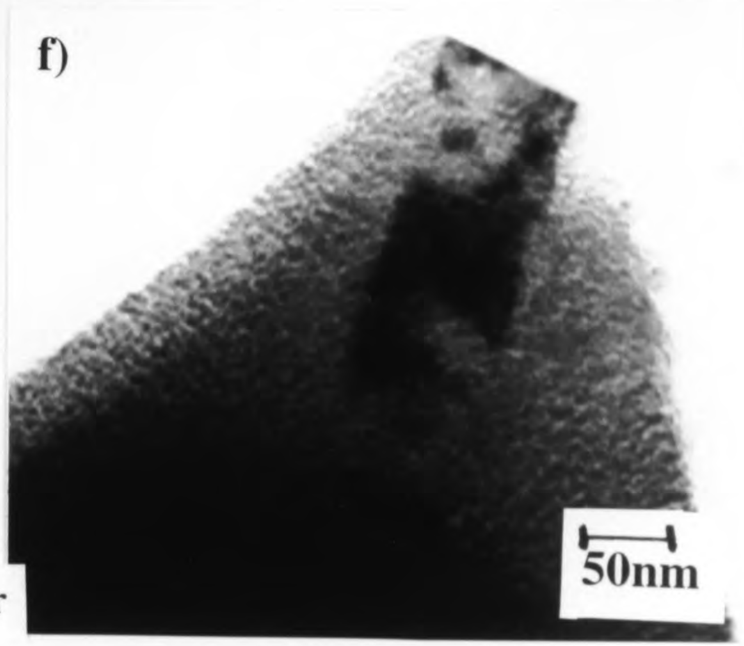


c) Dark-Field Image formed using different diffraction spot

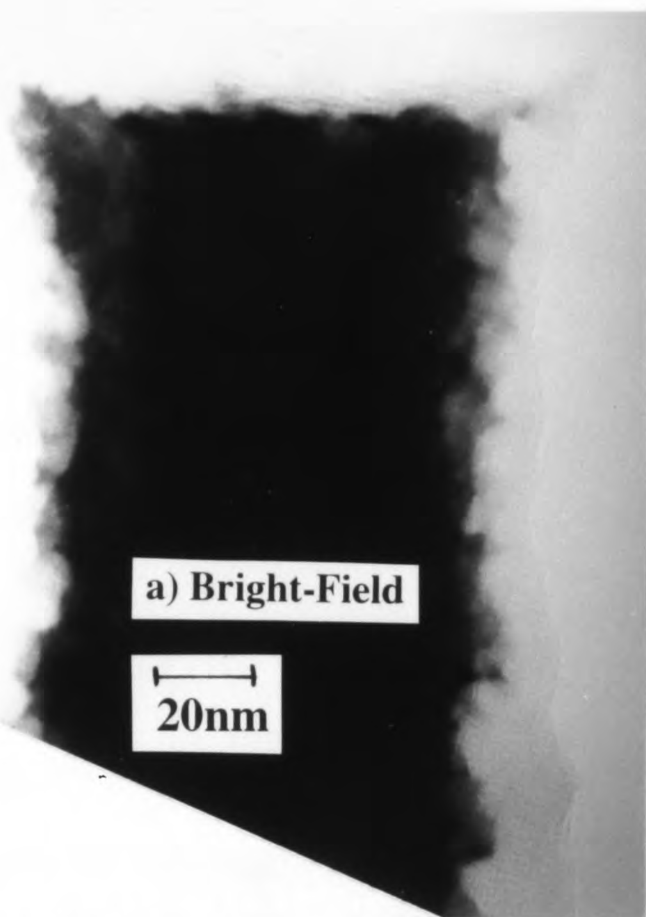


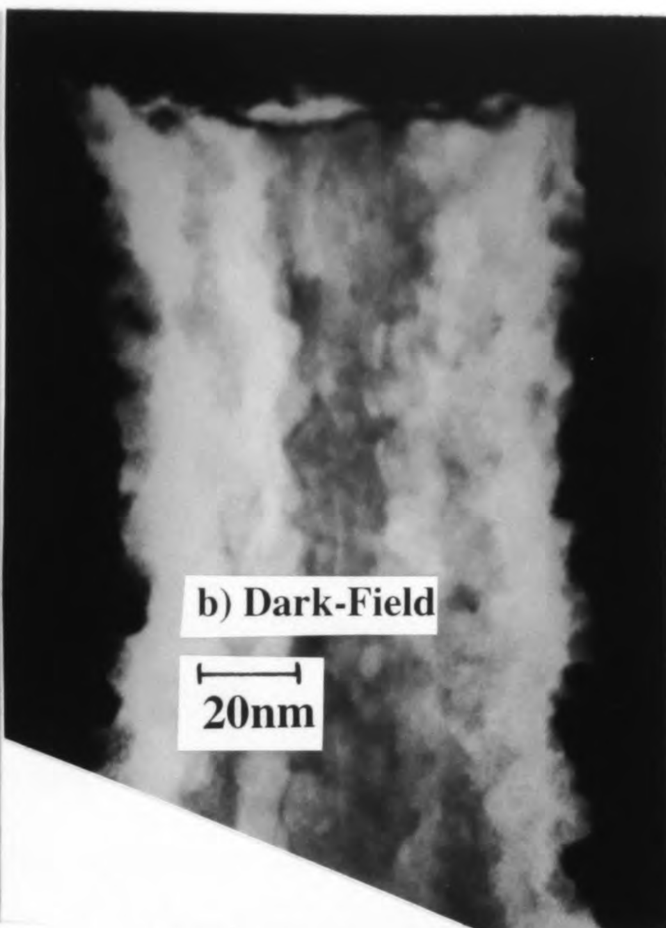
d) Flat-topped tip which was over-etched prior to anodisation, and has almost formed a wedge-shaped emitter



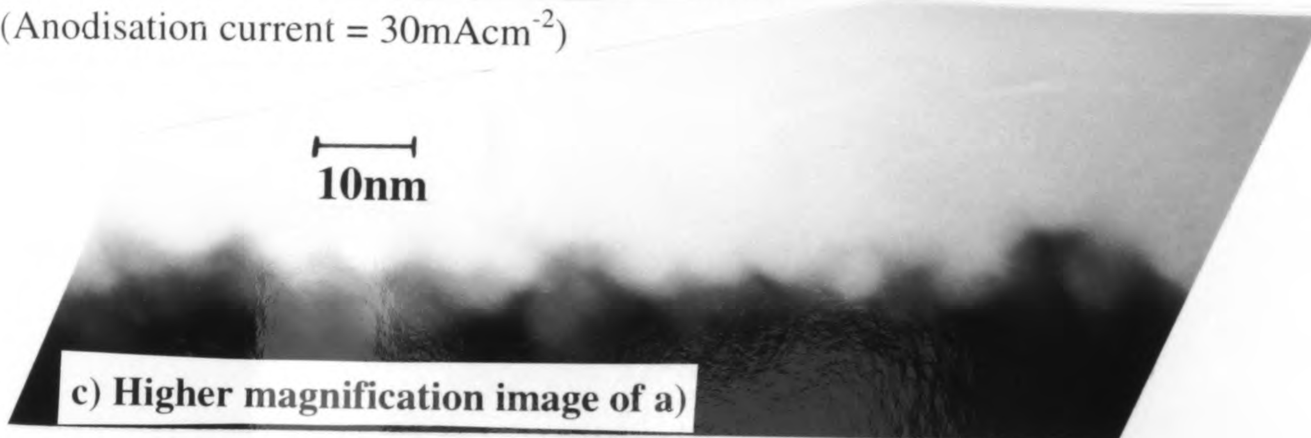


e) and f) Cores of wedge-shaped emitter

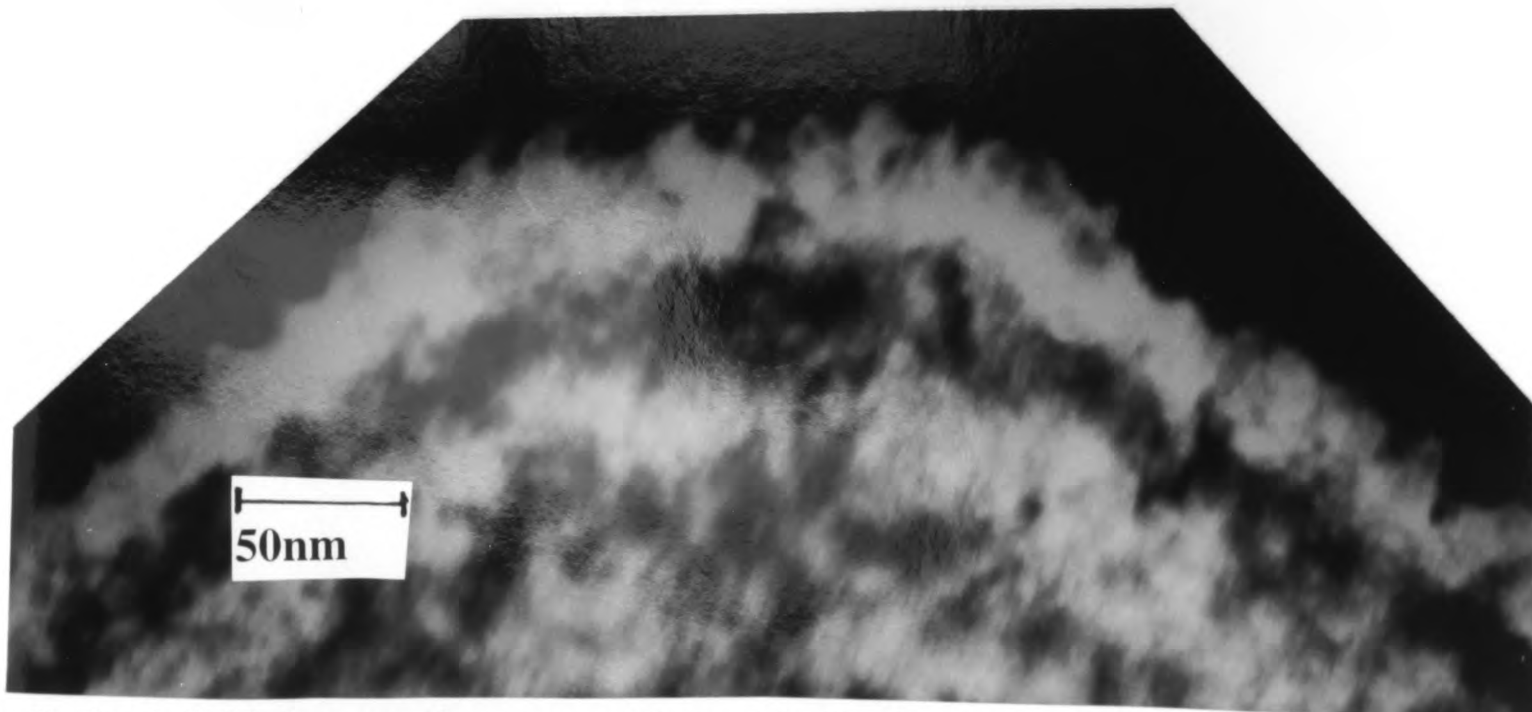




a) and b) Bright-Field and Dark-Field images of p-type emitter anodised for 5 seconds
Note rough porous silicon / bulk silicon interface
(Anodisation current = $30mAcm^{-2}$)



c) Higher magnification image of a)



d) Dark-field image of porous silicon / bulk silicon interface of p^+-type emitter - Anodised for 10 seconds (Anodisation current = $100mAcm^{-2}$)

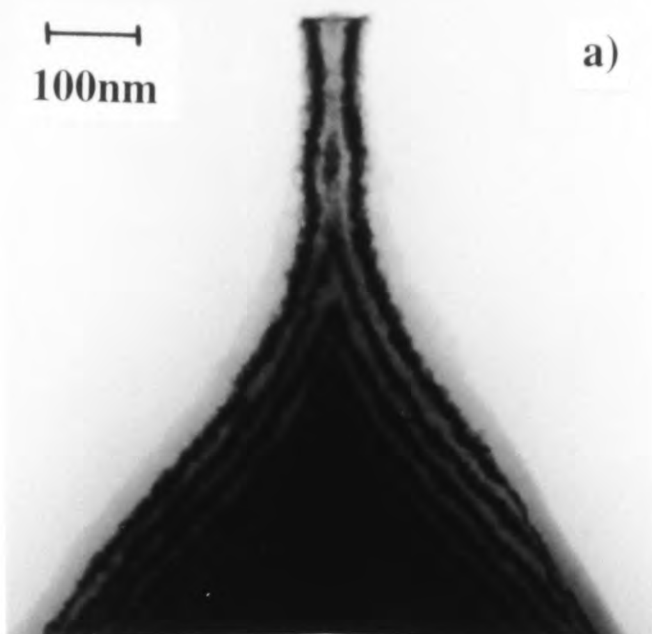


Figure 6.19 - P-Type emitters anodised for 5 seconds and for 120 seconds

(Anodisation current = 30mAcm^{-2})

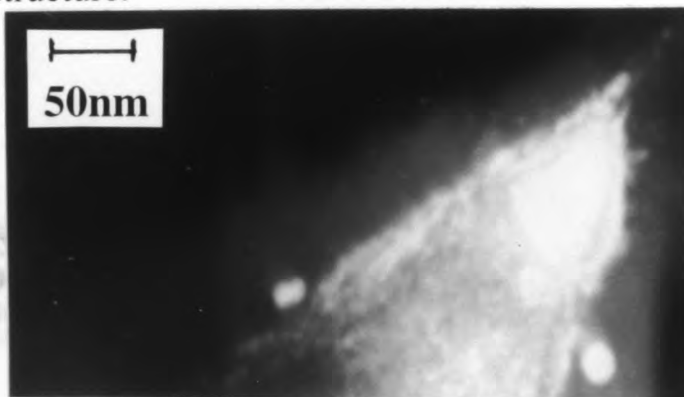
a) 5 second anodisation

Porous silicon layer is ~14nm thick at the tip apex and ~25nm thick on the {111} planes. For this short anodisation time, the geometry of the core still appears to be similar to the original geometry of the tip prior to anodisation.

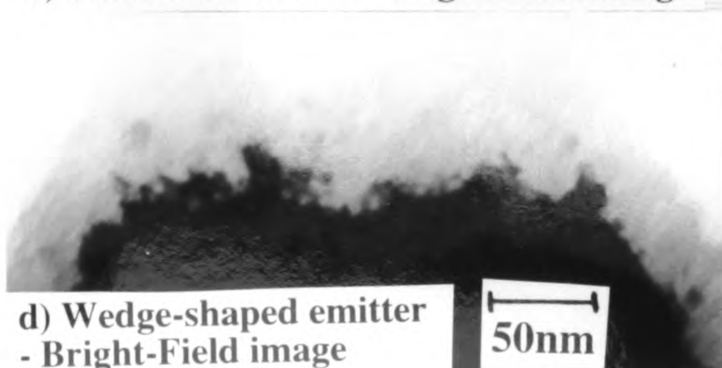
b) - g) 120 second anodisation

Porous silicon layer is ~40nm thick at the tip apex. The thickness of porous silicon on the {111} planes is ~1μm (although this is not shown here). The resulting core geometry is a bullet-shaped core having almost vertical sides and which is ~1.5μm long. The overall core geometry is totally different to the original tip structure.

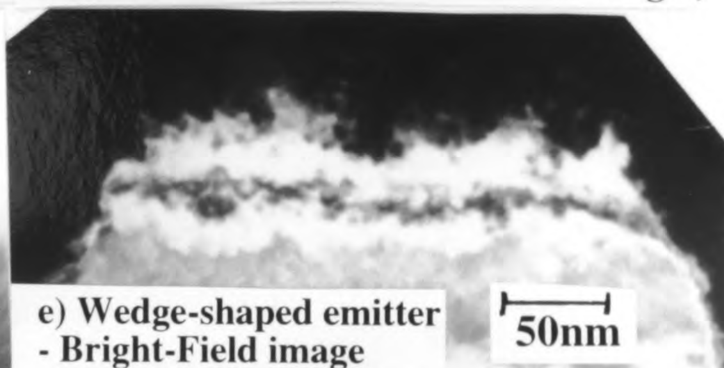
b) Point-like emitter - Bright-Field image



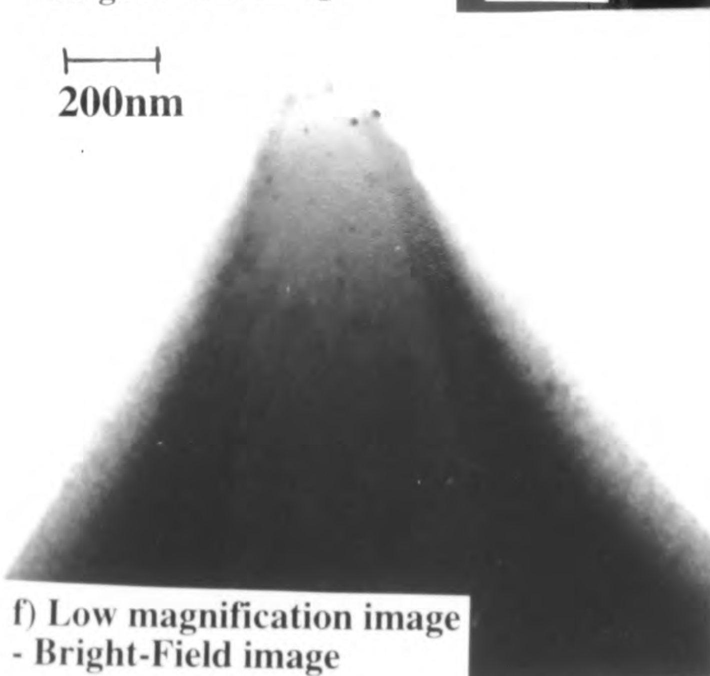
c) Point-like emitter - Dark-Field image



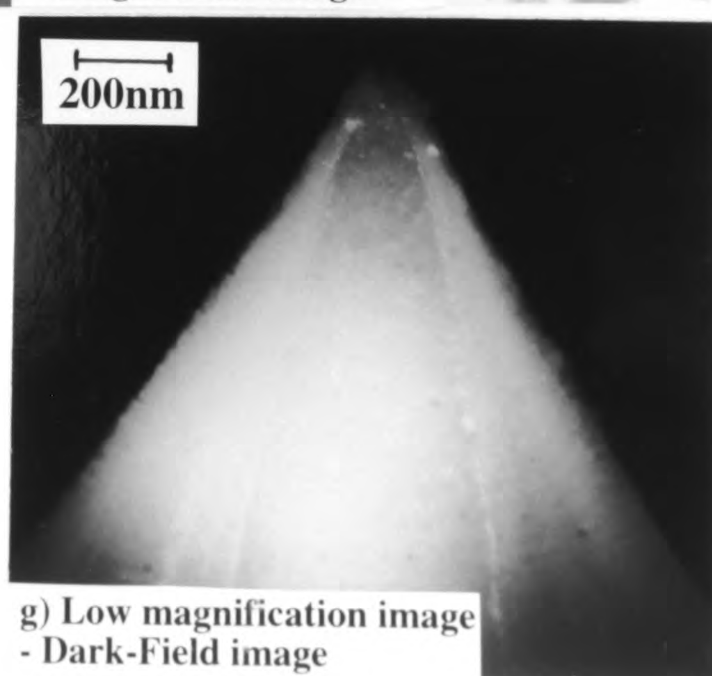
d) Wedge-shaped emitter - Bright-Field image



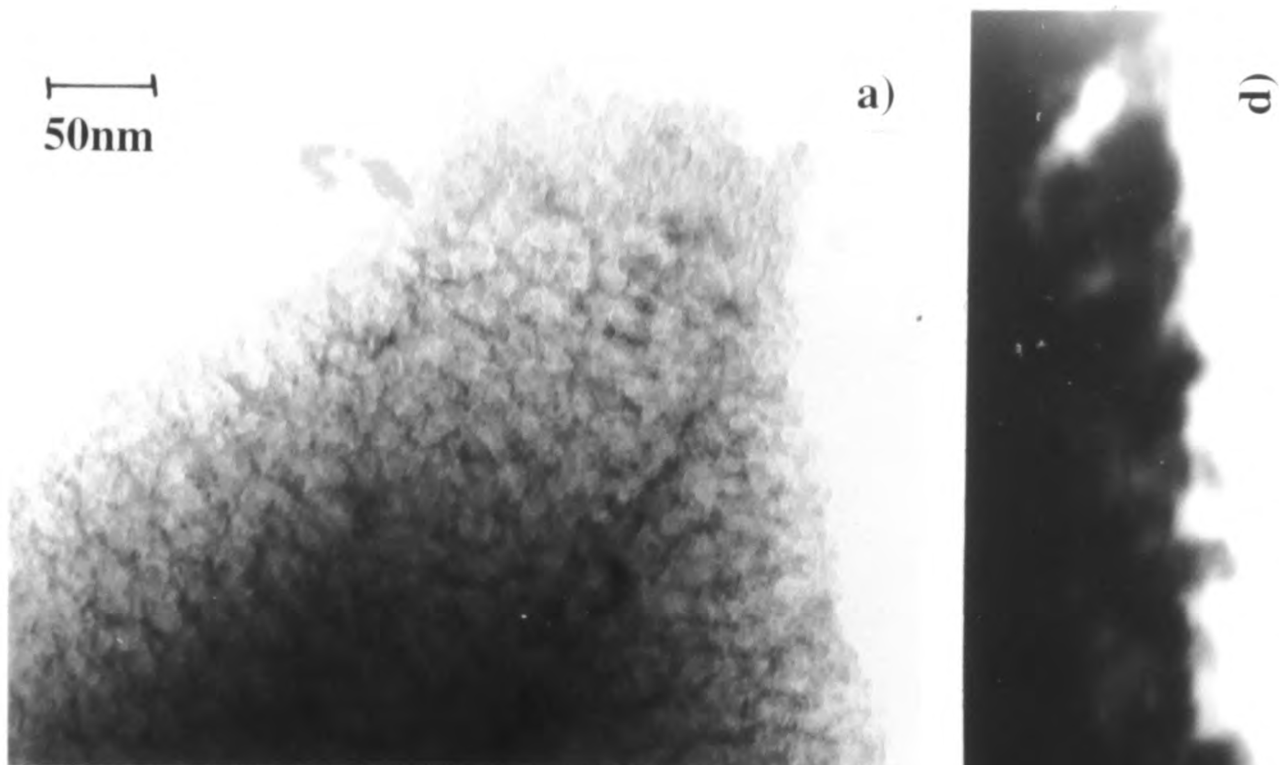
e) Wedge-shaped emitter - Bright-Field image



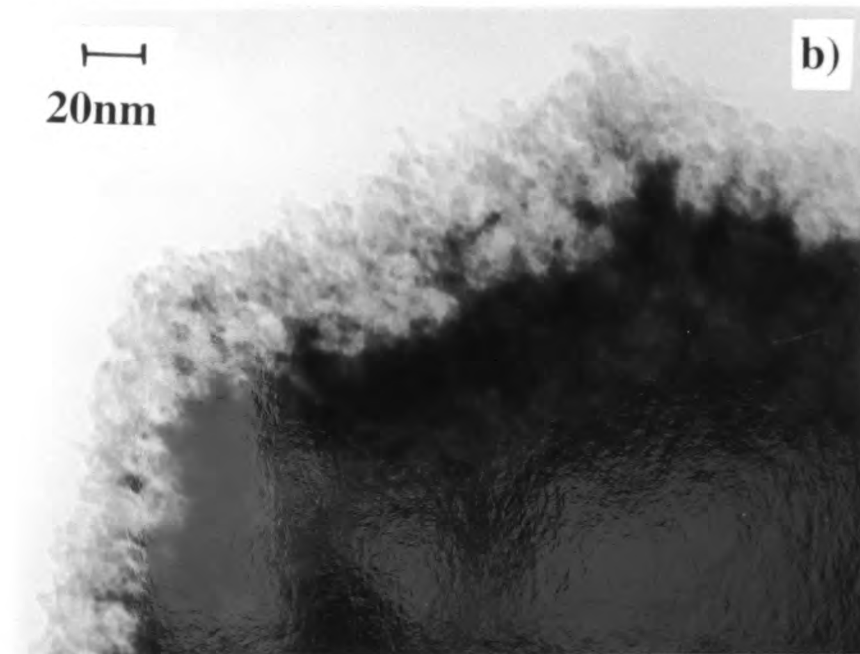
f) Low magnification image - Bright-Field image



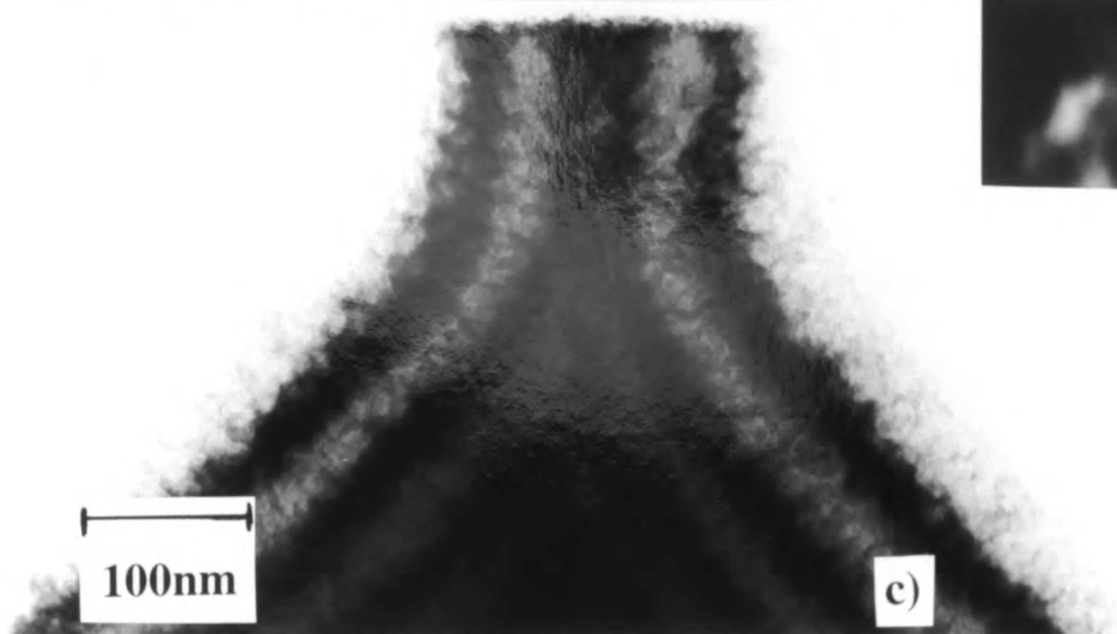
g) Low magnification image - Dark-Field image



a) Anodised emitter showing that even a short 0.25 seconds anodisation resulted in the formation of a large density of fibrils at the tip apex



b) Bright-Field image of emitter showing thickness of porous silicon layer at emitter tip is ~40nm thick



c) Bright-Field image of different emitter showing that thickness of porous layer down emitter sides is also ~40nm thick

d) Dark-Field image of side of anodised emitter showing rough nature of porous silicon / bulk silicon interface

Figure 6.20 - P^+-Type emitters anodised for only 0.25 seconds

Anodisation Time / Seconds	5	10	30	120	300
Thickness at tip	7nm(1) 14nm(2)	20nm(1)	10-25nm(1) 25-40nm(2)	40nm(1) 50nm(2)	40nm(1) 50nm(2)
Thickness on {111} planes	15nm(1) 24nm(2)	50nm(1)	200nm(1) 250nm(2)	1μm(1)	~3μm(1)

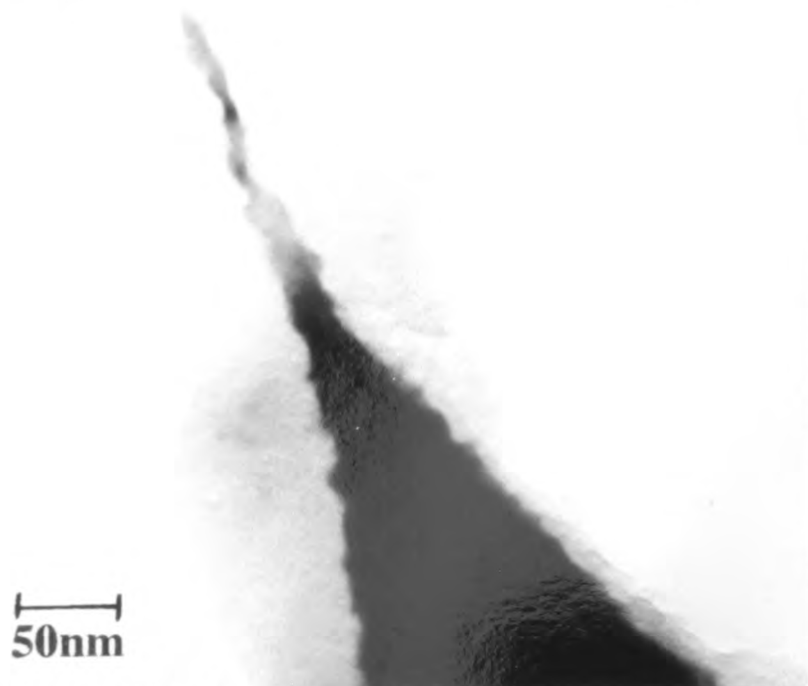
(1) Sharp-tip emitter; (2) Flat-topped emitter

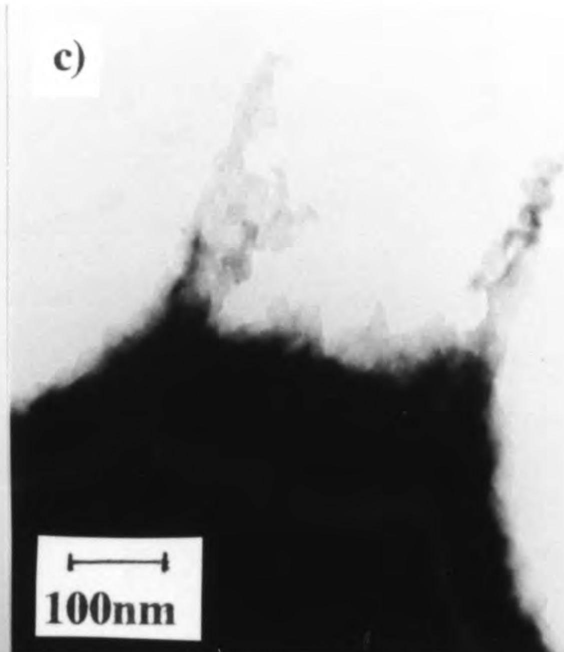
The accuracy with which the PS layer could be measured was ±5nm.

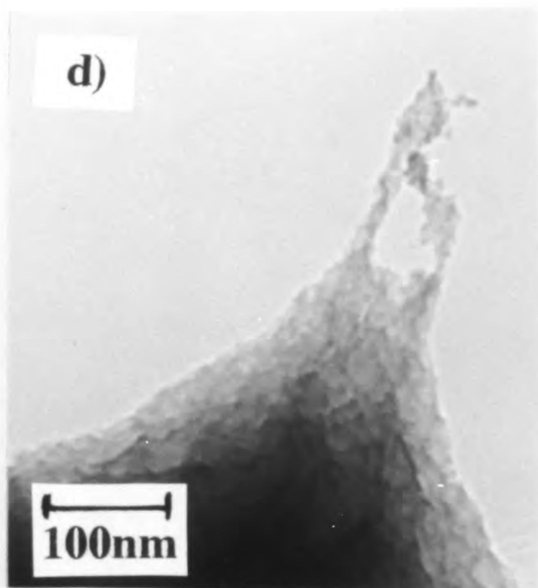
Table 6.8: Effect of Anodisation Time on P-Type PS Layer Thickness at Apexof Field Emitter Tips

Anodisation Time / Secs	0.25	10	30
Thickness of PS at tip	40nm	400nm	Too thick to observe
Thickness on {111} planes	30nm	300nm	Too thick to observe

Table 6.9: Effect of Anodisation Time on P^+-Type PS Layer Thickness atApex of Field Emitter Tips







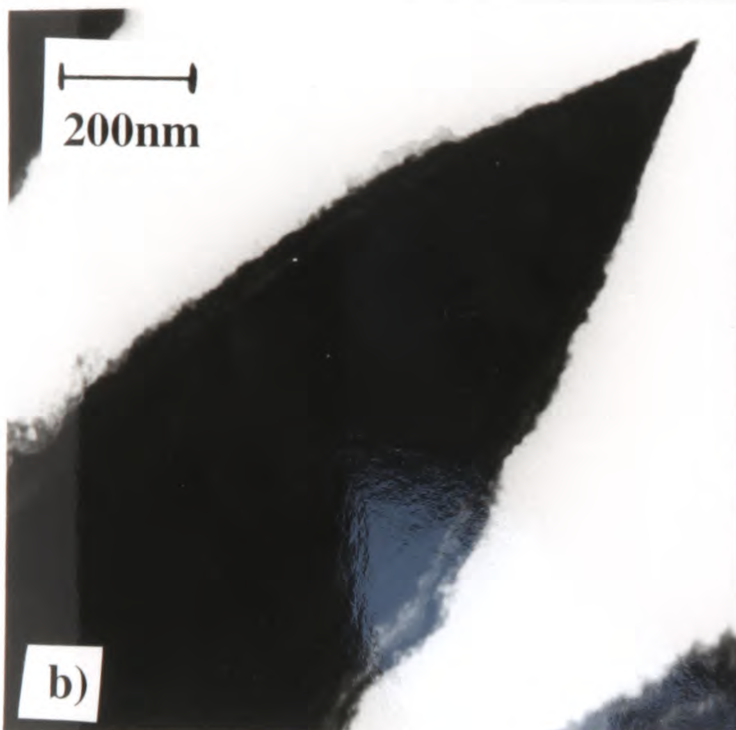
a) Point-like tip apex which has been dipped into buffered HF only one day after anodisation
Note that some of the porous silicon layer has been removed by dipping into buffered HF, but that some of the layer remains adhered to the silicon core.

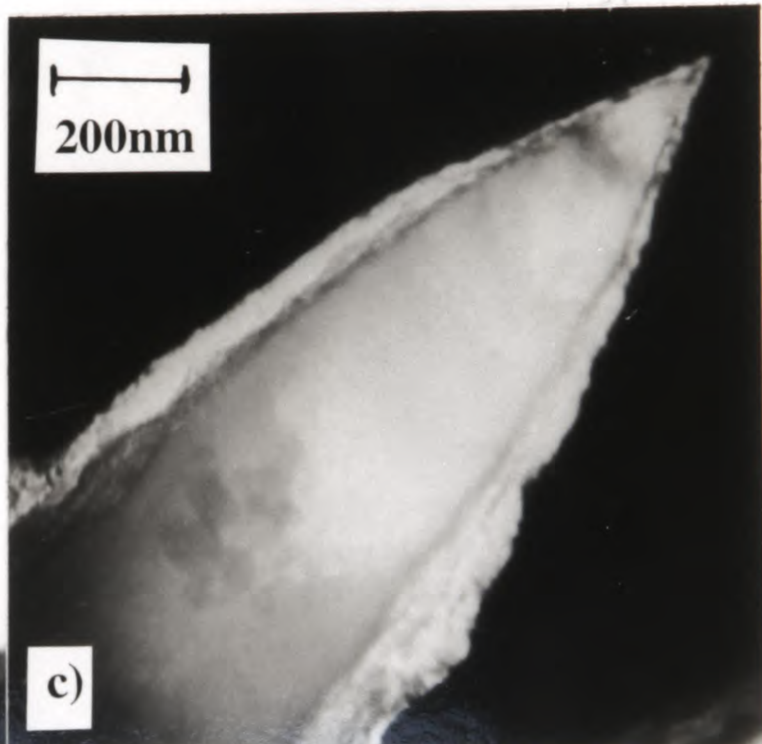
b) Point-like tip apex which has been dipped into buffered HF following oxidation at 900°C for 30 seconds
Note that all the porous silicon layer has been removed from the silicon core following this treatment. Note the high aspect ratio silicon core left behind. This confirms that for sharp emitters, the core appears to have been continuous along the vertical section. Note that a similar effect was observed when samples were left in air for several months, prior to dipping into HF - all porous silicon was removed.

c) and d) Wedge-like tip apexes which were left in air for several months before being dipped into HF
Note that the silicon core left behind after removal of the porous silicon layer, was quite different to that observed for point-like tip apexes. In these cases, a double-peaked tip was formed - two vertical silicon rods stand in the position where the sides of the silicon core used to be. In Section 6.6.2d, it was suggested that the thicker silicon cores of wedge-shaped and flat-topped emitters may have cracked under the stress in the oxidised PS layer (oxidation due to ageing). During the HF dip, the mis-oriented silicon grains may have broken apart and floated away. This would have resulted in removal of the core centre, leaving behind just two silicon rods, as has been observed here.

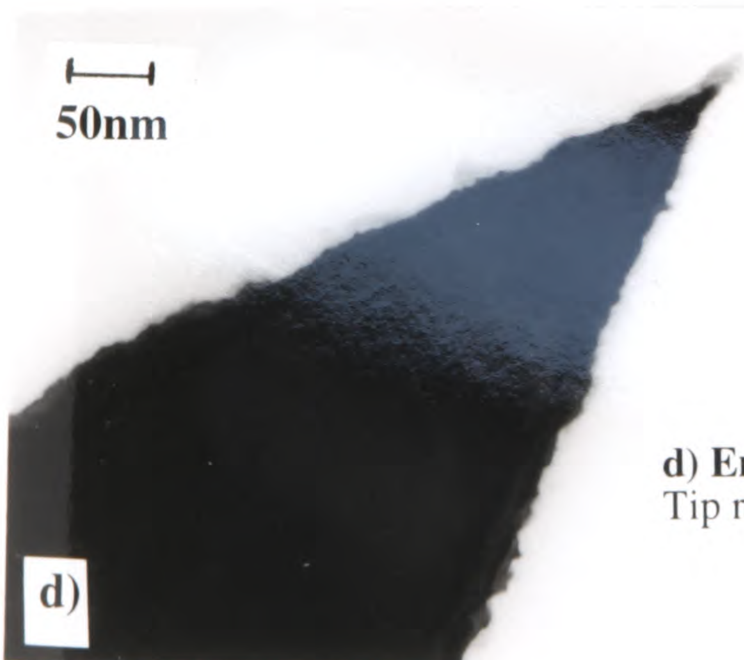
Figure 6.22 - TEM image of p-type porous silicon tip (originally anodised for 30 seconds at 30mAcm-2) following various treatments

a) Neighbouring emitters showing unusual bullet-shaped core geometry
Note that core structure is completely different to the original pyramid-like structure. These cores are almost vertical –sided. The structure which can be seen here is almost 2μm high and only ~0.8μm thick. The original tip structure was ~2.5μm tall and was 5μm by 5μm at the base. The dimensions of the residual core show that a considerable amount of the original tip was anodised during the 120 second anodisation.





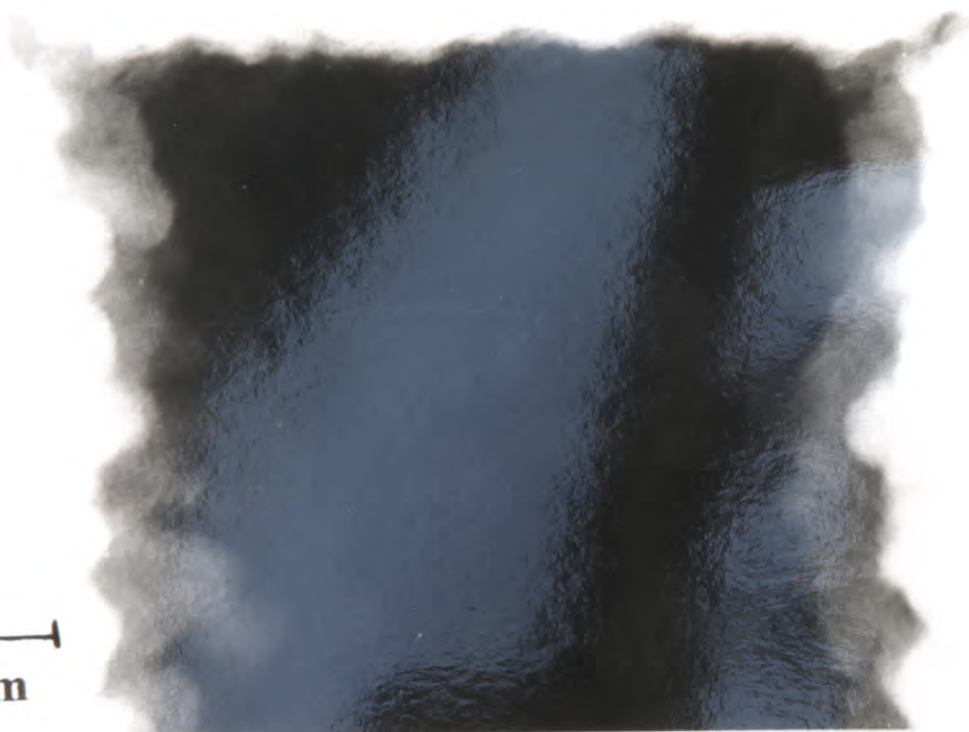
b) and c) Bright and Dark-Field images of one emitter



d) Emiiter tip at higher magnification
Tip radius is ~3nm

Figure 6.23 - P-type emitters anodised for 120 seconds (current density $30mAcm^{-2}$) following removal of the porous silicon layer by HF dipping (specimen was ~6 months old prior to HF dipping)

a)



a) Exposed rough interface of flat-topped emitter

Note the very sharp corners - tip radii are ~1.5nm

b) High magnification image of exposed interface

b)

Figure 6.24 - Anodised p-type porous silicon interfaces (originally anodised for 30 seconds with an anodisation current of 30mAcm^{-2}) which were dipped into buffered HF following oxidation at 900°C for 30 seconds
Note that all porous silicon has been removed from these tips, exposing a rough surface which was the original porous silicon / bulk silicon interface.

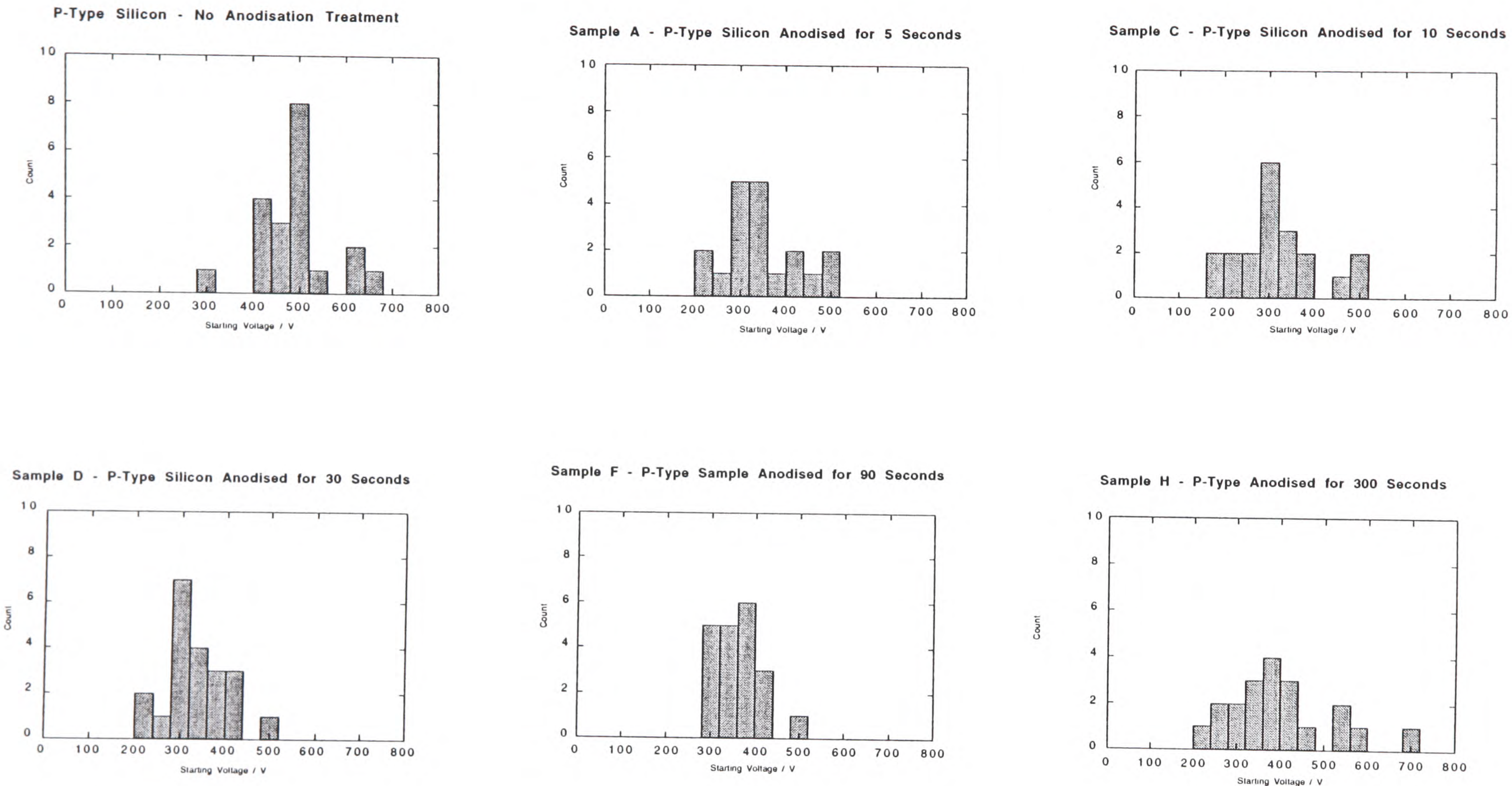


Figure 7.1a - Comparison of Distributions of Starting Voltage for Different Anodisation Times
≈20 tips examined per sample

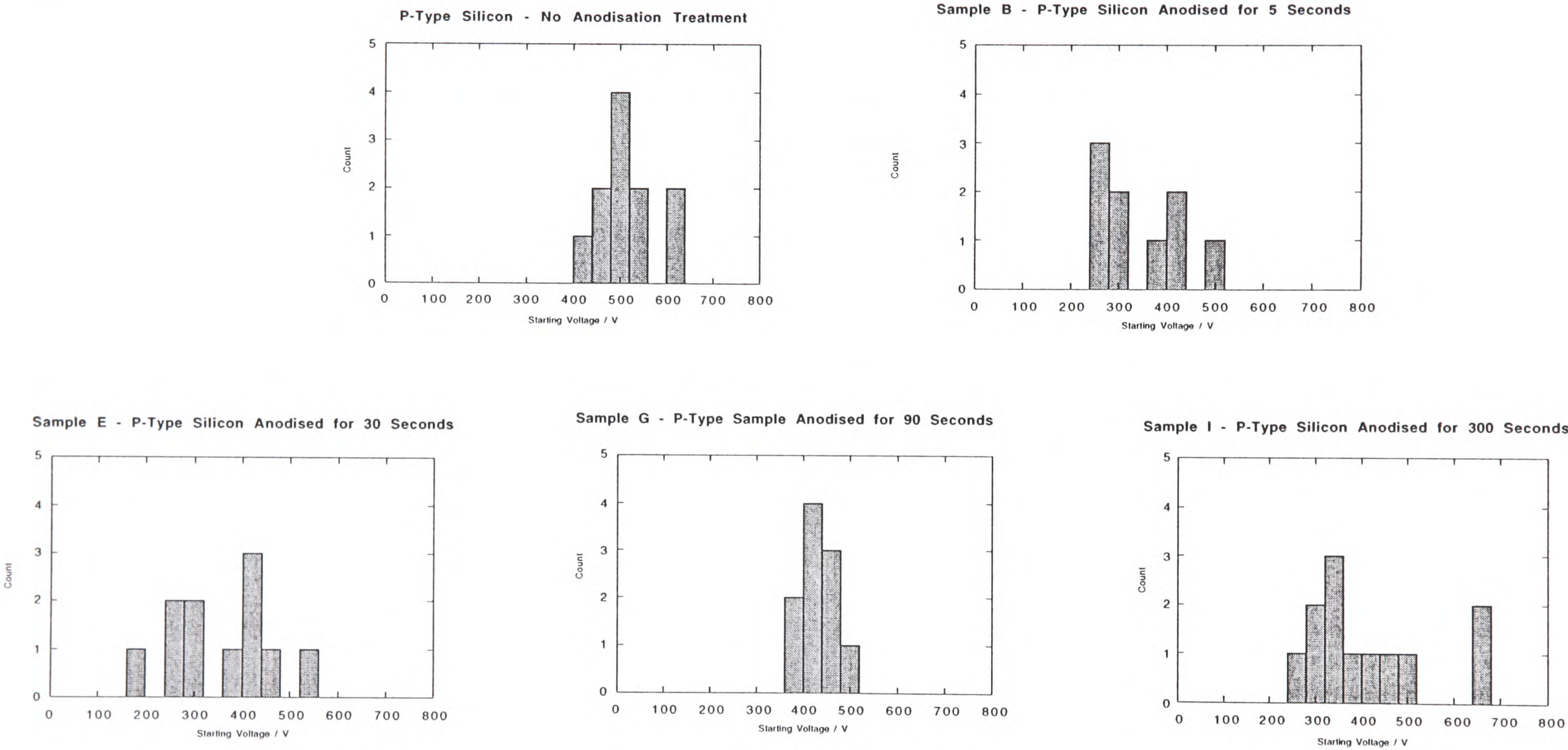
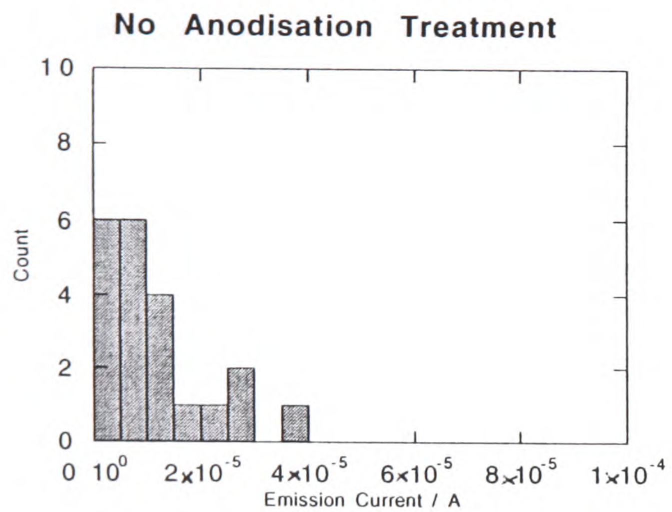
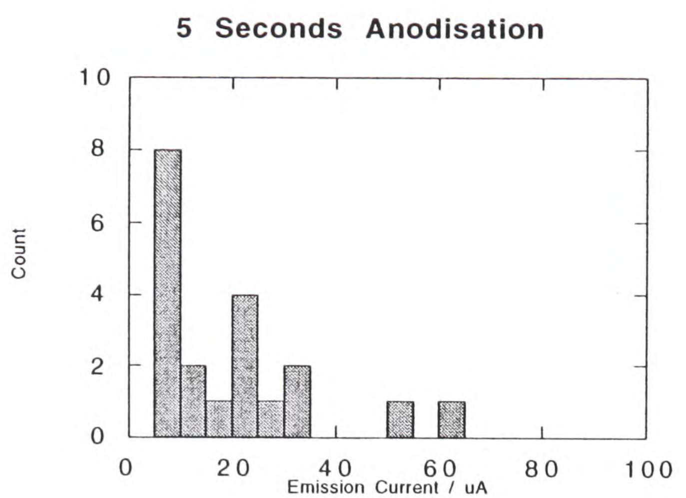
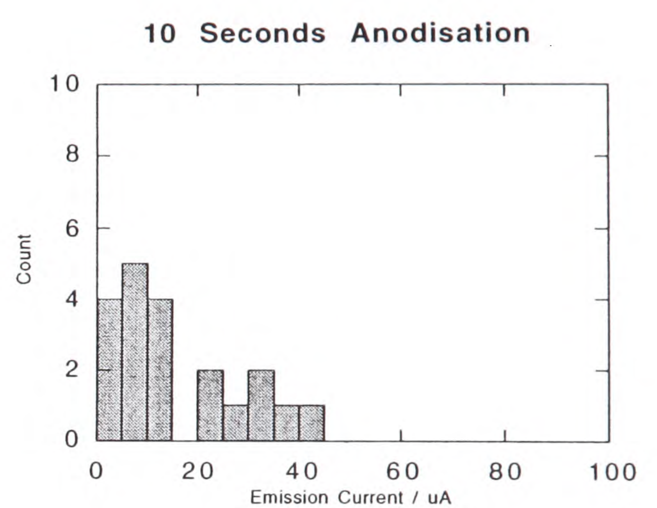
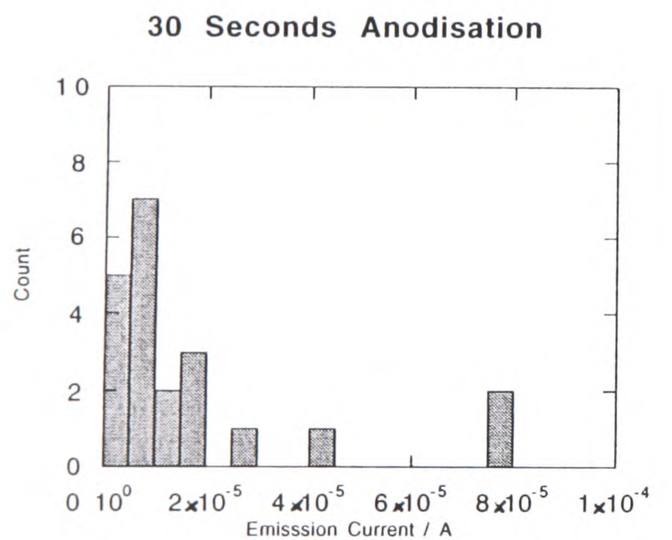


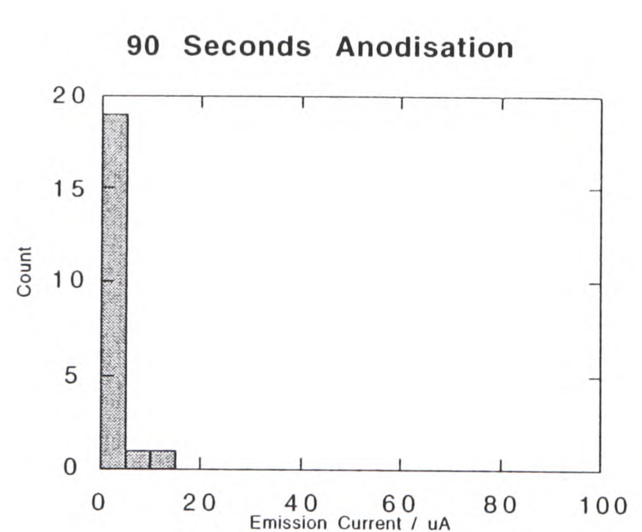
Figure 7.1b - Comparison of Distributions of Starting Voltage for Different Anodisation Times
≈10 tips examined per sample











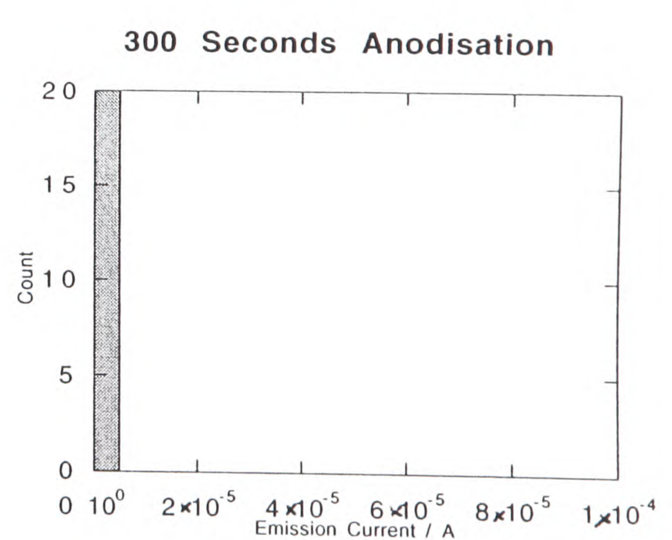
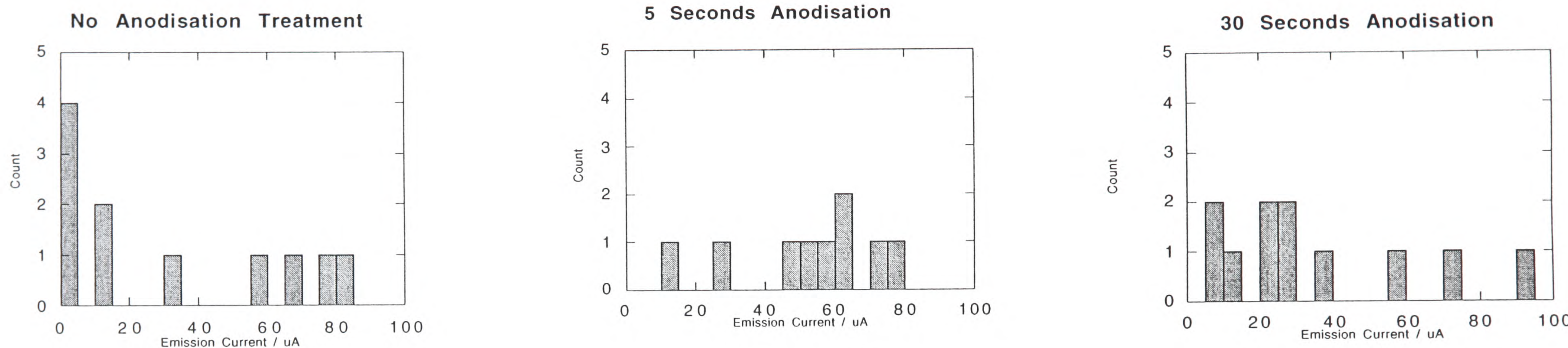


Figure 7.4a **Distributions of Maximum Current for Each Anodisation Time** $\approx$20 tips per sample



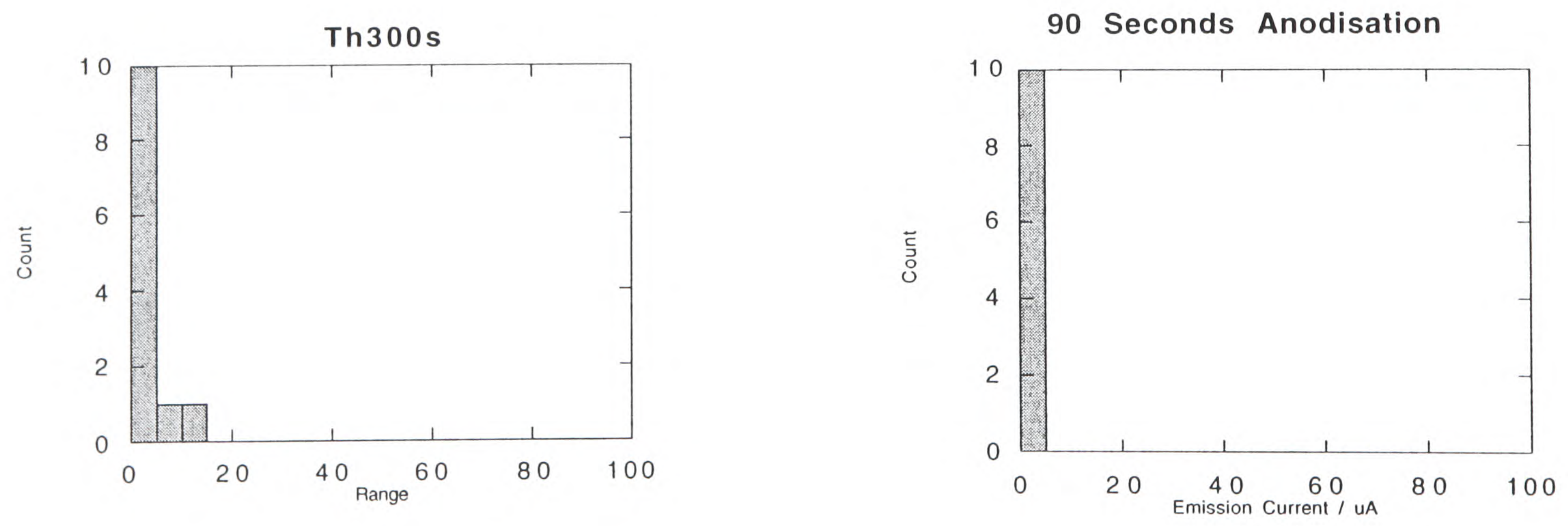
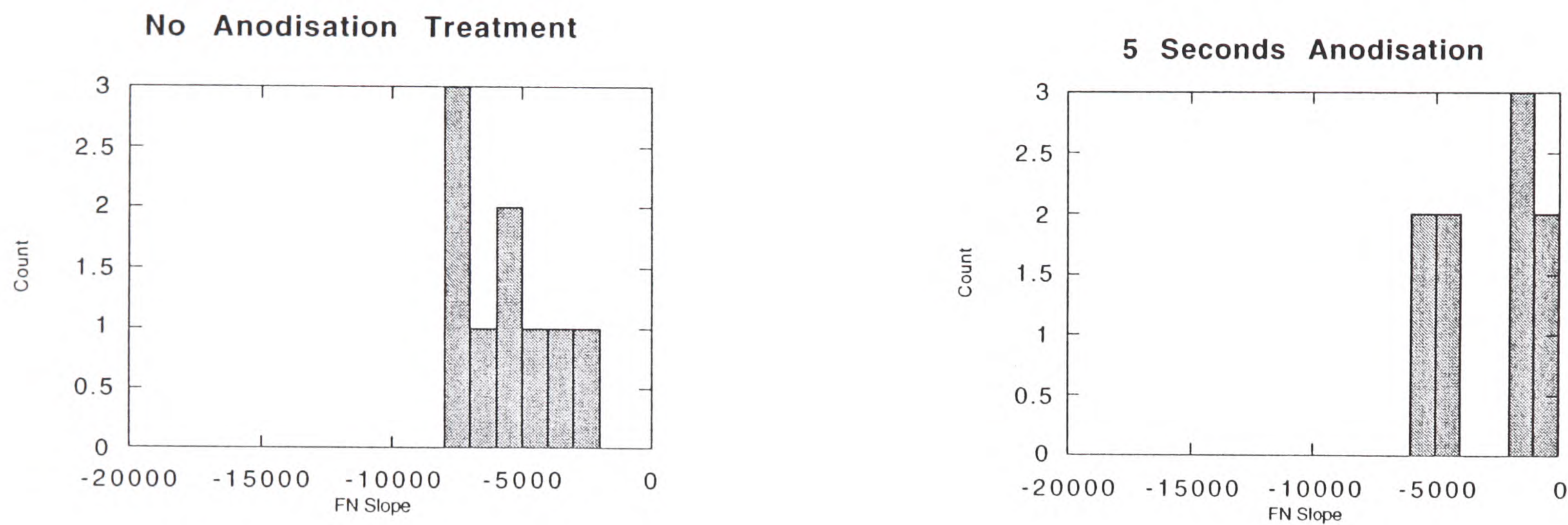


Figure 7.4b **Distributions of Maximum Current for Each Anodisation Time** ≈10 tips per sample



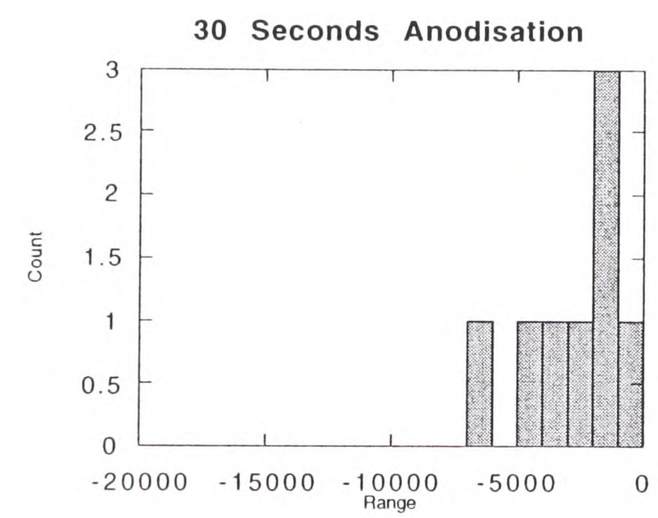
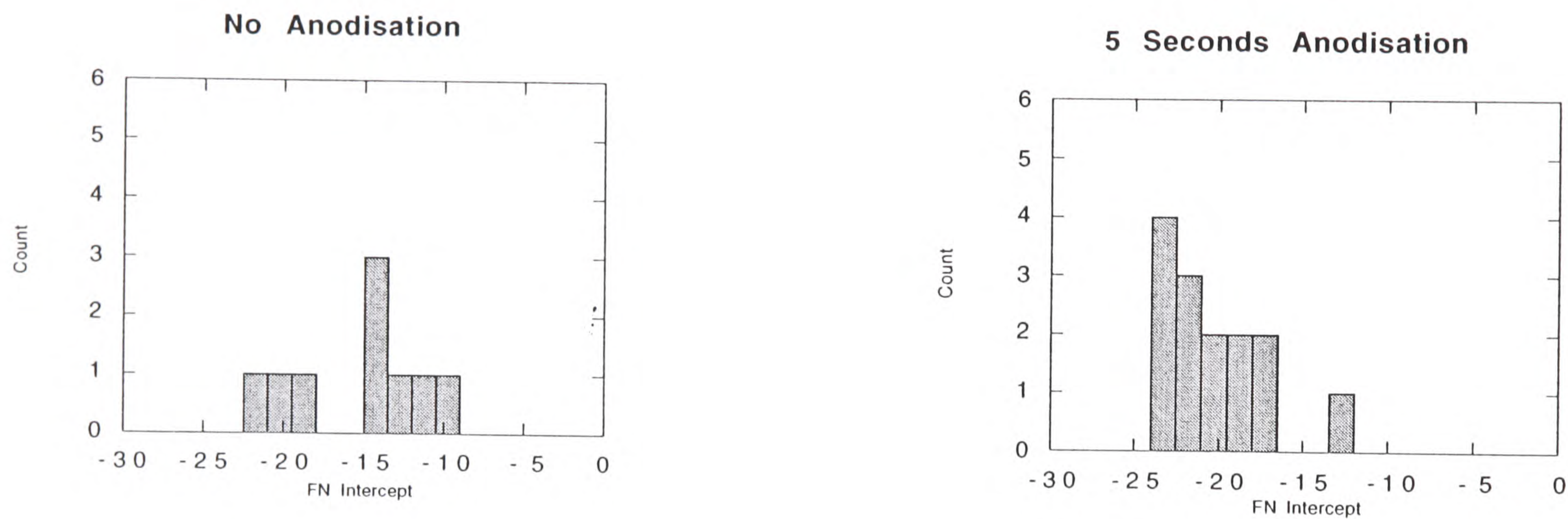


Figure 7.6b Distributions of Fowler-Nordheim Slope for different Anodisation Times
≈10 tips per sample



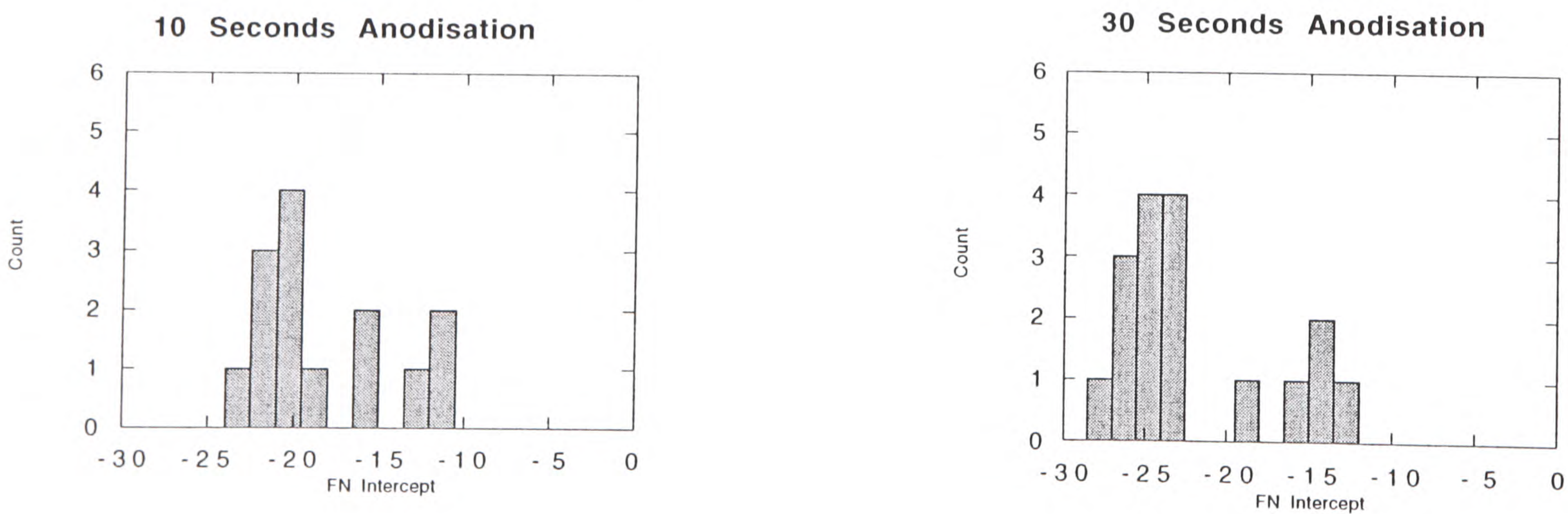
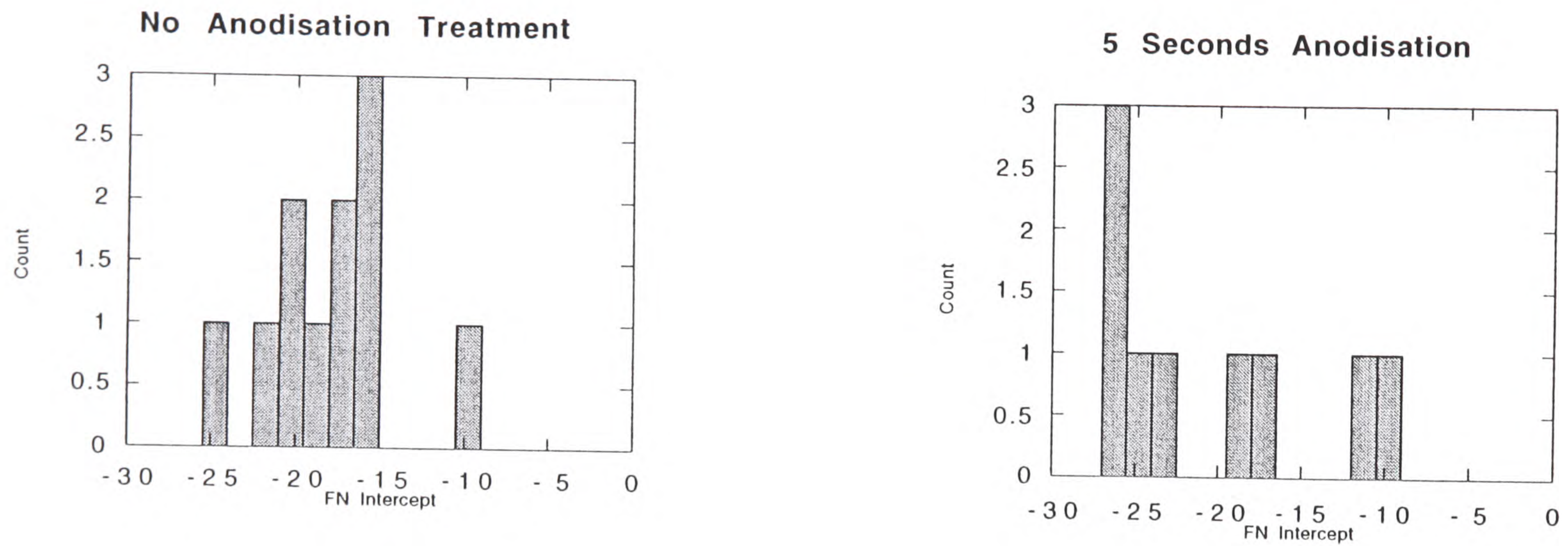


Figure 7.6c **Distributions of Fowler-Nordheim Intercept for different Anodisation Times**
≈20 tips per sample



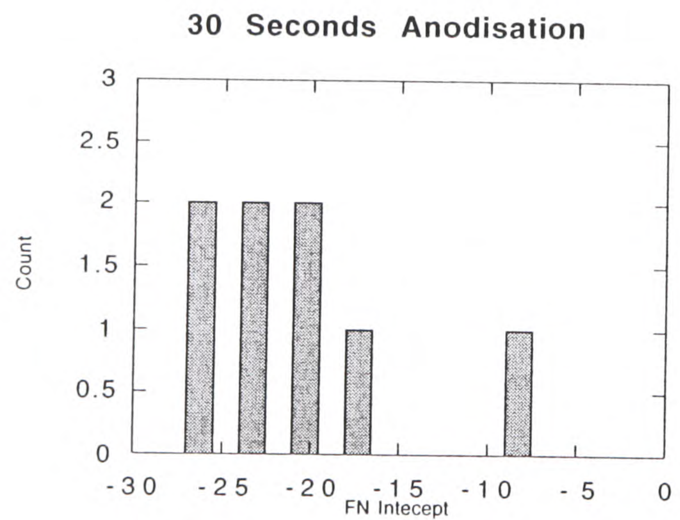
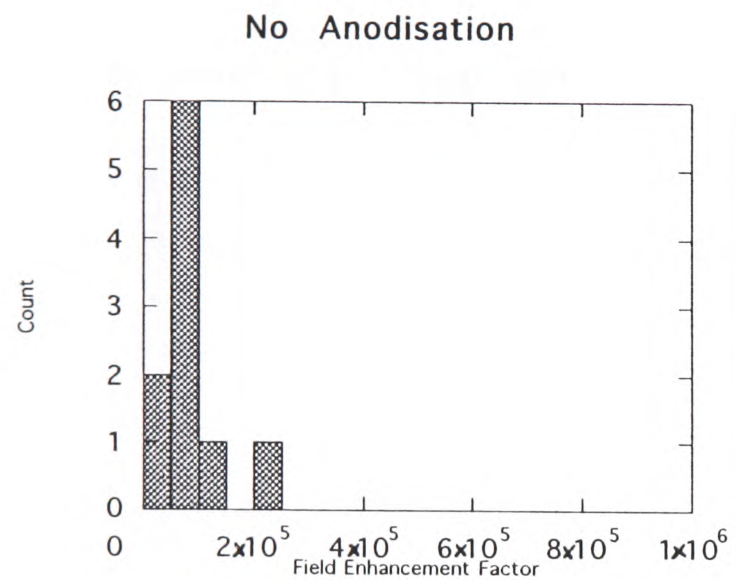
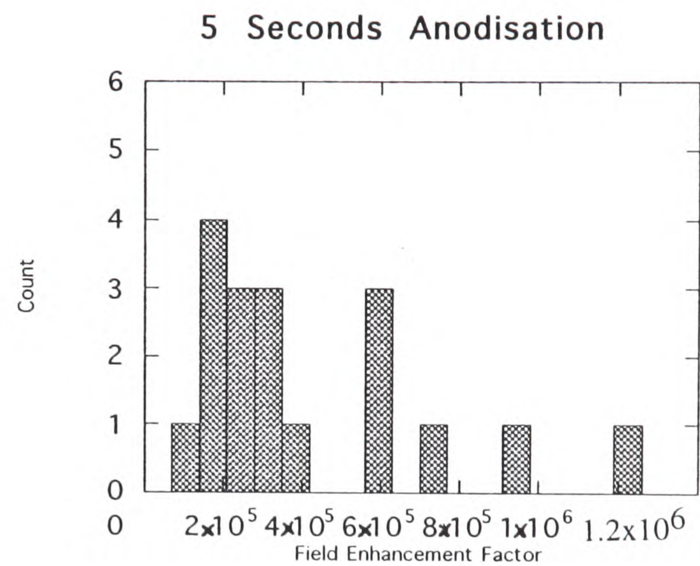
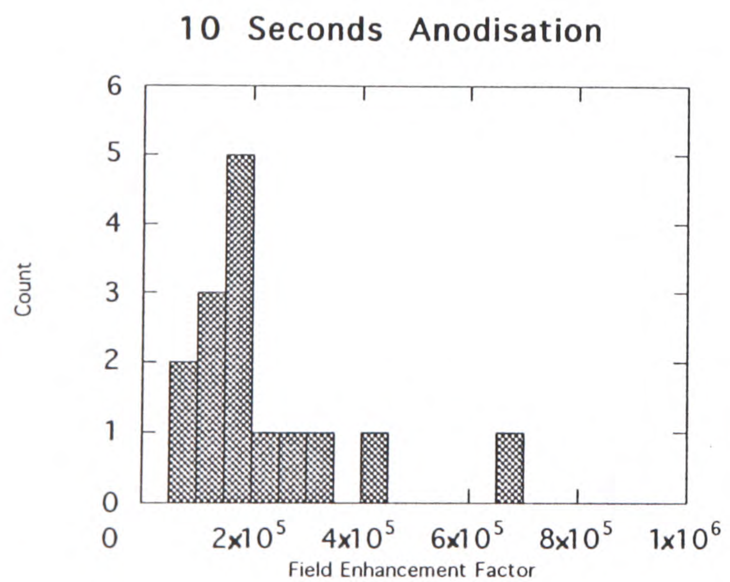


Figure 7.6d Distributions of Fowler-Nordheim Intercept for different Anodisation Times
- 10 tips per sample







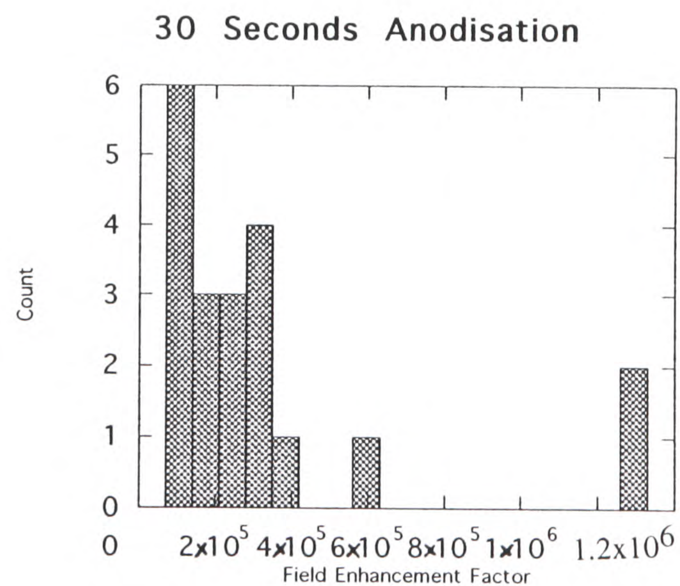
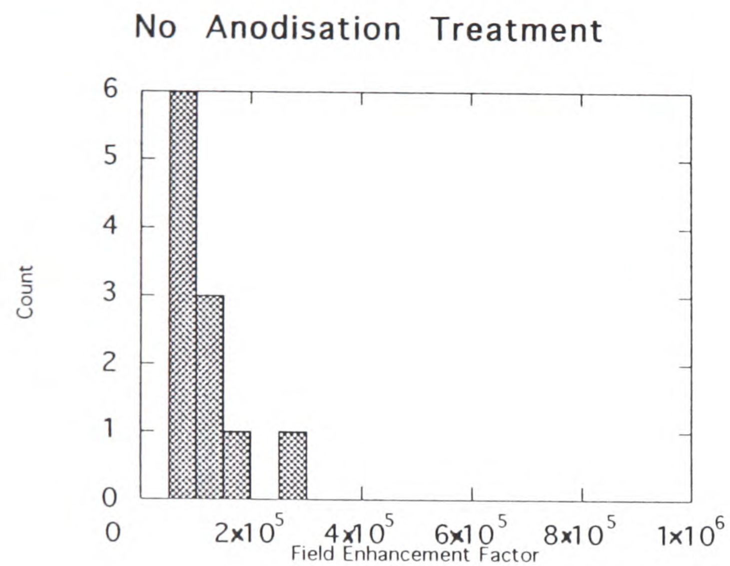
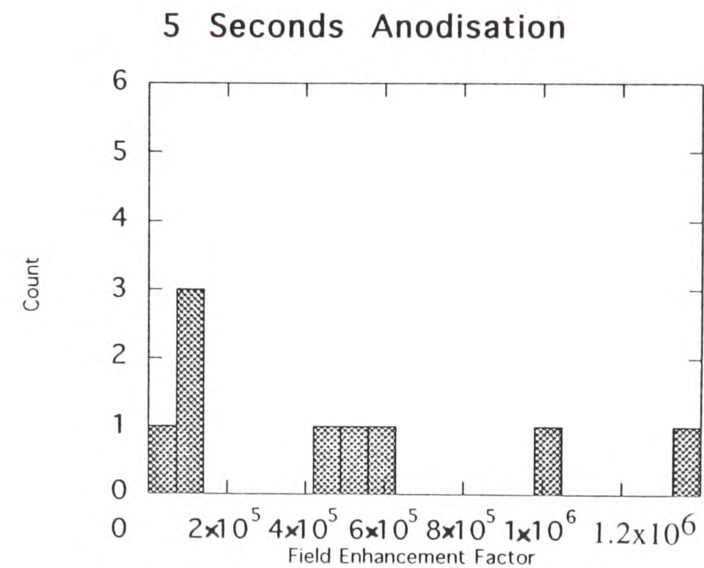


Figure 7.8a - Distribution of Field Enhancement Factor for different Anodisation Times
≈20 tips per sample





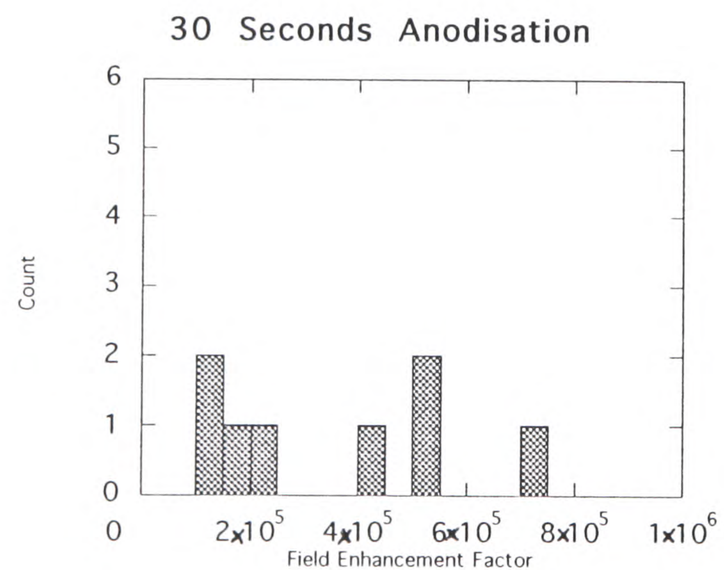
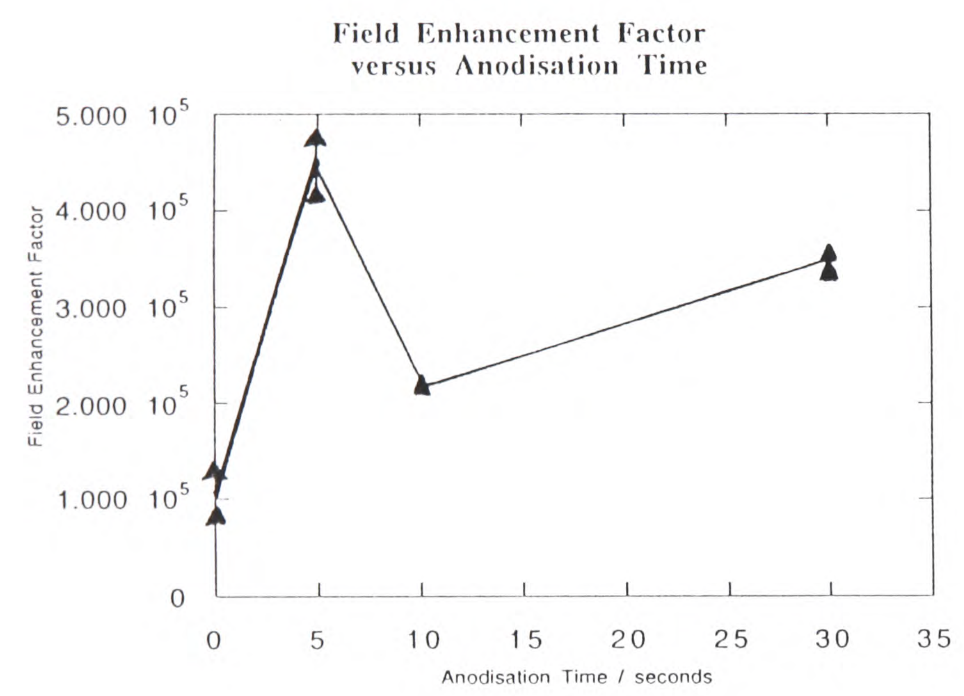


Figure 7.8b - Distribution of Field Enhancement Factor for different Anodisation Times
≈10 tips per sample



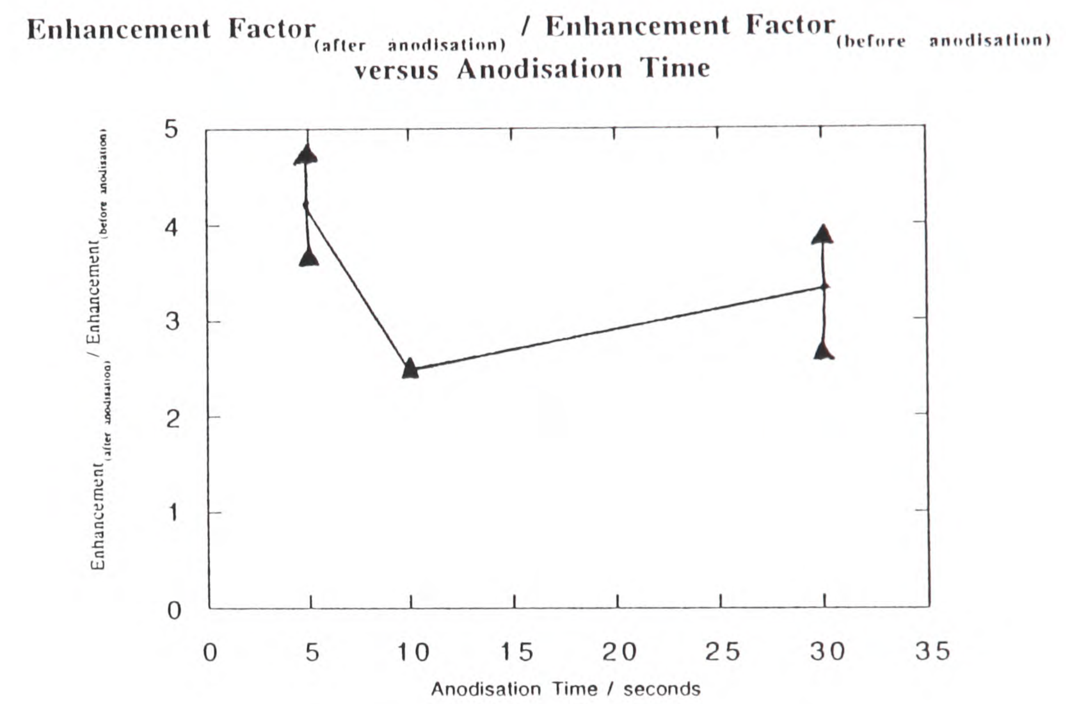
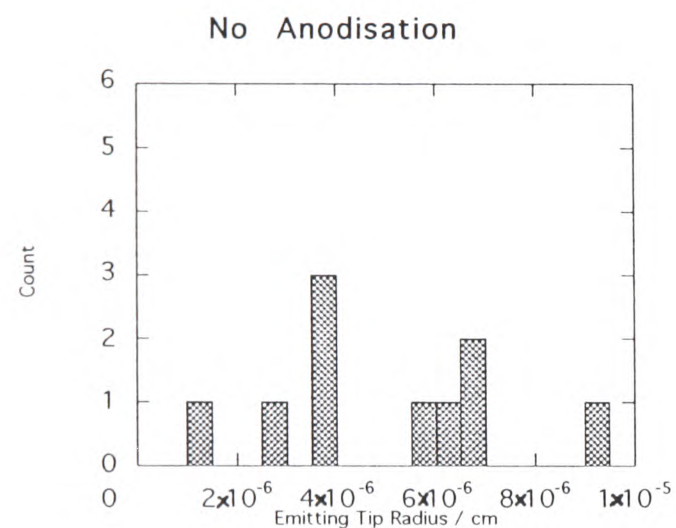
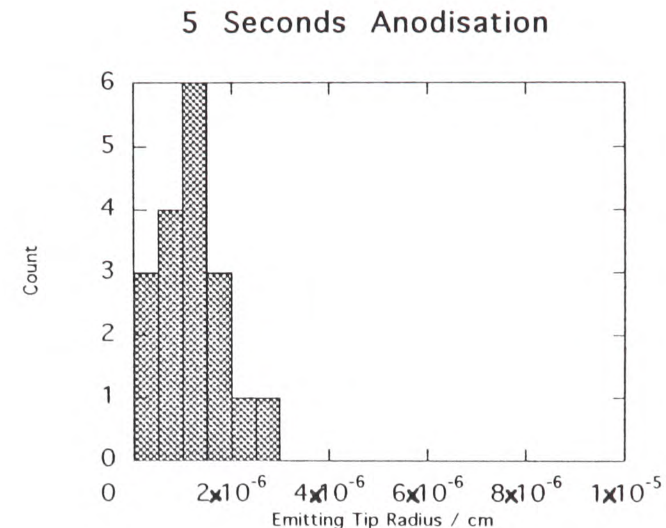
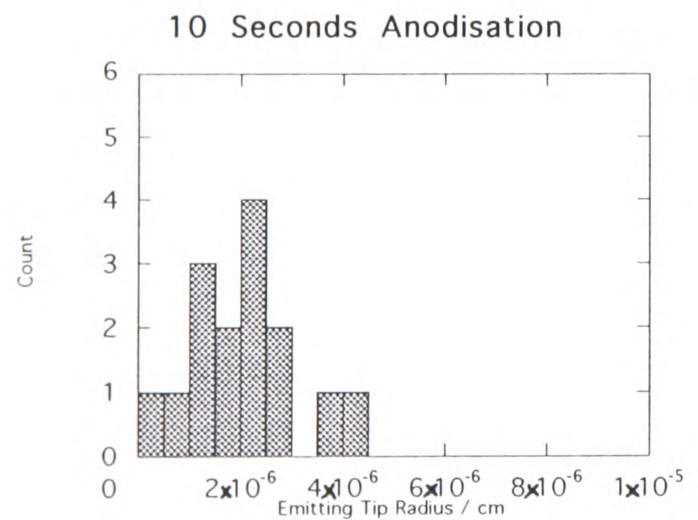


Figure 7.9 - Plot of Field Enhancement Factor and Comparative Field Enhancement Factor versus Anodisation Time

Data from both sets of samples presented here







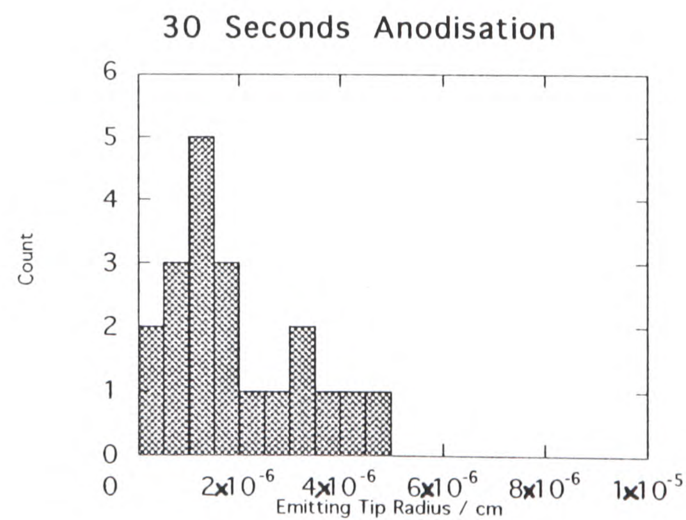
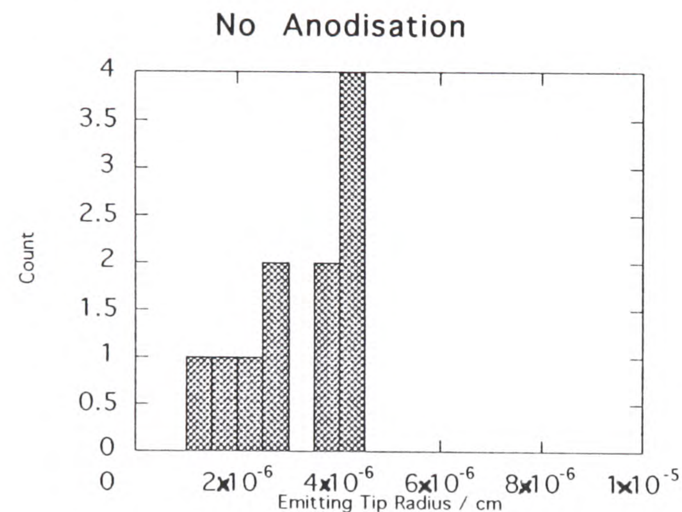
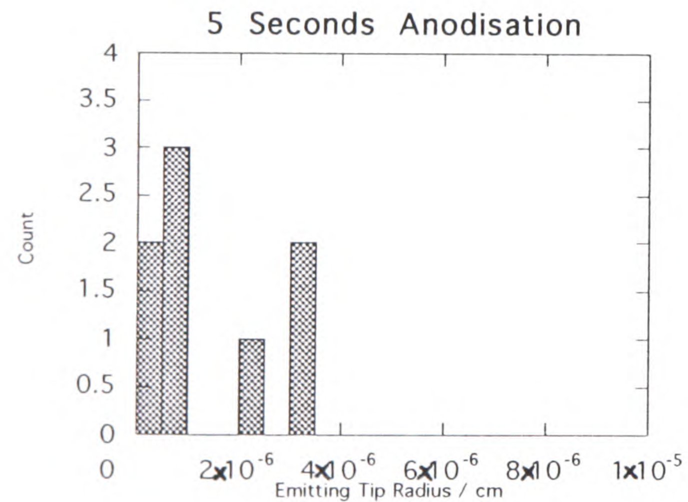


Figure 7.10c - Distribution of Value of Tip Radius (Calculated from Field Enhancement Factor) for Different Anodisation Times
≈20 tips per sample





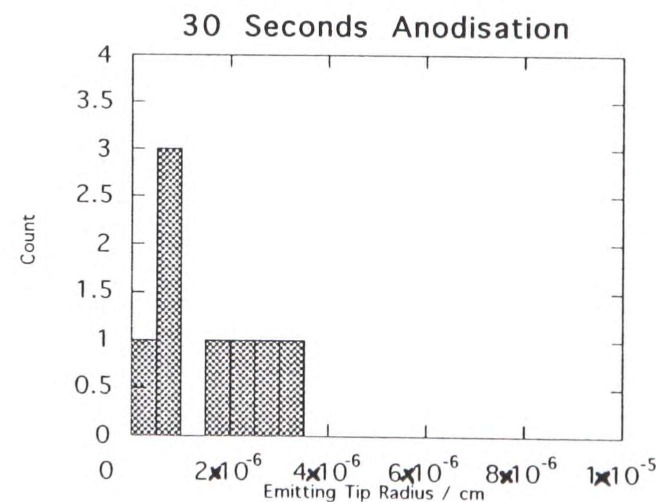
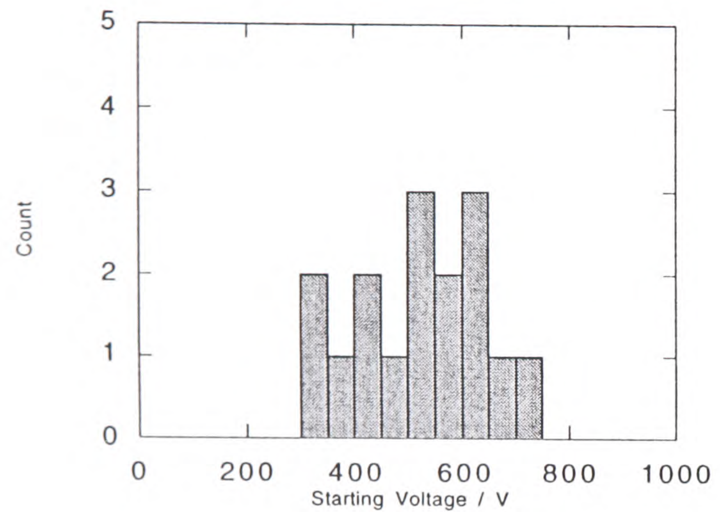
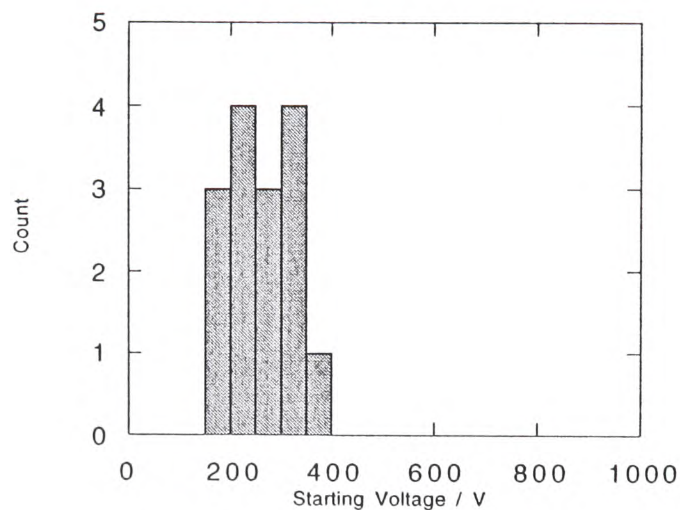
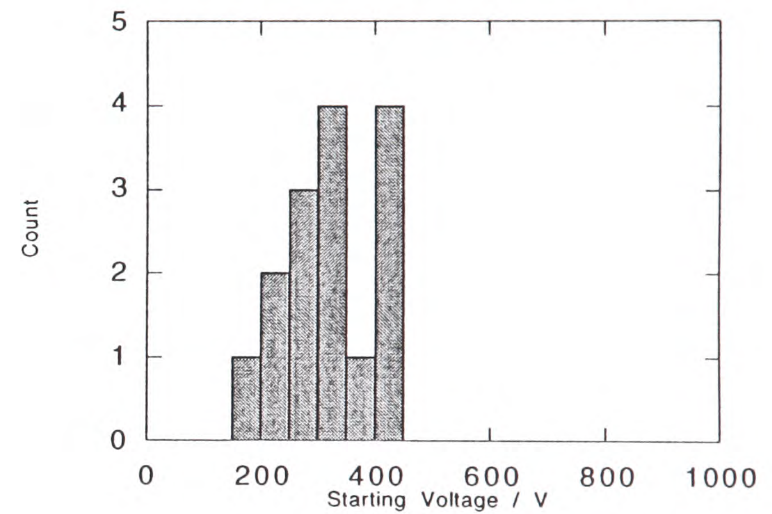
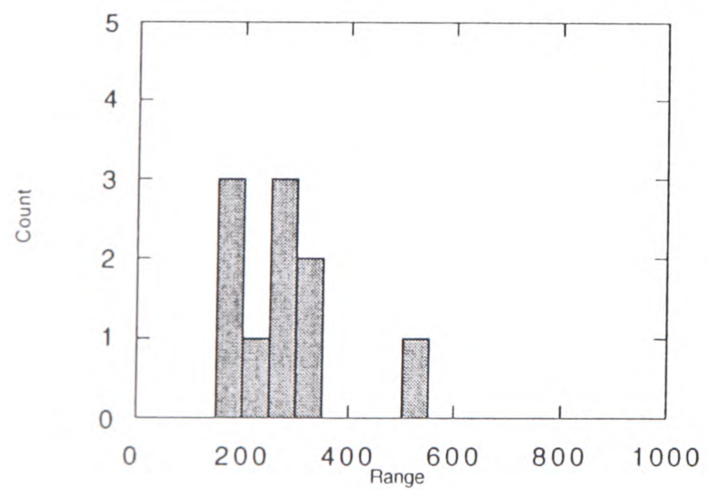


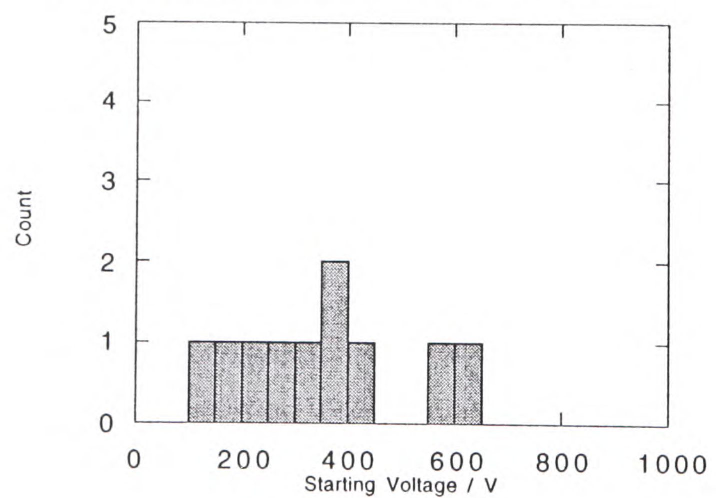
Figure 7.10d - Distribution of Value of Tip Radius (Calculated from Field Enhancement Factor) for different Anodisation Times
≈10 tips per sample

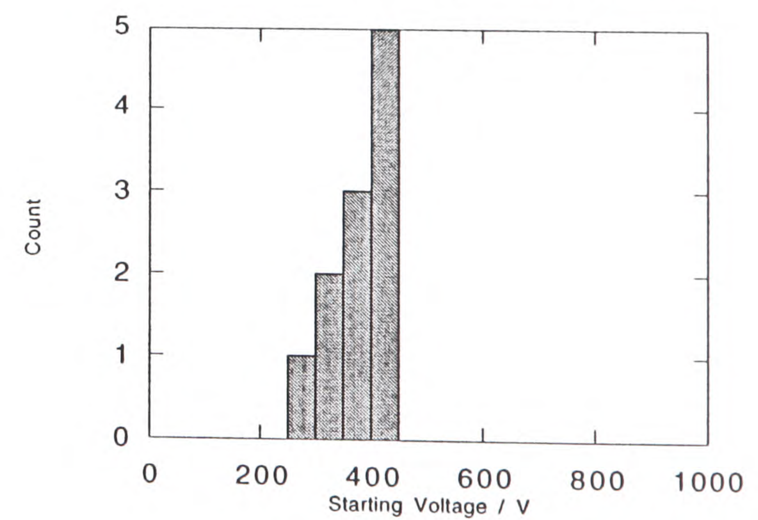

No Anodisation
Count
0
1
2
3
4
5
0
200
400
600
800
1000
Starting Voltage / V

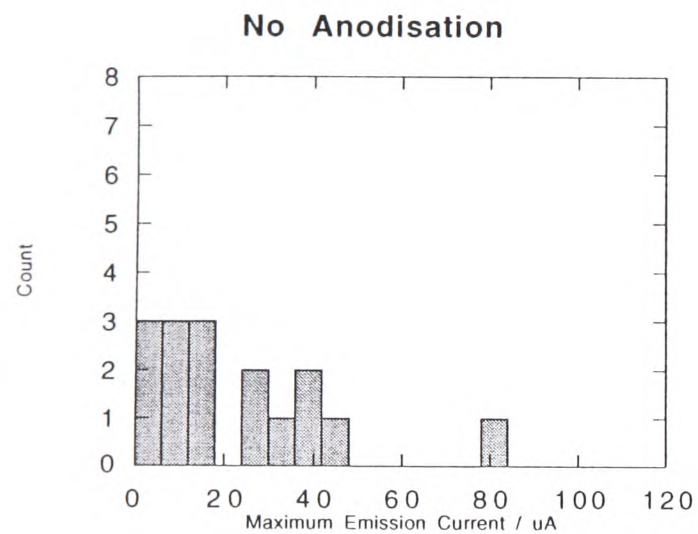

0.25 Second Anodisation - Sample J
Count
0
1
2
3
4
5
0
200
400
600
800
1000
Starting Voltage / V

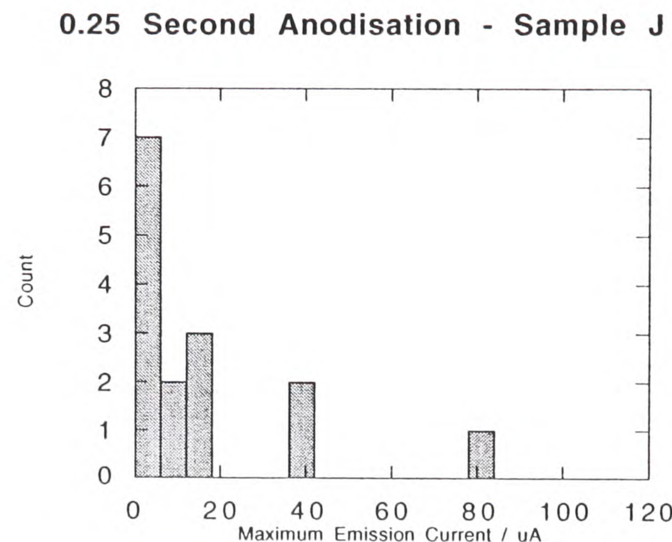

0.25 Second Anodisation - Sample K
Count
0
1
2
3
4
5
0
200
400
600
800
1000
Starting Voltage / V

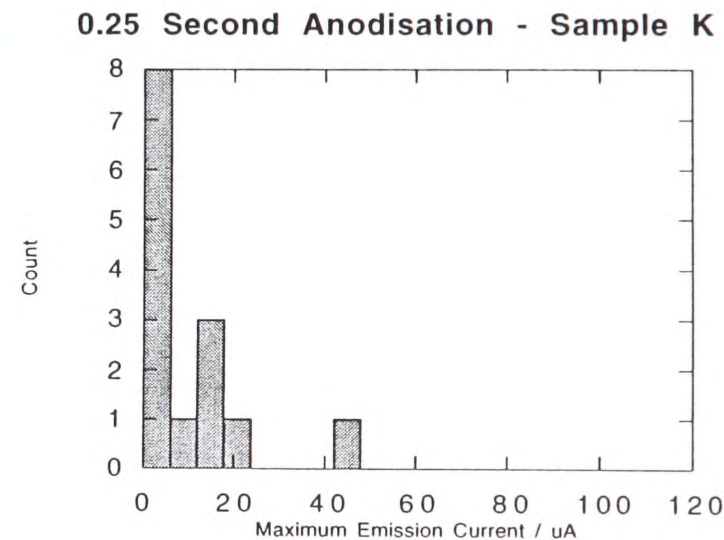

0.25 Second Anodisation - Sample L
Count
0
1
2
3
4
5
0
200
400
600
800
1000
Range

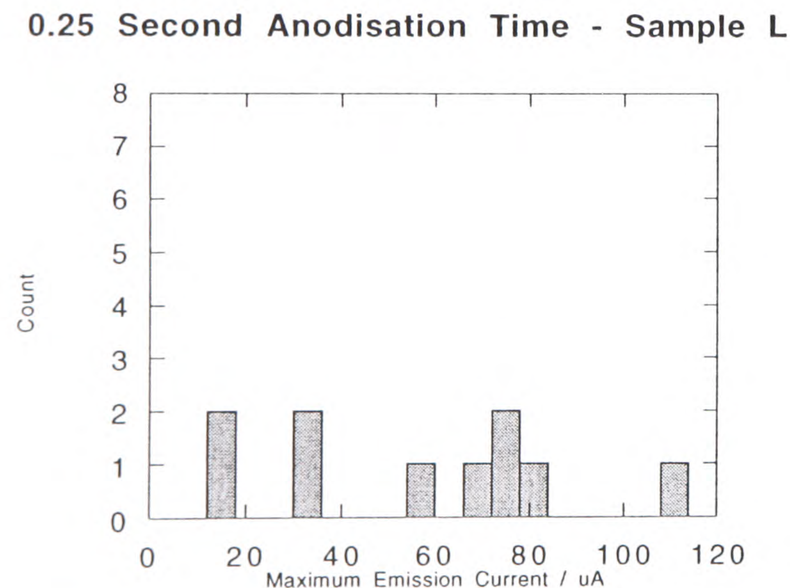

3.5 Second Anodisation - Sample M
Count
0
1
2
3
4
5
0
200
400
600
800
1000
Starting Voltage / V

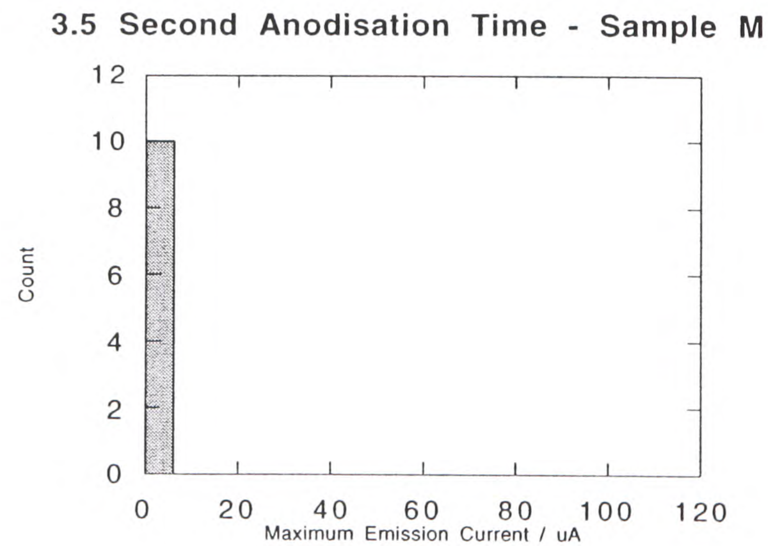

10 Second Anodisation - Sample N
Count
0
1
2
3
4
5
0
200
400
600
800
1000
Starting Voltage / V











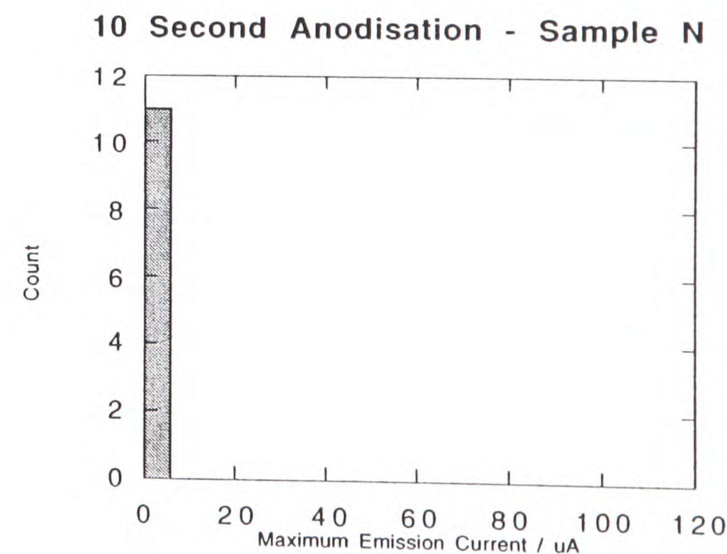
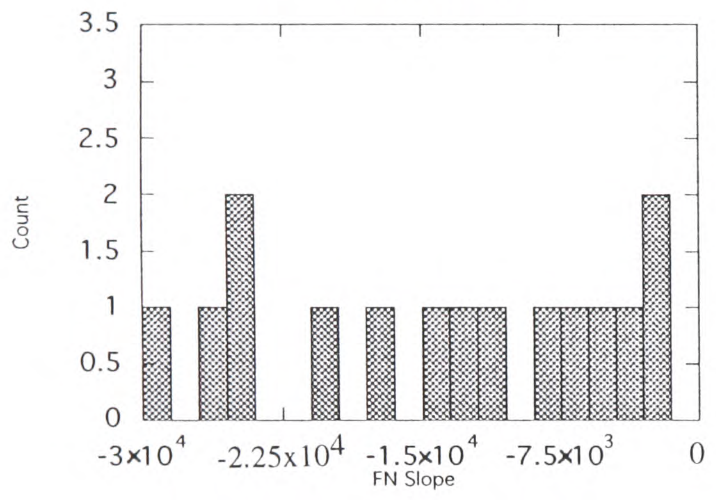
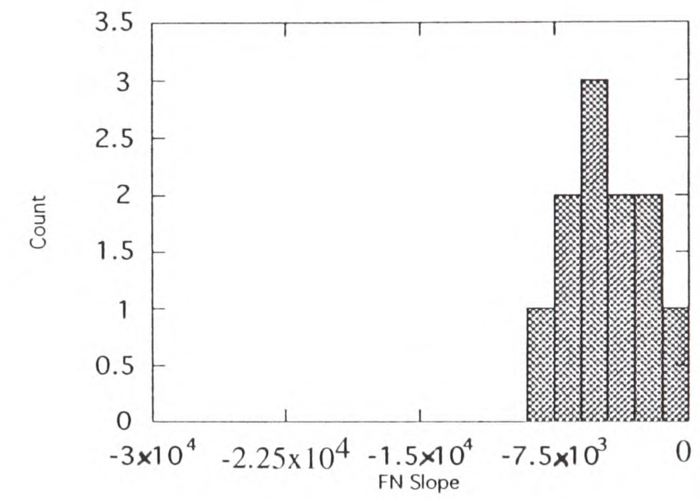
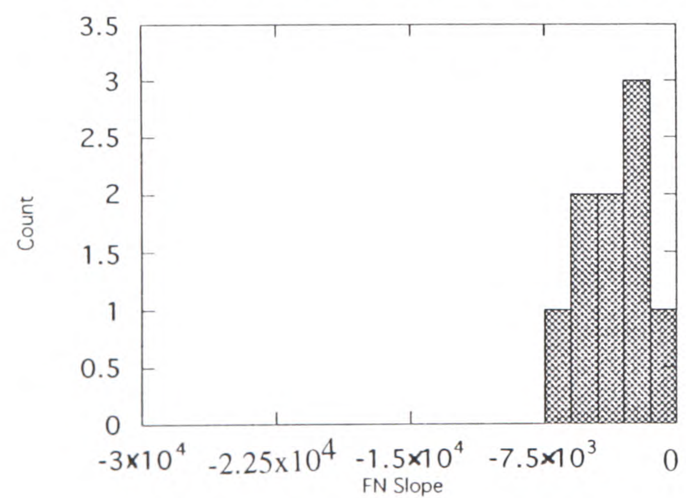


Figure 7.17 - Distribution of Maximum Emission Current for different Anodisation Times - P+-Type Si







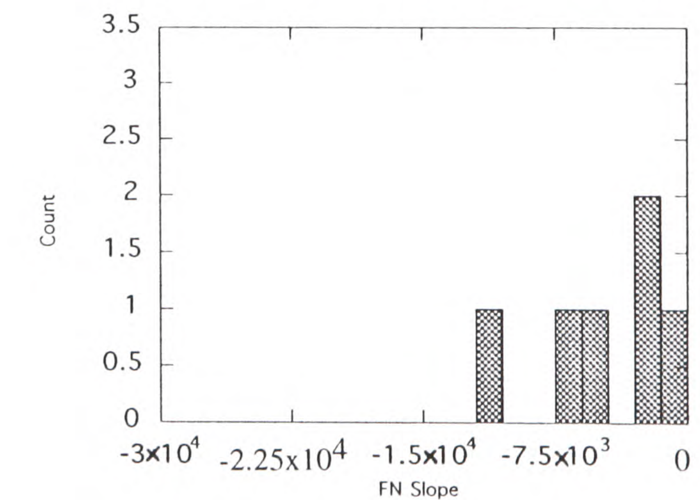
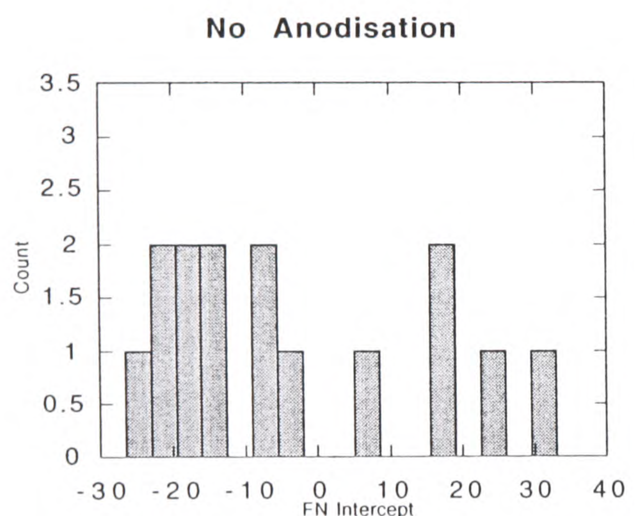
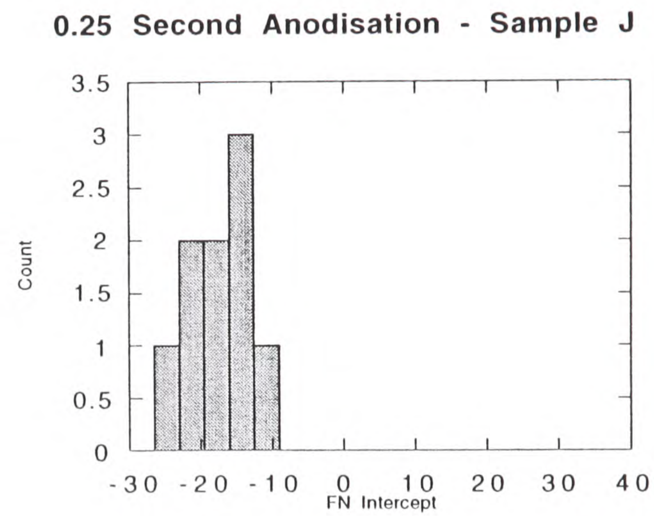
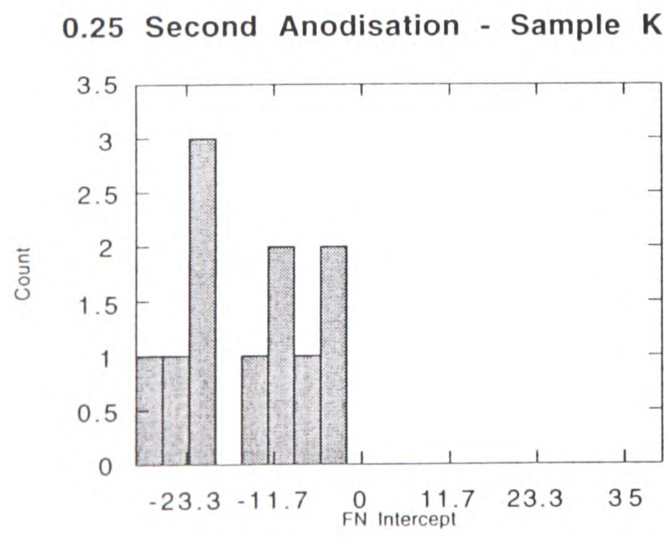


Figure 7.20a - Distribution of Fowler-Nordheim Slope for Different Anodisation Times - P+-Type Si







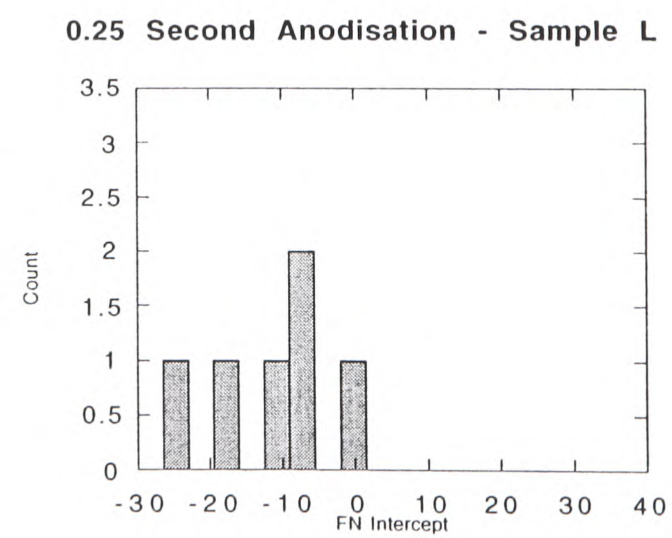


Figure 7.20b - Distribution of Fowler-Nordheim Intercept for Different Anodisation Times - P^+-Type Si

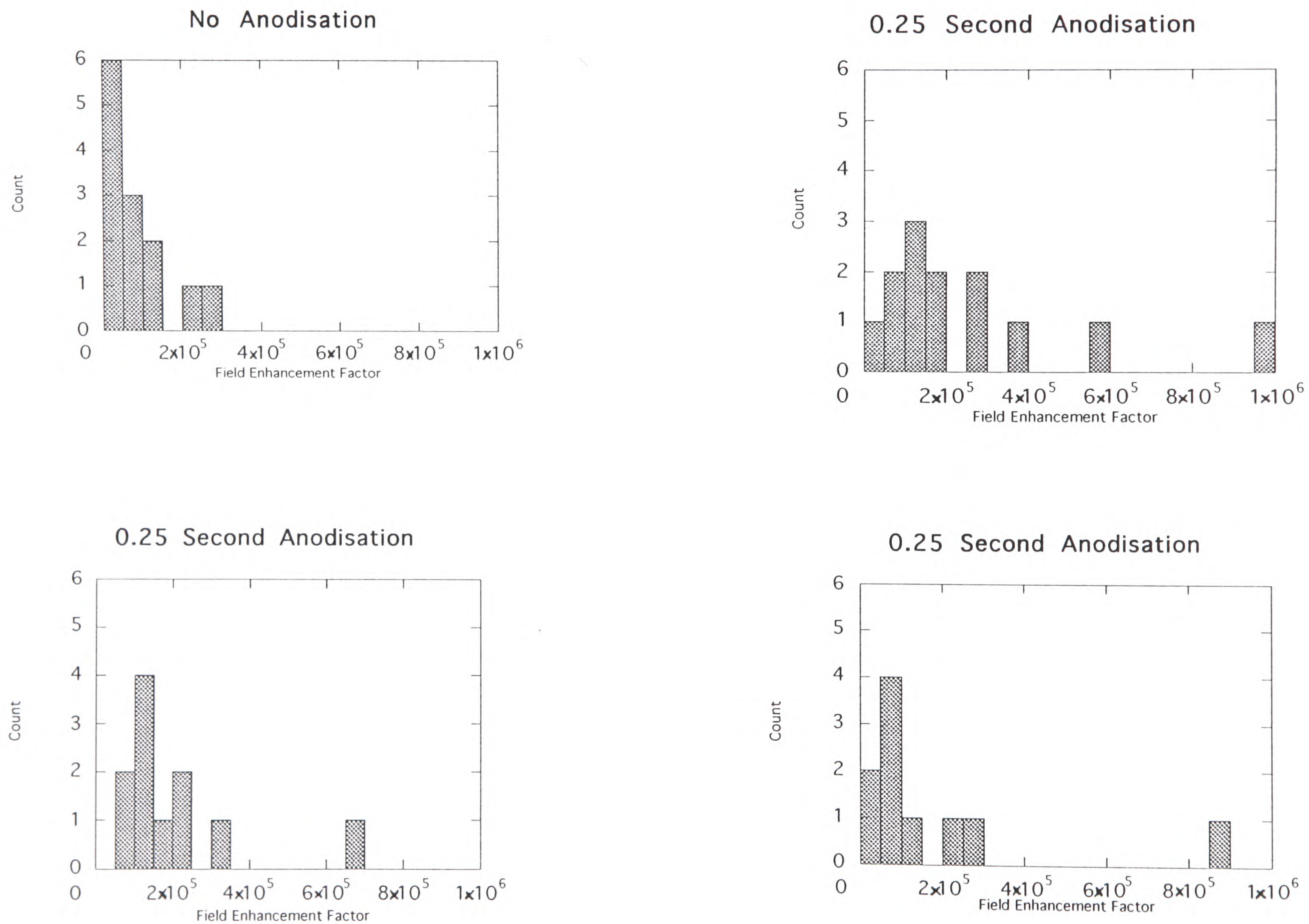
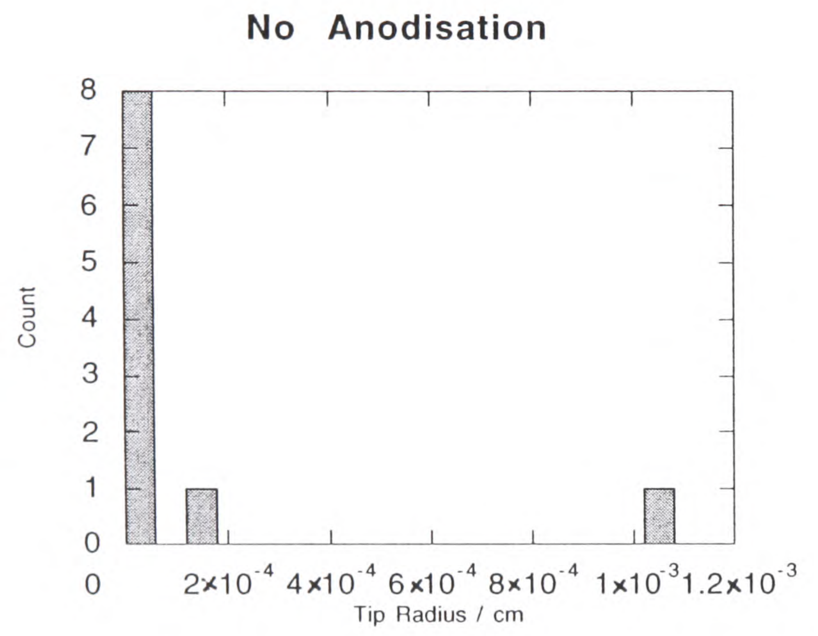
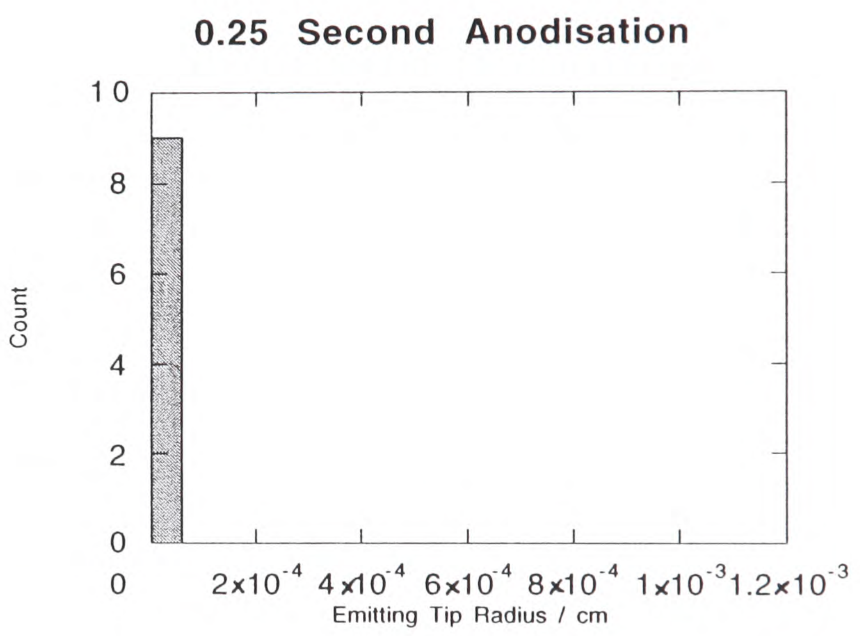
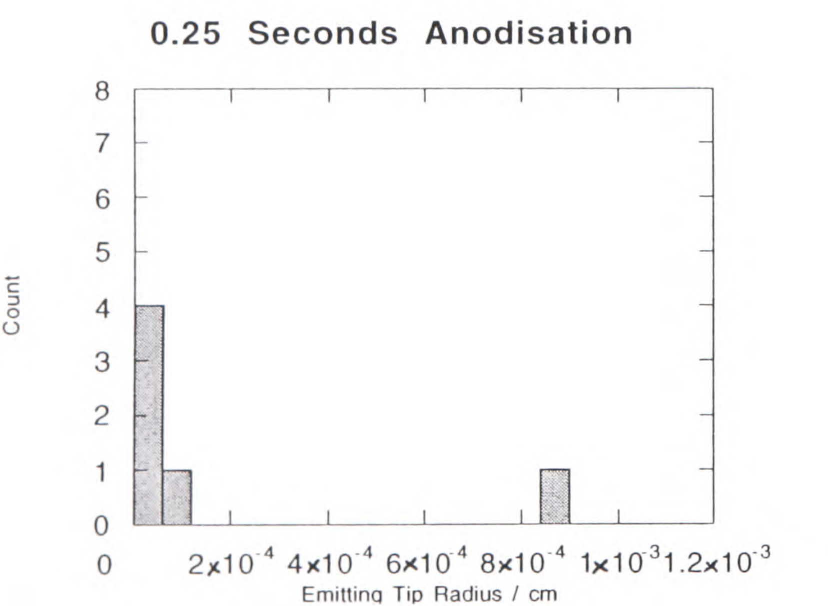


Figure 7.22 - Distributions of Field Enhancement Factor for Different Anodisation Times - P+-Type Si







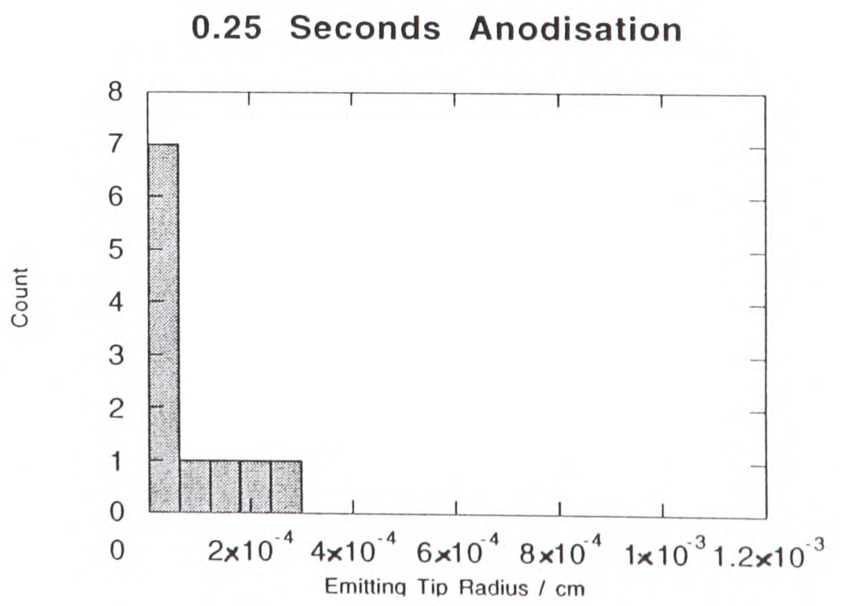
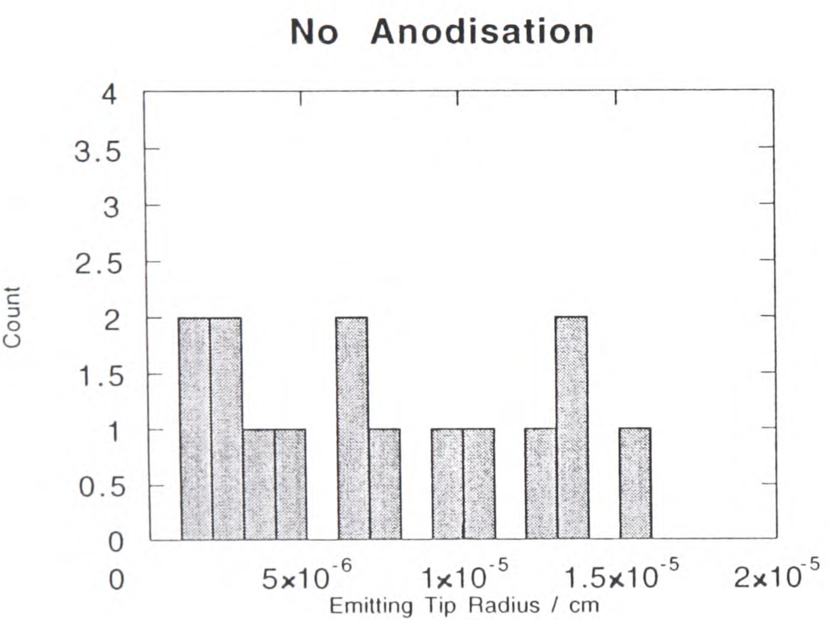
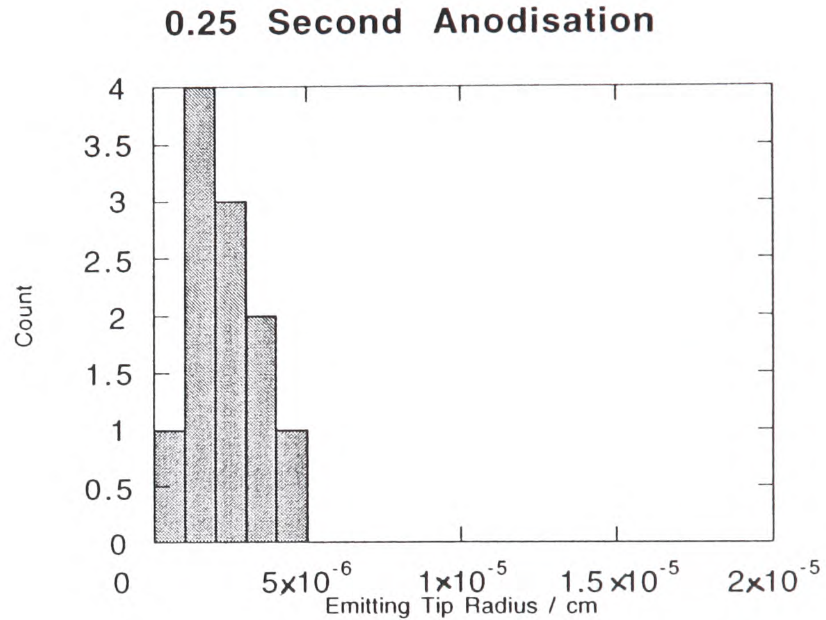
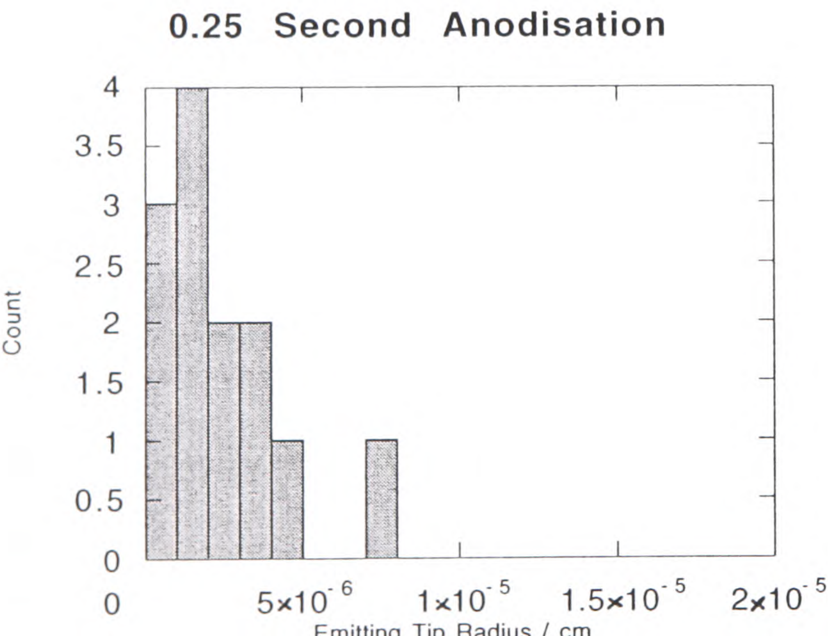


Figure 7.24a - Distributions of Emitting Tip Radius (Calculated from Emission Area) for Different Anodisation Times - P+-Type Silicon







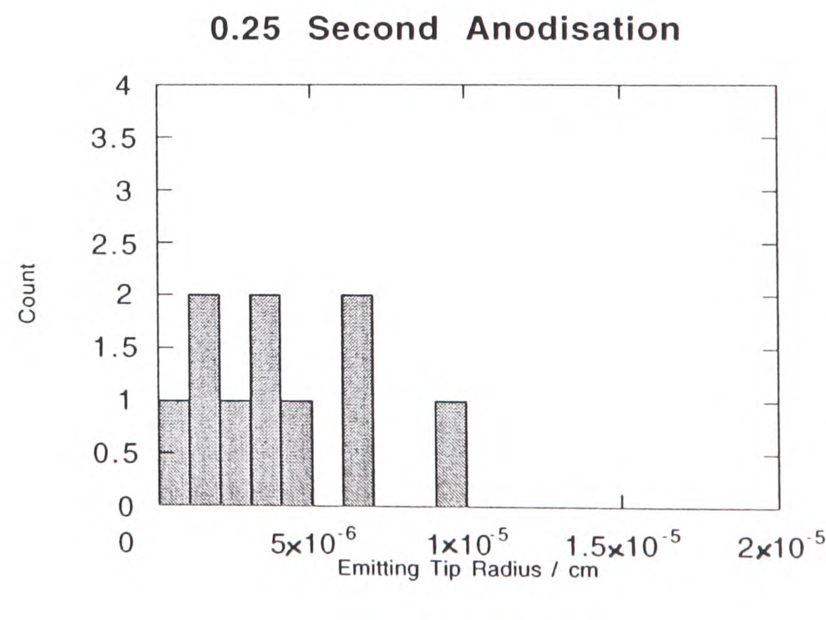


Figure 7.24b - Distributions of Emitting Tip Radius (Calculated from Field Enhancement Factor) for Different Anodisation Times - P+-Type Silicon

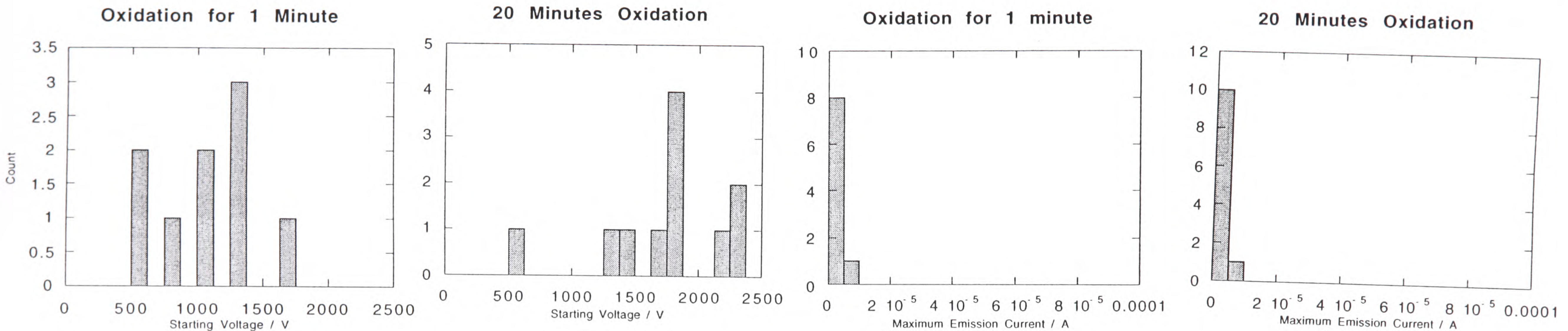


Figure 7.27 - Distribution of Starting Voltage and Maximum Emission Current following Oxidation for 1 and 20 Minutes at 950°C

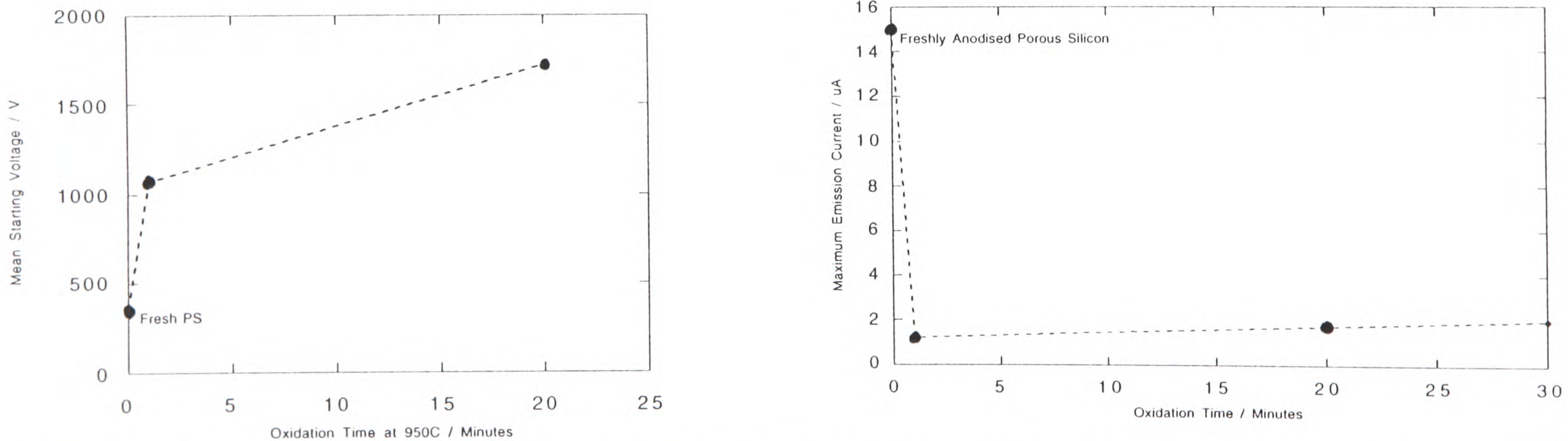
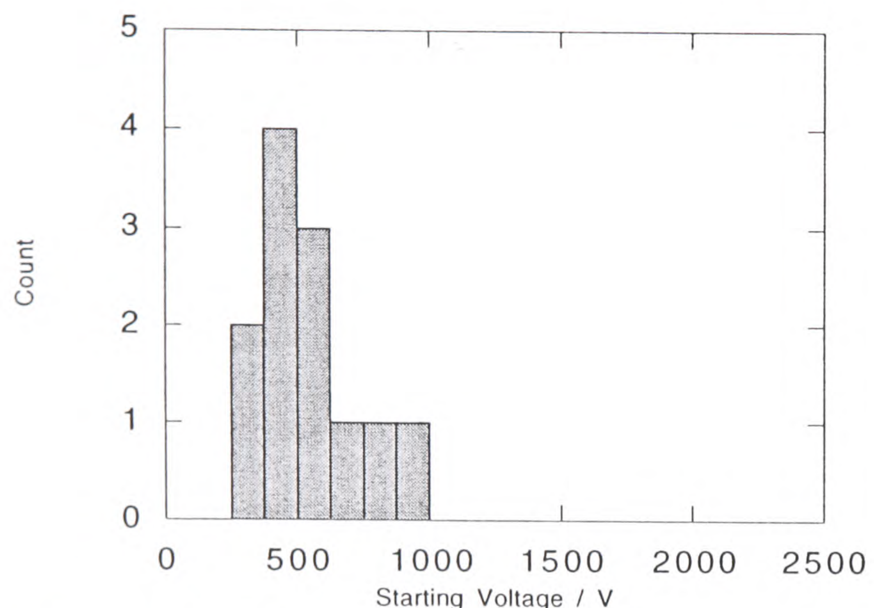


Figure 7.28 - Starting Voltage and Maximum Emission Current Following Oxidation at 950°C



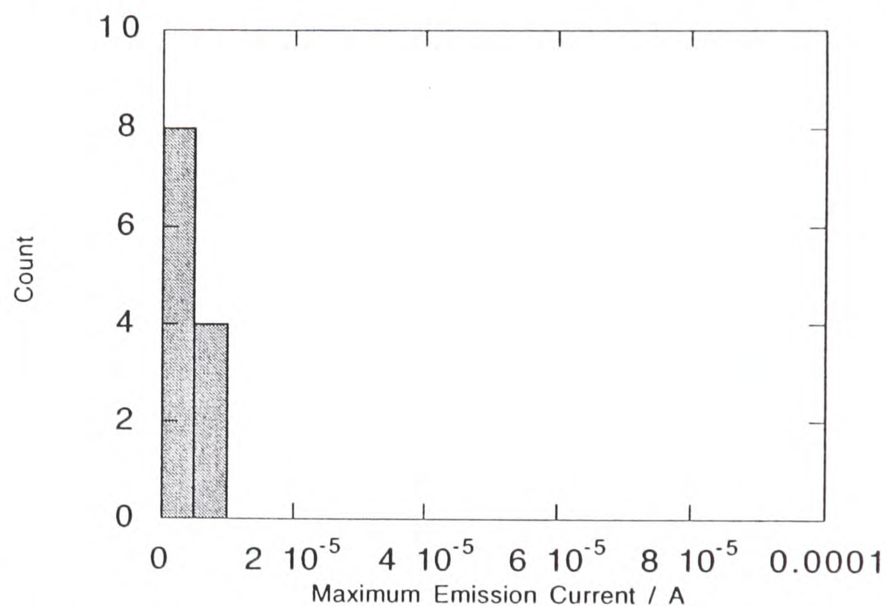
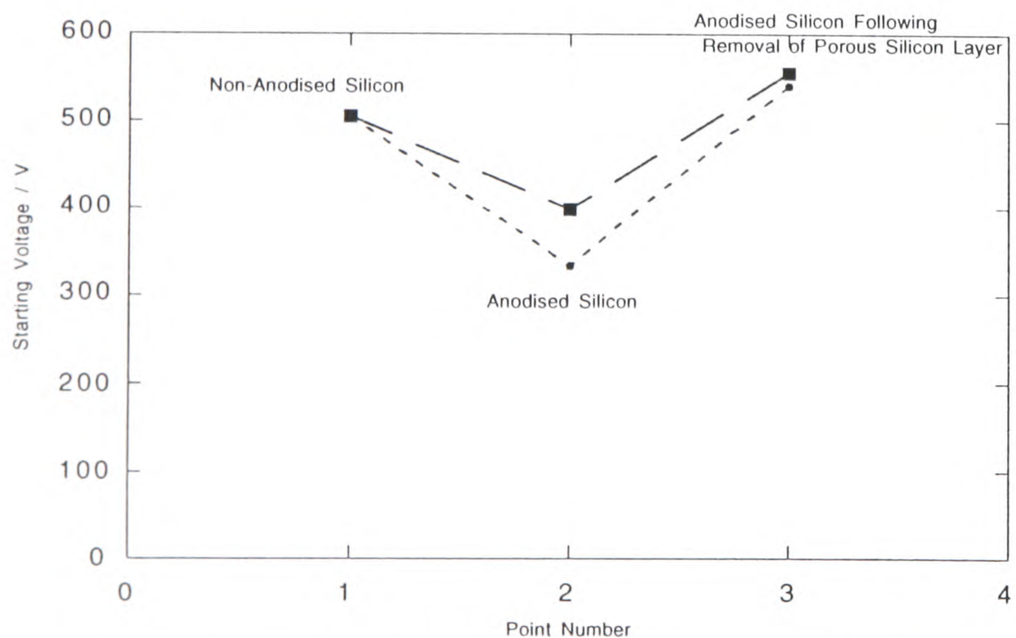


Figure 7.29 - Distributions following Dipping of Oxidised Samples into HF



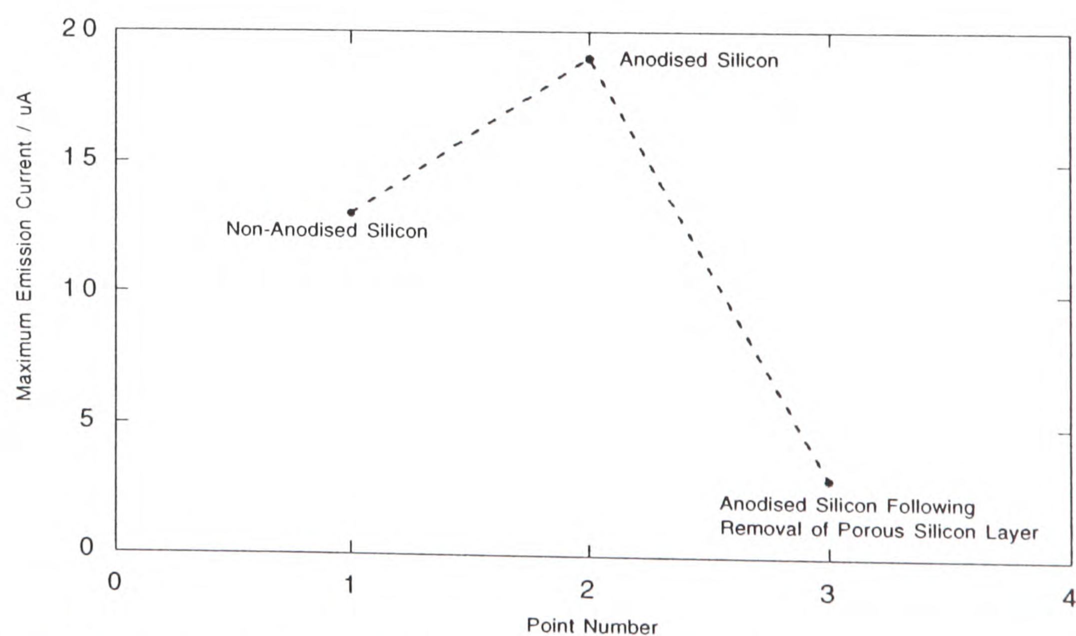
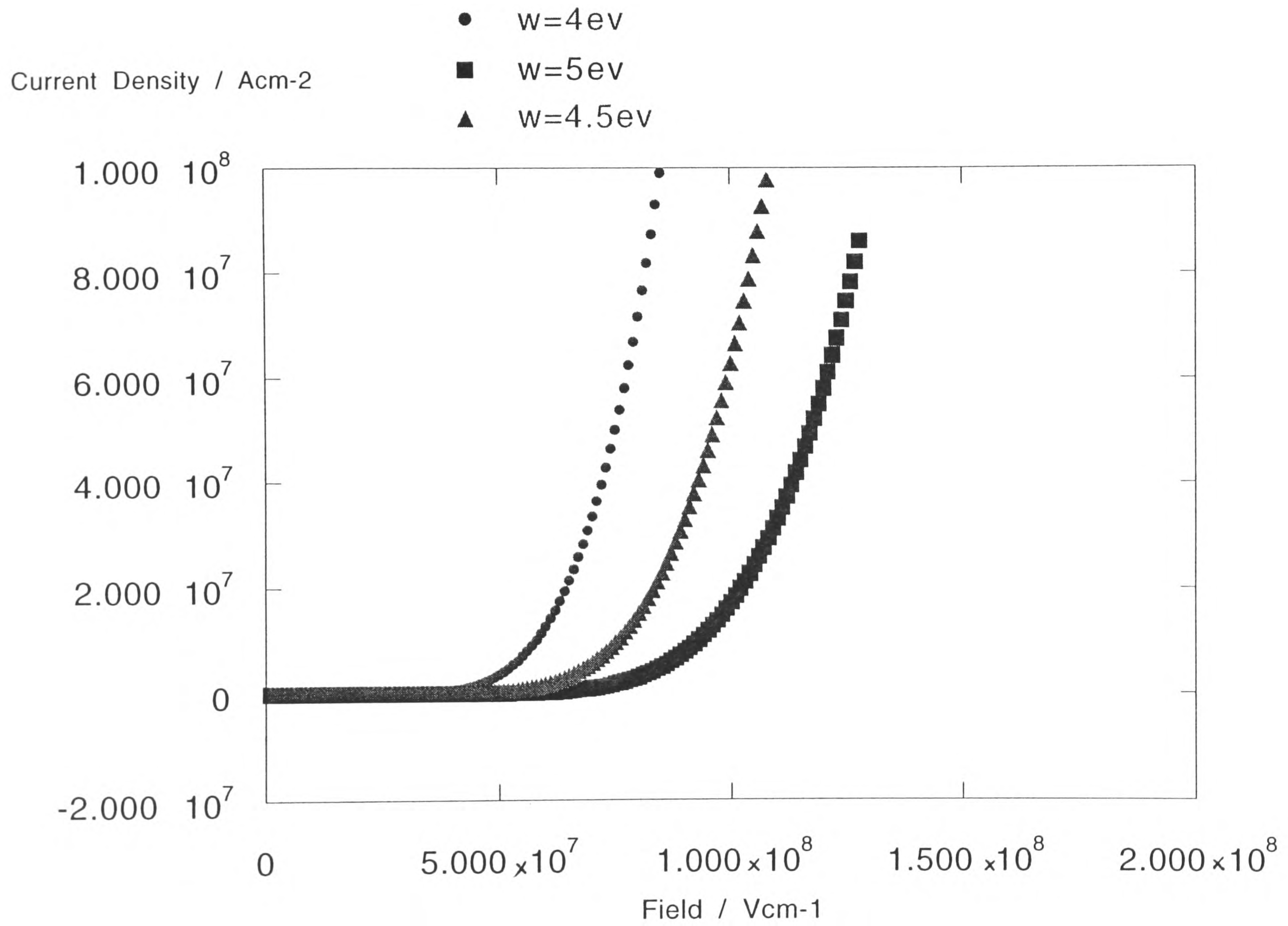


Figure 7.30 - Starting Voltage and Maximum Emission Current Following Removal of Porous Silicon Layer by Oxidation and HF Dipping


w=4ev
w=5ev
w=4.5ev
Current Density / Acm-2
1.000 10^8
8.000 10^7
6.000 10^7
4.000 10^7
2.000 10^7
0
-2.000 10^7
0
5.000 x10^7
1.000 x10^8
1.500 x10^8
2.000 x10^8
Field / Vcm-1

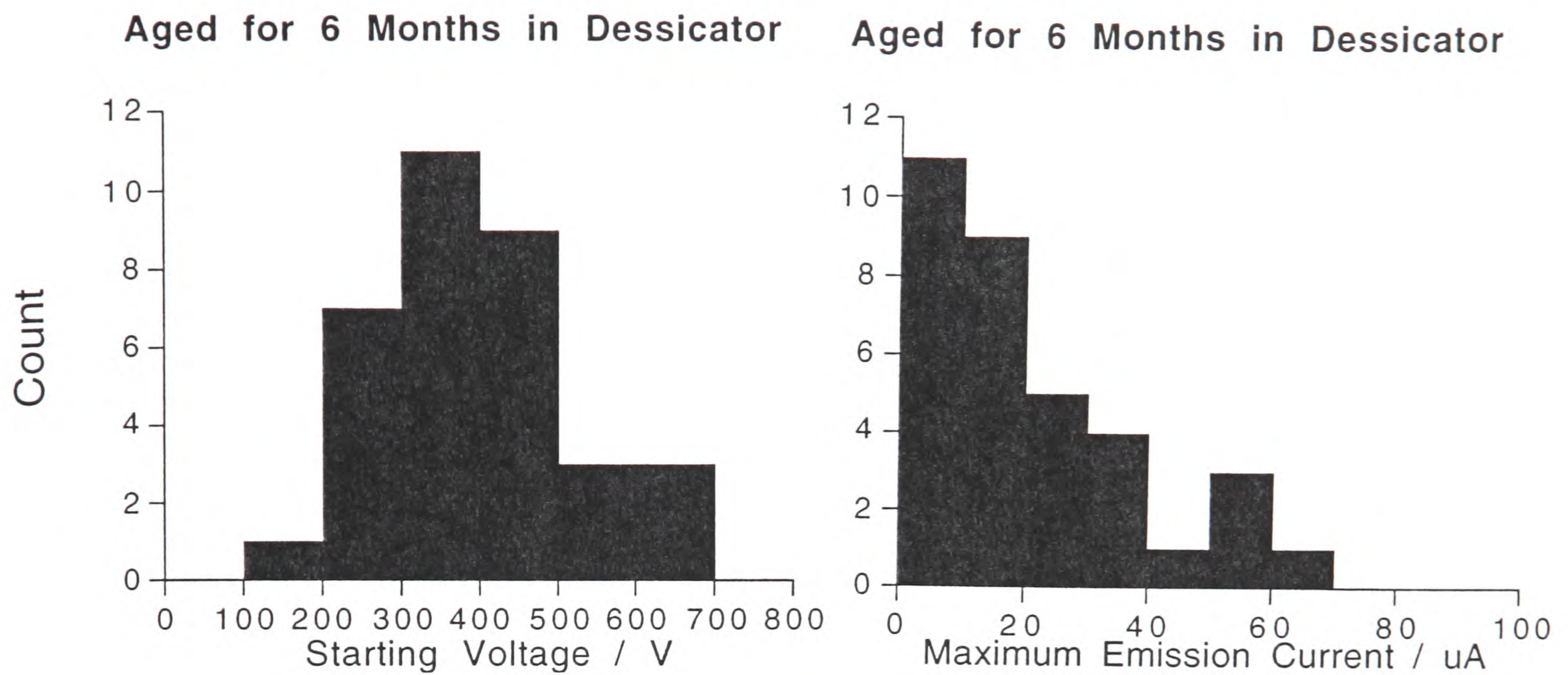


Figure 7.40 - Distributions of Starting Voltage and Maximum Emission Current After Ageing

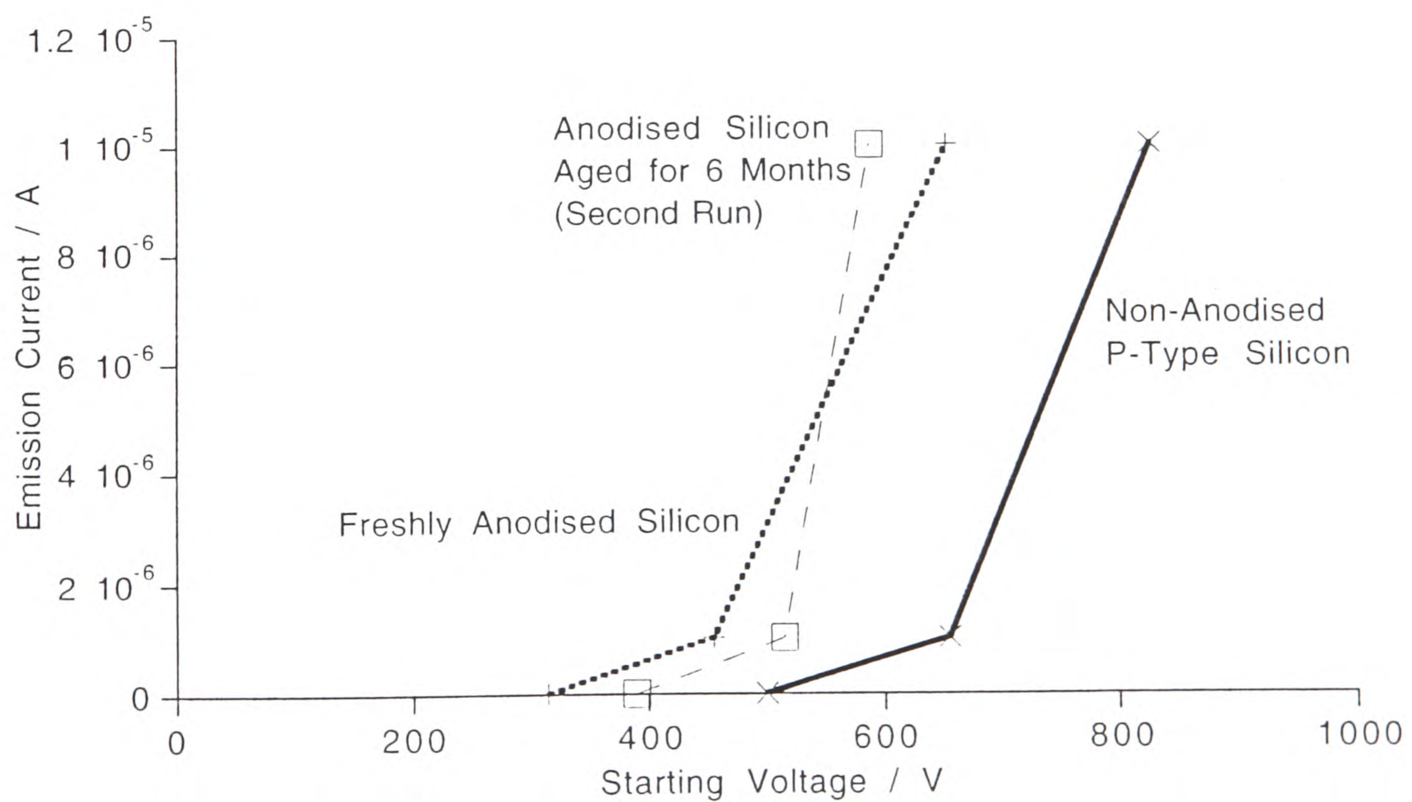


Figure 7.41 - Comparison of Current versus Voltage Before and After Ageing

Figure 8.2 a

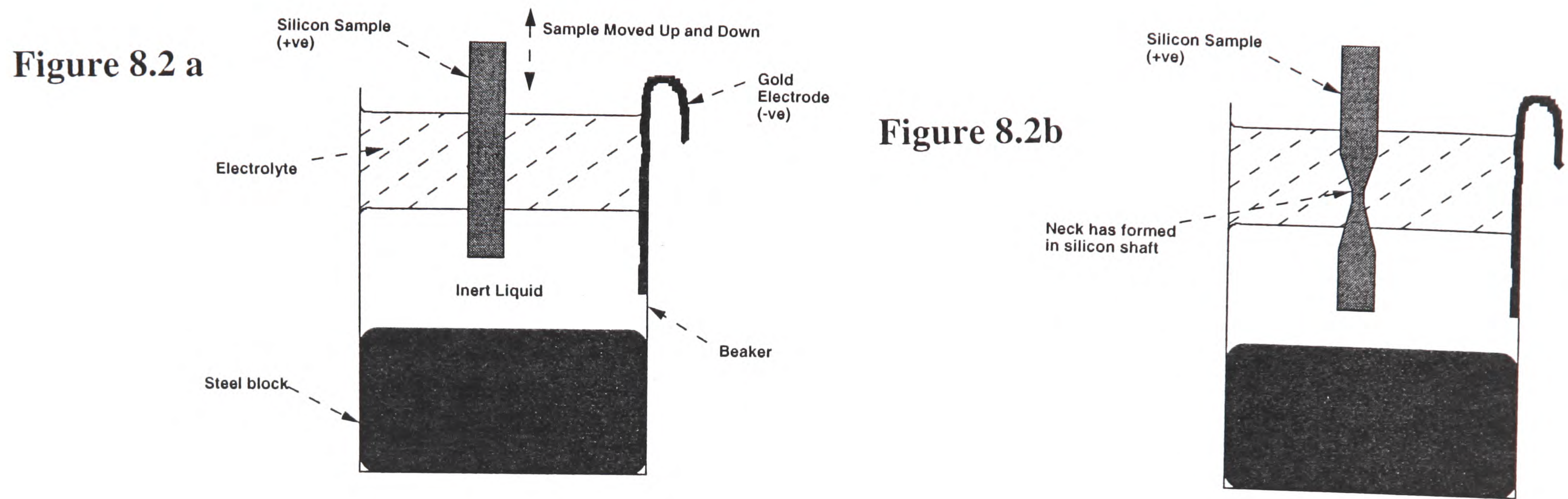


Figure 8.2b

Figure 8.3

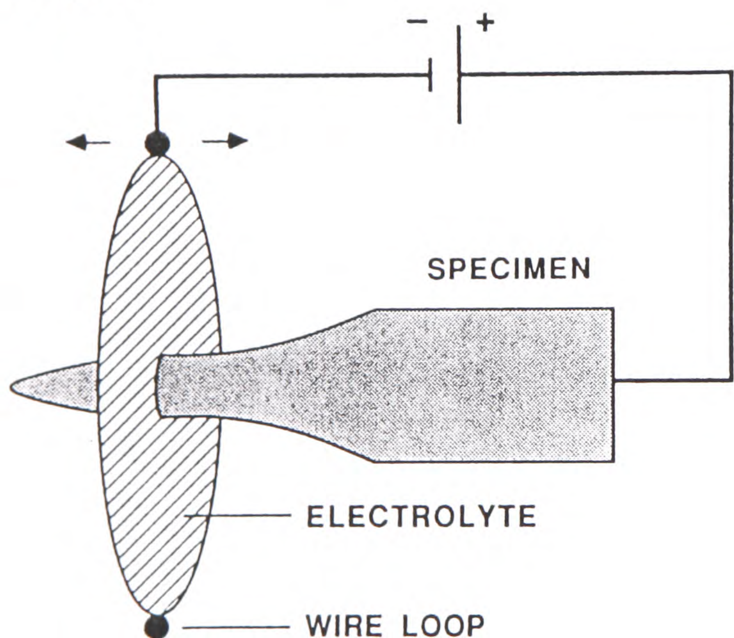
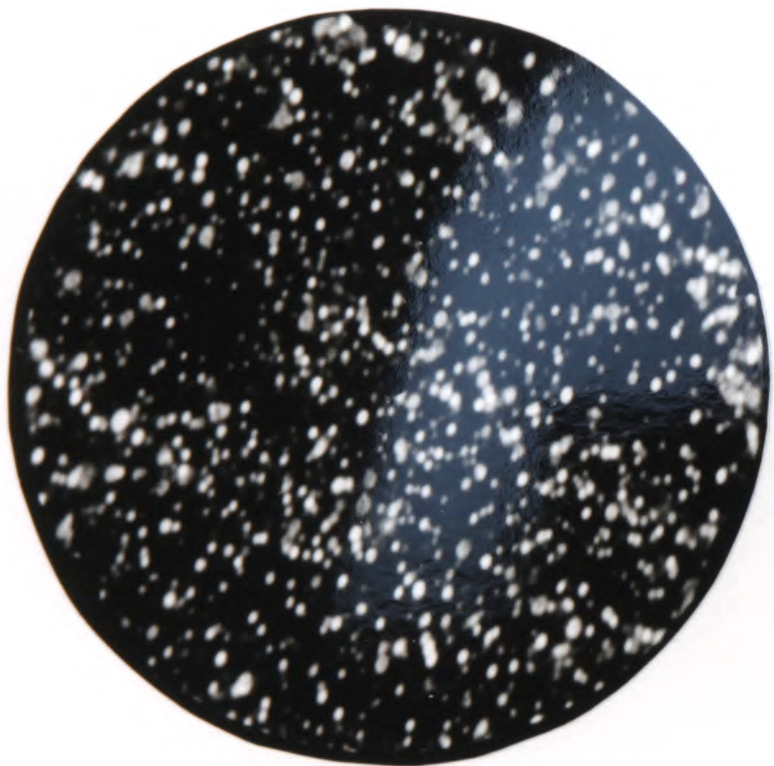


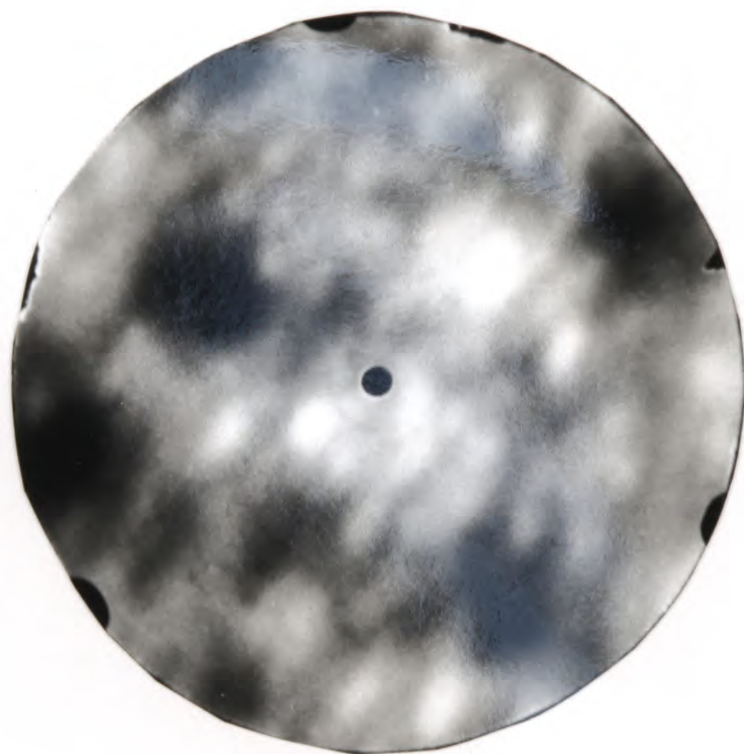
Figure 8.2 - Fast Polishing of Silicon FIM Tips
To produce a gradually tapered needle from a blank shaft, fast electropolishing was carried out. The tip was lowered in and out of the solution - see Figure 8.2a. This movement was carried out until the tip formed a neck (see Figure 8.2b), and the weight of the lower half became too heavy to be supported by the necked region and so broke in two.

Figure 8.3 - Slow Polishing of Silicon FIM Tips
Slow polishing was carried out after fast polishing, in order to produce a very sharp tip. A small gold counter electrode was filled with a drop of electrolyte. This was placed on the specimen stage of a low power optical microscope, so that the polishing process could be observed. The specimen was moved in and out of the centre of the electrode ring, while controlled pulses of ~1 second duration were applied to the tip. Polishing was stopped when the tip became vanishingly sharp.

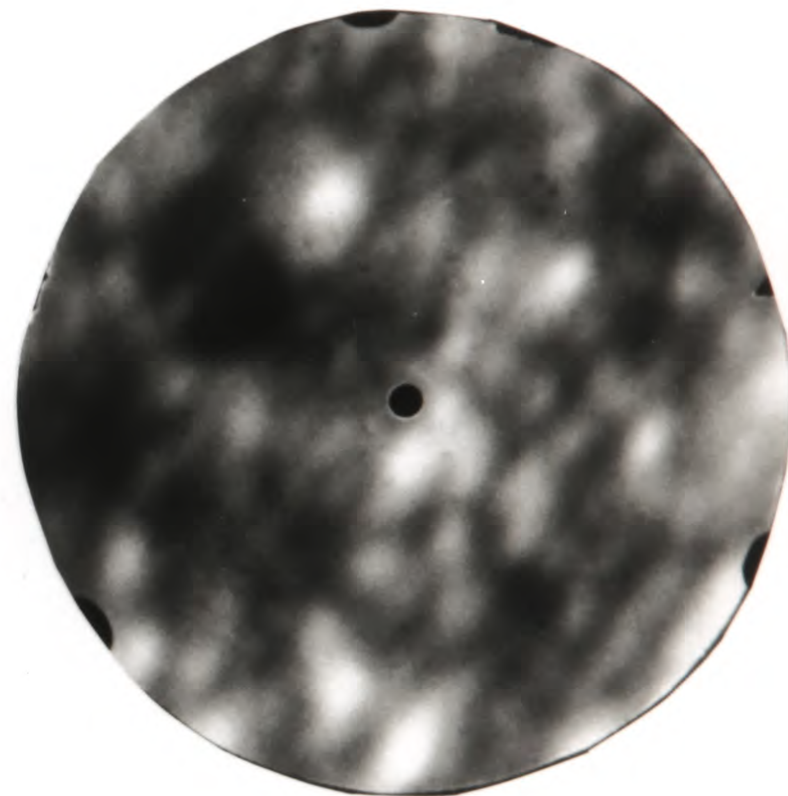
(Ref: M.K.Miller & G.D.W.Smith, "Atom Probe Microanalysis: Principles and Applications to Materials Problems, (Materials Research Society, 1989)



a) FIM image at 7.01kV
Note the uniform distribution of spots



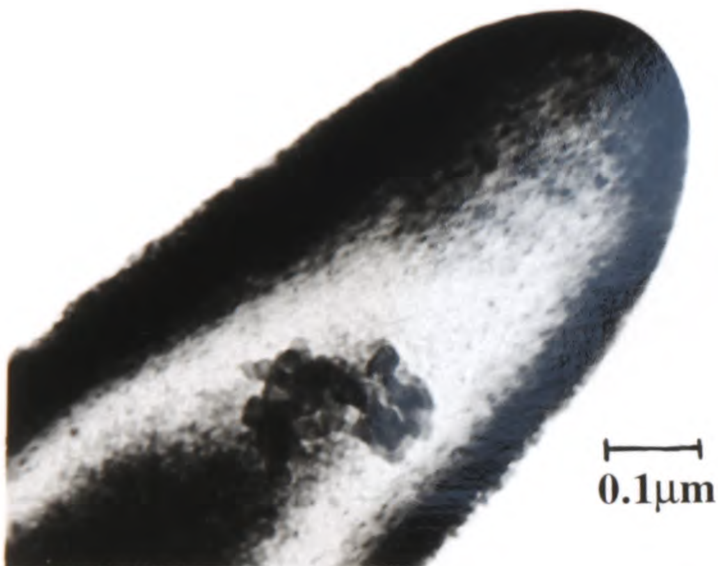
b) FEM image at 1030V
Note uniform distribution of small spots.
Bright spots indicate regions of highest emission.



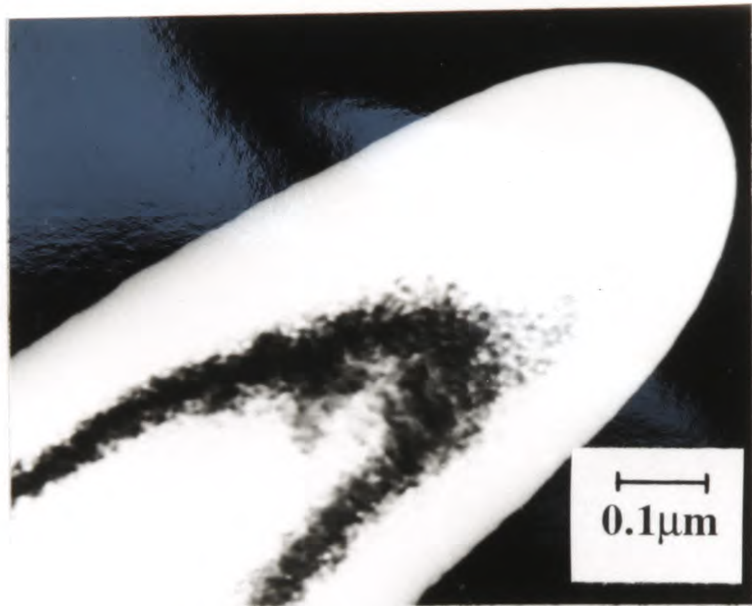
c) FEM image at 1030V after field emission run
Note that distribution of spots is still
but position of brightest spots has sh
field emission run was carried out to

Axis of tip lies along [110] direction.

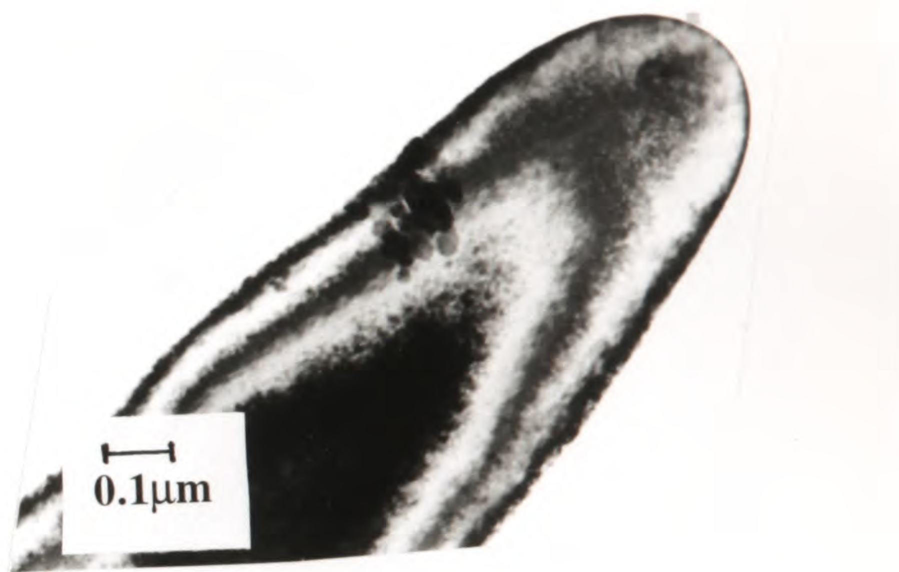
Figure 8.6 - FIM and FEM images obtained from symmetric field evaporated P^+-type silicon tip which exhibited fully fogged out image at 7.7kV (ref: 4/6/95)
All tips which exhibited fully fogged out FIM images at 7.7kV produced a series of images similar to those shown here.



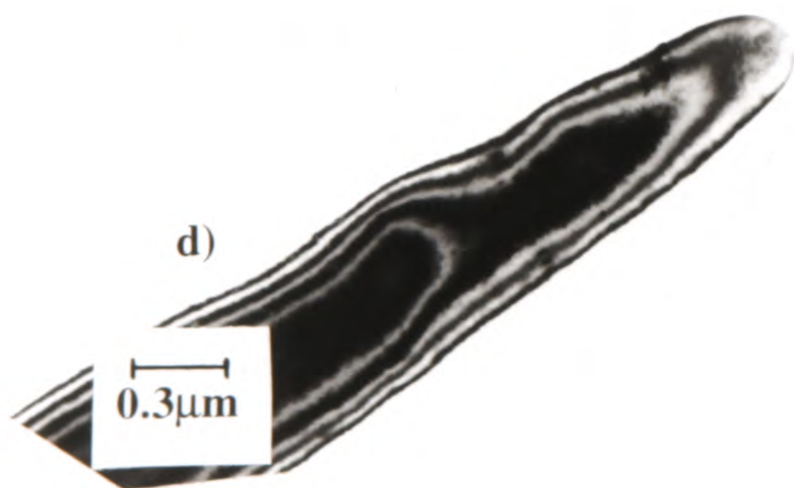
a) Bright-Field image of tip
Tip radius is ~100nm
Note tip end is smooth and round



b) Dark Field image of same tip
Note tip end is smooth and round

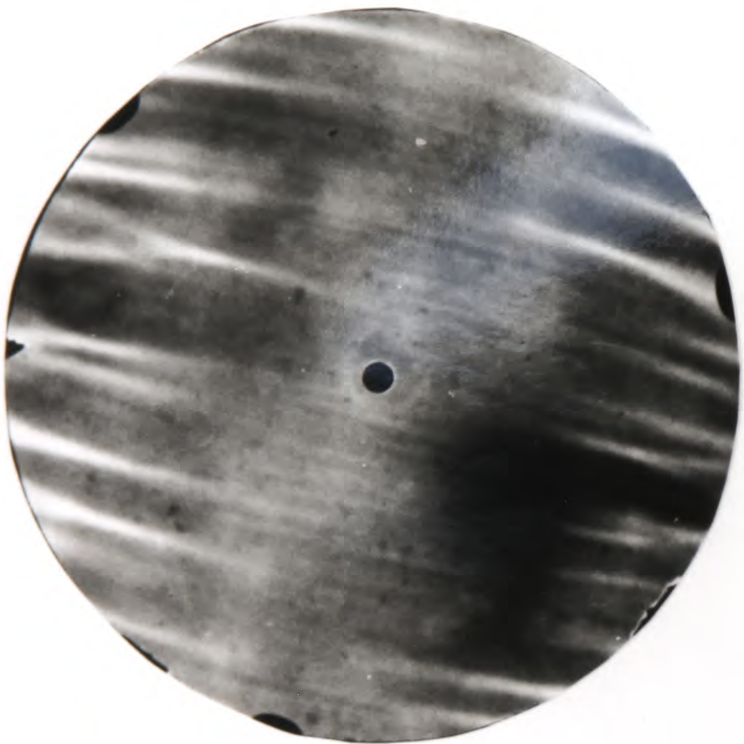


c) Bright-Field image of same tip rotated through ~90°
Note that tip has similar geometry when rotated through ~90°
(observe position of dust particle near tip),
showing that emitter is symmetric.

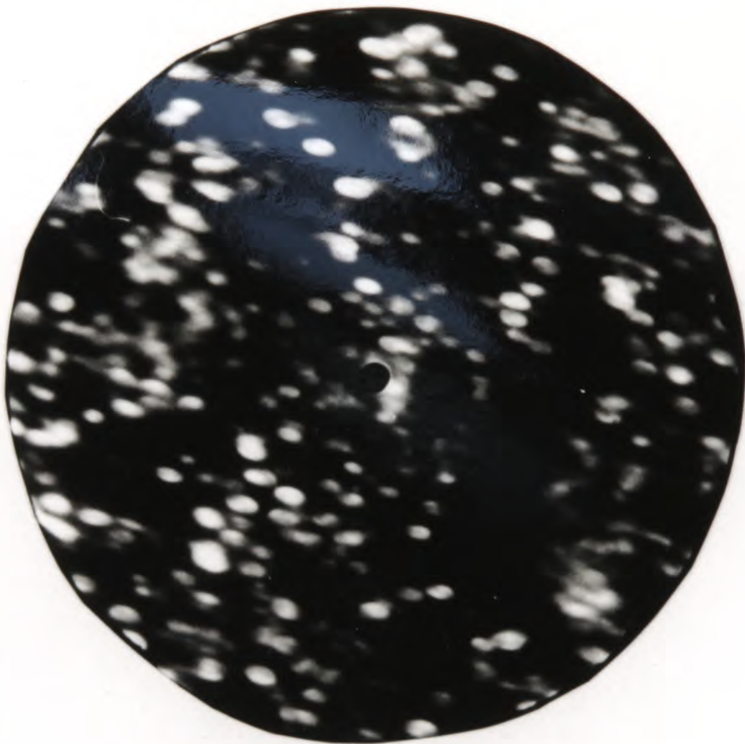


d) and e) same tip at lower magnifications showing overall geometry of shaft of FIM tip

Figure 8.7 - TEM images of typical symmetric silicon tip field evaporated to 7.7kV (exhibiting fully fogged out FIM image at 7.7kV)

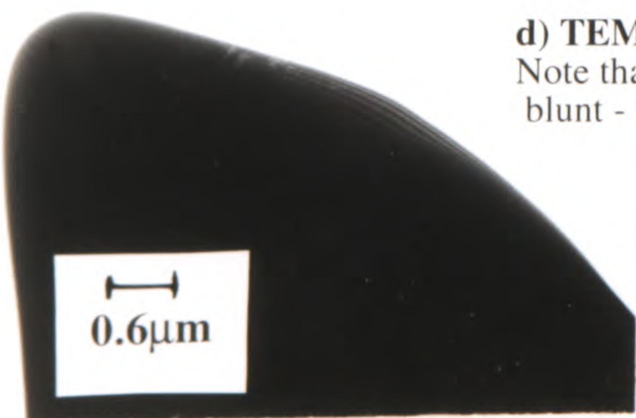


a) FIM image at 7.7kV
Note streaks across image indicating that tip is blade-shaped.

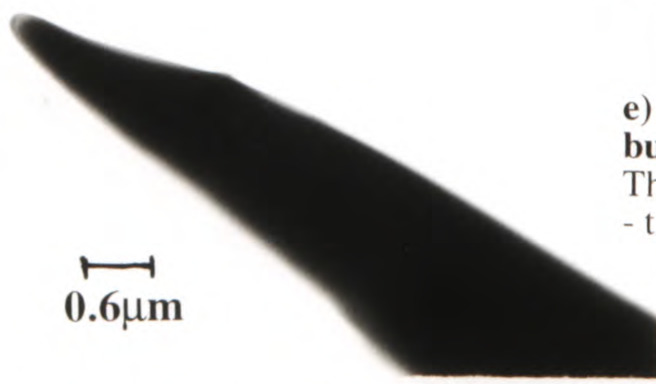


b) FIM image at 6.3kV
Note that distribution of spots is less uniform and spots are larger than for FIM image for uniform tip shown in Figure 8.6a.

c) FEM image at 1090V
Note that some spots are much larger and brighter than other spots. Image is less uniform than for FEM image obtained from uniform tip shown in Figure 8.6c.

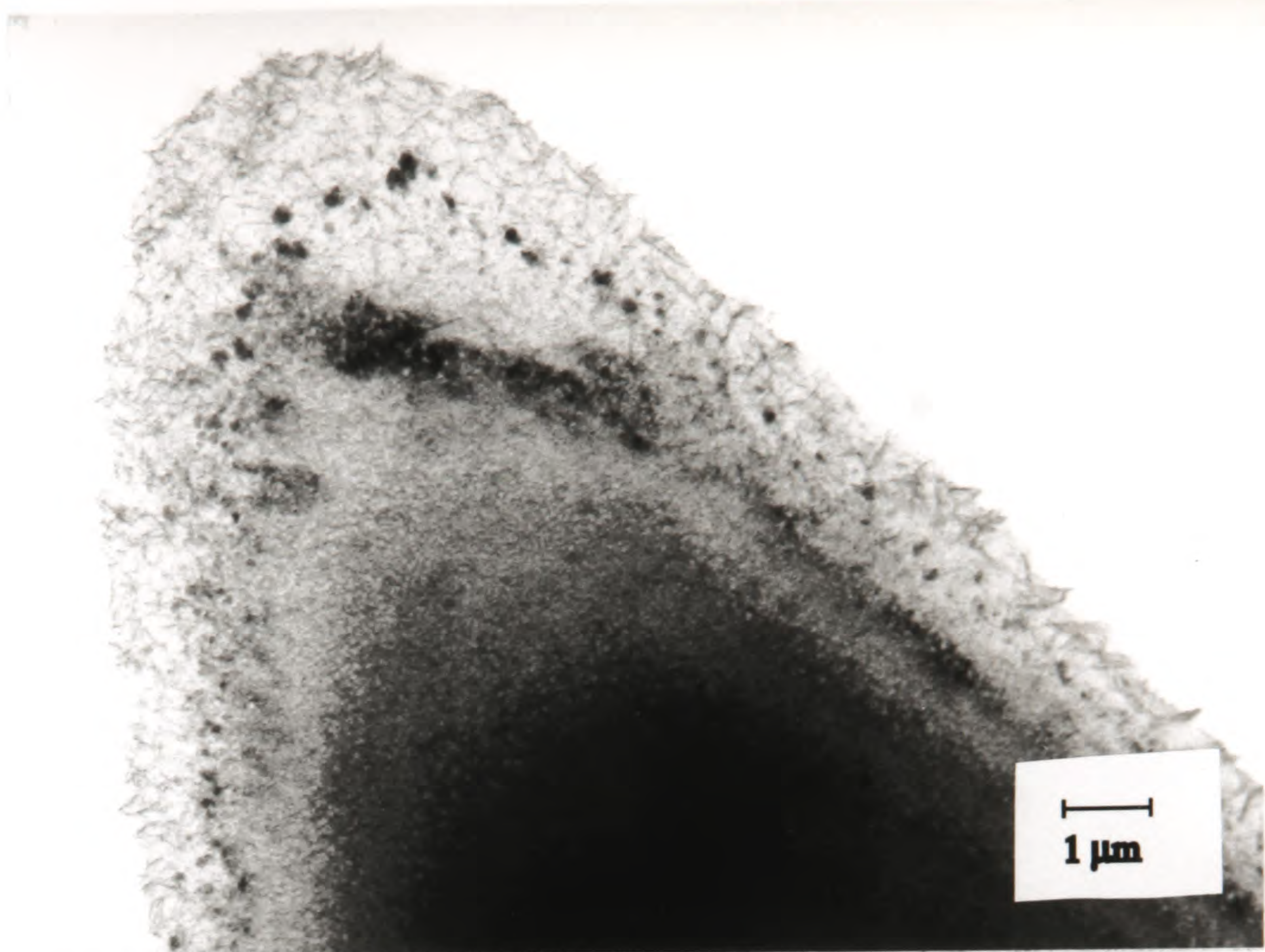


d) TEM image of similar tip
Note that tip appears to be quite blunt - tip radius is ~0.7μm

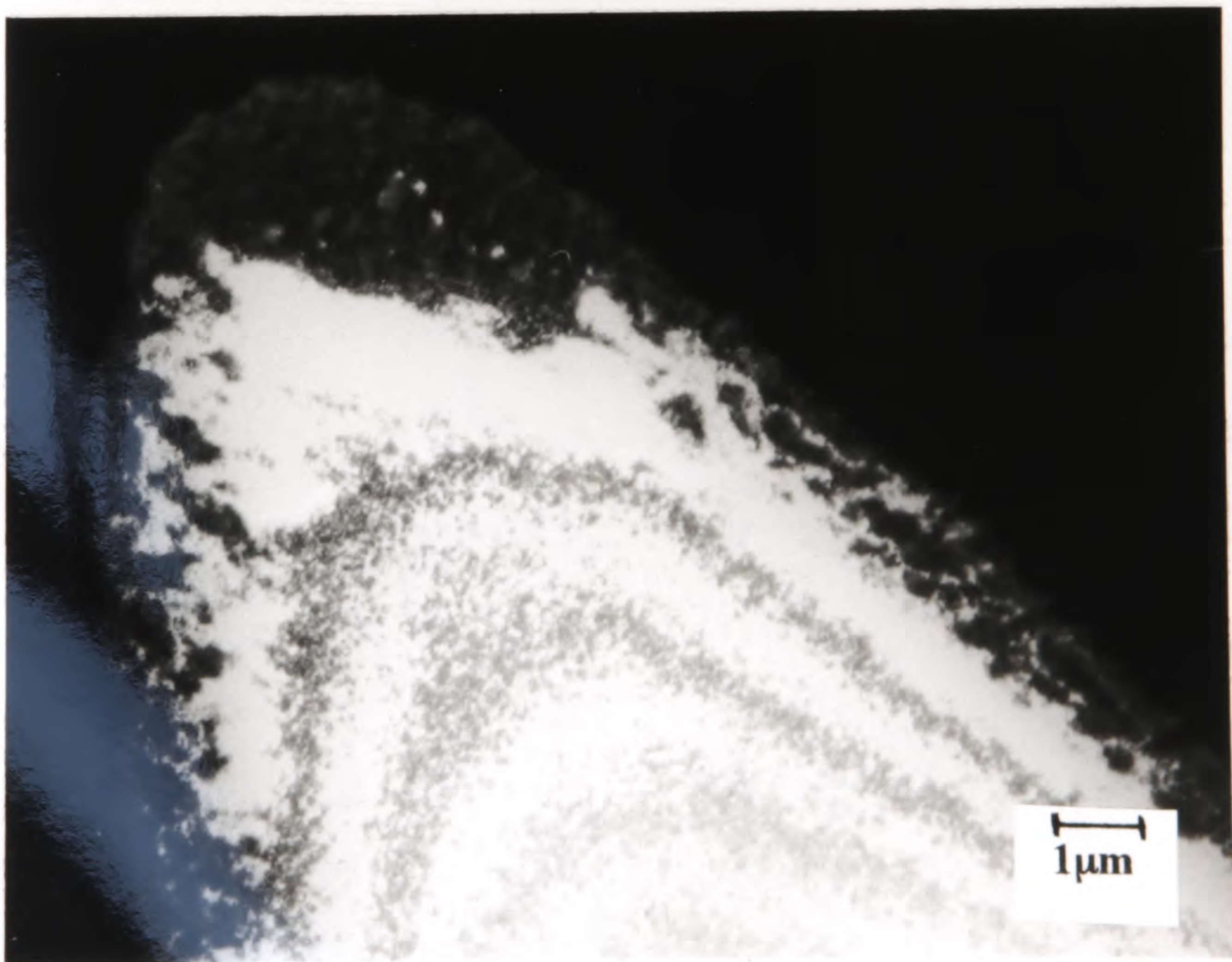


e) TEM image of tip shown in d), but rotated through 90°
This shows that tip is blade-shaped - tip radius is ~0.1μm in this direction.

Figure 8.8 - FIM and FEM images from non-symmetrical blade-shaped tip which did not exhibit fully-fogged out FIM image at 7.7kV
Note that in order to obtain a uniform FIM and FEM image, this tip would have to be field-evaporated to 11kV (ref: 22/10/94)

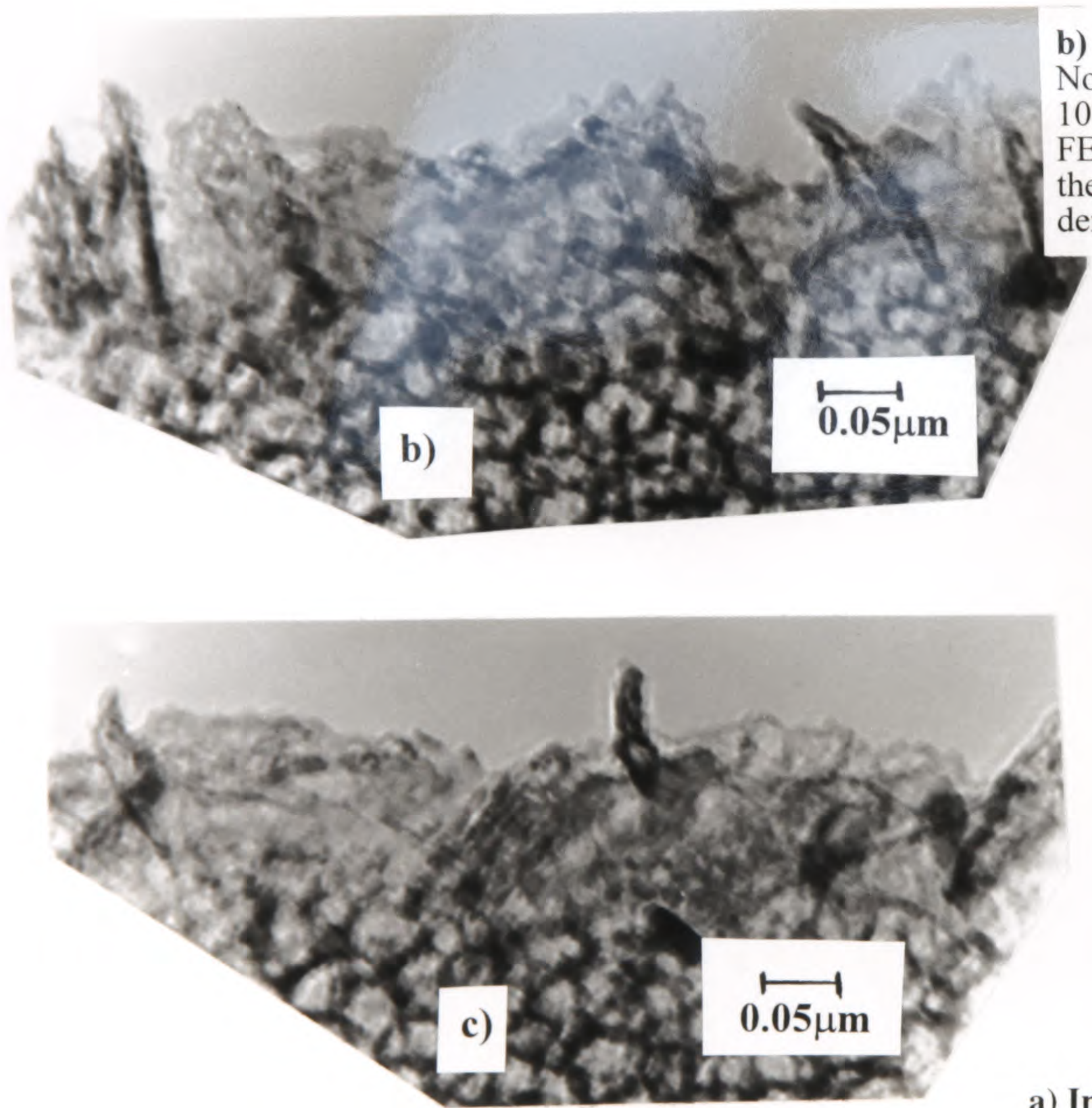


Bright-Field Image

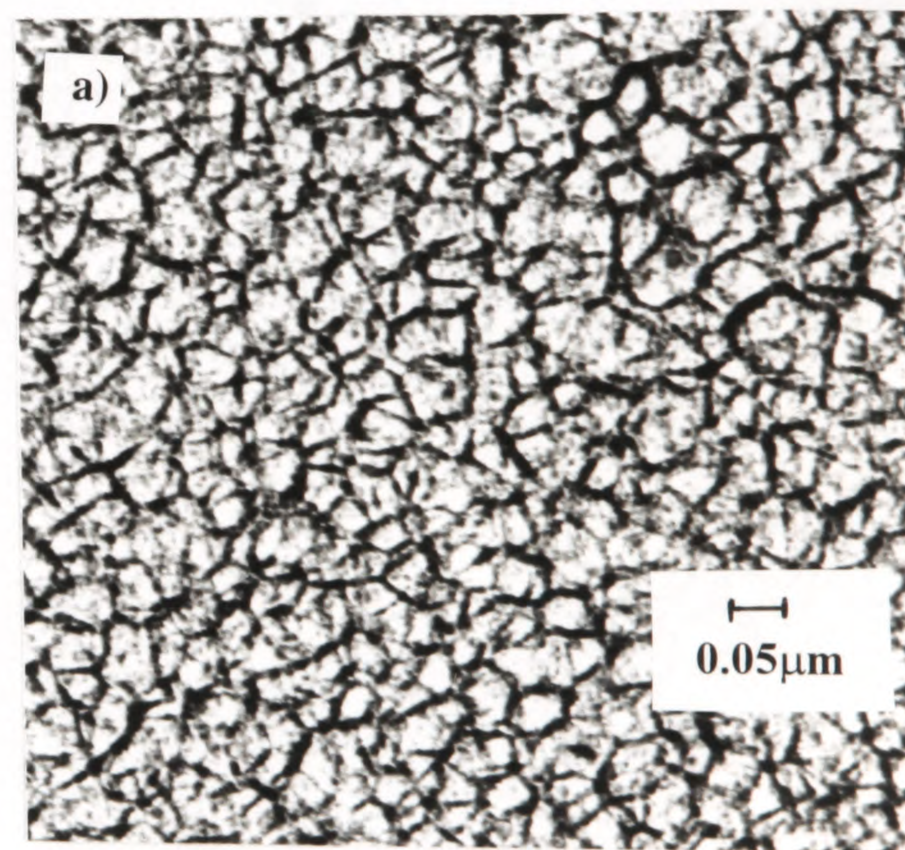


Dark-Field Image

Figure 8.10 - TEM of Anodised P+-Type Silicon FIM Tip
Note high concentration of fibrils all over tip surface. These fibrils could act as points of field enhancement. Comparing the bright and dark field images, also the note the silicon core. Anodisation conditions were 1mA for 2 seconds.

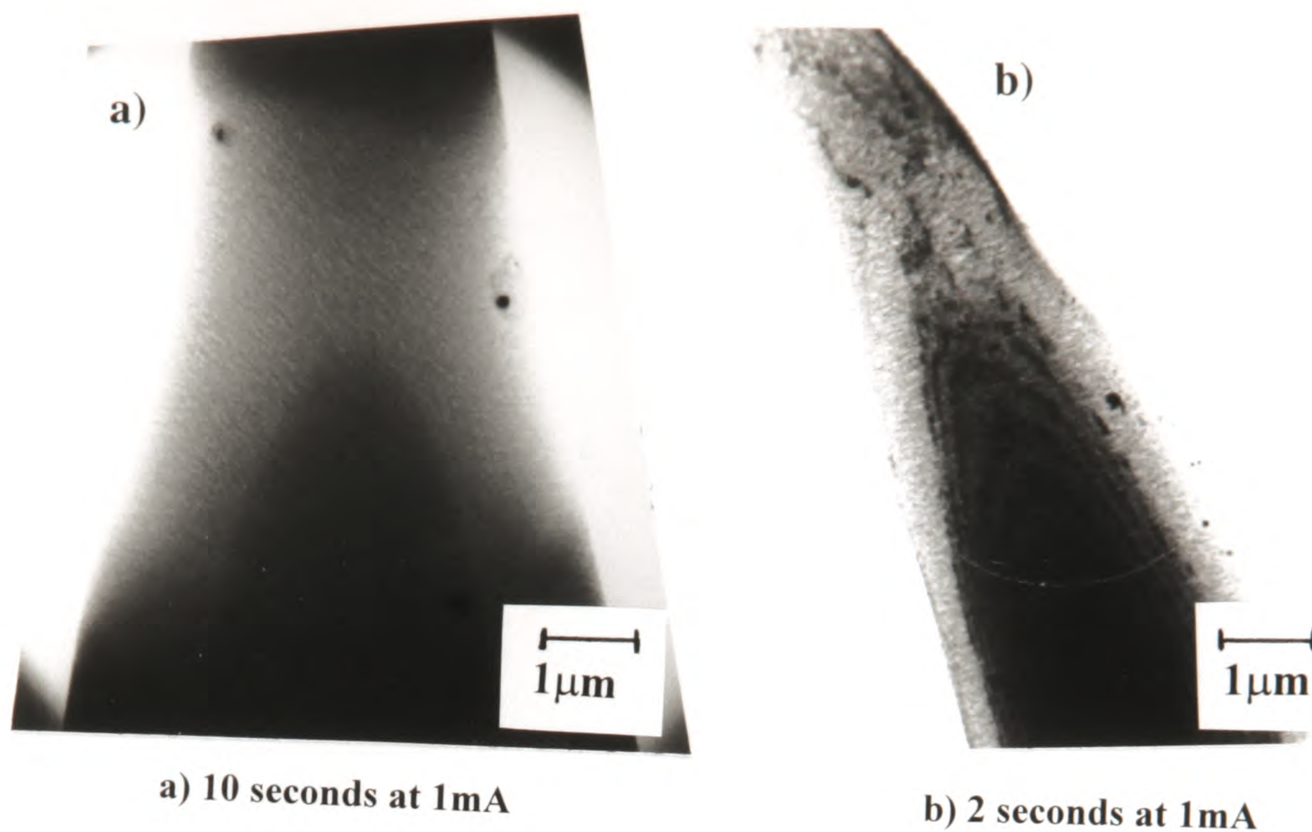


b) and c) Tip surface at high magnification
Note the fibrils standing proud of the emitter surface. Some of the fibrils are up to 100nm in height. Fibrils are higher than for those observed at the surface of anodised FEAs, where fibrils were ~5-10nm high. Again, the difference in morphology between these two structures is likely to be due to differences in the applied anodisation current density at the different tips.



a) Image of tip taken looking through pores
Note the honeycomb structure which is similar to that observed for anodised FEAs. The pore width is also similar, being in the range 20-50nm wide.

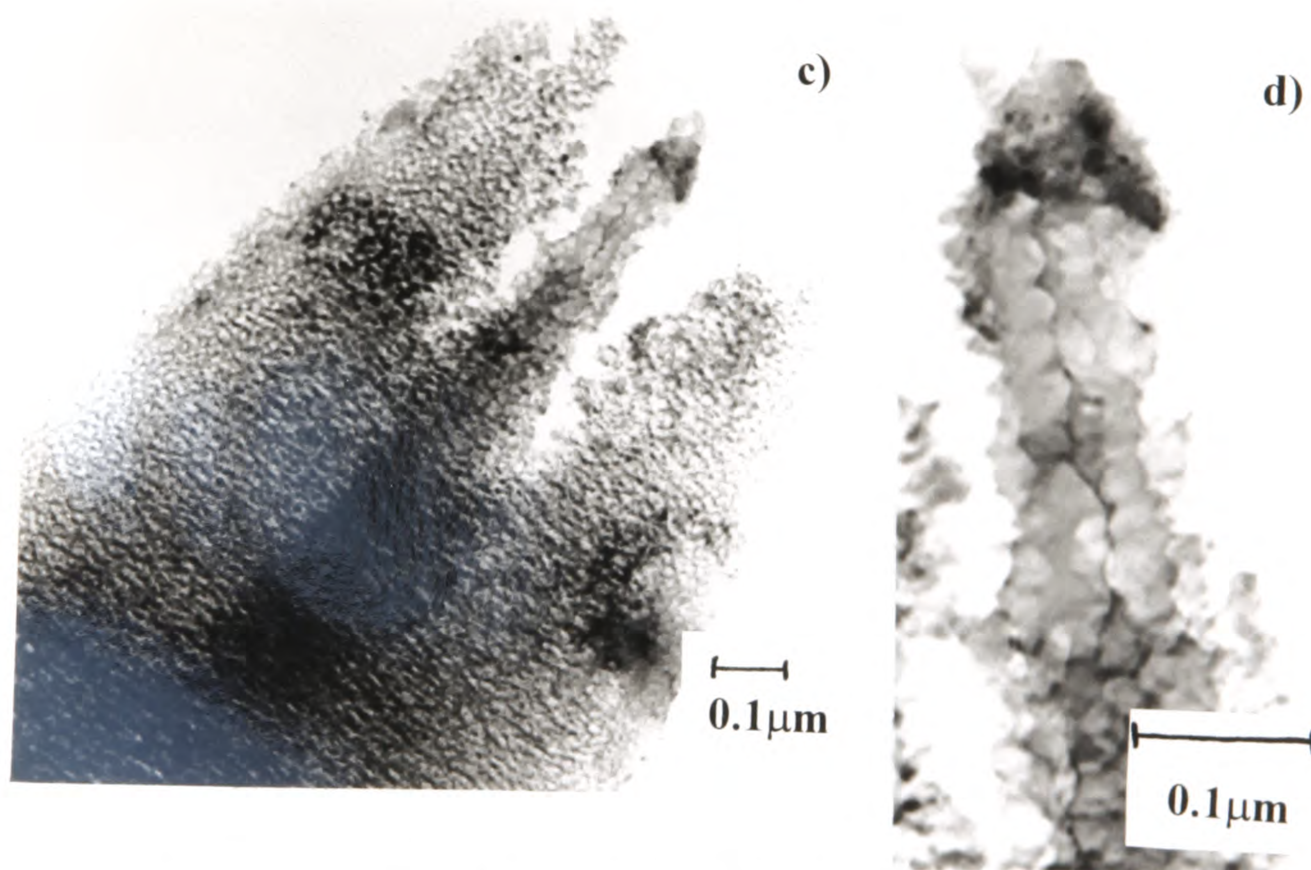
Figure 8.11 - High magnification TEM images of anodised p^+-type silicon FIM tip shown in Figure 8.10



a) 10 seconds at 1mA

b) 2 seconds at 1mA

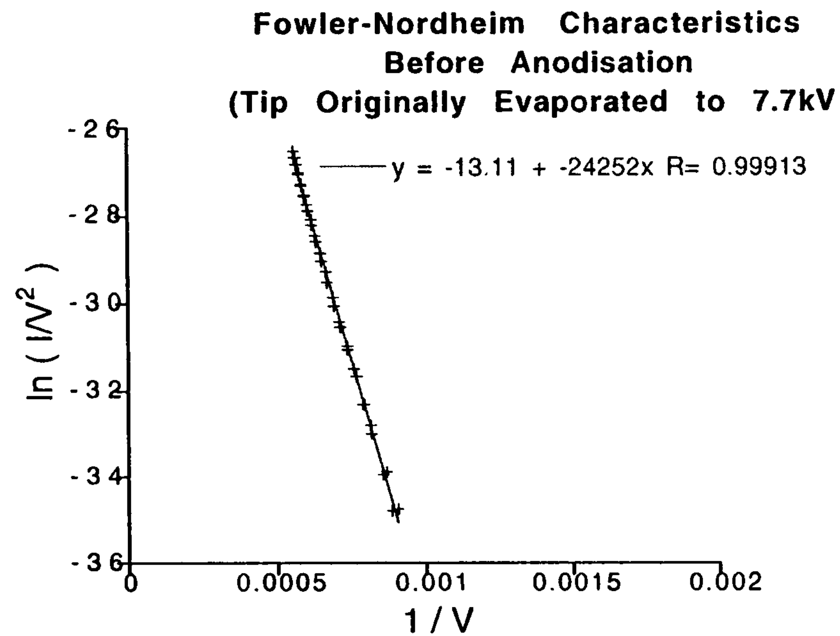
a) and b) Core structure of two tips anodised with different tip geometry or anodisation time compared to tip shown in Figure 8.10
Note that thickness of porous silicon layer at tip apex is thicker than up sides of the tip.

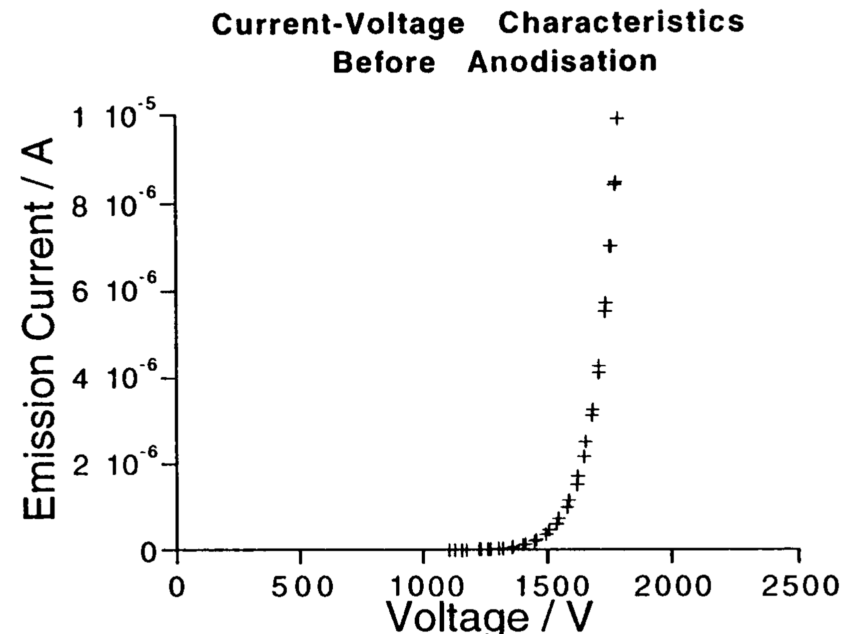


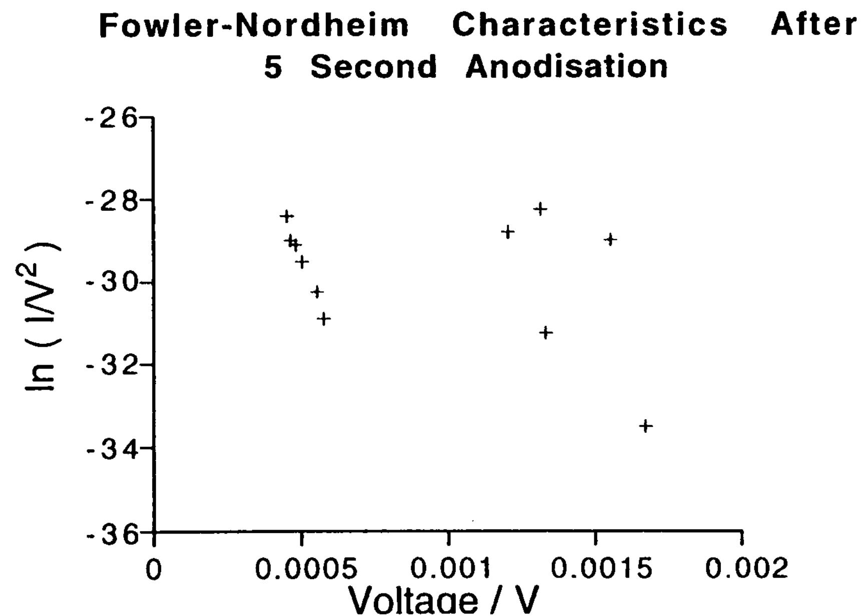
c) Silicon core protruding from surrounding porous silicon layer which has been damaged

d) Higher magnification image of silicon core
Note that surface of core, which was the interface between the porous silicon and the bulk silicon, is very rough.

Figure 8.12 - TEM image showing core structure of anodised p^+-type FIM tips







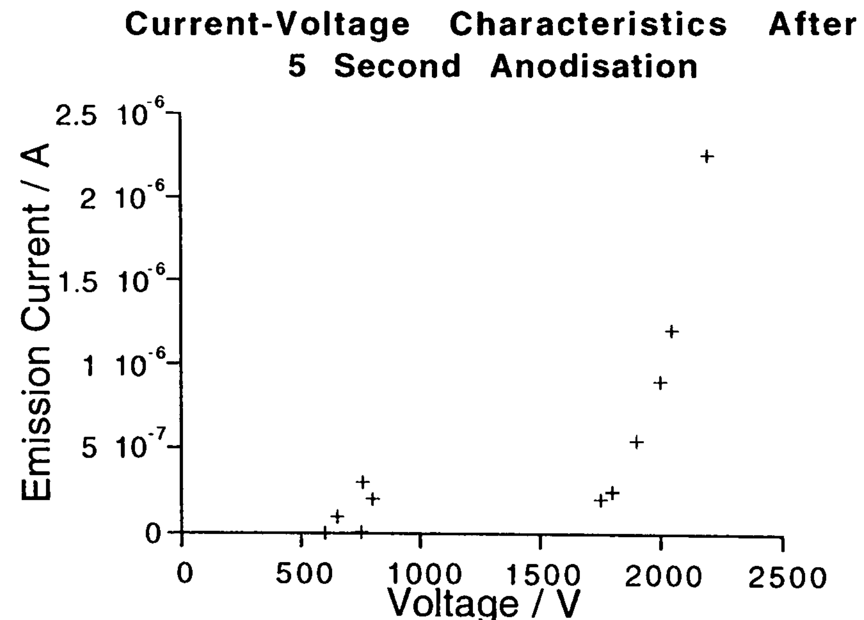
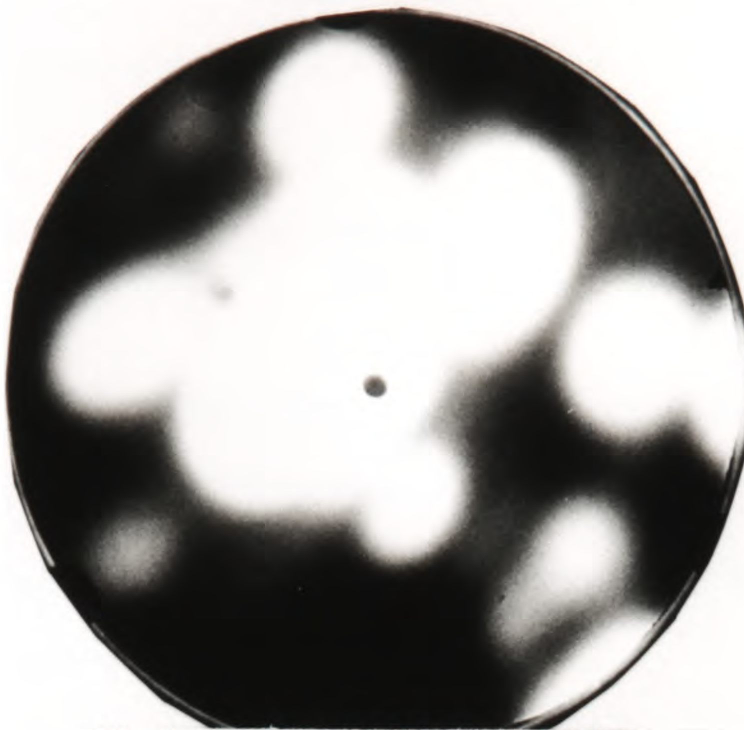
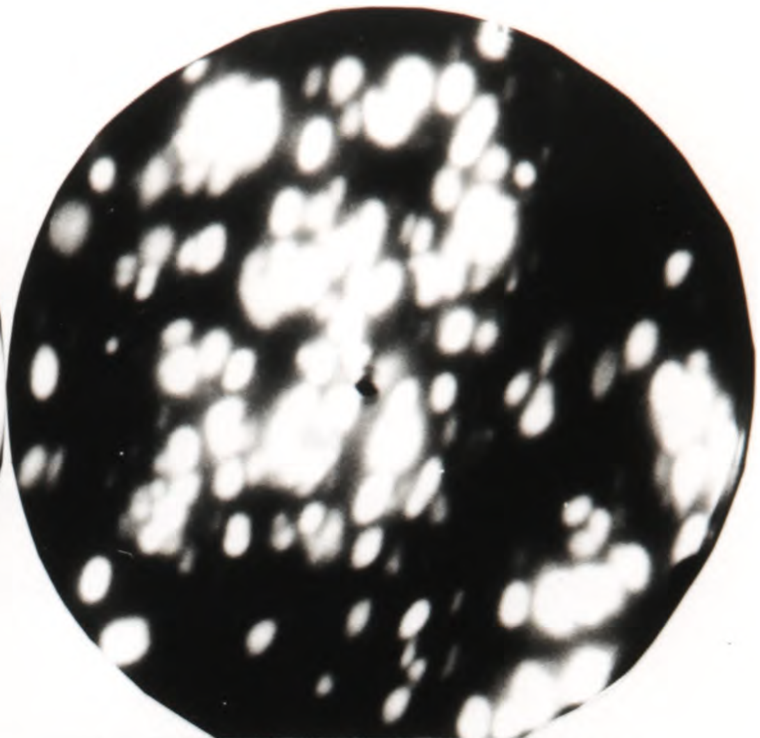


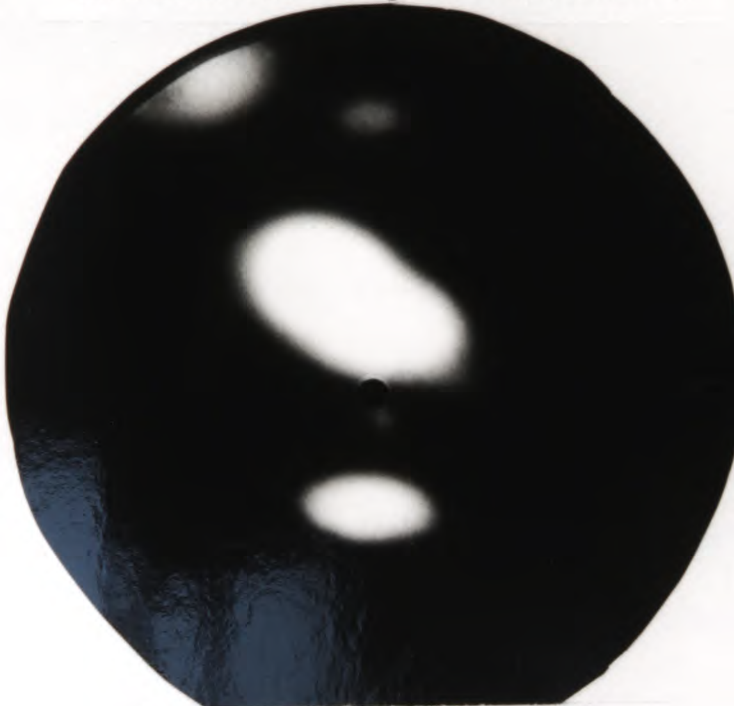
Figure 8.13 - Field Emission Before and After Anodisation for 5 Seconds (i.e. Formation of Thick Porous Silicon Layer on Tip Surface)
Field emission before anodisation produced a straight line Fowler-Nordheim plot. However, after anodisation, the Fowler-Nordheim plot was not a straight line and the emitter blew at low current (emission then only re-occurred at a much higher voltage).



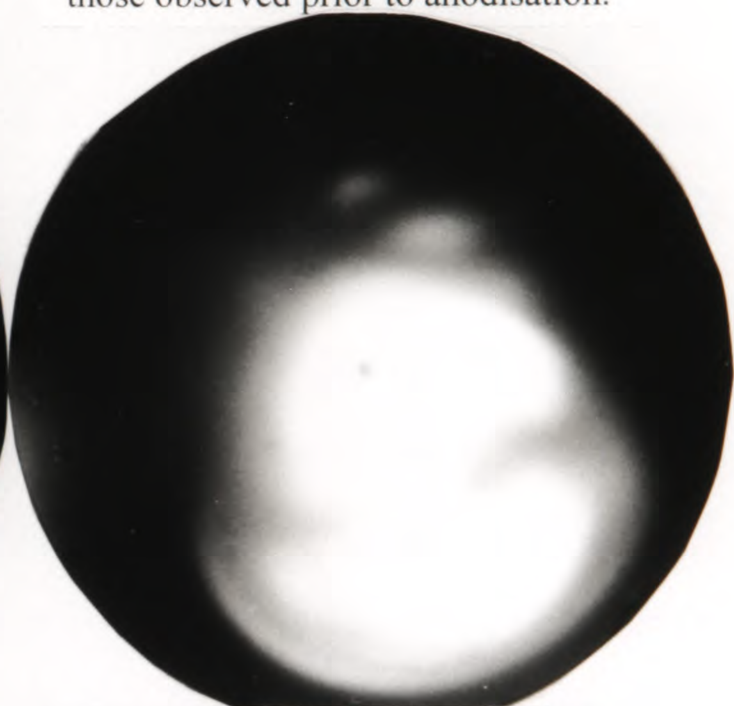
Tip 1 - FEM at 800V (ref:20/5/95)
0. 5 second anodisation
Note that the emission spots are larger than those observed prior to anodisation.



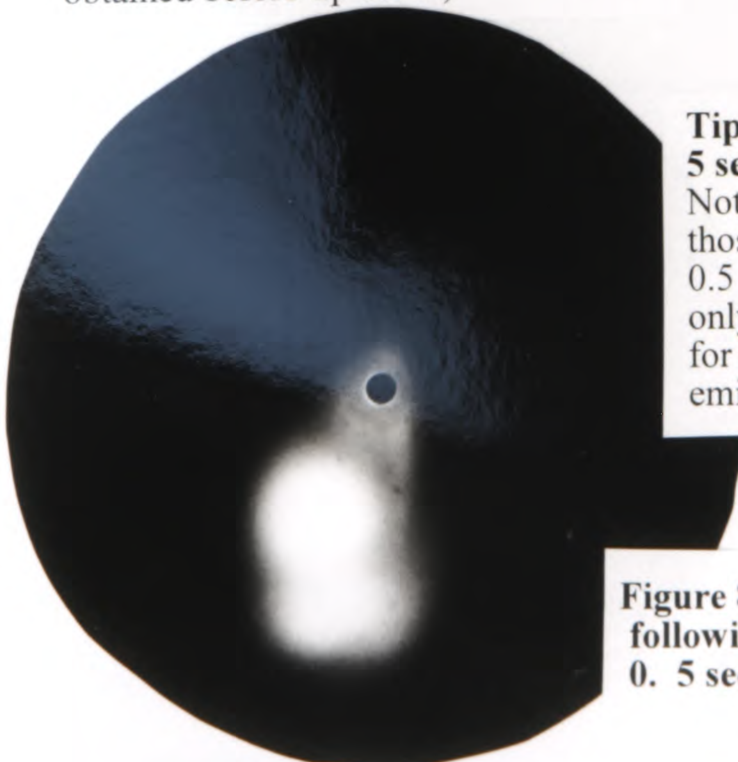
Tip 1 - FIM at 2.6kV (ref:20/5/95)
0. 5 second anodisation
Note that the FIM spots are larger than those observed prior to anodisation.



Tip 2 - FEM at 754V (ref:28/1/95)
0. 5 second anodisation
(Corresponding FIM image could not be obtained before tip blew.)

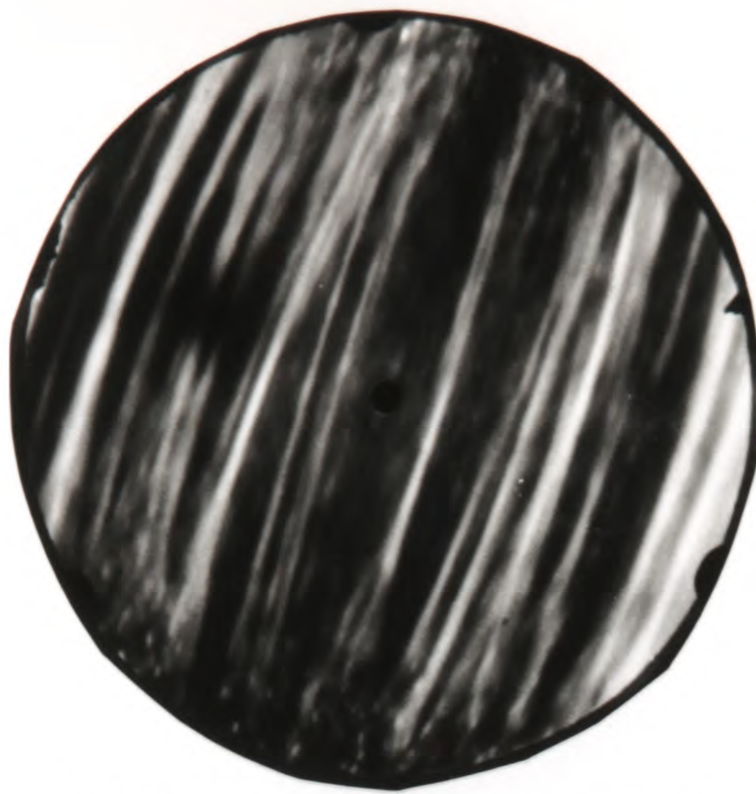


Tip 3 - FEM at 760V (ref: 16/3/95)
0. 5 second anodisation
(Corresponding FIM image could not be obtained before tip blew.)

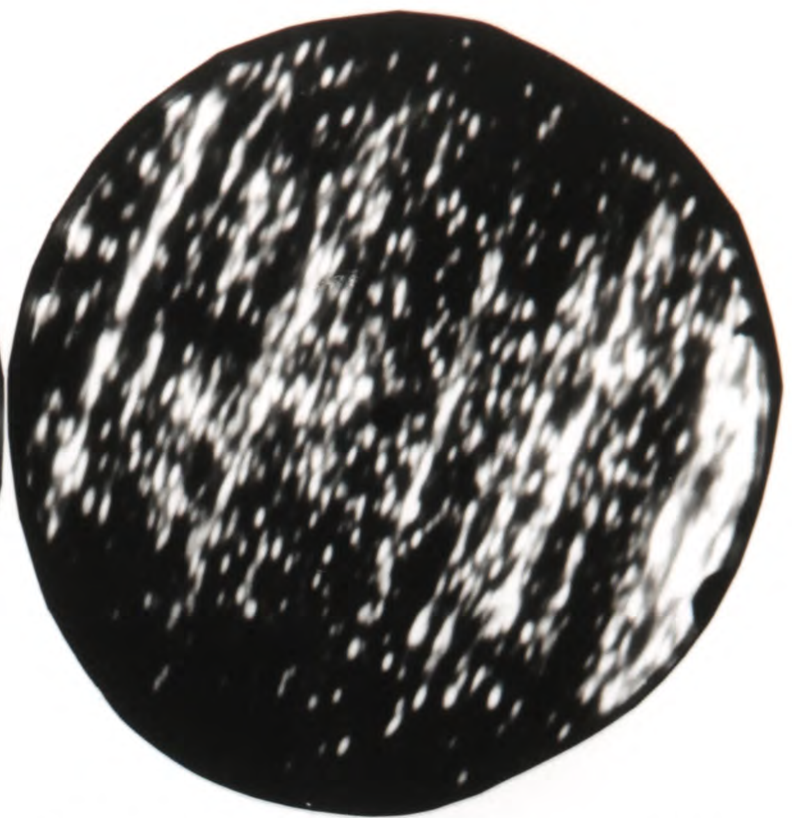


Tip 4 - FEM at 512V (ref: 20/10/94)
5 second anodisation
Note that spots appear to be similar in size to those obtained from tips anodised for only 0.5 seconds. However, tips anodised for 5 seconds only exhibited one spot, compared to tips anodised for only 0.5 seconds which exhibited several emission spots.

Figure 8.15 - Comparison of FIM and FEM images following anodisation of several tips anodised for 0. 5 seconds and for 5 seconds



a) FIM image following field evaporation to 11.23kV
Note the streaked image, indicating that the tip is very blade-shaped.



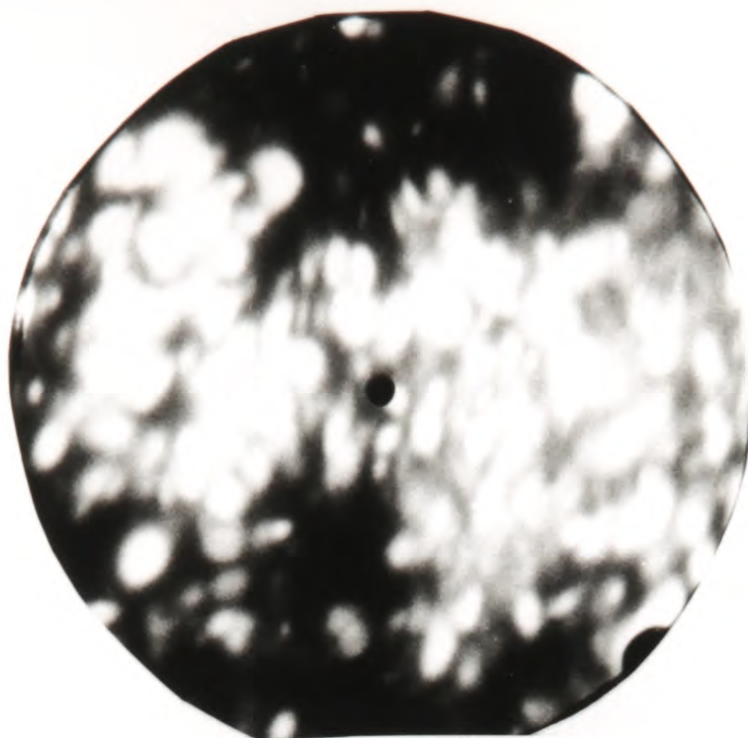
b) FIM image from same tip at 8.65kV
This image was taken after the voltage was reduced from 11.23kV.

c) FEM image from same tip at 1500V
This image was taken before a field emission run was carried out. Emission appears to be localised along blade.

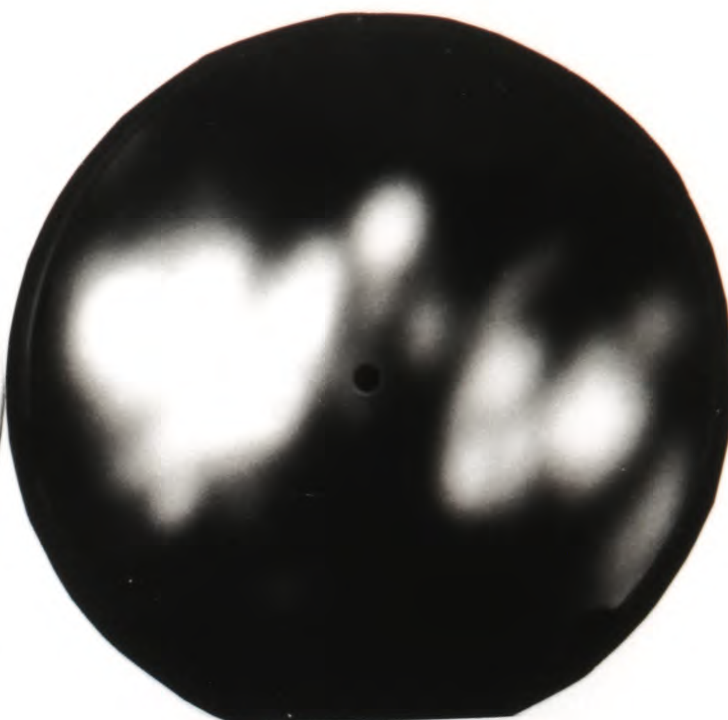
d) FEM image from same tip at 1508V
This image was taken after a field emission run was carried out to ~1μA. Note that FEM image is less bright following emission.

(Ideally, the tip used for these experiments would have been uniform and fully fogged out at 7.7kV. However, it was difficult to prevent the formation of blade-shaped tips.)

Figure 8.16 - Identification of surface fibrils as emission source - FIM and FEM images from plain silicon tip prior to anodisation
The tip shown in this figure was field evaporated to 11.23kV. This tip was used for the experiments described in Section 8.8, in order to identify the source of emission from anodised silicon tips. These FIM and FEM images show that this tip is asymmetric and blade-shaped. Figures 8.17 and 8.19 show FIM and FEM images from this tip, following anodisation and evaporation of nickel onto the tip surface respectively.

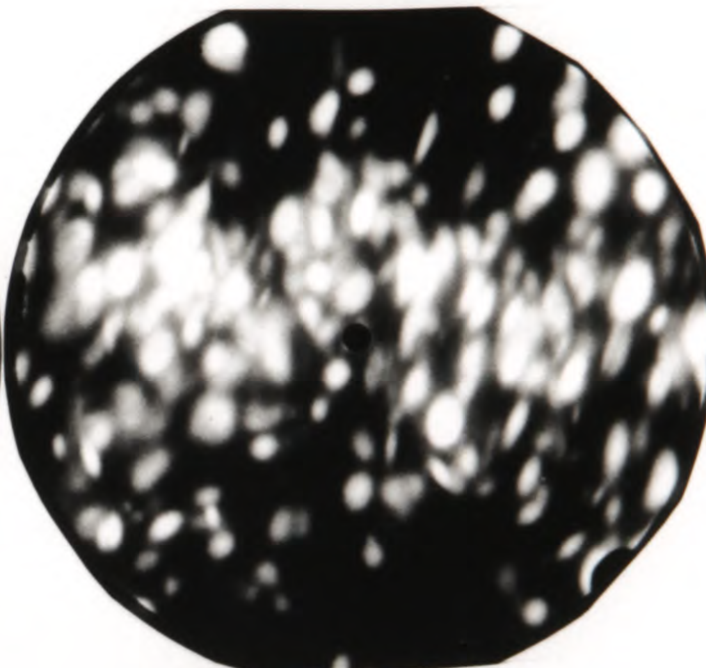


a) First FIM image at 4.13kV



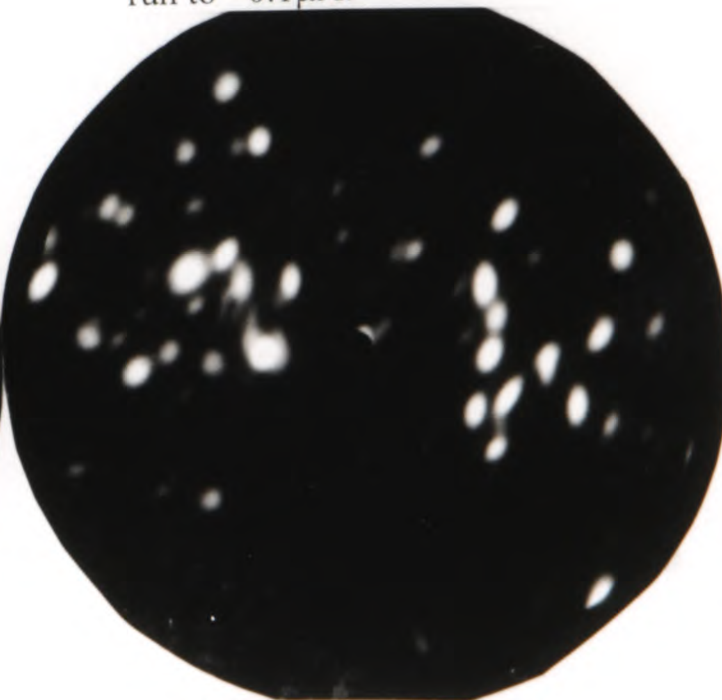
b) FEM image at 930V
Taken after FIM image

c) FEM image at 1068V
Voltage increased from 930V

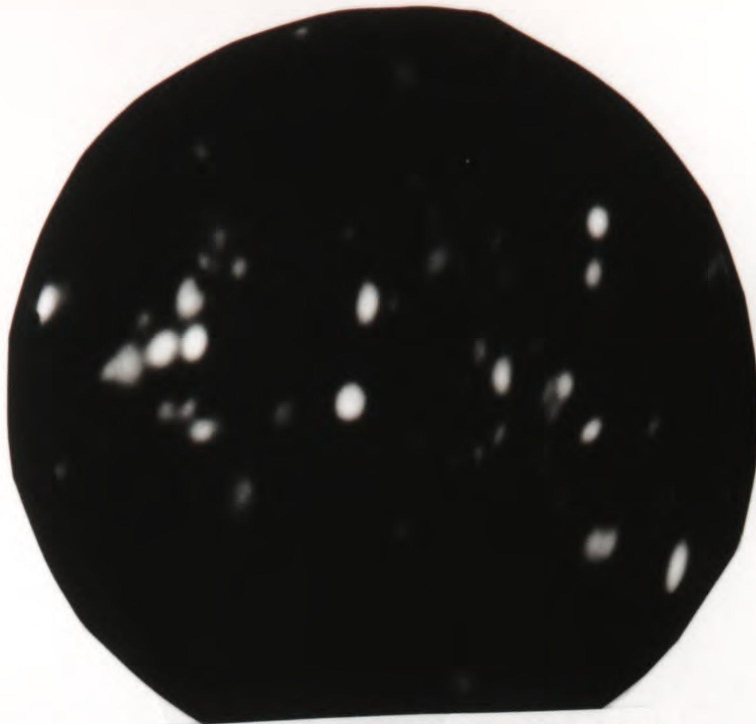


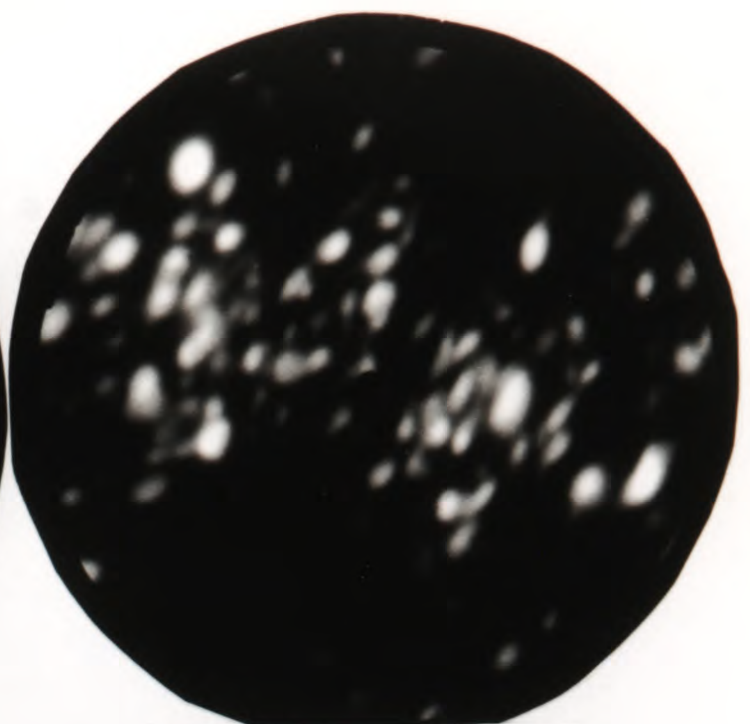
d) FIM image at 4.13kV
Image taken after emission run to ~0.1μA.

e) FEM image at 960V
Taken after d)



f) FIM image at 3.5kV
Taken after e)


a) First FIM image at 3.34kV


b) FIM image at 3.62kV

c) FEM image at 808V

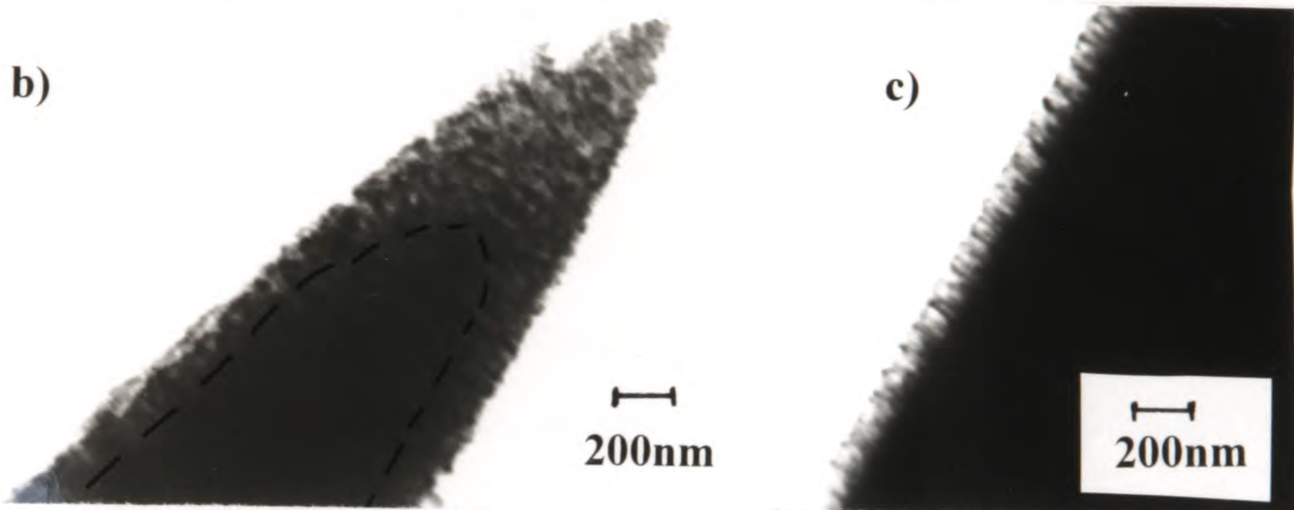
d) FEM image at 886V

e) FEM image at 748V
Following emission run to ~0.1μA

f) FEM image at 820V
Taken after voltage increased from e)

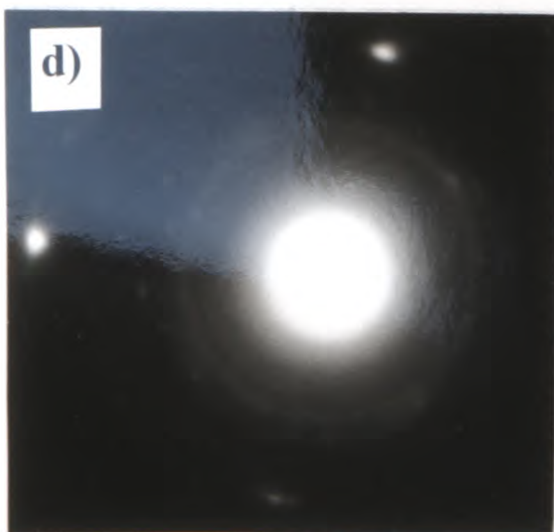
Figure 8.19 - Identification of surface fibrils as emission source - FIM and FEM image after evaporation of nickel onto anodised tip

a) Tip apex
Image shows that porous silicon layer is still present at the tip following anodisation, characterisation by FIM/FEM, evaporation of nickel and re-characterisation by FIM/FEM.
- Note that there is small nick on one side of the tip - it is believed that this was caused at the same time a flash occurred as the voltage was increased in order to obtain field emission.
- Also note that, although the tip appears to be quite sharp, the FIM/FEM images show that it is very blade-shaped. It is therefore believed that if the tip was turned through 90°, it would appear be ridge-shaped rather than point-like.



b) Core
The core is difficult to observe. However, the outline of the silicon core is marked in pen on this image, in order to demonstrate the core geometry. The porous silicon layer at the tip is ~1μm thick. This also shows that the nick in the porous silicon layer (believed to be caused by a flash as the field emission voltage was increased) did not expose the silicon core.

c) Porous Silicon Layer Thickness
This images shows the thickness of the porous silicon layer down the edges of the tip. The thickness of the porous silicon layer is ~100nm, which is much thinner than at the emitter tip.



d) Diffraction pattern
The diffraction pattern confirms that metal is present at the tip. Note the spots which are characteristic of a polycrystalline metal layer.

Figure 8.20 - TEM images of FIM tip following FIM/FEM characterisation after anodisation and nickel evaporation