

# Zero-Additional-Hardware Power Line Communication for DC-DC Converters

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**Abstract**—A Power Line Communication (PLC) solution to provide a data link between two or more DC-DC power converters is proposed. The approach does not require additional analog circuitry or high-sample-rate analog-to-digital converters to be added on top of the original system. A modulation and signal injection method for the transmitter, and a sampling and demodulation strategy for the receiver are developed. The PLC frequency band is placed between the control loop cut-off frequency and the power electronics circuit cut-off frequency, in a region that we identify as the ‘intermediate frequency band’. The transmitter modulates the converter voltage or current output by injecting perturbations into the control loop at the input to the PWM unit. To tolerate unsynchronized transmitter and receiver clocks, a virtual zero-crossing location algorithm is combined with long/short pulse identification to achieve demodulation at the receiver. The solution is verified experimentally and achieves reliable bidirectional PLC communication at 2 kbps with an 8 kHz receiver sampling frequency.

**Index Terms**—Zero-additional-hardware PLC, Virtual zero-crossing, Long/short pulses identification

## I. INTRODUCTION

**P**OWER electronic converters and communication links are key elements of microgrids, smart grids and the Internet of Things (IoT) [1], [2]. Power electronic converters underpin low-level operation (e.g. power transmission, stability) and communication underpins high-level system operation (e.g. dispatch, balancing, metering) [3]. Conventional communication techniques, such as field bus or CAN bus, need extra cables beyond the power cable itself and so imply additional installation cost. Wireless communication, such as Zigbee and LoRa, avoid extra cables, but wireless solutions are vulnerable to interference and congestion, and require an antenna. In contrast, Power Line Communication (PLC) [4] uses the electrical power cable as the channel for data transmission and is therefore potentially an attractive low-cost solution. However, conventional PLC solutions need transmitter and receiver circuitries to achieve modulation and demodulation which increases system complexity and cost.

The overlap between the operating principles of power converter control and PLC [5] has been investigated previously. Papers [6]–[9] modulate the converter by changing the switching frequency or phase to create the PLC signal (Frequency

or Phase Shift Keying (FSK or PSK)). The authors of [6] study this method applied to a half-bridge synchronous buck converter, and [7] proposes phase shift-based modulation for full-bridge isolated converters. Both methods take advantage of an imperfect electromagnetic interference (EMI) filter to measure DC bus voltage ripple, which means that a better EMI filter could cause communication failures. To improve EMI performance, spread spectrum based PLC is proposed in [8]. Receivers for all the above methods need either bandpass op-amp filters or other additional circuits to filter and amplify signals. A high-frequency ADC is needed in all these works since the data are embedded in switching frequency ripple (the sampling frequency should be at least two times the switching frequency according to the Nyquist theorem). An exception is [9] where information is embedded in weakly-damped oscillations generated at the input bus during switching commutations. To avoid a high sampling frequency for demodulation, alias effects are carefully exploited. However, several filters are required at the receiver side, which represent additional system complexity. Recently, [10] presented an analysis of different data coding methods to improve the communication bit rate and reliability. In most cases, the Discrete Fourier transform (DFT) is used in the demodulation procedure which is likely to represent a high computational load compared to standard PID controllers used for the control of power electronics, especially if it must be executed at a high sampling frequency.

A typical application of converter-based PLC is for monitoring photovoltaic (PV) systems [11]–[14]. The transmitters in [11]–[13] include additional circuits to couple with the main power circuitry, either in series or parallel with the DC bus. In contrast, [14] proposes embedding perturbations in the reference of the control loop of a buck converter such that additional transmitter circuitry is not required. In all of [11]–[14], the receiver requires additional circuits such as coupling transformers and/or amplifiers, and high sample rate ADCs. Although not strictly PLC (as there are no lines), wireless power transfer and data transfer can be combined by taking advantage of the high-frequency harmonics in the trapezoidal form generated by phase-shift control of full-bridges [15], however, additional analog circuits are still needed in the receiver for demodulation.

The PLC solution presented in this paper requires no extra circuits at the transmitter or receiver (hence the term ‘zero-additional-hardware PLC’); it is implemented purely in software on top of the existing control loops in the transmitter and receiver. In addition, the solution needs much lower receiver ADC sampling rates compared to many previous works, and

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No new data were created during the study.

produces low additional computational load as it does not use the DFT. The main contributions in this paper are: 1) The frequency band between the control and output filter cut-off frequencies is shown to be suitable for relatively low-frequency PLC; 2) a complete PLC solution is demonstrated including modulation, signal injection, data framing, sampling and demodulation strategies; 3) experimental results showing reliable communication between two DC-DC converters at 2 kbps are presented. A comparison between the proposed PLC solution and similar literature is given in Table I ('Add. HW' stands for 'additional hardware required').

TABLE I: Comparison with literature

Reference	Bit rate	Sample rate	Add. HW	Uses DFT
[6]	2 kbps	500 kHz	yes	yes
[7]	5 kbps	10 kHz	yes	yes
[8]	6.67 kbps	400 kHz	yes	yes
[9]	1.5 kbps	200 kHz	yes	no
[14]	2 kbps	100 kHz	yes	yes
This work	2 kbps	8 kHz	no	no

This paper is organized as follows. Section II introduces the PLC channel, which is shown to exist in most types of DC-DC converters. The transmitter modulation and receiver demodulation strategies are presented in Section III and Section IV respectively. Experimental results are shown in Section V and applicability is discussed in Section VI-A. Section VII concludes the paper.

## II. PLC SYSTEM MODELLING

The PLC system consists of at least two DC-DC power converters. These can be different types, such as buck, boost, Dual Active Bridge (DAB) or Dual Active Half Bridge (DAHb) converters. In this work, one converter is assumed to be under voltage control and all others under current control. Two DAHB converters are illustrated in Fig. 1, one acting as a transmitter, another as a receiver. In this example, Fig. 1 illustrates one possible combination, which is that the transmitter is under voltage control to maintain terminal voltage  $V^{TX}$  and the receiver uses a current controller to regulate the current flowing between the transmitter and the receiver,  $I^{TX} = I^{RX}$ . Either converter can be the transmitter or receiver, the roles are not determined by the choice of voltage or current controller.

Five frequencies can be identified in digital control systems for power converters: the switching frequency  $f_{sw}$ , the sampling frequency  $f_s$ , the control loop execution frequency  $f_c$ , the cut-off frequency of the transfer function of the power electronic circuit and filter  $f_{pef}$ , and the closed-loop control bandwidth  $f_{ctrl}$  [16], [17]. In practice, the sampling frequency is often set equal to the switching frequency by configuring the same timer and interrupt on the microcontroller, however not all the sampled data are necessarily used for calculating control outputs due to microcontroller speed limitations (the full sampled data may be used only for fast-acting protection). The controller operates on sampled data at the control loop execution frequency. The switching frequency is typically an

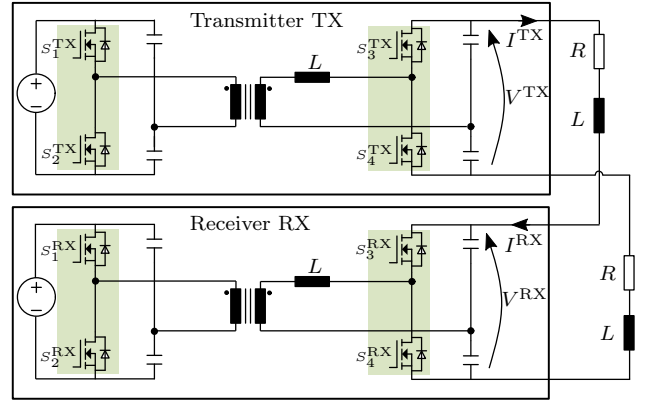


Fig. 1: An example PLC system with one transmitter and receiver.

integer multiple of control loop execution frequency to guarantee a constant number of switching periods per control output sample [18]. The control bandwidth is lower than the control loop execution frequency and the open-loop cut-off frequency from control output to system output  $f_{pef}$  is normally higher than the control bandwidth for simple converters (although this may not be the case in high-performance designs that implement active damping of the filter). In this paper, the relationship for these five frequencies is assumed to be

$$f_{sw} \geq f_s \geq f_c > f_{pef} > f_{ctrl}. \quad (1)$$

A general control structure for power converters is given in Fig. 2, in which frequencies mentioned above are labelled on the corresponding parts.  $G_C(s)$  represents the controller transfer function,  $G_{pef}(s)$  represents the transfer function of the power electronic circuit and filter.  $V^*$ ,  $V$  and  $\bar{V}$  represent voltage reference, actual voltage and sampled quantized voltage respectively.

### A. Bandwidth analysis for the single converter

Fig. 3 qualitatively illustrates frequency-gain curves according to the structure given in Fig. 2. The left-most is the closed-loop amplitude response from system reference ① to filtered system output ④ whose transfer function is defined as  $G_{sys}(s)$  (the reference and output may be voltage or current signals, depending on controller type). The right-most is the amplitude response of the power electronic circuit and filter transfer function ③→④ (open-loop). The power electronics with filter bandwidth is higher than the closed-loop control bandwidth, which leaves a 'bandwidth gap' which we define as the Intermediate Frequency Band (IFB) labelled in red. Intuitively, the closed loop-gain from the perturbation ② added at the control output to the filtered system output ④ will be largest in the IFB, as neither the control loop nor the output filter will attenuate signals with frequencies in this range. The IFB transfer function (closed-loop) ②→④ is defined as  $G_{IFB}(s)$ . The IFB exists in most DC-DC power converters under voltage and current control modes.

Three example circuits are used to explore the features of the IFB: the buck, boost, and DAHB converters with

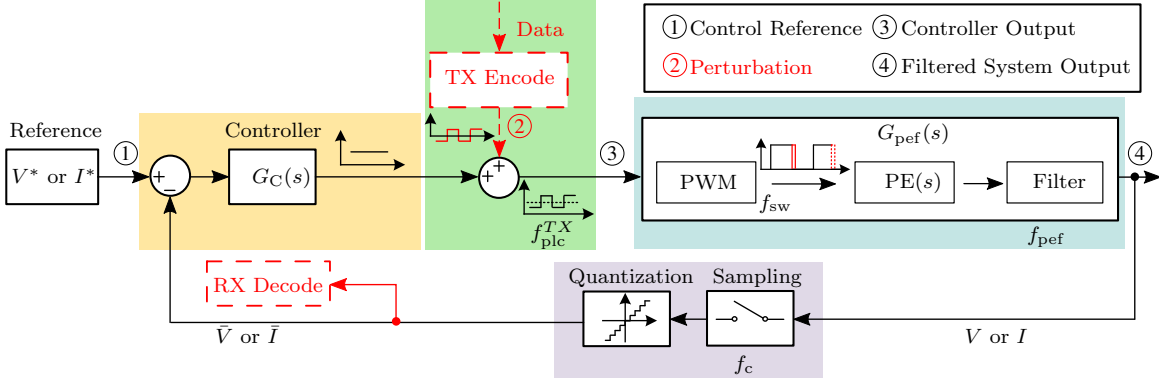


Fig. 2: Fundamental closed-loop system structure for DC-DC converters.

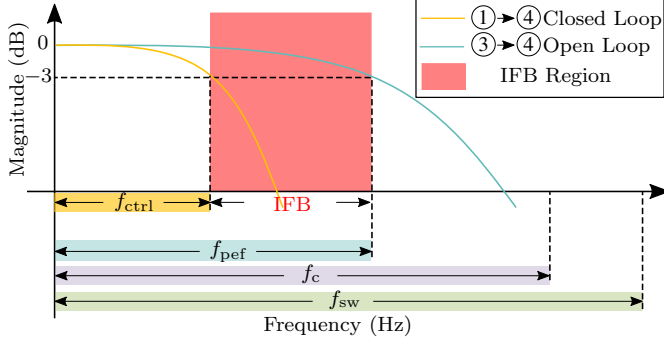


Fig. 3: Bandwidth comparison.

TABLE II: Parameters for three types of converters

	Buck	Boost	DAHB
Source voltage	240 V	60 V	12 V
Filter/link inductor	2.3 mH	0.59 mH	15.8 uH
Output capacitor	0.33 uF	6.5 uF	3.6 uF
Switching frequency	64 kHz		
Nominal output voltage	120 V		
Output voltage ripple	2 %		
Nominal output current	3 A		
Output current ripple	20 %		

the parameters in Table II. To allow direct comparison, the nominal output voltage for all three converters is  $V_{op} = 120$  V for the voltage-controlled converter, and  $I_{op} = 3$  A output current for the current-controlled converter. All other design parameters are equal and the inductor and capacitor values are chosen according to the switching frequency, as shown in Table II.

Small signal averaged models for buck [19], boost [20] and DAHB [21] converters are analysed in both voltage and current control modes. The voltage controlled buck and boost converters use voltage-current double-loop PI controllers. The current controlled buck and boost converters use a single-loop PI controller. The DAHB converter uses a single-loop phase shift controller for voltage and current control, with a fixed 0.5

duty cycle on both primary and secondary sides. A controller design procedure similar to that given in [17] is followed.

Fig. 4 illustrates the key characteristics of the converter transfer functions  $G_{sys}$  and  $G_{IFB}$ . The left y-axis gives  $|G_{sys}(s)|$  i.e., a voltage-to-voltage or current-to-current gain. The right y-axis gives the normalized IFB gain:

$$A_{IFB}(s) = \begin{cases} \frac{\Delta D(s)|G_{IFB}(s)|}{V_{op}}, & \text{voltage control} \\ \frac{\Delta D(s)|G_{IFB}(s)|}{I_{op}}, & \text{current control} \end{cases} \quad (2)$$

where  $\Delta D(s)$  is the perturbation injected into the controller output (2). In this analysis, the perturbation magnitude is 10% of the nominal control output that achieves  $V_{op}$  or  $I_{op}$ .

When under voltage control or current control, it is clear that neither the closed-loop controller nor the power electronics with filter provides significant attenuation of perturbations injected at frequencies in the IFB. Even though different converters give varying gains in the IFB, it is clear that the IFB exists in different types of converters with voltage and current controllers subject to standard power converter control loop design practices. This suggests that using the IFB for PLC is applicable to many converter types.

### B. Bandwidth analysis for two converters

The frequency response of two interconnected converters (e.g., Fig. 1) will differ from that of a single converter. Either the shared voltage or the current can be chosen as the information carrier. In Fig. 5, the left y-axis gives the response from perturbation injection at the transmitter to the voltage measured at the receiver  $V^{RX}$ , and the right y-axis gives response from perturbation to the current measured at the receiver. Both y-axes give the absolute response magnitudes about a 120 V, 3 A operating point.

From these figures it can be seen that, in the IFB, the injection of a relatively small perturbation at the transmitter will generate a strong signal at the receiver. Depending on the choice of converter circuit and design, the voltage or current signal may be stronger; the decision of which to use will therefore vary from application to application. In the rest of this paper we sense the voltage signal at the receiver.

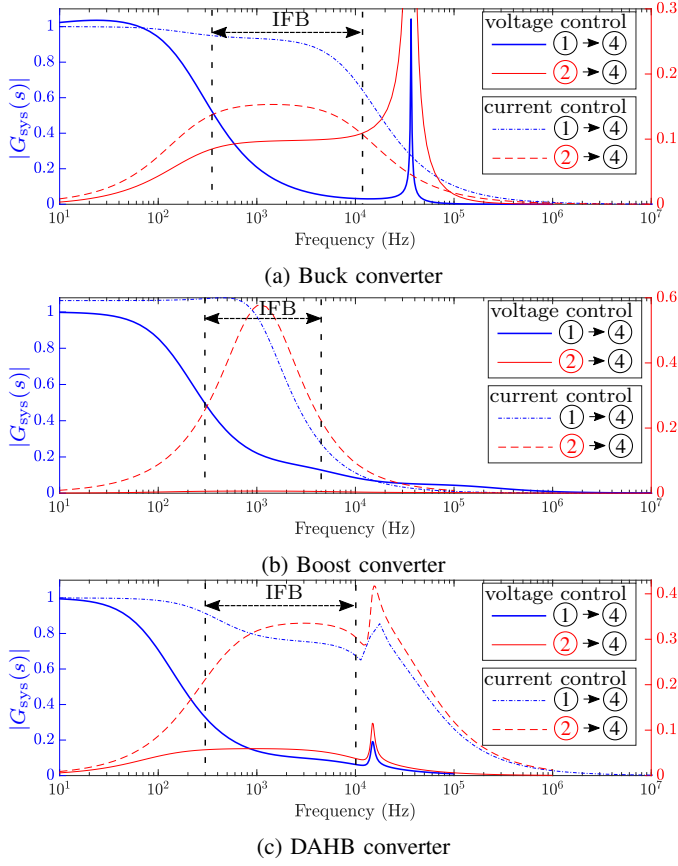


Fig. 4: Normalized frequency response of a single converter.

### C. PLC approach

The central idea is that a data sequence is encoded using a PLC clock at  $f_{\text{plc}}^{\text{TX}}$  which lies within the IFB. The sequence is used to perturb the control output of the transmitter ② as illustrated in Fig. 2. Since the filter cut-off frequency is higher than the PLC clock frequency, the perturbations will not be filtered out. Also, since the PLC clock frequency is higher than the control bandwidth, the controller does not ‘see’ (and therefore cannot act to suppress) the perturbations in the converter output. For the receiver, the sampling frequency must be at least two times the PLC clock frequency according to the Nyquist theorem. The maximum bit rate of the proposed method is limited by the cut-off frequency of the low pass filter at the converter output, and so converters that operate at higher switching frequencies will tend to achieve higher bit rate.

## III. TRANSMITTER MODULATION

In this section, we introduce the PLC approach using the DAHB converter pair shown in Fig. 1. The analysis uses the parameters in Tables II and III. The transmitter is under voltage control acting as a voltage source, and the receiver is under current control acting as a current sink. The output voltage or current is controlled by varying the phase shift between primary and secondary sides within the range  $-90^\circ$  to  $90^\circ$  [21]. The PLC modulation signal is referred as a ‘perturbation

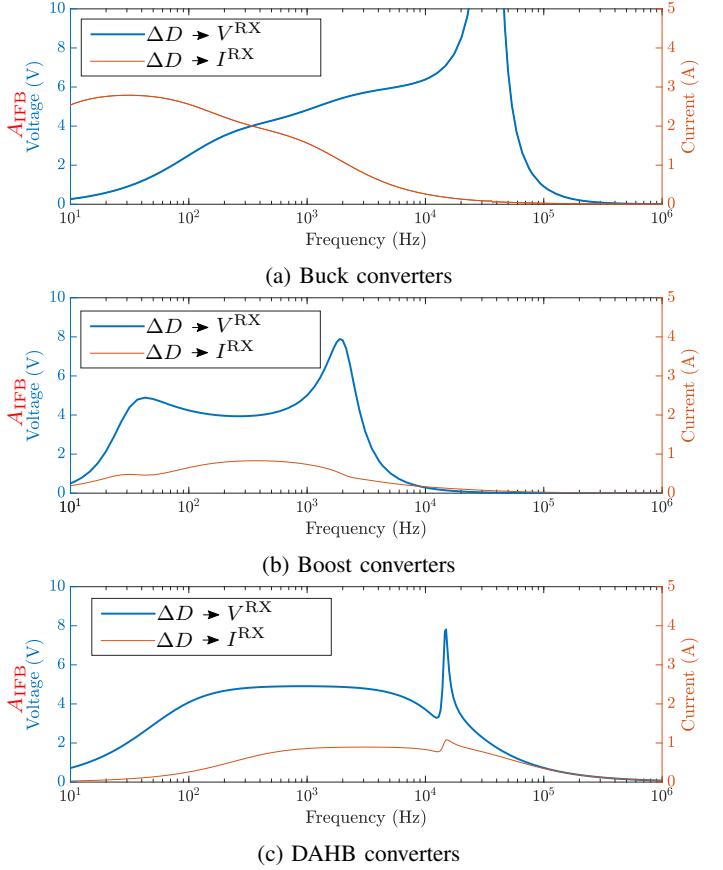


Fig. 5: IFB response of two interconnected converters under voltage or current control.

sequence’ that is added to the transmitter voltage controller phase shift output.

### A. Manchester encoding

The type of Manchester Encoding (ME) [22] used here is an XOR logic operation between data and clock, as defined by the IEEE 802.3 standard. This generates a low-to-high transition for bit 1, or a high-to-low transition for bit 0. Importantly, ME data has zero DC average over any number of data bits and so the injected perturbations will not cause any drift away from the controller set point (i.e., the injected perturbations will cause only high-frequency ripple in the output). Fig. 7 shows the power spectral density of random data encoded using ME. The power is zero at DC, low below  $0.2R$ , maximum at approximately  $0.75R$ , and low above  $1.5R$ . This implies that good communication performance can be expected so long as the bandwidth of the IFB is roughly  $2R$ .

As illustrated in Fig. 6, there are four basic bit combinations (10, 01, 11, 00), in which  $f_{\text{plc}}^{\text{TX}}$  is the ME clock frequency, which is equal to the data bit rate  $R$ . Any longer data consists of only these four combinations. Coded data of 10 or 01 generates long pulses as illustrated in Figs. 6a and 6b. Coded data of 11 and 00 generate short pulses as illustrated in Fig. 6c and 6d. The coded data is the reference for the generation of perturbation sequences.

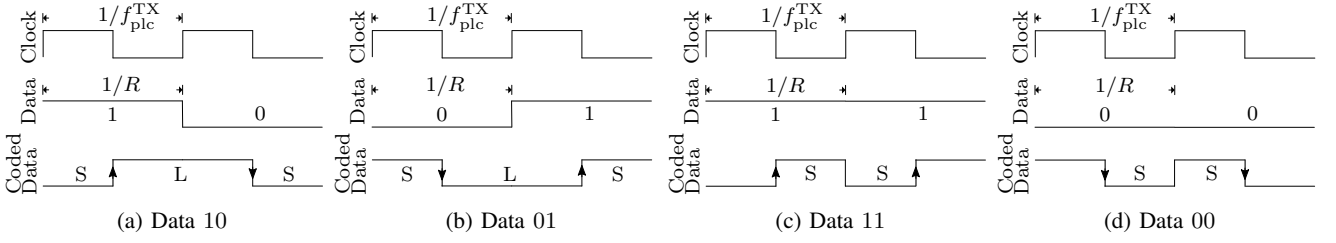


Fig. 6: Transmitter sequences for the four basic bit combinations. S = short pulse, L = long pulse.

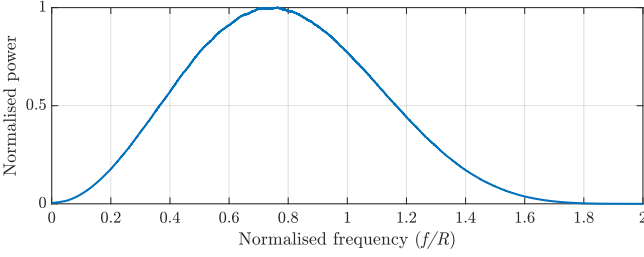


Fig. 7: ME power density spectrum.

### B. Manchester encoding clock frequency

The maximum ME clock frequency is constrained by three conditions: 1) it must lie in the IFB, 2) it cannot be higher than the transmitter switching frequency, and 3) it must be low enough that the receiver will reliably sample at least one unambiguous high or low valued during short pulses.

In most applications it is likely that the third constraint will be the more severe, unless a very fast ADC is available at the receiver. Assuming the transmitter and receiver hardware is identical, this constraint means that the highest possible ME clock frequency (and so bit rate) is one-quarter of the sample rate (the reasoning behind this is discussed in more details in Section IV-A and IV-B). For the experimental system with parameters listed in Table III, the ME clock frequency is set to this maximum one-quarter rate (2 kHz), and so the bit rate is 2 kbps.

### C. Perturbation sequence

The data are encoded in the edges of the signal, and so it is important to form sharp step changes in the output voltage and maintain the voltage between edges constant. In other words, the objective is to produce a voltage waveform at the receiver side that is as-close-as-possible to the coded data. To achieve this, the perturbation sequence is constructed from single-sample perturbations that form the pulse edges (called ‘edge perturbations’), followed by several smaller perturbations to hold the pulse constant (called ‘hold perturbations’). This can be understood by noting that the transfer function of a DC-DC converter is invariably low-pass and the edge perturbations act as impulses that drive a fast rate-of-change of the output.

In the experimental system, the edge perturbations were chosen to be  $\pm 14$  Least Significant Bits (LSBs) of the microcontroller phase shift modulator, corresponding to  $\pm 3.22^\circ$ . The

hold perturbations were chosen to be  $\pm 4$  LSBs, corresponding to  $\pm 0.92^\circ$ . The perturbation sequence and resulting receiver voltage for data 0x5F are illustrated in Fig. 8a as an example. The length of the pulses in terms of the control period  $T_c = 1/f_c$  are marked. As a comparison, Fig. 8b shows a receiver voltage generated with constant perturbations (i.e., no difference between the edge sample and the remaining samples). The waveform is triangular without obvious sharp step changes or periods of constant value. In contrast, Fig. 8a shows that the receiver samples contain obvious short and long pulses that the demodulator should be able to identify easily.

### D. Data framing

A data frame consists of three parts: One start bit, up to 30 data bytes and two Cyclic Redundancy Check (CRC) bytes. The start bit is 1 which causes a sharp change from low to high, therefore allowing the receiver to recognize the start of data transmission.

## IV. RECEIVER DEMODULATION

A receiver demodulation and decoding strategy composed of two parts is proposed: 1) a method to measure pulse widths despite unsynchronized transmitter and receiver clocks and the limited signal slew rate of the received voltage, and 2) a method to detect the framing of data by distinguishing the start and end of a transmission from background fluctuations and noise. Fig. 11d illustrates the complete receiver process to record, manipulate and decode the data. Details of each step are given in the following subsections.

### A. Unsynchronized transmitter and receiver clocks

For microcontrollers using a low-cost RC clock source, the clock matching between transmitter and receiver can be expected to be within 10% such that

$$0.9 < \frac{f_c^{RX}}{f_c^{TX}} < 1.1. \quad (3)$$

Higher-cost quartz-crystal based clock sources are often accurate within a few parts per million. Since there will always be some non-zero frequency difference and there is no clock synchronization mechanism between the transmitter and the receiver, the relative phase of the clock sources will unavoidably drift over time. For the demodulation scheme to be robust, it must cope with this drift.

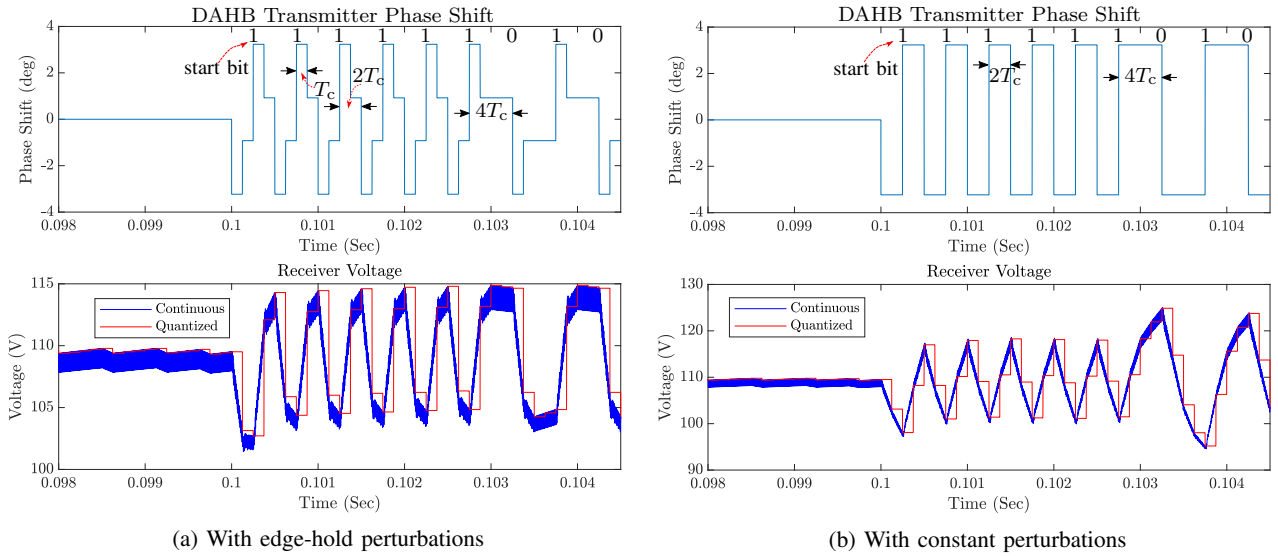


Fig. 9 illustrates the receiver sampled data (dots) for matched and mismatched transmitter and receiver clocks when the received voltage waveform is ideal (i.e., has perfectly sharp edges). For matched clocks, as illustrated in Fig. 9a, the controller will reliably observe two samples per short pulse and four samples per long pulse. In this case, decoding is trivial. In contrast, in Fig. 9b, when the receiver clock is slow, the receiver sometimes observes one sample per short pulse and four samples per long pulse. When the receiver clock is fast, as illustrated in Fig. 9c, the receiver sometimes observes five samples per long pulse and two samples per short pulse. Thus, if the receiver does not know whether its clock is fast or slow, it cannot distinguish reliably between long and short pulses merely by counting samples.

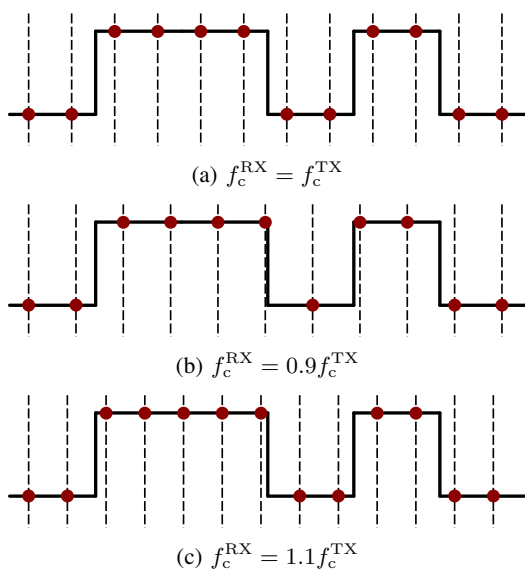


Fig. 9: Sharp-edged receiver waveforms for different  $f_c^{\text{RX}}$ .

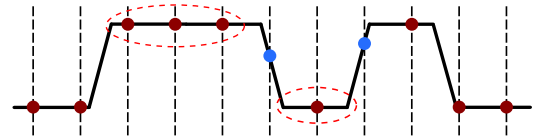


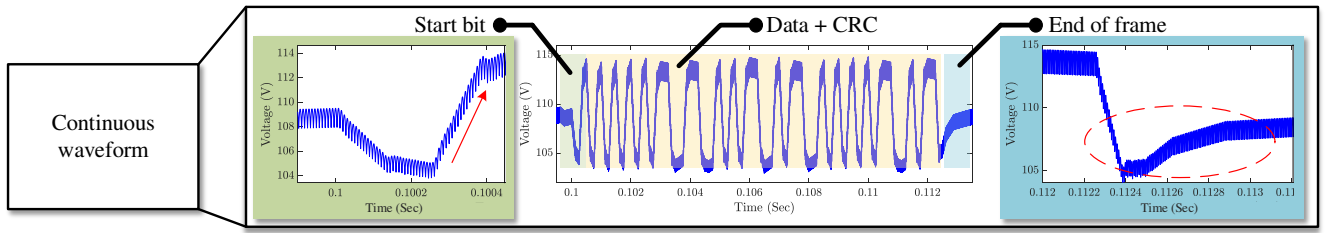
Fig. 10: Limited slew-rate receiver waveform for  $f_c^{\text{RX}} = 0.9f_c^{\text{TX}}$ .

### B. Limited received signal slew rate

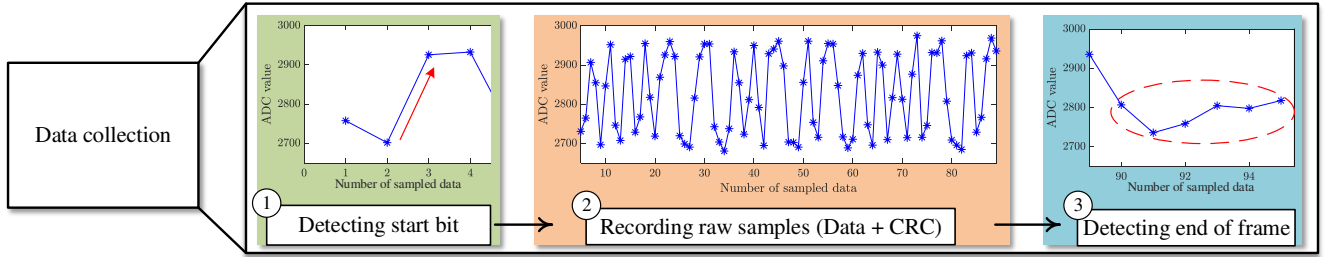
In practice, because of the low-pass effect of the transmission channel, the voltage measured by the receiver does not display ideal sharp edges (the slew rate is limited). This means that some of the receiver samples will be ambiguous (neither clearly high nor low) making simple counting of the high/low samples unreliable in practice. This effect is illustrated in Fig. 10, where the blue dots are not clearly high or low. This makes decoding more challenging. The solution is to use the sampled data to estimate the instant of zero-crossing of the receiver voltage. Here, ‘zero’ is taken to be the moving average value of the signal over several data bits (an average over 9 samples was used in the experimental system). Once the timing of the zero-crossings are established, the true length of pulses can be estimated. In general, this will be a fractional number of sample periods. A simple rule can then be used for decoding pulse lengths: if the number of samples between two zero-crossings is greater than three sample periods then the pulse is identified as long (L), otherwise it is short (S). This process is called Zero-Crossing Location (ZCL). Fig. 11c shows ZCL applied to an example sample stream; here the blue stars are the receiver samples and the red squares are the zero-crossings.

ZCL requires at least one receiver sample to measure unambiguously high or low during a short pulse, despite unsynchronised clocks and limited slew rate. This explains why the max ME clock can be at most one quarter of the receiver sample frequency.

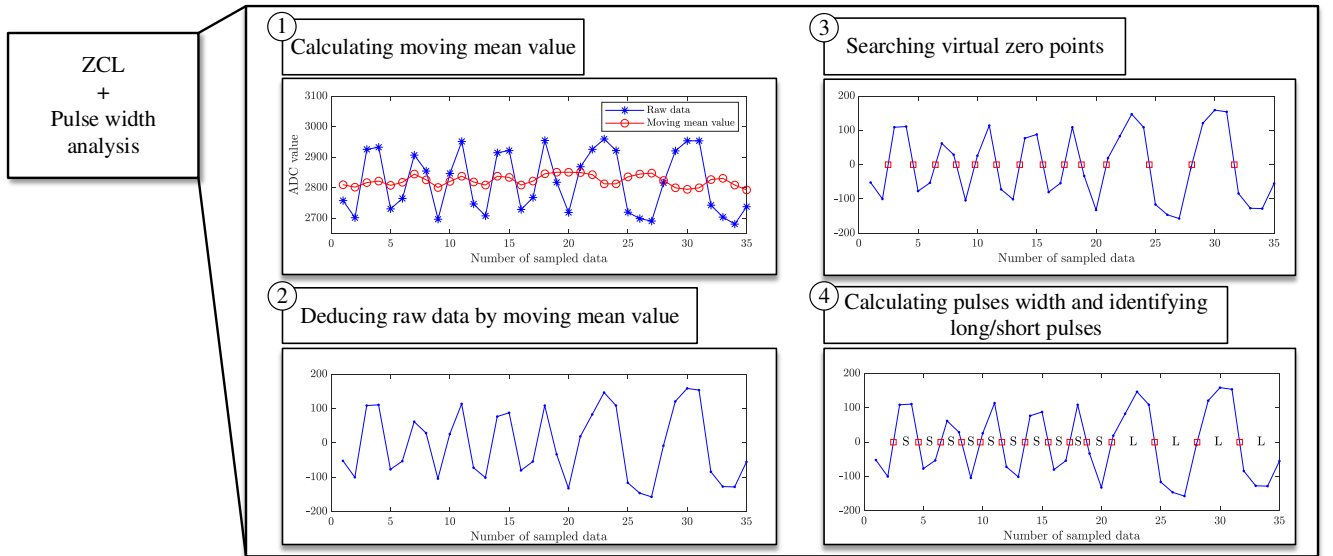




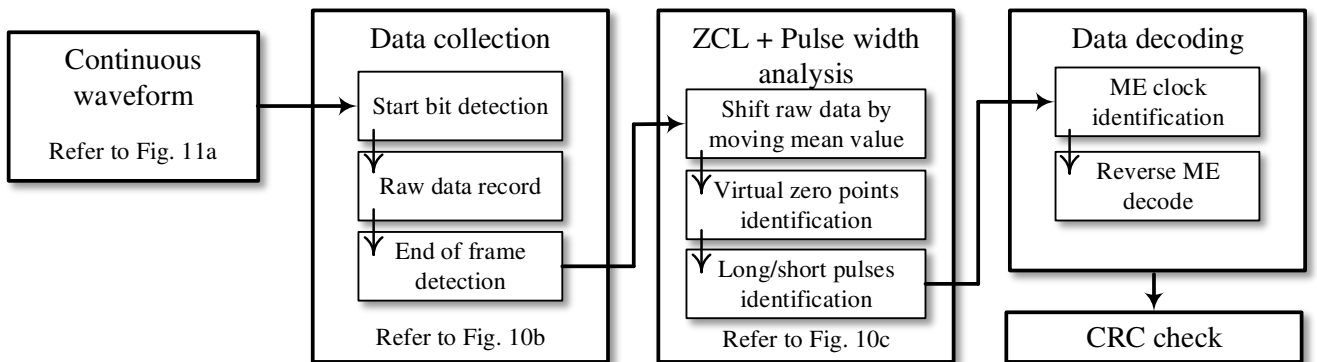
(a) Continuous waveform



(b) Data collection with 10% slow receiver clock



(c) ZCL algorithm and long/short pulses identification for the data part



(d) Complete flow chart

Fig. 11: Demonstration about receiver demodulation procedures: assuming receiver clock is 10% slower than transmitter and taking data 0x5F as an example.

### C. Data framing

The ZCL algorithm implemented in this paper is an ‘offline’ process. It operates on a buffer containing raw sample data for one frame. Therefore, it is necessary to accurately detect the start and end of a frame in order to start and stop the recording of data to the buffer, and then trigger the ZCL algorithm. This is a relatively simple process: the transmitter inserts a start-bit into the frame and the receiver detects edges using a simple discrete-difference calculation

$$\begin{aligned} \text{positive-going edge: } x_k - x_{k-1} &> x_t \\ \text{negative-going edge: } x_k - x_{k-1} &< -x_t \end{aligned} \quad (4)$$

where  $x_t > 0$ . Assuming the start bit is 1, there will be a positive-going edge at the beginning of each data frame. Therefore the receiver starts recording samples to the buffer on detection of the first positive-going edge. To detect the end of a frame the results of Section IV-A are exploited: the maximum length of a pulse that can ever be observed in a valid data stream is five samples, and so recording six samples without observing a positive- or negative-going edge implies that the data transmission has ceased, in which case the receiver will stop recording samples to the buffer and execute the ZCL algorithm on the contents of the buffer. The start bit detection and end of frame detection are illustrated in Fig. 11b. The continuous waveform (from which the sampled data is taken) is given in Fig. 11a.

The receiver therefore contains only a single tunable parameter: the threshold  $x_t$ . A reasonable choice for  $x_t$  is about 25% of the pulse magnitude expected at the receiver. Setting the threshold too high will cause the receiver to miss start bits or detect end-of-frame too early, resulting in missed or truncated frames. Setting it too low will tend to make the system spuriously trigger as a result of electrical noise experienced by the receiver; this may result in bad data being decoded, although it is extremely likely that such data would be rejected by the CRC stage, and so in practice this is not of undue concern.

### D. Decoding

The phase of the ME clock must be reconstructed at the receiver in order to decode the ME data. The decoder uses the knowledge that the start bit (1) causes the first rising edge to occur at the falling edge of the ME clock, i.e., at 180° ME clock phase. From this starting phase, the ME clock advances 180° per short pulse and 360° per long pulse. Thus the logical state of ME the clock should start low, and then be flipped every short pulse and left unaltered every long pulse. The original data is recovered by sampling the ME data when the ME clock is low.

### E. Data integrity and cyclic redundancy check

In practice, the communication channel is likely to be noisy. The voltage detected by the receiver will fluctuate due to changes in power flow on the line, switching noise, coupled interference, etc. If a fluctuation is large and sudden enough, the receiver will detect one or more spurious positive- or negative-going edges, leading to a corrupted ME bitstream

and bad data being decoded. The transmitter should therefore inject adequately large perturbations into the line to cause large enough voltage variation at the receiver such that the true ME data can be reliably distinguished by the receiver. Setting appropriate transmitter edge and hold perturbations and the receiver threshold  $x_t$  is therefore an important step in commissioning a practical system.

It is inevitable that data will be corrupted occasionally, even if the transmitter perturbation magnitude is large. As in any reliable communication scheme it is important to detect bad data, and if necessary, request a retransmission. In this work, data integrity was ensured by applying a 16 bit CRC to each 30 byte data. The CRC16 polynomial 0x5935 was selected for the experimental system. This polynomial can detect all four-bit errors in data lengths up to 241 bits. This allows corrupted data to be rejected with a high degree of reliability. An acknowledge/resend mechanism is not discussed, as this is higher-level functionality than the datalink layer considered in this paper.

## V. EXPERIMENTAL DEMONSTRATION

Fig. 12a shows the experimental setup, consisting of two DAHB converters powered by two Li-ion batteries. The communication is bidirectional, i.e., both converters act as transmitter and receiver, so we refer to them as transceivers. Transceiver 1 is under current control and Transceiver 2 is under voltage control. 100 meters of two-core steel wire armoured (SWA) cable with 1.5 mm<sup>2</sup> cross section is used as the transmission line. The common bus voltage is 110 V DC. Fig. 12b illustrates the experimental circuit setup. The receiver voltage signal is chosen as the information carrier.

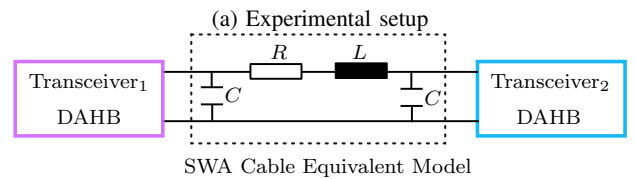
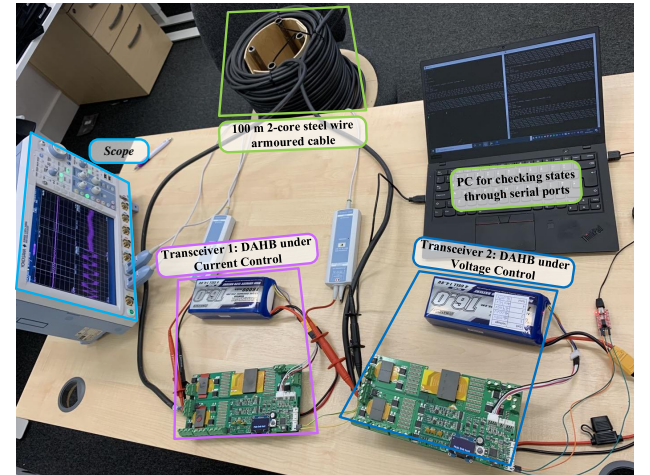
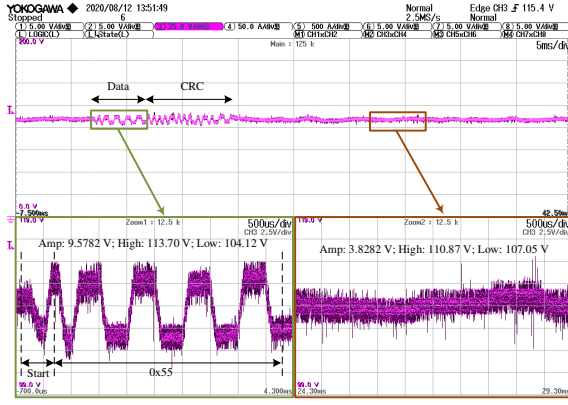
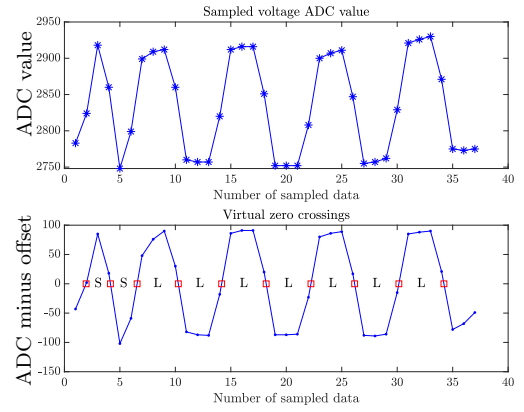


Fig. 12: Schematic of experimental setup.



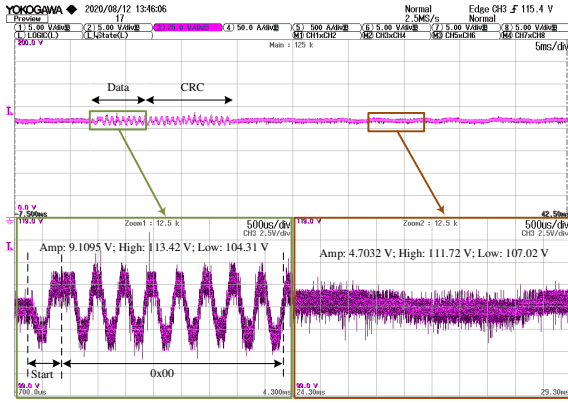


(a) Receiver terminal voltage waveform

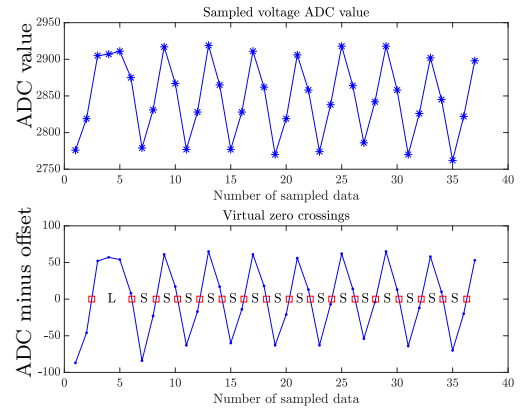


(b) Data analysis

Fig. 13: Experimental results for 0x55 (voltage source is the transmitter).

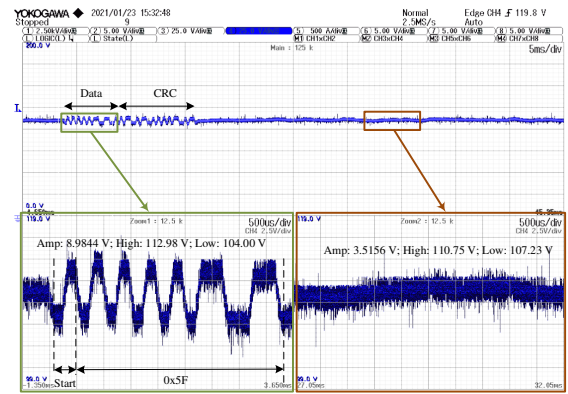


(a) Receiver terminal voltage waveform

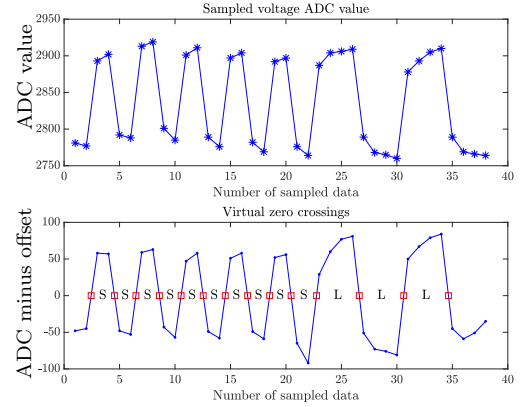


(b) Data analysis

Fig. 14: Experimental results for 0x00 (voltage source is the transmitter).



(a) Receiver terminal voltage waveform



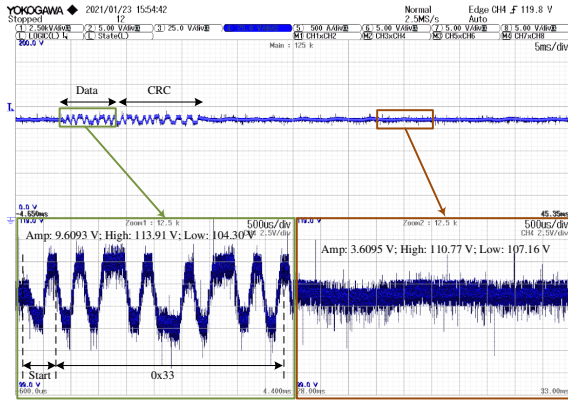
(b) Data analysis

Fig. 15: Experimental results for 0x5F (current source is the transmitter).

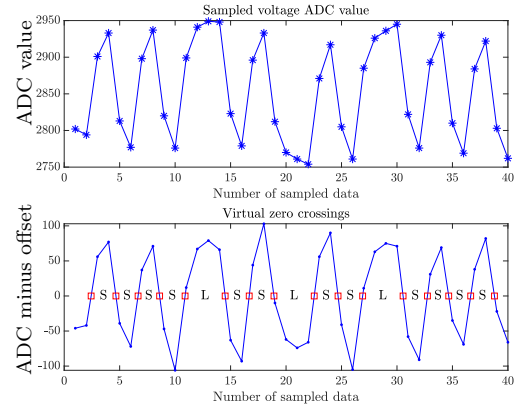
### A. Peer-to-peer bidirectional communication

Firstly, the voltage controlled converter acts as the transmitter by adding perturbations at the output of the voltage controller (transceiver 2 acts as the transmitter and transceiver 1 acts as the receiver). Results are given in Fig. 13 for transmitting 0x55 which consists of long pulses only, Fig. 14

for transmitting 0x00 which consists of short pulses only. Figs. 13a and 14a are voltage waveforms at the transceiver 1 side. These illustrate that the voltage ripple (due to switching) under normal operation is around 3%, and the voltage ripple during transmission is around 8%. The upper part of Figs. 13b and 14b illustrate the sampled raw ADC data from the receiver



(a) Receiver terminal voltage waveform



(b) Data analysis

Fig. 16: Experimental results for 0x33 (current source is the transmitter).

TABLE III: Parameters for Transmitter and Receiver

Parameter	Symbol	Nominal value
CPU frequency	$f_{cpu}^{TX} \& f_{cpu}^{RX}$	100 MHz
Switching frequency	$f_{sw}^{TX} \& f_{sw}^{RX}$	64 kHz
Control loop execution frequency	$f_c^{TX} \& f_c^{RX}$	8 kHz
ME clock frequency	$f_{plc}^{TX}$	2 kHz
Date bit rate	$R$	2 kbps
Voltage ADC LSb	-	38.6 mV (12-bits)
Current ADC LSb	-	4 mA (12-bits)
Phase Shift LSb	-	0.23°

(blue stars). The lower part of Figs. 13b and 14b illustrate the data after the moving average subtraction operation and the virtual zero-crossing locations are calculated (red squares). It is clear that the length of short pulses is shorter than 3 sample periods and the length of long pulses is longer than 3 sample periods. Thus, the short and long pulses can be distinguished, as per the discussion in Section IV. There are three or four sampled points for long pulses, indicating that the receiver clock is slightly slower than the transmitter clock in this example.

Secondly, the current controlled converter acts as transmitter by adding perturbations at the output of the current controller, (i.e., transceiver 1 acts as the transmitter and transceiver 2 acts as the receiver). Results are given in Figs. 15 and 16 for transmitting 0x5F and 0x33, which are mixtures of long and short pulses. Figs. 15a and 16a are voltage waveforms at the transceiver 2 side. The voltage waveforms are similar to the first case, which demonstrates that perturbations added to the voltage or current controller outputs at the transmitter provide similar effects at the receiver sides, as per Section II-B.

### B. Data packet communication demonstration

Practical applications are likely to require the exchange of more than one byte. As an example, the transmission of a 30-byte message “free PLC for any PE converter!” (plus two CRC bytes) is illustrated in Fig. 17. A zoomed-in view of first three bytes are given in the lower part of Fig. 17. In practice, we

observed approximately one failed CRC check in every 500 32-byte transmissions. This implies a bit error rate of one in 128k bits, or a Bit Error Rate (BER) of the order  $10^{-5}$ . The BER achieved in the end application will depend strongly on the signal to noise ratio at the receiver, and can be improved by increasing the magnitude of the perturbations injected at the receiver.

## VI. PRACTICAL DESIGN CONSIDERATION

### A. Parallel-connected converters

In the experimental setup described in this paper, the receiver voltage is sampled in order to extract the transmitted data. Therefore, for the method to work as intended, the transmitter must be able to adequately perturb the voltage of the shared DC bus such that the receiver is able to distinguish the PLC data from background noise. In the example presented here, the total DC bus capacitance is relatively small, and so this condition is met. However, if many converters share the DC bus (are connected in parallel), the bus capacitance may be large, and so even large perturbations injected by the transmitter will result in very small voltage signals at the receiver, leading to a poor BER. In addition, when many converters are connected in parallel, the overall closed-loop transfer function of the system will be modified [23] and the IFB may be affected. In all cases, the complete system should be modelled to identify the IFB, and so choose a suitable ME clock frequency, perturbation magnitude, and  $x_t$ .

In some scenarios, it may be advantageous to reduce the ME clock frequency and/or sense the current signal at the receiver, instead of the voltage. In general, the use of the minimum DC bus capacitance that ensures converter stability will allow the highest ME clock frequency to be achieved using the smallest perturbations, leading to high PLC data rates and low BER. Of course, this has the additional benefit of reducing the size and cost of the DC capacitors.

### B. Existence of the IFB

This paper demonstrates a PLC at 2 kbps where the control loop design is a simple, conventional single or double PI type.

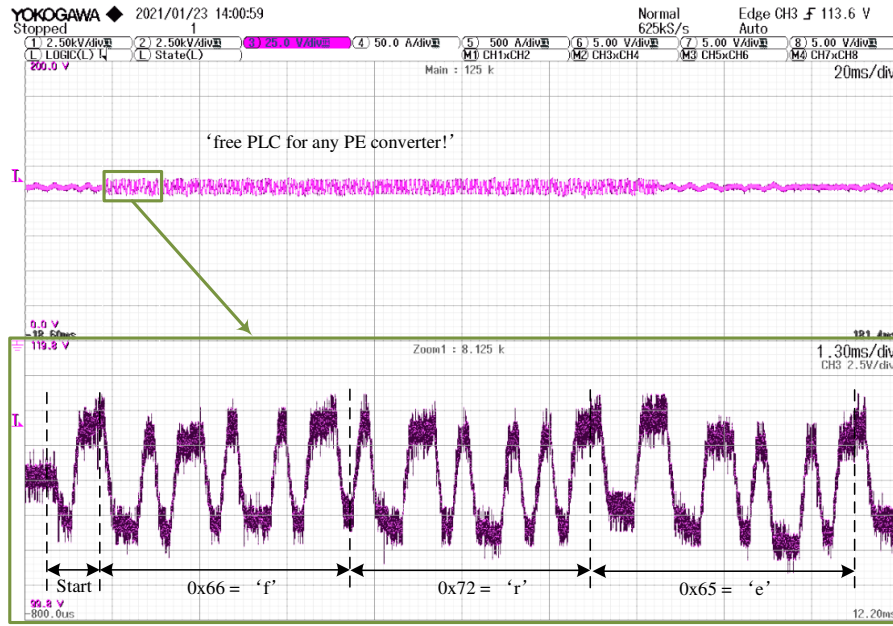


Fig. 17: Experimental results for 30 bytes data packet.

The bandwidths of the controllers were not compromised (not deliberately decreased) in order to reach this bit rate; the bit rate is the highest that can be achieved given the receiver sampling rate of 8 kHz. As per the discussion in Section II-A, conventional controllers will tend to exhibit an IFB and so allow PLC as described here. However, more advanced controllers, for example controllers with high sample rates that perform active damping of the output filter, may act to reject disturbances at frequencies approaching  $f_{\text{pef}}$ . This may make PLC difficult or impossible to achieve without modification of the controllers to artificially introduce an IFB.

### C. Bit rate limit

The bit rate of the PLC scales as per (1). If the switching frequency and control loop execution frequency are increased, the cut-off frequency of the power electronics circuit and filter may be increased proportionally, allowing the bitrate to also be increased proportionally. A wide-bandgap power stage switching in the megahertz range, coupled to a fast microcontroller with a sample rate of 100 kHz could achieve a bit rate of 25 kbps.

## VII. CONCLUSION

The PLC solution presented in this paper is broadly applicable to any power electronic converter circuit and control system exhibiting an Intermediate Frequency Band. The IFB is a region of relatively high gain from transmitter control system output to receiver input voltage (or current), and many practical converter designs exhibit it. A simple Manchester Encoding approach is applied at the transmitter, and then a set of signal processing steps at the receiver were shown to reliably recover the original data. The challenge of mismatched transmitter and receiver clocks is addressed and used to set limits

on the maximum encoder clock frequency. A zero-crossing location algorithm is used to generate accurate measurements of encoded data pulse lengths and allow reliable decoding. The practical feasibility of the scheme was demonstrated by achieving reliable communication at 2 kbps in a two-converter system using an 8 kHz sampling frequency.

Uniquely, the proposed solution is completely implemented in software on top of an existing power converter design. It does not require any additional analog circuits or high sample rate ADCs beyond those already incorporated in the power converter as part of its control system. It is therefore a true zero-additional-hardware option to add low data-rate PLC to networks of power converters.

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