

# Novel Stacking Design of a Flexible Thin-Film Thermoelectric Generator with a Metal–Insulator–Semiconductor Architecture

Xudong Tao, Botao Hao, and Hazel E. Assender\*

A stacked thermoelectric generator on a flexible polymer sheet is investigated that can utilize a low-cost high throughput roll-to-roll process, employing a metal–insulator–semiconductor structure of <100 nm thick Cu and bismuth telluride films with a  $\approx 1 \mu\text{m}$  thick acrylate insulating coating. Thermoelectric strips can be stacked and connected in the out-of-plane direction, which significantly decreases the size required in the substrate plane and also gives rise to the opportunity for greatly extending power output by stacking thousands of layers. A smooth surface of stacked layers is confirmed due to the nature of the acrylate layer. Room-temperature sputtering can produce good quality/crystalline films, indicated by X-ray diffraction and transmission electron microscope. Both experimental and simulation results observe a small temperature gradient across the stack from the bottom heat source to the top free surface. A stacked thermoelectric generator shows comparable performance to an in-plane device, and most notably, the stacked architecture allows a higher power output without increasing the dimension of the device in the substrate plane, while the thickness is increased within only a  $\mu\text{m}$  range. Cyclic buckling fatigue tests suggest that the performance of stacked functional strips can be protected under deformation within the acrylate matrix.

## 1. Introduction


Due to the tremendous growth of the wearable electronics market (e.g., \$34 billion of wearable fitness market in 2020<sup>[1]</sup>), there is an increasing demand for wearable thermoelectric generators (TEGs) to be an alternative to lithium batteries (which have some critical issues, e.g., explosion, environmental

pollution, a tradeoff between size and storage, inconvenience of disassembly and replacement for wearers<sup>[2]</sup>) for such applications. As a green/clean and self-powered source, wearable TEGs can locally/continuously convert thermal energy (i.e., the temperature difference,  $\Delta T$ , between the human body and the surroundings) into electrical energy according to the Seebeck effect using thermoelectric (TE) materials. Flexible/wearable TEGs are commonly developed as either fully organic<sup>[3–6]</sup> or inorganic/organic hybrids.<sup>[7–10]</sup> Inorganic TE thin-film deposition on flexible polymer sheet is a typical route to inorganic/organic hybrids, which has attracted significant attention recently because a thin-film configuration has the potential compatibility with low-cost fabrication technologies (e.g., roll-to-roll, R2R<sup>[11]</sup>), low material consumption/cost,<sup>[12]</sup> minimum size/weight,<sup>[13]</sup> large-area manufacturability,<sup>[14]</sup> and a wide range of structural designs of TEGs (e.g., planar,<sup>[15]</sup> cylindrical,<sup>[16]</sup> Y-type,<sup>[17]</sup> corrugated-structure<sup>[18]</sup> or folded-mode,<sup>[14]</sup> slope-type,<sup>[19]</sup> coil-up

coin-shape,<sup>[20]</sup> and oxide-based transversal<sup>[21]</sup>). In laboratory research, various techniques have been investigated to fabricate TE thin films, e.g., sputtering,<sup>[22]</sup> evaporation,<sup>[23]</sup> inkjet<sup>[24]</sup>/screen<sup>[25]</sup> printing, pulsed laser deposition,<sup>[26]</sup> molecular beam epitaxy,<sup>[27]</sup> and electrodeposition.<sup>[28]</sup> Among them, only sputtering shows the most promise for scale-up manufacture of TEGs like R2R processing.<sup>[29]</sup> Hence, sputtering is employed in this study.

Flexible thin-film TEGs can be assembled in both cross-plane (CP-TEG) and in-plane (IP-TEG) structural designs, which allow heat flows/TE legs perpendicular and parallel, respectively, to the substrate.<sup>[30]</sup> CP-TEG has already been commercialized in bulk TEGs and some  $\mu\text{TEGs}$ , however, to further decrease the size to nanorange, the crossplane configuration is not practical since maintaining a large  $\Delta T$  across a nanothick TE leg is an almost impossible challenge<sup>[14,31]</sup> and the power output is very poor (e.g., refs. [32–39]). Although the development of nanosize CP-TEG is restricted, nanomaterials still attract significant interest for scientists, and the research on IP-TEG is moving toward the use of nanomaterials (e.g., thin film,<sup>[40]</sup> quantum well,<sup>[41]</sup> and nanowire<sup>[42]</sup>),

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 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/aelm.202100201>.

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DOI: 10.1002/aelm.202100201

due to an extraordinary improvement in TE performance.<sup>[43]</sup> Our previous work<sup>[29]</sup> observed an increase in power factor ( $PF = S^2 \rho^{-1}$ , where  $S$  is Seebeck coefficient and  $\rho$  is electrical resistivity) for a thinner sputtered bismuth telluride (Bi-Te) film, which experimentally confirmed the calculated prediction in.<sup>[44]</sup> Compared with CP-TEG, IP-TEG mainly has two drawbacks: 1)  $\Delta T$  of wearable TEG should be perpendicular to a wearer's skin,<sup>[45]</sup> while IP-TEG utilizes  $\Delta T$  in the plane which limits the use of IP-TEG on the human body.<sup>[2]</sup> 2) Because of a long-strip architecture in the plane, the internal electrical resistance of IP-TEG is usually large thereby leading to a relatively high voltage output but a tiny working current output, hence the power output is limited.<sup>[30,46,47]</sup>

Drawback (1) is a common question of how to apply IP-TEG in a real wearable application. To solve it, scientists have proposed a variety of feasible means/designs (such as coiled-up coin-shape, Y-type, slope-type, and corrugated-structure). In terms of drawback (2), the high internal resistance and low power output can be adjustable according to the dimension of the TE strip. In the design of IP-TEG, a major tradeoff is considered between the TE-strip dimension and fill factor (FF).<sup>[48,49]</sup> FF quantifies how efficiently a TEG occupies a substrate, i.e., the ratio between the surface area of TEG materials and the overall surface area of the device. A maximum power density requires a balance of factors: FF, inter-strip spacing, dimension, and the number of TE strips.

An IP-TEG is typically fabricated on a substrate with a number of TE strips that are electrically connected in series or parallel. Herein, we investigate a stacked architecture of TE strips, to improve the TE performance. Funahashi et al.<sup>[50]</sup> reported a bulk TEG based on multilayer ceramic capacitor technology in which a number of n-i-p junctions (where n, i, p are n-type, insulator, and p-type semiconductor, respectively) were stacked and cofired. Funahashi's study stacked bulk layers along the in-plane direction, while what we are reporting here is a stack design of nanothick coatings in the crossplane direction.

TEGs are traditionally designed round n-i-p elements and this is more commonly used than m-i-s (where m, i, and s are metal, insulator, and semiconductor, respectively), because the m-i-s TEG has an inherent and parasitic drawback that the metal strip has good thermal conductivity and can conduct heat from the hot side to the cold side (consequently a decrease in  $\Delta T$  leads to less power output). However, many studies<sup>[14,51]</sup> have investigated m-i-s TEGs, and it has been confirmed that the difference of power outputs between these two architectures (m-i-s vs n-i-p) is very small.<sup>[14]</sup> Most importantly, a stacked m-i-s structure in a thin-film configuration is easier to fabricate than a stacked n-i-p structure (e.g., the ease of synthesis/deposition, material stability, and reliability), causing fewer issues (e.g., a short or open circuit) for reliable TEG devices. Overall, a faster prototype/demonstration could be achieved with one type (n or p) coupled with a metal shunt,<sup>[48]</sup> hence we utilized the m-i-s architecture in this study.

The manufacturing process of TEGs depends on the architecture of TEGs and the TE material employed.<sup>[52]</sup> A traditional inorganic TE material, bismuth telluride ( $\text{Bi}_2\text{Te}_3$ ), is investigated in this study because it shows the best TE performance for room-temperature applications<sup>[53]</sup> and has good

R2R manufacturability by sputtering.<sup>[29]</sup> The metal and insulator are copper and acrylate coatings,<sup>[54]</sup> respectively, and both are R2R manufacturable. Several m-i-s junctions are stacked in a single strip (electrically connected in series or parallel) and then several single stacked strips are electrically in-plane connected in series or parallel. Stacking TE layers in parallel is equivalent to making a thicker TE layer; however, stacking TE layers with a polymer interlayer in this way avoids the need to deposit a thick TE film, and a thinner TE film can show a better TE performance.<sup>[29]</sup> Second, inserting acrylate polymer layers in a stacked composite structure should improve the mechanical resilience of the device, as compared with a monolithic thick layer. The stacked arrangement also allows full flexibility in combining in-series and in-parallel connection between TE strips, thus allowing a preferred voltage and current characteristic of the device to be tailored for the application.

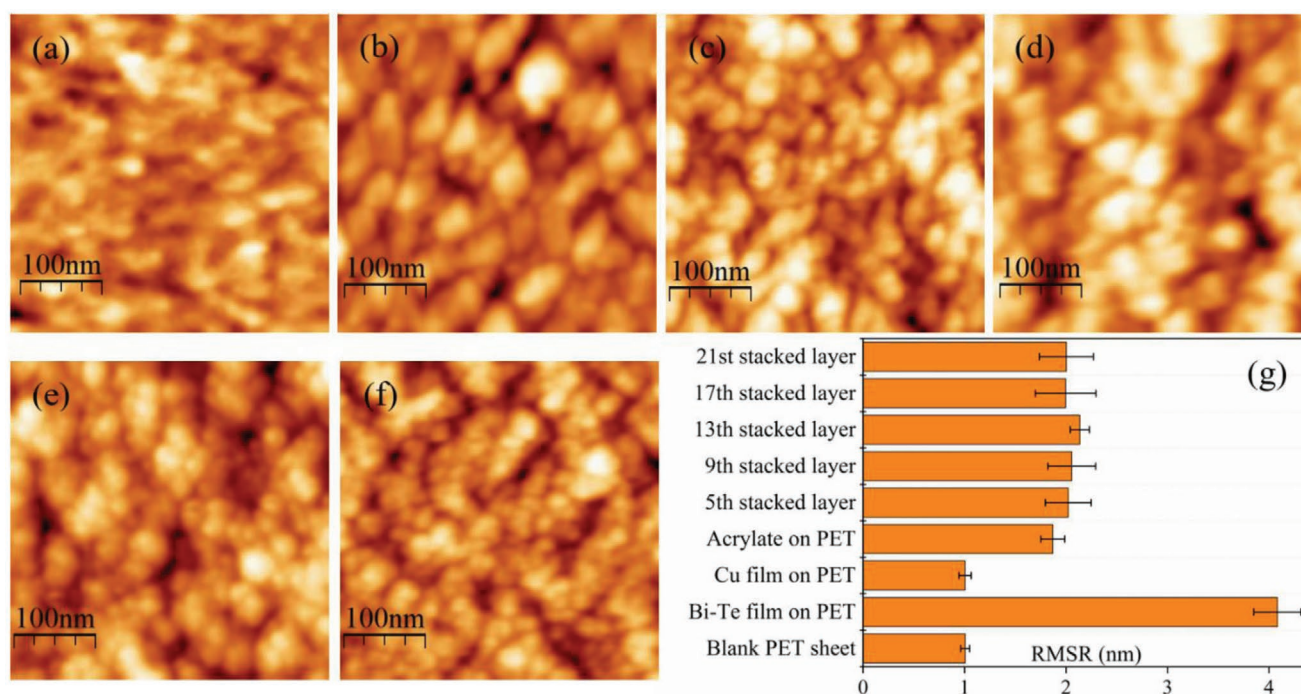
Therefore, in this paper, we explore the feasibility of stacking TE nanomaterials in the crossplane direction for IP-TEGs. All experimental designs are highly compatible with a real low-cost high throughput R2R process, all under the same vacuum condition, that we seek to emulate.

## 2. Results and Discussion

### 2.1. Surface Topography and Cross-section of Stacking

The thicknesses of Bi-Te, Cu, and acrylate coatings were measured:  $87 (\pm 5)$ ,  $97 (\pm 8)$ ,  $1195 (\pm 155)$  nm, respectively. **Figure 1** shows surface topographies (atomic force microscopy, AFM images) of a) the polyethylene terephthalate (PET) substrate, b) Bi-Te, c) Cu, and d) acrylate on the PET substrate, as well as e,f) stacked layers (the top layer is Cu). In **Figure 1e,f**, the layer immediately beneath the top Cu layer is an acrylate insulating coating. The surface features on (e) and (f) are quite similar to that in (c), indicating that a Cu film can grow in a similar fashion on both PET and acrylate surfaces. Unlike the very fine crystals of the Cu film (c), bigger granules are observed on the Bi-Te film (b), causing a higher surface roughness (g). This has been confirmed in scanning electron microscope (SEM) images (**Figure 2a,b**) and transmission electron microscope (TEM) images (**Figure 2d,h**) with consistent grain size for the Bi-Te of about 20 nm.

The acrylate coating displays a smooth surface as observed in **Figures 1d** and **2c**. This smooth surface is a product of the deposition route: evaporation and condensation of a monomer liquid onto a substrate followed by radiation curing. This process has been previously reported as a smoothing layer for gas barrier films in packaging applications,<sup>[55]</sup> a reflector/interferometer in optical applications,<sup>[56]</sup> a dielectric layer in capacitors,<sup>[57]</sup> and an insulator layer in organic transistors.<sup>[58]</sup> A thin, smooth, insulating layer in between the metal contact and the TE layer is important in a stacked structure, as any protrusion can cause a short circuit (locally thin areas can lead to carrier tunneling) and it will affect the surface feature of the next metal or TE layer as well as their electrical properties. Most importantly, we see that as more layers are stacked, the surface roughness (RMSR, root mean square roughness, see **Figure 1g**) remains close to that of the immediately underlying smooth acrylate



**Figure 1.** a–c) AFM images of a) the PET substrate, and b) Bi-Te, c) Cu and d) acrylate polymer coatings on PET sheets, e) 9th stacked Cu film, f) 13th stacked Cu film, and g) RMSR of PET, Bi-Te, Cu, acrylate coatings and in stacked layers (the 5th, 9th, 13th, 17th, and 21st layers are Cu and the layer beneath this is acrylate in each case). RMSR values are measured over an area of 400 nm by 400 nm in four different locations on each sample.

layer. In stacks, a sufficiently thick acrylate coating presents a constant surface roughness due to its manufacturing process in which acrylate monomer is coated as a low viscosity liquid, filling in undulations in the layer beneath. This suggests that the roughness will not limit the number of layers to be stacked.

A cross-sectional image of a stacked structure is shown in Figure 2e, with a line profile of the topography (Figure 2f). A clear stacked structure is confirmed by C, Bi, and Cu profiles, representing acrylate, Bi-Te, and Cu coatings, respectively.

## 2.2. Phase Identification

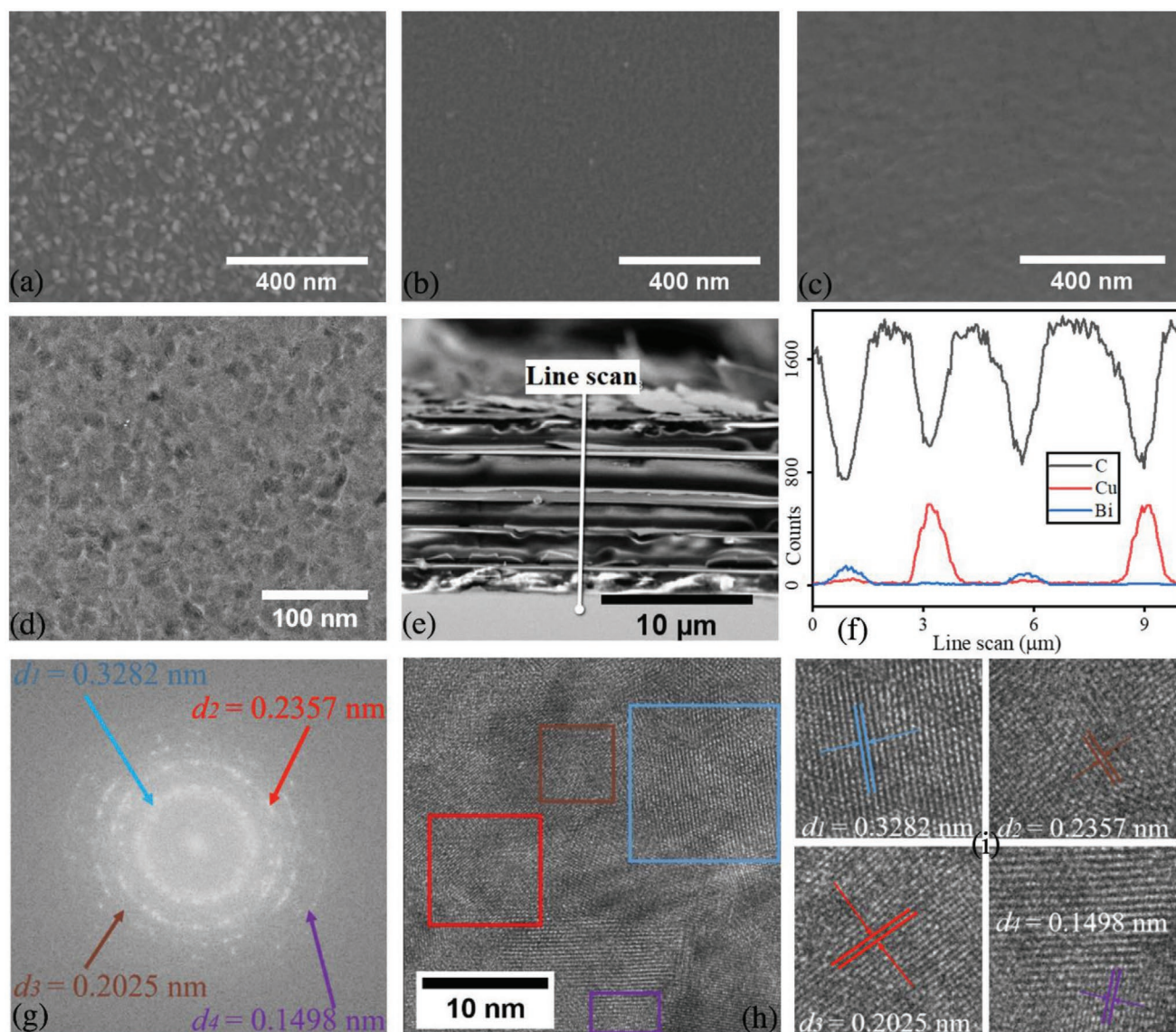
X-ray diffraction (XRD) results of Bi-Te and Cu are shown in Figure 3a,b, though only one peak of Bi-Te (0 1 5) and one peak of Cu (1 1 1) are identified because the film is so thin. Energy dispersive X-ray (EDX) results can confirm the presence of these elements (Bi, Te, and Cu) in the films and the elemental ratio of Bi and Te is measured as 34.96: 65.04 ( $\pm 0.69$ ) at%. To further explore the crystallinity of the Bi-Te film that grows at room temperature, high-resolution TEM (HRTEM) and fast Fourier transform (FFT) images are analyzed (Figure 2g–i), in which four d-spacings (0.3282, 0.2357, 0.2025, and 0.1498 nm) are identified and a polycrystalline structure can be observed. Supporting information (see Appendix Figure SA1 and Table SA1, Supporting Information) of XRD confirms these d-spacings in a much thicker Bi-Te film ( $\approx 1 \mu\text{m}$ ), corresponding to miller indices of (0 1 5), (1 0 10), (1 1 6), and (1 1 15), respectively. The HRTEM result here indicates that the very thin Bi-Te film is also crystallized. In Appendix Figure SB1 in the Supporting

Information, XRD peaks (0 1 5) of Bi-Te and (1 1 1) of Cu can be seen to increase in intensity as more layers are included in the stack. In addition, a new peak of Bi-Te (1 0 10) appears and grows. This is because more signals from the Bi-Te film can be detected in XRD as more layers are stacked (equivalent to a thicker Bi-Te coating).

X-ray photoelectron spectrometer (XPS) results (Figure 3c,d) also confirm that the elements Bi, Te, and Cu are present, in agreement with EDX. There is no clear oxidation of elements Bi and Cu, however, a  $\text{TeO}_2$  state is detected (Figure 3c). This is inconsistent with previous reports with other fabrication methods in which both Bi and Te were found to be oxidized<sup>[59–62]</sup> and Bi is expected to be more reactive.<sup>[61]</sup>

The oxidation phase in the Bi-Te film was predicted in our previous studies<sup>[29,63]</sup> which could account for the film performance. In this study, we can only confirm the oxidation state at the film surface (XPS penetration depth: a few nm), while it is not clear for the bulk of the film ( $\approx 87$  nm). Both EDX (Figure 3e) and XRD (Appendix Figure SA1, Supporting Information), with a penetration depth of  $\mu\text{m}$  range, suggest that the oxidation of the whole film is unlikely, or the content of oxygen is too low (negligible) to be identified by EDX and XRD (although peak overlapping in EDX and XRD could exist, there is no other extra peak that uniquely indicates the oxidation phase). Hence, the truth might be similar to the case of Al/Al-O mixed phases, which is to say, the  $\text{TeO}_2$  could form at the film surface once the vacuum breaks (after sputtering), as reported<sup>[62]</sup> that the oxidation of Bi-Te could happen under ambient atmospheric conditions and the surface oxidation layer could be readily removed using etching methods. In our case,





**Figure 2.** a–c) SEM surface image of Bi-Te, Cu, and acrylate coatings (there is a 3 nm Pt coating on the surface of acrylate insulating coating for SEM imaging), d) TEM image of Bi-Te film, e, f) SEM cross-sectional view of stacked layers and elemental analysis in a line scan mode of EDX, g) HRTEM FFT image of a Bi-Te film, and h, i) HRTEM images of a Bi-Te film.

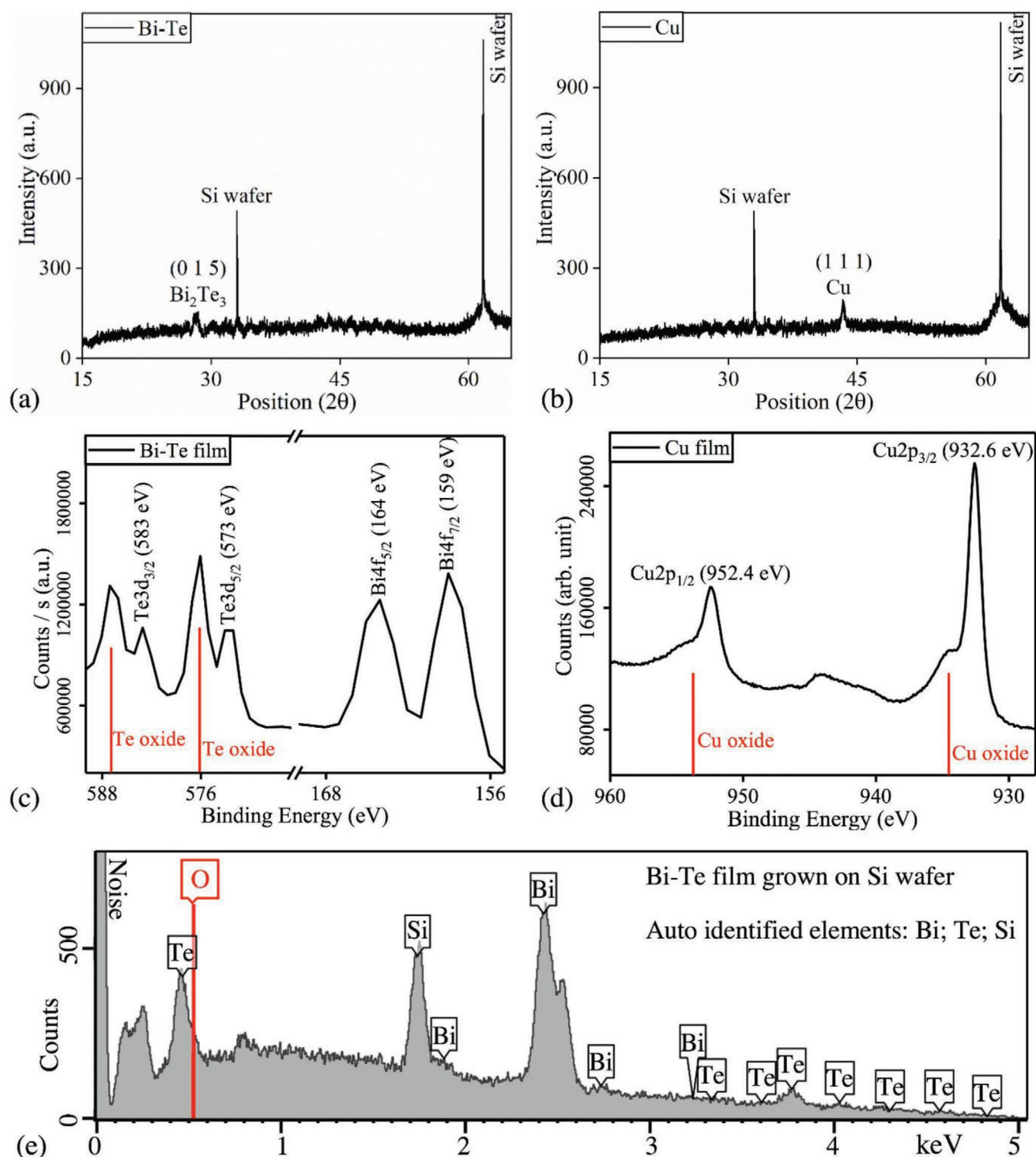
there is no obvious deterioration in the TE performance after a year, suggesting that 1) the oxidation at the surface will not go further into the bulk of the film or 2) the whole film has already been oxidized once the vacuum is broken.

### 2.3. Thermoelectric Performance

$S$  of the Bi-Te film is found to be  $57 (\pm 0.6) \mu\text{V K}^{-1}$ .  $\rho$  of Bi-Te and Cu films are  $1.67 (\pm 0.21)$  and  $0.032 (\pm 0.003) \text{ m}\Omega \text{ cm}$ , respectively. Thus, PF of Bi-Te film can be calculated as  $2.0 (\pm 0.2) \times 10^{-4} \text{ W m}^{-1} \text{ K}^{-2}$ , which is comparable to the latest reported result ( $\approx 2.8 \times 10^{-4} \text{ W m}^{-1} \text{ K}^{-2}$ ) from a  $1 \mu\text{m}$  thick Bi-Te film sputtered at room temperature (Haidar et al.<sup>[65]</sup>).

#### 2.3.1. Seebeck Behavior of Stacked TEGs

The connection of TE strips in series and parallel should theoretically give rise to a voltage-dominant and current-dominant output, respectively. **Figure 4a,b** plots the open-circuit voltage and short-circuit current as  $\Delta T$  increases, corresponding to an in-series stacked structure and an in-parallel stacked structure, respectively. The slope of the fit line in **Figure 4a** is defined as the Seebeck coefficient ( $S$ ) to describe the induced voltage across a  $\Delta T$ . Similarly,  $S'$  (the slope of the fit line in **Figure 4b**) can describe an induced TE current in response to a  $\Delta T$  across the two ends of TE strips stacked in parallel. Ideally,  $S$  or ( $S'$ ) should present a linear relationship with the number of TE strips. This is further analyzed as shown in figures inset in

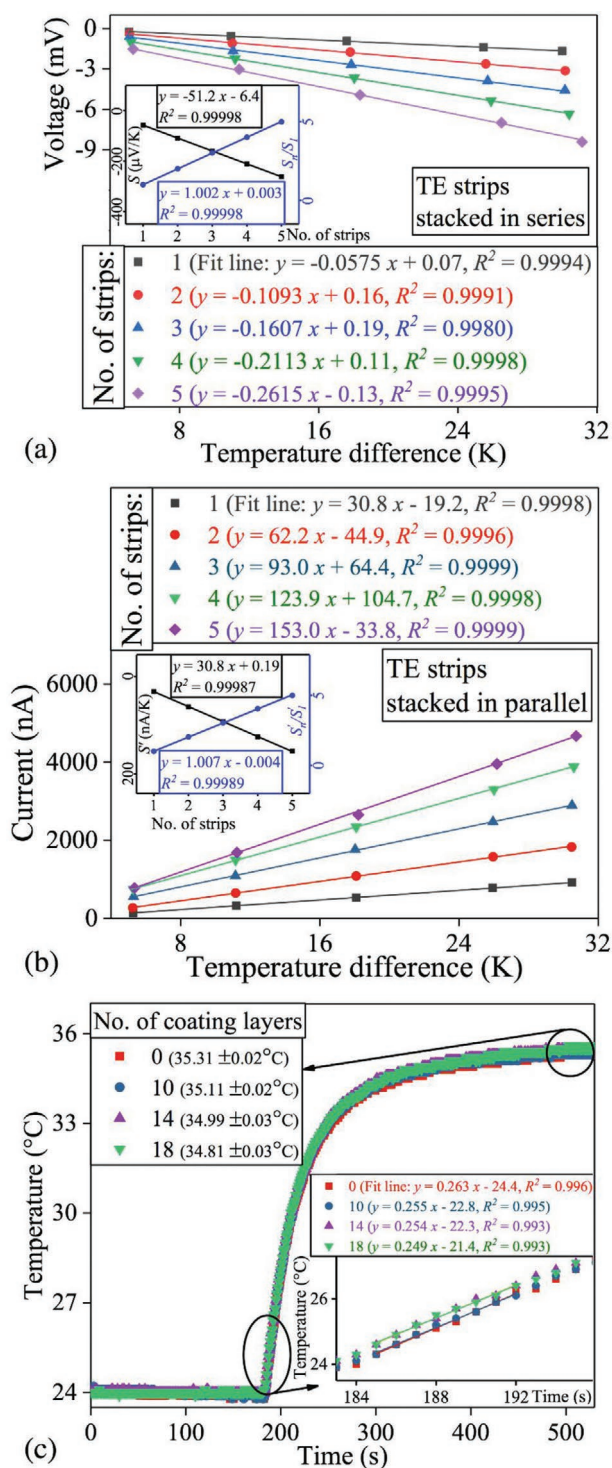


**Figure 3.** a,b) XRD patterns of Bi-Te and Cu films on Si wafers, c,d) XPS analysis of Bi-Te and Cu films on polymer sheets (the peak position of Bi4f and Te3d are referenced from ref. [59] and the peak position of Cu2p is referenced from ref. [64]), and e) EDX spectrum of a Bi-Te film grown on a Si wafer.

Figure 4a,b. A plot of  $S_n$  (or  $S'_n$ ) versus the number of strips shows an almost perfect linear relationship ( $R^2$  approaches 1). For the  $S'$  values this plot passes through zero as expected, although for the case of  $S$  for the in-series connected device

there is a small systematic error of  $6.4 \mu\text{V K}^{-1}$ . Removing this systematic offset for the case of  $S$ , and then plotting the corrected  $S_n/S_1$  (and  $S'_n/S'_1$ ) shows a linear trend with a slope very close to 1, as would be expected for the ideal device.





**Figure 4.** a) Plot of the open-circuit voltage versus  $\Delta T$  as the number (No.) of stacked strips in series is increased (the slope of the fit line is Seebeck coefficient; the inset figure plots  $S$  and the corrected  $S_n/S_1$  vs No. of TE strips). b) Plot of the short-circuit current versus  $\Delta T$  as increasing the number of stacked strips in parallel (the slope of fit line is defined as Seebeck coefficient',  $S'$ , in this study which describes the change of short-circuit current with  $\Delta T$ ). c) Plot of the temperature on the sample surface versus time for samples with different stacked layers by applying a hot temperature at the bottom side of the sample (numbers in bracket

We considered the possible effect of a drop in temperature on the hot (non-ambient) side of a device because the thickness increases with the number of stacked layers. The temperature measured on the upper surface at the hot side of a device is shown in Figure 4c. As seen in the inset figure of Figure 4c, a total of 18 coating layers, which corresponds to five-TE strips stacked in series, shows a slow rate of increasing temperature at an initial stage. The slopes of fit lines for 0 layer and 18 layers (including nine thermally insulating acrylate layers) are 0.263 and 0.249 °C s<sup>-1</sup>, respectively. A lower equilibrium temperature is also observed (the equilibrium temperature for 0 layers and 18 layers are 35.31 ± 0.02 and 34.81 ± 0.03 °C, respectively). As the current and voltage measurements are taken once the sample temperature reaches equilibrium, we can estimate the effect of this temperature difference. Take the TEG with five-TE strips stacked in series as an example ( $S = 57 \mu\text{V K}^{-1}$ ), the 1st TE strip that contacts with the polymer substrate (given a hot-side temperature of 35.31 °C, i.e.,  $\Delta T = 15.31 \text{ K}$ ) would generate a potential difference of 873 μV. The upper TE strip, which has  $\Delta T = 14.81 \text{ K}$  (due to the thermal insulation effect of the stack), would generate 844 μV, i.e., less than 3% difference over five TE layers.

In addition to the simple thermocouple measurement, the possibility of a temperature gradient in a stacked TEG from bottom to top is considered using COMSOL simulation. A single surface emissivity parameter ( $\epsilon$ ) is used in the simulation although various materials in the stack have different values of  $\epsilon$  (see Table 1). The PET and acrylate layers are significantly the thickest and the top layer is acrylate, so these materials should have a predominant effect on surface emissivity. Thus, the value  $\epsilon = 0.8$  is likely closest to the real situation. However, to check the effect of these values, simulations using three different values,  $\epsilon = 0.1, 0.3$ , and 0.8, were trialed.

**Figure 5** simulates a) a temperature profile at the "hot side" of a stacked structure (with an  $a$ - $b$  dimension of 2 mm × 2 mm) under a heater of 305 K applied at the bottom side of PET and d) the heat transfer along a TE strip with a temperature of 305 K applied at the side face. In this case, we did not fix the temperature on the cold side (which simulates a real wearable condition). Simulated results of the heat transfer in a stacked structure are demonstrated in Figure 5a–c. A decrease in the temperature of successive TE layers is observed as more layers are stacked and the decreasing trend is greater (i.e., a bigger slope of the linear fit in Figure 5b) with a bigger  $\epsilon$  since more heat radiates to the ambient. To illustrate this difference, Figure 5c shows the temperature difference between the 1st TE layer and the 5th TE layer at the hot side of the device under different  $\epsilon$ . The maximum difference is 0.11 K, i.e., 0.022 K strip<sup>-1</sup> ( $\epsilon = 0.8$ ), smaller than the measured result of 0.1 K strip<sup>-1</sup> (Figure 4c), using the idealized parameters in the COMSOL simulation, e.g., free convection in the air. As the temperature loss in the upper layer is smaller in the

describe the highest temperature under an equilibrium condition during Seebeck measurement; inset: a zoomed-in figure at the initial stage of increasing temperature and the slope of the fit line describes the rate of increase of temperature. Nota bene: the offset in temperature with the number of stacks reflects the variation in the exact time at which the heater is switched on).

**Table 1.** Material properties used in COMSOL simulation.

Materials	Thermal conductivity [W m <sup>-1</sup> K <sup>-1</sup> ]	Surface emissivity	Thickness [nm]
PET	0.16 <sup>[71]</sup>	0.8 <sup>[72]</sup>	125 000
Bi-Te	0.4 <sup>[73]</sup>	0.34 <sup>[74]</sup>	87
Cu	100 <sup>[75]</sup>	0.1 <sup>[76]</sup>	97
Acrylate	0.182 <sup>[77]</sup>	0.81 <sup>[78]</sup>	1195

simulation, the predicted change in voltage and current output would be smaller, suggesting that the experimental results are not underestimating the scale of the effect.

Therefore, to eliminate the heat loss within the stack, decreasing the main contributor to the device thickness (i.e., the acrylate insulating layer in this case) would be favorable, provided that its reliable electrical insulating property is maintained. Since there is a significant temperature drop across the PET substrate, it is also favorable to decrease this thickness and to improve its thermal conduction properties on the hot side.

The reduction in  $\Delta T$  on the upper layer could be an issue if many layers are stacked (e.g., imagine a stack of 1000 layers). However, it is notable that this is only the case when the heat is applied to the polymer substrate (i.e., the bottom side of the device substrate), which is common in laboratory measurements. This, however, may not be the case in architectures developed in wearable applications. If we take the coil-up coin-shape<sup>[20]</sup> as an example, the heat source is on the cross-section of the IP-TEGs, thus all TE materials would obtain the same  $\Delta T$ .

The COMSOL simulation also allows us to consider the effect of heat transfer along the length of a TE strip (Figure 5d). The temperature difference that is required for power generation can only be maintained if the heat from the hot side does not warm the material on the cold side. Figure 5e shows a simulated profile of the temperature along the strip length at the top surface of the device. It is clear that if the length of the strip is greater than  $\approx 6$  mm, the temperature at the cold side is not affected by the heat from the hot side, as the cold side surface reaches the ambient temperature (293 K). This 6 mm length sets a limitation for the application of the IP-TEGs to prevent a loss of  $\Delta T$  in the plane, i.e., losing TE performance. In this study, the length of the TE strip is 20 mm, hence, no matter how many layers are stacked, the temperature at the cold side will remain 293 K. This is consistent with the experimental measurement of temperature at the cold side of TEGs, i.e., the temperature was found to be same as the ambient.

### 2.3.2. Comparison between TE Strips Connected in Plane and in Stacking

The performance of TE strips in this novel stacked formation is compared here with that of the device made up of connections between strips in the plane of the substrate, as shown in Figure 6a. Compared with the in-parallel TEG, the in-series configuration is found to have a much higher power output. The measured maximum power output ( $P_{\max}$ ) reaches  $-0.26$  nW (the stacked in-series case) and  $-0.27$  nW (the in-plane in-series case) under a rheostat of  $\approx 10$  k $\Omega$ . As shown in ref. [66], the  $P_{\max}$

is reached when the load resistance is equal to the internal resistance of a TEG.

In-series and in-parallel structures can provide a maximum voltage and a maximum current, respectively, and according to the requirement of a particular application, a power source that is either current dominant or voltage dominant will be preferred. A linear relationship between voltage or current with the number of strips was predicted in ref. [67] from MATLAB simulation. Performances of in-plane and stacked structures can be directly compared in plots of Figure 6b. In this case, the voltage for in-series connected devices and the current for in-parallel connected devices are plotted as a function of the number of strips at each of i) the maximum rheostat setting in this experiment, 50 k $\Omega$ , where there is little change with load resistance, and ii) at the rheostat setting (load resistance) that gives the  $P_{\max}$  of the device, the point at which the device, ideally, would be used. Note that the load resistance of the  $P_{\max}$  changes with the number of strips. The load resistance of the  $P_{\max}$  is determined by a fit of the power data to Equation (1)<sup>[68]</sup>

$$P = I^2 \cdot R_L = \left( \frac{S_{\text{TEG}} \cdot \Delta T}{R_{\text{TEG}} + R_L} \right)^2 \cdot R_L \quad (1)$$

where  $P$  is the power output,  $I$  is the current,  $\Delta T$  is the temperature difference applied,  $R_L$  is the resistance of a load resistor;  $S_{\text{TEG}}$  is the Seebeck coefficient of the whole device; and  $R_{\text{TEG}}$  is the internal resistance of the whole device.

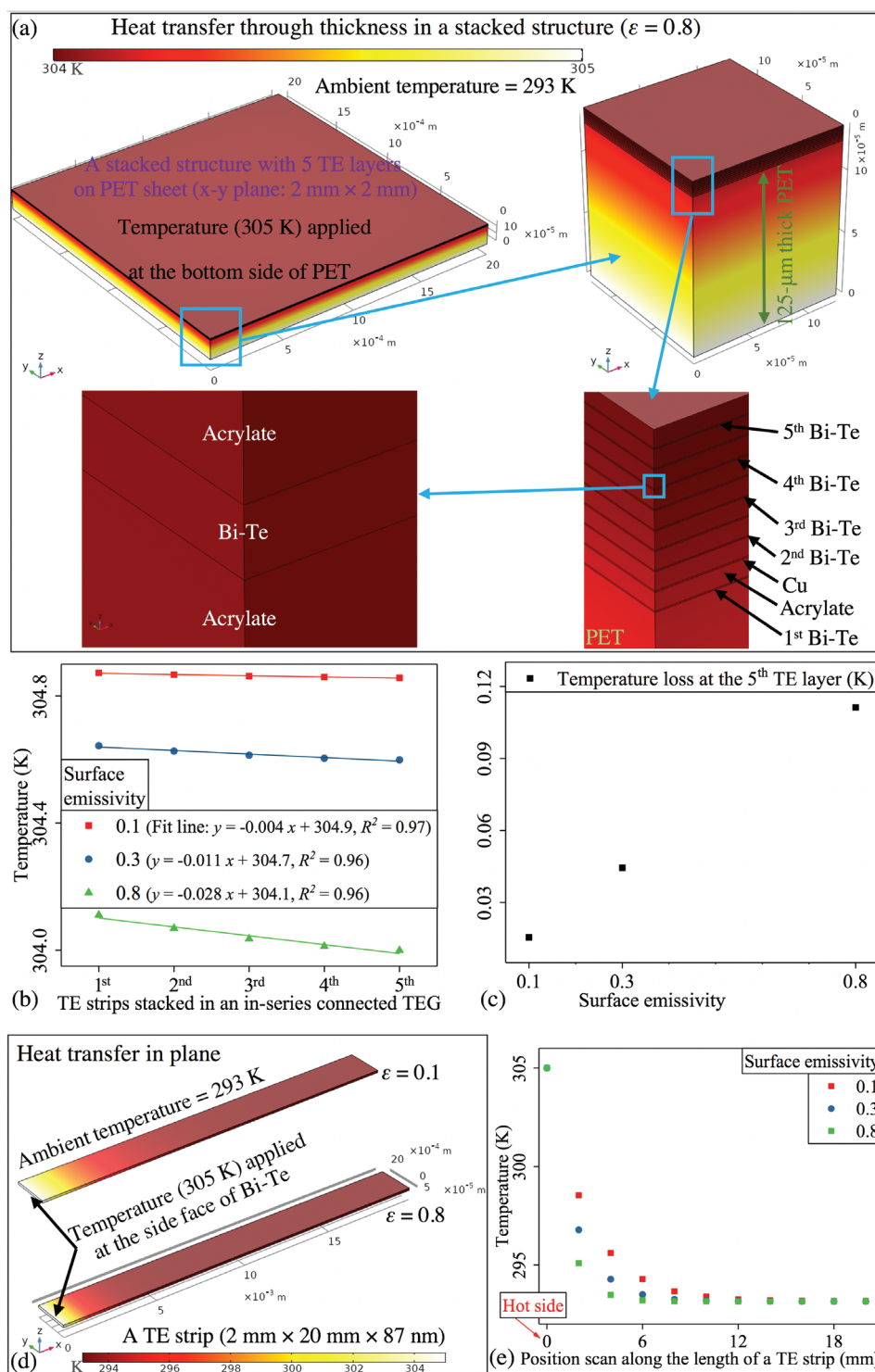
In each case, the plots of  $V$ ,  $I$ , or  $P$  increase linearly with the number of strips and there is close agreement between the performance of the in-plane and stacked structures. A slight decrease in the slope of linear fit for the stacked case demonstrates a loss in TE performance as more layers are stacked, which could be attributed to the temperature loss at the top layer as discussed above.

Most notably, Figure 6a reveals that whether TE strips are connected in series or parallel, the stacked architecture can provide a very similar TE output to the in-plane TEG. This electrical response is accompanied by a greater FF for the architecture in the stacked case. For example, in the case of a TE strip of 2 mm  $\times$  20 mm, an in-plane TEG with five strips connected in series occupies an  $a$ - $b$  dimension of (5  $\times$  2 + 5  $\times$  2 + 10  $\times$  1) mm  $\times$  (20 + 2) mm = 660 mm<sup>2</sup> (corresponding to the width of 5 metal strips + 5 TE strips + 10 inter-strip spacings; the length of metal or TE strip + the margin at two ends), i.e., 660/5 = 132 mm<sup>2</sup> per footprint of the device, while a stacked structure only requires an  $a$ - $b$  dimension of 2 mm  $\times$  25 mm = 50 mm<sup>2</sup> and  $c$ -axis of  $\approx 11.8$   $\mu$ m ( $\approx 435$  nm thick Bi-Te of five layers,  $\approx 582$  nm thick Cu of six layers, and  $\approx 10.8$   $\mu$ m thick acrylate of nine layers, for a five TE-strip stacked TEG). Thus, in respect of the  $a$ - $b$  plane, FF is calculated as below.

For the stacked TEG

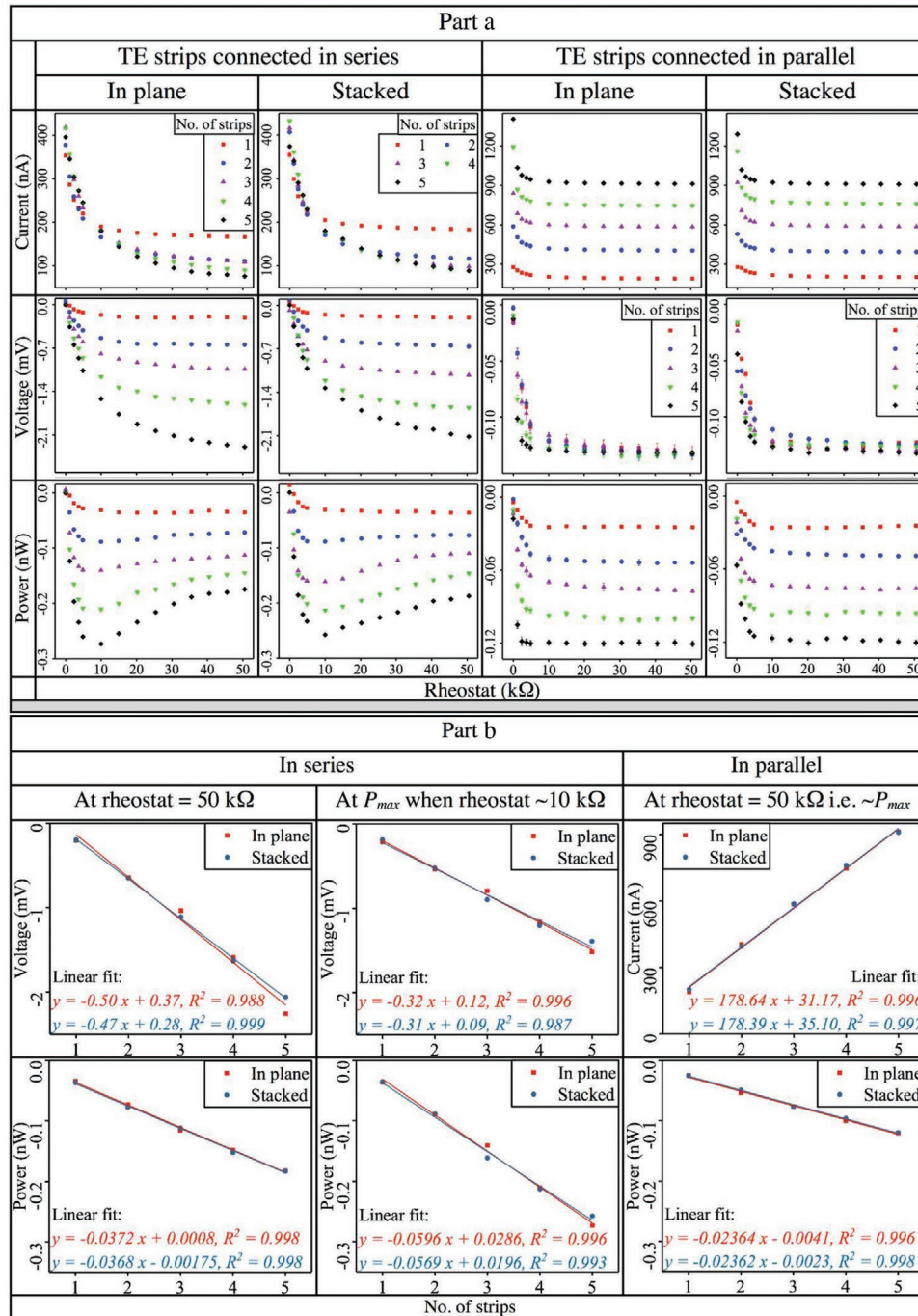
$$\text{FF} = \frac{n \times 2 \times 20}{50} = 0.8 n \quad (2)$$

where  $n$  is the number of TE strips involved, (2  $\times$  20) is the TE-strip size, and 50 is the strip area per footprint of the device regarding the stacked TEG.



**Figure 5.** COMSOL simulation of the heat transfer in TEGs under an ambient condition of 293 K with hot side at 305 K to simulate a real wearable application ( $\Delta T \approx 11.4$  K, same as the experimental study). a) An in-series stacked structure with five TE layers as well as Cu and acrylate layers on PET (2 mm  $\times$  2 mm  $\times$  125  $\mu$ m) under a heat applied at the bottom face of the PET ( $\epsilon = 0.8$ ), with increasingly zoomed images following the arrows (Nota bene: in the cross-section of the top region, the coatings look darker than the top surface in the first two images because the edge of each layer is indicated with a black line which is not resolved in large-area images: it is not an indication of a sudden drop in temperature in the top section of the sample, as is clearly demonstrated in the close-up images). b) Simulated temperature at the side face of each TE layer in the stacked TEG in (a) (at the hot side of the strip), with surface emissivities of 0.1, 0.3, and 0.8 (The temperature of 1<sup>st</sup> TE layer could represent the temperature on the top of PET sheet. The bottom side of PET is 305 K). c) Heat loss at the 5<sup>th</sup> TE layer compared to that at the 1<sup>st</sup> TE layer from results in (b). d) Heat transfer in the a-b plane of a TE strip under a heat applied at the side face. e) Temperature scan at the upper surface from the hot side along the length of a TE strip in (d).





**Figure 6.** Part a: Comparisons of the measured current, voltage, and calculated power output between TEGs structured in plane and in stacking. Both in-series stacked TEG and in-parallel stacked TEG with various TE strips (1–5) are presented. Part b: Plots of voltage, current, and power as the number of strips in the device, comparing the in-plane device with the stacked device.

For the in-plane TEG

$$FF = \frac{n \times 2 \times 20}{n \times 132} = 0.3 \quad (3)$$

where  $(n \times 2 \times 20)$  is the total area of TE strips, 132 is the strip area per footprint of the device regarding the in-plane TEG,  $(n \times 132)$  is the total area of device

footprint. (Notably, the FF of the in-plane TEG is independent of the number of strips once all strip parameters are fixed.)

Thus, compared with the in-plane TEG, the stacked TEG improves FF by

$$\text{Improvement\%} = \frac{0.8 \times n - 0.3}{0.3} \times 100\% = \frac{8n}{3} - 1 \quad (4)$$

It is clear that the stacked architecture improves FF immensely. Extrapolating these data to more layers, if we assumed that the linearity seen in Figure 6b continued, we would envisage that, for example, a 1000 TE-strip stacked TEG could generate a power of approximately  $(0.26/5) \times 1000 = 52$  nW while only occupying an  $a$ - $b$  dimension of  $50 \text{ mm}^2$  with about  $(11.8/5) \times 1000 = 2360 \text{ }\mu\text{m}$  thickness in stacking. To make this even thinner, decreasing thickness of acrylate insulating layers to the nanorange is of interest for further studies. A challenge will be to make an acrylate layer as thin (and smooth) as possible (which is dependent on the manufacturing process) while avoiding any charge leakage (shorting or tunneling). Various thinner electrically insulating but thermally conductive materials could be investigated although any such material would also need to avoid doping problems with the TE material, as the acrylate trialed here appears to do.

The negligible change in surface roughness (see Figure 1g) with more stacked layers suggests that stacking thousands of layers is feasible to achieve significant power output provided. Most importantly, afterward, these stacked TEGs (i.e., a single stacked strip in the plane view) can additionally be connected in plane (by printing to accommodate this thickness, e.g.,  $2360 \text{ }\mu\text{m}$ , in the side face of each stack), and thus further increasing TE output linearly.

### 2.3.3. In-Plane Connection of Stacked TEGs

As designed in Figure 9c,d, both in-series stacked strips (Figure 7a) and in-parallel stacked strips (Figure 7b) involving two or five TE strips were connected in plane (in series or parallel). A  $P_{\text{max}}$  of  $\approx 1.4$  nW (with  $V$  of  $\approx 5.5$  mV at the maximum power point) is obtained when four stacked strips are connected in series in the plane of the substrate, with each stacked strip containing five TE strips connected in series.  $I$  of  $\approx 4.2 \text{ }\mu\text{A}$  (with a  $P_{\text{max}}$  of  $\approx 0.7$  nW) is obtained with four stacked strips connected in parallel in the plane with each stacked strip containing five TE strips connected in parallel. Hence, an in-series mode for both in-stacking and in-plane connections benefits voltage (and power) output, while an in-parallel mode for both in-stacking and in-plane connections is favorable to current output. In this study, the maximum power density is  $0.003 \text{ nW mm}^{-2}$ , corresponding to the prototype of  $P_{\text{max}} \approx 1.4$  nW in this device that only stacks five TE strips.

## 2.4. Mechanical Tests

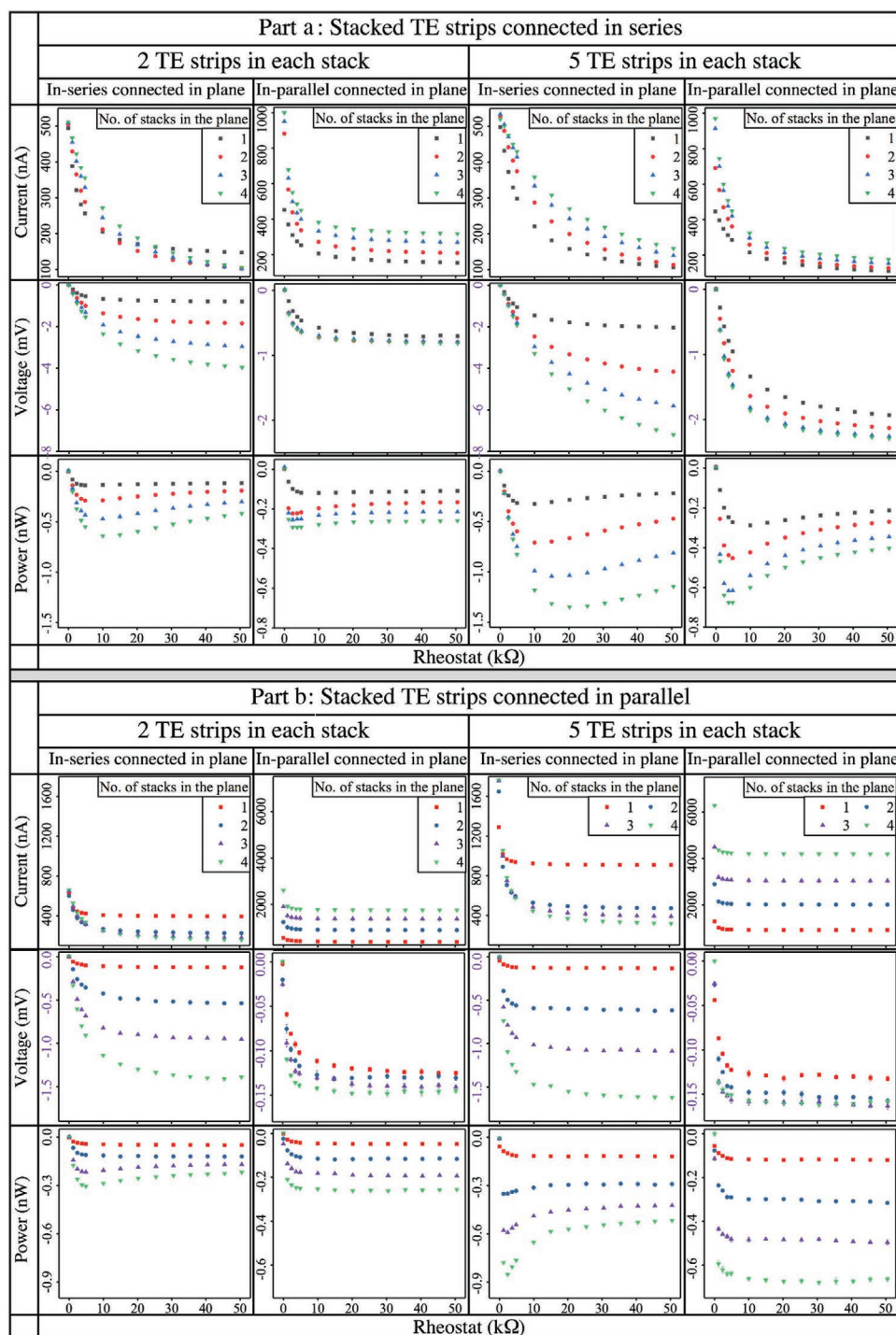
With a vision toward flexible/wearable electronics, the effect of mechanical deformation on these devices, during manufacture and in use, should be considered. A 1% strain is of interest for both situations, corresponding to a typical 85 N tensioning load between rollers in the Oxford R2R web coater and the stretchability requirement in use as reported in ref. [69]. Cyclical bending fatigue of a stacked strip, such as might be encountered in use as a flexible device, is explored. A relation of strain and displacement during buckling is

calculated as shown in Figure 8a, with respect to a  $\approx 21$  mm long specimen. A negligible change ( $\approx 5\%$ ) in the internal resistance is found in a stacked strip buckled under a 1% strain over 150 cycles (a 5000 s test), see Figure 8b, while the resistance significantly increases under a 2% strain and there is an upward trend in resistance over 75 cycles of the test. The 1% strain cycling is further analyzed with regards to TE performance, as shown in Figure 8c. The change in power output over the first 100 cycles is negligible, and afterward, a slight decrease ( $\approx 30\%$ ) is observed. By comparison, where the TE coating is directly deposited on PET sheets, under the same condition of 1% strain buckling, the internal resistance is measured to increase by  $\approx 15\%$ , and the TE performance is completely destroyed (a decrease of  $\approx 99\%$ ) after 12 cycles (see Appendix Figure SC1, Supporting Information, for more details). Hence, using the stacked architecture, both TE and metal strips are protected between the acrylate polymer layers, thus maintaining the TE performance.

## 3. Conclusion

A process based on low-cost high throughput roll-to-roll manufacture was used to explore the feasibility of fabricating a stacked TEG in the crossplane direction, which has the potential to locally provide sufficient power to wearable electronics, e.g., personal sensors and wireless earphones. Bi-Te and Cu films, each less than 100 nm thick, were fabricated as thermoelectric and contact materials, respectively. A  $\approx 1 \text{ }\mu\text{m}$  thick acrylate coating behaved as an electrically insulating layer in between Bi-Te and Cu layers.

1. AFM, SEM, and TEM images confirmed the smooth surface of these coatings. Most importantly, surface roughness remained steady as more layers were stacked due to the nature of the acrylate-layer deposition process. An SEM cross-sectional view of stacked layers presented a uniform stacking/alternating architecture.
2. XRD, XPS, and HRTEM identified the phases of Bi-Te and Cu films, indicating that the room-temperature sputtering could also produce good quality and crystalline films.
3. A temperature gradient arose in stacked TEGs from the bottom to top layers because a thick acrylate layer also behaved as a thermal insulator, thus the top thermoelectric layer would produce slightly less power than the bottom one due to a smaller temperature difference. A comparison of in-plane and stacked devices showed only a very small difference in power output, as predicted from the observed temperature change over five layers. As more layers were stacked of course the effect would increase. This would not be a significant problem in an architecture design that applied heat to the cross-section of the device.
4. The stacked architecture only occupied a one-strip dimension in the  $a$ - $b$  plane which significantly improved the spatial fill factor of the device.
5. In-series connection in plane of in-series stacked strips could generate a maximum voltage (and power) output, while in-parallel connection in plane of in-parallel stacked strips could generate maximum current output. Combinations of these



**Figure 7.** Part a: In-plane connection (in series and in parallel) of in-series stacked (2 and 5) TE strips. Part b: In-plane connection (in series and in parallel) of in-parallel stacked (2 and 5) TE strips.

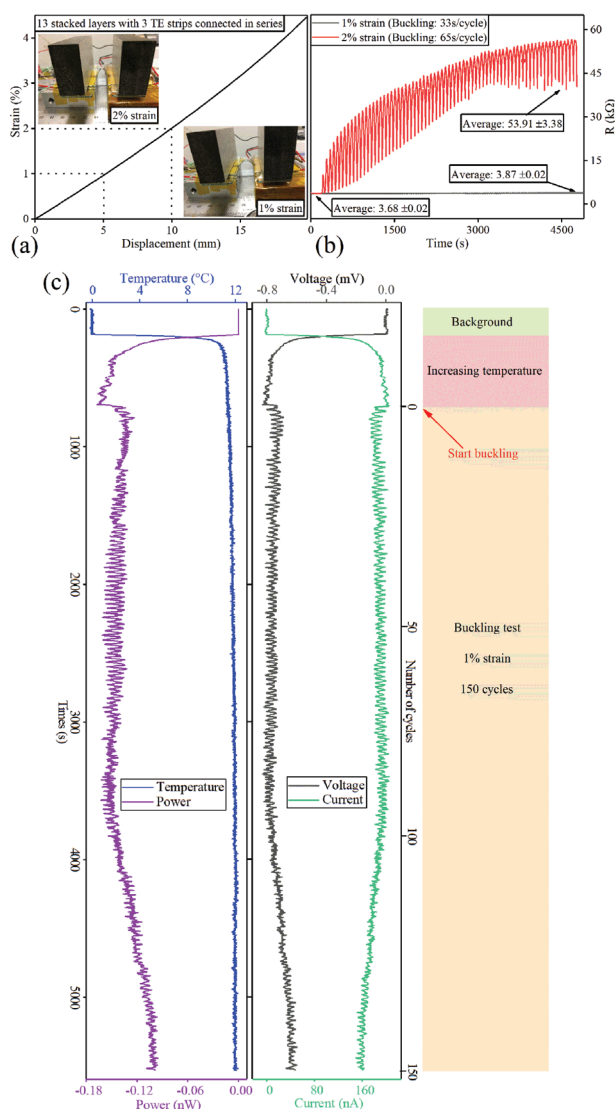
two could be used to design a power output suitable for applications of wearable devices that required a current or voltage power source.

6. An acrylate polymer matrix could protect the Bi-Te and Cu films, which maintained the performance of stacked TEGs within a 100-cycle buckling fatigue test under 1% strain.

## 4. Experimental Section

**Materials Fabrication:** All vacuum depositions were performed in an *Aerre Machine Vacuum Web Coater* operating under a high vacuum, which is typical for a low-cost high throughput R2R process. Bi-Te and Cu films were deposited onto flexible PET sheets (*Dupont Melinex*, 125  $\mu\text{m}$ ) at room temperature by DC magnetron





**Figure 8.** Cyclical strain testing under buckling of a series-connected stack of three TE strips. a) The calculated relation between the strain and displacement during buckling tests. b) Change in the internal resistance of a stacked TEG during the buckling test. c) Current, voltage, and power output of a stacked strip (with three TE strips) during the buckling test (Seebeck setup uses a load resistor of  $\approx 4$  k $\Omega$  which is close to the internal resistance of the stacked TEG to obtain a maximum power output. Temperature increases from 180 s and gets equilibrium at 690 s).

sputtering a three-inch target (purity of Bi<sub>2</sub>Te<sub>3</sub> and Cu: 99.999%, Mi-Net Technology Ltd.) under a condition of  $\approx 3.9 \times 10^{-4}$  mbar after 250 sccm Ar flow rate and 0.2 kW DC power. These conditions have been previously shown to give desirable film properties following a study of room-temperature deposition conditions.<sup>[63]</sup> Our latest work<sup>[79]</sup> also suggests Cu as the contact electrode in TEGs. Using polyimide tapes, PET substrates were attached on a 1.8 m circumference coating drum rotating at 25 m min<sup>-1</sup> during vacuum deposition, thereby allowing multiple passes under the deposition target source in a single deposition process. The film thickness was controlled by changing the deposition time, which was set at 3 min (Bi-Te) and 10 min (Cu) for these experiments. A target precleaning process without the substrate passing under the sputter target was carried out for  $\approx 3$  min prior to coating. In terms of acrylate coatings,<sup>[54]</sup>

tripropylene glycol diacrylate monomers were injected (0.6 mL min<sup>-1</sup>) into a hot tank ( $\approx 270$  °C) and then flash evaporated onto a rotating substrate (25 m min<sup>-1</sup>), followed by a plasma cure (using an Al cathode under  $3.8 \times 10^{-4}$  mbar after 200 sccm Ar and 5 sccm O<sub>2</sub> flow rate, 1.12 kW DC power). The thickness of the acrylate coating was controlled by adjusting the amount of monomer injected into the hot tank. The acrylate needs to function as an electrically insulating layer, so, although thinner layers are possible, in this study the polymer layer thickness was maintained at about 1  $\mu$ m to avoid the risk of electrical leakage or tunneling.<sup>[70]</sup>

A TEG was fabricated by depositing materials in sequence onto the PET substrate, as shown in Appendix Figure SD1d in the Supporting Information. Bi-Te, Cu, and acrylate coatings were patterned using polymer shadow masks (which could closely attach to the polymer substrate, thus avoiding shadowing issues, i.e., an unclear pattern, as can occur with typical solid stainless-steel masks). 125  $\mu$ m PET sheets were designed (AutoCAD) and cut (TS 3040 40W Laser cutter), as shown in Appendix Figure SD1a–c in the Supporting Information. There were two types of stacking depending on the electrical connectivity of the stack: in-parallel and in-series (Figure 9a). In the crossplane direction of the PET substrate, a single strip was stacked up using an in-parallel or in-series structure, and then these stacked single strips were connected by Cu contacts (under the same sputtering parameters as above) using polymer shadow masks (Appendix Figure SD1c, Supporting Information), either in series or in parallel (see Figure 9b–d) in the in-plane direction along the PET substrate.

**Sample Characterization:** The uncertainty values quoted for all quantitative figures included the sample-to-sample variation. Three independent batches were characterized for run-to-run variations: 4.4% in film thicknesses, 3.0% in electrical measurements, and 1.5% in Seebeck results.

The film thickness was characterized using a Veeco DekTak 6M stylus profilometer to measure the step height between the coating and substrate on partially masked (by a polyimide tape before deposition) Si wafers (averaged from six different locations).

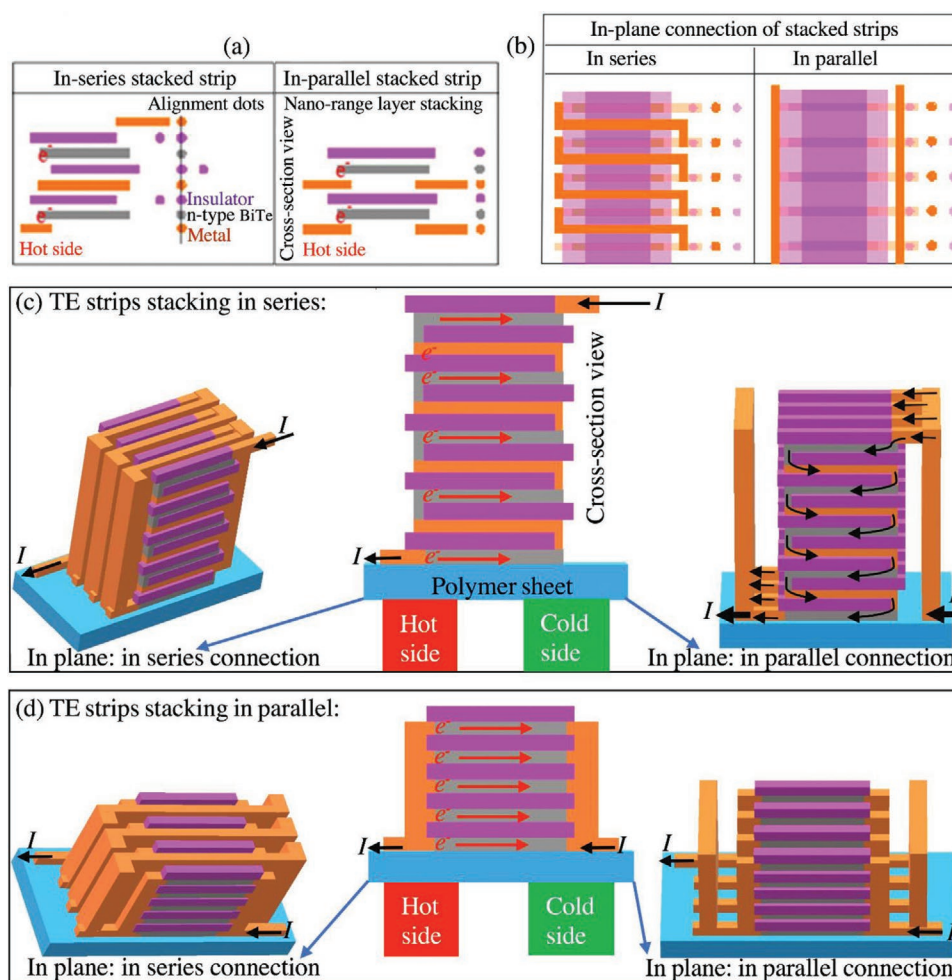
A field emission SEM, Zeiss Merlin, was used to analyze the film surface morphology and composition (EDX using point mode over six independent points in two locations), under 3.0 kV voltage, 100 pA current probe, 5.0 mm working distance, and 50.23 kX magnification. In addition, a cross-section view of stacked layers on a Si wafer was polished using a Gatan PECS II AJW Unit and analyzed using line scan mode in EDX (AZtec software). The composition/oxidation of the film was also checked using a ThermoFisher Scientific Al K $\alpha$  XPS system.

AFM (JEOL JSTM-4200D) using tips (NCHV-A, Bruker Ltd.) in tapping mode was used to characterize the film surface morphology and determine the surface roughness averaged from four different locations.

The film phase identification was assessed using XRD (Rigaku Miniflex diffractometer) with a Cu  $k_{\alpha}$  radiation ( $\lambda = 0.154$  nm) under 40 mA and 40 kV in a  $2\theta$  range of  $10^{\circ}$ – $80^{\circ}$  (step size:  $0.007^{\circ}$ ). To clearly identify diffraction peaks from the thin film, the XRD specimen was prepared in situ (in Oxford web coater) onto a (111) Si wafer. Data processing was performed in X'Pert Highscore software.

Held by the single-tilt holder ( $\pm 25^{\circ}$ ), the film-surface feature and crystallinity were characterized by a high vacuum JEOL 3000F analytical TEM under 200 keV connected to a 4 K Gatan Ultrascan filtered camera. Films were directly deposited onto lacey carbon-supported copper grids (300 mesh, Agar Scientific) and air dried for 2 h prior to observation. The data were then processed using Gatan Digital Micrograph software for grain size.

The thermal conduction through stacked layers was analyzed using a simple setup (see Figure 10). A thermocouple was placed on the sample surface. As a heater placed under the sample was turned on, a temperature on the sample surface was recorded as the temperature of the heater increased. Samples included a blank PET sheet and a stacked TEG on PET.



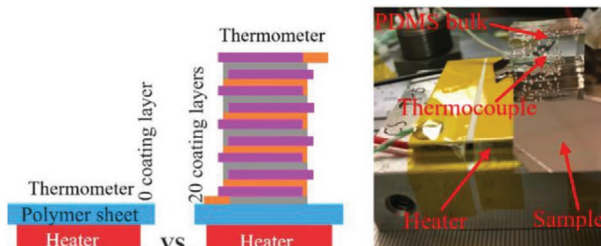
**Figure 9.** a) A cross-section view of an in-series and an in-parallel stacked strip (The orange colors indicate Cu strips, gray the Bi-Te sputtered TE layers, and purple the acrylate insulating layers. It demonstrates how the layers are stacked one by one ensuring that there is a contact region between Cu and Bi-Te layers. The acrylate layer insulates the region that it covers). b) Display of a top view of final devices with the lighter purple showing where offsetting of layers means there is less acrylate thickness. In-series/parallel connection in plane of c) in-series stacked strips and d) in-parallel stacked strips. The dimension of the Bi-Te strip is 2 mm × 20 mm. Nota bene: the “7” shape of Bi-Te or Cu layers in the cross-sectional view of in-series stacked TEGs is not real. The thickness is approximately uniform for each layer thus there is a slope at the acrylate step.

A simulation study using COMSOL was also conducted to analyze the thermal conduction in a stacked TEG. Heat transfers in both in-plane direction and cross-sectional direction were simulated, as a heat source of 305 K (i.e., the human-body temperature minus the temperature loss from the human skin to TEGs due to contact issues) was applied. The ambient temperature was fixed at 293 K. This simulation of heat transfer mainly considered three parameters: heat flux, surface-to-ambient radiation, and thermal contact (see Appendix COMSOL for more details). The latter two strongly depend on  $\epsilon$ ; however, this parameter varies a lot between the stacked materials in this study. Hence, heat transfer is simulated using three different  $\epsilon$  (see Table 1). Most of the material properties used for the heat-transfer simulation were directly from the material library in COMSOL, considered under an ideal situation to give the best result, while several parameters were adjusted from references as shown in Table 1.

The sheet resistance ( $R_s$ ) of the film was measured from an in-house custom four-point probe system by applying current ( $I$ ) in the range  $10^{-3}$ – $10^{-5}$  A through the outer two probes and simultaneously recording voltage ( $V$ ) between the two inner probes using an Agilent 34420 A nanovolt/micro-ohm meter (at nine different locations for each sample).

Then, the electrical resistivity was calculated by  $R_s$  and film thickness ( $t$ ) using the relation as follow

$$\rho = R_s \cdot t = \frac{\pi}{\ln 2} \left( \frac{V}{I} \right) \cdot t \quad (5)$$



**Figure 10.** Setup of the temperature measurement on a sample surface (the thermocouple was embedded in a polydimethylsiloxane block to hold the thermocouple lead in direct contact with the sample surface).

An in-house custom Seebeck setup was used to assess the Seebeck performance of Bi-Te films. By using two Peltier modules,  $\Delta T$  was applied between two opposing sides of a Bi-Te film, meanwhile, an open-circuit voltage ( $V_{OC}$ ) and short-circuit current ( $I_{SC}$ ) were recorded by applying a series of  $\Delta T$  in the range of 5–31 °C. The  $S$  was obtained from Equation (6)

$$S = \frac{\Delta V_{OC}}{\Delta T} \quad (6)$$

The Seebeck behavior of the fabricated TEG was characterized in the same Seebeck setup. The power output of the TEG was measured in a simple Ohm's circuit with a varying rheostat (0.84–50.5 k $\Omega$ ). By applying a constant  $\Delta T$  (11.4  $\pm$  0.2 °C) between the hot and cold sides of a TEG, two Keithley 2400 source meters were used to record voltage and current and then power was calculated using Ohm's law.

A cyclical bucking test was carried out on a rectangular-shaped sample (2 mm  $\times$  21 mm. 13 stacked layers on PET correspond to a total thickness of  $\approx$ 0.13 mm) within the in situ Seebeck system. The hot-side block was movable at a speed of 0.3 mm s<sup>-1</sup> using a 24 V DC geared motor. The strain was calculated according to the sample length and thickness, using a method as reported in ref. [80]. Both internal resistance and power output of a stacked strip were recorded during a cyclical bending test to characterize the fatigue behavior. The external load resistor was fixed close to the internal resistance of a stacked strip to obtain the maximum power output.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

## Acknowledgements

The project received the funding from Engineering and Physical Sciences Research Council [Grant No. EP/M015173/1] via the Wearable and flexible technologies enabled by advanced thin-film manufacture and metrology collaboration. The authors are grateful to Jennifer Holter, Dr. Colin Johnston, Dr. Clara Barker, Dr. Kai Zhang, Nicola Flanagan, Radka Chakalova, and Richard Turner for technical assistance. DuPont Teijin Films are gratefully acknowledged for providing PET substrate materials.

## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Keywords

bismuth telluride, flexible/wearable thermoelectric generator, roll-to-roll manufacture, room-temperature sputtering, stacking architecture

Received: March 1, 2021

Revised: June 22, 2021

Published online: August 7, 2021

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