Deep integration of power electronics in battery systems



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A thesis submitted for the degree of

Doctor of Philosophy

Trinity 2018

Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other university. This dissertation is my own work and contains nothing which is the outcome of work done in collaboration with others, except as specified in the text and Acknowledgements. Parts of the work have been presented at conferences and published in journal papers; these are specified in the text and referenced accordingly.

Efstratios Chatzinikolaou

July 2018

Acknowledgements

I would like to thank my supervisor, Dan Rogers, for his guidance, patience and continuous support over the course of my DPhil study. Thanks to his mentorship I like to think that I became a better engineer. I express my gratitude to the UK Engineering and Physical Science Research Council for funding this research through the Energy Storage for Low Carbon Grids project (EP/K002252/1). I would like to thank Alasdair Burchill (Cardiff University) for his work on the mechanical design of the experimental setup and Amir Eleffendi for his help on cycling the LTO cells and fruitful discussions. I would also like to thank all the researchers and PhD/DPhil students from the CIREGS group at Cardiff University and the Energy and Power Group at Oxford for making these years memorable. Finally, I would like to express my greatest gratitude to my family for their emotional and material support. And to Hara, for her love, companionship and continuous encouragement. This work would not have been possible without you.

Abstract

This thesis explores the concept of Power Electronics Enhanced Battery Packs (PEEBPs) where each cell (or small groups of cells) is connected to an individual converter and can be bypassed without interrupting operation of the system. The control flexibility provided can enhance system reliability by enabling failed cells to be bypassed online and improve balancing performance by controlling the duty cycle of each cell according to their respective capacity. However, the increased amount of power electronics compared to conventional system designs can potentially increase cost and power losses, while introducing additional control challenges especially for large-scale systems including thousands of cells.

This thesis introduces a linear programming framework for evaluating the balancing performance of PEEBPs that perform duty cycle balancing, compared to energy redistribution active balancing circuits. The numerical results demonstrate the superior balancing performance of PEEBPs, especially when using cells with extreme capacity variations. In order to compare battery energy storage system (BESS) designs with different levels of integration of power electronics in the battery pack, a design methodology is proposed that takes into account power losses, reliability and cost. This methodology is used to compare three competing system designs for a 1 MW/ 1 MWh BESS connected at 11 kV. The results of this case study indicate more than an order of magnitude improvement in reliability when using a PEEBP (when the failure rate of the cells is similar to that of the power electronic switches), with a relatively small increase in power losses (~2% lower efficiency for the deeply modular PEEBP considered in this study).

Regarding the implementation of a PEEBP, the Cascaded H-Bridge multilevel converter (CHB) is identified as an attractive candidate due to its modular design and the ability to perform direct DC-to-AC conversion. This work presents a theoretical analysis

of the operation of the CHB in a BESS application and proposes a method to achieve relative state-of-charge (RSoC) estimation by making pseudo open-circuit voltage (POCV) measurements. In order to address control complexity of large scale systems a hierarchical balancing control algorithm is proposed. In this case the system is organised in conceptual hierarchical layers and each layer is equipped with a local controller. The developed algorithm can achieve global cell balancing by balancing the objects of the intermediate layers of the system with limited information exchange between the local controllers. This hierarchical balancing algorithm is experimentally validated using a CHB-BESS comprising 144 lithium titanate cells.

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Nomenclature

Abbreviations

AC	alternating current
A-C2C	adjacent cell-to-cell balancing
ADC	analog-to-digital converter
(A)NPC	(active) neutral-point clamped converter
BESS	battery energy storage system
BMS	battery management system
C2P	cell-to-pack balancing
CHB	cascaded H-bridge multilevel converter
DAB	dual active bridge converter
DC	direct current
DCB	duty cycle balancing
D-C2C	direct cell-to-cell balancing
DG	distributed generation
EIS	electrochemical impedance spectroscopy
ERB	energy redistribution balancing
ES	energy storage
ESS	energy storage system
FC	flying-capacitor converter
FPGA	field-programmable gate array
IBP	intelligent battery pack
IGBT	insulated-gate bipolar transistor
LCO	lithium-ion cells with lithium-cobalt oxide cathode
LFP	lithium-ion cells with lithium-iron-phosphate cathode

LMO	lithium-ion cells with lithium-manganese oxide cathode
LTO	lithium-ion cells with lithium titanate anode
MMC	modular multilevel converter
MOSFET	metal-oxide-semiconductor field-effect transistor
MTTF	mean time to failure
NCA	lithium-ion cells with lithium-nickel-cobalt-aluminium oxide cathode
NiMH	nickel-metal hydride cells
NMC	lithium-ion cells with lithium-nickel-manganese-cobalt oxide cathode
NLC	nearest-level control modulation scheme
OCV	open-circuit voltage
PB	power block
PCB	printed circuit board
PEEBP	power electronics enhanced battery pack
PLL	phase-locked loop
POCV	pseudo open-circuit voltage
PWM	pulse width modulation
RC	resistor-capacitor
RES	renewable energy sources
RSoC	relative state-of-charge
SHE	selective harmonic elimination modulation scheme
SoC	state-of-charge
SoH	state-of-health
SPM	single particle model
STATCOM	static synchronous compensator
SVM	space vector modulation scheme
VHDL	very high speed integrated circuit hardware description language

Roman symbols

a_i	turn-on switching angle of element at position i [rad]
b	coefficient that determines the ‘size’ of the balancing circuit
$\cos\theta$	power factor of BESS
d_0	idle state duration [s]
f	grid frequency [Hz]

f_{SW} switching frequency of two-level converter [Hz]

I current of battery pack comprising series connected cells [A]

$I_{\max}$ maximum cell current [A]

$I_{\min}$ minimum cell current [A]

I_i average current of cell i [A]

I_i^{b} balancing current of cell i [A]

I_j^{p} average current of the cell(s) placed in position j [A]

I_{pb} balancing current that is returned from the balancing circuit to the pack [A]

I_{rms} RMS value of BESS output current [A]

I_{C} lithium ion cell DC current [A]

$I_{\mathrm{rms(i)}}$ RMS current in the CHB-BESS of the i th lithium ion cell [A]

K_{P} proportional gain

k_{on} turn-on switching loss constant calculated using the datasheet information [W/(A Hz)]

k_{off} turn-off switching loss constant calculated using the datasheet information [W/(A Hz)]

$\boldsymbol{L}$ vector of cell position in the priority list, where cells are sorted according to their relative state-of-charge

M modulation ratio of two-level converter

N_{a} number of cells that should always be active throughout the operation of the pack to ensure the output voltage is maintained at a constant level

N_{C} total number of cells in a BESS

N_{M} total number of battery modules in a BESS

$N_{\mathrm{P}}, N_{\mathrm{S}}$ number of parallel and series modules in a IBP-BESS

N_{PB} number of power blocks in a PB-BESS

N_{SS} number of series connected IGBTS in an arm of the centralized converter of the IBP-BESS

N_{HB} number of H-Bridge converter modules in each phase of the CHB-BESS

N_{o} number of additional cells for over-provision in the PB-BESS

N_{e} number of elements within a module

N_{m} number of modules within a bank

N_{b}	number of banks in the CHB
n_i	useable (or accessible) fraction of the capacity of cell i
n_{C}	number of cells within a module
n_{P}	number of parallel strings in a PB-BESS
n_{S}	number of series modules in a PB-BESS
$P_{\mathrm{CN}}, P_{\mathrm{SW}}$	conduction and switching losses of semiconductors [W]
P_{BP}	battery pack losses of the BESS [W]
P_{bal}	balancing losses of the BESS [W]
P_{C}	lithium ion cell power losses due to internal resistance [W]
$P_i(t)$	probability of the system being in state i at time t
Q_i	capacity of cell i [Ah]
Q_{n}	nominal cell capacity [Ah]
Q_{u}^*	maximum useable capacity as produced from the solution of the linear programming problem [Ah]
Q_{u}	useable capacity achieved experimentally [Ah]
Q_i^{v}	virtual capacity of cell i [Ah]
Q_{M}	nominal battery module capacity [Ah]
$Q_{\min}$	$= 0.95Q_{\mathrm{M}}$. Minimum module capacity [Ah]
$\boldsymbol{Q_{\mathbf{b}}}$	vector of bank layer capacities
$\boldsymbol{Q_{\mathbf{m}}^{i}}$	vector of module layer capacities for bank i
$\boldsymbol{Q_{\mathbf{e}}^{ij}}$	vector of element layer capacities for module j of bank i
r	$= \frac{N-N_{\mathrm{a}}}{N}$. Cell redundancy ratio
r_{v}	voltage redundancy ratio
r_{e}	energy redundancy ratio
R_{Q}	on-state resistance of an IGBT [Ω]
R_{D}	on-state resistance of a Diode [Ω]
R_{F}	on-state resistance of a MOSFET [Ω]
R_{C}	internal resistance of a lithium ion cell [Ω]
R_i^{L}	resistance of RC branch of cell i associated with long time-constant transient phenomena [Ω]
SoC_i	state-of-charge of cell i [%]

SoC_i^0 initial state-of-charge of cell i [%]

SoC_i^{T} state-of-charge of cell i at the end of operation [%]

SoC^{ijk} state-of-charge of element k in module j of bank i [%]

SoC^{ij} average state-of-charge of elements in module j of bank i, $SoC^{ij} = \frac{\sum_{k=1}^{N_{\mathrm{e}}} SoC^{ijk}}{N_{\mathrm{e}}}$ [%]

SoC^{i} average state-of-charge of modules in bank i, $SoC^{i} = \frac{\sum_{j=1}^{N_{\mathrm{m}}} SoC^{ij}}{N_{\mathrm{m}}}$ [%]

T length of operation (the length of one charging or discharging cycle) [h]

T^* $= \frac{Q_{\mathrm{u}}^*}{\sum_{i=1}^{N} I_i}$. Length of operational time as calculated from the solution of the linear programming problem [h]

t_i^{b} balancing time of cell i [h]

t_i^{c} 'charging' balancing time i.e. the time during which cell i receives charge [h]

t_i^{d} 'discharging' balancing time i.e. the time during which charge is extracted from cell i [h]

t_i^{cc} 'charging' time of cell i through circuit i i.e. the time during which the balancing circuit i is extracting energy from cell $i+1$ to cell i [h]

t_i^{cd} the 'discharging' time of cell i through circuit i, that is the time during which the balancing circuit i is extracting energy from cell i to cell $i+1$ [h]

t_{ij} total time that cell i spends at position j [h]

V_{ref} reference voltage of the CHB-BESS [V]

V_{CHB} output voltage of CHB converter [V]

V_{e} voltage of the battery module within each element of the system [V]

V_{rms} RMS value of (CHB) BESS output voltage [V]

V_i^{OC} open-circuit voltage of cell i [V]

V_i^{POC} pseudo pen-circuit voltage of cell i [V]

V_i Terminal voltage of cell i [V]

V_{D} on-state voltage drop of an IGBT [V]

V_{Q} on-state voltage drop of a diode [V]

V_{M} battery module nominal voltage [V]

V_{pk} peak AC output voltage of the BESS [V]

V_{max} battery module maximum voltage [V]

V_{C} lithium ion cell nominal voltage [V]

V^{ijk} voltage of element k in module j of bank i [V]

$V_{\max}^{ij}$ maximum output voltage of elements in module j of bank i, $V_{\max}^{ij} = \sum_{k=1}^{N_{\mathrm{e}}} V^{ijk}$ [V]

$V_{\max}^{i}$ maximum output voltage of modules in bank i, $V_{\max}^{i} = \sum_{j=1}^{N_{\mathrm{m}}} V_{\max}^{ij}$ [V]

$V_{\max}$ maximum output voltage of the system, $V_{\max} = \sum_{i=1}^{N_{\mathrm{b}}} V_{\max}^{i}$ [V]

V_{ref}^{ij} voltage reference for the controller of module j of bank i [V]

V_{ref}^{i} voltage reference for the controller of bank i [V]

V_{m} average module voltage [V]

V_{b} average bank voltage [V]

V_{S} voltage step (i.e. the variable used to control balancing priority between layers) [V]

Greek symbols

Δ maximum variation e.g. ΔSoC represents difference between maximum and minimum bank SoC

η efficiency of balancing circuit

θ angle of grid voltage [rad]

<u>failure rates [failures/10^6h]</u>

λ_{C} of lithium ion cell

λ_{V} of power converter

λ_{A} of capacitor

λ_{X} of transformer

λ_{D} of diode

λ_{Q} of IGBT

λ_{F} of MOSFET

λ_{R} $= n_{\mathrm{S}} n_{\mathrm{C}} \lambda_{\mathrm{C}}$. Of a string of cells in a PB-BESS

λ_{M} $= n_{\mathrm{C}} \lambda_{\mathrm{C}}$. Of cell module

λ_{P} $= (\lambda_{\mathrm{M}} + \lambda_{\mathrm{F}}) N_{\mathrm{P}}$. Of parallel modules in a IBP-BESS

λ_{W} $= \lambda_{\mathrm{Q}} + \lambda_{\mathrm{D}}$. Of a switching device

λ_{A} of converter arm in IBP-BESS

λ_H $= 4\lambda_F$. Of an H-Bridge

λ_Θ of one phase in a CHB-BESS

π factors

π_T temperature factor

π_A application factor

π_Q quality factor

π_E environmental factor

π_V voltage stress factor

π_{CC} contact construction factor

π_C capacitance factor

π_R power rating factor

Quick reference guide

Chapter 3

Duty cycle balancing architectures (DCB): Circuits that perform cell balancing by controlling the duty cycle of each cell according to their respective capacities.

DCB-DC: Power electronics enhanced battery packs with a DC output voltage that perform duty cycle balancing.
DCB-AC: Power electronics enhanced battery packs with an AC output voltage (such as the Cascaded H-bridge converter based battery pack) that perform duty cycle balancing.

Energy redistribution balancing architectures (ERB): Circuits that perform cell balancing by redistributing charge between cells in the pack.

D-C2C: Circuits that perform direct cell-to-cell balancing by transferring charge between any two cells in the battery pack.
A-C2C: Circuits that perform adjacent cell-to-cell balancing by transferring charge only between neighbouring cells in the battery pack.
C2P: Circuits that perform cell-to-pack balancing by transferring charge between one or more cells to the whole battery pack.

Chapter 4

Competing Battery Energy Storage System designs:

PB-BESS: Conventional battery system design where the system is divided in power blocks of lower power and energy ratings that operate in parallel. Each power block comprises a battery pack where the cells are connected in parallel and in series in a static manner coupled to a passive balancing circuit, a centralised two-level DC/AC converter and a step-up transformer.

IBP-BESS: Battery system with an ‘intelligent battery pack’ i.e. a deeply modular DC battery pack were MOSFETs are used in series and in parallel with the battery modules, allowing to bypass failed modules online and perform duty cycle balancing. Due to this control flexibility a large number of modules can be connected in series to achieve a higher DC link voltage without the need of a transformer. A centralised two-level converter is used in this case, where each switch is a series connection of IGBTs.

CHB-BESS: A battery system based on the cascaded H-bridge converter with each battery module individually controlled by an H-bridge. This system configuration enables bypassing a single module in case of failure or in order to perform duty cycle balancing. The DC voltages of the modules can be combined in order to achieve direct DC-to-AC conversion without the need of a separate centralised converter.

Chapter 1 Introduction

This thesis explores the concept of integrating power electronics into battery packs in order to overcome cell-to-cell variations that could otherwise limit the performance of battery systems. The aim is to present the tools that will evaluate the benefits and drawbacks of this approach and to address the control challenges in large scale modular systems. This chapter starts by discussing the role of energy storage systems in future grids, focusing on systems using lithium-ion batteries. The main characteristics of lithium-ion cells are presented and the challenges in grid scale systems are identified. The role of the battery management system is discussed focusing on the functions of state-of-charge estimation and cell balancing. Finally, the current trends in converter topologies for battery systems are reviewed and the reader is introduced to the concept of modular power electronics enhanced battery packs. The objectives and research contributions of this thesis are presented at the end of this chapter.

1.1 Grid scale energy storage

The electrical grid is constantly evolving, driven by the need to meet increasingly higher standards in efficiency, reliability, power quality and cost-of-service [1], while addressing global environmental issues such as climate change, national security concerns and a growing need to reduce cost and environmental impact by better managing energy usage [2]. Achieving these objectives will require a shift away from traditional centralised large-scale generation with a passive distribution grid, to an active network that enables bi-directional power flow between the distribution and transmission systems and integrates larger quantities of distributed generation (DG) [3]. Although DG refers to

various nonconventional technologies that generate electricity, the increased adoption of sustainable energy policies has propelled the use of renewable energy sources (RES) [4].

Renewable energy is the energy that derives from natural processes (e.g. wind, solar, biomass, biogas etc.) that do not involve consumption of exhaustible resources such as uranium or fossil fuels. The increased penetration of RES can be attributed to their declining cost, driven by technological advances, economies of scale, market competition and clear government commitment [5, 6]. The United Kingdom (UK) in particular has signed up to the European Union renewables energy directive which includes the target of achieving 15% of its energy consumption from RES by 2020 and a further reduction of greenhouse gas emission to at least 80% below the 1990 levels by 2050 [7, 8].

An important drawback of RES such as wind and solar, is their intermittent nature and unpredictable behaviour [9]. The high penetration of this stochastic renewable generation can potentially lead to a severe degradation of the power system's operation, creating problems such as voltage and frequency fluctuations, stability issues and violation of power line capacity. These problems are especially challenging when RES are connected to weak power grids with reduced grid inertia due to the increased use of converter-interfaced power generation [10, 11].

Energy storage (ES) technologies can be a key element in facilitating integration of RES since they decouple the time of generation and consumption [12]. According to [13], ES can be a major factor in defining the optimal combination of low carbon generation technologies required to deliver a cost-effective shift to a low carbon energy system, since the flexibility provided by ES could reduce the integration cost of RES.

Traditionally ES has been used in energy shifting applications, to provide arbitrage by storing energy at off-peak times when it is cheap and release it at peak demand when the price is higher [14]. Other energy shifting applications include load levelling and peak shaving which can help delay investments in infrastructure by presenting flatter loads with smaller peaks to generators [15]. These services operate at a timescale of up to several hours. Energy storage is also used to improve grid stability providing ancillary services such as frequency regulation, voltage control and spinning reserve [16, 17]. These services require that the energy storage system (ESS) is able to respond to small timescale fluctuations in demand and generation, ranging from seconds to tens of minutes. ES can also enhance grid power quality by improving harmonic distortion of

voltages and currents or by providing 'fault ride through' capability by temporarily supplying the load until the standby power generation reaches its operating point [18].

ESSs can be characterised based on their power rating, energy rating and their operation cycles/lifetime (cycles/year). According to their power ratings ESSs are categorised as large-scale (GW), medium-scale (MW) or micro-scale (kW). The total time required to fully (dis)charge the system at the rated power depends on the energy rating of the ESS. Based on its energy rating, an ESS can be characterised as very short-term (milliseconds), short-term (seconds), medium-term (minutes) and long-term (hours) storage [19]. Accordingly, the services provided by ESSs can be categorised in power services which require ESSs with energy ratings lower than medium-term and energy services that require long-term ESSs [20].

The impact of ES services is highly dependent on the location of the ESS, which can be integrated at the transmission level, distribution level and customer side (i.e. behind-the-meter). Each level involves different stakeholder groups such as power system operators, utilities and customers as well as different ES services. The grid services provided by ES to the three stakeholder groups (system operators, utilities, customers) at the different levels of the power network are presented in Fig. 1.1. System operator services include medium and long-term ES for arbitrage, load levelling, peak shaving, nonspinning reserve and black start. They also include short term ES for ancillary services such as voltage and frequency control and spinning reserve. Centralised ES (GW range) located at the transmission level or decentralised ES at the distribution level (MW range) can be used to facilitate the integration of intermitted RES and enhance grid resiliency by providing power in critical facilities such as hospitals, in case of weather-caused grid outages [21]. Utility services can use ES to delay upgrades in infrastructure and make better use of the existing assets by providing peak-shaving and load shifting services on the transmission and distribution side. ESSs located behind-the-meter can provide direct services to end-consumers and can also indirectly benefit system operator and utilities. These services aim at lowering overall system costs by using price signals to incentivise end-users to adjust their load profile [22]. ES at the consumer level also facilitates dispersed generation from RES such as PVs and can improve power quality by providing enough energy to 'ride through' short-term power delivery anomalies and

provide backup power to sensitive consumers at scales ranging from seconds to hours [18].

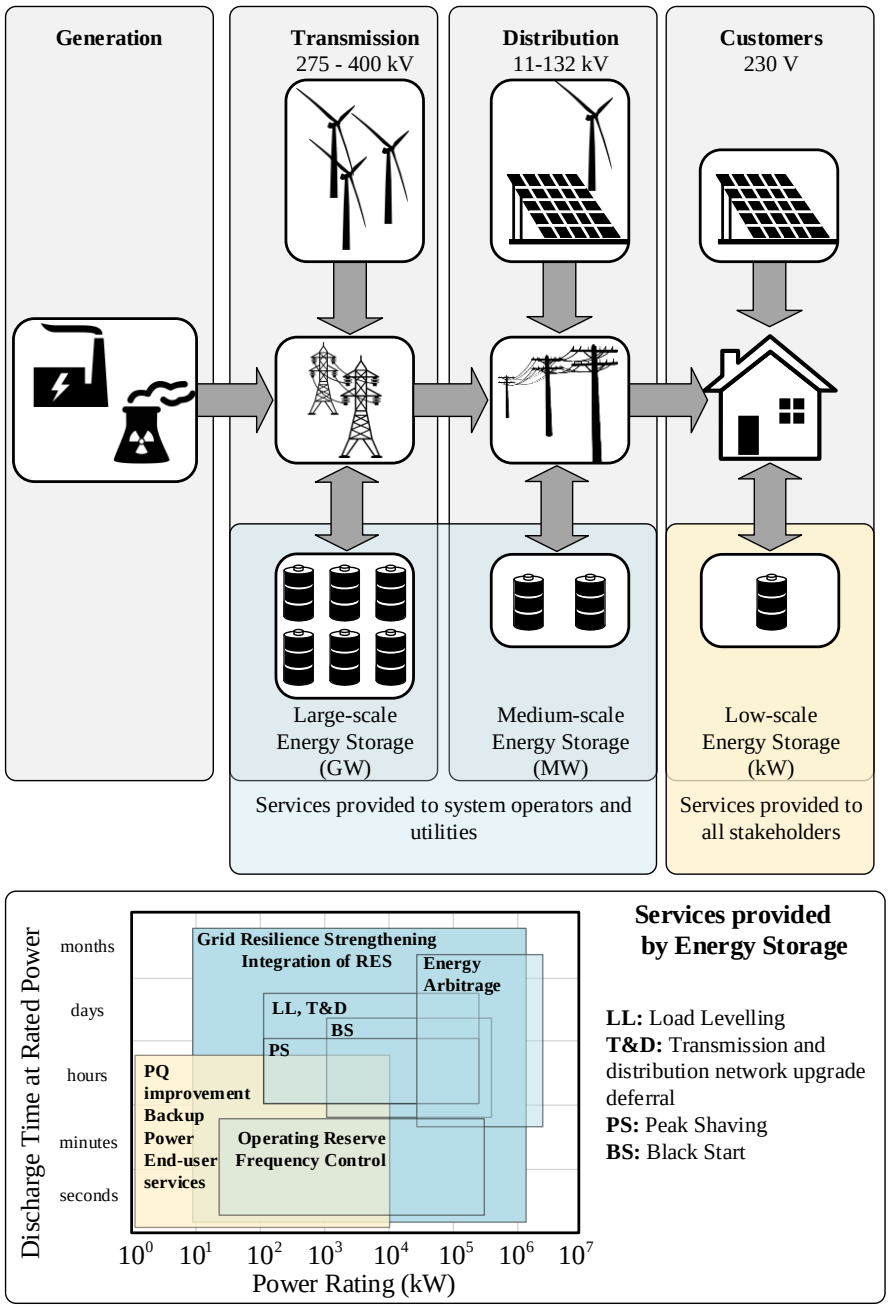


Fig. 1.1 Energy storage at different grid locations and grid services provided to different stakeholders (adapted from [12]). The blue colour indicates services provided to system operators and utilities while the beige colour indicates services provided to all stakeholders.

The value of the grid services depends highly on the location of the ESS on the electricity grid as well as the stakeholders involved. As a general rule, ES can provide more services to the system when located closer to the end-customer [12]. Low-voltage (<1 kV) micro-scale decentralised ES on the customer side (e.g. residential, commercial or industrial buildings) can theoretically provide all the services presented in Fig. 1.1. The challenge is to ensure that this decentralised ES is operated in a way that is mutually beneficial for all the stakeholders involved e.g. reducing the electricity cost of the end-customer while providing ancillary services to the distribution network operator. On the other hand, when decentralised medium-scale ES is deployed at the distribution network, it losses the ability to deliver bill-management services to customers but is still able to deliver services to system operators and utilities such as facilitating the integration of RES. At the transmission network, centralised ES losses the ability to provide services to the end-customers and utilities (e.g. deferral of distribution network upgrades) and is exclusively used to support system operators.

1.1.1 Overview of energy storage technologies

The choice of ES technology depends on various parameters such as the power and energy ratings of each application, the number of charge-discharge cycles, sizing constraints and operating temperature [23]. According to the previous section, power services require short and very short-term duration storage whereas energy services require medium and long term duration systems. ESSs are most commonly classified based on the form of the energy storage vector: mechanical, electrical, thermal, chemical and electrochemical energy storage [24, 25]. The various energy storage technologies with their corresponding power and energy ratings are presented in Fig. 1.2.

Currently, there is not a single 'winning' ES technology that covers all applications at the lowest cost and so different types of ES are required in order to deliver different services to the grid. For energy services, storage technologies such as pumped hydro, compressed air, flow batteries, hydrogen and thermal ES can be used, while power services can be satisfied by supercapacitors, flywheels and superconducting magnetic ES. The discharge times of electrochemical ES technologies can range from minutes to hours [26, 27], making these technologies attractive for both power and energy applications. This thesis focuses on BESSs using lithium-ion (Li-ion) batteries.

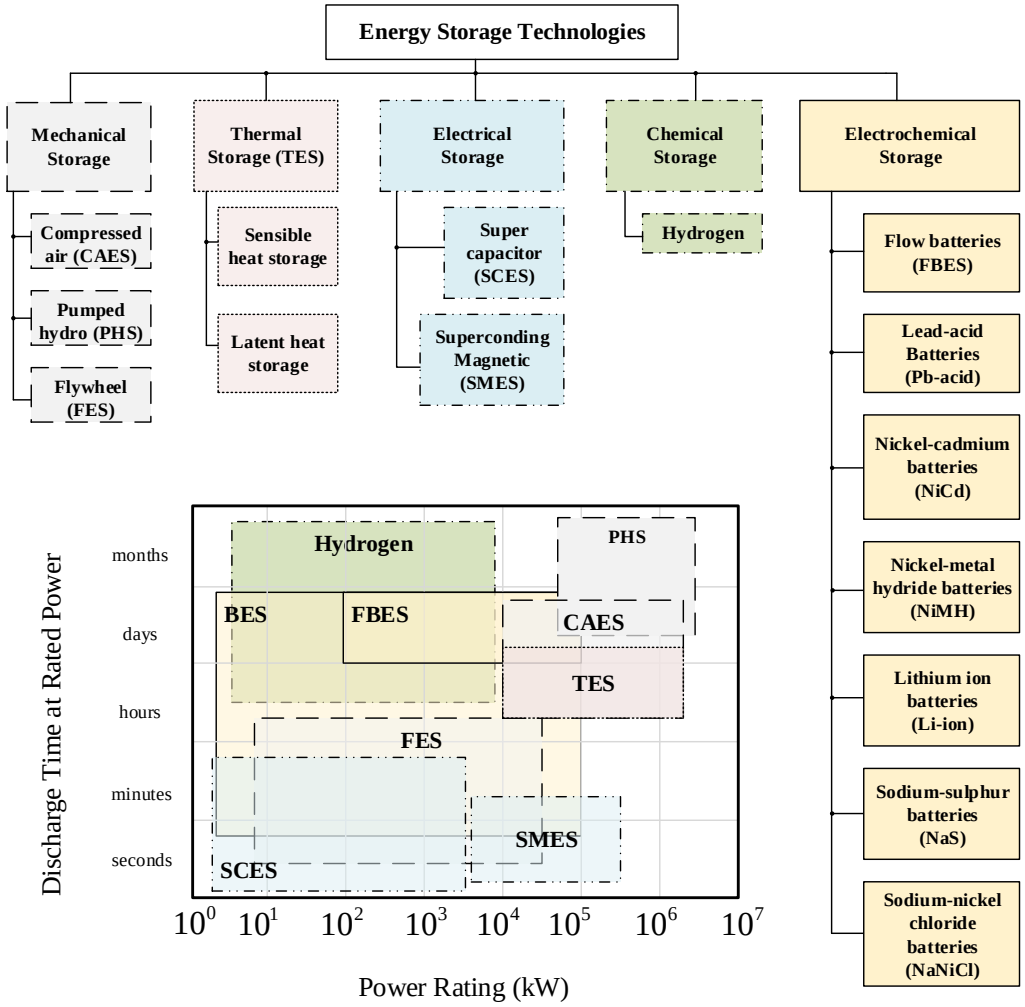


Fig. 1.2 List of energy storage technologies with their respective discharge times and power ratings (adapted from [12]).

A typical BESS comprises three main parts as presented in Fig. 1.3:

1. The battery pack, including Li-ion cells connected in series and in parallel.
2. The Battery Management System (BMS), including the software and hardware used to monitor the states of the cells (i.e. cell voltage, temperature, current) and ensure the safe operation of the battery.
3. The converter interface used to connect the DC battery pack to the AC grid and control the power supplied to/from the battery bank, as dictated by the BMS and system controller.

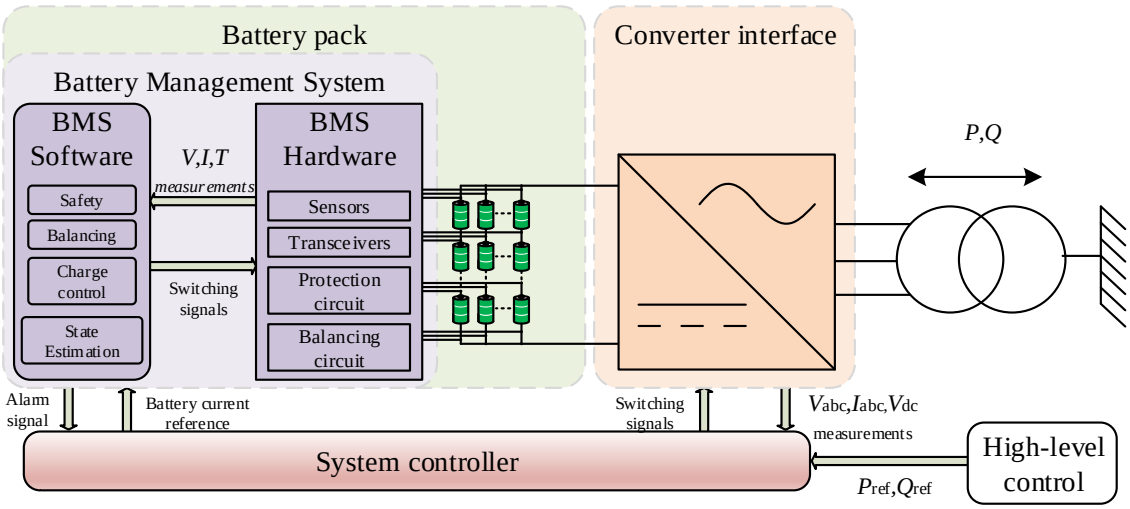


Fig. 1.3 Main parts of a battery energy storage system.

1.2 Lithium-ion batteries

The term Li-ion battery is used to characterise any battery that utilizes insertion reactions for both positive and negative electrodes with lithium ions as charge carriers [28]. Consequently, this term does not describe a single chemistry but rather a family of chemistries that comply with the above definition. The fundamental building block of a Li-ion battery, the Li-ion cell, consists of a positive electrode (cathode) and a negative electrode (anode) with an electrolyte between them that is used to support the movement of Li-ions from one electrode to the other during charge and discharge (Fig. 1.4). When charging, the lithium atoms in the cathode become ions and migrate from the cathode to the anode through the electrolyte. At the anode Li-ions recombine with the electrons that flow to the same direction through an external circuit and the produced lithium atoms are deposited between the carbon layers. This reaction is reversed during discharge. The electrochemical reaction for a cell with a graphite anode is:

$$\mathrm{MO_y + Li^+ + e^-} \underset{\text{charging}}{\overset{\text{discharging}}{\rightleftharpoons}} \mathrm{LiMO_y} \qquad \text{(cathode)}$$

$$\mathrm{LiC_6} \underset{\text{charging}}{\overset{\text{discharging}}{\rightleftharpoons}} \mathrm{Li^+ + e^- + C_6} \qquad \text{(anode)} \tag{1.1}$$

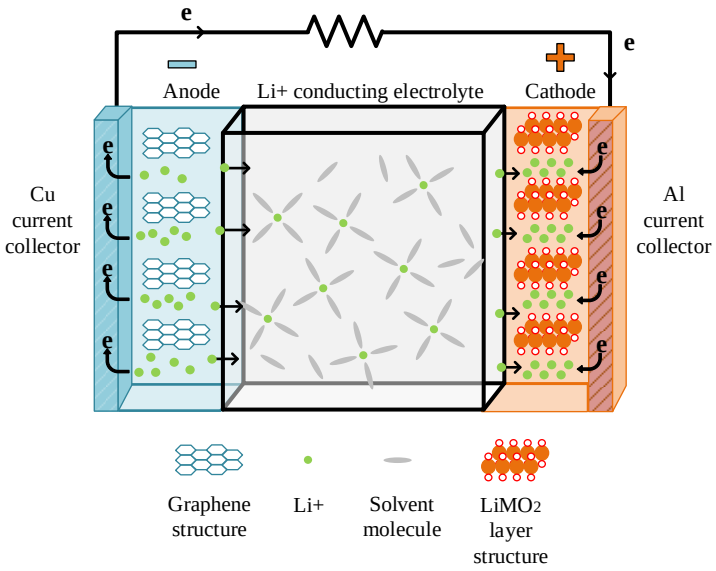


Fig. 1.4 Structure of a Li-ion cell (adapted from [13]).

Although a wide range of cathode and anode materials can be combined to create new Li-ion cells, only a limited number of Li-ion chemistries have been commercialized so far. The anode active materials that have been used for mass production are graphite, hard carbon, soft carbon and lithium titanate (LTO). The cathode active materials most commonly employed are lithium-cobalt oxide (LCO), lithium-nickel-manganese-cobalt oxide (NMC), lithium-nickel-cobalt-aluminium oxide (NCA), lithium-manganese oxide (LMO) and lithium-iron-phosphate (LFP) [13, 28, 29]. Aluminium (Al) and copper (Cu) are used as the current collectors for the cathode and anode respectively, since they exhibit the desired stability and oxidation potentials [30].

1.2.1 Li-ion cells for grid applications

The advantages of Li-ion over other cell chemistries are the high energy density (250–600 Wh/L), high specific energy (160–200 Wh/kg) [31, 32], fast response time (milliseconds) [32], long cycle lifetime (400–1500 cycles, with newest commercial batteries exceeding 3500 cycles), low self-discharge rate (around 2%–5% per month) [12], high specific power (around 250–2000 W/kg) [12], very high cycle efficiencies (around 90%–97%) [33] and relatively high nominal cell voltages (up to 3.7 V). Moreover, Li-ion cells do not suffer from memory effects (i.e. a reduction in cell capacity

after repeated cycles, as the cell appears to 'remember' the depth of discharge from the previous cycle) [13], they are more environmentally friendly compared to other battery technologies e.g. nickel-metal hydride (NiMH) and the expansion of worldwide production capacity is continuously driving their cost down. It is worth mentioning that although the unit cost in 2009 was estimated between 900 and 1300 $/kWh [34], this was reduced to about 600 $/kWh in 2012 [35] and today (2018) a battery pack costs around 200 $/kWh.

The properties of the cells (such as the energy and power density) depend on the materials used for the electrodes and the electrolyte, as well as the interface area between the components. Different variations of Li-ion cells can thus be engineered according to the specific requirements of each application. In grid storage applications, energy density requirements are not as strict as in portable electronics or automotive applications due to the extensive site area of windfarms and photovoltaic parks, but it becomes important for domestic ESSs. Regarding the required C-rates, less than 3 C is sufficient for most grid services (the C-rate represents the rate at which a battery is (dis)charged relative to its capacity e.g. 2 C is equivalent to the current required to fully (dis)charge the battery in half an hour). On the other hand, cell characteristics such as long cycle life, robustness and good thermal stability are mostly preferred [28]. The dominant anode material in Li-ion batteries for the grid is graphite due to its low potential compared to the lithium metal electrode that maximises the energy of the cell. Regarding the cathodes, there is a focus on utilising low-cost elements such as manganese and iron as the basis of the materials to replace costly and toxic elements such as cobalt. Lithium manganese oxides and related materials containing other transition metals such as nickel are already in use [36]. NMC has similar or higher achievable specific capacity (i.e. Ah/kg) compared to the LCO and similar operating voltage, while having lower cost, better cycle life and safety [30]. The LMO chemistry uses low-cost materials that are naturally abundant but has insufficient long-term cyclability [30, 37]. The NCA chemistry provides high specific energy but at a relatively high cost due to the use of cobalt and nickel [28]. The LFP cells offer increased safety and longer cycle life at the expense of lower specific energy (typically 150 mAh/g) and voltage [28]. As an alternative anode material, LTO has some advantages over graphite such as superior safety, higher C-rates and high cycle life but at the cost of lower cell terminal voltage and consequently lower energy density [13]. Some examples of

commercially available cells for grid storage applications, based on the above chemistries are presented in Table 1.1.

Table 1.1 Lithium-ion cell datasheet values [29].

Cell identification	SDI94Ah	NCR18650B	US26650FTC1	SCiB titanate
Manufacturer	Samsung	Panasonic	Murata	Toshiba
Cathode material: Anode material	NMC:C	NCA:C	LFP:C	MOx:LTO
Cell capacity (Ah)	94.0	3.2	3.0	20
Energy density (Wh/L)	355	676	278	177
C-rate (discharge/charge)	3 C/1 C	2 C/0.5 C	6 C/1 C	8 C/>3 C
Cycle life (full equivalent cycles until 20% capacity lost)	>5,000	320	>6,000	10,000
Voltage range (V)	2.70–4.15	2.50–4.20	2.0–3.6	1.5–2.7
Nominal voltage (V)	3.7	3.6	3.2	2.3

There are many examples of grid storage applications using the above Li-ion chemistries: A 1 MW/1 MWh LMO based BESS has been installed at the Reese Technology Centre in Lubbock, Texas as part of a Smart Grid Demonstration Project (SGDP) [38]. A 1.2 MW/0.9 MWh BESS using NCA cells was built in Sardinia, Italy as part of the Storage Lab project that aims at the installation of multi-technology storage plants of 16 MW in Sicily and Sardinia in order to support the grid as well as host research activities to develop smart grid applications [39]. The Shin-Gimje substation BESS in South Korea, rated at 24 MW/9 MWh was, at the time of commissioning, the largest capacity NMC system used for frequency regulation in the world [40]. A 2 MW/4 MWh LFP BESS operates in Dublin, California as part of a smart grid demonstration project [41] and the same battery chemistry is used in a 6 MW/36 MWh BESS in China, as part of the Zhangbei National Wind and Solar Energy Storage and Transmission demonstration project [42]. In Leighton Buzzard, Bedfordshire, UK the Smarter Network Storage facility rated at 6 MW/12 MWh comprises over 50,000 LMO cells and is used to assess the value of ES across the power system [43]. Rated at 2 MW/1 MWh and including 21,120 LTO cells, the Willenhall BESS is a research facility used to provide services to the grid with a response time of 0.4 s [44]. Currently, the world's largest Li-ion BESS rated at 100 MW/129 MWh is the Hornsdale Power Reserve, built by Tesla in Jamestown, South Australia [40]. The system includes NMC cells that are preferred by the company for their grid storage applications due to their longer cycle life and more

stable performance compared to the (more energy dense) NCA cells used in the company's automotive batteries [13].

1.2.2 Challenges when using Li-ion cells

Since the voltage of a single cell is limited to less than 5 V and the capacity is usually less than 100 Ah (i.e. a maximum cell energy < 500 Wh), cells are connected in series and in parallel in order to achieve the required voltage and capacity ratings for the system [45]. From the aforementioned grid storage project examples it can be seen that BESSs, ranging from a few kilowatts to hundreds of megawatts, require battery packs that comprise thousands to hundreds of thousands of cells. The basic arrangement of cells in a BESS along with the sensing and balancing hardware is called a battery module. Battery modules are combined together to form a battery pack as presented in Fig. 1.5.

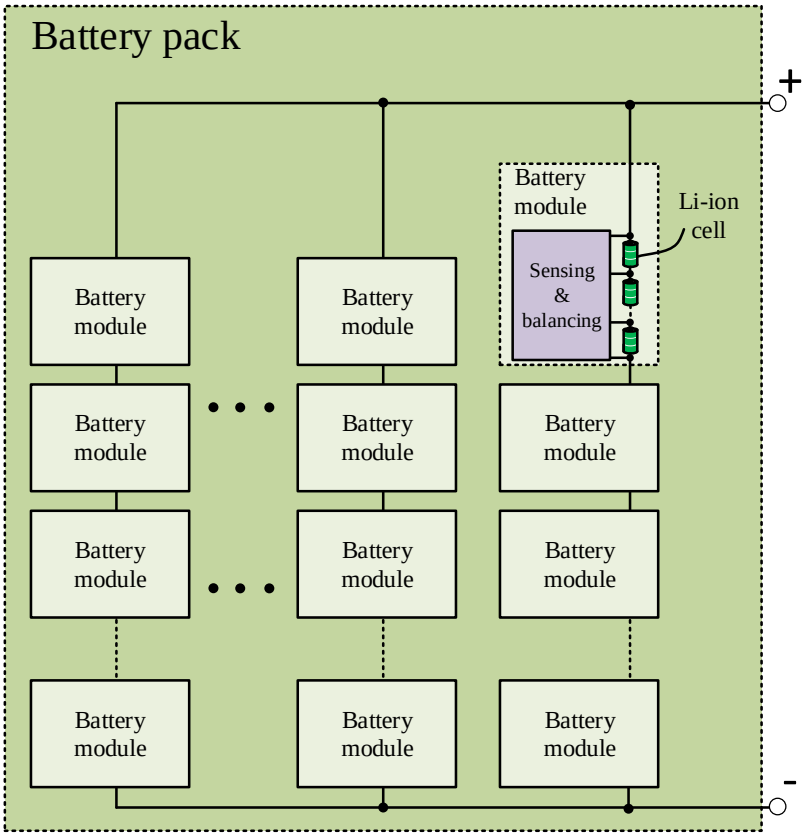


Fig. 1.5 Basic architecture of a battery pack.

Building reliable and long lasting battery packs can be challenging due to cell-to-cell variations in capacity and internal resistance observed even between cells of the same size, type and manufacturer [46, 47]. Cell-to-cell variations are caused by manufacturing tolerances or varying shipping and storage conditions [48, 49] and are exacerbated due to ageing [50, 51].

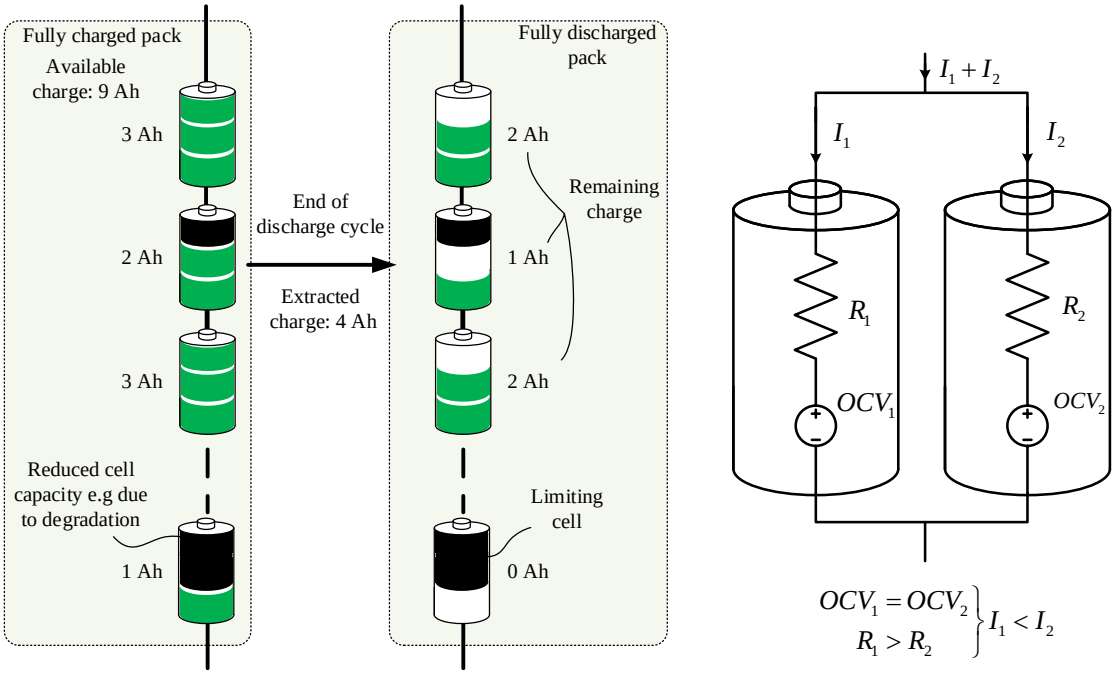


Fig. 1.6 Example of cell-to-cell variations and their impact a) on the useable capacity of series connected cells b) on the cell currents of parallel connected cells. Each cell is divided in three "capacity sections" with the following colour code: black indicates that no charge can be stored in this section e.g. due to degradation, green indicates that there is 1 Ah charge stored in this section and white indicates an empty section that can store 1 Ah.

These variations can negatively affect the performance of the pack. When connecting cells in series the total capacity is limited by the lowest capacity cell, as demonstrated in Fig. 1.6a [52]. For parallel connected cells, varying cell impedances result in different currents flowing through cells (Fig. 1.6b) causing state-of-charge (SoC) unbalance, non-uniform temperatures and varying degradation rates within the pack [53-55]. In order to

overcome the issues that arise from cell-to-cell variations and which can negatively affect the performance of the battery pack, a BMS is required.

1.3 Battery management system

The term BMS is used to describe the combination of software (i.e. algorithms for cell monitoring, fault detection, state estimation and charge control) and hardware (i.e. sensors, transceivers, balancing circuits and active cooling) required to ensure safe, reliable and efficient operation of the battery pack [56]. The interactions between the different parts of the BMS are presented in Fig. 1.7.

The BMS monitors the terminal voltage, current and temperature of (preferably) each cell in the battery pack and these measurements are used in order to ensure that cells operate within a safe voltage and temperature range. When a cell is in danger of exiting the safe operating area, the appropriate alarm signal is sent from the charge control algorithm to the system controller in order to set the battery pack current (C-rate) accordingly. The reference current of the battery pack is calculated in the central system controller according to the active and reactive power references, based on the requested grid service. The BMS checks the current reference to ensure that the cells are able to operate at the requested C-rate, there is sufficient charge available in the pack (using the estimated SoC) and the requested current will not cause violation of the voltage and temperature limits. If the requested current cannot be provided, a new current reference will be used for the control of the converter. Apart from controlling the C-rate, the charge control algorithm of the BMS also enables cell balancing. In order to achieve cell balancing the BMS can control the flow of charge to/from the cells according to their respective SoC using a balancing circuit (this will be discussed in detail in the following sections). Other functions of the BMS include thermal management by monitoring the temperature and controlling a fan and a heater to ensure that the battery operates in the optimal temperature range, and fault management by bypassing a failed cell or module using a protection circuit (e.g. contactor).

The primary task of the BMS is thus to ensure that all cells operate within safe voltage and temperature limits and under appropriate C-rates. More advanced BMSs may also use

state estimation (e.g. to estimate state-of-health) to define an operating profile for the battery that will reduce the degradation rate of the cells and improve the overall performance of the system [57].

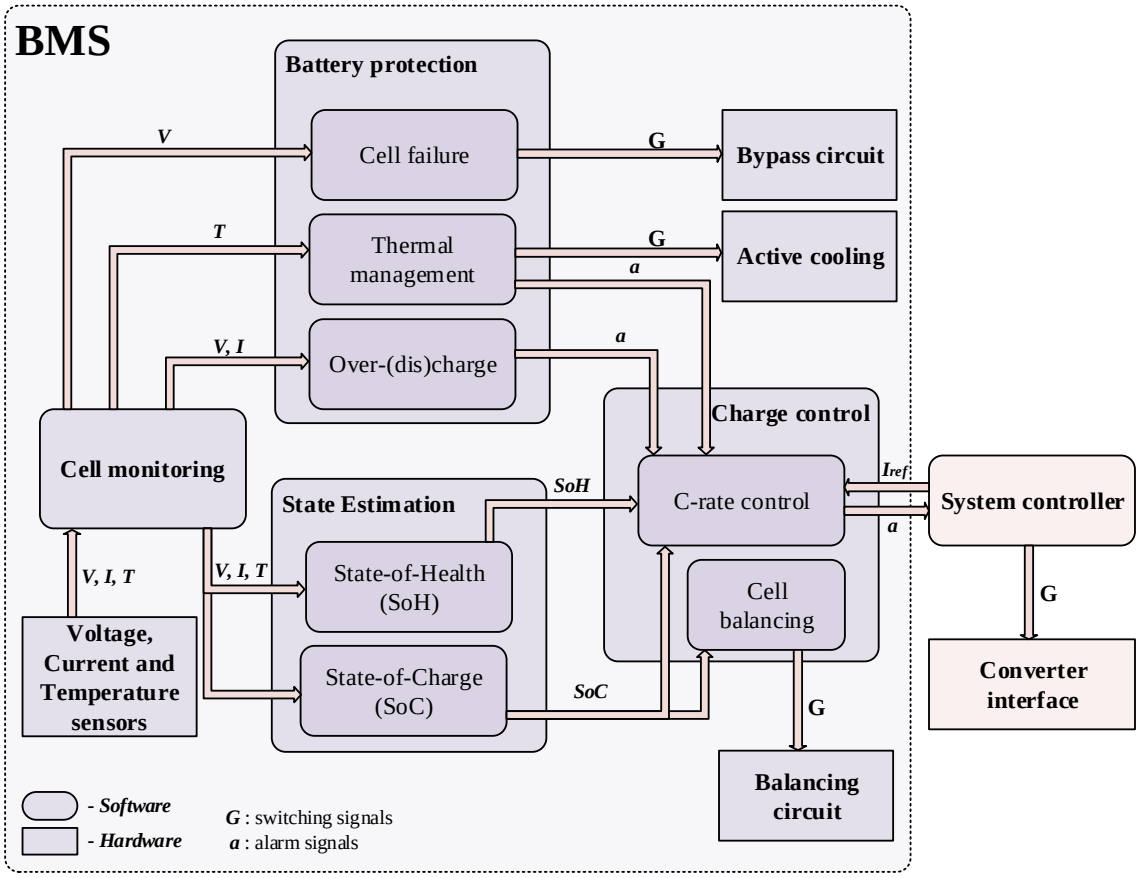


Fig. 1.7 Graphical representation of a battery management system and its basic functions.

1.3.1 State-of-charge estimation techniques

The term SoC refers to the available charge that is stored in a cell as a percentage of the total charge capacity of the cell [58]. An accurate SoC estimation is important because it provides an indication of the available energy in the battery pack that will dictate the ability of the system to provide ancillary services to the grid. It is also used to protect the battery from overcharge or deep charge conditions that can degrade battery life [59]. Conventionally, SoC is estimated using *coulomb counting* [57], where the SoC is given by (1.2) as the integral of the cell current I over the cell capacity Q.

$$SoC(t) = SoC_0 + \frac{\int_0^t I.\,\mathrm{d}t}{Q} 100 \tag{1.2}$$

where SoC_0 is the initial SoC of the cell.

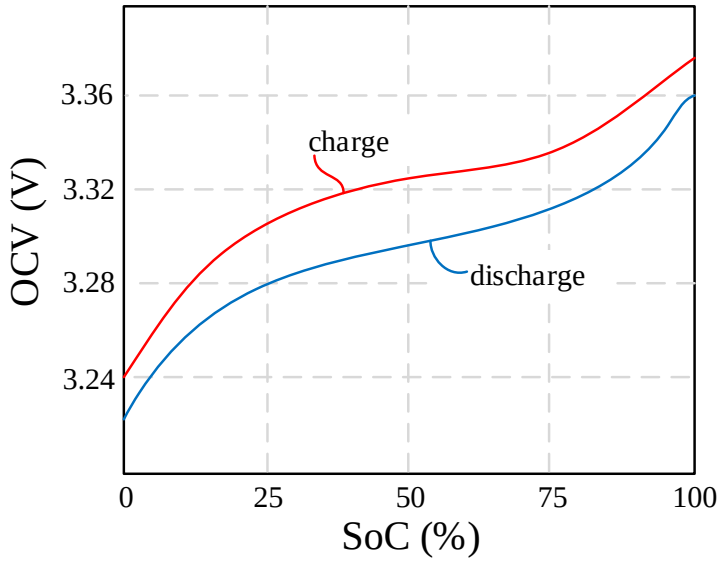
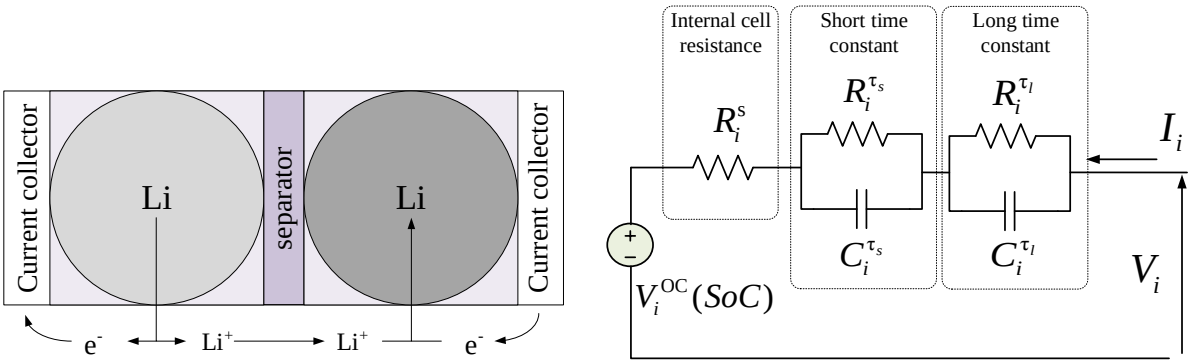


Fig. 1.8 Example OCV vs SoC curve of a Li-ion cell during charging and discharging.

This method, although simple to implement, requires prior knowledge of the initial SoC as well as the capacity of the cell, which decreases gradually over time due to cell ageing. Moreover, the accuracy of SoC estimation will tend to be reduced due to current sensor errors which accumulate over time (during the integration process) [58]. Another approach is estimating the SoC by measuring the open circuit voltage (OCV) of the cell and using appropriate look-up tables with different curves for charging and discharging to account for the hysteresis effect (Fig. 1.8) [60]. However, to get a high quality OCV measurement the cell should be rested (i.e. cell current equal to zero) for lengthy periods of time [61]. This is not possible in conventional battery packs unless underlying hardware that enables bypassing single cells or modules without interrupting operation of the system exists.



(a) (b)

Fig. 1.9 Li-ion cell modelling examples: a) single particle model b) equivalent circuit model.

Model based approaches have also been extensively discussed in literature. Electro-chemical models incorporate chemical/electrochemical kinetics and transport phenomena to generate meaningful predictions but due to their relatively high computational requirements they are considered to be too complex for real time application in large battery packs at the cell level [62, 63]. An example of this approach is the single-particle model (SPM), where each electrode is represented as a single particle (Fig. 1.9a). The SPM can estimate SoC and predict capacity fade due to growth of solid electrolyte interface (SEI) [64] but is not valid for high C-rates, thick electrodes or other conditions where the electrolyte effects and variations across the electrodes are significant [65]. On the other hand, empirical models built by curve fitting experimental data are easy to develop and implement, but their accuracy is limited when the cell is operated under different conditions from those used for model derivation [57]. Equivalent circuit models use electric circuit components such as voltage sources, resistances and parallel resistor-capacitor (RC) pairs to simulate the dynamic behaviour of cells [66]. In general, a higher number of RC pairs can provide increased accuracy at the cost of additional complexity, however, two RC pairs (similar to Fig. 1.9b) are usually enough to represent long-term (associated with diffusion) and short-term (associated with charge transfer) relaxation effects [67], while even models using a single RC pairs have demonstrated adequate accuracy [68, 69]. These models are relatively easy to implement, however a single model with constant parameters cannot accurately describe a cell throughout its life or for different (dis)charging currents, temperatures and SoC, thus models that update their

parameters online have been proposed [70, 71]. In order to increase the accuracy of SoC estimation, equivalent circuit models have been used in tandem with adaptive filter algorithms such as variations of the Kalman filter [72-74] or state observers such as the sliding mode observer [75, 76], at the expense of additional complexity. Other approaches include learning algorithms such as neural networks [77, 78] or fuzzy logic [79, 80] that are not practical for online applications since they need to store large amounts of data for training that increase the memory and processing requirement of the BMS.

According to the above, SoC estimation is conventionally performed using coulomb counting and although a plethora of advanced modelling techniques and filter algorithms have been developed to increase the accuracy of estimation, they are usually impractical for online implementation due to their increased complexity. An alternative approach is to address the fundamental limitation of conventional battery packs, where cells are connected in a static manner, by introducing the hardware that will allow bypassing cells without interrupting operation of the system. The provided control flexibility will enable online OCV measurements and thus greatly simplify the process of SoC estimation. In this case, appropriate selection of the bypass duration is crucial in order to ensure that the internal cell dynamics can be neglected without introducing additional imbalance between cells in the pack (since some cells will be online while others are bypassed).

1.3.2 Cell balancing methods and circuits

The capacity of a battery pack comprising series connected cells is limited by the lowest capacity cell, unless a balancing circuit is used [81]. Cell balancing aims at operating the cells of a pack within a close SoC range and can be either passive or active [82]. Passive balancing is the most common approach due to its low cost and simple implementation [83]. In passive balancing circuits such as the one depicted at Fig. 1.10a, each cell is connected in parallel with a resistor through a controllable switch. During charging, once a cell reaches the upper voltage limit the respective switch is turned on and the excess energy is dissipated through the resistor, while charging continues for the rest of the cells at a lower C-rate (depending on the rating of the resistors), until all cells are fully charged. The disadvantage of passive balancing is that it dissipates energy as heat which is wasteful and challenging to deal with, especially in space-constrained applications.

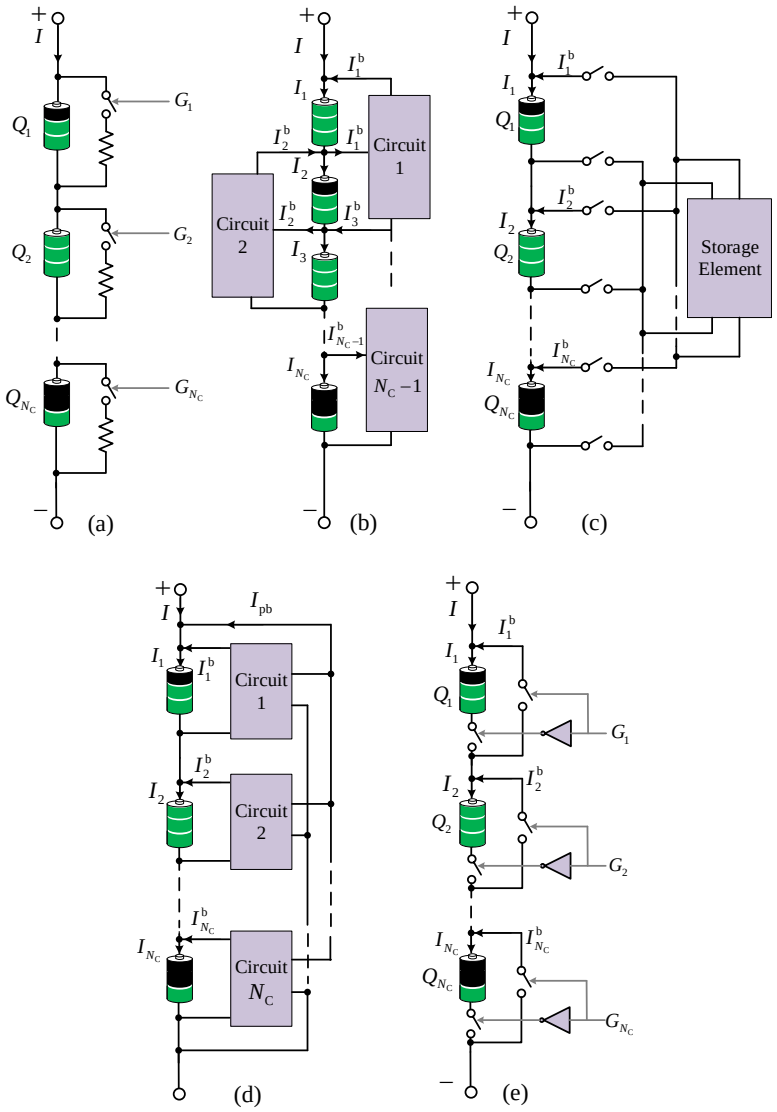


Fig. 1.10 Balancing circuit architectures: a) passive balancing circuit b) adjacent cell-to-cell balancing circuit c) direct cell-to-cell balancing circuit d) cell-to-pack balancing circuit e) duty cycle balancing circuit

Active balancing on the other hand is not dissipative but rather aims to individually control the rate of cell charging and discharging so that cells have an equal SoC at all times during operation. The majority of active balancing circuits described in the literature implement Energy Redistribution Balancing (ERB). In conventional battery packs where cells in the pack are connected in series and conduct the main pack current at all times, ERB is performed by introducing smaller shunt currents that transfer energy between cells. ERB circuits can be placed in one of three categories, based on their

architecture [84]: the adjacent cell-to cell (A-C2C), the direct cell-to-cell (D-C2C) and cell-to-pack (C2P). The A-C2C (Fig. 1.10b) includes balancing circuits such as the switched capacitor [85], the bidirectional buck-boost converter [86] and the Ćuk converter [87]. The advantages of the A-C2C circuits are the simple structure, modular design and low cost. Their main disadvantage is that energy can be transferred only between adjacent cells, increasing balancing time and energy losses, especially when implemented in packs with a relatively large number of cells.

Conversely, in the D-C2C architecture presented in Fig. 1.10c, energy can be transferred between any two cells in the string, regardless of their position, using appropriate switches and a storage element such as capacitor or inductor. However, only two cells can be balanced simultaneously and so balancing time will be lengthened for a large number of unbalanced cells. Some of the circuits that correspond to this architecture are the flying capacitor [88], shared inductor [89] and quasi-resonant converter [90]. In the C2P architecture depicted in Fig. 1.10d, energy can be transferred between a cell and the battery pack to provide flexible balancing. In this case, energy redistribution is achieved either by using distributed circuits such as multiple transformers or shared storage elements such as the multiwinding transformer with leakage inductance [91]. These circuits tend to suffer from increased volume and cost compared to the previous architectures. Apart from the inherent restrictions regarding energy redistribution between cells in each of these circuits, the ability to effectively equalise cell SoC depends on the maximum balancing power (or balancing current) that can be transferred to/from each individual cell. The maximum balancing current of ERB circuits depends on the size of the passive storage elements (inductors, capacitors) as well as the ratings of the active switches (usually MOSFETs) that are used in the balancing circuit.

Duty Cycle Balancing (DCB) is a sub-category of active balancing where balancing is performed by controlling the duty cycle of each cell according to their relative SoC [92, 93]. In contrast to the ERB where all cells are in the main current path at all times, DCB relies on the ability to bypass cells during operation. This can be achieved by using additional power electronics switches in the pack, thus creating power electronics enhanced battery packs (PEEBPs) [94-96]. The simplest form of a PEEBP is given in Fig. 1.10e and it comprises cells connected in series using half-bridge (two-switch) circuits around each cell so that any cell can be either in series (with a cell current equal to the

string current) or bypassed (with a cell current equal to zero). As a requirement for DCB, the system should be designed to include some 'redundant cells' so that the required output voltage can be reached even when bypassing some cells. In contrast to the ERB circuits, the switches used in a PEEBP should be rated at the full pack current (whereas in ERB they are rated at the balancing current that is usually only a fraction of the pack current) [97], while the conduction losses of the switches affect the total efficiency of the system even if no balancing is performed (since at least one switch is always on the current path).

When the different balancing topologies are compared in the literature, assessment criteria such as the balancing speed, cost and efficiency are often qualitatively evaluated by assigning grades such as 'excellent', 'good' and 'poor' [83]. On the other hand, more–quantitative performance analysis often focus on a single proposed balancing circuit and are therefore quite application specific [98]. Reference [81] quantitatively describes the ability of five different balancing topologies to overcome a random initial charge imbalance by computing the balancing time and energy losses using a simple analytical model. The main assumption in [81] that enables this sort of analysis is that the cells will be able to achieve balancing after a certain time, which is not always the case as will be shown later in Chapter 3. A study of balancing systems using convex optimisation is presented in [99]. Here the objective is the minimisation of pack losses, balancing circuit energy losses and pack temperature. In [100] a relatively complex vehicle simulation is used to compare ten different active balancing circuits as well as the influence of control variables (e.g. voltage, SoC and charge capacity) for active cell balancing. This model-based approach provides a quantitative evaluation of the useable capacity when a number of cells with different capacities are used. However, even these quantitative comparisons are not very meaningful if the compared balancing circuits have not been designed under the same considerations.

In order to be able to choose between the different balancing architectures mentioned above, each candidate circuit should be designed so that a target balancing performance can be achieved at the minimum cost. This can be achieved by developing a framework that can determine the minimum value of balancing current (for ERB) or cell redundancy (for DCB) in order to perfectly balance a pack of cells with a given capacity distribution.

1.3.3 Battery management system architectures

The BMS architectures are often categorised into two types: flat and modular [95, 101]. In a flat BMS architecture as the one presented in Fig. 1.11a, the pack is usually organised in elements i.e. the fundamental units that include the battery module with the sensing hardware to monitor the voltage of each cell and the temperature within the element (preferably per cell) and the balancing circuit, as well as any integrated power electronics in case a PEEBP is considered [102]. In packs comprising series connected elements, current measurements need only be performed in one location by a single element equipped with a hall-effect sensor [102]. Sampling is performed by a centralised BMS controller that collects the information from the elements (i.e. cell voltages, currents and temperatures), processing it (e.g. SoC estimation) and providing the switching signals ($\boldsymbol{G}$) for the active switches used in the balancing circuit within the element units (passive balancing is most commonly used in this case). This architecture is inherently very difficult to scale as the wiring complexity and communication latency increases unacceptably with the number of elements [103].

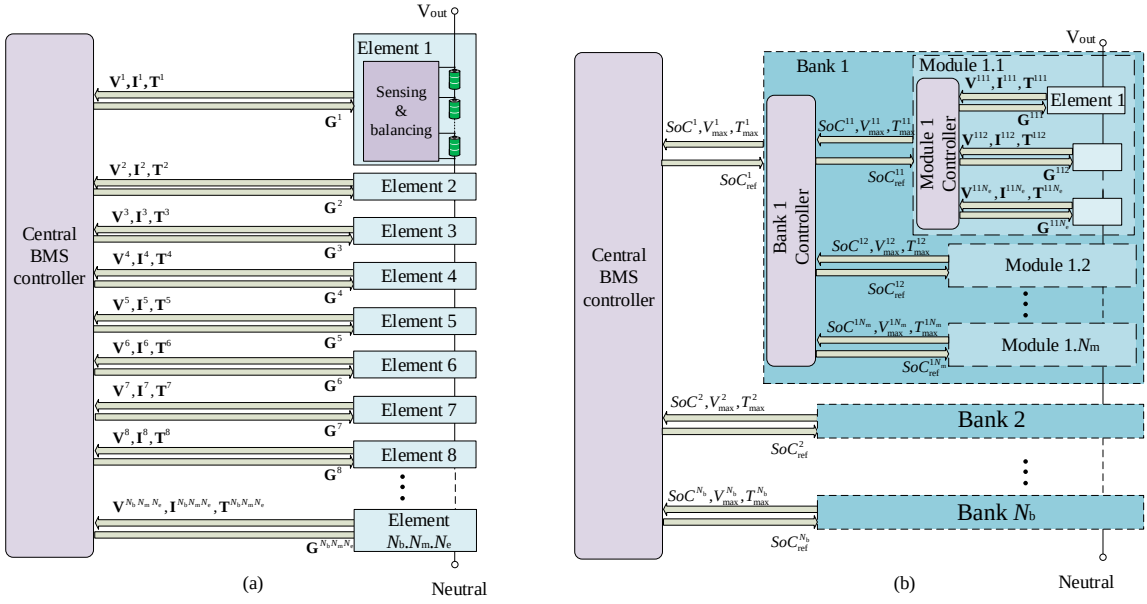


Fig. 1.11 Battery management system architectures: a) battery pack with a flat BMS architecture b) battery pack with a modular BMS architecture using three conceptual hierarchical layers (i.e. banks, modules and elements).

In contrast, the modular BMS architecture is a decentralised scheme enabled by organising the system in conceptual hierarchical layers [97] such as banks, modules and elements in Fig. 1.11b. Each object in a layer (i.e. the entities that make up a layer) is equipped with a controller that acts as a master for a subset of slave controllers located in the next lower hierarchical level. Each local controller receives the required sensing signals such as cell voltages, currents and temperatures (for the module layer controllers) or the average SoC and maximum voltage and temperature (for the intermediate layer controllers), and sends back control signals such as the SoC reference for the intermediate layer balancing or the driving signals for the active switches in the element's balancing circuit. A centralised controller is still required in this case, however by limiting the total amount of information that is transferred between layers the processing power requirements for that controller are significantly reduced.

A decentralised modular BMS can provide several advantages such as a greatly reduced wiring harness [104] and simple scalability which enables rapid construction of different sized systems leading to a reduced time-to-market. A modular BMS can also facilitate the implementation of more advanced ERB or DCB circuits in battery packs. These circuits require complex control patterns for the Pulse Width Modulation (PWM) signals that are used to drive the switches. Although these signals can be very challenging to generate and distribute from a central controller, especially in large scale battery packs [102], in a modular BMS they can be produced by the local controller that will directly drive the switches. Modular BMSs can also facilitate second-life applications. These applications use cells that no longer meet the requirements of their initial application, in a less demanding environment, such as EV cells used in grid storage applications [105]. Having a dedicated local controller with a detailed log of a cell's operating history can greatly enhance the management of second-life cells. Modular BMS architectures however, require a paradigm shift from an algorithmic perspective. Without global supervision of the cells from a central controller, the efficient and safe operation of the pack is dependent on the effective communication between the local controllers. This requires a new class of algorithms that transfer centralised battery management functions, such as cell SoC balancing, into a distributed mode of operation [102]. Regarding the hardware implementation of modular BMS, the challenge is to produce design solutions

for the on board power supply, microprocessor, balancing circuitry and communication interface, considering cost, efficiency and isolation requirements.

1.4 Power electronics topologies for battery systems

Power electronics is the key enabling technology that facilitates the connection of DC battery packs to the AC grid [23, 106]. The power electronics converter acts as the interface between the battery and the electricity grid and, in combination with the BMS, controls the power flow in the BESS and regulates the operating points of the battery [107]. This section presents a review of the converter architectures that are used in BESS applications.

1.4.1 Conventional battery system architecture

In a conventional BESS, the battery is connected to the grid through either a single-stage or a two-stage converter (Fig. 1.12). In the single stage architecture, the battery pack is directly connected to the DC link and a two-level bidirectional DC/AC converter is used to connect to the grid [23]. BESSs larger than 1 MW and 1 MWh are typically connected to the lower distribution network at medium voltage (MV) e.g. 11 kV in the UK [44]. The standard practice is to connect 200-300 cells in series to achieve a DC bus voltage of approximately 700-1,000 V, thus a line-frequency transformer is required for connection to the MV grid [108, 109]. A disadvantage of the single-stage architecture is that the DC-link voltage is directly defined by the battery voltage and thus varies according to the SoC. This results in oversized switches, since the switches should be rated according to the maximum expected DC link voltage. A wide range of modulation indices is required to produce a fixed AC voltage from a variable DC voltage, leading to decreased efficiency and higher harmonics at the output [107]. These issues can be addressed by using a two-stage converter architecture, with an additional DC/DC converter that controls the DC-link voltage. The most common topology for the DC/DC converter is the bidirectional half-bridge converter due to its simple design and relatively high efficiency [110]. However, the boost capability is quite limited so the line-frequency transformer is still required for integration to the MV grid. If galvanic isolation is necessary between the DC-link and the battery pack, the dual-active-bridge (DAB)

converter can be used [111]. The high-frequency transformer (switching frequency in the range of 5-20 kHz) used in the DAB provides isolation and a higher boost ratio than that of the bidirectional half-bridge converter. The enhanced controllability achieved with the two-stage architecture comes at the price of increased component count and a subsequent increase in cost and power losses [107]. As the power and energy rating of the system increases, a parallel configuration of complete BESSs (either single or two-stage) referred to as power blocks (PBs), is often used to avoid the construction of a very large monolithic battery pack. In this case, the total capacity is divided between several identical smaller systems which operate together (Fig. 1.12) [57]. An advantage of this arrangement is that failure of one cell will cause the loss of only one series string in one PB [112], as opposed to a much larger series string as would be found in a monolithic system.

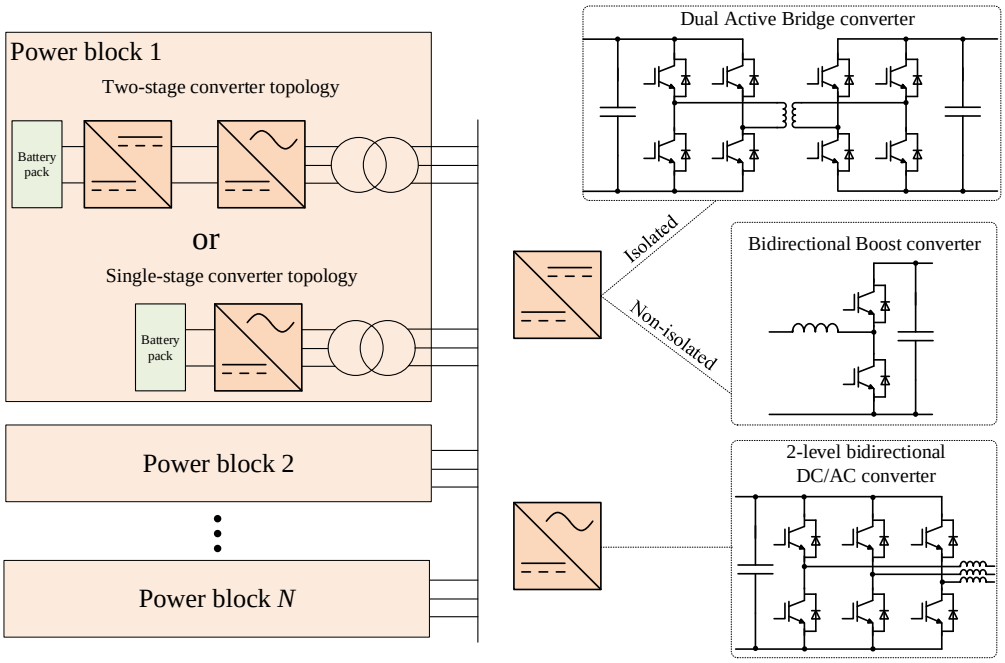


Fig. 1.12 Conventional power block configuration of BESSs using either a single or a two-stage converter topology.

1.4.2 Transformerless battery systems using power electronics enhanced battery packs

In order to avoid using a transformer, a battery pack with sufficiently high output voltage is required. The reliability concerns that arise when connecting a high number of

cells in series can be addressed by using a PEEBP that has the ability to bypass a single cell in case of failure without interrupting the operation of the system [92]. For large scale systems with a high number of cells, using a bypass circuit for each cell is impractical so this method can be implemented in module level instead [113].

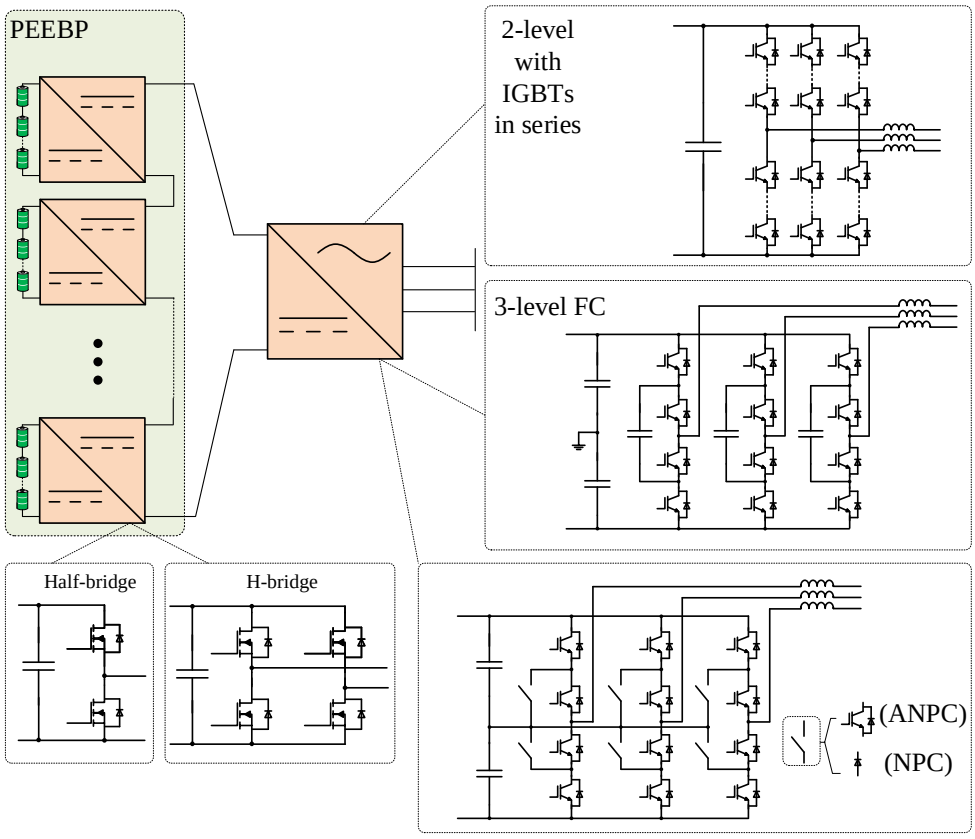


Fig. 1.13 Transformerless BESS configuration using a PEEBP.

In this case, the single-stage converter architecture presented in Fig. 1.13 can be used, since the DC-link voltage will be controlled by the PEEBP, but the DC/AC converter needs to be properly sized to block a higher DC-link voltage. In order to use the two-level topology, a series connection of switches would be required for each converter arm. The implementation of appropriate gate drivers to ensure that the devices are turned on/off synchronously can be challenging and a lower switching frequency will be required to reduce switching losses, thus leading to increased filtering requirements [107]. Alternatively, multilevel converter topologies such as the neutral-point clamped (NPC) [114] and the flying capacitor (FC) [115] can be used. The NPC uses series connected capacitors to divide the DC-link voltage in several lower voltage levels. The main

disadvantage of this topology is that capacitor balancing is required. A variation of the NPC is the Active NPC (ANPC) where the neutral-point clamped diodes are replaced by active switches [106]. As a result, more than one switching state can be used to generate a zero output voltage, hence better loss distribution can be achieved by optimising the switching sequence [116]. The FC is similar to the NPC, using capacitors instead of clamping diodes to divide the DC-link voltage. The drawbacks of this topology are the size of the flying capacitors and the additional complexity introduced by the DC-link capacitor charge controller [109].

1.4.3 Modular multilevel battery systems

A fundamentally different approach in designing BESSs without the need of separated DC/AC converter and battery pack is based on modular converter topologies such as the modular multilevel converter (MMC) and the cascaded H-bridge converter (CHB) [117]. The MMC (Fig. 1.14a) is a two-port converter in contrast to the single port CHB (Fig. 1.14b), so it is more suitable in applications where a DC/AC converter with additional storage capability is required. A detailed analysis of a BESS based on the MMC is presented in [118], focusing on a balancing controller that allows SoC balancing between phases, arms and elements. Balancing between the three phases of the MMC is achieved using zero-sequence voltage injection to ensure different power flow at each phase without affecting the total output power of the three-phase system. Balancing between the arms of each phase is performed by injecting a circulating current component at the fundamental frequency and with the same angle as the respective phase voltage. Element balancing within each arm is enabled by multiplying the voltage reference of each element with a power ratio factor to ensure that the arm active power is distributed within the elements according to their respective SoC. The proposed controller was implemented in a single-phase MMC comprising four elements per arm, with a 25.6 V LFP battery included in each element. An issue when using the MMC in BESS applications is the low-order harmonic currents observed in the MMC elements, which is expected to increase cell losses since a li-ion cell is usually modelled as a voltage source with a series resistance. In order to address this issue, a filter capacitor or even an additional DC/DC conversion stage can be used between the battery and the half-bridge [117, 119, 120]. It is not clear however if the advantages of using a DC/DC converter outweigh the additional

cost and losses introduced in the BESS by the intermediate conversion stage. Moreover, a charging current with a sinusoidal ripple may actually improve the charging efficiency and lifetime of li-ion cells compared to conventional constant current charging strategies, by minimising the AC impedance of the cells [121].

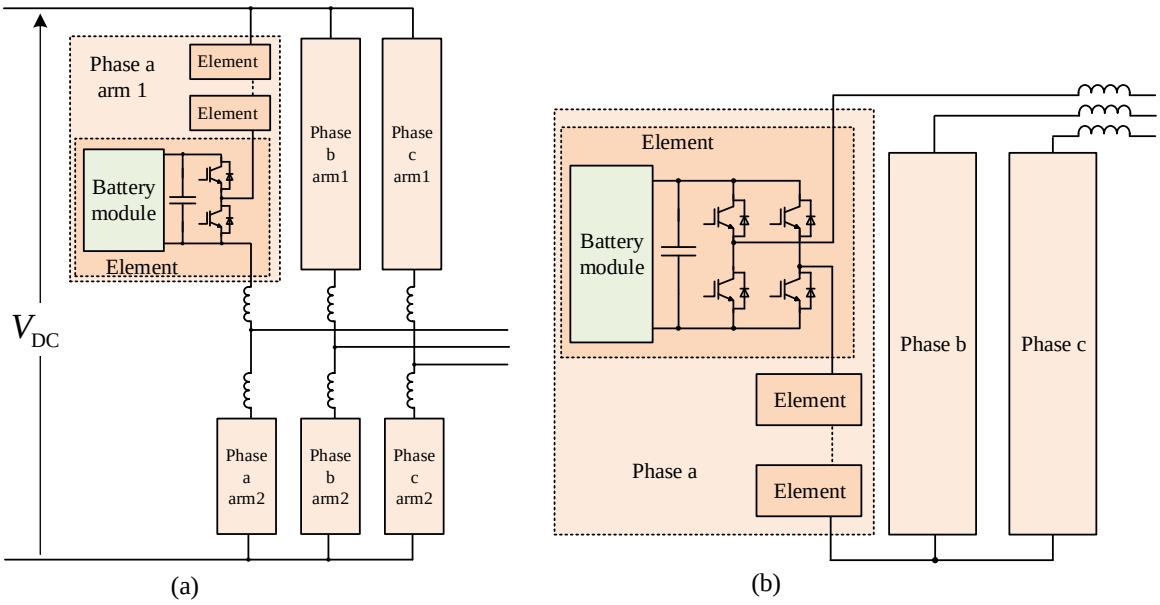


Fig. 1.14 Modular battery system designs: a) MMC topology and b) CHB topology.

The CHB is another topology that has been favoured among multilevel converters for BESS applications, due to its modular design that makes it inherently scalable to higher voltages. The CHB elements include a battery module connected in series with an H-bridge converter, as presented in Fig. 1.14b. The modules within each element can thus be individually controlled in order to achieve SoC balancing or in order to be bypassed in case of failure, without interrupting the operation of the system. Another advantage of the CHB is the ability to produce a high quality stepped waveform by combining the DC voltages of the elements. The IGBT switches in each H-bridge are rated at only a fraction of the total DC voltage (sum of battery modules voltages) and can be operated at a relatively low switching frequency (depending on the modulation scheme and the available voltage steps). Compared to the MMC, the CHB does not require a DC-link to operate and provides a better utilisation of the available DC voltage i.e. the peak-to-peak output voltage of the CHB is equal to $2V_{DC}$ compared to $0.5V_{DC}$ in case of the MMC,

when the total DC voltage distributed among the elements of the multilevel converters is equal to V_{DC}.

An early concept of a BESS based on the CHB is presented in [122] for a static synchronous compensator (STATCOM) application. In this case, the output voltage is a staircase waveform produced by combining the DC-voltages of the different elements, resulting to a different conduction time for each battery module at each half-cycle. Balancing between the battery modules can then be achieved by controlling their conduction times according to their relative SoC. The examined system included only two elements per phase with six 12 V batteries connected in series per element.

In [123] a SoC balancing controller for a BESS based on a CHB-PWM converter is presented, where a centralised controller performs active power control of the BESS based on a conventional *d-q* current controller and SoC balancing is performed between the three phases by using a zero-sequence voltage injection. SoC balancing between the elements of each phase is achieved by using a superimposed voltage at the voltage reference of each element in order to minimise the SoC difference between them (the sum of the superimposed voltages is zero so that the individual element balancing does not interfere with the active-power control of the system). The same authors present [124] a slightly different approach for achieving element balancing by directly controlling the output power of each element. The overall control is very similar to [123] since in both cases balancing is essentially performed by distributing the voltage references to the elements of each phase in proportion to each element's SoC (or power reference) deviation from the average phase SoC (or power reference). Their approach was validated experimentally using a 200 V 10 kW/3.6 kWh prototype that comprises three cascaded elements at each phase, with each element including 60 cells connected in series. Each element is equipped with a BMS that monitors the cells and provides SoC estimation for the centralised controller where SoC balancing is performed. PWM is implemented locally using the FPGAs located at each element. [123] does not address SoC balancing within the element but it is likely that an additional passive or active balancing circuit will be required. The aforementioned control scheme is also implemented in a 500 kW/238 kWh BESS based on the CHB with six cascaded elements per phase [125]. Each element includes a Toshiba LTO battery pack with a nominal voltage of around 300 V. The switching devices in this case are IGBTs rated at 600 V and 600 A and the H-bridges are

controlled using a phase-shifted unipolar sinusoidal PWM with a carrier frequency equal to 1.35 kHz.

A nine-level CHB-BESS is discussed in [106] where a battery pack with a nominal voltage of either 950 V or 1.5 kV is included in each converter element. The specific harmonic elimination modulation method is adapted here due to the lower switching frequency compared to PWM methods and the ability to balance elements by controlling their duty cycle while producing the stepped waveform (the different modulation techniques for multilevel converters are discussed in more detail in Chapter 2). In [126] a 15-level CHB-BESS is built using 125 V battery modules in each element.

1.4.4 Modular battery systems with deep integration of power electronics in the battery pack

In all the cases mentioned above, the number of cascaded elements per phase is relatively low (less than 7) and so the modularity of the CHB is not fully utilised. The large battery packs included in each converter element (reported battery pack voltage per element ranges from 72 V to 1.5 kV) require IGTBs with relatively high voltage ratings for the H-bridge converters (Fig. 1.15a) and a PWM scheme with carrier frequencies at the range of kHz that would allow producing a high quality output voltage. Although SoC balancing between elements and phases can be performed utilising the CHB, additional balancing circuits would be required to address balancing within the battery module of each element.

An alternative approach that suggests deep integration of the power electronics in the battery pack is presented in [127]. This paper explores the concept of using single cells (or very few cells connected in series) at each H-bridge element in the CHB (Fig. 1.15b). This deeply modular approach enables fine-grained control of the cells in the pack, which can significantly enhance system reliability and balancing performance. An improved reliability is expected when using a modular system due to the ability to address local cell or converter failures more effectively by bypassing failed elements without interrupting operation of the system. A modular CHB-BESS is also able to fully utilise the available capacity by performing DCB, even if cells with widely different capacities are used in the pack. This is particularly important for grid scale BESS with an expected lifetime greater than ten years because cell-to-cell variations due to cell degradation can significantly

limit the capacity that can be extracted from the pack, unless an active cell balancing circuit is in place. The ability to perform DCB can also greatly facilitate the maintenance process since a replacement element does not need to have the same capacity or be pre-charged at the same SoC level as the existing elements before being placed in the pack. Another benefit of the modular CHB architecture is the use of low-voltage MOSFET switches with very low on resistance and the ability to produce a high quality stepped voltage waveform by combining the voltages of the individual cells without the need of a high switching frequency PWM scheme.

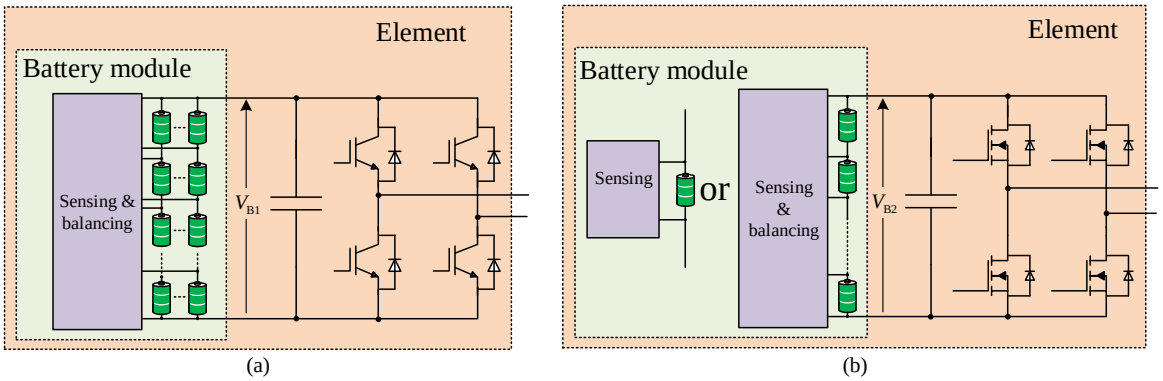


Fig. 1.15 Element structure of BESSs with different levels of modularisation: a) conventional modular CHB-BESS b) CHB-BESS with deep modularisation where $V_{\mathrm{B2}} \ll V_{\mathrm{B1}}$.

Although the concept of the modular PEEBP is attractive in terms of balancing performance and reliability, the integration of additional power electronics in the battery pack is often treated with scepticism due to the large number of switches required. Specifically in the CHB topology, two switches per element will always be present in the current path, which is expected to increase the total conduction losses of the converter, while the overall cost and system reliability might also be affected by the increased number of components. In terms of control complexity, a deeply modular CHB-BESS would require a significantly higher number of driving signals (four signals per H-bridge to allow control of each MOSFET independently) compared to a conventional BESS with a centralised monolithic converter. As a result, a modular BMS is necessary and the appropriate control algorithms should be developed in order to achieve an equivalent

balancing performance to that of a system that uses a centralised controller with global knowledge of the states of every cell in the battery pack.

1.5 Research contribution

The aim of this work is to address the following research questions:

1. How does a deeply-modular power electronics enhanced battery compare to conventional system designs?
2. What is an appropriate converter topology for the implementation of such a deeply-modular battery system?
3. How can the provided control flexibility be utilised to achieve SoC estimation?
4. How can we overcome the control complexity of large-scale deeply-modular battery systems with an increased number of controllable switches?

Compared to conventional battery packs, modular PEEBPs offer fine-grained control over cells that can enhance system reliability and improve capacity utilisation over the lifetime of the system. Potential drawbacks are the increased cost and power losses due to the high number of switches in the current path. In order to evaluate the feasibility of building a modular BESS, a framework is required that will allow the quantification of key performance parameters such as efficiency, reliability, cost and balancing capability. Current studies usually focus on converter losses [107] while reliability is determined based on the simple approach of 'parts count method' [128] (refer to the introduction of Chapter 4). Balancing performance is either evaluated through detailed system simulations [100] or via analytical approaches that use simplifying assumptions (e.g. that cell balancing can always been achieved [81]).

Regarding the implementation of a PEEBP, the CHB converter topology has been identified as an attractive candidate topology because of its modularity and the ability to perform direct DC/AC conversion and cell balancing. Previous research focusing on this topology presented different control algorithms that either required a flat BMS architecture [123, 129], which is not appropriate for a grid scale CHB-BESS, or when a decentralised BMS was implemented [127] the modularity of the CHB was not fully utilised (for a detailed comparison of the proposed control algorithm with existing work in literature please refer to Table 5.1).

The research contributions of this thesis can be summarised as:

1. Theoretical analysis of the CHB operation in a BESS application.
2. A method for calculating the relative SoC of cells in a CHB-BESS using POCV measurements by bypassing cells online.
3. A linear programming tool in order to quantitatively evaluate the balancing performance of active balancing circuits performing energy redistribution and duty cycle balancing.
4. A general methodology to evaluate competing BESS designs in terms of cost, power losses and reliability, taking into account the design and operation of the individual system components (i.e. battery pack, converter interface and balancing circuit).
5. The design and experimental validation of a hierarchical balancing algorithm for large scale CHB-BESSs with a distributed BMS architecture.

1.6 Thesis outline

Chapter 1 (Introduction) reviewed the characteristics and operation of the main components of a BESS (i.e. the battery pack, BMS and converter interface), introduced the concept of modular PEEBPs and highlighted the contributions of this thesis towards developing the framework to evaluate the performance of PEEBPs and presenting a novel control algorithm for use in large scale BESSs based on the CHB converter topology.

Chapter 2 (Analysis of the CHB converter and relative SoC estimation) presents a theoretical analysis of the operation of the CHB in BES applications and a method for relative SoC estimation using POCV measurements, including the experimental validation using a 25-level CHB with a centralised BMS (based on my publication [130]).

Chapter 3 (Balancing performance evaluation of active balancing circuits) presents a method for evaluating the performance of DCB schemes and conventional ERB schemes, using a common linear programming framework. The numerical prediction of the useable capacity is validated through simulation using different ERB circuits and experimentally for the DCB case using the hardware described in Chapter 2 (based on my publication [131]).

Chapter 4 (Battery energy storage system design evaluation) presents a methodology for evaluating grid-connected BESS designs, taking into account power losses, reliability and capital cost. This method is used to compare three design options for a 1 MW/1 MWh BESS with different levels of integration of power electronics in the battery pack (based on my publication [132]).

Chapter 5 (Control algorithms for large scale battery energy storage systems based on the CHB converter) presents a hierarchical balancing algorithm for large scale BESSs based on the CHB topology and a decentralised BMS. The developed algorithm is explained in detail and its operation is validated through simulation and experiment (based on my publication [133]).

Chapter 6 (Conclusion and future work) includes a summary of the work presented in this thesis and some suggestions for future work.

Chapter 2 Analysis of the CHB converter and relative SoC estimation

The CHB multilevel converter topology is emerging in BESS applications because of the advantages of using low voltage semiconductor switches, producing low output voltage harmonic distortion and the inherent modularity that leads to simple voltage scaling properties. The CHB converter provides the ability to achieve SoC balancing between the phases and between the elements of a phase without using additional balancing circuits [118, 123-125, 129, 134, 135]. In some cases, cell balancing is based on pack terminal voltage measurements [129]. The drawback of this approach is that voltage measurements cannot provide an accurate estimation of SoC due to the voltage error introduced by the internal resistance and the transient electrochemical phenomena. This chapter explores the operation of a CHB using the nearest level control modulation (NLC) technique. The analytical expressions for the different average cell currents due to the NLC are derived and a balancing scheme based on ordering cells according to their relative SoC is explained. The modularity of the CHB is utilised in order to introduce a method for relative SoC estimation using pseudo-OCV measurement by bypassing cells. The considerations for choosing appropriate resting times for an accurate POCV measurement are discussed and the validity of this method is tested through simulation and experiment, using 12 Li-po cells controlled individually by an H-bridge converter. This chapter is based on my publication [130].

2.1 Principles of cell balancing using a CHB converter with nearest level control

The modulation techniques used in multilevel converters can be classified according to their switching frequency as high switching frequency and low switching frequency [136]. High switching frequency techniques include carrier based modulation schemes such as the Phase-Shifted (PS) PWM [137] and Level-Shifted (LS) PWM [138]. In the PS-PWM presented in Fig. 2.1a, the same reference signal is used for all the converter modules but a phase shift is introduced between the carrier signals, producing a phase-shifted switching pattern between them. PS-PWM typically has a carrier frequency greater than 1 kHz and its operation results to evenly distributed power between the converter modules. This however is not particularly useful in battery applications where the ability to unequally (dis)charge cells is desired in order to achieve cell balancing. In the LS-PWM scheme the carriers are arranged in different vertical positions as depicted in Fig. 2.1b, with each carrier located between two voltage levels and the total number of carriers residing within the voltage range of the multilevel converter output voltage. Balancing between cells located at different converter modules can be achieved using this scheme by assigning a different carrier to each cell according to their SoC. In Space Vector Modulation strategies (SVM), each possible switching state of the multilevel converter, as well as the three-phase voltage reference are mapped in the α-β complex plane as can be seen in the example of Fig. 2.1c for a three-level converter. An appropriate algorithm has to be used to identify the three nearest vectors (of the converter states) to the reference, calculate the required duty-cycle for each of these vectors so that their time average equals the reference space vector and choose the appropriate switching state when more than one states can be selected (redundant states) [139]. In order to achieve a high resolution in time when following the reference voltage, a small modulation period is required, resulting to a high switching frequency (above 1 kHz) [140]. As the number of level increases, implementing a SVM scheme becomes more challenging due to the increased number of switching states. The actual number of vectors is less than that of the switching states due to the existence of redundant states (which are represented by the same vector) [141]. These redundant states can be used in order to

achieve different control objectives such as balancing the DC sources (e.g. cells) in the converter modules [142].

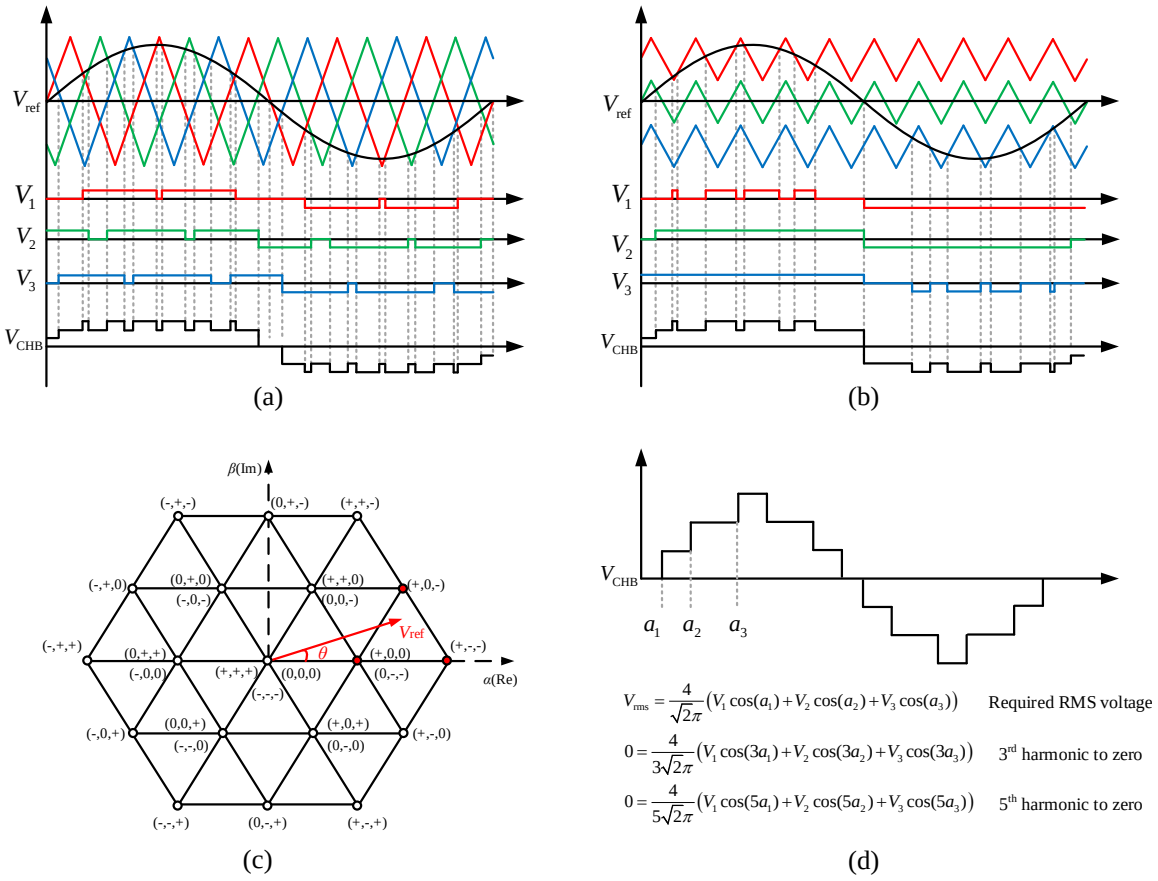


Fig. 2.1 Modulation techniques: a) phase-shifted PWM for seven-level converter b) level-shifted PWM for seven-level converter c) space vector modulation of three-level converter d) specific harmonics elimination for seven-level converter (adapted from [136], [140]).

The Selective Harmonic Elimination (SHE) modulation technique on the other hand is a low-frequency modulation technique (i.e. maximum switching frequency of converter modules is equal to twice the fundamental frequency) that uses Fourier analysis to calculate the appropriate switching angles for each converter module, so that the undesired low-order harmonics are eliminated. In order to achieve this, a set of equations is derived by setting the Fourier coefficients of the undesired harmonics to zero and that of the fundamental component equal to the required reference amplitude. These equations are then solved using numerical methods such as the Newton-Raphson method or genetic

algorithms [143]. An example of the use of SHE to eliminate the third and fifth harmonics in a seven-level converter is presented in Fig. 2.1d. The number of equations to be solved increases with the number of converter levels so calculating the switching angles on-line quickly becomes impractical. Instead, these calculations could be performed off-line for different modulation indexes and the resulting switching angles are then stored in look-up tables [140].

Implementing a carrier based modulation technique such as the PS-PWM or the LS-PWM in large scale CHB-BESSs can be challenging due to the high switching frequency and the subsequent increase in switching losses. Similar concerns arise when SVM is considered, while control complexity in that case is also an issue. SHE can achieve low-switching frequency modulation but is not scalable due to its high computational complexity. The modulation technique used in the CHB in this thesis is based on the NLC as it provides low switching frequency operation and is relatively simple to implement even for large-scale deeply-modular systems [136]. The principles of the operation of NLC are the same for any number of converter elements and are explained here using the example of a nine-level CHB-BESS (Fig. 2.2a).

NLC is performed by comparing the actual output of the CHB (V_{CHB}) to the voltage reference (V_{ref}) and switching on the appropriate number of converter elements in order to achieve a good matching between the two. A new element will be switched on if the resulting CHB output voltage is closer to the reference than it was before the switching event according to (2.1).

$$\left||V_{\mathrm{ref}}| - |V_{\mathrm{CHB}}|\right| > \left||V_{\mathrm{ref}}| - (|V_{\mathrm{CHB}}| + |V_{\mathrm{e}}|)\right| \tag{2.1}$$

As a result, a stepped voltage waveform that follows the sinusoidal reference is produced (Fig. 2.2b). Each step of the V_{CHB} waveform is equal to the voltage of the respective element (V_{e}) that is switched on to produce that step. Due to the operation of the NLC each element is switched on at a different instant in time (different switching angles a_i) and it remains on (i.e. operating states P and N for the H-bridge according to Fig. 2.2c) for a different amount of time ($2d_i$) during each fundamental period. As a result, each pack (or cell) is (dis)charged with a different average current:

$$I_i^{\mathrm{p}} = \frac{1}{\pi}\int_{a_i}^{\pi-a_i} \sqrt{2} I_{\mathrm{rms}} \sin(\varphi) d\varphi \tag{2.2}$$

where I_{rms} is the RMS value of the CHB output current (Fig. 2.2b).

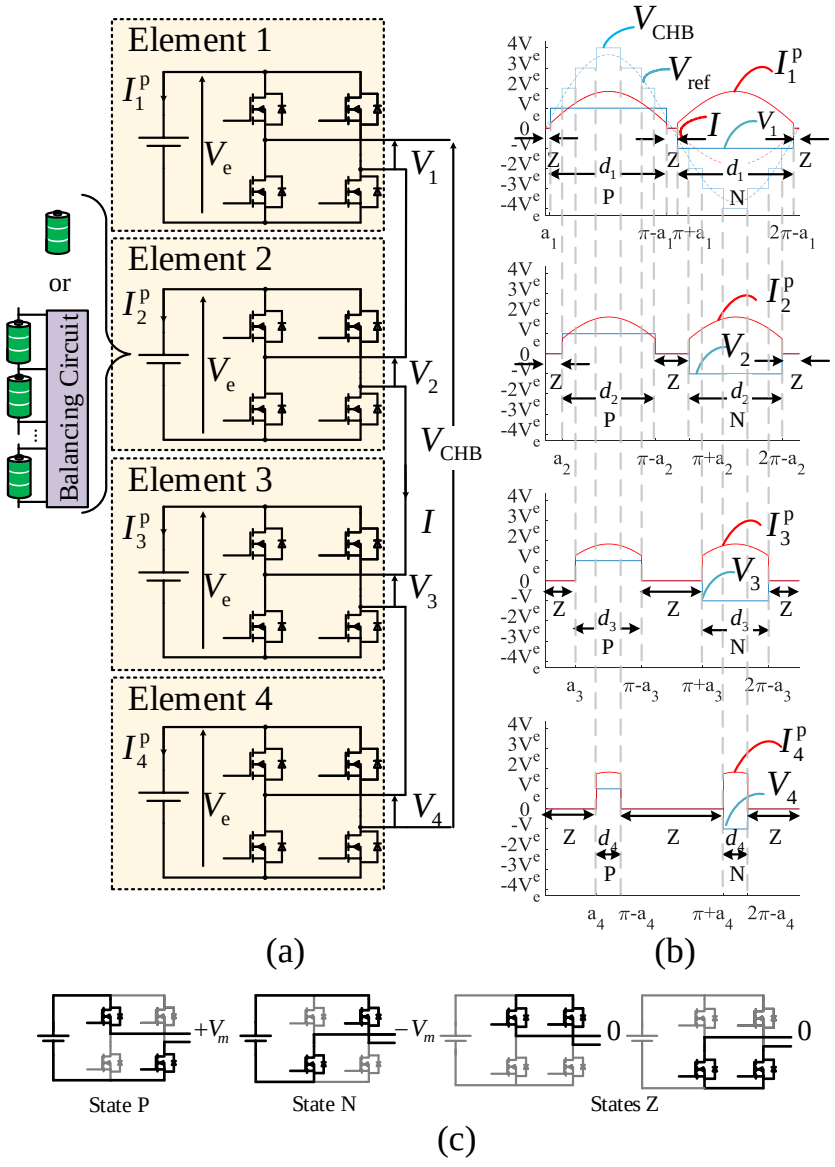


Fig. 2.2 Demonstration of element balancing using a nine-level CHB.

Assuming that the elements have equal and constant voltages, the switching angle a_i can then be calculated by:

$$\sqrt{2}V_{\text{rms}}\sin(a_i) = V_{\text{e}}(i - 0.5) \tag{2.3}$$

where V_{rms} is the rms value of the CHB voltage.

Taking into account element redundancy, the total voltage of the active elements in the CHB should be enough to supply the peak AC voltage of the CHB:

$$\sqrt{2}V_{\text{rms}} = N_{\text{a}}V_{\text{e}} \tag{2.4}$$

where N_{a} is number of active elements in the CHB.

From (2.3) and (2.4) the switching angle can be calculated as:

$$a_i = \arcsin\left(\frac{i - 0.5}{N_{\text{a}}}\right) \tag{2.5}$$

By substituting (2.5) in (2.2), the average current at position i is calculated:

$$I_i^{\text{p}} = \frac{2}{\pi}\sqrt{2}I_{\text{rms}}\sqrt{1 - \left(\frac{i - 0.5}{N_{\text{a}}}\right)^2} \tag{2.6}$$

A single-phase CHB with N elements can produce $2N + 1$ different voltage levels from a total of $2^{N+1} - 1$ operating states (assuming that each voltage level can be reached only by adding the output voltages of the elements). This state redundancy is particularly useful in battery applications as it can be used to perform SoC balancing. In order to choose between the available switching states that result to a specific output voltage, the switching sequence of the elements is determined using a priority list L. The priority list includes all the available elements sorted based on their relative SoC in ascending or descending order, with respect to whether the system is discharging or charging. Each element's position i in the priority list corresponds to a specific switching angle a_i and thus a different average position current I_i^{p}. The term 'position' used throughout the

thesis describes the position of the element in the respective priority list and is equivalent to the effective duty cycle of that element. In general, a higher position (i.e. a position closer to 1) corresponds to a higher duty cycle and thus higher average position current. In the example of Fig. 2.2, where the pack is charging (V_{CHB} is in phase with the pack current), the element at position 1 is charged with the highest average position current (I_1^{p}) whereas the element at position 4 is charged with the lowest average position current (I_4^{p}). If N_{a} voltage steps are required to produce the output voltage and the number of available elements is N, where $N > N_{\mathrm{a}}$, the $N - N_{\mathrm{a}}$ lower positions in the priority list correspond to zero position current (elements occupying these positions remain idle with their respective H-bridges always in the Z state). This sort of element redundancy is not necessary in order to achieve balancing with the CHB since each element can be operated under a different current by controlling its position. However, generally a higher value of element redundancy will enhance the balancing capability of the CHB by providing additional flexibility in controlling the effective duty cycle of each element.

2.2 Cell balancing based on POCV measurements

The effectiveness of a cell balancing strategy is highly dependent on accurate cell SoC estimation [144]. The OCV measurements could provide the information needed to estimate the relative cell SoC but would require each cell to be removed from the current path for a considerable time [145], which is not possible during operation of conventional battery packs that include cells connected in series. From Fig. 2.2b it can be seen that although cell currents vary depending on cell position, during the zero crossings all cell currents are zero. An intuitive way to achieve accurate relative SoC estimation is by exploiting these periods to eliminate the effect of the internal cell resistance on cell voltage measurements [19]. If a cell is well modelled only by a series resistance, the measured voltage at the zero crossing would be equal to the OCV; however due to cell dynamics (with time constants of the order 100 ms), the measured cell voltage is affected by the recent current flow history of the cell.

The proposed balancing strategy uses the modularity of the CHB in order to enable POCV measurements. Utilising the Z-state of the H-bridge, any single cell or pack of cells (provided that the packs are equipped with voltage sensors for each individual cell)

connected to the H-bridge can be bypassed (i.e. removed from the current path) for a predefined period of time, referred to as the idle state, without interrupting operation of the battery pack.

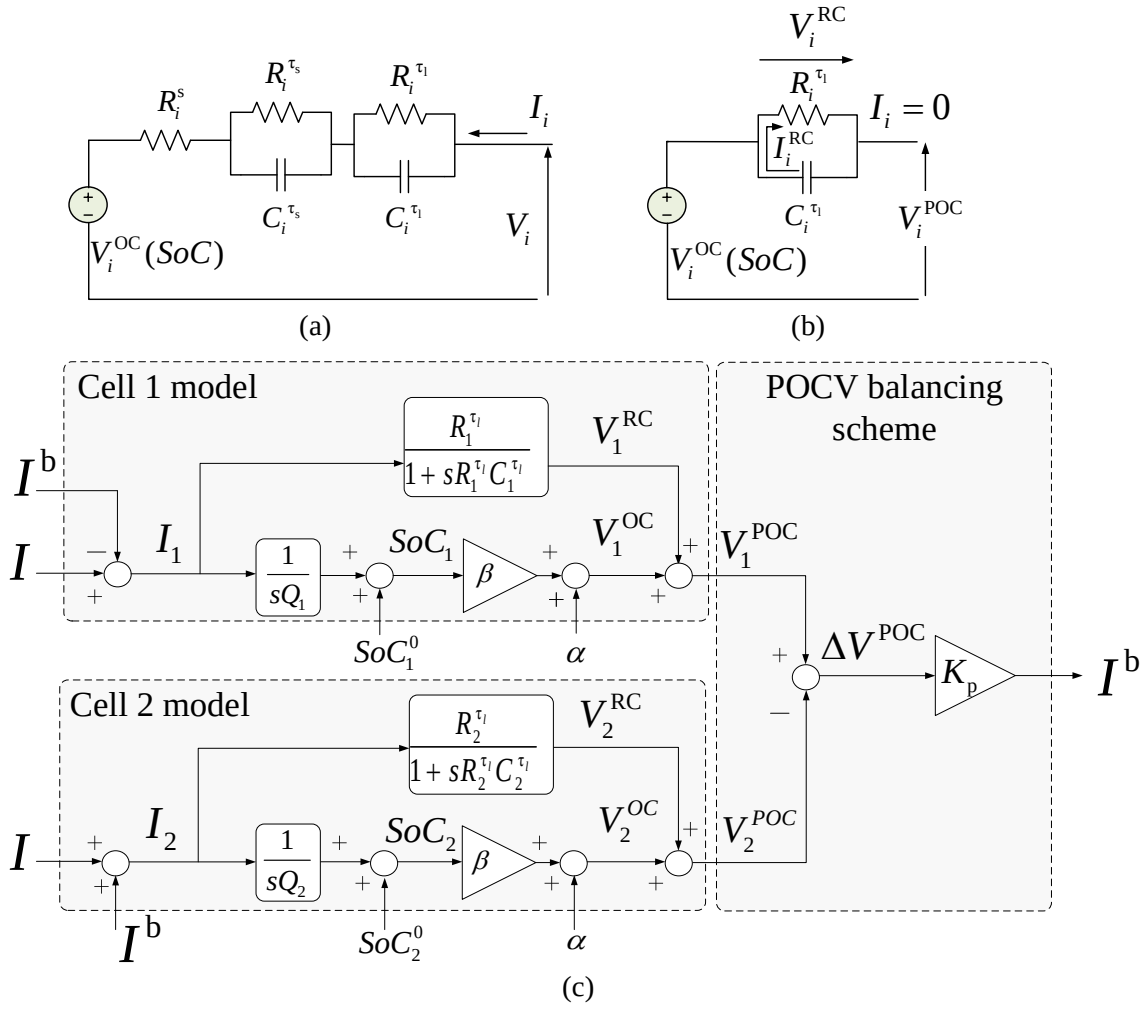


Fig. 2.3 Explaining POCV balancing with the use of RC equivalent circuits: a) generalized equivalent RC circuit of a li-ion cell b) equivalent circuit during idle state (OCV is a function of SoC) c) POCV balancing implemented on two cells (modelled using RC equivalent circuits).

During the idle state, a POCV measurement is made by neglecting the effect of the internal cell resistance and transient phenomena shorter than the duration of the idle state. If the POCV can be considered as an accurate indication of RSoC, SoC balancing can be achieved by balancing the POCVs of the cells. In order to quantify the accuracy of SoC balancing (i.e. the actual difference between the SoC or OCVs of the cells) when their

respective POCVs are balanced, the equivalent cell circuit models presented in Fig. 2.3a are used. The equivalent circuit consists of a controlled voltage source, a series resistance and a number of RC networks depending on the required modelling accuracy [67]. The voltage source V_i^{OC} represents the OCV of the cell i as a function of cell SoC and the series resistance R_i^{s} is used to represent the internal resistance of the cell. The RC branches model the transient behaviour (time constants) associated with diffusion (long time constant typically tens of seconds to minutes, $\tau_{\mathrm{l}} = R^{\tau_{\mathrm{l}}} C^{\tau_{\mathrm{l}}}$) and charge transfer phenomena (short time constant typically tens of milliseconds to seconds, $\tau_{\mathrm{s}} = R^{\tau_{\mathrm{s}}} C^{\tau_{\mathrm{s}}}$) within the cell [146].

With the introduction of the idle state, the effect of the series resistance and the short time constant RC circuits can be neglected so the equivalent circuit is simplified as presented in Fig. 2.3b. However, although the battery current is zero during the idle state, the measured cell voltage is not equal to the true OCV due to the voltage drop caused by the circulating current in the long time constant RC section, thus it is referred to as pseudo-OCV.

In order to estimate the performance of the proposed balancing scheme where POCV is used as an indication of the RSoC, a simplified linear model is constructed. This model contains two cells of different capacities and with different time constants as shown in Fig. 2.3c. Each cell is charged or discharged under a constant current I, that depends on the C-rate, and an additional balancing current I^{b}. To preserve linearity, a linear relationship between OCV and SoC is assumed (i.e. $V^{\mathrm{OC}} = \alpha + \beta SoC$) and a proportional gain K_{P} is used to determine the balancing current from the POCV difference.

Under these assumptions, the final value of the POCV difference is described by (2.7) and the effectiveness of the POCV balancing scheme can be evaluated from the final value of the OCV difference (2.8) (that corresponds to the SoC difference between the cells).

$$\Delta V_{\mathrm{fv}}^{\mathrm{POC}} = \lim_{s \to 0} s \Delta V^{\mathrm{POC}}(s) = \frac{I(Q_2 - Q_1)}{K_{\mathrm{P}}(Q_1 + Q_2)} \tag{2.7}$$

$$\Delta V_{\mathrm{fv}}^{\mathrm{OC}} = \lim_{s\to 0} s\Delta V^{\mathrm{OC}}(s) = \frac{\frac{I}{K_{\mathrm{p}}}(Q_2 - Q_1) + 2I(Q_2 R_2^{\tau_1} - Q_1 R_1^{\tau_1})}{(Q_1 + Q_2)} \tag{2.8}$$

where Q_1, Q_2 are the nominal cell capacities and $R_1^{\tau_1}, R_2^{\tau_1}$ are the respective transient resistances of the cells.

Based on (2.8), the effectiveness of the proposed POCV balancing scheme depends on the applied C-rate (I), the variation between cell parameters (cell capacity and the transient resistance) and the balancing gain K_{P}. In the actual system, the cells are operated under different average currents based on the respective cell position. Each cell position corresponds to a specific average current and therefore even for very low POCV difference between the cells, K_{P} is effectively very large. This is because a difference of a single mV in ΔV^{POC} causes the cells to occupy different places in the priority list and therefore to experience non zero balancing currents. As a result, ΔV^{POC} and ΔV^{OC} can be described by (2.9) and (2.10) for the real system.

$$\lim_{K_{\mathrm{P}}\to\infty} \Delta V_{\mathrm{fv}}^{\mathrm{POC}} = 0 \tag{2.9}$$

$$\lim_{K_{\mathrm{P}}\to\infty} \Delta V_{\mathrm{fv}}^{\mathrm{OC}} = \frac{2I_0\left(Q_2 R_2^{\tau_1} - Q_1 R_1^{\tau_1}\right)}{Q_1 + Q_2} \tag{2.10}$$

According to (2.10), ΔV^{OC} will be zero when identical cells (i.e. cells with equal transient resistance and capacity) are considered, so in this case POCV balancing is expected to lead to OCV and thus SoC balancing.

However, the characteristics of seemingly identical cells are likely to vary due to manufacturing tolerances and cell aging. These variations in cell capacity and circuit parameters introduce a voltage difference between OCVs according to (2.10). A study regarding the effect of cell aging in the parameters of a lithium ion cell is presented in [147], reporting a monotonic increase in the total resistance and the diffusion time constant and a decrease in cell capacity. The change in cell parameters over 3,000 and 6,000 cycles is presented in Table 2.1.

Table 2.1 Cell parameter variation due to aging (from [147]).

Number of cycles	0	3,000	6,000
Cell capacity	Q_{n}	$0.85Q_{\mathrm{n}}$	$0.75Q_{\mathrm{n}}$
Cell resistance	R_{n}	$1.5R_{\mathrm{n}}$	$2R_{\mathrm{n}}$
Diffusion time constant	τ_{n}	$1.25\tau_{\mathrm{n}}$	$1.6\tau_{\mathrm{n}}$

where Q_{n} is the nominal cell capacity at 0 cycles, R_{n} is the nominal cell resistance and τ_{n} is the nominal value of the diffusion time constant.

The OCV difference after POCV balancing of a new and an aged cell (after 6,000 cycles) assuming operation at a 1 C-rate, a nominal capacity of $Q_{\mathrm{n}} = 2.2$ Ah and a nominal cell transient resistance $R_{\mathrm{n}} = 10$ mΩ is 12.6 mV according to (2.10). The corresponding SoC difference depends on the slope of the OCV-SoC curve for the particular cell chemistry under examination. For the Li-po cells whose SoC-OCV curve is presented in Fig. 2.4, a 12.6 mV OCV difference corresponds to 7% SoC difference when the SoCs of the cells are between 10 % and 40 %. The ΔSoC for the same ΔOCV is reduced to 2% when the SoCs of the cells are higher than 80%.

2.2.1 Selecting the duration of the idle state

The idle state duration should be set short enough so that high quality POCV measurements can be taken without increasing the SoC difference between cells (due to different average cell currents) but long enough to ensure that the voltage drop across the short time constant RC network can be neglected. In order to choose an appropriate idle state duration, the operation of the NLC as described in section 2.1 is considered.

The idle state duration is calculated here for a CHB including twelve converter elements with a single cell per element. This configuration is selected as it corresponds to the experimental hardware that will be described later. Although the CHB includes twelve cells, the number of active cells N_{a} is set equal to ten as one cell is always at the idle state and to allow the system to tolerate failure of one cell. The maximum and minimum average cell currents can be calculated by (2.6) with $\sqrt{2}I_{\mathrm{rms}} = 3$ A.

$$I_{\max} = I_1^{\mathrm{p}} = 1.91 \text{ A} \tag{2.11}$$

$$I_{\min} = 0 \text{ A} \quad (\text{redundant cell}) \tag{2.12}$$

The upper limit for the duration of the idle state is selected so that SoC variation due to unequal (dis)charge rates across cells does not exceed 1%, between two consecutive POCV measurement updates. The maximum SoC variation is observed between a cell operating under the maximum cell current and a cell remaining idle and can be found by solving (2.13).

$$I_{\max} d_0 (N_{\mathrm{a}} - 1) \leq 3600 \cdot 0.01 Q_{\mathrm{n}} \tag{2.13}$$

where d_0 is the idle state duration in sec ($d_0(N_{\mathrm{a}} - 1)$ is the duration between two consecutive POCV measurements) and Q_{n} is the nominal capacity of the cell in Ah.

By solving (2.13) for d_0, the maximum idle state duration is 4.6 sec for 2.2 Ah cells (Li-po cells used to validate POCV balancing). According to [148] the charge transfer time constant of Li-po cells of similar capacities to the ones used in this study is 0.12 - 0.46 s depending on cell SoC. As a result, the duration of the idle state is selected to be 3 seconds to ensure that the effect of the short time constant may be neglected whilst also limiting the SoC difference between cells.

2.3 Simulation results of POCV balancing

In order to validate the concept of POCV and quantify the effect of the large time constant on cell balancing, the equivalent RC circuit of a 2.2 Ah Li-po cell is developed and used for simulation. A first-order equivalent RC circuit is typically considered a good compromise between accuracy and computational demands [149]. For the construction of the equivalent circuit model, a SoC – OCV profile extraction test is contacted, followed by the equivalent circuit parameters' estimation. The SoC-OCV extraction test followed here is described in [150]. The cell is discharged from 100 % SoC to 0 % at 1 C (2.2 A for the 2.2 Ah cell). The discharge process is paused (0 A cell current) for 10 min at every 10% change in SoC in order to record the dynamic behaviour of the cell. Once the cell

reaches the lower limit (0% SoC) and after resting for 10 min, the charging process starts using 1 C charging rate and 10 min pauses every 10 % SoC. Once the upper voltage limit is reached (4.2 V) the charging resumes in constant voltage mode until the current is reduced to zero. The SoC – OCV curve presented in Fig. 2.4 is the average of the measured OCVs during the charge and discharge cycles.

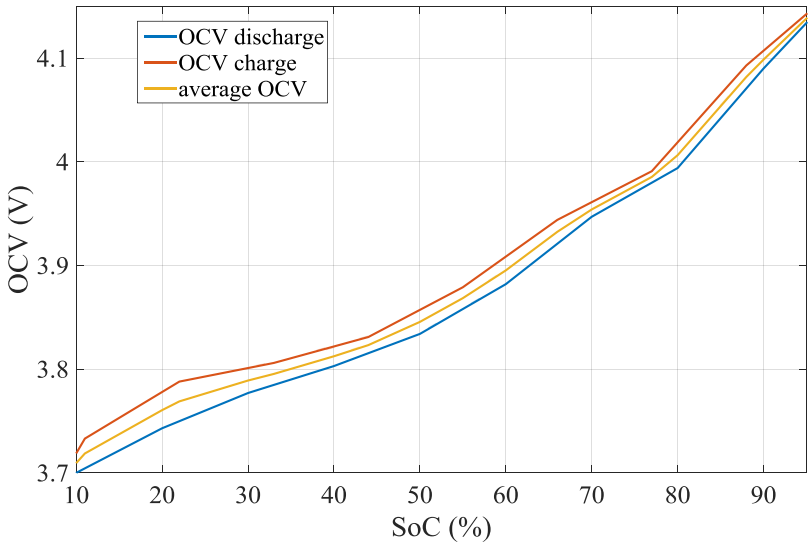


Fig. 2.4 Extracted SoC-OCV curve for the lithium-polymer cell.

To simplify the study, an equivalent circuit with constant parameters over the range of SoC is used. Based on [150] the constant parameters of the equivalent circuit model can be calculated by minimizing the squared error between the measured cell voltage (V_{meas}) and the cell voltage calculated using the equivalent circuit model (V_{mod}) according to (2.14). This optimisation problem is solved using MATLAB Optimisation Toolbox (solver `fmincon`).

$$
\begin{aligned}
F(R^{\mathrm{S}}, R^{\tau_1}, \tau_1) &= \sum_{i=1}^{N} \left(V_{\mathrm{mod}}(i) - V_{\mathrm{meas}}(i)\right)^2 \\
V_{\mathrm{mod}}(i) &= V^{\mathrm{OC}}(i) + I(i)R^{\mathrm{S}} + V^{\mathrm{RC}}(i) \\
V^{\mathrm{RC}}(i) &= V^{\mathrm{RC}}(i-1)e^{\frac{t(i)-t(i-1)}{\tau_1}} + I(i)R^{\tau_1}\left(1 - e^{\frac{t(i)-t(i-1)}{\tau_1}}\right)
\end{aligned}
\tag{2.14}
$$

where N is the number of samples.

The resulting parameters for the equivalent RC circuit are given in Table 2.2.

Table 2.2 Calculated parameters of the equivalent RC circuit model.

Parameter	Symbol	Value
Series resistance	R^{s}	18.4 mΩ
Transient resistance	R^{τ_1}	7.72 mΩ
Diffusion time constant	τ_1	45.0 s

The equivalent circuit model is used to simulate the cases of balancing between twelve identical new cells (i.e. same capacities and parameters of the RC circuit) with a 55% initial SoC variation and balancing between eleven new and one aged cell (using the data from Table 2.1) with the same initial SoC variation. In both simulations the initial cell SoCs are evenly spread between 85% and 30%. In the case of balancing between twelve identical cells (Fig. 2.5a), POCV balancing is achieved at 64 min. During the first discharge cycle, the cells with the highest POCVs are discharged with higher currents but when the charging cycle begins, priority is given to the cells with lower POCVs. In this case, the close agreement between the transient resistances of the cells combined with the equal cell capacities results in accurate OCV balancing ($\Delta V^{\mathrm{OC}} = 0$).

In the second simulation presented in Fig. 2.5b, the parameters of cell 12 are set based on Table 2.1 (considering as nominal values the values presented in Table 2.2), in order to simulate an aged cell (i.e. a cell that has experienced 6,000 cycles). POCV balancing is achieved at 68 min and is retained throughout the simulation. In this case however, the POCV balancing does not lead to a perfect OCV balancing because of the different V^{RC} between the aged cell and all other cells. In order to balance the POCVs, a lower cell current is applied to the aged cell (cell 12 with decreased capacity). This current combined with the increased cell resistance (the internal resistance is doubled based on Table 2.1) introduces a voltage difference ΔV^{RC} of 4 to 6 mV that corresponds to the OCV difference. This difference in OCV is translated to a 0.8 % difference in SoC between the cells at the end of each cycle using Fig. 2.5b. A close agreement is observed in this case, as the effect of the decreased average current of the aged cell is negated to some extent by the simultaneous increase in the transient resistance. Using (2.10) the OCV difference between the cells is calculated at 4.95 mV, thus a good agreement is

observed between simulation and the theoretical calculations. Simulations also confirm the dependence of cell balancing on the C-rate. The OCV error tends to increase proportionally with the C-rate as indicated by (2.10). However the SoC error at the end of a (dis)charge cycle is less than 3.5% for up to 2 C-rate.

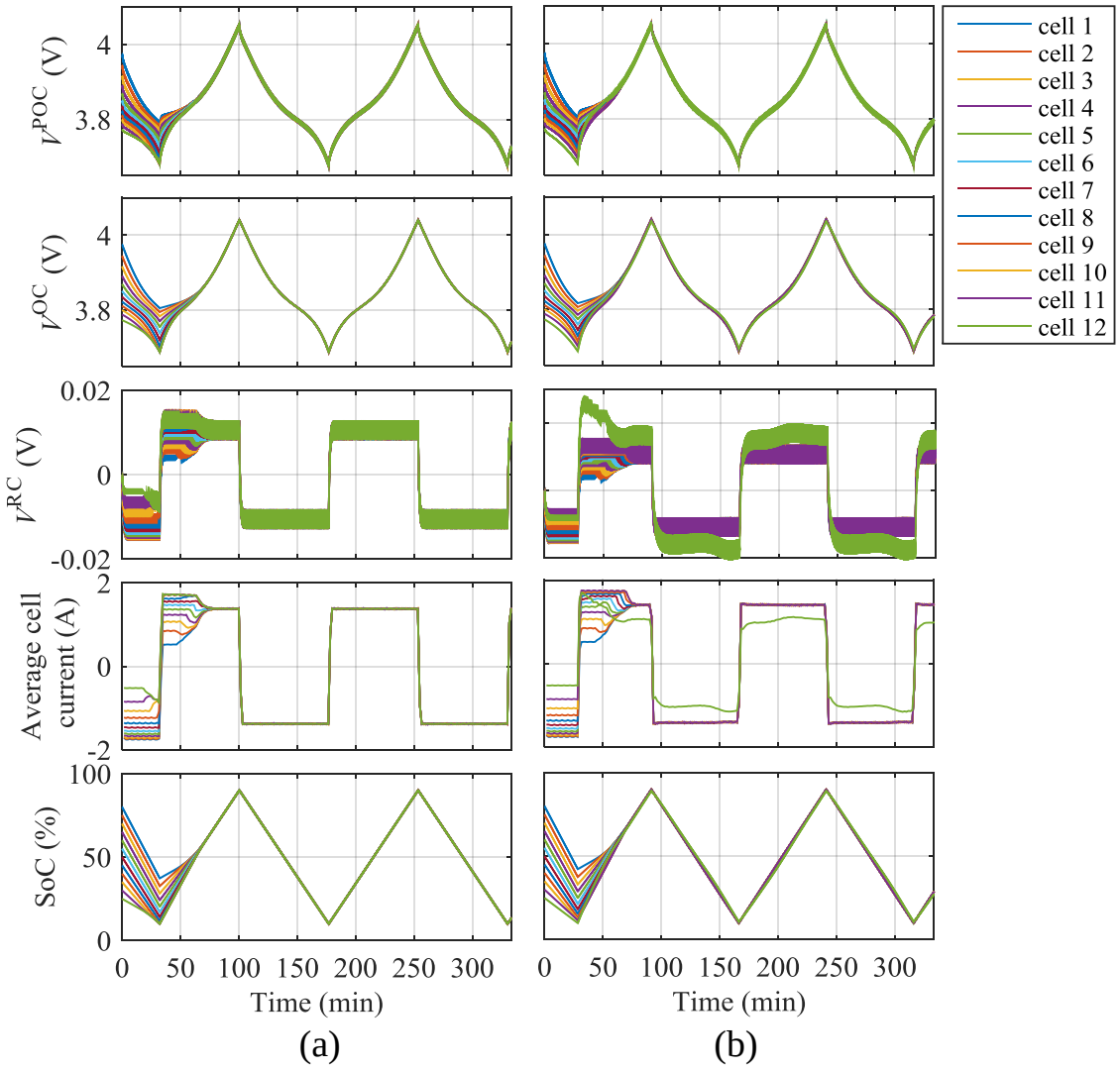


Fig. 2.5 POCV, OCV, RC voltage drop, average cell current and SoC for the simulated balancing of Li-po cells: a) twelve identical new cells b) eleven identical new cells and an aged cell (after 6,000 cycles based on Table 2.1).

2.4 Implementing POCV balancing on a CHB with a centralised BMS

The complete balancing strategy including converter switching using the NLC and RSoC estimation based on POCV measurements is presented in Fig. 2.6a for a single phase CHB with a centralised BMS. The balancing strategy consists of two parallel operations at different execution rates: A slow process of disabling a cell every 3 seconds (idle state) followed by the cell sorting and fast processes (50 kHz in our case) including cell voltage measurements, NLC and switching signal generation.

During the initialisation stage, the POCVs of the cells are updated using their current voltage measurements as the cells are initially idle. After that, each cell is bypassed periodically for a predefined amount of time equal to the idle state duration. At the end of each idle state, the measured cell voltage of the disabled cell is used to update the POCV measurements of that cell. Once a new POCV measurement is made, the priority list L is updated by sorting the cells in ascending or descending order of POCV, depending on the operation (discharging or charging).

The CHB reference voltage used in the NLC is provided by the current controller presented in Fig. 2.6b. For the current controller to work, a single-phase phase locked loop (PLL) [151] is required to synchronize with the angle of the grid voltage θ. Cell current is controlled using two PI controllers to control the *d*-axis and *q*-axis components of the current. The *q*-axis current reference is set to zero to achieve output with unity power factor and the *d*-axis current reference is set to the desired charging/discharging current magnitude. The output of the PI controllers corresponds to the respective *d-q* axis components of the reference voltage. The reference output voltage is then acquired by using the reverse Park transformation.

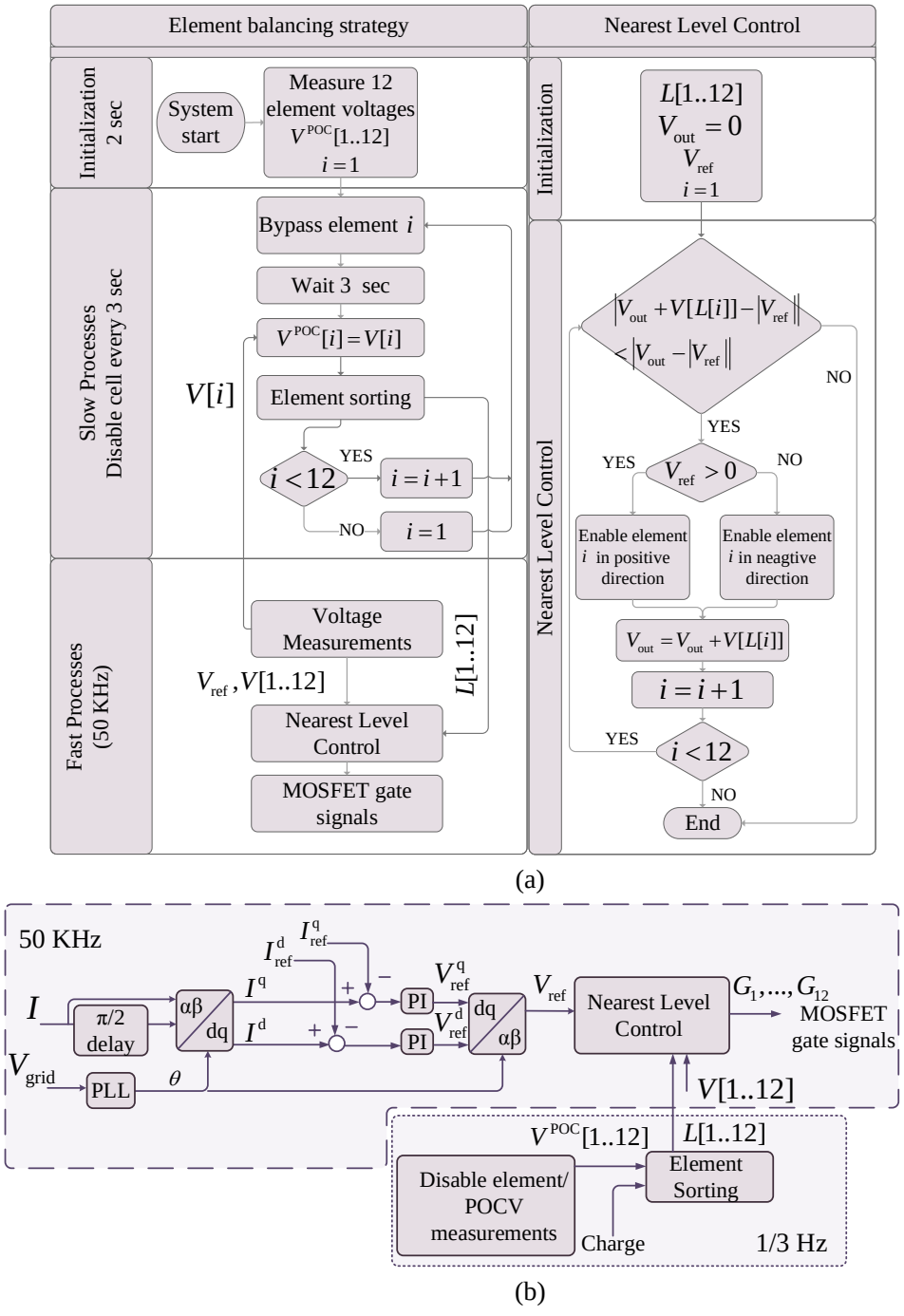


Fig. 2.6 Controller of a CHB-BESS with a flat BMS: a) description of the proposed POCV balancing strategy b) complete control of the single-phase CHB prototype.

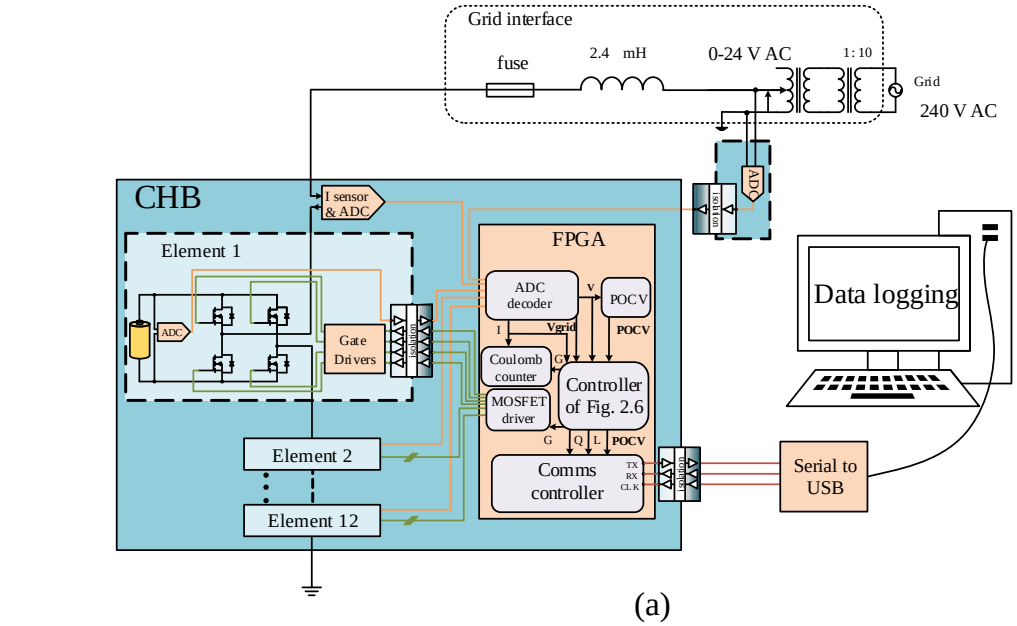
2.5 Experimental validation of POCV balancing

In order to verify the performance of the proposed balancing strategy based on POCV measurements, a single-phase 12 cell CHB is used, where each H-bridge converter element is connected to a single 2.2 Ah Li-po cell. The voltage of each cell and the grid voltage are measured using 12-bit Analog-to-Digital Converters (ADCs) and the output current of the CHB using a Hall effect sensor. The overall control of the CHB as presented in Fig. 2.6 is implemented in Very High Speed Integrated Circuit Hardware Description Language (VHDL) using a Terasic Cyclone IV E Field-Programmable Gate Array (FPGA) located at the Altera DEO-Nano development board. The 12 H-bridges with the respective MOSFET drivers, the ADCs, the current sensor and the FPGA are located on a single Printed Circuit Board (PCB) presented in Fig. 2.7c. Although this is the same hardware as the modules that are combined to form the experimental BESS in Chapter 5, the controller implemented in the FPGA is fundamentally different. In this chapter (as well as in Chapter 3), the centralised BMS approach presented in Fig. 2.6 is used, in contrast to the decentralised architecture explained in Chapter 5. In order to interface the CHB to the grid, a step-down isolation transformer (1:10 turns ratio) is used and the input voltage to the CHB is controlled using a single-phase variac (input voltage can be controlled between 0 and 24 V and is fixed to 20 V RMS during the tests). A 2.4 mH inductor is used to control the power flow to/from the CHB-BESS. The complete experimental system is presented in Fig. 2.7. Once a new POCV measurement is made (every 3 seconds) and the priority list of cells is updated, these data are sent to the lab PC via a serial to USB converter and are stored for further processing.

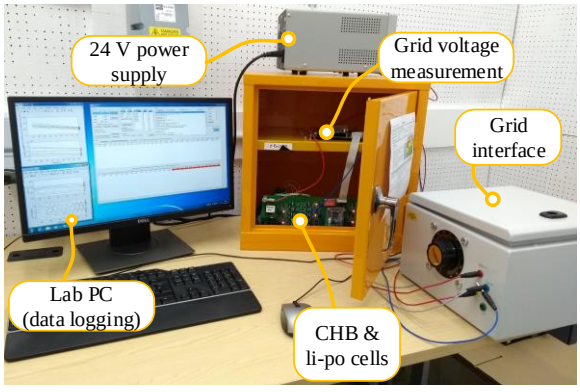
The experimental procedure is described as follows:

1. Initialisation: Prior to each test, all twelve cells are discharged from 100% SoC to different SoC values between 75-20%. After discharge the cells are left to rest for 30 min in order to measure their OCV.
2. Consecutive charging and discharging cycles: The single phase multilevel converter is connected to the grid. The current reference is set as $I_{\mathrm{ref}}^{\mathrm{d}} = 3$ A, $I_{\mathrm{ref}}^{\mathrm{q}} = 0$ A for charging and $I_{\mathrm{ref}}^{\mathrm{d}} = -3$ A, $I_{\mathrm{ref}}^{\mathrm{q}} = 0$ A for discharging. The controller is set to operate the cells in consecutive charging and discharging cycles between the following POCV limits: $V_{\mathrm{max}}^{\mathrm{POC}} = 3.9$ V, $V_{\mathrm{min}}^{\mathrm{POC}} = 3.7$ V. This corresponds to

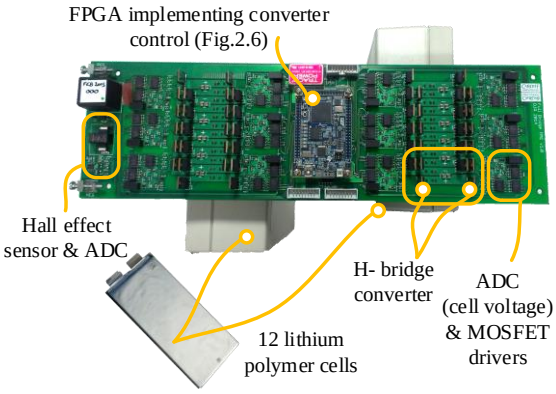
consecutive cycles between 15% and 65% SoC. The above POCV limits are selected in order to ensure that the terminal voltage of any cell does not exceed the suggested voltage limits (3 V when discharging and 4.2 V when charging) at any point during operation. After five consecutive cycles, operation is terminated and the cells are left to rest for 20 min. The results from two tests are presented here: balancing of twelve 2.2 Ah cells and balancing of eleven 2.2 Ah cells and a 1 Ah cell.



(a)



(b)



(c)

Fig. 2.7 Experimental setup of POCV balancing: a) schematic of experimental setup b) photo of the experimental setup c) 25-level CHB prototype.

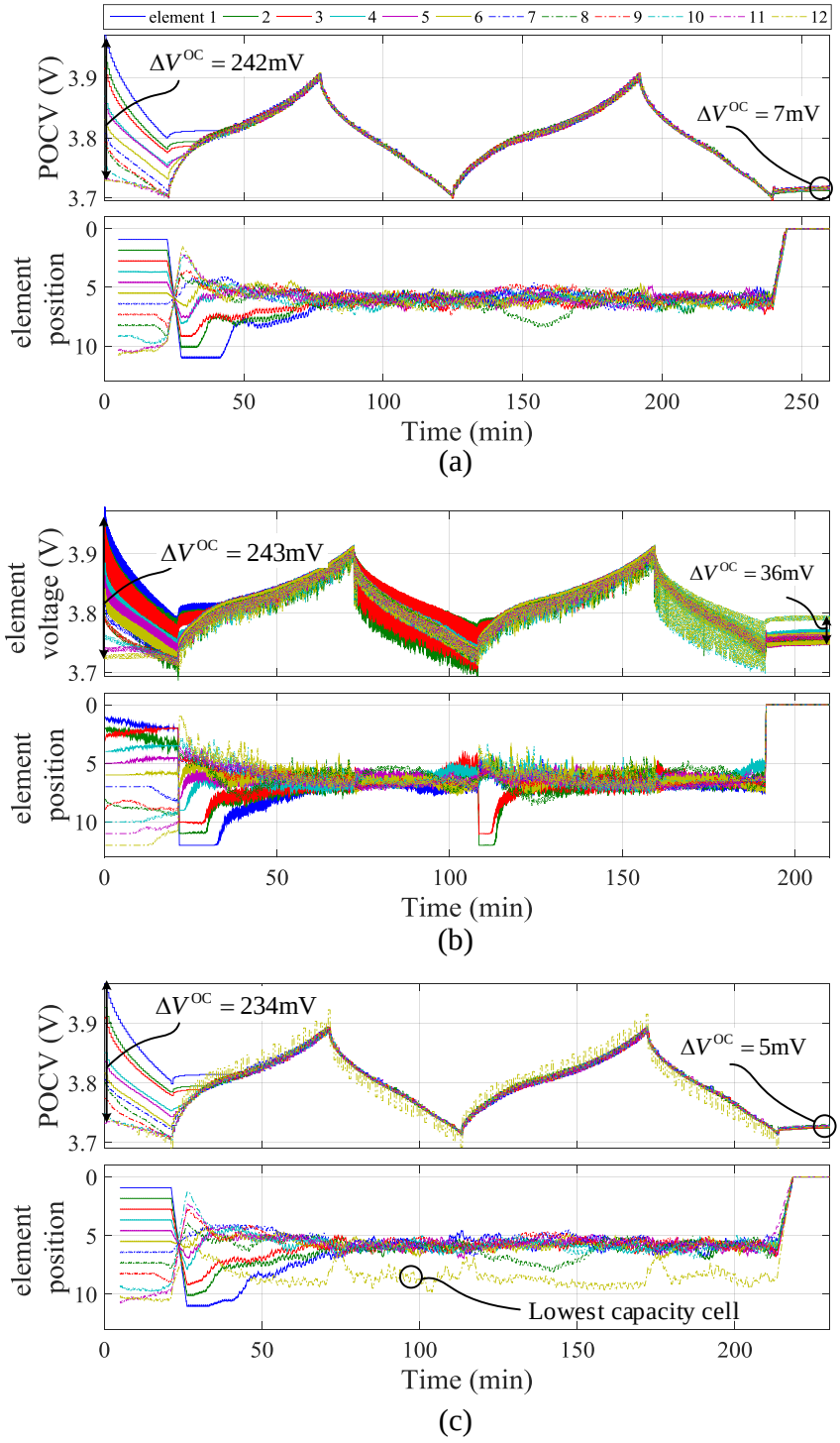


Fig. 2.8 POCV and average element position over 100 samples for the balancing test: a) of twelve cells with a 2.2 Ah nominal capacity b) of twelve cells with a 2.2 Ah nominal capacity, without using the idle state for POCV measurements. (c) Eleven cells with a 2.2 Ah nominal capacity and a cell with a 1 Ah nominal capacity

2.5.1 Balancing of twelve 2.2 Ah cells

The different POCVs of the twelve cells in Fig. 2.8a at the beginning of the test correspond to the initial SoC variation between the cells. During discharge, the cells with the highest POCVs (cells 1-3) are placed in the highest cell positions (closer to one) in order to be discharged with higher cell currents. Discharge operation is terminated when $V_{\min}^{\mathrm{POC}}$ is reached by cell 11 and the first charging cycle begins. The output voltage and current of the CHB at the transition between discharging and charging is presented in Fig. 2.9. Since the magnitude of the output current is constant, the increase in the converter output voltage observed during discharge (due to grid impedance) leads to a higher discharge rate at 0.6 C compared to 0.45 C during charging (since more cells participate in the construction of the stepped output voltage).

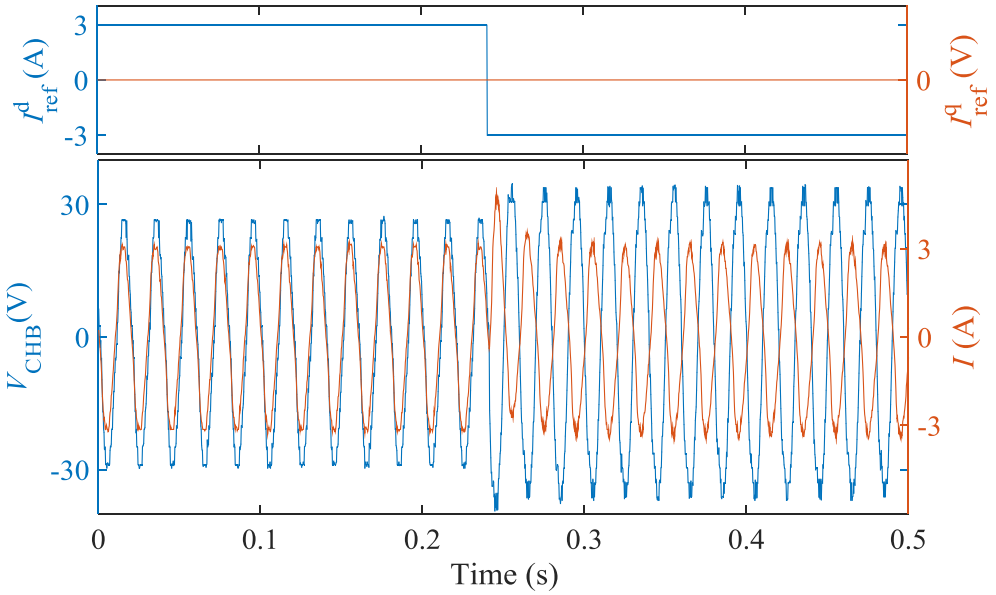


Fig. 2.9 Experimental multilevel converter output voltage and current during the transition between charging and discharging.

During charging, priority is given to the cells with the lowest POCVs (cells 10-12) which are now placed in the higher cell positions and POCV balancing is achieved around 40 min. In order for the cells to remain balanced, the algorithm needs to respond rapidly to POCV deviations by adjusting cell position. Balancing is retained by operating the cells equally as indicated by the close agreement in average cell position in Fig. 2.8a.

The adaptiveness of the balancing is demonstrated around 150 min where the position of cell 8 is adjusted to lower values in order to compensate for the decreased capacity of the cell compared to the rest (2 Ah measured cell capacity for cell 8 compared to 2.2 Ah nominal capacity). After the end of the third discharge cycle the cells are left to rest for 20 min. The effectiveness of the balancing strategy is verified by the close agreement of the measured OCV (within 8 mV).

In order to demonstrate the effect of the short time constant on cell balancing, the previous test is repeated but instead of the POCV, balancing is now performed using the cell voltage measured during the zero crossings (Fig. 2.2b). The negative effect of the low quality voltage measurements used in this case is evident during the discharge cycles of Fig. 2.8b. During the second discharge cycle (72-108 min) the voltages of cells 2 and 3 alternate, causing the cells to be placed constantly either on the first or the last cell position. As a result these cells are always discharged either with the highest or with the lowest cell current, maintaining a voltage fluctuation that reaches up to 80 mV. Due to the low quality of voltage measurements, the SoC variation between these two cells and the rest cannot be detected by the balancing algorithm and so the cells are equally discharged as can be seen by the close agreement of their average cell position (Fig. 2.8b). Similar behaviour is observed during the third discharge cycle (159-191 min) between cells 10 and 12. After the cells relax at the end of the test a 30 mV difference is observed between the voltages of these two cells and the rest.

2.5.2 Balancing of eleven 2.2 Ah cells and a 1 Ah cell

In this test cell 12 was replaced with a 1 Ah cell (45% of the nominal capacity of the other cells) and the operation of the CHB is presented in Fig. 2.8c. The balancing strategy in this case is expected to overcome the initial SoC imbalance between the cells as well as the difference in cell capacity. During discharge the balancing algorithm places the cells with the higher POCVs (cells 1-3) on higher cell positions (higher discharge current). When charging, operation is reversed and the cells with the lower POCVs (cells 9-11) are placed at the top positions of the priority list. POCV balancing in this case is achieved at 40 min. Here, a large fluctuation in POCV measurements is observed for cell 12 (i.e. the low capacity cell). The reason for this is the difference in cell capacity that causes it to experience rapid changes in SoC between two consecutive POCV measurements (36

seconds), compared to the other cells (that have approximately twice the capacity). These rapid SoC changes are reflected in the OCV and can be observed in the measured POCV. Based on the estimated SoC and the observed cell position, cell balancing is achieved around 75 min. In order for the cells to remain balanced, the balancing algorithm ensures that cell 12 is operated at a lower duty cycle (average cell position between 8 and 10) compared to cells 1-11 (average cell position close to 6). The position of cell 8 is also adjusted around 130 min in the test (since this cell has 10% lower capacity). After the cells relax at the end of the test, the good agreement between OCVs (within 5 mV) demonstrates that the balancing strategy can tolerate very large capacity variation as well as a SoC difference between cells.

2.6 Conclusions

This chapter demonstrated the operation of a single phase CHB-BESS with a centralised BMS. Using a NLC modulation strategy, a high quality stepped output voltage can be produced and cell balancing can be achieved by controlling the average current of each cell according to their relative SoC. In order to accurately estimate the relative cell SoC, the concept of the idle state was introduced. During the idle state, the cell is temporarily removed from the current path for a short period of time. As a result, the effect of the series resistance and short time transient phenomena can be neglected and therefore cell voltage measurements taken during the idle state can be used as a pseudo-OCV measurement. The effectiveness of the proposed POCV balancing depends on the applied C-rate and the difference in cell capacities and transient resistance. The proposed strategy was validated experimentally using a 25-level CHB converter prototype for the balancing of 12 Li-po cells during consecutive charging and discharging cycles, demonstrating the ability to overcome significant SoC and capacity variations between cells. The experimental results further support the importance of selecting an appropriate idle state duration, since the effect of the short time constants on POCV measurements can otherwise significantly reduce the quality of balancing.

Chapter 3 Balancing performance evaluation of active balancing circuits

This chapter approaches the balancing problem as a linear programming problem with the objective of maximising the useable capacity of a pack comprising cells with different capacities. The proposed framework encompasses DCB architectures such as the CHB and ERB architectures such as A-C2C, D-C2C and C2P. The aim of this chapter is to compare and contrast the balancing performance of battery packs that use ERB and DCB balancing circuits. Here, 'balancing performance' is defined as the ability to effectively distribute charge among the cells of the pack according to their respective capacities. Accessing the total cell capacity (sum of individual cell capacities) of a pack comprising cells with different individual cell capacities is not always possible as it depends on cell redundancy for the DCB and the maximum balancing current (that dictates the size of balancing circuit) in ERB circuits. As a result, the balancing performance can be quantitatively evaluated by calculating the useable capacity of the pack i.e. the percentage of the total cell capacity that can be accessed and used. The numerical prediction of the useable capacity when different ERB circuit are used is validated through simulation and experimentally for the DCB case using the hardware described in Chapter 2. This chapter is based on publication [131].

3.1 Duty cycle balancing as a linear programming problem

In this section, the balancing performance of DCB circuits is modelled under the same linear programming framework. The balancing performance is evaluated by examining

the ability of each circuit to overcome a capacity imbalance between the cells within one cycle of operation. It should be noted that capacity imbalance is fundamentally different to SoC imbalance. A balancing circuit can eventually overcome any SoC imbalance between the cells as long as a slightly different charge can be applied to each cell during each cycle. However, in order to overcome a capacity imbalance between cells, the balancing circuit should be able to operate different cells under sufficiently different currents (according to each cell's capacity) at every operating cycle. The SoC balancing speed is also directly associated with the ability of the system to cope with varying capacities since this also depends on the rate at which the system is able to differentially distribute charge between cells.

3.1.1 Duty cycle balancing for DC PEEBPs (DCB-DC)

In a PEEBP using DCB, balancing can be performed by controlling the effective duty cycle of each cell so that the cells with higher capacities are 'used more' than those with lower capacities. This can be achieved by bypassing the cells using active switches as in Fig. 3.1. The average current of each cell i during operation can be described by:

$$I_i = I + I_i^{\mathrm{b}} \tag{3.1}$$

where I is the pack output current and I_i^{b} is the average balancing current of cell i:

$$I_i^{\mathrm{b}} = \frac{-It_i^{\mathrm{b}}}{T} \tag{3.2}$$

where T is the length of operation (the length of one full charge or discharge cycle) and t_i^{b} the balancing time of cell i. When performing DCB a cell can either be operated normally with the cell current equal to pack current, or bypassed so that cell current is equal to zero.

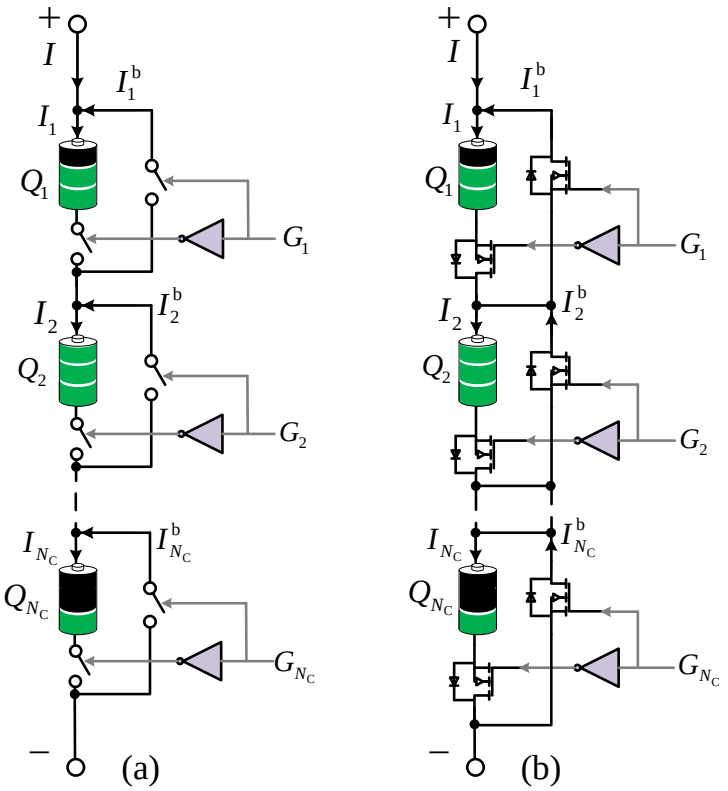


Fig. 3.1 Duty cycle balancing circuit architecture: a) general circuit b) duty cycle balancing DC pack using a half-bridge converter per cell.

The constraints on the balancing time t_i^{b} are then:

$$0 \leq t_i^{\mathrm{b}} \leq T \tag{3.3}$$

When t_i^{b} is equal to T the cell is bypassed throughout the operation and the average cell current is zero. For a balancing time equal to zero the cell is always in the current path and the average cell current is equal to the pack current I. In order to be able to provide the required output voltage while performing DCB, a number of redundant cells should be included in the pack:

$$r = \frac{N_{\mathrm{C}} - N_{\mathrm{a}}}{N_{\mathrm{C}}} \tag{3.4}$$

where r is the cell redundancy ratio, N_{C} is the total number of cells and N_{a} is the number of cells that should always be active throughout the operation of the pack to ensure the output voltage is maintained at a constant level. Due to the redundancy the average cell current is:

$$\frac{\sum_{i=1}^{N_{\mathrm{C}}} I_i}{N_{\mathrm{C}}} = \frac{N_{\mathrm{a}} I}{N_{\mathrm{C}}} \tag{3.5}$$

Substituting (3.1) and (3.2) into (3.5):

$$\frac{N_{\mathrm{a}} I}{N_{\mathrm{C}}} = I - \frac{I}{T N_{\mathrm{C}}} \sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{b}} \tag{3.6}$$

The length of operation T is equal to the duration of time needed to extract the useable capacity of the cells with a pack current I. Taking into account redundancy the operational time is given by:

$$T = \frac{\sum_{i=1}^{N_{\mathrm{C}}} n_i Q_i}{N_{\mathrm{a}} I} \tag{3.7}$$

where n_i is the useable (or accessible) fraction of the capacity Q_i of cell i. This fraction must lie between 0 and 1 for all cells:

$$0 \leq n_i \leq 1 \,, \forall\, i \in [1 \ldots N_{\mathrm{C}}] \tag{3.8}$$

Substituting (3.7) into (3.6):

$$\frac{N_{\mathrm{C}} - N_{\mathrm{a}}}{N_{\mathrm{a}} I} \sum_{i=1}^{N_{\mathrm{C}}} n_i Q_i = \sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{b}} \tag{3.9}$$

The useable capacity of each cell is:

$$I_i T = n_i Q_i \tag{3.10}$$

Substituting (3.1), (3.2) and (3.7) into (3.10):

$$\overbrace{\frac{\overbrace{\sum_{\mathrm{i=1}}^{N_\mathrm{C}} n_i Q_i}^{\substack{\text{average cell}\\ \text{charge in pack}}}}{N_\mathrm{a}}}^{\substack{\text{average cell}\\ \text{charge in pack}}} - \overbrace{I t_i^\mathrm{b}}^{\substack{\text{cell } i\\ \text{bypass charge}}} = \overbrace{n_i Q_i}^{\substack{\text{useable capacity}\\ \text{of cell } i}} \tag{3.11}$$

3.2 Duty cycle balancing for AC PEEBPs (DCB-AC) based on the CHB

Battery packs that perform direct DC to AC conversion, such as the CHB topology presented in Chapter 2, can be considered as a more complex version of DCB-DC. Using the CHB with a NLC modulation scheme, a stepped output voltage (with a voltage step equal to the cell voltage) close to a sinusoidal voltage reference is produced by sequentially switching the converter modules and as a result of this operation, each cell experiences different average cell current due to the varying duration of time that the cells are placed in the current path (Fig. 2.2). The average cell current assigned to each cell position j was calculated in Chapter 2:

$$I_j^\mathrm{p} = \frac{2}{\pi}\sqrt{2} I_\mathrm{rms} \sqrt{1 - \left(\frac{j - 0.5}{N_\mathrm{a}}\right)^2} \tag{3.12}$$

where I_rms is the output rms current of the DCB-AC pack.

Due to the different average cell currents associated with each position, it is necessary to track the total duration of time that each cell spends at each of the different positions. The number of cell positions is always equal to the number of cells since even when a number of redundant cells are used, these will be allocated to an equivalent number of idle positions with zero cell current. Consequently, the total time that each cell i spends at the different positions j as well as the total time a position j is occupied by any cell i should sum to the total time of operation:

$$\sum_{i=1}^{N_\mathrm{C}} t_{ij} = \sum_{j=1}^{N_\mathrm{C}} t_{ij} = \frac{\sum_{i=1}^{N_\mathrm{C}} n_i Q_i}{\sum_{j=1}^{N_\mathrm{C}} I_j^\mathrm{p}} \quad ,\forall\, i,j \in [1 \dots N_\mathrm{C}] \tag{3.13}$$

$$t_{ij} \geq 0, \qquad \forall\, i,j \in [1 \dots N_\mathrm{C}] \tag{3.14}$$

The useable capacity of each cell is in this case equal to accumulated charge that the cell receives while occupying different cell positions:

$$\sum_{j=1}^{N_\mathrm{C}} I_j^\mathrm{p} t_{ij} = n_i Q_i, \qquad \forall\, i \in [1 \dots N_\mathrm{C}] \tag{3.15}$$

The DCB-DC case can also be formulated as a DCB-AC problem with the position current of the first N_a positions equal to the pack current (N_a cells should always be online during operation to ensure that the rated pack voltage is met) and the remaining $N_\mathrm{C} - N_\mathrm{a}$ positions equal to zero current (these correspond to the positions of the redundant cells which are bypassed). However, this results in a problem with redundant decision variables and thus it is reduced to the more compact formulation presented in the previous section.

3.3 Energy redistribution balancing as a linear programming problem

In this section the balancing performance of the direct cell-to-cell (D-C2C), adjacent cell-to-cell (A-C2C) and cell-to-pack (C2P) ERB architectures is explored under a common linear programming framework.

3.3.1 Direct cell-to-cell active balancing (D-C2C)

For a battery pack including series connected cells coupled to a D-C2C balancing circuit as in Fig. 3.2, the average current of each cell i is given by (3.1). Using a shared

energy storage element, energy can be extracted or inserted to cell i from any cell in the pack. The balancing current of cell i is then:

$$I_i^{\mathrm{b}} = \frac{bI}{T}(t_i^{\mathrm{c}} - t_i^{\mathrm{d}}) \tag{3.16}$$

where b effectively determines the 'size' of the balancing circuits: a larger value of b means a larger balancing current can be applied; this makes the problem formulation independent of C-rate because the maximum balancing current, and therefore the balancing circuit size, is scaled with the pack current I. t_i^{c} is the 'charging' balancing time i.e. the time during which cell i receives charge and t_i^{d} the 'discharging' balancing time i.e. the time during which charge is extracted from cell i. The balancing times t_i^{c} and t_i^{d} are constrained such that:

$$0 \leq t_i^{\mathrm{c}} \leq T \quad \forall\, i \in [1 \ldots N_{\mathrm{C}}] \tag{3.17}$$

$$0 \leq t_i^{\mathrm{d}} \leq T \quad \forall\, i \in [1 \ldots N_{\mathrm{C}}] \tag{3.18}$$

$$t_i^{\mathrm{c}} + t_i^{\mathrm{d}} \leq T \quad \forall\, i \in [1 \ldots N_{\mathrm{C}}] \tag{3.19}$$

When a shared storage element is used for energy exchange (e.g. in a single-inductor balancing circuit) the sum of the charging times should be less than the total time of operation since balancing can be performed only between two cells at a time:

$$\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{c}} \leq T \tag{3.20}$$

Assuming a constant efficiency η for the balancing circuit [81], the total power the cells receive is:

$$\sum_{i=1}^{N_{\mathrm{C}}} V_i \frac{bIt_i^{\mathrm{c}}}{T} = \eta \sum_{i=1}^{N_{\mathrm{C}}} V_i \frac{bIt_i^{\mathrm{d}}}{T} \tag{3.21}$$

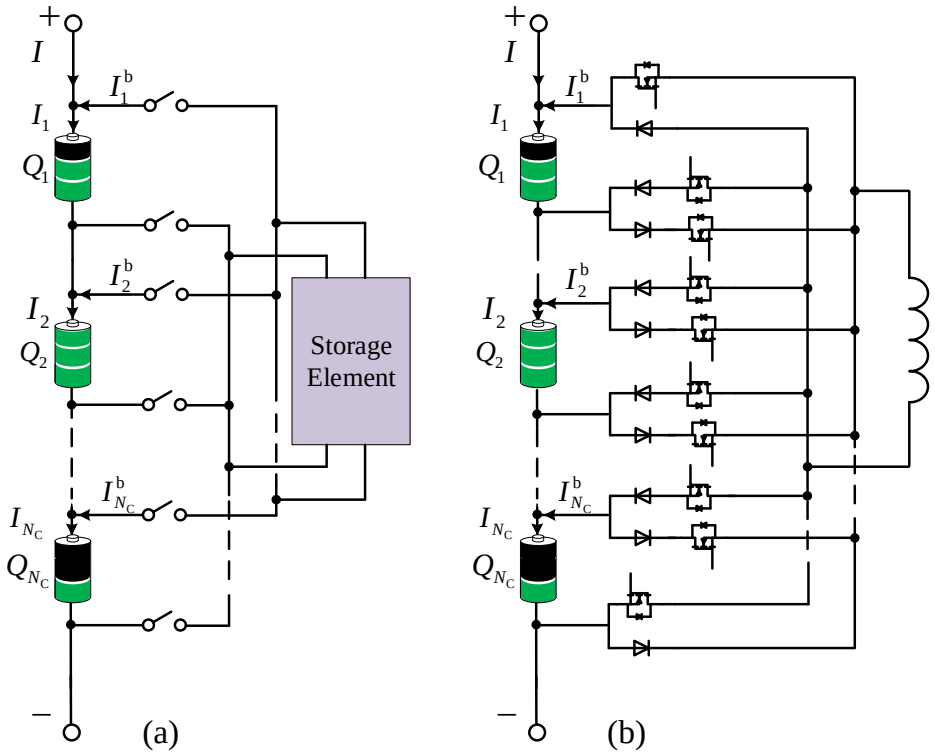


Fig. 3.2 Direct cell-to-cell balancing circuit architecture: a) general circuit b) single inductor D-C2C balancing circuit.

Since the purpose of the balancing circuit is to ensure that the cells remain balanced or within a close SoC range during operation (and thus have similar cell voltages), the cell voltages V_i can be assumed to be equal [81] and (3.21) can be simplified to:

$$\sum_{i=1}^{N_C} t_i^c = \eta \sum_{i=1}^{N_C} t_i^d \tag{3.22}$$

In a battery pack with a D-C2C balancing circuit and a pack current I, using (3.1), (3.10) and (3.16) T is given by:

$$T = \frac{\sum_{i=1}^{N_C} n_i Q_i - bI\left(\sum_{i=1}^{N_C} t_i^c - \sum_{i=1}^{N_C} t_i^d\right)}{N_C I} \tag{3.23}$$

Substituting (3.1), (3.16), (3.22) and (3.23) in (3.10) provides:

$$\overbrace{\frac{\overbrace{\sum_{i=1}^{N_\mathrm{C}} n_i Q_i}^{\text{average cell charge in pack}}}{N_\mathrm{C}}}^{\text{useable capacity of cell } i} - \overbrace{\frac{\overbrace{bI(\eta-1)\sum_{i=1}^{N_\mathrm{C}} t_i^{\mathrm{d}}}^{\text{balancing circuit losses}}}{N_\mathrm{C}}}^{\text{useable capacity of cell } i} + \overbrace{\overbrace{bI(t_i^{\mathrm{c}} - t_i^{\mathrm{d}})}^{\text{balancing charge for cell } i}}^{\text{useable capacity of cell } i} = \overbrace{n_i Q_i}^{\text{useable capacity of cell } i} \tag{3.24}$$

The time of operation T should always be less than or equal to the maximum possible time of operation i.e. the time needed to completely extract the charge from every cell at the average pack current: $T \leq \frac{1}{N_\mathrm{C} I}\sum_{i=1}^{N_\mathrm{C}} Q_i$. This results in the following inequality expressed in terms of the decision variables:

$$\sum_{i=1}^{N_\mathrm{C}} (1 - n_i) Q_i \geq bI(1-\eta)\sum_{i=1}^{N_\mathrm{C}} t_i^{\mathrm{d}} \tag{3.25}$$

3.3.2 Adjacent cell-to-cell active balancing (A-C2C)

When the A-C2C architecture is used, each cell is restricted in exchanging energy only with its adjacent cells. According to Fig. 3.3, each cell i (apart from the first and last cells in a string) is connected to balancing circuits i and $i-1$ and the cell can either receive or extract energy from its adjacent cells using these two balancing circuits.

The average cell current in this case can also be described by (3.1), with the average cell balancing current now being equal to the sum of the currents provided by the adjacent balancing circuits (assuming equal cell voltages):

$$\begin{aligned} I_i^{\mathrm{b}} &= \left(\eta\frac{bIt_i^{\mathrm{cc}}}{T} - \frac{bIt_i^{\mathrm{cd}}}{T}\right) - \left(\frac{bIt_{i-1}^{\mathrm{cc}}}{T} - \eta\frac{bIt_{i-1}^{\mathrm{cd}}}{T}\right) \\ &= \frac{bI}{T}\left(\eta t_i^{\mathrm{cc}} - t_i^{\mathrm{cd}} - t_{i-1}^{\mathrm{cc}} + \eta t_{i-1}^{\mathrm{cd}}\right) \end{aligned} \tag{3.26}$$

where t_i^{cc} is the 'charging' time of cell i through circuit i i.e. the time during which the balancing circuit i is extracting energy from cell $i+1$ to cell i, t_i^{cd} is the 'discharging' time of cell i through circuit i, that is the time during which the balancing circuit i is extracting energy from cell i to cell $i+1$ and η the efficiency of the balancing circuit. For the charging and discharging times:

$$0 \leq t_i^{cc} \leq T\,, i \in [1..N_C - 1] \tag{3.27}$$

$$0 \leq t_i^{cd} \leq T\,, i \in [1..N_C - 1] \tag{3.28}$$

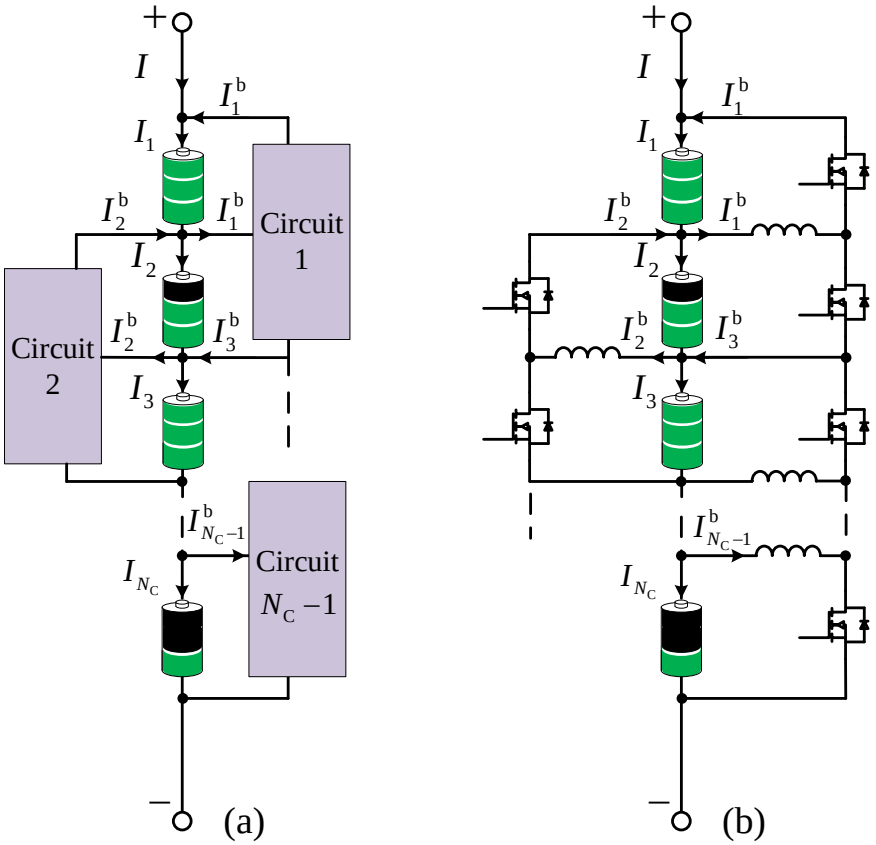


Fig. 3.3 Adjacent cell-to-cell balancing circuit architecture: a) general circuit b) coupled inductor A-C2C balancing circuit

The total time duration that a balancing circuit is used should be less than or equal to the total time of operation:

$$t_i^{\mathrm{cc}} + t_i^{\mathrm{cd}} \leq T \ , i \in [1..N_{\mathrm{C}} - 1] \tag{3.29}$$

From (3.1), (3.10) and (3.26) the balancing time for A-C2C is calculated:

$$T = \frac{\sum_{i=1}^{N_{\mathrm{C}}} n_i Q_i + bI(1-\eta)\left(\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{cc}} + \sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{cd}}\right)}{N_{\mathrm{C}} I} \tag{3.30}$$

Substituting (3.1), (3.26) and (3.30) in (3.10) provides the following equality:

$$\overbrace{\frac{\sum_{i=1}^{N_{\mathrm{C}}} n_i Q_i}{N_{\mathrm{C}}}}^{\substack{\text{average cell} \\ \text{charge in pack}}} + \overbrace{\frac{bI(1-\eta)\left(\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{cc}} + \sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{cd}}\right)}{N_{\mathrm{C}}}}^{\text{balancing circuit losses}} + \overbrace{bI\left(\eta t_i^{\mathrm{cc}} - t_i^{\mathrm{cd}} - t_{i-1}^{\mathrm{cc}} + \eta t_{i-1}^{\mathrm{cd}}\right)}^{\substack{\text{balancing} \\ \text{charge for cell } i}} = \overbrace{n_i Q_i}^{\substack{\text{useable} \\ \text{capacity} \\ \text{of cell } i}} \tag{3.31}$$

Similar to (3.25):

$$\sum_{i=1}^{N_{\mathrm{C}}} (1 - n_i) Q_i \geq bI(1-\eta)\left(\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{cc}} + \sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{cd}}\right) \tag{3.32}$$

3.3.3 Cell-to-pack active balancing (C2P)

In the C2P architecture, energy is extracted from individual cells according to their relative SoC and is fed back to the pack (Fig. 3.4a):

$$\eta \sum_{i=1}^{N_C} V_i I_i^b = N_C V_i I_{pb} \tag{3.33}$$

where I_{pb} is the balancing current that is returned from the balancing circuit to the pack and η the efficiency of the balancing circuit. With the assumption of equal cell voltages:

$$I_{pb} = \eta \frac{\sum_{i=1}^{N_C} I_i^b}{N_C} \tag{3.34}$$

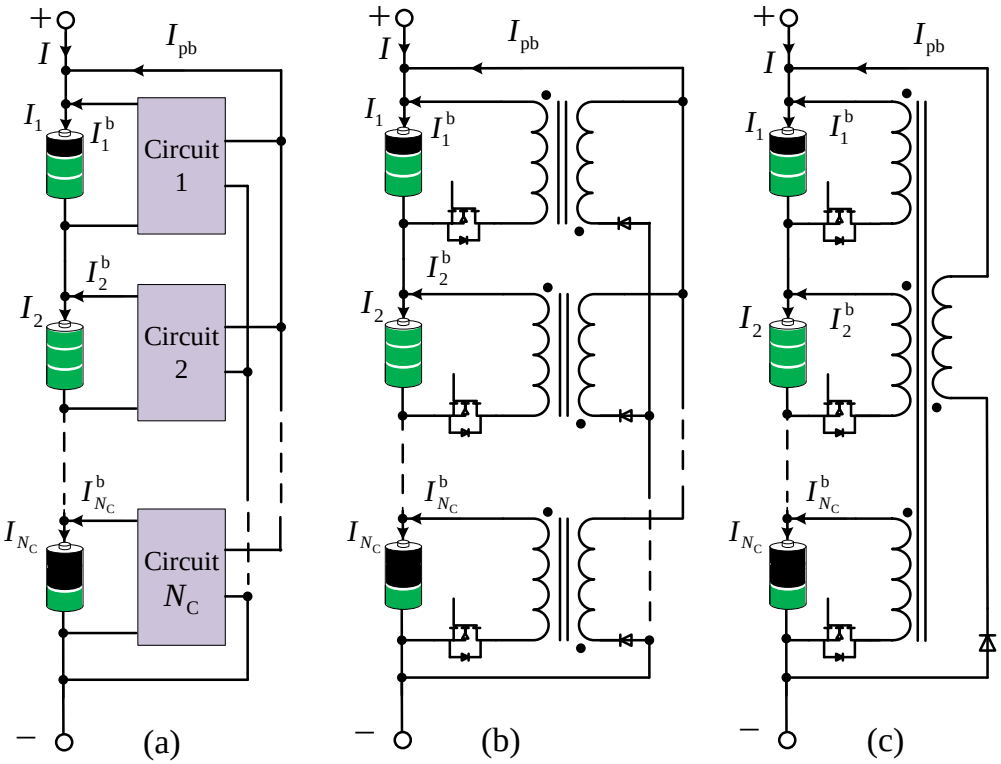


Fig. 3.4 Cell-to-pack balancing circuit architecture: a) general circuit b) multiple transformers balancing circuit (C2P-distributed) c) multi-windings forward transformer balancing circuit (C2P-shared)

The average cell current is:

$$I_i = \overbrace{I}^{\text{pack current}} - \overbrace{\frac{bIt_i^{\mathrm{b}}}{T}}^{\text{balancing current extracted from cell } i} + \overbrace{\eta\frac{bI\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{b}}}{N_{\mathrm{C}}T}}^{\text{balancing current returned to the pack}} \tag{3.35}$$

The balancing time t_i^{b} in this case is equal to the total time during which energy is transferred from cell i to the pack via its respective balancing circuit:

$$0 \leq t_i^{\mathrm{b}} \leq T\,, \forall\, i \in [1 \ldots N_{\mathrm{C}}] \tag{3.36}$$

When a shared storage element is used for energy exchange (e.g. balancing circuits with a single winding or multiwinding transformer as in Fig. 3.4c) the sum of the cells' balancing times must be less than the total time of operation:

$$\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{b}} \leq T \tag{3.37}$$

This constraint should not be considered in cases where individual balancing circuits are used for each cell, such as in multiple transformers C2P balancing depicted in Fig. 3.4b [152].

From (3.10) and (3.35), the operation time for the C2P is:

$$T = \frac{\sum_{i=1}^{N_{\mathrm{C}}} n_i Q_i + bI(1-\eta)\left(\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{b}}\right)}{N_{\mathrm{C}} I} \tag{3.38}$$

From (3.1), (3.35) and (3.38) the useable capacity of each cell in a C2P architecture is:

$$\overbrace{\frac{\sum_{i=1}^{N_\mathrm{C}} n_i Q_i}{N_\mathrm{C}}}^{\text{average cell charge in pack}} + \overbrace{\frac{(1-\eta) bI \sum_{i=1}^{N_\mathrm{C}} t_i^\mathrm{b}}{N_\mathrm{C}}}^{\text{balancing losses}} - \overbrace{bI t_i^\mathrm{b}}^{\text{balancing charge for cell } i} + \overbrace{\frac{\eta bI \sum_{i=1}^{N_\mathrm{C}} t_i^\mathrm{b}}{N_\mathrm{C}}}^{\text{balancing charge returned to pack}} = \overbrace{n_i Q_i}^{\text{useable capacity of cell } i} \tag{3.39}$$

which can be simplified to:

$$\frac{\sum_{i=1}^{N_\mathrm{C}} n_i Q_i}{N_\mathrm{C}} - bI t_i^\mathrm{b} + \frac{bI \sum_{i=1}^{N_\mathrm{C}} t_i^\mathrm{b}}{N_\mathrm{C}} = n_i Q_i \tag{3.40}$$

Similar to (3.25) and (3.32):

$$\sum_{i=1}^{N_\mathrm{C}} (1 - n_i) Q_i \geq bI(1-\eta) \left(\sum_{i=1}^{N_\mathrm{C}} t_i^\mathrm{b} \right) \tag{3.41}$$

A summary of the balancing problems (DCB-DC, DCB-AC, D-C2C, A-C2C and C2P) is given in Table 3.1. The table contains all the necessary information required to formulate and solve the linear programming problems, including the decision variables, the equality and inequality constraints and the objective function.

Table 3.1 Balancing problem formulation as a linear programing problem.

	DCB-DC	DCB-AC	D-C2C	A-C2C	C2P
Decision variables	t_i^{b}, n_i $\forall i$ $\in [1, \cdots, N_{\mathrm{C}}]$	t_{ij}, n_i $\forall i, j$ $\in [1, \cdots, N_{\mathrm{C}}]$	$t_i^{\mathrm{c}}, t_i^{\mathrm{d}}, n_i$ $\forall i \in [1, \cdots, N_{\mathrm{C}}]$	$t_i^{\mathrm{cc}}, t_i^{\mathrm{cd}}$ $\forall\, i \in [1, \cdots, N_{\mathrm{C}} - 1]$ $n_j\, \forall\, j \in [1, \cdots, N_{\mathrm{C}} - 1]$	t_i^{b}, n_i $\forall\, i$ $\in [1, \cdots, N_{\mathrm{C}}]$
Objective function	$Q_{\mathrm{u}}^* = \max(\sum_{i=1}^{N} n_i Q_i)$				
Equality constraints	$\frac{\sum_{i=1}^{N_{\mathrm{C}}} n_i Q_i}{N_{\mathrm{a}}} - I t_i^{\mathrm{b}} = n_i Q_i$	$\sum_{i=1}^{N_{\mathrm{C}}} t_{ij} = \sum_{j=1}^{N_{\mathrm{C}}} t_{ij} = \frac{\sum_{i=1}^{N_{\mathrm{C}}} n_i Q_i}{\sum_{j=1}^{N_{\mathrm{C}}} I_j^{\mathrm{p}}}$ $\sum_{j=1}^{N_{\mathrm{C}}} I_j^{\mathrm{p}} t_{ij} = n_i Q_i$	$\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{c}} = \eta \sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{d}}$ $\frac{\sum_{i=1}^{N_{\mathrm{C}}} n_i Q_i}{N_{\mathrm{C}}} - \frac{bI(\eta-1)\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{d}}}{N_{\mathrm{C}}} + bI(t_i^{\mathrm{c}} - t_i^{\mathrm{d}}) = n_i Q_i$	$\frac{\sum_{i=1}^{N_{\mathrm{C}}} n_i Q_i}{N_{\mathrm{C}}} + \frac{bI(1-\eta)\left(\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{cc}} + \sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{cd}}\right)}{N_{\mathrm{C}}} + bI\left(\eta t_i^{\mathrm{cc}} - t_i^{\mathrm{cd}} - t_{i-1}^{\mathrm{cc}} + \eta t_{i-1}^{\mathrm{cd}}\right) = n_i Q_i$	$\frac{\sum_{i=1}^{N_{\mathrm{C}}} n_i Q_i}{N_{\mathrm{C}}} - bI t_i^{\mathrm{b}} + \frac{bI\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{b}}}{N_{\mathrm{C}}} = n_i Q_i$
Inequality constraints	$0 \le n_i \le 1$ $0 \le t_i^{\mathrm{b}} \le T$	$0 \le n_i \le 1$ $t_{ij} \ge 0$	$0 \le n_i \le 1$ $0 \le t_i^{\mathrm{c}} \le T$ $0 \le t_i^{\mathrm{d}} \le T$ $t_i^{\mathrm{c}} + t_i^{\mathrm{d}} \le T$ $\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{c}} \le T$ $\sum_{i=1}^{N_{\mathrm{C}}} (1 - n_i) Q_i \ge bI(1 - \eta)\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{d}}$	$0 \le n_i \le 1$ $0 \le t_i^{\mathrm{cc}} \le T$ $0 \le t_i^{\mathrm{cd}} \le T$ $t_i^{\mathrm{cc}} + t_i^{\mathrm{cd}} \le T$ $\sum_{i=1}^{N_{\mathrm{C}}} (1 - n_i) Q_i \ge bI(1 - \eta)\left(\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{cc}} + \sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{cd}}\right)$	$0 \le n_i \le 1$ $0 \le t_i^{\mathrm{b}} \le T$ $\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{b}} \le T$ (shared storage element) $\sum_{i=1}^{N_{\mathrm{C}}} (1 - n_i) Q_i \ge bI(1 - \eta)\left(\sum_{i=1}^{N_{\mathrm{C}}} t_i^{\mathrm{b}}\right)$

3.4 Comments on the optimization framework

The solution generated by the linear program is not necessarily unique (the uniqueness of solution can be checked using e.g. theorem 2 from [153]). If the solution is not unique then there are multiple decision variable values that satisfy all constraints and result in the same maximum usable capacity. In order to choose between the different solutions, a secondary optimisation problem needs to be solved. For the ERB architectures, the objective of this secondary problem is to find the set of balancing currents (balancing times) that will result in the maximum useable capacity with the lowest overall balancing circuit power losses. Since a constant efficiency is assumed for the balancing circuits, balancing losses can be minimised by minimising the total time that the balancing circuits are used.

The objective function of the secondary problem for the D-C2C in that case is:

$$\min\left(\sum_{i=1}^{N_\mathrm{C}} t_i^\mathrm{c} - \sum_{i=1}^{N_\mathrm{C}} t_i^\mathrm{d}\right) \tag{3.42}$$

For the A-C2C:

$$\min\left(\sum_{i=1}^{N_\mathrm{C}} t_i^\mathrm{cc} + \sum_{i=1}^{N_\mathrm{C}} t_i^\mathrm{cd}\right) \tag{3.43}$$

And for the C2P:

$$\min\left(\sum_{i=1}^{N_\mathrm{C}} t_i^\mathrm{b}\right) \tag{3.44}$$

The equality and inequality constraints of the linear programming problem continue to apply, but now the total extracted capacity is set equal to the maximum useable capacity Q_u^*:

$$\sum_{i=1}^{N_\mathrm{C}} n_i Q_i = Q_\mathrm{u}^* \tag{3.45}$$

For the DCB-DC and DCB-AC, since a fixed number of cells are always operating, total cell losses will be constant (assuming no variation in internal cell resistances between cells). In that case, the optimum set of balancing times that result to the maximum useable capacity may be considered to be the one where the balancing times of each cell are as close as possible to the average balancing time calculated from the linear programming problem, so that losses are equally distributed among cells. This is expressed as a convex quadratic programming problem with the following objective function for the DCB-DC (using (3.9)):

$$\min\left(\sum_{i=1}^{N_\mathrm{C}}\left(\frac{(N_\mathrm{C}-N_\mathrm{a})T^*}{N_\mathrm{C}}-t_i^\mathrm{b}\right)^2\right) \tag{3.46}$$

Similarly for the DCB-AC using (3.13):

$$\min\left(\sum_{j=1}^{N_\mathrm{C}}\sum_{i=1}^{N_\mathrm{C}}\left(\frac{T^*}{N_\mathrm{C}}-t_{ij}\right)^2\right) \tag{3.47}$$

In both cases, the equality and inequality constraints used in the respective linear programming problems should be used, with the inclusion of (3.45).

3.5 Numerical results and discussion

In this section, the balancing performance of a pack comprising twenty cells connected in series is evaluated using the different balancing approaches and the linear programming formulation. Cell capacities are considered to be evenly distributed with a mean capacity of 1 Ah. The range of cell capacities (the difference between maximum and minimum cell capacities) is varied between 0 and 1.6 Ah with the output pack current equal to 1 A in all cases. The useable capacity of the pack is calculated by solving the linear programming problem as formulated in Table 3.1, for different levels of cell redundancy (0-50% redundancy ratio) for the DCB-DC and DCB-AC architectures and for different values of the maximum balancing current (10%-100% of the output pack current) in the D-C2C, A-C2C and C2P architectures. The MATLAB `linprog` function (with default settings) is used in all cases and, as an example, exhibits a computation time of approximately 100 ms for a 20 cell system using a standard desktop PC when solving the DCB-AC problem.

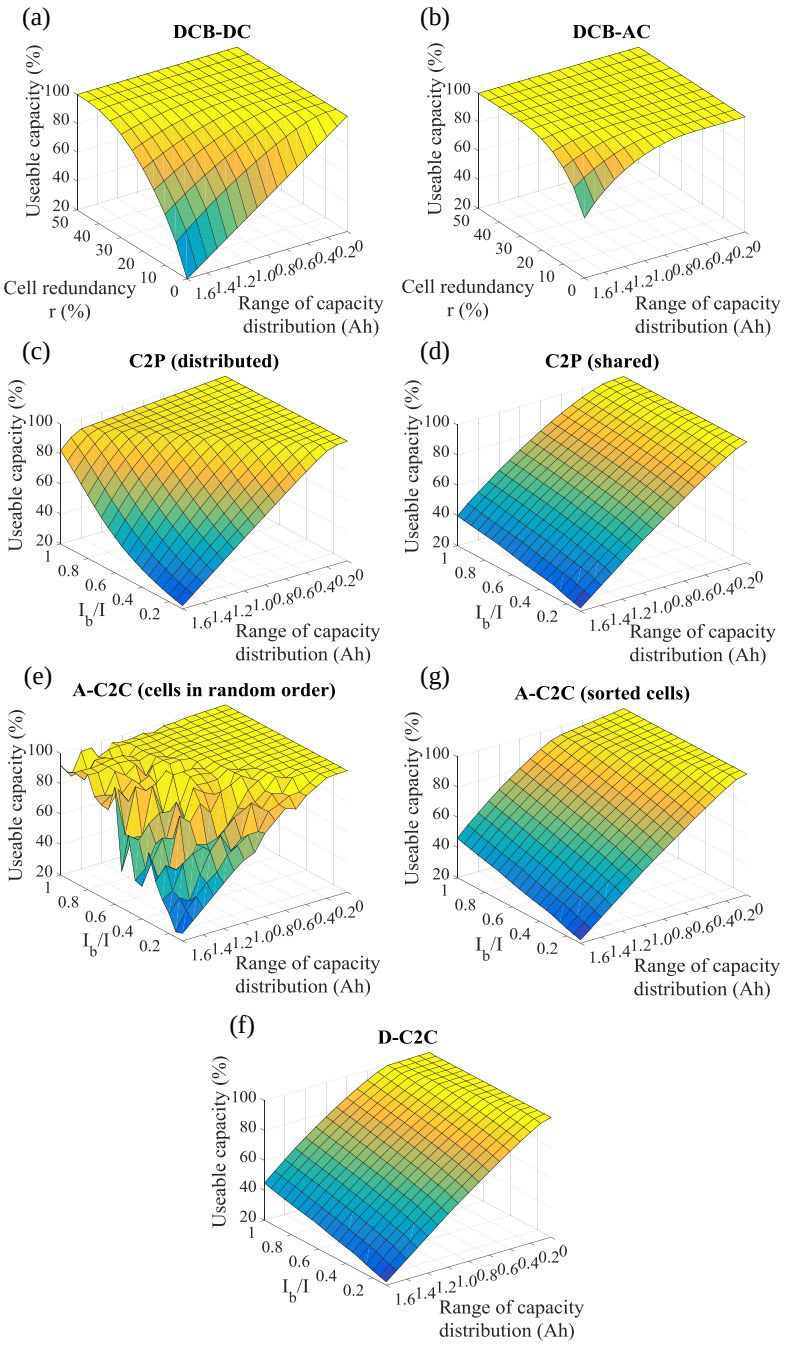


Fig. 3.5 Useable pack capacity of a pack of 20 cells implementing different active balancing approaches: a) DCB-DC and b) DCB-AC for different values of cell redundancy, c) C2P using distributed balancing circuits, d) C2P using a shared storage element, e) A-C2C with cells placed randomly in the pack in a different order for each data point f) A-C2C with cells sorted based on their individual capacities and g) D-C2C for different values of maximum balancing current and $\eta = 0.9$.

From Fig. 3.5 it is obvious that the maximum useable capacity is a function of the cell capacity distribution and the maximum balancing current for the ERB architecture or cell redundancy for the DCB. As the range of cell capacities increase, a higher balancing current or a higher redundancy ratio is required to achieve full capacity utilisation. The DCB-AC system can achieve balancing even with no redundant cells, due to the different currents that cells experience based on their switching position (Fig. 2.2). This is contrast to the DCB-DC case where cell redundancy is required to achieve balancing since without redundancy all cells would be operated all the time and thus experience the same cell currents.

According to Fig. 3.5b, under the worst case capacity distribution (i.e. cell capacities spread in the range 0.2 to 1.8 Ah), the useable capacity in the DCB-AC case is approximately 60% of the total pack capacity, whereas in the other cases, without balancing (i.e. zero redundancy in DCB-DC and zero balancing current in the ERB cases) it is limited by the lowest capacity cell to just 20%. For the same extreme case of capacity variation, full utilisation requires 30% redundancy ratio for the DCB-AC while a DCB-DC system would require 45% redundancy (Fig. 3.5a). The D-C2C and the C2P ERB circuits using a shared storage element and the A-C2C ERB circuit in which the cells in the pack are sorted based on their capacities present a similar (but not identical) balancing performance according to Fig. 3.5. This behaviour is attributed to the limitations in energy redistribution between cells i.e. in the A-C2C balancing can be performed only between neighbouring cells so when the cells with the maximum capacity difference are placed in the opposite ends of the string, transferring energy from the cell with the lowest capacity to the highest capacity cell means that the intermediate balancing circuits are effectively buffering this energy and thus limiting the balancing performance of the intermediate cells in the string. Similarly, when a shared storage element is used in D-C2C, only two cells can be balanced at a time or energy can be extracted from only one cell in the C2P, while the rest are operated normally. When distributed balancing circuits are used to perform C2P a significant enhancement in balancing performance is observed (Fig. 3.5c) since more than two cells can take part in the balancing process simultaneously. In Fig. 3.5e, the cells are placed in the A-C2C pack in a random order of capacity and as a result balancing performance is enhanced since the balancing circuits can now generally be used more effectively to redistribute energy between cells rather

than being forced to buffer energy from the one end of the string to the other. The non-smooth graph in this case is due to different random order being used for each data point.

A 100% usable capacity is observed in some regions of Fig. 3.5. It should be noted here that usable capacity should not be interpreted as energy efficiency but as the ability of the system to extract charge from the cells: A figure of 100% implies that all cells will simultaneously reach 0% SoC at the end of a discharge cycle or 100% SoC at the end of a charge cycle. Power losses occurring in the DCB circuits (due to e.g. MOSFET on-resistance) do not impact this measure but will inevitably reduce the overall energy efficiency of the BESS. In contrast, the efficiencies of the ERB circuits do impact this measure and so are included in the formulation of the linear programming problem.

The calculated balancing times and average cell currents for 20 cells with cell capacities evenly spread in the range 0.5 to 1.5 Ah are presented in Fig. 3.6 for the active balancing schemes ($b = 0.5,\ \eta = 0.9$). In Fig. 3.6a, C2P balancing is performed using a shared storage element, with only three of the cells with the lowest capacities providing energy to the pack ($t^{\mathrm{b}} \neq 0$). In contrast, when distributed circuits are used for C2P balancing, balancing performance is improved since more cells contribute to balancing as can be seen from Fig. 3.6b, where energy is transferred to the pack from eight different cells ($t^{\mathrm{b}} \neq 0$). In the A-C2C (Fig. 3.6c) the cells are sorted based on their capacity in order to observe the restrictions in energy transfer. Here energy from the three cells with the lowest capacity is transferred (resulting in negative balancing times since $t_i^{\mathrm{cc}} + t_{i-1}^{\mathrm{dc}} < -t_i^{\mathrm{dc}} - t_{i-1}^{\mathrm{cc}}$) to the next four cells in the pack (for which the balancing times are positive as $t_i^{\mathrm{cc}} + t_{i-1}^{\mathrm{dc}} > -t_i^{\mathrm{dc}} - t_{i-1}^{\mathrm{cc}}$). In the D-C2C (Fig. 3.6d), the four cells with the lowest capacities have a negative balancing time ($t_i^{\mathrm{b}} = t_i^{\mathrm{c}} - t_i^{\mathrm{d}}$), thus energy is extracted from these cells ($t_i^{\mathrm{c}} < t_i^{\mathrm{d}}$), resulting in lower average cell currents compared to cells with higher capacities which receive an additional charge from their balancing currents ($t_i^{\mathrm{c}} > t_i^{\mathrm{d}}$).

In the case of DCB-DC balancing time is non zero for the cells with the lowest capacities, indicating that these cells are bypassed during operation for different amounts of time according to their respective capacities (Fig. 3.6e). Seven of the cells with the highest capacities are online during the entire time the pack operates (t^{b} is zero) demonstrating an average current equal to the pack output current.

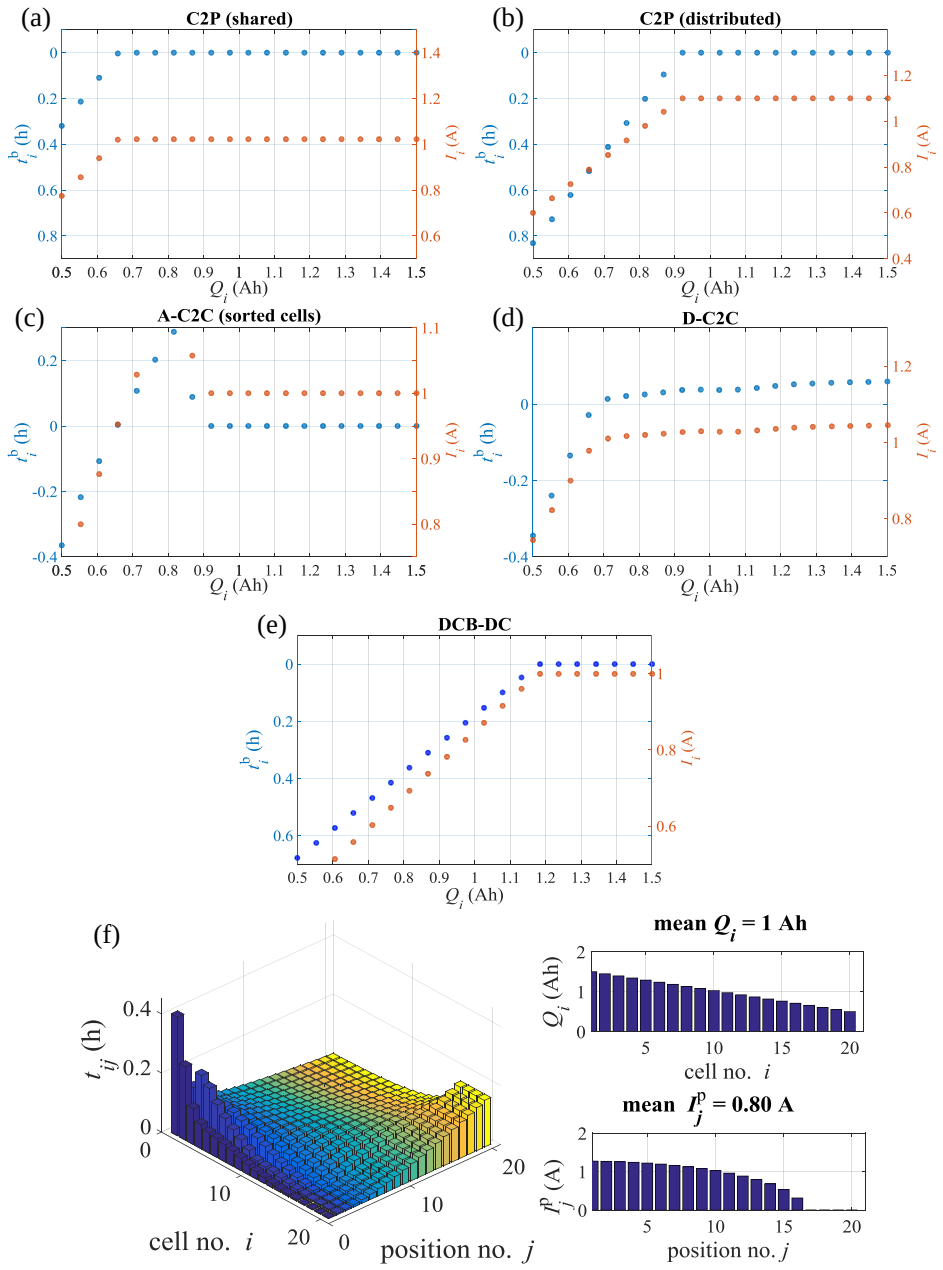


Fig. 3.6 Balancing times and average cell currents: a) of a pack using C2P with a shared storage element b) of a pack using C2P with distributed balancing circuits c) of a pack using A-C2C ($t_i^{\mathrm{b}} = t_i^{\mathrm{cc}} - t_i^{\mathrm{dc}} - t_{i-1}^{\mathrm{cc}} + t_{i-1}^{\mathrm{dc}}$) with cells sorted based on their capacities d) of a pack using D-C2C (note that $I_i = \frac{n_i Q_i}{T}, t_i^{\mathrm{b}} = t_i^{\mathrm{c}} - t_i^{\mathrm{d}}$) e) of a DCB-DC pack (note that $I_i = I - \frac{t_i^{\mathrm{b}} I}{T}$) f) amount of time that each cell spends in the different positions of the DCB-AC pack (cell capacities evenly distributed).

The average time a cell spends at each switching position is presented in Fig. 3.6f for the DCB-AC case. Here, 20 % redundancy is assumed so the last four positions correspond to idle positions with a zero current. As expected, the six cells with the highest capacities spend a significant amount of time occupying positions that result in a higher cell current i.e. positions closer to one. Conversely, the cells with the lowest capacities are bypassed for most of the time or spend it at the higher positions with the least cell current.

3.6 Simulating the balancing performance of ERB architectures

Table 3.2 Details of PLECS models and comparison to linear programming results.

	Single inductor (D-C2C) Fig. 3.2b	Coupled inductor (A-C2C) Fig. 3.3b	Multi-windings forward transformer (C2P-shared) Fig. 3.4c	Multiple transformers (C2P-distributed) Fig. 3.4b
Inductance (mH)	1	1 (each inductor)	4 (magnetising inductance at each primary)	1 (magnetising inductance at each primary)
Maximum balancing current (A)	0.25			
PWM switching frequency (Hz)	1,000			
PWM duty cycle (%)	50			
Mean cell capacity (Ah)	1			
Capacity range (Ah)	0-1.6 (step of 0.1)			
Mean Average Percentage Error of useable capacity $\left(\frac{\sum_{i=1}^{17} 100\frac{Q_{\mathbf{u}}^{*}(i)-Q_{\mathbf{u}}(i)}{Q_{\mathbf{u}}^{*}(i)}\%}{17}\right)$	0.008	0.080	0.023	2.646

In order to check the validity of the assumptions regarding the constraints of energy redistribution in the proposed linear programming models for the ERB architectures (D-C2C, A-C2C and C2P), a representative model of each category is built and simulated using the Piecewise Linear Electrical Circuit Simulation (PLECS) software package [154]. In all the models a four cell battery pack is used and the cells are represented by

constant voltage sources (2 V) in order to enable a direct comparison with the linear programming models. The SoC of each cell i is calculated using:

$$SoC_i(t) = SoC_i^0 + \frac{\int_0^t I_i . \mathrm{d}t}{Q_i} 100 \tag{3.48}$$

where SoC_i^0 is the initial state-of-charge set equal to 0% for all cells at the beginning of each simulation. The simulation is terminated once a cell reaches 100% SoC, when charging the pack with 1 A pack current. The details of the simulation models are given in Table 3.2.

The representative circuit for the D-C2C architecture is the single inductor circuit of [152], presented in Fig. 3.2b. At every switching cycle, the cell with the maximum SoC is connected in parallel with the inductor causing a balancing current to flow out of the cell. The balancing energy is then transferred via the inductor to the cell with the lowest SoC. For the A-C2C, the coupled inductor circuit of Fig. 3.3b is used [152]. In this case, balancing occurs between adjacent cells by switching the higher SoC cell across the coupled inductor, followed by the lower SoC cell. The C2P with a shared storage element is validated using the multi-winding transformer in the forward structure as in Fig. 3.4c. Here the MOSFET of the cell with the highest SoC is switched on, discharging the cell and transferring the energy to the pack through the secondary of the multi-winding transformer. For the validation of the C2P with distributed balancing circuits, the operation of the multiple transformer circuit of Fig. 3.4b is simulated. The individual transformer connected to each cell is used to transfer energy from the cells with a SoC higher than the average cell SoC to the whole pack.

A total number of 17 simulations were performed for each balancing circuit, with the capacity range between cells varying from 0 to 1.6 Ah. The useable capacity achieved in these simulations (Q_{u}) is compared to the maximum useable capacity calculated using the linear programming tool (Q_{u}^*) for the same set of cells and maximum balancing currents and the results are presented in Table 3.2. In all the cases, apart from the C2P-distributed, the error between the output of the linear programming tool and the useable capacity achieved through simulation is less than 0.1%. The difference in the C2P-distributed case is attributed to the inability of the balancing algorithm used in the simulation to fully

utilise the balancing capabilities of the circuit. In order to test this assumption, the balancing times (duty cycles) of each cell as calculated from the solution of the linear programming problem were applied to the simulation circuit (open loop control) and the maximum useable capacity as calculated by solving the linear programming problem was then achieved.

3.7 Experimental validation of DCB-DC and DCB-AC

The balancing performance of DCB-DC and DCB-AC methods was experimentally tested using the twelve-cell CHB presented in Chapter 2. The H-bridge converter connecting each cell enables operating the pack as a DC pack where duty cycle balancing can be performed by bypassing cells, or a DCB-AC pack where each cell is controlled independently in order to produce a stepped output voltage following a sinusoidal reference.

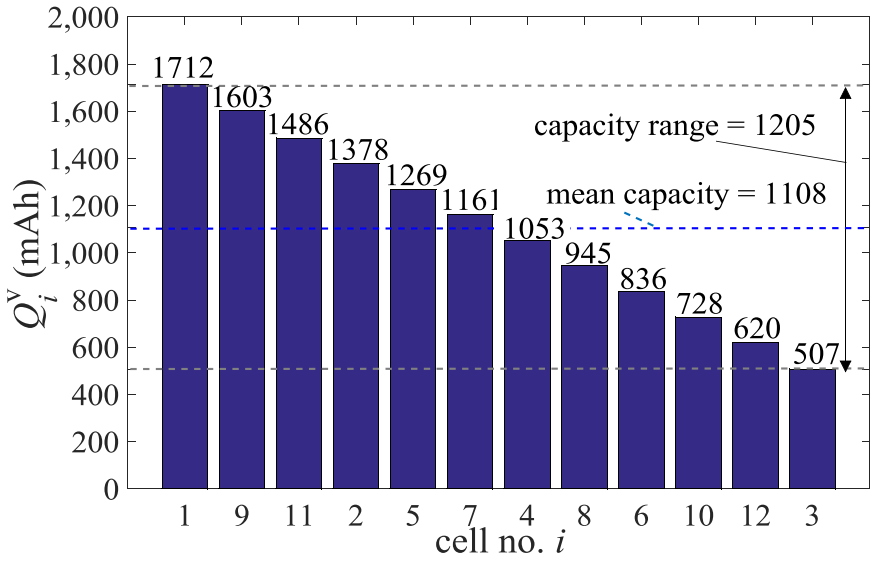


Fig. 3.7 Virtual capacities of cells used in experiments.

The cell used for these tests are LTO cells (SCiB cells from Toshiba) with a nominal capacity of 20 Ah. In order to test the balancing performance for extreme capacity variations which were not available from the real cells, the 'virtual capacities' presented in Fig. 3.7 are used. Due to the extreme differences between the actual cell capacities and the virtual capacities, POCV measurements cannot be used for cell balancing in these

tests. Instead, the cells are sorted here based on their SoC that is calculated by coulomb counting using the Hall effect current sensor connected in series with the pack. A virtual capacity Q_i^{v} is preselected for each cell i and is used in (3.49) during SoC estimation, instead of the actual cell capacity (Q_i). Using a single Hall effect sensor that measures the pack current, the current of each cell can be calculated from (3.50):

$$I_i = gI \tag{3.49}$$

where $g = 1$ if the cell in operated and $g = 0$ if the cell is bypassed.

The SoC of the cells are sequentially updated every 2 seconds, so for each cell in the twelve cell pack the SoC is updated every 24 seconds. The priority list is updated every 2 seconds once a new SoC is received and cell balancing is performed using the NLC as described in Chapter 2. Apart from the use of SoC instead of POCV for cell balancing, another difference compared to the controller presented in Fig. 2.6 is that the current controller is not used here to provide the output voltage reference for the CHB. Since in practice cell voltages vary during operation according to the SoC, in order to ensure the redundancy ratio is kept constant (i.e. a constant number of cells are always bypassed) the following reference voltages are used as input to the NLC:

$$V_{\mathrm{ref}} = \begin{cases} \dfrac{N_{\mathrm{a}}}{N_{\mathrm{C}}} \displaystyle\sum_{i=1}^{N_{\mathrm{C}}} \mathrm{V}_i & \text{for DCB} - \text{DC} \\ \dfrac{N_{\mathrm{a}}}{N_{\mathrm{C}}} \displaystyle\sum_{i=1}^{N_{\mathrm{C}}} \mathrm{V}_i \cos(2\pi f t) & \text{for DCB} - \text{AC} \end{cases} \tag{3.50}$$

The use of (3.50) produces a gradual decrease in the output voltage as the pack discharges, thus ensuring that cell redundancy remains constant during the test.

The balancing performance is evaluated during a discharge cycle. The initial state-of-charge SoC_i^0 is set equal to 100% for all cells at the beginning of each test and operation terminates when a cell reaches zero SoC. For both DCB-DC and DCB-AC configurations, the load connected at the output of the CHB is a 12 Ω resistor.

According to Table 3.3, the balancing performance of each balancing method is evaluated when all cells are operated $(N_{\mathrm{a}}/N_{\mathrm{C}} = 12/12)$ and when only ten out of twelve

cells are active ($N_\mathrm{a}/N_\mathrm{C} = 10/12$). In the DCB-DC case, when ten out of twelve cells are active, the cells placed at positions 1-10 are connected in series and are discharged at the pack current while cells at positions 11 and 12 are bypassed (zero cell current). In the DCB-AC configuration, the current assigned to each position decreases as the position number increases and cells at position 11-12 are always bypassed (i.e. correspond to redundant positions). In both configurations the switching frequency is 100 Hz or 0 since a cell is turned on and off twice every fundamental period, unless it is bypassed. The useable capacity Q_u that is achieved experimentally is calculated using:

$$Q_\mathrm{u} = \sum_{i=1}^{12} \left(SoC_i^0 - SoC_i^\mathrm{T} \right) Q_i^\mathrm{v} \tag{3.51}$$

where SoC_i^T is the SoC of cell i at the end of the test.

The SoC variation during operation is presented in Fig. 3.8. In the DCB-DC case duty cycle balancing cannot be performed without any redundant cells and so pack capacity is limited by the lowest capacity cell, in that case cell 3. The calculated useable capacity is then equal to 45% of the total pack capacity. By reducing the number of active cells to ten, duty cycle balancing can now be implemented. As a result of balancing, 88% of the total capacity can now be used. In order to achieve full capacity utilisation (i.e. zero SoC variation between cells) a higher redundancy ratio would be required, as can be seen from Fig. 3.5a. The good agreement of the experimental and numerical results is also evident by the close matching of the balancing times presented in Fig. 3.9a. The balancing times of the cells for the experimental setup are calculated by measuring the total time that each cell spends at positions 11 and 12 (idle positions), normalised by the total time of operation. As expected, the six cells with the highest capacities spend almost all of their time on, while the rest of the cells spend a considerable amount of time bypassed (cell positions 11 and 12).

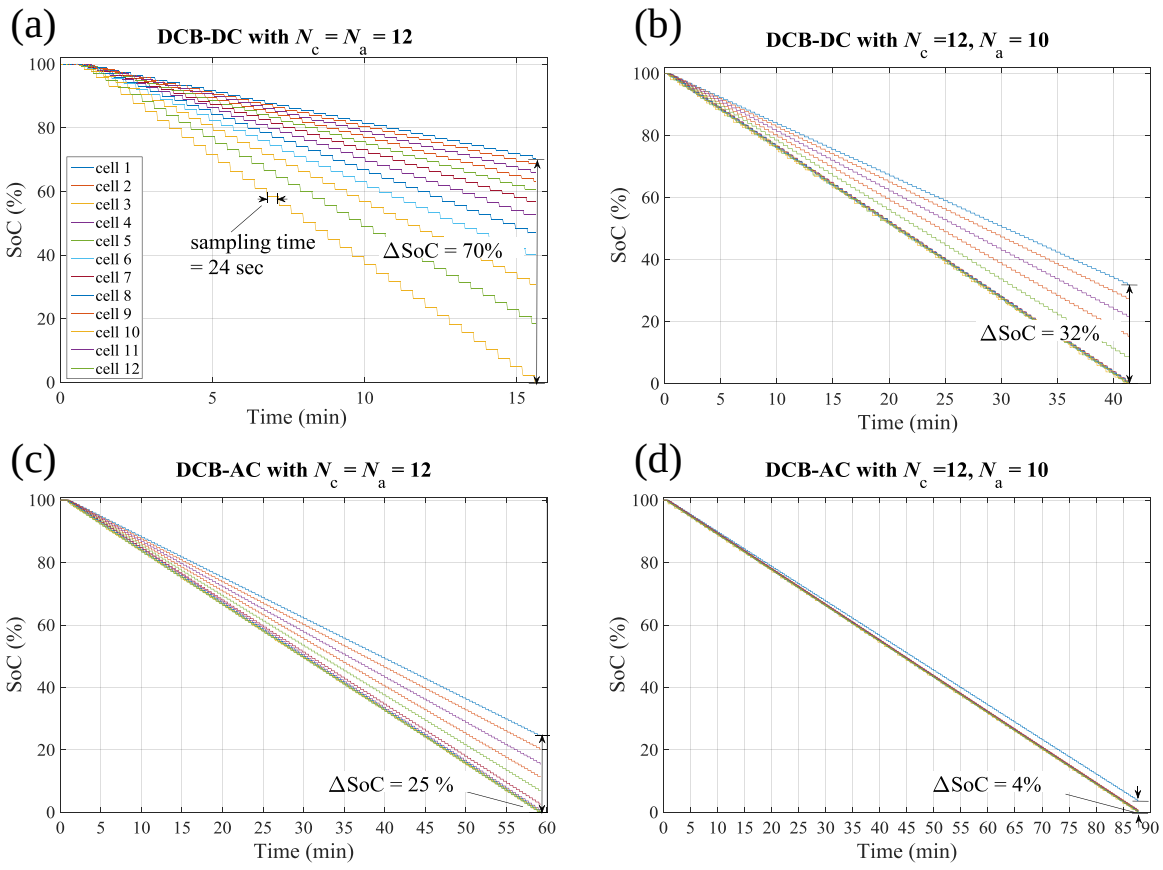


Fig. 3.8 SoC variation of cells during experiments: a) DC pack with no balancing b) DCB-DC pack with $r = 1/6$ c) DCB-AC with no redundant cells d) DCB-AC with $r = 1/6$.

In the DCB-AC case, good capacity utilisation is observed even without the use of redundant cells, due to the ability of the system to operate cells with different cell currents. Based on the numerical results, 90% of the capacity is usable for the cell capacity distribution of Fig. 3.7. The capacity utilisation achieved in the test is also 90% for no cell redundancy and 99% percent when ten out of twelve cells are used, agreeing well with the numerical results. The difference between numerical and experimental results (<1%) is within the experimental error (experimental error is mostly due to the accumulated error during current integration in the SoC estimation process).

Table 3.3 Useable capacity achieved with different duty cycle balancing methods using different cell redundancy.

Balancing Method	DCB-DC		DCB-AC	
N_a/N_C	$Q_u^*/\sum_{i=1}^{N_C} Q_i$ (Numerical)	$Q_u/\sum_{i=1}^{N_C} Q_i$ (Experimental)	$Q_u^*/\sum_{i=1}^{N_C} Q_i$ (Numerical)	$Q_u/\sum_{i=1}^{N_C} Q_i$ (Experimental)
$10/12$	0.8798	0.8759	0.9977	0.9912
$12/12$	0.4575	0.4536	0.8986	0.9046

The average position of each cell in the priority list (i.e. the effective duty cycle of each cell) is presented in Fig. 3.9b and Fig. 3.9c. In the DCB-AC with no redundancy, the five cells with the highest capacities all have an average cell position close to 3 based on the numerical results, whereas according to the experimental results each cell has a different average cell position with the highest capacity cells occupying positions closer to 1, which correspond to a higher average position current (see (3.12)). This mismatch can be explained by considering the small variation between the average current of the neighbouring positions 1-5: for cell 5, the significant difference in average cell position (position 3 according to numerical and 5 according to experimental results) corresponds to less than 5% difference in average current. For packs with a different number of cells and therefore cell positions, the variation between the average current of neighbouring positions will be different but can always be calculated using (3.12). The linear programming tool is setting the duration that each cell spends at each position by considering the average current associated with that position and thereby calculates constant 'position duty cycles'. On the other hand, the sorting algorithm that is used in the experiment places cells in different positions based only on the SoC measured from moment to moment without having any knowledge of the cell capacities i.e. the resulting position duty cycles are not constant and change over the course of the discharge. A slight variation should therefore be expected between the balancing trajectories generated by the linear programming tool and the experiment. However, due to the relatively weak dependence of position and current for position numbers less than 5, the different

solutions found by the linear programming tool versus the experimental balancing algorithm produce very similar total usable capacities.

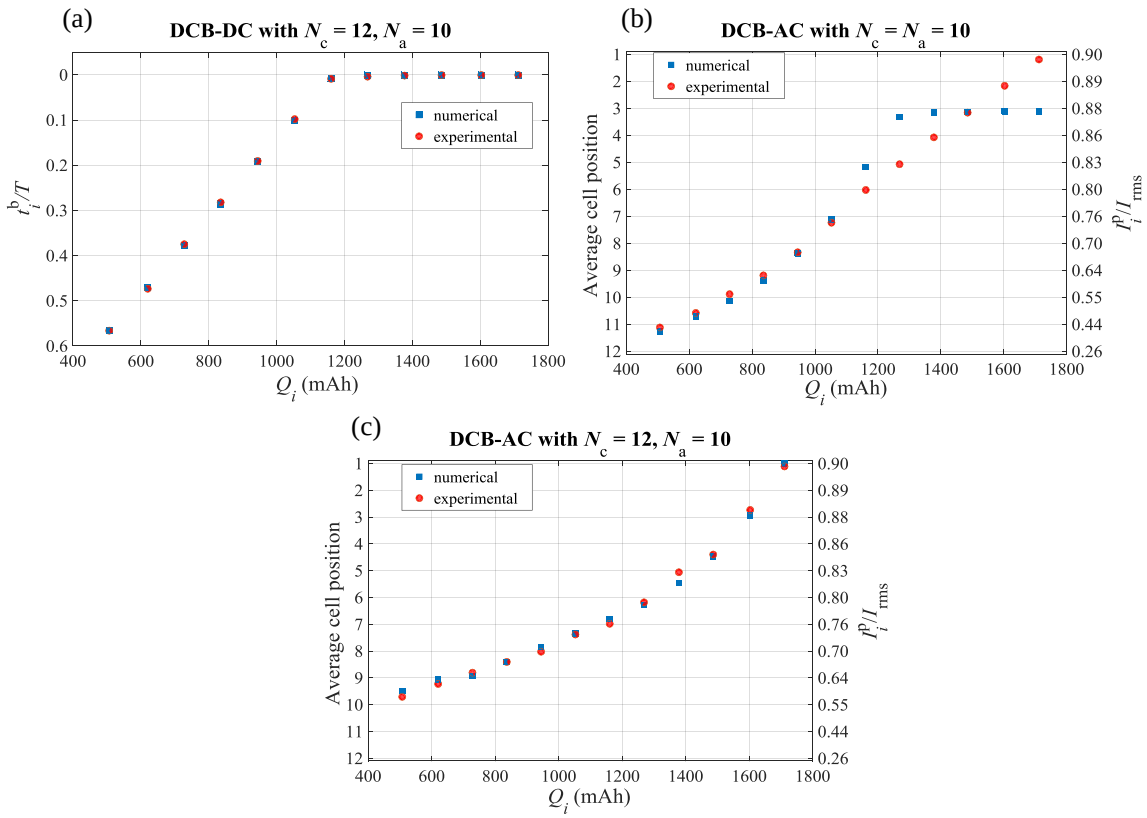


Fig. 3.9 Numerical vs experimental results: a) balancing time in case of DCB-DC with $r = 1/6$ b) the average cell position (and average current, note non-linear axis) versus cell capacity in case of DCB-AC with no redundancy c) the average cell position (and average current, note non-linear axis) versus cell capacity in case of DCB-AC with $r = 1/6$.

3.8 Conclusions

This chapter presents a method for quantitatively evaluating the balancing performance of battery packs implementing either energy redistribution balancing or duty cycle balancing, under the simplifying assumption of constant cell voltage. The balancing problem is formulated as a linear programming problem with the objective of maximising the useable capacity of a pack of cells for a given set of cell capacities. This method can be used to determine the minimum design specifications of each balancing circuit (i.e. balancing current or cell redundancy) in order to achieve an equivalent balancing

performance. Duty cycle balancing enabled by integrating power electronics in the battery pack can provide a significant improvement in balancing performance compared to conventional ERB and thus can accommodate cells with a wide capacity variation in the pack. However, the increased conduction losses due to the high number of MOSFETs in the current path may reduce system efficiency. In the next chapter the overall performance of the battery system will be examined taking into account losses, reliability and cost, for different design options with different levels of power electronics integration in the pack.

Chapter 4 Battery energy storage system design evaluation

This chapter presents a method for evaluating grid-connected BESS designs taking into account capital cost, efficiency and system reliability. Although several examples of similar studies can be found for various converter topologies and applications such as photovoltaic systems [155, 156] and wind turbines [157-160], studies focusing on BESS reliability are limited in the current literature. In most cases a 'parts count method' is followed which is a relatively simple approach where the failure rate of the system is calculated as the sum of the respective failure rates of the system components [161]. An example of this approach is the study of power loss, reliability and cost of a 1 MW/500 kWh BESS presented in [128], in which the failure rate of each electrochemical cell is calculated based on the stress imposed on the internal cell resistance using the MIL-HDBK-217F [162] and the failure rate of the system is calculated as the sum of the local failure rates without considering in-built system redundancy. In [156] a methodology is presented for calculating system reliability using Markov-based models. The advantage of this methodology is that it takes into account the steady state behaviour of the system in order to specify each component's failure rate. The reliability analysis presented in this chapter applies such Markov-based models in the analysis of the BESSs, taking into account the built-in redundancy of the system and varying failure rates due to component failure ('state dependent failure rates'). The complete design evaluation methodology is described in Fig. 4.1. At the first step the respective components of the BESS such as the battery pack, converter interface and balancing circuit are designed based on the required energy and power ratings. The steady-state power losses of the grid interface converter, the battery pack and the balancing circuit are calculated and the temperature rise of each component is estimated. State dependent variables such as component temperature and

voltage stress of the switches are then used to calculate the failure rate of each component. This process is repeated for all the possible operating states identified in the Markov models, taking into account the built-in redundancy of the system as well as performance degradation caused by faults. Finally, a simple economic analysis based on capital cost and efficiency is used to provide a basis for direct comparison between competing system designs.

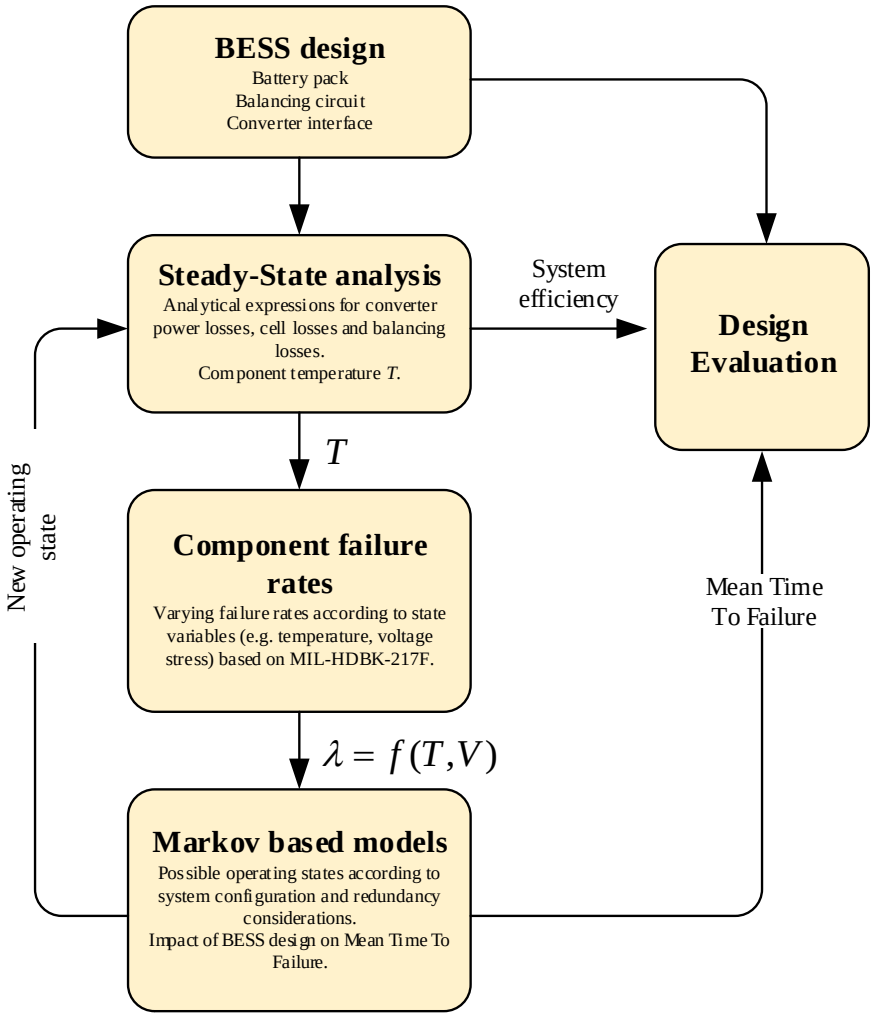


Fig. 4.1 BESS design evaluation methodology.

Three design options for a 1 MW/ 1 MWh BESS connected at 11 kV are compared: a conventional design using parallel power blocks (PB-BESS, Fig. 4.2a), a design using power electronics enhanced ‘intelligent battery packs’ (IBP-BESS, Fig. 4.2b), and a CHB design (CHB-BESS, Fig. 4.2c). This chapter is based on publication [132].

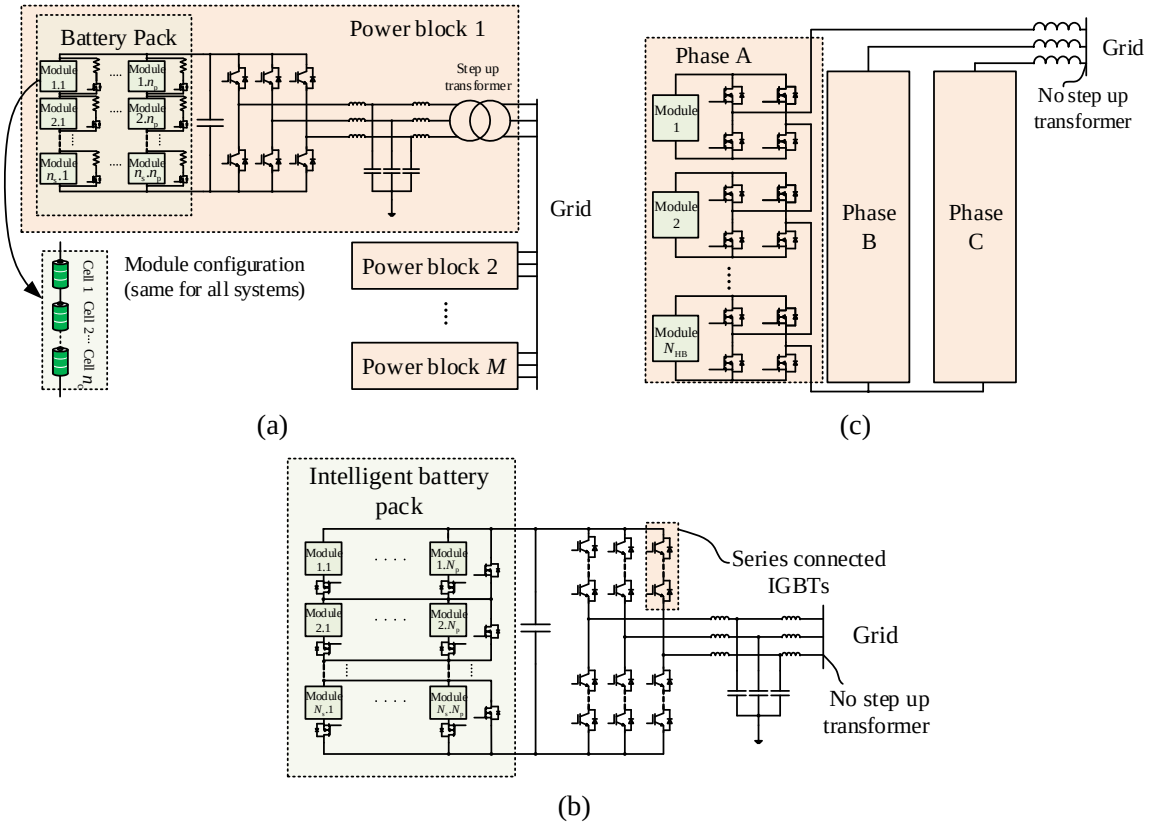


Fig. 4.2 Competing BESS designs: a) BESS using a parallel power block configuration (PB-BESS) b) BESS using an intelligent battery pack with a single-stage two-level converter interface (IBP-BESS) c) BESS using a cascaded H-bridge multilevel converter (CHB-BESS).

4.1 Power loss analysis

Power loss calculations for all three BESS designs presented in Fig. 4.2 take into account converter losses and cell losses due to internal cell resistance as well as losses due to cell balancing.

4.1.1 Converter losses

The power losses of a switching device are calculated as the sum of conduction (P_{CN}) and switching losses (P_{SW}) [163]. For the IGBT and diode, conduction losses are modelled as a forward voltage plus slope resistance [164] while for the MOSFET only a resistance is used [165]. The switching losses are calculated as the sum of turn-on and

turn-off losses for IGBTs and MOSFETs. For the diodes, only losses at diode turn-on are considered significant. A simple model of switching losses is used where a linear relationship between losses and device current at the instant of switching is assumed, with the constants of proportionality estimated according to the manufacturer's datasheet [164]. The total power converter losses are then given in (4.1) - (4.3) for the different BESS configurations [164]. For the centralised power converters of the PB-BESS and IBP-BESS:

$$P_{\mathrm{CN}}^{\mathrm{PB/IBP}} = 6\left(\sqrt{2}I_{\mathrm{rms}}\left(\frac{1}{2\pi}+\frac{M\cos\theta}{8}\right)V_{\mathrm{Q}} + 2I_{\mathrm{rms}}^{2}\left(\frac{1}{8}+\frac{M\cos\theta}{3\pi}\right)R_{\mathrm{Q}} + \sqrt{2}I_{\mathrm{rms}}\left(\frac{1}{2\pi}-\frac{M\cos\theta}{8}\right)V_{\mathrm{D}} + 2I_{\mathrm{rms}}^{2}\left(\frac{1}{8}-\frac{M\cos\theta}{3\pi}\right)R_{\mathrm{D}}\right)N \tag{4.1}$$

$$P_{\mathrm{SW}}^{\mathrm{PB/IBP}} = \frac{6\sqrt{2}}{\pi}\left(k_{\mathrm{on}}^{\mathrm{Q}} + k_{\mathrm{off}}^{\mathrm{Q}} + k_{\mathrm{on}}^{\mathrm{D}}\right)f_{\mathrm{SW}}I_{\mathrm{rms}}N \tag{4.2}$$

where N is equal to N_{PB} (PB) or N_{SS} (IBP).

For the CHB-BESS the calculation of converter power loss is substantially different due to the distributed nature of the converter and the use of many low voltage MOSFETs instead of a small number of higher voltage IGBTs. Considering the cascaded arrangement of the H-bridges, during the operation of the CHB-BESS two MOSFETs in each module are always conducting the load current even when the module is bypassed. The total conduction loss for the three-phase CHB-BESS is:

$$P_{\mathrm{CN}}^{\mathrm{CHB}} = 6N_{\mathrm{HB}}I_{\mathrm{rms}}^{2}R_{\mathrm{F}} \tag{4.3}$$

The switching strategy of the CHB-BESS is based on the NLC described in Chapter 2, resulting in a very low effective switching frequency of 100 Hz. In this case, the switching losses are insignificant compared to the conduction losses of the MOSFET and so are neglected.

In the PB, transformer losses are assumed to be 1% which is commensurate with a 1 MVA class transformer operated at a high load factor [166]. Control system, cooling, LCL filter and DC link capacitor losses in the PB and IBP as well as the losses in the

CHB output inductors are assumed to be small compared to other losses and so are neglected [167].

4.1.2 Battery pack losses

Cell losses are considered to be the result of an internal cell resistance only. In this study it is assumed that the internal resistances of all cells are similar, cell capacities vary across a small range (5% in the following case study) and the system is operated at a low C-rate. As a result the difference in cell currents across parallel connected cells will be small and cell power losses will be similar throughout the system (this assumption would not be valid at high C-rates associated with EV applications and a more detailed model would be required [48, 53, 168]). All cells are therefore modelled as having an identical resistance R_{C} representing an average cell power loss. In order to calculate total cell power losses for the conventional battery pack of a power block, converter power losses are neglected so that DC and AC power are related by

$$n_{\mathrm{P}} n_{\mathrm{S}} V_{\mathrm{M}} I_{\mathrm{C}} = \sqrt{3} V_{\mathrm{rms}} I_{\mathrm{rms}} \cos\theta \tag{4.4}$$

And

$$r_{\mathrm{v}} n_{\mathrm{S}} V_{\mathrm{M}} = \sqrt{2} V_{\mathrm{rms}} \tag{4.5}$$

The voltage redundancy ratio $r_{\mathrm{v}} = \frac{V_{\mathrm{pk}}}{n_{\mathrm{S}} V_{\mathrm{M}}} \left(= \frac{V_{\mathrm{pk}}}{N_{\mathrm{S}} V_{\mathrm{M}}} = \frac{V_{\mathrm{pk}}}{N_{\mathrm{HB}} V_{\mathrm{M}}} \right) \leq 1$ is defined here as the number of cells required to provide the peak AC output voltage divided by the total number of cells in a series string. Later in this chapter, the term $r_{\mathrm{e}} = \frac{E_{\mathrm{n}}}{N_{\mathrm{C}} V_{\mathrm{C}} Q_{\mathrm{C}}} \leq 1$ is defined as the energy redundancy ratio, equal to the number of cells required to provide the rated energy E_{n}, divided by the total number of cells N_{C}. In all three systems $r_{\mathrm{e}} \geq r_{\mathrm{v}}$ in order to ensure that the failure criterion for each system is loss of rated power and energy delivery capability and not loss of voltage availability. In practice, third harmonic injection would likely be used (provided the ability to individually control the neutral-point voltage of the converter) to increase the effective output voltage of the converter

(i.e. lower the effective V_{pk}), however it is not included here in order to simplify the analysis.

By solving (4.5) for V_{M} and substituting into (4.4), the total cell losses for the PB-BESS can be found:

$$P_{\mathrm{BP}}^{\mathrm{PB}} = n_{\mathrm{C}} n_{\mathrm{S}} n_{\mathrm{P}} N_{\mathrm{PB}} P_{\mathrm{C}} = \frac{3}{2n_{\mathrm{P}}} n_{\mathrm{C}} n_{\mathrm{S}} N_{\mathrm{PB}}\, r_{\mathrm{v}}^2 \cos^2\theta\, I_{\mathrm{rms}}^2 R_{\mathrm{C}} \tag{4.6}$$

Similarly, for the IBP-BESS the total cell losses are:

$$P_{\mathrm{BP}}^{\mathrm{IBP}} = \frac{3}{2N_{\mathrm{P}}} n_{\mathrm{C}} N_{\mathrm{S}}\, r_{\mathrm{v}}^2 \cos^2\theta\, I_{\mathrm{rms}}^2 R_{\mathrm{C}} \tag{4.7}$$

In case of the CHB-BESS, the current is different for each converter module due to the operation of the NLC. Using (2.5) the RMS value of the cell current at each position i can be calculated as:

$$\begin{aligned} I_{\mathrm{rms}(i)} &= \sqrt{\frac{1}{\pi}\int_{a_i}^{\pi-a_i} \left(\sqrt{2} I_{\mathrm{rms}} \sin(\varphi-\theta)\right)^2 d(\varphi)} \\ &= \sqrt{\frac{2I_{\mathrm{rms}}^2}{\pi}\left(\frac{\pi-2a_i}{2} - \frac{1}{2}\sin(2a_i)\cos(2\theta)\right)} \end{aligned} \tag{4.8}$$

Finally the cell power losses for the CHB-BESS can be found using:

$$\begin{aligned} P_{\mathrm{BP}}^{\mathrm{CHB}} &= 3N_{\mathrm{HB}} n_{\mathrm{C}} P_{\mathrm{C}} = 3n_{\mathrm{C}} R_{\mathrm{C}} \sum_{1}^{r_v N_{\mathrm{HB}}} I_{\mathrm{rms}(i)}^2 \\ &\cong \frac{6}{\pi} n_{\mathrm{C}} N_{\mathrm{S}} r_{\mathrm{v}} \left(\frac{\cos(2\theta)}{3} + 1\right) I_{\mathrm{RMS}}^2 R_{\mathrm{C}} \end{aligned} \tag{4.9}$$

4.1.3 Over-provision of cells and cell balancing

Due to the lack of active balancing in the PB-BESS, the useable capacity of a series string of cells is limited to that of the lowest capacity cell and as a result additional cells must be included in the PB-BESS to guarantee that the rated energy capacity can be provided as the system ages. The number of additional cells (over-provision) depends on the worst case variation between the nominal and minimum capacity of the cells:

$$N_{\mathrm{o}} = \frac{N_{\mathrm{C}}(Q_{\mathrm{M}} - Q_{\mathrm{min}})}{Q_{\mathrm{min}}} \tag{4.10}$$

This effect also occurs within modules in the IBP and CHB-BESS designs but because full active balancing can be performed between modules, the impact on the capacity of the series connection of modules is negligible, i.e. effectively all capacity is accessible from all cells despite variation in cell capacity.

Although a passive balancing circuit is considered for the PB-BESS, balancing in that case is only performed periodically (once every few cycles) to equalize the module voltages at the end of a charging cycle: once a module reaches the cut-off voltage it is clamped at this voltage by external circuitry and energy dissipated resistively while the rest of the modules continue to be charged, normally at a lower C-rate [83]. As a result, passive balancing losses in the PB-BESS will depend on the operating regime and the requirements of the particular cell technology, making them difficult to model in a general sense. However, if balancing only occurs infrequently, overall losses will be relatively small and so they are neglected in this study.

In the case of the IBP-BESS and CHB-BESS, balancing at module level is achieved by controlling each module's effective duty cycle by appropriately switching the MOSFETs and exploiting module redundancy (i.e. these systems perform DCB as described in Chapter 3). For the IBP, the losses in the pack MOSFETs can effectively be assigned to the balancing operation and are therefore referred to as *balancing losses* (i.e. the pack MOSFETs are 'used' to perform balancing only and do not perform a direct power conversion function as in the CHB). When a module is in-circuit the MOSFET in series with the module is turned on, whereas when a module is bypassed the MOSFET in

parallel is turned on, i.e. there is always one MOSFET conducting in each module. The balancing losses for the IBP-BESS are therefore

$$P_{\mathrm{bal}}^{\mathrm{IBP}} = \frac{3}{2N_{\mathrm{P}}} N_{\mathrm{S}} r_{\mathrm{v}}^2 \cos^2\theta \, I_{\mathrm{rms}}^2 R_{\mathrm{F}} \tag{4.11}$$

For the CHB-BESS balancing is 'free' since conduction losses in the MOSFETs of each H-bridge have already been accounted for in the converter loss calculation and as a result balancing losses are considered to be equal to zero.

4.2 Reliability analysis

In all the cases considered in this study, the system is assumed to have failed when the rated power can no longer be provided, i.e. when a predefined number of cells have failed or become unusable because their associated power converter has failed. Throughout the operation of the system all cells and converter components are active so during steady state they all share the same failure rates (i.e. redundant cells are not kept idle and then 'switched in' after failure). In order to maintain a constant power output even after a component failure, the steady state loading of the remaining components is increased and this change is reflected in an increased failure rate. For example, after losing one module in the any of the three systems, the remaining modules must be operated at a higher C-rate to maintain the same output power, resulting in greater internal heating of the cells and an increased cell failure rate.

4.2.1 Failure rates of the individual components

The failure rates used in this study are based primarily on MIL-HDBK-217F [162]. However, if other component failure models are used [169], the general approach presented in this paper remains valid. The Markov-based modelling approach requires a constant failure rate for all system components. According to [170] the base failure rate of the Li-ion cell can be modelled as

$$\lambda_{C0} = \frac{1}{\mathrm{MTTF_C}} \tag{4.12}$$

where $\mathrm{MTTF_C}$ is the average life of the cell. For a typical lithium ion cell with a life equal to 10,000 cycles, the base cell failure rate is $\lambda_{C0} = 2$ failures/10^6 Hours which is in the range of typical MOSFET failure rates [171]. The effect of cell temperature on the failure rate of the cell is modelled using (4.13) where a temperature rise of ΔT above ambient (T_A) causes the failure rate of the cell to increase by a factor of c_T [172].

$$\lambda_C = \lambda_{C0} c_T^{\frac{T_C - T_A}{\Delta T}} \tag{4.13}$$

where $T_C = T_A + P_C R_{th_C}$, $T_A = 25$ ℃ is the ambient temperature, $R_{th_C} = 10$ ℃/W is the thermal resistance of the cell, $\Delta T = 10$ ℃ and $c_T = 1.5$. The internal cell resistance R_C used in the calculation of cell power losses (P_C) is 1 mΩ leading to a temperature rise of up to 12 ℃ in this study under worst-case conditions. In reality, due to the aging mechanisms of lithium-ion cells, the failure rate of the cell is likely to be an increasing function of time [173]. This time dependency is not capture in the used model but will be addressed in section 4.3.2.1.

The failure rates for the diodes, MOSFETs and capacitors are derived using the MIL-HDBK-217F. A change in the steady state of the system results to a varying failure rate due to the change in the temperature and voltage stress π factors.

The MOSFET failure rate is given by:

$$\lambda_F = \lambda_{F0} \pi_T \pi_A \pi_Q \pi_E \tag{4.14}$$

where $\lambda_{F0} = 0.012$ is the base failure rate of the MOSFET, $\pi_T = \exp\left(-1925\left(1/(T_j + 273) - 1/298\right)\right)$ is the temperature factor where T_j is the junction temperature of the MOSFET and can be calculated similar to T_C, using the MOSFET power losses and thermal resistance. The thermal resistances of the MOSFET and IGBT junction-to-ambient are taken to be twice the junction-to-case resistances given in the manufactures data sheet. π_A is the application factor that depends on the power

rating of the MOSFET (< 2 W for linear amplification and > 2 W for power MOSFETs). For a MOSFET with a power rating greater than 250 W, $\pi_{\mathrm{A}} = 10$. π_{Q} is the quality factor that depends on the level of quality control during the manufacturing process (since poor equipment design, production and testing facilities can degrade part quality) and in this case is 8 (for plastic) and $\pi_{\mathrm{E}} = 1$ is the environmental factor for stationary applications (non-mobile, temperature and humidity controlled environments readily accessible to maintenance).

For the diodes:

$$\lambda_{\mathrm{D}} = \lambda_{\mathrm{D0}}\pi_{\mathrm{T}}\pi_{\mathrm{V}}\pi_{\mathrm{CC}}\pi_{\mathrm{Q}}\pi_{\mathrm{E}} \tag{4.15}$$

where the base failure rate is $\lambda_{\mathrm{D0}} = 0.003$ and the temperature factor is given by $\pi_{\mathrm{T}} = \exp\left(-3091\left(1/(T_{\mathrm{j}} + 273) - 1/298\right)\right)$. $\pi_{\mathrm{V}} = V_{\mathrm{St}}^{2.43}$ is the voltage stress factor where V_{St} is the ratio of the voltage applied to the diode over the rated voltage of the component. The voltage stress factor is used to model diode failure due to a high reverse voltage that can cause avalanche. $\pi_{\mathrm{CC}} = 1$ is the contact construction factor while the environmental and quality π factors have the same values as in (4.14).

For the capacitors:

$$\lambda_{\mathrm{A}} = \lambda_{\mathrm{A0}}\pi_{\mathrm{T}}\pi_{\mathrm{C}}\pi_{\mathrm{V}}\pi_{\mathrm{Q}}\pi_{\mathrm{E}} \tag{4.16}$$

where $\lambda_{\mathrm{Q0}} = 0.012$ is the base failure rate of the capacitor, $\pi_{\mathrm{T}} = \exp\left(-0.35/8.617 \times 10^{-5}\left(1/(T_{\mathrm{j}} + 273) - 1/298\right)\right)$ is the temperature coefficient, $\pi_{\mathrm{C}} = C^{0.23}$ is the capacitance (C) factor, $\pi_{\mathrm{V}} = 1 + (V_{\mathrm{St}}/0.6)^5$ is the voltage stress ratio factor, $\pi_{\mathrm{Q}} = 10$ is the quality factor for a commercial capacitor and $\pi_{\mathrm{E}} = 1$ is the environmental factor.

Since MIL-HDBK-217F was last updated in 1991 it does not include information about the calculation of IGBT failure rates. According to [174] the failure rate for the IGBTs can be calculated using the base failure rate of MOSFETs and the π factors of bipolar transistors:

$$\lambda_{\mathrm{Q}} = \lambda_{\mathrm{Q0}} \pi_{\mathrm{T}} \pi_{\mathrm{A}} \pi_{\mathrm{R}} \pi_{\mathrm{V}} \pi_{\mathrm{Q}} \pi_{\mathrm{E}} \tag{4.17}$$

where $\lambda_{\mathrm{Q0}} = \lambda_{\mathrm{F0}} = 0.012$, $\pi_{\mathrm{T}} = \exp\left(-2114\left(1/(T_{\mathrm{j}} + 273) - 1/298\right)\right)$, $\pi_{\mathrm{A}} = 0.7$ is the application factor, $\pi_{\mathrm{R}} = P_{\mathrm{Q}}^{0.37}$ is the power rating (P_{Q}) factor, $\pi_{\mathrm{V}} = 0.045 \exp(3.1 V_{\mathrm{St}})$ is the voltage stress ratio factor. π_{Q} and π_{E} are equal to the respective π factors of the MOSFET.

The failure rate for a liquid filled transformer (λ_{X}) is 0.468 failures/10^6 hours (no temperature dependent failure rates were implemented for this component since the transformers operate at a constant output power except for the worst case where one power block has failed and the output power of the rest is increased by ~10%) [175].

4.2.2 Power block system reliability

In conventional battery packs that such as the ones in the PB-BESS, failure of a single module is addressed by isolating the whole series string of modules containing the failed module [112]. The PB-BESS will continue to operate normally as long as $N_{\mathrm{PB}} n_{\mathrm{P}} r_{\mathrm{e}}$ parallel strings are available to provide the rated power. The Markov state transition diagram for the PB-BESS is presented in Fig. 4.3. P_i represents the probability of the system being in a steady state where i parallel strings have failed. The failure rate describing a transition from state i to $(i+1)$ is $(N_{\mathrm{PB}} n_{\mathrm{P}} - i)\lambda_{\mathrm{R}[i]}$. A failure of a power converter will cause the system to lose n_{P} strings and move to state $P_{i+n_{\mathrm{P}}}$ with a transition rate $(N_{\mathrm{PB}} - w)\lambda_{\mathrm{V}[i]}$ where w is the number of failed PBs at the state P_i. It should be noted here that all the cells in the PB-BESS are assumed to be operated under equal C-rates in order to maintain access to the capacity of each cell. As a result, the converters that correspond to PBs with all their cells operational are stressed more than those with failed strings. However, in the analysis presented here it is assumed that the load on all PB converters increases equally after the failure of a string of cells. This is done to significantly reduce the number of states and transitions required in the Markov model.

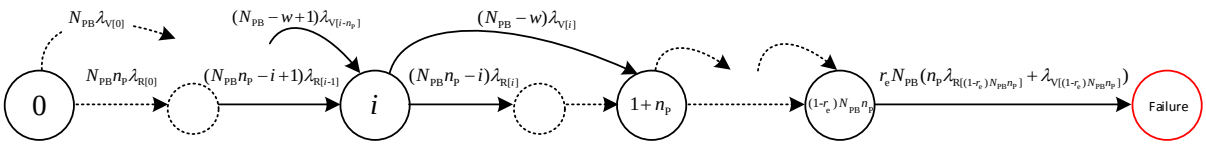


Fig. 4.3 Markov state transition diagram of the PB-BESS.

The distribution of the Markov process (Fig. 4.3) at time t is expressed by the probability vector time $\boldsymbol{P}(t)$:

$$\boldsymbol{P}(t) = [P_0(t), \dots, P_i(t), \dots, P_{N_{\mathrm{PB}}n_{\mathrm{P}}(1-r_{\mathrm{e}})}(t)] \tag{4.18}$$

The time evolution of the transition probabilities $P_i(t)$ is governed by the Kolmogorov forward equations [156]. For the transition diagram presented in Fig. 4.3, the following differential equations are derived by inspection (at time $t = 0$ the system is assumed to be in state 0, *i*.e. $P_0(0) = 1$ and $P_i(0) = 0$ for $i > 0$):

$$\frac{\mathrm{d}P_0}{\mathrm{d}t} = -(N_{\mathrm{PB}}\lambda_{\mathrm{V}[0]} + N_{\mathrm{PB}}n_{\mathrm{P}}\lambda_{\mathrm{R}[0]})P_0 \tag{4.19}$$

$$\begin{aligned}\frac{\mathrm{d}P_i}{\mathrm{d}t} = {} & (N_{\mathrm{PB}} - w + 1)\lambda_{\mathrm{V}[i-n_{\mathrm{P}}]}P_{i-n_{\mathrm{P}}} + (N_{\mathrm{PB}}n_{\mathrm{P}} - i + 1)\lambda_{\mathrm{R}[i-1]}P_{i-1} \\ & - ((N_{\mathrm{PB}}n_{\mathrm{P}} - i)\lambda_{\mathrm{R}[i]} + (N_{\mathrm{PB}} - w)\lambda_{\mathrm{V}[i]})P_i \\ & i = 1..N_{\mathrm{PB}}n_{\mathrm{P}}(1 - r_{\mathrm{e}})\end{aligned} \tag{4.20}$$

Since the DC link capacitor, transformer and converter semiconductors are a series connected system in terms of reliability [176], the failure rate of the power converter is given by

$$\lambda_{\mathrm{V}} = \lambda_{\mathrm{A}} + \lambda_{\mathrm{X}} + 6(\lambda_{\mathrm{Q}} + \lambda_{\mathrm{D}}) \tag{4.21}$$

The reliability of the system is quantified using the mean time to failure (MTTF) of the system:

$$\text{MTTF} = \int_{t=0}^{\infty} R(t).\,\mathrm{d}t \tag{4.22}$$

where $R(t)$ is the reliability function of the system, given by:

$$R(t) = \sum_{i=1}^{N_{\text{PB}} n_{\text{P}} (1-r_{\text{e}})} P_i(t) \tag{4.23}$$

Taking the Laplace transformation of (4.23):

$$R^*(s) = \sum_{i=1}^{N_{\text{PB}} n_{\text{P}} (1-r_{\text{e}})} {P_i}^*(s) \tag{4.24}$$

The Laplace transform of the reliability function $R^*(s)$ is:

$$R^*(s) = \int_{t=0}^{\infty} R(t) e^{-st}.\,\mathrm{d}t \tag{4.25}$$

From (4.22) and (4.25), the MTFF can be expressed as follows:

$$\text{MTTF} = \int_{t=0}^{\infty} R(t).\,\mathrm{d}t = \int_{t=0}^{\infty} R(t) e^{-0t}.\,\mathrm{d}t = R^*(0) \tag{4.26}$$

Using (4.24) and (4.26), the MTTF of the PB can be calculated using the Laplace transformation of P_i, P_i^* :

$$\text{MTTF}_{\text{PB}} = \sum_{i=0}^{N_{\text{PB}} n_{\text{P}} (1-r_{\text{e}})} P_i^*(0) \tag{4.27}$$

4.2.3 Intelligent battery pack system reliability

In order to assess the reliability the IBP-BESS it is assumed that the pack can operate as long as $r_e N_S$ parallel connected module blocks (with a parallel bypass MOSFET) are operational. The Markov state transition diagram for the IBP is presented in Fig. 4.4. P_{ij} represents the probability of the pack being in a state where i parallel module blocks have failed and are bypassed by their parallel MOSFETs, while j parallel MOSFETs from the remaining module blocks have failed closed circuit. A transition from a state ij to $(i+1)j$ is realized with a failure rate $(N_S - i - j)\lambda_{P[ij]}$ and to $i(j+1)$ with a failure rate $(N_S - j - i)\lambda_{F[ij]}$. It should be noted here that semiconductor switches (MOSFETs, IGBTs and diodes) in all three systems are assumed to reliably fail closed circuit. This assumption serves to simplify the analysis and generally improves reliability compared to open or undefined impedance failures because current paths are not interrupted.

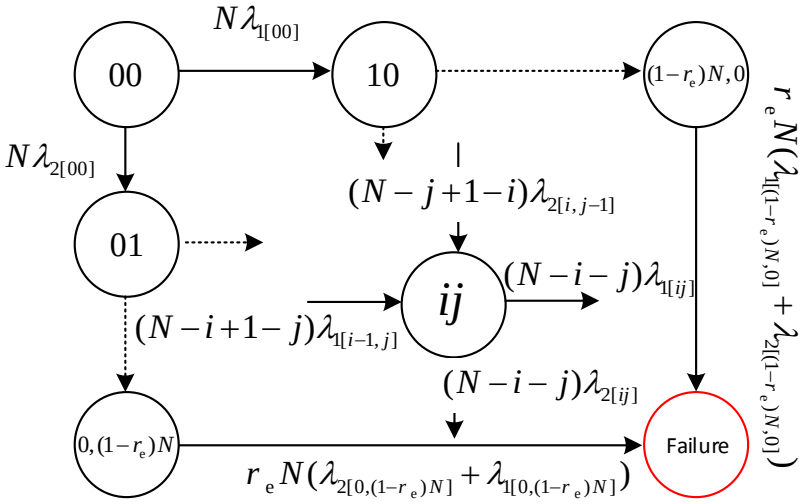


Fig. 4.4 Markov state transition diagram for the IBP-BESS and CHB-BESS. For the IBP-BESS $N = N_S, \lambda_1 = \lambda_P, \lambda_2 = \lambda_F$. For the CHB-BESS $N = N_{HB}, \lambda_1 = \lambda_M, \lambda_2 = \lambda_H$.

In the IBP-BESS the failure of the one module's series and parallel MOSFET or in the CHB-BESS the failure of two MOSFETS in the same leg will result in the short-circuiting of the module. It is assumed that reliable fusing is included in the module to prevent catastrophic failure under these conditions. In a real life application the failure

modes of these devices and the fusing action should be verified in order to ensure that the system will behave as expected.

The operating behavior of the IBP is described by (4.28) - (4.31).

$$\frac{\mathrm{d}P_{00}}{\mathrm{d}t} = -(N_{\mathrm{S}}\lambda_{\mathrm{P}[00]} + N_{\mathrm{S}}\lambda_{\mathrm{F}[00]})P_{00} \tag{4.28}$$

$$\begin{aligned}\frac{\mathrm{d}P_{ij}}{\mathrm{d}t} = {} & (N_{\mathrm{S}}-i+1-j)\lambda_{\mathrm{P}[i-1,j]}P_{(i-1)j} + (N_{\mathrm{S}}-j+1-i)\lambda_{\mathrm{F}[i,j-1]}P_{i(j-1)} \\ & -(N_{\mathrm{S}}-i-j)\left(\lambda_{\mathrm{P}[ij]}+\lambda_{\mathrm{F}[ij]}\right)P_{ij}\end{aligned} \tag{4.29}$$

$$\mathrm{MTTF}_{\mathrm{BP}} = \sum_{i=0}^{N_{\mathrm{S}}(1-r_{\mathrm{e}})} \sum_{j=0}^{N_{\mathrm{S}}(1-r_{\mathrm{e}})-i} P_{ij}^{*}(0) \tag{4.30}$$

Assuming a constant failure rate for the battery pack, it can be calculated by:

$$\lambda_{\mathrm{BP}} = \frac{1}{\mathrm{MTTF}_{\mathrm{BP}}} \tag{4.31}$$

Due to the increased DC link voltage of the IBP-BESS, a series connection of switches will typically be needed for each converter arm (this design assumes a two-level MV converter as opposed to a more complex multilevel converter). The Markov state diagram for a converter arm as presented in Fig. 4.5 is described by (4.32) - (4.34). Here i represents the number of IGBTs that have failed and the transition from state i to $(i+1)$ is described by a failure rate $(N_{\mathrm{SS}}-i)\lambda_{\mathrm{W}[i]}$.

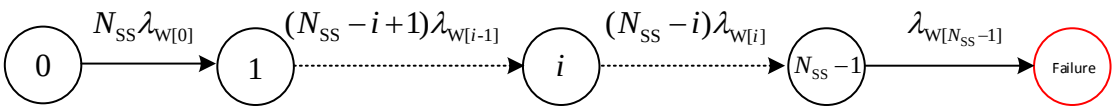


Fig. 4.5 Markov state transition diagram of a phase arm of the converter comprising of N_{ss} IGBT switches in series.

$$\frac{\mathrm{d}P_0}{\mathrm{d}t} = -N_{\mathrm{SS}}\lambda_{\mathrm{W}[0]}P_0 \tag{4.32}$$

$$\frac{\mathrm{d}P_i}{\mathrm{d}t} = (N_{\mathrm{SS}} - i + 1)\lambda_{\mathrm{W}[i-1]}P_{i-1} - (N_{\mathrm{SS}} - i)\lambda_{\mathrm{W}[i]}P_i \tag{4.33}$$

$$\mathrm{MTTF}_{\mathrm{arm}} = \sum_{i=0}^{N_{\mathrm{SS}}-1} P_i^*(0) \tag{4.34}$$

Since the six converter arms are connected in series in terms of reliability, the failure rate of the converter in the IBP-BESS can be calculated by (4.35), assuming a constant arm failure rate.

$$\lambda_{\mathrm{V}} = 6\lambda_{\mathrm{arm}} = \frac{6}{\mathrm{MTTF}_{\mathrm{arm}}} \tag{4.35}$$

The MTTF of the IBP-BESS is then calculated using:

$$\mathrm{MTTF}_{\mathrm{IBP}} = \frac{1}{(\lambda_{\mathrm{A}} + \lambda_{\mathrm{BP}} + \lambda_{\mathrm{V}})} \tag{4.36}$$

4.2.4 Cascaded H-Bridge system reliability

For the CHB-BESS the reliability of each phase is calculated based on (4.37) - (4.40), according to the Markov state diagram presented in Fig. 4.4. At state ij, i represents the number of converter modules that are not operational due to a failure in the battery module and are bypassed using the H-bridge MOSFETs and j denotes the number of modules that are bypassed due to a fault in the H-bridge. The failure rates associated with a transition from ij to $(i+1)j$ or $i(j+1)$ are $(N_{\mathrm{HB}} - i - j)\lambda_{\mathrm{M}[ij]}$ and $(N_{\mathrm{HB}} - i - j)4\lambda_{\mathrm{H}[ij]}$ respectively.

$$\frac{\mathrm{d}P_{00}}{\mathrm{d}t} = -N_{\mathrm{HB}}(\lambda_{\mathrm{M}[00]} + \lambda_{\mathrm{H}[00]})P_{00} \tag{4.37}$$

$$\begin{aligned}\frac{\mathrm{d}P_{ij}}{\mathrm{d}t} = {} & (N_{\mathrm{HB}} - i + 1 - j)\lambda_{\mathrm{M}[i-1,j]}P_{(i-1),j} \\ & + (N_{\mathrm{HB}} - i - j + 1)\lambda_{\mathrm{H}[i,j-1]}P_{i,(j-1)} \\ & - (N_{\mathrm{HB}} - i - j)\left(\lambda_{\mathrm{M}[ij]} + \lambda_{\mathrm{H}[ij]}\right)P_{ij}\end{aligned} \tag{4.38}$$

$$\mathrm{MTTF}_{\Theta} = \sum_{i=0}^{N_{\mathrm{HB}}(1-r_{\mathrm{e}})} \sum_{j=0}^{N_{\mathrm{HB}}(1-r_{\mathrm{e}})-i} P_{ij}^{*}(0) = \frac{1}{\lambda_{\Theta}} \tag{4.39}$$

Taking into account that the three phases are connected in series in terms of reliability, the MTTF of the three phase CHB-BESS can be calculated by

$$\mathrm{MTTF}_{\mathrm{CHB}} = \frac{1}{3\lambda_{\Theta}} \tag{4.40}$$

4.3 Case study

In this section the designs of three 1 MW/1 MWh BESSs based on the system architectures presented in Fig. 4.2 are compared using the preceding analysis at unity power factor. The details of each system are presented in Table 4.1. The PB-BESS uses 5% additional cells to compensate for the loss in accessible capacity caused by the lack of active balancing (31,500 15Ah LTO cells compared to 30,000 for the IBP and CHB). The energy redundancy ratio is the same (r_{e}=0.9) for all three BESS (3,150 redundant cells for the PB and 3,000 for the IBP and CHB). A passive balancing circuit including a shunt resistor and MOSFET switch is used for each module of the PB-BESS. These components are not included in the IBP and CHB-BESSs because these systems are able to perform active module balancing. Due to the higher DC link voltage of the IBP-BESS compared to the PB-BESS, each converter arm includes 18 IGBT switches in series.

Table 4.1 Detailed characteristics of the three BESSs.

	PB-BESS	IBP-BESS	CHB-BESS
Number of power blocks	10	1	1
Module configuration (cells in series)	5	5	5
Battery pack (cells)	315 in series, 10 in parallel (each PB)	15,000 in series, 2 in parallel (in IBP)	10,000 in series (per phase)
Transformers	10 (transformer turns ratio 1:28, 99% efficiency)	(none)	(none)
Balancing circuit	6,300 MOSFETs (IR IRL6283MTR) 6,300 resistors	9,000 MOSFETs (IR IRL6283MTR)	24,000 MOSFETs (IR IRL6283MTR)
Converter	60 IGBTS (6 per PB) (Infineon FF600R12ME4)	108 IGBTs (18 IGBTs per arm) (Infineon FF200R33KF2C)	
Total apparent power of switches (MVA)	43.20 (converter) + 25.20 (balancing) = 68.40	71.28 (converter) + 36.00 (balancing) = 107.28	96.00 (all H-bridge circuits)

4.3.1 Power loss analysis

A breakdown of the system losses for the three BESS designs is presented in Fig. 4.6. The PB-BESS and IBP-BESS have almost the same losses in the battery pack because similar DC currents flow in all cells. The battery losses in the CHB are increased due to the pulsed nature of the cell current (as presented in Fig. 2.2b). Since in all three cases the battery losses are calculated as the losses in the internal resistance of the cells (i.e. are proportional to the square of the RMS value of cell current), higher losses are expected in the CHB due to the higher RMS-to-average current ratio compared to PB and IBP (where the RMS value of the current is equal to the average value). As discussed previously, power losses due to passive balancing in the PB-BESS are not considered in this analysis but it should be noted that these losses in practice are expected to lead to a small increase in average losses. Balancing losses are zero in the CHB-BESS since they are included in the power converter losses as part of normal operation. Although there is a significantly

higher number of switches in the current path in the CHB-BESS, there is no centralized converter and the power electronics losses are actually reduced compared to the IBP-BESS due to the very low on-state resistance of the MOSFETs and the low switching frequency operation (using the NLC modulation technique). Switching losses are proportionally larger for the IBP due to the series connection of high-voltage IGBTs used to form the two-level MV converter. In order to reduce switching losses in that case, a multilevel converter such as the FC or NPC may be employed.

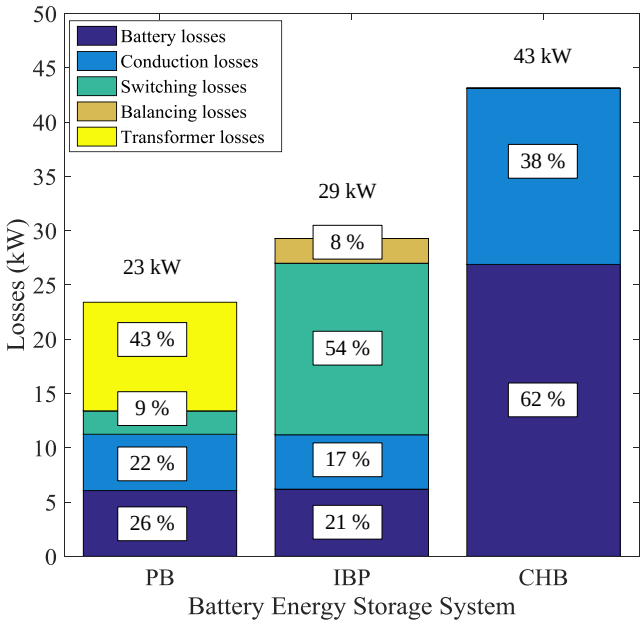


Fig. 4.6 Loss breakdown for the three BESSs.

4.3.2 Reliability analysis

Table 4.2 Failure rates and MTTF of the three BESSs.

Failure rates (failures/10^6h)	**PB-BESS**	**IBP-BESS**	**CHB-BESS**
Battery	681 (string of 315 cells)	235 (IBP of 30,000 cells)	Battery integrated in converter
Converter	32 (each PB converter)	57 (single large converter)	
System	6087	292	528
MTTF of the system (h)	164	3,424	1,895

The failure rates for the different components in each BESS and the total system MTTF are presented in Table 4.2.

The failure rate of the PB-BESS is highly dependent on the failure rate of the battery string since according to Table 4.2 string failure is 20 times more likely than power converter failure. This is because a single cell failure will result in the failure of the whole string and the subsequent loss of a tenth of the PB's available capacity.

In the IBP-BESS, due to the high battery pack voltage, each arm of the converter comprises 18 IGBTs connected in series resulting in an increased converter failure rate compared to the PB-BESS. However, the overall system MTTF of the IBP-BESS is significantly greater than the PB-BESS due to the much higher reliability of the battery pack. The substantial decrease in the failure rate of the battery pack, although the IBP-BESS includes 95 times as many cells as a single battery string in the PB-BESS (30,000 compared to 315), can be attributed to the additional MOSFETs in the pack, which enable the IBP-BESS to effectively address single module faults by bypassing only two parallel modules rather than a whole string of modules.

For the CHB-BESS, the failure rates for the battery pack and the converter cannot be calculated separately since each battery module is integrated with an H-bridge converter. Compared to the PB-BESS, the CHB has an increased MTTF due to the ability to isolate single modules in case of failure. However, its reliability is decreased compared to the IBP-BESS due to the increased number of MOSFETs used in the battery pack (four rather than two per module).

4.3.2.1 Notes on the cell failure model

In order to explore the effect of the time dependency of cell failure rates to the overall system MTTF, the reliability study is repeated for different base cell failure rates in Fig. 4.7. According to Fig. 4.7, for a very low cell failure rate ($\lambda_{\mathrm{C}0i}/\lambda_{\mathrm{C}0} \leq 10^{-3}$, where $\lambda_{\mathrm{C}0i}$ is the varying base cell failure rate) the MTTF of the PB-BESS is much improved compared to the base case (where $\lambda_{\mathrm{C}0i}/\lambda_{\mathrm{C}0} = 1$) despite the lack of controllability over series connected modules, since the failure rate is in this case dictated mainly by the power electronics. This lower failure rate represents very reliable cells, for example very high quality cells at the beginning of their life.

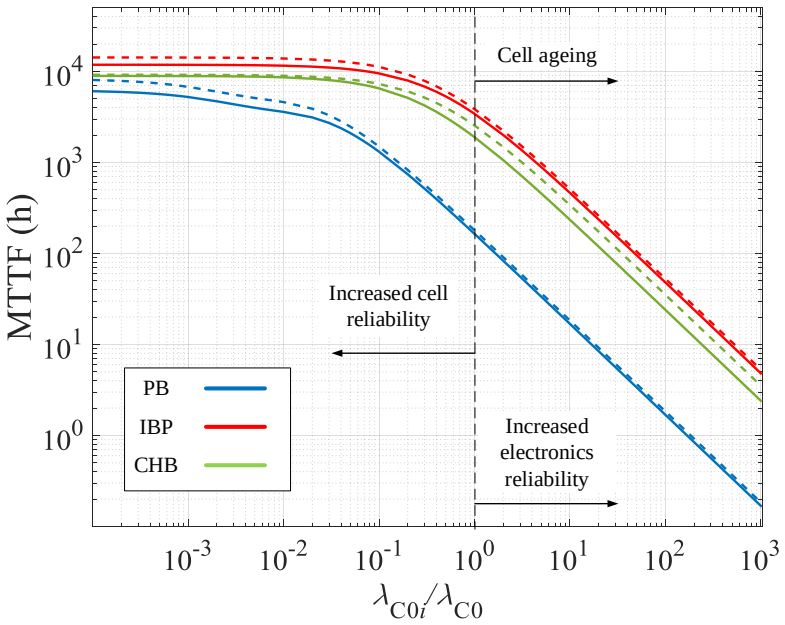


Fig. 4.7 MTTF for different base cell failure rates λ_{C0i} compared to the base failure rate λ_{C0} used in this study. Dotted lines represent results with no temperature dependence of failure rates. Note that $\lambda_F/\lambda_{C0} = 0.33$ and $\lambda_Q/\lambda_{C0} = 0.8$, i.e. in the base case individual switches are assumed to be slightly more reliable than individual cells.

As the failure rate of the cells increases, corresponding to cells of lower quality and/or aged cells, the IBP-BESS and CHB-BESS demonstrate much higher reliability than the PB. This is due to the granular control of these modular systems that enables bypassing only the module where the failed cell is located (or just two parallel modules in the IBP), without interrupting operation of the system. In contrast, a single cell failure in the PB-BESS will cause a whole string to be taken offline and thus a significant fraction of the available capacity in the power block to be inaccessible (10% of each PB in this case study). The CHB-BESS is slightly less reliable than the IBP-BESS because of the increased cell temperature (caused by the pulsed cell current and the subsequent increase in cell losses in the CHB-BESS). The higher temperature leads to an increased cell failure rate according to (4.13) and therefore a decrease in the MTTF of the system. This effect begins to dominate when cells become significantly less reliable than the MOSFETs.

In order to evaluate the effect of temperature on failure rate, the MTTF for each system is calculated assuming all components operate at ambient temperature (dotted lines in Fig. 4.7). This condition corresponds to very low C-rates or highly effective

cooling in the BESS. As expected, reliability is improved in all cases, demonstrating that thermal management of the cells and power electronics is an important aspect of BESS design. The effect of temperature on MTTF is more obvious in the PB-BESS and IBP-BESS than for the CHB-BESS when cell failure rate is low and the MTTF of the system is mostly dependent on converter reliability. This is because the IGBT temperature rise is much higher in the centralized converter of the PB-BESS and IBP-BESS compare to the MOSFET temperature rise in the distributed converter of the CHB-BESS. However, when the failure rate of the cells becomes dominant, a larger increase in the MTTF of the CHB-BESS becomes visible due to the higher cell losses in that system in contrast to the PB-BESS and IBP-BESS where cells experience a smooth DC current.

4.3.3 Cost analysis

The total capital cost of the three BESSs is presented in Table 4.3. In order to compare reliability and capital cost the 'reliability figure of merit' (RFoM) index is used [159].

$$\mathrm{RFoM} = \frac{\eta \mathrm{MTTF}}{\mathrm{CC}} \tag{4.41}$$

where CC is the capital cost of each system in £/MWh. The cost per unit energy is divided by the round-trip efficiency of the system (η) in order to obtain the 'cost per useful energy' [177].

The cost of lithium ion cells is currently approximately £200/kWh according to [178]. The cost of the rest of the components is based on supplier data [179]. Table 4.3 shows the IBP-BESS and the CHB-BESS have very similar and much improved RFoM compared to the PB-BESS: they both offer lower capital costs but substantially improved reliability which outweighs a slight loss in efficiency. Although the CHB-BESS utilizes three times as many individual switches when compared to the IBP, the capital cost is significantly lower due to the use of many low voltage MOSFETs with a lower cost-per-kVA than the few high voltage IGBTs used in the IBP-BESS.

Table 4.3 Cost breakdown and RFoM of the three BESSs.

Capital Cost (£)	**PB-BESS**	**IBP-BESS**	**CHB-BESS**
Battery pack	210,000	200,000	200,000
Balancing circuit	7,533	5,381	-
Converter	3,462	21,347	14,350
Transformer	24,360	-	-
Total capital cost per MWh (CC)	245,355	226,728	214,350
System efficiency (η)	0.977	0.971	0.957
Cost per unit energy (£/MWh)	251,131	233,499	223,981
MTTF of the system (h)	164	3,424	1,895
RFoM (normalized to the PB-BESS)	1	22	13

4.4 Conclusions

This chapter has presented a methodology for the evaluation of competing BESS designs. The power losses of the system are calculated analytically, taking into account converter losses, battery losses and balancing circuit losses. The subsequent temperature rise of the various system components is used to calculate component failure rates that vary according to the operating state of the system. The different operating states are captured using a Markov-based modelling approach, where the MTTF of the system is calculated considering the configuration of the system. This methodology was used to compare three BESS designs with a different level of integration of power electronics in the battery pack. The results of this analysis indicate that a greatly improved RFoM can be achieved when using power electronics enhanced system designs (such as the IBP and CHB) compared to the conventional PB-BESS, mainly due to enhanced reliability of these systems as a result of the ability to manage individual cell failure online without interrupting the operation of the system. The main drawback of the CHB-BESS is the significantly higher battery losses compared to the other two designs, due to the pulsed nature of the cell current caused by the operation of the NLC. However, in this study battery losses were calculated assuming a constant internal cell resistance. According to [121] a pulsed current can actually reduce losses by minimizing the AC impedance of the li-ion cells and this would further improve the efficiency of the CHB-BESS.

Chapter 5 Control algorithms for large scale battery energy storage systems based on the CHB converter

Although the CHB power circuit is inherently scalable to large numbers of cells and output high voltages, the control of a grid scale system comprising tens of thousands of cells would be very challenging if a flat BMS architecture is followed (Fig. 5.1a). This is mainly because in order to produce a stepped voltage waveform using NLC and to maintain stability of the grid current controller, switching signals must be updated at a relatively high rate and with low latency. According to the operation of the NLC as described in Chapter 2, each H-bridge must be updated four times in each cycle of the mains waveform: i.e. in each positive and negative half-cycle the H-bridge must be turned on and off, and these events must occur with high resolution in time. For a 50 Hz grid frequency this equates to an average 200 Hz update rate along with better than 100 μs time resolution to ensure a high quality wave-shape and provide adequately low loop delay for the centralised current controller to track the grid voltage. These requirements make the flat BMS architecture increasingly impractical to implement as cell-count increases. For example, a flat BMS for a large grid-scale battery pack with 50,000 individually controllable cells (generating 200,000 switching events per grid cycle), assuming 16 bits for the packet address and 4 bits for the H-bridge switching signals results in a data rate at the central controller of 200 Mbits/s for a grid frequency of 50 Hz. This implies a very large communication and computational load for the master controller.

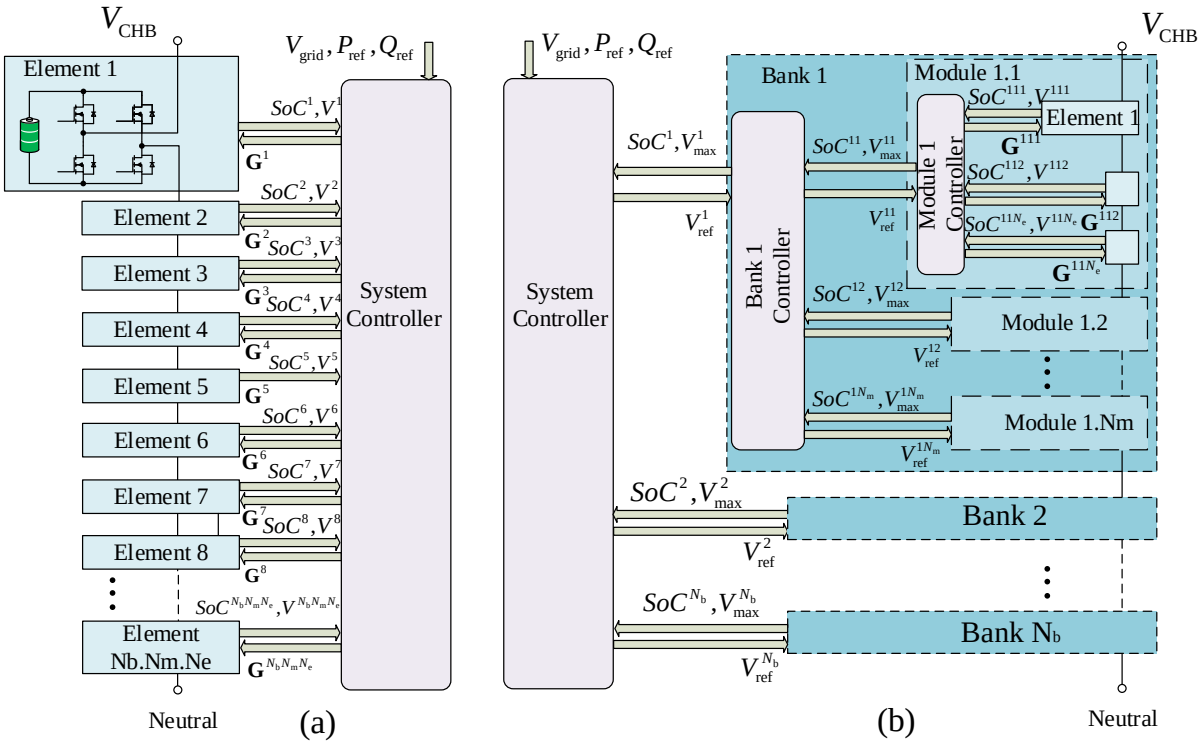


Fig. 5.1 Different BMS design approaches for a CHB-BESS comprising $N_b N_m N_e$ elements: a) a flat BMS structure where a central controller gathers information from all elements and produces switching signals for each H-bridge b) the proposed hierarchical system structure where the BMS is organised in three conceptual control layers: N_b banks, each bank includes N_m modules and each module contains N_e elements.

A modular BMS following a hierarchical control structure such as that presented in [127] goes some way to addressing this problem. The modular BMS control is enabled by organising the elements of the CHB into three conceptual control layers, labelled *banks*, *modules* and *elements*. Each *object* in a layer (i.e. the entities that make up a layer, such as the banks in the bank layer) is equipped with a controller that acts as a master for a subset of 'slave' objects that are located in the next lower hierarchical level. Each master controller receives the required sensing signals such as voltages and SoC from the respective slave controllers. Using this information, a balancing algorithm produces the appropriate voltage references for the slave controllers to follow. This hierarchical scheme enables global cell balancing (i.e. cell balancing between all cells in the system) by balancing the objects of the intermediate layers using the distributed layer controllers.

As a result of limiting the total amount of information that is transferred between layers, the requirement for a powerful central controller is avoided and the system becomes inherently scalable. An example of a hierarchical structure is presented in Fig. 5.1.b. The system controller, including the grid current controller and the higher level balancing control, acts as a master for the bank controllers and each bank controller is a master to a group of modules. Each module controller is responsible for monitoring a group of elements and providing the switching signal for the respective H-bridges. It should be noted that the top-level controller is still required to provide the overall voltage reference for the entire system (which is produced by the grid current controller) but this is communicated only to the next layer down in the hierarchy from where it is propagated down to the next layer and so on. This propagation must still occur with high time-resolution in order to produce a high quality output waveform, but crucially it is not necessary for the central controller to address every element in the system individually. As an example, when a system of N elements is organised in l similarly sized hierarchy layers (i.e. each layer comprises the same number of objects) the total number of slaves that each master must address is reduced from N to $\sqrt[l]{N}$ when this hierarchical control scheme is implemented.

In [127], balancing of an intermediate layer is realised by distributing the voltage reference for each object of the layer in proportion to that object's SoC deviation from the average layer SoC. A disadvantage of this method is that once balancing is achieved, the voltage reference is equally distributed to the layers resulting in the simultaneous switching of multiple H-bridges. As a result, the output voltage generated by this control scheme includes steps that are a multiple of the element voltage and so produces a poorer voltage quality compared with what the CHB circuit is inherently capable of producing. Moreover, the balancing controller requires an additional level of control (called the 'peak sharing algorithm' [127]) to ensure that the output voltage can be achieved even when certain modules are not able to meet the demand due to cell failure.

In this chapter the hierarchical approach of [127] is followed to develop an alternative hierarchical balancing algorithm that addresses some of the weaknesses of prior work. The proposed algorithm can prioritize balancing between hierarchical layers according to the maximum SoC variation between the objects of each layer and can ensure that the output voltage reference can always be met so long as there are an adequate number of

cells available in the overall system, even for varying module voltages caused by element failures. The ability of this balancing scheme to overcome variations in element capacities and initial SoC is examined by simulating the operation of a CHB-BESS comprising 1,000 elements. Finally an experimental validation of the hierarchical balancing is presented using a CHB-BESS comprising 144 LTO cells. A summary of the advantages and disadvantages of the proposed hierarchical balancing algorithm compared to existing work that can be found in literature is presented in Table 1. This chapter in based on publication [133].

Table 5.1 Comparison of proposed hierarchical balancing algorithm with existing work in literature.

	Proposed balancing algorithm	**Ooi et al. [127]**	**Young et al. [129]**	**Maharjan et al. [123, 124]**
Advantages	• Scalable balancing algorithm. • Output voltage limitations are integrated in algorithm. • 100 Hz maximum switching frequency. • Experimentally validated using single-phase 289-level CHB.	• Scalable balancing algorithm. • Output voltage limitations are considered. • 100 Hz maximum switching frequency. • Number of values sent from slaves to master: $2N_S$ (SoCs and voltages for N_S objects).	• Harmonics elimination. • 100 Hz maximum switching frequency. • Experimental validation for a single-phase seven-level CHB.	• Balancing achieved by active power control of each converter element. • Experimental validation for a three-phase seven-level CHB.
Disadvantages	• Number of values sent from slaves to master: $2N_S + 1$ (SoCs and voltages for N_S objects and maximum ΔSoC, i.e. one more than **[127]**). • Low inter-layer latency required for accurate following of the reference waveform.	• Additional peak sharing algorithm necessary. • Not all available voltage steps are utilised when cells balanced. • Low inter-layer latency required for accurate following of the reference waveform.	• High computational complexity of SHE (obtain switching angles using Newton-Raphson). • Not scalable.	• Higher switching frequency (800 Hz PS-PWM). • Output voltage capability of each element is not addressed. • Centralised controller needs to provide a voltage reference for each element.

5.1 Description of the hierarchical balancing algorithm

In this section the hierarchical balancing algorithm is explained using a single-phase CHB-BESS with three layers of hierarchy: N_{b} banks (bank layer), where each bank contains N_{m} modules (module layer) and each module contains N_{e} elements (element layer). Although the discussion here is limited to three layers, the control approach can be simply extended to include more layers and can be implemented in a three-phase system where balancing between phases is achieved using zero sequence voltage injection [123].

The hierarchical balancing control as implemented in the controllers of the different system layers is presented in Fig. 5.2a (a detailed description of the algorithm is given in the Appendix). Similar to the flat BMS system control presented in Chapter 2, the balancing control consists of two parallel processes operating at different rates: a slow process occurring every 2 sec and a fast process occurring at 50 kHz (these frequencies are somewhat arbitrary and will depend on the particular implementation, these values are those used in the experimental work). Due to the different operating frequencies of the two processes, during implementation the appropriate synchronisation signals are used to ensure that the passing of the relevant control variables (i.e. priority lists and V_{S}) from the slow to the fast processes takes place during the initialisation stages according to Fig. 5.2b and c.

During the slow process, each individual controller receives the average SoC of each object from a group of objects at the next layer down in hierarchy and the maximum SoC variation (ΔSoC) between the objects of the lower hierarchical levels, from the respective slave controllers. Based on this information a priority list $\boldsymbol{L^S}$ is produced where the lower layer slave objects are sorted according to their average SoC. The average SoC of the current layer and the maximum SoC variation are then calculated and sent to the controller of the next layer up in the hierarchy.

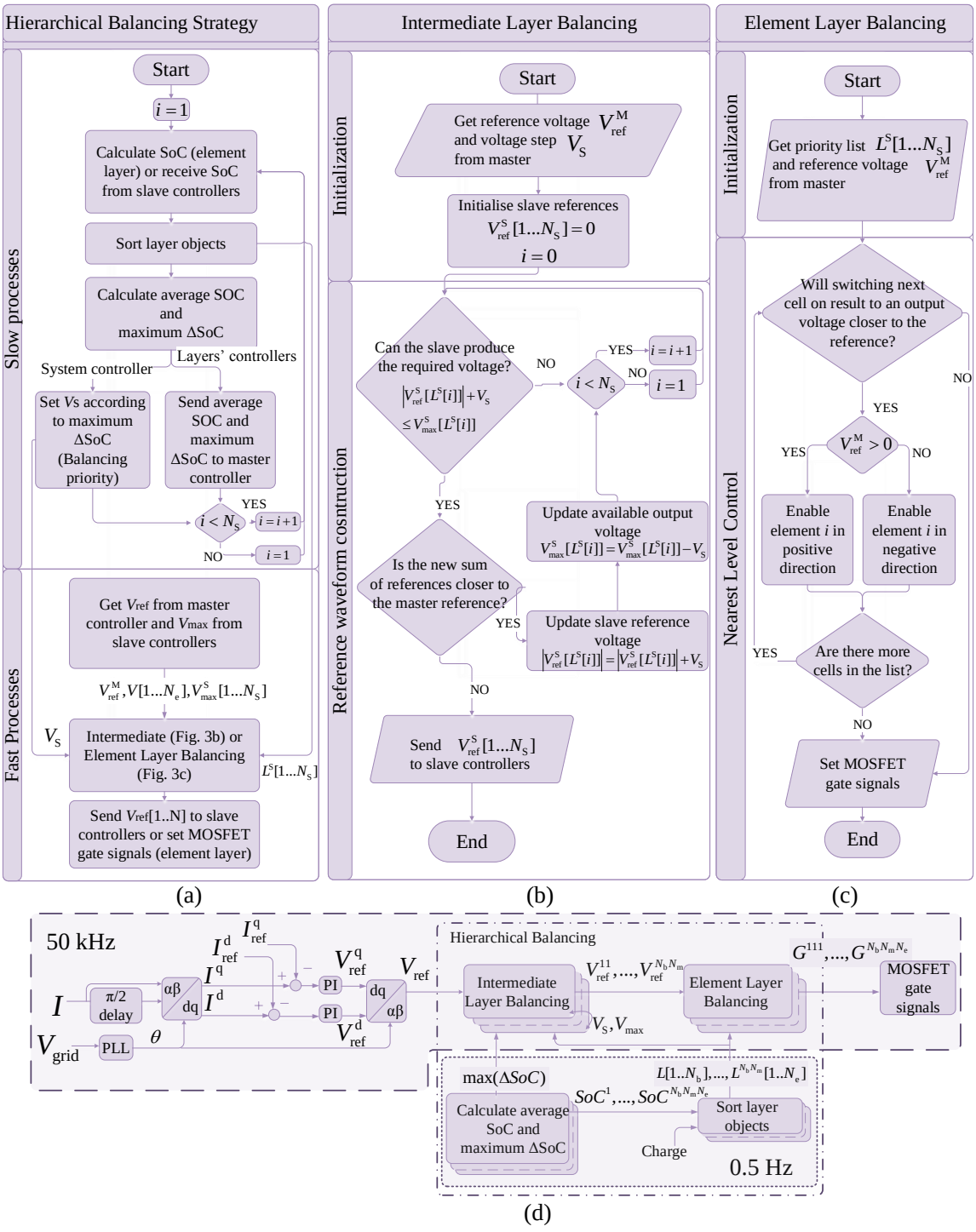


Fig. 5.2 Proposed modular BMS controller: a) hierarchical balancing control b) intermediate layer balancing control c) element layer balancing control d) complete control of a single-phase CHB-BESS including hierarchical balancing.

During the fast process, each layer controller receives a voltage reference $V_{\mathrm{ref}}^{\mathrm{M}}$ and a voltage step V_{S} from its master and the maximum output voltage from its slaves

($V_{\mathrm{max}}^{\mathrm{S}}[1 \dots N_{\mathrm{S}}]$) and uses that to calculate the voltage reference that will be sent to the slave controllers ($V_{\mathrm{ref}}^{\mathrm{S}}[1 \dots N_{\mathrm{S}}]$). The process of deconstructing the voltage reference $V_{\mathrm{ref}}^{\mathrm{M}}$ to produce the slave references $\boldsymbol{V_{\mathrm{ref}}^{S}}$ is described in Fig. 5.2b and depicted in Fig. 5.3. Each $V_{\mathrm{ref}}^{\mathrm{S}}(i)$ corresponds to a different duty cycle so balancing between layer objects can be achieved by assigning a voltage reference at each object based on their position in the respective priority list $\boldsymbol{L^{S}}$ (i.e. $V_{\mathrm{ref}}^{\mathrm{S}}$ that correspond to higher duty cycles are assigned to the objects with positions closer to 1). The developed algorithm ensures that the slave reference voltages are constructed in a way so that all available voltage steps are used even when the elements are balanced, by switching the elements on and off at different instances in time and thus avoiding simultaneous switching of the H-bridges. This is an advantage of the proposed algorithm compared to [127], where under balanced conditions all the modules will receive the same voltage reference and thus switch their respective elements at the same time effectively limiting the output voltage quality of the CHB (the smaller output voltage step in this case would be $N_{\mathrm{b}}N_{\mathrm{m}}V_{\mathrm{e}}$ instead of V_{e}). The output voltage capability of the slave objects $\boldsymbol{V_{\mathrm{max}}^{S}}$ (i.e. the maximum output voltage that the slave can provide) is taken into consideration during the reference waveform construction and if an object is not able to produce the reference voltage (for example due to an element failure in that module) the next object in the priority list with the ability to satisfy the voltage requirement will be used. It should be noted that although the switching frequency of each element's MOSFETs is twice the fundamental frequency of the grid (in this case 100 Hz for a grid frequency of 50 Hz) the switching events are located with a resolution in time of the reciprocal of the fast process frequency (in this case 20 μs).

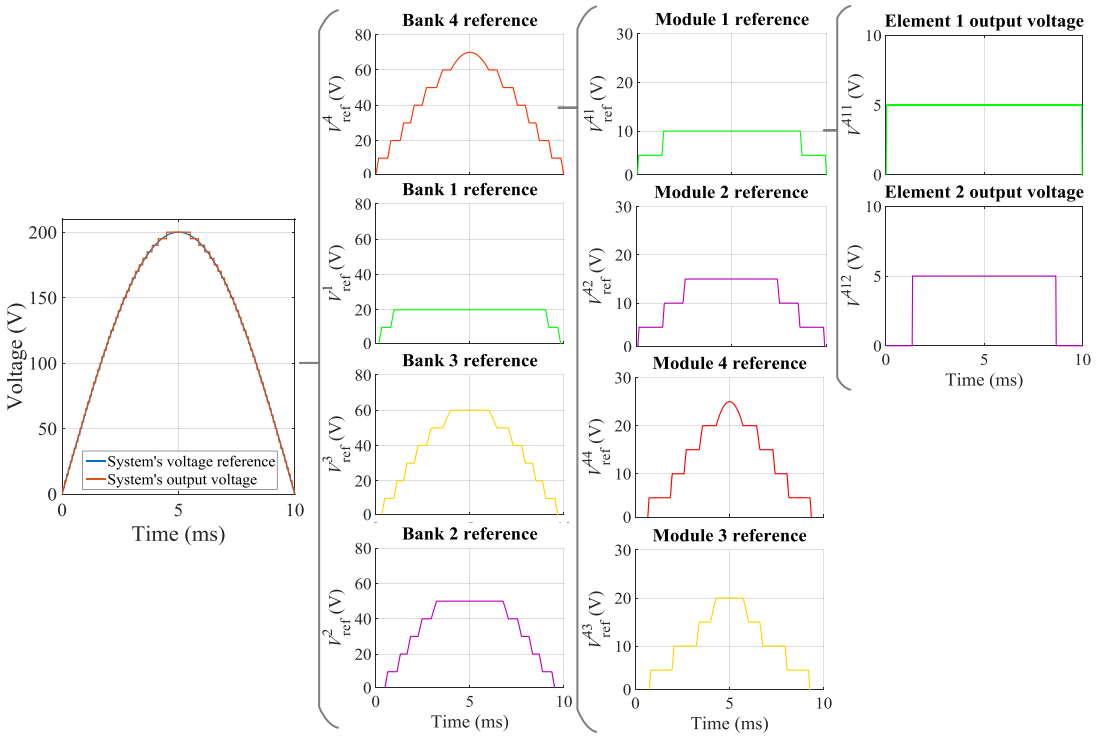


Fig. 5.3 Demonstration of bank and module layer reference construction from the system's reference output voltage. Bank layer reference voltages for $L = [4\ 1\ 3\ 2], V_{\max} = [20\ 50\ 70\ 70], V_{\mathrm{s}} = 10$. Module layer reference voltages for $L^4 = [1\ 2\ 4\ 3], V_{\max}^4 = [10\ 15\ 25\ 25], V_{\mathrm{s}} = V_{\mathrm{e}} = 5$.

The waveform of each slave reference voltage $V_{\mathrm{ref}}^{\mathrm{S}}(i)$ and thus the sequence based on which different elements are introduced to the current path is highly dependent on the choice of the voltage step V_{S}. The voltage step should be set equal to the average voltage of the objects in any one particular layer. In this study the voltage step is set equal to either the element voltage V_{e}, module voltage V_{m} or bank voltage V_{b}. When $V_{\mathrm{S}} = V_{\mathrm{e}}$ the i^{th} elements of each module will be introduced in the current path only after all the $(i-1)^{\mathrm{th}}$ elements have been switched on (i.e. element 1 of module 1 of bank 1 is turned on first, then element 1 of module 1 of bank 2 etc.) thus all elements in a module will experience very different duty cycles which will enhance the balancing performance between elements. However the average duty cycles of the higher layer objects (modules and banks) are very similar since the respective slave objects occupy neighbouring steps in the voltage waveform. This is demonstrated using the example of a two layer system in Fig. 5.4. Here, the pack comprises three modules of five elements each. When a voltage

step equal to the element voltage V_e is used, the elements of module three occupy voltage steps 3, 6, 9, 12 and 15 in the output voltage with the maximum charge difference between the elements depicted in the grey area. The charge difference between elements is directly associated with the ability of the system to perform balancing i.e. the greater the charge difference the wider capacity or SoC differences can be accommodated. When $V_S = V_m$ all the elements in module 1 are introduced to the current path sequentially (voltage steps 1-5), followed by the elements in module 2 (voltage steps 6-10) and then module 3 (voltage steps 11-15). In that case the maximum charge difference between elements is noticeably less compared to Fig. 5.4a but this positioning will result to a higher charge difference between the three modules. In general, by setting V_S equal to the voltage of a layer's object, balancing priority is given to that layer i.e. the objects of that layer can be operated under very different charges compared to the objects of the other layers. The proposed algorithm can prioritise balancing between layers during operation by dynamically setting V_S equal to the voltage of the layer where the maximum SoC variation between objects can be found. Balancing priority may be important in some scenarios, for example if the system operator replaces a module after failure, this module may have a very different average SoC compared to other modules but module balancing speed would be limited due to the small variation of average module currents. When a flat BMS is used where the master controller has a detailed knowledge of the state of every element in the system, balancing priority is not an issue since any element can be used at any voltage step in the construction of the output voltage so that an optimum charge can be allocated to each element based on their capacity or SoC. This is not the case in the modular BMS considered here, where only limited information is exchanged between layers and thus no one controller has detailed knowledge of the state of every element in the system.

The layer balancing control presented in Fig. 5.2b is identical for all hierarchical layers except the element layer. Element layer balancing control is similar to the balancing control of the flat structure discussed in Chapter 2 except with the reference voltage provided by the respective master module controller instead the centralised controller (Fig. 5.2c). The complete system control including the single-phase PLL and a *d-q* current controller is presented in Fig. 5.2d. The output of the current controller is the voltage reference used as input in the higher level balancing controller.

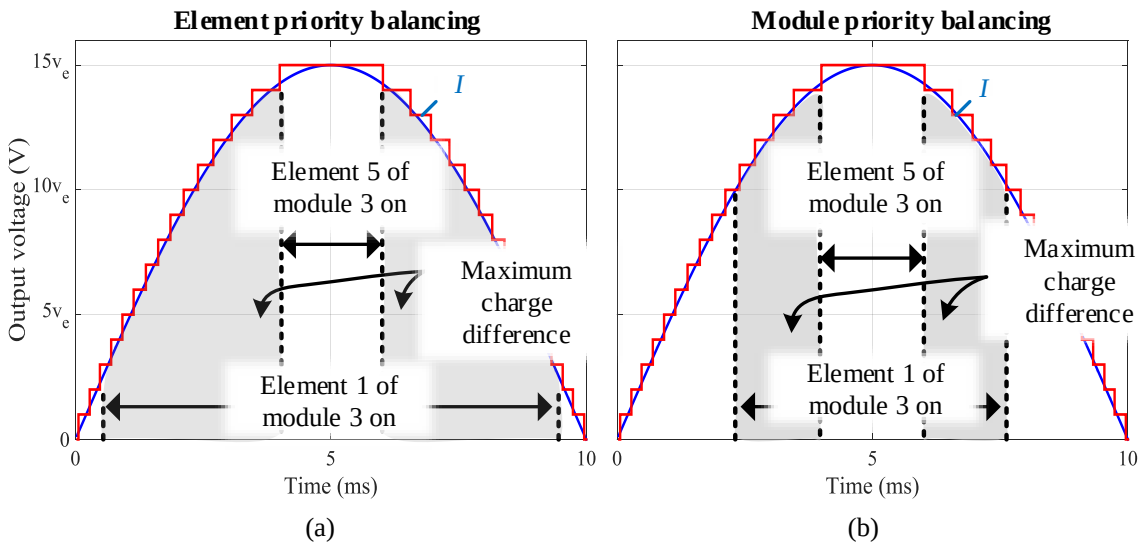


Fig. 5.4 Example of maximum achievable charge difference between the elements of a module: a) when balancing with element priority is implemented b) when balancing with module priority is implemented.

5.2 Simulation results

In order to validate the proposed hierarchical balancing control, the balancing of 1,000 elements during consecutive charging and discharging cycles is simulated in MATLAB, assuming 4% redundant elements and $I_{\mathrm{rms}} = 4$ A. The simulated system includes ten banks, each bank ten modules and each module ten elements. The balancing performance is evaluated for three different cases: 1) when maximum capacity imbalance is observed in the element layer, 2) maximum imbalance in the module layer and 3) maximum imbalance in the bank layer. In all cases, a maximum initial SoC variation of 10% is introduced between elements and their capacities are normally distributed according to (5.1).

$$\begin{aligned} \boldsymbol{Q_{\mathrm{b}}} &\sim N(\mu, \sigma_{\mathrm{b}}^2) \\ \boldsymbol{Q_{\mathrm{m}}^{i}} &\sim N(Q_{\mathrm{b}}(i), \sigma_{\mathrm{m}}^2) \;\; i \in [1, \cdots, N_{\mathrm{b}}] \\ \boldsymbol{Q_{\mathrm{e}}^{ij}} &\sim N\left(Q_{\mathrm{m}}^{i}(j), \sigma_{\mathrm{e}}^2\right) \;\; i \in [1, \cdots, N_{\mathrm{b}}], j \in [1, \cdots, N_{\mathrm{m}}] \end{aligned} \tag{5.1}$$

where $\boldsymbol{Q}_{\mathbf{b}}$ is the vector of bank capacities, $\boldsymbol{Q}_{\mathbf{m}}^{\boldsymbol{i}}$ the vector of module capacities for bank i, $\boldsymbol{Q}_{\mathbf{e}}^{\boldsymbol{ij}}$ the vector of element capacities for module j of bank i, μ is the mean of the bank capacity distribution and is equal to 1 Ah. For the other distributions, the mean is equal to the average capacity value of the respective object in the previous hierarchical layer. The variance σ^2 of each layer is equal to 0.06 if this layer has the maximum capacity variation and equal to 0.006 if not (i.e. in the case of maximum capacity variation in element layer, $\sigma_{\mathrm{e}}^2 = 0.06$ and $\sigma_{\mathrm{m}}^2 = \sigma_{\mathrm{b}}^2 = 0.006$).

Each cycle ends when any element reaches the upper (95 %) or lower (5%) SoC limit and then the next discharging or charging cycle begins.

The flat BMS approach is used here as the reference case since the sorting balancing algorithm used in that case (presented in Chapter 2) is able to fully utilise the inherent ability of the CHB circuit to perform DCB as demonstrated in Chapter 3 (i.e. with global supervision of all the elements in the system it can place any element at any switching position and thus provide the best overall balancing performance).

Balancing performance of the proposed algorithm is examined for three cases where the dynamic balancing priority between layers is disabled i.e. the algorithm cannot change the V_{s} variable during operation and thus loses the ability to prioritise balancing according to the maximum observed SoC imbalance between the objects of each layer. Instead the system operates with either a continuous priority in element balancing ($V_{\mathrm{s}} = V_{\mathrm{e}}$), continuous priority in module balancing ($V_{\mathrm{s}} = V_{\mathrm{m}}$) or continuous priority in bank balancing ($V_{\mathrm{s}} = V_{\mathrm{b}}$ for the banks and $V_{\mathrm{s}} = V_{\mathrm{m}}$ for the modules). As previously explained, when priority is given in balancing the objects of one layer, balancing the objects of the other layers becomes more challenging.

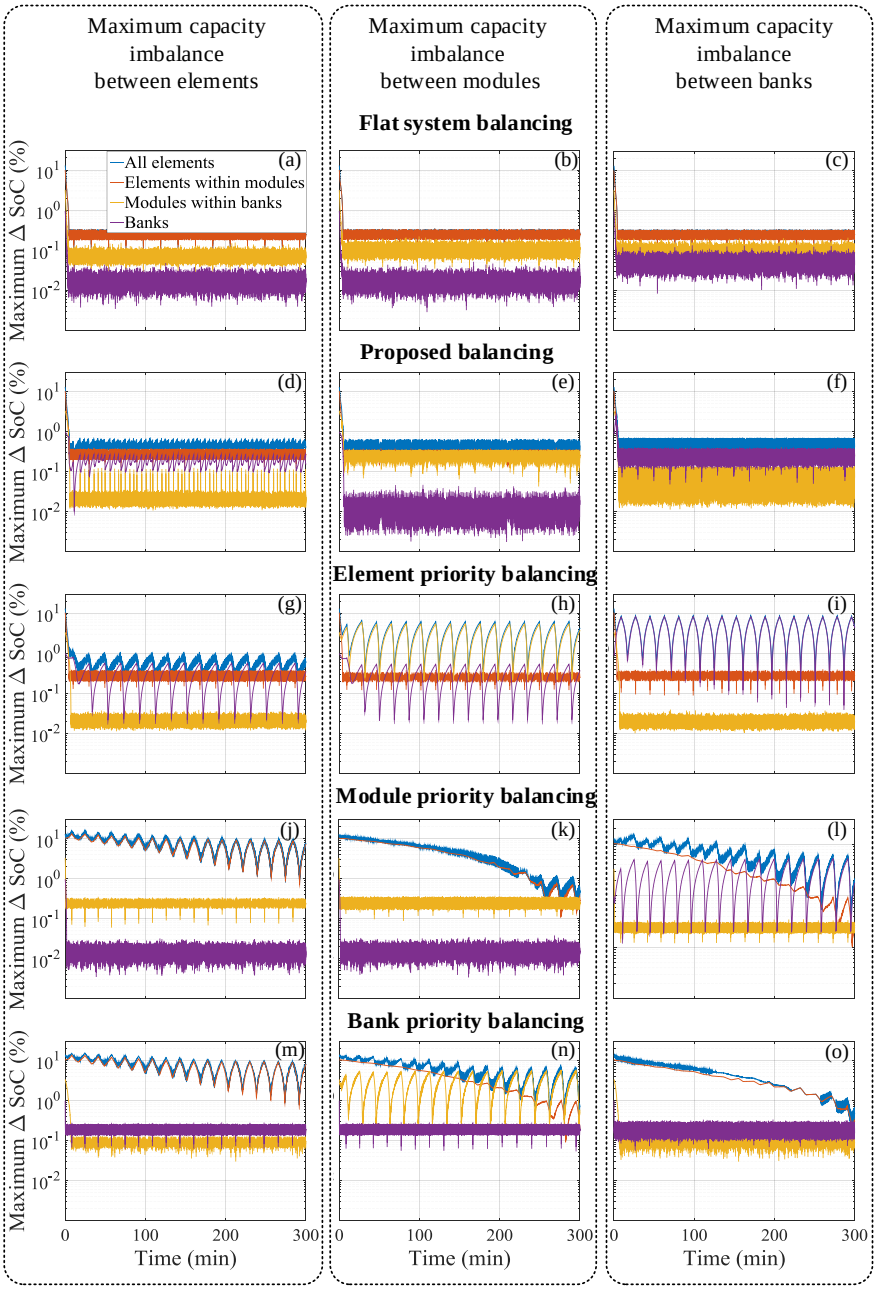


Fig. 5.5 Simulation results of hierarchical balancing. Performance of flat system balancing under maximum capacity variation at: a) element, b) module, c) bank level. Performance of the proposed balancing algorithm under maximum capacity variation at: d) element, e) module, f) bank level. Element priority balancing under maximum capacity variation at: g) element, h) module, i) bank level. Module priority balancing under maximum capacity variation at: j) element, j) module, l) bank level. Bank priority balancing under maximum capacity variation at: m) element, n) module, o) bank level.

The results of balancing using the flat BMS are presented in Fig. 5.5(system structure, e.g. the layer grouping, is retained here to facilitate comparison between different approaches although the flat system does not require such subdivisions). For all three cases of capacity imbalance, a satisfactory balancing performance is observed (maximum SoC variation between elements <0.5%) and the flat system is able to overcome an initial 10% SoC variation between elements after only 5 minutes.

When the proposed hierarchical balancing algorithm is used, a balancing performance close to that of the flat system is achieved with limited information exchange between layers. In that case, the system overcomes the initial SoC variation again at 5 minutes and the SoC variation between all elements is maintained below 0.5 % throughout operation. The importance of prioritising balancing of different layers dynamically according to their respective SoC variation is evident when the proposed algorithm, where the prioritised layer is chosen dynamically, is compared to the cases where priority is fixed to a specific layer. From all these cases it can be observed that when the layer with the maximum capacity variation is different than the layer which is given balancing priority, the system is not able to overcome that capacity variation resulting in a decreased balancing performance, e.g. in Fig. 5.5i where element balancing is given priority but the maximum capacity variation is observed between banks. In this case, the swings in the maximum SoC variation are due to the capacity variations between banks. In steady state, the ΔSoC reaches a peak value due to the limited ability of the algorithm to redistribute charge between the objects of a layer according to their capacities. In the following cycle after the maximum ΔSoC is reached, the objects start at a different initial SoC at which point the objects have very similar available capacities (i.e. the capacity that corresponds to the available SoC range for this cycle) and thus balancing will from then on be more effective resulting to a lower maximum ΔSoC. This process will be repeated resulting in these swings being observed in the maximum SoC variation between objects of different layers, as shown in Fig. 5.5.The deteriorated balancing performance in case of module and bank balancing priority is also evident in the fact that it takes more than 250 min for the system to overcome the initial SoC imbalance between elements since in these cases the system is restricted to placing elements in neighbouring positions which correspond to similar average position current and thus a weak balancing effect.

5.3 Experimental validation of the hierarchical balancing algorithm

In this section the experimental validation of the hierarchical balancing algorithm is presented, using a single-phase CHB-BESS comprising 144 LTO cells.

5.3.1 Experimental set-up

The experimental CHB-BESS includes 144 Toshiba SCiB cells (LTO cells) with a 20 Ah nominal capacity. Each cell is connected to an H-bridge forming an element and the elements are organised in twelve physical groups of twelve elements each, referred to as modules (Fig. 5.6c). Each module is equipped with a PCB including twelve ADCs to measure cell voltages and a current sensor that is used to calculate cell charge by coulomb counting. Cell monitoring and control is performed locally at each module using an FPGA. Although the module configuration is the same as the one used in the experiments presented in Chapters 2 and 3, the controller implemented in the FPGAs is fundamentally different. In the previous chapters, a single module was used individually to simulate a CHB-BESS with a flat BMS architecture, implementing the balancing control scheme presented in Fig. 2.6. In the complete CHB-BESS used in this chapter, a modular BMS architecture is implemented as described in Fig. 5.2. The element layer balancing control is performed in the FPGA of each module, which produces the priority list of the cells included in that module and generates the switching signals for their respective MOSFET drivers using the NLC modulation scheme. A daisy-chain communication link connects these twelve slave FPGAs to a master FPGA where the power controller (including single-phase PLL and current *d-q* controller) is implemented. The master FPGA is also responsible for coordinating communication between the slave FPGAs and a lab PC that runs a MATLAB GUI where the hierarchical balancing control is implemented. The GUI allows the user to set a grid current reference and monitor cell voltages and SoCs which are broadcast by the slave FPGAs and collected by the master FPGA. The hierarchical balancing control is performed in MATLAB and once the reference voltages are produced from the upper layer balancing controller they are sent to the master FPGA that distributes them to the respective slave FPGAs where the element balancing is performed.

The system is coupled to the grid using a single inductor that serves as a low pass filter and as an impedance for the current controller to work against. A single-phase isolation transformer is used connected to a variac that allows controlling the voltage level at the input of the BESS. The experimental setup is presented in detail in Fig. 5.6.

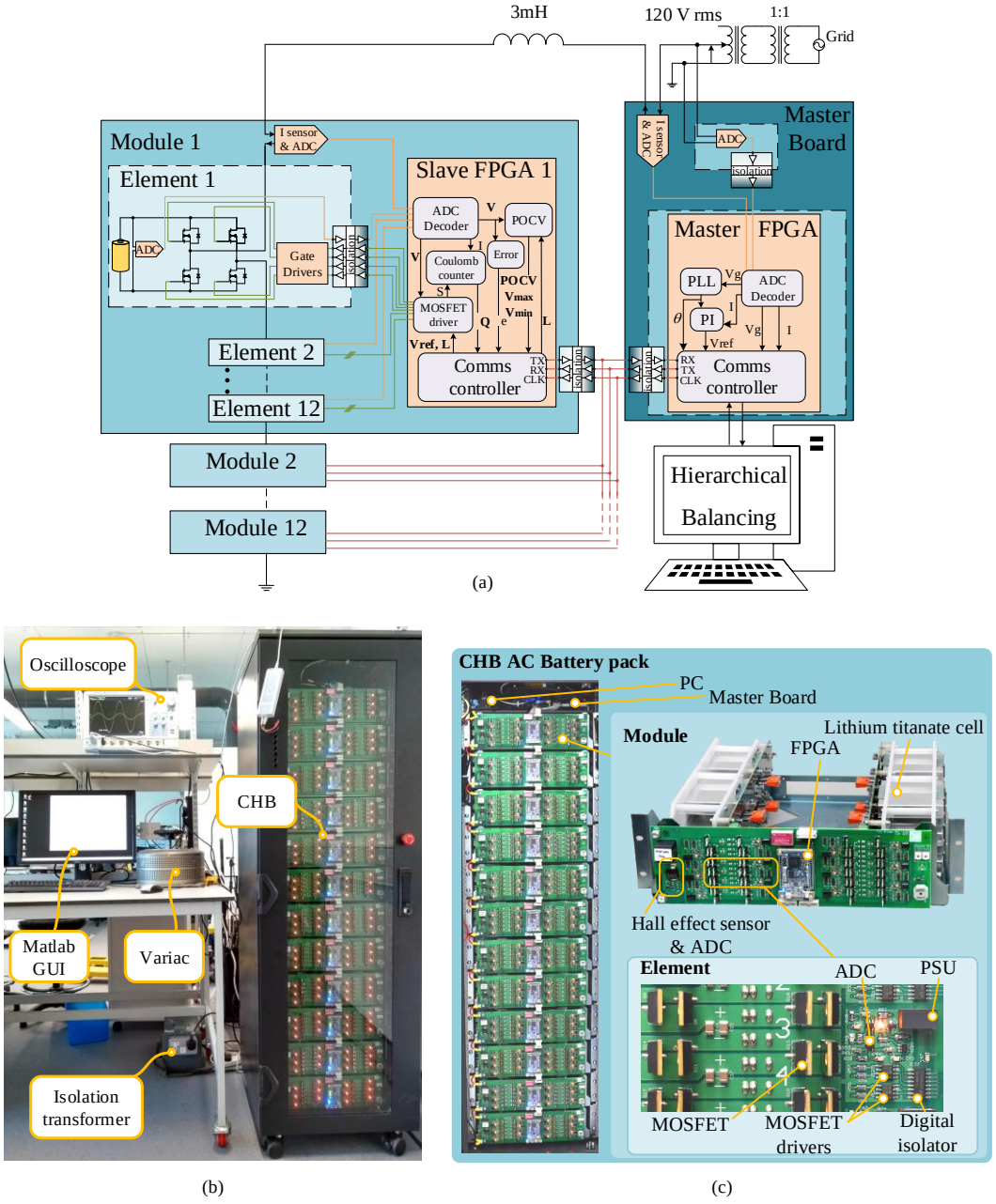


Fig. 5.6 Experimental setup for hierarchical balancing validation: a) schematic of the experimental CHB-BESS including control blocks b) photo of the experimental setup c) detailed breakdown of the CHB-BESS including twelve modules of twelve elements each.

5.3.2 Experimental procedure

In order to demonstrate hierarchical balancing control, the CHB-BESS is divided in three virtual layers as follows: three banks including four modules of twelve elements each. During the test, the voltage at the input of the CHB is set at 120 V RMS. The actual output voltage of the CHB is higher than 120 V when the system is discharging and lower when charging due to the voltage drop across the grid coupling inductor. Consequently, the redundancy ratio of the CHB varies accordingly during operation due to the varying element voltages: as element voltage increases during charging, fewer elements are required to synthesise the output voltage and thus an increased balancing performance can be achieved. The CHB is operated in three consecutive charging (current reference -10 A RMS) and discharging (current reference 10 A RMS) cycles of 1 hour duration each. After the end of the second charging cycle, the elements are left to rest for 30 min in order to accurately measure the OCV. The CHB output voltage and current waveforms are presented in Fig. 5.7.

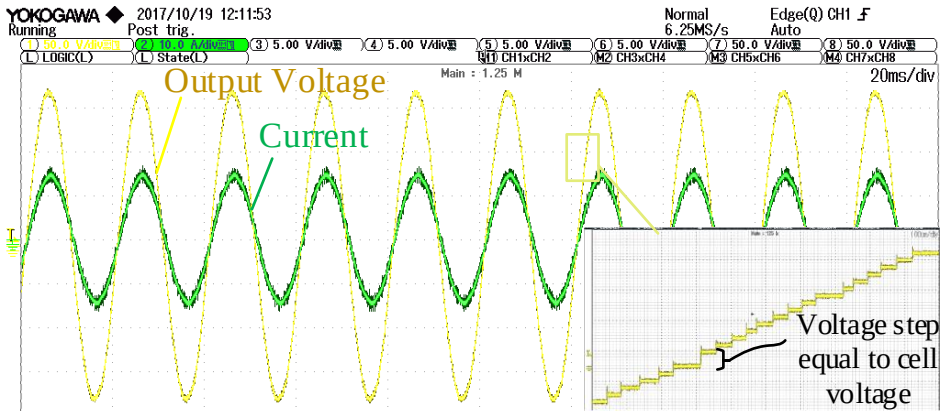


Fig. 5.7 Output voltage and current of the CHB during the tests.

To evaluate the balancing performance of the proposed algorithm, before the beginning of the test the elements are unevenly discharged according to the initialisation process described in Fig. 5.8 so that a maximum initial SoC variation equal to 7% is introduced between the banks and between the modules of the system. The maximum initial SoC variation between the elements within a module is equal to 10% and the maximum initial SoC variation between all elements of the system is equal to 20% (observed between element 1 of module 1 and element 12 of module 12). To evaluate the

ability of the system to overcome capacity variations between elements, the cell of element 1 of module 9 is replaced with a cell that has been cycled over 3,000 cycles so that its capacity is decreased by 5% (19 Ah). All the steps followed during the experimental validation are presented in detail in the flowchart of Fig. 5.8.

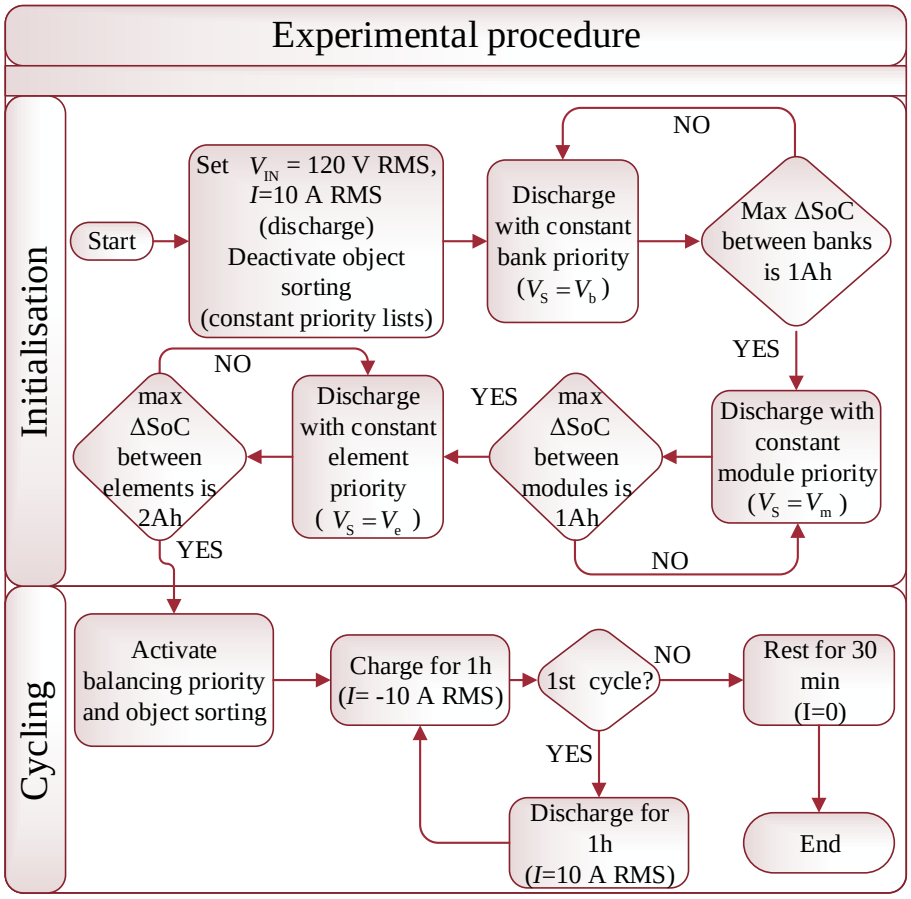


Fig. 5.8 Flowchart of the experimental process.

Here, balancing is performed using POCV as described in Chapter 2. In order to obtain a POCV, one cell from each module is bypassed every two seconds. The sorting of elements, modules and banks is thus performed every two seconds after a new POCV measurement is made. The idle state duration is different here since in this test LTO cells are used compared to the Li-po cells used in Chapter 2. The balancing priority is updated every two minutes by calculating the maximum POCV variation between the objects of each layer using the average POCV during this period.

5.3.3 Experimental results and discussion

The balancing of the objects in the three conceptual layers (i.e. banks, modules and elements) is presented in Fig. 5.9. In order to smooth the experimental data (POCV and element position) a moving average filter is used, taking the average of 50 samples from the POCV data and 500 samples from the position data. An increased number of samples is required for the position data since element position is updated every 2 s (discrete values ranging from 0-12 for the elements, 0-4 for the modules and 0-3 for the banks) so the average value of the position is required in order to produce a relatively smooth line that can give us an insight on the behaviour of the algorithm. Since the voltage difference of the POCV measurements between subsequent samples is only limited to a few millivolts, a lower number of samples are used in the POCV average filter. The CHB is able to overcome the initial SoC variation and achieve balancing within the first charging cycle, demonstrating the ability of the system to effectively allocate charge between elements and to overcome a capacity imbalance between the objects of a layer.

Balancing between the objects of a layer is more noticeable when balancing priority is given to that layer. From the subplot in Fig. 5.9a it can be seen that the average POCVs of the three banks converge when priority is given to bank balancing. When priority is given to any other layer, the POCVs of the banks vary with almost the same rate since in that case balancing is slower due to the smaller average current variation between banks. Similar behaviour can be observed in the other two layers as can be seen in the respective subplots in Fig. 5.9c and Fig. 5.9e. After achieving balancing at around 50 mins, balancing priority is given to the element layer in order to overcome the variation in element capacities observed mainly in module 9 (or module 1 of bank 3 considering the conceptual hierarchical arrangement) where the lowest capacity element is located (capacity of cell in element 1 is 19 Ah compared to 20 Ah nominal capacity).

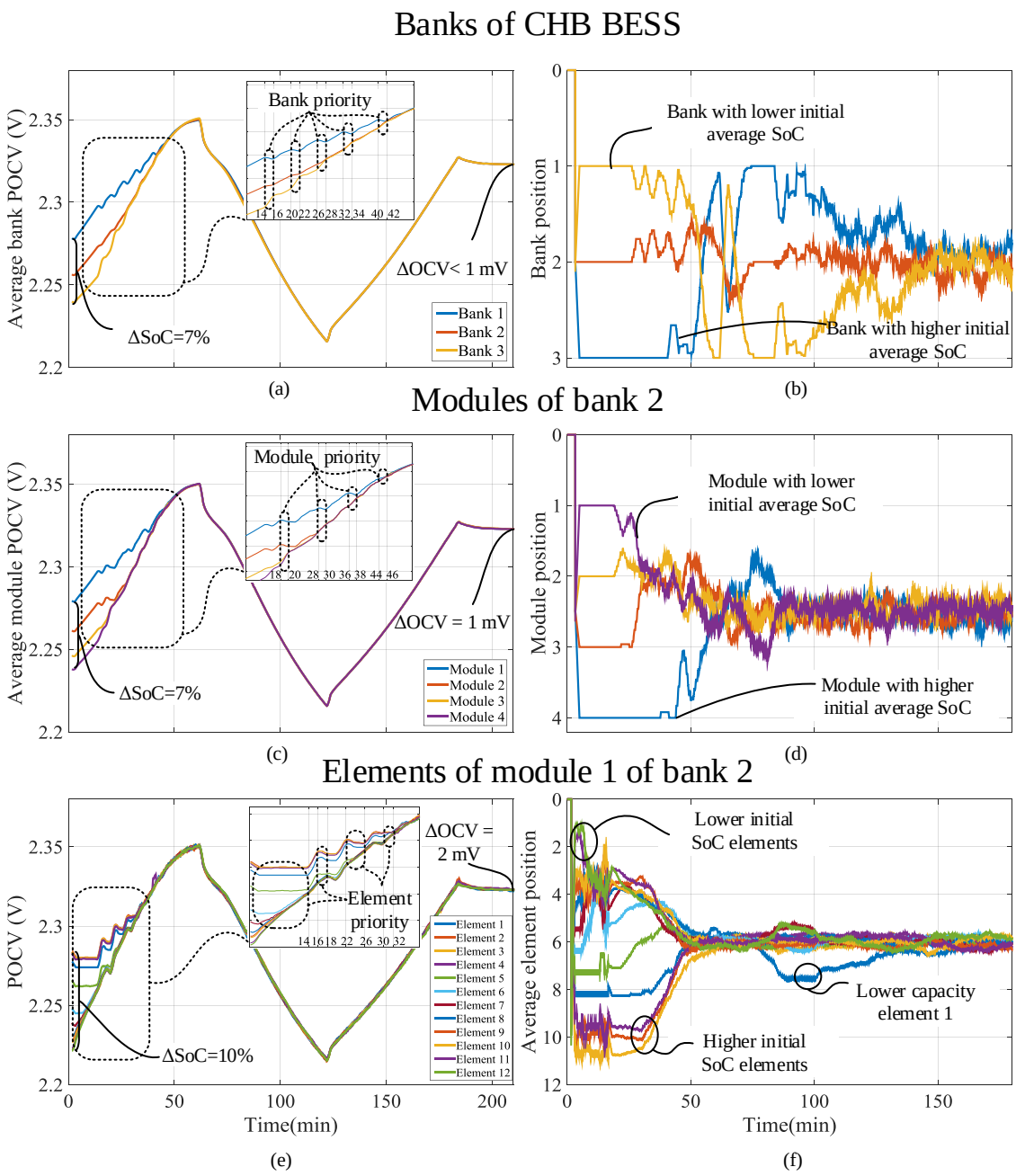


Fig. 5.9 Experimental results of cell balancing using the CHB and the proposed balancing algorithm: a) POCV balancing and b) average bank position of the banks of the CHB-BESS c) POCV balancing and d) average position of modules in bank 2 e) POCV balancing and f) average element position in module 1 of bank 3.

The position of the objects of each layer in their respective priority list is also presented in Fig. 5.9. As the system is initially charging, the objects with a higher SoC are placed in positions closer to 1 since this position corresponds to a higher average current

compared to higher-numbered positions. After POCV balancing is achieved and since all three banks have essentially equal average capacities, balanced operation is achieved by operating all banks equally as indicated by the close matching of their average position (average bank position close to 2 for all banks) in Fig. 5.9b. Similarly, the modules in bank 2 remain balanced by operating with an average position close to 2.5. Regarding the elements in bank 3 it can be observed in Fig. 5.9f that all elements have an average position equal to 6 except element 1 which has a lower average element position (between 7 and 8). This is the element including the cell with the lowest capacity and so it is operated with a lower effective duty cycle in order for the cells to remain balanced. The successful balancing is also confirmed by the close agreement of the OCVs after the cells are left to rest at the end of the test.

5.4 Conclusions

This chapter presents a decentralized modular BMS architecture following a hierarchical structure for the control of large scale CHB-BESSs. The elements of the CHB are organised in conceptual control layers and the objects of each layer are equipped with a local controller that acts as a master for the controllers of the next lower hierarchical level. Although a high update rate and time resolution is required in order to produce a high quality output voltage, the signal processing and bandwidth requirement of the local controller communication interface is dramatically decreased when compared to the centralised control of a flat BMS architecture, because the relevant control signals need only be sent to a relatively small number of slave controllers.

In this context, a hierarchical balancing algorithm is developed that enables balancing the elements of the battery pack by balancing the objects of the different layers. The proposed algorithm can adapt its balancing performance dynamically during operation by continuously monitoring the maximum SoC variation between the objects of each layer. This way it can ensure that different objects will be operated under sufficiently different charge in order to effectively overcome capacity variations within different layers. Another important feature of the proposed algorithm is the ability to fully utilize the available voltage steps of the pack thus increasing output voltage quality whilst also

ensuring that the output voltage reference can always be met given that an adequate number of cells are available in the pack.

The ability of the hierarchical balancing algorithm to overcome initial SoC and capacity variations between the elements was validated in simulation for a 1,000 element system organised in three symmetrical layers of ten objects each, and experimentally using a CHB-BESS comprising 144 lithium titanate cells organised into three layers following a non-symmetrical layer configuration i.e. three banks, four modules per bank and twelve elements per module.

Although the hierarchical system structure results to scalable control architecture, the balancing performance of the CHB cannot be guaranteed if the system is not able to freely place the cells at the available switching positions. The simulation and experimental results demonstrate that by implementing the proposed algorithm, a decentralised system can fully utilise the underlying hardware and thus achieve equivalent balancing performance to that of a CHB with a centralised controller and global supervision of the cells.

Chapter 6 Conclusions and future work

This thesis presented the framework for evaluating the performance of modular BESS with the power electronics integrated deep in the battery pack, in order to allow comparison with conventional BESS architectures. The operation of the modular CHB-BESS was analysed and a balancing algorithm that can be used as part of a modular BMS was developed and validated experimentally. In this chapter, the contributions of the thesis are summarised in detail, followed by a discussion of areas where further research is required as identified from the current work.

6.1 Conclusions

The contributions of this thesis can be summarised in two groups: (i) the framework for evaluating competing BESS designs and (ii) the development of control algorithms for large scale, modular CHB-BESSs.

6.1.1 Framework for evaluating competing BESS designs

In this section the contribution of this thesis on developing a framework for the evaluation of competing BESS designs is discussed. This includes the linear programming framework for the evaluation of balancing performance presented in chapter 3 and the methodology for comparing BESS considering power losses, reliability and cost, presented in chapter 4.

6.1.1.1 Balancing performance evaluation

Chapter 3 presented a method for quantitatively evaluating the balancing performance of active balancing circuits implementing either energy redistribution or duty cycle balancing, under the simplifying assumption of constant cell voltage. The balancing problem was formulated as a linear programming problem with the objective of maximising the useable capacity of a pack of cells for a given set of cell capacities. It has been shown that balancing performance depends on the maximum balancing current of ERB circuits and the available cell redundancy of DCB circuits. The maximum balancing current that can be achieved in ERB circuits is a function of cell voltage, switching frequency and size of passive elements (e.g. capacitors and inductors). By identifying the minimum value of the balancing current (ERB) and cell redundancy (DCB) that is required in order to fully utilise the available cell capacity throughout the lifetime of the system (assuming capacity variation between cells over the lifetime of the system can be modelled), it is possible to design ERB and DCB circuits with equivalent balancing performance and compare them in terms of cost, efficiency and ease of implementation before choosing the best solution for a specific battery pack design.

The output of the linear programming tool is the maximum useable capacity (Q_{u}^{*}) that can be achieved for a given balancing circuit, set of cell capacities and cell redundancy, without modelling any one particular control algorithm. This tool can be used to set a benchmark for any proposed balancing algorithm by comparing the usable capacity (Q_{u}) that can be achieved when a specific algorithm is implemented on-line to the theoretical maximum useable capacity (Q_{u}^{*}): If $Q_{\mathrm{u}} = Q_{\mathrm{u}}^{*}$ the algorithm can deliver the best possible utilisation of pack capacity whereas if $Q_{\mathrm{u}} < Q_{\mathrm{u}}^{*}$ then there is room for improving the algorithm to achieve better capacity utilisation. By this criteria, the sorting algorithm presented in chapter 2 is successful because Q_{u} and Q_{u}^{*} agree to within the experimental error in all cases trialled in chapter 3. However this does not necessarily imply that the algorithm used in the experiment will always extract maximum usable capacity e.g. for different cell capacities, different charge/discharge rates, different cell chemistries etc.

In general, a DCB-AC pack based on the CHB converter is able to handle relatively extreme capacity variations between the cells in the battery pack due to the inherent ability to operate cells under different currents (as demonstrated in chapters 2 and 3), even when no redundant cells are included in the pack. This makes the CHB-BESS particularly attractive for grid scale systems with expected lifetimes more than 10 years. For these applications it is important to design the system appropriately in order to ensure that the rated capacity will be accessible throughout the lifetime of the BESS, even when the capacity of the cells has degraded and cell capacity variations are exacerbated. The improved balancing performance of the CHB also greatly facilitates the maintenance procedure: when replacing a module it is not necessary for the new cells to have an equal capacity or SoC to that of the existing cells, since the useable capacity is no longer limited by the lowest capacity (or SoC) cells.

6.1.1.2 Overall BESS design evaluation

Chapter 4 presented a method for evaluating competing designs for grid-connected BESSs with different level of integration of power electronics in the battery pack. The steady-state power losses of the grid interface converter, the battery pack and the balancing circuit are calculated analytically and used to produce variations in component failure rates according to the operating state of the system. The reliability of each system is then calculated using a Markov-based modelling approach that captures the performance degradation caused by faults. This methodology was used in a case study to compare three design options for a 1 MW/1 MWh BESS connected at 11 kV: a conventional BESS using parallel low-voltage power blocks (PB-BESS), a BESS using a high-voltage power electronics enhanced battery pack (IBP-BESS) and a BESS using a CHB converter (CHB-BESS).

The results of this analysis indicate that power electronics enhanced systems such as the IBP and CHB can achieve a significant improvement of the overall system reliability (an order of magnitude when the reliability of the cells is equivalent to that of the power electronics switches) at a lower capital cost (capital cost of CHB-BESS is 13% lower than that of the PB-BESS) but with a relatively minor decrease in efficiency (CHB has approximately 2% lower efficiency compared to the PB-BESS). The improvement in reliability is attributed to the ability of the IBP-BESS and CHB-BESS to bypass failed

modules without causing many other modules to become inaccessible (as is the case in the conventional PB-BESS configuration, where a single module failure is addressed by isolating the whole string that includes the failed module). This is based on the assumption that MOSFETs in the deeply modular designs will fail short-circuit so that the current path is not disrupted. If a MOSFET in an H-bridge fails short circuit, when the other MOSFET of the same converter leg is turned on, the li-ion cell will be shorted and the high short-circuit current can blow the bond wires and cause the MOSFET to fail open-circuit in a second stage. This could be avoided by using a high speed fuse in series with the cell, however reliable operation of the system after semiconductor failure should be validated experimentally. Moreover, this study does not consider the reliability of the supporting electronics (control system, gate drives etc.). These components may have substantial impact on the system's MTTF, especially in the case of the IPB-BESS and CHB-BESS designs which include many more controllable power electronic components when compared to the conventional BP-BESS design.

Another limitation of the proposed method is that the component failure rates are not time dependent and thus cannot capture degradation of li-ion cells due to cell ageing. Moreover, although the effect of component temperature is considered in the failures rates by using the appropriate π factors, the failure rate of certain components e.g. MOSFETs would be more accurately described by considering the thermal cycling of the device. As a result, although the proposed method can be used to perform an initial evaluation of competing system designs, an in depth investigation of system reliability would require more advanced failure models as well as a detailed simulation of the system's operation under real load profiles.

The higher cost of the PB-BESS is partially due to the necessity to oversize the battery pack in order to ensure that the system will be able to deliver the required energy capacity, even when no active balancing is implemented. This is not the case when the IBP or CHB architecture is used since the ability to perform DCB effectively reduces the number of cells that are required to achieve a certain capacity by ensuring that the useable capacity is not limited by the lowest capacity cells.

The increased power losses of the IBP compared to the PB are due to the increased switching losses, indicating that a multilevel converter topology might be more appropriate for the centralised converter. For the CHB, the increased losses are due to the

non-smooth current waveform that the cells experience and the accumulated conduction losses of the MOSFETs. These issues can be addressed by using an additional DC/DC converter between the cell and the H-bridge in order to provide a smooth DC current to the cell and by reducing the on-state resistance of the MOSFET at each H-bridge (either by using more expensive, lower resistance MOSFETs or by connecting two MOSFETs in parallel per switch). These design choices however will increase the overall cost of the system and possibly affect system reliability. It should be noted that the three systems compared in chapter 3 where designed under the assumption that the voltage and current stress of the power electronics switches should be equal in all three systems (i.e. the designs were optimised for cost and not efficiency). An alternative design approach for example would specify a minimum efficiency requirement that all systems should meet. In this case the design choices will be different compared to the current case study but the system evaluation methodology will still be valid.

6.1.2 Deeply modular CHB-BESSs

This section summarises the contributions of this thesis on the analysis of the modular CHB-BESS and the proposed control algorithms than can be used as part of a decentralised BMS architecture.

6.1.2.1 Analysis of the operation of CHB in a BES application

The CBH has been identified as an attractive converter topology to use in deeply modular power electronics enhanced BESS designs. Chapter 2 explores the operation of the CHB assuming a flat BMS architecture where the centralised controller has global supervision of the cells in the system and each cell is individually controlled using an H-bridge converter. In this case, a high quality stepped output voltage waveform can be produced by switching the cells based on a NLC modulation scheme. Cell balancing can then be performed by controlling the switching sequence of the cells in the NLC, which determines their effective duty cycle. Taking advantage of the enhanced controllability over cells, a method that allows relative SoC estimation through POCV measurements has been developed. In order to make a POCV measurement the cell is temporarily

removed from the current path for a short period of time so that the effect of the series resistance and short time transient phenomena can be neglected. It has been shown that the effectiveness of cell balancing, when using the POCV to estimate the relative SoC, depends on the applied C-rate and the difference in cell capacities and transient resistance. Simulation results demonstrated a successful balancing to within 0.8 % of SoC between cells operated at 0.5 C and 3.5 % for cells at 2 C, with 55% initial SoC variation and up to 25% difference in nominal capacity. POCV balancing was validated experimentally using a 25-level CHB converter prototype during consecutive charging and discharging cycles of 12 Li-po cells. Through POCV balancing the system was able to overcome an initial 55% SoC variation and 45% capacity difference to achieve balancing within 5 mV of the OCV between cells.

6.1.2.2 A balancing algorithm for large scale CHB-BESSs

In order to address control complexity due to the increased amount of controllable power electronics in large scale CHB-BESSs, a decentralised BMS can be implemented where the system is organised in control layers each equipped with a local layer controller that is responsible for a small number of slave controllers. This hierarchical architecture can significantly reduce communication and centralised processing requirements, however the appropriate control algorithms need to be developed in order to ensure that balancing performance is equivalent to that of a system with a flat BMS architecture and thus global knowledge of the states of all the cells in the system. A hierarchical balancing algorithm is presented in chapter 5, which enables global cell balancing in the pack by balancing the objects of intermediate layers, while using all available voltage steps in the pack to ensure a high quality sinusoidal output voltage. The algorithm has also the in-built functionality to tolerate cell failures, ensuring that the output voltage reference is always met as long as there are an adequate number of cells available in the pack. An important feature of the algorithm is the ability to swap balancing priority dynamically between layers according to the maximum SoC variation between the objects of each layer. This is significant as it ensures that the enhanced balancing performance of the CHB (as discussed in chapter 3) is not limited by the balancing algorithm and the system is able to accommodate objects of different capacities within any hierarchical layer, without being limited by the lowest capacity object.

The hierarchical balancing algorithm was validated in simulation for a 1,000 element system (organised in three symmetrical layers of ten objects each) and was successful in retaining SoC variation between all elements below 0.5 % throughout operation, for different cases of element capacity distributions and up to 10% initial SoC variation between elements. The algorithm was implemented in a 14 kW/7 kWh CHB-BESS prototype comprising 144 LTO cells, organised into three non-symmetrical layers i.e. three banks, four modules per bank and twelve elements per module. Cell balancing to within 2 mV of the cell OCV is achieved between cells with 20% initial SoC variation and 5% capacity difference, when operated under consecutive charging and discharging cycles.

6.2 Future work

This thesis explored the concept of deeply modular power electronics enhanced battery packs and provided the tools to compare competing BESS designs. Through the detailed analysis of the CHB topology the following areas for further research work have been identified.

6.2.1 Optimum BESS design tool

The linear programming framework presented in chapter 3 and the BESS design evaluation methodology discussed in chapter 4 could be developed together in order to create an optimal BESS design tool. This concept is presented graphically in Fig. 6.1. This tool would receive as inputs specific system parameters such as the required energy and power ratings, grid voltage at the point of connection, converter topology, cell chemistry, cost of inefficiency and minimum expected MTTF. Other inputs will include specific information about the cells such as cost, voltage range, maximum allowable C-rate and temperature rise, the statistical distribution of capacities, capacity degradation rates and cell failure rates, while the tool should also be preloaded with datasheet information for a range of MOSFET and/or IGBT switches that can be used in the converter design. Based on that information the tool will design a BESS (based on a specific converter topology) that satisfies the system requirements at the minimum cost. The envisioned tool would use the linear programming framework to calculate the

minimum cell redundancy or balancing current to ensure that the required energy can be provided throughout the lifetime of the system, while the Markov-based models can be used to determine relevant design specifications (e.g. number of cells per converter modules in the CHB-BESS or number of modules that can be bypassed using the same switches in the IBP-BESS) in order to meet the expected reliability standards at the most cost efficient way. Such a tool would provide a complete solution for the design of BESSs by enabling the comparison of (optimum) system designs when different modular and conventional power electronics topologies are considered.

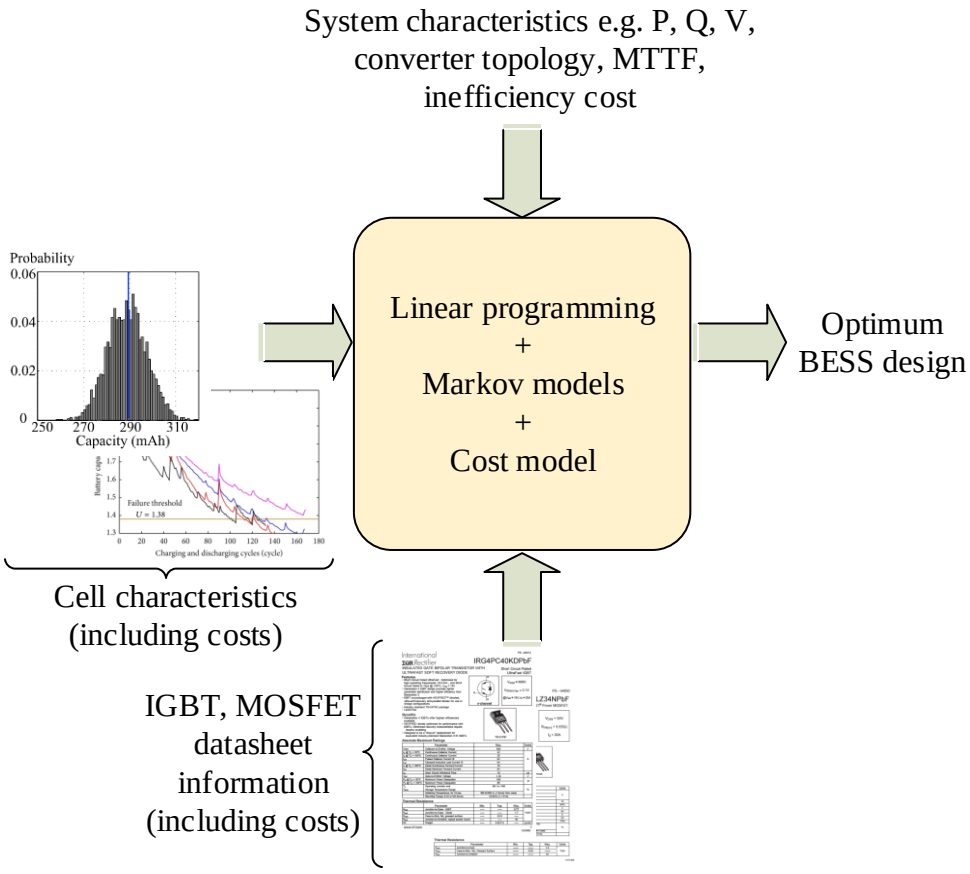


Fig. 6.1 Representation of optimum BESS design tool.

6.2.2 SoH estimation and balancing

This thesis mainly considered relative SoC estimation and balancing, however an important function of the BMS is also SoH estimation. SoH is a general term used to describe the ageing of a cell and is usually expressed as the ratio of the current capacity

over the nominal capacity of the cell. SoH estimation is important because it informs the user of the maximum energy that can be stored in the battery and because accurate knowledge of the current cell capacity is necessary for SoC estimation using coulomb counting. In order to measure cell capacity, the cell has to be fully charged and discharged which is not always possible during operation. Alternatively, various studies have presented ways of calculating cell capacity as a function of the cell internal resistance. According to [180] cell capacity $Q(t)$ can be modeled as a linear function of the internal cell resistance $R(t)$:

$$Q(t) = aR(t) + b \tag{6.1}$$

where a, b are constants that depend on the specific cell chemistry and operating conditions during the experiments that produced the data used to get (6.1) [181].

The time dependence of the internal resistance is modelled using:

$$R(t) = ce^{dt} \tag{6.2}$$

where c and d are ageing parameter constants.

In a similar study in [182] the increase of the series resistance ΔR is formulated as a power function of the number of cycles n_{C} :

$$\Delta R = kn_{\mathrm{C}}^{m} \tag{6.3}$$

where k is the coefficient and m is the exponent of the power function.

In these studies the internal resistance is used as an indication of the SoH as well as the power capability of the cell. The internal cell resistance is usually calculated using Electrochemical Impedance Spectroscopy (EIS) or through the voltage response of the cell to a current pulse [183], using:

$$R = \frac{\Delta V}{\Delta I} = \frac{V_1 - V_2}{I_1 - I_2} \tag{6.4}$$

where V_1 the voltage before the current pulse ΔI (at current I_1) and V_2 the voltage immediately after the current pulse (at current I_2).

These measurements can be challenging to perform on-line in conventional battery packs that do not allow control of individual cells. Deeply modular battery packs such as the CHB-BESS allow subjecting each cell to the desired pulsed current by controlling the exact instances of when a cell is introduced or removed from the current path, thus enable measurements of cell resistance (using similar current pulses for all cells), while the system is in operation. The resistance estimation can be used to calculate cell capacity based on pre-loaded look-up tables, to update the parameter values of RC models used for SoC estimation and to provide information about the remaining cycle life of the cell. Another potentially interesting area to explore would be the use of the cell resistance as a control variable during cell balancing. The objective of (relative) SoC balancing is maximizing the capacity/energy utilization. In other applications the objective could be maximizing the lifetime of the battery or the efficiency of the system. In that case different balancing algorithms should be implemented aiming at minimizing the resistance variation (or temperature variation) between cells or prioritizing cells with the lowest internal resistance values when high C-rates are required. The modular CHB-BESS prototype can be used as the experimental apparatus to test such balancing algorithms under various operating modes (i.e. different services provided to the grid). A combination of different cell chemistries at different degradation rates can also be used to explore the performance of the CHB in second-life applications. In these applications the BMS should be able to overcome cell-to-cell variations (e.g. in capacity and internal resistance) and the system should be able to deal effectively with unexpected cell failures in order to reliably provide the required services to the grid.

6.2.3 Completely decentralized BMS for CHB-BESS

The hierarchical balancing algorithm and the modular BMS architecture presented in Chapter 5 can significantly reduce the number of objects that each controller (top-level or local) has to address. However, the top-level controller still must provide the voltage reference from the current controller and the intermediate local controllers must produce and distribute the voltage references to their respective slaves with a high time-resolution. Further work might investigate the idea of completely decentralized BMS for a CHB-

BESS, where the local controller at each converter element would have the ability to synchronize to the grid frequency based only on local measurements e.g. current measurements. Such a concept has been discussed in [184], where the authors present a decentralized control scheme for a grid connected CHB. However, this work assumes that power is equally split between the converter modules and thus does not provide the flexibility to perform balancing between modules. A decentralized BMS implemented on a DC-PEEBP is presented in [92]. In this work the controller at each element monitors the voltage across a local inductor and is using that information to control the element's duty cycle and switching pattern in order to achieve SoC balancing while minimizing the ripple of the output DC voltage. This method could potentially be extended to an AC pack such as the CHB where the control objective would be to synchronize the switching of the modules in order to produce a sinusoidal output voltage.

6.3 Publications

1. E. Chatzinikolaou and D. J. Rogers, "Performance evaluation of duty cycle balancing in power electronics enhanced battery packs compared to conventional energy redistribution balancing", IEEE Transactions on Power Electronics, Jan. 2018 (accepted, preprint available).

2. E. Chatzinikolaou and D. J. Rogers, "Hierarchical Distributed Balancing Control for Large Scale Reconfigurable AC Battery Packs", IEEE Transactions on Power Electronics, vol. 33, no. 7, pp. 5592-5602, Dec. 2017.

3. E. Chatzinikolaou and D. J. Rogers, "A Comparison of Grid-Connected Battery Energy Storage System Designs", IEEE Transactions on Power Electronics, vol. 32, no. 9, pp. 6913-6923, Sept. 2017.

4. E. Chatzinikolaou and D. J. Rogers, "Cell SoC Balancing Using a Cascaded Full-Bridge Multilevel Converter in Battery Energy Storage Systems", IEEE Transactions on Industrial Electronics, vol. 63, no. 9, pp. 5394-5402, Sept. 2016.

5. C. Patsios, B. Wu, E. Chatzinikolaou, D. J. Rogers, N. Wade, N. P. Brandon, P. Taylor, “An integrated approach for the analysis and control of grid connected energy storage systems”, Journal of Energy Storage, vol.5, pp. 48-61, Feb. 2016.

6. E. Chatzinikolaou and D. J. Rogers, “Electrochemical cell balancing using a full-bridge multilevel converter and pseudo-open circuit voltage measurements”, 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, UK, 2016.

References

[1] R. Ferroukhi, D. Gielen, G. Kieffer, M. Taylor, D. Nagpal, and A. Khalid, "REthinking Energy: Towards a new power system," *Retrieved from Abu Dhabi, UAE: http://www. irena. org/rethinking/IRENA_REthinking_fullreport_2014. pdf*, 2014.

[2] H. Wuester, R. Ferroukhi, L. El-Katiri, D. Saygin, T. Rinke, and D. Nagpal, "REthinking energy: Renewable energy and climate change," *Int. Renew. Energy Agency, Tech. Rep*, 2015.

[3] H. Farhangi, "The path of the smart grid," *IEEE power and energy magazine*, vol. 8, no. 1, 2010.

[4] E. A. Committee, "Smart grid: Enabler of the new energy economy," *A Report by the Electricity Advisory Committee*, 2008.

[5] O. Ellabban, H. Abu-Rub, and F. Blaabjerg, "Renewable energy resources: Current status, future prospects and their enabling technology," *Renewable and Sustainable Energy Reviews*, vol. 39, pp. 748-764, 2014.

[6] C. Stark, J. Pless, J. Logan, E. Zhou, and D. J. Arent, *Renewable electricity: Insights for the coming decade*, National Renewable Energy Lab.(NREL), Golden, CO (United States), 2015.

[7] N. S. Pearre, and L. G. Swan, "Technoeconomic feasibility of grid storage: mapping electrical services and energy storage technologies," *Applied Energy*, vol. 137, pp. 501-510, 2015.

[8] P. G. Taylor, R. Bolton, D. Stone, and P. Upham, "Developing pathways for energy storage in the UK using a coevolutionary framework," *Energy Policy*, vol. 63, pp. 230-243, 2013.

[9] N. Hatziargyriou, H. Asano, R. Iravani, and C. Marnay, "Microgrids," *IEEE power and energy magazine*, vol. 5, no. 4, pp. 78-94, 2007.

[10] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. De Vicuña, and M. Castilla, "Hierarchical control of droop-controlled AC and DC microgrids—A general approach toward standardization," *IEEE Transactions on industrial electronics,* vol. 58, no. 1, pp. 158-172, 2011.

[11] N. Hatziargyriou, *Microgrids: architectures and control*: John Wiley & Sons, 2014.

[12] M. Molina, "Energy Storage and Power Electronics Technologies: A Strong Combination to Empower the Transformation to the Smart Grid," *Proceedings of the IEEE*, pp. 1-29, 2017.

[13] N. Brandon, J. Edge, M. Aunedi, P. Bruce, B. Chakrabarti, T. Esterle, J. Somerville, Y. Ding, C. Fu, and P. Grant, "UK research needs in grid scale energy storage technologies," 2016.

[14] V. Viswanathan, M. Kintner-Meyer, P. Balducci, and C. Jin, "National assessment of energy storage for grid balancing and arbitrage phase II volume 2: Cost and performance characterization," *Pacific Northwest National Laboratory,* vol. 690, 2013.

[15] M. G. Molina, *Emerging advanced energy storage systems: dynamic modeling, control and simulation*: Nova Science Publishers, 2013.

[16] Y. G. Rebours, D. S. Kirschen, M. Trotignon, and S. Rossignol, "A survey of frequency and voltage control ancillary services—Part I: Technical features," *IEEE Transactions on power systems,* vol. 22, no. 1, pp. 350-357, 2007.

[17] Y. G. Rebours, D. S. Kirschen, M. Trotignon, and S. Rossignol, "A survey of frequency and voltage control ancillary services—Part II: Economic features," *IEEE Transactions on power systems,* vol. 22, no. 1, pp. 358-366, 2007.

[18] P. Denholm, E. Ela, B. Kirby, and M. Milligan, *Role of energy storage with renewable electricity generation*, National Renewable Energy Laboratory (NREL), Golden, CO., 2010.

[19] H. Chen, T. N. Cong, W. Yang, C. Tan, Y. Li, and Y. Ding, "Progress in electrical energy storage system: A critical review," *Progress in Natural Science,* vol. 19, no. 3, pp. 291-312, 2009.

[20] B. Roberts, "Capturing grid power," *IEEE Power and Energy magazine,* vol. 7, no. 4, 2009.

[21] D. T. Ton, and W. P. Wang, "A more resilient grid: The US department of energy joins with stakeholders in an R&D plan," *IEEE Power and Energy Magazine,* vol. 13, no. 3, pp. 26-34, 2015.

[22] G. Fitzgerald, J. Mandel, J. Morris, and H. Touati, “The Economics of Battery Energy Storage: How multi-use, customer-sited batteries deliver the most services and value to customers and the grid,” *Rocky Mountain Institute*, 2015.

[23] S. Vazquez, S. M. Lukic, E. Galvan, L. G. Franquelo, and J. M. Carrasco, “Energy storage systems for transport and grid applications,” *Industrial Electronics, IEEE Transactions on,* vol. 57, no. 12, pp. 3881-3895, 2010.

[24] H. Ibrahim, A. Ilinca, and J. Perron, “Energy storage systems—characteristics and comparisons,” *Renewable and sustainable energy reviews,* vol. 12, no. 5, pp. 1221-1250, 2008.

[25] A. Dekka, R. Ghaffari, B. Venkatesh, and B. Wu, "A survey on energy storage technologies in power systems." pp. 105-111.

[26] J. C. Beardsall, C. A. Gould, and M. Al-Tai, "Energy storage systems: A review of the technology and its application in power systems." pp. 1-6.

[27] A. Alhamali, M. E. Farrag, G. Bevan, and D. M. Hepburn, "Review of energy storage systems in electric grid and their potential in distribution networks." pp. 546-551.

[28] T. Horiba, “Lithium-ion battery systems,” *Proceedings of the IEEE,* vol. 102, no. 6, pp. 939-950, 2014.

[29] H. C. Hesse, M. Schimpe, D. Kucevic, and A. Jossen, “Lithium-Ion Battery Storage for the Grid—A Review of Stationary Battery Storage System Design Tailored for Applications in Modern Power Grids,” *Energies,* vol. 10, no. 12, pp. 2107, 2017.

[30] N. Nitta, F. Wu, J. T. Lee, and G. Yushin, “Li-ion battery materials: present and future,” *Materials today,* vol. 18, no. 5, pp. 252-264, 2015.

[31] J. Baker, “New technology and possible advances in energy storage,” *Energy Policy,* vol. 36, no. 12, pp. 4368-4373, 2008.

[32] X. Luo, J. Wang, M. Dooner, and J. Clarke, “Overview of current development in electrical energy storage technologies and the application potential in power system operation,” *Applied Energy,* vol. 137, pp. 511-536, 2015.

[33] G. Graditi, M. Ippolito, E. Telaretti, and G. Zizzo, “Technical and economical assessment of distributed electrochemical storages for load shifting applications: An Italian case study,” *Renewable and Sustainable Energy Reviews,* vol. 57, pp. 515-523, 2016.

[34] I. Hadjipaschalis, A. Poullikkas, and V. Efthimiou, “Overview of current and future energy storage technologies for electric power applications,” *Renewable and sustainable energy reviews*, vol. 13, no. 6, pp. 1513-1522, 2009.

[35] T. Kousksou, P. Bruel, A. Jamil, T. El Rhafiki, and Y. Zeraouli, “Energy storage: Applications and challenges,” *Solar Energy Materials and Solar Cells*, vol. 120, pp. 59-80, 2014.

[36] Y. Xia, H. Takeshige, H. Noguchi, and M. Yoshio, “Studies on an Li・ Mn・ O spinel system (obtained by melt-impregnation) as a cathode for 4 V lithium batteries part 1. Synthesis and electrochemical behaviour of LixMn2O4,” *Journal of power sources*, vol. 56, no. 1, pp. 61-67, 1995.

[37] J.-M. Tarascon, and M. Armand, "Issues and challenges facing rechargeable lithium batteries," *Materials For Sustainable Energy: A Collection of Peer-Reviewed Research and Review Articles from Nature Publishing Group*, pp. 171-179: World Scientific, 2011.

[38] D. Geiling, “Project Description,” 2010.

[39] E. Telaretti, G. Graditi, M. Ippolito, and G. Zizzo, “Economic feasibility of stationary electrochemical storages for electric bill management applications: the Italian scenario,” *Energy Policy*, vol. 94, pp. 126-137, 2016.

[40] Sandia. "DOE global energy storage database," 20/01/2018, 2018; http://www.energystorageexchange.org.

[41] R. Lasseter, A. Akhil, C. Marnay, J. Stephens, J. Dagle, R. Guttromson, A. Meliopoulous, R. Yinger, and J. Eto, “The CERTS microgrid concept,” *White paper for Transmission Reliability Program, Office of Power Technologies, US Department of Energy*, vol. 2, no. 3, pp. 30, 2002.

[42] X. Li, D. Hui, M. Xu, L. Wang, G. Guo, and L. Zhang, "Integration and energy management of large-scale lithium-ion battery energy storage station." pp. 1-6.

[43] G. Strbac, I. Konstantelos, and P. Djapic, “Smarter Network Storage.”

[44] T. Feehall, A. Forsyth, R. Todd, M. Foster, D. Gladwin, D. Stone, and D. Strickland, "Battery energy storage systems for the electricity grid: UK research facilities."

[45] R. Spotnitz, “Scale-Up of Lithium-Ion Cells and Batteries,” *Advances in Lithium-Ion Batteries*, pp. 433-457, 2002.

[46] K. Rumpf, M. Naumann, and A. Jossen, “Experimental investigation of parametric cell-to-cell variation and correlation based on 1100 commercial lithium-ion cells,” *Journal of Energy Storage,* vol. 14, pp. 224-243, 2017.

[47] B. Kenney, K. Darcovich, D. D. MacNeil, and I. J. Davidson, “Modelling the impact of variations in electrode manufacturing on lithium-ion battery modules,” *Journal of Power Sources,* vol. 213, pp. 391-401, 2012.

[48] T. Bruen, and J. Marco, “Modelling and experimental evaluation of parallel connected lithium ion cells for an electric vehicle battery system,” *Journal of Power Sources,* vol. 310, pp. 91-101, 2016.

[49] T. Baumhöfer, M. Brühl, S. Rothgang, and D. U. Sauer, “Production caused variation in capacity aging trend and correlation to initial cell performance,” *Journal of Power Sources,* vol. 247, pp. 332-338, 2014.

[50] S. Paul, C. Diegelmann, H. Kabza, and W. Tillmetz, “Analysis of ageing inhomogeneities in lithium-ion battery systems,” *Journal of Power Sources,* vol. 239, pp. 642-650, 2013.

[51] N. Yang, X. Zhang, B. Shang, and G. Li, “Unbalanced discharging and aging due to temperature differences among the cells in a lithium-ion battery pack with parallel combination,” *Journal of Power Sources,* vol. 306, pp. 733-741, 2016.

[52] S. Miyatake, Y. Susuki, T. Hikihara, S. Itoh, and K. Tanaka, “Discharge characteristics of multicell lithium-ion battery with nonuniform cells,” *Journal of Power Sources,* vol. 241, pp. 736-743, 2013.

[53] G. J. Offer, V. Yufit, D. A. Howey, B. Wu, and N. P. Brandon, “Module design and fault diagnosis in electric vehicle batteries,” *Journal of Power Sources,* vol. 206, pp. 383-392, 2012.

[54] L. Wang, Y. Cheng, and X. Zhao, “A LiFePO4 battery pack capacity estimation approach considering in-parallel cell safety in electric vehicles,” *Applied Energy,* vol. 142, pp. 293-302, 2015.

[55] M. J. Brand, M. H. Hofmann, M. Steinhardt, S. F. Schuster, and A. Jossen, “Current distribution within parallel-connected battery cells,” *Journal of Power Sources,* vol. 334, pp. 202-212, 2016.

[56] T. Dragičević, J. M. Guerrero, J. C. Vasquez, and D. Škrlec, “Supervisory control of an adaptive-droop regulated DC microgrid with battery management capability,” *IEEE Transactions on Power Electronics,* vol. 29, no. 2, pp. 695-706, 2014.

[57] M. T. Lawder, B. Suthar, P. W. Northrop, S. De, C. M. Hoff, O. Leitermann, M. L. Crow, S. Santhanagopalan, and V. R. Subramanian, "Battery energy storage system (BESS) and battery management system (BMS) for grid-scale applications," *Proceedings of the IEEE,* vol. 102, no. 6, pp. 1014-1030, 2014.

[58] K. S. Ng, C.-S. Moo, Y.-P. Chen, and Y.-C. Hsieh, "Enhanced coulomb counting method for estimating state-of-charge and state-of-health of lithium-ion batteries," *Applied energy,* vol. 86, no. 9, pp. 1506-1511, 2009.

[59] M. Hannan, M. Lipu, A. Hussain, and A. Mohamed, "A review of lithium-ion battery state of charge estimation and management system in electric vehicle applications: Challenges and recommendations," *Renewable and Sustainable Energy Reviews,* vol. 78, pp. 834-854, 2017.

[60] I. Snihir, W. Rey, E. Verbitskiy, A. Belfadhel-Ayeb, and P. H. Notten, "Battery open-circuit voltage estimation by a method of statistical analysis," *Journal of Power Sources,* vol. 159, no. 2, pp. 1484-1487, 2006.

[61] L. Zheng, L. Zhang, J. Zhu, G. Wang, and J. Jiang, "Co-estimation of state-of-charge, capacity and resistance for lithium-ion batteries based on a high-fidelity electrochemical model," *Applied Energy,* vol. 180, pp. 424-434, 2016.

[62] R. Klein, N. A. Chaturvedi, J. Christensen, J. Ahmed, R. Findeisen, and A. Kojic, "Electrochemical model based observer design for a lithium-ion battery," *IEEE Transactions on Control Systems Technology,* vol. 21, no. 2, pp. 289-301, 2013.

[63] V. Ramadesigan, P. W. Northrop, S. De, S. Santhanagopalan, R. D. Braatz, and V. R. Subramanian, "Modeling and simulation of lithium-ion batteries from a systems engineering perspective," *Journal of The Electrochemical Society,* vol. 159, no. 3, pp. R31-R45, 2012.

[64] M. B. Pinson, and M. Z. Bazant, "Theory of SEI formation in rechargeable batteries: capacity fade, accelerated aging and lifetime prediction," *Journal of the Electrochemical Society,* vol. 160, no. 2, pp. A243-A250, 2013.

[65] M. Guo, G. Sikha, and R. E. White, "Single-particle model for a lithium-ion cell: Thermal behavior," *Journal of The Electrochemical Society,* vol. 158, no. 2, pp. A122-A132, 2011.

[66] R. C. Kroeze, and P. T. Krein, "Electrical battery model for use in dynamic electric vehicle simulations." pp. 1336-1342.

[67] M. Chen, and G. A. Rincon-Mora, “Accurate electrical battery model capable of predicting runtime and IV performance,” *IEEE Trans. Energy Convers.,* vol. 21, no. 2, pp. 504-511, 2006.

[68] I.-S. Kim, “A technique for estimating the state of health of lithium batteries through a dual-sliding-mode observer,” *IEEE Transactions on Power Electronics,* vol. 25, no. 4, pp. 1013-1022, 2010.

[69] M. A. Roscher, and D. U. Sauer, “Dynamic electric behavior and open-circuit-voltage modeling of LiFePO 4-based lithium ion secondary batteries,” *Journal of Power Sources,* vol. 196, no. 1, pp. 331-336, 2011.

[70] H. Rahimi-Eichi, F. Baronti, and M.-Y. Chow, "Modeling and online parameter identification of Li-Polymer battery cells for SOC estimation." pp. 1336-1341.

[71] H. Rahimi-Eichi, and M.-Y. Chow, "Adaptive parameter identification and State-of-Charge estimation of lithium-ion batteries." pp. 4012-4017.

[72] G. L. Plett, “Extended Kalman filtering for battery management systems of LiPB-based HEV battery packs: Part 2. Modeling and identification,” *Journal of Power Sources,* vol. 134, no. 2, pp. 262-276, 2004.

[73] W. Zhang, W. Shi, and Z. Ma, “Adaptive unscented Kalman filter based state of energy and power capability estimation approach for lithium-ion battery,” *Journal of Power Sources,* vol. 289, pp. 50-62, 2015.

[74] M. Mastali, J. Vazquez-Arenas, R. Fraser, M. Fowler, S. Afshar, and M. Stevens, “Battery state of the charge estimation using Kalman filtering,” *Journal of Power Sources,* vol. 239, pp. 294-307, 2013.

[75] I.-S. Kim, “Nonlinear state of charge estimator for hybrid electric vehicle battery,” *IEEE Transactions on Power Electronics,* vol. 23, no. 4, pp. 2027-2034, 2008.

[76] X. Chen, W. Shen, Z. Cao, and A. Kapoor, “A novel approach for state of charge estimation based on adaptive switching gain sliding mode observer in electric vehicles,” *Journal of Power Sources,* vol. 246, pp. 667-678, 2014.

[77] M. Charkhgard, and M. Farrokhi, “State-of-charge estimation for lithium-ion batteries using neural networks and EKF,” *IEEE Trans. Ind. Electron.,* vol. 57, no. 12, pp. 4178-4187, 2010.

[78] I.-H. Li, W.-Y. Wang, S.-F. Su, and Y.-S. Lee, “A merged fuzzy neural network and its applications in battery state-of-charge estimation,” *IEEE Transactions on energy conversion,* vol. 22, no. 3, pp. 697-708, 2007.

[79] P. Singh, R. Vinjamuri, X. Wang, and D. Reisner, “Design and implementation of a fuzzy logic-based state-of-charge meter for Li-ion batteries used in portable defibrillators,” *Journal of Power Sources,* vol. 162, no. 2, pp. 829-836, 2006.

[80] W. Shen, C. C. Chan, E. W. Lo, and K. Chau, “Adaptive neuro-fuzzy modeling of battery residual capacity for electric vehicles,” *IEEE Transactions on Industrial Electronics,* vol. 49, no. 3, pp. 677-684, 2002.

[81] F. Baronti, R. Roncella, and R. Saletti, “Performance comparison of active balancing techniques for lithium-ion batteries,” *Journal of Power Sources,* vol. 267, pp. 603-609, 2014.

[82] J. Gallardo-Lozano, E. Romero-Cadaval, M. I. Milanes-Montero, and M. A. Guerrero-Martinez, “Battery equalization active methods,” *Journal of Power Sources,* vol. 246, pp. 934-949, 2014.

[83] M. Daowd, N. Omar, P. Van Den Bossche, and J. Van Mierlo, "Passive and active battery balancing comparison based on MATLAB simulation." pp. 1-7.

[84] Z. Zhang, H. Gui, D.-J. Gu, Y. Yang, and X. Ren, “A hierarchical active balancing architecture for lithium-ion batteries,” *IEEE Trans. Power Electron.,* vol. 32, no. 4, pp. 2757-2768, 2017.

[85] Y. Yuanmao, K. Cheng, and Y. Yeung, “Zero-current switching switched-capacitor zero-voltage-gap automatic equalization system for series battery string,” *IEEE transactions on power electronics,* vol. 27, no. 7, pp. 3234-3242, 2012.

[86] B. Dong, Y. Li, and Y. Han, “Parallel architecture for battery charge equalization,” *IEEE Transactions on Power Electronics,* vol. 30, no. 9, pp. 4906-4913, 2015.

[87] Y.-S. Lee, and M.-W. Cheng, “Intelligent control battery equalization for series connected lithium-ion battery strings,” *IEEE Transactions on Industrial electronics,* vol. 52, no. 5, pp. 1297-1307, 2005.

[88] F. Baronti, G. Fantechi, R. Roncella, and R. Saletti, “High-efficiency digitally controlled charge equalizer for series-connected cells based on switching converter and super-capacitor,” *IEEE Transactions on Industrial Informatics,* vol. 9, no. 2, pp. 1139-1147, 2013.

[89] S. Yarlagadda, T. T. Hartley, and I. Husain, “A battery management system using an active charge equalization technique based on a DC/DC converter topology,” *IEEE Transactions on Industry Applications,* vol. 49, no. 6, pp. 2720-2729, 2013.

[90] Y. Shang, C. Zhang, N. Cui, and J. M. Guerrero, “A cell-to-cell battery equalizer with zero-current switching and zero-voltage gap based on quasi-resonant LC

converter and boost converter," *IEEE Transactions on Power Electronics,* vol. 30, no. 7, pp. 3731-3747, 2015.

[91] T. Anno, and H. Koizumi, "Double-input bidirectional DC/DC converter using cell-voltage equalizer with flyback transformer," *IEEE Transactions on Power Electronics,* vol. 30, no. 6, pp. 2923-2934, 2015.

[92] D. Frost, and D. Howey, "Completely decentralised active balancing battery management system," *IEEE Trans. Power Electron.,* 2017.

[93] Y. Li, and Y. Han, "A Module-Integrated Distributed Battery Energy Storage and Management System," *IEEE Trans. Power Electron.,* vol. 31, no. 12, pp. 8260-8270, 2016.

[94] T. Morstyn, M. Momayyezan, B. Hredzak, and V. G. Agelidis, "Distributed Control for State-of-Charge Balancing Between the Modules of a Reconfigurable Battery Energy Storage System," *IEEE Trans. Power Electron.,* vol. 31, no. 11, pp. 7986-7995, 2016.

[95] S. Ci, N. Lin, and D. Wu, "Reconfigurable battery techniques and systems: A survey," *IEEE Access,* vol. 4, pp. 1175-1189, 2016.

[96] A. Manenti, A. Abba, A. Merati, S. M. Savaresi, and A. Geraci, "A new BMS architecture based on cell redundancy," *IEEE Trans. Ind. Electron.,* vol. 58, no. 9, pp. 4314-4322, 2011.

[97] H. Rahimi-Eichi, U. Ojha, F. Baronti, and M.-Y. Chow, "Battery management system: an overview of its application in the smart grid and electric vehicles," *Industrial Electronics Magazine, IEEE,* vol. 7, no. 2, pp. 4-16, 2013.

[98] W. C. Lee, D. Drury, and P. Mellor, "Comparison of passive cell balancing and active cell balancing for automotive batteries." pp. 1-7.

[99] C. Pinto, J. V. Barreras, E. Schaltz, and R. E. Araújo, "Evaluation of Advanced Control for Li-ion Battery Balancing Systems Using Convex Optimization," *IEEE Trans. Sustain. Energy,* vol. 7, no. 4, pp. 1703-1717, 2016.

[100] M. Caspar, T. Eiler, and S. Hohmann, "Systematic Comparison of Active Balancing: A Model-based Quantitative Analysis," *IEEE Trans. Veh. Technol.,* 2016.

[101] X. Kong, Y. Zheng, M. Ouyang, X. Li, L. Lu, J. Li, and Z. Zhang, "Signal synchronization for massive data storage in modular battery management system with controller area network," *Applied Energy,* vol. 197, pp. 52-62, 2017.

[102] S. Steinhorst, Z. Shao, S. Chakraborty, M. Kauer, S. Li, M. Lukasiewycz, S. Narayanaswamy, M. U. Rafique, and Q. Wang, "Distributed reconfigurable battery system management architectures." pp. 429-434.

[103] H. Kim, and K. G. Shin, "DESA: Dependable, efficient, scalable architecture for management of large-scale batteries," *IEEE Trans. Ind. Informat.,* vol. 8, no. 2, pp. 406-417, 2012.

[104] S. Narayanaswamy, M. Kauer, S. Steinhorst, M. Lukasiewycz, and S. Chakraborty, "Modular Active Charge Balancing for Scalable Battery Packs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.,* vol. 25, no. 3, pp. 974-987, 2017.

[105] C. R. Birkl, D. F. Frost, A. M. Bizeray, R. R. Richardson, and D. A. Howey, "Modular converter system for low-cost off-grid energy storage using second life li-ion batteries." pp. 192-199.

[106] M. Bragard, N. Soltau, S. Thomas, and R. W. De Doncker, "The balance of renewable sources and user demands in grids: Power electronics for modular battery energy storage systems," *IEEE Transactions on Power Electronics,* vol. 25, no. 12, pp. 3049-3056, 2010.

[107] G. Wang, G. Konstantinou, C. D. Townsend, J. Pou, S. Vazquez, G. D. Demetriades, and V. G. Agelidis, "A review of power electronics for grid connection of utility-scale battery energy storage systems," *IEEE Trans. Sustain. Energy,* vol. 7, no. 4, pp. 1778-1790, 2016.

[108] W. Huang, and J. A. Abu Qahouq, "Energy sharing control scheme for state-of-charge balancing of distributed battery energy storage system," *IEEE Trans. Ind. Electron.,* vol. 62, no. 5, pp. 2764-2776, 2015.

[109] V. Fernão Pires, E. Romero-Cadaval, D. Vinnikov, I. Roasto, and J. F. Martins, "Power converter interfaces for electrochemical energy storage systems – A review," *Energy Conversion and Management,* vol. 86, no. 0, pp. 453-475, 10//, 2014.

[110] R. M. Schupbach, and J. C. Balda, "Comparing DC-DC converters for power management in hybrid electric vehicles." pp. 1369-1374.

[111] S. Inoue, and H. Akagi, "A bidirectional DC–DC converter for an energy storage system with galvanic isolation," *IEEE Transactions on Power Electronics,* vol. 22, no. 6, pp. 2299-2306, 2007.

[112] J. I. Y. Ota, T. Sato, and H. Akagi, "Enhancement of Performance, Availability, and Flexibility of a Battery Energy Storage System Based on a Modular Multilevel

Cascaded Converter (MMCC-SSBC)," *IEEE Trans. Power Electron.* , vol. 31, no. 4, pp. 2791-2799, 2016.

[113] F. Baronti, G. Fantechi, R. Roncella, and R. Saletti, "Design of a module switch for battery pack reconfiguration in high-power applications." pp. 1330-1335.

[114] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on industry applications*, no. 5, pp. 518-523, 1981.

[115] T. Meynard, and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters." pp. 397-403.

[116] H. Patel, and R. Hoft, "Generalized harmonic elimination and voltage control in thyristor converters: Part II–voltage control technique," *IEEE Transactions on Industry Applications,* vol. 10, pp. 666-673, 1974.

[117] T. Soong, and P. W. Lehn, "Evaluation of emerging modular multilevel converters for BESS applications," *IEEE Transactions on Power Delivery,* vol. 29, no. 5, pp. 2086-2094, 2014.

[118] M. Vasiladiotis, and A. Rufer, "Analysis and control of modular multilevel converters with integrated battery energy storage," *IEEE Trans. Power Electron.,* vol. 30, no. 1, pp. 163-175, 2015.

[119] I. Trintis, S. Munk-Nielsen, and R. Teodorescu, "A new modular multilevel converter with integrated energy storage." pp. 1075-1080.

[120] M. Vasiladiotis, N. Cherix, and A. Rufer, "Impact of grid asymmetries on the operation and capacitive energy storage design of modular multilevel converters," *IEEE Transactions on Industrial Electronics,* vol. 62, no. 11, pp. 6697-6707, 2015.

[121] L.-R. Chen, S.-L. Wu, D.-T. Shieh, and T.-R. Chen, "Sinusoidal-ripple-current charging strategy and optimal charging frequency study for Li-ion batteries," *IEEE Transactions on Industrial Electronics,* vol. 60, no. 1, pp. 88-97, 2013.

[122] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," *IEEE Transactions on Industrial Electronics,* vol. 53, no. 5, pp. 1512-1521, 2006.

[123] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "State-of-charge (SOC)-balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Trans. Power Electron.,* vol. 24, no. 6, pp. 1628-1636, 2009.

[124] L. Maharjan, T. Yamagishi, and H. Akagi, “Active-power control of individual converter cells for a battery energy storage system based on a multilevel cascade PWM converter,” *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1099-1107, 2012.

[125] N. Kawakami, S. Ota, H. Kon, S. Konno, H. Akagi, H. Kobayashi, and N. Okada, “Development of a 500-kW Modular Multilevel Cascade Converter for Battery Energy Storage Systems,” *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 3902-3910, 2014.

[126] L. Baruschka, and A. Mertens, "Comparison of cascaded H-bridge and modular multilevel converters for BESS application." pp. 909-916.

[127] C. A. Ooi, D. Rogers, and N. Jenkins, “Balancing control for grid-scale battery energy storage system,” *Proceedings of the Institution of Civil Engineers-Energy*, vol. 168, no. 2, pp. 145-157, 2015.

[128] M. Arifujjaman, “A comprehensive power loss, efficiency, reliability and cost calculation of a 1 MW/500 kWh battery based energy storage system for frequency regulation application,” *Renewable Energy*, vol. 74, pp. 158-169, 2015.

[129] C.-M. Young, N.-Y. Chu, L.-R. Chen, Y.-C. Hsiao, and C.-Z. Li, “A single-phase multilevel inverter with battery balancing,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1972-1978, 2013.

[130] E. Chatzinikolaou, and D. J. Rogers, “Cell SoC Balancing Using a Cascaded Full-Bridge Multilevel Converter in Battery Energy Storage Systems,” *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5394-5402, 2016.

[131] E. Chatzinikolaou, and D. Rogers, “Performance evaluation of duty cycle balancing in power electronics enhanced battery packs compared to conventional energy redistribution balancing,” *IEEE Transactions on Power Electronics*, 2018.

[132] E. Chatzinikolaou, and D. J. Rogers, “A Comparison of Grid-connected Battery Energy Storage System Designs,” *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6913-6923, 2016.

[133] E. Chatzinikolaou, and D. J. Rogers, “Hierarchical Distributed Balancing Control for Large-Scale Reconfigurable AC Battery Packs,” *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5592-5602, 2018.

[134] M. Vasiladiotis, and A. Rufer, "Balancing control actions for cascaded H-bridge converters with integrated battery energy storage." pp. 1-10.

[135] M. Chen, B. Zhang, Y. Li, G. Qi, and J. Liu, "Design of a multi-level battery management system for a Cascade H-bridge energy storage system." pp. 1-5.

[136] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*

, vol. 57, no. 7, pp. 2197-2206, 2010.

[137] G. S. Konstantinou, M. Ciobotaru, and V. G. Agelidis, "Analysis of multi-carrier PWM methods for back-to-back HVDC systems based on modular multilevel converters." pp. 4391-4396.

[138] M. Saeedifard, and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Transactions on power delivery,* vol. 25, no. 4, pp. 2903-2912, 2010.

[139] N. Celanovic, and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Transactions on industry applications,* vol. 37, no. 2, pp. 637-641, 2001.

[140] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proceedings of the IEEE,* vol. 97, no. 11, pp. 1786-1817, 2009.

[141] A. K. Gupta, and A. M. Khambadkone, "A space vector PWM scheme for multilevel inverters based on two-level space vector PWM," *IEEE Transactions on industrial electronics,* vol. 53, no. 5, pp. 1631-1639, 2006.

[142] W. Yao, H. Hu, and Z. Lu, "Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter," *IEEE transactions on Power Electronics,* vol. 23, no. 1, pp. 45-51, 2008.

[143] K. Sundareswaran, K. Jayant, and T. Shanavas, "Inverter harmonic elimination through a colony of continuously exploring ants," *IEEE Transactions on Industrial Electronics,* vol. 54, no. 5, pp. 2558-2565, 2007.

[144] S. Tong, M. P. Klein, and J. W. Park, "On-line optimization of battery open circuit voltage for improved state-of-charge and state-of-health estimation," *Journal of Power Sources,* vol. 293, pp. 416-428, 2015.

[145] Y. Xing, W. He, M. Pecht, and K. L. Tsui, "State of charge estimation of lithium-ion batteries using the open-circuit voltage at various ambient temperatures," *Applied Energy,* vol. 113, pp. 106-115, 2014.

[146] C. Fleischer, W. Waag, H.-M. Heyn, and D. U. Sauer, "On-line adaptive battery impedance parameter and state estimation considering physical principles in reduced order equivalent circuit battery models: Part 1. Requirements, critical review of methods and modeling," *Journal of Power Sources,* vol. 260, pp. 276-291, 2014.

[147] G. K. Prasad, and C. D. Rahn, "Model based identification of aging parameters in lithium ion batteries," *Journal of Power Sources,* vol. 232, pp. 79-85, 2013.

[148] J.-H. Lee, and W. Choi, "Novel state-of-charge estimation method for lithium polymer batteries using electrochemical impedance spectroscopy," *Journal of Power Electronics,* vol. 11, no. 2, pp. 237-243, 2011.

[149] X. Hu, S. Li, and H. Peng, "A comparative study of equivalent circuit models for Li-ion batteries," *Journal of Power Sources,* vol. 198, pp. 359-367, 2012.

[150] J. Li, and M. S. Mazzola, "Accurate battery pack modeling for automotive applications," *Journal of Power Sources,* vol. 237, pp. 215-228, 2013.

[151] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "Improved PLL structures for single-phase grid inverters," *Proc. of PELINCEC,* vol. 5, no. 6, 2005.

[152] M. Hoque, M. Hannan, A. Mohamed, and A. Ayob, "Battery charge equalization controller in electric vehicle applications: A review," *Renewable and Sustainable Energy Reviews,* 2016.

[153] O. L. Mangasarian, "Uniqueness of solution in linear programming," *Linear algebra and its applications,* vol. 25, pp. 151-162, 1979.

[154] 2017; https://www.plexim.com/plecs.

[155] A. Ristow, M. Begović, A. Pregelj, and A. Rohatgi, "Development of a methodology for improving photovoltaic inverter reliability," *IEEE Trans. Ind. Electron.,* vol. 55, no. 7, pp. 2581-2592, 2008.

[156] S. V. Dhople, A. Davoudi, A. D. Domínguez-García, and P. L. Chapman, "A unified approach to reliability assessment of multiphase DC–DC converters in photovoltaic energy conversion systems," *IEEE Trans. Power Electron.,* vol. 27, no. 2, pp. 739-751, 2012.

[157] E. Kostandyan, and K. Ma, "Reliability estimation with uncertainties consideration for high power IGBTs in 2.3 MW wind turbine converter system," *Microelectronics Reliability,* vol. 52, no. 9, pp. 2403-2408, 2012.

[158] C. Busca, R. Teodorescu, F. Blaabjerg, S. Munk-Nielsen, L. Helle, T. Abeyasekera, and P. Rodriguez, "An overview of the reliability prediction related aspects of high power IGBTs in wind power applications," *Microelectronics Reliability*, vol. 51, no. 9, pp. 1903-1907, 2011.

[159] M. Boettcher, J. Reese, and F. W. Fuchs, "Reliability comparison of fault-tolerant 3L-NPC based converter topologies for application in wind turbine systems." pp. 1223-1229.

[160] C. W. Zhang, T. Zhang, N. Chen, and T. Jin, "Reliability modeling and analysis for a novel design of modular converter system of wind turbines," *Reliability Engineering & System Safety*, vol. 111, pp. 86-94, 2013.

[161] B. Abdi, A. H. Ranjbar, G. B. Gharehpetian, and J. Milimonfared, "Reliability considerations for parallel performance of semiconductor switches in high-power switching power supplies," *IEEE Trans. Ind. Electron.* , vol. 56, no. 6, pp. 2133-2139, 2009.

[162] U. S. o. A. D. o. Defense, *Military Handbook: Reliability Prediction of Electronic Equipment: MIL-HDBK-217F: 2 December 1991*: Department of defense, 1991.

[163] C. Patsios, B. Wu, E. Chatzinikolaou, D. J. Rogers, N. Wade, N. P. Brandon, and P. Taylor, "An integrated approach for the analysis and control of grid connected energy storage systems," *Journal of Energy Storage*, vol. 5, pp. 48-61, 2016.

[164] G. Kalcon, G. P. Adam, O. Anaya-Lara, G. Burt, and K. Lo, "Analytical efficiency evaluation of two and three level VSC-HVDC transmission links," *International Journal of Electrical Power & Energy Systems*, vol. 44, no. 1, pp. 1-6, 2013.

[165] D. Graovac, M. Purschel, and A. Kiep, "MOSFET power losses calculation using the data-sheet parameters," *Infineon application note*, vol. 1, 2006.

[166] "Schneider Electric," 09/09/2016; http://mt.schneider-electric.be/Main/tfo/catalogue/an_IEC.pdf.

[167] L. Wu, J. Qin, M. Saeedifard, O. Wasynczuk, and K. Shenai, "Efficiency evaluation of the modular multilevel converter based on Si and SiC switching devices for medium/high-voltage applications," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 286-293, 2015.

[168] J. Zhang, S. Ci, H. Sharif, and M. Alahmad, "Modeling discharge behavior of multicell battery," *IEEE Trans. Energy Convers.*, vol. 25, no. 4, pp. 1133-1141, 2010.

[169] M. Held, and K. Fritz, “Comparison and evaluation of newest failure rate prediction models: FIDES and RIAC 217Plus,” *Microelectronics Reliability,* vol. 49, no. 9, pp. 967-971, 2009.

[170] X. Liu, J. Zou, and X. Zhang, "Investigations on the reliability of storage battery array with high capability." pp. 735-737.

[171] N. Mukherjee, and D. Strickland, "Second life battery energy storage systems: Converter topology and redundancy selection." pp. 1-6.

[172] M. Ecker, J. B. Gerschler, J. Vogel, S. Käbitz, F. Hust, P. Dechent, and D. U. Sauer, “Development of a lifetime prediction model for lithium-ion batteries based on extended accelerated aging test data,” *Journal of Power Sources,* vol. 215, pp. 248-257, 2012.

[173] S.-W. Eom, M.-K. Kim, I.-J. Kim, S.-I. Moon, Y.-K. Sun, and H.-S. Kim, “Life prediction and reliability assessment of lithium secondary batteries,” *Journal of Power Sources,* vol. 174, no. 2, pp. 954-958, 2007.

[174] A. Stupar, D. Bortis, U. Drofenik, and J. Kolar, "Advanced setup for thermal cycling of power modules following definable junction temperature profiles." pp. 962-969.

[175] J. W. Aquilino, “Report of transformer reliability survey-industrial plants and commercial buildings,” *IEEE Trans. Ind. Appl.,* no. 5, pp. 858-866, 1983.

[176] F. Richardeau, and T. T. L. Pham, “Reliability calculation of multilevel converters: Theory and applications,” *IEEE Trans. Ind. Electron.,* vol. 60, no. 10, pp. 4225-4233, 2013.

[177] B. Zakeri, and S. Syri, “Electrical energy storage systems: A comparative life cycle cost analysis,” *Renewable and Sustainable Energy Reviews,* vol. 42, pp. 569-596, 2015.

[178] R. E. Ciez, and J. Whitacre, “The cost of lithium is unlikely to upend the price of Li-ion storage systems,” *Journal of Power Sources,* vol. 320, pp. 310-313, 2016.

[179] "Mouser Electronics, Inc," 10/05/2016, 2016; http://www.mouser.co.uk/.

[180] H. Dong, X. Jin, Y. Lou, and C. Wang, “Lithium-ion battery state of health monitoring and remaining useful life prediction based on support vector regression-particle filter,” *Journal of power sources,* vol. 271, pp. 114-123, 2014.

[181] S. F. Schuster, M. J. Brand, C. Campestrini, M. Gleissenberger, and A. Jossen, “Correlation between capacity and impedance of lithium-ion cells during calendar and cycle life,” *Journal of Power Sources*, vol. 305, pp. 191-199, 2016.

[182] D. I. Stroe, M. Swierczynski, A. I. Stan, V. Knap, R. Teodorescu, and S. J. Andreasen, "Diagnosis of lithium-ion batteries state-of-health based on electrochemical impedance spectroscopy technique." pp. 4576-4582.

[183] C. Pastor-Fernández, K. Uddin, G. H. Chouchelamane, W. D. Widanage, and J. Marco, “A Comparison between Electrochemical Impedance Spectroscopy and Incremental Capacity-Differential Voltage as Li-ion Diagnostic Techniques to Identify and Quantify the Effects of Degradation Modes within Battery Management Systems,” *Journal of Power Sources,* vol. 360, pp. 301-318, 2017.

[184] Y. Sun, X. Hou, H. Han, Z. Liu, W. Yuan, and M. Su, “A Fully Decentralized Control of Grid-Connected Cascaded Inverters,” *arXiv preprint arXiv:1709.03822*, 2017.

Appendix

Hierarchical Balancing Algorithm

A detailed description of the hierarchical balancing algorithm presented in Chapter 5 is given in the following figure:

