High Performance Pixels for CMOS Image Sensors

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Abstract

Complementary Metal-Oxide Semiconductor (CMOS) image sensors are the principal technology employed in commercial image sensing applications. The research interest in these devices is driven by the high demand of cameras. High-quality imagers are relevant in the mobile devices business and are even more important in the automotive market segment where the image quality is crucial for safety. However, CMOS image sensors performance can still be improved. In particular, a leakage current, intrinsic to the process of manufacturing CMOS technology, reduces the sensitivity in low light and should be minimised. In addition, the capability of the sensor to collect electrons, known as full well capacity, should be maximised.

The methods proposed in the literature to reduce the leakage current and to increase the full well capacity are either insufficient or costly as they may require process modifications. To overcome these limitations, a different approach based on simple layout modifications is proposed. The principal source of leakage current is due to the photodiode isolation. By designing pixels adjacently, the isolation can be removed thereby reducing the leakage current contribution. In order to maximise the full well capacity, a novel technique is proposed here which consist in minimising the area reserved to the transistors in the pixel array by sharing the maximum number of diffusions. The result is a pixel with a 50% increase in fill factor compared to a traditional pixel.

The proposed optimisation strategy results in a staggered pixel arrangement. This may introduce artefacts in the image when displayed. Hardware-efficient image reconstruction algorithms able to correct the artefacts are presented. Test chips were manufactured to prove the performance improvement and experimental data showed that the proposed layouts effectively reduces the leakage current and improved the full well capacity of the presented pixels. In addition, the proposed algorithms are shown to correctly reconstruct and represent the staggered acquired image on a standard display.

to the memory of my father Antonio,

man of knowledge and wisdom.

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Chapter 1

Introduction

The human desire of retaining visual information dates from prehistoric times when the first cave paintings appeared [1]. Painting is a non-ideal form of imaging as it is dependent on the painter's skills. Their techniques were refined over the centuries to reproduce scenes with the highest fidelity. This continuous improvement led to a form of art known as realism [2]. Since the invention of photography, scenes are captured and stored as images by means of a technical solution [3]. Initially, photographs were collected by employing chemical techniques and imprinting the scene on a film. More recently, with the development of electronics and information encoding efficiency, digital imaging replaced films [4]. The two prominent electronic devices employed in commercial cameras are Charge Coupled Devices (CCD) and Complementary Metal Oxide Semiconductor (CMOS) image sensors. The advantages and disadvantages of these technologies have been discussed extensively in the past, with CMOS being the clear winner for its reduced fabrication cost, its low power consumption, and its high integration capability [5, 6].

Presently, a number of CMOS image sensors are present in a variety of devices. These include phones wherein cameras were introduced for the first time on a mobile phone more than fifteen years ago by Sharp [7]. This was a small resolution image sensor with 0.1 Megapixels. Since then, the imaging quality has increased up to 8K video resolution [8]. Moreover, camera modules are present on both the front and the back of modern devices. This is so because pictures and selfies are pushing the demand for high-quality front cameras, and the increased internet bandwidth availability enables the users to instantly share the acquired visual information around the world.

In addition to phones and portable devices, the car industry is another area where the use of images is increasing. In the automotive market segment, self-driving cars are leading the demand for reliable machine vision systems, which will be in the next generation of cars. It is vital for passengers safety to have complete information about the scene surrounding the car. These examples show how the CMOS image sensors market is also expected to continue to grow in the future [9]. With such business opportunities, volumes are rising and leading players are increasing their interest in this industrial sector. The competition is fierce and the industrial research aims to improve imaging performances while reducing the fabrication cost [10].

1.1 Motivation

As CMOS image sensing is a growing market, the interest for higher imaging performances does not belong exclusively to the scientific community but is expanding in the consumer industry as well. As an example, HTC is employing a market differentiation strategy based on low light performances with their UltraPixel camera [11]. Their pixel is larger compared to the market competitors. Therefore, it is capable of collecting more light and to accommodate a higher number of electrons.

Despite all this effort and technological development, CMOS image sensors still suffer from limitations of the imaging performance. In particular, these are the sensor capability of producing images in low light conditions which is due to a leakage current in the devices called the *dark current*. In some fields, such as X-Ray imaging or star observation, the capability to image at low light levels is crucial as the dark current increases with radiation. Moreover, for these applications the typical pixel pitch is between 20 μm and 100 μm [12] allowing the designer to add circuitry at the pixel level. Finally, the large-scale diffusion of CMOS technology allows the manufacturing of higher performance devices with reduced cost.

The literature suggests a number of different approaches, including process modifications [13–16] to improve the imaging quality in low light. However, these are either costly or often not in control of the designer. Other approaches are present in the literature where layout techniques are used to reduce the dark current [17, 18], however, these are insufficient as the fundamental layout techniques are not disclosed. This is surprising giving that the layout has a strong impact on the pixel performance but, unfortunately, companies preserve their trade secrets.

This thesis aims to study and analyse CMOS image sensors and to improve their performances by layout optimisation techniques which can be controlled by the designer. In particular, this work was produced within the European Doctorate in Image Sensing and Optical Nanotechnology (EDISON) project. This is a European Industrial Doctorate (EID) part of the Initial Training Network (ITN) and funded by the European Commission through the FP7 Framework. The EID aims to form researchers in an industrial context. For this reason, half of the doctoral time should be spent in industry. The industry partner for this project is Awaiba (now part of the AMS group), which is a fabless image sensor design house based on the island of Madeira (Portugal). One of the main business interests of Awaiba is producing image sensors for the biomedical sector. Their most famous product, NanEye, is amongst the smallest market available image sensors in the world and was designed for endoscopy applications [19]. Furthermore, within his secondment in Awaiba, the author had the opportunity to collaborate with LFoundry, which is a silicon manufacturing company based in Avezzano (Italy), where, after silicon manufacturing, he spent a year working on the analysis and characterisation of the novel pixel designs. The LFoundry plant in Avezzano used to be an Aptina fab where the production of CMOS image sensors started more than a decade ago. During the time of this project, ONSemi, which acquired Aptina [20] is the fab main customer and utilises the plants for automotive applications image sensors [21].

In 2014, the R&D team in LFoundry were developing a proprietary process technology for CMOS image sensors at the 110 nm node. The partnership with Awaiba was serving the purpose of designing test chip vehicles to define and build the PDK (Process Design Kit) for their process. This enabled the collaboration between a design house and a foundry within a research and development project. In order to gather information about the CMOS pixels and the manufacturing process, a test chip with market standard pixels was required. In exchange for the design of a test vehicle, LFoundry agreed to provide additional free silicon space in order to try new R&D pixel variations. This was a unique opportunity to try the novel research ideas proposed in this thesis and to implement them by discussing with an experienced team of process engineers.

In order to fulfil this objective, an extensive experiment was designed. From a design point of view, nine test chips were designed with a total of 65 pixel variations. From a process point

of view, LFoundry designed a number of processing variations to measure and extract the best performance for their process technology. This thesis is focusing on the work conducted by the author which consisted of the design, the layout and the measurement of the test chips. Not all the variations will be presented as the information generated by these variations is reserved to LFoundry.

All these factors and the unique opportunity to work closely with a Foundry have motivated the study of layout techniques to improve the pixel performance. The two main objectives are to reduce the dark current by using a simple layout modification and to improve the pixel capability of collecting light and electrons by using a novel smart layout arrangement. The next section describes the thesis organisation.

1.2 Organisation

The thesis is organised into Chapters. First, an analysis of the main functional blocks of a CMOS image sensor is conducted in Chapter 2. This Chapter will revisit the main CMOS image sensors parameters and the sources of noise in the sensor. Then, a literature review on the dark current is presented. The causes of dark current in a CMOS image sensor are analysed and previous work on modelling of the dark current as well as techniques to reduce the dark current are reviewed. Many of these techniques require direct access to the process technology, which is risky, costly and often not available to the design companies. The principal pixel architectures are reviewed and analysed these will be useful for the ensuing discussion of the pixel layouts. The chapter concludes with a review of the state of the art of CMOS image sensors. In particular, an analysis on the fill factor, pixel pitch and process technology is undertaken and an effective metric to compare the layout efficiency is proposed, which allows making a comparison between these pixels. In addition, state of the art layouts redrawn from SEM images are presented.

Chapter 3 introduces in detail the design of the experiment and begins by introducing and motivating the layout variations designed within the purpose of this project. It then describes and explains the measurement techniques utilised to extract the main CMOS image sensor parameters and the dark current. After this introduction, the Chapter continues by describing the proposed layout technique to reduce the dark current. In fact, the main source of dark current

comes from the defects introduced during the process manufacturing of the isolation mechanism of the devices. This is known as Shallow Trench Isolation (STI) and a layout technique to remove this source of dark current is presented. The experimental results prove that by removing the interaction of the STI with the photodiode, the dark current could be reduced. In addition, by changing the isolation mechanism, it is possible to design a larger photodiode, which can accommodate a higher number of electrons. The results are analysed and a simple model to predict the dark current with this approach is proposed.

The layout has hence been proven to have an impact on the pixel performance. Chapter 4 revisits the layout techniques and the thought process to generate a pixel layout in CMOS image sensors. Some standard 4T pixel layouts are reviewed and presented. The state of the art shared pixel layout is also presented. However, the core part of this chapter is the introduction of a novel layout technique to maximise the fill factor. This technique consists to place the transistors in the pixel array so that they can share the maximum number of diffusions. In fact, the diffusion-to-diffusion spacing is a wasted space that could be dedicated to the photodiode instead. In the pixels, an optimisation path, defined as the path that maximises the number of diffusion contact sharing, lead to an efficient optimised layout. The experimental results prove that the CMOS parameters, like the capability of the pixel to collect electrons, are improved. However, this technique introduces a slightly different arrangement of the pixels in the matrix which causes them to be ”staggered” as alternate rows are shifted. An algorithm is hence needed to reconstruct the image in a matrix fashion in order to be displayed onto a standard device.

Chapter 5 presents the images acquired by the standard and the novel layout arrangements. Here, the effect of the staggering arrangement of the pixels is discussed and analysed. Three algorithms with increasing hardware complexity are proposed and compared. These can be used as effective ways to reconstruct the image and to display it on a standard device. However, a simple hardware efficient algorithm, which only requires a sum and a division, can suffice to reconstruct the image. In addition, colour images are presented with the proposed algorithms applied also to colour images.

Finally, the thesis is concluded by Chapter 6 which summarises the results of the presented CMOS image sensor pixels. The major results obtained are re-emphasised and compared to the state-of-the-art pixels presented in the literature review of Chapter 2. Moreover, a generalisation

of the layout techniques to other pixel pitches and technologies is presented with diagrams and modelling. This work was conducted within a defined period of time and with many constraints. The limitations of this work are better clarified in a dedicated section. The Chapter ends by presenting possible future work as an outcome of this research.

The Appendix adds more detail to the design of the CMOS image sensor, on the printed circuit board and lists all the 65 pixel variations designed for the purposes of this project, with the ones presented in this thesis highlighted in grey.

Chapter 2

CMOS Image Sensors

This Chapter introduces the topic of this work by reviewing the fundamental principles of the CMOS image sensor operation. The camera is described in 2.1 where building blocks of an imaging system are presented. The focus of the chapter is on the image sensors itself and Section 2.2 starts by describing the physical effect of photogeneration of charges in a p-n junction. Then, the Chapter continues by analysing the main characteristics and limitations. An overview of the parameters and the noise contributions is presented in sections 2.3 and 2.3.3 respectively. In addition, Section 2.5 introduces the principal pixel architectures employed in the sensors and later presented in this thesis while Section 2.6 presents a range of published work in the literature and provides an analysis of commercial pixel layouts. Finally, Section 2.7 concludes the Chapter.

2.1 Camera

In order for an image to be collected, stored and displayed, many functional blocks are needed. An imaging system is usually referred to as a camera. Light rays enter into an optical system and are focused through a lens on the focal plane where the image sensor resides. The amount of light and the direction of the rays are controlled by an adjustable aperture. The image sensor transduces the light information into an analogue electrical information. CMOS image sensors, in particular, generally also convert the information into a digital value which can be transferred to an external image processing unit for elaboration and correction. The corrected image is then ready to be stored or to be displayed on a screen [22].

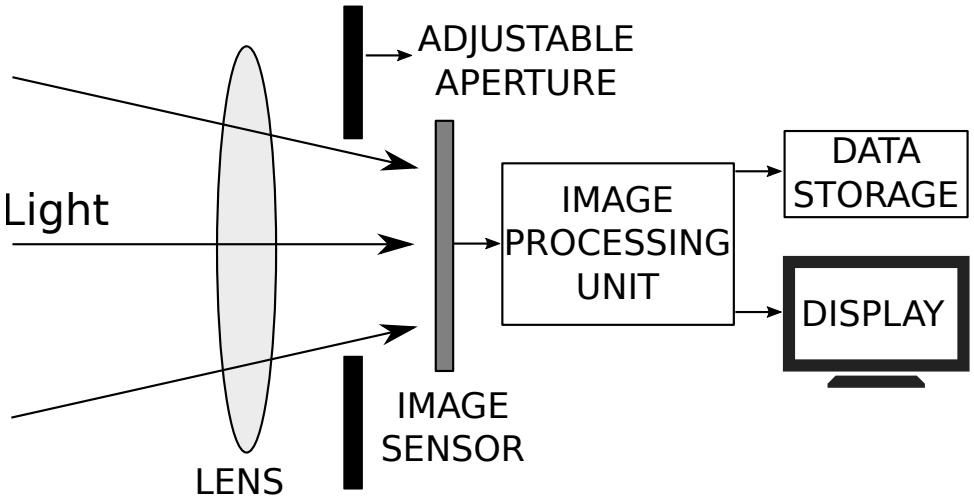


Figure 2.1: Camera system block diagram.

This is a complex system which comprises an optical system, a transducer, an amplifier, an analogue-to-digital converter, a microprocessor and a display. Each of these functional blocks has its own particularities and limitations and is the object of research for the system improvement. This work focuses on the image sensor block of this diagram, which is a mixed-signal device composed of both analogue and digital circuits in CMOS technology. A particular focus is given to the pixels which are the principal elements of an image sensor. In the image sensor, they are organised in a matrix as in Figure 2.2, which illustrates the block diagram of a typical sensor. In each pixel, light is collected and converted into an electrical signal and this information is then transferred to the peripheral circuitry for digital conversion and elaboration. Each pixel is accessible by horizontal and vertical scanners, which select the matrix rows and columns in turn [23].

In Figure 2.2, the vertical scanner selects the first row while the horizontal scanner selects the first column. The analogue value of the selected pixel is read at the output through the highlighted path. Then, a suitable data converter is used to convert the pixel's analogue response into a digital value. This thesis focuses on the design and layout of novel pixels and their performance improvement. Before analysing circuits for imaging and improving their performances, it is worth analysing the physical effect and the metrics of operation.

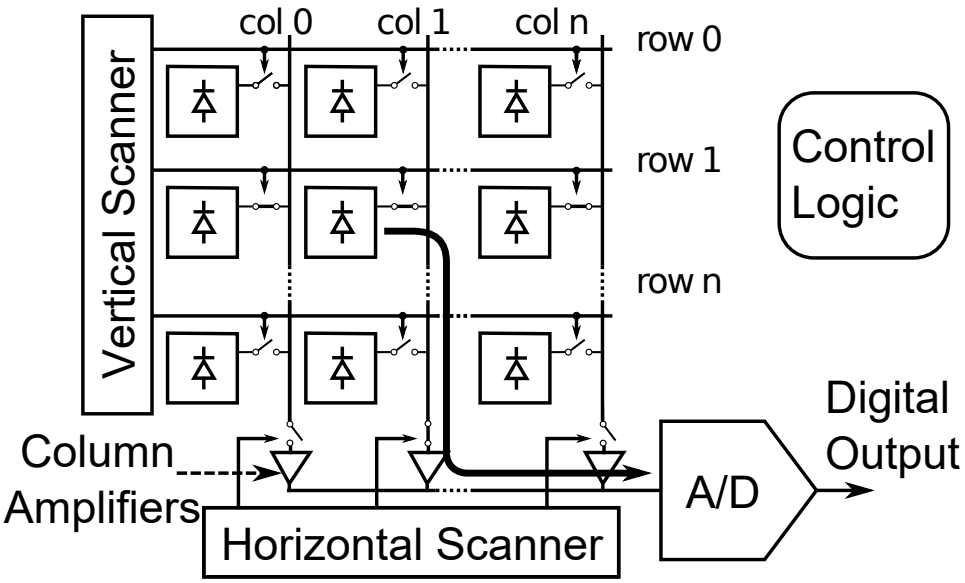


Figure 2.2: CMOS image sensor architecture.

2.2 Physical effect

Silicon is a semiconductor with a bandgap energy of 1.12 eV at room temperature. This is the gap in energy between the valence and conduction bands. At zero Kelvin, the valence band is completely full while the conduction band is empty. When the temperature increases and energy is given to the system, electrons are excited and can jump from the valence band to the conduction band. Another mechanism to excite electrons in the conduction band is when a photon with energy higher than the bandgap hits the Silicon [24].

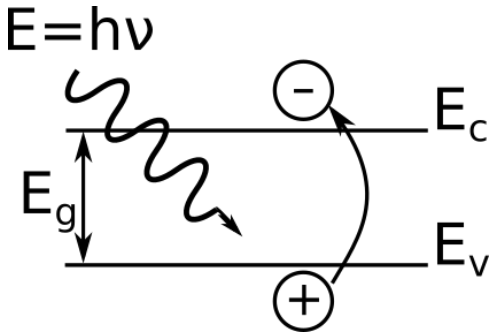


Figure 2.3: Physical effect of a photon hitting Silicon.

In Figure 2.3 this effect is represented visually with the energy diagrams. Here, E_g is the bandgap energy, $E = h\nu$ is the photon energy, E_c and E_v are the conduction and valence band energy levels respectively. Silicon is an indirect band gap semiconductor, which means that the phonon, a quantum of momentum, is also needed in order for the electron-hole pair to be generated. The properties of Silicon make this material sensible to the visible light spectrum and

near infra-red. To collect this charge a p-n junction is used. The electric field of the depletion region pushes holes and electrons toward the p and n regions respectively. Photodiodes are hence p-n junctions usually operating in reverse bias.

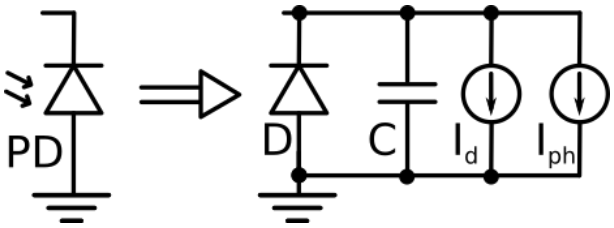


Figure 2.4: Equivalent electrical model of a p-n photodiode in reverse bias.

In this condition, the photodiode can be modelled as in Figure 2.4 where PD is the photodiode, D is an ideal diode, C is the junction capacitance, I_d and I_{ph} are the dark current and the photogenerated current respectively. The total current is hence the sum of the p-n junction leakage current and the contribution related to photogeneration [25].

2.3 CMOS image sensor parameters

An ideal CMOS image sensor would return an electrical signal proportional to the amount of light falling on the device. Unfortunately, this does not happen in reality due to a number of limitations.

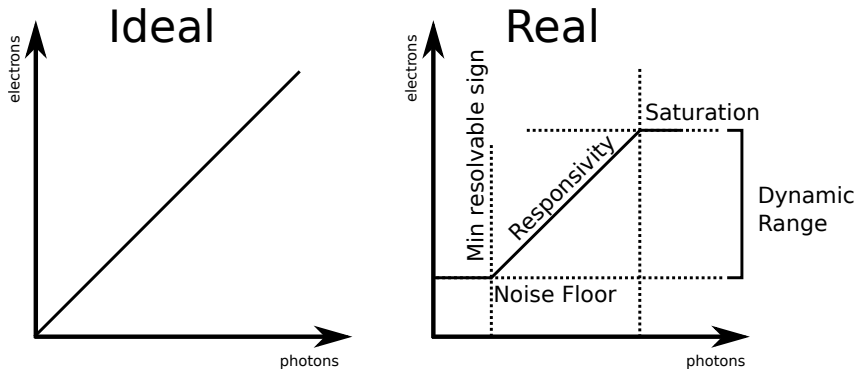


Figure 2.5: Ideal vs real image sensor performance.

Figure 2.5 shows the ideal versus the real image sensor performance. The ideal curve has a direct correspondence between photons and electrons. In the real curve, a noise floor and a minimum resolvable signal limit the performance in low light while the photodiode saturation and a maximum resolvable signal limit the performance in high-light conditions. While the ideal photodiode can accommodate an infinite number of electrons still responding linearly, a

real photodiode can only store a finite number of electrons. This finite number is defined as full well capacity or saturation level [22]. The linear full well capacity is defined as the maximum number of electrons the photodiode can store in a linear region, which equates the saturation level in the example. Real data shows a smooth transition from the linear region to saturation when the saturation level of the ADC is higher than the maximum output signal. Two levels of the full well are defined, a linear full well capacity, which is the maximum number of electrons that the photodiode can accommodate behaving linearly, and a saturation full well capacity, which is the absolute maximum number of electrons that the photodiode can accommodate [26].

The Dynamic Range is the range where the sensor is sensitive to incident photons and it is defined as the ratio between the full well capacity and the noise floor [22] and it can be expressed in dB as:

$$DR = 20\log(\frac{N_{FW}}{n_{floor}}) \tag{2.1}$$

where DR is the dynamic range, N_{FW} is the linear full well capacity and n_{floor} is the noise floor. In an integrating pixel, when the charge is transferred to the floating diffusion, the difference in voltage drop can be expressed as [22]:

$$\Delta V_{FD} = \frac{\Delta Q}{C_{FD}} \tag{2.2}$$

where ΔV_{FD} is the voltage difference on the floating diffusion due to the presence of the photogenerated charge ΔQ and C_{FD} is the floating diffusion junction capacitance. It is worth considering the variation in output voltage per electron, which is defined as the conversion gain [27]:

$$CG = \frac{q}{C_{FD}} \tag{2.3}$$

where CG is the conversion gain and q is the elemental charge. The higher the capacitance the lower the voltage change. This parameter is critical for the pixel sensitivity as a high floating diffusion capacitance would result in a low voltage on the floating diffusion and, on the other side, a small capacitance may not be able to accommodate all the photogenerated electrons. Finally, the responsivity is given by the gain of the curve and it can be defined as the ratio

between the optical input power and the amount of generated electrons [28].

2.3.1 Fill Factor

Typically, a CMOS pixel consists of a photodiode that is sensitive to light. In addition, there are transistors that are not designed to collect light and where light generates an undesired contribution of electron-hole couples. In a pixel design, additional transistors can be added in the pixel itself to improve its functionality. Unfortunately, the introduction of additional circuits at the pixel level has the drawback of reducing the available area of the photodiode.

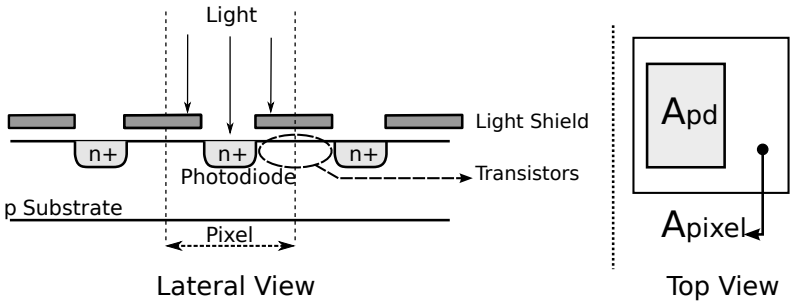


Figure 2.6: Pixel matrix: lateral and top views.

Figure 2.6 shows the lateral and top views of a typical CMOS image sensor. The transistors are usually covered with a metal light shield or by the metal routing of the signals. Only the light fraction that hits the photodiode is useful for the photoconversion while the reflected light does not contribute to it. The *Fill Factor* is a figure of merit typically used to quantify the amount of light that can shine on the photodiode compared to the pixel size. It is defined as the ratio between the photodiode area and the total pixel area as [22]:

$$FF = \frac{A_{pd}}{A_{pixel}} \times 100 \tag{2.4}$$

where A_{pd} is the area of the photodiode and A_{pixel} is the total pixel area. Inserting additional transistors at the pixel level increases the amount of area used for circuitry and, hence, decreases the fill factor. The fill factor depends on the pixel area and can be increased by enlarging the photodiode.

In order to improve the light collection, it is possible to employ small microlenses on top of each pixel [29]. These are usually made of a resin and shaped to focus the light on the photodiode. With this technique, the amount of light that falls on the photodiode is increased

at the cost of additional processing steps [30]. The effect of microlenses is shown in Figure 2.7 where part of the incoming light that would have been reflected is focused on the photodiode. In this case, a higher number of photons are collected and, hence, microlenses mitigate the impact of a pixel with a low fill factor. Unfortunately, a pixel with a smaller photodiode still has less capability to accommodate electrons compared to a larger photodiode.

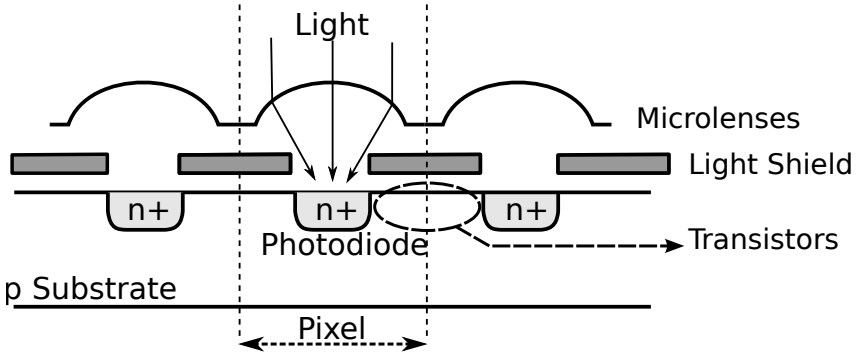


Figure 2.7: Microlenses focusing the light on the photodiode.

2.3.2 Non-Uniformities in CMOS image sensors

In CMOS image sensors, noise impacts the performance by degrading the imaging quality. This image quality degradation can be distinguished as a spatial variation and as a temporal variation. The temporal variation differs from frame-to-frame over time and it is referred to as temporal noise. The spatial variation is referred to as Fixed-Pattern Noise (FPN) as it does not describe noise varying over time but inhomogeneities and mismatch effects and, hence, it can also be referred to as non-uniformity according to the EMVA1288 standard [28]. The signal non-uniformity in the dark is referred to as Dark Signal Non-Uniformity (DSNU), which can be seen as a pattern in the collected dark images of a sensor [31].

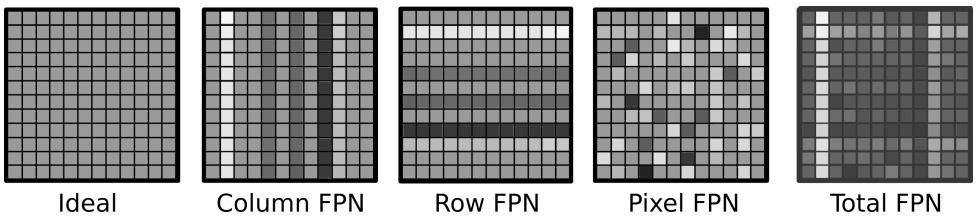


Figure 2.8: Effect of the dark FPN contribution on the ideal image.

Figure 2.8 shows the effect of the fixed pattern noise on an ideal image where the different contributions are highlighted separately. The DSNU is due to the CMOS image sensor itself and to the mismatch effects that occur during its fabrication. In fact, the manufactured MOSFETs

have slightly different geometries from the ideal aspect ratios they were designed for [32, 33]. In addition, the process variability may introduce mismatch in the threshold voltage and in the transistor gain. These differences at the transistor level impact the circuits, translate into different biasing currents or voltage levels and can be visible in the image. The DSNU represents the pixel-to-pixel variation in the signal floor and can be divided into three main components: the column contribution, the row contribution and the pixel contribution. The row and column FPN depend on the periphery rather than the pixel itself and are common along a row or a column, while the pixel FPN is due to the pixel contribution and it varies from pixel-to-pixel.

In the case of spatial differences in illumination conditions, the difference of gain in the response curve is referred to as Photo Response Non-Uniformity (PRNU) [28]. A similar effect to the one of Figure 2.8 appears for a fixed level of illumination. DSNU and PRNU can be represented as the offset and the gain mismatch of pixels within the image sensor. These can be minimised with design techniques and can be corrected with image processing techniques after the sensor is manufactured.

2.3.3 Noise in CMOS image sensors

While the spatial non-uniformities can be corrected with image processing techniques, a deeper analysis is needed for temporal noise. In fact, temporal noise is a true random noise which varies over time and sets limitations to the imaging performance. Three main noise sources can be identified which are the thermal noise, the shot noise and the flicker noise. For the central limit theorem, provided that enough points are collected, any sum of distributions can be estimated as Gaussian. For this reason, temporal noise can be estimated by collecting multiple samples of the signal and its mean and variance can be evaluated [22]. However, each of these noise sources will be evaluated separately.

Thermal noise is due to the kinetic energy of the electrons. In a resistor, its spectral density can be modelled as [34]:

$$S_v(f) = 4kTR \tag{2.5}$$

where $S_v(f)$ is the spectral density in function of the frequency f, k is the Boltzmann's constant, T is the temperature in Kelvin and R is the resistance value. The spectral distribution

of thermal noise is constant in the frequency domain and it is referred to as white noise for this property. When a resistor is connected to a capacitor, thermal noise is stored on it and it is known as *kTC* noise. The thermal fluctuation of charge translates into noise charge that can be expressed as $q = kTC$ where C is the capacitance value, T is the temperature, and k is the Boltzmann constant. In the voltage domain, the root mean square reset noise can be written as $V_n = \sqrt{kT/C}$. This noise appears when the floating diffusion, which can be modelled as a capacitance, is reset and hence it is also known as reset noise. A readout technique, known as correlated double sampling and presented later in this chapter, can be used to remove the reset (*kTC*) noise.

In any electronic system, the quantised nature of the charge leads to electron shot noise. In addition, the quantised nature of light lead to the fundamental limit of an imaging system which is the photon shot noise. This is stochastic and can be described by a Poisson distribution. In fact, for such a distribution, the noise variance is equal to its average value. This is an important property that can be exploited to extract information from a light signal value by knowing the noise variance [22].

Finally, in CMOS image sensors, flicker noise is present in the source follower transistor. It is mainly due to defects in the transistor channel which induce a current fluctuation by trapping and de-trapping charge. Flicker noise is also known as *1/f* noise because its spectral density is proportional to $1/f$ and its contribution is mostly visible at low frequencies while at high frequencies white noise becomes dominant [35].

2.4 Dark current

Ideally, the current should be equal to the photogenerated current in the photodiode. However, at low light levels, the leakage of the diode is comparable to the photogenerated current. In fact, the leakage current exists even in the absence of illumination. Therefore, this undesired leakage contribution is referred to as the dark current [36]. In CMOS technology, the dark current in a p-n junction consists of different components that are due to the thermal generation of charge in the depletion region, to the injection-diffusion at the edges of the depletion region and to the discontinuity at the surface [22]. Figure 2.9 shows a representation of the different sources of dark current in a typical photodiode [36].

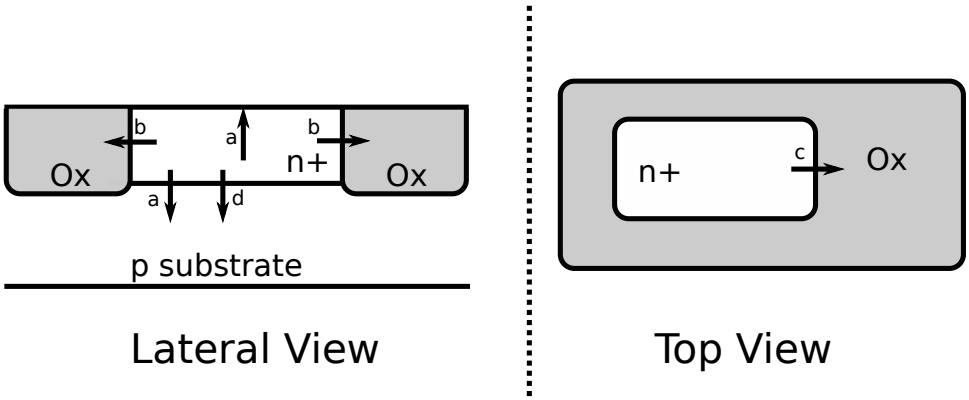


Figure 2.9: Dark current sources in a p-n junction. Lateral and top views. a. thermal generation in the depletion region. b. lateral leakage current. c. surface leakage current. d. injection-diffusion current.

In Figure 2.9, a is the thermal generation-recombination current in the depletion region, b is the lateral leakage current, c is the surface leakage current and d is the injection-diffusion current. One can write a formal expression for the dark current when the junction is biased with a voltage $V \geq 3kT/q$ [37]:

$$J_R \cong q\sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A} + q\frac{n_i}{\tau_{gen}}W \tag{2.6}$$

where D_n is the electron diffusivity, τ_n is the electron lifetime, N_A is the doping level of the p-type region, n_i is the intrinsic concentration of silicon, τ_{gen} is the generation lifetime and W is the depletion width. A similar expression is valid for holes. The first term of this equation is the diffusion current while the second term is the thermal generation current.

2.4.1 Models for dark current

Physical models are useful for an understanding of the dark current but are not practical to deal with from an electronic design perspective. Therefore, empirical approaches have been used to characterise and understand dark current. One such empirical approach assumes that dark current is the sum of three different components as stated in the following equation [38]:

$$I_{dark} = J_1 A + J_2 L + I_3 \tag{2.7}$$

where I is the measured leakage current, J_1 is the current density generated in the bulk, A is the area of the junction in the bulk, J_2 is the linear density current generated at the surface, L

is the depletion length at the surface and I_3 is a current offset. The first term is the leakage from the p-n junction at the surface which is a length-dependent phenomenon. The second term is the current generated in the depletion in the bulk which is area-dependent. The third contribution includes parameters that do not depend on the photodiode geometry as the contact area.

In 4T pixels, which will be introduced later, the contribution of I_3 is not present as the photodiode does not have any contact. In fact, it is accessed through the transfer gate transistor. The surface contribution is due to the discontinuity of the silicon. In fact, dangling bonds are present and one strategy to reduce this contribution is to use a pinned layer to fill the dangling bonds with exceeding charge [39]. The photodiode area A also impacts the dark current. Unfortunately, reducing the area is not always an option as a lower photodiode area translates into a lower full well capacity and less capability of the photodiode of collecting charge. Shscherback *et al.* have postulated the following model for dark current [40]:

$$I_{dark} = \alpha A + \beta n \tag{2.8}$$

where α is a coefficient that determines the junction unity area contribution, n is the number of corners of the photodiode and β is the coefficient that determines the corner contribution to the dark current. This means that in addition to the area of the photodiode also its shape and the number of corners impact the dark current. For these reasons, a good photodiode design is crucial for the dark current reduction.

2.4.2 Dark current reduction techniques

The principal source of parasitic leakage current in CMOS process technology comes from the isolation mechanism used. The two main techniques that provide isolation are Local Oxidation of Silicon (LOCOS) and Shallow Trench Isolation (STI) [41]. Figure 2.10 shows the typical oxide conformation with LOCOS and STI techniques in the section view.

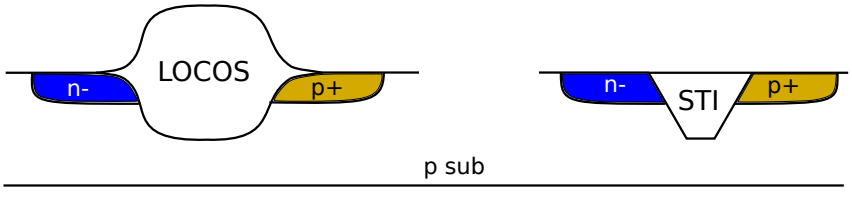


Figure 2.10: LOCOS and STI isolation in CMOS technology.

The main difference between LOCOS and STI is that in LOCOS the insulating structure is larger and, therefore, less area can be used for transistors. In addition, LOCOS requires longer processing time to be manufactured. For these reasons, STI is the most used process to provide isolation in CMOS technology. However, both introduce a high stress into the devices during isolation formation [42, 43]. This causes defects in the structure and, hence, dark current. An effective way to reduce the dark current is to improve the CMOS manufacturing process [13]. To do so, plasma doping has been suggested to be employed around the STI isolation [14] to prevent the interaction of the photodiode and the STI. Moreover, additional stress layers can be employed to reduce defects formation [44]. To reduce the defects at the surface, Hydrogen anneals [45], as well as Fluorine passivation, have been proposed [15]. Furthermore, multi-pinning layers [16], as well as a double buried charge channel (deep-shallow) [46], have also been used to reduce surface-generated dark current. Unfortunately, process optimisation is a very costly approach and often not in control of the designer.

It is possible to reduce the dark current by changing the pixel operation. The leakage current may also come from the transfer gate, which will be better explained in the next section, and solutions were proposed to reduce this contribution. The transfer gate is a transistor and can be biased with a negative voltage to increase the barrier and reduce the leakage current [47]. A ground contact structure close to the transfer gate also reduces the dark current [48]. Recently, an additional n-implant layer underneath the transfer gate was also proposed [49].

The layout has an impact on the dark current performance and it is accessible to the designer. A successful approach to reduce the dark current was presented by McGrath *et al.* where all the nMOS are substituted with pMOS in the pixel [50]. Other layout approaches have been attempted to avoid the interaction of the STI with the photodiode. One possible way is to enclose the photodiode with another layer. As an example it is possible to use the p-well [51] or a polysilicon guard ring [52]. To optimise the pixel layout, the guard ring had a double useful function and was used as a reset transistor also [53]. More advanced techniques, like using a ring-gate shared pixel design enclosed by p-type layers, were also used [18]. Choi *et al.* used a hybrid approach to remove STI around the photodiode by isolating it with a p-well and remaining the STI near the transistors to guarantee their electrical isolation [17]. Their work presents good results in terms of dark current reduction in the case of complete isolation.

However, the isolation between the photodiode and the transistors is achieved thanks to a high spacing which may result in a fill factor loss. In the next Chapter, a hybrid approach where the STI is retained between the transistors and removed on two edges of the photodiode will presented.

2.5 Pixel architectures

Pixels are devices that measure the amount of photogenerated charge and convert it into an analogue voltage. Having explored the parameters, the noise, and the dark current, it is now suitable to consider various architectures.

2.5.1 3T pixel

A simple approach to read the photogenerated current is using a 3T pixel that is a three nMOS Transistor (3T) Active Pixel Sensor (APS), whose schematic is shown in Figure 2.11 [54]. Here, the nMOS transistors, M1 and M3, are switches while M2 is a source follower (SF). M1 is controlled by a digital signal and it is used to reset the photodiode to the supply voltage and, in this thesis, is referred to as Reset transistor. M3 is used to select the row of the pixel, it is controlled by the 'SEL' signal and will be referred to as Row selector. M2 acts as a source follower with its bias provided by a current generator in the column. It is used to buffer the floating diffusion node $n1$ from the output node.

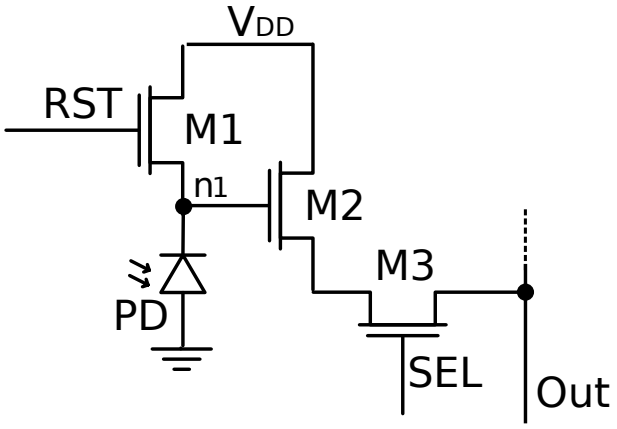


Figure 2.11: 3-transistor active pixel sensor.

Figure 2.12 shows the pixel operation [55]. At the beginning of the frame, the RST signal is set high, which pulls the voltage of the node $n1$ to its reset voltage. The node $n1$ reaches the

reset voltage V_{rst} by time t_1. It is worth noting that the reset voltage V_{rst} of node $n1$ is equal to $Vdd - Vtn$, where V_{tn} is the threshold voltage of the nMOS reset transistor. In order for the node to reach Vdd the reset voltage is usually set higher than Vdd. The RST signal is reduced to zero and the voltage of node $n1$ is equal to the voltage stored on the photodiode capacitance. The incident light on the photodiode discharges the node $n1$ during the integration time for the photoelectric effect. At the time t_2 the output voltage is read out in the column by opening the row selector transistor. The output voltage is proportional to the exposure, which is the amount of light collected by the photodiode during the integration time.

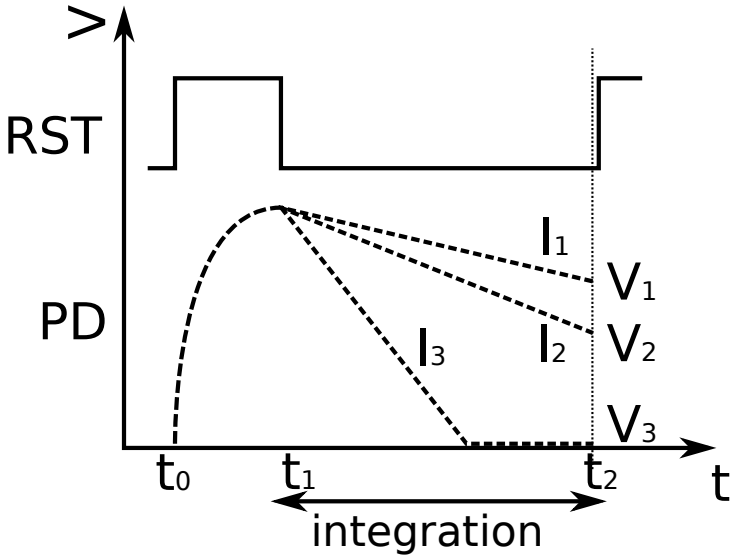


Figure 2.12: 3-Transistor pixel operation.

In Figure 2.12, $I1$ to $I3$ are increasing photogenerated currents due to different light contributions. At the end of the integration time, the voltage of the node is read through the source follower M2 using the M3 select switch. The voltage of the node $n1$ can be expressed as:

$$V = V_{rst} - \frac{t_{int} I_{ph}}{C_{PD}} \tag{2.9}$$

where V_{rst} is the reset voltage of the node $n1$ at the time t_1, $t_{int} = t_2 - t1$ is the integration time, I_{ph} is the photogenerated current and C_{PD} is the junction capacitance. In this example, $V1$ and $V2$ represent two typical converted intensities of light into voltages. For all the light intensities above a threshold, such as I3, the node $n1$ discharges to zero. In this case, the converted voltage will be equal to zero for both the intensities. As a consequence, the pixel's response is saturated thereby limiting the pixel dynamic range.

2.5.2 4T pixel

The 3T pixel approach suffers from intrinsic limitations of noise and dark current. In fact, reset noise is present as the junction capacitance stores the thermal noise of the reset transistor, which varies from frame to frame and it appears as temporal noise. In addition, in the 3T pixel, the photodiode is connected with a contact on its surface, which creates defects and, hence, leakage current. The 4T pixel solves this issues by utilising a buried photodiode, which is not accessed with a contact but through an additional special transistor called transfer gate [56].

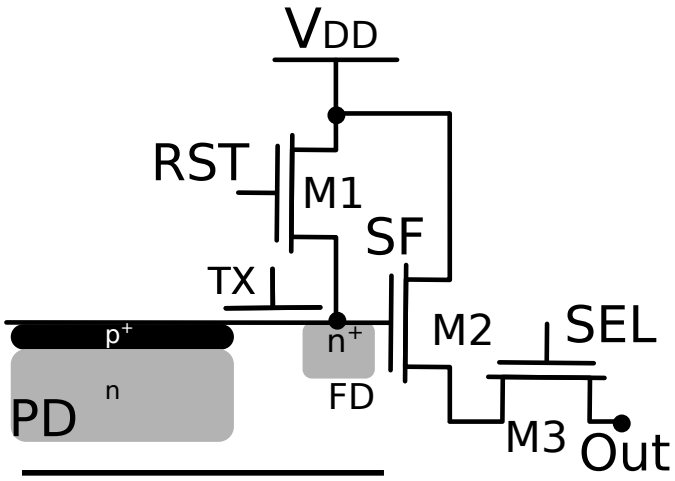


Figure 2.13: 4T Pixel Schematic.

Figure 2.13 shows the schematic of the 4T pixel where the transistors M1, M2 and M3 are the reset, source follower and row selector respectively, FD is the floating diffusion and TX is the transfer gate transistor, which enables the connection to the photodiode PD. The structure of the *pinned* photodiode consists in three layers: p+, n-implantation and p-substrate. The p-n junction is made by the n-implantation and p-substrate layers while the p+ layer is a surface pinning layer which reduces the superficial dark current due to the discontinuity of the n-implant in the standard photodiode as the dangling bonds at the surface are filled with this additional layer. The ideal behaviour of the pinned photodiode is shown in Figure 2.14.

Here, V_{pin} is the pinning voltage that is defined as the voltage that depletes the n-region of the photodiode, while OFF and ON are the potential levels for the transfer gate closed and opened respectively. The potential levels are shown in the negative direction. The photodiode is not directly connected to a voltage as it was in the 3T pixel. For this reason, when it is depleted, its potential is equal to the pinning voltage which only depends on the implantation of the p-n junction. The photodiode and the floating diffusion implantations are engineered to let

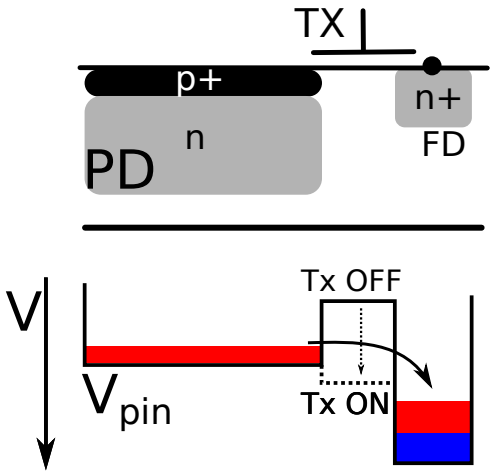
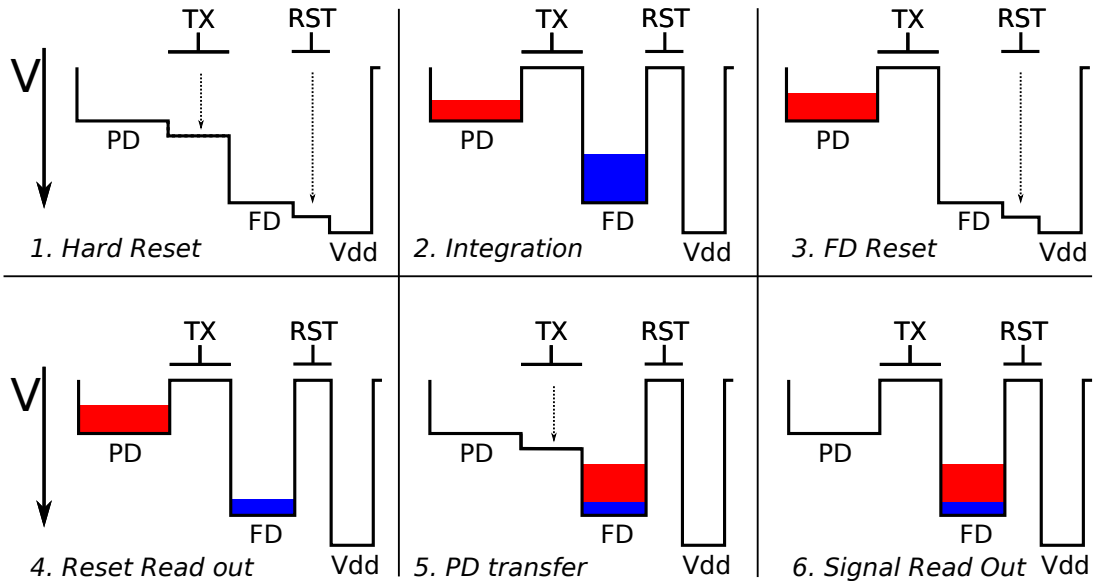
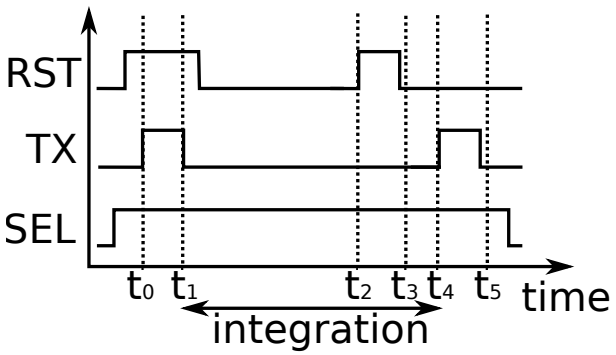


Figure 2.14: Pinned photodiode and ideal voltage domain representation. In red the photogenerated charge, in blue the floating diffusion charge.

the charge flow from the photodiode to the floating diffusion when the transfer gate is opened. When the transfer gate is closed, the charge, in red, accumulates in the photodiode.



(a) Pinned photodiode and ideal voltage domain representation. In red the photogenerated charge, in blue the floating diffusion charge.



(b) Control signals.

Figure 2.15: 4T pixel operation.

The 4T pixel operation is shown in Figure 2.15. At the time t_0 the transfer gate and the reset transistors are opened to empty both the photodiode and the floating diffusion. At the time t_1, the transfer gate is closed and the integration begins. The photogenerated charge (in red) is accumulated in the photodiode. During this time, the floating diffusion is filled with dark current and the parasitic charge (in blue) limits the capability of the floating diffusion to accommodate the charge from the photodiode. For this reason, the floating diffusion is reset again at the time t_2 and the reset noise is stored on the floating diffusion as an additional contribution of charge and its standard deviation can be written as $Q = \sqrt{kTC}$. At the time t_3, this value is read out by opening the SEL transistor, it is stored on a memory element in the column. The charge present in the photodiode is read by opening the transfer gate transistor at the time t_4. On the floating diffusion, there is the sum of the reset value and the signal generated during the integration time. This sum is transferred to another memory element outside the pixel. The difference between the two readouts is equal to the charge generated by the photodiode. This readout technique is known as correlated double sampling, which eliminates kTC noise [57]. In addition, the dark current is reduced thanks to the buried structure of the photodiode [39].

The operation of the 4T pixels has some practical limitations. An incomplete depletion of the photodiode introduces image lag which is the memory of a previous signal persisting on the image for several frames. This could be due to a large photodiode where the electrons need time to be transferred, to an insufficient transfer gate voltage which works as a barrier during the transfer of charge from the photodiode to the floating diffusion [58]. Another limitation is blooming which arises when the pixel is exposed to high illumination. The charge exceeds the full well capacity and spills over to the neighbour pixels appearing as an additional noise contribution.

In addition, when the photodiode capacitance is filled with charge, the 4T pixel is not sensitive to light as it saturated. Many solutions were developed to solve the issue of a limited dynamic range. Special signal driving [59] or integration time control [60, 61] were used. One possible architecture to increase the dynamic range is to use a logarithmic pixel [62–64], which is presented in the next section.

2.5.3 Logarithmic pixel

The logarithmic pixel has the advantage of imaging broad variations of light and translates them into a limited output voltage. Figure 2.16 shows a typical logarithmic pixel that uses the photodiode as a current generator and the load transistor as a current-to-voltage converter. Here, M1 is the load transistor, M2 is the source follower and M3 is the select transistor.

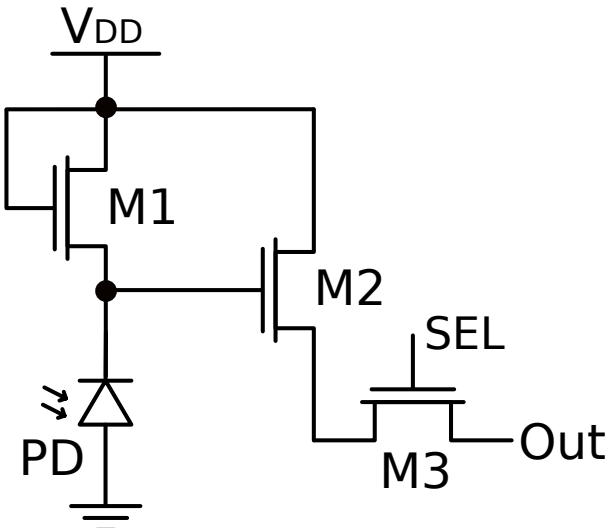


Figure 2.16: A typical logarithmic pixel with single nMOS load.

The load transistor, M1, operates in subthreshold thereby providing a logarithmic response as, in this region, the drain to source current is given by [65]:

$$I_{DS} = I_S e^{\frac{V_{GS}-V_{TH}}{nV_T}} \tag{2.10}$$

where I_{DS} is the drain source current, where I_S is a multiplicative factor that depends on the aspect ratio of the nMOS device, V_{GS} is the gate source voltage, V_{TH} is the threshold voltage, n is the subthreshold slope factor (that has a usual value range between $1 \sim 1.5$) and V_T is the thermal voltage. Using this equation, one can derive the source voltage of the nMOS, M1, as [66]:

$$V_{S,M1} = V_{DD} - V_{TH} - nV_T \log \frac{I_{ph} + I_{dark}}{I_{DS_0,M1}} \tag{2.11}$$

where V_{DD} is the supply voltage, I_{ph} is photogenerated drain current flowing in M1 summed to the dark current I_{dark} and $I_{DS_0,M1}$ is a characteristic value that defines the current that leaks through the transistor M1. The slope factor defines the effect of the gate voltage on the drain

current. The logarithmic pixel solves the problem at the brighter end of the pixel's response. However, at the darker end, both the linear and logarithmic pixel are limited by the characteristics of the photodiode. This determines the photoconversion quality and, hence, the image quality [36]. The logarithmic pixel, however, can be the pixel design of choice when a high dynamic range is needed as it is able to image more than five decades of illumination levels [62]. Unfortunately, logarithmic pixels are not the choice in standard products as they still suffer from high fixed pattern noise, due to the threshold voltage, lag and subthreshold slope mismatch. Information processing of logarithmic pixels is also more difficult due to their nonlinear response [67, 68].

2.5.4 4T shared pixels

CMOS image sensors light collection capability is directly proportional to the photodiode size. From a layout point of view, the transistors are limiting the area reserved to the photodiode and, hence, with a standard 4T pixel, it is difficult to further increase the photodiode area. For this reason, one way to shrink the area reserved to the transistors and, therefore, increase the photodiode size is to remove transistors in the array. This can be achieved by sharing the readout [69, 70]. With this approach, neighbour pixels use the same readout transistors. Sharing can be implemented in different ways, for example by sharing 4 or 8 pixels. These are generally referred to as 1.75T and 1.375T where the total number of transistors is divided by the number of photodiodes. In the case of the 4T pixels, there are 4 transfer gates, 1 source follower, 1 reset transistor and 1 select transistor for a total of 7 transistors. Each pixel has hence 7/4 transistors which is equal to 1.75T. The same calculation applies to the other sharing techniques and can be generalised as $\frac{N_{tr}}{N_{pix}}$, where N_{tr} is the total number of transistors and N_{pix} is the number of pixels.

A typical pixel consists of four neighbour pixels sharing the readout transistors as shown in Figure 2.17. In this architecture, the source follower, the row selector and the reset transistors are shared in between four neighbour pixels. Four transfer gates with their photodiodes are connected to the common floating diffusion and are read out sequentially. The photodiode size increases as there is a lower number of transistors in total. For a 2-shared pixel, there are 3 fewer transistors while for a 4-shared pixel there are 9 fewer transistors. Most of the major CMOS

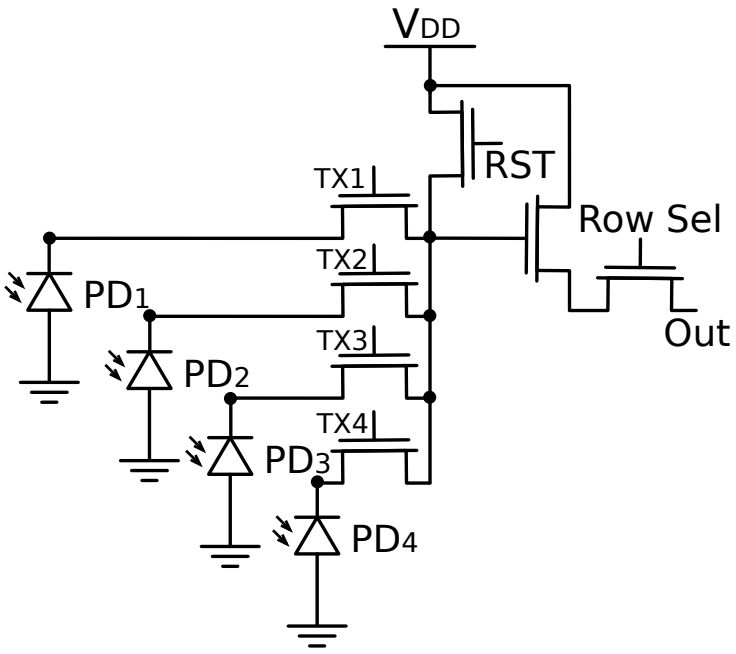


Figure 2.17: 4T 4-shared pixel schematic (1.75T).

image sensors producers offer a shared pixel readout to shrink the pixel size [71]. Unfortunately, sharing the readout comes with a cost of additional metal lines driving the transfer gates and a more complicated readout control. Each pixel is read out by the same transistors. Moreover, the floating diffusion size may increase, which means that the conversion factor is reduced. Unfortunately, shared architectures do not provide a high advantage in a readout mode known as global shutter where memory elements may be present. These memory elements usually occupy larger space than the readout transistors and make sharing techniques less attractive. In the next section, the readout modes are presented.

2.5.5 Readout modes

The normal readout operation of a 4T pixel is assuming a rolling shutter readout. In the rolling shutter readout mode, the rows are read sequentially. Figure 2.18 depicts the rolling shutter operation by dividing the readout sequence in reset, exposure (integration) and readout. With this approach, the control and the readout of the information are sequential. The first row is reset, the integration time begins and the readout is scheduled to happen at the end of the integration time. Then, the second row is reset and the integration time begins for the second row slightly after the first one. This operation is repeated for all the rows of the array. While this is a simple mechanism, it has the drawback of having the integration time shifted from row-

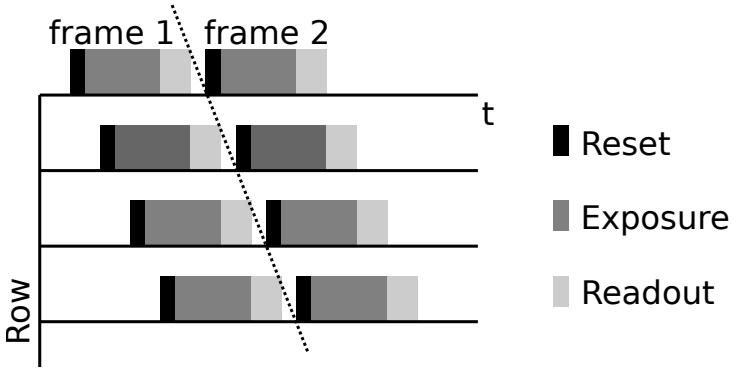


Figure 2.18: Rolling shutter operation.

to-row. In a fixed scene, this does not represent a problem as the signal to be integrated will not change during the operation. However, in a moving scene, the signal can change during the operation generating artefacts in the acquired image [72]. In order to correct this effect, another readout mode was introduced and known as global shutter.

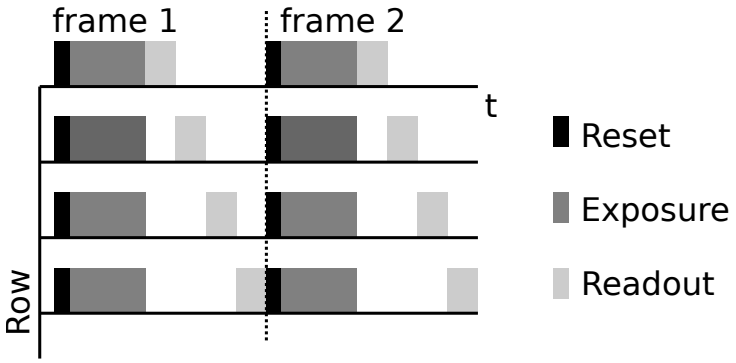


Figure 2.19: Global shutter operation.

Figure 2.19 shows the global shutter operation. With this readout mode, the reset and the exposure (integration) start at the same time for all the rows. At the end of the integration time, the measured signal is transferred on a memory element (which can be the floating diffusion itself) and it is then read out on each row in turn. This approach solves the issues related to motion artefacts but introduces other problems, which require additional transistors to be solved. For example, as during the readout the photodiodes can be filled with charge and can generate blooming. An antiblooming gate can be added to let the excess charge flow to a defined voltage rather than to spill in a neighbour photodiode. In addition, if there is a single memory element, it cannot be reset before the readout operation to correct for the kT/C noise, hence, additional memory elements can be added to enable a correlated double sampling operation to remove this noise [73].

2.5.6 Pixel noise chain

In the previous sections, the noise contributions were first described separately and then the pixel architectures presented. In this section, the noise sources for a typical 4T pixel architecture are described synthetically. Each of the noise sources contribute to the total amount of noise in the readout chain and Figure 2.20 presents a simplified block diagram of the CMOS image sensor where each of these is highlighted.

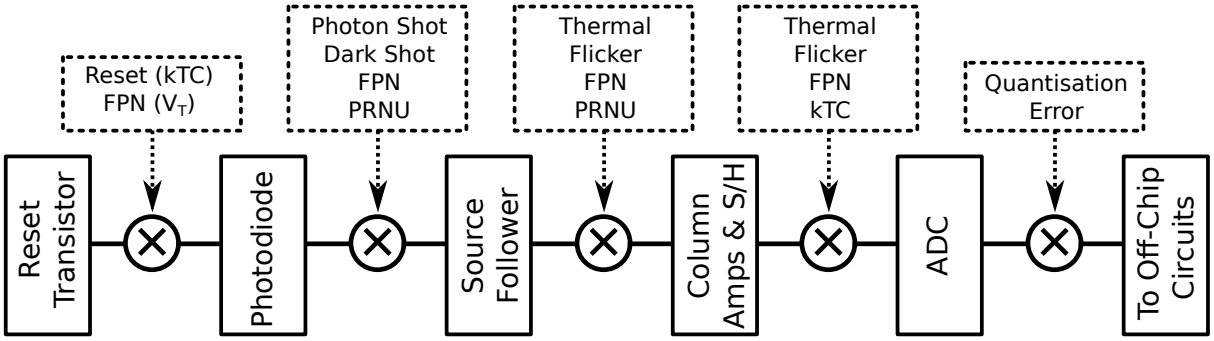


Figure 2.20: CMOS image sensor diagram of the noise contributions.

During the reset operation, the reset transistor stores the thermal noise on the floating diffusion capacitance introducing reset noise and FPN due to its threshold voltage variability. The charge collected in the photodiode and transferred to the floating diffusion adds photon shot and dark shot noise as well as FPN and PRNU. The in-pixel source follower adds thermal and flicker noise and FPN and PRNU due to mismatch effects. The column amplifiers also add flicker and thermal noise, however, while the in-pixel transistors and capacitances are small due to space requirements, the column circuitry can occupy a larger space and, hence, can be designed to introduce little noise. Furthermore, the ADC introduces a quantisation error due to the discrete nature of a digital signal. Finally, the converted signal is transferred to other noisy off-chip circuits. In each of this blocks, the input noise is amplified by the gains of each stage. The noise analysis of each of these blocks can be complex. Typically, in CMOS image sensors, the noise is input referred, which means that all the noise is attributed to the detector at the input. The total noise can be evaluated by measuring it at the output in Volts and referring it at the input through the Conversion Gain (CG) as:

$$N_I = V_{n,rms}[\mu V] \times CG \left[\frac{e-}{\mu V}\right] \tag{2.12}$$

where N_I is the input referred noise in electrons, $V_{n,rms}$ is the noise root mean square in Volts and CG is the conversion gain. The noise is hence typically expressed in equivalent electrons generated at the detector.

2.6 CMOS pixels review

In the CMOS image sensors community, a variety of pixel architectures and solutions have been proposed over the years. Unfortunately, while data on the electro-optical performance of the pixels is generally provided, information on the pixel layout is rarely available. Table 2.1 presents a condensed summary of information available in the literature on fill factor, technology, architecture, pixel pitch and their measured performance on a number of pixels.

This table already showcases the diversity in CMOS image sensors design which makes it difficult to compare.. The architecture of the pixels as well as the manufacturing technology and the pixel size is different. In this table, the values have been recalculated, where possible, to be presented by employing the same metric. Despite this effort, in many publications, data is either unavailable or hard to compare. The dark current, as an example, is measured at different temperatures for different pixel architectures. As it is proportional to the area, it is often reported as a density of current for the unit of area in $\frac{nA}{cm^2}$ rather than in $\frac{e-}{s}$. It may be possible to estimate the dark current at a given temperature by assuming it increases with a

Table 2.1: Comparison of pixels in CMOS technology

First Author	Mendis	Yadid-Pecht	Bermak	Waeny	Takahashi
Year	1994	1997	2000	2003	2004
Reference	[74]	[75]	[76]	[77]	[78]
Technology [μm]	2	1.2	0.7	0.5	0.350
Pixel Architecture	4T	4T	log 3T	4T	1.5 T
Pixel Pitch [μm]	40	20.4	13.4	10	3.9
Fill Factor [%]	26	28.9	46	30	17
Conv. Gain [$\mu V/e$]	4	5.6	-	-	23
Temporal Noise [e]	42	39	-	-	14.3
Dark Current [e/s]	62k @27C	3k @27C	-	-	8.3 @45C
Full Well [e]	150k	350k	-	-	10k
Image Lag [e]	0	-	-	-	0
Dynamic Range [dB]	71	81	-	-	-

Table 2.1 continued...					
Author	Storm	Acosta	Kim	Yoshiara	Han
Year	2004	2004	2006	2006	2006
Reference	[79]	[80]	[81]	[82]	[51]
Technology [nm]	180	180	130	180	180
Architecture	7T	5T	1.75T	1.75	3T
Pitch [μm]	5.6	7.5	2.25	2.5	3.6
FF [$\%$]	33	49	57	38	48.8
CG[$\mu V/e$]	-	-	-	-	-
Noise[e]	-	-	6	7	-
Dark Current [e/s]	660	-	15 @40C	15 @60C	5@25C
FW [e]	-	-	14	12k @60C	28k
Lag [e]	-	-	-	0	-
DR [dB]	58+85	-	-	64.7	-

Table 2.1 continued...					
Author	Cheng	Tochigi	Seo	Seo	Cho
Year	2012	2013	2013	2014	2014
Reference	[83]	[84]	[85]	[86]	[87]
Technology [nm]	180	180	180	180	130
Architecture	5T	12T +CAP	5T	1.75T	6T
Pitch [μm]	6	32	7.1	7.5	5
FF [$\%$]	27	37	45	43	58
CG[$\mu V/e$]	-	74	73.2	22.9	80
Noise[e]	-	5 @ 60C	1.1	4	-
Dark Current [e/s]	-	-	-	104 @60C	10e
FW [e]	-	-	-	-	45k
Lag [e]	-	-	-	-	-
DR [dB]	-	-	87.5	-	-

Table 2.1 continued...					
Author	Bouriama	Ma	Rezaeii	Yu	Yin
Year	2016	2017	2017	2017	2017
Reference	[88]	[89]	[90]	[91]	[92]
Technology [nm]	180	180	350	350	110
Architecture	4T	5T	3T	3T	1.375T
Pitch [μm]	7.5	6.5	6	15	2.5
FF [$\%$]	66	67	44.8	49	52
CG[$\mu V/e$]	185	80/20	-	-	-
Noise[e]	0.4	2	-	2.7 mV_{rms}	-
Dark Current [e/s]	-	10 @27C	-	-	-
FW [e]	-	45k	-	-	-
Lag [e]	-	1.5	-	-	-
DR [dB]	-	87	-	58	-

defined law [93]. The aim of this table, however, is to give the reader an overview of the CMOS pixel performance landscape. For example, Bouriama *et al.* have reached a very low level on readout temporal noise of 0.4 e or Yoshiara *et al.* presented a low level of dark current of 15 $e-/s$ at 60 Celsius. Over the years, the process technology minimum length was improved and reduced. This enabled finer pixel pitches. Figure 2.21 reports the pitches of the pixels presented in Table 2.1 for the range of their respective process technologies. Each blue dot represents a pixel of the table. For lower process technologies the pixel pitches are smaller up to 2.5 μm. This is consistent with Moore's law and the overall shrinking of electronics. [94].

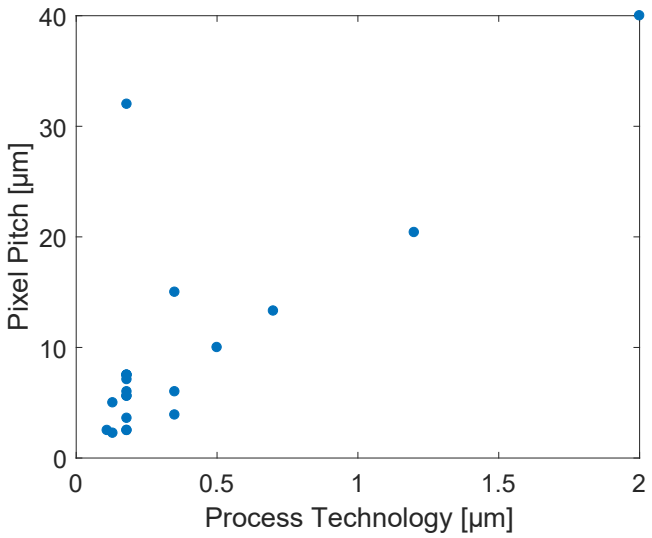


Figure 2.21: Pixel pitch for different process technologies from Table 2.1.

In the presented publications there is a significant amount of detail about the system and pixel architecture while the information on the pixel layout is very limited. This is so because the layout has a strong impact on the pixel performance and companies operating in the CMOS image sensor market tend to protect the intellectual property of their layout by not disclosing it. The only parameters given are the fill factor and the pixel pitch. The layout information is so precious that specialised companies exist to provide the layout through de-processing and reverse engineering of the manufactured devices. Pixel layouts from the major players in the market are beautiful and extremely compact and efficient designs. Examples are reported hereafter.

Figure 2.22 shows the layout of an Aptina 1.4 μm 4T 4-shared pixel layout redrawn from a SEM image published in [71]. The geometries are estimated from the image and are not representing the exact pixel layout but can serve to the reader to have an idea about the original

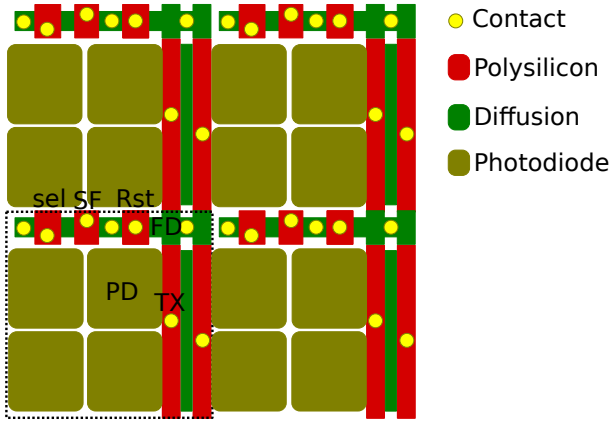


Figure 2.22: Aptina 1.4 μm 4T 4-shared pixel layout (redrawn from [71]).

layout. Here, the contacts are represented by yellow circles, the polysilicon in red, the diffusions in green and the photodiode area in light brown. In this pixel, the transfer gates are shared between two different photodiodes to create an even more compact layout. The estimated fill factor of this pixel is 55%.

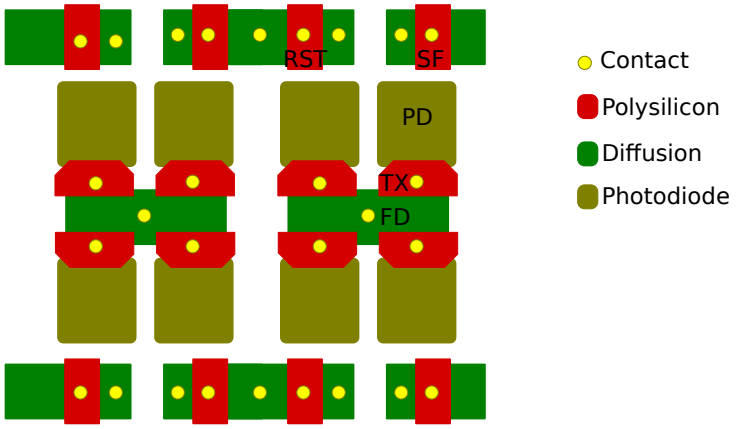


Figure 2.23: Kodak 1.4 μm pMOS 4-shared pixel layout (redrawn from [50]).

A pixel layout with a very low dark current of 30 pA/cm^2 measured at 60C based on pMOS transistors is presented by McGrath *et al.* in [50]. Figure 2.23 shows the redrawn layout. In this Figure, the same colour combination has been used as in the previous one employing yellow for the contacts, red for the polysilicon, green for the diffusion and light brown for the photodiode. The four transfer gate share the common floating diffusion and the common readout transistors. This pixel does not require a select transistor which enables a larger area of the photodiode. The space in between the groups of photodiodes is occupied by metal routing which is not reported here. A 130 nm process technology was used and the estimated fill factor is 30% which allows to calculate the dark current as being equivalent to 22 e/s.

A market popular commercial still camera pixel was de-processed and published by Fontaine

in [95]. The pitch is larger compared to the layout showed previously. In this pixel, the photodiode is split in two for auto-focus purposes. Figure 2.24 shows the layout of the 4.1 μm 4T

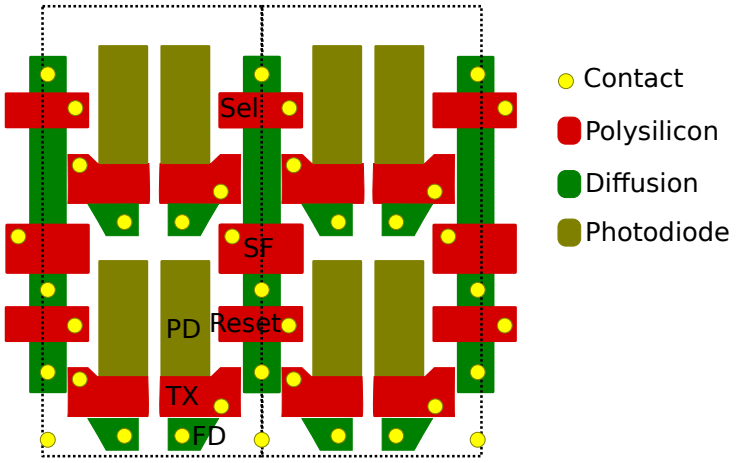


Figure 2.24: Canon LC1290A (EOS-70D) 4.1 μm Dual Pixel layout (redrawn from [95]).

4-shared pixel with dual photodiode. The color convention is the same as the one presented previously (yellow for the contacts, red for the polysilicon, green for the diffusion and light brown for the photodiode). The estimated fill factor of this pixel is calculated by assuming that the two photodiodes belong functionally to the same pixel and is 25%.

Despite the pixels having similar functionality and number of transistors, their layouts are different as this was the result of different strategies. The last example to show this diversity is a 2-shared 1.4 μm pixel from Fujifilm [71] that is presented hereafter.

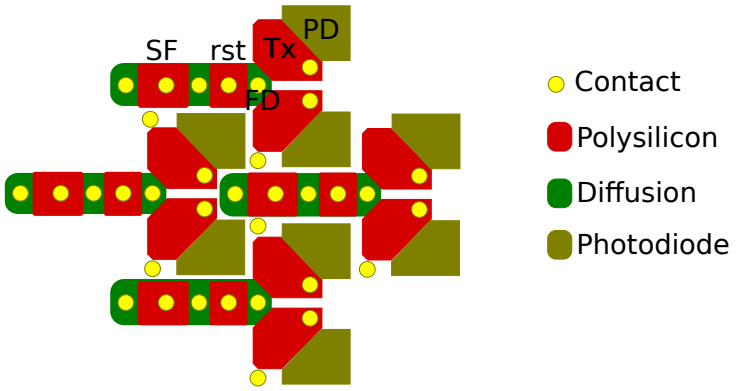


Figure 2.25: Fujifilm Back-illuminated 1.4 μm 2-shared pixel layout (redrawn from [71]).

Figure 2.25 shows the pixel layout of the Fujifilm pixel. The colour used to define the contacts, the transistors and the photodiode are again the same as used previously. This is a 2-shared design where the floating diffusion is shared between two photodiodes and transfer gates. The select transistor was removed also in this design to save space. The estimated fill

factor is only 25 % which is smaller compared to the solution presented previously. However, this a back-illuminated pixel [56] where the light shines on the other side of the silicon wafer and hence the photodiode size could be underestimated. This is a clever design as the readout pixels are nested in order to occupy the area more efficiently and has been studied also by Bogaerts *et al.* in front illuminated pixels [96].

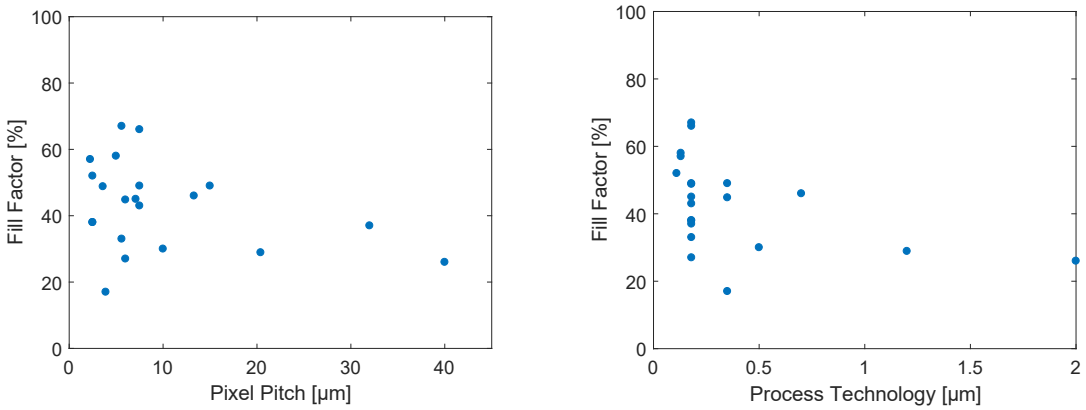
These pixel layouts show the strong diversity between them. Despite performing the same function, the only elements that are similar in every design are the readout transistors (source follower and reset) while the photodiode shape, the transfer gate design and the pixel position and orientation change drastically between one design and the other. As an example, the Aptina transfer gate is long and thin while the Fujifilm transfer gate is almost triangular which may have an impact on the transfer of the charge. Furthermore, the floating diffusion of the Canon pixel is isolated and small while the floating diffusion of the Kodak Pixel is large and shared. This choice will translate into two different capacitances of the floating diffusion node and, hence, different conversion gains.

The general conclusion is that the same pixel architecture could result in many different layouts. A question about which metric should be used when comparing the layout quality arises. In the literature, the fill factor is the parameter usually given to synthetically describe the pixel layout. An analysis of this metric and additional considerations are undertaken in the next section.

2.6.1 Considerations on the Fill Factor

In section 2.3.1, the fill factor was defined as the ratio between the photodiode area and the pixel area. This a standard parameter that gives a rapid synthetic information on the photodiode dimension compared to the pixel area. In the previous section, a table with a number of pixels having different fill factors was collected. In this section, the fill factor is analysed for these pixels and considerations on this metric are introduced.

In Figure 2.26, each dot represents a column of the Table 2.1 where the fill factor is compared either to the pixel pitch or to the process technology. From these Figures, there is no apparent correlation between the fill factor and the process technology or the pixel pitch. In general, it is a number comprised between 20 % and 80 %. This is so because, when it is pos-



(a) Fill factor for different pixel pitches. (b) Fill factor for different technologies.

Figure 2.26: Fill factor for different pixel pitches and process technologies (Table 2.1).

sible, the pixel pitch is reduced to keep a reasonable fill factor in a given technology. However, the fill factor helps to compare the efficiency of the layout design only if the pixels have the same architecture, process technology and pitch otherwise it is a poor metric for this scope. To better explain this idea, the following example is reported.

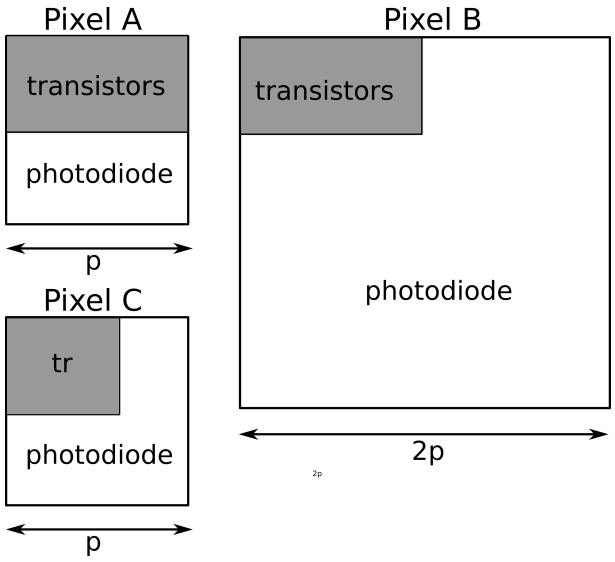


Figure 2.27: Fill Factor examples for different pixels.

Figure 2.27 shows the fill factor for 3 pixels namely A, B and C. The pixel A has a fill factor of 50%, in the same technology pixel B has a higher fill factor of 87.5% but its size is doubled. Finally, pixel C has a higher fill factor of 75% and the same pixel pitch. Without expressing the pixel pitch and the process technology used, the fill factor only returns a limited amount of information. As in the example, one could increase the pixel pitch and, consequently, the photodiode area, to achieve a higher fill factor. Furthermore, when shrinking the technology, the transistors occupy less area leading to the same effect. In addition, two different pixel

architectures have different fill factors because of the diverse number of transistors employed.

These considerations suggest a layout quality metric that represents how the pixel area is used to layout the pixel. According to the assumptions of this Chapter, the area occupied by a single transistor is fixed in the process technology. Instead, their organisation in the available pixel area is a feature accessible to the designer. However, for a given technology and a given number of transistors, it is impossible for the designer to layout a pixel smaller than the physical area occupied by the transistors in that technology. The fill factor is not technology and process independent. A better way to describe the pixel layout characteristic could be the Area Utilisation Factor (AUF), which is introduced here and defined as the ratio between the photodiode area and the pixel size minus the transistor area:

$$AUF = \frac{A_{pd}}{A_{pixel} - A_{tr}} \times 100 \tag{2.13}$$

where A_{pd} is the photodiode area and A_{pixel} is the total pixel area and A_{tr} is the area of the transistors. This factor is a layout design quality metric and represents the area utilisation efficiency of the pixel layout. It is worth considering how the transistor area is defined. One way to define it would be to take into account the size of a standard transistor in a given technology and compare it to the actual space occupied by the transistors in the pixel design. Unfortunately, this requires to know the standard transistor size for each process technology.

From Table 2.1, the fill factor, the pitch, the pixel architecture and the process technology is reported for a number of publications. It is possible to estimate the average area of each transistor in each of these published pixels by calculating the total area of the transistors. This is done by computing the area of the photodiode, by evaluating the difference with the total area by assuming that the area that is not reserved to the photodiode is dedicated to the transistors, and by dividing by the number of transistors in the architecture. This can be written as:

$$E(A_{tr}) = \frac{(1 - FF/100) \times p^2}{N_{tr}} \tag{2.14}$$

Where $E(A_{tr})$ is the estimated transistor area, FF is the pixel fill factor, p is the pixel pitch and N_{tr} is the number of transistors in the pixel architecture. By dividing by the total number of transistors an error is introduced as not all the transistors are of the same size and generally the transfer gate is larger. However, this could be a good first order approximation. This estimation

is undertaken to the pixels presented in Table 2.1 and generates the following result.

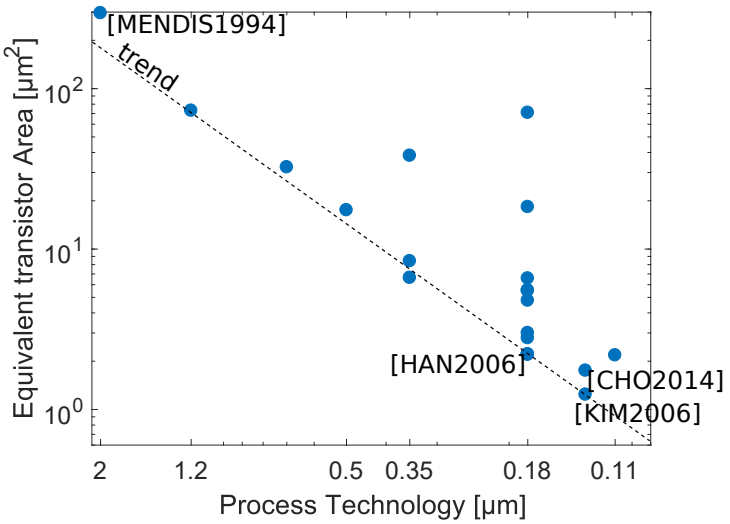


Figure 2.28: Estimated Transistor area for different process technologies of the pixels in Table 2.1.

Figure 2.28 shows the estimated transistor area for the pixels presented in Table 2.1. Each dot represents a published work and it is plotted on logarithmic axes to better visualise the differences between the transistor areas. Older works, like Mendis *et al.* (1994), have a higher transistor area as they employ a larger process technology. As expected, with the technology shrinking the transistor area is reduced. Within the technologies lower than 180 nm the best three works are reported in the figures and are: Kim *et al.* (2006) for a technology of 130 nm and an estimated transistor area of 1.24 μm^2 and a fill factor of 57 %, Cho *et al.* (2014) for the same process technology and an estimated transistor area of 1.75 μm^2 and a fill factor of 58 %, and Han *et al.* (2006) for a technology of 180 nm and an estimated transistor area of 1.24 μm^2 and a fill factor of 49 %. If only the fill factor would have been evaluated as a metric, the pixel of Kim would be considered worse than the one of Cho while being more compact in the transistor design. Without taking into account the electro-optical performances, a pixel with a more efficient transistor area would hence translate in a pixel with a better fill factor given the same process technology and pixel pitch.

2.7 Summary

In this Chapter, a general overview of a Camera was presented with a particular attention to the CMOS image sensor itself. An overview of the noise sources, the pixel performances and archi-

tectures was introduced. In addition, A literature review of the dark current and to the various techniques to model and reduce the dark current was presented. One of the main sources of the dark current is the STI and layout techniques are proposed in the literature to reduce the interaction of the STI with the photodiode. The layout has a direct consequence on the electro-optical performance of the pixels, for this reason, an analysis of the performances and the layouts of the pixels present in literature was undertaken. This analysis shows that the amount of information given on the layout is extremely limited despite its impact on the performance. The metric usually employed to describe the layout is the fill factor, which does not provide enough information about the quality of the pixel layout. Another metric, the Area Utilisation Factor, was introduced and an analysis of the in-pixel transistor sizes undertaken from data available in the literature. The next Chapter describes the experiments conducted during this work and presents a pixel which reduces the dark current by layout techniques.

Chapter 3

Dark current reduction by layout

In Chapter 2, the concept of dark current was introduced and an overview of the various techniques to reduce it was presented. In particular, the pixel layout can have a strong impact on the sensor performance. This is related in particular on the interaction of the STI with the photodiode which causes the dark current to increase. Many layout techniques aim to reduce this interaction, however, these usually come at the cost of other performances like a reduction of the fill factor. In this Chapter, a layout technique to reduce the dark current which also increases the fill factor is presented. The Chapter is organised as follows: Section 3.1 introduces the experiment that was designed for the purpose of this thesis, Section 3.2 presents the techniques and the methodology of the measurements of the CMOS image sensor parameters, then, Section 3.3 proposes an alternative approach to remove the in-pixel isolation, Section 3.4 presents the experimental results which shows that this technique is able to reduce the dark current and Section 3.5 summarises the Chapter.

3.1 Experiment design

This section presents the test chips that have been designed and manufactured to prove the assumptions made in this thesis. All the pixels described in this thesis were designed and manufactured in the LFoundry Image Sensor 110 nm process technology. When this work was conducted, LFoundry was not offering a mature Image sensor technology to their customers and partners. The partnership with the design house Awaiba was intended to realise a high number of pixel variations to extract as much information as possible and to compare different

pixel performances which were made and manufactured. In return, Awaiba was receiving free Silicon to evaluate the process technology in order to potentially use it in their products. This required a negotiation between the stakeholders of the projects to define the number of pixels that would be needed for the LFoundry process development and the ones that were free to use for the purposes of this project.

After this agreement, several different test chips were designed, laid out, manufactured and measured. Each test chip has a similar core and architecture structure while the arrays are divided in variations. Each test chips has a 400-by-400 pixel array. the pixel pitch of choice is 2.4 μm which is a relatively large pitch but in line with the process technology and with the target applications of Awaiba.

Each test chip has a starting baseline pixel configuration and parametric layout pixel variations in order to evaluate the impact on the electro-optical performance of these different layout changes. A complete list of the variations is presented in the appendix A.2 although not all of them will be presented in this thesis. In fact, the majority of the pixel variations were reserved for LFoundry internal purposes. In total, nine different test chips were manufactured. These are listed and briefly described thereafter:

- 4-shared 4T p-well isolated pixel (VA1)
- 4-shared 4T p-well isolated pixel with readout variations (VA2)
- 4-shared 4T STI pixels (VA3)
- 4T fully symmetric pixel (VB1)
- 4T p-well isolated pixel (VB2)
- 4T STI pixel (VB3)
- 4T staggered pixels (VB4)
- 3T pixels (VC)
- Single pixels (4T-logarithmic) (VD)

This is a high number of architectures for studying the process technology. However, at the time, there was no previous data on CMOS image sensors from the foundry. These architectures

were prepared as a result of the trade-off between the probability of having a working device and the desire of gathering deeper information on the best samples. It has to be considered the introduction of a new technology is different from a standard tape-out of an established process technology. As an example, the usual time for a product to be manufactured in the production line is 2-3 months. However, when a new technology is introduced, the foundry creates a matrix with variations on the process conditions for the chips to be manufactured in order to find the best process conditions for the targeted performance. This means that the silicon in the production line is split at the selected process steps. The manufacturing lot of wafers has to wait that all the process variations are completed in order to move to the next step. The final result is a manufacturing process which lasts 6-8 months and at a higher cost. In this context, the risk mitigation was crucial. Design errors could slow down the product release of more than one year.

The main targets for the experiment were the state-of-art 4-shared architectures which can offer a higher fill factor and full well capacity and can open the path to a further shrinking of the pixel size. However, the readout operation of a shared architecture is slightly more complex of a standard 4T pixel. For this reason, as a backup plan, also non-shared 4T pixel versions were designed. Many layout variations implemented in the 4-shared architectures were replicated in the non-shared architectures. This redundancy could be used to gather more statistical information in the case all the pixels worked.

In addition, as the 4-shared versions cannot be symmetrical by definition as the sharing introduces an asymmetric pattern in the pixel block. In order to study the optical symmetry, a fully symmetric pixel version was designed and manufactured as well (VB1). Furthermore, a novel layout approach is presented here where the STI is retained in between the transistors but it is removed between the photodiodes, these are 4T p-well isolated pixels (VB2). Another test chip was designed where the STI is present between the photodiodes to compare the results, this is the 4T STI isolated pixel (VB3).

The 4T staggered pixel version (VB4) is introduced here but will be presented in the next chapter. This chip is the test device which includes a novel pixel layout arrangement that maximises the fill factor.

The 3T pixel test chip (VC) has been added to the project to mitigate the risk of having a

non-working transfer gate. In fact, the transfer gate is a critical component and a failure in the transfer of the electrons to the floating diffusion could have compromised the entire experiment on 4T pixels. In the case of transfer gate failure, neither of the 4T pixels would have worked but at least it would have still been possible to collect electro-optical data from the 3T pixel devices.

Finally, in the last chip (VD), single test pixels versions were added to directly measure the pixel performance. This was designed to account for failures in the readout circuitry. A direct access to single pixel devices could have granted at least pixel information. This test chip contains the standard pixels all the pixels present in the other chip versions (VA, VB and VC) as well as logarithmic pixels and additional research pixels that are not presented in this thesis.

The pixel matrices are accessible thanks to mixed-signal on-chip electronics which is detailed in the Appendix. In this project, each test chip has a 400-by-400 pixel matrix which was designed for each of the different pixel variations. One example of a test chip layout is shown in Figure 3.1. The pixel matrix occupies the centre of the test chip while the row scanners and the column readout circuitry are respectively put on the left and on the bottom of the matrix. The pad frame surrounds the sensor to enable its communication to the external world. The dimension of the chip is 2-by-2 mm with a pixel matrix of 960-by-960 μm.

It was decided to build each test chip version with in-pixel variations. The matrices were then divided in 8 variations each of 100-by-200 pixels separated by optical black top metal stripes (in pink). The aim of these variations was to find the best candidates for the transfer gate, for the pixel-to-pixel isolation, for studying the effect of the ground contact and the effect of metal shields in the array. To summarise, the variations in each matrix are numbered as in Figure 3.2.

Figure 3.3 shows the layout of the 3-by-3 reticle of the test chips designed for the purposes of this work. The variations are physically divided into sub-matrices by the means of metallic stripes. With this organisation, the viewer can quickly identify the region of interest.

Figure 3.4 shows the microphotograph of one of the manufactured test chips. This is a packaged chip and the bonding wires are visible in the image. The brighter yellow stripes are the top metal layers that divide the pixel array into the variations. These metal stripes are covering four pixels and hence they are visible in an acquired image in the light.

Figure 3.5 shows a mid-level acquired image of the standard 4T pixels. In the acquired

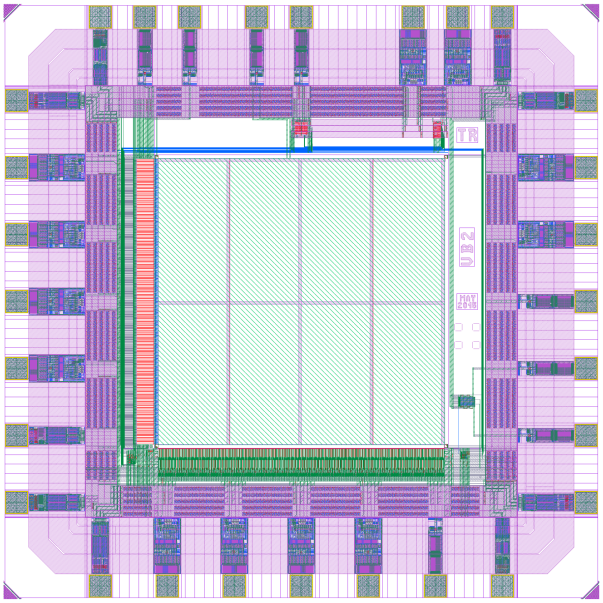


Figure 3.1: Standard pixel (VB2) test chip final layout with padframe.

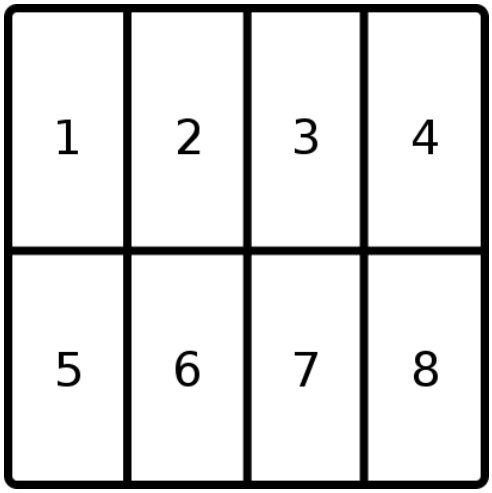


Figure 3.2: Variation numbering of the pixel matrix.

image, the contrast between the pixels covered by top metal and the uncovered pixels is visible. The analysis of the mid-level illumination image is used to check the sensor functionality, the presence of the metal stripes immediately gives the information that the sensor is correctly responding to light. The next sections will introduce how the dark current and light measurements are performed.

Table 3.1 reports a summary of the pixel versions prepared for the purposes of this project where the common features and the main differences are highlighted. Please note that for version VD some descriptions criteria were Not Applicable (NA) and have been marked in this way. All the chips present in this work have the same pixel pitch, process technology and were manufactured on the same process batch which makes them good candidates for layout

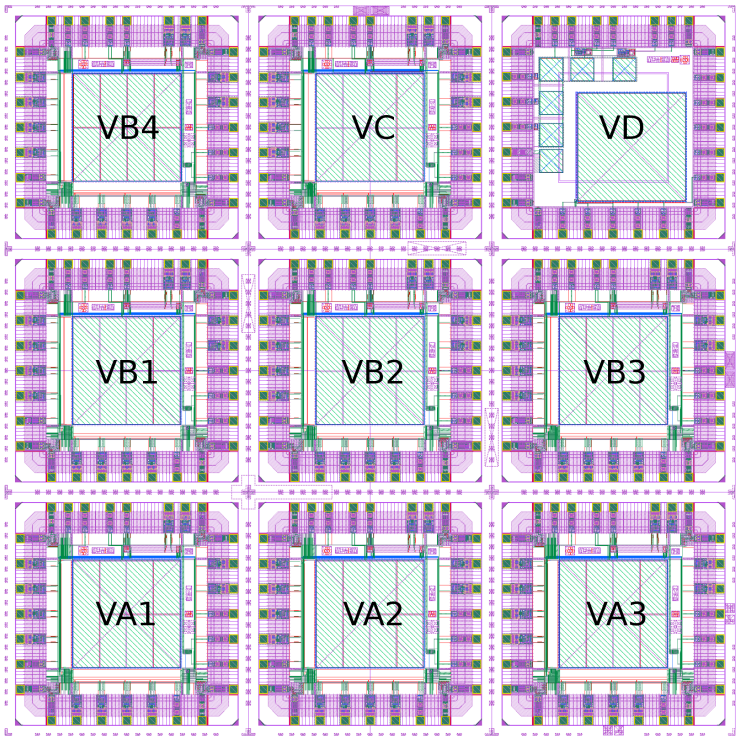


Figure 3.3: Final LFoundry 110 nm IS testchip reticle set.

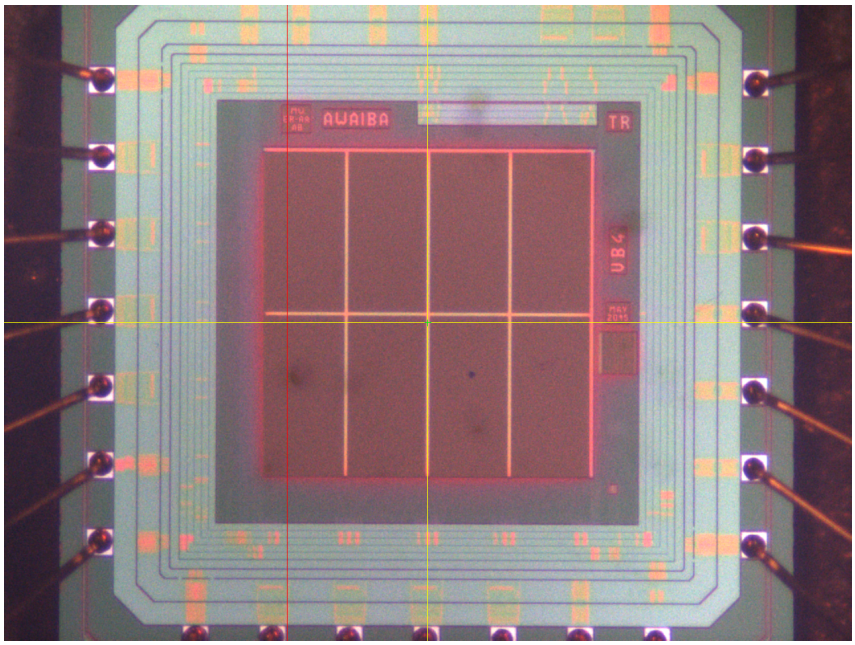


Figure 3.4: Microphotograph of a packaged test chip.

comparison.

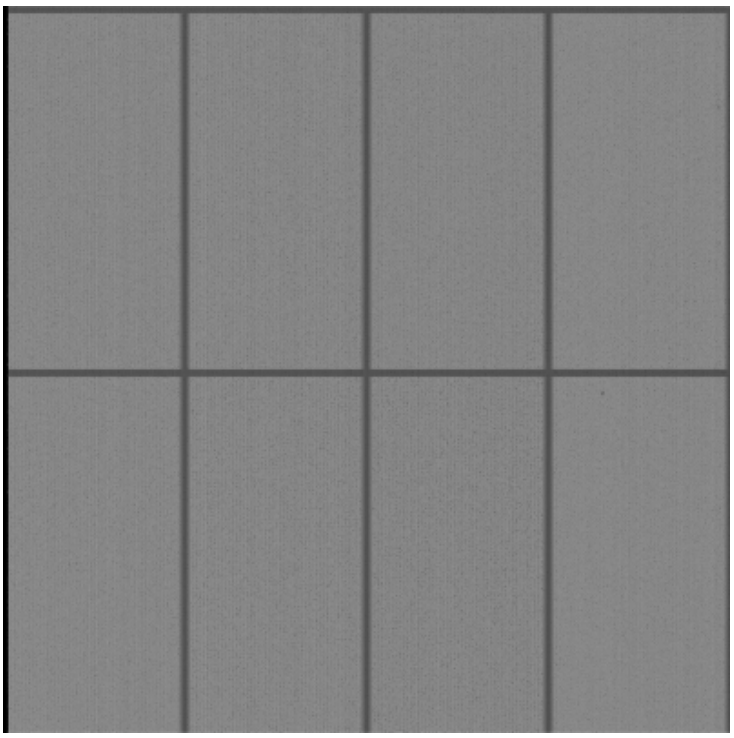


Figure 3.5: Standard 4T pixel mid level illumination image.

Table 3.1: Test chip version summary

Pixel Version	VA1	VA2	VA3	VB1	VB2	VB3	VB4	VC	VD
Pixel architecture	4T-shared			4T				3T	3T,4T,log
Pixel pitch [μm]	2.4								NA
Pixel Matrix Size	400 x 400								NA
Operating Frequency	4 MHz			2 MHz					NA
Readout	Analogue								
Technology	LF 110 nm Image sensor technology								
Illumination	Front side illumination								
Chip Size	2-by-2 mm								

3.1.1 4T Pixel layout summary

The layouts and the main features of the baselines of the pixels design within the project of this thesis are introduced in this section. The designed pixel layouts are compared and their parameters are summarised in Table 3.2.

This table highlights the main parameters of consideration that will be discussed later in this thesis. For each pixel architecture, the isolation mechanism of the photodiode is shown. Both the fill factor and the area utilisation factor are compared for these pixels. It is clear how the shared versions fulfil the purpose of increasing the photodiode area compared to the non-shared versions VB1, VB2 and VB3. This comes at a cost of a larger size of the floating diffusion that translates into a larger floating diffusion capacitance. A novel staggered layout strategy will be

Table 3.2: Pixel layout summary.

Version	Pixel	Isolation	Fill Factor	AUF	FD Area	Tx type
VA1, VA2	4T 4-Shared	p-well	53 %	69 %	0.53 μm^2	Single edge
VA3	4T 4-Shared	STI	42 %	55 %	0.53 μm^2	Single edge
VB1	4T Sym	STI	28 %	48 %	0.10 μm^2	Single edge
VB2	4T	p-well	36 %	62 %	0.21 μm^2	Single edge
VB3	4T	STI	29 %	51 %	0.21 μm^2	Single edge
VB4 v1	4T Stag	STI	42 %	72 %	0.10 μm^2	Round edge
VB4 v2	4T Stag	p-well	43 %	74 %	0.10 μm^2	Single edge

presented in the next Chapter which leads to an increase in the fill factor only by means of a smart organisation of the pixels to minimise the number of contacts. This staggered pixel has a comparable fill factor to the 4-shared pixel although its area utilisation factor is higher. This is so because it occupies the available space more efficiently, which means that each transistor occupies less area. Figure 3.6 introduces the pixel layouts for each version close to each other

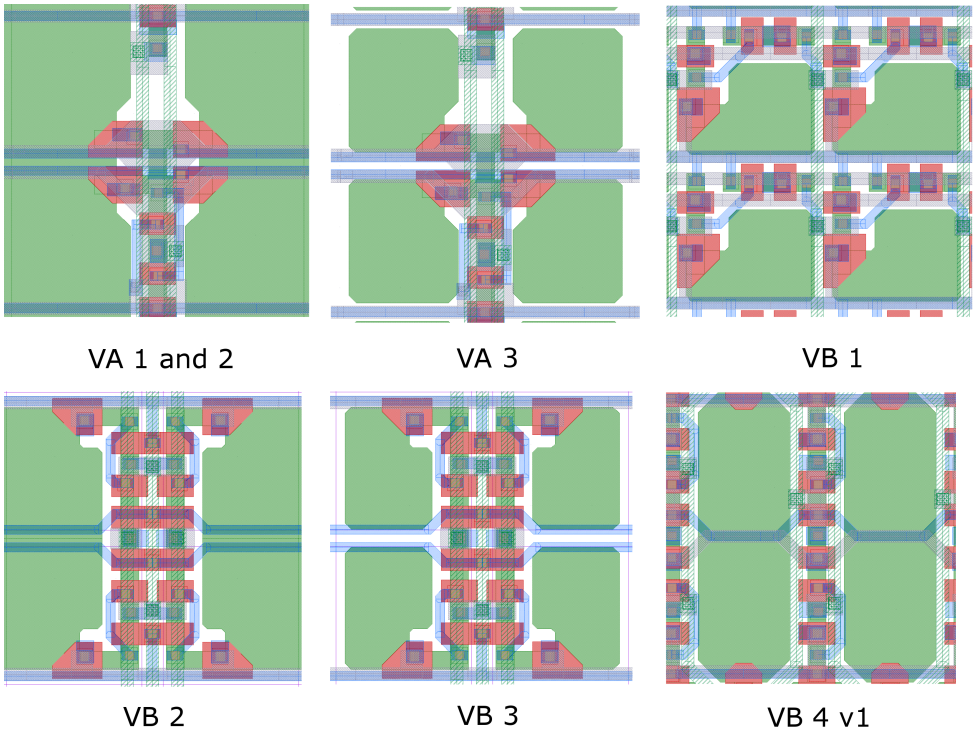


Figure 3.6: 4T pixel layout summary.

for a visual comparison. In this figure, the diffusion is in green, the polysilicon is in red and the contacts are represented with clear squares. In addition, the levels of metal are visible and these are designed in order to avoid any coverage of the photodiode. All these pixels have the same pixel pitch of 2.4 μm.

The next section will present the measurement techniques used in this thesis to extract the sensor performances. Measured experimental data of the versions VB2 and VB3 will then fol-

low to show how dark current can be reduced by removing the STI in between the photodiodes.

3.2 Measurement setup

This section introduces the techniques and the approach followed in this thesis to measure the CMOS image sensors parameters and the dark current. A brief introduction on the photon transfer theory is also given here.

3.2.1 Dark sweep setup

In a CMOS image sensor, the dark current information is obtained through an indirect measurement. The electrons generated in absence of light are integrated to obtain a measurable signal. The charge accumulates in the photodiode during the integration time. When the charge generated in the dark is transferred to the floating diffusion, the voltage on the floating diffusion, for a given temperature, is proportional to: $\frac{t_{int} I_{dark}}{C_{FD}}$ where t_{int} is the integration time, I_{dark} is the dark current, and C_{FD} is the floating diffusion capacitance. Hence, to measure the dark current, at least two points are needed to evaluate the slope of this curve. Each pixel will have a different dark current due to both spatial variations and to temporal noise. The effect of the spatial variation, also known as Dark Signal Non-Uniformity (DSNU), can be mitigated by averaging the dark current value for all the pixels of the same frame. Instead, the temporal noise effect can be reduced by collecting and averaging more than one frame. Ideally, the higher the number of frames the lower the impact of temporal noise on the measurement. However, a high number of frames translates into a high measurement time which results in an increased cost for high volumes of production and testing. For the purposes of this work, 40 frames are averaged for each integration time. Although it is possible to calculate the dark current from only two points, more data points will reduce the linearity error. In particular, the EMVA1288 standard suggests taking at least six equispaced points for this measurement [28]. As the dark current is proportional to the temperature, these measurements are undertaken in a controlled temperature environment.

Figure 3.7 shows a mosaic of temporal averaged frames of the dark signal for increasing integration times. Every rectangle is the average of the same window of pixels averaged in

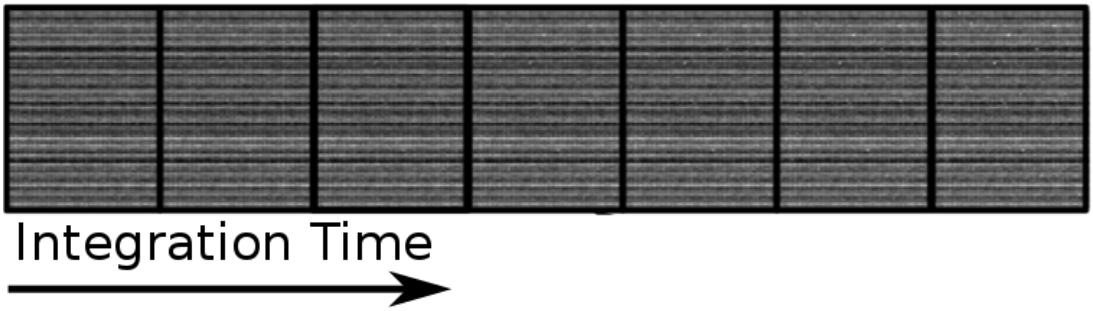


Figure 3.7: Mosaic of averaged dark images for increasing integration times at 60 Celsius.

time. Visually, from this image, it is hard to derive any information on the dark current as the increase in dark current is low. Nevertheless, if the spatial average signal of the window is considered, the dark signal can be plotted versus the integration time as in Figure 3.8 where each point represents the spatial average of each rectangle and the red line shows the linear fit of the data points.

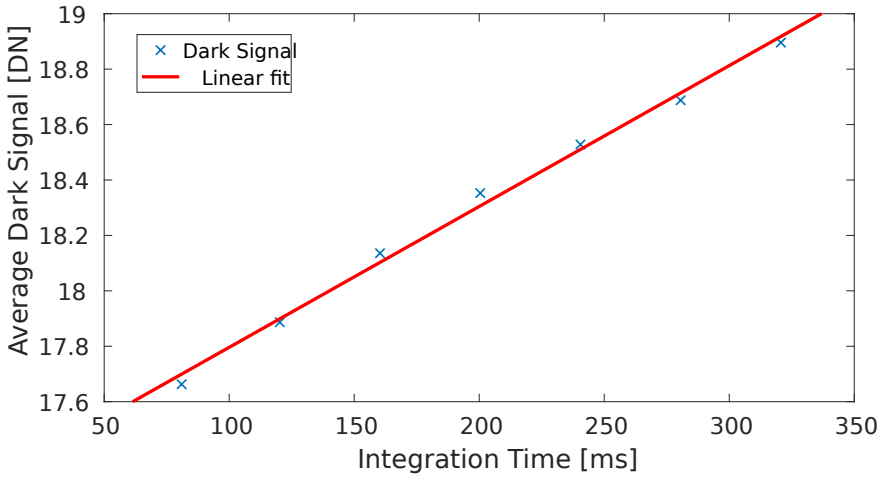


Figure 3.8: Average dark signal at increasing integration times of a 4T pixel at 60 Celsius and its linear fit.

In order to measure a stronger dark current signal, the measurement temperature is set to 60 Celsius. The floating diffusion capacitance is defined by layout and cannot be modified. The only other parameter left to actually change the measured signal is the integration time. A higher integration time will provide a higher measured dark signal for the same dark current. The test chips were designed with a programmable integration time which has a range (1.2-162 ms). Even at 60 Celsius and at the maximum programmable integration time of 162 ms the measured dark signal was below 1 numerical digit. In order to solve this issue, different paths could be undertaken. From one side, the resolution of the ADC could be increased and its range and gain matched to the dark signal. Unfortunately, this required a modification of the

PCB board where the external ADCs were located and hence was not the solution of choice. From another hand, one could increase the dark signal by increasing the temperature. However, all the measurement conducted by LFoundry for their other products were undertaken at 60 Celsius. Hence, There was a need to keep the temperature at 60 Celsius to ensure the capability to compare these new measurements with the previous and future work. Nevertheless, a further way to increase the dark signal is to slow down the chip operation by reducing the main clock frequency. In fact, all of the internal signals are generated from the external main clocks. The main clock was then halved and set to 1 MHz. This means that the integration time is doubled and ranges from 2.4 ms to 324 ms. This is the operation condition used for the dark signal measurements in this work and Figure 3.8 was obtained with this clock setting. The dark current information is derived from the slope of the linear fit and given in LSB per second. The photon transfer theory utilises the statistical information of the measured signal to convert the digital numbers into electrons as explained in the following subsection.

3.2.2 Photon transfer theory

Pixel information in electrons is obtained thanks to the photon transfer theory. Collected images from the sensor are the final result of a complex readout chain. However, in CMOS image sensors interacting photons generate electrons. Photon shot noise follows a Poisson distribution and, hence, its variance is proportional to the signal $\sigma_S = \sqrt{S}$. By considering the readout chain as a black box, the following expressions can be written [97]:

$$S = IK \tag{3.1}$$

$$\sigma_S = \sigma_I K \tag{3.2}$$

where S is the unknown electrical signal, I is the measured encoded digital information (image), σ_S and σ_I are the respective noise standard variations and K is a sensitivity constant. The input signal is usually measured in electrons while the encoded digital information can be expressed in digital numbers. The sensitivity constant can be written as:

$$K = \frac{I}{\sigma_I} \tag{3.3}$$

This is an important result as it means that for a CMOS system the original unknown signal can be obtained only by observing the output digital signal and its related statistical information such as mean and variance. This correlation enables the possibility to collect data in digital numbers and to convert it into the number of electrons. To do so, statistical data needs to be collected. For the purposes of this work, the constant K is called Conversion Factor (CF) and it is measured in electrons per digital number.

3.2.3 Exposure sweep setup

In order to extract the image sensor parameters, a sweep of exposure is performed. To do so, a constant light level that enables the sensor to reach the saturation at the maximum integration time is chosen. To modulate the exposure, the integration times are swept by modifying the number of rows in reset. In addition, multiple frames are collected for each integration time to evaluate and average the temporal noise.

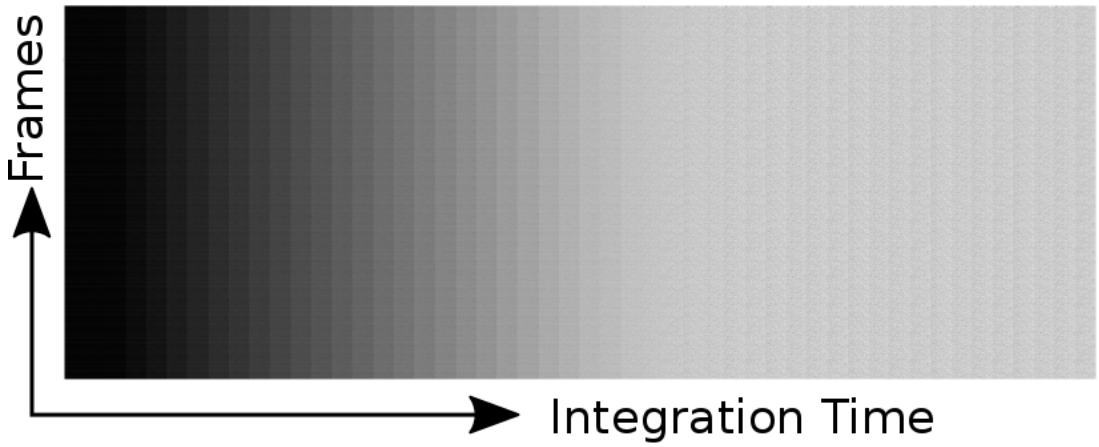
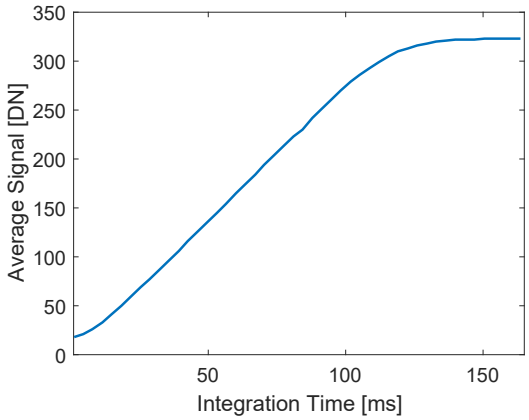


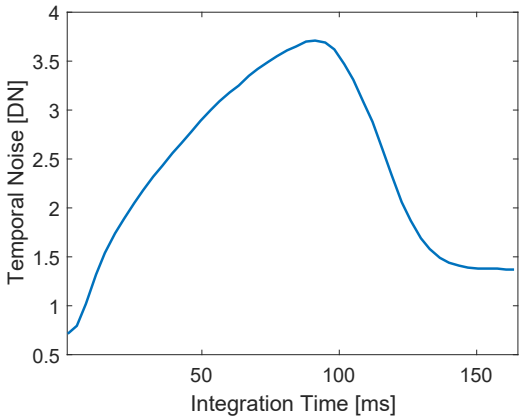
Figure 3.9: Mosaic of multiple frames collected at increasing integration times of a standard pixel.

Figure 3.9 shows the collected mosaic of the baseline window of the standard 4T pixel version. Here, 50 increasing exposures of 40 frames each were captured. Each part of the frame of the considered variation is cut and pasted into this mosaic. The result is an image that is dark for low integration times and bright for higher integration times showing that the sensor correctly responds to increasing levels of exposure with a brighter image. This is confirmed by

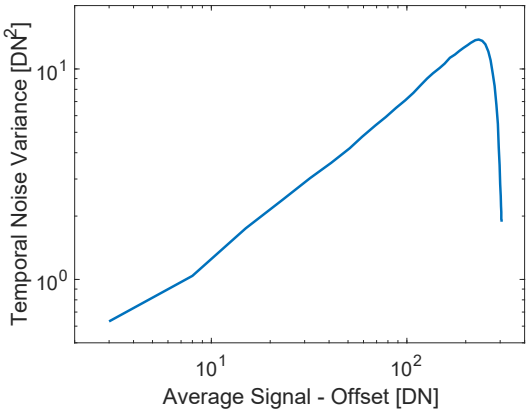
the average signal curve. The temporal noise can be extracted for each light level of intensity from the frame-to-frame variability.



(a) Average signal in digital numbers vs integration time at constant illumination level for the standard pixel (VB1).



(b) Temporal noise in digital numbers vs integration time at constant illumination level for the standard pixel (VB1).



(c) Temporal noise variance vs average signal on a logarithmic scale (VB1).

Figure 3.10: Measured signal and noise of the VB1 version.

Figure 3.10 shows that the average pixel signal is linear for increasing values of exposure and reaches saturation. The correlation between the average signal and the temporal noise allows extracting information from the sensor on noise, conversion factor, linear full well capacity. This set up is used in the following sections to measure and analyse the manufactured devices.

Table 3.3 summarises the test chip parameters obtained from the light sweep of five different dies each of them containing a chip. These parameters are obtained similarly to the EMVA1288 standard. The dark level is the offset level in the dark measured in LSB. The read noise is obtained by measuring the temporal noise in the dark at the minimum integration time in LSB and it is multiplied by the conversion factor to obtain a value in electrons. The conversion

Table 3.3: VB1 Baseline measured parameters

Version	**VB1 Baseline**					
Chip	1	2	3	4	5	**Avg**
Noise[e]	11	11	8	14	25	**14**
CF[e/LSB]	16	17	14	17	19	**16**
LFW[e]	3670	3907	3206	3751	3826	**3672**
Sat[e]	4790	5115	4267	5055	5243	**4894**
DSNU[%]	3.51	2.89	2.65	2.56	10.24	**4.37**
PRNU[%]	4.47	4.59	4.42	4.56	10.45	**5.70**
DR[dB]	50	51	52	48	44	**49**
SNR[dB]	36	36	36	36	36	**36**
DC[e/s]	151	142	120	140	150	**141**

factor is extracted from the regression in the central region of Figure 3.10c which correlates the signal in LSBs and the noise variance as explained in section 3.2.2. The conversion factor is measured in $\frac{e}{LSB}$. The Linear Full Well is calculated as the signal in LSBs at the maximum of the temporal noise multiplied by the conversion factor. The saturation in electrons is calculated as the maximum signal level multiplied by the conversion factor.

The Dark signal non-uniformity (DSNU) is calculated as the ratio between the average FPN in the dark and the signal in the dark at the minimum integration time multiplied by 100. The Photo response non-uniformity (PRNU) is calculated as the per cent ratio of the FPN and the signal evaluated at 50% of the signal saturation. The Dynamic Range is calculated in dB between the LFW and the read noise while the Signal-to- Noise Ratio (SNR) is the ratio in dB between the signal and the noise evaluated at 50% of the signal saturation. In addition, the table also reports the measured dark current for each chip version.

The temporal noise is high and particularly high if compared with the state of the art pixels. The high conversion factor is due to the mismatch of the ADC compared to the analogue output signal. This means that a lower number of codes is available to represent the signal, hence the high conversion factor. Finally, the DSNU and PRNU are also very high showing the immaturity of the process technology. The contributions of FPN for this sensor. In the chip versions presented in this thesis, the readout circuitry is the same so that it could be re-utilised for each test chip. Figure 3.11 shows the contributions of fixed pattern noise for the VB1 baseline version.

In the Figure, the total FPN (blue) was decomposed in Row FPN (red), Column FPN (yel-

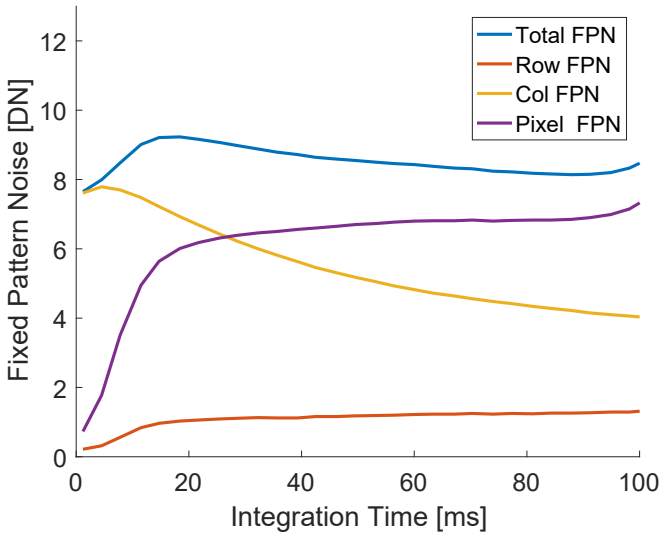


Figure 3.11: FPN contributions vs integration time (VB1 baseline).

low), Pixel FPN (violet) for the range of integration times where the pixels are sensitive to light. For low integration times, the column FPN gives the strongest contribution of pattern noise. The column FPN is also one of the most visible as the human eye is very sensitive to this kind of pattern. This analysis suggests that the column readout circuit could be improved. Furthermore, a measurable row FPN is also present in this analysis. The readout circuitry was not optimised for noise purposes. The main objective of the circuits was to mitigate the risks of failure and to have a layout as compact as possible for future applications in the Awaiba products. The high level of FPN masks the pixel FPN and, for this reason, FPN analysis will not be further conducted for the other variations presented.

3.3 Hybrid Pixel Isolation

In order to reduce the dark current, previous works available in the literature show that the STI was removed by completely surrounding the photodiode with a different layer (p-well or polysilicon guard ring). In a standard pixel, the STI surrounds the photodiode as it is needed for electrical isolation especially close to the transistors. The p-well layer provides less isolation compared to the STI and, hence, it cannot be used to isolate the in-pixel transistors. A hybrid approach is here proposed and consists in using the p-well to provide isolation of neighbour photodiodes and STI to provide isolation where the transistors are present.

Figure 3.12 shows how the isolation is granted for neighbour photodiodes. The STI also

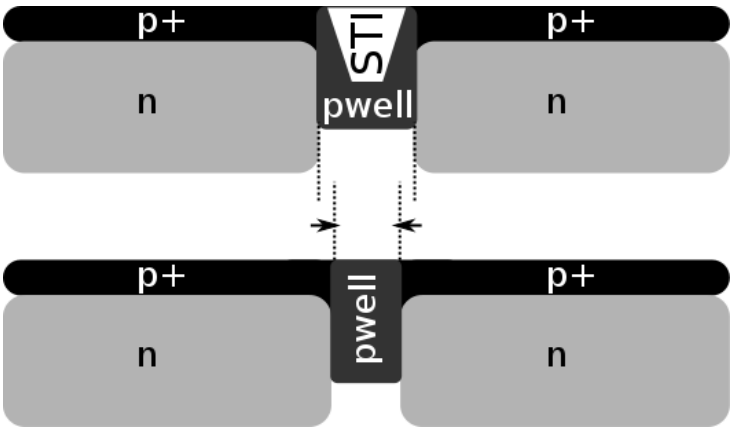
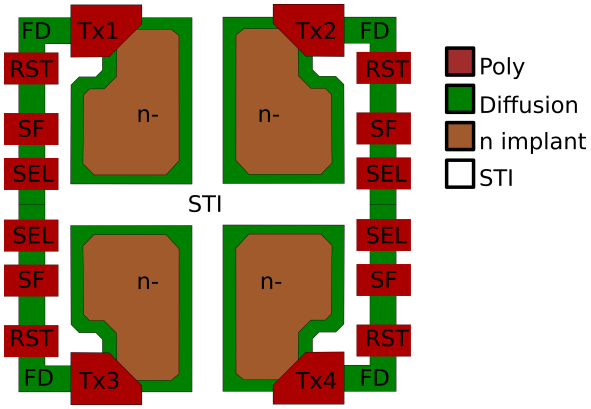
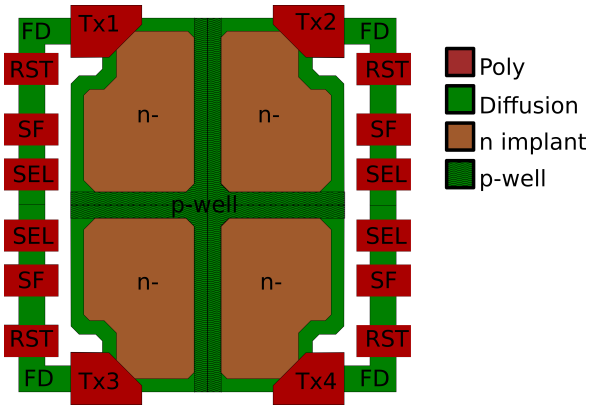


Figure 3.12: STI and p-well isolation for neighbour photodiodes.

occupies more area on the Silicon surface compared to the p-well. The advantage is that the n-doped region of the photodiode can be further extended to increase the pixel fill factor. In order to use this isolation, a different arrangement of the pixels should be considered. Two blocks of pixels were designed. The first with STI and the second without STI. This is possible thanks to a particular arrangement of the pixel layout where two sides of the photodiodes are designed close to each other.



(a) VB3 baseline (STI).



(b) VB2 baseline (p-well).

Figure 3.13: Layout comparison of VB2 and VB3. A block of four 4T pixels with STI and p-well isolation is shown for each version.

Figure 3.13 shows the pixel layouts of the STI (VB3) and p-well (VB2) isolated pixels. Two different pixels are used for comparison. The first with STI which is shown in Figure 3.13a and the second *STI-less* with this proposed hybrid approach shown in Figure 3.13b. The active n-diffusion is in brown, the transistors are in red and the diffusion is in green. In the first case, the photodiodes are separated by the STI while in the second case they are separated by the p-well. As the design rule for the p-well separation is more relaxed compared to the one for the

STI minimum width, the photodiodes can be designed of a higher area in the p-well separation layout thereby achieving a higher fill factor. In the next section, the dark current reduction and the full well capacity increase of the p-well isolated pixels compared to the STI isolated pixels will be evaluated for test chips manufactured in the LFoundry 110 nm CMOS image sensor process technology.

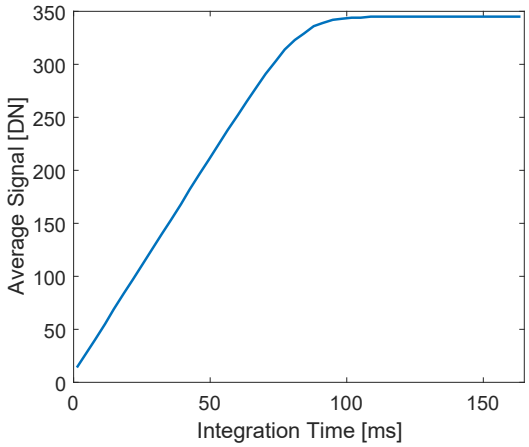
3.4 Experimental results

In this section, to compare the effect of the STI and the p-well isolation on the dark current, the experimental results from the test chips VB2 (p-well) and VB3 (STI) are presented. The two manufactured chip versions were first measured and their photoresponse curve evaluated. As mentioned previously, the process technology was novel and the pixel functionality had to be verified before comparing any result.

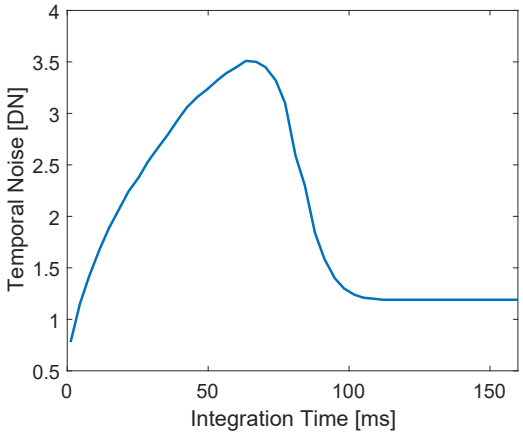
Figure 3.14 shows the photoresponse of the STI isolated pixel version. The curve plots the signal in Digital Numbers (DN) on the left axis and the temporal noise standard deviation on the right axis versus the integration time at a constant light level. The constant light was provided with a green LED centred at a wavelength of 550 nm (green) and with a power of 1.97 $\mu W/m^2$. Both the signal and the temporal noise are evaluated from a set of 40 images for each data point on a window of 186-by-84 pixels. The signal curve shows that the signal correctly increases linearly for increasing integration times. A higher integration time at the same light level, in fact, generates more electron-holes couples in the photodiode. The curve also shows a saturation level which represents the maximum photodetectable signal for this system.

The chip utilises an external analogue-to-digital converter with a 10-bit precision. Unfortunately, the signal has only a 300 DN swing because the sensor output range does not match the input range of the converter. Temporal noise is also expressed in DN, it reaches a maximum and decreases when the pixel saturates. This is because, in saturation, the photodiode is full of charge. In this condition, there is almost no possibility for the signal to vary over time as it reaches its maximum value. The linear full well capacity is evaluated when the temporal noise is at its maximum value ensuring a linear photoresponse.

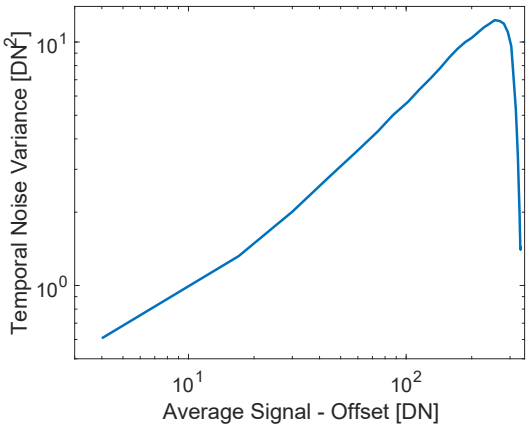
Figure 3.15 shows the photoresponse curve of the p-well isolated version. The photon transfer theory [28, 97] provides techniques to extract the CMOS image sensor parameters from the



(a) Average signal in digital numbers vs integration time at constant illumination level for the STI pixel (VB3 baseline).



(b) Temporal noise in digital numbers vs integration time at constant illumination level for the STI pixel (VB3 baseline).



(c) Temporal noise variance vs average signal on a logarithmic scale (VB3 baseline).

Figure 3.14: Measured signal and noise of the VB3 version.

signal and the temporal noise in digital numbers. It is important that the sensors are correctly working and that they have a linear behaviour in their sensitivity region.

Tables 3.4 and 3.5 compare the measured parameters for both the p-well (VB2) and STI (VB3) baseline versions respectively. The measured parameters are similar with the exception of the full well capacity. In addition, the p-well pixel has also a point more of DR and SNR.

These parameters depend on process variations. For this reason, the analysis was performed on a number of test chips. The chips measured at the LFoundry premises come all from the same processed wafer. Within the wafer, the chips were chosen in locations that were as close as possible. The measured parameters are reported in the following variability charts.

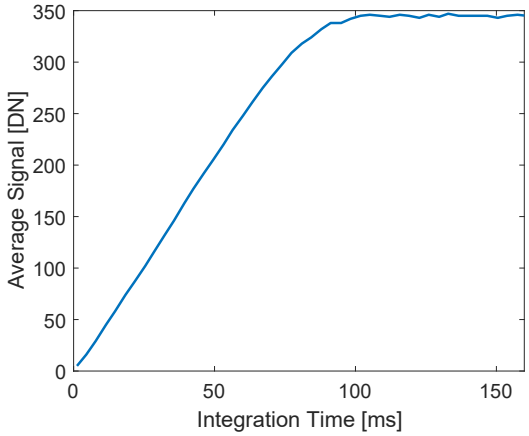
In Figure 3.16, each black dot represents the measured average value of the linear full well capacity extracted from similar curves to the one presented in Figures 3.14 and 3.15 except that

Table 3.4: VB2 Baseline measured parameters

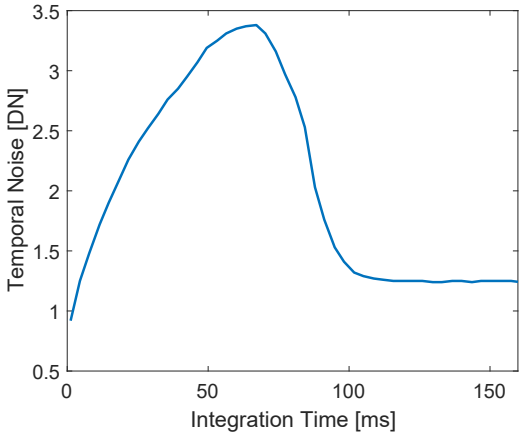
Version	**VB2 Baseline**					
Chip	1	2	3	4	5	**Avg**
Noise [e]	17	17	14	13	15	**15**
CF [e/LSB]	23	22	20	20	21	**21**
LFW [e]	6034	5761	5664	5461	5284	**5641**
Sat [e]	8005	7311	7014	6842	7098	**7254**
DSNU [%]	1.86	2.29	2.63	2.16	2.53	**2.29**
PRNU [%]	1.46	1.37	1.47	1.01	1.44	**1.35**
DR [dB]	51	50	52	52	51	**51**
SNR [dB]	38	38	38	38	37	**38**

Table 3.5: VB3 Baseline measured parameters

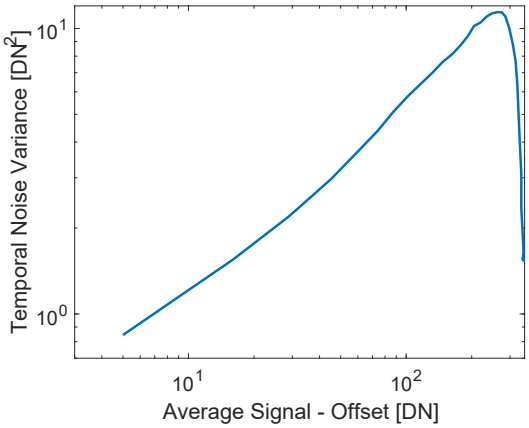
Version	**VB3 Baseline**					
Chip	1	2	3	4	5	**Avg**
Noise[e]	12	12	15	13	15	**14**
CF [e/LSB]	20	20	22	20	21	**20**
LFW [e]	5137	5449	5311	5116	5318	**5266**
Sat [e]	6761	6817	4904	6677	6855	**6403**
DSNU [%]	2.20	2.66	2.88	2.42	2.38	**2.51**
PRNU [%]	1.26	1.45	3.98	0.88	1.68	**1.85**
DR [dB]	52	53	51	52	51	**52**
SNR [dB]	37	38	37	37	37	**37**



(a) Average signal in digital numbers vs integration time at constant illumination level for the p-well isolated pixel (VB2 baseline).



(b) Temporal noise in digital numbers vs integration time at constant illumination level for the p-well isolated pixel (VB2 baseline).



(c) Temporal noise variance vs average signal on a logarithmic scale (VB2 baseline).

Figure 3.15: Measured signal and noise of the VB2 baseline version.

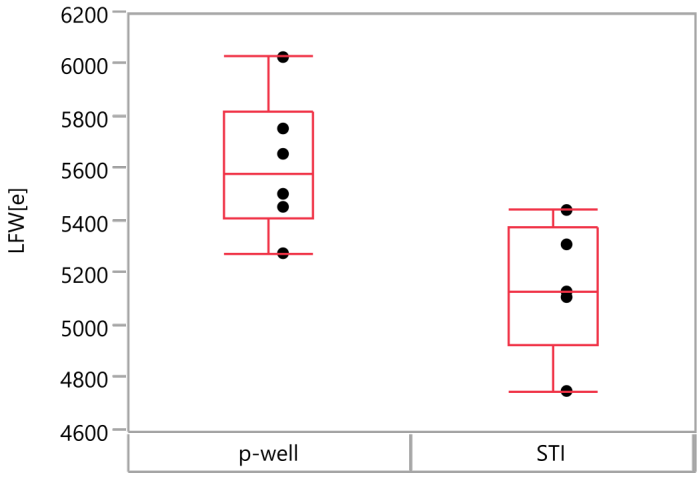


Figure 3.16: Statistical variation of the linear full well expressed in electrons and variability box plot for measured STI and p-well isolated pixels.

they were extracted from a different test chip. The red box plot highlights the median value and the statistical distribution of the samples. This analysis confirms that the median value of the full well capacity is higher for the p-well isolated photodiode.

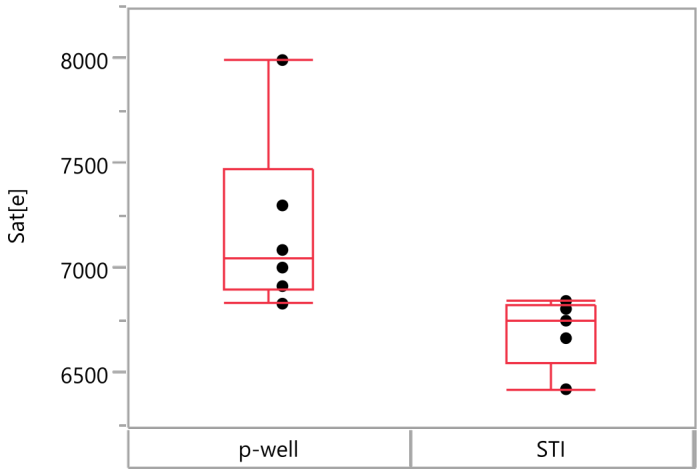


Figure 3.17: Statistical variation of the saturation expressed in electrons and variability box plot for measured STI and p-well isolated pixels.

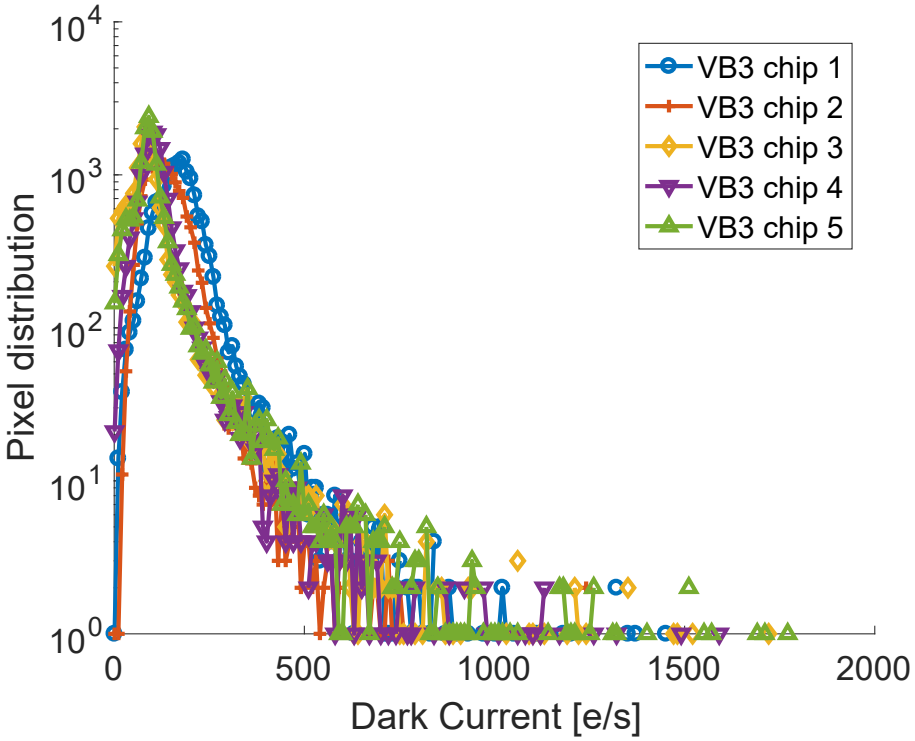
Similarly, in Figure 3.17 each black dot represents the average value of the saturation level for the measured chip. This shows that the p-well isolated photodiode has a higher saturation value. The increase in saturation is confirmed and of approximately 400 electrons. The larger photodiode area of the p-well isolated version shows an increase of the pixel capability to accommodate electrons.

Table 3.6 compares the extracted linear full well and saturation values of the presented curves to their respective fill factor, photodiode area and perimeter. The increase in fill factor is correlated to the full well capacity and to the saturation values. This is coherent with the expectation of an increase in the saturation value for a photodiode with a higher active area. The increase in saturation did not scale with the fill factor. An increase of the fill factor of 19% only gives an increase in saturation of 12 %. This could be limited by the shape of the photodiode which is not rectangular.

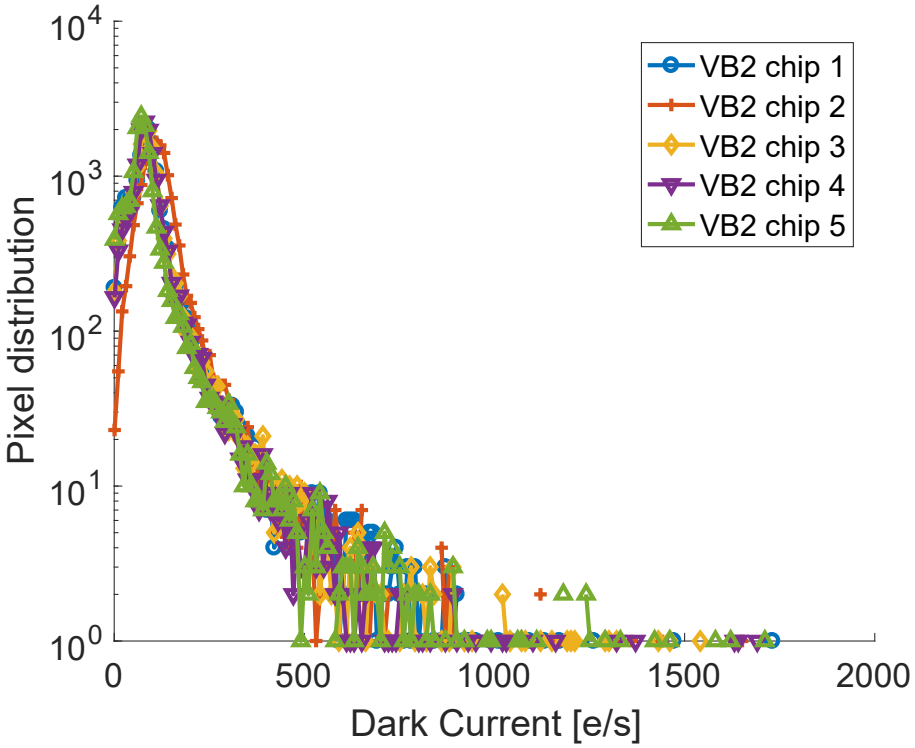
Table 3.6: Comparison between VB2 and VB3

Version	LFW [e]	Sat [e]	PD Area [μm^2]	Perimeter [μm]	FF [%]
VB3 base	5266	6403	1.69	5.63	29
VB2 base	5641	7254	2.08	5.88	36
Δ [%]	7	12	19	4	19

The increase in full well capacity is already a promising result, however, the main reason for removing the STI is to reduce the dark current. In order to evaluate the benefits in terms of dark current, dark current measurements were undertaken on these manufactured test chips.



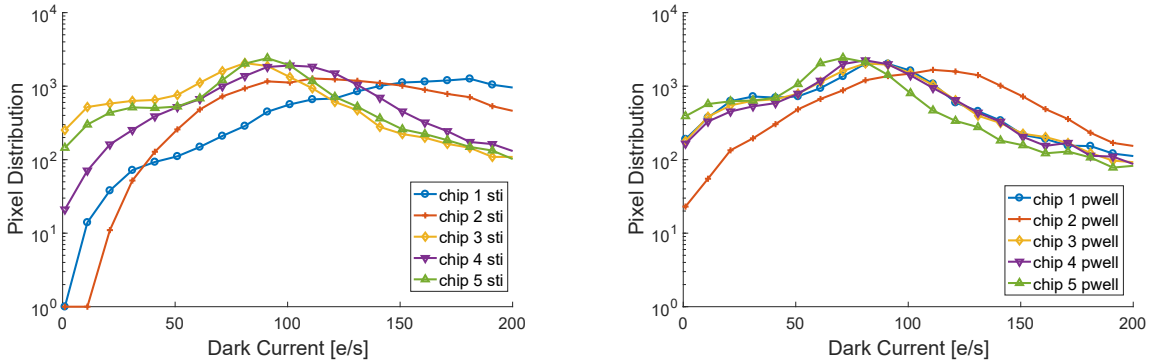
(a) STI pixel dark current distributions.



(b) P-well pixel dark current distributions.

Figure 3.18: Dark current distribution of STI and p-well isolated pixels. Measured at 60 Celsius.

Figure 3.18 illustrates the dark current distribution for five test chips manufactured within the same wafer. The distributions were evaluated for windows of 186-by-84 pixels at 60 Celsius. These histograms show the main peak of the dark current and the tails of the dark current of the leaky pixels. The histograms are plotted on semi-logarithmic axes to better show the tails. In order to evaluate the peaks, logarithmic histograms focusing on the peak region are presented.



(a) STI pixel dark current distributions.

(b) P-well pixel dark current distributions.

Figure 3.19: Dark current distribution of STI and p-well isolated pixels on a logarithmic scale. Measured at 60 Celsius.

Figure 3.19 shows the distribution of the STI and p-well isolated pixels respectively on a logarithmic scale. In addition, the histograms are reporting dark current values up to 200 electrons to focus on the peaks. In Figure 3.19b the distributions are shifted towards the left compared to Figure 3.19a.

Table 3.7: Dark current comparison between VB2 and VB3 baselines.

Version	**VB3 base DC [e/s]**	**VB2 base DC [e/s]**
Chip 1	183	104
Chip 2	144	128
Chip 3	106	103
Chip 4	121	101
Chip 5	113	90
Avg	**133**	**105**

Table 3.7 reports the mean value of the dark current for the STI (VB3) and p-well (VB2) isolated pixels respectively. The p-well isolated pixels shows that the dark current decreases on average from 133 to 105 electrons. This reduction of the dark current is achieved while increasing the fill factor and, hence, the full well capacity given all the other parameters. By

increasing the photodiode area, the dark current should increase. Instead, with this isolation method, the dark current is decreased.

Table 3.8: Dark current % comparison of VB2 and VB3 with Photodiode Area and Fill Factor.

Version	DC [e/s]	PD Area [μm^2]	Perimeter [μm]	FF [%]
VB3 base	133	1.69	5.63	29
VB2 base	105	2.08	5.88	36
Δ [%]	-27	19	4	19

Table 3.8 shows the percentage difference between the average dark current of the STI and p-well isolated pixels. The net decrease in dark current is 27% despite the increase in photodiode area and perimeter. If the increase in photodiode area is taken into account, the actual estimated dark current reduction for two pixels having the same photodiode area would be 56%.

This is a first preliminary result which shows that, in addition to achieving a larger full well capacity, the approach of removing the STI region has a benefit on the dark current distribution. In order to better study the effect of the STI and p-well isolation on the dark current, further experiments are undertaken and reported in the next sections.

3.4.1 Photodiode interaction with the STI

In terms of dark current, the experimental results obtained in the previous section show a performance increase when the STI region is removed. However, the optimal distance of the photodiode n-implantation from the STI region is a design rule suggested by LFoundry. This means that this distance is already optimised in terms of the trade-off between the fill factor and the dark current. For this reason, variations of the pixels were designed to evaluate the impact of a wider and narrower photodiode n-implantation. Ensuring a higher distance of the n-implant from the STI region should let the photodiode collect fewer charges generated in the STI. Unfortunately, the n-region of the photodiode cannot be too narrow as this also reduces the fill factor and subsequently the full well capacity. The n-implant can be made larger to increase the fill factor. However, this means that the photodiode n-region will be closer to the STI region which will result in a stronger interaction of the photodiode with the STI interface. To study these interactions, two pixel variations were designed: the first has a photodiode n-implant reduced of 50 nm from the baseline while the second has an n-implant region increased of 100

nm. These numbers were chosen because the standard separation between the photodiode and the transistor diffusion is 300 nm. An increase of 100 nm represents a 30% reduction of the diffusion separation distance.

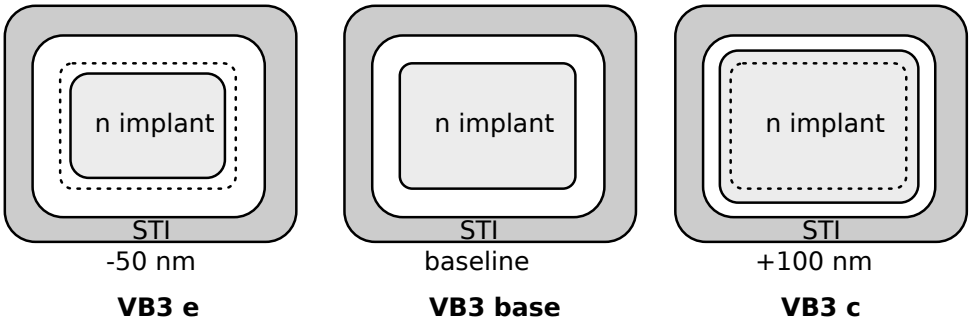


Figure 3.20: Designed variations of the n-implant toward the isolation region.

Figure 3.20 presents a schematic representation of the designed variations. The baseline is in the centre, on the left the photodiode n-implant is shrunk by 50 nm while on the right it is expanded by 100 nm. Experimental measurements were undertaken to extract the electro-optical performance of these newly introduced variations and are reported hereafter.

Table 3.9: Measured performance of VB3 variation e.

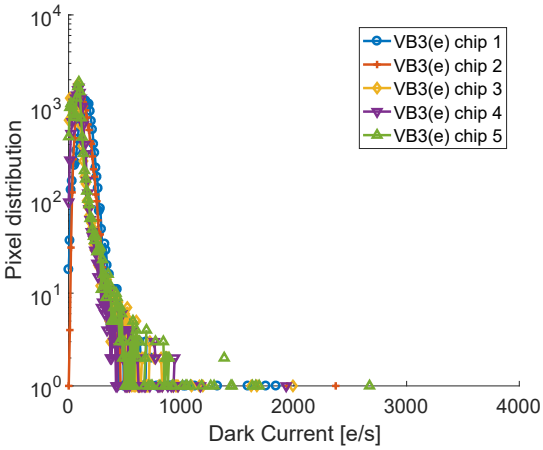
VB3 variation e						
Chip	1	2	3	4	5	**Avg**
Noise [e]	12	13	15	14	15	**14**
CF[e/LSB]	20	20	22	20	21	**21**
LFW[e]	4837	5156	4735	5160	5003	**4978**
Sat[e]	6372	6474	4533	6378	6493	**6050**
DSNU[%]	2.47	3.31	3.16	2.50	2.29	**2.75**
PRNU[%]	2.46	2.08	5.26	1.43	2.41	**2.72**
DR[dB]	52	52	50	51	50	**51**
SNR[dB]	37	37	36	37	37	**37**

Tables 3.9 and 3.10 report the measured performance for the variations VB3 (e) and VB3 (c) respectively. As the n-implant photodiode area increases, the measured full well capacity increases as well. The only significant difference between these two and the baseline is, in fact, the full well capacity increase and the subsequent small increase of DR and SNR. In addition to these parameters, a dark current measurement was undertaken and the collected histograms are reported.

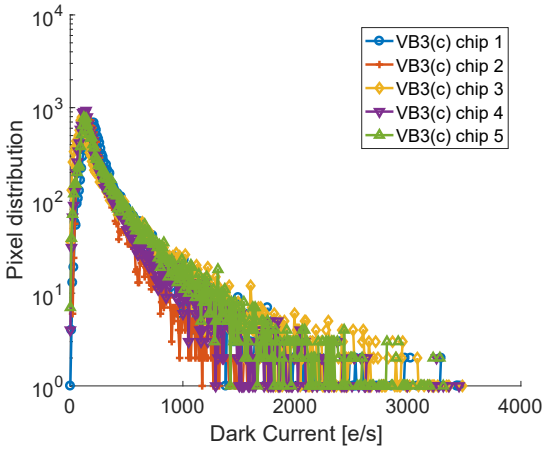
Figure 3.21 shows the histograms of the STI isolated pixel variations plotted on a logarith-

Table 3.10: Measured performance of VB3 variation c.

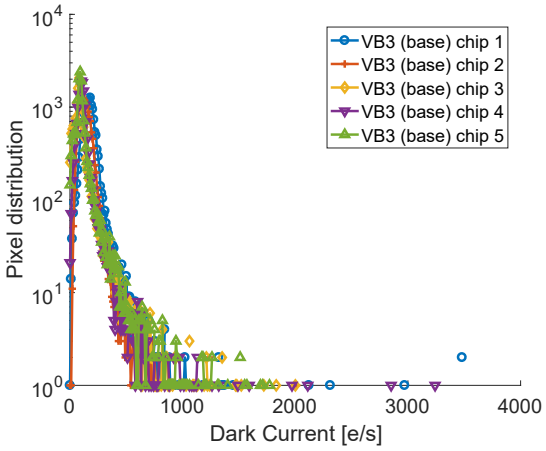
VB3 variation c						
Chip	1	2	3	4	5	**Avg**
Noise [e]	12	13	15	14	16	**14**
CF[e/LSB]	20	20	22	20	21	**20**
LFW[e]	6054	5843	5962	6308	6268	**6087**
Sat[e]	7587	7714	5627	7514	7669	**7222**
DSNU[%]	2.30	3.33	2.56	2.56	2.30	**2.61**
PRNU[%]	1.15	1.39	3.72	0.86	2.18	**1.86**
DR[dB]	54	53	52	53	52	**53**
SNR[dB]	38	38	38	38	38	**38**



(a) STI pixel with n-implant reduced of 50 nm (VB3 c).



(b) STI pixel with n-implant increased of 100 nm (VB3 e).



(c) STI pixel (VB3 baseline).

Figure 3.21: Dark current distributions of n-implant variations in STI isolated pixels (logarithmic scale). Measured at 60 Celsius.

mic scale. Unlike the histograms in Figure 3.19 where the pixel information was extracted from different test chips, these variations are each present on the same test chip and they are easier to

compare. Figure 3.21a shows a slight shift of the distribution towards the left compared to the baseline which does not appear significant. However, Figure 3.21b shows a different behaviour of the dark current. The peaks shift towards the right but, more importantly, the tails become relevant. Pushing the implantation towards the STI has a double effect. From one side the main peak of the dark current is shifted towards higher values and from another side, the queue of the histogram is higher. The probability of having pixels with a higher dark current is hence increased. In order to have a numerical estimation of the dark current increase, a statistical analysis of this effect is reported by evaluating the mean of the distributions.

Table 3.11: Dark current comparison of VB3 variations.

Version	VB3 e DC [e/s]	VB3 base DC [e/s]	VB3 c DC [e/s]
Chip 1	158	183	338
Chip 2	132	144	234
Chip 3	77	106	321
Chip 4	94	121	269
Chip 5	85	113	332
Avg	**109**	**133**	**299**

Table 3.11 shows the measured dark current average values for the n-implantation variations. The average dark current explodes in version VB3 c. The dark current is almost three times as high as the baseline.

When the distance is increased, the dark current is reduced by 20 e/s which is not a significant decrease. However, when the distance is shrunk, the dark current increase is relevant. The result is a dark current of approximately 300 e/s which is almost three times higher compared to the baseline mean value. The objective of increasing the fill factor and, hence, the full well capacity may not justify the choice of using a larger photodiode. Recalling equations 2.7 and 2.8, the dark current is proportional to the photodiode area and, hence, Table 3.12 shows the dark current of each variation with respect to photodiode area, Fill factor and perimeter.

If it is assumed that the dark current is mainly related to the photodiode area, an estimation of the dark current could be made based on the measurements of version VB3e and VB3 baseline which have an area of 1.40 and 1.69 μm^2 respectively.

Figure 3.22 shows the measured average dark current levels for each of the variations. A linear fitting is shown in the image assuming that the dark current would scale linearly with

Table 3.12: Dark current comparison of VB3 variations with PD area and Fill factor.

Version	DC [e/s]	FF [%]	PD Area [μm^2]	Perimeter [μm]
VB3 e	109	24	1.40	5.04
VB3 base	133	29	1.69	5.63
VB3 c	299	38	2.22	6.13

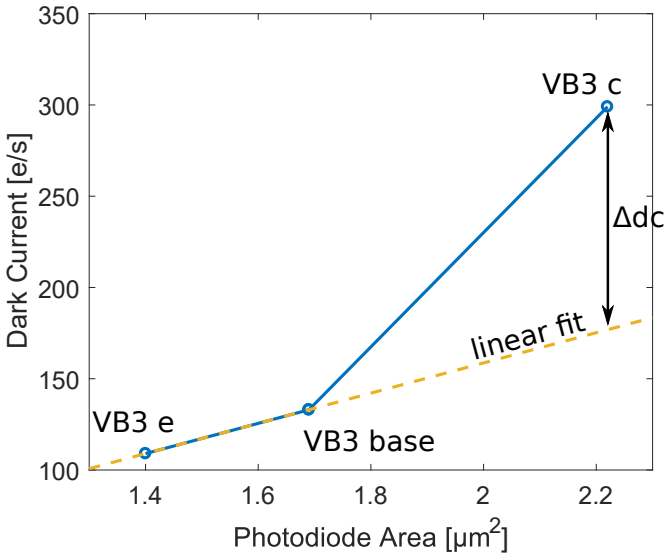


Figure 3.22: Dark current vs Photodiode Area for the variations and linear fitting.

the area. However, the increase in dark current is higher than the one expected from the linear fitting. In fact, by fitting, a dark current of 175 e/s while the measured dark current is 300 e/s. This additional dark current contribution, Δdc, may come from the interaction with the STI. In fact, when the n-implant of the photodiode becomes closer to the STI region, it collects the extra charges generates in the defective region. The increase of the tail in the histogram for version VB3 c is an additional indication of this phenomenon. The number of hot pixels, i.e. the pixels with high dark current, can be compared to evaluate the tails. By observing the mean peaks, these are centred at the mean of their dark current and are significantly decreased for dark current values above 500 e/s. In this analysis, the number of pixels with a dark current higher than 500 e/s is evaluated for each version.

Table 3.13 shows the number and the percentage of hot pixels for the three pixel variations. It can be observed that the hot pixels double from version VB3 e to VB3 baseline. More importantly, this number literally explodes for version VB3 c. This is probably due to the interaction with the STI region. In order to verify that this not purely due to the increase of

Table 3.13: Hot pixels ($> 500\ e/s$) comparison of VB3 variations.

Version	VB3 e	VB3 base	VB3 c
Chip 1	51	156	2427
Chip 2	16	58	1037
Chip 3	66	146	2769
Chip 4	41	98	1714
Chip 5	74	160	2647
Avg	**50**	**124**	**2119**
Avg [%]	**0.32**	**0.79**	**13.56**

the photodiode size, another analysis was undertaken on the p-well isolated pixels and it is presented in the next section.

3.4.2 Photodiode interaction with the p-well

A similar experiment was undertaken with the p-well isolated pixels. In the previous section, an analysis of the n-implant variations showed that expanding the photodiode n-implantation towards the STI let the dark current increase. A preliminary analysis on the dark current, show that this increase is not directly proportional to the photodiode area and that the number of hot pixels is significantly increased for those pixels. To verify that this dark current increase is related to the STI interaction and not to the photodiode area, in this section, a similar experiment is conducted on the p-well isolated pixels. In the p-well isolated pixel baseline, the n-region is already designed line-to-line with the p-well to obtain the maximum fill factor. In order to further increase the n-implantation, the p-well width isolating the two photodiodes should be reduced. For the purpose of this experiment, a pixel variation was designed. In this version, the p-well is shrunk by 40 nm while the n-implant region is increased by 40 nm as well. While these can appear as small increments, they are really pushing the technology. The increment of 40 nm of the n-implant means that the photodiodes are only separated by 260 nm of p-well. The process engineers in LFoundry advised against pushing the layer further as this may have caused problems in the manufacturing process.

Pixel versions diagrams are shown in Figure 3.23. On the left, the schematic version of the p-well variation is shown while, on the right, the version with both the p-well and n-implantation is illustrated. The measurements were undertaken on five different chips also for this pixel

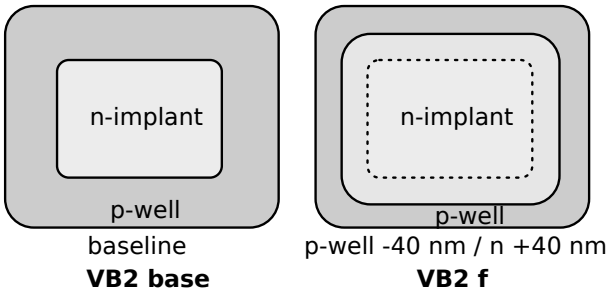


Figure 3.23: Designed variation of the n-implant layer of the p-well isolated pixels.

variation. However, for brevity, only the averaged measurements are reported and compared to the baseline.

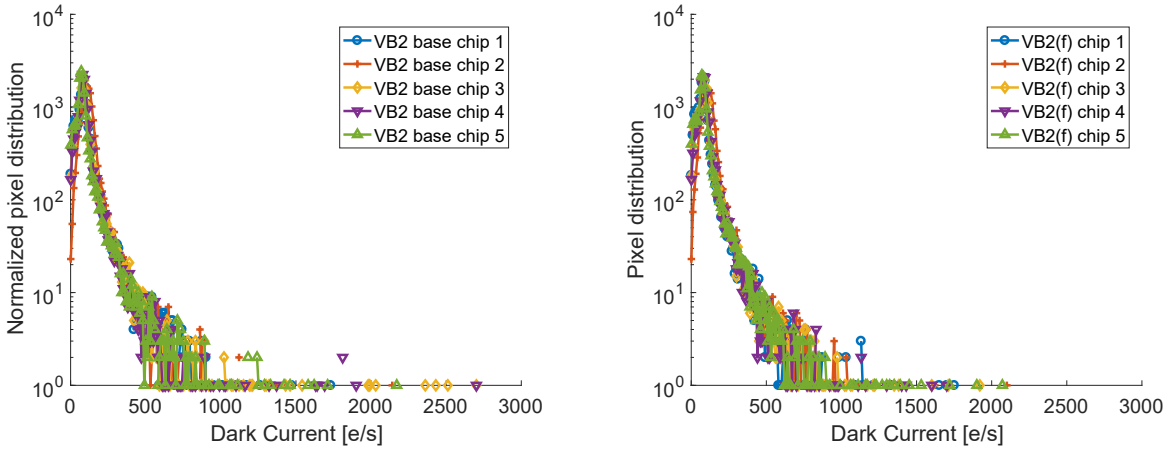
Table 3.14: VB2 variation parameters compared to baseline.

Version	VB2 base	VB2 f
Noise[e]	15	16
CF[e/LSB]	21	21
LFW[e]	5641	5954
Sat[e]	7254	7460
DSNU[%]	2.29	2.13
PRNU[%]	1.35	1.43
DR[dB]	51	51
SNR[dB]	38	38

Table 3.14 shows that the measured parameters are almost identical for the two versions apart from a slight increase of the full well capacity which it is expected as the area of the photodiode is increased. It is worth analysing the measured dark current histograms of the variation.

Figure 3.24 shows the dark current histogram for the two p-well isolated pixel variations plotted on a logarithmic scale and measured at 60 Celsius. The dark current distributions are almost identical. In particular, subfigure 3.24b plots the histograms of the pixel variation where the photodiode n-implant was increased and does not show an increase of the dark current tail as it was demonstrated for the STI version. If the mean value of the dark current and the number of hot pixels are evaluated for these variations, Table 3.15 can be obtained.

As the VB2 f pixel variation has a slightly higher photodiode area, a higher mean value of dark current was expected. However, given the high dark non-uniformity and noise level of these sensors, a small change in dark current could be masked. With a mature process and a



(a) VB2 baseline pixel.

(b) VB2 f pixel.

Figure 3.24: Dark current distributions of the n-implant variation in p-well isolated pixels (logarithmic scale). Measured at 60 Celsius.

Table 3.15: VB2 Dark current compared to baseline with photodiode area and fill factor.

Version	DC [e/s]	N Hot	PD Area [μm^2]	Perimeter [μm]	FF [%]
VB2 base	105	118	2.08	5.88	36
VB2 f	103	102	2.16	6.01	37

better readout, it would be possible to observe the dark current increase. For the purpose of this work, if the number of Hot pixels, N Hot, is observed, it is possible to conclude that this is not increasing as it was in the case of the STI version. This shows that, by removing the STI, the dark current is reduced and the number of hot pixels is lowered.

3.4.3 Analysis of the results

Experimental results have shown that if the n-region of the photodiode is expanded towards the STI region, the dark current increases. This increase does not occur for the p-well pixel version. However, the fill factor of the p-well pixel baseline version is 36 % which is similar to the STI pixel variation with increased photodiode dimension. The photodiode baselines of the two pixel versions were designed as large as possible according to the LFoundry design rules. This causes the photodiodes to have a different area. If Equations 2.7 and 2.8 are recalled, the dark current is dependent on the area. The impact of the STI isolation should be hence demonstrated by comparing pixels with similar photodiode area. These are the VB2 f p-well isolated variation with an increased n+ of 40 nm and the VB3 c STI variation with 100 nm larger photodiode

n-implant. To compare the levels of measured dark current for pixels that have a different photodiode area, it can be expressed as a density per unit of area which is usually reported in pA/cm^2 and added to the following table.

Table 3.16: Summary of the STI vs p-well pixel variations.

Version	**VB2**	**VB2**	**VB3**	**VB3**	**VB3**
Variation	**base**	**f**	**e**	**base**	**c**
Isolation	p-well	p-well	STI	STI	STI
FF[%]	36	37	24	29	38
Noise[e]	15	16	14	14	14
CF[e/LSB]	21	21	21	20	20
LFW[e]	5641	5954	4978	5266	6087
Sat[e]	7254	7460	6050	6403	7222
DSNU[%]	2.29	2.13	2.75	2.51	2.61
PRNU[%]	1.35	1.43	2.72	1.85	1.86
DR[dB]	51	51	51	52	53
SNR[dB]	38	38	37	37	38
DC [e/s]	105	103	109	133	299
N Hot [%]	0.76	0.65	0.32	0.79	13.56
DC [pA/cm^2]	813	773	1266	1279	2187

Table 3.16 compares side-by-side the measured parameters of the pixels presented in this chapter. A photodiode with an increased area, in fact, is expected to generate more dark current. The dark current of the STI isolated pixel increased more than expected when the photodiode n-implant is moved towards the STI region. In addition, the number of hot pixels is twenty times higher compared to the other variations. In order to ensure that this was not an effect related to the increase of the photodiode n-implant, the same methodology was applied to the p-well isolated pixels where the dark current and the number of hot pixels remained low. If the dark current density is compared, the result shows that there is little difference between the baseline and the version VB3 e where the n-implant is moved inwards. The dark current density almost doubles when the n-implant is moved towards the STI. The p-well isolated pixel shows a lower dark current density and a higher full well capacity. From the results presented in this Chapter, it is concluded that the pixel hybrid isolation by means of a p-well is an effective method to reduce the total dark current and to improve the pixels linear full well capacity.

3.5 Summary

In this Chapter, the experiment designed for the purposes of this thesis was first presented. The methodologies used to extract the sensor information like full well capacity and dark current were reviewed and explained. The purpose of this Chapter was to present a novel layout methodology to reduce the dark current. Recalling the literature review of Chapter 2, the process to provide isolation is the main source of dark current in CMOS image sensors and a variety of techniques to reduce the dark current have been explored in the literature. Improving the process technology is an effective way to improve the performance, however, this is a costly approach and not in control of the designer. This motivated the study of alternative dark current reduction techniques through layout optimisation. A hybrid approach was proposed where the STI is retained to isolate the transistor and it is removed in between neighbour photodiodes where the isolation is granted by the means of a p-well. Experimental results are presented demonstrating that the STI causes the dark current distribution average and tail to increase. This can be reduced by employing the proposed hybrid isolation. As an additional advantage, the p-well isolation method has less restricting design rules which enable the n-implant of the photodiode to be designed with a larger area in the same pixel pitch. The higher fill factor is shown to increase the pixel full well capacity. As a final consideration, the pixel layout has a strong impact on the pixel performance and Chapter 4 will explore pixel layout optimisation techniques to enhance the light performance.

Chapter 4

Pixel layout optimisation

In Chapter 3, layout was shown to have a strong impact on the pixel dark current performance. The pixel layout can be optimised to improve its light response. In particular, pixel design requires to consider multiple factors such as the pixel architecture, the process technology and the pixel pitch. In fact, smaller process technologies enable the reduction of the pixel size [95]. With a smaller pitch, a higher resolution can be achieved in the same silicon area or, alternatively, area can be saved to reduce production costs. Collecting light effectively in a small pixel is a challenging task. This Chapter explores the rationale of an optimised layout which improves the pixel light response. The topic is introduced in Section 4.1. The constraints of a readout cell are explored in Section 4.2. In Section 4.3, the layout constraints on a 4T pixel are discussed. Section 4.4 presents the proposed layout arrangement that maximises the fill factor. Experimental results are presented in Section 4.5 and, finally, Section 4.6 summarises the Chapter.

4.1 Introduction

The actual implementation of the pixel layout is usually not disclosed by industries. Unfortunately, the scientific community has more consideration of the design rather than the layout. It is surprising how limited is the number of publications available in the literature given the impact that the layout has on the imaging performance. Shcherback *et al.* [98] studied photodiode sizes and shape variations to find an optimal predictable pixel response. A pixel is composed of a light-sensitive part (the photodiode) and a non-sensitive part (the readout transistors). Fig-

ure 4.1 represents the typical layout constraints in a CMOS image sensor. The chosen pixel pitch typically defines constraints for the readout pitch for both the row and column circuits.

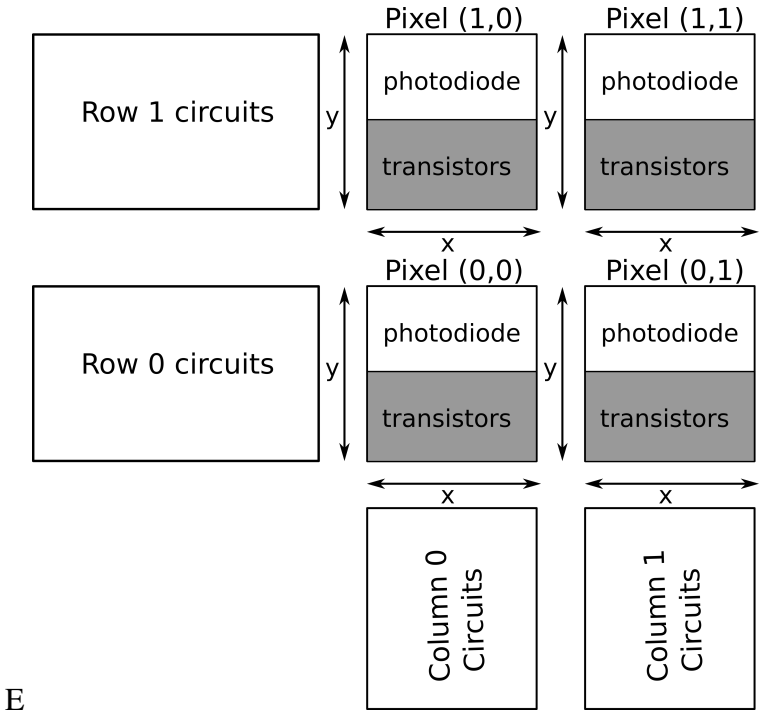


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Figure 4.1: Typical CMOS image sensor layout constraint.

Most researchers have looked to minimise layout area [99, 100]. This is typical in digital design where area occupation of the transistors is a strong constraint. The pixel layout design is a 2-Dimensional constraint problem as both the width and the length of the pixel are fixed once the pitch is defined. The pixel readout is a single dimension constraint problem, as either the row or the column pitch is defined. To start with, it is worth analysing the readout structures and getting inspired by digital design techniques.

4.2 Read-out constraints: 1D

The layout constraints of a circuit can be split into two main branches. The first is a spatial limitation defined by the available area where the transistors can be placed. The number of transistors depends on their size, which in turn depends on the technology chosen. As an example, the readout circuits are both analogue and digital. The process technology rules for analogue and digital are different and limit the minimum cell size. The transistor sizing is typically larger for the analogue transistors as they operate with a thicker gate oxide to sustain a higher supply voltage [101]. The second is a connection limitation and it is related to the num-

ber of metal levels available to connect all the devices. The higher the stack of metals the higher the connection flexibility. However, in the CMOS image sensor technology, a lower stack of metals is preferable as it enables a better light collection [102].

The conventional logic standard cells usually provided in the process development kits, such as AND/OR ports or basic building blocks like flip-flops are designed to satisfy general purpose constraints. When it comes to image sensors, these designs may not be sufficient to satisfy spatial constraints. As an example, in a standard inverter, a typical choice is to have the pMOS transistors wider compared nMOS transistors to compensate for the diversity in mobility of electrons and holes. In addition, standard cells have body connections to power supply and ground on top and on the bottom of the cells which define the standard power rail distance [103]. These are good design choices for a general purpose Application Specific Integrated Circuit (ASIC) as they provide good symmetry of the ports, easy cell stitching and low overall occupied area but may not be sufficient in a CMOS image sensor. To understand the approach, let us revisit a standard AND cell and its layout.

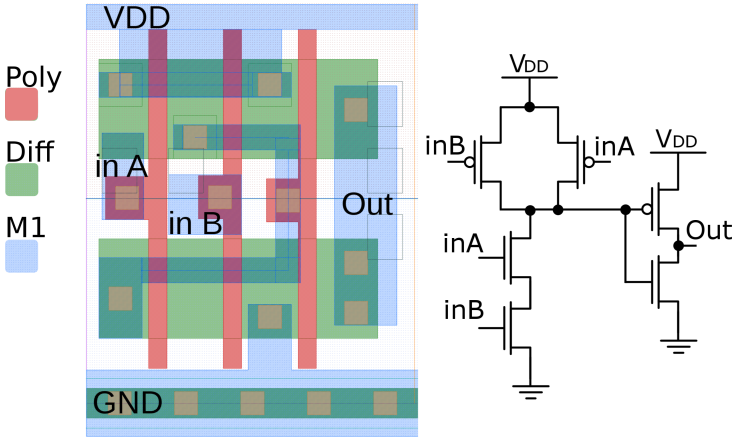


Figure 4.2: AND port (2 inputs) used in the row driver circuitry where the green layer is diffusion, the red layer is polysilicon, the yellow squares are contacts and the blue layer is Metal 1.

Figure 4.2 shows an AND cell used in the readout circuitry. The pitch of this cell was forced to match the one of the pixels (2.4 μm). Here, the green diffusion is identical for the nMOS and the pMOS where the minimum size was used. The ground tap to the substrate is present in the cell while there is no power supply tap to the n-well of the pMOS. The contact has to be placed on the side of the cell as a consequence of the pixel pitch limitation. This philosophy of design and the considerations for this AND cell lead to compact and efficient readout layouts.

Figure 4.3 shows the implemented layout of a group of 4 row drivers. The row driver is

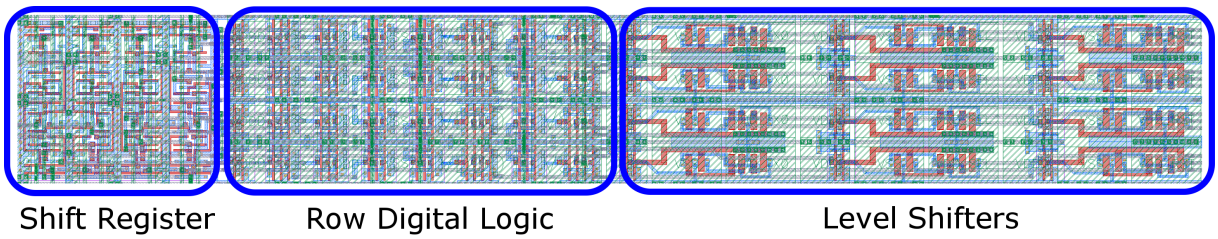


Figure 4.3: Block of four row drivers.

divided into three blocks. The first is a digital shift register which scans the rows sequentially. The second is a digital circuit which enables the right timings for the transfer gate, row selector and reset signals to the pixels. Then, in the third block, the level shifters raise the voltage of these digital signal to the right analogue voltage needed in the pixel. This layout is the final result of a single dimensional design optimisation for the row driver chain. The cell appears compact in the constrained direction and longer in the other one.

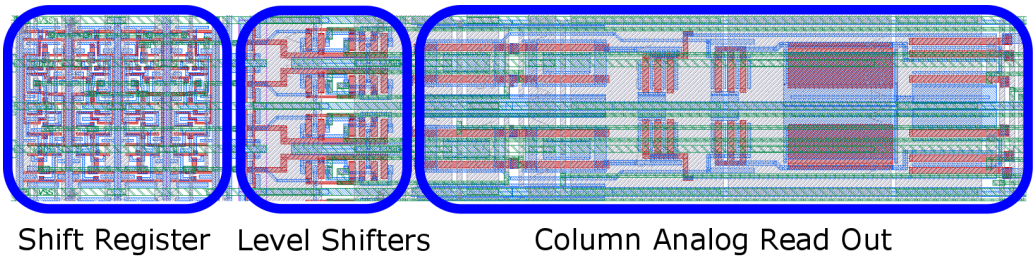


Figure 4.4: Column read out block rotated for display purposes.

A similar layout technique is applied to the column readout which is shown (rotated for display purposes) in Figure 4.4. The column has an analogue readout that samples both the signal and reset values from the pixels. The shift registers sequentially scan the columns generating digital signals that are converted into analogue by the intermediate block of level shifters.

This section briefly explored the layout read out optimisation. For these circuits, one dimension was fixed while the other dimension was used with the flexibility to add electronic circuits. Unfortunately, the pixel has constraints on both the directions and, hence, lower flexibility. The next section will explore the pixel constraints and pixel layout optimisation strategies.

4.3 4T pixel: a 2-D constrained problem

The 4T pixel has a source follower, a row selector switch, a reset switch, a transfer gate and a photodiode connected as in Figure 4.5. The pixel layout derives from a number of considera-

tions:

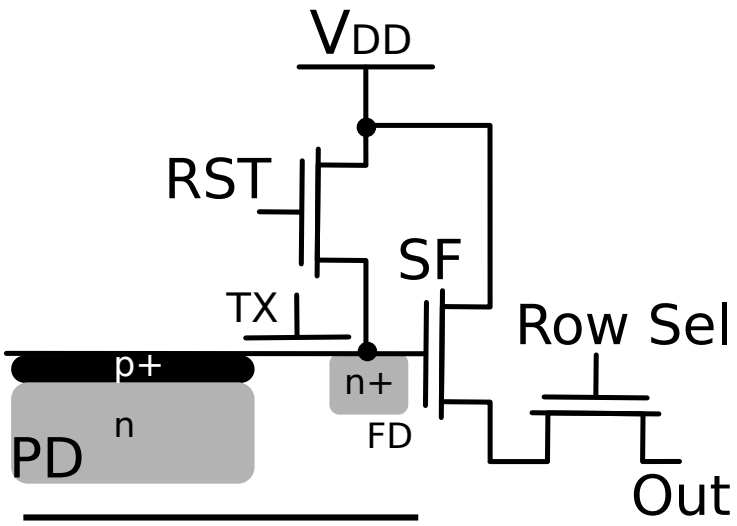


Figure 4.5: 4T pixel schematic

- A larger photodiode collects more light, accommodates more electrons and will increase the performance given all the others parameters.
- The transistors have to be connected to the metal layers driving power supply and to the different read-out signals.
- Metal paths should not cover the photodiode as they would shield the incoming light reducing or destroying the signal.
- The number of metal layers should be low to reduce the optical stack.
- The floating diffusion should be properly sized to maximise the conversion gain without saturating.
- A symmetric layout improves the pixel response uniformity.

The layout task is complex as it has a high number of degrees of freedom. This means that the same schematic design can lead to different layout implementations depending on the designer choices. Hence, it would be beneficial to have synthetic parameters to quickly identify the layout quality in the pixel. In this regard, the fill factor is the figure of merit conventionally used to express the percentage of area occupied by the photodiode. A pixel with a higher fill factor and the same pixel pitch also has a higher photodiode area compared to the one with lower fill factor. These considerations will be used in the following sections to generate different pixel

layouts with the purpose of comparing their performances. For this purpose, the technology and the pixel pitch will be fixed. In particular, the process used is the LFoundry Image Sensor 110 nm process and the chosen pixel pitch is 2.4 μm.

4.3.1 4T fully symmetric pixel layout

The typical approach to compose the pixel matrix is to design a single pixel cell and then copy this cell multiple times to fit the available space of the matrix. The first layout presented is a simple symmetric layout that can meet the aforementioned requirements. First, by observing the schematic in Figure 4.5, it can be noticed that there is no need for a metal connection between the source follower transistor and the row selector switch and these two transistors can be connected by using a single diffusion without contact. This is a common practice in pixel layout. Furthermore, the transfer gate and the reset transistor are connected to the floating diffusion. This is laid out as small as possible to minimise its parasitic capacitance and to improve the conversion gain. This preliminary analysis gives two groups of transistors that are placed in the pixel square.

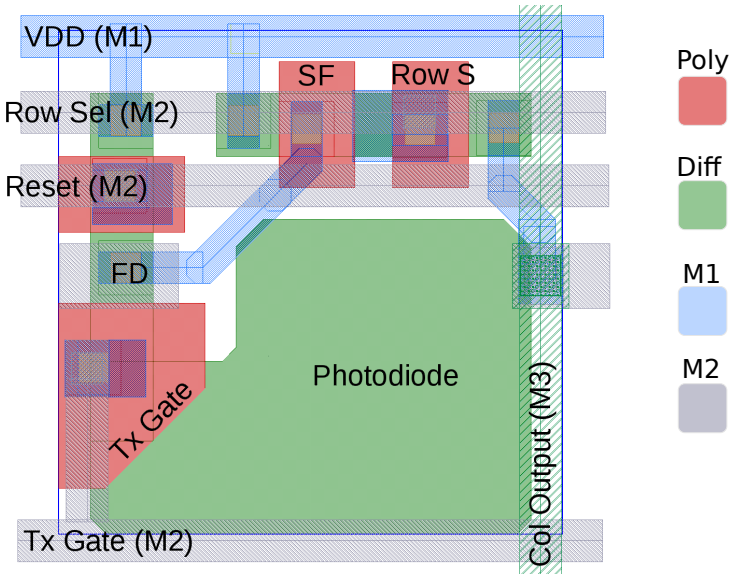


Figure 4.6: Fully symmetric 4T pixel layout 2.4 μm pitch in LFoundry 110 nm technology

Figure 4.6 shows a 4T symmetric pixel. In this example, the power supply is routed in Metal 1 (blue), the row selector, the reset and the transfer gate control signals are routed in Metal 2 (grey) while the column output is taken out from the matrix in Metal 3 (light green). The diffusions are in green. Note that no metal covers the photodiode. The floating diffusion,

FD, is covered by Metal 2 to prevent parasitic photocurrent from exposure. The fill factor of this pixel is of 28 %. In this configuration, there is no ground contact as the p-tap would occupy additional area thereby reducing the fill factor. This choice is possible if the pixel matrix dimension is small enough to avoid a ground gradient and if it has a good ground contact in the surroundings (guard ring). In the LFoundry process technology, a deep n-well insulates the pixel matrix from the wafer substrate. The ground contact of the inner ring utilises a ground pad reserved to the matrix.

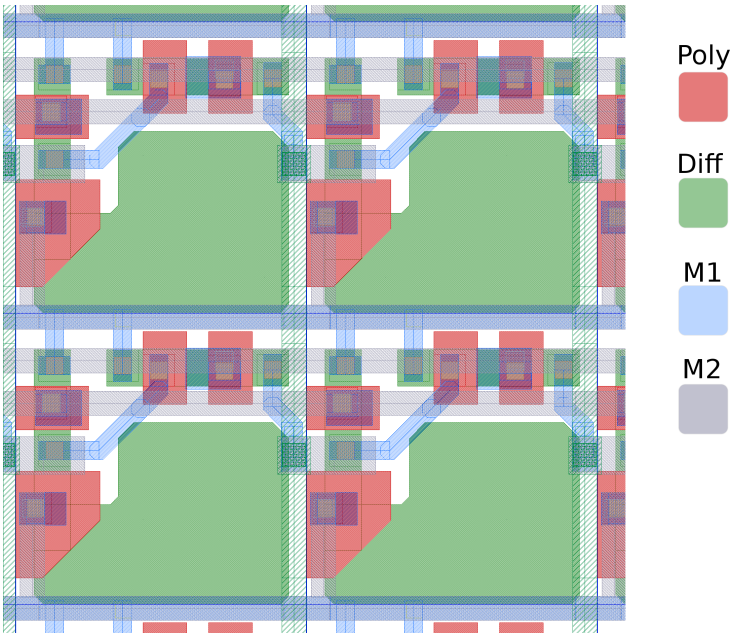


Figure 4.7: Block of fully symmetric 4T pixels

Figure 4.7 shows a block of symmetric pixels in the matrix. This is a typical array layout and represents a good starting point for further optimisation. This pixel was manufactured and presented in Section 3.1 as VB1. Here, two diffusions are connected to the supply voltage: the source follower drain and the reset switch drain. If this area would be shared, the available space created could be reserved to the photodiode thereby increasing the fill factor. The next sections will explore further optimisation of the pixel layout.

4.3.2 4T vertically flipped pixel layout

Instead of considering just one pixel, additional optimisations can be achieved if the neighbour pixels are considered. As an example, the supply voltage of each pixel is common and can be shared. Here, two vertical neighbours can share the power supply connection by flipping

one of the two pixels. The diffusion is centred at the edge of the pixels allowing for additional photodiode area.

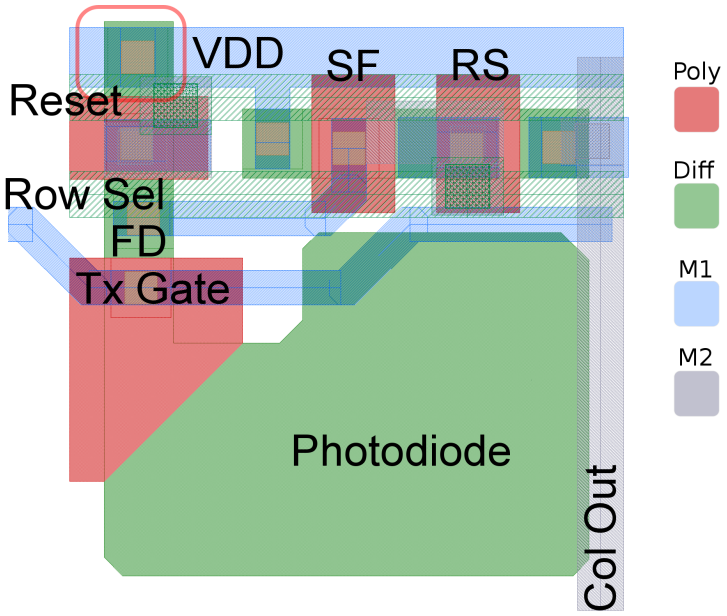


Figure 4.8: Supply shared 4T pixel layout 2.4 μm pitch in LFoundry 110 nm technology

In Figure 4.8 the shared supply contact is highlighted with a red box. In this example, the metal routing has been changed. The transfer gate signal is routed with Metal 1, the reset and row selector are routed in Metal 3 while the column output is driven out through Metal 2. This highlights some of the different options available to the layout designer. In this case, there is room for improvement as, even though a contact has been shared, the photodiode is still smaller than the fully symmetric version due to not choosing the most optimum routing. In fact, the transfer gate metal limits the area where the photodiode can be expanded without metal coverage. A better routing can be achieved using the empty space between two neighbour photodiode diffusions. This can be appreciated in Figure 4.9 where a better path for the transfer gate signal is highlighted.

Yet another layout can be obtained by observing that two neighbour pixels share the same column output. The output diffusion can be placed at the edge of the square cell to save additional space as it was undertaken for the supply voltage. Moreover, in both the supply shared design and the fully symmetric design there are two diffusions connected to the power supply which are the reset transistor and the source follower. From these considerations, a more compact layout can be achieved by sharing the power supply diffusion between the source follower transistor and the column output of two vertical neighbour pixels.

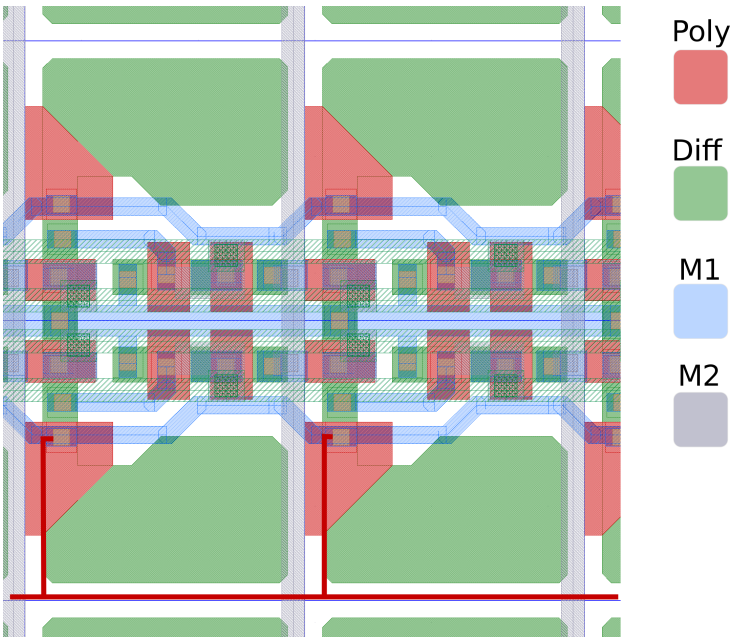


Figure 4.9: Block of supply shared 4T pixels showing a better routing path (in red) for the transfer gate signal.

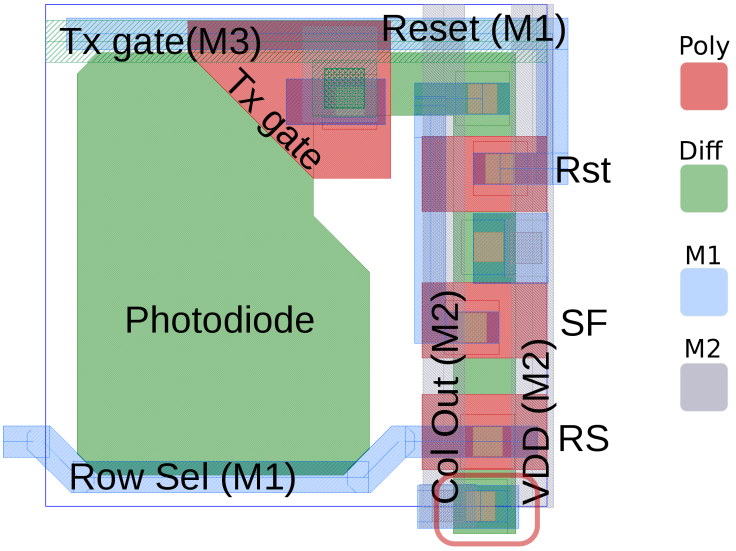


Figure 4.10: Column output shared 4T pixel layout 2.4 μm pitch in LFoundry 110 nm technology.

Figure 4.10 shows the design of a 4T shared-column-contact pixel. The shared output diffusion in highlighted in red. The orientation of some transistors changed from horizontal to vertical leading to a complete pixel rearrangement. The transfer gate signal is routed in Metal 3 and the reset signal is routed in Metal 1 underneath the first one. The row selector signal is routed in Metal 1 and has a serpentine shape in order to provide the necessary space to open the output contact. Power supply and the column output are routed vertically in Metal 2. It is worth noting that the diffusion region is now a continuous region from the photodiode to the output.

This design has the drawback of the floating diffusion being bigger than the previous one which reduces the conversion factor and of a reduced symmetry shape. The advantage, however, is to provide a larger photodiode and, hence, a higher fill factor of 30%.

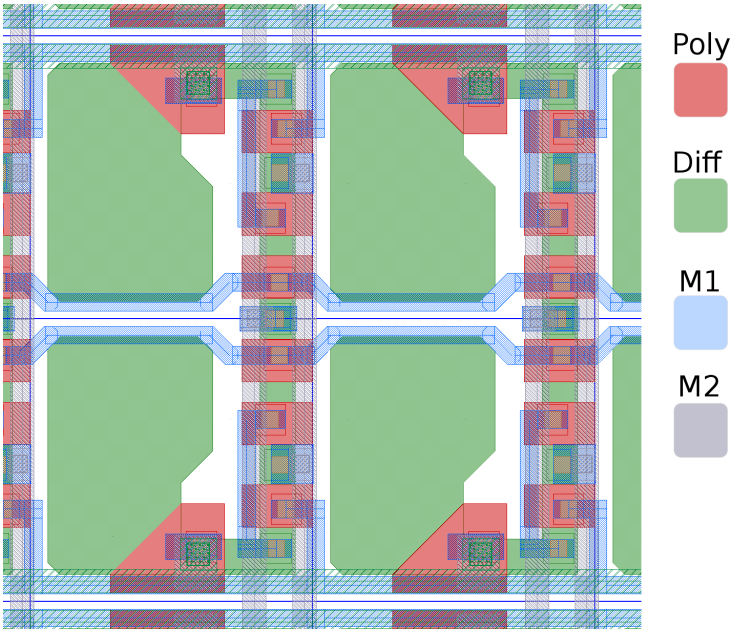


Figure 4.11: Block of column output shared 4T pixels.

The array block of output shared 4T pixels is shown in Figure 4.11 where another consideration is possible. A block of two vertical shared pixels can be flipped to share their row selector switches and their reset switches (in polysilicon). In fact, these are shared along a row. The subsequent design is shown in Figure 4.12. In this case, metals were swapped (Metal 2 horizontal and Metal 3 vertical). This is the pixel version VB3 with STI isolation that was already introduced in Chapter 3. In this pixel, there is extra space to add a ground path in the pixel array by paying the price of a fill factor reduction.

The ground path is highlighted with the red line and a potential region for the ground contact opening is shown with the red box in the middle of the photodiode corners. In this design, the power supply is now routed vertically in Metal 3 and shared between four neighbour pixels. There is, hence, additional space for another metal route without covering the photodiode. In addition, the reset and the row select contacts are shared and connected through polysilicon (in red). The photodiode is occupying all the available area. If the ground path is added, the layout in Figure 4.13 is obtained.

The ground contact is made with p-diffusion and needs to be separated from the photodiodes. In addition, the via placed in the centre forces the row selector routing in Metal 1 to

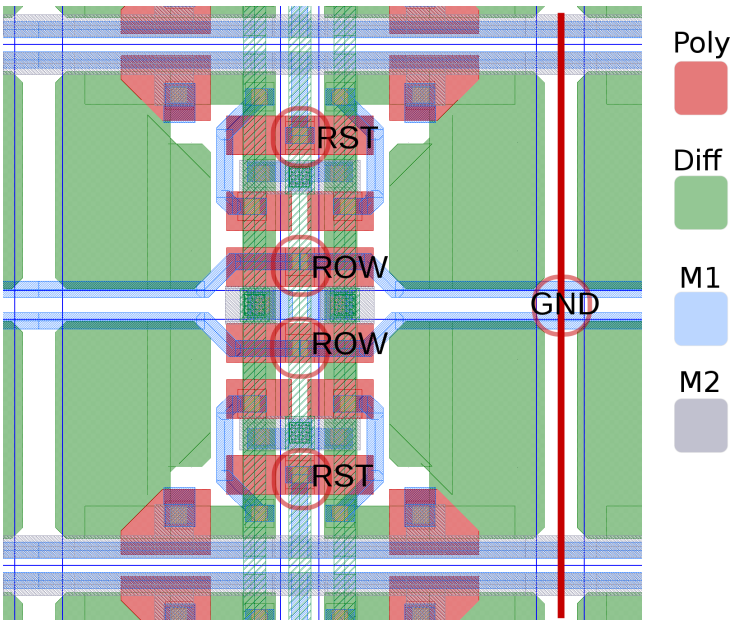


Figure 4.12: Block of horizontally flipped column output shared 4T pixels.

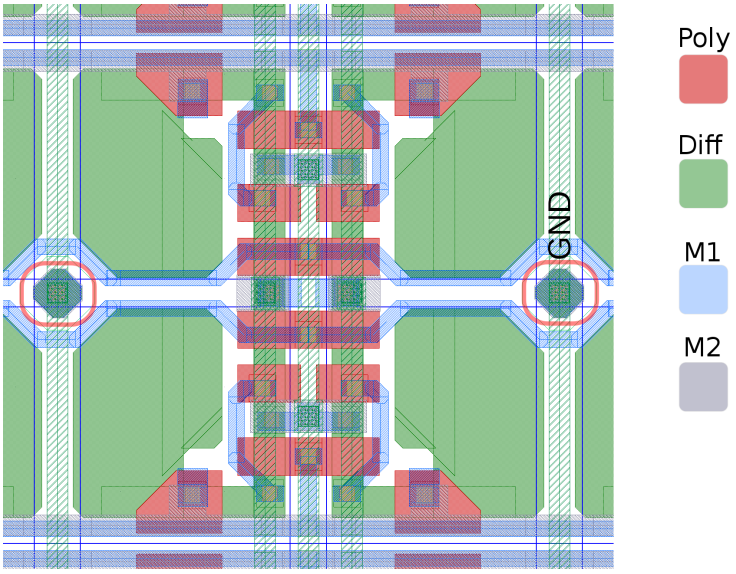


Figure 4.13: Block of horizontally flipped column output shared 4-T pixels with ground contact.

have a serpentine shape. The resulting layout shows the direct compromise between a ground uniformity distribution and the fill factor. The fill factor decreases from 30 % to 27 % in the grounded version. A possible choice is not to use a ground contact in the image sensor array to further increase the fill factor. This, however, may result in a ground mismatch in larger image sensors where the ground non-uniformity could affect the electro-optical response.

4.3.3 4T 4-shared pixel layout

The state of the art pixels uses the readout sharing technique to maximise the fill factor. These pixels could share a number of photodiodes which leads to a compact design. Examples from the industries of these layouts were presented in Chapter 2. In this section, the version VA3 layout, first introduced in Chapter 3, is presented. The sharing of the readout translates into an increase in fill factor up to 42 % with this pitch and process technology.

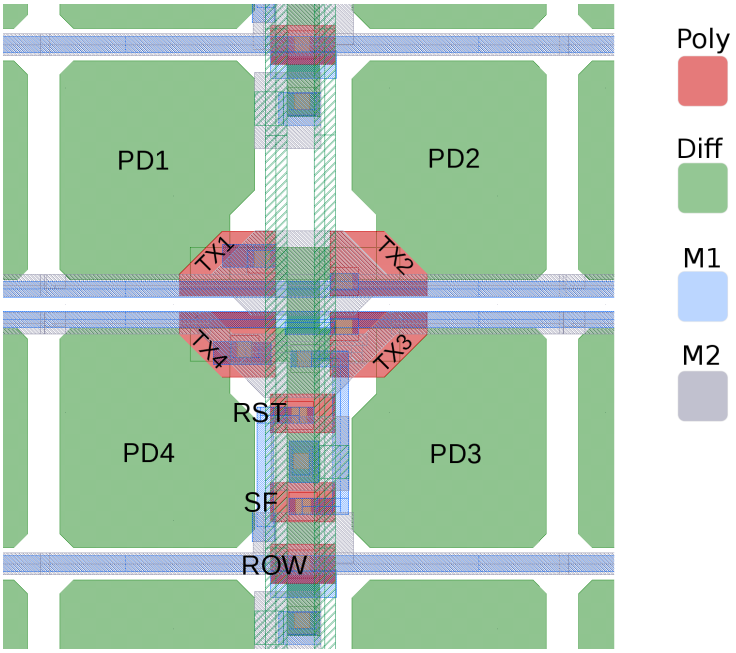


Figure 4.14: 4T 4-shared pixel layout (VA3 baseline).

The resulting layout of this design choice is shown in Figure 4.14. The block of four pixels is shown and it is controlled by the four transfer gates at the centre. The readout transistors, in red, are placed at the centre of the design similar to the Aptina or the Kodak pixel. In addition to version VA3, Versions VA1 and VA2 are 4-shared pixels isolated by a p-well layer by using the same technique presented in Chapter 3. The resulting layout is shown in Figure 4.15 where the photodiode occupies a larger area due to the more relaxed constraints already discussed previously.

The baselines of VA1 and VA2 are identical. The difference between these versions resides in the choice of their variations. The fill factor that is obtained by sharing the readout and using the p-well instead of the STI is 53% for these versions.

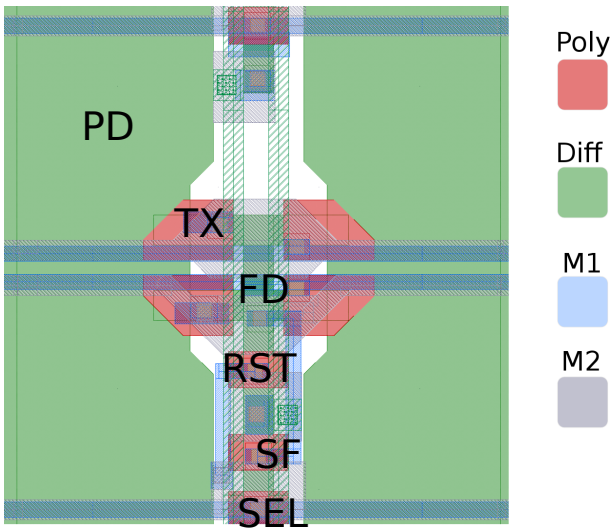


Figure 4.15: 4T 4-shared pixel layout (VA1 baseline).

4.4 4T pixel layout optimisation

The analysis conducted in Section 4.3 show that 4T-shared pixel has a higher fill factor, however, it also has a more complicated readout compared to a non-shared pixel. The aim of this section is to increase the photodiode area without having the drawbacks introduced by the sharing technique. Unfortunately, yet another constraint is that the pixel matrix has, by its definition, a rectangular readout. The assumption used in all the layouts designed is to have square pixels which fit into the defined readout pitch (2.4-by-2.4 μm in this work). The hypothesis of having squared pixel was implicit and used during the discussion of the pixel layouts. When designing the layout, sharing common diffusions saves space and leaves more area for the photodiode. Let us analyse more in detail this concept.

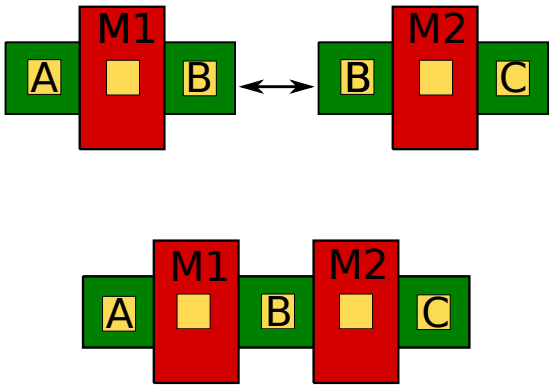


Figure 4.16: 2 Mosfets with and without sharing of the common node diffusion.

Figure 4.16 shows two MOSFETs, M1 and M2, which share the node B. The polysilicon is in red, the diffusion in green and the contacts are in yellow. If M1 and M2 are drawn indepen-

dently, the rule of the minimum distance between the two diffusions will force M1 and M2 to be separated. In addition, two contacts for the node B have to be manufactured and they should be surrounded by enough diffusion area for manufacturing tolerance. The node B can hence be shared by creating a common single diffusion and a single contact thereby saving area.

4.4.1 Optimisation path

In the pixel layout, the hypothesis of a squared pixel can be relaxed as the real constraint is not to have a real square pixel but a pitch-defined row control and column readout which represents an equivalent square pixel. If this is done, one possible pixel optimisation is straightforward: the transistors occupy less area when sharing a diffusion, hence, finding the path that leads to the maximum number of shared diffusions will reduce the area reserved to the transistors and, consequently, leave more area for the photodiode. This approach is already used in digital electronics wherein sharing diffusion paths enable more compact layouts. If a similar approach is applied to the 4T pixel, an optimisation path can be found.

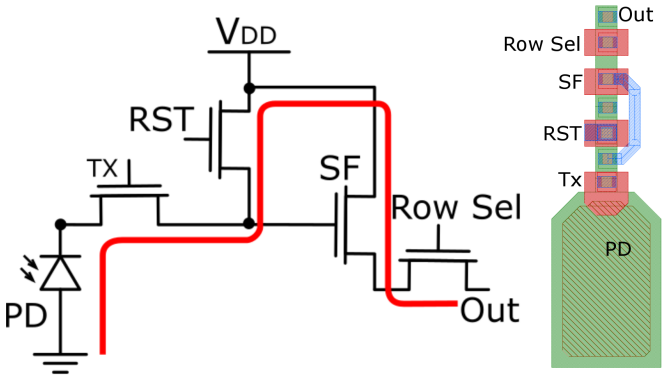


Figure 4.17: 4T pixel. The red line highlights the common diffusion path. On the right, the in-line layout.

Figure 4.17 shows a possible common diffusion path for the 4T pixel. Here, the photodiode is connected to the floating diffusion through the transfer gate. The reset transistor is connected from the floating diffusion to the supply voltage, which is in turn connected to the source follower drain. The path ends with the row selector, which is connected between the source follower and the column output diffusion. Furthermore, Figure 4.17 also shows the layout resulting from this approach. All the transistors share the same single diffusion leading to this compact layout. The layout ends with a transfer gate connecting the floating diffusion to the photodiode, which is then sized to fit the required pixel pitch. This layout arrangement leads to

a non-square pixel. If it is considered that the output is shared in a column and two neighbour pixels share their output diffusion, a longer common path can be found. Figure 4.18 highlights the path that includes twice the number of transistors compared to the first case leading to an even more compact layout.

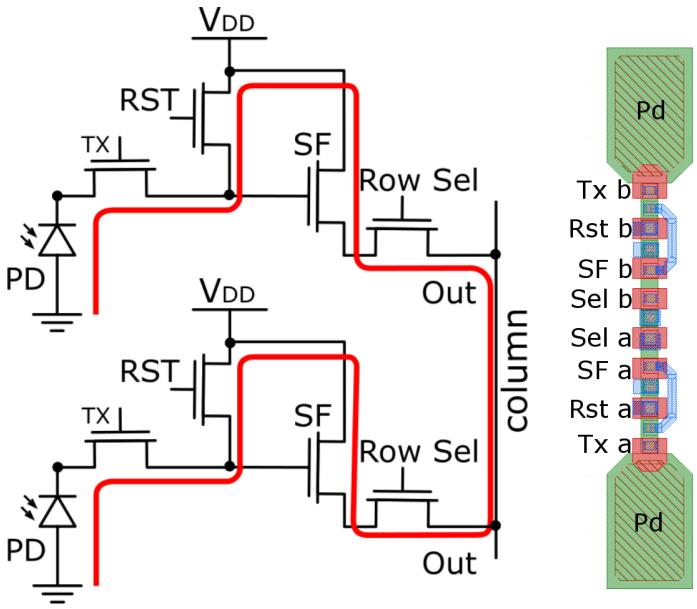


Figure 4.18: Adjacent 4T pixels. The red line highlights the common diffusion path in two neighbour column pixels. On the right, the in-line layout.

4.4.2 Staggered pixels

The resulting shape of the pixel differs from the square one used in the classical approach. The photodiodes of two pixels in the same column are positioned at a distance equal to the dimension of the transistor diffusion. One possible solution to fix this issue is to *stagger* the pixel rows by nesting and replicating the structure shifted by half a pixel pitch. This layout is shown in Figure 4.19.

The combination of staggered arranged pixels forms an hexagonal-like structure. However, this is addressable by a matrix as its X and Y pitch is squared and fixed. This novel layout technique maximises the photodiode area while minimising the transistor area thereby achieving a high fill factor of 42 %. This is the same fill factor obtained in the case of the 4T shared pixels without the drawback of sharing and with 2.25 more transistors. The routing layout can be adjusted to correctly control the signals driving each pixel.

Figure 4.20 shows a possible routing for the 4T staggered pixel layout cell. The rows a and

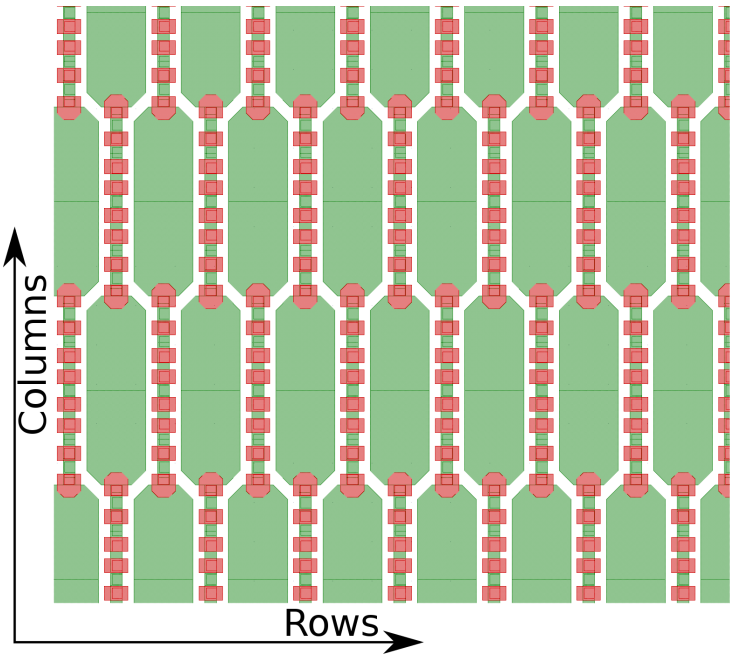


Figure 4.19: 4T nested half a pitch staggered pixel layout.

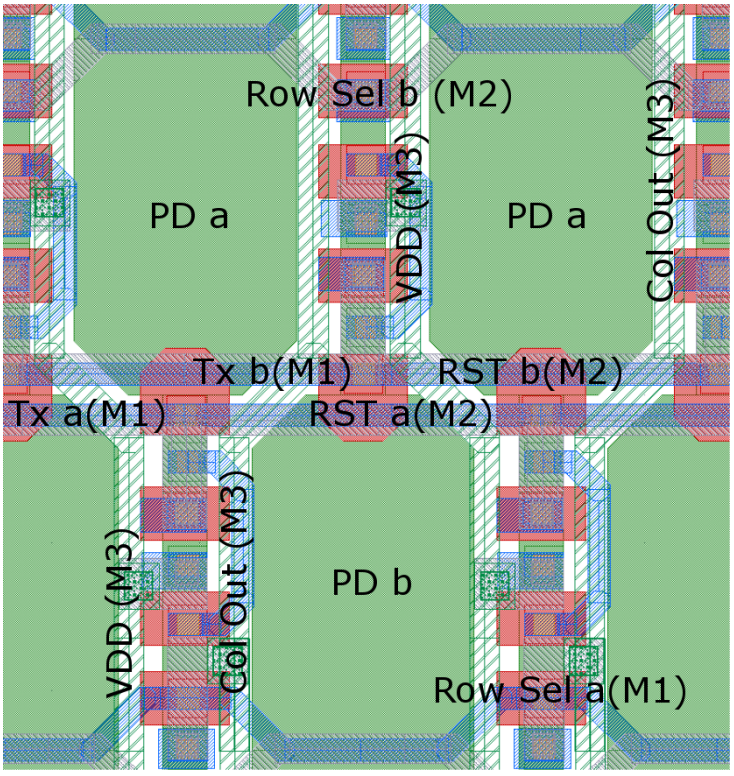


Figure 4.20: 4T staggered pixel layout cell routing.

b are controlled through the signals labelled with a and b respectively. The transfer gate metal is routed in Metal 1 underneath the reset signal routed in Metal 2. The row selectors for the two rows are routed in Metal 1 and Metal 2 in order to limit their coverage of the photodiode. For this design, the RC time constant difference is negligible given the speed of operation and the length of routing. However, for faster applications, the width of Metal 1 may be adjusted

to meet an equivalent RC constant compared to the Metal 2 routing. Finally, Metal 3 routes the supply voltage and the column output. Two neighbour pixels are connected to power supply and to the output alternating a contact on the left and one on the right. It is worth noting that this routing read out directly fits into a square matrix. This is a strength of this layout as it does not require any change to the external matrix periphery. This layout was implemented in the test chip version VB4.

4.4.3 Staggered p-well isolated pixels

A second way to implement the single diffusion path length concept is achieved by joining two blocks of staggered transistors. The photodiodes become adjacent and the p-well isolation technique can be applied to this layout. The other advantage of this configuration is a minimum size floating diffusion compared to the p-well isolated 4T where the floating diffusion was larger.

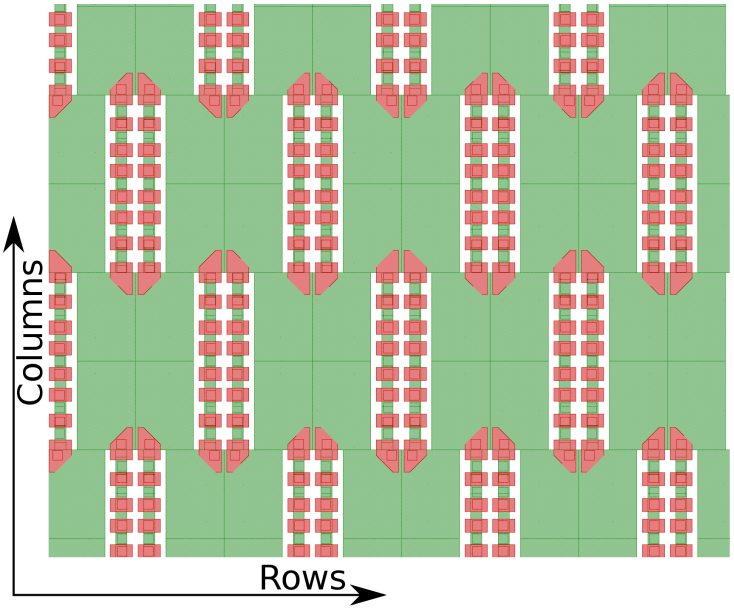


Figure 4.21: 4T p-well isolated staggered pixel layout.

Figure 4.21 shows the result of this different layout arrangement. This second approach produces an hexagonal-like structure as well. However, this design allows having blocks of four pixels. The photodiodes relative positioning allows the p-well isolation mechanism. This leads to an even higher fill factor of 43 % compared to the first staggered layout arrangement.

Figure 4.22 shows the routing for the p-well isolated staggered configuration which is compatible with the first staggered version. Even with a different photodiode arrangement, the

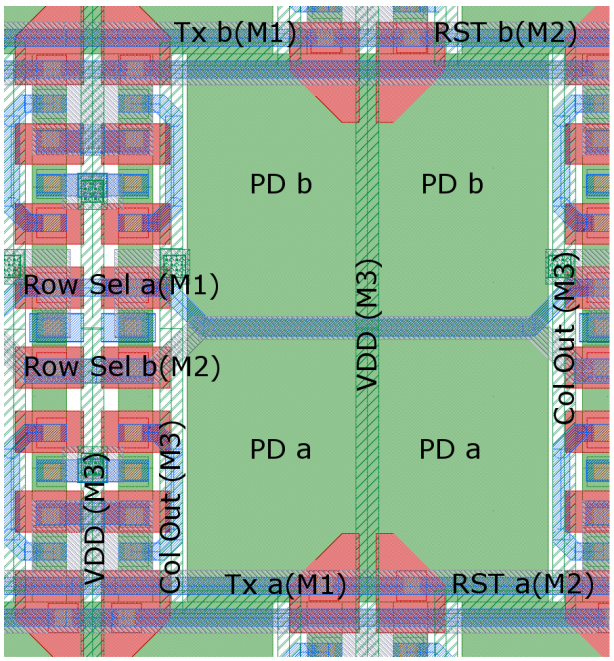


Figure 4.22: 4T staggered Bayer-like pixel layout cell routing.

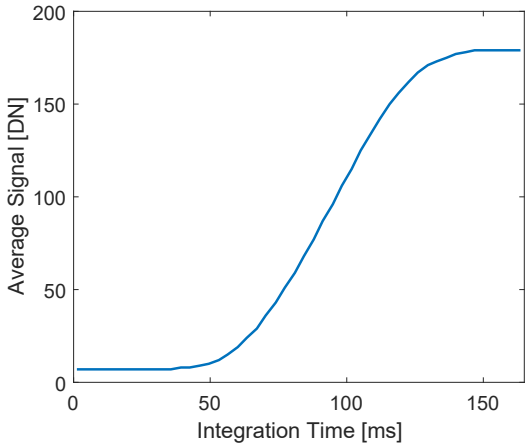
routing is similar to the STI staggered isolated pixel case and the metal levels used to route the signals are identical. The only difference here is that the power supply is routed in Metal 3 at the centre between the pixels instead of having a serpentine shape. Furthermore, the column output has a 90 degrees bending instead of a 45 one that increases the column metal length by 8%. This layout was also implemented in the test chip version VB4. The minimum path technique described in this section could be applied to other pixel architectures or even to shared architectures to minimise the number of contacts and therefore increase the fill factor.

4.5 Experimental results

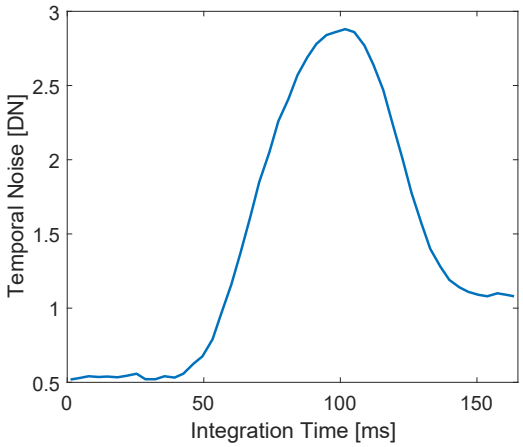
4.5.1 VA experimental results

In this Chapter, the optimised staggered pixel was proposed as a solution to increase the fill factor by minimising the transistor area. A shared diffusion between two transistors will occupy less area and, hence lead to an increased fill factor. The popular strategy employed to increase the fill factor is to share the readout between neighbour transistors. In order to compare the performance of the novel staggered pixel to a 4-shared approach, a shared pixel version was designed and manufactured. The light response of the shared pixel is reported hereafter.

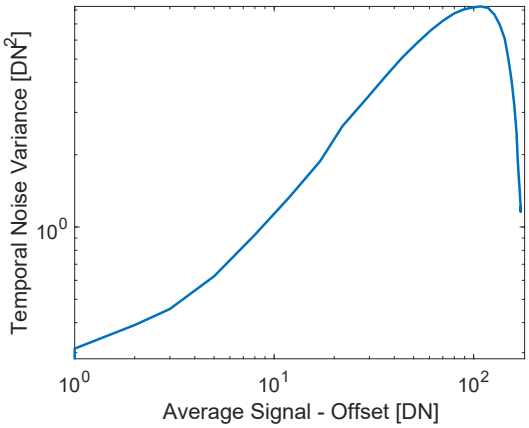
Figure 4.23 shows the measured signal and noise to a constant light level for an increasing



(a) Average signal in digital numbers vs integration time at constant illumination level for the p-well 4-shared isolated pixel (VA1 baseline).



(b) Temporal noise in digital numbers vs integration time at constant illumination level for the p-well 4-shared isolated pixel (VA1 baseline).



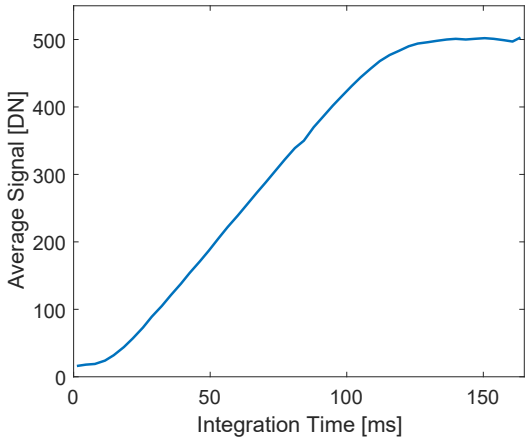
(c) Temporal noise variance vs average signal on a logarithmic scale (VA1 baseline).

Figure 4.23: Measured signal and noise of the VA1 baseline version.

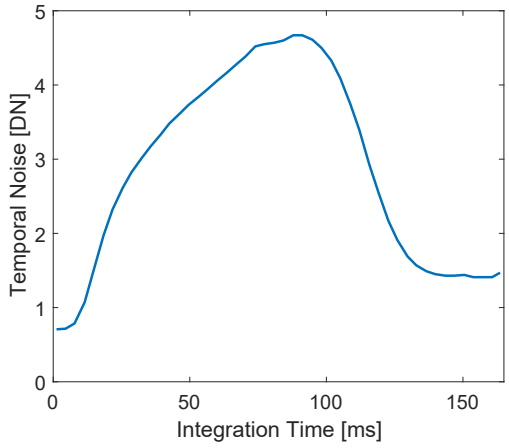
integration time. Unfortunately, Figure 4.23a shows that this pixel is not responding to light until an integration time of 50 ms. This means that this pixel is not sensitive to light for any of these exposures. However, the photodiode technology is the same as the other pixels presented in this thesis. The main reason for this failure can be associated with the transfer gate. In this pixel, the transfer gate is slightly different from the ones of the 4T pixels. A bad transfer of charge does not allow to have a precise characterisation of the pixel full well capacity, dynamic range and signal to noise ratio as these parameters could be strongly underestimated. For this reason, results on the 4-shared pixels are not included in this thesis. LFoundry has utilised the results to improve the transfer gate and the manufacturing process in their next learning cycle.

4.5.2 VB4 experimental results

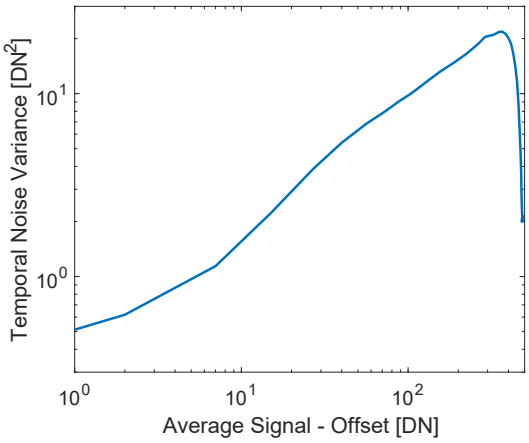
The optimised staggered pixel response will be compared to the standard 4T pixels. The rationale of a spatial optimisation led to this pixel design with an improved fill factor and area utilisation factor. Two staggered pixel versions were designed and manufactured The first is staggered and surrounded by STI isolation while the other has p-well isolated photodiodes. Their photoresponse curves are reported hereafter.



(a) Average signal in digital numbers vs integration time at constant illumination level for the p-well isolated pixel (VB4 v1 baseline).



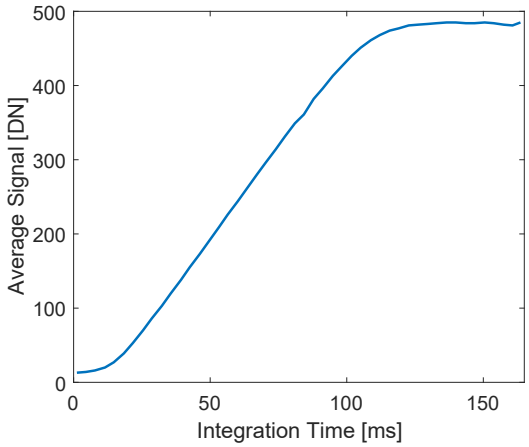
(b) Temporal noise in digital numbers vs integration time at constant illumination level for the p-well isolated pixel (VB4 v1 baseline).



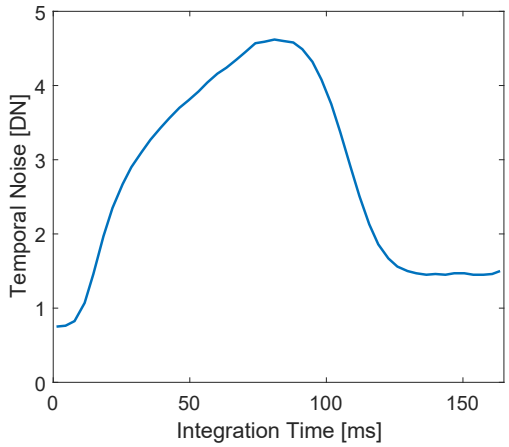
(c) Temporal noise variance vs average signal on a logarithmic scale (VB4 v1 baseline).

Figure 4.24: Measured signal and noise of the VB4 v1 baseline version.

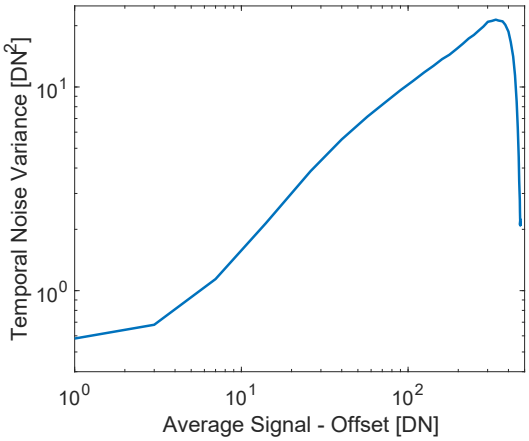
Figure 4.25 reports the photoresponse curves and the temporal noise of the two staggered version with STI and p-well isolation. Both these curves exhibit a different behaviour compared to the standard pixel photoresponses presented in Chapter 3. In fact, for low integration times, the response is not linear. This may be caused by the transfer gate which limits the charge



(a) Average signal in digital numbers vs integration time at constant illumination level for the p-well isolated pixel (VB4 v2 baseline).



(b) Temporal noise in digital numbers vs integration time at constant illumination level for the p-well isolated pixel (VB4 v2 baseline).



(c) Temporal noise variance vs average signal on a logarithmic scale (VB4 v2 baseline).

Figure 4.25: Measured signal and noise of the VB4 v2 baseline version.

transfer from the photodiode to the floating diffusion. When the residual charge fills the photodiode to the right exposure level, the excess charge is then correctly transferred and the response starts to be linear. This problem is not intrinsic to the layout but it is related to the novel process technology. The two versions correctly reach the saturation level which, however, may be underestimated. Fortunately, both these versions suffer less from the transfer gate problems compared to the shared version VA which only started to respond to a 50 ms integration time. From the undertaken measurements, the linear full well can be estimated and the results of the 4T pixel staggered variations are reported in Table 4.1.

For these versions, despite the underestimation, the full well is higher compared to the 4T pixels presented in Chapter 3. It has to be noted that these pixels suffer from a strong non-uniformity due to the immature process of manufacturing.

Table 4.1: VB4 measured parameters (p-well and STI).

Version	VB4 v1 (STI)	VB4 v2 (p-well)
Noise[e]	13	14
CF[e/LSB]	17	18
LFW[e]	6622	5973
Sat[e]	8002	7800
DSNU[%]	2.24	2.18
PRNU[%]	4.39	5.22
DR[dB]	54	53
SNR[dB]	39	38

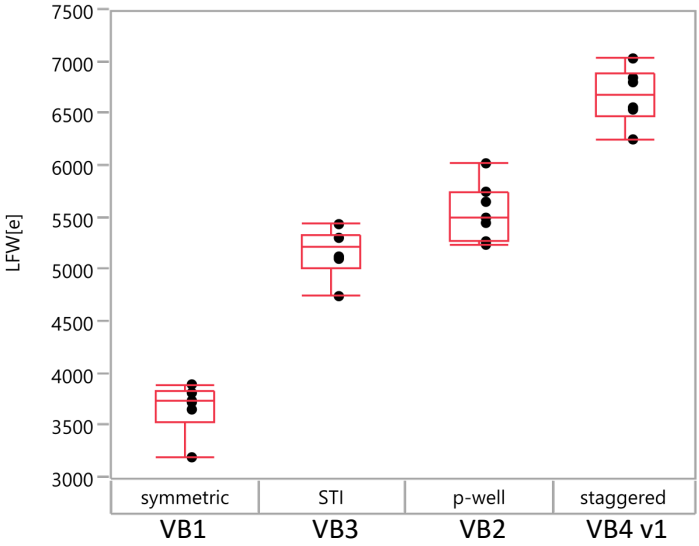


Figure 4.26: Full well statistical variation of the 4T pixel versions.

Figure 4.26 shows the linear full well capacity variability for the presented versions. Each black dot represents the average full well capacity of a pixel variation window of 186-by-84 pixels. The fully symmetric pixel (VB1) has the lower full well capacity while VB2 and VB3 pixels have a slight advantage due to the sharing of the supply and the output voltage contacts. The p-well isolated pixel version has a larger n-implant as discussed in Chapter 3 which increases the full well capacity. The 4T staggered pixel with STI isolation is reported in Figure 4.26 showing that the layout optimisation by the sharing of diffusions leads to an increase in full well capacity compared to the standard pixel layouts.

The pixel capability of collecting more light given all the other parameters is already an advantage. The impact of the staggered layout on the dark current will be evaluated as well. Unfortunately, at short integration times, the charge transfer is poor. This means that the transfer gate is not able to transfer all the charge from the photodiode to the floating diffusion and the

dark current can be underestimated. In addition, the pixels suffer from a strong non-uniformity From a first analysis, some pixels have a nonlinear behaviour for short integration times while others have a linear response. As an example, the dark signal response is shown for two pixels: a non-linear behaving pixel and a linear behaving one.

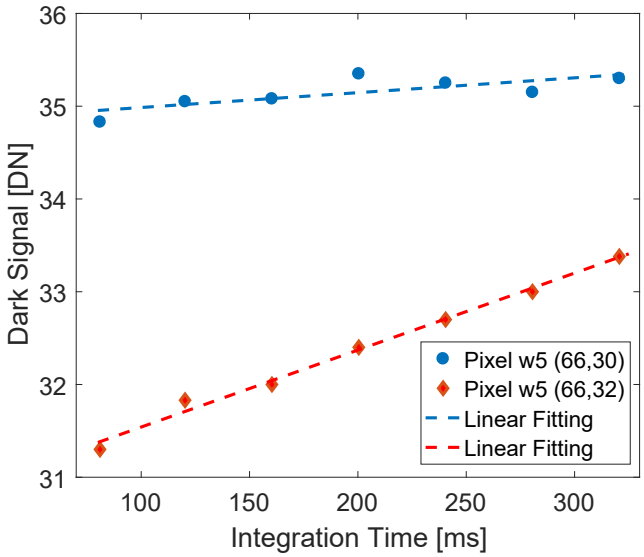
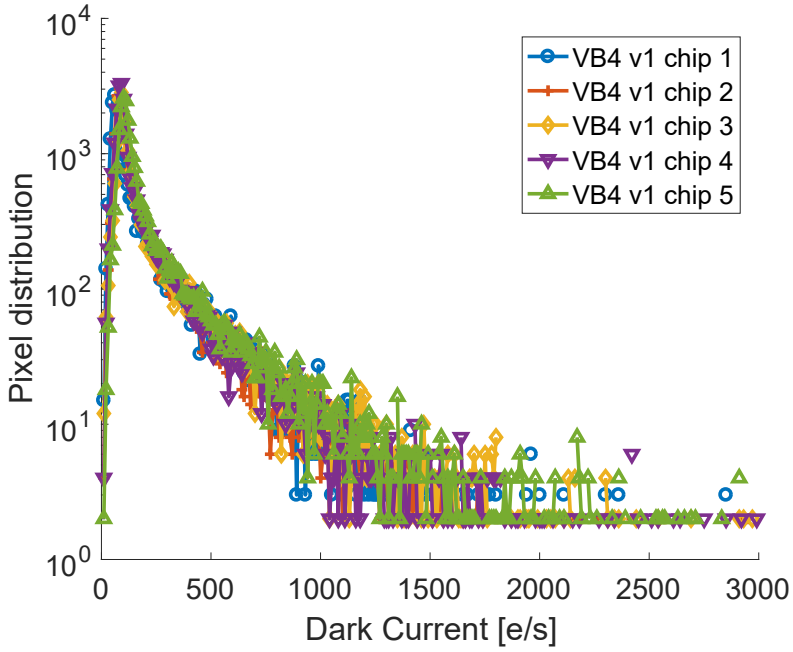


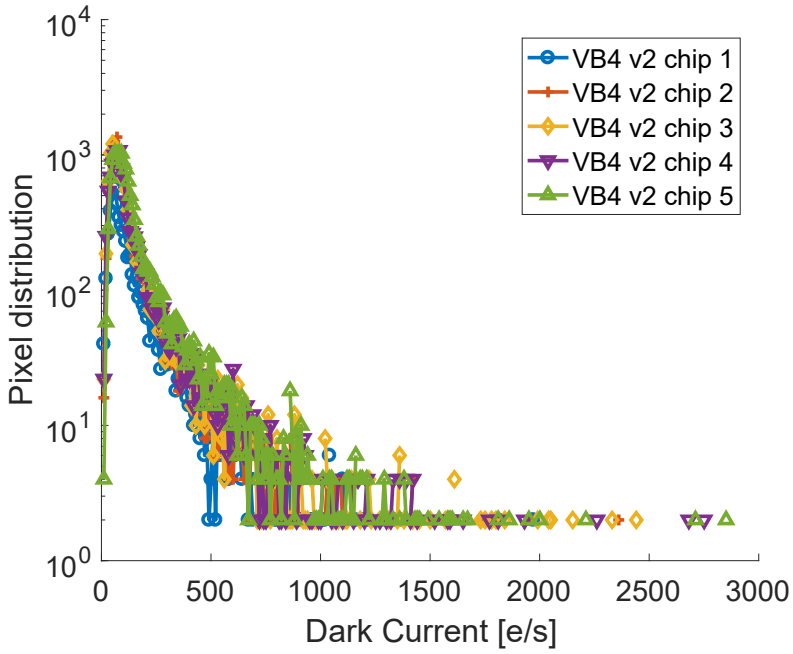
Figure 4.27: Dark signal of two pixels with different linearity.

Figure 4.27 show the response of two pixels chosen close to each other in the same window (window 5 row 66 columns 30 and 32). These two pixels have a different behaviour. The pixel in red exhibit a linear response and its R-squared linear regression coefficient is 0.992 while the pixel in blue shows a strong non-linear response with an R-squared linear regression coefficient of 0.597. As the dark current is measured as the slope of the linear fit, the blue pixel will result in an underestimated dark current value due to its non-linear behaviour. The red pixel instead will be correctly evaluated. Unfortunately, for this pixel version, many pixels suffer from this strong non-linear behaviour. For this reason, the dark current of this version will be estimated by taking into account only the pixels which exhibit a linear behaviour (R-squared > 0.9).

Figure 4.28 shows the dark current histogram of the staggered pixels at 60 Celsius. These were collected from five different chips located close on the wafer. The two pixel versions presented for each chip belong to different sub-windows of the same chip. Although this is an estimation of the dark current which accounts only for linear pixels, the comparison between these two versions confirms the hypothesis made in Chapter 3 where the STI causes the main peaks to slightly shift towards higher values of dark current and, more importantly, the number



(a) STI staggered pixel dark current distributions.



(b) P-well staggered pixel dark current distributions.

Figure 4.28: Dark current distribution of STI and p-well isolated staggered pixels (with R-squared > 0.9) on a logarithmic scale. Measured at 60 Celsius.

of hot pixels to increase. Table 4.2 reports the mean values of the dark current and the percent proportion of hot pixels (dark current higher than 500 e/s).

The quantitative analysis confirms that the STI version has a dark current higher by 50 e/s and a higher percentage of hot pixels. This is so despite their photodiode areas which are reported in the next table.

Table 4.2: VB4 measured dark current and hot pixels (p-well and STI).

Version	**VB4 v1 (STI)**		**VB4 v2 (p-well)**	
Parameters	DC [e/s]	Hot [%]	DC [e/s]	Hot [%]
Chip 1	180	7.58	150	4.44
Chip 2	180	6.41	125	2.63
Chip 3	208	8.46	140	3.72
Chip 4	185	6.42	145	4.11
Chip 5	222	8.79	159	4.40
Avg	**195**	**7.53**	**144**	**3.80**

Table 4.3: Dark current % comparison of VB4 v1 and VB4 v2 with Photodiode Area and Fill Factor.

Version	DC [e/s]	PD Area [μm^2]	Perimeter [μm]	FF [%]
VB4 v1 base	195	2.41	6.15	42
VB4 v2 base	144	2.57	6.53	45
Delta [%]	-26	7	6	7

Table 4.3 reports the dark current related to the photodiode area and perimeter. The dark current is decreased by 26 % despite a larger photodiode area of 7%. This means that the net reduction of the dark current can be estimated as the 33% which is different compared to the result obtained in Chapter 3. The correlation of the dark current to the photodiode area is not sufficient to generate a good prediction model. However, the STI was proven to increase the dark current and the number of hot pixels. A better model could be built by taking into account the part of the perimeter in contact with the STI which leads to:

$$J_{dark} = J_1 A + J_2 l_{STI} \tag{4.1}$$

This is a simple model which does not take into account the dark current generated at the interface with the p-well region and the dark current generated at the transfer gate. In this equation, J_{dark} is the dark current density, A is the area of the photodiode, l_{STI} is the part of the photodiode perimeters in contact with the STI, J_1 is the dark current contribution per unity of Area and J_2 is the dark current contribution per unity of length. By design, the Area and the STI length are known. In addition, the dark current was measured for a number of pixel variations. By solving the system, J_1 and J_2 are obtained and are equal to 44.7 $\frac{e}{s \cdot \mu m^2}$ and 15.7

$\frac{e}{s \cdot \mu m}$ respectively. If this simplified model is used to predict the dark current of these versions, the following result can be obtained.

Table 4.4: Dark Current model verification

Version	VB2	VB3	VB4 v1	VB4 v2
PD Area	2.08	1.69	2.41	2.57
STI length	1.78	4.6	4.2	1.78
DC meas [e/s]	105	133	195	144
DC model [e/s]	123	149	176	145

Table 4.4 shows the STI interaction length for the baselines of the versions presented in this work. It presents the measured current and the result of the modelled current with the evaluated coefficients. This simplified model can help to quickly predict the dark current from a layout in this technology.

4.6 Summary

This Chapter discussed the layout constraints of a CMOS image sensor. The analysis of sharing techniques used in digital circuits leads to a novel pixel layout design optimisation strategy. This strategy consists of reducing the space occupied by the transistors by finding a common diffusion sharing path. As a result, the fill factor is increased for pixels designed in the same process technology and with the same pixel pitch. The common technique to increase the fill factor consists in sharing the readout transistors. This has the drawback of increasing the readout complexity and to reduce the operating speed. Experimental results show that the proposed pixels increase the linear full well capacity. In addition, the dark current reduction strategy, where the STI is removed between the photodiodes, was applied to this optimised pixel. This lead to a high full well low dark current pixel. Furthermore, a simple model was proposed to estimate the dark current from the photodiode area and the length of the STI. It is worth noting, that the staggered pixel has a novel spatial arrangement that may not be displayed on a standard device without artefacts as it is acquired. The next Chapter presents a strategy for displaying images acquired with this technique.

Chapter 5

Image display and reconstruction

In Chapter 4, the electro-optical performances of the staggered pixels were presented. Captured images need to be displayed on a screen. The presence of a staggered array with a non-uniform spatial sampling of the image will introduce artefacts as displays expect to receive a matrix of data wherein each pixel samples its exact position in the matrix. However, for the staggered array, alternate rows are shifted by half a pixel pitch. This introduces artefacts when displaying the acquired image without any processing. This Chapter presents strategies and hardware-efficient algorithms to display the images acquired with the staggered pixel arrangement and it is organised as follows: Section 5.1 explains how the standard and staggered images are sampled and displayed, Section 5.2 introduces algorithms to display staggered images onto a standard display and the shows the application of these algorithms to a colour image. Section 5.3 summarises the chapter.

5.1 Image sampling

The typical CMOS image sensor pixel array is arranged in a regular matrix. Despite pixel layout flipping or sharing techniques, the image sensor samples the incoming light with a regular equally spaced pattern that can be represented as in Figure 5.1, which illustrates a typical pixel matrix arrangement.

Images acquired with this spatial sampling could directly be displayed on a screen. However, image sensors suffer from temporal noise and non-uniform responses like FPN or PRNU. To reduce the temporal signal fluctuation, a number of frames are collected and averaged. Im-

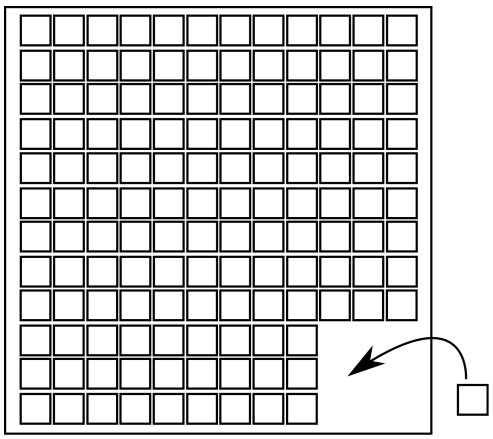


Figure 5.1: Typical pixel matrix arrangement in a CMOS image sensor.

ages can be corrected thanks to a technique known as flat field correction. This consists of removing the dark signal and accounting for the pixel-to-pixel slope mismatch and can be expressed as:

$$I_{corr} = \frac{I_{acq} - D}{M - D} k \tag{5.1}$$

where I_{acq} is the acquired image, D is the dark image, M is the mid-level image and k is a correction factor that compensates the difference in signal level and is expressed as $k = \overline{M - D}$. In a fixed scene, these images are the result of averaged frames over time. The dark signal is subtracted from the acquired image and from a mid-level illumination image. The results are then divided to correct for linear slope variations. This changes the gain of the resulting image. To compensate for this gain loss, the image is multiplied again by the correction factor k.

Figure 5.2 shows the dark image collected with these conditions. This image appears brighter because an offset was added for display purposes. The dark image immediately shows that this sensor suffers from a high column-to-column mismatch and, hence, column FPN. This is due to the mismatch of the biasing column transistors that are present in the column drivers to bias the pixel source follower. When the mid-level image of a uniform background of this sensor is collected, it also shows a high FPN as shown in Figure 5.3.

In the staggered pixel version, images are sampled in a slightly different arrangement. If the layout of the staggered pixel is recalled, the resulting matrix can be represented as in Figure 5.4. With this arrangement, a block of four rows is repeated. Two rows are shifted by half a pixel pitch and two occupy a standard pixel position of a matrix. Fortunately, it is still possible to

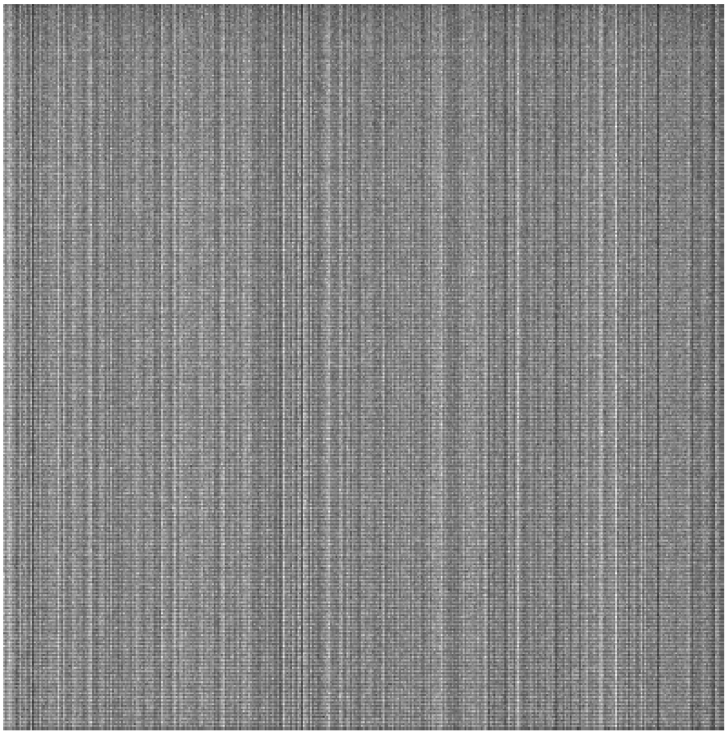
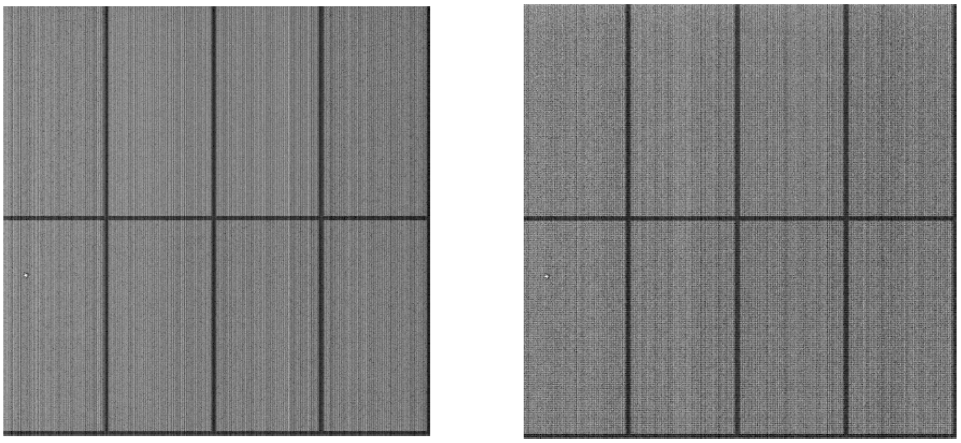


Figure 5.2: Averaged dark image of a standard 4T pixel.



(a) Standard 4T pixel mid-level image without dark offset correction.

(b) Standard 4T pixel mid-level image with dark offset correction.

Figure 5.3: Averaged mid-level image of uniform background with and without dark offset correction.

use the flat field correction technique to compensate for gain and offset mismatch. However, standard displays are designed to accept a matrix of values as input. For this reason, the display of this image produces artefacts as introduced in Figure 5.5 where the metallic continuous edge present on top of the pixels appears staggered. The appearance of this pattern is strictly correlated to the spatial position of the pixels in the array, which do not have a corresponding position in the display.

Figure 5.6 shows the model of the sampling of an ideal edge on a staggered pixel sensor.

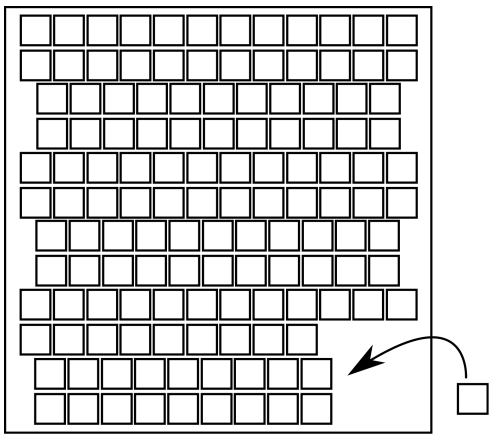


Figure 5.4: Staggered pixel matrix arrangement in the manufactured CMOS image sensor.

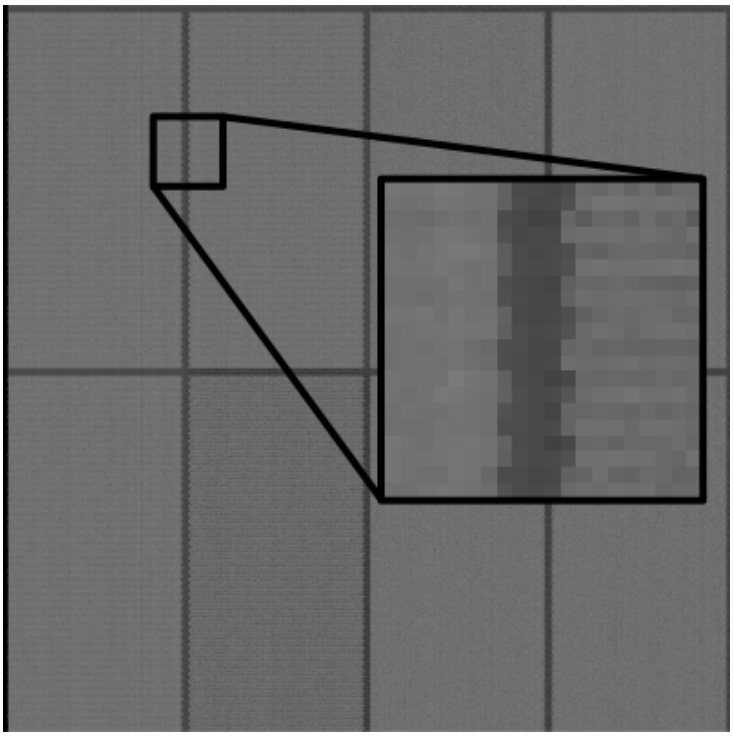


Figure 5.5: Mid-level acquired image of the staggered pixel matrix.

The edge (red) represents a region where the pixels to the right are dark and the pixels to the left are white. The edge acquired with the staggered arrangement of pixels is then displayed on a standard matrix, which causes some of the rows to shift by half a pixel pitch position. The result is a distorted image with artefacts as the acquired edge is shifted as well. In a standard matrix, the presence of the edge translates to a grey level, which represents the edge position within the pixel column. The pixel staggered arrangement advantages have been discussed for CCD image sensors by Harada *et al.* [104]. The staggered arrangement changes the Nyquist limits of the spatial acquisition by increasing the resolution in the horizontal and vertical directions while loosing resolution in the diagonal direction. The resolution increase was also demonstrated in

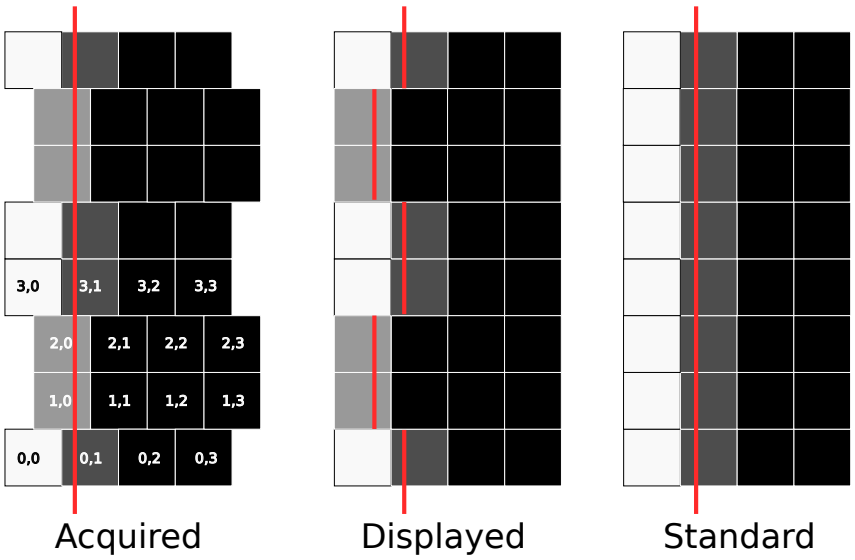


Figure 5.6: Edge capture and display on a STI staggered pixel versus a standard pixel.

line scan sensors where a row of pixels is staggered compared to the other [105]. In addition, chessboard-like patterns were presented claiming to improve image resolution by interpolating the missing pixels in the chessboard pattern [106, 107].

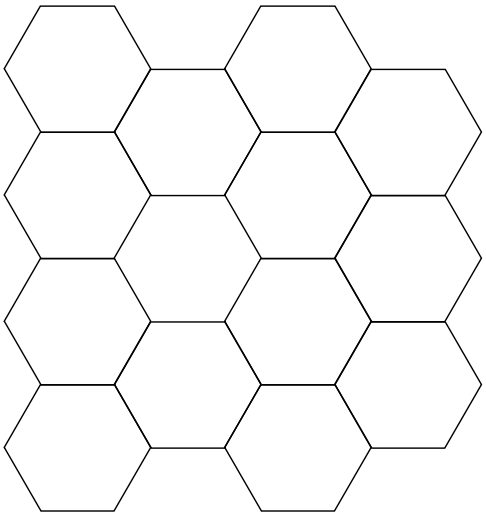


Figure 5.7: Hexagonal pixel arrangement.

Hexagonal pixel structures like the one shown in Fig 5.7 have been discussed in the past. In 1997, Hupperts *et al.* [108] presented an image sensor with hexagonal pixel sampling. The hexagonal pixel shape attracts interest because it can sample a two dimensional space well and can increase the resolution by sub-pixel interpolation in both the Cartesian axes. Choi *et al.* patented an hexagonal based honeycomb pixel structure for Samsung [109]. Hexagonal pixel structures have been also studied to improve the color image acquisition [110, 111]. The staggered arrangement presented in this thesis, however, aims to maximise the fill factor and to

increase the photodiode area rather than improving the resolution or the color response. The issue with this arrangement is finding a strategy to represent the acquired images on a standard display. In the next section, the effect of staggering is analysed on collected images and simple reconstruction algorithms are proposed.

5.2 Target images and reconstruction algorithms

In order to study the reconstruction strategy for the staggered pixel, experimental images were collected from a packaged sensor. A focused image was projected on the sensor thanks to an Optoliner [112]. The Optoliner is a tool, which integrates a light source, an integration sphere, and a lens system to change the focal plane. By using this tool, black and white slides are projected on the sensor in focus. The integration time is defined and fixed to 163 ms. All the images are collected with the same integration time and at room temperature. In this example, the Optoliner slides were projected on both the sensors. An average of the frames was performed to reduce temporal noise variations.

Figure 5.8 presents the images acquired for both the standard version (VB2) and the staggered version (VB4). The staggered pixels were arranged by sliding their positions along the horizontal dimension. For this reason, a vertical edge slide was chosen to evaluate this effect. In addition, a target slide with concentric shapes is used to evaluate the effect of the spatial sampling when the direction changes. From the acquired images it is possible to see slight performance differences between windows of pixel variations. However, this does not have an impact on the reconstruction strategy. With the high level of resolution, it is hard to evaluate the effect of a spatial sampling difference. For this reason, the analysis will be conducted on the image details.

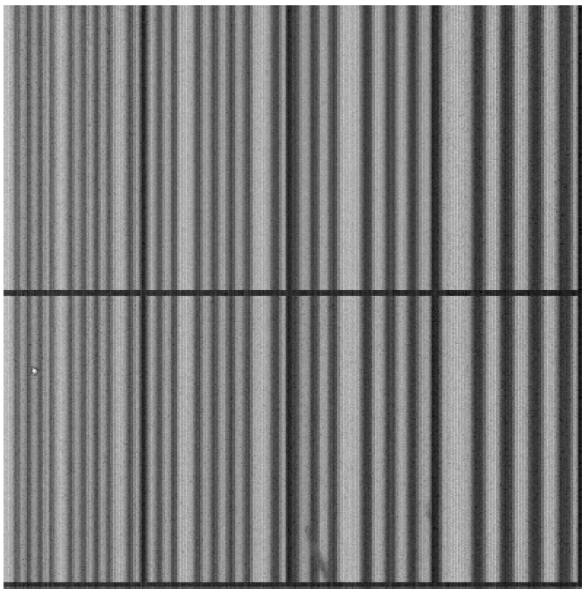
First, a schematic analysis of the pixel arrangement will be undertaken. For the purposes of spatial sampling, the pixels can be represented by a part that is sensitive to light (the photodiode) and a part that is not sensitive to light (the transistors). The information collected in the photodiode is extended to the whole pixel when the image is displayed.

Figure 5.9 shows a schematic of the pixel sampling for the standard and the staggered matrices. The transistor location is represented with a grey zone while the photodiode sampling is represented with a white zone. The STI pixel version is a true staggered matrix while the p-well

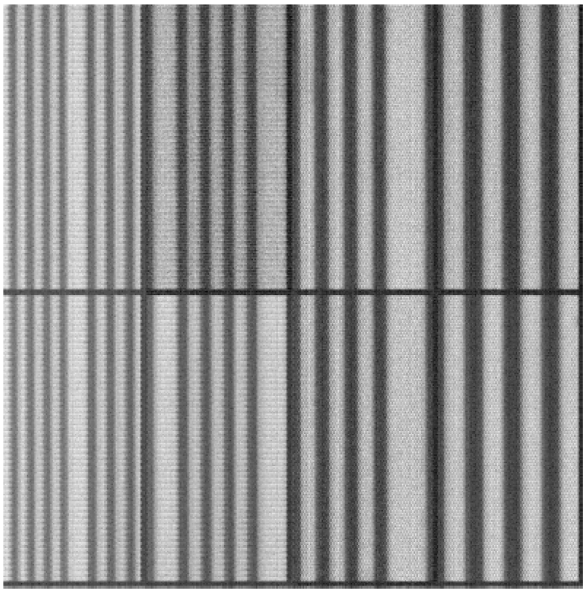
staggered matrix can still be represented on a grid even if it has an irregular sampling pattern.

Figure 5.10 shows the effect of this sampling on vertical edges for the three pixel versions. Here, the edge of the standard pixel appears sharp as the pixels are arranged in a matrix fashion. The staggering appears different for the two versions of the staggered pixels. The STI version appears as a two-by-two staggering while the p-well version appears staggered in blocks of four. The vertical edge, however, maximizes the effect of staggering in the horizontal direction. For this reason, details of the target slides are presented.

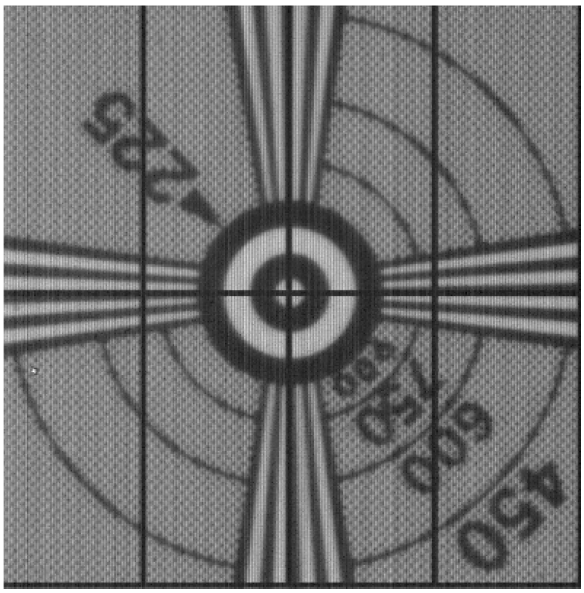
Figure 5.11 shows the details of the concentric target image the standard and the staggered



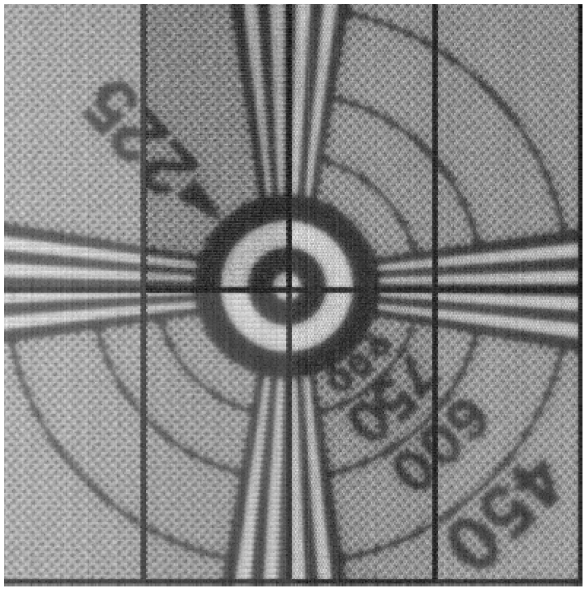
(a) Standard pixel edges image.



(b) Staggered pixel edges image.

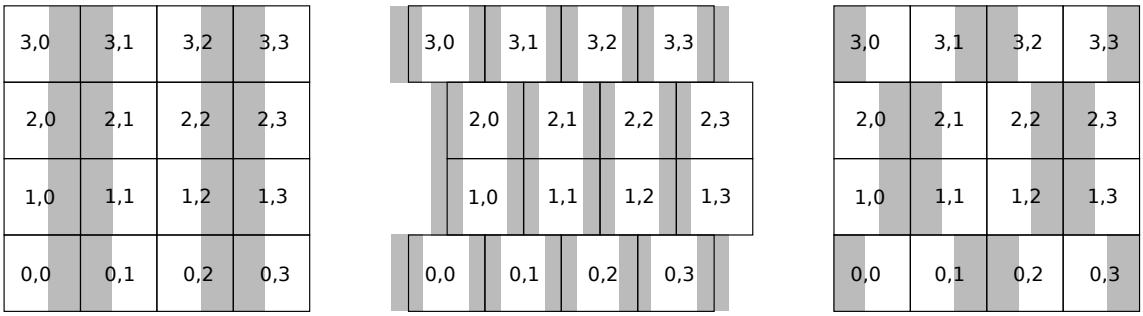


(c) Standard pixel target image.



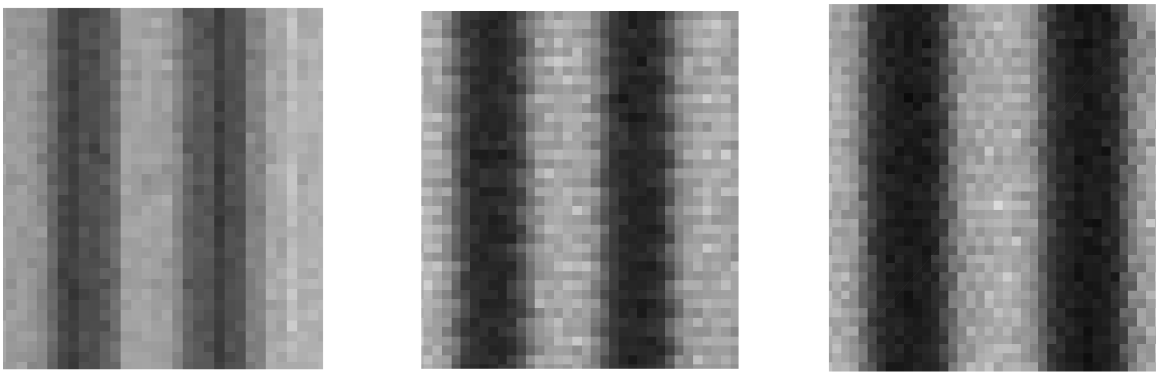
(d) Staggered pixel target image.

Figure 5.8: Standard vs staggered collected images of edges and target slides.



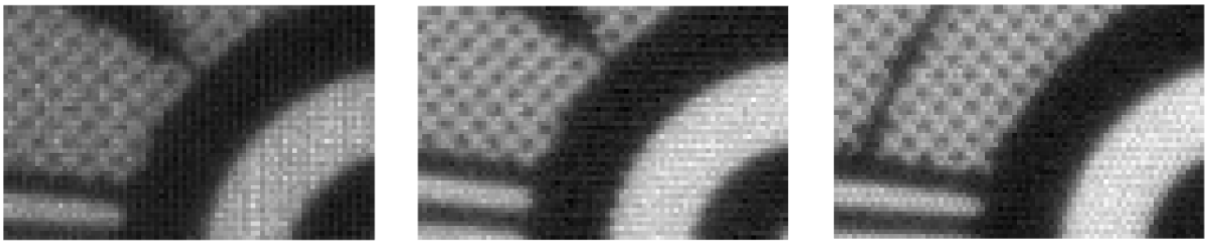
(a) Standard pixel. (b) STI staggered pixel. (c) Pwell staggered pixel.

Figure 5.9: Schematic of the pixel arrangement. The transistors area is in grey while the photosensitive area is in white.



(a) Standard pixel. (b) STI staggered pixel. (c) P-well staggered pixel.

Figure 5.10: Image comparison of the edge details for the different pixel versions.



(a) Standard pixel. (b) STI staggered pixel. (c) Pwell staggered pixel.

Figure 5.11: Image comparison of the target details for the different pixel versions.

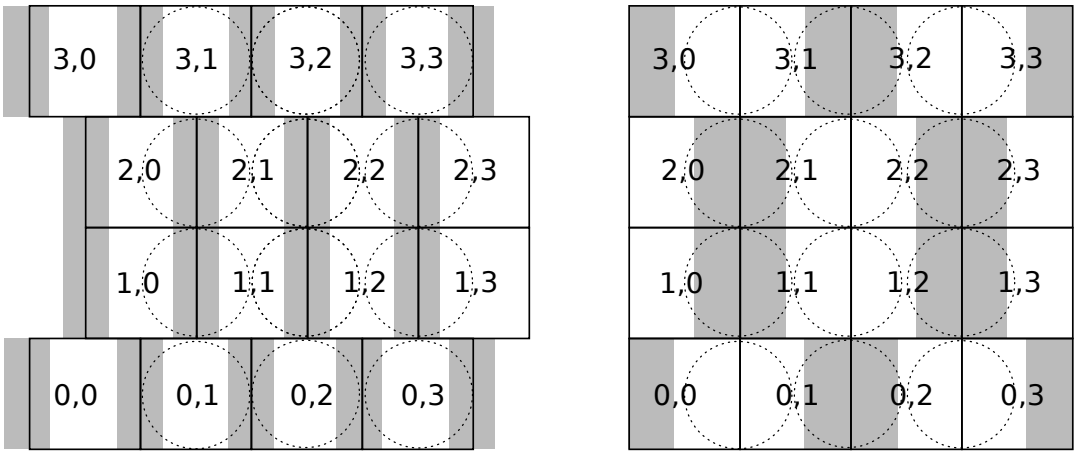
pixels. For a vertical edge, the difference between the images appeares immediately, but the horizontal lines in the bottom left corner do not appear as distorted because the staggering occurs in the horizontal direction. The circles appear noisy in the STI staggered version at the centre of Figure 5.11b where the circle tangent is vertical. In the p-well staggered version this effect does not appear as relevant as the STI one. In fact, the p-well version can be displayed on a standard matrix. For display purposes, the pixels of the staggered versions need to be rearranged in a matrix. Note that in these images it might appear to the human eye that the vertical FPN was removed although this is not the case. The staggering scrambles the vertical

lines to which the human eye is very sensitive.

5.2.1 Averaging algorithm

Algorithm

An initial, simple hardware-efficient algorithm can be implemented by computing the average of two neighbouring pixels. The average only requires a sum and a division by 2 in hardware that can be implemented with an adder and a register.



(a) Staggered pixel STI.

(b) Staggered pixel p-well.

Figure 5.12: Staggered Pixel STI representation. The squares are the real pixels, the grey areas are the location of the transistors, and the dotted circles are the calculated pixels by averaging neighbour pixels and to fit a matrix position.

Figure 5.12 shows the pixel representation of the two staggered versions where the dotted circles represent the locations that the computed pixels will occupy after the average algorithm execution. If the algorithm is not applied, the image appears shifted. In the STI version, pixels (0,0), (0,1), (0,2) and (0,3) will occupy their respective coordinates in an ordered matrix while pixels (1,0), (1,1), (1,2) and (1,3) will occupy the position of the pixels half a pitch shifted to the left. However, if the average of the pixels (1,0) and (1,1) is computed, it is possible to redefine a new (1,1) pixel represented by a dotted circle, which occupies the right position in the matrix array. This dotted circle pixel can be computed as the average of its two adjacent pixels:

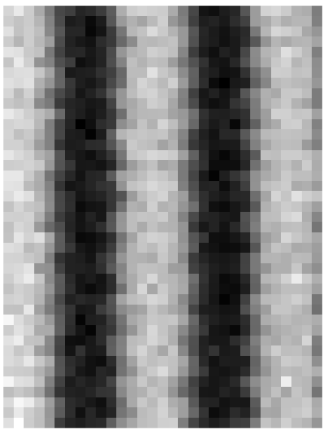
$$pn_{11} = \frac{p_{10} + p_{11}}{2} \tag{5.2}$$

where pn_{11} is the new pixel in the dotted circle p_{10} and p_{11} are the pixels in the old (1,0) and

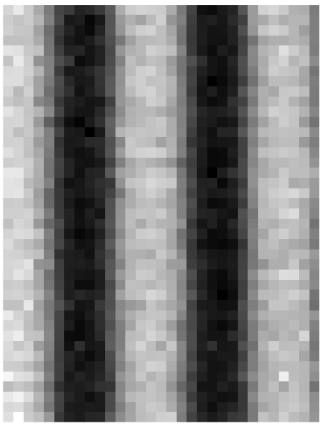
(1,1) positions. The same algorithm can be applied to the position of the other dotted circles. In the STI version, this average is not computed for the pixels in positions like the (0,1) pixels as they already occupy a position that fits the matrix. For those pixels, the new pixel will have the same value of the old pixel $pn_{10} = p_{10}$. In the p-well version, the average is computed on every row as each pixel is shifted compared to the new centred grid made of dotted circles.

Application

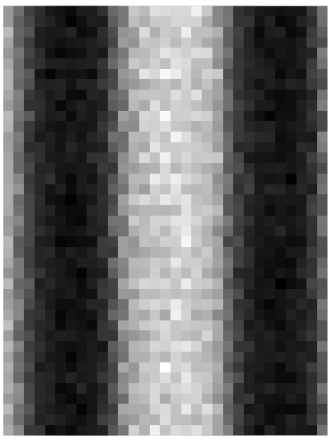
The algorithm is applied on both the edges and the target image. First, the reconstructed image of the edges is shown by focusing on a detail in Figure 5.13. The edges appear to be reconstructed correctly. In both the versions the edges are less noisy. However, the application of an averaging algorithm smoothed the image details.



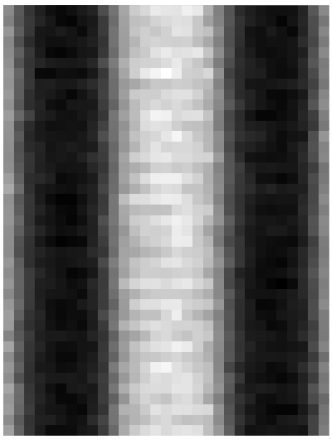
(a) Staggered pixel STI before average algorithm.



(b) Staggered pixel STI after average algorithm.

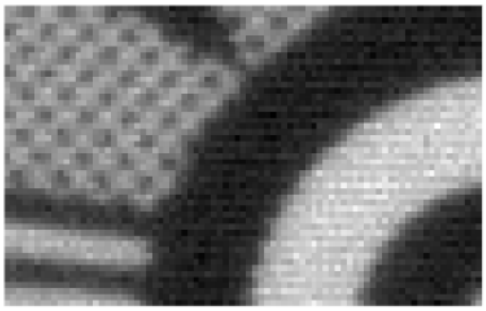


(c) Staggered pixel p-well before average algorithm.

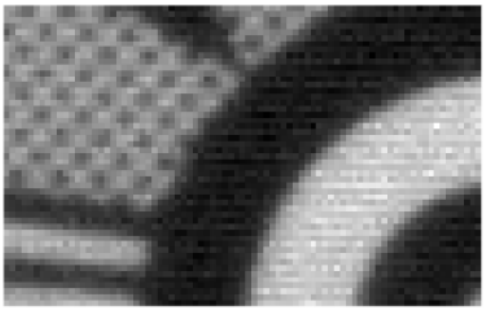


(d) Staggered pixel p-well after average algorithm.

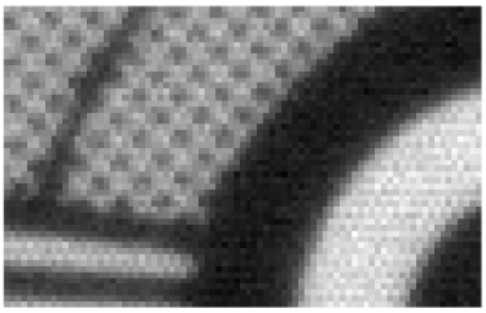
Figure 5.13: Comparison of edge detail after the neighbour averaging algorithm for the two staggered pixel variations.



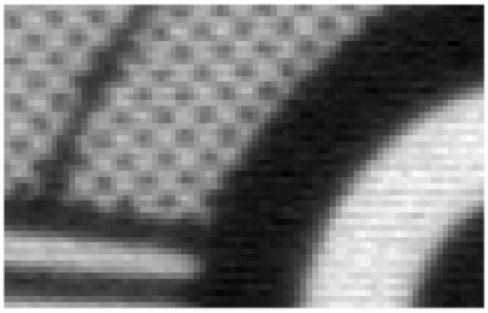
(a) Staggered pixel STI before average algorithm.



(b) Staggered pixel STI after average algorithm.



(c) Staggered pixel p-well before average algorithm.



(d) Staggered pixel p-well after average algorithm.

Figure 5.14: Comparison of target detail after the neighbour averaging algorithm for the two staggered pixel variations.

Figure 5.14 shows the target detail images before and after the average algorithm image processing. Unfortunately, the average operation is a low-pass filter applied to the image and has the effect of smoothing the image variations. This is of particular relevance in the pwell algorithm where all the rows are averaged. The resulting image has lost some of the bright pixels, which is particularly visible in the lower left corner between the horizontal dark lines. In the STI image, the algorithm is applied every two rows. For this reason, some of the bright pixels continue to be visible in the image. For the circular shapes, the algorithm is more effective when the edge is vertical and less when the edge becomes horizontal like in the top right corner of the images. For these reasons, it is not worth the effort of applying an algorithm on the staggered pwell version while it is worth considering other algorithms for the staggered STI version. Another averaging strategy is presented in the next subsection.

5.2.2 Double resolution grid

Algorithm

In the previous section, an averaging algorithm was applied to compute pixels in an equivalent matrix position. In this subsection, another averaging algorithm is presented. If the staggered STI version is considered in the region where the transistors are present, a missing pixel can be computed by interpolating values of the neighbour pixels. In this way, the resolution is doubled along the abscissa. Bloss *et al.* presented a similar method to compute missing pixels in a chessboard pattern [106]. They computed the gradient of neighbour pixels and interpolated by using the lowest gradient effectively doubling the resolution. For simplicity, in the presented algorithm the gradient is not evaluated.

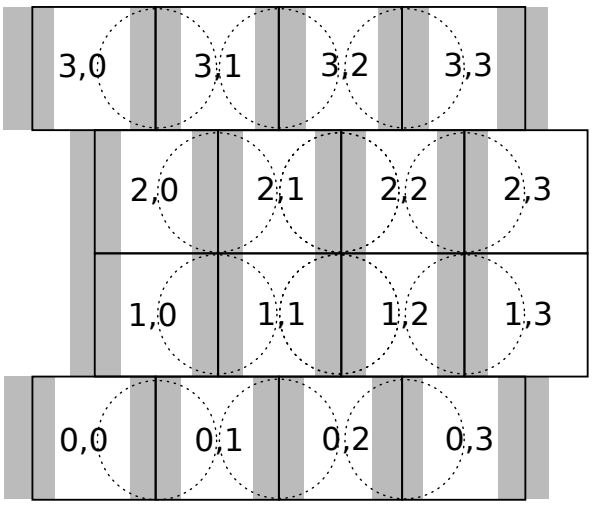


Figure 5.15: Staggered pixel STI resolution enhancement by interpolation.

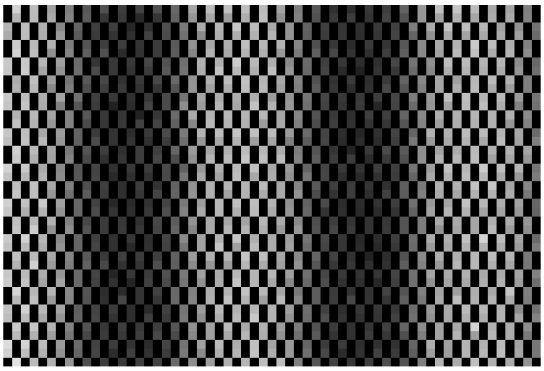
Figure 5.15 shows the locations where the interpolated pixels are calculated by the average of their neighbours. The real sampling space is represented by the square box while the final pixel location is represented by a dotted circle. This technique doubles the number of pixels along the x-direction. As an example, the interpolated pixel in the location between pixels (0,0), (0,1) and (1,0) can be computed as the average of these three pixels:

$$pn_{01} = \frac{p_{00} + p_{01} + p_{10}}{3} \tag{5.3}$$

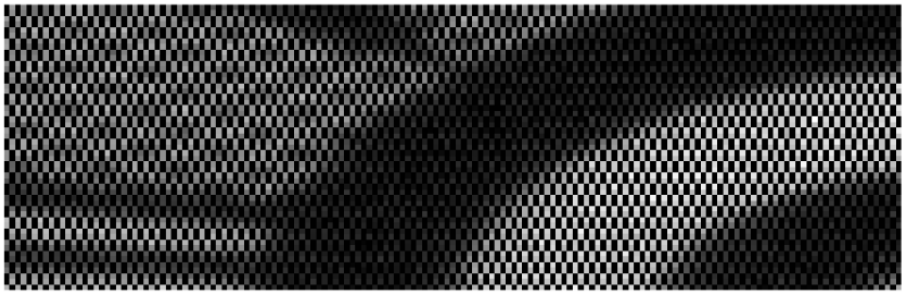
where pn_{01} is the new interpolated pixel and p_{00}, p_{01} and p_{10} are the neighbour pixels in their respective locations.

Application

The image is represented in a different space with a double resolution on the x-axis. The result of this process is shown in Figure 5.16 where images appear stretched as the resolution is doubled. The black squares represent the transistor location. This region is not sensitive to light and, in this example, it was assumed that this region occupies the same area of the photodiode, which is the sensitive region. This is a valid assumption as the fill factor is in the range of 40-50%. The interpolation is performed and the missing black codes are replaced with the calculated values.



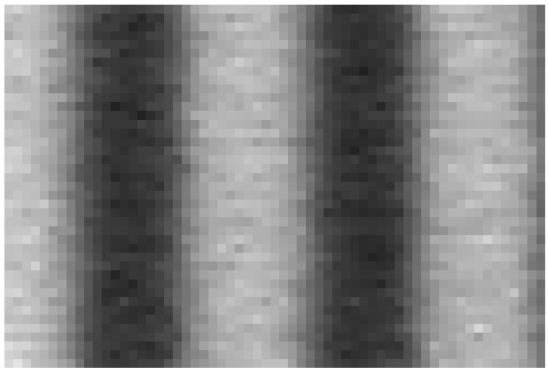
(a) Edges image.



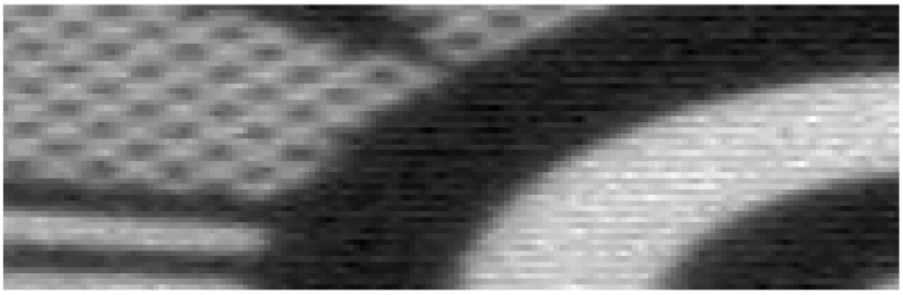
(b) Target image.

Figure 5.16: Staggered STI pixel acquired images with highlighted spatial sampling.

Figure 5.17 shows the edge and target images where the black locations of Figure 5.16 have been replaced with the interpolated pixel value. In this case, even if the interpolation is computed through an average, the real pixel information is not lost. The interpolated values are added to the image without removing the original pixel values. This is hence a lossless operation and it is possible to recover the exact copy of the original image. The advantage is that the staggering is corrected as each pixel is now occupying the right position in the double resolution matrix. This is visible in the edge image where edges appear in the correct location and in the target image where the circular paths appear less noisy. Nevertheless, these images occupy twice the memory to store the information. In addition, the image is stretched and it is



(a) Edges image.

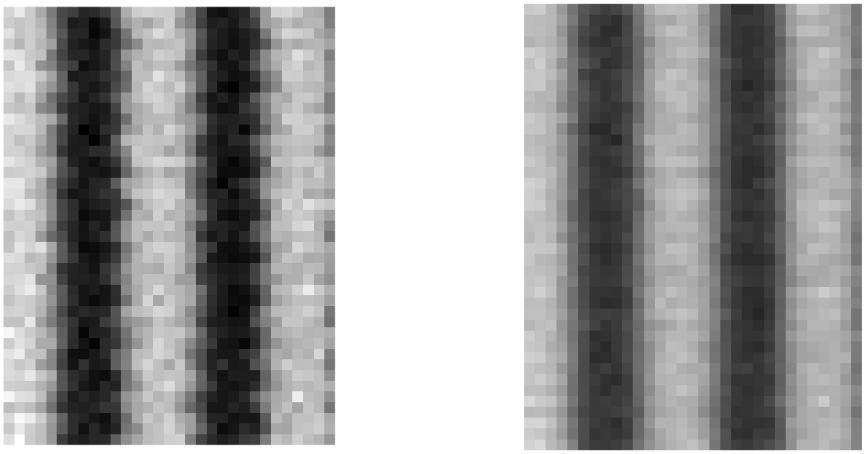


(b) Target image.

Figure 5.17: Staggered STI pixel interpolated images after sampling.

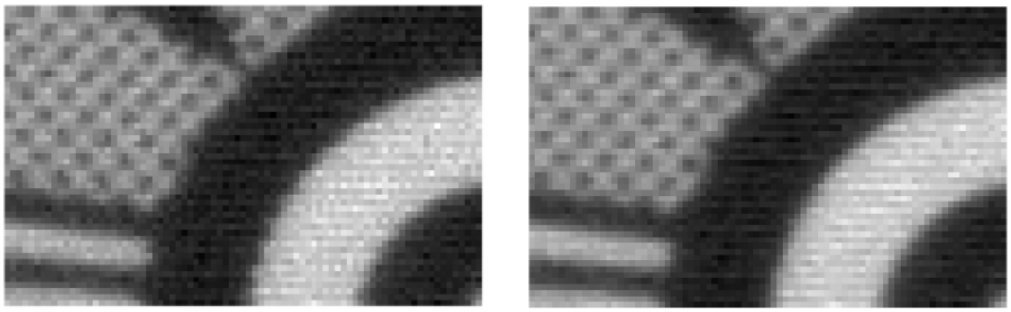
necessary to reshape the image in order to compare it with the real acquired images. A possible simple way to do it is by using the Matlab bicubic regression function. This is a 2-Dimensional extension of a 1-Dimensional cubic interpolation function. It is applied it to the stretched image to obtain the equivalent single-resolution final reconstructed image.

The result of the reshaping bicubic function is shown in Figure 5.18. The image was acquired and represented on a spatial grid with double the resolution along the x-axis, the missing pixels were interpolated and the image was reshaped to be represented with the same axis of the original image. While the interpolation operation of the missing pixels was lossless, the reshaping function introduces a loss. Again, this acts as a low pass filter and has the effect of smoothing the image. The edges, however, now appear as a straight line and the round circles in the target image are sharper. By staggering, the resolution can be increased in one of the two dimensions of the spatial sampling and the image can be reconstructed by interpolation. This method requires an interpolation operation and twice the memory to store all the values. Then, a fitting could be applied to the interpolated image in order to represent it with the same resolution of the acquired image. In this case, the computation intensity increases significantly.



(a) Edges before.

(b) Edges after.



(c) Target before.

(d) Target after.

Figure 5.18: Comparison of target and edges detail after the double resolution grid interpolation and reshaping with bicubic function of the staggered STI pixel.

5.2.3 Double matrix dimension

Algorithm

The acquired pixels of the staggered image sensor occupy positions shifted by half a pixel pitch in the matrix. Another method to reconstruct the original image is to represent the acquired image as a matrix with double the dimension along both the x and y-axes. In this way, the position of each pixel is an integer and can be displayed in the same location as it was acquired in the pixel array.

Figure 5.19 shows the STI staggered pixel matrix and a possible representation on a grid with double the resolution along both axes. As an example, the pixel (0,0) is copied four times in the pixels (0,0), (0,1), (1,0) and (1,1) of the new matrix. The pixel (1,1) of the original matrix is shifted of half a pitch and it is copied in the pixels (2,1), (2,2), (3,1) and (3,2), which are shifted by an entire pitch in the new double resolution matrix. This operation can be written as:

$$pn_{00} = pn_{10} = pn_{01} = pn_{11} = p_{00} \tag{5.4}$$

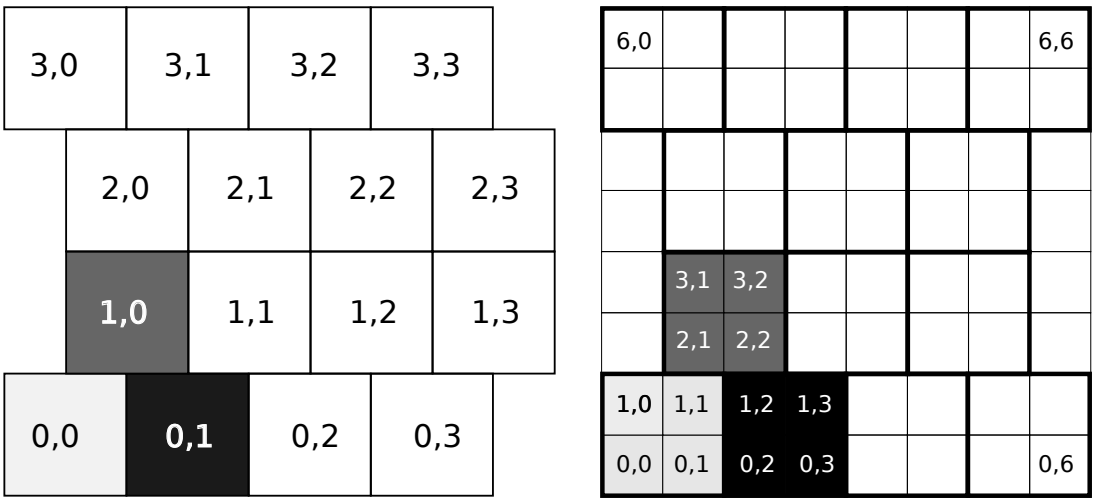


Figure 5.19: Staggered Pixel STI representation of a matrix of double dimension.

where pn_{00}, pn_{01}, pn_{10} and pn_{11} are the new pixels in the double matrix dimension and p_{00} is the pixel in the acquired staggered matrix. In the first row instead the index is moved by one position to the right so that:

$$pn_{21} = pn_{22} = pn_{31} = pn_{32} = p_{10} \tag{5.5}$$

where pn_{21}, pn_{22}, pn_{31} and pn_{32} are the new pixels in the double matrix dimension and p_{10} is the pixel in the acquired staggered matrix. For the first and forth row these expression can be generalised as:

$$pn_{2n,2m} = pn_{2n,2m+1} = pn_{2n+1,2m} = pn_{2n+1,2m+1} = p_{n,m} \tag{5.6}$$

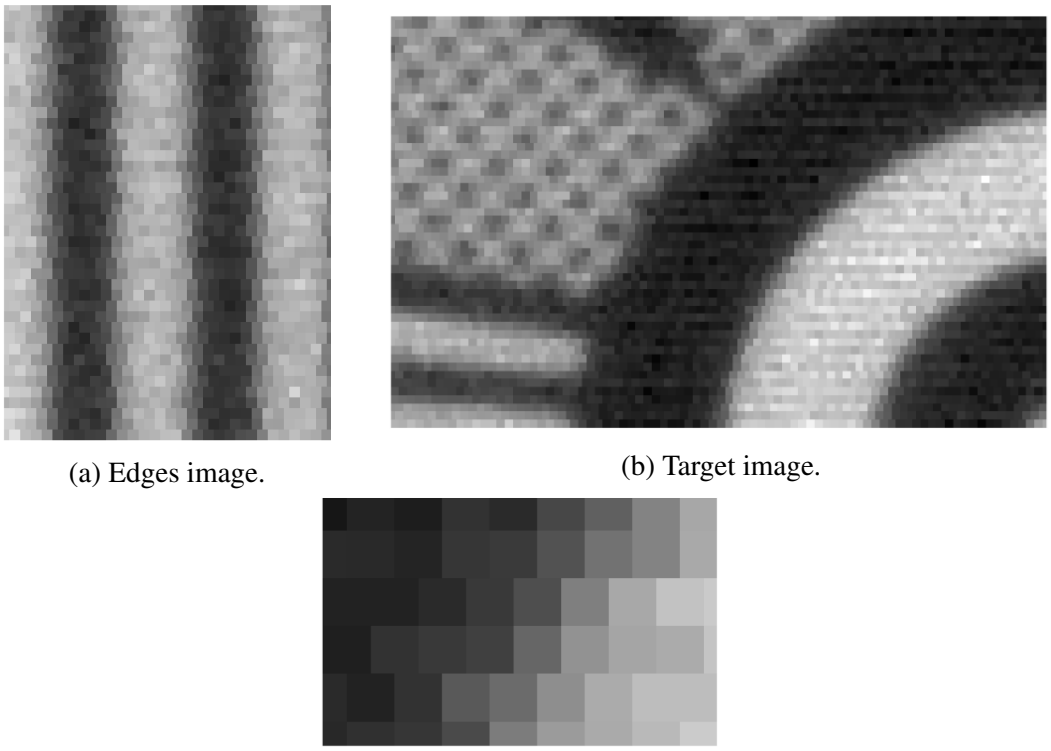
where $pn_{2n,2m}$, $pn_{2n,2m+1}$, $pn_{2n+1,2m}$ and $pn_{2n+1,2m+1}$ are the new pixels in the double matrix dimension and $p_{n,m}$ is the pixel in the acquired staggered matrix. While for rows two and three the expression can be rewritten as:

$$pn_{2n+1,2m} = pn_{2n+1,2m+1} = pn_{2n+2,2m} = pn_{2n+2,2m+1} = p_{n,m} \tag{5.7}$$

where all the n indices were shifted by an entire position in the double resolution matrix to match the half pixel position in the acquired staggered matrix. Although this process requires four times as much memory as the acquired image, it best represents the original acquired image as each pixel is displayed in the location where it was acquired.

Application

The acquired images are represented on a grid with double the resolution in Figure 5.20. The edge image looks similar to the ideal acquired image of an edge with the staggered pixel arrangement shown in Figure 5.6. The edge does not look as sharp as in the standard version because it is sampled irregularly. In addition, circular shapes appear correct with the pixels already representing the correct information. A detail of the image is presented as well to show the staggered pattern.



(a) Edges image.

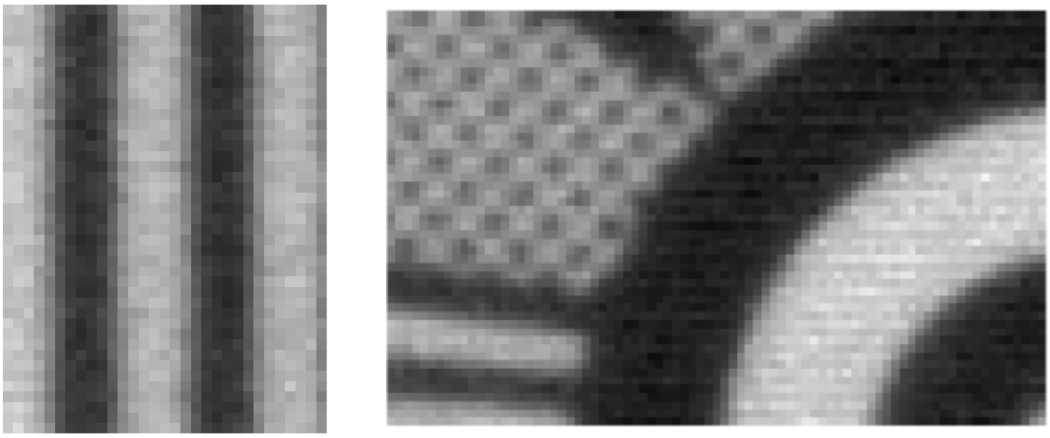
(b) Target image.

(c) Detail of the target image.

Figure 5.20: Staggered pixel STI representation of the pixels on a double resolution grid.

These images do not need any processing to be displayed as they are the true signal acquired by the sensor. Unfortunately, they require significantly more memory to be stored. In order for these to be displayed in a matrix with the same resolution as the original acquired image, a reshaping algorithm can be applied. The Matlab bicubic reshaping algorithm returns an image to the same resolution domain of the original acquired images.

Figure 5.21 shows the edge image and the target image represented on a double resolution grid and reshaped on a single resolution grid. The algorithm has again smoothed the images. The edges are sharper but the target image has lost definition. The bright pixels are no longer visible especially in the bottom left corner where the image appears smooth. This method



(a) Edges image. (b) Target image.

Figure 5.21: Staggered pixel STI representation on a double resolution grid and after a bicubic reshaping.

required four times more memory space and a bicubic reshaping algorithm. Even if the final result is better, it may not justify all this computational overhead.

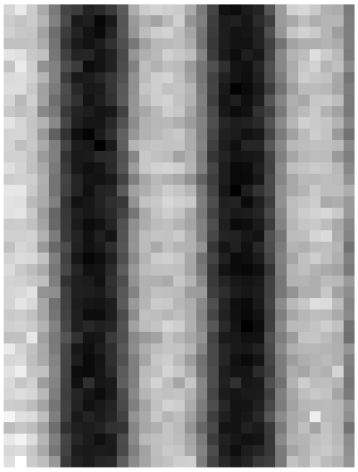
Result comparison

The results of the algorithms introduced in this chapter are presented side by side in Figure 5.22. The difference in the final images is hard to see. The average algorithm is applied on two rows of every four, which means that some of the pixels maintain their true value. As an example, one bright pixel is present in the bottom right corner. This is mitigated by the smoothing of the reshaping regression in the two other cases. In conclusion, three methods were presented to acquire and prepare for display the staggered images. These methods have increasing levels of memory requirements and complexity. The hardware efficient averaging of neighbour pixels can suffice for simple applications while the last double matrix method can be applied to enhance the image quality.

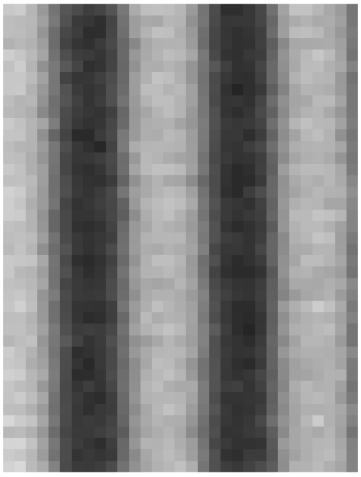
5.2.4 Colour images and RGB filtering

Silicon is sensitive to the visible spectrum but it cannot discriminate the incoming light frequency. In CMOS image sensors, colours are typically obtained by means of color filters on top of the pixel array. The color filters let only one colour pass to the single pixel and, hence, each pixel retains the color information of the built-in filter it has on top.

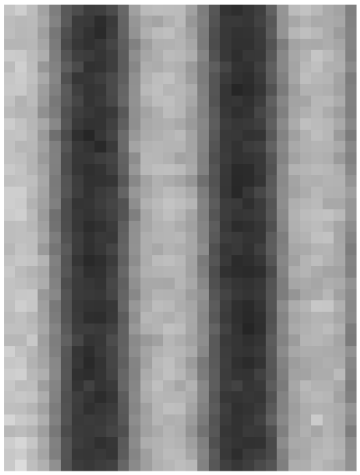
A possible Red-Green-Blue (RGB) transmittance spectrum of colour filters is shown in



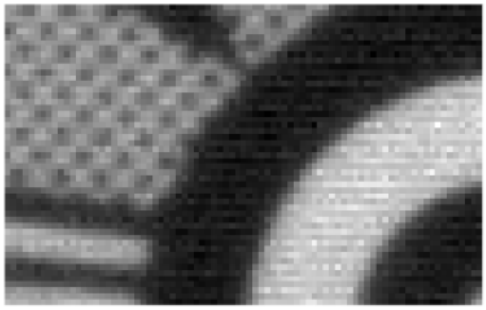
(a) Edges image average without reshape.



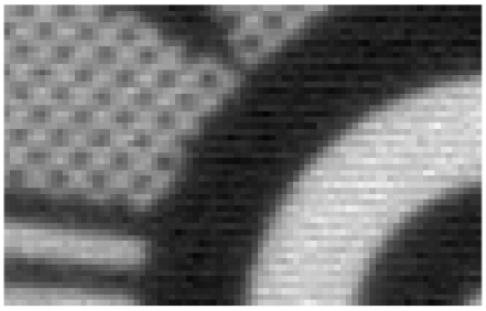
(b) Edges image interpolation reshape.



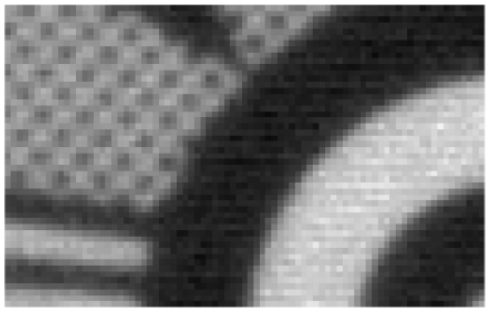
(c) Edges image double resolution reshape.



(d) Target image average.



(e) Target image interpolation reshape.



(f) Target image double resolution reshape.

Figure 5.22: Staggered pixel STI representation of the pixels on a double resolution grid and after a bicubic reshaping.

Figure 5.23. The peaks of the colour channels are centred in their corresponding wavelength. In addition, the filters are lossy as their transmittance does not reach 100 %. Many different arrangements were studied for colour filter placement on top a standard array [113]. However, the typical arrangement is known as Bayer pattern and consist of a block of four filters [114]. Two green filters are present as the human eye is more sensitive to its wavelength [115].

Figure 5.24 shows the arrangement of the Bayer pattern. The two green pixels have an additional letter to distinguish them. Gr represents the Green Red pixel while Gb represents the

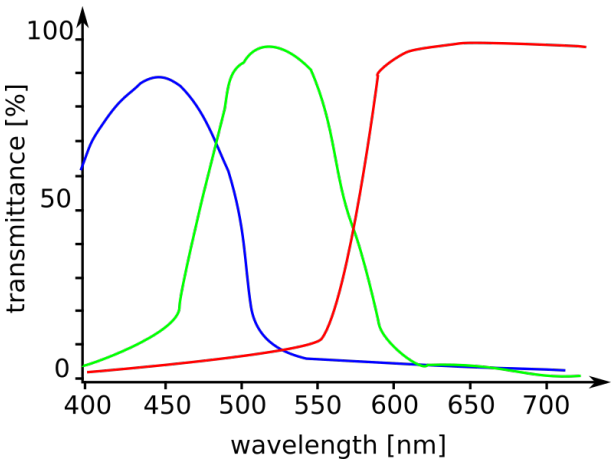


Figure 5.23: A typical color filter RGB transmittance for CMOS image sensors.

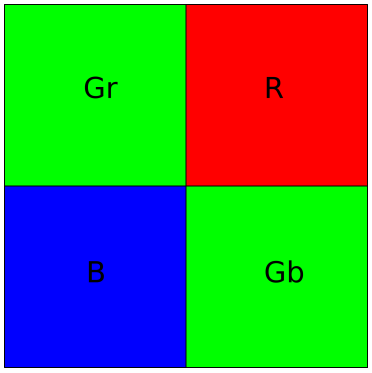
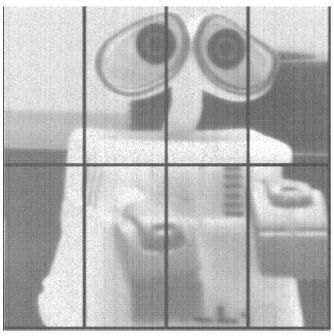


Figure 5.24: RGB Bayer pattern.

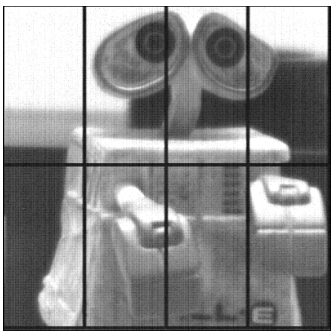
Green Blue pixel. In a standard imager, the colour information of the two missing channels in each pixel is obtained by interpolation.

In this work, no colour filters were present in the CMOS manufacturing process. For this reason, multiple images of a fixed scene were captured with RGB external filters to simulate the effect of the Color Filter Array (CFA) on top of the image sensor. The filters have different transmittance and, hence, their gain needs to be compensated to obtain white. In this project, the external filters were characterised to evaluate their gain and compensate for it in each colour channel. By using external filters, the color information of every RGB channel is acquired by each pixel.

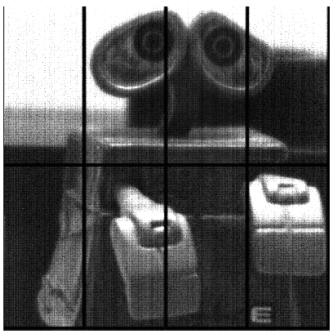
Figure 5.25 shows the acquired images with the three colour filters corrected for the different attenuation coefficient of each colour channel. The three colour channels are shown both independently and in a combined colour image. In this image, the red channel is predominant while the Blue channel is low as the scene has a limited amount of blue. Each colour channel is



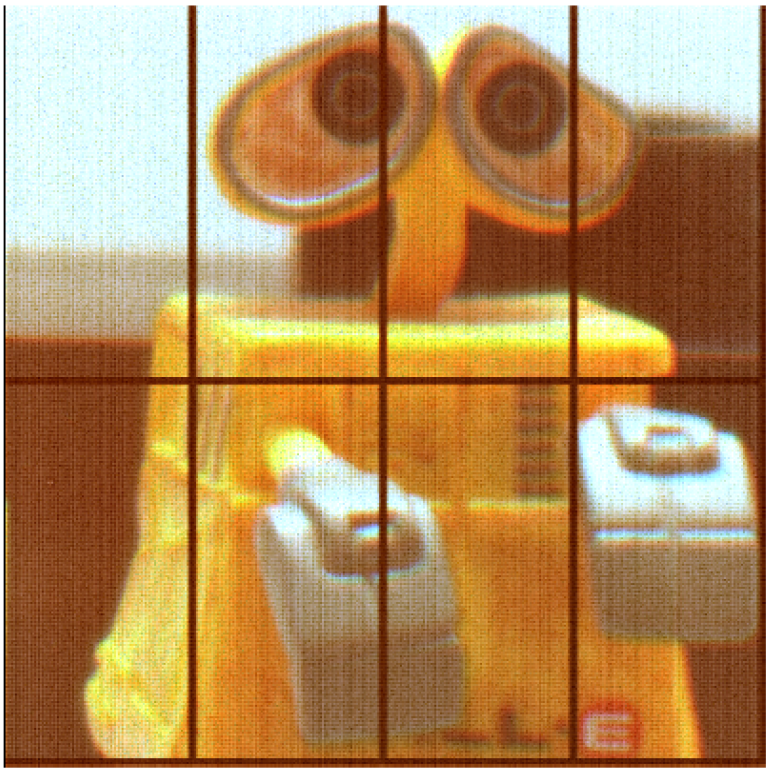
(a) Standard pixel color image. Balanced red channel.



(b) Standard pixel color image. Balanced green channel.



(c) Standard pixel color image. Balanced blue channel.



(d) Standard pixel final color image.

Figure 5.25: Standard pixel 4T color image composition of the RGB channels.

obtained by averaging 100 frames and subtracting the dark frame according to the following:

$$\begin{aligned} R_{ch} &= R_{filt} - Dark \\ G_{ch} &= G_{filt} - Dark \\ B_{ch} &= B_{filt} - Dark \end{aligned} \tag{5.8}$$

Where R_{filt}, G_{filt} and B_{filt} are the acquired images with the single color filters in front of the lens (red, green and blue respectively), $Dark$ is the dark frame acquired at the same integration time and R_{ch}, G_{ch} and B_{ch} are the acquired color channels, respectively. As each filter as a different attenuation coefficient, a flat field image is captured to evaluate the attenuation with

and without color filters.

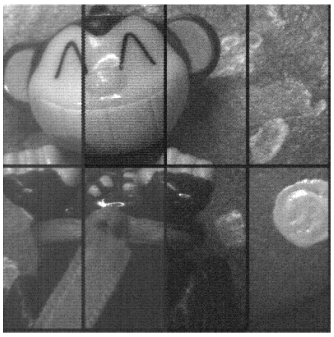
$$\begin{aligned} R_{att} &= W_{ff} - R_{ff} \\ G_{att} &= W_{ff} - G_{ff} \\ B_{att} &= W_{ff} - B_{ff} \end{aligned} \tag{5.9}$$

where W_{ff}, R_{ff}, G_{ff} and B_{ff} are the white, red, green and blue flat field images, respectively; and R_{att} G_{att} B_{att} are the attenuation coefficients for each color channel. Finally, the balanced color image is obtained by compensating each color channel with its respective filter attenuation.

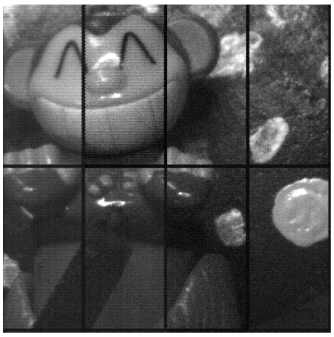
Unfortunately, high levels of non-uniformity are present in this image. However, for the purposes of color reconstruction, the white appears balanced and colors are reconstructed with a good fidelity. To study the effect of color images on the staggered pixel layout, the same technique was applied to the staggered image sensor on a different scene.

Figure 5.26 shows the effect of staggering on a natural scene image. In this case, the three different channels are combined to form the final image. At a first sight, the staggering effect is not clearly visible on this image. The sheet is limiting the image resolution and, for display purposes, no algorithm may be necessary if the resolution of the display method is lower than the acquisition resolution. However, when the display resolution increases this is no longer the case. When focusing on a detail, the staggering effect becomes more visible. For this reason, a detail is highlighted and a reconstruction algorithm developed for black and white images is applied to this colour image.

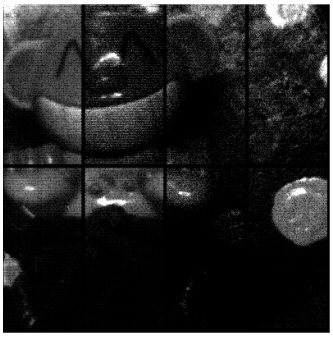
In Figure 5.27 the acquired image is displayed in a standard matrix (a). The effect of the different spatial sampling makes the vertical edge staggered and noise is visible in the eye of the puppet. The image (b) shows the acquired image displayed on a grid with double the resolution. The edge now appears straight and the eye appears smoother. This would be the image displayed on a display with the same arrangement of the pixels in the CMOS image sensor. Finally, (c) is the image obtained after a bicubic regression from the image (b) on a single resolution grid. Here the edge looks sharp while the image is smoothed overall. This is because a filtering function was applied to the image. In this work, color images were obtained by means of an external RGB filter wheel. However, in a final product, the position of a color filter array is



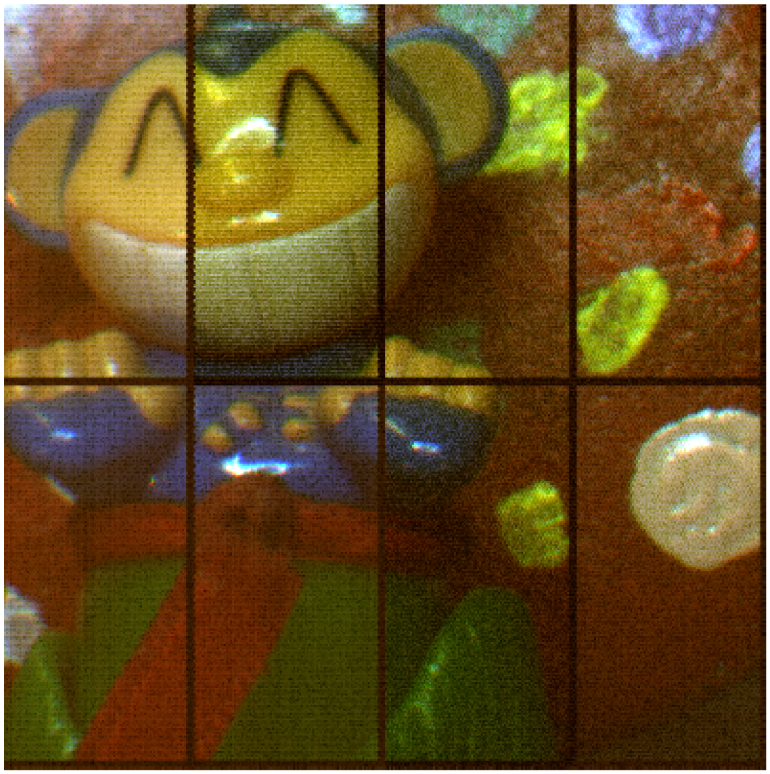
(a) Staggered pixel color image. Balanced red channel.



(b) Staggered pixel color image. Balanced green channel.



(c) Staggered pixel color image. Balanced blue channel.



(d) Staggered pixel final color image.

Figure 5.26: Staggered pixel color image composition of the RGB channels.

embedded in the CMOS image sensor. While in a standard imager the Bayer pattern is used, in a staggered arrangement of the pixels it is not possible to use the same pattern.

Figure 5.28 shows possible implementations of color filters on top of the staggered image sensor. Color information extraction and demosaicing have been widely studied for standard image sensors [116]. However, with this arrangement, new techniques are needed. The data acquired from a real color image where all the colors are present for each pixel can be used to simulate an RGB filter pattern. Algorithms can be studied to reproduce color information. The reconstructed color information can be compared to the real data in order to have a metric for the different proposed color filters.

(a) Staggered pixel color image detail. Acquired image on standard resolution grid.

(b) Staggered pixel color image detail. Acquired image on double resolution grid.

(c) Staggered pixel color image detail. Reconstructed image with bicubic algorithm.

Figure 5.27: Staggered pixel image reconstruction algorithm on a detail.

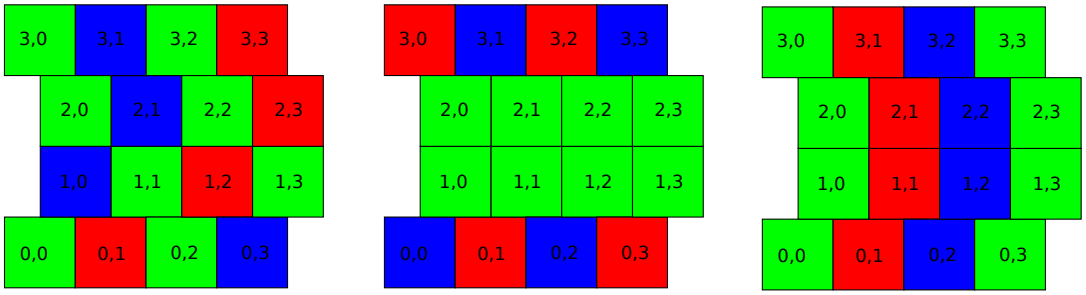


Figure 5.28: Examples of possible color filter implementations for the staggered pixel sensor.

5.3 Summary

In this chapter, acquired images from both the standard 4T pixels and the staggered pixels were presented. The staggered arrangement of pixels produces artefacts in the image display as these are caused to be reallocated in a standard matrix. In order to correctly display an image on a standard display, three different methods with increasing hardware requirements and complexity have been introduced. Results show that these three methods enable a representation of the staggered image on a matrix. In addition, a simple hardware efficient averaging between neighbour pixels is already able to return a correct image display. The considerations made in this chapter open various research questions regarding other possible algorithms that can be used with this pixel arrangement. As an example, colour images were acquired and displayed, The image processing algorithms were applied on the acquired colour image. Possible colour filter arrangements were introduced although this arrangement opens further research questions on their organisation.

Chapter 6

Conclusions

This Chapter summarises the outcome of the work conducted during four years spent on industrial research within the EDISON project. This was a broad, multidisciplinary work in the field of CMOS image sensors where analysis, design, layout, verification, characterisation and image processing were involved. It was possible to undertake many paths to enhance pixel performance. In this work, the dark current and pixel optimisation were the main concerns. In order to reduce the dark current, its sources were analysed. Process modifications and technology upgrades are the industry standards to improve on dark current performance. In this thesis approaches that do not require process modifications were proposed. In addition, a pixel optimisation strategy which maximises the fill factor was presented. This Chapter is organised as follows. Section 6.1 summarises the major conclusions of this thesis, compares the achievements to the state-of-the-art and presents a generalisation of the approach to other process technologies and pixel pitches . Section 6.2 illustrates the limitations of this work while Sections 6.3 and 6.4 introduce short and long-term future work, respectively.

6.1 Major results

This thesis explored different strategies to improve the pixel performances with a particular attention to dark current and layout optimisation. The major results can be briefly described as follows:

- A novel metric to evaluate the layout quality based on the transistor area was introduced.

- A hybrid layout strategy was proven to effectively reduce the dark current with no drawbacks on the fill factor or on the pixel full well capacity.

- A layout design strategy to minimise the number of contacts was applied to a 4T pixel causing it to be staggered. It was proven to significantly increase the fill factor and the full well capacity.

- A hardware-efficient strategy to display images acquired with the optimised staggered pixel was proposed.

The dark current can be reduced without process modification. The proposed strategy consists of a layout modification to remove the principal source of dark current around the photodiode. This technique reduces the dark current and enhances the pixel full well capacity by increasing the photodiode area. The design rules for the p-well isolation, in fact, require a narrower region for the isolation compared to the STI. This enables the photodiode to occupy the leftover space created after this modification with a relative photodiode area increase of approximately 20%. An additional study was undertaken to maximise the fill factor. By sharing the transistor contacts, their occupied area can be reduced. This means that more overall area can be occupied by the photodiodes. A staggered arrangement of the pixels was proposed with a further increase in fill factor. The relative increase for this pixel version is of approximately 50% which translates into an increased pixel full well capacity.

Table 6.1: Pixel summary

Technology	LFoundry 110 nm Image Sensors Process (preliminary)						
Version	VB1	VB2	VB3	VB4 v1	VB4 v2	VA1/2	VA3
FF [%]	24	36	29	42	45	53	42
pitch [μm]	2.4	2.4	2.4	2.4	2.4	2.4	2.4
Isolation	STI	p-well	STI	STI	p-well	p-well	STI
Noise [e]	14	15	14	13	14	-	-
CF[e/LSB]	16	21	20	17	19	-	-
LFW[e]	3672	5641	5266	6622	5300	-	-
Sat[e]	4894	7254	6403	8002	6638	-	-
DSNU[%]	4.37	2.29	2.51	2.24	2.85	-	-
PRNU[%]	5.70	1.35	1.85	4.39	3.32	-	-
DR[dB]	49	51	52	54	52	-	-
SNR[dB]	36	38	37	39	37	-	-
DC [e/s]	141	105	133	195	144	-	-
DC [pA/cm^2]	1634	813	1279	1291	890	-	-

Table 6.1 summarises the baseline versions of the pixels presented in this thesis. It is worth noting that the process was preliminary and not optimised and, hence, many parameters are not comparable to the state of the art. For example, these pixels suffer from strong non-linearity, which appeared as a visible FPN in the images presented in Chapter 5. It was impossible to measure the shared-pixel version performance with the current process and the VB4 version parameters suffered from a strong non-linear behaviour which causes an underestimation of the full well capacity. However, these results are sufficient to prove the hypothesis assumed in this thesis. The dark current density can be decreased by using the p-well and an effective layout strategy increases the fill factor.

6.1.1 Dark current reduction by layout

In CMOS technology, photodiodes are isolated by shallow trench isolation. This isolation process is shown in the literature to create a high number of defects in the silicon and, hence, to increase the dark current. Many techniques have been proposed in the literature to remove the STI around the photodiode, however, the proposed approaches are either insufficient to grant transistor isolation or to reduce the photodiode area. In this work, a hybrid approach was proposed. This consisted of sharing and flipping the layout in order to let the photodiodes sharing of their edges. In this region, the STI is removed and the isolation is granted by the means of a p-well. The STI is retained in between the photodiode and the transistors to guarantee electrical isolation. Two layouts were presented: one with STI isolation and the other with a p-well isolation. The measured dark current histograms showed a reduction of the dark current without the drawback of a smaller photodiode.

In fact, the p-well isolation design rules enable an increase in the photodiode area. The p-well isolated pixel has a higher fill factor compared to the STI isolated pixel. This is also verified through measurements of the full well capacity, confirming that the p-well version is able to accommodate more electrons. In addition, to study the effect of the distance between the photodiode and the STI, three pixel variations for each pixel version were laid out and measured. The dark current histograms show that if the photodiode is designed closer to the STI region, the dark current increases and, in particular, it has an effect on the tails of the histogram. This is due to the interaction with the STI which causes the number of hot pixels to increase. The

same experiment was conducted with the p-well isolated pixels which did not show an increase in dark current when increasing the photodiode area. This confirmed that the hybrid approach is a valid method to reduce the dark current without losing full well capacity.

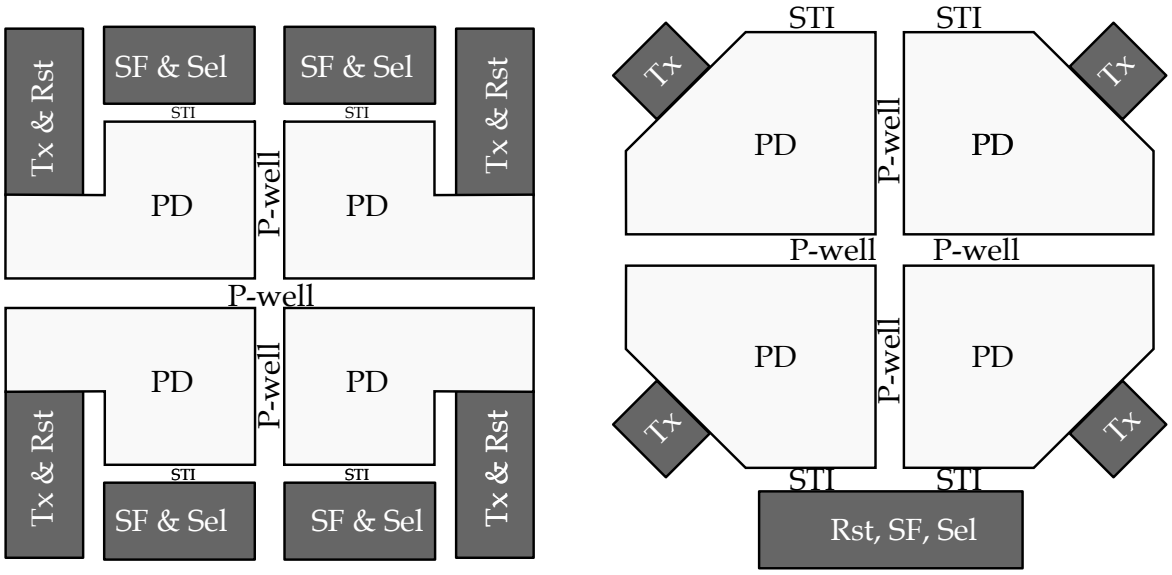
Recalling the literature review presented in Chapter 2, three pixels had their dark current measured at 60 Celsius which allows comparing the results presented in this thesis with the literature.

Table 6.2: VB2 Dark Current compared to the literature.

Author	McGrath	Yoshiara	Seo	This Work
Year	2009	2006	2014	2017
Reference	[50]	[82]	[86]	VB2
Technology [nm]	110 nm	180nm 1P3M	180 nm	110
Architecture	1.75T PMOS	1.75T	1.75T	4T
Pitch [μm]	1.4	2.5	7.5	2.4
Fill Factor [%]	30	38	43	36
Noise [e]	-	7	4	15
DC @ 60C [e/s]	22	15	104	105
DC @ 60C [pA/cm^2]	30	101	68	813
FW [e]	5500h	12000	-	7254
Lag	0	0	-	-
DR [dB]	-	64.7	-	51

Table 6.2 shows the performance of VB2 compared to the relevant work published in the literature. By comparing the density of the dark current of VB2 with the relevant literature, the dark current level presented in this work is very high. The absolute level of dark current, however, is often not in control of the designer as it is dependent on the process technology. Nevertheless, the results presented in this thesis have shown how a designer could optimise the full well capacity and the dark current by employing layout techniques within the same process technology. The technique of isolating neighbour photodiodes by the means of a p-well instead of employing the STI could be applied to any other process technology. In order to apply this technique to other processes, it is important to design the photodiodes close to each other so that they share at least two of their edges.

Figure 6.1 shows a schematic layout where a generalisation fo the approach is presented. Here, the pixel pitch is not specified. In order for the edges to be shared, a simple method could be applied. A pixel could be designed as a single square and then the same pixel could be



(a) Schematic layout to apply the p-well isolation to a 4T pixel.

(b) Schematic layout to apply the p-well isolation to a 4T 4-shared pixel.

Figure 6.1: Schematic layout to apply the p-well isolation technique to a 4T pixel and a 4T 4-shared pixel.

flipped horizontally and vertically to create a symmetric block of four pixels. The STI is then removed between the photodiodes while it is retained close to the transistors.

6.1.2 Pixel layout optimisation

Pixel layout has a strong impact on its performance. Unfortunately, there is a little literature available on this topic because layouts are usually not disclosed by the companies. This motivated a study of pixel layout optimisation and of strategies to increase the pixel performance in the light. A larger photodiode is able to accommodate more electrons and, hence, to have a higher saturation value.

In digital design, contacts are shared to find the connection schematic which minimises the area for both the pMOS and nMOS transistors. In this work, the connections were minimised by sharing the transistor contact of the supply node and of the output node. In addition, if the constraint of having a square pixel is relaxed, it is possible to share the contacts of eight transistors in line for a 4T pixel architecture. This approach increases the fill factor by 50% compared to the fully symmetric pixel layout (VB1). The considerations on the STI isolation were then applied to this staggered pixel. A version with a hybrid approach was proposed for this optimised pixel. The results show that the staggered pixels have a higher full well capacity

compared to the other versions presented in this work.

The fill factor is not the best metric to describe how well the layout is designed. This is because it can only be compared to the same pixel architecture, technology, and pixel pitch. A different metric, called Area Utilisation Factor, was introduced. It describes the area occupation by taking into account the in-pixel transistor requirements. The Area Utilisation Factor takes into account the transistor area which is usually not given in the literature. In Chapter 2, an equivalent transistor area was introduced and evaluated for the pixels presented in the literature review. This lead to Figure 2.28 which compared the equivalent transistor area for a range of pixels.

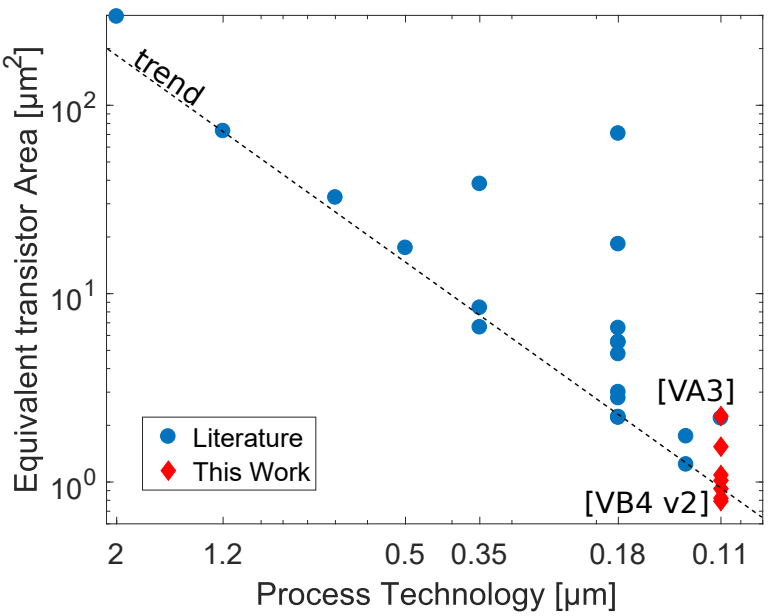


Figure 6.2: Estimated Equivalent transistor Area for different process technologies of the pixels in Table 2.1 compared to the pixels presented in this work.

Figure 6.2 compares the calculated equivalent transistor area to the pixels presented in this work. While the standard version VB2 is in line with the trend, the staggered version VB4 v2 is above the predicted trend for a lower geometry feature. The layout optimisation technique is, hence, an effective way to reduce the area reserved to the transistors and increase the photodiode area.

This technique could be applied to other pixel pitches and processes as well. To reproduce the design, it is needed to first find the optimisation path which leads to the maximum number of shared diffusions and, hence, the lower possible area occupied by the transistors. Once this is found, the transistors could be placed in line at the centre of a target grid of pitch p.

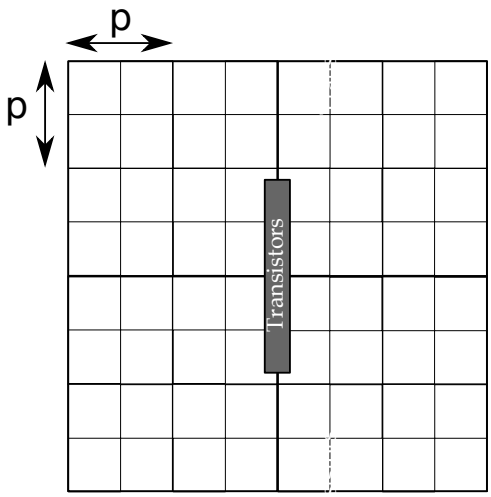


Figure 6.3: Schematic layout of the staggered approach. First step.

Figure 6.3 shows where to place initially the in-line transistors on a grid of target pitch p at the centre of that grid. The transistors are placed in line. In the case presented during this thesis, these could be the one of a 4T pixel. It is important that the first and last transistors are the transfer gate if the process foresees it. Otherwise, for a 3T pixel, it would be better to have the reset transistor at the end which certainly shares a contact with the photodiode. Once this has been placed, the transistor structure should be repeated to match the pixel pitch.

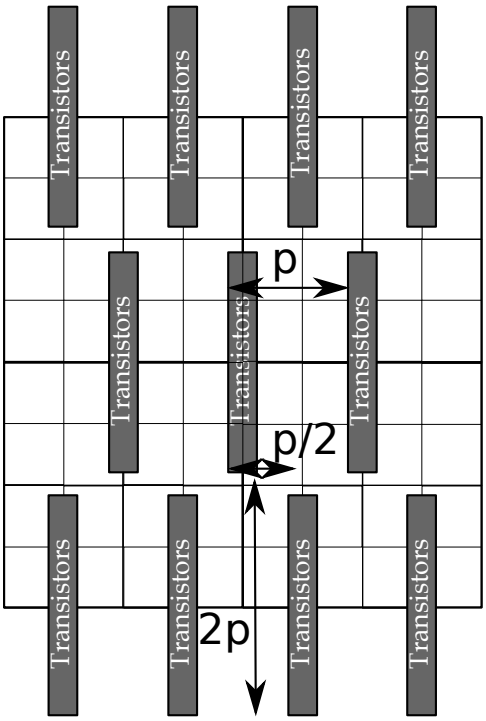


Figure 6.4: Schematic layout of the staggered approach. Second step.

The transistor line should be copied and translated first by a pixel pitch in the horizontal direction and then by half a pitch in the horizontal direction and by two pixel pitches in the ver-

tical direction as depicted in Figure 6.4. Please note that the pixels are shifted by two pitches in the vertical direction because it has been chosen that the transistor area represents the transistors of two pixels shared in the column. If this hypothesis was not true, then the transistors should be only shifted by a single pixel pitch in the vertical direction. Once this step is completed, the photodiode can then be drawn to occupy the leftover area as shown in Figure 6.5.

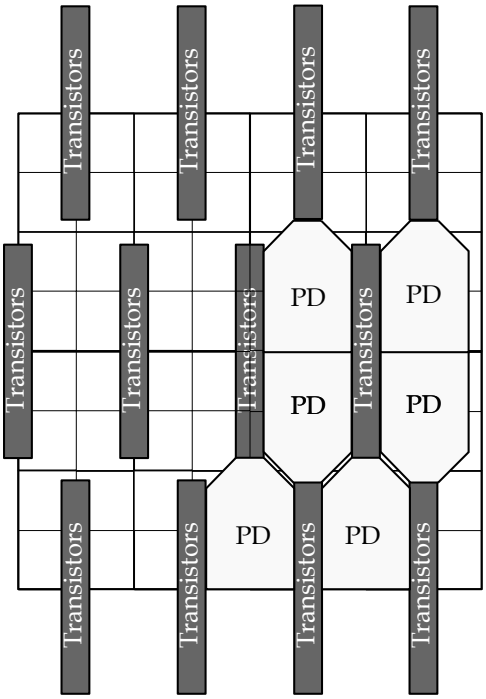


Figure 6.5: Schematic layout of the staggered approach. Final step.

By assuming that the length of the transistors is equal to L, their width is equal to W, the distance set by the technology from a diffusion to another diffusion is d, the pixel pitch is p and that the photodiode is a rectangle, a simple technique could be used to predict the fill factor for another pixel pitch and technology.

Figure 6.6 shows the assumptions made to evaluate the fill factor on a schematic layout. The photodiode area can be then found by evaluating x and y of the photodiode rectangle. Its horizontal dimension x can be written as:

$$x = p - W - 2d \tag{6.1}$$

where p is the pixel pitch, W is the width of the transistors and d is the separation between two

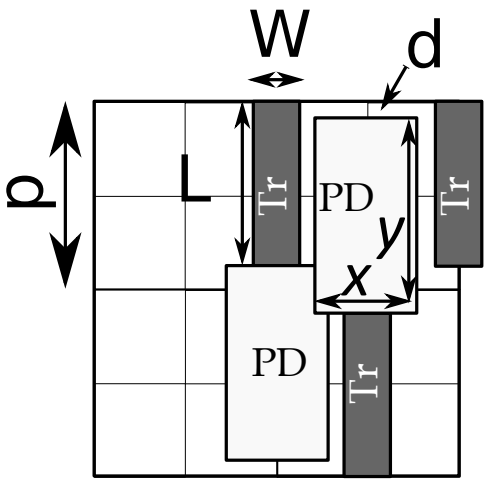


Figure 6.6: Schematic layout of the staggered approach to evaluate the fill factor.

diffusions. The photodiode vertical dimension y can be written as:

$$y = 2p - L - d \tag{6.2}$$

where L is the length occupied by the transistors. The resulting Fill Factor is hence:

$$FF = \frac{(p - W - 2d) \times (2p - L - d)}{p^2} \tag{6.3}$$

This equation models the fill factor based on simple geometrical spacing and it can be used as a tool to predict the fill factor given the pixel pitch and a process technology. If this equation is used with the LFoundry process technology parameters the result in Figure 6.7 is obtained.

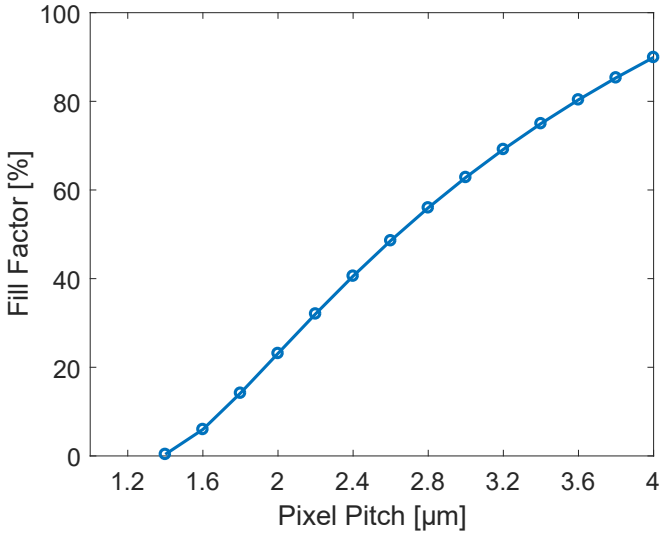


Figure 6.7: Fill Factor prediction model of the staggered pixel applied to LFoundry process technology.

This Figure shows the calculated fill factor for the geometry rules of LFoundry. The evaluated fill factor for a pitch of 2.4 μm is 40 % which is a good prediction of the real pixel fill factor. The model overestimates the fill factor for larger pitches as it was simplified as a rectangle. In fact, the corners of the rectangle are superimposed. A better, more complex model would describe the exact geometry of the implemented photodiode.

6.1.3 Display algorithms of a staggered pixel

The staggered pixel version has a different spatial sampling compared to the standard 4T pixel. When the image is displayed on a standard matrix arrangement, artefacts are visible in the image. The causes of these artefacts were investigated and three simple methods to display the images were proposed. The first is based on the averaging of two neighbouring pixels. The second represents the image on a grid with double the resolution in the x-direction and interpolates the missing pixels from the neighbours. The third represents the image as it is acquired by the sensor by doubling the resolution in both the x and y-directions. Each acquired pixel is copied four times in its correct location of the new matrix. These three methods require increasingly memory space: the first does require the same memory space as the acquired image, the second two times this amount and the third four times the same amount. If the image has to be displayed in the same resolution grid of the acquired image an additional reshaping algorithm needs to be applied to the image. This has the effect of smoothing the image. As a result, a simple average between neighbour pixel can suffice to display the image with little hardware cost.

6.2 Limitations of this work

This work was conducted within a new technology introduction of LFoundry 110 nm CMOS image sensor process. While this was an exciting opportunity to contribute to the development of a new state of art technology, it had the drawback of the unforeseen circumstances of industrial research. First, the process development kit was not completed for this technology when the sensors were designed. This introduced limitations in the design of the pixels.

In the design of the CMOS image sensor readout, the analogue models of the transistors

were not ready at that time. The readout was designed conservatively by increasing the transistor size of the switches and by decreasing the sensor clock speed operation. This was a reasonable choice as the main objective of the project was to characterise and optimise the pixel performance rather than to boost the product development. Unfortunately, the level shifters and the column bias transistors were designed with a small width. The consequence of having non-optimised periphery circuitry is translated in a higher noise and non-uniformity of the images. The absence of previous data of the pixel swing has also limited the ADC choice for the PCB board. An ADC matching the output signal from the sensors could have been chosen.

In addition to the design issues, when a new process technology is introduced, there were issues in the manufacturing process flow. The CMOS image sensors of this work suffered from a misprocess causing higher PRNU and image lag (data reserved to LFoundry). Fortunately, the chips were all manufactured with the same process and, as the scope of the work was to compare different pixel design and layout performances, it was still possible to achieve this objective. PRNU and lag were not the focus of the work. The manufacturing process is now corrected and the next generation of sensors does not present these issues.

Finally, although this was an exciting project, it was very challenging on time. In these four years, the author conducted his research at the university in Oxford, in Awaiba, a fabless design house in Funchal (PT) and in LFoundry, a Silicon foundry in Avezzano (IT). The skills required in each of these workplaces are very different and the ability to quickly learn those were crucial. The time allocated to define the project, design, manufacturing, setting up the measurement environment, debugging, measuring and writing was critical. The support of the stakeholders involved in this project was of fundamental importance to finish this project on time. The available silicon and data that generated from all the sensors under different biasing conditions and with access to the process split is significant and represents the continuation of this work which has been already undertaken by LFoundry to continuously improve their CMOS image sensor performance.

6.3 Short-term future work

In this project, nine image sensors were designed, laid out and manufactured. The obvious continuation of this work would be to analyse and compare the other already available result

from variations present on the silicon. This section will present an overview of the major analyses that could be conducted and introduce further ideas on the research topics presented in this thesis.

6.3.1 Edge detection

The impact of an edge falling on a staggered pixel arrangement was shown in Figure 5.6. On a standard matrix arrangement, all the pixels where the edge falls will have the same value in an ideal case. However, in the staggered arrangement of the pixels, the edge will fall on different positions of the photodiodes. This means that half of the pixels will have a brighter response and half of the pixels will have a darker response. In the ideal case, no transistors would be present in the pixels. If transistors are present, in the standard arrangement, the edge might fall on the transistors and hence it would not be possible to discriminate the exact location of the edge. In the staggered pixel, however, if the edge falls on the transistors in two rows it will be falling on the photodiode of the other two rows of the functional block. Implementing a method to identify and represent an edge on the staggered pixel with the available acquired images is a possible extension of this work.

6.3.2 3T pixels

Version C was designed with 3T pixels. In particular, two main variations were designed. The first is a standard 3T pixel, and the second is a 3T pixel with a tone mapping function at the pixel level that it is called 3T wide dynamic range (WDR). For the aim of this work, the pixel was designed to show that the dynamic range of a 3T pixel could be increased without increasing the pixel pitch. This is done by adding a fourth transistor at the pixel level, working as a comparator.

The schematic of this pixel is shown in Figure 6.8 where the reset transistor, $M1$, the source follower, $M2$ and the row select, $M3$, are functionally identical to those of the 3T pixel. However, the nMOS $M4$ acts as a comparator and a V_{ref} voltage is applied to its drain. This V_{ref} voltage is increased during the integration time. The pixel voltage is stored on the capacitance C. When the reference voltage is higher than the floating diffusion voltage, the nMOS $M4$ switches off. The compared value is stored on the capacitance C ready to be read out.

Figure 6.9 shows the pixel operation and the advantages of this configuration. At the be-

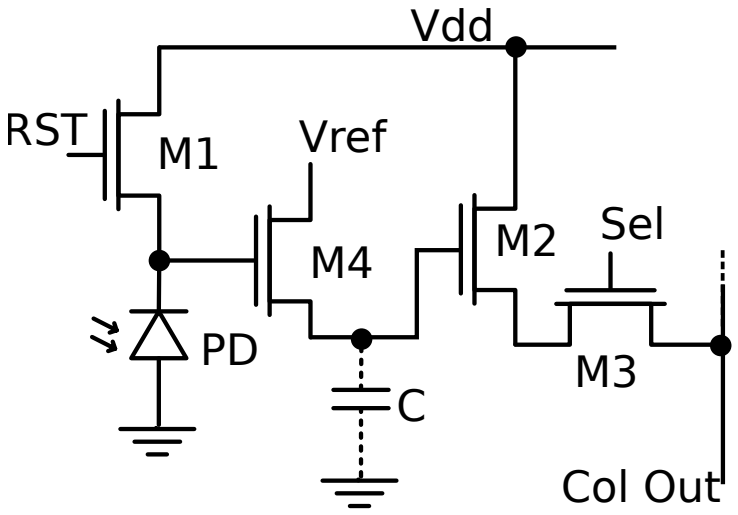


Figure 6.8: 3T wide dynamic range pixel schematic.

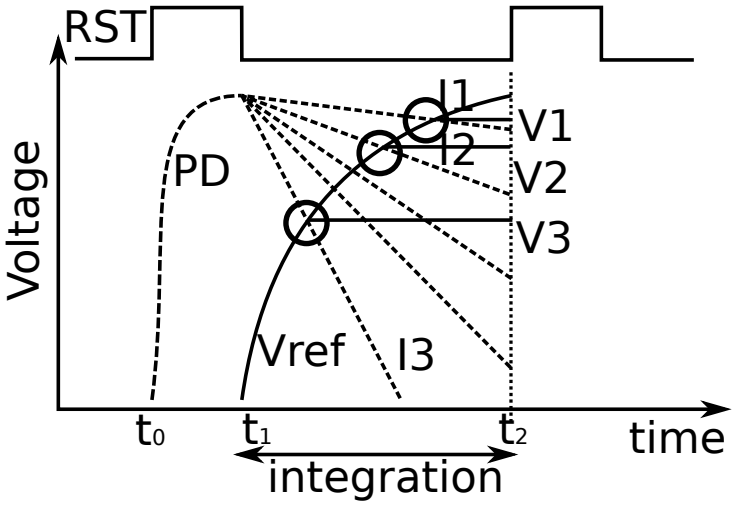


Figure 6.9: 3T wide dynamic range pixel operation.

ginning of the integration time, the reset transistor is switched off. The dotted lines are the voltage drop of the floating diffusion in the presence of increasing light levels. A low light associated with the photogenerated current $I1$ would generate the top dotted line and a voltage $V1$ in a standard 3T pixel. Unfortunately, a higher light level would produce a current $I3$ that completely discharges the photodiode during the integration time. With this pixel, the V_{ref} is increased and the output voltage $V3$ is stored on the in-pixel capacitance. This is increasing the dynamic range of the pixel as this configuration is able to discriminate more light values. Furthermore, the V_{ref} function can modulate the pixel response to enhance the low light sensitivity or the high light sensitivity according to the particular application. The capacitance C is crucial as in high light conditions it suffers from parasitic leakage. It needs to be shielded from incoming light to ensure the storage during exposure.

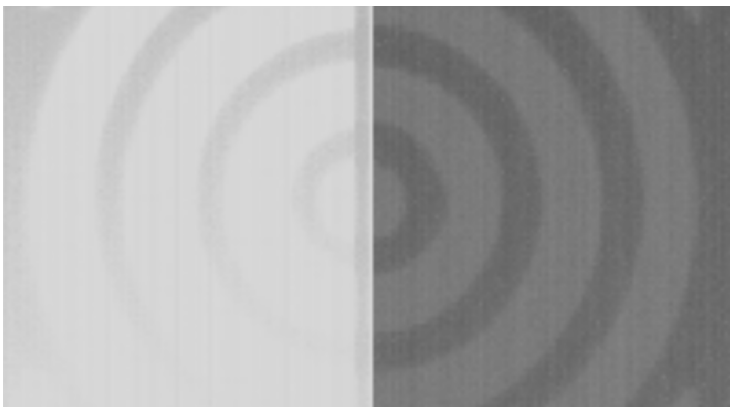


Figure 6.10: Preliminary 3T versus 3T wide dynamic range pixel image.

A preliminary result from this pixel was obtained by acquiring an image of VC where both the 3T and the 3T WDR are present. Figure 6.10 shows the image of a circular concentric target projected with the optoliner on the centre of the VC pixel matrix version. The left part of the matrix is the standard 3T pixel with a 2.4 μm pitch while the right part of the image is the novel 3T WDR pixel with the same pitch. In the same light conditions, the standard 3T pixel is completely saturated while the novel WDR pixel is holding the signal value. This is a promising result and an improved characterisation setup should be chosen to demonstrate the capability of this novel pixel.

Furthermore, the VC version has an additional layout technique to reduce the dark current of 3T pixels. In fact, two photodiodes were employed for the 3T variation. One with a pinning layer and another without a pinning layer. The boron implantation at the surface should reduce the dark current of the 3T pixel as it should fill the dangling bonds at the surface of the Silicon which are intrinsic defects of the photodiode structure. This additional implantation should improve the dark current performance of 3T pixels. A measurement set up needs to be put in place to demonstrate this effect.

6.4 Long-term future work

6.4.1 Hybrid STI pixels

In order to reduce the dark current, a hybrid layout strategy was proposed to remove the STI between neighbour photodiode and provide isolation by means of a p-well. This was removed on two of the four sides of the transistors. However, in retrospect, a better layout could have

been proposed with 2.5 sides of the photodiodes isolated by the means of a p-well.

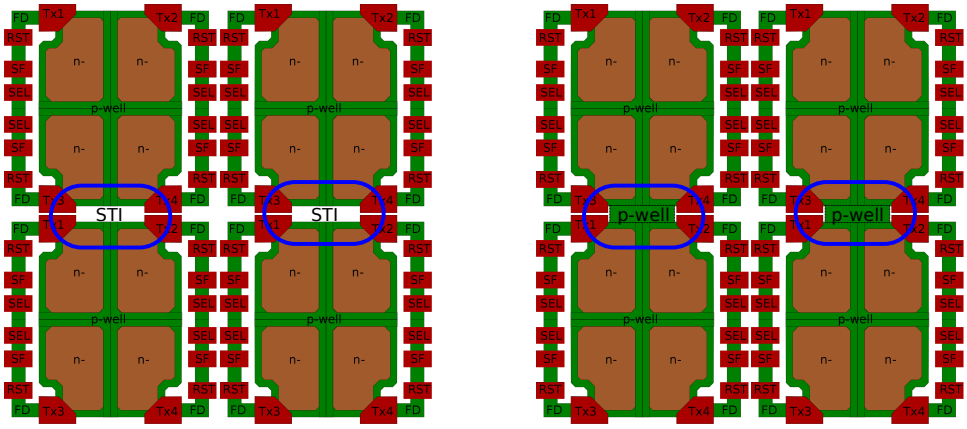


Figure 6.11: Improved p-well configuration in a block of 16 pixels.

Figure 6.11 shows the layout of the original p-well configuration version and the one with another p-well region added in between blocks of pixels. The STI close to the transistors still remains, but half of the photodiode edge can be isolated with a p-well rather than an STI. This pixel would require a new layout and another silicon run to be manufactured, however, it is expected to have a lower dark current and an even higher full well as the n-implant of the photodiode can be further expanded as the rules for the p-well minimum distance are more relaxed compared to the rules of the STI isolation.

Furthermore, for a complete study of this technique, it would be interesting to access different process technologies and study a wider range of dimensions and distances from the STI to generate a precise modelling predicting the dark current.

6.4.2 Staggered pixel architectures

One of the main results obtained in this work was the introduction of the pixel optimisation strategy that leads to a staggered arrangement of pixels. This opened other research questions already such as image display, colour filtering, and edge detection algorithms which are not related to the CMOS image sensor design itself. From a design point of view, this strategy can be applied to more complex pixel architectures to explore possible layout optimisations.

The considerations on the best path to ensure a higher fill factor were applied to a standard 4T pixel. However, the same concept can be applied to other architectures like 5T, 6T, 7T or 8T pixels [73]. As an example, let us consider the 8T pixel which is a global shutter architecture with in-pixel correlated double sampling [117, 118].

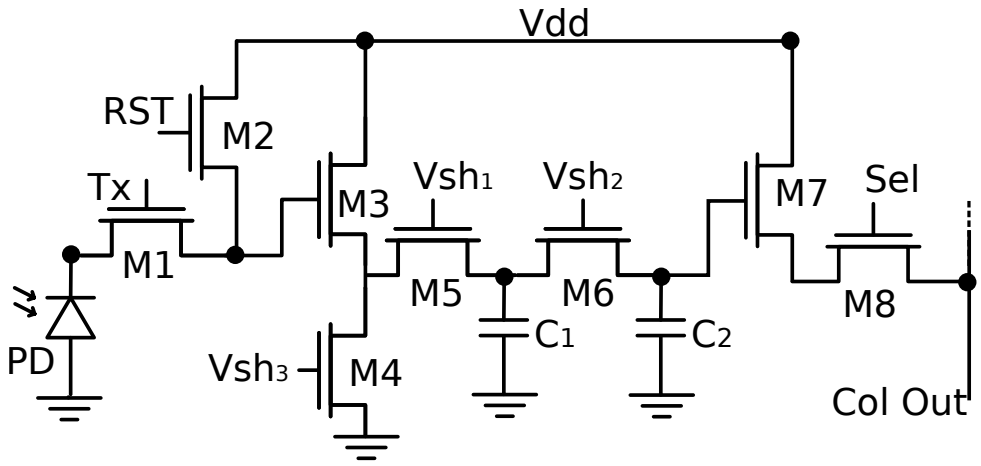


Figure 6.12: 8T Global Shutter pixel (CMOSIS like).

Figure 6.12 shows the 8T pixel architecture. In this pixel $M1$ is the transfer gate, $M2$ is the reset transistor, $M3$ and $M4$ are two in-pixel source followers, $M4$ is the in-pixel bias transistor for the first source follower stage, $M5$ and $M6$ are switches, $M8$ is the row select transistor and C_1 and C_2 are storage capacitors. The pixel operation starts after a reset of the diode. Then, the integration begins and the charge is accumulated in the photodiode. After the reset of the floating diffusion, the reset value is stored on the capacitor C_2 through the switches V_{sh1} and V_{sh2}. The second switch is closed and the integrated charge is transferred to the capacitor C_1. These values are then read out through the row selector. First, the reset is read discharging the capacitor C_2 and then the second switch is opened. The charge present on C_1 is redistributed on the parallel configuration of C_1 and C_2 and read again through the row selector. In this configuration, kTC noise is a strong issue and it can be reduced by increasing the capacitor size. In this pixel, where the number of transistors and constraints are high, sharing diffusions provides a significant amount of saved space. By using the staggered approach and sharing the column node, a possible path for this architecture can be found.

Figure 6.13 shows a possible common diffusion path in the 8T pixel. Multiple paths were used. It is more difficult to find the path that minimises the transistor area as the number of transistors and the way these are connected together increase the complexity of the choice. In this example, the red path highlights a connection from the photodiode to the column output through the transistors $M1$, $M2$, $M7$ and $M8$. The path could continue in the neighbour pixel as shown for the 4T architecture. The source ground connection of the $M4$ transistor can be shared between neighbour pixels as well. The supply voltage drain of the $M3$ transistor can be shared while the transistors $M5$ and $M6$ are placed in line to control the capacitors. Other paths

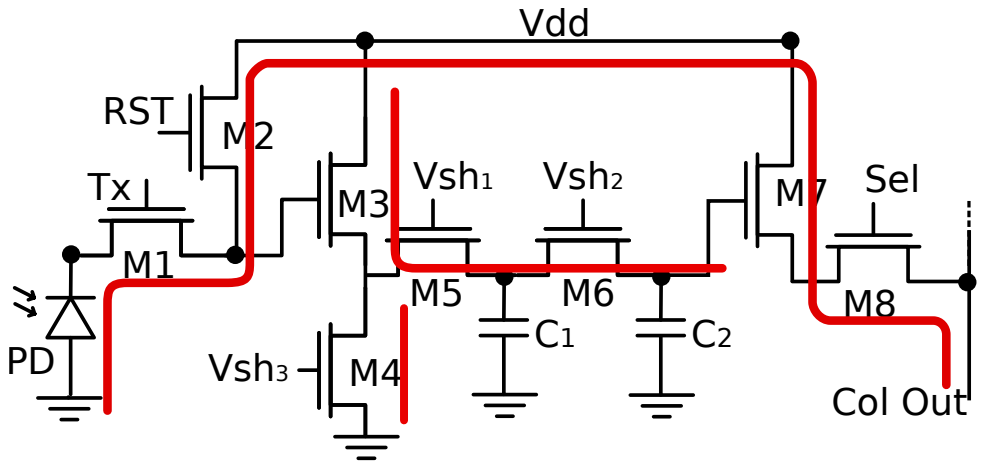


Figure 6.13: A possible sharing path for the 8T Global Shutter pixel (CMOSIS like).

are possible for this same design and a deeper layout study is needed to find which of these paths provides the best advantage in terms of space optimisation.

Appendix A

Experimental and measurement setup

This appendix presents the experimental setup, the measurement techniques, and the pixel variations. This work was conducted within the EDISON project and in collaboration with Awaiba, in order to measure the pixel performance, a printed circuit board was provided by Awaiba. In fact, their commercial image sensor evaluation board was modified to match the requirements of the test chips designed with the LFoundry IS 110 nm process, which is presented in Section A.1. Section A.2 presents the test chip features that were introduced in Chapter 3. Finally, Section A.3 presents all the pixel variations designed and manufactured for the purposes of this project.

A.1 Printed circuit board

The printed circuit board is divided into two main parts. The first is a commercially available FPGA board and the second is a custom in-house design to communicate to the sensor. The FPGA module is a Cesys EFM-02 FPGA board with an onboard Xilinx Spartan 6 X150. The board is controlled by a PC through fast USB as in Figure A.1 where the Printed Circuit Board (PCB) schematic is shown. Awaiba also provided custom software to read data from the FPGA and store it as a file image. Additional OS software was written with Autohotkeys to automate the image collection. The custom printed circuit board was designed to interface the test chip to the Cesys board. While this is not the topic of this work, it is worth noting that the test chip has two pads for output as shown in Figure A.2. One pad is used for the pixel signal value while the other is used for the reset value. Each of these pads is connected to a 10 bit ADC converter,

which converts the analogue information from the sensor to a digital value readable by the FPGA. In addition, the digital signals generated by the FPGA to control the ASIC operation are converted to analogue values through dedicated DACs present on the custom board.

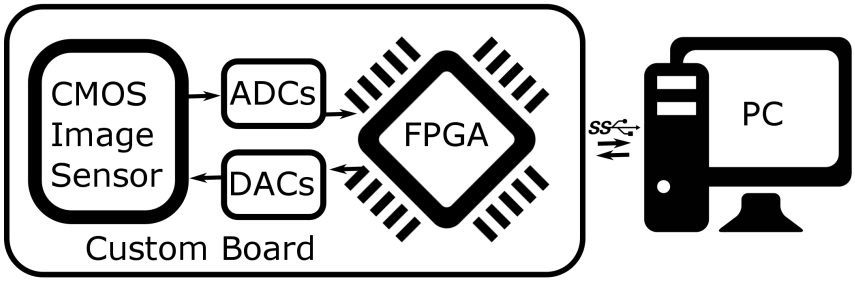


Figure A.1: Board and sensor communication to a PC.

This custom board was designed to enable the testing both at the package level and at the wafer level. In fact, two different boards were manufactured. The first with a chip holder, which allowed to insert packaged chips for bench testing, and the second with special needles to enable image readout directly on the manufactured wafers. While this is not a standard requirement in the image sensing field, this feature was requested from LFoundry to enable fast wafer-level image sensor characterisation.

A.2 ASIC features

The pixel matrix needs a full imaging system in order to collect images. In this section, the version B test chip is presented to give a full picture of the design and to explain the testing operating conditions of the test chips. Although slightly different chips were designed, their functionalities are identical. A single chip readout is presented as an example.

Figure A.2 shows the block diagram of the chip. Pads are the grey boxes with a cross, and enable external communication of the sensor to the board and the FPGA. Table A.1 describes the functions of each pad signal. The core of the chip consists of the pixel matrix, the analogue column readout and the row addressing blocks. Additional functional blocks are present such as output drivers and bias generators, a test multiplexer for debugging purposes, and a state machine to switch operation from readout to register setting. Power supplies and grounds are highlighted in bold.

External signals control the chip functional blocks. In particular, the main programmable

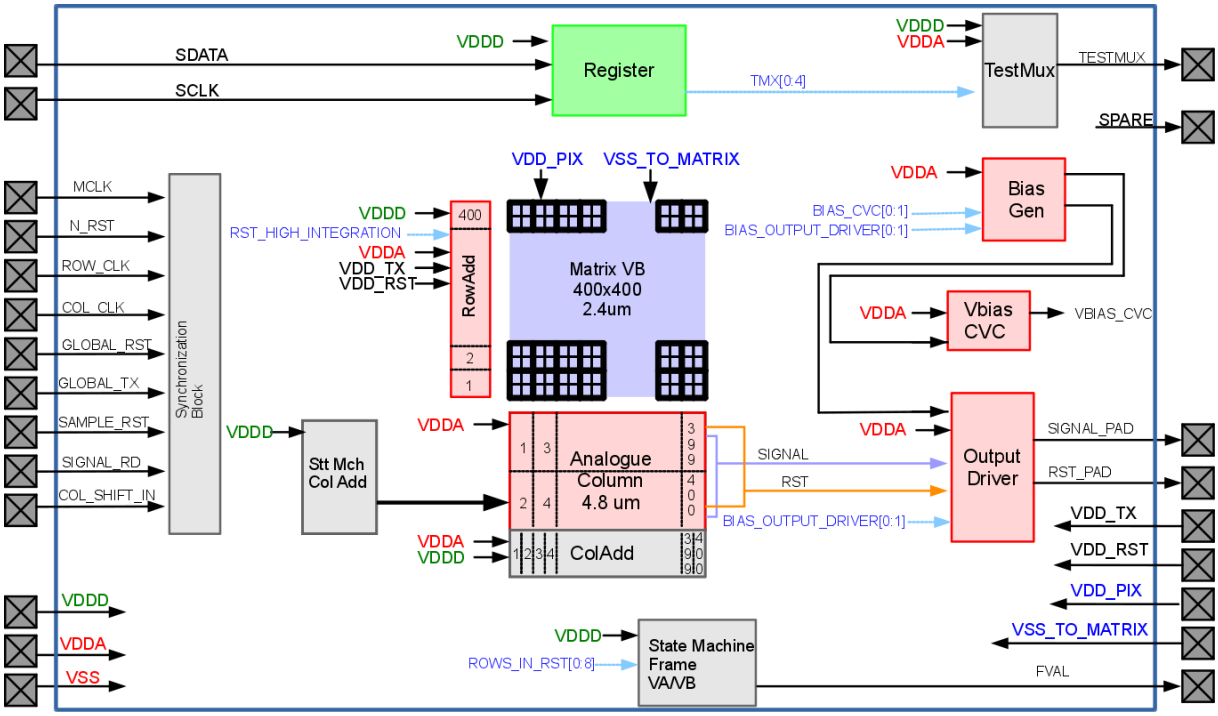


Figure A.2: VB test chip block diagram.

Table A.1: Signal summary and functionality

Signal	**Functionality**
Global	
MCLK	Main Clock
RST_LOGIC_N	Negative Logic Reset
Row *Addressing*	
ROW_CLK	Row Clock
GLOBAL_RST	Generates the Reset signal RST[1:400] for the pixel matrix
GLOBAL_TX	Generates the Transfer gate signal TX[1:400] for the pixel matrix
Column Addressing and Readout	
COL_CLK	Column Clock
SAMPLE_RESET	Stores the reset value on a capacitor to perform CDS
SIGNAL_READOUT	Reads the pixel data
COL_SHIFT_IN	Triggers the column readout
Register Writing	
SCLK	Serial Clock for the internal register
SDATA	Serial Data for the internal register
Power Supply	
VDDA	Analogue Power Supply
VDDD	Digital Power Supply
VSS	Ground
VDD_PIX	Pixel Matrix Power Supply
VSS_TO_MATRIX	Pixel Matrix Ground
VDD_RST	Reset Voltage
VDD_TX	Transfer Gate Voltage

features of the sensors are the number of rows in reset, which controls the integration time, and the bias currents for the column and the output stages. When correctly controlled, the ASIC sequentially sends analogue data to the output pads. The output sequence starts from the bottom left pixel (1,1) to the top right pixel (400,400).

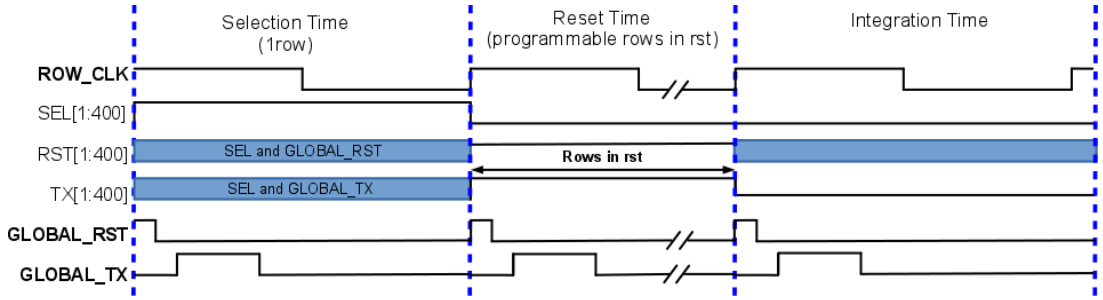


Figure A.3: VB rows timing diagram

A timing example to control these signals is shown in Figure A.3, where the signals in bold (ROW_CLK, GLOBAL_RST, GLOBAL_TX) are provided externally to the ASIC, while the others (SEL, RST, TX) are generated internally. Once the row is selected (SEL high), first, the reset signal of the floating diffusion is read (GLOBAL_RST and RST high). This is stored on a capacitor along the column, then the transfer gate is opened to enable the charge transfer from the photodiode. After the readout, rows are held in reset for a programmable amount of time. The number of rows in reset defines how many rows are held in reset after the readout. A higher number of rows in reset translates into shorter integration times. For the sensors characterisation, it is worth considering the integration time. For this ASIC it can be calculated as:

$$Integration\ Time = Row_{period} \times (Row_{btwf} + Row_{nbr} + Rows\ in\ Reset) \tag{A.1}$$

where Row_{period} is the Row period, Row_{btwf} is the number of row periods between the frames allowed for register configuration, Row_{nbr} is the total number of rows, and $Rows\ in\ Reset$ is the programmable number of rows in reset. For the considered version, the minimum and maximum integration times can be calculated, and are 1.2 ms and 163.6 ms respectively. The flexibility to program the integration time enables a fine control of the exposure. The four shared pixel integrated circuit has a similar architecture to the non-shared version. The main

difference is on the row selection. As the rows are shared, the readout of two adjacent rows is simultaneous. For this reason, the main clock to control the sensor is provided at a lower frequency. This enables the possibility of having comparable integration times for the two chip versions.

A.3 Pixel variations

The complete variation sets for all the windows are listed in table A.2 which highlights in grey the variations presented in this thesis. The number of pixels present in this experiment is high. However, for each chip version, the pixels only have a limited number of variations. The variation column summarises what is modified for each window of pixels. In particular, PD are photodiode variations while TX are the transfer gate variations. In addition, the column refers to the variation type. The lable p-well refers to variations of the p-well, n-implant refers to variations of the n-implantations. SF, RST, SEL length are variations of the channel length of the readout transistors, FD area is an increased floating diffusion area, metal grid is a grid of symmetric dummy metal around the photodiode, top metal is a window covered by an additional level of metal, GND represents the presence of a ground contact in the array. The variations in VC are on the photodiode (presence of a pinning layer in 3T pixels) and on the opened contact on the photodiode. The version VD has instead single pixels to test low dark current structures introduced in this thesis. In particular, these are a logarithmic pixel, low dark current pixels, 5T Operational Amplifiers pixels and a single photodiode structure. This high number of pixels was needed to characterise the LFoundry imaging sensing process technology.

Table A.2: Variation split table of the manufactured pixels.

Version	**Pixel**	**Isolation**	**Fill Factor**	**Variation**
VA1_base	4T-Shared	p-well	53%	no
VA1_a	4T-Shared	p-well	53%	TX p-well
VA1_b	4T-Shared	p-well	53%	TX n-implant
VA1_c	4T-Shared	p-well	53%	TX p-well & n-implant
VA1_d	4T-Shared	p-well	54%	PD p-well & n-implant
VA1_e	4T-Shared	p-well	53%	PD p-well

Table A.2: Variation split table of the manufactured pixels.

Version	Pixel	Isolation	Fill Factor	Variation
VA1_f	4T-Shared	p-well	54%	PD n-implant
VA2_base	4T-Shared	p-well	53%	no
VA2_g	4T-Shared	p-well	53%	SF length
VA2_h	4T-Shared	p-well	53%	RST length
VA2_i	4T-Shared	p-well	53%	SF + RST length
VA2_k	4T-Shared	p-well	53%	Tx - (FD Area)
VA2_l	4T-Shared	p-well	53%	metal grid
VA2_m	4T-Shared	p-well	53%	GND
VA3_base	4T-Shared	STI	42%	no
VA3_a	4T-Shared	STI	42%	TX p-well & n-implant
VA3_b	4T-Shared	STI	47%	PD n-implant
VA3_c	4T-Shared	STI	53%	PD n-implant
VA3_d	4T-Shared	STI	37%	PD n-implant
VA3_e	4T-Shared	STI	42%	GND
VA3_f	4T-Shared	STI	42%	Tx FD Area
VB1_base	Fully Sym	STI	28%	no
VB1_a	Fully Sym	STI	28%	TX p-well
VB1_b	Fully Sym	STI	28%	TX n-implant
VB1_c	Fully Sym	STI	28%	TX p-well & n-implant
VB1_d	Fully Sym	STI	28%	metal grid
VB1_e	Fully Sym	STI	28%	top metal
VB1_f	Fully Sym	STI	28%	metal grid & top metal
VB2_base	4T-NS	p-well	36%	no
VB2_a	4T-NS	p-well	36%	TX p-well
VB2_b	4T-NS	p-well	36%	TX n-implant
VB2_c	4T-NS	p-well	36%	TX - (FD Area)
VB2_d	4T-NS	p-well	36%	TX n-implant

Table A.2: Variation split table of the manufactured pixels.

Version	Pixel	Isolation	Fill Factor	Variation
VB2_e	4T-NS	p-well	37%	PD n-implant
VB2_f	4T-NS	p-well	37%	PD n-implant
VB2_g	4T-NS	p-well	36%	PD n-implant
VB3_base	4T-NS	STI	29%	no
VB3_a	4T-NS	STI	29%	TX p-well
VB3_b	4T-NS	STI	29%	TX n-implant
VB3_c	4T-NS	STI	36%	PD n-implant
VB3_d	4T-NS	STI	29%	TX p-well & n-implant
VB3_e	4T-NS	STI	24%	PD n-implant
VB3_f	4T-NS	STI	27%	GND
VB4_base_v1	4T-NS	p-well	42%	no
VB4_a_v1	4T-NS	p-well	42%	TX n-implant
VB4_b_v1	4T-NS	p-well	42%	TX p-well & n-implant
VB4_c_v1	4T-NS	STI	38%	PD STI
VB4_base_v2	4T-NS	p-well	43%	no
VB4_a_v2	4T-NS	p-well	42%	PD n-implant
VB4_b_v2	4T-NS	p-well	43%	PD n-implant
VB4_c_v2	4T-NS	p-well	42%	TX size
VC1_base	3T	STI	36%	no
VC1_a	3T	STI	36%	PD pinning
VC1_b	3T	STI	36%	contact
VC1_ac	3T	STI	36%	contact
VC1_base_w	3T-WDR	STI	21%	no
VC1_a_w	3T-WDR	STI	21%	PD pinning
VC1_b_w	3T-WDR	STI	21%	contact
VC1_c_w	3T-WDR	STI	21%	contact
VD1_a	4T-NS	p-well	36%	parallel matrix

Table A.2: Variation split table of the manufactured pixels.

Version	**Pixel**	**Isolation**	**Fill Factor**	**Variation**
VD1_b	3T LOG	na	na	log pixel
VD1_c	LDC	na	na	low dark current pixel
VD1_d	LDC	na	na	low dark current pixel v2
VD1_e	5TOPA	na	na	5TOPA
VD1_f	5TOPA	na	na	5TOPA
VD1_g	photodiode	na	na	Accessible single PD

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