

Roll-to-roll processing of flexible electronics: transistors, circuits and devices

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Abstract

The breakthrough of flexible electronics depends upon suitable large-scale manufacturing routes, likely requiring very low cost, high-throughput processing techniques. Our approach to development of organic electronics considered high-speed roll-to-roll processing routes already employed industrially to consider their applicability in creating transistors and circuits. We consider the advantages and challenges of a vacuum-deposition approach, and then discuss the development of organic field effect transistors that use evaporation for all required layers. These transistors have been employed in simple circuit elements and these circuits and transistor arrays have shown yields of close to 100%. For circuit development, in-line in-vacuum high throughput patterning techniques require further exploration, and first steps considered in Oxford are described.

Introduction

An approach to flexible electronics

The attraction of electronics devices or circuits as a technology can be based around: i) the mechanical flexibility of the end product, such as for wearable technologies or flexible displays for example; ii) because of the conformality of the product to complex shapes, such as for flexible lighting or photovoltaics on curved surfaces; iii) or because of the opportunity for low cost roll-to-roll processing.

One approach to development of flexible electronics is to design and build lab-scale devices and then to consider the manufacturing options at this point. If the manufacturing issues cannot be addressed, an alternative is to return to design of new device structures. Our approach has been to start from the perspective of what manufacturing routes are available and use this to inform the device design and materials choices. As an example of this approach, this paper describes our approach to the roll-to-roll manufacture of organic thin film transistors (OTFTs) and circuits based on them.

OTFTs

Several requirements were chosen for our approach:

- i) High deposition rates: our base manufacturing methods are based on those already employed in packaging films.
- ii) Mechanical properties: all materials used are ductile, metals or organics
- iii) Multiple layers: building device structures requires the deposition of multiple, different layers, so the processes employed need to allow for deposition without damage to underlying layers.
- iv) Temperature: all processes need to be compatible with the temperature limitations of low-cost polymer film substrates.
- v) Stability: any materials used need to be stable to subsequent deposition processes and show adequate stability for application with available encapsulants.
- vi) Patterning: for the creation of circuits, all layers need to be patterned in the plane of deposition using in-line processes, and the dimensions of the device should reflect the patterning resolution available.

Comparison with solvent deposition methods

The example demonstrated here is based on an all-vacuum-deposited device, however there has also been considerable development of organic electronics based on materials deposited ambiently from solution. Summarized briefly here are some of the benefits of each of the approaches over the other. For solvent-based processing the capital expenditure on equipment is often lower – the cost of running the process may be comparable between the two cases, but the initial investment required for the vacuum approach may be unattractive. However, the vacuum deposition route can give rise to some clear materials advantages such as:

- i) Pure materials can be deposited e.g. a wider range of highly conductive metals, pure molecular materials;
- ii) Multiple layers can be deposited without the requirement of orthogonal solvents and wettability issues;
- iii) Thinner layers may be possible with good thickness control.

In-line patterning and registration for vacuum roll-to-roll is currently less developed and this paper will mention a couple of routes of investigation in materials patterning.

Experimental methods

Our devices are based on a bottom gate top contact configuration on 125 μm thick polyethylene naphthalate (PEN) substrates (DuPont Teijin Films). Al gate contacts were evaporated through a shadow mask, followed by a $\sim 1\text{ }\mu\text{m}$ thick tripropyleneglycol diacrylate (TPGDA) layer deposited by flash evaporation followed by Ar plasma cure. In some cases the TPGDA surface was modified by a spin-coated polystyrene from 0.6wt% toluene solution. A 70nm Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) semiconductor was evaporated followed by gold source/drain contacts. Transistor and circuit characteristics were measured in air using two source meter units (Keithley, Model 2400) or a Keithley 4200 semiconductor characterization system following the IEEE Standard [1].

Results and Discussion

Metallization

Conductive track and vias are deposited by resistive evaporation with shadow masking, but can be patterned using an oil demetallization process, in essence a thermal lithography [2].

Gate insulator

The gate insulator material employed is based on a diacrylate monomer, TPGDA, that is flash evaporated onto the polymer substrate (Figure 1). On condensation of the monomer it can be cured by an energy source sufficient to invoke free radicals into the coating, and hence to initiate polymerization.

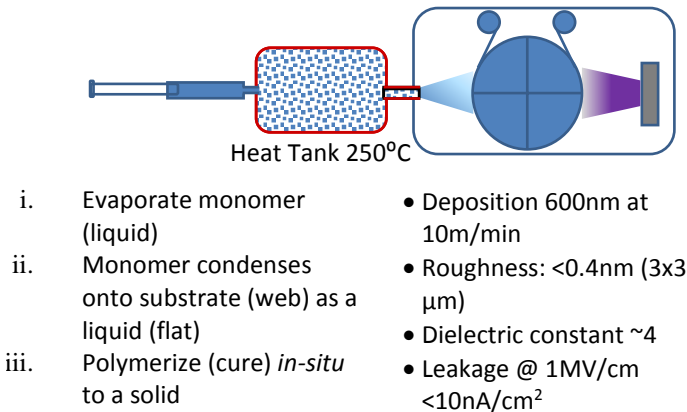


Figure 1: Schematic diagram of the polymer deposition process. The injected monomer is evaporated and condenses onto the moving web where it is subsequently polymerized, in the case of a difunctional acrylic to a cross-linked network, by either an electron beam or a plasma.

The attractions of this approach to deposition of the gate insulator are that it is high-rate deposition process (e.g. several hundred m/min is possible), and it produces very flat, homogeneous, layers arising from the fact that the film first forms as a liquid layer, filling any roughness or steps (e.g. gate contacts) in the underlying layer. Finally, this deposition approach provides a high quality continuous layer: in contrast to solution deposited polymers, in which the majority of the mass deposited (the solvent) is removed from the layer subsequent to deposition. We manufactured batches of 96 transistors to test the yield of consistently-performing transistors from our manufacturing process. The first batch employed a solution-deposited PS gate insulator, and the second batch the evaporated TPGDA layer with a spin-coated PS surface modification layer. The solution-deposited batch showed a 66% yield of transistors, with those that failed failing primarily due to leakage of current from gate to drain

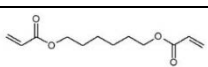
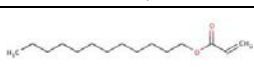
through the insulator layer. By contrast, with the exception of a few transistors mechanically damaged at the edge of the sample, all the transistors gave good and consistent transistor behavior, giving an effective 100% yield [3].

Curing the acrylate layer is critical to high performance of the transistor devices. The degree of cure of the acrylate can be characterized by FTIR spectroscopy to identify the presence of any C=C groups remaining in the layer, which are characteristic of unreacted acrylate groups [4]. However, even once there is no trace of C=C in the spectrum, curing is not complete, and we observed that we needed to cure more completely than this to avoid leakage of current between gate and drain in the first instance, and, subsequently to remove traces of hysteresis in the current-voltage behavior as the gate voltage is cycled. The best performing devices were those that were cured in the Ar plasma struck in front of one of our sputter cathodes, through which the substrate passes.

With a well-cured acrylate, gate leakage and hysteresis can be eliminated [5], and this is assisted by the difunctional material which forms a crosslinked network of polymer in which the molecules are not mobile. Such a functional network material will tend to give rise to a polarizable surface chemistry, but previous observations have suggested that a non-polar surface is preferable to promote high mobility in the subsequently deposited semiconductor [6,7]. Our own investigation, comparing a range of materials of varying surface polarity spin-coated onto the TPGDA layer prior to semiconductor deposition position confirmed this [8]. The highest mobility transistors were achieved with the least polar surface, such as with a spin-coated PS layer. Transistors with a TPGDA gate insulator with a PS surface modification and DNTT semiconductor showed very strong transistor characteristics for a roll-to-roll processable deposition method: a mobility in excess of $1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, $I_{\text{on}}/I_{\text{off}}$ of 10^7 , threshold voltage smaller than -1V and a subthreshold swing of 0.5V/decade. The characteristics are limited by the size of the gap between source and drain consistent with this high speed roll-to-roll process, in comparison to the narrower gaps that can be achieved with photolithography methods.

Having established that a TPGDA insulation layer surface-modified with a non-polar polymer layer performs well as the dielectric layer in transistors, we have been able to give a first demonstration of an in-line in-vacuum method to achieve this [9]. In this case we mixed a difunctional acrylate, 1,6-hexanediol diacrylate (HDDA) with a monofunctional acrylate, lauryl acrylate (LA) which has a long aliphatic, non-polar 'tail', and then flash evaporated a cured this mixture. Contact angle measurements (Table 1) indicated that the LA at the surface made this surface less polar, and the transistor performance (illustrated in Table 1 as the semiconductor mobility) was improved substantially by this non-polar addition. Figure 2 illustrates how similar the performance is between the vacuum-deposited surface-modified material and the control sample, which had a spin-coated PS layer.

Table 1: Comparison of a single monomer (HDDA) dielectric layer with that containing 17vol% lauryl acrylate.

	HDDA	HDDA/LA
Molecular structure		
Water contact angle	60°	86°
OTFT mobility ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	0.08 ± 0.06	0.51 ± 0.02

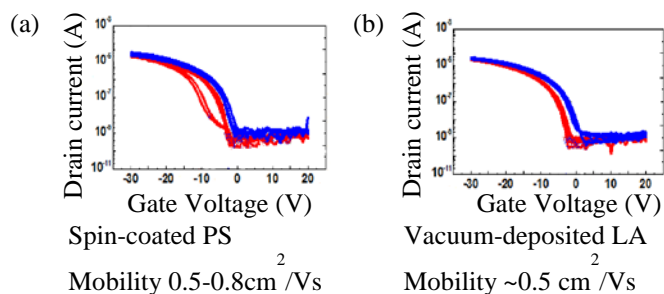
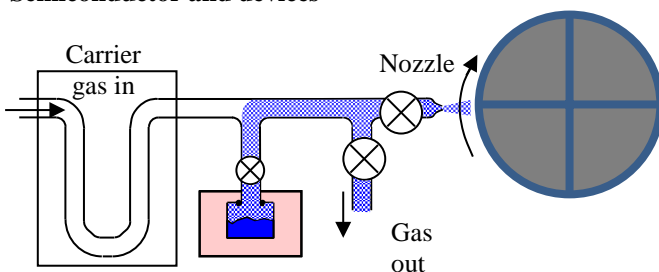


Figure 2: Transfer transistor characteristics of batches of 7 transistors comparing HDDA acrylate gate insulator layer with (a) a subsequently spin-cast PS layer and (b) an in-line deposited HDDA containing 17vol% LA.

Semiconductor and devices



Gas heating Semiconductor
furnace furnace

Figure 3: Schematic diagram of the OVJP process. As the valve at the nozzle is opened and closed the semiconductor vapour is deposited in lines or spots onto the moving substrate.

The semiconductor material can be deposited under modest vacuum conditions, such as found in a typical R2R metallization system, and produce the good devices performances reported above. As a step towards avoiding the requirement for a solid mask for patterning, which is cumbersome in a R2R system, we have investigated the use of organic vapour jet printing (OVJP) as a means to in-line pattern the semiconductor for transistor applications. OVJP, illustrated schematically in Figure 3, has been used for OLED production [10] and has also been demonstrated for OTFTs in the lab [9,11-13]. This approach is essentially the vapour analogue of ink-jet printing. We have demonstrated its applicability in a R2R system, producing well-performing transistors with webspeeds of up to 15cm/min with a deposition rate of up to 200nm/s.

Circuits

Now that this OTFT manufacture using R2R methods has been demonstrated, we have applied it to a range of circuit elements, starting with simple invertors and logic gates, 5, and 7 stage ring oscillators [14] and a static ram circuit [15]

Conclusions

High quality transistors have been demonstrated based on an all-evaporated manufacturing route suitable for high-speed roll-to-roll processing. Approximately 100% yield of reproducible transistors has been demonstrated with a mobility in excess of $1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ with source/drain width $1000 \text{ }\mu\text{m}$ and length $50 \text{ }\mu\text{m}$. An in-line interfacial dielectric surface modification using lauryl acrylate has been demonstrated along with OVJP patterning of the evaporated organic semiconductor, showing good device performance.

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