

Device-Level Photonic Memories and Logic Applications Using Phase-Change Materials

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Inspired by the great success of fiber optics in ultrafast data transmission, photonic computing is being extensively studied as an alternative to replace or hybridize electronic computers, which are reaching speed and bandwidth limitations. Mimicking and implementing basic computing elements on photonic devices is a first and essential step toward all-optical computers. Here, an optical pulse-width modulation (PWM) switching of phase-change materials on an integrated waveguide is developed, which allows practical implementation of photonic memories and logic devices. It is established that PWM with low peak power is very effective for recrystallization of phase-change materials, in terms of both energy efficiency and process control. Using this understanding, multilevel photonic memories with complete random accessibility are then implemented. Finally, programmable optical logic devices are demonstrated conceptually and experimentally, with logic “OR” and “NAND” achieved on just a single integrated photonic phase-change cell. This study provides a practical and elegant technique to optically program photonic phase-change devices for computing applications.

either by using different materials, for example, carbon nanotube,^[3] graphene-like 2D materials,^[4,5] spintronic materials,^[6] or novel technologies, such as quantum computing,^[7] in-memory computing,^[8,9] neuromorphic computing,^[10,11] and photonic computing.^[12–14] In high-performance computing industries, on-chip optical interconnects have been purported to replace electronic wires in connecting central processing units and memories to mitigate the von Neumann bottleneck with high speed and low power consumption in data transmission.^[15,16] In general, photonics is one of the best candidates for a future computing system, being capable of performing data storage and processing in an optical manner at high speeds and with unprecedented bandwidth.^[17]

With Moore's law slowing and nearing its end,^[1] modern computing technology based on the von Neumann approach^[2] is reaching its physical limitations. Several studies toward the shift to next-generation computing have been proposed


For photonic computing, photonic memories are considered to be one of the most important yet difficult to realize optical counterparts of essential electronic devices compatible with semiconductor processing. Previous studies on integrated photonic memories using tunable photonic crystals,^[18–20] microring or micro-disk lasers,^[21,22] and semiconductor quantum wells^[23] have the limitation of volatility. Phase-change material (PCM) based photonic memories have recently emerged as a leading candidate to offer true nonvolatility.^[24] PCMs show a difference in both electronic and optical properties between two stable solid phases, the amorphous and crystalline states. They can reversibly cycle between these states under appropriate thermal, electrical, or optical stimulation with high reproducibility and long-term stability.^[25–28] These unique properties have led to other emerging photonic applications of PCMs, such as nonvolatile optoelectronic displays,^[29] reconfigurable optical metamaterials,^[30] and mid-infrared absorbers and thermal emitters.^[31–33] By incorporating such PCMs with photonic circuits, Ríos et al. have achieved up to eight memory levels (3 bits) in a single device, using optical pulses for write, read, and erase.^[24] To switch between levels in that memory implementation, single pulses with varying powers were used for amorphization (low-to-high switching) and a multipulse, multipower scheme for re-crystallization (high-to-low switching). Herein, we demonstrate a pulse-width modulation (PWM) method for optical switching of PCMs can bring efficiency gains in terms of both speed and energy, especially for the recrystallization process. Perhaps more importantly, the use of a PWM write scheme enables direct access to (i.e., the writing of) a particular memory

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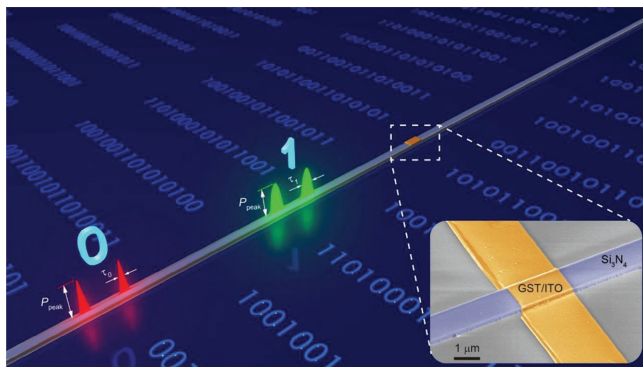


Figure 1. Schematic of optical switching of photonic memories using PWM. Optical pulses with PWM is used to switch photonic phase-change devices with PCMs on waveguides. With fixed peak power (P_{peak}) of optical pulses, the transmission level will be determined by the widths of the pulses (for example, τ_0 and τ_1 in the figure). Inset: Scanning electron microscopy (SEM, false colored) image of a zoomed-in structure of a photonic device, with a GST/ITO unit (gold) on top of a Si_3N_4 waveguide.

level from any starting state (i.e., from any other stored level) using the same PWM pulse sequence (i.e., each memory level has an associated PWM sequence that will always result in that memory level being written, whatever the starting state). Moreover, the use of the PWM excitation scheme naturally lends itself to the realization of simple yet efficient form of nonvolatile integrated photonic logic, which we also demonstrate.

The concept of PWM switching is illustrated in **Figure 1**, where optical pulses at fixed peak power or amplitude (P_{peak}) yet with different widths (τ) are confined in a waveguide to switch, via evanescent coupling, a piece of PCM cell on top of the waveguide (inset of **Figure 1**). Different levels (“0” and “1”) can be accessed by different τ (τ_0 and τ_1). We use the prototypical PCM, $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) for the memory unit, with indium tin oxide (ITO) as the capping layer (see the Experimental Section), which are evanescently coupled on top of a silicon nitride (Si_3N_4) waveguide. A typical device is shown in **Figure S1a** (Supporting Information), along with the diffraction couplers as the input/output for optical measurements. In this Communication, we elucidate the switching mechanism qualitatively, implement the PWM scheme experimentally, and demonstrate its application to the provision of nonvolatile logic (“OR” and “NAND”) integrated photonic devices.

To find a fast, energy-efficient, and practical optical switching method for PCMs, finite-difference time-domain (FDTD) and finite element method (FEM) simulations are combined to qualitatively study the transient temperature profile of GSTs under excitation by optical pulses sent down the waveguide. The detailed dimensions of the photonic memory used for simulations are illustrated in **Figure S2a** (Supporting Information). The electric field amplitude distribution ($|E|$) as well as the unit power absorption (P_{abs}) can be calculated from the FDTD simulation, with noticeable differences between the amorphous GST and crystalline GST cases in the photonic memory (**Figure S2b–e**, Supporting Information). The 3D P_{abs} profile in GST/ITO modulated by a shutter function (mimicking an optical pulse) is subsequently used as the heat source in an FEM heat transfer simulation to obtain the

transient temperature profile in the photonic memory. Starting from the GST cell in the fully crystalline state (cGST) and stimulating by a 50 ns pulse at 5 mW, the peak temperature profile in GST happens at the falling edge of the pulse with the maximum temperature of 983 K occurring at the middle left ($x = -0.42 \mu\text{m}$, $y = 0 \mu\text{m}$) of the GST cell and decaying very quickly toward the edges of the cell (**Figure S2f**, Supporting Information). If the temperature T exceeds the melting point (T_m) of GST, an amorphous GST (aGST) region will form inside the cGST (assuming of course a sufficiently high cooling rate), which leads to an intermediate state of the photonic memory. For simplicity, we assume a binary GST (a/cGST) structure formed in the intermediate state: aGST forms inside a region ($T > T_m$) with cGST outside ($T \leq T_m$). If $T_m = 900 \text{ K}$, the aGST region could here be further estimated as a circular area with the radius of $0.2 \mu\text{m}$ (**Figure S2f** and Supplementary Text S1 of the Supporting Information, and **Figure 2a**).

To study the recrystallization of the photonic memory from the above intermediate state, $|E|$ and P_{abs} were simulated for the case with the GST cell in the mixed amorphous-crystalline state (a/cGST) (**Figure 2b,c**). $|E|$ in the a/cGST case decays from left to right, yet with high localized field in the aGST region (**Figure 2b**). The crystalline part of the a/cGST cell has a much higher P_{abs} than the amorphous region with the maximum values at the left and right boundaries of the amorphous and crystalline regions (**Figure 2c**). For the recrystallization of the a/c GST, P_{abs} modulated by pulses with different parameters is used as the heating source to simulate the temperature distributions. A typical temperature profile of the a/cGST at the falling edge of an applied pulse ($\tau = 10 \text{ ns}$, $P_{\text{peak}} = 1 \text{ mW}$) is shown in **Figure 2d**. The high-temperature region is in the cGST close to the boundary of aGST and cGST regions, and decays gradually toward the aGST and the cell edges. The temperature of the PCM increases with time upon the initiate of the optical pulse with the maximum value close to the falling edge of the pulse, then decreasing slowly ($>35 \text{ ns}$) down to ambient temperature (inset of **Figure 2d**). The temperature analysis is carried out at the GST/ITO interface ($z = 0.01 \mu\text{m}$), which has the highest temperature along the z -direction (**Figure S3**, Supporting Information). In the following simulations, the temperatures of three typical positions (a , c_1 , and c_2 in **Figure 2d**) are particularly compared where position a (x_a , 0) has the lowest temperature in aGST, position c_1 (x_{c1} , 0) has the highest temperature in cGST, and c_2 (x_a , y_{c2}) has the highest temperature along $x = x_a$ (see Supplementary Text S2 in the Supporting Information).

Next, we examined the temperature responses of the a/cGST for pulse amplitude modulation (PAM) and PWM, respectively. In PAM switching, optical pulses have a fixed pulse width (here $\tau = 10 \text{ ns}$) and a varying amplitude, P_{peak} : here 1, 2, 3, and 4 mW (**Figure 2e**). Using PAM switching, the maximum temperature (T_{max}) achieved of the a/cGST along $y = 0$ (the horizontal dashed line in **Figure 2d**) is illustrated in **Figure 2f**, where T_{max} increases with P_{peak} . On the other hand, for PWM switching, at fixed peak power ($P_{\text{peak}} = 1 \text{ mW}$), optical pulses use different pulse widths τ : here 10, 20, 30, and 40 ns (**Figure 2g**). T_{max} rises with increasing τ , but the rise is slower than with the increasing

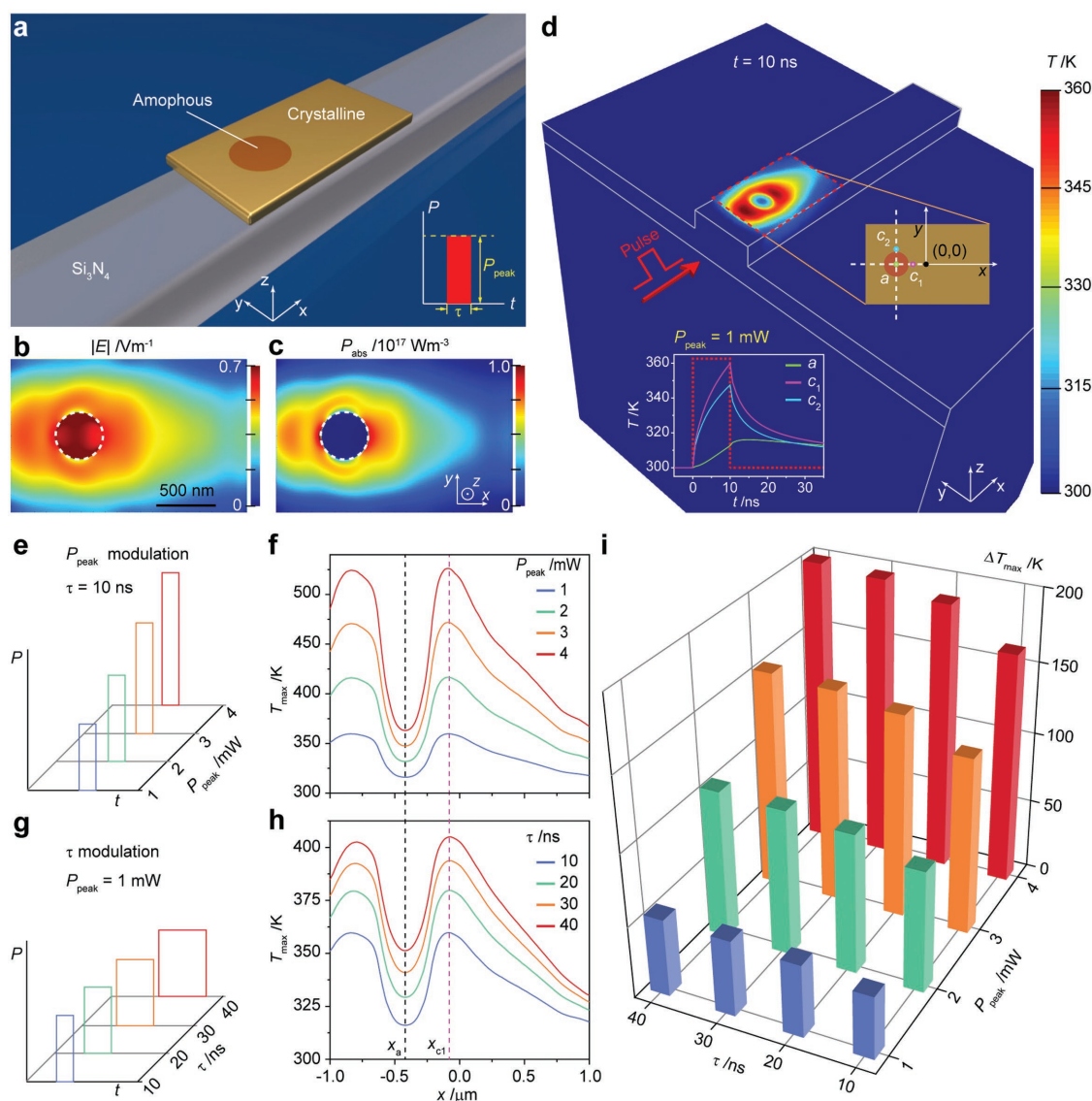


Figure 2. FDTD and FEM simulations of optical switching of photonic memories. a) Schematic of the photonic phase-change memory at an intermediate state consisting of both aGST (brown) and cGST (gold) parts. Inset: The optical pulse implemented to switch the photonic memory device, with the peak power and width as P_{peak} and τ , respectively. b,c) FDTD simulation of the photonic memory showing the amplitude of b) the electric field distribution $|E|$ and c) the unit power absorption P_{abs} in the GST unit (the central plane). The dashed white circle illustrates the boundary of the aGST. d) 3D temperature distribution in the photonic memory with the same structure as in (b) and (c). Power absorption in (c) together with an optical shutter was used as the heating source to mimic a single optical pulse ($P_{\text{peak}} = 1$ mW, $\tau = 10$ ns) incident to the waveguide (the red arrow). The temperature distribution is at the falling edge of the optical pulse ($t = 10$ ns). The red dashed box is the a/cGST unit with a combination of amorphous (brown) and crystalline (gold) GST parts. Inset: The transient temperature profiles at three different positions of the GST/ITO interface, corresponding to the olive (a), pink (c_1), and cyan (c_2) dots in the figure. The dotted red line is the optical pulse shape. e) Schematic of the pulse amplitude modulation (PAM). At the input of the photonic memory, four optical pulses at fixed τ (10 ns) with P_{peak} from 1 mW, 2 mW, 3 mW to 4 mW are used to simulate the transient temperature profile in the a/cGST. f) The maximum temperature (T_{max}) achieved along $y = 0$ (horizontal dashed line in (d)) is analyzed for input pulses in (e). g) Schematic of the pulse-width modulation (PWM). Four optical pulses at fixed P_{peak} (1 mW) with $\tau = 10, 20, 30$, and 40 ns are used to simulate the transient temperature profile in the a/cGST respectively. h) T_{max} along $y = 0$ is analyzed for input pulses in (g). i) The maximum temperature difference ($\Delta T_{\text{max}} = T_{\text{max}}(x_{c1}) - T_{\text{max}}(x_a)$) between the position c_1 (x_{c1}) and a (x_a) in (f) and (h), as a function of P_{peak} and τ .

of P_{peak} in PAM (Figure 2h and Figure S4, Supporting Information). For both cases, $T_{\text{max}}(x_{c1})$ in the cGST region (position c_1) and $T_{\text{max}}(x_a)$ at the center of the aGST (position a) have the highest and lowest T_{max} , with the temperature difference $\Delta T_{\text{max}} = T_{\text{max}}(x_{c1}) - T_{\text{max}}(x_a)$ further calculated, as shown in Figure 2i. ΔT_{max} increases significantly with P_{peak} but

increases less dramatically with increasing τ (Figure S5, Supporting Information). For practical recrystallization processes, small ΔT_{max} is preferable for less re-amorphization of the cGST. With regard to the energy efficiency, an estimate of the ratio between the energy absorption in aGST (E_a) and the input optical pulse energy (E_{pulse}) can be given as

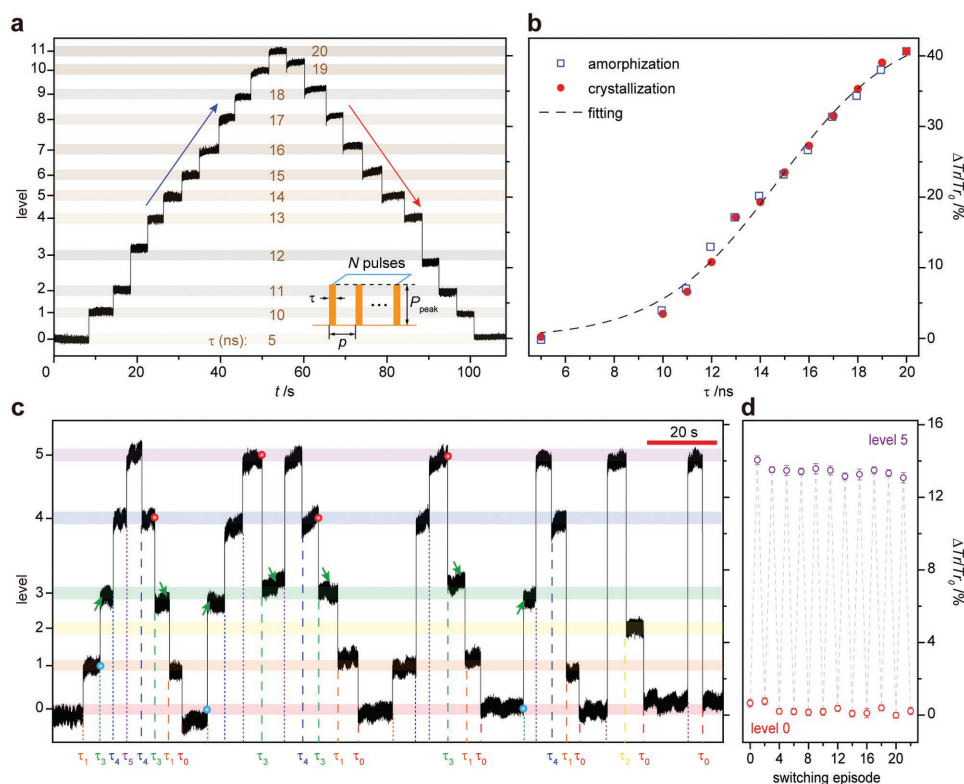


Figure 3. Multilevel photonic memory using multipulse PWM. a) Experimental demonstration of 12 different levels in a single device with the relative change in transmission ($\Delta Tr/Tr_0$) recorded. A multiple-identical-pulse train including ten pulses with $p = 30$ ns and $P_{\text{peak}} = 1.4$ mW is implemented to switch the photonic memory and each level is reached by a determined τ , from 5 to 20 ns. b) $\Delta Tr/Tr_0$ as a function of τ . The blue squares and the red circles are data obtained from the amorphization and crystallization processes, corresponding to the blue and red arrows in (a). The dashed black curve is the fitting of the data with detailed fitting parameters shown in Table S1 (Supporting Information). c) Random access of six different levels of a single photonic memory with $\Delta Tr/Tr_0$ recorded. A multiple-identical-pulse train is used to reach different levels, with $N = 12$, $p = 20$ ns, and $P_{\text{peak}} = 1.6$ mW. Each level can be reached with the same pulse train at a determined width (τ_0 to τ_5) from any previous level, where $\tau_0 = 10$ ns, $\tau_1 = 10.5$ ns, $\tau_2 = 11$ ns, $\tau_3 = 11.5$ ns, $\tau_4 = 12.5$ ns, and $\tau_5 = 15$ ns, respectively. The dotted and dashed lines denote the times when optical pulse trains are applied for amorphization and crystallization, respectively. d) Repeatability of the switching between levels “0” and “5” of the same photonic memory in (c) over multiple cycles. The parameters of the optical pulses for switching are the same as that in (c).

$$\frac{E_a}{E_{\text{pulse}}} = \frac{\int (C_{\text{aGST}} \times \Delta T_a) dV}{P_{\text{peak}} \times \tau} \quad (1)$$

where C_{aGST} is the heat capacity for aGST, ΔT_a is the maximum temperature change (under certain optical pulse) with ambient temperature (T_0) in aGST: $\Delta T_a = T_{\text{max}}(x, y, z \in V_a) - T_0$, and the integration is over the entire amorphous GST volume (V_a). A more detailed calculation of E_a/E_{pulse} is shown in the Supplementary Text S2 (Supporting Information) with the dependence of E_a/E_{pulse} on P_{peak} and τ shown in Figure S5 (Supporting Information). While E_a/E_{pulse} depends little on P_{peak} , the ratio significantly increases with decreasing τ , consistent with our previous study.^[24] Therefore, for good control of the recrystallization process and for low energy consumption, PWM at low P_{peak} together with small τ is desirable for a/cGST switching.

Practically, sufficient energy above a certain threshold is required to switch a phase-change photonic memory,^[24,34] which makes it challenging to implement a PWM scheme using a single pulse having a small P_{peak} and τ , while still allowing access to (i.e., the writing of) multiple memory levels. To address this issue, we developed a multiple-identical-pulse

scheme for PWM (inset of Figure 3a) with the temperature profile in GST during amorphization and recrystallization estimated in Supplementary Text S3 and Figure S6 (Supporting Information). Although the qualitative FDTD/FEM simulations have indicated the direction for optimizing the switching of GST, we used empirical methods to choose the parameters of optical pulses for experimental implementation of photonic memories and logic devices below. A photonic memory with a $4 \mu\text{m} \times 1.3 \mu\text{m}$ GST unit on top of a waveguide was fabricated followed by a thermal annealing process to completely crystallize the GST. A probe-pump technique^[14,24] was used to switch the photonic memory meanwhile monitoring the optical transmission (Tr) or the memory level (Figure S1b, Supporting Information). The optical transmission of the cGST was measured as the baseline (Tr_0) or level “0” (arbitrarily defined number). A ten-pulse train with fixed period (p) of 30 ns and fixed peak power (P_{peak}) of 1.4 mW was sent to the photonic memory. When $\tau = 10$ ns, the ten-pulse train amorphized the cGST to level “1” with increased Tr . By increasing of τ from 11 to 20 ns, higher levels from level “2” up to level “11” were sequentially achieved (again using a sequence of ten pulses in each case). The PWM switching can also work vice versa for the

recrystallization. For example, from level “11,” lower levels can be subsequently obtained with decreased τ (Figure 3a). Importantly, each level accessed from an amorphized state (lower level) and a recrystallization state (higher level) has the same corresponding τ , illustrated in Figure 3b. The dependence of the optical transmission change ($\Delta Tr/Tr_0$) on τ can be well fitted by a logistic function (Figure 3b), with a threshold regime ($\tau = 0\text{--}10$ ns), a linear regime ($\tau = 10\text{--}18$ ns), and a saturation regime ($\tau > 18$ ns). The threshold regime is attributed to the property of GST, which requires a threshold temperature for switching.

Furthermore, we demonstrated a random accessing of memory levels with PWM, shown in Figure 3c. A 12-pulse train ($p = 30$ ns, $P_{\text{peak}} = 1.6$ mW) with various τ (τ_0 to τ_5 : 10, 10.5, 11, 11.5, 12.5, and 15 ns) was applied to a photonic memory to achieve six distinguishable levels (levels “0” to “5”). Each level can be accessed by a specific τ , from any previous level. For example, we can switch the photonic memory to level “3” (green arrows) by τ_3 , from lower levels “0” and “1” (blue disks) by amorphization, as well as from higher levels “4” and “5” (red disks) by recrystallization. Furthermore, the back and forth switching between levels “0” and “5” with a transmission change of $\approx 15\%$ using determined pulse widths τ_0 and τ_5 has been repeated up to 22 cycles (Figure 3d), though of course many more cycles are possible, bearing in mind the high endurance of phase-change memories (e.g., up to 10^{12} cycles^[27]), which demonstrates the high durability of the random access using PWM.

To address the dramatic increase in logic devices required in high-performance computing, PCM-based electrical logic devices with multiple operations have been developed.^[35–38] Implementation of logic devices in an optical manner could benefit the field of all-optical signal processing and computing.^[39] Using this simple yet powerful PWM switching of photonic memories with random accessibility, we now demonstrate logic device applications using photonic memories with PWM switching. A double-pulse train at fixed time separation ($p = 30$ ns) and peak power ($P_{\text{peak}} = 1.14$ mW) was used to program digital inputs 0, 1, and reset, corresponding to pulse widths of τ_0 (15.5 ns), τ_1 (20 ns), and τ_r (10 ns), respectively, as shown in Figure 4a. Two input signals In_1 and In_2 with different combinations of digits 0 and 1, followed by a reset signal, were applied to a photonic memory as the transmission Tr was recorded. Starting from the cGST state (Tr_0 , level “0”), digits 0 and 1 switch the photonic memory to high levels with $\approx 10\%$ (level “1”) and $\approx 15\%$ (level “2”) relative changes in transmission ($\Delta Tr/Tr_0$) (Figure 4b), subsequently the reset signal switches it back to level “0” (cGST state). With different digit combinations of In_1 and In_2 , we can obtain distinct $\Delta Tr/Tr_0$ values and shapes (Figure 4b). By comparing the peak amplitude of $\Delta Tr/Tr_0$ with a reference value (ref), the digital output (X) of the photonic memory can be either 0 or 1 (Figure 4c).

When the photonic memory was reset to level “0” after the digital inputs (Figure 4b), the relative transmission change can be simplified as Figure 4d. Assuming there is a clock signal working at a similar time scale, the dashed windows in Figure 4d–f are synchronized with this clock signal. To determine the logic output by comparing $\Delta Tr/Tr_0$ with ref , the whole trace shape of $\Delta Tr/Tr_0$ in that dashed window is compared with ref . The comparator in Figure 4c could be an edge-triggered device (ref value is the trigger point). If ref was defined between $\approx 10\%$ and $\approx 15\%$, the

photonic memory works as an “OR” function with the truth table shown in Figure 4g. Next, the photonic memory can also be reset to any other levels, for example, the levels “1” and “2,” shown in Figure 4e,h and Figure f,i, respectively. If we reset the photonic memory to level “2” by digit 1 ($\tau_r = \tau_1$) with the baseline moved and $\Delta Tr/Tr_0$ values changed accordingly, shown in Figure 4f. By defining the ref ($-5\% < ref < 0$), the photonic memory will be a “NAND” logic device (Figure 4i). This is a crucial development as “NAND” has the property of functional completeness to implement any other logic functions using only “NAND” devices.^[40]

Using FDTD optical simulations and FEM heat analysis, we studied the transient temperature response in the recrystallization process of photonic memories via PAM and PWM switching methods, respectively. These demonstrate that when compared to PAM switching, PWM switching is more efficient in heating the amorphous region of the photonic memory, and more practical in controlling the recrystallization process. To further understand the mechanism of multilevel switching of GST, dynamic switching models, such as phase-change cellular automata model^[41] and nucleation and growth model,^[42] should be included in optical/thermal simulations, with accurate simulation parameters obtained by materials characterization (see detailed discussion in Supplementary Text S4, Supporting Information). Inspired by the simulation results, an improved PWM switching using multi-identical-pulse scheme was experimentally demonstrated for nonvolatile, multilevel, and energy-efficient switching of photonic memories with true random programming capability, which is crucial for practical memory applications. A recent study has demonstrated long-term drift-free properties of photonic phase-change devices,^[9] which could further benefit reliable multilevel data storage. As a proof of concept, we also demonstrated programmable optical logic devices based on a single photonic memory cell using PWM. By resetting the photonic memory at different levels, logic “OR” and “NAND” have been achieved on the same device with functional completeness. Based on CMOS design rules, the layout of electronic “OR” and “NAND” gates can be estimated to be $300\text{ nm} \times 600\text{ nm}$ and $100\text{ nm} \times 200\text{ nm}$, respectively,^[43] at recent lithography process node (10 nm). Compared to this, our photonic logic device has an area of $2.6\text{ }\mu\text{m}^2$ ($2\text{ }\mu\text{m} \times 1.3\text{ }\mu\text{m}$ GST) at the moment but with complex functionalities. By decreasing and optimizing the device structure, e.g., using smaller footprint silicon waveguides or plasmonic waveguides,^[44] optical ring resonators with picosecond laser switching,^[45] and embedding phase-change materials within the waveguide to reach higher modulation contrast,^[46] such programmable functionalities could make our photonic devices very promising candidates for future photonic computing applications. PWM switching of photonic memories enables a practical and energy-efficient way to program the photonic memory for reconfigurable photonic devices applications that could result in all-optical computing using phase-change materials in future.

Experimental Section

Photonic Memory Device Fabrication: Photonic memories were fabricated on a Si_3N_4 wafer with 335 nm $\text{Si}_3\text{N}_4/3,350\text{ nm SiO}_2$ film on Si wafer as reported elsewhere.^[12,14,24] Electron-beam lithography

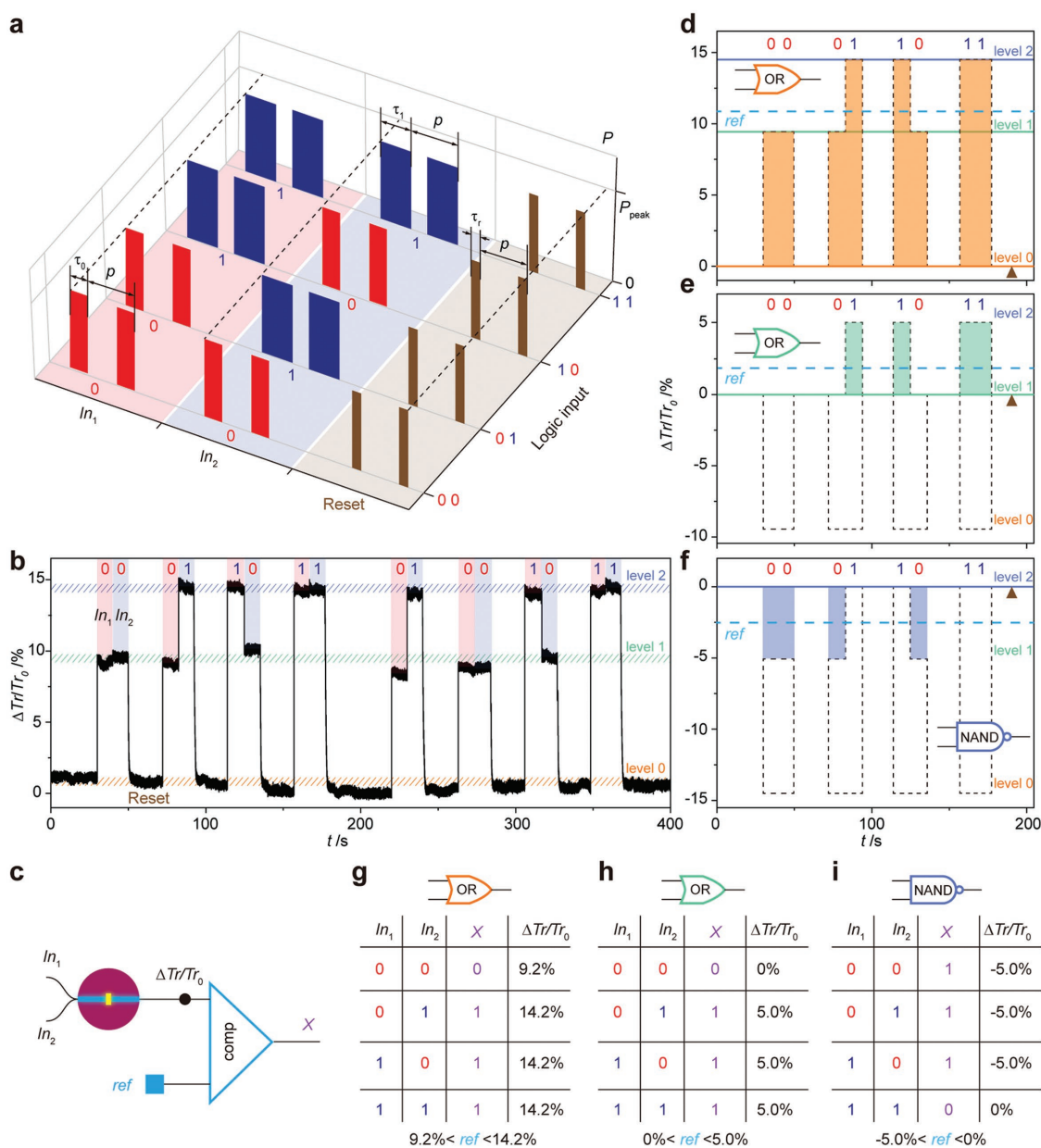


Figure 4. Programmable optical logic devices based on a single photonic memory using PWM. a) Optical pulse trains including two pulses with fixed period p (30 ns) and peak power P_{peak} (1.14 mW) are encoded as **reset** (brown), digit **0** (red), and digit **1** (dark blue) corresponding to pulse widths τ_r (10 ns), τ_0 (15.5 ns), and τ_1 (20 ns), respectively. Two input signals encoded either as digit **0** or **1** (four combinations: 00, 01, 10, and 11) with sufficient time separation to interact with a photonic memory to achieve various levels, followed by a **reset** signal to initialize the device. b) Transmission change of the photonic memory with different input digital encoded signals, as illustrated in (a). Three distinct levels “0” (orange), “1” (green), and “2” (blue) were accessed by **reset**, digit **0**, and digit **1**, respectively. c) Schematic of an optical logic device based on the photonic memory with two signal inputs In_1 and In_2 . A comparator (comp) is used to determine the output (X) by comparing $\Delta Tr/Tr_0$ with a reference value ref . d) Simplified recording trace of $\Delta Tr/Tr_0$ in (b) with the baseline Tr_0 (the brown triangle) defined at level “0” (the orange line) by using the **reset** signal to initialize the photonic memory. The green and blue lines illustrate levels “1” and “2.” The photonic memory acts as the logic gate “OR” with the ref value shown as the dashed cyan line, between levels “1” and “2.” e, f) Schematics show the traces $\Delta Tr/Tr_0$ of the same photonic memory in (b) and (d) with the baselines set at e) levels “1” and f) “2” by using digits **0** and **1** as the initialization signals, respectively. The photonic memory can work as logic gates “OR” (e) and “NAND” (f) with the ref values illustrated in the figures. The dashed black lines denote the contour of the experimental $\Delta Tr/Tr_0$ recordings in (b) and (d). g–i) The truth tables and the $\Delta Tr/Tr_0$ corresponding to the logic devices demonstrated in (d)–(f).

(JEOL 5500FS) was used to pattern the photonic waveguide structure on the wafer spin coated with an ≈ 300 nm MaN-2403 negative resist, subsequently treated by reactive ion etching (PlasmaPro 80, Oxford Instruments) to etch down 165 nm of Si_3N_4 . A second layer of lithography on a positive resist poly(methyl methacrylate) was utilized to

determine the GST pattern followed by a sputtering deposition (Nordiko) of 10 nm GST/10 nm ITO. The structures of photonic memories were characterized by optical microscopy (Nikon Eclipse LV100ND) as well as scanning electron microscopy (Hitachi S-4300) with accelerating voltages ≈ 1 –3 kV, working distances ≈ 15 mm, and tilted angle 0° or 50° .

FDTD and FEM Simulations: The FDTD optical simulations were calculated by Lumerical FDTD Solutions. With fundamental transverse electric (TE) mode source injected into a waveguide with a GST/ITO unit on top, 3D FDTD simulation calculated the electric field distribution $|E|$ with normalized mode source as well as the unit power absorption P_{abs} with 1 mW mode source power. Next, P_{abs} in the GST/ITO region was imported as the heat source and modulated by a global shutter (to mimic a single optical pulse) in 3D FEM heat simulations (Lumerical DEVICE HT) with time-dependent temperature distribution resolved. By adjusting peak powers or pulse widths, transient temperature profiles in photonic memories can be simulated for PAM and PWM, respectively.

Optical Measurements: The optical measurements were implemented by a probe/pump technique that has been described previously^[12,14,24] and in the Supplementary Materials and Methods section in the Supporting. The measurement schematic was illustrated in Figure S1b (Supporting Information). To switch a photonic memory while in situ monitoring its optical transmission, pump and probe signals, working at different wavelengths, were guided into the photonic memory from opposite directions. The probe signal is a continuous-wave (CW) diode laser (TSL-550, Santec) working at lower power that was used to interrogate the photonic memory with optical transmission recorded by a photodetector (2011-FC-M, Newport). To obtain the high-power pump signal, another CW diode laser (N7711A, Keysight) modulated by an electro-optic modulator (EOM, 2623NA, Lucent) was connected by an electrical pulse generator (8131A, 500 MHz, Hewlett Packard) and was subsequently amplified by a low-noise erbium-doped fiber amplifier (AEDFA-CL-23, Amonics). Optical circulators were utilized to guide the probe (pump) laser into the photonic memory while extracting the pump (probe) laser out from it, with optical bandpass filters (OTF-320, Santec) incorporated in the probe/pump route to suppress any interference between the probe and pump signals.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Z.C., C.R., and N.Y. fabricated the samples and performed the optical measurements and simulations. W.H.P.P., C.D.W., and H.B. led the project. All the authors discussed the results and wrote the manuscript. The authors acknowledge discussions with Emanuele Gemo on the FDTD and FEM simulations. This research was supported via the Engineering and Physical Sciences Research Council Manufacturing Fellowships (EP/J018694/1), the Wearable and Flexible Technologies (WAFT) collaboration (EP/M015173/1), the Chalcogenide Advanced Manufacturing Partnership (EP/M015130/1), and the European Union's Horizon 2020 research and innovation program (780848, Fun-COMP project).

All data need to evaluate the conclusions in this Communication are present in this Communication and/or the Supporting Information. Additional data related to this Communication may be requested from the corresponding author (H.B.; harish.bhaskaran@materials.ox.ac.uk or Oxford Research Archive for Data (<https://ora.ox.ac.uk>)).

Keywords

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