Supplemental Material

for the paper

How Contact Layers Control Shunting Losses from Pinholes in Thin-Film Solar Cells

Pascal Kaienburg[1]*, Paula Hartnagel[1,2], Bart E. Pieters[1], Jiaoxian Yu[1,3], David Grabowski[1], Zhifa Liu[1,4], Jinane Haddad[1], Uwe Rau[1] and Thomas Kirchartz[1,2]*

[1]IEK5-Photovoltaics, Forschungszentrum Jülich, 52425 Jülich, Germany

[2]Faculty of Engineering and CENIDE, University of Duisburg-Essen, Carl-Benz-Str. 199, 47057 Duisburg, Germany

[3]Shandong Provincial Key Laboratory of Processing and Testing Technology of Glass & Functional Ceramics, School of Materials Science and Engineering, Qilu University of Technology (Shandong Academy of Sciences), 250353 Jinan, P. R. China

[4]State Key Laboratory of Structural Chemistry, Fujian Institute of Research on the Structure of Matter, Chinese Academy of Sciences Fuzhou, 350002 Fujian, P. R. China

Pascal Kaienburg* – paskai@posteo.de

Thomas Kirchartz* – t.kirchartz@fz-juelich.de

* Corresponding author

1. Experimental Details

Chemicals: PEDOT:PSS (PEDOT) was purchased from Ossila, PCBM was purchased from Solenne, ZnO nanoparticles (ZnO:NP) were purchased from Avantama, KP115 was purchased from 1-material and 18 NR-T paste for mp-TiO_2 was purchased from Dyesol. All other chemicals were purchased from Sigma Aldrich. Dried solvents with analytical (p.a.) quality were used.

ETL/HTL diodes: c-TiO_2/P3HT: full stack of FTO/c-TiO_2/P3HT/MoO_x/Ag. FTO TEC7 substrates by Pilkington were used and structured by Kintec. The cleaned FTO layers were ozone-treated prior to use. The compact TiO_2 layer was prepared via spray-coating a 0.2 M solution of titanium diisopropoxide bis(acetylacetonate) 75 wt% in ethanol on a hot plate at roughly 470 °C. After cooling down to about 200 °C, samples were transferred to a N_2-filled glovebox. P3HT was dissolved in chlorobenzene (CB) with a concentration of 15 mg/ml and stirred overnight at 65 °C. The cooled solution was spin-coated at 6000 rpm for 120 s with an acceleration time of 3 s. The samples were then annealed at 130 °C for 15 min. Finally, 30 nm of MoO_x and 200 nm of Ag were evaporated thermally.

c-TiO_2/KP115: full stack of FTO/c-TiO_2/KP115/MoO_x/Ag. For the FTO, c-TiO_2, MoOx and Ag layers see the c-TiO_2/P3HT ETL/HTL diode. KP115 was dissolved in 1,2-dichlorobenzene (DCB) with a concentration of 10 mg/ml and stirred overnight at 110 °C. The hot solution was spin-coated at for 120 s with an acceleration time of 3 s. Then the samples were dried in a closed petri dish for 3 h.

PEDOT/PCBM: full stack of ITO/PEDOT:PSS/PCBM/ZnO/Al. Corning glass substrates with sputtered ITO layers (15 Ω/□) were purchased from Kintec Company, Hongkong, and plasma-cleaned before use for 12 minutes. Five drops of PEDOT:PSS solution were dispensed onto the ITO from a syringe with 0.45 μm nylon filter, followed by spin-coating in air at 2000 rpm for 60 s. The samples were then transferred to a glovebox where they were annealed at 110 °C for 10 min. The samples were left to cool down on the side. A 20mg/ml solution of PCBM in chlorobenzene was prepared a day before and left stirring overnight. After the samples were cooled down the PCBM solution was filtered and spin-coated onto the PEDOT layer at 1000 rpm for 60 s. A dispersion of ZnO:NP in IPA (2,5 wt%) was used to prepare another solution of ZnO:IPA with 5:2 volume ratio, that was put in an ultrasonic bath for 1 h before use. It was then filtered with 0.2 μm PTFE filter and spin coated on top of the PCBM at 3000 rpm for 60 s. Finally, 100 nm of Al were evaporated thermally.

c-TiO_2/spiro: full stack of FTO/c-TiO_2/Spiro:MeOTAD/Au. For the FTO and c-TiO_2 layers see the c-TiO_2/P3HT ETL/HTL diode. Spiro:MeOTAD was dissolved in chlorobenzene (CB) at a ratio of 72.6 mg/ml. Subsequently 17.5 µl of Li-TFSI solution (520 mg/ml in acetonitrile) and 28.8 µl of 4-tert-butylpyridine (TBP) are added. The solution is stirred at 100 °C for 3 minutes and left to cool for at least 30 min before spin-coating the layer at 3000 rpm for 60 s. The finished layer was kept in a dehydrated climate chamber in a dry atmosphere of artificial air overnight and subsequently 100 nm of gold were evaporated as the back contact.

mp-TiO_2/spiro: full stack of FTO/c-TiO_2/ mp-TiO_2/spiro/Au. For the FTO, c-TiO_2, spiro and Au layers see the c-TiO_2/spiro ETL/HTL diode. For the mp-TiO_2, TiO_2 paste was mixed with dry ethanol with a weight ratio of 1:4. The suspension was stirred overnight after ultrasonication for 1 h. Then Li-TFSI (520 mg in 1 ml acetonitrile) solution was added to the TiO_2 suspension with a volume ratio of 1:10. After stirring for 10 min, 180 µl of the mixed solution was spin-coated at 5000 rpm for 45 s and the sample was annealed at about 500 °C for 30 min.

Solar cells Sb_2S_3: full stack of FTO/c-TiO_2/Sb_2S_3/HTM/MoO_x/Ag. Following the "Sb-TU" process described in ref.[1]. For the FTO, c-TiO_2, MoO_x and Ag see the c-TiO_2/P3HT ETL/HTL diode. As hole transport material (HTM) P3HT or KP115 were used. The processing is described in the context of the corresponding ETL/HTL diodes. For the Sb_2S_3 absorber layer 1 mmol of $SbCl_3$ was dissolved in 1 ml of N,N-dimethylformamide (DMF) and stirred for 30 minutes. The solution was then added to thiourea (TU) with an $SbCl_3$:TU molar ratio of 1:1.8, stirred again overnight and filtered before use. The solution was spin-coated at 70 rps for 40 s with 10 s of acceleration. The samples were annealed for 60 minutes at 100 °C on a hot plate which was then heated up to 180 °C where the samples remained for another 10 min followed by crystallization at 265 °C on another hot plate for 30 min.

Perovskite: full stack of FTO/c-TiO_2/mp-TiO_2/perovskite/spiro/Au. For the FTO, c-TiO_2, mp-TiO_2, spiro and Au layers see the mp-TiO_2/spiro process. For the perovskite absorber layer, 1 mmol FAI, 1 mmol PbI_2, 0.2 mmol MABr, 0.2 mmol $PbBr_2$ and 0.06 mmol CsI were dissolved in a mixed solution of 800 µl DMF and 200 µl DMSO and stirred for 10 min at 68°C to get a clear yellow solution. 140 µl of the filtered perovskite solution were spin-coated on the substrate using three steps, first at 1500 rps for 10 s with 3 s of acceleration, then at 4000 rps for 25 s with 4 s of acceleration, finally at 5000 rps for 25 s with 3 s of acceleration. 100 µl of toluene were dropped on the sample during the third step. Then the sample was annealed at 100 °C for 60 min.

Characterization The dark *J-V* characteristics of the ETL/HTL diodes were obtained in inert atmosphere and –if applicable - after UV exposure in order to activate the TiO_2. Illuminated *J-V* characteristics of the full solar cells were measured under illumination from a white LED whose output power was calibrated via solar simulator measurements of the J_{sc}.

SEM: The scanning electron microscope was a *Zeiss (Leo) Gemini 1550* with Shottky field-emission cathode and an in-lens detector. The lateral resolution equals approximately 1 nm at 20 kV and the measurement was performed under a vacuum base pressure of 10^{-6} mbar. The FTO/c-TiO_2/Sb_2S_3 in fig. 1(a) was produced according to the procedure of solar cell fabrication. The perovskite in fig. 1(b) was produced on PEDOT:PSS-coated and previously cleaned Corning glass which was plasma-cleaned before use for 12 minutes. Five drops of PEDOT:PSS solution were dispensed onto the ITO from a syringe with 0.45 μm nylon filter, followed by spin-coating in air at 4000 rpm for 30 s with 1 s acceleration. The samples were then transferred to a glovebox where they were annealed at 110 °C for 20 min. The perovskite precursor solution was prepared by mixing $Pb(CH3COO)_2$ (0.8 M), PbCl2 (0.2 M) and MAI (3.0 M) in a mixed solvent of DMF/DMSO (30/1, v/v). The prepared solution was stirred at room temperature for 30 min before use. The perovskite solution was spin-coated on the PEDOT:PSS-coated substrates at 2000 rpm for 60 s with a ramping rate of 400 rpm/s. The films were then heated at 80 °C for 6 min.

2. Photovoltaic module simulator (PVMOS)

As mentioned in the main script, PVMOS[2] is a device simulator that applies the network simulation method to solar cells and modules. The network consists of resistors and diodes that are interconnected laterally via resistors as shown in fig. S1. The electrical properties in vertical direction along the stack can be parametrized via equivalent circuit elements or by simply providing tabular data. Different domains can be defined across the simulated device whereby lateral inhomogeneity can be accounted for which we use to verify the simpler equivalent circuit model as described in section S5. The two-dimensional approach also enables the modelling of the distributed series resistance arising from the TCO which is needed to remove the TCO resistance from the ETL/HTL diode characteristic as described in section S2. PVMOS is open source and available online free-of-charge[3].

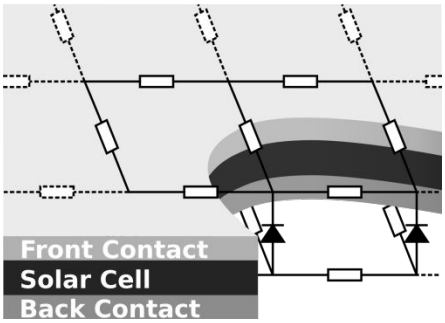

Figure S1: Exemplary 2D diode network simulated with PVMOS[2].

3. Removing series resistance from ETL/HTL diodes (Method)

As described in the main part of this paper, we measured dark current-voltage (J_{exp}-V_{exp}) data for the stacks without absorber – termed ETL/HTL diode – of square-shaped cells with an area of 16mm^2. The obtained *J-V* data includes the series resistance from the electrodes. In order to obtain the characteristic of a pinhole (J_{pin}-V_{pin}) we need to correct for this series resistance. For this purpose the experimental data is fitted with Photo-Voltaic Module Simulator (PVMOS). With PVMOS we simulate, for a given J_{pin}-V_{pin} characteristic of a pinhole, a second J_{out}-V_{out} characteristic including the series resistance from the electrodes. Using non-linear optimization the resulting J_{out}-V_{out} including series resistance is subsequently fitted to the experimental data J_{exp}-V_{exp}, by varying the *J-V* characteristic of the pinhole. In this way we can extract a J_{pin}-V_{pin} characteristic of the pinhole which is unaffected by the electrode series resistance.

For the non-linear optimization of the pinhole *J-V* characteristic (J_{pin}-V_{pin}) we need a convenient parametrization. Here we opt for a purely descriptive model rather than a physical

model to avoid imposing physical assumptions about the pinhole *J-V* characteristic. A fairly compact description may be obtained using several cubic Bézier curves. Since only high shunt currents have an impact on solar cell performance, the fitting of the dark *J-V* curves was done in a linear representation. The curve is divided into three sections as shown in fig. S2(a): One section from 0 V to 0.5 V with handles at 0.15 V and 0.35 V, one from 0.5 V to 0.9 V with handles at 0.6 V and 0.8 V and one section from 0.9 V to 1.3 V with handles at 1.0 V and 1.2 V. At the handles and section borders, the experimental data are used as start parameters. The voltages at the section borders are fixed whereas all current densities and the handles' voltages are varied. This adds up to 16 free parameters of the model that parameterizes the pinhole's *J-V* characteristic (J_{pin}-V_{pin}).

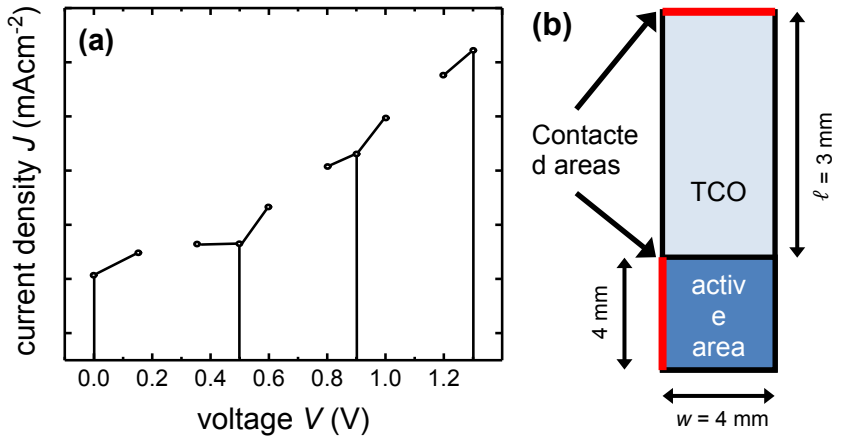

Figure S2: (a) Illustration of the parametrization of a cubic Bézier curve with section borders (open symbols with anchor lines) and handles (solid symbol). (b) Contact configuration of experimental devices, that is also used by PVMOS to correct for the TCO's series resistance.

The ETL/HTL diode is modeled in PVMOS by defining the device geometry according to the experimental cell layout shown in fig. S2(b). The electrodes are contacted along the left and the bottom side of the cell. The sheet resistance of the well-conducting metal electrode was set to 1 mΩ/□ and the sheet resistance of the TCO electrode was defined according to the measured value of the applied material (e.g. 11.8 Ω/□ for ITO and 9.6 Ω/□ for FTO substrate). The pinhole J_{pin}-V_{pin} characteristic defines the layer between the electrodes. The simulated *J-V* output from PVMOS is then compared to the original experimental data and the free parameters are varied so that the linear relative error

$$E = \frac{1}{n}\sqrt{\sum\left(\frac{J_{exp} - J_{out}}{J_{exp}}\right)^2}$$

is minimized. Here, J_{exp} is the experimental current density of the stack without absorber, J_{out} is the output from PVMOS for the ETL/HTL diode including series resistance and n is the number of measured data points. The Bézier curve that minimizes the error is taken as the final J_{pin}-V_{pin} characteristic of the pinhole without the electrodes' series resistance.

In the case of c-TiO_2/spiro and mp-TiO_2/spiro, the experimentally obtained small currents at voltages below 0.5 V are too noisy to be fitted adequately. Therefore, it was fitted in the range of 0.5 V-1.3 V with sections from 0.5 V to 0.7 V with handles at 0.55 V and 0.65 V, from 0.7 V to 0.9 V with handles at 0.75 V and 0.85 V and from 0.9 V to 1.3 V with handles at 1.0 V and 1.2 V. For voltages below 0.5 V, we used the original experimental data. This step is uncritical, since the impact of the series resistance is negligible at low voltages and the shunt currents are of minor relevance at these voltages since they are too low to affect the solar cell performance.

4. Removing series resistance from ETL/HTL diodes (result)

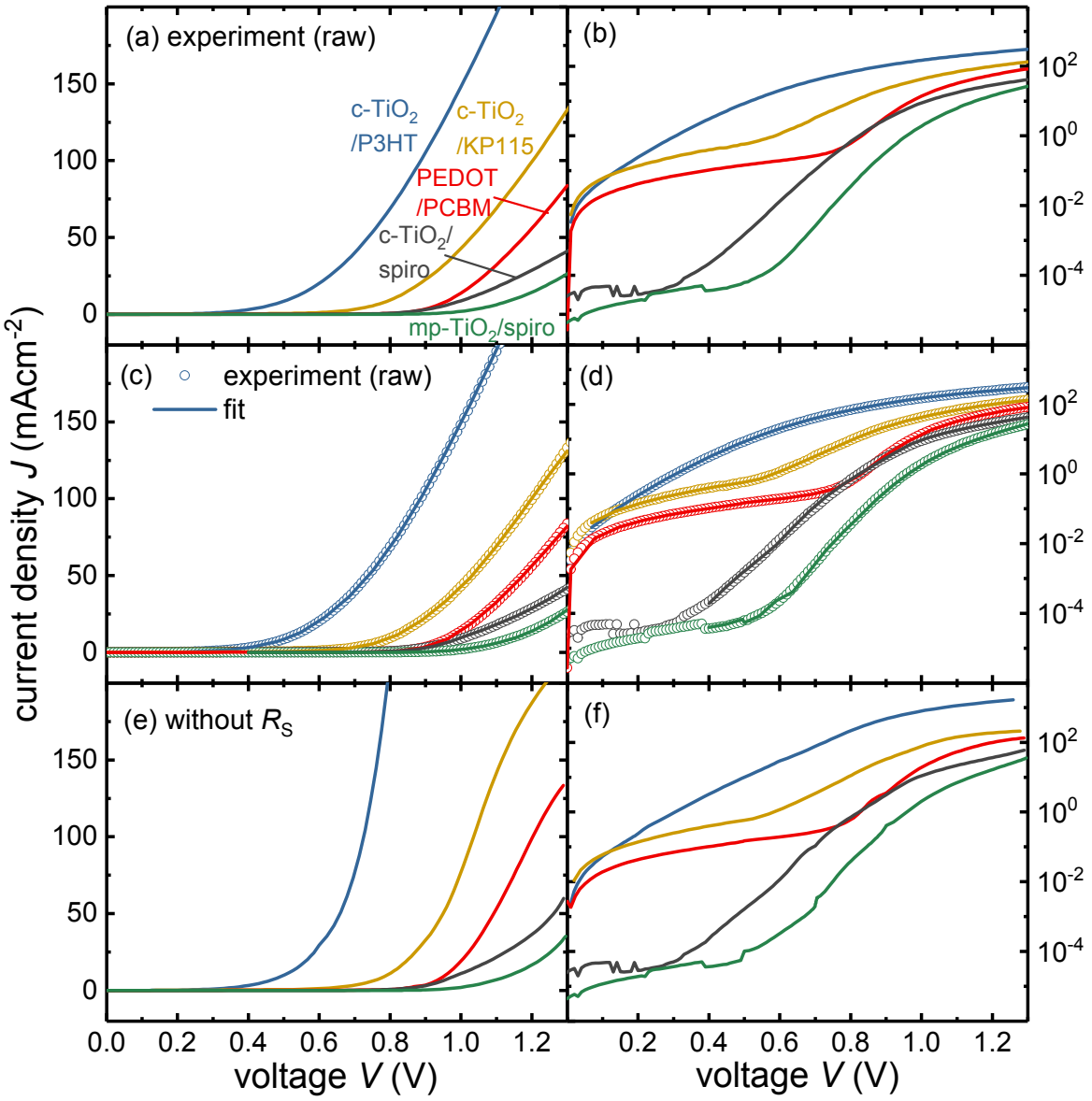

Figure S3: Current-voltage data of the investigated ETL/HTL diodes on a linear (a,c,e) and logarithmic (b,d,f) scale. Experimental data as-measured (a,b). Experimental data as-measured (circles) with curves fitted with PVMOS (c,d) to remove the TCO resistance which was done on a linear scale. Resulting pinhole characteristics (e,f) that were also shown in fig. 3 of the main paper.

5. Effective series resistance of TCO

As a last step in the simulation of the pinholes' impact on solar cell performance the series resistance of the TCO is taken into account. As we show here, this series resistance can be approximated by an effective ohmic resistor R_{TCO}. The value of R_{TCO} is given by the geometry of the electrode and the TCO's sheet resistance $R_{\square}$ and can be estimated from these quantities via $R_{TCO} = R_{\square} \cdot \ell/w$. Here, w is the width of the TCO and ℓ is the effective length of the TCO that can be approximately taken as the distance from the middle of the active area to the point where the cell is contacted as indicated in fig. S2(b). For our cell geometry shown in fig. S1(b) this estimation yields R_{TCO} = 14.8 Ω for the case of ITO (measured $R_{\square}$ = 11.8 Ω/□) and R_{TCO} = 12.0 Ω for the case of FTO TEC7 (measured $R_{\square}$ = 9.6 Ω/□). In many cases, the effective series resistance introduced by TCO is known in groups that produce and optimize solar cells since it is an important loss mechanism for the *FF* of any solar cell.

For a more precise treatment, the TCO's distributed series resistance can be simulated in PVMOS by specifying the electrodes as described in the previous section of the supplement and by assigning the layer in-between the *J-V* characteristic of the solar cell with pinholes (e.g. the output from the parallel circuit or the mini-cell discussed in the paper's main part). However, this approach with PVOS requires significantly more computation time that can be reduced at the costs of voltage resolution. However, the value of an effective ohmic series resistance as shown in fig. 2(b) could be obtained by fitting the results from PVMOS. The fit should be performed only up to V_{oc} and for each ETL/HTL combination and pinhole area. From this, we extracted a fixed series resistance (the fit results show some fluctuations) of R_{TCO} = 17 Ω for the case of ITO and R_{TCO} = 14 Ω for the case of FTO TEC7. These values were used for the calculations in the main part of the paper and are close to the ones obtained from the simple estimation described before. Figure S4 compares the results from the PVMOS simulations with the effective series resistance model. To estimate the sensitivity of the results towards the value of the effective series resistance, the results for R_{TCO} = 10 Ω and R_{TCO} = 20 Ω are also shown. While *FF* and V_{oc} show slight deviations, the efficiency coincides quite well, meaning that the maximum power point is robust against some variration of the effective series resistance of the TCO. Overall, it can be seen that an ohmic resistor is a valid approximation which significantly simplifies the calculations of our model once the pinhole *J-V* characteristic has been obtained from experimental data.

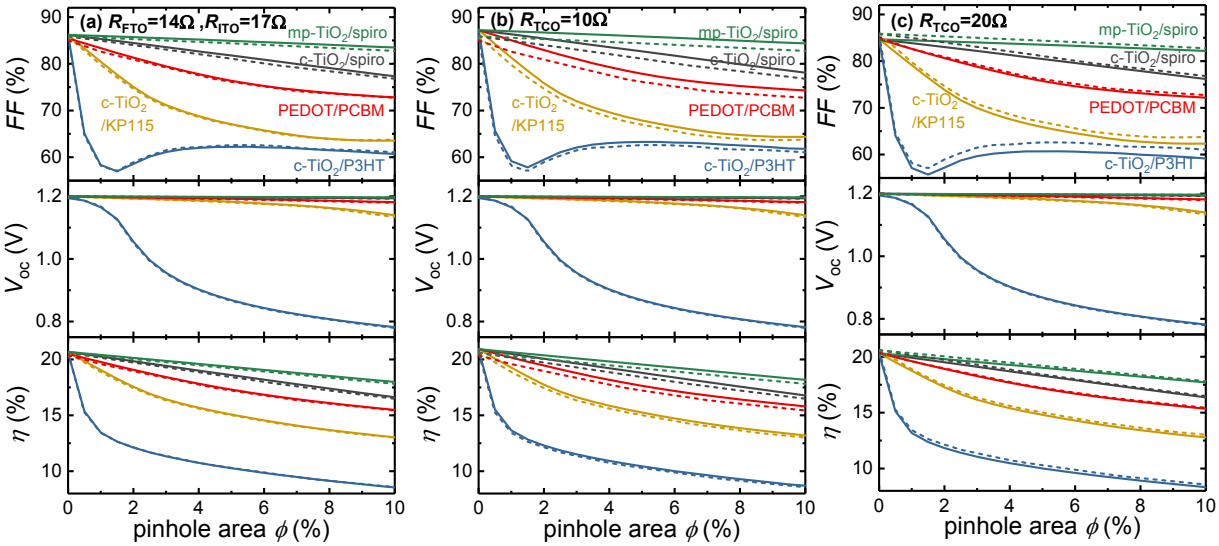

Figure S4: (a-c) Comparison of different values of an effective ohmic series resistance for the TCO with the results from PVMOS simulations.

Note that this approach of an effective ohmic resistor is only feasible because only the *J-V* characteristic for voltages up to V_{oc} is of interest. At higher voltages and currents the distributed series resistance of the TCO will result in a non-ohmic effective series resistance that depends on voltage (or current)[4,5]. In particular, the TCO resistance of the ETL/HTL diode cannot be approximated by an ohmic resistor since much higher current densities are relevant at the pinholes.

6. Validation of parallel circuit model

To verify the results obtained from the simple equivalent circuit model we again make use of 2D simulations with PVMOS. We therefore model a mini-cell illustrated in fig. S5 with 12 µm radius that contains randomly distributed pinholes with a radius of 100 nm. The small size of the cell is necessary to keep computation times acceptable. The same ideal diode characteristics and photocurrent-density from the parallel circuit model is assigned to the pristine area of the mini-cell. Every single pinhole got assigned the resistance-corrected experimental *J-V* characteristic of the respective ETL/HTL diode. The number of pinholes $n_{\mathrm{pin}} = \phi / A_{\mathrm{pin}}$ is given by their size A_{pin} and the cumulative pinhole area ϕ that shall be simulated. For this micrometre-sized cut-out of the original cell the series resistance of the electrodes is negligible and can thus be taken as reference for the parallel equivalent circuit model before accounting for the TCO's series resistance.

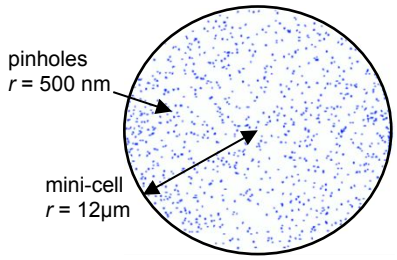

Figure S5: Illustration (top view) of the mini-cell with randomly distributed pinholes that is used to verify the results of the parallel circuit model. This cut-out of a large solar cell allows simulating an inhomogeneous cell with nm-sized pinholes.

Due to numerical issues related to the meshing, the *FF* and thereby the efficiency are overestimated for the mini-cell. The problem is also evident in the absence of pinholes at $\phi = 0$ so that any meaningful physical effect related to pinholes can be excluded. The effect is corrected by normalizing the values of the mini-cell to the values of the parallel circuit at $\phi = 0$ where the system is a homogeneous ideal diode. Figure S6(a) compares the results of the mini-cell and the parallel circuit model which are in good agreement. The deviations are further quantified in fig. S6(b) by defining the error for some key characteristic *X* as

$$\sigma_{\mathrm{x}} = \left({}^{X_{\mathrm{mini\text{-}cell}}} \big/ _{X_{\mathrm{par\text{-}circ}}} - 1 \right) \times 100\% \quad .$$

The relative error is never large than 2% and mostly manifests in the *FF* and thereby in the efficiency η.

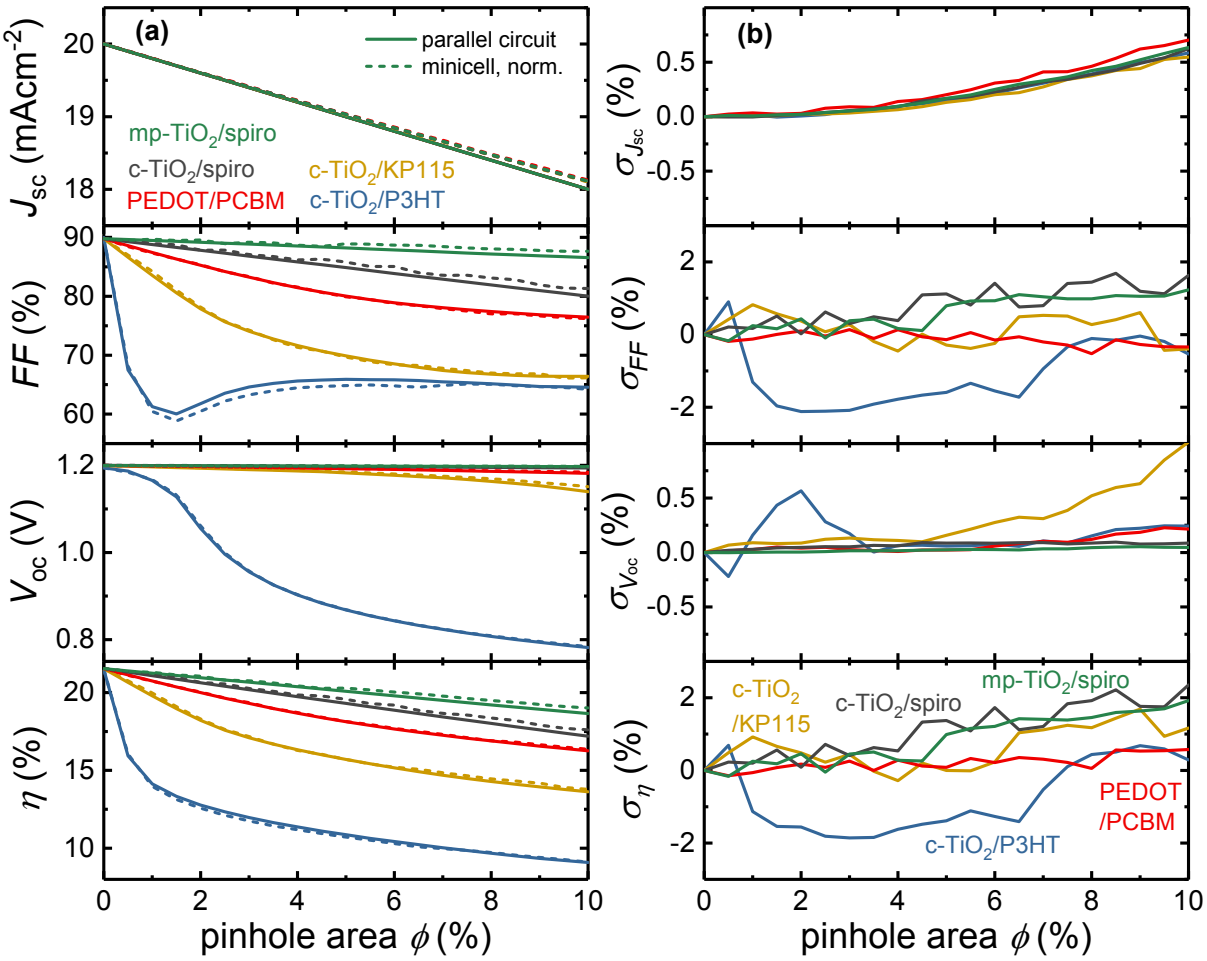

Figure S6: Comparison of the results obtained from the parallel circuit model and the mini-cell simulated with PVMOS. The small deviations between the two approaches apparent in (a) are quantified in (b).

References

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