How Contact Layers Control Shunting Losses from Pinholes in Thin-Film Solar Cells

Pascal Kaienburg[1]*, Paula Hartnagel[1,2], Bart E. Pieters[1], Jiaoxian Yu[1,3], David Grabowski[1], Zhifa Liu[1,4], Jinane Haddad[1], Uwe Rau[1] and Thomas Kirchartz[1,2]*

[1]IEK5-Photovoltaics, Forschungszentrum Jülich, 52425 Jülich, Germany

[2]Faculty of Engineering and CENIDE, University of Duisburg-Essen, Carl-Benz-Str. 199, 47057 Duisburg, Germany

[3]Shandong Provincial Key Laboratory of Processing and Testing Technology of Glass & Functional Ceramics, School of Materials Science and Engineering, Qilu University of Technology (Shandong Academy of Sciences), 250353 Jinan, P. R. China

[4]State Key Laboratory of Structural Chemistry, Fujian Institute of Research on the Structure of Matter, Chinese Academy of Sciences Fuzhou, 350002 Fujian, P. R. China

Pascal Kaienburg* – paskai@posteo.de

Thomas Kirchartz* – t.kirchartz@fz-juelich.de

* Corresponding author

Abstract

An absorber layer that does not fully cover the substrate is a common issue for thin-film solar cells such as perovskites. However, models that describe the impact of pinholes on solar cell performance are scarce. Here, we demonstrate that certain combinations of contact layers suppress the negative impact of pinholes better than others. The absence of the absorber at a pinhole gives way to a direct electrical contact between the two semiconducting electron and hole transport layers. The key to understand how pinholes act on the solar cell performance is the resulting non-linear diode-like behaviour of the current across the interface between these two layers (commonly referred to as a shunt current). Based on experimentally obtained data that mimic the current-voltage characteristics across these interfaces, we develop a simple model to predict pinhole-induced solar cell performance deterioration. We investigate typical contact layer combinations such as TiO2/spiro-OMeTAD, PEDOT:PSS/PCBM and TiO2/P3HT. Our results directly apply to perovskite and other emerging inorganic thin-film solar cells and the methodology is transferable to CIGS and CdTe. We find substantial differences between five commonly applied contact layer combinations and conclude that it is not sufficient to optimize the contact layers of any real-world thin-film solar cell only with regard to the applied absorber. Instead, in the context of laboratory and industrial fabrication, the tolerance against pinholes (i.e., the mitigation of shunt losses via existing pinholes) needs to be considered as an additional, important objective.

I. Introduction

The rapid market growth of solar cells goes along with increased research efforts on new photovoltaic absorber materials. Motivated by potentially lower production costs in comparison to silicon technology, many efforts focus on wet-chemical solution-based or gas-phase processing routes that simultaneously aim for high power conversion efficiencies. In an early state of technology new polycrystalline absorber materials suffer from inhomogeneous films and especially pinholes in the absorber layer[1]. Examples are Sb_2S_3[2,3], SnS[4] and lead-free perovskites[5,6]. In the case of more optimized lead-based perovskites, the complex mechanisms of film formation from solution[7,8] can be controlled by certain spin-coating processes which yield compact, homogeneous and pinhole-free perovskite layers for small-scale devices in the lab [9–13]. For up-scaled industrial fabrication, spin-coating is not suitable[14] and the applied deposition methods face more processing constraints such as high yields, high throughput and low solvent toxicity[15,16]. As of today, pinholes in the absorber layer remain an issue in up-scaled perovskite fabrication[16,17] as well as in the already established thin-film photovoltaic technologies CdTe[18–20], Cu(In,Ga)Se_2 (CIGS)[21,22] and thin-film silicon[23].

A pinhole in the absorber layer of a thin-film solar cell results in a direct electrical contact between the top and the bottom contact layer. These layers are in most cases not made of metallic conductors but semiconducting materials and are commonly denoted as the electron and the hole transport layer (ETL, HTL), optimized to extract the specific type of charge carrier from the photovoltaic absorber material. The area of the pinhole, i.e. the contact area between the two charge transport layers, will provide a current path connected in parallel to the main diode of the regular cell area. As the conductivity of the ETL/HTL interface is expected to be much higher than the conductivity of the regular cell areas, these pinholes provide a significant loss path, commonly denoted as shunt. Thus, the current-voltage characteristic of the ETL/HTL contact determines whether or not such a shunt is detrimental for the solar cell[24,25] and different ETL/HTL combinations are expected to cause different shunt characteristics.

For the case of CIGS solar cells it has been shown that incorporation of an layer of undoped zinc oxide (*i*-ZnO) reduces the detrimental impact on solar cell performance caused by inhomogeneity across the absorber film[26] – including the worst case of a pinhole. The *i*-ZnO is unfavorable when considered only in a one-dimensional band diagram, but its benefit can be understood in terms of two-dimensional variations of the electronic quality across the absorber film[26]. As demonstrated by a detailed experimental study[27], the impact of shunts from pinholes in the CIGS absorber is further reduced reliably by an additional layer of CdS deposited in a chemical bath that better ensures a closed coating than the sputtered *i*-ZnO. The example of CIGS shows that careful engineering of the contact layers also with respect to inhomogeneity or shunts is mandatory to achieve a high solar cell performance.

For the case of perovskite and other solution-processed thin-film solar cell technologies, a large variety of electron and hole contact layer combinations is applied which represents a powerful degree of freedom in the stack design. Certain interlayers were also reported to increase the robustness of perovskite solar cells towards shunts[25,28]. While a detrimental impact of pinholes is thus widely recognized and postulated[29–32], the electronic nature of pinholes is not well understood and models that

describe the impact of pinholes on solar cell performance are missing. Additionally, neither a systematic evaluation of contact layers with respect to robustness against shunting from pinholes, nor a suitable method to do so has been reported so far.

In this work, we accept the existence of pinholes in the absorber layer as a given feature of real-world thin-film solar cells. We furthermore acknowledge the physical nature of pinholes which give way to a direct physical and electrical contact between the semiconducting ETL and HTL. This semiconductor heterojunction is shown to produce a diode-like and thus clearly non-linear current-voltage characteristic. First, we illustrate how non-linear shunting affects the current-voltage characteristic of a solar cell and compare it to the qualitatively different behavior of a linear shunt. We then proceed to investigate different electron and hole transport material combinations, namely mesoporous TiO_2/spiro-OMeTAD, compact TiO_2/spiro-OMeTAD, PEDOT:PSS/PCBM, compact TiO_2/P3HT and compact TiO_2/KP115. These contact layer materials are commonly used with emerging solar cell absorber materials such as perovskites (both lead-based and lead-free) and Sb_2S_3. Additionally, the methodology can be applied to other thin-film technologies like CdTe and CIGS that typically use different contact layer materials. Experimentally obtained current-voltage characteristics of the pinholes, that indeed have a diode-like characteristic, are used to predict the impact of pinholes on solar cell performance with numerical simulations and simple equivalent circuits. We discuss under which circumstances pinholes have a severe impact on fill factor and open-circuit voltage. Finally, we identify interlayer combinations that reduce the impact of shunting from pinholes and discuss options to improve the contacts' tolerance against pinholes. We thereby highlight the importance of optimizing contact layers also with respect to real-world solar cells that contain pinholes instead of only considering the unharmed absorber domains.

Qualitative Picture

In this section, we consider the physical and electrical situation at a pinhole and illustrate the consequence of such inhomogeneity in the device on the current density-voltage (*J*-*V*) characteristic of a solar cell. Figures 1(a) and (b) exemplarily show scanning electron microscope images of two absorber layers that were deposited via spin-coating from solution and suffer from incomplete substrate coverage. Lead-based perovskites[9,33,34] (a) are prominent candidates for highly efficient thin-film solar cells and Sb_2S_3[35,36] (b) serves as an example for a less-optimized absorber technology. Both films contain pinholes with sizes in the range of 10-100 nm.

The layer sequence at a pinhole and at the regular domains with absorber is illustrated in fig. 1(c) for a typical solar cell. The regular cell stack consists of a HTL, an absorber and an ETL that are sandwiched between a metal and a TCO electrode. Given that the material deposited on top of the absorber infiltrates the pinholes, these become domains where the ETL and HTL are in direct physical contact. The pinhole domains thus form parasitic current paths - indicated by the arrow in fig. 1(c). The schematic energy level diagram of the ETL/HTL interface in fig. 1(d) reveals the nature of this shunt: the two (doped or undoped) semiconductors that function as electron and hole transport material form a (type-II) heterojunction – meaning that both the conduction and valence band of the ETL are

energetically below those of the HTL - that should have a diode-like, and thus clearly non-linear, current-voltage *J-V* characteristic.

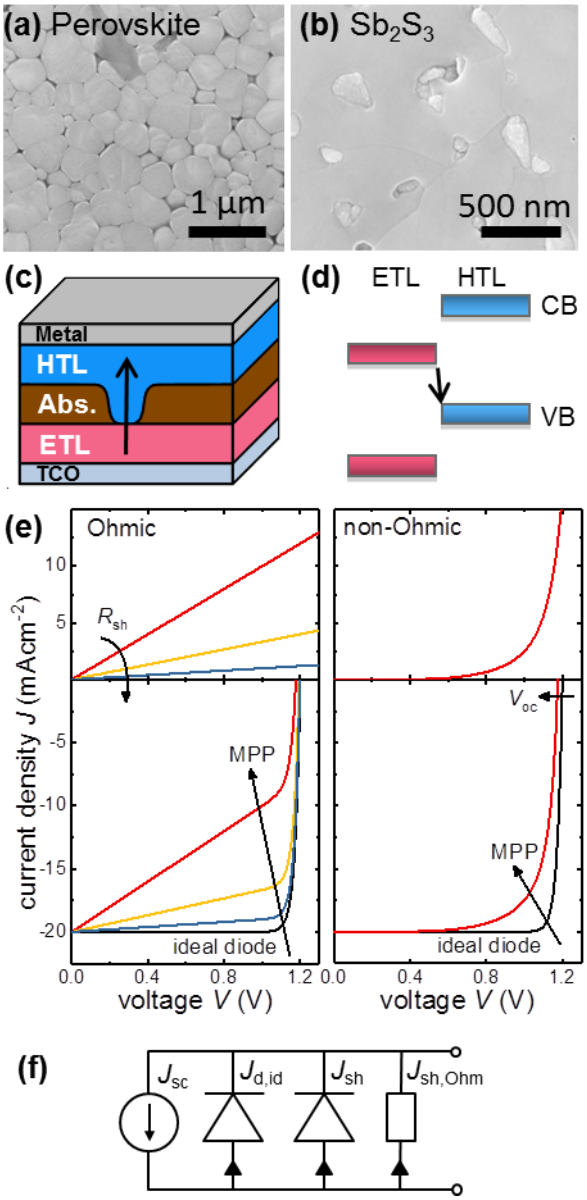

Figure 1: SEM images of (a) perovskite and (b) Sb_2S_3 absorber films with pinholes that expose the underlying substrate. (c) Typical layer stack with a pinhole in the absorber that results in a shunt current at the physical contact between ETL and HTL. (d) Schematic energy diagram at the ETL/HTL interface pinhole. The bars indicate the conduction (CB) and valence (VB) bands. The arrows in (c) and (d) indicate the diode-like recombination current. (e) Shunt characteristics (top panels) and impact on an ideal solar cell (bottom panels) with J_{sc}=20 mAcm^{-2}, n_{id}=1 and J_0 chosen such that V_{oc}=1.2 V. The maximum power point (MPP) is affected in different ways for the two cases. The non-Ohmic shunt has the form $a(\exp(qV/(nkT)) - 1) + bV^c$ to model a non-linear but also not purely exponential shunt. (f) Equivalent circuit for a solar cell with photocurrent source J_{sc}, ideal diode $J_{d,id}$, a non-linear shunt J_{sh} from

pinholes in the absorber and an additional Ohmic shunt $J_{sh,Ohm}$ that could result from a metal-metal interface if also ETL and HTL contain pinholes.

Regarding the influence on the solar cell *J-V* characteristic, textbooks typically discuss shunts in terms of an Ohmic resistor[37–40] which allows the development of simple models and approximations, concerning e.g. the fill factor[41,42]. An Ohmic shunt is sometimes also used to describe pinholes in thin-film solar cells[43] with layer stacks similar to the one depicted in fig. 1(c) although the shunt characteristic should be clearly non-linear as discussed before. The non-linearity of shunts has been discussed in different contexts[44–50] but not with a focus on pinholes in the absorber and their impact on solar cell performance. In the following we illustrate the qualitative difference between the influences of linear (Ohmic) versus non-linear (non-Ohmic, diode-like) shunts. The top panels of fig. 1(e) depict the *J-V* characteristics of an Ohmic and non-Ohmic shunt. To illustrate the shunts' impacts on an ideal solar cell as depicted in the bottom panels, we calculate the current of a simple equivalent circuit that is defined via the parallel connection of the shunt current J_{sh}, the current of an ideal diode $J_{d,id}$ and a photocurrent J_{sc} resulting in

$$J(V) = -J_{\mathrm{sc}} + J_{\mathrm{d,id}} + J_{\mathrm{sh}} = -J_{\mathrm{sc}} + J_0 \left(\exp\left[\frac{q\,V}{n_{\mathrm{id}} k_{\mathrm{b}} T}\right]\right) + J_{\mathrm{sh}}. \qquad (1)$$

Here, q is the elementary charge, k_b is the Boltzmann constant, T is the temperature, n_{id} is the diode ideality factor, J_0 is the saturation current density and V is the externally applied voltage. The parameter values for the ideal diode are given in the figure caption and all series resistances are neglected in this simple model. According to eq. 1, the shunt current from a pinhole can be interpreted as an additional recombination current, also indicated by the arrow in fig. 1(d). The Ohmic shunt in fig. 1(e) introduces a characteristic slope at J_{sc} and reduces the fill factor *FF*. Only for very large shunts (small Ohmic shunt resistance) the V_{oc} is slightly affected but at the same time the *FF* has decreased more dramatically to almost 25%. Compared to the Ohmic case, the diode-like (exponential) shunt in fig. 1(e) has a substantially different impact on the ideal solar cell. The current at low voltages is not affected at all and the decrease in fill factor differs qualitatively from the Ohmic case. Even more strikingly, there is a decrease in V_{oc} while the value of the *FF* is still decent. This behaviour can be rationalized from the exponential drop in resistance of a diode-like shunt. Figure 1(f) shows an equivalent circuit that contains both, a non-Ohmic diode-like and an Ohmic linear shunt. The latter could for example result from a direct interface between the metal contacts that would appear if also the ETL and HTL had pinholes. In this work, we focus on the non-Ohmic shunt stemming from pinholes in the absorber layer.

In summary, Ohmic and non-Ohmic shunts might – in general - reduce the maximum power point to the same degree. However, while an Ohmic shunt reduces the total current at lower voltage; the non-Ohmic shunt becomes radically more harmful towards higher voltage. Consequently, the key to a qualitative understanding of the influence of pinholes on the *J-V* characteristic of a solar cell is to consider the non-linear nature of the diode-like shunt source in some detail. Going one step further, we will develop a quantitative model to analyze potential differences between ETL/HTL combinations.

II. Method

To evaluate differences in shunt behavior between various ETL/HTL combinations the respective current-density-voltage (*J*-*V*) characteristic at the pinholes must be known. To do so, we produced devices from ETL/HTL combinations in a stack without absorber layer as displayed in the inset of fig. 2(a). For the *n*-*i*-*p* case, the stack is thus TCO/ETL/HTL/metal. Such structures, which we refer to as ETL/HTL diodes, are thought to mimic the pinhole domains in a full solar cell. We found the devices to be imperfect diodes that cannot be easily parametrized, so that we worked with the full *J*-*V* characteristic of the ETL/HTL diode obtained from measurements. The dark *J*-*V* characteristic of the ETL/HTL diode displayed by the black circles in fig. 2(a) we basically represents the shunt characteristics at a pinhole. However, for large voltages this experimental *J*-*V* characteristic is dominated by the series resistance of the TCO ($R_{ETL/HTL}$) stemming from the lateral charge transport across the TCO, so that the measured current of the ETL/HTL diode underestimates the current through a pinhole. Consequently, $R_{ETL/HTL}$ has to be removed in order to obtain the *J*-*V* characteristic of the pinholes themselves. We do so by fitting the experimental data and obtain the pinhole's *J*-*V* characteristic shown in red in fig. 2(a). The fitting is done with the numerical device simulator PVMOS[51], which is described in detail in supplement section S2 and S3. In brief, PVMOS is a device simulator that applies the network simulation method for a network of resistances and diodes that are interconnected laterally via resistors as shown in fig. S1. The open-source code of PVMOS is available online[52]. The subsequent calculations build on the pinhole's *J*-*V* characteristic simulated with PVMOS.

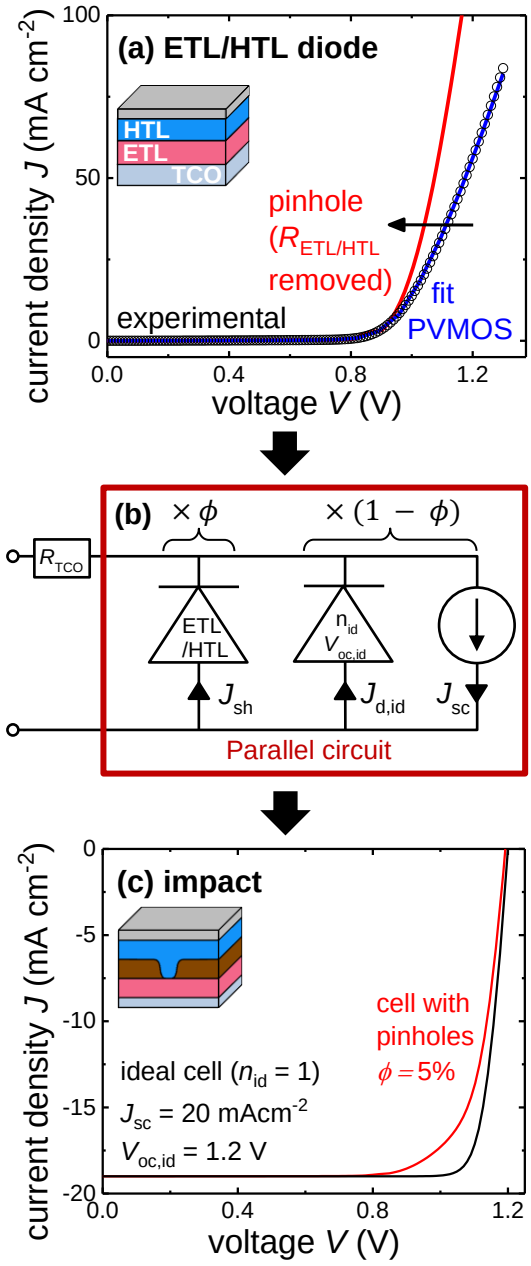

Figure 2: Methodology to predict the impact of pinholes on device performance. (a) A device without absorber layer, termed ETL/HTL diode, is produced to mimic the situation at a pinhole. The measured *J-V* characteristic is corrected for the TCO series resistance $R_{ETL/HTL}$ and then serves as shunt characteristic for the simple parallel equivalent circuit in (b). The current of the shunt and the ideal solar cell are weighted by the cumulative pinhole area fraction ϕ and in a last step the effective series resistance R_{TCO} of the TCO is added again. (c) Exemplary result of the equivalent circuit model.

We propose a simple parallel circuit model to predict the impact of the pinhole's experimentally obtained shunt characteristic on the performance of the solar cell. We later show the validity of this quasi-zero-dimensional approximation. We call the percentage of uncovered area with respect to the

total cell area the (cumulative) pinhole area (fraction) ϕ. Thus, for ϕ = 0%, the absorber layer completely covers the substrate while ϕ = 100% means that there is no absorber at all. We focus on realistic cases of reasonably efficient solar cells with pinhole area fractions up to 10%. The parallel circuit indicated by the red frame in fig. 2(b) consists of a non-linear shunt J_{sh} – given by the pinhole's characteristic - and an ideal diode J_{id} with photocurrent source J_{sc} that represents the ideal pinhole-free parts of the solar cell. To obtain the current of the parallel circuit J_{par}, the current contributions from the ideal solar cell and the shunt are weighted according to the pinhole area fraction ϕ via

$$J_{\mathrm{par}} = \phi\, J_{\mathrm{sh}} + (1-\phi)(J_{\mathrm{d,id}} - J_{\mathrm{sc}}). \tag{2}$$

As a standard parametrization of the ideal solar cell we chose a photocurrent of J_{sc} = 20 mAcm^{-2} and an ideal diode with ideality factor n_{id} = 1 and a saturation current density J_0 that yields an open-circuit voltage of $V_{oc,id}$ = 1.2 V.

To finally obtain the *J-V* characteristic of a full solar cell, the series resistance of the TCO has to be added to the *J-V* characteristic of the parallel circuit. This can be done via modelling the distributed series resistance of the TCO with PVMOS or by replacing it by an effective Ohmic series resistance R_{TCO} as indicated in the equivalent circuit in fig. 2(b). For our cell geometry and TCO sheet resistance we find $R_{TCO} \approx 17\ \Omega$ when ITO is used and $R_{TCO} \approx 14\ \Omega$ when FTO is used. This effective series resistance can be either estimated by a simple calculation or by fitting it to the results obtained from PVMOS as described in supplement section S4. The resulting *J-V* characteristic of the equivalent circuit is displayed in fig. 2(c) for a pinhole area fraction of 5% and an ETL/HTL diode based on PEDOT/PCBM. The deviations from the ideal solar cell characteristic indicate the detrimental impact of the shunt from pinholes on the device performance. The impact on *FF* and V_{OC} is similar to our illustration in fig. 1(e).

While an inhomogeneous device can always be described by a single effective *J-V* characteristic, we need to validate that the simple zero-dimensional equivalent circuit proposed in fig. 2(b) approximates this effective *J-V* characteristic well. We therefore performed more complex simulations of a pinhole-containing solar cell with PVMOS and compare the results to the simple equivalent circuit model. With PVMOS we are able to simulate the actual lateral inhomogeneity of the solar cell consisting of randomly distributed nanoscopic pinholes within domains of an ideal absorber. The model used for validation is described in supplement section S5. Deviations between the parallel circuit model and the full solar cell amount to less than 2% for all investigated ETL/HTL combinations and pinhole areas as shown in fig. S6(b). We thus continue our analysis with the simple parallel circuit model which also facilitates the qualitative understanding of the pinhole's impact.

III. Results

Prediction of pinhole impact

In the following, we compare different contact layer combinations that are typically used in today's solution-processed thin-film solar cells. The experimental dark *J-V* data of the corresponding ETL/HTL diodes is shown in fig. 3(a) after the TCO's series resistance has been removed. All *J-V* characteristics are indeed non-linear and resemble a diode rather than an Ohmic resistor. Despite the qualitative similarity,

different ETL/HTL combinations differ substantially in quantitative terms. Common layer stacks used with perovskites in an *n-i-p* configuration are mesoporous titanium dioxide with Spiro-OMeTAD (mp-TiO_2/spiro) and compact TiO_2 with Spiro-OMeTAD (c-TiO_2/spiro), while the *p-i-n* configuration is typically based on a combination of Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS, short: PEDOT)with phenyl-C_{61}-butyric acid methyl ester (PEDOT/PCBM). Other new absorber materials like Sb_2S_3 that are embedded in an *n-i-p* stack make use of the versatility of conjugated polymers to choose an appropriate hole transport material. We investigated compact TiO_2 with Poly(3-hexylthiophene) (c-TiO_2/P3HT) and compact TiO_2 with KP115 (c-TiO_2/KP115). Figure 3(a) shows that certain interlayer combinations like TiO_2/P3HT reach high current densities at much lower voltages than other combinations such as mp-TiO_2/spiro.

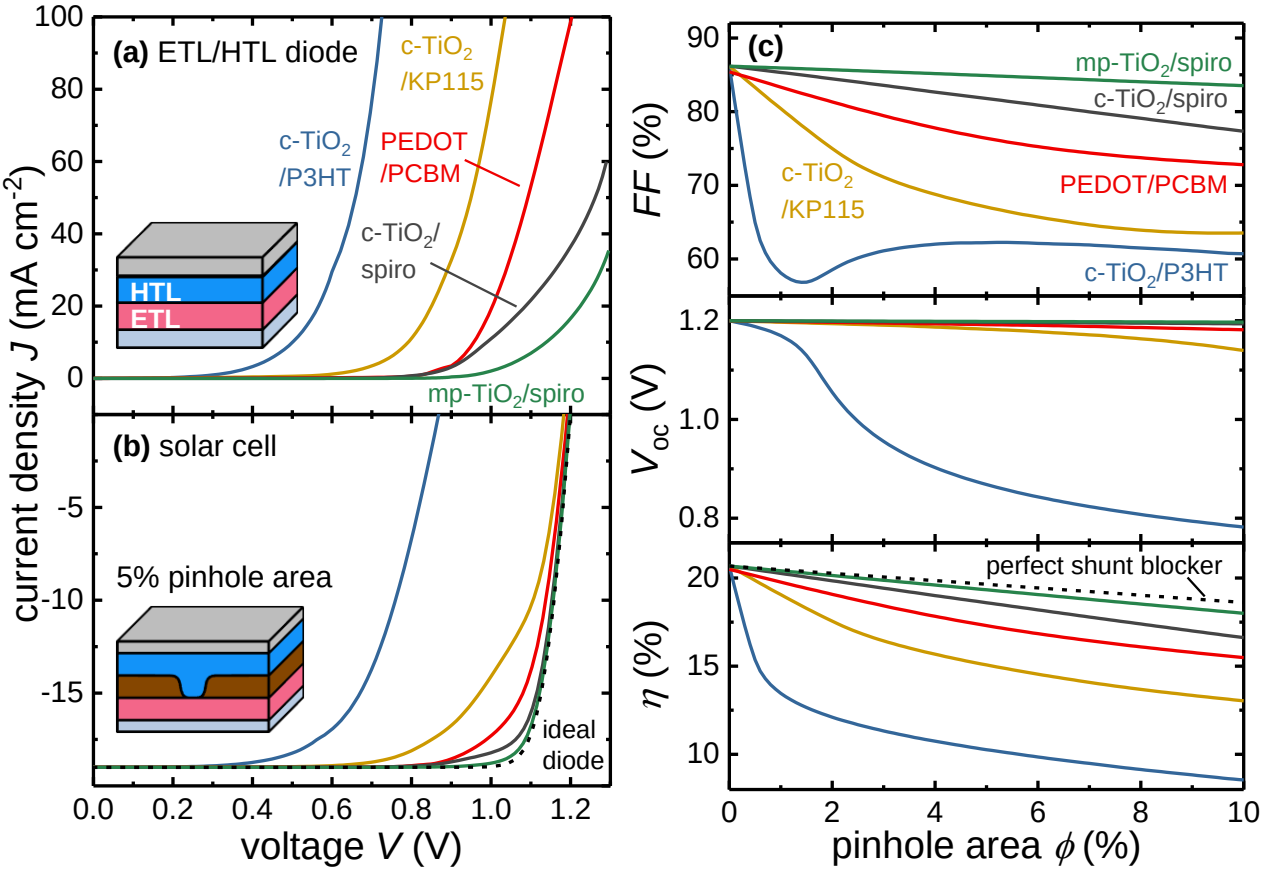

Figure 3: Results for five commonly used contact layer combinations: (a) Experimental *J-V* characteristics of ETL/HTL combinations without absorber after correcting for the TCO's series resistance. (b) Resulting simulated light *J-V* curves of a full solar cell with a pinhole area fraction of 5%. The dashed line represents an ideal solar cell that covers 95% of the cell area and, just like the other curves, takes R_{TCO} into account. (c) Fill factor *FF*, open-circuit voltage V_{oc}, and efficiency η for different cumulative pinhole area fractions. The perfect shunt blocker indicated in the bottom panel describes an ideal ETL/HTL combination where the solar cell only suffers from the decrease in active cell area and additional shunt losses are avoided.

The difference in shunt characteristic directly translates into solar cell performance as shown by the calculated illuminated *J-V* curves at a pinhole area fraction of $\phi = 5\,\%$ in fig. 3(b). While the *J-V* characteristic of the mp-TiO_2/spiro configuration is almost identical to the ideal solar cell, all other ETL/HTL combinations show a reduced fill factor *FF*. In the extreme case of c-TiO_2/P3HT not only the *FF* decreases but also the open-circuit voltage V_{oc} drops by several hundreds of meV. We qualitatively refer to the degree to which an ETL/HTL combination prevents a pinhole-induced decline in performance as its ability to block shunts. In this sense mp-TiO_2/spiro would be a good shunt blocker and c-TiO_2/P3HT would be a bad one.

The shunt impact on *FF*, V_{oc}, and efficiency η is further analyzed for varying pinhole area fractions in fig. 3(c). As expected, the performance drops with increasing pinhole area fraction. Solar cells based on ETL/HTL combinations with good shunt blocking properties are affected less than those that conduct high shunt currents at the pinholes. With the exception of c-TiO_2/P3HT all ETL/HTL combinations mostly suffer from a decline in *FF* rather than V_{oc}. A slight impact on V_{oc} can be identified for c-TiO_2/KP115 and PEDOT/PCBM at pinhole area fractions >5%. For the case of the bad shunt blocker c-TiO_2/P3HT the *FF* drops sharply at small pinhole area fractions while the V_{oc} is barely affected. However, for pinhole area fractions larger than 1% the *FF* almost saturates around 60% while the V_{oc} declines heavily. The strong impact of pinholes on the V_{oc} also explains the qualitatively different behaviour of the *FF* for c-TiO_2/P3HT. For pinhole area fractions below 1% the shunt current is not large enough to decrease the V_{oc} and only affects the maximum power point (*MPP*) and thus the *FF*. Towards larger pinhole area fractions the V_{oc} is affected in addition to the *MPP*. The *FF* is composed by the ratio of the voltage at *MPP* and the V_{oc} via $FF = (J_{\mathrm{mpp}}V_{\mathrm{mpp}})/(J_{\mathrm{sc}}V_{\mathrm{oc}})$, which yields the irregular shape of the *FF* in the transition regime from a decrease only in V_{mpp} to a regime with decrease also in V_{oc}. The *MPP* itself behaves more regular as can be seen from the monotonous decrease in efficiency that is proportional to the power at the *MPP*. Between the different ETL/HTL combinations, the resulting efficiency varies over several (absolute) per cent for a given pinhole area fraction. With increasing pinhole area fraction there is always a decrease in efficiency mediated by the short-circuit current and caused by the decreased active cell area. The dashed line in fig. 3(c) represents this obvious loss, which can also be regarded as the upper limit of a perfectly shunt-blocking ETL/HTL combination. The mp-TiO_2/spiro stack comes very close to this ideal case even for large pinhole area fractions. It can be concluded that with increasing pinhole area fraction or decreasing shunt blocking capability, the *FF* is affected first but eventually the V_{oc} becomes limiting to device performance.

It is important to note that this behaviour directly results from the specific *J-V* characteristic of the pinhole, which is not linear but not a single exponential, either. If the pinhole was an ideal diode described by an exponential function, the current of the parallel circuit would be given by the sum of two exponentials according to eq. (2). If the exponential pinhole current was then dominant, it would determine the total current according to its ideal diode properties, formally taking the role of the recombination current. This means it would decrease the V_{oc} but yield the *FF* of an ideal diode. However, from the data of the ETL/HTL diodes we found that the pinhole characteristic is not a simple exponential and the impact on the *FF* is stronger than on the V_{oc} which can be rationalized by the fact that the current density through the pinholes is much higher than the current density through the absorber

domains. To illustrate this we consider the situation where the current through the pinholes fully compensates the current through the absorber domains. According to eq. (2) this requires the shunt current to be a factor of $(1-\phi)/\phi$ larger than the current through the absorber domains which is a factor of 19 for $\phi = 5\%$. At such high currents non-exponential terms seem to dominate the pinhole *J-V* characteristic with one possible cause being the series resistance of the ETL and HTL.

As stated above, the impact of a shunt is determined by the ratio between the current through the pinhole and the current through the absorber layer of the solar cell. Therefore not only the shunt characteristic and the pinhole area fraction affects the shunt impact but also the electrical properties of the absorber domains – in our case the parameterization of the ideal diode. As a consequence of their non-linear shunt characteristic, pinholes have a stronger influence at higher voltages. In fig. 4 the $V_{oc,id}$ of the ideal diode was varied while the pinhole area fraction was fixed at 5%. With increasing $V_{oc,id}$ of the ideal diode the V_{oc} of the device with pinholes increases almost proportionally for four of the five tested ETL/HTL combinations. Only c-TiO_2/P3HT deviates and even saturates at a certain voltage that depends on the pinhole area fraction which then leads to a saturated efficiency as well. The initial increase of the *FF* for the discussed ETL/HTL combinations with increasing $V_{oc,id}$ can be simply attributed to the larger V_{oc}[41,42]. At a certain $V_{oc,id}$ the detrimental impact of the shunt becomes large enough to affect the *FF* which then reaches a maximum and decreases for higher $V_{oc,id}$ which in some cases also leads to a saturation of the efficiency. This means that by limiting the V_{oc} as for c-TiO_2/P3HT or the *FF* as for c-TiO_2/KP115 and PEDOT/PCBM, the presence of pinholes can – depending on the ETL/HTL's shunt blocking quality and the pinhole area fraction - set a firm upper limit for the solar cell efficiency even if the intact absorber domains are further improved. Moreover, the issue of pinholes becomes more critical for solar cells that reach high open-circuit voltages in the absence of pinholes. Exactly these materials are of special interest for photovoltaic research and industrial application which underlines the practical relevance of pinholes and the need for charge transport layer combinations that effectively suppress the resulting shunts.

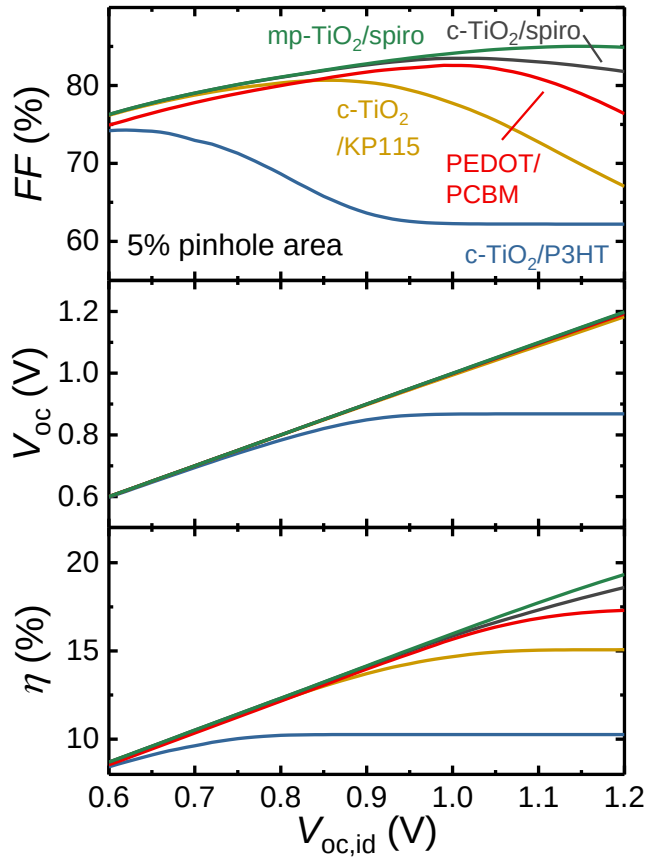

Figure 4: For higher $V_{oc,id}$ of the absorber domains, pinholes become more critical to device performance due to significantly higher shunt currents at higher voltages.

There are few parameters to tune and improve the shunt blocking properties for a given ETL/HTL material combination because the ETL/HTL interface largely determines the shunt characteristic. One available option is to increase the series resistance of the ETL/HTL stack, for example by simply increasing the layer thickness or introducing an additional resistive layer as in the case of CIGS solar cells[26,27]. An increased series resistance restricts the exponential shunt current at high voltages. However the same series resistance will act on the intact absorber domains. We illustrate the described effect by adding an Ohmic series resistance ΔR_s to the pinhole's *J-V* characteristic as well as to the ideal diode that represents the absorber domains of the solar cell. The trade-off between better shunt blocking and increased overall series resistance can be clearly seen in *FF* and efficiency for c-TiO_2/KP115 and PEDOT/PCBM in fig. 5 where a maximum in efficiency is reached for a finite additional series resistance. For c-TiO_2/P3HT a higher series resistance also improves the V_{oc}. Altogether, more resistive electron and hole transport layers can improve the efficiency of certain ETL/HTL combinations but the optimized efficiency still stays behind that of mp-TiO_2/spiro or c-TiO_2/spiro. Here, no benefit of an additional series resistance is observed because these ETL/HTL combinations are already good shunt blockers. A similar effect of beneficial finite series resistance was pointed out by Rau et al.[53] for inhomogeneous diode properties where an optimum series resistance was found that – depending on the degree of

fluctuations – balances the benefits of smoothing electronic fluctuations and the decrease in *FF* caused by the additional series resistance.

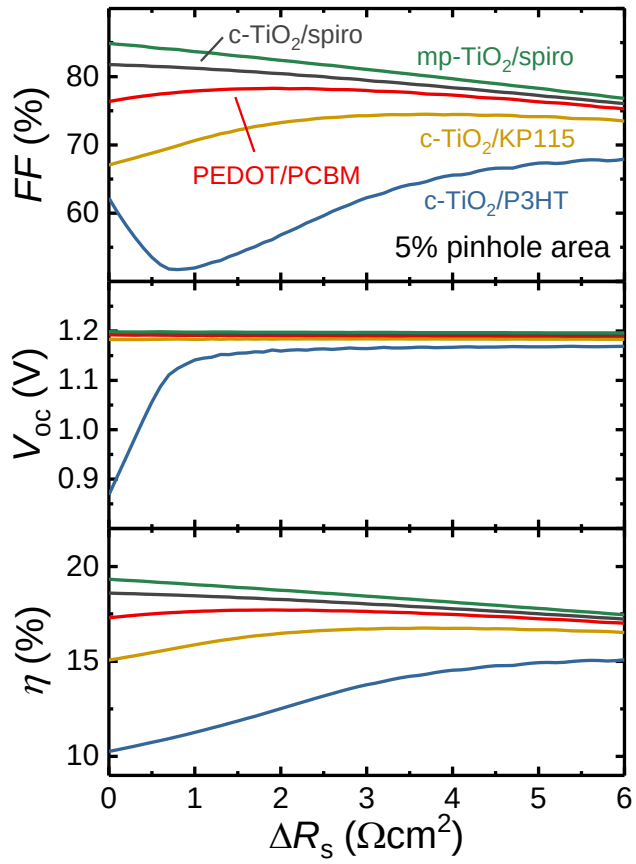

Figure 5: An additional series resistance ΔR_s of the ETL/HTL combination suppresses the shunt current through the pinhole and can be beneficial for the device performance. The trade-off with the increased overall series resistance leads to an optimum performance at finite ΔR_s in some cases.

Comparison of devices with and without absorber

Experimental *J-V* characteristics of full solar cells based on the pinhole-bearing spin-coated absorber layers Sb_2S_3 shown in fig. 6(b) and perovskite shown in fig. 6(d) support the proposed impact of non-linear shunts. Both cases apply an *n-i-p* layer stack where the hole transport layer HTL is varied which changes the shunt characteristic at the pinholes. The underlying ETL is not varied so that differences in the film formation of the absorber can be dismissed. Figure 6(a) and (c) show the experimental *J-V*-curves of the stacks without absorber and fig. 6(b) and (d) show the illuminated *J-V* characteristic of the full cell.

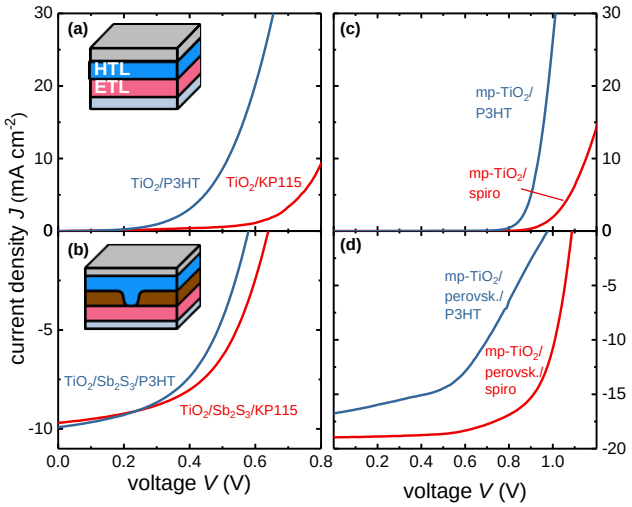

Figure 6: Experimental current density vs. voltage (*J-V*) characteristics of (a),(c) different ETL/HTL diodes in the dark and (b),(d)full solar cells under illumination based on (a),(b) Sb_2S_3 and(c),(d) perovskite absorbers. In both cases the interlayer combination with higher shunt currents shows a decrease in V_{oc} and *FF*. For perovskite (d) other effects seem to be superimposed on the shunt deterioration. The solar cell parameters in (b) are J_{sc}=9.9 mAcm^{-2}, *FF*=51%, V_{oc}=0.578 V for c-TiO_2/Sb_2S_3/P3HT and J_{sc}=9.7 mAcm^{-2}, *FF*=53%, V_{oc}=0.641 V for c-TiO_2/Sb_2S_3/KP115. In (d) we obtained J_{sc}=16.8 mAcm^{-2}, *FF*=47%, V_{oc}=0.977 V for mp-TiO_2/ perovskite/P3HT and J_{sc}=19.0 mAcm^{-2}, *FF*=67%, V_{oc}=1.09 V for mp-TiO_2/perovskite/spiro.

Antimony sulfide Sb_2S_3 is employed in fig. 6(b) according to ref.[35] as an example of a relatively unexplored absorber material. It can be seen from fig. 6(a) that the interlayer combination c-TiO_2/P3HT causes worse shunts than c-TiO_2/KP115. The V_{OC} of the corresponding c-TiO_2/Sb_2S_3/P3HT solar cell is significantly lower compared to c-TiO_2/Sb_2S_3/KP115. This behaviour is expected from the model developed in this article and can be attributed to the higher shunt currents of c-TiO_2/P3HT at open circuit. The pinholes thus represent a significant limitation of the V_{OC} and the solar cell performance in the case of the c-TiO_2/P3HT contact layer combination. Again, the drop in V_{OC} in conjunction with a still appreciable *FF* cannot be explained by an Ohmic shunt but only by a non-linear one.

As a second example, lead-based perovskite is applied in a solar cell with the interlayer combinations mp-TiO_2/spiro and mp-TiO_2/P3HT in fig. 6(c) and (d). The mp-TiO_2/P3HT diode in fig. 6(c) conducts much larger currents around the V_{OC} and MPP than the mp-TiO_2/spiro. The strong suppression of shunts in the case of the mp-TiO_2/perovskite/spiro allows a solar cell with decent performance while V_{OC} and *FF* are reduced in the case of mp-TiO_2/ perovskite/P3HT. However, the J_{sc} also decreases which cannot be explained within the framework described in this work. By applying P3HT instead of spiro-OMeTAD more properties of the solar cell seem to change than just the shunt currents at the pinholes.

IV. Discussion

Generally, it is difficult to experimentally distinguish between shunting and other effects that are superimposed on the *J-V* characteristic. As an obvious example, when one interlayer is exchanged by

another not only the interface at the pinhole which dictates the shunt characteristic is altered, but also the band diagram of the pinhole-free absorber domains. When the underlying interlayer is exchanged, the growth conditions and resulting properties of the absorber may change as well[54]. Neglecting this influence on absorber layer formation and taking a broader perspective, the capability of a certain charge transport layer combination to suppress shunt currents at a pinhole can be regarded as a contact property. Other contact properties include optical aspects such as parasitic absorption and light management[55,56] as well as selectivity - comprising surface recombination of minority carriers and series resistance of majority carriers[57] – and built-in electric field. While the optical contact properties mostly affect the cell's J_{sc}, selectivity and built-in field directly affect V_{oc} and FF[57–59]. These properties mainly depend on one of the contacts - namely its geometric dimensions, the choice of material (including details of processing) and the interface it forms with the absorber layer which for example determines trap densities. In contrast, the non-linear shunting behavior results from the combination of both contacts and the interface they form. In the final illuminated *J-V* characteristic all of the mentioned contact characteristics are superimposed so that the impact of shunting cannot be clearly identified experimentally. Nevertheless, the shunt blocking properties are crucial for the quality of the contact with regard to solar cell performance in the presence of pinholes in the absorber layer.

Different concepts to circumvent pinholes or moderate their impact on device performance have been proposed or established. The resistive shunt mitigation discussed in section IV appears as a general concept for optimizing the efficiency of real world thin-film solar cells[53,60,61]. In the case of CdTe, pinholes are avoided by simply depositing an absorber layer that is much thicker than is required for efficient photon absorption [18,19] which could generally reduce charge carrier collection efficiency[58] and increase fabrication time and costs. Given that the absorber film contains pinholes, these could be passivated via selectively depositing a highly resistive polymer as is done for CdTe[62,63] - a route that has also been explored for perovskites[25]. However, such extra efforts and tradeoffs can be spared if a shunt-blocking ETL/HTL is used as shown in this work and has been argued recently for CdTe[20].

Pinholes may not only appear in the absorber layer of a thin-film solar cell but also in any of the other layers including the directly adjacent ETL and HTL. Then, a more refined contact configuration consisting of a sequence of different layers, maybe deposited via different methods, might prevent a deterioration from pinholes as was shown in the systematic study[27] on CIGS solar cells mentioned in the introduction. Our findings should also apply to other (opto-) electronic devices with large aspect ratios such as photodetectors based on thin films. Indeed, it was shown for perovskite[64–68] and PCDTBT:PCBM[69] photodiodes that an additional layer of C_{60} as ETL improves the device performance by reducing the noise current. These devices operate under reverse bias, where the shunt current through pinholes competes with the diode's saturation current density J_0, which is significantly lower than the J_{sc} or forward diode current that are most relevant for pinholes in solar cells. Although the relevant quantities and physical phenomena are different, the general methodology should be applicable to similar problems in other applications.

V. Conclusion

Pinholes in the absorber layer are a common feature of real-world thin-film solar cells. The physical contact between electron and hole transport layer at the pinhole leads to non-linear shunting that can decrease the solar cell's fill factor and even drastically reduce its open-circuit voltage. We found an easy-to-apply parallel equivalent circuit model that predicts the impact of an experimentally obtainable shunt characteristic on the solar cell performance. Different charge transport layer combinations result in substantially different shunt currents which are reflected in the degree of performance deterioration – with certain advantageous combinations having a vanishing impact on the solar cell.

For today's novel thin-film solar cells that apply a large variety of contact layers, criteria to evaluate the quality of a contact are needed. We have shown that the current characteristic at pinholes, which is determined by the contact layer configuration, may dictate the solar cell performance. This finding highlights the importance of not only optimizing the contacts with regard to the absorber layer, but to pay equal attention to the contacts' behaviour at pinholes. In other words, it may be that the optimum contact configuration of a pinhole-free thin-film solar cell differs from the optimum contact configuration of a real-world, imperfect thin-film solar cell that contains pinholes. Especially when aiming at up-scaled production of perovskite solar cells, a high tolerance of the contact layer combination against shunting from pinholes is likely to increase fabrication yields and reduce process requirements for the absorber film deposition which will eventually reduce production costs.

Conflicts of interest

There are no conflicts of interest to declare.

Supporting information

Experimental details, mainly on the fabrication of ETL/HTL devices. Description of simulation software PVMOS. Method to remove distributed series resistance of TCO from experimentally recorded ETL/HTL diodes with PVMOS and corresponding results. Lumped element representation of the effective TCO resistance that is added again in a last step to the diode/pinhole parallel equivalent circuit. Validation of equivalent circuit model based on network diode simulations with PVMOS of a mini-cell with randomly distributed nm-sized pinholes.

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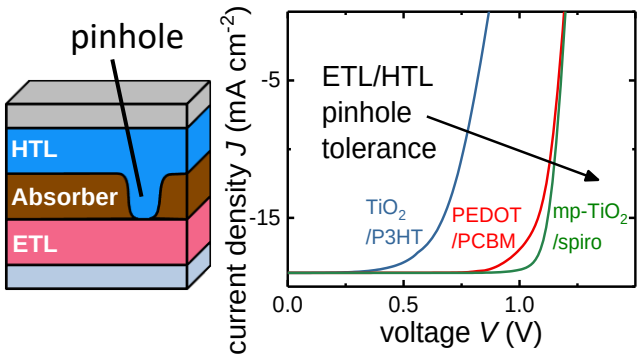
TOC Graphic


pinhole
HTL
Absorber
ETL
current density J (mA cm-2)
-5
-15
ETL/HTL
pinhole
tolerance
TiO2
/P3HT
PEDOT
/PCBM
mp-TiO2
/spiro
0.0
0.5
1.0
voltage V (V)