Active Gate Drive to Increase the Power Capacity of Hard-Switched IGBTs

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***Abstract*—The effect of the gate drive on the power-processing capacity of a hard-switched Insulated Gate Bipolar Transistor (IGBT) in a bridge leg is investigated in this paper. The performance of two Active Gate Drive (AGD) techniques (Variable Ramp (VR) and Push-Pull (PP)) is compared against a conventional two-level (Fast Gate Drive (FGD)) gate drive method. The two proposed techniques reduce the voltage overshoot, which allows the dc-bus voltage to be increased closer to the IGBT voltage rating, improving the utilization of the device's blocking voltage. Consequently, the safe operating area of the IGBT is extended without exceeding the thermal limit of the device (limited by maximum junction temperature). An experimental method, the first of its kind in the literature, is developed to determine whether using these active gate drives can lead to an increase in the power that the IGBT can process. The study reveals that the PP-AGD technique can increase the IGBT power throughput by approximately 5%-8% across a range of switching frequencies. This better IGBT utilization allows a given device to process more power or may allow the designer to choose lower-power rated devices potentially leading to higher converter power density.**

I. Introduction

As power electronic converters become pervasive in consumer, industrial, and grid applications, the need for greater efficiency, power density, and reliability drives innovation across all aspects of system design. Power density is determined by several components, including the semicondutor devices, passive components, and heatsinks. [1]. Maximum power density is achieved through operating each component at its full capacity, i.e. under-utilized components should either be resized or the power throughput should be increased [2]. The focus of this paper is on maximising the utilization of the semiconductor switch by using an Active Gate Drive (AGD) technique.

The switching behaviour of power transistors such as Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and Insulated Gate Bipolar Transistors (IGBTs) can be controlled, to an extent, by the gate drive circuit. Conventionally, such control has been limited to selection of the resistors in the gate current path, for example in [3] an analytical model is used to evaluate IGBT switching performance for different turn-on and turn-off gate resistances. Such added resistance acts to limit the charge/discharge rate of the capacitive gate of the device and control the switching speed. Since the gate resistance is fixed, at the design or commissioning stage it must be chosen to ensure that criteria relating to the switching behaviour, such as slew rates and peak voltage limits, are satisfied across the full operating range of the converter. For instance, the highly non-linear Miller capacitance between gate and drain/collector leads to the $\mathrm{d}v/\mathrm{d}t$ being largest when operating at the maximum dc-bus voltage, and a gate resistor conservatively sized to satisfy a $\mathrm{d}v/\mathrm{d}t$ limit at this operating point will lead to slower slew rates at lower dc-bus voltages, leading to unnecessary additional switching loss [4].

Over the last twenty years, several AGD concepts have been proposed to improve power transistor switching behaviour. Early research in the 1990s enabled current balancing of paralleled IGBT modules through the use of closed-loop control of gate voltage [5], [6], a concept which was later developed in [7]. Similarly, control of $\mathrm{d}v/\mathrm{d}t$ using feedback of IGBT collector voltage [8]–[11] has been developed to obtain desired collector-emitter voltage slew-rates, which allows series connection of IGBTs through voltage-balancing without the use of external snubber circuits.

More generally, the AGDs proposed in the literature address the challenging task of controlling the switching trajectory to reduce the switching energy loss, while at the same time managing electromagnetic interference (EMI) issues and reducing the stress applied to the semiconductor devices (such as peak voltage stress induced by $\mathrm{d}i/\mathrm{d}t$ across parasitic inductance in the commutation current path). Additionally, overcurrent and overvoltage protection can be implemented in the gate drive. The research can be divided into open-loop methods [12]–[20] which operate without feedback of the switching behaviour, and closed-loop methods where measurements are fed back to modify the control signal [21]–[27].

A high-speed open-loop active gate drive in [12] uses a selectable number of drive transistors to shape the switching trajectory of a GaN FET to reduce overshoot and EMI. Another open-loop approach limits the maximum $\mathrm{d}v/\mathrm{d}t$ of a SiC MOSFET [13], while in [14] a Laplace-domain switching model of a SiC MOSFET is used to derive gate drive parameters (resistance, drive voltage levels, external gate-source capacitance). In several studies the switching transient is divided into four periods, and different gate drive strengths are applied during each period. The duration of each period is either manually set [15] or dynamically updated based on stage-detection circuitry [16]–[19]. Open-loop control is shown to be effective for some changes in operating conditions through the use of a look-up table that contains pre-determined information about the gate control for each operating condition [20].

A closed-loop approach is required to closely track the

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desired switching behaviour without using a look-up table as the operating conditions change. Analogue feedback of $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ with P or PI control has been used to obtain particular slew rates across a range of load currents for several IGBT modules [21]–[26]. Independent control of $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ is demonstrated with optically-triggered MOSFETs in [27]. Gate-assist circuits are connected based on the voltage drop across the Kelvin inductance in [28] to increase the $\mathrm{d}v/\mathrm{d}t$ and reduce delay time, while the current slew rate is unaffected and is still controlled by the gate resistor.

Closed-loop control in fast switching transients requires high control loop bandwidth. This is a particular challenge for digital implementations where ADC and DAC latency may combine to produce input-to-output delay in the control loop of approximately 30 ns, even with fast ∼1 GS/s ADC/DACs [29]. In the case of SiC devices, where the switching times are in the order of tens of nanoseconds [15], this latency makes the digital closed-loop control extremely challenging. An alternative is the 'iterative control' or 'sequential optimization' that has been widely investigated [29]–[38]. In this scheme, measurements of the previous switching edge are used to modify the gate control of subsequent switching transitions. In [32]–[35] an IC with multiple drive current strengths is used to improve the trade-off between voltage overshoot and switching energy loss. The gate current profile is iteratively adapted in [37] to constrain the maximum $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}^2v/\mathrm{d}t^2$ to reduce EMI, while gate current profile adaptation can also be applied to reduce EMI in low-voltage contexts such as the 1.2 V 1.8 MHz converter in [39].

An intriguing possibility raised by these technologies is an increase in the capacity of the semiconductor switch by managing the voltage overshoot, and therefore allowing the dc-bus voltage to be increased closer to the rated maximum voltage of the switch. Due to the inherent trade-off between switching loss and voltage overshoot, it does not automatically follow that a reduction in voltage overshoot will lead to increased switch power capacity. Figure 1 illustrates three gate drive waveforms which are compared in this paper: (a) a conventional two-level (Fast Gate Drive (FGD)) waveform, (b) a Variable Ramp (VR) AGD waveform, and (c) a Push-Pull (PP) AGD waveform. More detail about the design of the gate drive waveforms is given in Section III-B. To compare these gate drive waveforms, it is necessary to develop a framework to evaluate their impact on switch capacity. This paper presents such a framework, and is to the authors' best knowledge the first to develop this method. It is shown by experiment that the PP waveform increases IGBT capacity by 5%-8% compared to the FGD and VR waveforms. It should be emphasized that this paper does not present control of switching behaviour beyond what is already published in the literature cited above. Rather, the contribution is to demonstrate that such control can increase the maximum amount of power that a switch can process.

Section II introduces the analysis which leads to the hypothesis that switch capacity can be increased by using AGDs under certain conditions. Section III presents the experimental methodology, followed by the results in Section IV. The significance of the findings is discussed in Section V.

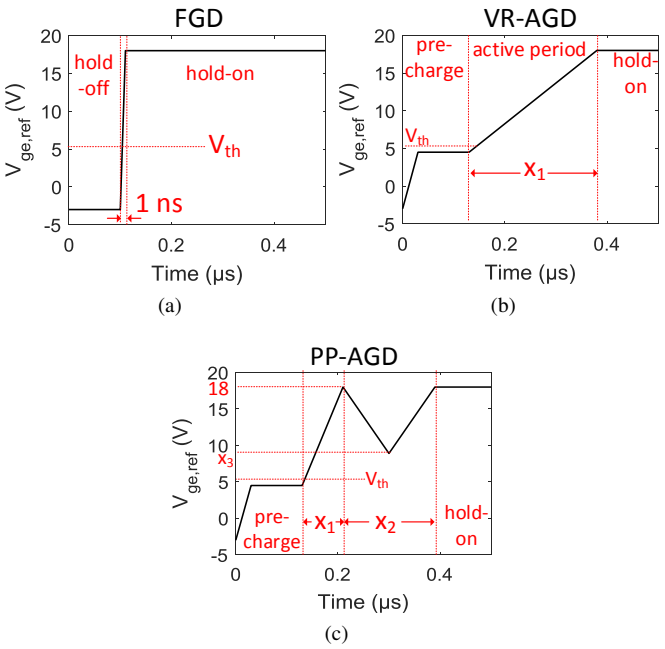


Fig. 1. Example AGD gate voltage references for turn-on with (a) *FGD*, (b) *VR-AGD*, and (c) *PP-AGD*. Parameter **x** is defined in Section III-B.

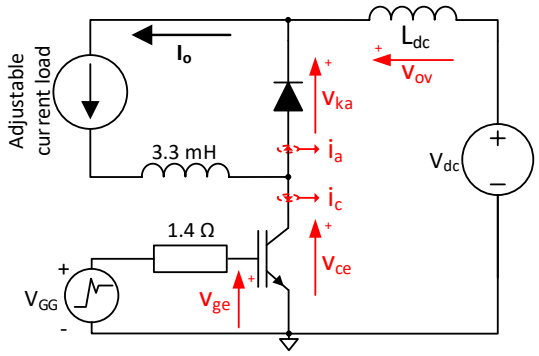


Fig. 2. Converter used in this study, with independent control of load current and dc-bus voltage.

II. Definition of Switch Capacity

The capacity of a switch is defined here as the maximum apparent power S it can process, i.e. the product of the voltage it can block when turned off and the conducted current when turned on. Considering a bridge-leg consisting of two devices in a totem-pole, for example in the buck converter shown in Fig. 2, the blocked voltage is the dc-bus voltage and the conducted current equals the output current, giving

$$S = V_{\mathrm{dc}} I_{\mathrm{o}}\,. \tag{1}$$

Here, L_{dc} is a lumped representation of parasitic inductances in the power loop which cause the voltage overshoot during switching due to $\mathrm{d}i/\mathrm{d}t$. The dc-bus voltage plus this transient voltage overshoot must be less than or equal to the rated blocking voltage of the switch:

$$V_{\mathrm{dc}} + V_{\mathrm{ov}} \leq V_{\mathrm{CE(max)}}. \tag{2}$$

where V_{ov} is the maximum transient voltage overshoot and $V_{\mathrm{CE(max)}}$ is the rated voltage of the switch.

The conducted current is limited by the allowable power loss of the switch, which can be expressed as the sum of conduction and switching loss for an IGBT as

$$\begin{aligned} P_{\text{loss}} &= P_{\text{c}} + P_{\text{sw}} \\ &= D I_{\text{o}} V_{\text{CE(on)}}(T, I_{\text{o}}) \\ &\quad + f_{\text{sw}} F(I_{\text{o}}, V_{\text{dc}}, T, \text{gate drive}, \dots) \end{aligned} \tag{3}$$

where

$V_{\text{CE(on)}}$	on-state collector-emitter voltage of the IGBT
T	junction temperature of the switch
D	duty cycle of the switch
f_{sw}	switching frequency
$F()$	an unknown function mapping switching energy loss to load current, dc-bus voltage, and other factors such as device physics, circuit layout, gate drive etc.

The form of the function *F*() is unknown, but the value of *F*() can be obtained during switching operation as the switching energy loss, calculated from the measured collector current and collector-emitter voltage waveforms as:

$$\begin{aligned} F() = E_{\text{sw}} &= E_{\text{on}} + E_{\text{off}} \\ &= \int_{t_1}^{t_2} v_{ce} i_c . \text{d}t + \int_{t_3}^{t_4} v_{ce} i_c . \text{d}t \end{aligned} \tag{4}$$

where t_1, t_2 and t_3, t_4 are respectively the start and end times of the turn-on and turn-off switching event, and v_{ce} and i_c are respectively the switch's collector-emitter voltage and collector current [40].

The form of *F*() in (3) is presented in this section to highlight the dependence of switching energy loss on load current, dc-bus voltage, and gate drive. Later in the work, the form of (4) is used when measurable values of E_{sw} are being discussed.

The maximum power loss is set by the junction temperature limit of the device

$$P_{\text{loss}}^{\text{max}} = \frac{T_j^{\text{limit}} - T_a}{R_{ja}} . \tag{5}$$

where

T_j^{max}	junction temperature limit
T_a	ambient temperature
R_{ja}	junction-ambient thermal resistance.

Rearranging (1)-(3), the maximum switch apparent power can be expressed as

$$S^{\text{max}} = \frac{(V_{\text{CE(max)}} - V_{\text{ov}})(P_{\text{loss}}^{\text{max}} - f_{\text{sw}} F(I_o, V_{\text{dc}}, \text{gate drive}, \dots))}{D V_{(\text{CE,on})}(T, I_o)} . \tag{6}$$

From (6), the switch apparent power can be increased by:

1) Using devices with a higher voltage rating - *allows higher dc-bus voltage*
2) Reducing the voltage overshoot occurring during switching - *allows higher dc-bus voltage*
3) Using devices with a smaller on-state voltage drop - *increases device current carrying capacity*
4) Reducing the junction to ambient thermal resistance - *increases device current carrying capacity*
5) Reducing the switching losses (e.g. by reducing the switching frequency or using lower gate resistance) - *increases device current carrying capacity*

However, each action has a penalty: 1) higher voltage devices have larger channel resistance or on-state voltage drop (per unit area), 3) lower conduction loss devices have higher switching loss due to higher output capacitance [2], 4) the size of the heatsink may be restricted, 5) lower switching frequency increases the size of passive components. There is a direct trade-off between 2) and 5) since lower gate resistance reduces switching loss but increases the voltage overshoot. This paper considers what could be gained from implementing point 2 by using an AGD, i.e. effectively increasing the switch capacity, without changing the switching device itself or other characteristics of the power converter.

The AGDs presented in the literature are able to reduce the voltage overshoot occurring during switching, however it is shown that this leads to increased switching loss [41]. Therefore, for a given switch rating in a power converter, it is expected that the use of AGDs would enable a higher output voltage due to reduced voltage overshoot, but also that the thermally-limited maximum output current would reduce as a result of increased switching losses.

There are two factors that contribute to the increase of switching loss at higher dc-bus voltages:

1) Simply increasing the dc-bus voltage causes switching losses to increase, since the product of drain current and drain-source voltage at any instant during switching is larger. This is the case even if the gate drive remains unchanged.
2) If the gate drive is an AGD which slows down the switching as the dc-bus voltage approaches the device voltage limit (in order to reduce the voltage overshoot), then the drain current and drain-source voltage overlap for longer, leading to a further increase in the switching energy loss.

Equation (6) shows that an AGD has potential to increase utilization of the switch if it enables an increase in dc-bus voltage great enough to counteract the increase in switching energy loss. In other words, the trade-off between the increased dc-bus voltage and the higher switching loss is investigated in terms of the switch capacity. Since $F()$ is a complicated function dependent on many variables, an experimental approach is used here to investigate the impact of AGD on switch capacity across a range of switching frequencies. As switching loss is proportional to switching frequency, the hypothesis is that there will be a critical switching frequency below which the AGD will increase the capacity of the switch compared to a conventional gate drive.

III. Experimental methodology

A. Power circuit topology and hardware

Switch capacity is investigated using the diode-clamped IGBT switching circuit shown in Fig. 2. Independent control of dc-bus voltage and load current is achieved by using an adjustable power supply to support the dc-bus and an electronic load in constant-current mode as the load. A 600 V, 25 A IGBT

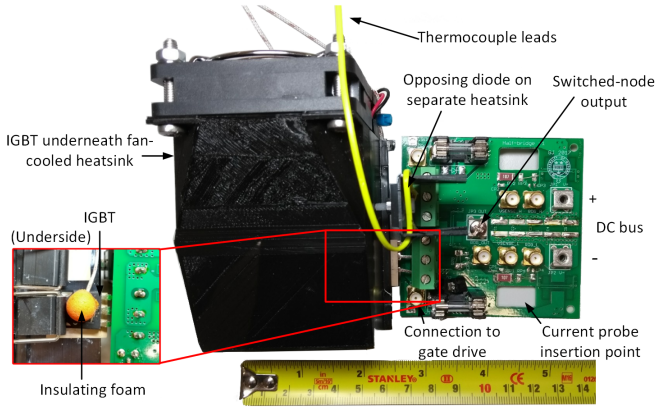


Fig. 3. Half-bridge circuit board, with separate heat-sinks for IGBT and opposing diode. Inset shows back-view of IGBT with thermocouple and insulating foam (explanation in Section III-E). Not shown are 2x 330 nF polypropylene capacitors on board underside.

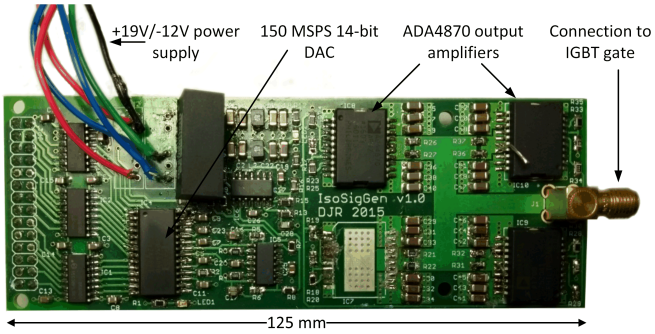


Fig. 4. Gate drive printed circuit board providing digital to analogue conversion and amplification. This same hardware is used to produce all the waveforms in Fig. 1.

(IRG4PC40KDPbF) and freewheeling diode ISL9R3060G2 are used for verification. Both are discrete devices in the TO247 package. The converter is run at a constant duty cycle of 0.3 throughout the experiment. The 0.3 ratio is selected because it corresponds to the maximum power capability (3 kW) of the external power supply which is delivering power to the dc-bus, when the converter is operating at the highest voltage (≈400 V) and load current (25 A).

During a switching event, the collector-emitter voltage of the IGBT, v_{ce}, and the cathode-anode voltage of the diode, v_{ka}, are measured with 300 MHz 100:1 passive voltage probes. A 100 MHz N2783A Keysight current probe measures the IGBT collector current, i_c, and the diode current i_a is inferred from Kirchoff's current law:

$$i_a(t) = I_o - i_c(t) \tag{7}$$

The gate-emitter voltage of the IGBT, v_{ge}, is measured with a 350 MHz 10:1 passive probe, and all signals are sampled at 1.25 GS/s using a 250 MHz-bandwidth oscilloscope (PicoScope PS6402C). All measurement devices are de-skewed before running the experiment. The implementation of the converter is shown in Fig. 3.

B. Gate drive methods

The gate drive unit used in this study is a custom-designed high-bandwidth voltage waveform generator. It allows a variety of drive voltage waveforms to be used to effect turn-on and turn-off of the IGBT. The gate drive is on a stand-alone circuit board, shown in Fig. 4, and connects to the half-bridge board via a 150 mm coaxial cable. Ideally, the gate drive voltage source would be connected to the IGBT gate through zero impedance to obtain direct control of the internal gate voltage. This would allow the gate voltage to be ramped at a controllable rate to tune the switching speed. However, because the gate is capacitive and the gate loop has parasitic inductance, a small series resistance is required to damp this LC oscillator. The gate resistor can be selected to achieve critical damping [42], i.e.

$$R_{g,\text{crit}} = 2\sqrt{\frac{L_g}{C_{\text{iss}}}} \tag{8}$$

where

L_g parasitic inductance of the gate loop
C_{iss} input capacitance of IGBT gate.

The resistance of the gate mesh inside the IGBT also contributes to the damping, allowing the external resistor to have a value smaller than that given by (8). Here, 1.4 Ω is added between the gate drive output and IGBT gate, which is found to obtain a good trade-off between switching speed and ringing. Smaller resistance would allow faster charging of the gate at the expense of increased overshoot and ringing at the gate.

Three gate drive waveforms are studied, as illustrated in Fig. 1. They are produced using the same gate drive hardware, depicted in Fig. 4, operating in different modes. The first gate drive mode (Fig. 1a) switches the IGBT as quickly as possible (so is referred to as the *Fast Gate Drive* or *FGD*, here). For the FGD, the voltage waveform undergoes a step change between the hold-off level of −3 V and the hold-on level of 18 V, and relatively rapid switching results.

The other two modes are AGDs. The AGD gate voltage waveform is represented as a sequence of voltage points generated by MATLAB on a desktop PC. This sequence is defined by a vector $\mathbf{x}$, where Figs. 1b and 1c show the role that each element of $\mathbf{x}$ has in defining the voltage waveform for each AGD case. In both cases, the reference is brought to a plateau below the IGBT threshold before switching in order to pre-charge the gate and make the IGBT sensitive to the upcoming AGD control.

In the first case, Fig. 1b, $\mathbf{x}$ has only one element, which defines the ramp time of the reference signal from pre-charge to hold-on/off level. Hence this case is termed the *Variable-Ramp AGD* or *VR-AGD*. The second case, termed the *Push-Pull AGD* or *PP-AGD* (Fig. 1c), introduces additional degrees of freedom to allow the driver to inject and extract charge from the gate during the switching event. Three variables make up $\mathbf{x}$

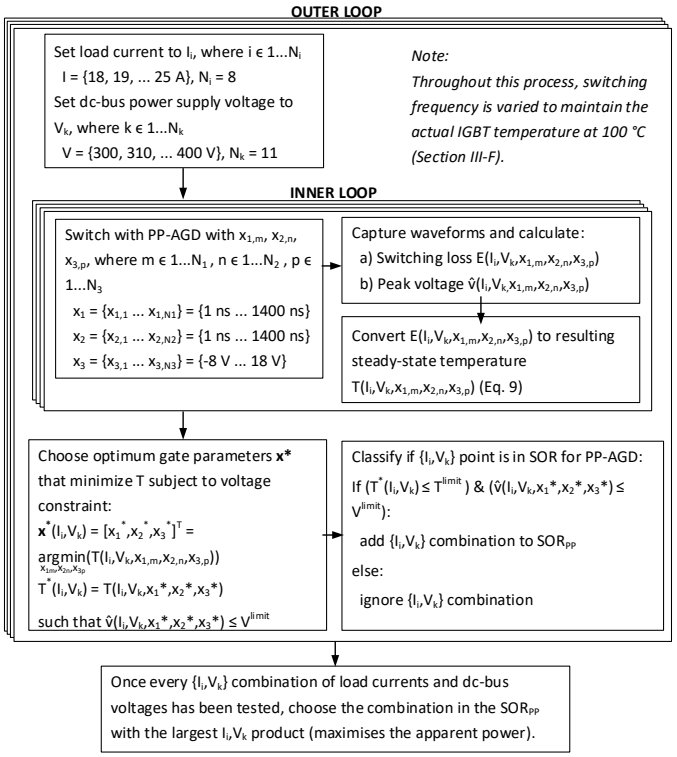


Fig. 5. The method flow for determining the maximum apparent power obtainable using the PP-AGD. All combinations of load current, dc-bus voltage and gate parameters are tested. The methods for the FGD and VR-AGD are identical, except that the VR-AGD only has one gate parameter, and the FGD has no gate parameters.

in this case: the first two variables are times, the third variable is a voltage.

The resulting piecewise linear reference signal is sampled at 256 points, and stored on an FPGA. To initiate switching, the FPGA clocks out the sequence of points to a 14-bit DAC at $150\,\mathrm{MS/s}$, and the output from the DAC is amplified and level-shifted. The output amplifiers (three ADA4870) together provide current buffering up to $3\,\mathrm{A}$ with an output swing of $-10\,\mathrm{V}$ to $18\,\mathrm{V}$. More information about the gate drive hardware is provided in [41].

C. Overview of method

Maximum IGBT capacity is found for each type of gate drive (FGD, VR-AGD and PP-AGD) by taking measurements of switching behaviour across a range of load currents and dc-bus voltages. The load currents tested are $18\,\mathrm{A}$, $19\,\mathrm{A}$ ... $25\,\mathrm{A}$, and the dc-bus voltages tested are $300\,\mathrm{V}$, $310\,\mathrm{V}$ ... $400\,\mathrm{V}$. Every combination of load current and dc-bus voltage is tested.

Figure 5 illustrates the method for the PP-AGD case. Subscript i refers to the load current, subscript k refers to the dc-bus voltage, and $x_{1,m}$, $x_{2,n}$ and $x_{3,p}$ refer to the gate drive parameters of the PP-AGD. Switching waveforms are captured for every combination of I_i, V_k, $x_{1,m}$, $x_{2,n}$, and $x_{3,p}$, and these waveforms are processed to calculate the switching energy loss (from (4)) and peak voltage, denoted $E(I_i,V_k,x_{1,m},x_{2,n},x_{3,p})$ and $\hat{v}(I_i,V_k,x_{1,m},x_{2,n},x_{3,p})$ respectively. Switching loss is converted into the resultant steady-state IGBT junction temperature using (10) as explained later in Section III-E.

For each load current and dc-bus voltage, the best waveform of the AGD is selected by choosing the gate parameters $x_{1,m}$, $x_{2,n}$, and $x_{3,p}$ that minimise the resultant IGBT temperature while also not causing peak voltages to exceed the device limit, i.e.

$$\begin{aligned}\mathbf{x}^*(I_i,V_k) &= [x_1^*,x_2^*,x_3^*]^{\mathrm{T}} \\ &= \arg\min_{x_{1,m},x_{2,n},x_{3,p}} T(I_i,V_k,x_{1,m},x_{2,n},x_{3,p}) \quad (9a)\\ T^*(I_i,V_k) &= T(I_i,V_k,x_1^*,x_2^*,x_3^*) \quad (9b)\\ \text{such that}\quad \hat{v}(I_i,V_k,x_1^*,x_2^*,x_3^*) &\le V^{\mathrm{limit}} \quad (9c)\end{aligned}$$

This leaves, for each I_i, V_k combination, only a single temperature $T^*(I_i,V_k)$ which is the lowest feasible IGBT temperature that the gate drive can obtain. If this temperature is less than the device limit, then the I_i, V_k combination of load current and dc-bus voltage is acceptable. Therefore the combination I_i, V_k is added to the set of acceptable operating points, which is called the *safe operating region* or *SOR* in this paper. However if $T^*(I_i,V_k)$ is above the device limit this means that the gate drive has been unable to produce acceptable switching behaviour at the load current and dc-bus voltage, therefore the I_i, V_k combination is not added to the SOR.

The maximum apparent power $S^{\max}$ is obtained at the point in the SOR whose product of load current and dc-bus voltage is larger than at any other point in the SOR. $S^{\max}$ and the load current and dc-bus voltage combination at which it occurs is saved for the PP-AGD.

The procedure is analogous for the FGD and the VR-AGD, the only difference being that there is only one gate drive parameter for the VR-AGD, and no gate parameters for the FGD. For the FGD, $T(I_i,V_k) = T^*(I_i,V_k)$, and only I_i, V_k combinations that result in both $T(I_i,V_k) \le T^{\mathrm{limit}}$ and $\hat{v}(I_i,V_k) \le V^{\mathrm{limit}}$ get added to the SOR.

At high dc-bus voltages, the SOR is dictated by the devices' rated blocking voltage limit, while at higher load currents the IGBT junction temperature constrains the SOR. The maximum IGBT capacities obtained using the different gate driving methods indicate the potential to increase IGBT capacity by expanding the SOR to higher voltages. It is reasonable to expect that the AGD SOR will be bounded by a higher dc-bus voltage (since AGDs reduce transient voltage overshoot) while the maximum load current boundary will be reduced (since using anything other than the fastest gate drive increases switching energy loss).

The IGBT and diode used in the experiment have a rated blocking voltage of $600\,\mathrm{V}$ and maximum rated junction temperature of $150\,^{\circ}\mathrm{C}$. To allow the SOR to be determined using this procedure, without destroying the devices when the limits are exceeded, the peak diode/IGBT voltage V^{limit} is taken as $430\,\mathrm{V}$ and the maximum junction temperature limit T^{limit} as $100\,^{\circ}\mathrm{C}$ (a $75\,^{\circ}\mathrm{C}$ rise above the ambient of $25\,^{\circ}\mathrm{C}$). Because the switching loss of the IGBT is greater than that of the diode [43], only the thermal constraint on the IGBT is considered in this work.

TABLE I
APPROXIMATE OVERSHOOT ON A DC-BUS OF 400 V FOR TURN-ON AND TURN-OFF WITH THE FGD. TURN-ON OVERSHOOT DOMINATES IN ALL CASES.

		Junction temperature	
		75 °C	100 °C
Load	18 A	On 36 % Off 10 %	On 32 % Off 6 %
	24 A	On 30 % Off 12 %	On 28 % Off 8 %

D. Focus on turn-on control

Voltage overshoot during turn-on has been observed to exceed turn-off overshoot across the range of load currents investigated. Table I displays measured overshoot as a percentage of the 400 V dc-bus for two load currents and junction temperatures, when using FGD. Turn-on behaviour, therefore, has the greater impact on IGBT capacity, and for this reason both PP-AGD and VR-AGD approaches are investigated for turn-on. However experiments indicate that the PP-AGD has limited influence on turn-off behaviour [41], therefore only the VR-AGD is applied to turn-off. It is noted that even though turn-on creates the higher voltage overshoot during FGD switching, it is still useful to apply the VR-AGD to turn-off, since the FGD turn-off can produce a voltage overshoot greater than an optimised PP-AGD turn-on.

E. Electrical measurement of switching loss used as proxy for junction temperature

Each AGD method requires the evaluation (by switching) of many different gate drive waveform shapes in order to find the optimal $\mathbf{x}^*$, as described above, each of which causes a different switching energy loss. Since the thermal time constant of the system is of the order of tens of seconds and several thousand $\mathbf{x}$ need to be evaluated, it is not feasible to directly measure the resulting steady-state junction temperature of the IGBT by allowing the system to reach thermal steady-state for each $\mathbf{x}$. Therefore, the steady-state junction temperature rise that would result from continuous operation at a given $\mathbf{x}$ is instead calculated from the device power loss and the junction-to-ambient thermal resistance as

$$\Delta T_j = P_{\text{loss}} R_{ja} = (P_c + P_{\text{sw}}) R_{ja} \tag{10}$$

where 3.00 °C/W is taken for thermal resistance R_{ja}.

Device conduction loss is calculated (using a similar method as found in [44]) as

$$P_c = D I_o V_{\text{CE(on)}} \,. \tag{11}$$

On-state voltage, a function of junction temperature and load current, is found by quadratic interpolation of the datasheet values. Device switching loss P_{sw} equals $f_{\text{sw}} E_{\text{sw}}$ where the switching energy E_{sw} is calculated using (4).

F. Regulation of device temperature at 100 °C

As switching loss is strongly temperature dependent (increasing with temperature) [4], the IGBT must be kept at 100 °C for all trial $\mathbf{x}$ to allow the boundary of the SOR to be determined. Device power loss varies with V_{dc}, I_o and $\mathbf{x}$, therefore the die temperature is held at 100 °C by varying the switching frequency as illustrated in Fig. 6. A PI controller compensates for changes in temperature that would otherwise occur when V_{dc} or I_o change.

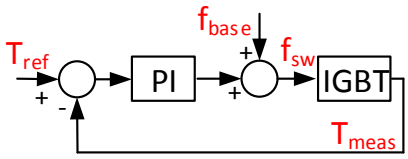


Fig. 6. IGBT temperature under closed-loop control during experiments. T_{ref} is held at temperature limit of 100 °C.

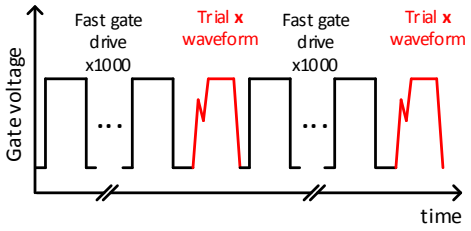
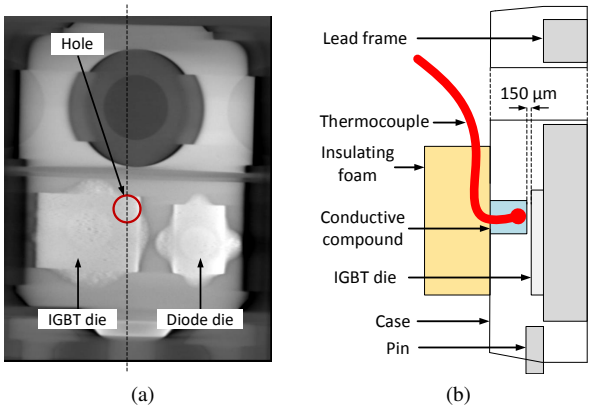


Fig. 7. IGBT gate voltage pulse-train when performing AGD search. Temperature fluctuations are reduced by keeping the majority of switching events constant.

During the AGD grid search of $\mathbf{x}$ at a given V_{dc} and I_o, the average power dissipation is kept almost constant by only having a changing gate parameter vector $\mathbf{x}$ for 1 out of 1000 switching transitions; the remaining switching edges use the constant fast gate drive shape (see Fig. 7). Therefore the actual die temperature is not significantly affected by the rapidly changing trial $\mathbf{x}$, and can be maintained at 100 °C.

To obtain accurate die temperature measurements, a type-T thermocouple is placed 150 µm from the IGBT die. The package has been imaged using x-ray tomography (Fig. 8a) to locate the dies and bond-wires, a 2.2 mm deep, 2 mm diameter hole has been milled above the die, and the thermocouple is fixed in this hole with thermally conductive compound (schematically illustrated in Fig. 8b). Thermally insulating foam is fixed on the case above and around the hole.



(a) (b)

Fig. 8. (a) Slice from an x-ray tomogram showing the silicon dies and the position of the milled hole. (b) Schematic side-view of TO-247 package showing thermocouple position relative to IGBT die.

IV. Results

A. Safe operating regions at 7 kHz

The IGBT steady-state junction temperature across a range of dc-bus voltages and load currents is presented in this section when using the three gate drive techniques. Temperatures are inferred using the ΔT_j from (10) and (4) based on a switching frequency of $7\,\mathrm{kHz}$ and the ambient temperature of $25\,^\circ\mathrm{C}$. Fig. 9 shows the resulting IGBT temperatures plotted against dc-bus voltage, one plot for each type of gate drive. Each load current is plotted as a curve; the temperature limit of $100\,^\circ\mathrm{C}$ is marked with a solid red line. Points with transient voltage overshoot above the limit of $430\,\mathrm{V}$ are joined with a dashed red line, whereas black solid lines connect points with overshoot below $430\,\mathrm{V}$. Note that Fig. 9 contains information about the IGBT power loss (conduction plus switching loss) but loss measurements are transformed into resulting junction temperatures using (10) and (4) since it is the maximum temperature that limits the IGBT power capacity. In other words, the red line marking the limit of $100\,^\circ\mathrm{C}$ indicates a constant IGBT power loss - in this case

$$\frac{100\,^\circ\mathrm{C} - 25\,^\circ\mathrm{C}}{3.00\,^\circ\mathrm{C/W}} = 25\,\mathrm{W} \tag{12}$$

The SOR for the FGD, Fig. 9a, is constrained by the voltage limit and the temperature limit. Large voltage peaks during switching limit the dc-bus voltage to less than $350\,\mathrm{V}$, while the maximum load current is $22\,\mathrm{A}$. The switch capacity in this case, obtained by operating at the maximum apparent power point marked by the green star, is $S = V_{dc}I_o = (334\,\mathrm{V})\,(22\,\mathrm{A}) = 7.35$ kVA.

For the VR-AGD, Fig. 9b, the voltage limit is respected at all points by slowing down the switching events. However, the penalty is larger switching loss leading to higher calculated steady-state die temperature. As a result, the point of maximum power is the same as for the FGD.

Fig. 9c reveals that the PP-AGD can, like the VR-AGD, respect the voltage limit all the way up to a $410\,\mathrm{V}$ dc-bus. However, the PP-AGD does this with less of an increase in switching loss, compared to the VR-AGD. This means the point of maximum apparent power is shifted to $396\,\mathrm{V}$, $20\,\mathrm{A}$, giving $S = 7.92$ kVA, an 8% increase in switch capacity compared to the other gate drives. This is due to the shape of the gate control reference allowing relatively fast switching without creating high transient voltages. The comparative performance of the gate drives at $7\,\mathrm{kHz}$ and $T_j = 100\,^\circ\mathrm{C}$ is summarised in Table II. The measured switching loss during turn-on is higher for the PP-AGD than for the FGD or VR-AGD since the *total* power loss is the same in all cases ($25\,\mathrm{W}$) and the conduction losses are lower for the PP-AGD maximum power point since it is at $20\,\mathrm{A}$ as opposed to $22\,\mathrm{A}$.

B. Switch capacity at different switching frequencies

The results can be generalised over a range of switching frequencies. At each frequency, the SOR is calculated using (10) and (4) in the same way as in Section IV-A, and the maximum apparent power is found. The switch capacity across a range of frequencies is shown in Fig. 10 for the three gate drive cases. The power drops as switching frequency increases due to the IGBT junction temperature limit.

In the 4-$8\,\mathrm{kHz}$ range, the PP-AGD enables higher power for the reasons discussed above. At higher switching frequencies the increased losses from the AGD become more significant and the apparent powers begin to converge, as predicted by (6). The AGDs always perform at least as well as the FGD: at frequencies above $10\,\mathrm{kHz}$ the AGD waveforms resemble the FGD waveform, resulting in the same switching behaviour - the AGDs never perform worse than the FGD.

It should be noted that the range of frequencies for which the PP-AGD outperforms the FGD depends on the thermal resistance between device and ambient, since it is the device temperature rise that limits the maximum load current when using PP-AGD at higher switching frequencies. Therefore, with lower thermal resistance the increased loss of the PP-AGD begins to dominate only at higher switching frequencies. For example, if the temperature rises are calculated using (10) with a thermal resistance of $2.00\,^\circ\mathrm{C/W}$ instead of $3.00\,^\circ\mathrm{C/W}$ the PP-AGD and FGD apparent powers converge at a switching frequency of approximately $19\,\mathrm{kHz}$.

There is no switch capacity increase from using the VR-AGD: the peak apparent power from using it is never greater than that of the FGD. This is because, at the maximum-power point, the VR-AGD always ramps the gate reference as rapidly as the FGD, and therefore produces the same switching behaviour as the FGD. In other words, the FGD can be thought of as a special (fastest) case of the VR-AGD.

C. Switching waveforms

This section presents waveforms captured during switching events to illustrate the action of the three gate drives. Fig. 11a shows the turn-on behaviour of the circuit when operating with the FGD at the maximum power point identified from Fig. 9a ($334\,\mathrm{V}$, $22\,\mathrm{A}$). IGBT gate voltage (reference and measured), measured collector-emitter voltage, and measured collector current are shown. In addition, the opposing diode cathode-anode voltage is shown, since the diode experiences the transient voltage peak during turn-on. It can be seen that the voltage peak across the diode is within the $430\,\mathrm{V}$ limit, since the dc-bus voltage is relatively low. The lowest plot in Fig. 11a shows the instantaneous power dissipation and cumulative energy dissipation in the IGBT. The turn-on loss is low at $0.57\,\mathrm{mJ}$.

The corresponding switching waveforms for the VR-AGD at its maximum power operating point are the same as for the FGD, as discussed above, so are not shown. Instead, the the VR-AGD turn-on waveforms (Fig. 11b) are shown at the maximum power point of the PP-AGD ($396\,\mathrm{V}$, $20\,\mathrm{A}$), for comparison against the PP-AGD waveforms (Fig. 11c). This is *not* the VR-AGD's maximum power operating point: it is outside its SOR. The rate of collector current increase is slower for the VR-AGD than for the PP-AGD. This has a two-fold effect on the switching loss: it takes longer for the diode to become reverse biased and allow the collector-emitter voltage to fall (longer switching time); and the collector-emitter voltage is depressed less by the voltage drop across the parasitic

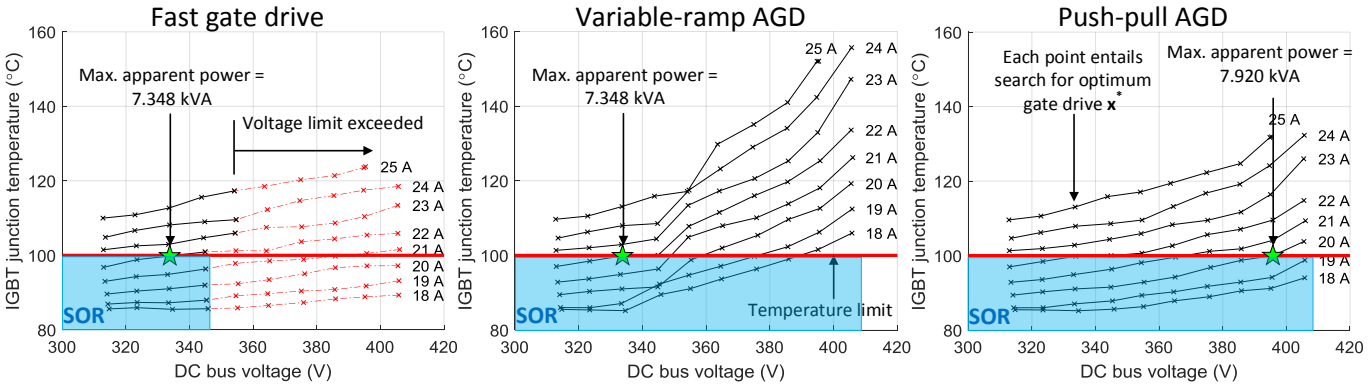


Fig. 9. IGBT junction temperature rise across operating point range, when switching with (a) FGD, (b) VR-AGD, and (c) PP-AGD. Solid lines join points with voltage peaks less than the limit of 430 V, dashed lines indicate unsafe area with voltage overshoot greater than the limit. The green star marks the point in the SOR at which the apparent power is maximised.

TABLE II
COMPARISON OF GATE DRIVES AT 7 kHz

	E_{on} (mJ)	V_{dc} (V)	I_o (A)	P_A (kVA)	P_A (%)	x_1 (ns)	x_2 (ns)	x_3 (V)
FGD & VR-AGD	0.57	334	22	7.35	100 %	1 (min. limit)	–	–
PP-AGD	0.76	396	20	7.92	108 %	61	290	7.4

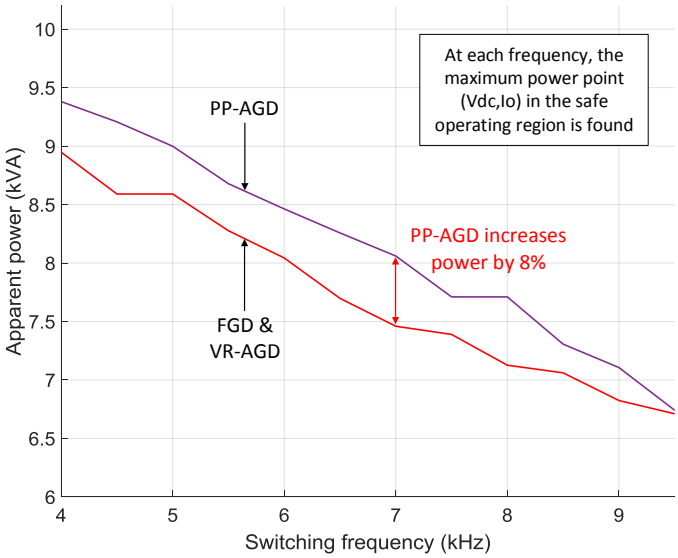


Fig. 10. Maximum apparent power for the three gate drive cases across a range of frequencies. At each frequency, the dc-bus voltage / load current combination that leads to the highest apparent power is chosen from the SOR.

inductance of the commutation path. Both factors lead to 1.5 mJ of switching loss, which causes the unacceptably high calculated junction temperature for the VR-AGD. The PP-AGD, in contrast, reduces voltage overshoot while achieving a lower switching loss of 0.76 mJ. The PP-AGD's extra degrees of freedom allow independent control of the collector current rise and the decay of the diode reverse recovery current. This means that the collector current can increase rapidly at first (reducing switching loss) and the peak $\mathrm{d}i/\mathrm{d}t$ when the reverse recovery current decays can be reduced (creating smaller voltage overshoot).

V. DISCUSSION

The AGD techniques investigated in this paper, compared with gate drives that switch as fast as possible, can reduce the peak voltage across the power devices and allow the converter to be operated at higher dc-bus voltages. However, only the more advanced AGD, the PP-AGD, is found to increase the switch power handling capability. On the other hand, the simpler VR-AGD results in higher switching losses which limit the switch power capacity. The VR-AGD is similar to a gate drive where the rate of gate charge/discharge is controlled by a series gate resistance that is varied between, but not during, the switching events. These results indicate that a variable gate resistance alone has limited utility, and cannot increase switch capacity. The better performance of the PP-AGD suggests that there is merit in a more advanced gate drive compared to the simpler option of implementing an adjustable gate resistance.

It should be recognized that the PP-AGD formulation of the gate drive is not necessarily the best possible, and there may be more complex gate waveforms that achieve greater performance improvements. The PP-AGD as presented here was chosen as a good trade-off between complexity (number of parameters to tune, i.e. experiment run-time) and control over switching behaviour. The theory here has been validated for a single device in a particular converter layout. It is expected that the benefits of AGD will be greater for layouts with large parasitic inductance between dc-link capacitors and the power switches. Conversely, careful power circuit layout may be sufficient to reduce the problem of overshoot without using AGD.

The procedure for finding the best reference waveform during operation is not considered in this paper. The exhaustive search for $\mathbf{x}^*$ conducted here results in switching voltage

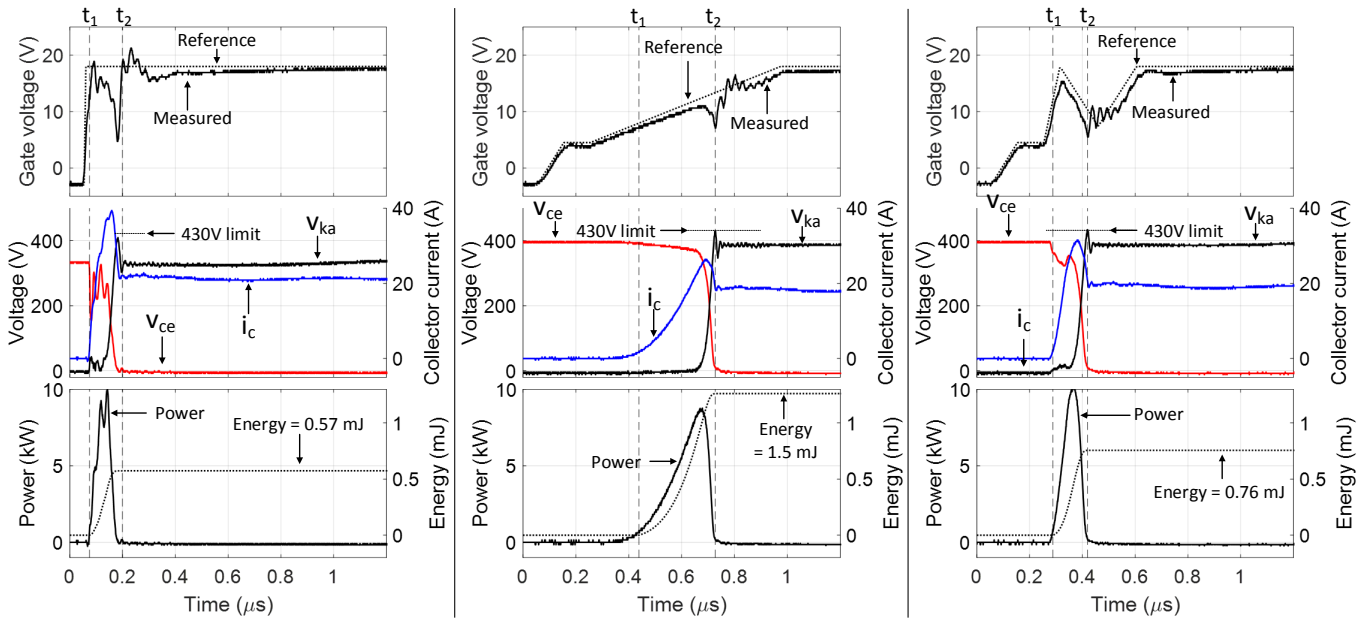


Fig. 11. Turn-on waveforms when switching with the three gate drives. (a) FGD at 334 V 22 A, (b) VR-AGD at 396 V 20 A, and (c) PP-AGD at 396 V 20 A. Plots (a) and (c) are at the respective maximum apparent power operating points for those gate drives, and illustrate acceptable switching behaviour. Plot (b) illustrates the VR-AGD keeping voltage overshoot below the 430 V limit but incurring a high switching loss.

overshoot that sometimes exceeds the device limit, and it is only the choice of a conservative limit that makes this approach possible. It is necessary in practical systems to search in a way that does not violate the peak voltage constraint.

The exact moment when the load current commutates between the switching devices depends on the variable $\mathbf{x}$. Therefore, for synchronous switching the deadtime between the 'on' PWM signals for two devices in a leg may need to be increased to guarantee the absence of shoot-through for all $\mathbf{x}$. Use of an adaptive deadtime mechanism such as that proposed in [36] could address this. Similarly, the duty cycle of the switched device will vary slightly with $\mathbf{x}$ as the instant of switching changes. However, the effect of this is small: the maximum variation in on-time observed during experiments is less than 1 µs, causing duty cycle to vary by less than 1 % when switching at 10 kHz.

The advantage of the improved switch capacity becomes apparent when considering converters with a transformer at the output, for example the three-phase grid-tied inverter depicted in Fig. 12. The transformer provides a degree of freedom to optimally match V_{dc} to grid voltage V_{LL} at the design stage by selecting the appropriate turns ratio n. AGD allows higher V_{dc} and therefore lower n, reducing nI_o and allowing higher output power for a given three-phase bridge.

Therefore, the AGD can be thought of as providing 'free silicon' by increasing the capacity of a given switch, meaning either more power can be processed by the same device, or a smaller device can be chosen to process a particular power level. The better switch utilization may imply higher converter power density if the power semiconductor devices and their heatsinks significantly contribute to the overall volume of the converter. This would have to be factored against the additional volume and weight of the AGD hardware compared to a conventional gate drive.

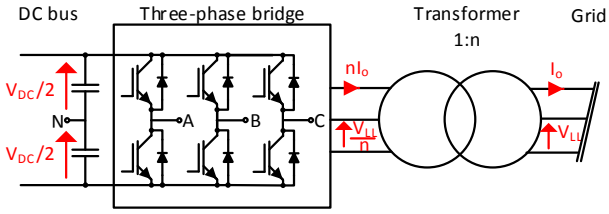


Fig. 12. A grid-tied three-phase inverter, where turns ratio n allows matching of dc-bus voltage to grid voltage.

VI. Conclusion

This paper proposes the first framework for evaluating the impact of an active gate drive on the power processing capability of an IGBT. The power capacity of the device is experimentally shown to increase by up to 8% at frequencies between 4 and 8 kHz (Fig. 10) when using the PP-AGD in a buck converter. The AGD method enables operation of a given converter at maximal dc-link voltages by limiting the voltage overshoot and enlarging the safe operating area of the device (Figs. 9 and 11). Consequently, the application of AGD may result in increased power density of power electronic systems.

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