Mechanical deformation of polycrystalline silicon for solar cell production

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Abstract

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This thesis presents a feasibility study for producing silicon sheet for photovoltaic applications via traditional hot deformation in clean conditions using high purity materials.
A special deformation rig has been designed and constructed for the compression tests. The cleanliness of the deformation conditions has been characterized and determined to be at a satisfactory level.
Deformation of Czochralski, dislocation-free, single crystalline silicon along the < 100 > axis has been conducted to determine a suitable and achievable deformation condition. It has been found that single crystalline silicon can be uniaxially compressed by 30 % without severe cracking at temperatures above 1050 ˚C using a low average strain rate of ~10^{-5} s^{-1}, the most uniform deformed microstructure has been obtained using an average stain rate of 1.67 x 10^{-5} s^{-1}. A dislocation density of order 10^{13} m^{-2} has been revealed by etch pit counting in an SEM. Dislocations with ½ < $1\bar{1}0$ > screw characters have been found using the TEM diffraction contrast technique. The most favourable post-annealing temperature has been determined to be 1400 ˚C.
High purity polycrystalline, chemical vapor deposition (CVD) grown silicon has been successfully deformed at 1150 °C by 10 % at an average strain rate of 6.94 x 10^{-6} s^{-1}. The as-received material has been found to have a strong < 110 > fiber texture as revealed by EBSD. Recrystallization occurs during pre-annealing at 1400 °C for 30minutes. Approximately 90 % of the material recrystallizes with a complete disappearance of the fiber texture. Stacking faults have been mainly observed in the recrystallized material by TEM. It has been observed that the deformed polycrystalline material develops a second recrystallization texture when subjected to post-annealing at 1400 °C for 15 min, resulting in large grains up to several hundred microns in size and a low dislocation concentration of 5 x 10^{10} m^{-2}.
The HR-EBSD cross-correlation method has been employed to quantitatively investigate the GND density distribution in polycrystalline silicon. It has been found that the as-received material has a GND concentration up to 10^{15} m^{-2} and recrystallization during pre-annealing reduces the value to 10^{13} m^{-2}.
The minority carrier lifetime of the polycrystalline sample deformed at 1150 °C by 10 % followed by subsequent annealing at 1400 °C for 120 min has been measured using the QSS-PC method. A value of 1.9 µs at an injection level of 1 x 10^{12} cm^{-3} has been obtained, which corresponds to a minority carrier diffusion length of approximately 100 µm for electrons and 50 µm for holes. H-passivation has been found to be effective in improving the measured minority carrier lifetime.
The results presented in this thesis suggest that producing silicon sheets for photovoltaic applications by conventional hot-deformation may be possible and should be a topic for further investigation.

Preface

This doctorial thesis is an account of the work carried out by the author in the Department of Materials, University of Oxford, between October 2009 and August 2014 under the supervision of Prof. P. R. Wilshaw and Prof. J. D. Murphy. All the work is original. No part of this thesis has been submitted or accepted for any other degree at this university or elsewhere.

Part of this work has been presented in the following conferences:

The 6th International Workshop on Crystalline Silicon for Solar Cells, October 8-11, 2012, Aix-les-bains, France

Min Wu, J. D. Murphy, Laurie Walton, P. R. Wilshaw: **Investigation of the high temperature deformed and annealed polycrystalline silicon**

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Min Wu, J. D. Murphy, P. R. Wilshaw: **The electrical properties of heavily deformed and annealed polycrystalline silicon**

GADEST 2013, Oxford, September 22-27, 2013

Min Wu, Laurie Walton, J. D. Murphy, Peter Wilshaw: **The electrical properties and microstructures of high temperature deformed and annealed polycrystalline silicon**

The 7th International Workshop on Crystalline Silicon for Solar Cells, October 22-25, 2013, Fukuoka, JAPAN
Min Wu, J. D. Murphy, Laurie Walton, P. R. Wilshaw: **The electrical properties and microstructures of high temperature deformed and annealed polycrystalline silicon**

EBSD 2014, Imperial College London, London, 31st March-1st April, 2014

Min Wu, Jun Jiang, Angus J Wilkinson, John Murphy, Peter Wilshaw: **The microstructure and geometrically necessary dislocation (GND) density evolution of high temperature deformed and annealed polycrystalline silicon by high resolution EBSD**

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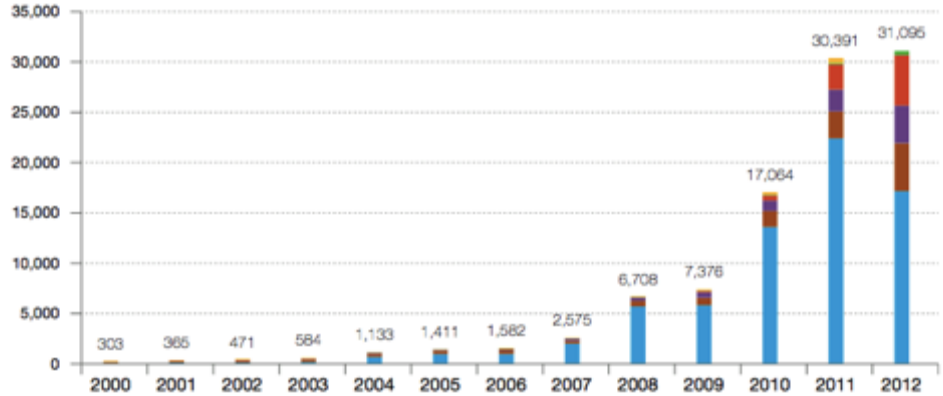
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Chapter 1

Introduction and literature review

1.1 Background

As a fast growing market, the photovoltaic (PV) industry features an average annual increase of more than 48 % solar cell installation in the period from 2000 to 2012 [1], even during a difficult economic period. The end-market demand in photovoltaic industry has reached an unprecedented 9 GW in the 3rd quarter of 2013 globally and the market research forecasts a total 45 GW ~ 55 GW annual demand in 2014 [2]. Figure 1.1 shows the global PV annual installation evolution during the period of 2000 ~ 2012.



	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
ROW	88	56	80	77	29	10	105	42	76	80	284	508	-*
MEA	n/a	n/a	n/a	n/a	1	n/a	n/a	1	1	22	46	121	410
China	19	5	19	10	10	8	10	20	40	160	500	2,500	5,000
Americas	24	32	47	66	104	106	150	213	346	543	1,029	2,179	3,758
APAC	117	140	191	230	282	303	324	271	535	742	1,583	2,672	4,769
Europe	56	133	135	202	707	984	992	2,028	5,710	5,830	13,622	22,411	17,159
Total	**303**	**365**	**471**	**584**	**1,133**	**1,411**	**1,582**	**2,575**	**6,708**	**7,376**	**17,064**	**30,391**	**31,095**

Figure 1.1. Evolution of global PV annual installations 2000-2012 (MW) [2].

Among all types of solar cells, crystalline silicon photovoltaic cells, with over 60 years of development, have the longest production history and now are used in the largest quantity, comprising up to 86 % of the world solar cell production share in 2012 [1][3]. The advantages of silicon are the mature processing technology, the large abundance in the crust of the earth and the non-toxicity which is an important consideration from the environmental perspective, also the stability leading to long in-service lifetimes for completed cells. Silicon solar cell modules are expected to play a prominent role in the future PV market. The PV cell is essentially a diode with a semiconductor structure as shown in Figure 1.2.

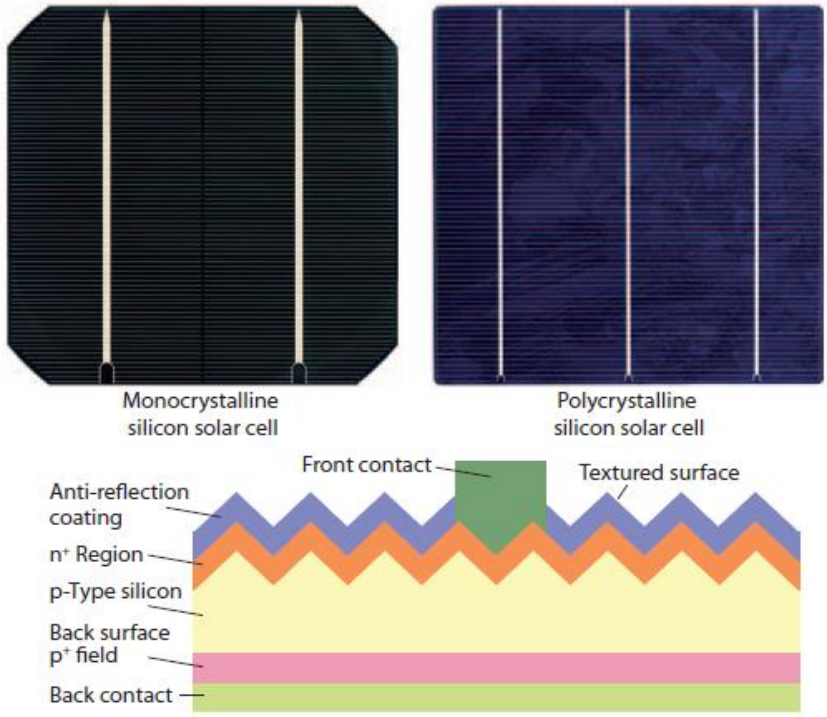


Figure 1.2. Representative single crystalline and multicrystalline silicon solar cells (upper), and simplified cross-section of a type of commercial single crystalline silicon solar cell (lower) [4].

Multicrystalline and polycrystalline silicon ingots and wafers were developed aiming at reducing the production costs as compared to single crystalline material. Modern

polycrystalline furnaces are designed for maximum productivity, casting ingots of around 450 kg. Standard multicrystalline industrial cells typically offer efficiencies in the range of 12 ~ 17 % (as of 2012), and most commercially available single crystalline silicon solar cells now have efficiencies of 18 ~ 20 % [4]. The efficiencies of both single crystalline and multicrystalline PV cells will be enhanced in the future through the introduction of high-efficiency structures or improved materials. Polycrystalline substrates are subject to higher rates of minority carrier recombination, both at active grain boundaries and within crystalline grains due to high dislocation and impurity densities in comparison with float zone (FZ) or Czochralski (Cz) single crystalline substrates.

1.2 Fabrication technology for silicon thin wafer generation

Currently more than 80 % of crystalline silicon solar cell production involves melting polycrystalline feedstock silicon material [5], then growing crystals into large ingots which are subsequently sliced into thin wafers. This manufacturing process is time consuming and generally results in the material loss, as ‘saw-dust’, of around 50 % of the expensive cast silicon material [3]. Cutting the cost of producing expensive high-purity crystalline silicon substrates is one aspect of reducing the cost of silicon solar cell modules. The sequence of crystalline silicon solar cell production, from raw materials to modules, is shown in Figure 1.3 [4].

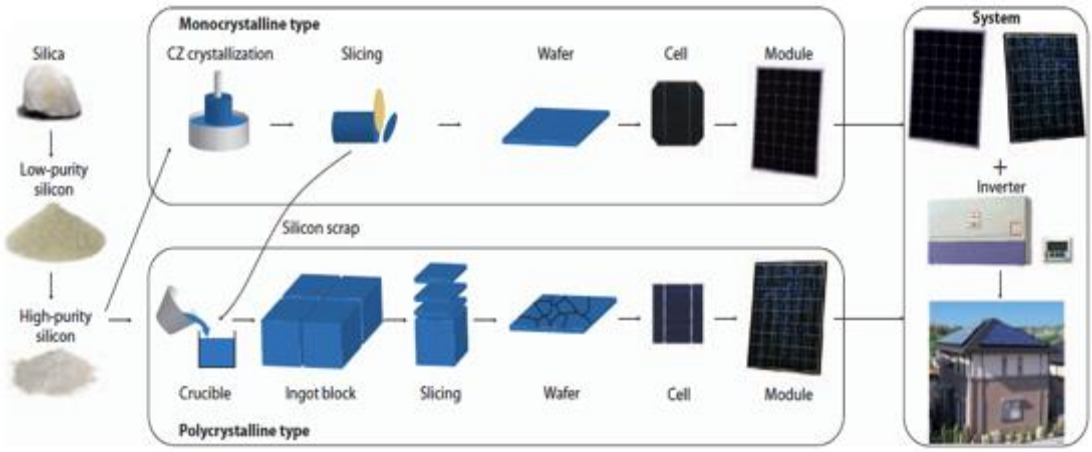


Figure 1.3. Production of typical commercial crystalline silicon solar cells [4].

1.2.1 Multi-wire sawing technique

While in the past few years the cost of solar cell processing and module fabrication has been reduced considerably, the sawing costs remain high [6]. At present the large crystals are cut using the multi-wire slicing technology into wafers with a thickness between 180 and 350 μm [4]. To fabricate such thin wafers, sophisticated manufacturing processes suitable for ultrathin wafers are required. In addition, the processes will need to provide high processing speed and high manufacturing yield.

The sawing process damages the wafer locally across the surface and at the edges by the formation of cracks of dimensions in the micrometer range [5], which considerably reduce the fracture strength of the wafers. In mass production fragile wafers can break easily which reduces the production yield.

Wire sawing, operating by the Free Abrasive Machining (FAM) technique, is a representative technology for large thin silicon wafer production in the semiconductor and photovoltaic industries. The brief schematic of a wire sawing process is illustrated

in Figure 1.4. During the process, a single strand of thin wire (~175 μm in diameter) moves from a feed reel into the rectangular arrangement of fixed shafts with replaceable wire guides, and wraps around the wire guides which have hundreds of grooves. This creates a multiple net of parallel wires, through which the ingot crystal is fed together with abrasive slurry to produce a cut [7].

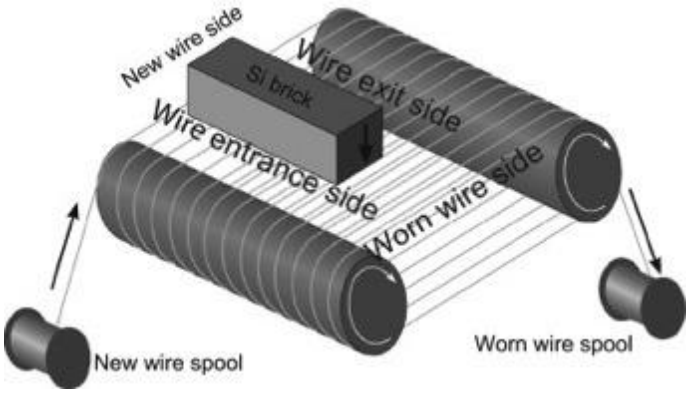


Figure 1.4. Schematic of a typical multi-wire sawing process [6].

1.2.2 Crystal growth technology

A reduction of costs might be achievable by using alternative growth methods that avoid the slicing step altogether. This could be realized by growing the silicon directly from molten silicon into final silicon wafers, featuring the advantage of efficient use of silicon feedstock with no kerf loss, and the elimination of mechanical sawing steps including etching to remove surface damage, which then translate directly into improved economics. A number of continuous ribbon growth techniques have been proposed over the past four decades [8]–[21]. These methods potentially make it possible to reduce the amount of silicon used in PV cell fabrication. Figure 1.5 illustrates the schematic descriptions of two of the most typical ribbon growth technologies.

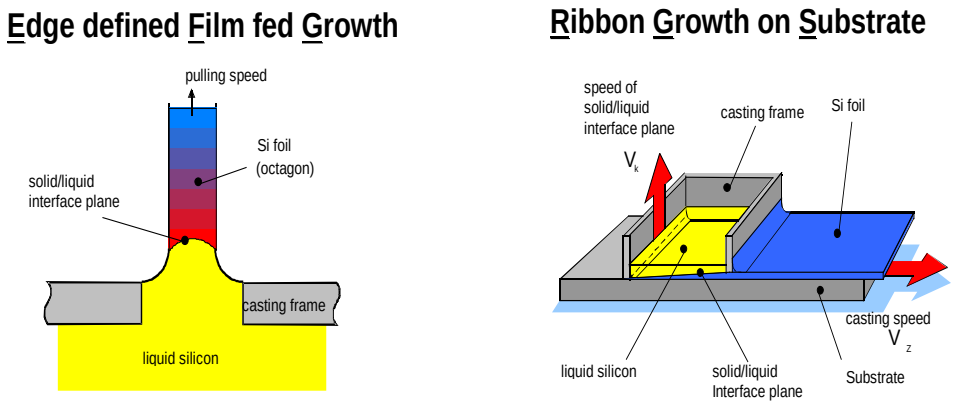


Figure 1.5. Schematic of two of the most typical ribbon growth techniques EFG and RGS [7].

The edge defined film fed growth (EFG) technique grows silicon sheets vertically from melted silicon in a crucible [16]. The crystallization and growth directions are parallel to each other. The sheet geometry is controlled by a slotted die through which silicon melt is fed via capillary effect. The sheet thickness is fixed by the width of the die top, distance between the die tip and melt level, meniscus shape, heat loss from the sheet and the pull rate. The growth rate is controlled by the velocity of heat conducted away from the liquid-solid interface and lost by radiation and convection from the solid crystal. Practically, in order to prevent fracture or buckling of the sheet caused by high thermal stresses, the typical growth rate is restricted to 1 to 3 $cm \cdot min^{-1}$ [10]. Because the die and the crucible are usually made of graphite, the contamination potential of the ribbon is very high. The resultant sheet material comprises of elongated grains and twins in the range of mm to cm wide and many cm long. The grains are columnar along the growth axis and extend through the thickness of the sheet. The dislocation density, however, is as high as 10^{10} m^{-2}. Stresses produced by high thermal gradients during the growth generate most of the intra-granular dislocations.

In the RGS growth technique, the silicon melt is poured in a casting frame under which a colder coated, ceramic substrate is moving, which causes the growth of a thin silicon layer [22]. The ribbon thickness is controlled by the shape of the die, pull rate and surface tension. The directions of crystallization and growth are nearly perpendicular, in contrast to EFG where they are parallel. The latent heat is extracted by conduction into the substrate predominantly and by radiation. This is more efficient heat removal than along the ribbon axis, so much faster growth rate can be achieved. Typical growth rates are ranging from 4 to 9 $m \cdot min^{-1}$. The ribbon thickness is very small compared to the area of the growth interface. However, due to the direct contact of the liquid and solid silicon to refractory materials (melting crucible, casting frame and substrate), the resultant silicon ribbon maintains high potential of impurity contamination. The mismatched thermal expansion coefficients between the silicon and substrate also raise a potential stress issue [21]. Furthermore, the dislocations in RGS, generated by thermal or mechanical stress during the crystallization phase and initial wafer cool-down, are found to have a general density between 10^9 m^{-2} and 10^{12} m^{-2}, which is beyond the acceptable level for solar cells [22].

Therefore, given all the advantages of ribbon growth techniques obtain, the trade-offs are lying in the difficulty of maintaining the intrinsic qualities of the silicon, including low defect density, long minority carrier lifetime, low stress, and mechanical integrity such as flatness, uniform thickness, and surface roughness. These techniques are still under ongoing research and development phase thus no large-scale cost competitive production has been reported.

1.2.4 Silicon deformation and previous work

Wire sawing is time consuming and wasteful, whereas ribbon growth technology has not been put into practice in large scale production or commercialization due to slow growth velocity and difficulty in maintaining the intrinsic quality of silicon sheet. Attempts to develop other low-cost alternatives for solar sheet production have been performed. One potential method for the rapid and inexpensive production of silicon sheets for photovoltaic power generation is the conventional mechanical hot rolling, which is a process commonly used in fabricating metallic sheets in industry. The aim of this project is to perform a feasibility study on producing silicon sheet by traditional hot deformation. The subsection presents a comprehensive literature review of previous silicon deformation work.

1.2.4.1 Deformation of single crystalline silicon

Little was known about the deformation of crystals with a diamond-cubic lattice until the work of Gallagher [23], who for the first time observed that germanium and silicon become ductile in the vicinity of 500 ˚C and 900 ˚C, respectively. Ever since then the mechanical behaviour of single crystalline silicon and other semiconductors with diamond structure has long been investigated [24]–[35]. In the early years special emphasis was placed on the yield point and its correlation to dislocation dynamics [24]–[27], [29], [31], [36], [37]. A comprehensive review of this period was given by Alexander and Haasen [38]. The research undertaken regarding plastic deformation of silicon crystals mainly focused on two aspects.

1. Investigating the genuine mechanical properties of single crystalline silicon at the elevated temperature by exploring the stress-strain behaviour under constant strain rates [28], [39], [40].
2. On the correlation between the dynamical behaviour of dislocations and the general plastic flow or even fractures of crystals by examining the dislocation generation and motion [41].

A < 123 > orientation was generally preferred during the dynamic yield experiments since it leads to single slip [42], [43]. For creep experiments a < 111 > orientation was often used [27], [32]. There was also some work undertaken associated with the impurities behaviour and interaction with dislocations during the plastic deformation [44]–[46]. Apart from uniaxial deformation (tension or compression), the micro-plastic deformation mechanism of silicon was also studied by indentation [33]. However, the majority of studies were performed in a rather restricted temperature range from 350 ˚C to 950 ˚C (where Tm = 1414 ˚C is the absolute melting point of silicon), there were only a few investigations performed at temperatures in excess of 1000 ˚C [27], [42], [43], [47]–[51].

The first high temperature deformation study on single crystalline silicon was conducted by Sylwestrowicz [27], aiming at understanding the part which dislocations play in plastic flow and fracture of crystals together with providing critical tests of Cottrell's theory of the upper and lower yield point phenomenon. During this study float zone dislocation-free single crystalline silicon was subjected to systematic tensile tests with the long axes coinciding with the < 111 > direction in a temperature range from 196 ˚C to 1380 ˚C with rate of straining 0.02, 0.20 and 1.00 min^{-1}. It was concluded from this study that at temperatures above 1100 ˚C crystals of silicon can be strained up to 30 %.

The extent of strain at the ultimate tensile strength is independent of strain rate and temperature. Besides, samples yielded to plastic deformation developed a very distinct slip band system corresponding to slip on the { 111 } plane. Besides, cross-slip was observed at an early stage of deformation.

Myshlyaev *et al.* [32]conducted research on the dislocation structure and macroscopic characteristics of plastic deformation via creep of silicon crystal. It was attempted to answer the question whether the difference in creep behaviour of homopolar and metallic crystals is connected with the difference in interatomic bonds. During the study, creep tests were undertaken on single crystalline silicon under uniaxial compression along the < 111 > direction in a temperature range from 900 ˚C to 1300 ˚C. Dislocation structures associated with each characteristic portions of the creep curve were observed. The structural study in this research provided a picture for the kinetics of dislocation structure and deformation at creep of silicon. It was found that the typical creep curves of silicon and metals are qualitatively similar except for the peculiarities at the very beginning of the process. In addition, relevant microstructure investigation demonstrated that the movement of dislocations in the interior of the sub-grains is far from being sufficient to provide the amount of deformation obtained experimentally. In accordance with the creep data, the conclusion was reached as that the stationary creep rate was not limited by the movement of dislocations in the field of crystal lattice but defined by a collective interaction of dislocations in the sub-grain boundaries. Furthermore, the relationship describing steady creep of silicon under uniaxial compression at high temperatures was found to be the same as the one governing steady creep of metals under uniaxial tension at intermediate temperatures.

Subsequently Aseev *et al.* [49] undertook linear-step loading creep experiments on single crystalline silicon and germanium along the $< 110 >$ direction in the range of 900 ˚C to 1300 ˚C and employed an etch pit method and transmission electron microscopy (TEM) to investigate the dislocation structure and process in sample subjected to plastic deformation at both low temperature and high temperature. A similarity of dislocations processes in silicon and germanium was found. In low-temperature range (700 ˚C to 1130 ˚C, silicon melts at 1414 ˚C) deformation in silicon is realized by dislocation glide and cross-slip is activated which gives rise to a multiplication of dislocations. The interaction and multiplication of dislocations are accompanied by the formation of dipoles including faulted ones, multi-poles, and bundles in slip bands. Dislocations from different slip planes interact resulting in the formation of Lomer dislocations, which serve as the main source of long-range internal stresses in low-temperature deformation. In high-temperature deformation of silicon (T > 1130 ˚C) gliding of dislocations combined with climb is realized, resulting in decrease of the number of dipoles on isolated dislocations and Lomer dislocations by annihilation. Fragments of Frank networks and dislocation walls are formed as well as networks in sub-grain boundaries. Besides, no source of long-range stresses hardening are observed. Typical dislocation structure in silicon deformed at 900 ˚C from their work is presented in Figure 1.6.

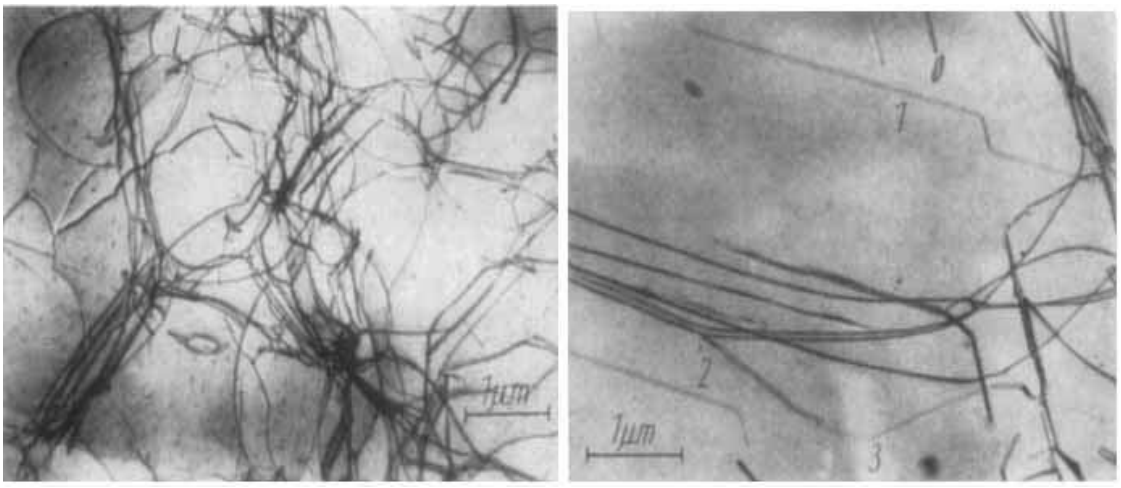


Figure 1.6. Dislocation structures of silicon observed in TEM at slip on (111) parallel to the foil surface in silicon deformed at 900 ˚C [49].

Czochralski grown < 001 > dislocation-free single crystalline silicon was uniaxially compressed at 1380 ˚C at a strain rate of 5.0 s^{-1} by 37 % in the study conducted by Mardesich *et al.* [51] as part of the investigation aiming at determining the feasibility of produce silicon solar cells from sheet formed by high temperature deformation. It was noted that single crystal material cracked at approximately 25 % strain during the compression. The deformation produced a dislocation density too high to be resolved by X-ray topography. A subsequent annealing at 1380 ˚C for 10 hours reduced the dislocation density to 5.0 x 10^{8} m^{-2}. It was also demonstrated that the samples experienced some recovery during the annealing. The etched surface of silicon deformed at 1325 ˚C by 40 % from their work is presented in Figure 1.7. The etch pit density of this sample was estimated as 10^{10} m^{-2}.

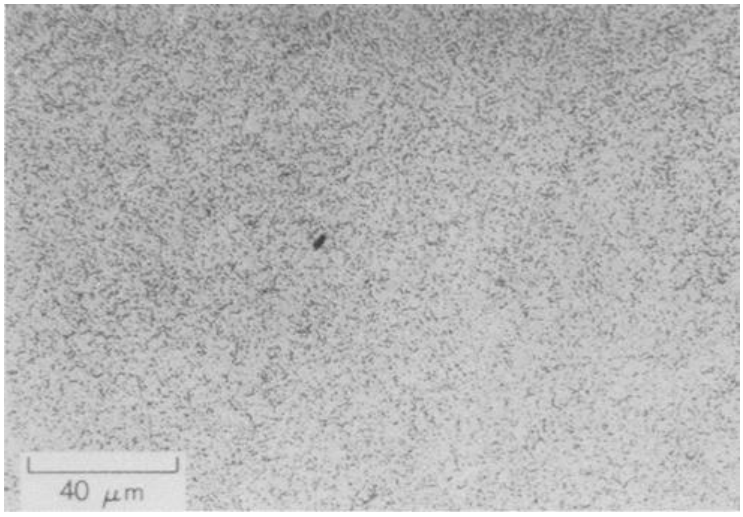


Figure 1.7. Etched surface of single crystalline silicon deformed by 40 % at 1325 ˚C, examined by optical microscopy [51].

Kulkarni *et al*. [50] also conducted hot uniaxial compression of < 100 > oriented p-type single crystalline semiconductor grade silicon at strain rates from 10^{-5} to 12 s^{-1} at temperatures ranging from 1100 ˚C to 1380 ˚C in a similar study as part of the project designed for investigating the possibility of using standard hot working techniques to produce silicon sheet for solar cell manufacturing. The stress-strain curve (see Figure 1.8) showed an extended range of no work hardening and provided evidence for recovery at low strain rate. Another interesting discovery of this study was that the stress necessary to produce a 10 % strain in the < 100 > single crystalline material is very similar to the value obtained for the polycrystalline material.

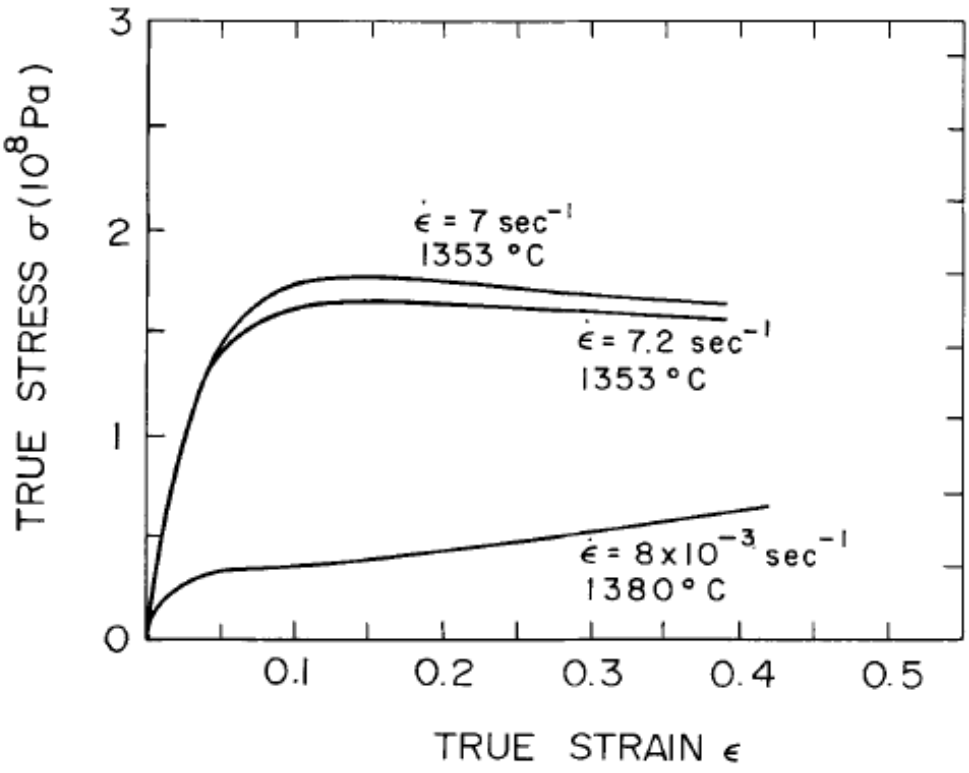


Figure 1.8. True stress train curves of p-doped < 100 > single crystalline silicon samples [50].

Michel *et al.* [42]carried out compression tests on float zone single crystalline silicon along < 100 > orientation by 5.5 % strain at different temperatures varying from 750 ˚C to 1350 ˚C. It was derived from this study that slip occurs by the usual { 111 } < 110 > systems and dislocations form { 110 } sub-grain boundaries.

Mathews *et al.* [43], [47] undertook a series of study attempting to provide data to form a constitutive equation for the mechanical deformation of single crystalline silicon at temperature above 1000 ˚C. Boron doped (14 Ω cm) Czochralski grown silicon with no initial grown-in dislocations were subjected to tensile tests by 5 % elongation at constant extension rates between 1.0 $x10^{-5}$ s^{-1} and 1.0 $x10^{-3}$ s^{-1}. The tensile axis orientations are < 001 > and < 011 >. It was observed that the dependence of yield stress on strain rate decreased to almost no strain rate dependence at 1100 ˚C became

negative at 1200 ˚C. In addition, the resolved shear yield stress did not significantly depend on temperature at strain rates of 1.0 x 10^{-5} s^{-1}. The corresponding microstructure examination demonstrated that well defined dislocation cell walls were formed for slow strain rates and high temperatures (T = 1200 ˚C), which is in good agreement with structures observed by Barrett and Taylor [48] in silicon deformed by creep at 1300 ˚C.

The first and closest attempt towards directly manufacturing solar cell using plastically deformed single crystalline silicon was undertaken by Nakajima *et al.* [52], [53]. In their pioneering work wave-shaped and hemisphere-shaped (100) and (111) boron doped p-type silicon crystal wafers were produced by plastic compression between two graphite dies in the temperature ranging from 1100 ˚C to 1300 ˚C in hydrogen atmosphere, see Figure 1.9. The compressed silicon wafers were then subjected to thermal treatment and manufactured into proper solar cells by firing p-n junction and metal contacts. The conversion efficiency was then measured and reported. Several interesting facts were revealed in their study, as following:

1. It was found that the plastically deformed wafers developed a very distinct slip band system, corresponding to the slip on the { 111 } plane.
2. The dislocation density in the shaped wafers decreases considerably as the pressing temperature increases and the curvature radius of the pressed wafer.
3. For wave-shaped silicon wafer pressed at 1100 ˚C and subjected to following thermal treatment at 1109 ˚C for 1 hour, the measured conversion efficiency obtained a value of 5.0 %, while the same material undergoing compression at 1200 ˚C and annealing at 1209 ˚C for 1 hour measured a distinguished 10.1 % conversion efficiency.

4. For hemisphere-shaped (100) silicon wafer, the solar cell fabricated by silicon compressed at 1200 ˚C but not annealed subsequently measured an efficiency of 5.6 %, whereas increasing annealing time substantially improved the conversion efficiency. The highest efficiency 11.5 % was obtained using silicon wafers compressed at 1120 ˚C followed by annealing at 1129 ˚C for 2 hours.
5. During examination the relation between dislocation density by TEM and the radii of hemisphere-shaped wafer, it was found that silicon wafer with 3 cm radius attains a dislocation density of 1.2 x 10^{12} m^{-2}, while 10cm radius wafer contains a dislocation density of 4.8 x 10^{10} m^{-2}.

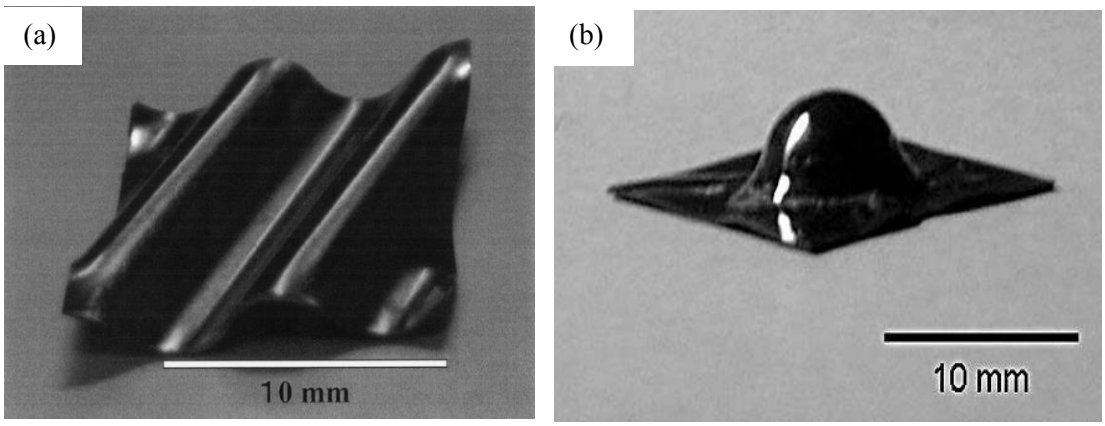


Figure 1.9. (a) Wave-shaped silicon wafer obtained by plastic deformation using the pressing process at 1394 ˚C [53]; (b) Hemispherical silicon crystal wafer fabricated by plastic deformation [52].

1.2.4.2 Deformation of polycrystalline silicon

During the 1960s through the early 1980s preliminary investigations of producing polycrystalline silicon for photovoltaic application by high temperature deformation were conducted [50], [51], [54]–[61]. The aim of these research programs is to determine the feasibility of hot-rolling silicon sheet for photovoltaic power generation [60], a standard process used industrially for the production of metallic sheet and strip

in very large quantities. The general advantages of hot-rolling include high production rates, good dimensional control, and minimal impurities introduction by working only in the solid state [55].

There are only two papers reporting on actual rolling of intrinsic semiconductor, both in the 1960s [62], [63], indicating that silicon (and germanium) can be rolled into thin sheets and the stored energy during deformation could be used for subsequent recrystallization. However, as rolling silicon at high temperatures is more experimentally demanding, compression and tension tests were performed in the late 1970s and early 1980s to investigate the deformation and recrystallization behavior of polycrystalline silicon [50], [51], [54], [55], [57], [59]–[61].

Schins and Radelaar *et al.* [58], [59] firstly investigated the recrystallization behavior of fine-grained (0.1 ~ 10 μm) polycrystalline silicon obtained by chemical vapor deposition (CVD). It was found that the sharply < 110 > fiber textured microstructure of the starting polycrystalline silicon was converted into an inhomogeneous assembly consisting of 20 μm ~ 2 mm long grains of 20 ~ 100 μm diameter after heating at temperatures between 1350 ˚C and 1400 ˚C for 3 hours (see Figure 1.10a). The resultant recrystallized microstructure features a strong < 111 > texture. Their subsequent study regarding hot-deformation of polycrystalline silicon illustrated that deformation by 5 % strain at 1140 ˚C in tension followed by subsequent thermal treatment at 1390 ˚C induced recrystallization, which produced large grain size of 1 mm order (see Figure 1.10b). Furthermore, it was elucidated that strain rate does not have an impact on the recrystallization behavior and the size of dislocation cell structure formed during the deformation process is independent of the total applied strain value.

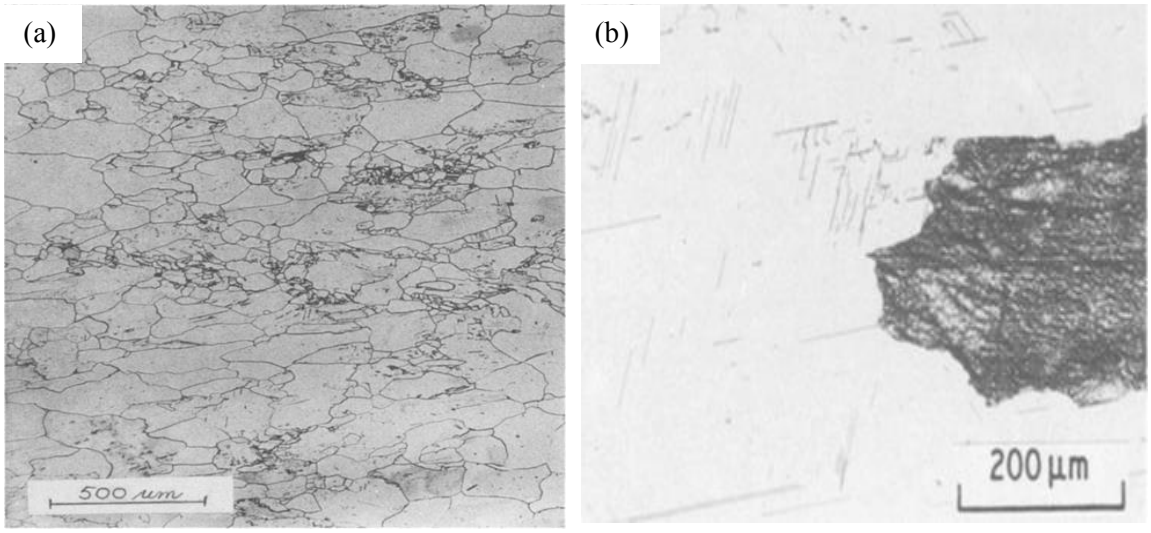


Figure 1.10. (a) Grains of CVD grown polycrystalline silicon after recrystallization at 1380 ˚C during 3 hours. The sample is sawn parallel to the original < 110 > growth direction which is from left to right on the micrograph [58]; (b) Recrystallized regions in CVD grown polycrystalline silicon deformed at 1140 ˚C by 5 %and post-annealed at 1390 ˚C [59].

Kinoshita and Champier [54], [61] conducted investigation on the as-cast bulk 'Silso' [64]polycrystalline silicon by tensile and annealing methods. They firstly figured that 13 % tensile strain at 950 ˚C and further annealing at 1395 ˚C for 4.5 hours induced a recrystallization microstructure of irregular grains with the dimension ranging from 80 µm to 1.8 mm. These recrystallized grains have rather homogeneous profiles of round but more or less elongated shapes comparing to the as-grown 'Silso' polycrystalline silicon which was reported to obtain the most frequent grain size between 150 µm and 750 µm. Further recrystallization microstructure investigation discovered that new grains nucleated in the midst of the grain boundaries (see Figure 1.11) and the recrystallized grain had less etch pits density, between 10^{7} m^{-2} and 10^{8} m^{-2}, suggesting a better crystalline perfection than the initial as-grown microstructure which has a dislocation density between 10^{10} m^{-2} and 10^{12} m^{-2}. A more detailed research concerning

the specification of the experimental conditions especially the tensile deformation of specimens and the parameters of annealing time and temperature was subsequently undertaken. Studies of the variation in the recrystallization fraction confirmed that it is proportional to the initial deformation and of the annealing time and temperature. The recrystallization requires a critical global strain of 7 % and local strain of 10 %. It is conclusive that silicon has a similar recrystallization behavior to metals, provided that a higher temperature and a longer annealing time are employed. The size, morphology and crystalline perfection of the recrystallized grains are comparable to those of metals.

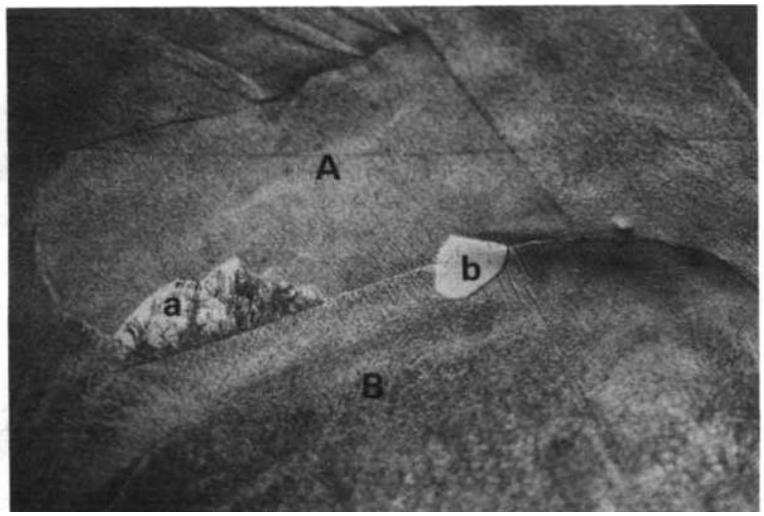


Figure 1.11. Microstructure of 'Silso' polycrystalline silicon deformed at 800 ˚C by 12 % followed by 23 hours annealing at 1395 ˚C.Grain growth by the boundary migration into grain A is marked by a, grain recrystallized from a nucleus situated in the boundary is marked by b. B is the neighbouring grain of A [61].

The most comprehensive and systematic study of manufacturing low-cost solar cells by means of polycrystalline silicon deformation methods was performed by Graham, Jr. *et al.* [50], [51], [55], [57], [65], [66]. The starting material was mainly high purity semiconductor grade CVD polycrystalline silicon grown by the decomposition of trichlorosilane at about 1150 ˚C. The typical stress strain curves of intrinsic

polycrystalline silicon deformed at temperatures from 1100 ˚C to 1380 ˚C are shown in Figure 1.12. The CVD polycrystalline silicon manifested a strong fiber texture, with the longitudinal fiber axis showing the crystallographic <110>, and with no preferred orientation about this axis. In addition, single and poly crystalline silicon grown by Czochralski method were employed for direct deformation behavior, microstructure and electrical properties comparison.

The main results could be summarized as follows:

1. Polycrystalline silicon can be uniaxially compressed by as much as 50 % at 1380 ˚C and a strain rate of 5 s^{-1} without cracking.
2. Large deformation is also possible at significantly lower temperatures, but lower strain rates must be employed to avoid cracking.
3. The silicon material does not recrystallize during the deformation, in the language of metallurgy, the process is regarded as ‘cold working’ rather than ‘hot working’. Thus high temperature annealing must be employed to promote subsequent recrystallization to produce low dislocation density microstructures.
4. A minimum deformation is necessary for recrystallization to occur. This limit depends on the temperature of the deformation was performed: 5 % is sufficient at 1100 ˚C while 30 ~ 40 % is required for 1380 ˚C.
5. Complete recrystallization may be achieved in the course of ~10min if the deformation is large and the annealing temperature is high (specifically, 10 % strain and subsequent annealing at 1380 ˚C).
6. Large grains were not possible to obtain after deformation because too many nucleation sites exist. After recrystallization induced by subsequent annealing,

the nucleated grains grew and impinged on each other, inhibiting further grain growth. A maximum grain size of a few mm was achieved by a low strain value (about 5 %) and long annealing period of 34 hours.

7. Dislocation density in the recrystallized grains revealed by etch pits counting is 10^7 ~10^8 m^{-2}, which is comparable to the best regions of modern multicrystalline silicon.

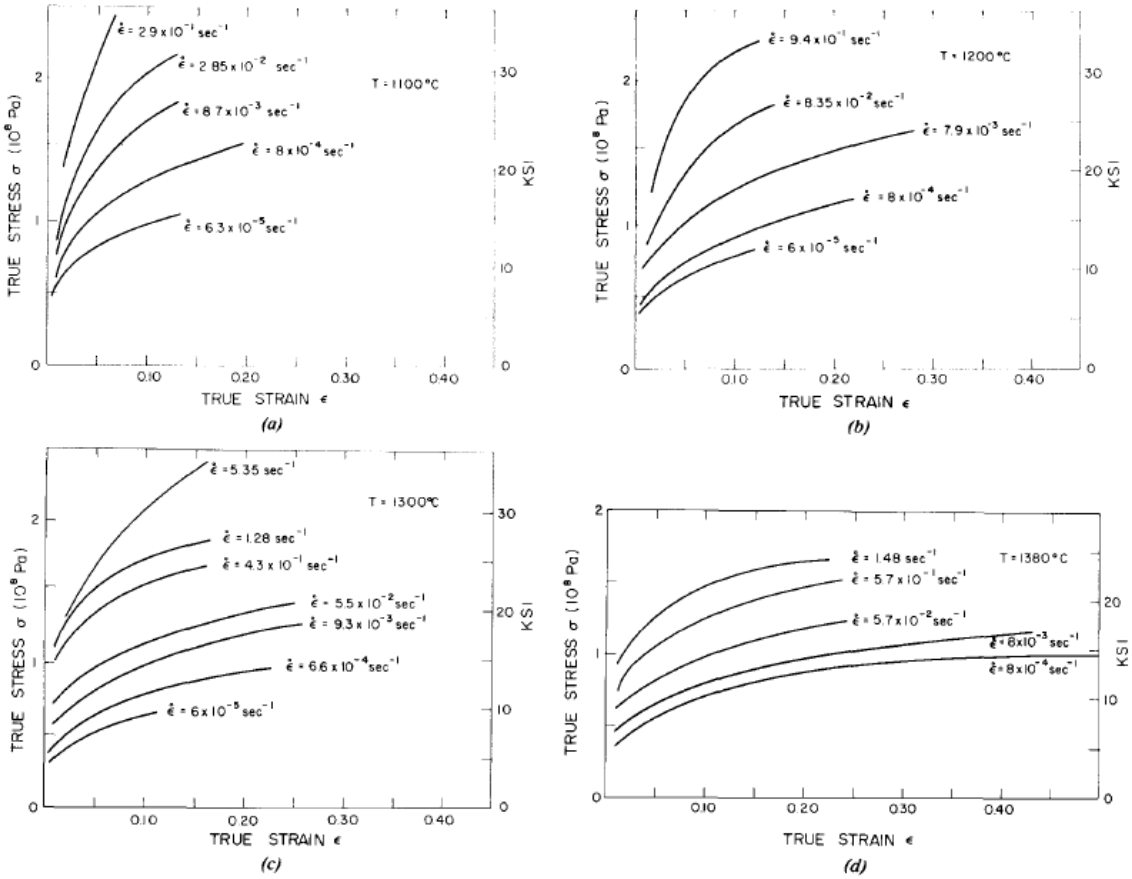


Figure 1.12. True stress strain curves for intrinsic polycrystalline silicon samples deformed at temperatures from 1100 ˚C to 1380 ˚C [50].

All these results are encouraging and indicating no fundamental limitation to the feasibility of producing silicon sheets by conventional hot rolling. However, while investigating the most important merit for silicon used for solar cell production, the

effective minority carrier diffusion length (L_d), researchers [51] found the L_d of the deformed and annealed single crystalline silicon was unmeasurable, while the untreated sample obtained a L_d of 34 μm. The deformed Czochralski polysilicon maintained a L_d of 1 ~ 2 μm, while the initial value was ~ 90 μm pre-deformation. Subsequent annealing at 1270 ˚C for 20 min recovered the L_d to 3 ~ 4 μm. Unfortunately, even the as-received CVD grown polycrystalline silicon yielded diffusion lengths near zero and deformed samples produced un-measurable results. The massive degradation of electrical properties after deformation and annealing led researchers to conclude that fabrication of high efficiency solar cells by high temperature deformation of silicon in unfeasible.

The contamination in the deformation apparatus during the hot-compression process was suggested to be responsible for the minority carrier diffusion length reduction, as the deformation and annealing were conducted in the filthy metallurgical conditions [50], [51], [66]. It is generally accepted that metallic impurities and especially their interaction with dislocations (massively produced by plastic deformation) exerts a detrimental impact on the electrical properties of silicon material [67]. The detailed conversion efficiency limit factors of silicon solar cell performance will be summarized in the following section. Besides, for the time being when these experiments were undertaken, modern gettering (see Section 1.4) and surface passivation technique (see Section 1.5), commonly integrated in current silicon wafer manufacturing industry, were not recognized or employed to improve the electrical properties.

1.3 Conversion efficiency limit factors

Important parameters for the assessment of the solar cell final efficiency and the production yield are the bulk minority carrier lifetime and mechanical stability. The

performance of crystalline silicon solar cells is partly limited by minority carrier recombination which is in general affected by crystalline defects such as dislocations, stacking faults and grain boundaries, and intra-grain defects for instance impurities, small cluster of atoms or precipitates [3], [46], [68]–[82]. The present section depicts the current understanding about the structure and properties of the most important defects (dislocations, stacking faults, grain boundaries and impurities) together with their interactions in brief. The reader is referred to classic text books such as Hirth and Lothe [83], and Hull and Bacon [84] for detailed depiction of structural defects.

1.3.1 Dislocations

All real crystals contain imperfections which may be point, line and surface or volume defects which disturb locally the regular arrangement of the atoms. Their presence can significantly modify the properties of crystalline solids. Dislocations are crystallographic line defects within a crystal structure and are the result of plastic slip between adjacent atomic planes. Plastic slip is associated with mechanical stresses, thermal stresses and impurities within the crystal lattice and occurs when the shear stress acting on the slip plane reaches a critical value, *i.e.* the Critical Resolved Shear Stress (CRSS). Dislocation are usually characterized by a vector parallel to the ***dislocation line*** (denoted by **u**) which is the boundary of an area over which slip displacement takes place, and a ***displacement or Burgers vector*** which is a certain finite increment **b**. The ***slip plane*** is uniquely defined as the plane which contains both the line and the Burgers vector of the dislocation. There are two primary typical types of dislocations: the ***edge*** and ***screw*** dislocations, which have **b** normal and parallel to the dislocation line vector **u**, respectively. In the most general case, the dislocation line lies at an arbitrary angle to its Burgers vector and the dislocation line has a mixed edge and

screw character. Dislocations are also classified as perfect or extended type. A perfect dislocation has a Burgers vector equal to the lattice vector, in which case the crystallinity of the materials is preserved. Extended dislocations are perfect dislocations dissociated into partials separated by stacking faults. Each of these partial dislocations has Burgers vector shorter than the lattice vector.

As the atoms in a crystal containing dislocations are displaced from their perfect lattice sites, the resultant distortion produces a stress field around the dislocation. Therefore the dislocation becomes a source of internal stress in the crystal. The existence of distortion around the dislocation implies that a crystal containing dislocations is not in its lowest energy state. The extra energy is called the strain energy, divided into two parts, namely the dislocation core energy and the most important elastic strain energy which is stored outside the core. The elastic strain energy per unit length of a dislocation (E_{el}) is approximately proportional to the square of the Burgers vector and can be written as [84]:

$$E_{el} = \alpha G b^2 \qquad \text{Equation 1.1}$$

where G is the shear modulus and α is a value approximately 0.5 ~ 1.0 for metallic and ceramic solids. Consequently, given a perfect dislocation with Burgers vector $\mathbf{b}_3$ is allowed to be split into two partial dislocation with Burgers vectors $\mathbf{b}_1$ and $\mathbf{b}_2$ respectively, *i.e.* $b_3 = b_1 + b_3$, if the condition $b_3^2 > b_1^2 + b_2^2$ is satisfied, then the dislocation with Burgers vector $\mathbf{b}_3$ is liable to dissociate into the other two as it is energetically favourable in terms of the reduction of the elastic stain energy in the crystal. In another word, it may also be feasible to form a perfect dislocation by two partials if $b_3^2 < b_1^2 + b_2^2$ is satisfied.

Applying sufficiently high stress to a crystal containing dislocations leads to the dislocation movement, producing irreversible plastic deformation either by glide (the dislocation moves in the slip plane) or at sufficiently high temperature by climb (the dislocation moves out of the slip plane) or cross-slip (dislocation moves from one slip plane to another). In general the dislocations distribute inhomogeneously in a plastically deformed crystal, predominantly in 'tangles' or 'forests', depending on the deformation temperature as well as the presence and distribution of other defects such as grain boundaries and precipitates. The deformed microstructure is often a 3-D cellular structure with walls consisting of dislocation tangles. Annealing at sufficiently high temperature causes dislocation to move. Dislocations with opposite physical characters (for example dislocation with the same line vector but opposite Burgers vectors) annihilate with each other and restore perfect crystallinity. The dislocations that cannot be effectively annihilated or escape from the crystal will rearrange into a lower energy configuration, aligning into ordered dislocation arrays and reducing the stored energy by the overlapping of their strain fields. This process is called ***recovery***, which includes crystal polygonization. As polygonization proceeds the cellular dislocation walls in the deformation structure will undergo a transition towards a genuine subgrain structure which is comprised of low-angle grain boundaries.

Silicon crystallizes in the cubic diamond structure belonging to space group Fd3m. The lattice constant is a = 0.543 nm. The glide plane is { 111 } and perfect dislocations have Burgers vector of the type b=1/2 < 110 >. Therefore silicon has twelve { 111 } < 110 > slip systems. Shockley commented the idea of splitting of perfect dislocations in the diamond structure for the first time (1953) [85] and the dislocation dissociation was experimentally proved by weak-beam method by Cockayne and Ray (1969) [86], as

shown in Figure 4.13. Hornstra [87] introduced two types of perfect dislocations in the diamond lattice: a pure screw dislocation and the so-called 60˚ dislocations, where the Burgers vector is inclined at 60˚ to the dislocation line. The diamond structure corresponds to two interpenetrating face-centred cubic (fcc) lattices with a relative displacement of a/4 (111), hence there are two distinct sets of { 111 } lattice planes. Consequentially there exist two possible { 111 } sets of glide systems for dislocations: the closely spaced glide subset and the widely spaced shuffle subset [83]. Both the screw and 60˚ dislocations of the glide set can dissociate into two parallel Shockley partial dislocations bounding an intrinsic stacking fault ribbon in between [79], [88], [89]. Most of the evidence indicates that the dislocations found in plastically deformed silicon belong to the glide set [90], [91]. The 60˚ dislocation can dissociate into a 30˚ partial and a 90˚ partial, while the screw dislocation dissociates into two 30˚ partials [92].

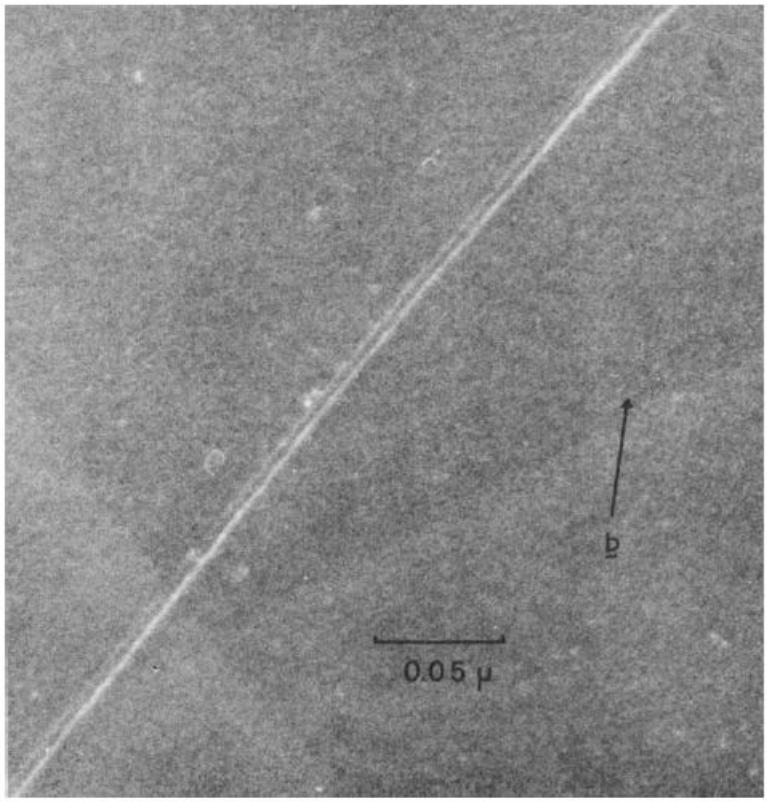


Figure 1.13. Observed dissociation of a 30° dislocation in silicon by weak beam dark field technique .

Dislocations in standard ingot multicrystalline silicon are usually formed during crystal growth by plastic deformation to reduce the thermal stresses. The average dislocation densities vary between 10^{7} and 10^{8} m^{-2} but local dislocation clusters have densities in excess of 10^{12} m^{-2} [3]. These dislocation networks often show high recombination rates and are potentially very detrimental to the solar cell performance. The dislocation density distribution in these multicrystalline silicon ingots are often highly non-uniform, increasing from the ingot bottom to the top and varying across grains and even within the same grain.

It has been also taken into evidence that charge carrier recombination at dislocations is not governed by the intrinsic properties of the dislocations but strongly influenced by

impurity decoration [93]–[97]. Theory predicts that ideal straight and clean dislocation segments are not associated with any deep electronic states in the band gap of silicon, i.e. electrically inactive. Interaction of dislocations with point defects of intrinsic or extrinsic origin is known to significantly change the deep level spectrum of dislocations [98]. A detailed summarization of impurities in crystalline silicon together with their interaction with dislocations and other lattice defects, together with their consequential influence on the electrical properties of silicon materials will be presented in Section 1.3.4.

1.3.2 Stacking faults

A perfect crystal can be described as a stack of atom layers arranged in a regular sequence. A stacking fault (SF) is a planar defect where the regular sequence is interrupted. It can alternatively be interpreted as the change in sequence resulting from inserting or removing an extra atomic layer, referred to as ***extrinsic*** and ***intrinsic***, respectively. A perfect FCC crystal can be depicted as stack of close-packed { 111 } planes. As the diamond cubic structure consists of two interpenetrating FCC cubic lattices, the close-packed { 111 } planes become pairs of { 111 } planes in the diamond structure. If the stacking sequence of the first sublattice is ABCABC, and that of the second abcabc, the structure is henceforth built up as aAbBcCaAbBcC…. [79]. The { 110 } projection of the diamond cubic lattice showing an intrinsic faults and an extrinsic faults is presented in Figure 1.14. It should be noted that the stacking faults in the diamond structure can be formed via a sliding process, by the movement of partial

dislocations or agglomeration of point defects, *i.e.* vacancies for the intrinsic case and interstitials for the extrinsic case.

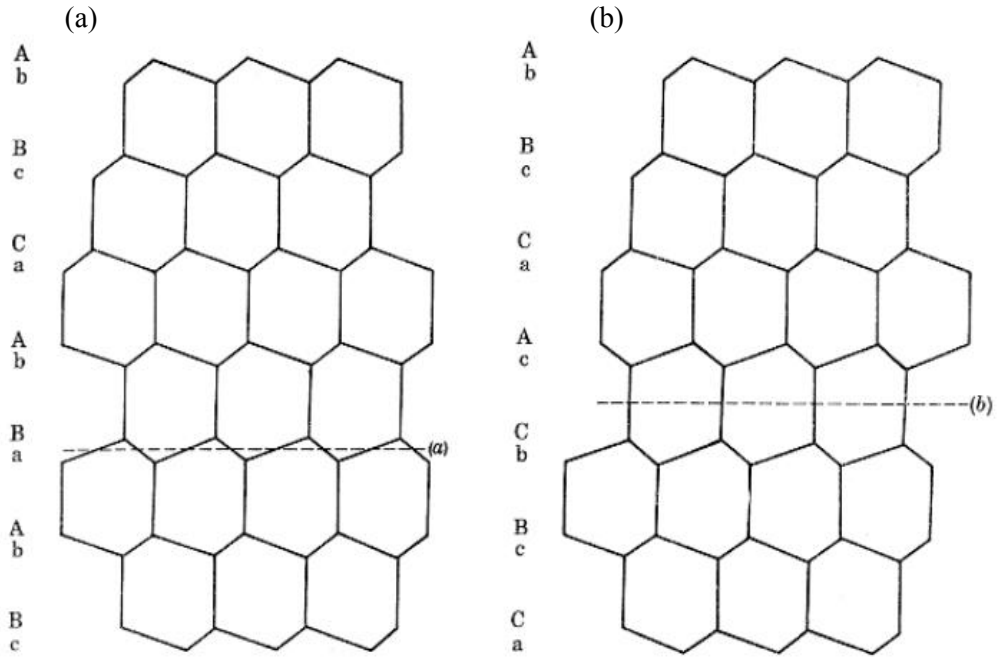


Figure 1.14. {110} projection of the diamond-cubic lattice showing (a) an intrinsic fault and (b) an extrinsic fault [79].

Stacking faults destroy the crystal perfection and the associated energy per unit area of fault is defined as the ***stacking fault energy***. Since a stacking fault consists of neither deformed nor broken bonds the SF energy is small (0.005 eV/Å^2) [99] compared to GBs, dislocations and surfaces. Experimental determination of SF energy is achieved by measuring the dissociation width, *i.e.* the equilibrium separation of partial dislocations, in weak-beam diffraction [79], [86], [100]–[104].

The nature and growth of SFs in silicon has been extensively studied over the past few decades [105]–[110]. It is generally accepted that formation of stacking faults in silicon is induced by two mechanisms, induction by oxidation which absorbs silicon atoms and thus generates vacancies in the silicon bulk (surface associated) or interstitials

nucleation at the sites of oxygen clusters (bulk precipitates associated) [99], [105]–[108], [110]–[115]. The stacking faults generated by oxidation is named as oxidation induced stacking faults (OISF). A consensus exists that the OISFs are extrinsic in nature, bounded by 1/3<111> Frank partials. [116]. It has been observed that stacking faults act as a dislocation generation source in silicon samples containing decorated OISFs annealed at elevated temperature (800 ~ 1000 ˚C), primarily due to precipitates formed at the faults [117], [118]. During investigating the grown-in defects in Cz-Si crystals by TEM, it was revealed that the material contains both the extrinsic Frank partial type SFs and perfect dislocations whose ends were contacting the edge of SFs. It was therefore concluded that the SFs were formed by the agglomeration of self-interstitial atoms during crystal growth and the dislocations are considered to be generated from the edge of SFs[119].

SFs plays an important role in dislocation motion and, consequently in plasticity, as well as in electrical properties. Since a stacking fault in silicon is not accompanied by elastic strain field or dangling bonds its electrical activity is expected to be smaller than that of dislocations [116], therefore the density of stacking faults in multicrystalline silicon is considered to be high. The electrical activity related to a stacking fault is usually brought about by the bounding Frank partial dislocations but not by the fault plane [120]. It was observed by Kimerling *et al.* [121] that undecorated Frank extrinsic stacking faults exhibited defect energy levels in the upper half of the gap to be ~ E_c-0.1 eV and the partial dislocations bounding these faults were determined to possess energy levels lower than E_c-0.3 eV, where E_c is the lower edge of the conduction band. A similar conclusion was reached by Haddad and Forbes [122] by investigating the correlation of the stacking fault size and density with the deep level transient

spectroscopy (DLTS) measurements. Their results indicate that the stacking faults are electrically active themselves rather than caused by the incorporation of impurities. It was further stated that properties of energy levels associated with the SFs could be modified by introduction of metallic impurities to decorate the partial dislocations bounding the faults and SFs could act as barriers to carrier diffusion rather than recombination centres [120]–[123]. Nevertheless, SFs are closely associated with dislocations and favour impurity precipitation therefore play a critical role in the determination of electrical properties of silicon materials at a macroscopic level.

1.3.3 Grain boundaries

Crystalline solids usually consist of numerous randomly oriented (single crystalline) grains. A grain boundary (GB) is an interface separating two grains of different crystallographic orientations [84]. Since the grains are generally in many different orientations the structure of GBs can vary substantially from one to another. The geometry of a GB is macroscopically characterized by the inclination of the boundary plane relative to the two crystal grains and by the misorientation between the two adjoining grains, i.e. the smallest rotation through a single axis required to coincide the two crystals [70]. In general the axis of rotation will not be simply oriented with respect to either grain or the boundary plane. There are, however, two special types of boundary exist, namely pure tilt boundaries and pure twist boundaries, as illustrated in Figure 1.15. GBs of the tilt type features the rotation axis parallel to the boundary plane, whereas the twist type has the rotation axis normal to the boundary plane. A general GB may have both tilt and twist components. GBs may also be classified by their angle of misorientation θ_{GB} into low-angle ($\theta_{GB} < 5^{\circ}$) and high-angle GBs. Special GBs exhibit a periodic structure, while general GBs manifest no apparent periodicity.

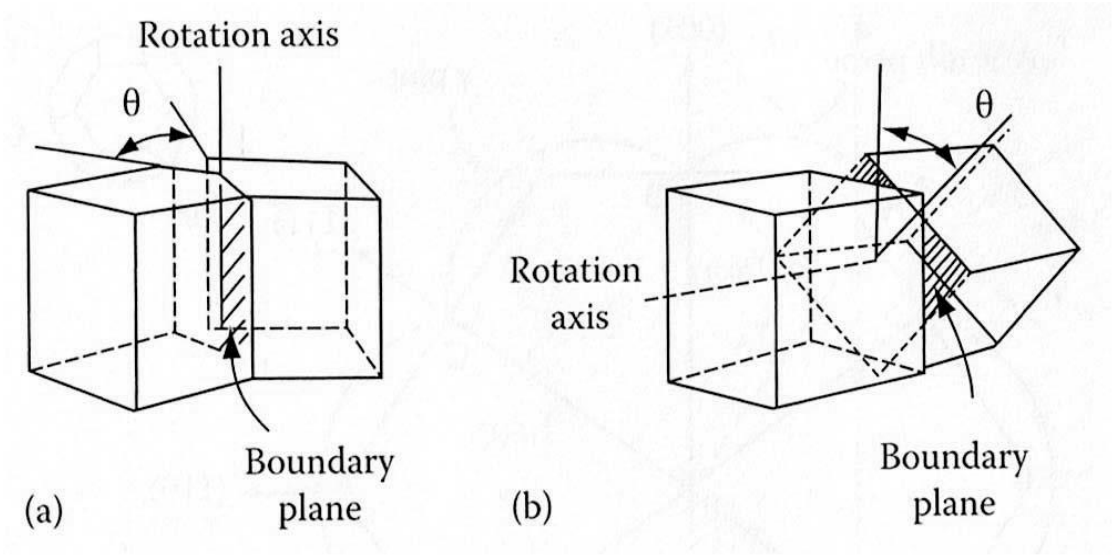


Figure 1.15. The relative orientations of the crystals and boundary forming (a) a tilt boundary and (b) a twist boundary.

Low-angle grain boundaries (LAGBs) can be simply described by a dislocation model where the boundary is regarded as a planar arrangement of individual dislocations and the atomic structures of the dislocation cores are modelled so as to minimise both the density of dangling bonds, bond bending and stretching. There are symmetrical low-angle tilt (an array of parallel edge dislocations) and low-angle twist boundaries (a cross-grid of two sets of screw dislocations) [124]. The simplest low-angle tilt boundary is illustrated in Figure 1.16. The energy of a LAGB is the total energy of the dislocations within unit area of boundary, which depends on the spacing of individual dislocations denoted as D. In the simple dislocation array case, the value of spacing D**,** the size of the Burgers vector b and the angular misorientation θ across the boundary satisfy the relation [124]:

$$D = \frac{b}{\sin(\theta)} \cong \frac{b}{\theta} \qquad \text{Equation 1.2}$$

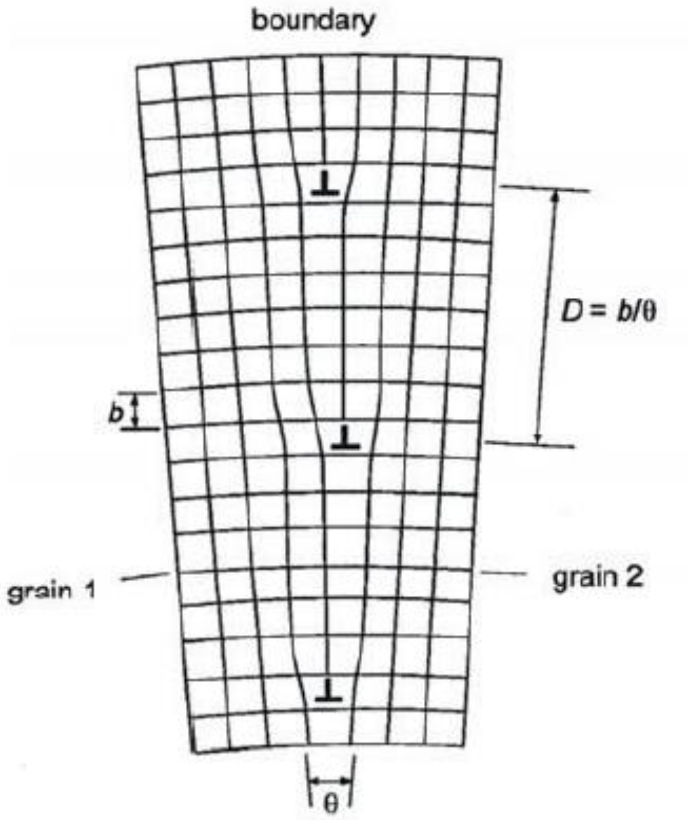


Figure 1.16. Dislocation model of a symmetric pure tilt boundary [94].

At very small value of θ the GB energy is approximately proportional to the density of the dislocations in the boundary. However as θ increases the dislocation spacing D decreases, leading to the strain fields of dislocations progressively cancel out so that GB energy increases at a decreasing rate. When θ exceeds ~ 15˚ the boundary dislocations lose their individuality as their dislocation cores overlap. The properties and structure of the boundaries are generally independent of the misorientation. This type of GB is then called high-angle grain boundaries (HAGBs).

High-angle boundaries contain large amount of poor fit regions between the two crystals and have a relatively open structure comprising of broken and highly distorted atomic bonds. Consequently the HAGBs are associated with relatively high energy.

However, not all HAGBs have an open disordered structure. At certain particular misorientation the boundary planes allow the two adjoining lattices to fit together with relatively little distortion of the interatomic bonds, henceforth these boundaries have significantly lower energies than the random HAGBs. The geometric relationship between the two grains forming this type of special boundaries can be described by the coincidence sites of lattice points between the two grains. In coincident site lattice (CSL) theory, the degree of fit (denoted as Σ) between the two crystals is defined by the reciprocal of the ration of coincidence sites to the total number of sites. Since the Σ value translates the degree of symmetry a low Σ boundary maintain a higher degree of order henceforth lower boundary energy.

The structure-energy correlation of CSL boundaries has been extensively studied in FCC (and diamond) structure crystals [125]–[128]. The calculated energies of symmetrical < 011 > tilt GBs with respect to the misorientation angle θ in silicon are shown in Figure 1.17 [125]. It is evident that Σ 3 (twin) boundaries have the lowest boundary energy and thus maintain the highest stability among HAGBs. Statistical observation of GB character distribution shows that Σ 3 together with its variants Σ 9 and Σ 27 boundaries are dominant, comprising virtually the entire population of CSL boundaries in low to medium stacking fault FCC materials [129].

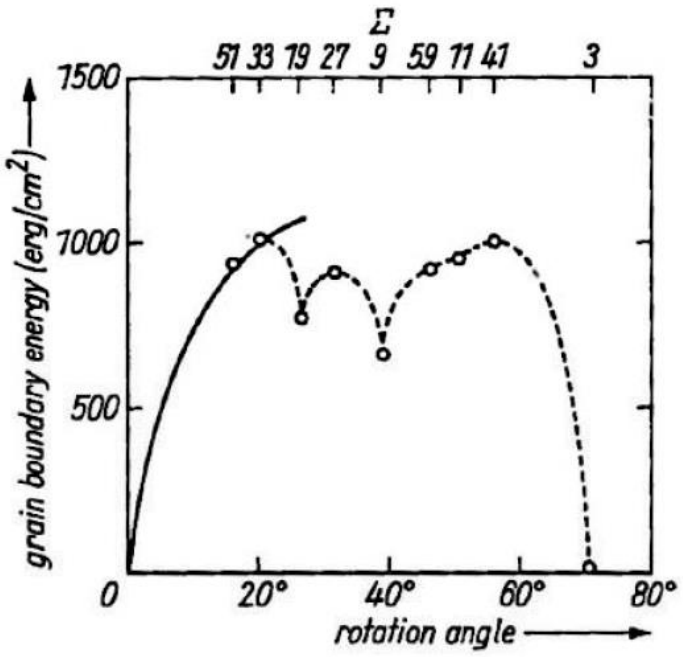


Figure 1.17. Calculated boundary energies of symmetrical < 011 > tilt boundaries versus the rotation angle θ in the range in the range $0^\circ \leq \theta \leq 70.53^\circ$ [125].

Numerous investigations have been carried out on the structure of GBs in polycrystalline silicon. A comprehensive review was conducted by Seager [74] and the principal conclusions are as following:

- Silicon grain boundaries are primarily composed of regular line defects: simple perfect dislocations, partial dislocations, and stacking faults. Observations reveal no evidence for a distinct amorphous phase at the boundary interface regardless of specific crystal growth technique (including chemical vapour deposition, web growth and edge-defined ribbon growth).
- Low-angle (GB < 5˚) tilt and twist boundaries are not composed of regular arrays of simple edge dislocations as suggested previously. Instead, several types of dislocations are present in the same boundary; some may be dissociated into partial dislocations forming a stacking fault in between. Most of these low-

angle grain boundaries are reconstructed by pairing neighbouring unsatisfied bonds such that no dangling bonds remain.

- High-angle grain boundaries are usually composed of distinct facets with lengths of one or more nanometres long. These facets are subsections of the boundaries where bonding rearrangements have occurred that are of a few known low-energy configurations [130]. These configurations can usually be predicted using the concepts of the coincidence site lattice (CSL) theory [131]–[134]. The arrangement of these facets is not always a simple, repetitive one and the average boundary interface angle can actually differ considerably over macroscopic distances [135].
- Even simple first-order twin boundaries can display this irregular faceted structure at their interfaces. Dislocations frequently terminate at coherent twin boundaries [136], and the resulting intersection points disturb the atomic arrangements on the boundary plane.

GBs are of paramount importance as they act as effective obstacles to dislocation motion and the interaction of intra-granular dislocations with GBs is a long-term research interest. The elastic interaction between dislocations and GBs is commonly repulsive and consequently the dislocations pile up at the boundary. Dislocations, however, may also transmit directly across the GB if the slip plane on both sides intersect along a line lying in the boundary plane. The Burgers vector of pure screw dislocations remains unchanged during the transmission, whereas in contrast, dislocations with an edge component requires the formation of a residual grain boundary dislocation with a Burgers vector equal to the difference of the Burgers vectors of the incoming and outgoing lattice dislocations. A dislocation may

alternatively be absorbed by the boundary without emitting another dislocation in the adjacent grain, in which case the lattice dislocation fully dissociates.

Another important issue related to GBs is the diffusion of impurities. It is general knowledge that impurity diffusion along GBs is orders of magnitude faster than volume diffusion. Therefore GBs play a major role in processes involving material transport, such as recrystallization, grain growth, and grain boundary segregation, etc. Particularly in semiconductor materials, high Σ and non CSL random boundaries favour segregation of metallic impurities owing to their highly defected nature. In addition, GBs can be employed as effective internal gettering sites for impurities leading to the enhancement of electrical properties. Studies on the structure-recombination activity relationship show that the structural properties of GBs and impurity decoration have a strong impact on the recombination activity of GBs [73], [76], [137]–[143]. Wang *et al.* [144] showed that the recombination activity greatly depends on the GB character by observing Σ3 and Σ9 GBs in polycrystalline silicon. Hamada *et al.* [77] observed that the Σ3 GB has shallow levels, whereas other GBs have deep levels. Aucouturier *et al.* [145] reported that the different part of one Σ3 GB showed different recombination strengths. In summary, it was concluded that random or high Σ GBs showed higher recombination activities than low Σ GBs which have a higher coherency degree. It was also suggested that HAGB with perfect periodicity and without impurity contamination should be electrically inactive. GB engineering in crystalline silicon, however, remains an ongoing discussion and major research interest.

1.3.4 Impurities and precipitates

It is well accepted that minority carrier recombination activity is closely related to the various impurity concentration and distribution in crystalline silicon [146]–[151]. Carbon, oxygen, hydrogen and fast diffusing 3d transition metals are the most important extrinsic point defects in silicon, apart from the doping elements (mainly B, Al and P) [146]. These impurities in cast multicrystalline silicon are usually introduced via the feedstock, during crystal growth and/or solar cell processing. Light element contaminants such as carbon, oxygen and hydrogen typically result from reaction of the chemically aggressive silicon melt with the crucible which is usually made of quartz material with silicon nitride layer coating. Carbon and nitrogen are known to form rod-like and filament-like precipitates consisting of SiC and Si_3N_4, which directly grow from the melt at the liquid/solid interface and frequently give rise to local shunts in solar cell emitters [3], [152]–[154]. Oxygen can be found as interstitial species and as SiO_2 precipitates frequently locating at GBs.

Transition elements (for instance Cr, Mn, Fe, Zn, Ag, Au, Ti, Co, Ni and Cu) diffuse interstitially and strongly interact with existing crystal structure defects. The majority of metallic impurities are indicated to form complexes, accumulate at grown-in dislocations or segregate at GBs in different forms (such as $FeSi_2$, $NiSi_2$ and Cu_3Si are frequently observed), or even form silicide precipitates which simultaneously contain several metal impurities [155]–[163]. These metal concentrations in commercial ingot-cast multicrystalline silicon materials can reach as high as $10^{13} \sim 10^{16}\ m^{-3}$, as measured by Neutron Activation Analysis (NAA) [164], [165].

Impurities in silicon reduce the efficiency of silicon based devices in a variety of ways. A ground breaking early study correlating the total metallic contaminants content to a quantified decrease in silicon solar cell conversion efficiency was performed by Davis *et al*. [146] involving introducing controlled concentrations of selected impurities (Al, B, C, Ca, Co, Cr, Cu, Fe, Mg, Mn, Mo, Nb, P, Pd, Ta, Ti, V, W, Zn, and Zr) into the melt during crystal growth. The threshold concentrations for individual metal species above which the efficiency of Cz-Si photovoltaic devices will degrade. An analytical first-order model was developed to predict the solar-cell performance as a function of the concentration, as shown in Figure 1.18. The experimental results also indicate that a reduction of the base diffusion length is the dominant mechanism of cell degradation, with the exception of Ni, Co and Fe, with whom substantial performance loss is due to junction defect phenomena at the higher concentration.

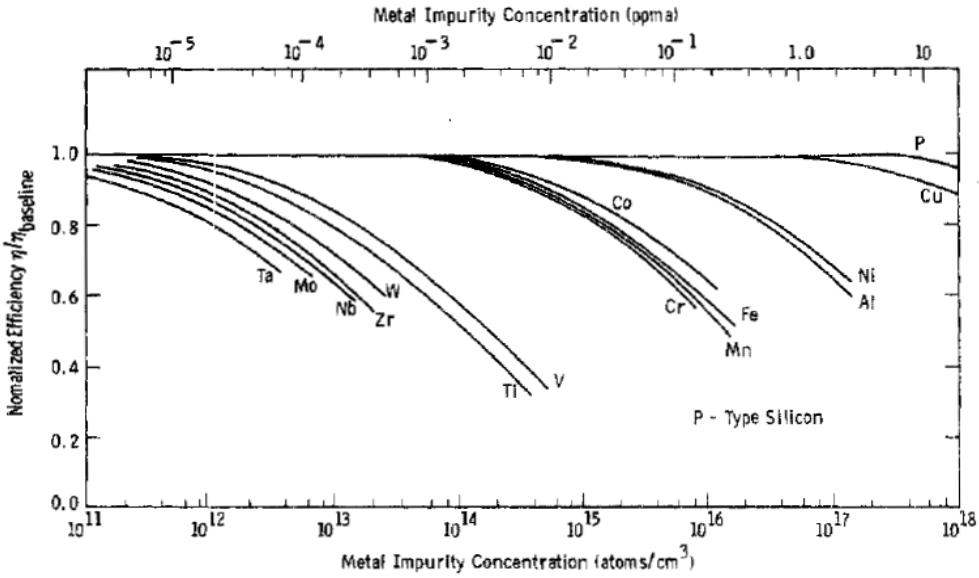


Figure 1.18. Solar cell efficiency as a function of impurity concentration for 4 Ω.cm p-base devices [146].

Subsequent studies, however, clarified that not only the total concentration of different metal species determine the solar cell performance, but also the spatial and size distributions of metal-related defects, their chemical natures, interactions with different types of extended defects and behaviour during the crystal growth process [53], [150], [151] , [131], [133], [140], [141].

A comprehensive review regarding the structural and electrical properties of metal impurities at dislocations in silicon was provided by Seibt, *et al.* [67]. For isolated point defects, the basic considerations of possible interactions of impurities and dislocations were roughly distinguished as following:

- Impurity atoms may chemically bind to the dislocation core in various configurations and also migrate along the dislocation core.
- Impurities segregate in the long-range strain field around a dislocation attributing to the size effect, *i.e.* the difference of the (covalent) radii of the impurity and the host lattices.
- Impurities precipitate at dislocations via heterogeneous nucleation and dislocation may also assist precipitate growth by the accommodation of volume misfit between precipitate phase and silicon matrix.
- For impurities that diffuse via intrinsic point defects, accumulation close to dislocations may occur since intrinsic point defects may quickly equilibrate there.

It is of particular importance to note that the fast diffusing transition metal impurities are mobile even near the room temperature, hence they may accumulate at dislocations even during storage at room temperature.

The electrical properties of silicon materials are strongly affected by deep levels at or close to the dislocation core which are frequently thought to attribute to metal impurity decoration [98].

1.4 Gettering

As stated in previous sections, metallic impurities and structural defects, specifically dislocations, GBs and micro-defects are the most conceivable sources for low conversion efficiency in solar grade materials. Metallic impurities, dissolved, precipitated or segregated at extended crystallographic defects generally act as recombination centres for minority carriers and degrade drastically the minority carrier diffusion length in silicon wafers. Henceforth it is imperative to remove these undesirable metal impurities from local regions or the bulk of device. An effective method to achieve this is via ***gettering***, which is possessed in current standard solar cell processing steps [168]–[174]. Gettering is a process of relocating unwanted metallic impurities within a wafer to a lower energy location. According to the final gettered location, gettering can be categorized into ***internal gettering*** and ***external gettering***. During ***internal gettering***, undesirable contaminant are deliberately transported from the electrically active areas into noncritical regions (typically defect sites) located within the same wafer, which is a process widely integrated in modern microelectronic devices manufacturing [175]. ***External gettering***, on the other hand, features removing impurities away from the entire wafer, which is typically employed in photovoltaic industry since solar cells are regarded as whole-wafer devices [172]. In general, gettering processes involves three steps:

1). Release of impurities from their original and undesirable associated form;

2). Impurities diffuse through the crystal to the gettering region;

3). Impurities captured at the gettering sites [173].

The concept of gettering process is shown in Figure 1.19. For effective gettering, the energy barrier for the release of impurities from the original sites should be low and the impurities captured at the gettering sites should not be released easily. The distance between the initial sites to the optimal gettering site should be shorter than the impurity diffusion length for the time and temperature used for gettering. However, the exact mechanisms by which gettering comes about are not yet well established.

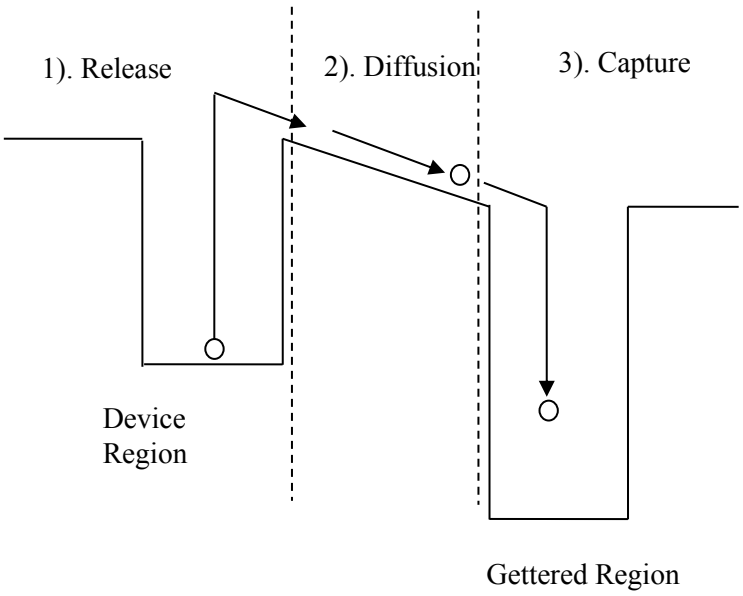


Figure 1.19. Concept of the gettering process involving releasing, diffusion and capture of impurities.

Two gettering processes are usually active during solar cell fabrication, *i.e.* phosphorus diffusion gettering (PDG), as part of the emitter diffusion in p-type solar cells, and aluminium gettering (AlG) which takes place during formation of the back-surface field. Both gettering methods have been demonstrated to be effective for bulk lifetime improvement [172].

AlG occurs by deposition and subsequent heating of a thin (≥ 1 μm) aluminium film on the backside of a silicon substrate. The aluminium alloys with the silicon and will melt above the eutectic temperature of the binary system Al-Si 577 ˚C. This melt has a significantly higher solubility of metal impurities and thus getters them from the silicon substrate by segregation [169]. On the other hand, during PDG process, phosphorus is diffused into silicon from a deposited or gaseous source. A heavily doped layer of phosphorus provides a number of potential mechanisms for gettering: solubility enhancement by the Fermi level effect and metal-dopant ion pairing, gettering to lattice imperfections, and silicon self-interstitial injection-assisted gettering. Phosphorus gettering by $POCl_3$ has been proven more efficient than other phosphorus diffusion treatments as it is the only way to obtain a very high phosphorus concentration at the surfaces, around 10^{21} cm^{-3} [173].

1.5 Passivation

Crystalline silicon is an indirect semiconductor and hence recombination losses in this material occur largely via defect levels within the band gap. Non-saturated (‘dangling’) bond defects present in the material play a detrimental role in reducing the electrical properties by introducing a large density of allowed energy states within the band-gap. These inner band energy levels cause a severe recombination loss, therefore these bond defects must be electronically well passivated [176]. There are primarily two passivation schemes, namely surface passivation and bulk passivation.

In general, there are two independent techniques for surface passivation: implementation of a doping profile below the silicon surface and field-effect passivation due to electrical charges in an overlying insulator (or on a gate electrode). A number of

technologically possible surface passivation methods have been developed based on these two fundamental passivation principles, including growth/deposition of a dielectric film, chemical passivation by liquids, the application of a gate voltage, and the formation of high-low junctions and p-n junctions. The standard method for passivation of silicon is the thermal oxidation (SiO_2) at high temperature (~ 1000 ˚C). On high-resistivity silicon this method is capable of providing extremely low surface state densities. However, for low substrate resistivity, the passivation quality depends on the doping type [176]. Beside, other problems such as the UV stability and problems arising from the high temperatures during the thermal oxide growth can severely degrade the bulk carrier lifetime thus impede this approach being desirable out of production cost and throughput consideration.

In recent years significant efforts have been devoted to develop low temperature (< 500 ˚C) surface passivation schemes as an alternative to the high temperature oxidation of silicon, among which the most successful method turned out to be the plasma enhanced chemical vapour deposition (PECVD) of silicon nitride (SiN_x) [177]–[179]. Hydrogenated amorphous silicon nitride layers (a-SiN_x: H) have become a very important part of modern silicon photovoltaic technology, achieved during antireflection coating. Hydrogen contained in the SiN_x layer diffuses to bond with the defect dangling bonds and this is known to be effective for interface, surface and bulk passivation [180]. The bulk, or defect passivation is achieved by driving hydrogen into the crystalline silicon by a short anneal [181]–[184]. In the meanwhile, the surface passivation is improved via reducing the number of dangling bonds and creating a positive field effect by K+ centres [185].

1.6 Conclusion and objectives of this project

Despite the remarkable price reduction in the past few years, the cost of solar cell processing and module fabrication remains high, especially the sawing step still consumes approximately 50 % of the expensive silicon material. The wire sawing process is wasteful of materials and expensive, meanwhile, ribbon growth technology is not as well commercialized as expected due to the issues described above. This provides the motivation of developing a new cost competitive approach to produce silicon solar cells.

In spite that silicon is a covalently-bonded diamond cubic structure crystal, it has been proved to be ductile at elevated temperature (> 900 ˚C). The recrystallization of silicon takes place just as it does in metals, provided that a higher temperature and a longer annealing time are employed. The size, morphology and crystalline perfection of the recrystallized grains are comparable to those of metals. Manufacturing silicon solar wafers using conventional industrial hot deformation was firstly attempted in the late 1970s and early 1980s, and was found promising. However, the work was discontinued because the electrical properties of the deformed silicon were extremely poor. At that time it was assumed that the only approach to make sufficiently high quality (electrically) material was by obtaining essential single crystal material. The importance of impurities and their interaction with extended defects leading to the deterioration of minority carrier diffusion length was not profoundly recognized. The high efficiency of modern solar cells can only be achieved by the incorporation of gettering techniques to remove harmful impurities and the subsequent electrical passivation of any remaining impurities or defects. In the earlier work, not only was the deformation carried out in

very filthy metallurgical conditions with no real attempt to keep it clean but neither the crucial gettering nor passivation steps were applied to the deformed material.

The main motivation of this project is to revisit high temperature silicon deformation, but, in contrast to earlier work, use very high purity conditions for deformation and apply subsequent gettering and electrical passivation to determine if the resultant silicon material maintain sufficiently good electrical quality for solar cell fabrication, thus answer the question whether it is feasible to produce silicon wafers via cheap hot rolling of silicon material under clean conditions.

The project comprises four steps, namely:

1. Construction and characterization of the deformation equipment,
2. Investigation of the optimal deformation and annealing conditions,
3. Deformation and annealing of polycrystalline silicon,
4. Characterization of the electric properties of deformed and annealed polycrystalline silicon after gettering and passivation.

Correspondingly the structure of the remainder of the thesis is as follows: Chapter 2 introduces the experimental techniques used during the investigation, while Chapter 3 describes the construction of the deformation rig and associated characterization of the clean conditions. Chapter 4 details the attempts to obtain the optimal deformation and annealing parameters by deforming single crystalline silicon samples, in which the dislocation structure, the defect morphology of deformed and annealed sample under varying deformation and annealing conditions were investigated using preferential etching/SEM and TEM. In Chapter 5 the experimental investigation of deformation and annealing of polycrystalline silicon is addressed, primarily on the microstructure

evolution of the as-received material during pre-annealing, after deformation and subsequent annealing by preferential etching/SEM, TEM and EBSD. The HR-EBSD cross-correlation method was applied to quantitatively investigate the dislocation distribution and structure of the polycrystalline silicon for the first time, and the obtained results are presented in Chapter 6. The deformed and annealed polycrystalline silicon was then subjected to gettering and passivation process, the minority carrier lifetime after each step was measured and the recorded details and results are reported in Chapter 7. Finally, in Chapter 8, the results and conclusions of the present work are summarised and suggestions for future work are made.

Chapter 2

Experimental method

2.1 Introduction

This chapter describes related sample preparation details and experimental techniques employed in this study. In order to investigate an achievable deformation condition provided by the self-constructed deformation rig (the construction details are presented in Chapter 3), single crystalline silicon (sc-Si) samples were firstly deformed under different conditions. A polycrystalline silicon (polysilicon) sample grown by chemical vapour deposition (CVD) was subsequently deformed using suitable deformation conditions obtained from the experiments conducted on sc-Si samples. Subsequent annealing was applied to enhance the recrystallization process in both materials. The microstructural evolution of both sc-Si and polysilicon samples after deformation and subsequent annealing were revealed by defect etching and scanning electron microscopy (SEM), while the crystallographic information and GND density distribution of poly-Si samples were additionally investigated by the high resolution electron backscattered diffraction (HR-EBSD) cross-correlation method. Plastic deformation of crystalline silicon gives rise to a large quantity of dislocations, which can then be annihilated by annealing at elevated temperatures due to static recovery and recrystallization. The detailed defect morphology of both sc-Si and poly-Si samples was examined by transmission electron microscopy (TEM). The focused ion beam (FIB) lift-out technique was used to fabricate the TEM specimens.

2.2 Silicon sample fabrication

High purity sc-Si bulk material produced by the Czochralski method and high purity semiconductor grade CVD polysilicon bulk material obtained by the Siemens process [186] were used in this project. Both materials are undoped and commercially available, provided by Prof. Robert Falster from SunEdison. A brief description of the key properties and sample preparation details are given in this section.

2.2.1 Silicon bulk samples for deformation

The majority of the as-received sc-Si material was initially cut into cubes in dimensions of 10 mm x 10 mm x 10 mm for deformation tests. The remaining material was cut into samples of size 15 mm x 15 mm x 10 mm to optimize the deformation behaviour. The heights of all samples remain the same as 10 mm due to the critical dimension of deformation rig assembly (see Section 3.2). High purity polycrystalline silicon was cut into size of 20 mm x 20 mm x 10 mm for the purpose of producing a piece of sufficiently large deformed sample for the minority carrier lifetime tester(see Section 2.12).

After silicon samples were sliced out from the raw bulk material by Buehler ISOMET 5000 using diamond wafering blade (blade number 11-4245), they were subjected to saw damage etching (planar etch, to be described in Section 2.5) to improve surface smoothness so to minimise friction effect between the sample and the contacting components during deformation.

2.2.2 Sliced silicon specimens for annealing and microstructure investigation

After high temperature deformation, deformed silicon samples were mechanically sawn into 1.5mm thick slices parallel and perpendicular to the compression axis, respectively. These samples were then subjected to planer etch to remove damaged layers introduced by sawing.

In order to investigate the surface microstructures and provide an initial flat reference surface for defect revealing etching, deformed and annealed specimens were ground and polished. The equipment used was Kemet lapping wheels. Grinding and polishing were performed manually, with water as the lubricant for grinding, Kemet GW2 for diamond polishing, and colloidal silica liquid for Syton polishing.

The grinding and polishing steps are as follows:

1. Samples mounted on glass discs (25mm in diameter) by a thin layer of wax using hot plate.
2. P2500 grit grinding for 3 minutes.
3. 6μm diamond polish, performed at 90˚ to previous step until grinding marks are not visible.
4. 1μm diamond polish, performed at 90˚ to previous step until 6μm polishing marks are not visible.
5. Chemo-mechanical Syton polishing until all visible surface damage was removed.

2.3 Cleaning

The fundamental difference between this work and previous research in the 1970s [50], [51], [55] is the compression experiments in the work were controlled strictly under clean conditions to the greatest extent possible. Henceforth, the amount of impurity introduced into the silicon samples was attempted to the minimum content. It is well known that metallic impurities are detrimental to the minority carrier lifetime in silicon (see Chapter 1 Section 1.3.4), and these impurities diffuse fast into the material at high temperature, therefore it is of great importance to maintain the cleanness of deformation components and conditions.

Standard RCA cleaning steps [187] were carried out to clean deformation components and silicon specimens prior to any treatments in the clean room. This process removes any native oxides and any organic residues (such as dust particles, grease or silica gel/ionic (metallic) contaminants) from the sample surface. The specific steps are:

1. RCA-1: Ammonia, hydrogen peroxide and deionized water mixed in the ratio 1:1:5 for 15 minutes at 75 ˚C to 85 ˚C.
2. Hydrofluoric acid (40%) for 10 seconds (exclusively for silicon specimen).
3. RCA-2: Hydrochloric acid, hydrogen peroxide and deionized water mixed in the ratio 1:1:6 for 15 minutes at minutes at 75 ˚C to 85 ˚C.
4. Hydrofluoric acid (40%) for 10 seconds (exclusively for silicon specimen).

The deformation components and samples were rinsed in deionized water after each cleaning stage and dried by nitrogen gas blowing. Deformation components were aligned and constructed in one piece as soon as possible to avoid any undesired contamination. The cleaning work was greatly aided by Dr. Radka Chakalova.

Subsequent annealing kit, described in the following section, was cleaned sequentially by acetone, methanol and hydrofluoric acid (40%), before rinsing by deionized water.

2.4 Subsequent annealing after deformation

In order to reduce the internal stress input by large amount of plastic deformation, deformed silicon samples were subjected to subsequent high temperature annealing (usually $\geq 0.8\ T_m$). Such high temperature treatments activate cross-slip of dislocations and facilitate them to move out of slip planes. This is thought to initiate dislocation annihilation and correspondingly an overall reduction of dislocation density. In this work, specimens were annealed at 1250 ˚C, 1375 ˚C and 1400 ˚C, respectively, for durations varying from 15 minutes to 2 hours.

All annealing treatments were carried out using high purity quartz ampule in an Argon ambient. Following the standard cleaning process of both specimens and quartz ampules, silicon specimens were first placed in one-end sealed silica ampules. The quartz ampules used in this work are shown in Figure 2.1. The ampules were then evacuated and filled with pure argon, then sealed at the other end to guarantee the specimens were annealed under protecting gas ambient and clean conditions. These ampules were then placed in a pre-heated chamber furnace Carbolite RHF 16/3. After the required amount of annealing time, the ampules were slowly cooled down in the furnace to room temperature. The cooling profile is approximately 4 ~ 5 ˚C·min^{-1} between 1400 ˚C and 200 ˚C, followed by 1~ 2 ˚C·min^{-1} between 200 ˚C and the room temperature. The annealing work gained substantial help from Mr. Ian Lloyd in the Furnace room.

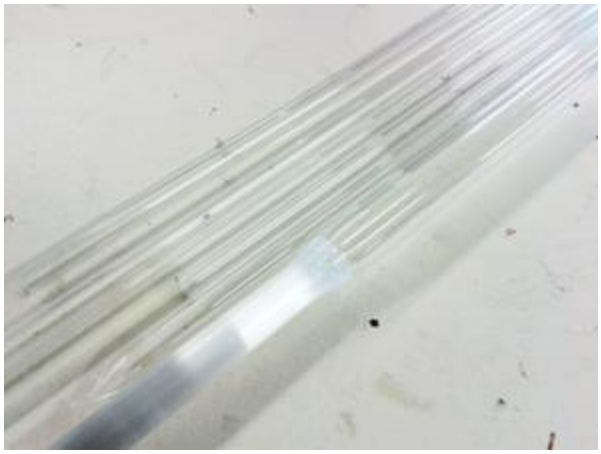


Figure 2.1.High purity quartz ampules used for high temperature annealing in this work.

2.5 Etching

Two types of wet chemical etching were used in this study. Bulk etching was used to remove uniform layers of material from the silicon surface. It is especially crucial to apply this step after the sawing process to remove damage. A preferential etching technique was used to reveal the intersection points and lines of crystal defects (*i.e.* dislocations, grain boundaries and stacking faults) with the material surface appearing as small etch pits (for dislocations) or etch groove (for grain boundaries and stacking faults). Thus these defects become visible under optical microscope (OM) and SEM.

2.5.1 Planar etching

A planar etch, comprising 8 % HF (40 %), 75% HNO_3 (69 %) and 17 % CH_3COOH, was used to remove uniform layers of silicon. The working process of this reaction can be described as follows [188]:

1. The nitric acid forms a thin layer of silicon oxide on the sample surface.
2. The hydrofluoric acid removes this thin layer of silicon oxide, according to the reaction equation below:

$$3Si + 4HNO_3 + 18HF \xrightarrow{\text{yields}} 3H_2SiF_6 + 4NO + 8H_2O$$ Equation 2.1

3. The acetic acid works as a buffer of the etch solution so the etching process can be well controlled.

The sample thickness was measured by micrometer after the etching and the approximate etching rate is 1.5 ~ 2 μm·min^{-1}. The total amount of saw damage removed by planar etch from sample surfaces in this work is approximately 50μm.

2.5.2 Preferential etching

The basic idea of preferential etching is to elucidate extended defects intersecting the sample surface by a small pit or groove so that they can be observed under microscopes. The preferential etching process also relies on oxidation and dissolution. The silicon atoms at, or adjacent to crystal defects such as dislocations and grain boundaries are oxidized preferentially by the etchant [189]. In this work, an etch comprising 0.3M CrO_3 and HF (40%) mixed in the ratio 5:4 was used to reveal the presence of dislocations, grain boundaries and stacking faults in silicon. This is also referred to as the **Sirtl** etch [190], with an etch rate 3 μm·min^{-1}. Due to the high dislocation densities, specimens were generally etched for 30 seconds.

The etch pits and grooves enable the grain structure and dislocation density to be visible and measured under SEM using etch pit counting. Etch pit counting is capable of measuring dislocation density as high as the order of 10^{13} cm^{-2} (based on observation of this work). The scanning electron micrograph in Figure 2.2 illustrates an etched surface microstructure containing dislocation etch pits, grain boundary and stacking faults grooves (observed in this work).

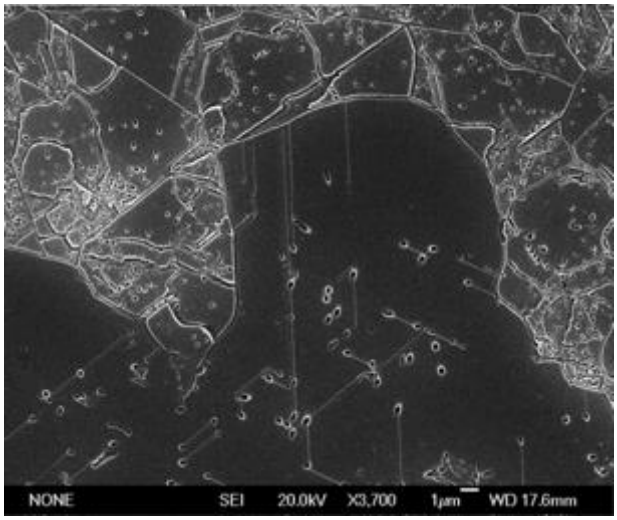


Figure 2.2. Etch pits and grooves revealed by Sirtl etch in polysilicon deformed at 1150 ˚C by 10 % and subsequently annealed at 1400 ˚C for 15min in this work, imaged using a Field Emission JEOL JSM-6500F scanning electron microscope.

2.6 SEM to image etched sample surface

SEM produces topographic information of sample surface by scanning across with a focused electron beam. The most common mode of detection is by collecting secondary electrons emitted by atoms with which the electron beam interacts. In this work, a JEOL-JSM 840A, using a tungsten filament cathode electron source and a Field Emission SEM JEOL-JSM 6500F, equipped with a cold cathode source, respectively, both operating at 20kV, were employed for the microstructure examination of the etched sample surfaces.

2.7 TEM used in defect morphology investigation and dislocation density measurement

TEM is the most widely used technique used for the observation of dislocations and other crystal defects, such as stacking faults, twin and grain boundaries, and voids. In this work, TEM was used for configuring detailed characters of defects associated with uniaxial compression and annealing processes. The nature and location of dislocations, the average dislocation density and sizes were investigated for each specimen. In some selected cases the dislocation Burgers vectors were determined. One thing to note is that it is difficult to measure dislocation densities greater than about 3×10^{13} lines/cm^2 using TEM[191].

JEOL 2000FX microscope, operating at 200kV, was used for the TEM examination. The microscope was equipped with a double tilt holder, with one tilt axis being eucentric. All TEM investigations used in this work were carried out using diffraction contrast analysis, the theory and practice of which have been described in several textbooks [83], [191], [192].

2.7.1 FIB lift-out technique to fabricate TEM specimens

A focused ion beam, also known as FIB, is a scientific instrument that resembles a SEM but uses a finely focused beam of ions (usually gallium). Secondary electrons are generated by the interaction of the ion beam with the sample surface and can be used be obtain high-spatial-resolution images. Unlike an electron microscope, due to the energies of the incident ions, FIB is inherently destructive to the sample surface. Such a sputtering capability of ion beam enables FIB precise machining or fabricating abilities at the micro-/nano-scale. In conjunction with the gas-injection capabilities, which

enables ion-beam-activated deposition and enhanced etching, a range of sample fabrication schemes are possible [193].

In this work, FEI-FIB 200 was used to fabricate thin foils of silicon from the bulk material for subsequent TEM observation. Four major steps are involved in the specimen preparation process, namely platinum deposition, preliminary milling, delicate polishing and final lift-out. The detailed fabrication methods are described and illustrated as follows:

1. Platinum deposition. A thin protective layer (1µm) of platinum is deposited on the specific area where the sample was chosen from, see Figure 2.3. The deposited platinum layer protects the material underneath from ion implantation and beam damage. In this process the incident ion beam cracks hydrocarbon precursor gases, leading to local deposition of the conducting material (platinum). The beam current used in this process is 100pA.

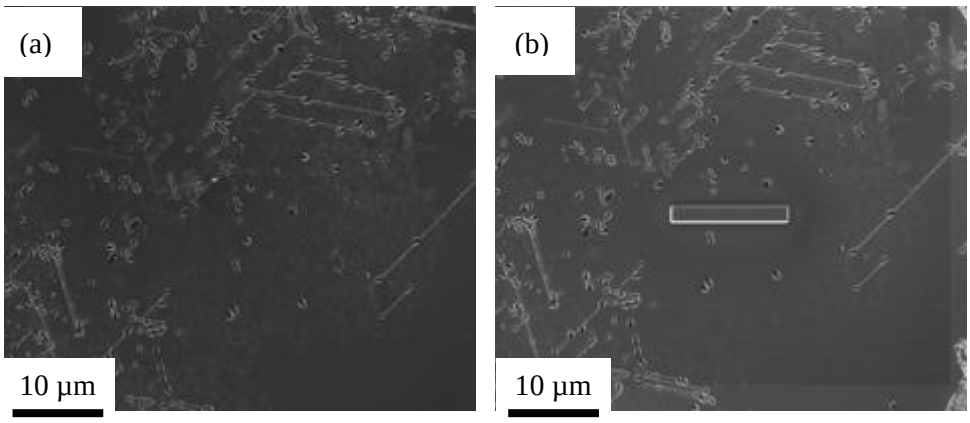


Figure 2.3. (a) Pre platinum deposition; (b) Post platinum deposition.

2. Preliminary milling and polishing from both sides of the specimen, details see Figure 2.4.

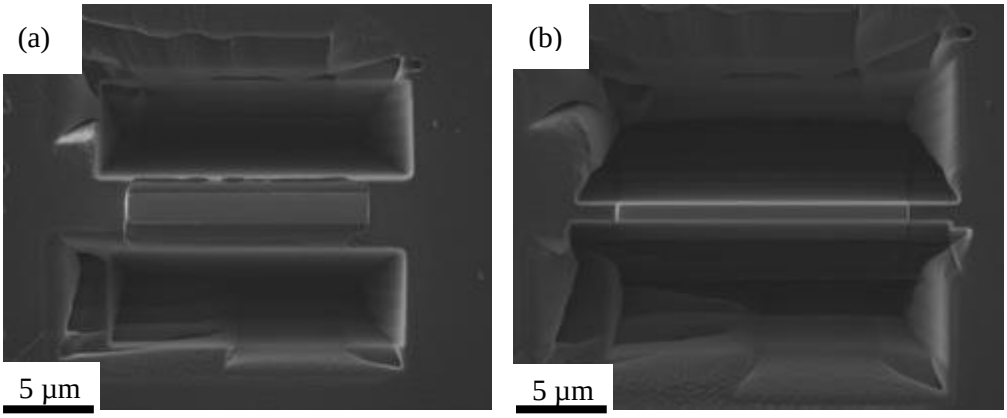


Figure 2.4. (a) Two deep staircases on either side of sample area, leaving a 1 µm gap between the edge of staircase pattern and the edge of platinum layer. The size of these staircases is usually 20 µm x 8 µm x 8 µm. The beam current used at this step is 7 nA or 5 nA; (b) Preliminary polishing towards sample from both sides, until the sample is thinned down to 500nm width. The beam current used at this step is 1 nA.

3. Delicate polishing process, details see Figure 2.5.

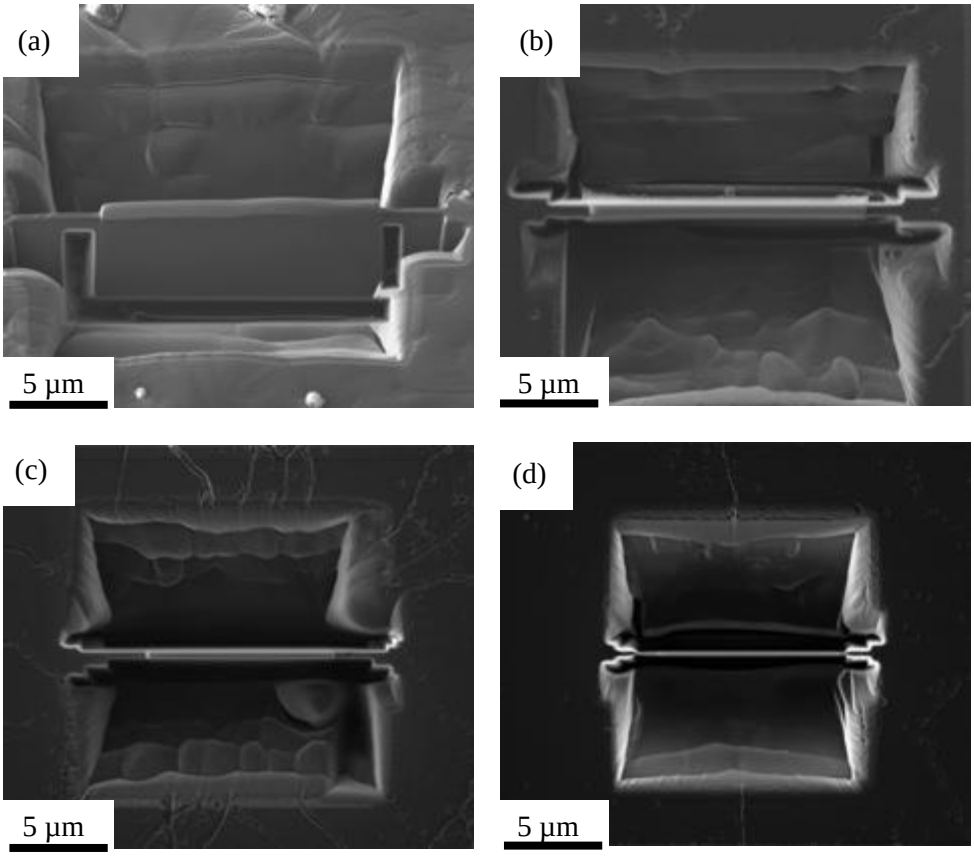


Figure 2.5. (a) Tilt the specimen by 45˚ and refine three boxes to mill the 'goal post' etch with a current 300 pA. The completeness of the mill can be checked by the projection of the patterns on the back wall of the staircase; (b) Specimen plane viewed post box cutting; (c) Tilt the specimen by 1˚ and polish the sample from both sides, until the sample is thinned down to 300 nm width. The beam current used at this step is 300 pA; (d) Tilt the specimen by 0.5˚ and polish the sample till 100nm width with a 100 pA beam current.

4. Release the specimen from the matrix and prepare for the ex-situ lift-out, see Figure 2.6.

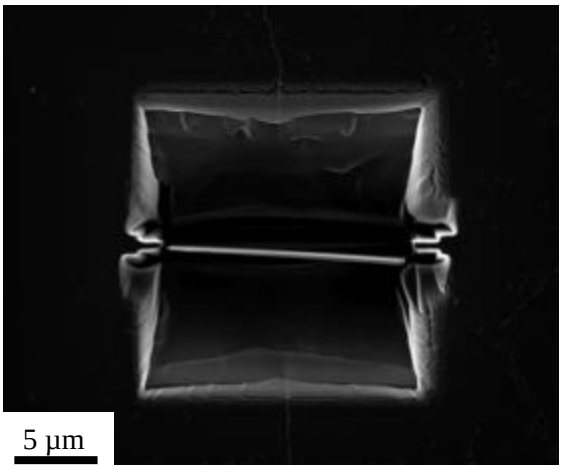


Figure 2.6. Tilt the specimen by 10˚ and release the sample for lift-out.

2.7.2 Diffraction contrast in TEM

The image obtained in the TEM is reveals the variation in the intensity of the electron beam leaving the bottom surface of the specimen in a direction selected by the object aperture. In the case where the direct beam is selected, the image appears dark where the electrons have been scattered out of the incident beam path. This is called bright field image. In contrast, by imaging using a selected diffracted beam, the image appears bright where electrons have been scattered into the selected diffracted beam path relative to a dark background, which is called dark field image. Therefore, contrast arises due to the perturbation of the local diffraction conditions. The contrast mechanism for a dislocation depends on the conditions of observation. Schematic ray diagrams of a conventional TEM are shown in Figure 2.7.

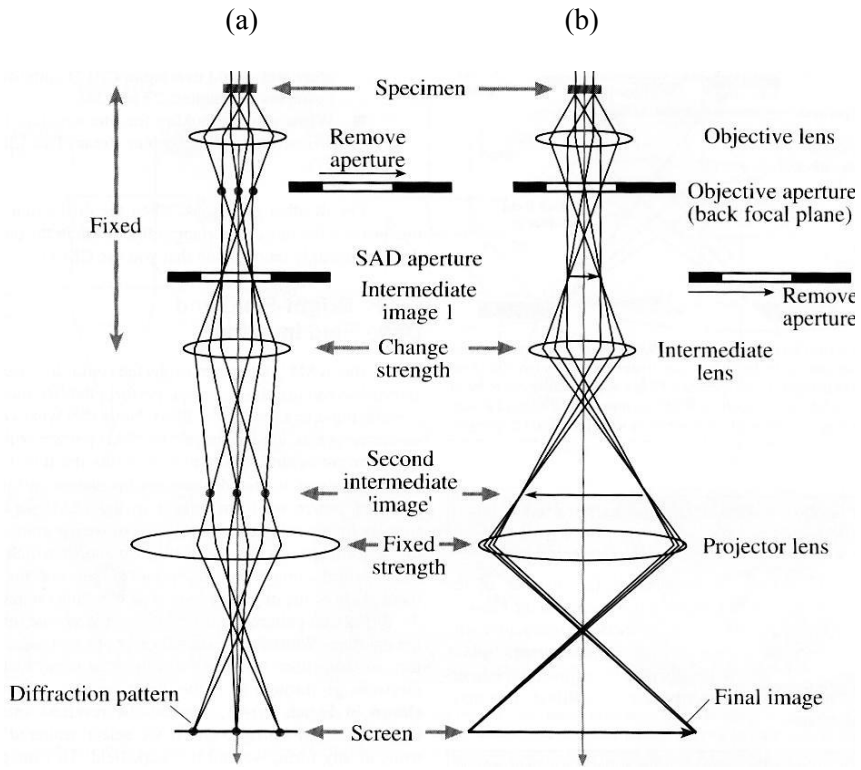


Figure 2.7. Schematic illustrations of two basic operations of the TEM imaging systems involving projecting: (a) the diffraction pattern; (b) the image on to the viewing screen. The intermediate lens selects either the back focal plane or the image plane of the objective lens as its object [84].

To undertake diffraction contrast imaging, a uniform thin crystal (a foil) is tilted so that a set of lattice planes with Miller indices g= (hkl) are at an angle θ to the incident electron beam, where θ is close to the Bragg angle θ_B. The latter is given by $\lambda = \sin\theta_B$ where λ is the wavelength of the electrons illuminating the specimen, $d^2 = {a^2}/{h^2 + k^2 + l^2}$ and a is the lattice parameter.

The deviation from the Bragg condition is characterised by the vector **s**, called the deviation parameter and defined as the vector parallel to the beam from the point g to the Ewald sphere in reciprocal space. For a dislocation to be visible it must distort the planes which are forming the diffracted beam, thus the Burgers vector, **b**, of a

dislocation can be determined from images if the conditions are chosen to satisfy the dislocation contrast criteria **g·b**= 0. The conventions used in **g·b** analysis are listed in Table 2.1.

Table 2.1 Conventions used in the TEM investigation

1. Indexing Crystallographic planes and directions have been indexed using a right handed system
2. Vectors **g**= reciprocal lattice vector describing the reflection satisfying Bragg's law in the operating diffraction conditions **s**=deviation parameter **b**=Burgers vector associated with a dislocation **u**=unit vector parallel to the line of a dislocation
3. Sign of s **s** is taken as positive when the crystal is tilted past the exact Bragg condition so that in the diffraction pattern the excess (bright) Kikuchi line lies outside the strongly diffracted beam
4. Dislocation contrast criteria For a dislocation with Burgers vector **b**, when imaged in a reflection **g** (a) **g·b**≠0; dislocation in contrast (b) **g·b**=0 whilst g·(bxu) ≠0;dislocation shows residual contrast (c) **g·b**= **g·(b**x**u)**=0;no dislocation contrast

2.7.2.1 Kinematical condition (s>0)

Figure 2.8 shows schematically an edge dislocation in a thin foil. In the region far from the dislocation, the crystal is tilted significantly away from the Bragg condition and the incident beam is not strongly diffracted. While near the dislocation the crystal planes are bent into the Bragg condition by the dislocation strain field, which results a stronger scattering of electrons into the diffracted beam. Thus dislocation would appear as a dark line in bright field image and bright line in dark field image [194].

2.7.2.2 Dynamical condition (s=0)

In dynamical condition, the crystal is tilted in order to satisfy the Bragg condition (**s**=0), and the dislocation strain field tilts the lattice planes away from the Bragg conditions. Therefore we would expect the dislocation to appear as a white line in bright field image and a dark line in dark field image.

2.7.2.3. Weak beam conditions (s>>0)

Weak beam dark field (WBDF) method provides strong contrast of crystal defect to the matrix. The positions of dislocation lines are well defined with respect to the dislocation cores and are also relatively insensitive to the both the foil thickness and the position of the dislocations in the specimen. As in this condition the specimen is tilted such that only very highly strained planes near the dislocation core satisfy the Bragg condition. The weak beam technique provides the highest resolution of conventional diffraction contrast.

The diffraction conditions and diffraction patterns observed in the microscope used in the three modes of diffraction-contrast imaging outlined above are shown in Figure 2.9 [194].

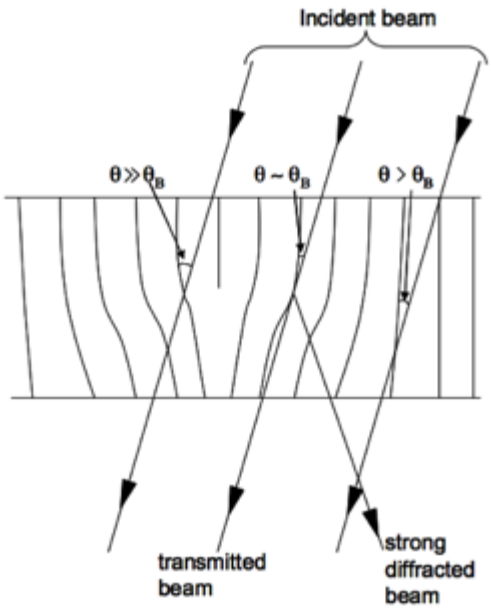


Figure 2.8. Schematic representation of an electron transparent single crystal containing a single dislocation (represented by the extra half-plane), θ is the angle between the electron beam and the lattice plane. When the planes immediately to the right-hand side of the dislocation are bent so that so that they closely approach the Bragg condition ($\theta = \theta_B$, the Bragg angle) the intensity of the direct beam emerging from the crystal is reduced. The dislocation appears as a black line in the bright field image. This corresponds to 'kinematical bright-field' diffraction conditions [194].

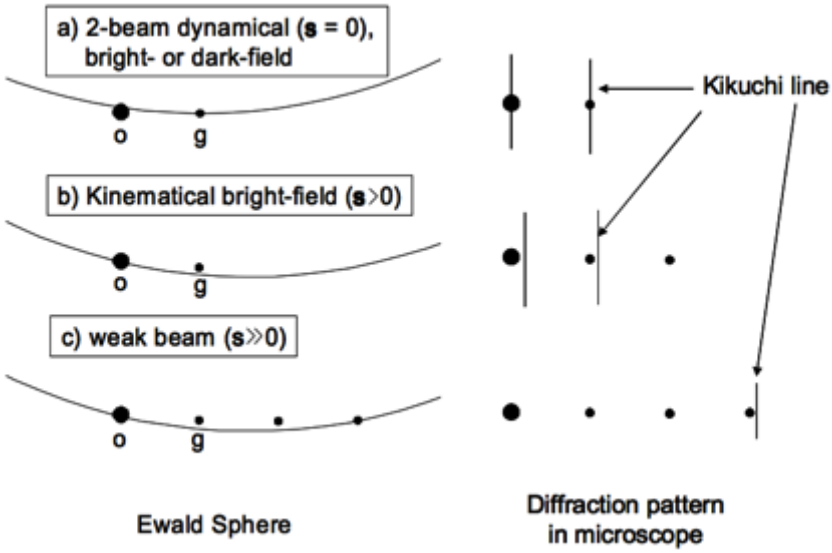


Figure 2.9. Schematic representation of the diffraction conditions used in diffraction contrast imaging, where s is the deviation parameter: (a) Two-beam dynamical; (b) Two-beam kinematical; (c) Weak beam. In each case the Ewald sphere is sketched on the left-hand side, and a schematic diffraction pattern showing the position of the relevant Kikuchi lines on the right-hand side. The curvature of the Ewald sphere has been exaggerated for clarity [194].

2.8 Electron backscatter diffraction

2.8.1 Conventional EBSD for crystallographic information

The electron backscatter diffraction (EBSD) technique provides the versatile microstructural-crystallographic information of a crystal material, including crystal mapping orientation, crystal type, and perfection over a wide range of scanning step size. Commercially available EBSD is conducted using a conventional SEM equipped with an EBSD detector. EBSD maps are constructed by moving a focused beam of electrons point by point across the surface of a bulk sample in a SEM. These electrons penetrate the sample surface and undergo elastic and inelastic interactions with the sample. The interactive volume size of ~20 nm x 80 nm x 20 nm to ~ 30 nm x 400 nm x100nm depending on the electron gun type (field emission gun or tungsten filament) [195], SEM settings and the nature of materials. At each point, some of these electrons backscattered from the sample are collected by the EBSD detector comprising a scintillator screen coupled generally by a lens, to a photon sensitive imaging detector (typically a sensitive charge coupled device (CCD) camera) to form an electron backscatter diffraction pattern (EBSP) [196]. The EBSD pattern (EBSP) generally comprises a large number of nearly straight bands, termed Kikuchi bands, formed by the intersection of Kossel diffraction cones with the plane of the detector, as shown in Figure 2.13 (b). In the SEM chamber, the sample is generally highly tilted (60˚ to 80˚) towards the detector, as is depicted schematically in Figure 2.13 (a), to increase the quality of the pattern obtained.

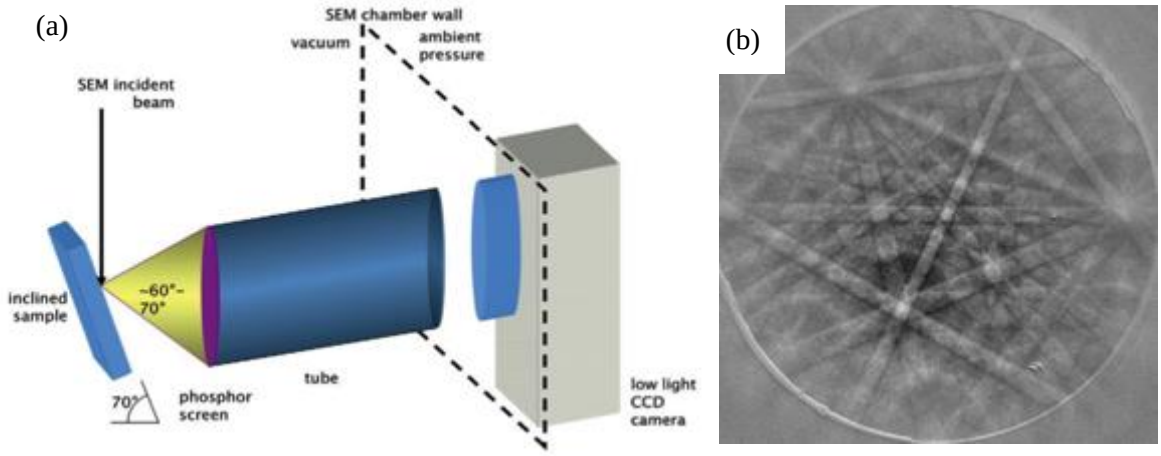


Figure 2.10. (a) Schematic diagram to show the standard experimental set-up of EBSD system in a SEM chamber [196]; (b) Typical captured EBSD pattern of silicon with background correction obtained in this work.

In this work, EBSD measurements were made on two independent equipment set up with the same sample tilt of 70˚. As regards to the radial section (Face A), illustrated in Chapter 5, the EBSD scans were operated on a JEOL-840A with accelerating voltage at 20 kV and a probe current of ~ 30 nA. At each measurement point a background subtracted EBSD pattern was recorded at 12 bit depth with a Digiview II using 4x4 hardware binning with OIM DC v5.3 (TSL-EBAX) EBSD system. No artificial addition of gain and black level were applied. Each EBSD map contained approximately 40,000 points with 225 x 225 pixel EBSPs. The EBSP collection time was approximately 2 hours. In contrast, as regards to the axial section (Face B), the EBSD scans were conducted on a FE-SEM JEOL JSM-6500F with accelerating voltage at 20 kv and a probe current of ~ 17 nA. EBSD patterns were recorded at the full -1k x 1k pixel x 12 bit deep resolution of the peltier cooled CCD camera and saved to hard disk for batch-wise off-line analysis. The data acquisition rate was approximately 1 pattern/sec with the camera gain kept low so as to achieve good signal to noise and the 100 µm x100 µm

area was mapped at a step size of 0.5 μm in approximately 14 hours. For both sections, areas of 100 μm x 100 μm were mapped using a square array with step size of 0.5 μm.These EBSPs were subsequently analysed by CrossCourt3 cross-correlation software in approximately three hours using a high performance computer that has six cores Intel® Core ™ i7-3930k CPU@ 3.20 GHz and 32 GB memory with thirty 64x64 regions of interest (ROI). Grains were demarked using OIM A v5.3 in which a grain boundary tolerance of 7˚ and minimum grain size of 5 points were applied for the annealed sample microstructures. Reference points were selected from the grain interior where high image quality (IQ) points were generated.

High and low band pass filters were applied to each Regions of Interest (ROI) in the Fourier domain to remove the low frequency background intensity variation and high frequency noise. In order to attain more statistical reliable measurement, robust fitting is used to find the best fit solution for more than four ROIs. Threshold values of Peak Height (PH) > 0.25 and Mean Angular Error (MAE) < 0.01 rads were used.

2.8.2 HR-EBSD cross-correlation method for GND density

Each Electron Backscatter Pattern (EBSP) contains rich information of crystal lattice structure such as lattice type, lattice arrangement and lattice distortion. The crystalline information obtained from the conventional EBSD systems is ‘geometrical’, discriminating phase or orientation through a Hough transform-based analysis of Kikuchi band positions and in some cases widths. Information like lattice distortion, i.e. stored deformation (both plastic and elastic strain) is more difficult to quantify in EBSPs.

In description of dislocations in crystals, dislocations could be classified the stored dislocations into two different categories, namely, the Statistically Stored Dislocations (SSDs) with net Burgers vector of zero and Geometrically Necessary Dislocations (GNDs) with non-zero net Burgers vector [197], [198]. SSDs are formed by random mutually trapped dislocations in the form of dipoles and multipoles during plastic deformation, and have no net geometrical consequence (e.g. are not associated with lattice curvature) as the total structure self-terminates within the volume, therefore cannot be detected by EBSD. Whereas on the other hand, GNDs are generated as accumulation of excess dislocations within a Burgers circuit to satisfy the geometrical compatibility, due to geometrical constraint of the crystal lattice, hence are closely related to lattice curvature and readily detected and characterized by EBSD [199] according to Nye's theory[197].

The presence of SSDs and GNDs both cause pattern blurring in EBSPs. Theoretically all stored dislocations should be quantitatively analyzed by measuring the degradation level of EBSPs, which is indicated by image quality maps. However, there are various critical factor deteriorating the image quality including the camera setting, beam interactive volume size, electron beam stability and surface contamination. Sometimes these factors play a dominant role in image quality rather than the genuine stored dislocation content [200]. Therefore practically EBSD is not yet suitable for the quantitative characterization of both SSDs and GNDs. However, as stated earlier, in addition to pattern degradation, stored GND content also result in rotation gradient within the crystals (lattice curvature), as shown in Figure 2.11(b) and (c), which can be readily and reliably measured using EBSD and is developed into a mature method for determining GND density.

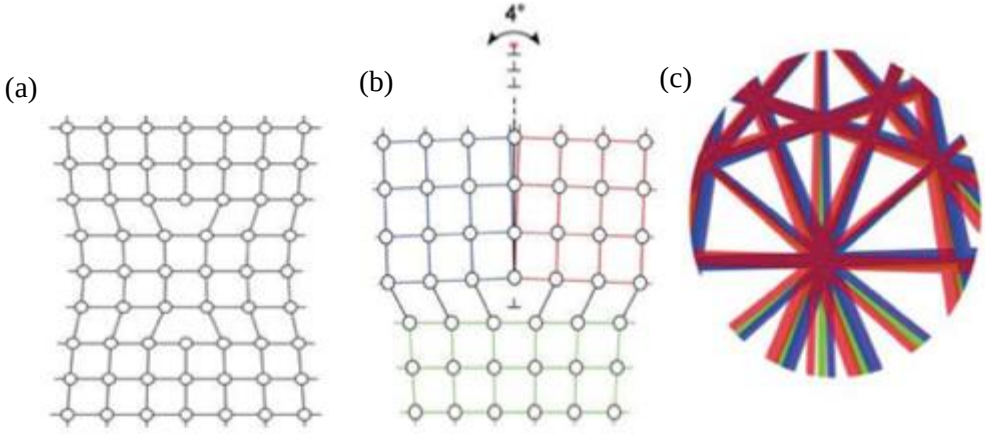


Figure 2.11. Schematic diagrams showing (a) the presence of an edge dislocation dipole in lattice and (b) the presence of lattice curvature caused by GND array in lattice, (c) the effect of GND on EBSPs [11].

There have been several attempts to use conventional 2-D Hough transform-based EBSD to provide the orientation gradient and determine the GND densities [201]–[203]. However, the relatively low angular resolution of such EBSD measurements has led to difficulties of studying plastic deformation. The problems lie either in the generation of high noise level on the GND densities that mask many of the important features in the dislocation structure, or in requiring sampling or averaging over relatively large step sizes so as to reduce problems with noise, which leads to removal of the shorter range fluctuations in the GND density distribution [204]. However, significant progress has been made on dislocation density assessment by measuring lattice curvature by EBSD technique in the past few decades, especially the crucial development of cross-correlation based high resolution EBSD (HR-EBSD) technique, which allows both high angular resolution and high spatial resolution to be achieved [199]. HR-EBSD is an off-line image processing method and it requires high quality full resolution EBSPs to be captured during EBSD scans. The aim is to extract the highest sensitivity, leading to high fidelity GND density, lattice rotation and elastic strain data. The highest angular

resolution (~0.005˚) was achieved by using image cross-correlation method in 2006 [199], comparing to the low angular resolution (0.5˚~1˚) attained by conventional Hough transform-based analysis [205].

Lattice distortion within the sample leads to shifts in zone axis positions in the EBSD pattern. In cross-correlation based analysis, a reference pattern is selected from the centre area of each grain. By comparing the relative patterns shifts of the thirty Regions of Interests (ROI) between the reference EBSP and tested EBSPs within the same grain, the displacement gradient tensor (the symmetric part corresponds to the elastic strain and the antisymmetric part corresponds to the lattice rotation) of the specific probing point can be back calculated. Therefore the lower bound GND density can be estimated from maps of lattice rotation gradients. The reader is referred to [206] for detailed mathematical deduction. On the other hand, the derivation process is illustrated as following:

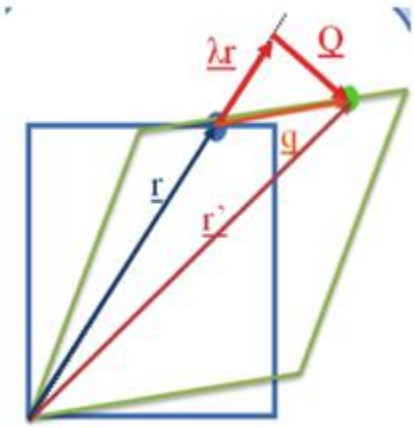


Figure 2.12. Schematic diagram shows the deformed (green square) and undeformed 2D lattice structure (blue square) due to elastic strain and body rotation and resultant shifts on EBSD [206].

A systematic comparison of GND measurement sensitivity using HR-EBSD and Hough-based analysis were conducted by Adams by examining the GND measurement noise floor generated using these two methods on a dislocation free semiconductor germanium, and Wilkinson and Randman [207] by comparing the GND distribution field near microindents on a large grains Fe. It was concluded that the lower bound GND content noise level/dislocation density limit was estimated as ~ 1.0 x 10^{12} m^{-2} using HR-EBSD and ~ 1.0 x 10^{14} m^{-2} using Hough based analysis.

The GND density analysis using HR-EBSD cross-correlation technique was greatly aided by Dr. Jun Jiang and Prof. Angus Wilkinson.

2.9 Passivation

Both surface and bulk passivation were utilized in this work. As regards to surface passivation, a silicon nitride film was deposited by plasma-enhanced chemical vapor deposition (PECVD) to improve surface recombination properties. It aims at eliminating surface recombination loss to ensure that measured minority carrier lifetime is exclusively affect by bulk minority carrier recombination activities. The instrument employed is an Oxford Instruments (OI) Plasmalab 80+PECVD system. Hydrogen bulk passivation used in this study was conducted using the same equipment. Hydrogen ions were generated from a remote gaseous source (pure ammonia NH_3) and diffused into the silicon bulk to passivate non-saturated bond defects. Detailed experimental parameters and procedures are presented in Section 7.2.

2.10 Gettering

Gettering is a process of reducing or eliminating undesired metallic impurities or other kinds of crystalline defects in a wafer by localizing them in defect containing regions

away from the device active regions or by removing them completely from the silicon wafers to a zone where the solubility is remarkably enhanced [171]. The gettering implemented in this work is phosphorus diffusion gettering (PDG) and was conducted at Tetreon ®. The detailed experimental details and thermal profiles are presented in Chapter 7 Section 7.2.

2.11 Electrical properties characterization

The main technique used in the analysis of electrical properties is a quasi-steady-state photo-conductance (QSS-PC) WCT-120 lifetime tester from Sinton instrument ® with a small coil of 15 mm in diameter, and the schematic is shown in Figure 2.13. It enables the effective minority carrier lifetime to be measured as a function of the excess carrier concentration [208]. The carrier recombination lifetime is the average time for which a carrier can exist in an excited state after electron-hole generation, before it recombines. This contactless technique measures the photo-conductance in a quasi-steady-state mode by supplying an intense pulse of illumination upon the sample. This pulse decays slowly relative to the sample's minority carrier lifetime. The illumination generates excess free carriers within the sample, which can then recombine. As the pulse is long relative to the carrier lifetime, a steady state situation develops where carrier lifetime generation matches carrier recombination, as detailed in Equation 2.2 below. An AC voltage is applied to the coil underneath the sample stage, inducing eddy currents in the sample. The magnitude of the eddy currents is dependent on sample conductivity, and is quantified by the resulting change in impedance of the coil. A light sensor measures the intensity of light, which can then be converted into the minority carrier generation rate *G*. The eddy current coil underneath the sample measures the sample conductivity, which can be converted into the excess carrier density Δn [208].

$$G = \frac{\Delta n}{\tau eff}$$ Equation 2.2

G is the minority carrier generation rate including minimal thermal generation,

Δn is the excess minority carrier density under steady state,

τeff is the effective minority carrier lifetime at an excess minority carrier density Δn.

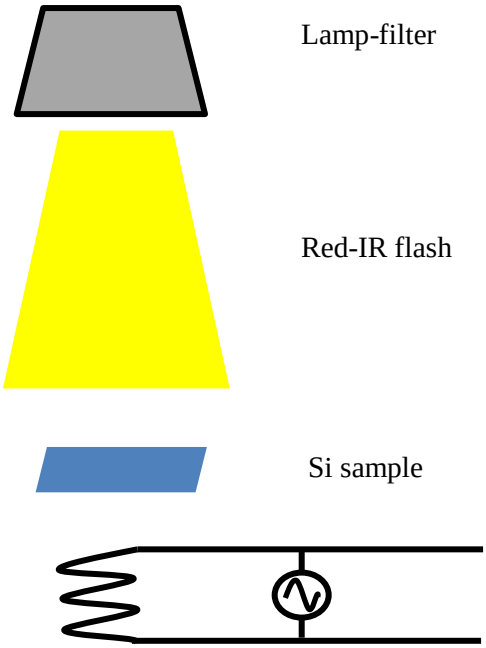


Figure 2.13. Schematic of the Photo-conductance apparatus

2.12 Summary

In this chapter, the sample preparation details and various experimental techniques utilized for sample characterization in this work are presented. The sample surface microstructures were mainly revealed by preferential etching followed by examination in SEM. The bulk defect morphology was configured by TEM diffraction contrast

method and TEM specimens were fabricated by FIB lift-out technique. EBSD was employed to extract relevant crystallographic information, whereas pioneering HR-EBSD cross-correlation analysis was used to calculate the GND density distribution. Gettering and passivation were applied to the deformed and annealed polycrystalline silicon. The change in minority carrier lifetime over individual treatment was measured by a QSS-PC lifetime tester.

The following chapter describes the details of the design and construction of the deformation rig used in the present study.

Chapter 3

Design and construction of the deformation rig

3.1 Introduction

A preliminary step of this project is to design and construct a suitable piece of apparatus for the deformation experiments. Finite resources available meant that constructing an actual piece of hot-rolling equipment was not feasible. However, a compression rig was instead designed and manufactured to mimic the effects of rolling and to produce an appropriate microstructure for further material characterization. One vitally important feature of the compression rig is that it must enable the deformation to take place under clean conditions, which is the primary difference from previous work [50], [51], [55], [57], [59], [61]. Consequentially a special deformation rig was designed and built to satisfy this demand.

A variety of challenges were encountered in practice due to the complexity of the rig construction and a substantial number of modifications were undertaken on the majority of deformation elements before this self-manufactured deformation rig was eventually assembled and tested to function properly. This chapter presents the detailed design of the deformation rig, the various challenges encountered together with practical modifications executed during the construction process.

3.2 Design of deformation rig

The deformation rig was constructed within the frame of an existing Instron 1362 equipped with a 100kN load cell attached to the upper beam. A stainless steel rod is attached to the upper beam, functioning as the primary load transfer mechanism. Crucially, in order to keep the deformation under clean conditions, the rig was specifically designed and is composed of three main elements:

1. A supporting structure which contains a sliding substructure, combined with a water cooling system and an ambient control system.
2. Deformation components, mainly the non-metallic elements in direct contact with the silicon sample.
3. A thermal system, specifically a split furnace providing heat required for the high temperature deformation.

The supporting structure comprises a base plate, a bottom plate and a top plate. Both bottom and top plates are adjoined by four rods and altogether form the substructure. This substructure is capable of sliding upwards and downwards flexibly from the base plate to allow the allocation and alignment of various deformation components. Two water cooling blocks were designed to attach to the top and bottom plates which play the constructive role in the water cooling system. The deformation components are contained in a gas-tight quartz tube and aligned between the base plate and top plate. The thermal source, a split furnace, encloses the entire deformation components alignment and the quartz tube during the compression tests.

In the original design, the position of engraved holes where the deformation alignment sits is in the exact middle of these plates. However, it was then discovered that in

practice the weight of the split furnace made it unrealistic to lift the furnace into the right position in every test. One plausible solution is to fix the furnace at an appropriate supporting structure adjacent to the Instron which enables it to be swung into place. This led to an imperative adjustment of the location of the engraved holes in the original design. Accurate measurements of various dimensions were undertaken and discreet calculation was conducted before the adjustment was permitted. Finally the hole position was modified towards one side of the supporting plates which creates sufficient space on the other side for furnace swinging. The modification was co-designed by Mr. Jim Thompson.

The adjusted design graphs of the supporting plates and a supporting bracket for the furnace containing various detailed dimensions are displayed in the Appendix. The detailed practical establishment of the deformation rig is described in the following section.

3.3 Construction of deformation rig

Following the finalized design of the rig components described in the prior section is the actual rig construction. This section presents the establishment of the three primary rig components and the details of miscellaneous modifications conducted. The construction and modification work was greatly aided by Mr. Laurie Walton and Mr. Ian Lloyd from the Department workshop and furnace room.

3.3.1 Construction of the supporting structure

The base, bottom and top plates together with the four supporting rods were manufactured in the Department workshop using aluminium alloy, whereas the water cooling blocks were made of copper alloy. Dimensions of these components strictly follow the modified design presented in the Appendix. The four aluminium alloy rods connect the top and bottom aluminium plates and together form the sliding substructure. Another two steel poles were adjoined to the base plate, allowing the substructure to move lengthways. Aluminium collets were also fabricated to enhance the sliding movement. These supporting components were altogether assembled into one integrated piece of apparatus as shown in Figure 3.1, with the supporting plates marked by red arrows, and the water cooling system and inert gas circulation system marked by blue arrows. In practice, the diameter of the steel loading rod was found unable to smoothly slide through the top supporting plate, therefore a small fraction of its lower end was machined slightly to facilitate the sliding, as marked by the yellow circle in Figure 3.1. Cooling water flows continuously through the top cooling block and subsequently the bottom cooling block before returning to the original source. This water cooling system was necessitated for effectively reducing the temperature of the supporting structure during hot compression experiments. The cooling blocks and aluminium plates were sealed by rubber O-rings to prevent water leakage. The inert gas circulation system mainly comprises a gas inlet, a quartz tube and a gas outlet. The protective gas originates from an Argon cylinder source and flows through the gas inlet integrated in the base plate into the system. This gas then flows through the deformation components encapsulated inside the quartz tube to protect the silicon sample from oxidation, and flows out through the gas outlet incorporated in the top plate and finally into a bubbler

containing silica oil before entering the atmosphere. The gas flow rate was determined by the bubble rate qualitatively.

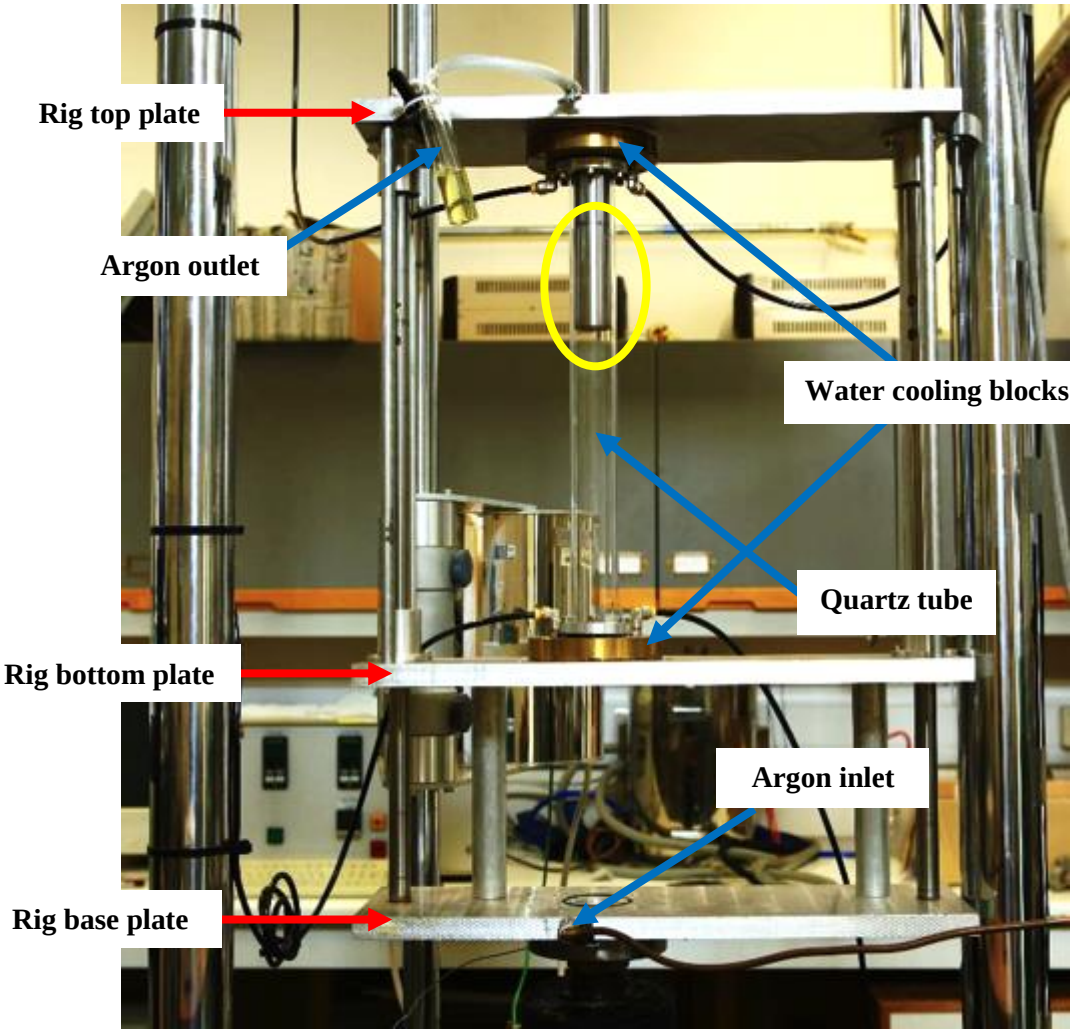


Figure 3.1. Assembled deformation rig supporting structure, with yellow circle highlighting the modified part of the steel loading rod, red arrows marking the major supporting plates, and blue arrows marking the water cooling system and the gas circulation system components.

The supporting steel pole section is presented in Figure 3.2, with holes on the poles highlighted by the yellow circle. These holes were specifically designed for allowing the substructure to stay in place after sliding upwards.

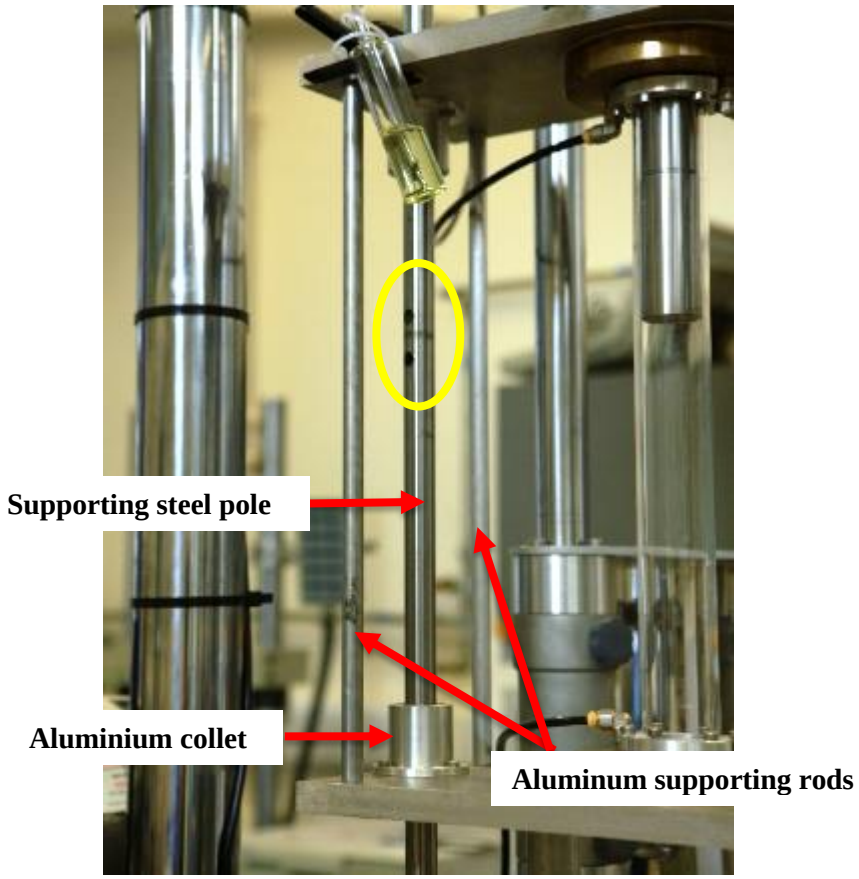


Figure 3.2. Supporting pole section, with the supporting elements marked by red arrows and the holes drilled in the steel pole marked by yellow arrow.

The quartz tube and water cooling blocks were originally sealed by rubber O-rings integrated in the cooling block. However, during the tests it was discovered that a gap always existed between the O-rings and the quartz tube resulting in a sealing issue. In addition, it was very difficult to obtain suitable sized O-rings which would fit both with the grave in the cooling blocks and the outer diameter of the quartz tube. An alternative

design was made: first surrounding the quartz tube with O-rings then sealing the O-rings to cooling blocks by specially manufactured aluminium collets, as illustrated in Figure 3.3(a). The aluminium collets were screwed into the cooling blocks, providing sufficient pressure to serve the gas-tight contact.

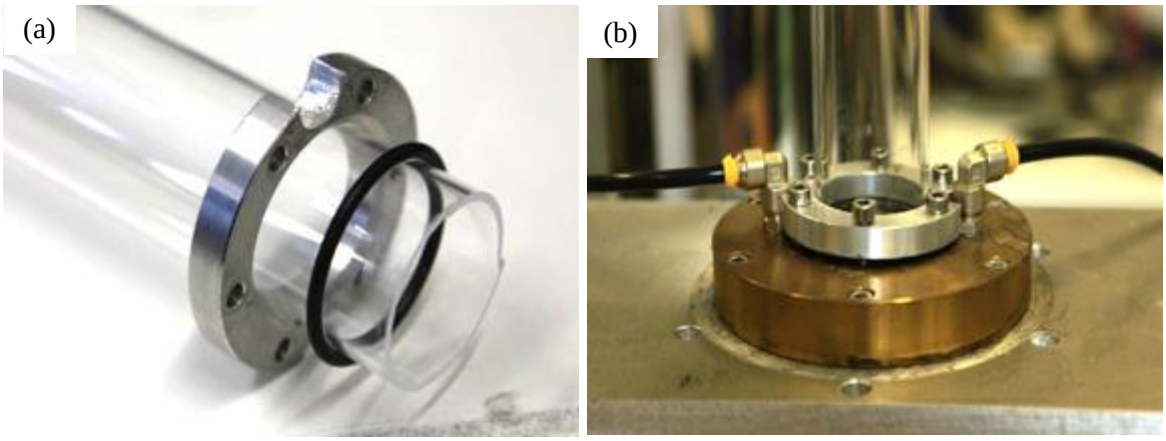


Figure 3.3. (a) Illustration of O-ring and aluminium collet on one end of quartz tube; (b) Quartz tube sealed with cooling block by O-ring in between which is fixed by aluminium collet.

3.3.2 Design and alignment of the deformation components

The crucial parts of the deformation construction are the components in direct contact with the silicon sample. It is therefore of vital importance that these components are not only obtain intrinsic high purity characteristics but also do not introduce extra metallic contamination during the hot deformation. In addition, these components need to possess extraordinary mechanical properties to sustain potentially high stress generated by compression at elevated temperatures. These components include high purity crystalline silicon samples, extra-high purity quartz discs (supplied by Edmund Optics

®), high purity alumina pushing rods (supplied by Multilab ®) and machinable ceramic (Macor ®) discs.

The complete alignment can be described as follows: The crystalline silicon sample sit in the middle of the entire alignment and is in direct contact with the extra-high purity quartz discs, whose major function is to maintain a high purity environment around the silicon sample. These quartz discs neighbour high purity alumina pushing rods. Macor ® discs are inserted between the alumina pushing rods and the steel loading rod from top, and the aluminium base plate from bottom. The detailed illustration is presented in Figure 3.4. Macor ® was specifically selected as a thermal insulator intervening between the alumina rods and their adjacent metallic elements due to its excellent thermal conductivity, 1.46 $W \cdot m^{-1} \cdot {}^{\circ}C^{-1}$, which is 3 times better than alumina.

Prior to the deformation, these components together with the quartz tube were firstly cleaned using standard RCA procedure (see Section 2.3) in the clean room in Begbroke, then assembled and enclosed in polytetrafluoroethylene (PTFE) jackets which also went through the RCA cleaning steps to maintain the alignment, as illustrated in Figure 3.4 (a). This assembled PTFE jig and the cleaned quartz tube were wrapped by clean tissues then encapsulated by aluminium foil before being transferred to the main mechanical testing laboratory in the Department. After allocating the quartz tube, the deformation elements were altogether aligned inside the deformation rig and the split furnace swung in place to enclose the entire alignment, as shown Figure 3.5 (b).

The dimensions of various deformation components were modified for several times and the final value was measured and shown in Table 3.1.

Table 3.1. Dimensions of deformation components.

	Diameter ∅ (mm)	***Length (mm)***
Alumina rods (Multilab ®)	35.5	215
Extra-high purity quartz discs (Edmund Optics ®)	25.4	20
Macor discs (Macor ®)	35.5	15
Quartz tube	Outer 47.8, Inner 43.8	475

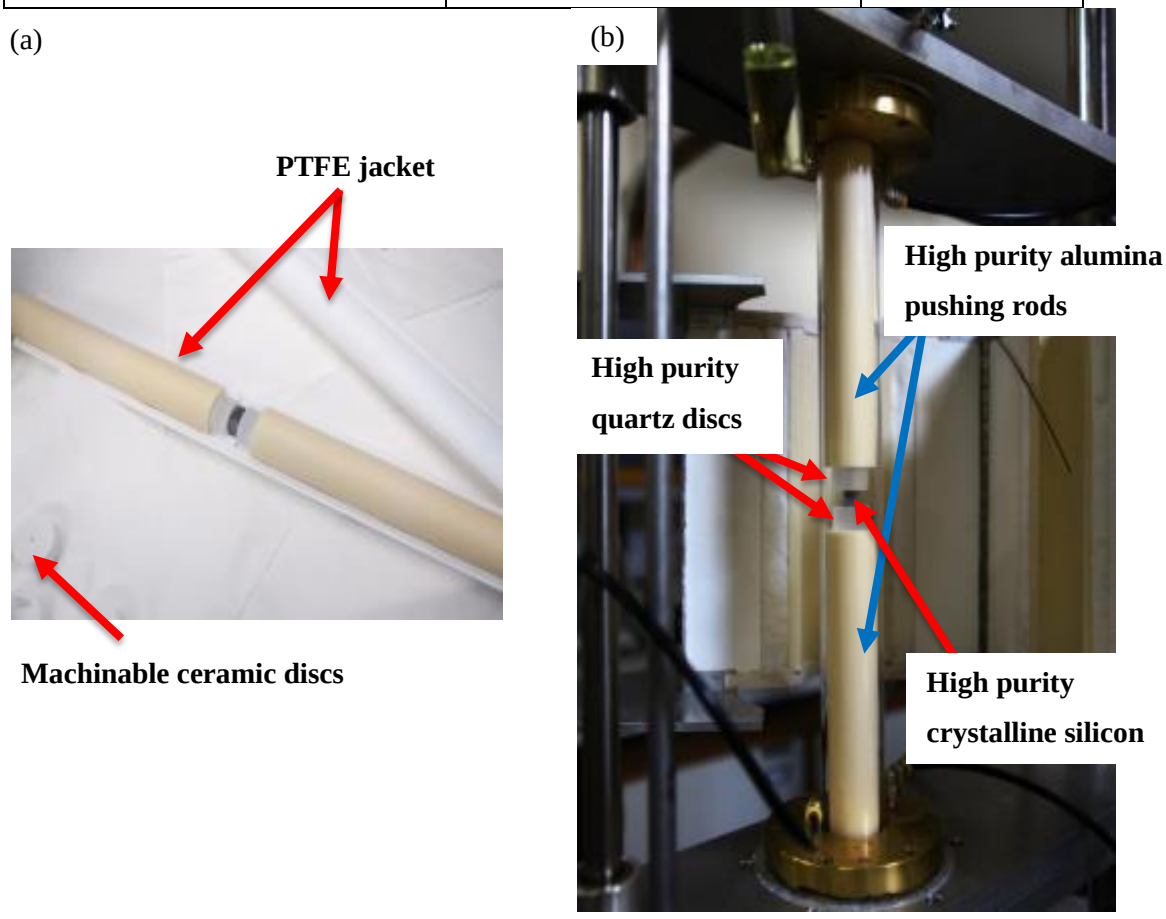


Figure 3.4. (a) Deformation components cleaned and assembled by PTFE jacket in the clean room; (b) Deformation components aligned and enclosed by clean quartz tube in the rig.

However, the alignment was found extremely challenging in practice. First of all, the fundamental issue was the fact that the steel ram on which the entire rig stands was not perfectly horizontal. Adjustment was carried out by placing small pieces of folded aluminium foil in between the steel ram and the base plate, see Figure 3.5 (a). Besides, it was found that using real deformation components to practise various rig alignment adjustments might cause serious damage to the components. Therefore aluminium counterparts were fabricated, in the dimensions of the real components, as substitutes, see Figure 3.5 (b).

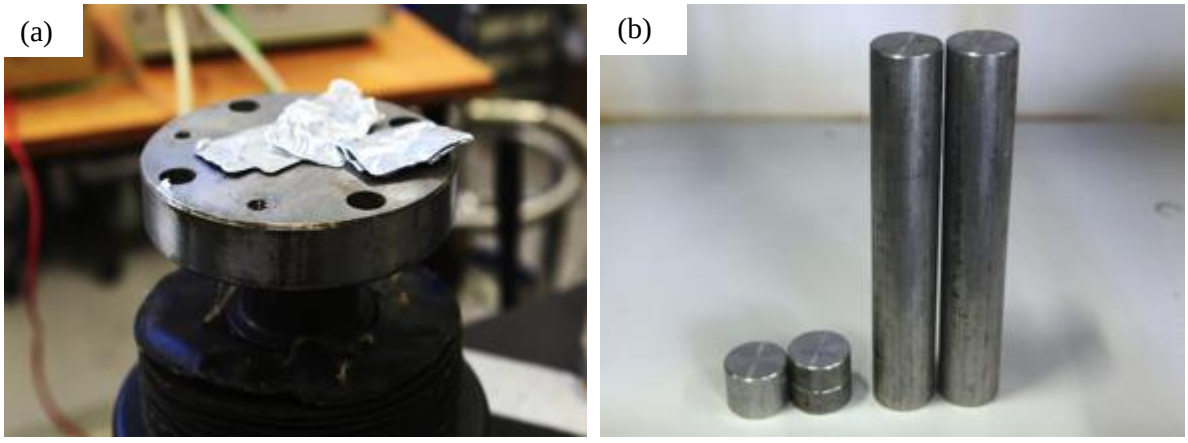


Figure 3.5. (a) Instron bottom ram and folded aluminium foils to adjust alignment; (b) Aluminium rods manufactured in the same size as real deformation components for alignment.

3.3.3 The supporting structure for split furnace

The thermal system consists of a split furnace as the heat source, a box furnace temperature controller and three K-type thermocouples measuring temperatures of different elements during the deformation.

The split furnace was manufactured specifically by Severn Furnace Limited (SFL ®) and is composed of embedded wire heating elements and high grade ceramic fibre insulation enclosed in a polished stainless steel case. Aluminium hardened insulation end plates are attached to both the top and bottom sides of the furnace case. The cross section of split furnace is shown in Figure 3.6 (a). Two aluminium brackets were utilized to stabilize the furnace with respect to the supporting frame which was clamped onto the Instron bottom table, see Figure 3.6 (b) and (c). Two additional ceramic insulation plates were machined and rested on top of the furnace to enhance thermal insulation.

The furnace controller features a feedback loop with a type K thermocouple inserted into the furnace body. The heating profile was maintained as ramping by 1 $^{\circ}C \cdot min^{-1}$. Another thermal couple was inserted inside the small gap between the furnace and quartz tube, approximately at the position of silicon sample. This measures the true temperature of the silicon sample and the top end of the lower alumina rod during the heating cycle. It was noticed that the true sample temperature was generally 30 $^{\circ}C$ lower than the furnace temperature. A third thermal couple was placed at the bottom end of the lower alumina rod, from which the thermal gradient across the alumina rod can be extracted.

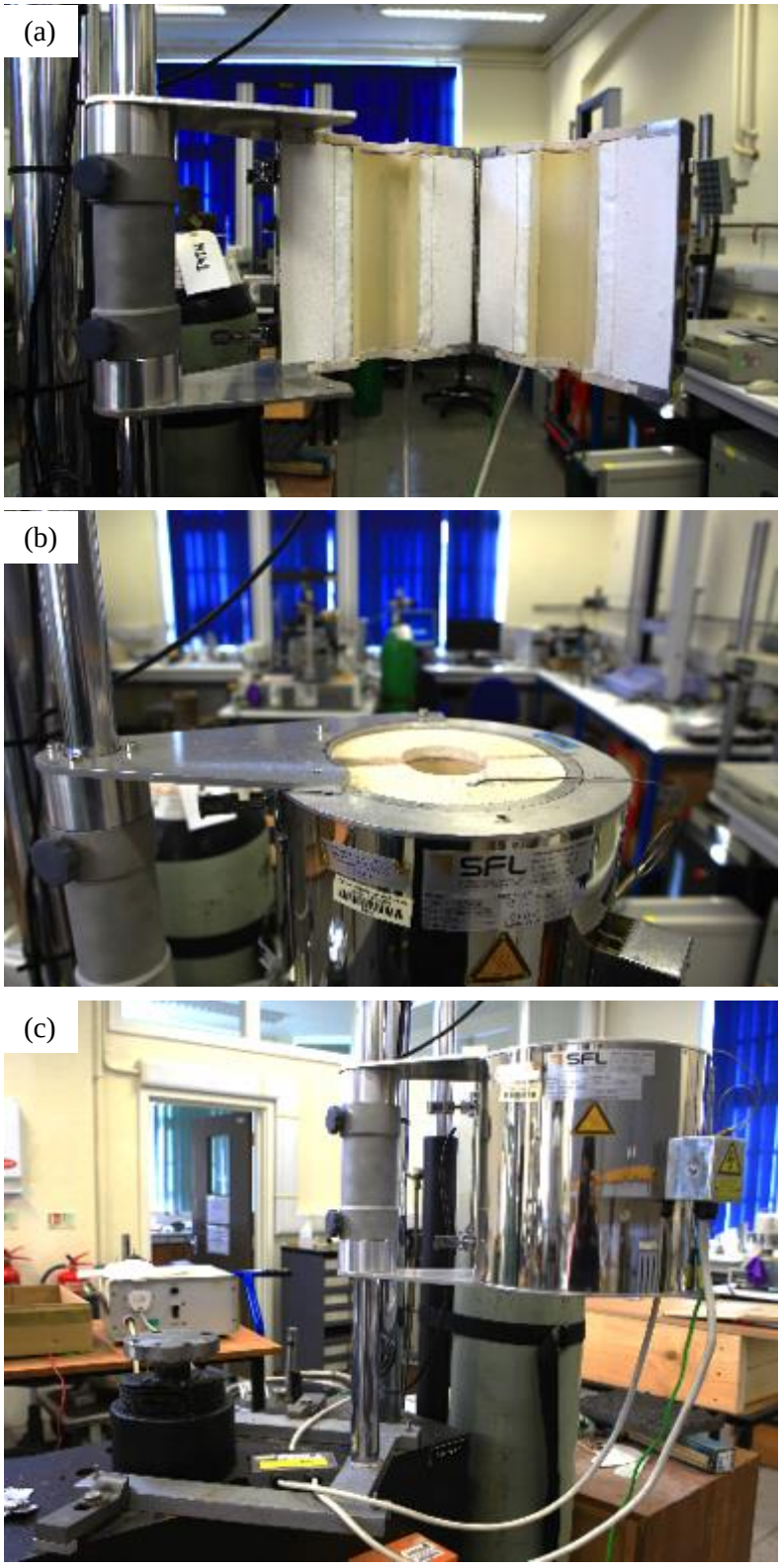


Figure 3.6. (a) Cross section of the split furnace; (b) Top view of enclosed furnace and the supporting bracket; (c) Furnace supporting structure clamped on the Instron bottom table.

After the completion of rig construction, the system was tested and verified to be adequate for hot deformation experiments. A photograph of the completed deformation rig in working state is shown in Figure 3.7.

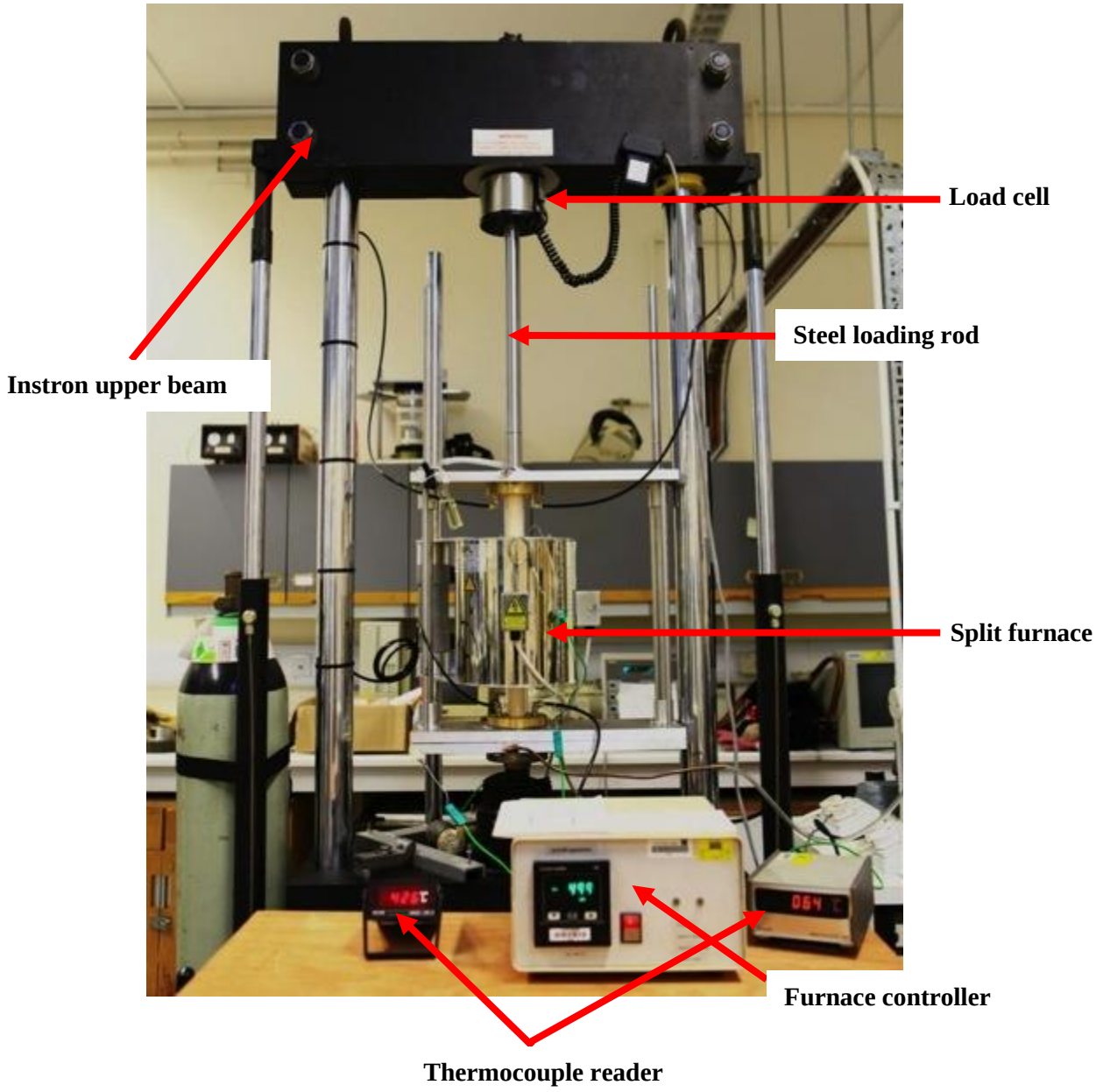


Figure 3.7. Photograph of the completed deformation rig in working state.

3.4 Deformation and silicon sample shape modification

3.4.1 Modification of deformation components

The quartz discs were found to be extremely fragile under high stress compression at temperatures beyond 1150 ˚C, according to experiments from the first four deformation tests. High purity alumina discs (Supplied by Multilab ®) were then substituted for the quartz discs, as alumina maintains significantly better mechanical properties at these temperatures. Their dimensions and thermal properties are shown in Table 3.2.

Table 3.2 Properties of high purity quartz discs an alumina discs

	Diameter ∅ (mm)	***Length (mm)***	***Chemical composition***	***Thermal expansion $10^{-6}\cdot K^{-1}$***
Extra-high purity quartz discs (Edmund Optics ®)	25	20	SiO_2	0.55
High purity alumina discs (Multilab ®)	33.5	20	Al_2O_3 99.7%, balance MgO,Na_2O,SiO_2	8.6 (20 ~ 1000 ˚C)

3.4.2 Silicon sample shape modification

Czchralski single crystalline silicon samples were originally manufactured in size 10 mm x 10 mm x 10 mm. However, during the series of compression tests it was found samples of this original size failed to produce deformed samples with sufficient size for

subsequent lifetime tests by the Sinton WCT-120 Quasi-Steady-State Photo-Conductance (QSS-PC) lifetime tester whose coil diameter is 15 mm.

Henceforth the sample size was modified as 15 mm x 15 mm x 10 mm, with the 10 mm side along the compression axis. Due to the marked friction observed between the silicon sample and adjacent quartz discs, the sample edges were further trimmed to eliminate sharp edges. The sample shape evolution during the compression experiments is illustrated below, in Figure 3.8.

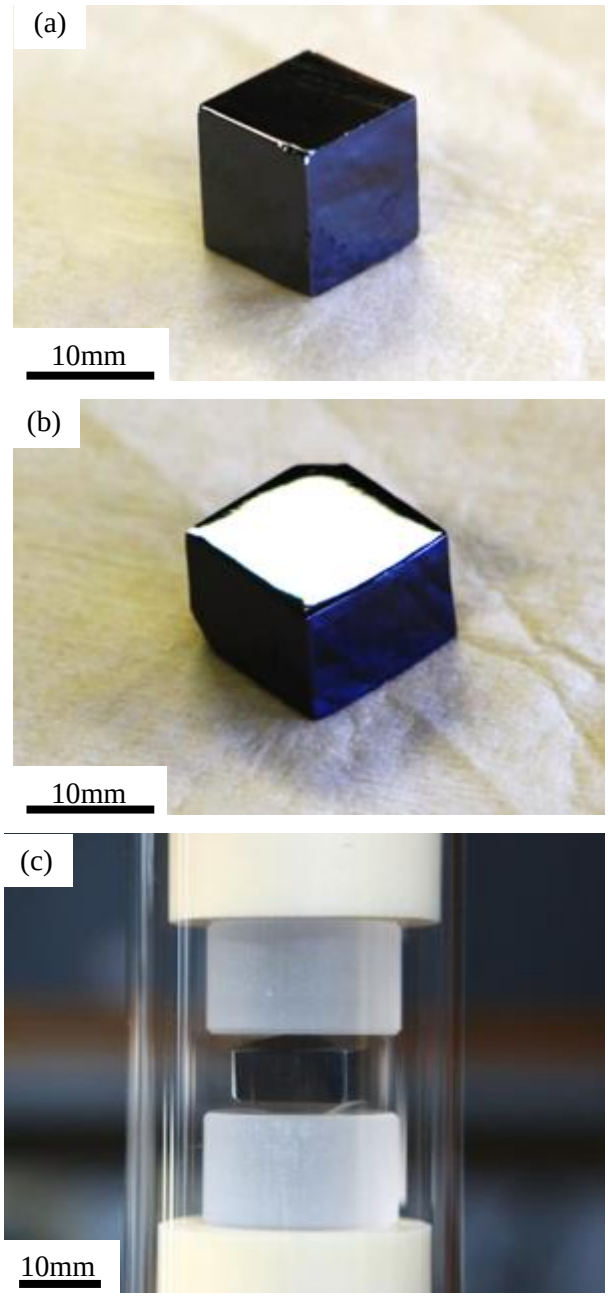


Figure 3.8. Silicon sample shape modification over compression tests: (a) Original cube shape sample in size of 10 mm x 10 mm x 10 mm; (b) Modified sample in size of 15 mm x 15 mm x 10 mm; (c) Trimmed sample with no sharp edges in the deformation alignment.

3.5 Characterization of the deformation cleanliness

One critical step before the occurrence of the actual crystalline silicon deformation was to evaluate the attainable cleanliness of the deformation rig. A control experiment was therefore designed to assess the deformation conditions by estimating the amount of metallic impurities introduced by high temperature processing in the rig. This was achieved by monitoring the change in electrical properties, specifically minority carrier lifetime, of silicon before and after the complete thermal cycle, apart from that no extra load was introduced.

Two adjacent pieces of silicon wafer samples sized 15 mm x 15 mm were cleaved from a piece of standard boron doped p-type Czochralski single crystalline silicon wafer, for the purpose of optimizing the identification of these control samples.

One piece of silicon wafer sample was then subjected to the actual deformation process with no load applied. The sample was prepared by a standard RCA clean and HF dip in the clean room along with other deformation components before being assembled in the deformation rig and went through the entire thermal cycle during which it was thermally kept at 1150 ˚C for 4 hours. The annealed sample together with the sample without high temperature processing were subsequently passivated with silicon nitride grown by plasma enhanced chemical vapour deposition (PECVD) on both surfaces.

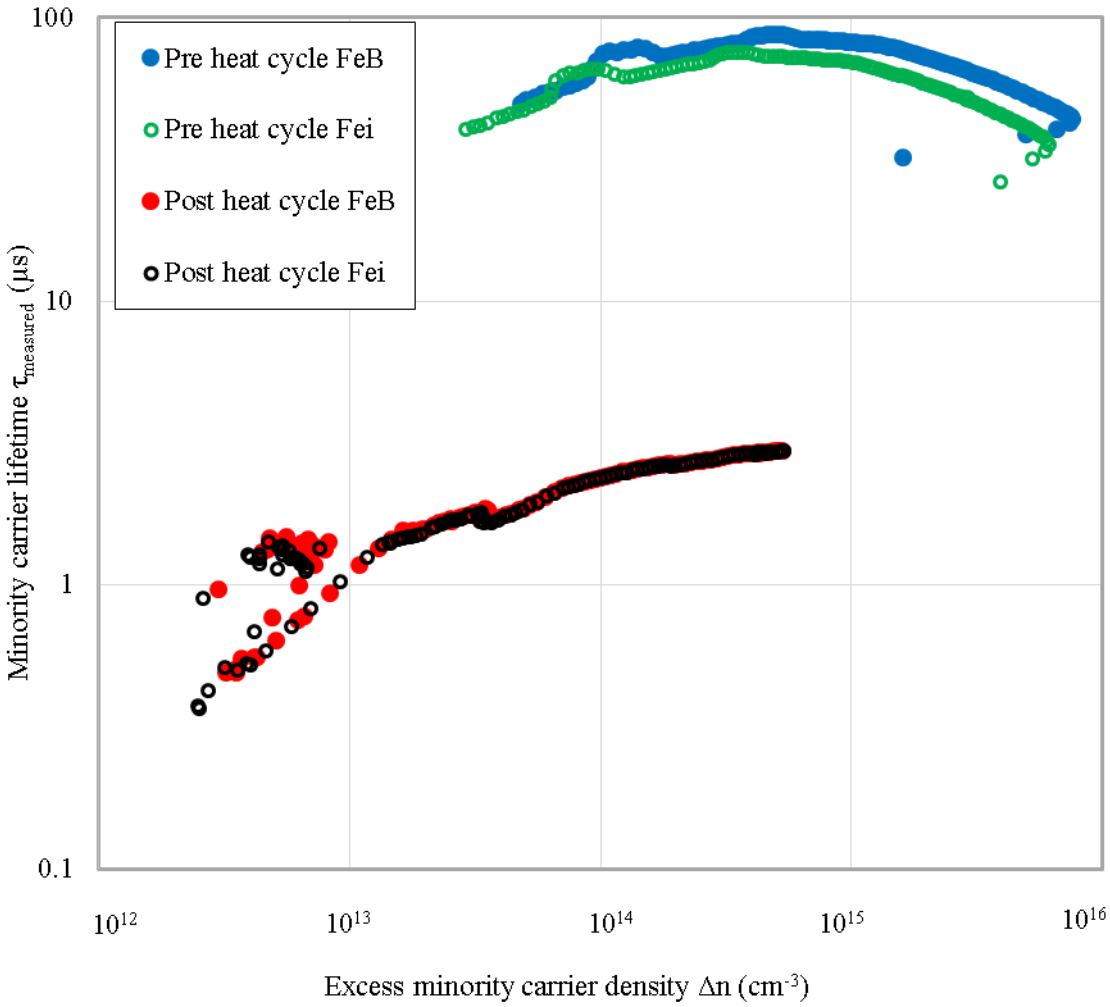


Figure 3.9. Measured minority carrier lifetime $\tau_{measured}$ versus excess minority carrier concentration Δn of p-type Czochralski sc-Si samples pre thermal cycle without flash (solid blue circle), pre thermal cycle with flash (hollow green circle), post thermal cycle without flash (solid red circle), and post thermal cycle with flash (hollow black circle), respectively.

The minority carrier lifetime of these two samples was then measured at room temperature by the QSS-PC technique and the corresponding minority carrier lifetime curves as the function of minority carrier concentration are shown in Figure 3.9. It is evident that the minority carrier lifetime deteriorated drastically after the heating cycle

in the deformation rig. The good minority carrier lifetime measured from the sample prior to the thermal processing shows that the starting material had excellent electrical properties. However, the lifetime was reduced by approximately an order of magnitude after heat treatment in the deformation rig. Since the starting material is pure dislocation-free single crystalline silicon, no pre-existing grain boundaries or dislocations should possibly propagate during the processing and grain boundaries are unlikely to account for the lifetime reduction. In addition, no extra load was exerted on the sample therefore no excessive dislocations should be induced by potential plastic deformation. The above assumptions led to the deduction that the lifetime degradation was most likely attributed to the introduction of metallic contaminants from the high temperature processing.

Should the contaminant be iron, the most common existent and deleterious metallic impurity in silicon [209], (presumably in the form of iron-boron (FeB) pairs since the material was boron-doped), the concentration of bulk iron after the thermal cycle was estimated to be approximately 1.0×10^{13} cm^{-3}. This is significantly lower than the solubility of iron in silicon at this temperature, which is up to 10^{16} cm^{-3} [209]. It is well recognised that iron is usually present in silicon in interstitial form (Fe_i), however at room temperature it tends to interact with substitutional boron to form FeB pairs [68]. These FeB pairs can be easily dissociated either by thermal annealing or optical activation [210]. In the present work, 50 flashes with a ~10 μs decay constant from a flash lamp located very close to the sample were used to dissociate FeB pairs [211]. The minority carrier lifetime curves appear nearly unchanged after the photo-dissociation of the FeB pairs, both before and after the thermal cycle, which suggests that the contamination source is unlikely to be interstitial Fe. In addition, due to the slow

cooling profile, should iron exist, the Fe atoms may have formed precipitates during this process. In comparison, the Fe concentration in current solar grade multicrystalline silicon (1Ωcm) is estimated to lie in the range from 10^{14} cm^{-3} to 10^{16} cm^{-3} (both in bulk and as precipitates) before and after the gettering process [210]. Consequently, despite the substantial reduction of minority carrier lifetime obtained after the thermal cycle, given the true deformation temperature is approximately 1150 ˚C, the results are not completely destructive. It can then be concluded that the cleanliness of the deformation conditions is at an acceptable level.

3.6 Summary

A special piece of deformation apparatus was designed and constructed for subsequent compression experiments. The deformation rig comprises a supportive structure, a cooling water system, a protective gas circulation system and a thermal system. The critical cleanliness of the deformation condition was also assessed and verified satisfactory by a control experiment.

In the next chapter, experiments conducted to determine suitable deformation and annealing conditions using single crystalline silicon and the microstructural examination during the process are presented.

Chapter 4

Investigation of the optimal deformation and annealing condition

4.1 Introduction

The first step of this project is to manufacture and construct a piece of suitable apparatus for hot compression experiments, which has already been described in details in Chapter 3. The following step is to determine the optimum realizable deformation conditions of this self-assembled deformation rig and establish suitable subsequent annealing conditions.

Due to the lack of precious polycrystalline silicon material, also because it is well known that the stress-strain curve of a single crystal loaded along a low index direction is commonly very similar to that of a polycrystal [50], dislocation-free intrinsic single crystalline silicon produced by Czochralski method was selected for the deformation and annealing condition investigation. As stated in Section 1.2.3, it was confirmed by tensile tests that silicon crystals can be plastically deformed above 900 ˚C [23], [27]. Plastic deformation of dislocation free single crystalline silicon has been of great interests since 1950's [23], [27], [28], [36], [37], [41], primarily on the mechanical behaviour especially the stress-strain behaviour and its correlation to dislocation dynamics. The research interests were generally promoted by the development of semiconductor industry. This topic has been extensively studied and comprehensively review in the past [23], [27], [31], [32], [36], [37], [40]–[43], [46]–[48], [212]–[217],

but mainly in the temperature range from 350 ˚C to 950 ˚C. Few studies related to plastic deformation of silicon crystals were carried out at temperatures above 1100 ˚C [27], [42], [43], [47]–[51].

Nevertheless, there is no systematic and precise data, particularly from compressive tests, to elucidate the relations among the parameters of temperature, stress load and area of the cross section of silicon samples. Besides, the attainable stress-strain parameters determined by the specific Instron machine and achievable thermal conditions determined by the furnace employed in the current project could possibly differ pronouncedly from literatures. Therefore, it is of great importance and also one of the primary goals of this work to establish the most favourable deformation condition for silicon crystal compressions in the specific deformation rig. The conditions determined by single crystalline silicon deformation could be practically applied to subsequent deformation tests on polycrystalline silicon. However, a systematic investigation of the dynamic mechanical behaviour of single crystalline silicon compression with respect to various temperatures and strain rates is beyond the research interests scope and time scale of this project, henceforth the current chapter will only present relevant results (predominantly by means of microstructural investigation) obtained in the seeking of suitable deformation and annealing conditions. The general microstructure and dislocation morphology, especially the observed dislocation density, of single crystalline silicon during the deformation and annealing process are selected to be the principal evaluation criteria.

4.2 Deformation and annealing parameters overview

Eight tests of compressing single crystalline silicon along < 001 > axis were performed over a range of elevated temperatures (1020 ˚C~1150 ˚C) and strain rates (1.67 x 10^{-5} s^{-1} ~ 1.00 x 10^{-4} s^{-1}) under clean conditions. The deformed material was subsequently subjected to various high temperature annealing conditions to select the optimal annealing parameters such as temperature and duration.

Initial silicon sample for the compression test had dimensions of 10 mm x 10 mm x 10 mm sawn from Czochralski grown silicon ingot with one axis along with the < 001 > crystal orientation. Four high temperature compression tests were performed on these silicon cubes along the <001> orientation. However, during the process it was found that the size of deformed sample was not sufficient for the QSS-PC lifetime tester. Therefore an adjustment of the initial sample dimensions was made. Due to the fixed dimension of the deformation rig the sample height was limited to 10mm, the dimensions of the other two sides were increased to 15mm. The modified sample size was 15 mm x 15 mm x 10mm.

The first four compression tests were conducted using cube-shaped samples and the rest using flat shape samples. In each case a uniaxial load was applied and was progressively increased to an appropriate amount. This maximum load was then maintained throughout the run. The average strain rate was estimated by simply dividing the total strain by time. Among all the deformations, the silicon samples produced by the 1^{st}, 2^{nd} and 6^{th} deformations were severely cracked either due to the high strain accommodated or high strain rates employed, resulting in unsuitable samples for further microstructural examination or subsequent annealing. The remaining deformed samples were subjected

to various annealing conditions to evaluate the effect of annealing temperature and time on the microstructure and defect morphology evolution.

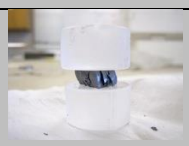
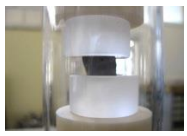
Table 4.1 illustrates the overview of deformation and subsequent annealing conditions applied to individual silicon samples. The samples severely cracked were shown in grey shade. The microstructural investigations of each deformation will be presented in the following sections of this chapter, respectively. Pictures of each deformation and the conditions employed during subsequent annealing are shown in Table 4.2. The overall microstructure and dislocation density measured by etch pit counting of single crystalline silicon after each deformation and subsequent annealing are shown in Table 4.3.

Table 4.1. Overview of deformation and annealing conditions conducted on single crystalline silicon with sampled severely cracked shown in grey shade.

Deformation	Sample size and shape	Deformation temperature/˚C	Strain/%	Stress/ MPa	Strain rate/s^{-1}
1st	Cube, 10mm x 10mm x 10mm	1020	Nil	180.0	Nil
2nd		1020	30	160.0	6.41×10^{-5}
3rd		1057	38	120.0	2.35×10^{-5}
4th		1068	36	100.0	1.25×10^{-5}
5th	Flat , 15mm x	1077	38	62.2	1.41×10^{-5}
6th		1140	47	66.7	1.00×10^{-4}
7th		1130	38	45.9	2.64×10^{-5}

8th	15mm x 10mm	1150	30	40.0	1.67×10^{-5}

Table 4.2. Pictures of deformed single crystalline silicon and the conditions employed during subsequent annealing, with sample number labelled. Sampled severely cracked are shown in grey shade.

Deformation	Deformed sample	Subsequent annealing
1st		Nil
2nd		Nil
3rd	 As-deformed (sample 3a)	1250 ˚C x 30 min (sample 3b) 1250 ˚C x 60 min (sample 3c) 1250 ˚C x 90 min (sample 3d) 1250 ˚C x 120 min (sample 3e)
5th	As-deformed (sample 5a)	1375 ˚C x 30 min (sample 5b) 1375 ˚C x 60 min (sample 5c)

		1375 ˚C x 90 min (sample 5d) 1375 ˚C x 120 min (sample 5e) 1400 ˚C x 120 min (sample 5f)
6th		Nil
7th	 As-deformed (sample 7a)	1375 ˚C x 120 min (sample 7b) 1400 ˚C x 120 min (sample 7c)
8th	 As-deformed (sample 8a)	1400 ˚C x 120 min (sample 8b)

Table 4.3. Overview of microstructures and measured dislocation densities by etch pit counting of each deformation and post-deformation annealing conducted on single crystalline silicon

		Overall microstructure	Cell interior average dislocation density measured by etch pit counting
3rd deformation	As-deformed (1057˚C by 38 %)	5 μm square cells	1.2 X 10^{12} ~ 1.0 X 10^{13} m^{-2}
	Post-deformation annealing 1250˚C x 120 min		1.1 X 10^{12} m^{-2}
4th deformation	As-deformed (1068˚C by 36 %)	5 μm square cells	1.0 X 10^{12} ~ 1.0 X 10^{13} m^{-2}
	Post-deformation annealing 1250˚C x 120 min	10 μm square cells	5.0 X 10^{11} m^{-2}
5th deformation	As-deformed (1077˚C by 38 %)	5~20 μm square cells	1.0 X 10^{11} ~ 1.0 X 10^{13} m^{-2}
	Post-deformation annealing 1375˚C x 120 min	10 μm square cells	

	Post-deformation annealing 1400˚C x 120 min	50 μm square cells	5.0 X 10^{10} m^{-2}
7th deformation	As-deformed (1130˚C by 38 %)	5~20 μm square cells	1.0 X 10^{13} m^{-2}
	Post-deformation annealing 1375˚C x 120 min	20 μm square cells	
	Post-deformation annealing 1400˚C x 120 min	50 μm square cells	1.0 X 10^{11} m^{-2}
8th deformation	As-deformed (1150˚C by 30 %)	3~20 μm square cells	1.0 X 10^{11}~ 1.0 X 10^{13} m^{-2}
	Post-deformation annealing 1400˚C x 120 min	70 μm square cells	1.5 X 10^{11} m^{-2}

4.3 Experimental methodology

The deformed samples were sawn into small slices by standard mechanic sawing, the surfaces of which are parallel to the compression axis. The sample thickness was approximately 1.5mm. Planar etching was applied to remove residual saw damage before subsequent high temperature annealing. For surface microstructure investigation, all specimens were first polished using 6μm and 1μm diamond paste to remove coarse scratches and produce flat surfaces. They were then subjected to colloidal silica (‘Syton’)

polishing to produce a damage free 'mirror' surface. These polished specimens were then submerged in Sirtl etchant for 30s (see Section 2.5.2 for details) to reveal dislocation pits and grain boundaries. The preferentially-etched surface microstructures were investigated by SEM. In order to gain insights into the bulk defects morphology, thin TEM foils were produced by FIB lift-out technique. In most cases the foil surface was perpendicular to the compression axis. The resultant foil then contains defects in the compression plane. TEM diffraction contrast technique was employed for detailed defect configuration. In order to reveal all defects, the TEM specimen was initially tilted to a low index pole, for instance close to the [001] zone axis. Bright field images were obtained using the centre spot (000). Images in different two-beam conditions were then used to inspect specific defects in greater contrast. The Burgers vector of the dislocations was determined by **g.b** = 0 criterion. Perfect dislocations in silicon lie in the (111) slip planes and are of the type ½ [110]. The values of **g.b** for these dislocations are shown in details in Table 4.4.

Table 4.4. Values of **g.b** for Burgers vector determination in silicon.

b	**g.b**								
Zone axis	001			111			011		101
g	400	040	220	$2\bar{2}0$	$20\bar{2}$	$02\bar{2}$	$1\bar{1}1$	$11\bar{1}$	$\bar{1}11$
½ [110]	2	2	2	**0**	1	1	**0**	1	**0**
½[101]	2	**0**	1	1	**0**	-1	1	**0**	**0**

½[011]	**0**	2	1	-1	-1	**0**	**0**	**0**	1
½[$1\bar{1}0$]	2	-2	**0**	2	1	-1	1	**0**	-1
½[$10\bar{1}$]	2	**0**	1	1	2	1	**0**	1	-1
½[$0\bar{1}1$]	**0**	-2	-1	1	-1	-2	1	-1	**0**

Measurements of dislocation density in thin foils mainly comprise two methods, according to P. B. Hirsch *et al*. [191]. The first one is to count the number of dislocation line intersections with the foil surface, which is an extension of the etch pit counting technique. It has the advantage that it is not necessary to know the foil thickness. Also the local rotations of the dislocations that occur during thinning do not affect the result. On the other hand, it is difficult to measure densities higher than 3.0 x 10^{13} m^{-2} [191]. The second method is to measure the total dislocation line length in a unit volume, which results in a parameter length·m^{-3}. In the present chapter, dislocation density measurement of TEM foil was performed by counting the dislocation line intersection per unit area.

It should be further noted that in any TEM micrographs some dislocations may be invisible, unless several strong reflections are operated at the same time. This calculation for the ½[110] Burgers vector in silicon is shown in Table 4.5.

Table 4.5. Proportion of Burgers Vectors of ½[110] invisible in various reflections in silicon lattice.

hkl	Proportion of invisible Burgers vectors
111	1/2
220	1/6
400	1/3
311	1/6
331	1/6
420	All visible

4.4 Deformation of cube-shape single crystalline silicon

Since the first two deformations produced 'cracked' silicon sample at 1020 ˚C, it was suspected that the deformation temperature was not sufficient for high strain (~ 30 %) compression of single crystalline silicon. Hence the 3rd and 4th deformations were conducted at approximately 1060 ˚C. The subsequent annealing temperature for samples deformed in these two runs was determined to be 1250 ˚C. The deformed silicon material was sliced along the compression axis, henceforth the surface microstructures observed in SEM were essentially those of the compression plane. This section presents detailed microscopic examination of silicon samples processed in these two deformations using preferential etching/ SEM and TEM.

4.4.1 Deformation at 1057 ˚C by 38 % along the [001] direction (3rd deformation)

The first attainable deformed sample was achieved by uniaxial compression at 1057 ˚C along the [001] crystallographic direction and the total strain introduced was 38 %. The strain rate is relatively low, approximately 2.35 x 10^{-5} s^{-1}.The deformed silicon sample was sliced to several small pieces and individually subjected to annealing at 1250 ˚C for 30 min (sample 3a), 60 min (sample 3b), 90 min (sample 3c) and 120min (sample 3d), respectively. The defects revealed surface microstructures of the as-deformed and subsequently annealed samples and selective TEM configuration of bulk defects are presented in this section.

4.4.1.1 Microstructures of the as-deformed and annealed samples by SEM

Etch pits examination showed a characteristic dislocation cell structure in the as-deformed initially undoped dislocation free Czochralski single crystalline silicon, as illustrated in Figure 4.1 (a). It is evident that the silicon sample was highly deformed after 30 % strain and the deformation involved a multi-slip mechanism deducing from the pronounced intersecting slip lines. These relatively straight intersecting slip lines primarily lie in two different directions approximately perpendicular to each other (as indicated by white lines) and both 45˚ with respect to the vertical compression direction and constitute a network structure consisting of 5 μm square cells.

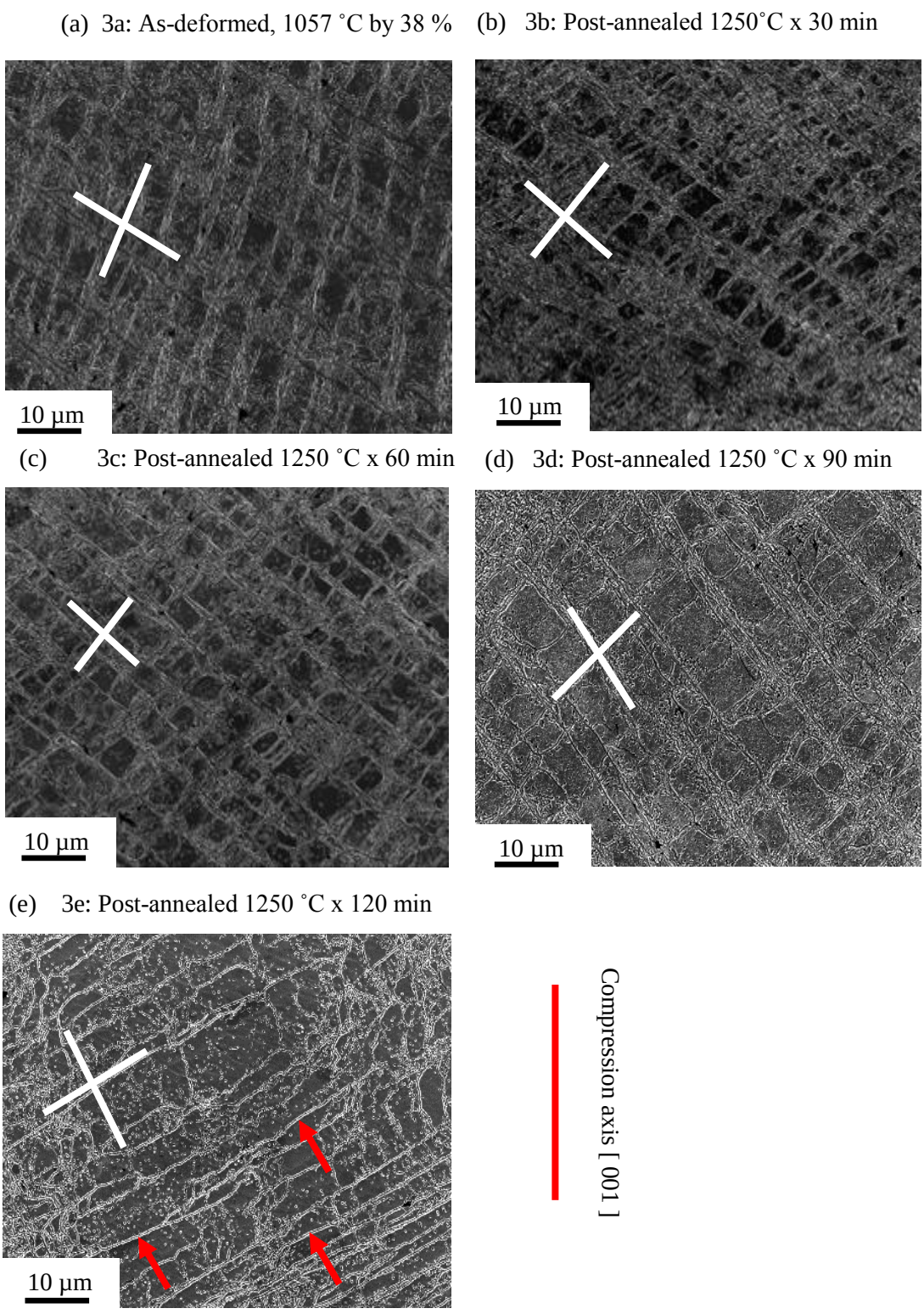


Figure 4.1. SEM micrographs reveal the dislocation etch pits and characteristic slip band structures of (a) sample 3a (deformed at 1057˚C by 38%), (b) sample 3b (deformed at 1057˚C by 38% and annealed at 1250˚C for 30min), (c) sample 3c (deformed at 1057˚C by 38% and annealed at 1250˚C for 60min), (d) sample 3d (deformed at 1057˚C by 38% and annealed at 1250˚C for 90min), (e) sample 3e (deformed at 1057˚C by 38% and annealed at 1250˚C for 120min), red arrows mark polygon boundaries. The compression axis is vertical in these micrographs. White lines point the intersecting slip line directions.

Annealing at 1250 ˚C for up to 90 min seemed insufficient to induce appreciable alteration in the cellular microstructure of the as-deformed silicon sample, as shown in Figure 4.1 (a)-(d). The slip line network possessed almost the identical character (*e.g*. pattern shape and cell size) throughout the annealing process from qualitative examination, although the microstructure appeared vaguely recovering from the as-deformed state. An appreciable polygonized structure was observed from the specimen thermally annealed at 1250 ˚C for 120 min, indicating an evident recovery process, as seen in Figure 4.1(e). Long straight polygon boundaries parallel with each other were displayed in this microstructure, as marked by red arrows in Figure 4.1 (e). The cellular structure of the as-deformed structure completely disappeared and the dislocation density is also considerably reduced after this treatment. It should be noted that this type of recovered structure only takes up a small amount of the whole annealed sample, which indicates the recovery process was initiated however obviously incomplete. Henceforth this annealing condition was decided to be not optimal.

A closer look at the etched surface of the as-deformed sample reveals an extremely high density of dislocation etch pits, as shown in Figure 4.2 (a). Etch pits appear heterogeneously distributed across the surface and the density varied from cell to cell. In general, dense overlapping etch pits were often found close to the cell walls and more scattered towards the cell interiors. Curved sub-grain boundaries formed by aligned intensive etch pit arrays were also observed in some cell interiors. However, the nature of these characteristic cell walls could not be determined only by surface microstructure examination, so these regions were then investigated by TEM, as described in detail in the following subsection. In contrast, the recovered region in the sample annealed at 1250 ˚C for 120 min displayed a relatively irregular defect structure in the form of

densely aligned dislocation etch pits arrays, as marked by red arrows in Figure 4.2 (b). These features may be recognized as polygon walls as an indication of an effective recovery process, which was reported in earlier studies [37]. The overall etch pits distribution was also found considerably diffuse comparing to the as-deformed microstructure. Dislocation density of the cell interior in the as-deformed sample revealed by etch pits counting is inhomogeneous, approximately ranging from 1.2 x 10^{12} m^{-2} to exceeding 10^{13} m^{-2}. In contrast, dislocation density in the sample annealed at 1250 ˚C for 120 min is more evenly distributed, approximately 1.1x10^{12} m^{-2} between the polygon walls.

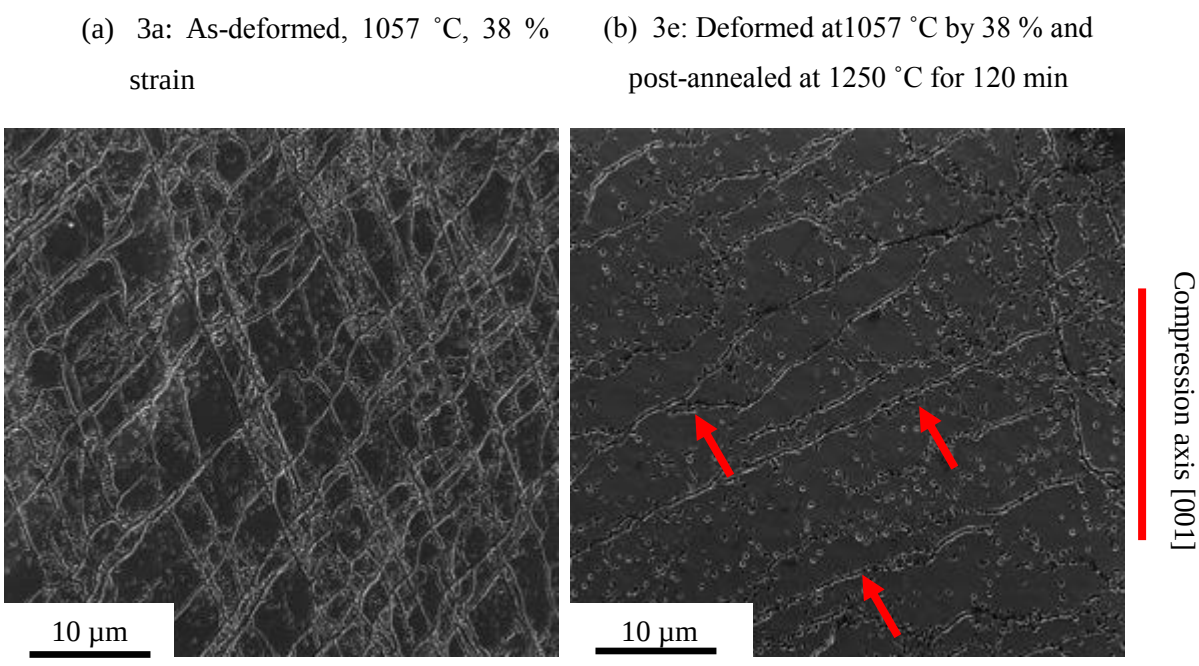


Figure 4.2 Higher magnification micrographs of surface etch pits morphology and distribution in (a) as-deformed state (sample 3a: 1057˚C, 38% strain) and (b) post subsequent annealing at 1250 ˚C for 120 min (sample 3e), polygon walls are indicated by red arrows. The compression axis is vertical in these micrographs.

4.4.1.2 TEM investigation of defect morphology in the as-deformed and annealed samples

In order to directly reveal the bulk defect morphology in the deformed silicon sample, the TEM diffraction contrast technique was determined to be the most suitable approach. Conventional TEM specimen preparation method was attempted however was proved to be infeasible due to the extremely high residual stress in the deformed sample. The thin silicon foil specimen was found cracking routinely during the process. FIB lift-out technique was then applied to produce thin TEM foils and the detailed processing steps were described in the previous chapter.

Since the defect microstructures of both deformed and annealed samples were rather inhomogeneous, and TEM specimens could only reveal defects in a limited area, the most representative region was chosen to produce TEM foil samples. As illustrated in Figure 4.3, in an as-deformed sample, a TEM foil was made across the cell walls and perpendicular to the compression axis. The foil surface is then approximately parallel to the strain plane and the foil normal is close to [001] direction. The foil size is initially 15 μm x 6.5 μm x 100 nm.

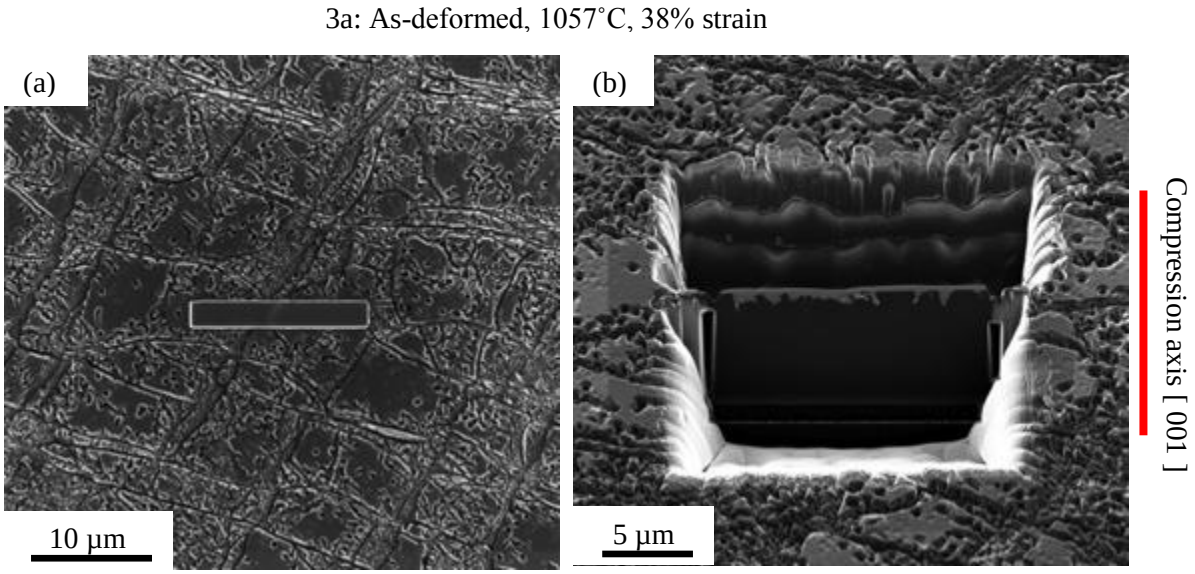


Figure 4.3 (a) A thin layer of platinum was deposited to protect the specimen from ion implantation in subsequent ion milling process; (b) Manufactured TEM foil in the ditch before lift out.

In order that all defects could be observed, the TEM specimen was initially examined by imaging along the [001] zone axis, using the centre spot (000), as shown in Figure 4.4. Long parallel sub-grain boundaries comprising dense short dislocation segments were observed across the whole specimen, as indicated by red arrows in Figure 4.4 (a). These sub-grain boundaries are on average spaced 2µm apart, corresponding to the surface cell wall structure. Henceforth it is inarguable that the slip lines observed constructing the cellular structures are essentially sub-grain boundaries. Higher magnification TEM bright field images revealed highly defected regions featured by intersected dislocation networks and sub-grain boundary composed of short dislocation arrays are clearly observed, as marked by the red arrow in Figure 4.4 (b). In addition, relatively long dislocation segments piled up at sub-grain boundary was also observed, as denoted by the red arrow in Figure 4.4 (c).

A representative region containing distinguishable individual dislocation segments was selected to image in different { 220 } two-beam conditions to characterize the relevant dislocation Burgers vector. It is evident that several dislocations disappeared under diffraction condition **g** = 220, and appear under **g** = $2\bar{2}0$, as marked by blue arrows in Figure 4.5 (a) and (b), respectively.

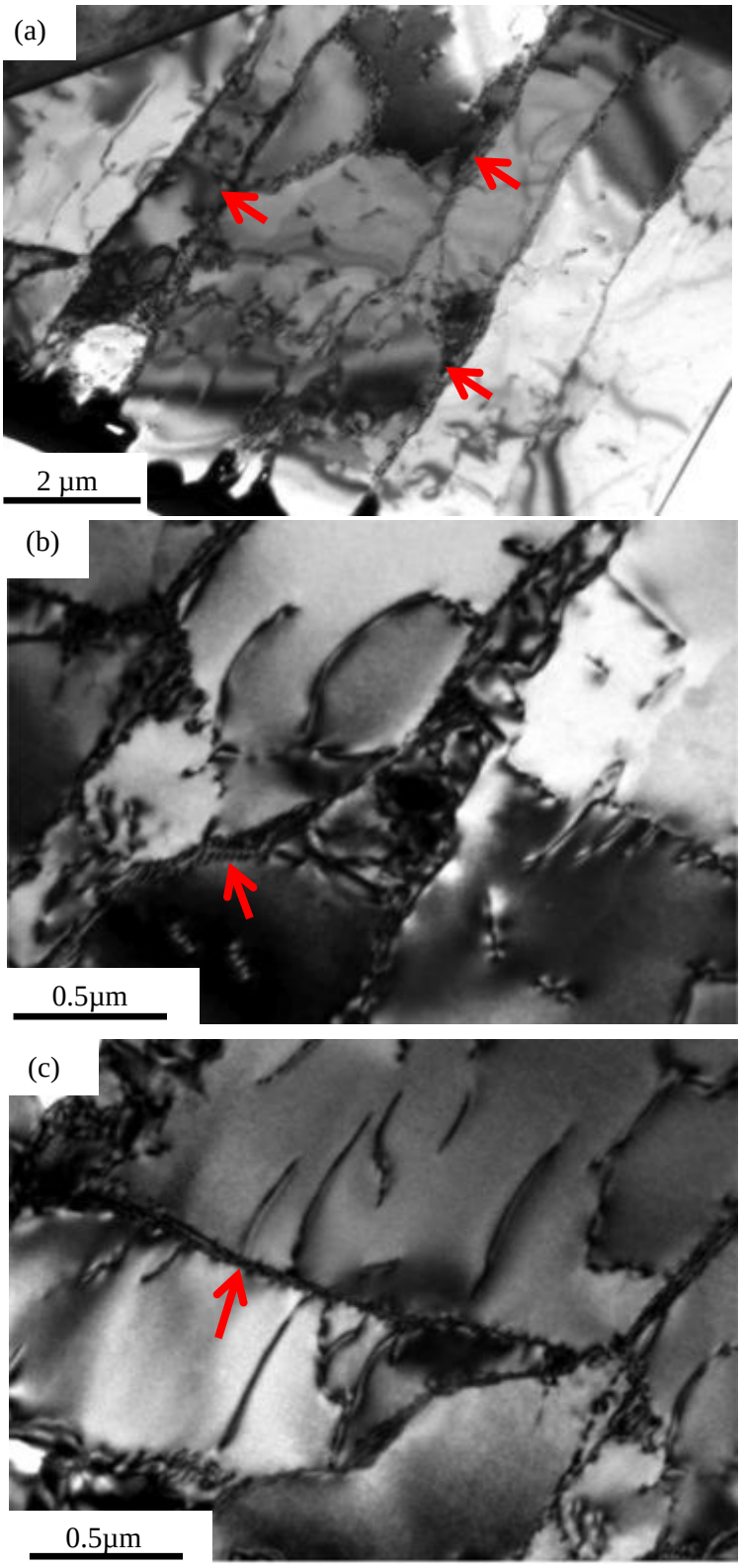


Figure 4.4 TEM bright field micrographs of as-deformed sample (3a: 1057 ˚C, 38 % strain), imaged close to (001) pole: (a) Low magnification micrograph revealing the overall defects morphology, sub-grain boundaries are denoted by red arrows; (b) and (c) Higher magnification micrographs showing detailed dislocation configuration and interaction, sub-grain boundaries are also marked by red arrows.

These dislocations were then determined to obtain Burgers vector ½ [$1\bar{1}0$] according to the **g .b** = 0 criterion. It is also observed that these dislocations lie approximately parallel to [$1\bar{1}0$] direction, henceforth they are configured to maintain ½ [$1\bar{1}0$] pure screw character. Since the foil normal is close to (001) pole, and dislocations in silicon lie in (111) slip planes, dislocation segments observed in this specimen are mostly very short, approximately 200nm long. However, there also exist few longer segments with line length of 2 ~ 3 μm.

For the purpose of observing dislocations in greater contrast, weak beam dark field imaging method was applied. Figure 4.5 (c) shows (**g, 3g**, with **g** = $2\bar{2}0$) condition was used and the micrograph was imaged using ($6\bar{6}0$) reflection. Only very close to the dislocation are the planes of atoms sufficiently tilted to come into the Bragg position, the dislocations appear as narrow bright lines against dark background under this condition.

By applying dislocation density measurements of counting the number of dislocation intersections with the foil surface [191], the dislocation density of this specific region was determined to be 7.5 x 10^{12} m^{-2}. Since not all dislocations in diamond lattice structure are visible under { 220 } reflection, specifically 1/6 dislocations with Burgers vector ½ [110] remain invisible under **g** = ($2\bar{2}0$) reflection condition. With this factor taken into account, the total dislocation density was compensated and determined as 9.0x10^{8} cm^{-2}. It should be noted that this value only applies to this specific region and only the magnitude might be representative. The dislocation density magnitude is in good agreement with the one calculated by etch pits counting, as discussed in Section 4.4.1.1.

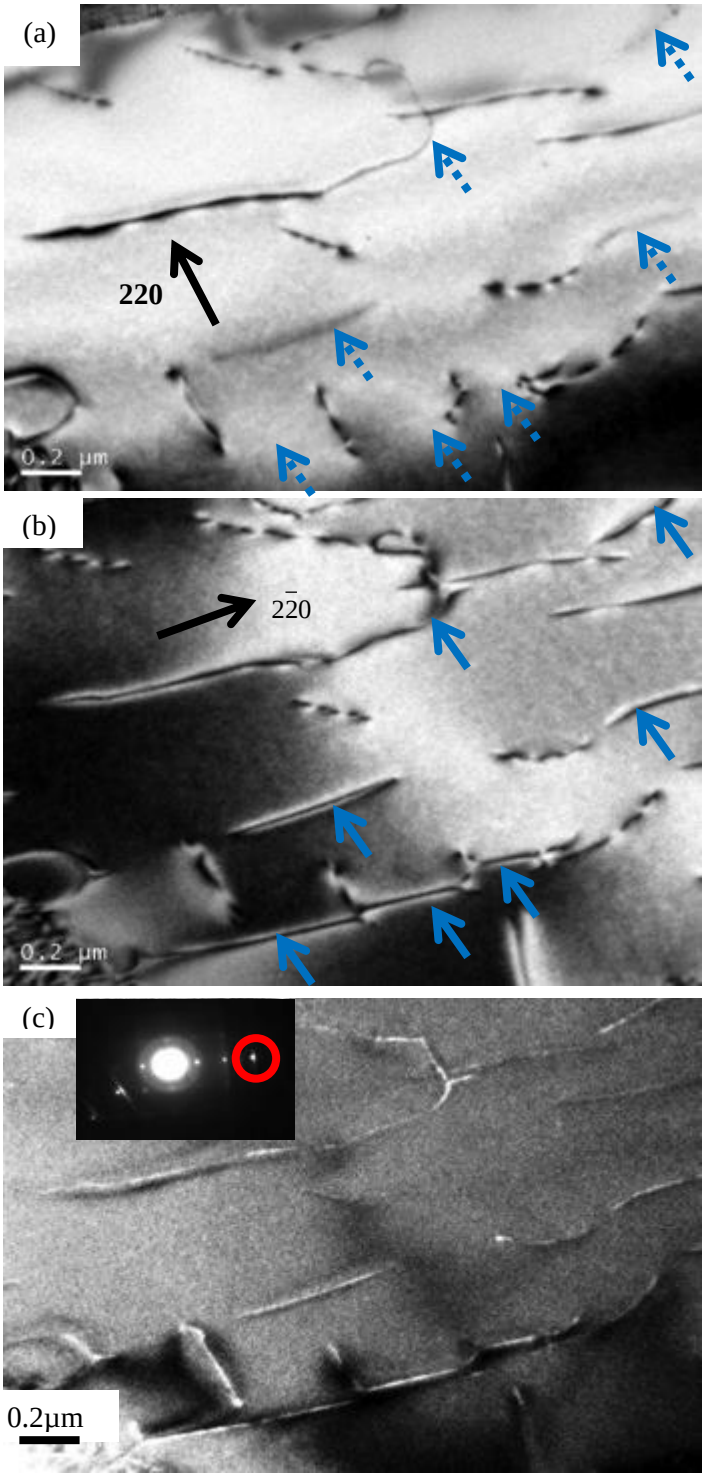


Figure 4.5 Representative TEM micrographs of the as-deformed specimen (3a: 1057 ˚C, 38 % strain), imaged using different {220} two-beam conditions close to (001) pole, illustrating the analysis used to determine ½($1\bar{1}0$) Burgers vector dislocation disappearing under (a) **g** = 220,

and appearing under (b) **g** = $2\bar{2}0$, (c) Weak beam dark filed image (**g**, **3g**, with **g** = $2\bar{2}0$) illustrating high distorted dislocation core areas, the diffraction spot used was marked by red circle.

In order to characterise the bulk defect morphology of samples annealed at 1250 ˚C for 120 min (sample 3e), a piece of TEM foil was also produced from the region where recovery took place, as shown in Figure 4.6 (a). The specimen was specifically manufactured across two polygon walls and the foil surface was close to (111) pole, therefore initially viewed along [111] zone axis, using (000) centre spot, as shown in Figure 4.6 (b). It is obvious that the recovered area manifests remarkably different dislocation morphology and the TEM micrograph shows two dislocation arrays extended from the sample surface into the bulk. The overall dislocation density is significantly lower than the as-deformed sample, from qualitative observation.

3e: Deformed at 1057 ˚C by 38 % and post-annealed at 1250 ˚C for 120 min

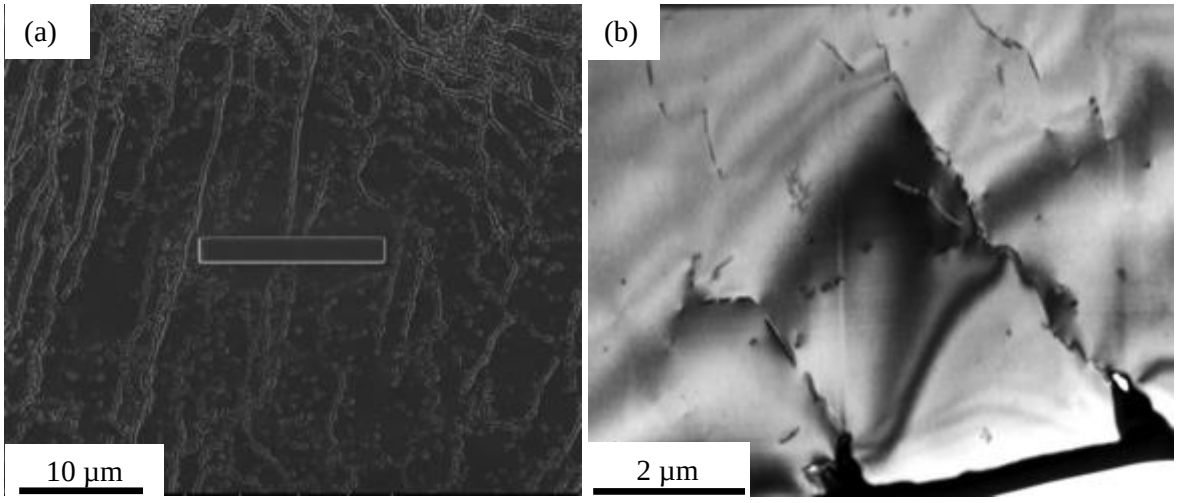


Figure 4.6. (a) TEM foil made from a selected representative polygonised region in sample 3e (deformed at 1057 ˚C by 38 % and annealed at 1250 ˚C for 120 min); (b) TEM bright field micrograph of this specimen imaged close to (001) pole.

A representative region was selected for detailed dislocation character configuration and bright field micrographs were recorded under different two-beam conditions, as shown

in Figure 4.7 (a)-(e). Two intersecting dislocation arrays were observed, as indicated by blue arrows and yellow arrows. The dislocation array marked by blue arrows lies approximately along [$2\bar{2}0$] direction and are invisible under ($1\bar{1}1$) and (220) reflection, whose Burgers vector was then unambiguously characterised as ½[$1\bar{1}0$] according to **g.b**=0 criterion, consequentially this dislocation array consists of ½[$1\bar{1}0$] screw dislocations. In contrast, the dislocation array denoted by yellow arrows lies parallel to [220] direction and disappear under ($2\bar{2}0$) and ($1\bar{1}0$) diffraction conditions, therefore they are identified as ½[110] screw dislocations. In addition, the dislocation marked by purple circle disappeared under ($1\bar{1}1$) and ($0\bar{4}0$) reflections, which is in consistent with ½[101] Burgers vector.

The dislocation density in this area is counted as 3.5 x 10^{12} m^{-2} by measuring the number of dislocation lines threading the foil surface, which is in the equivalent order of magnitude as the value measured by etch pits counting, see Section 4.4.1.1.

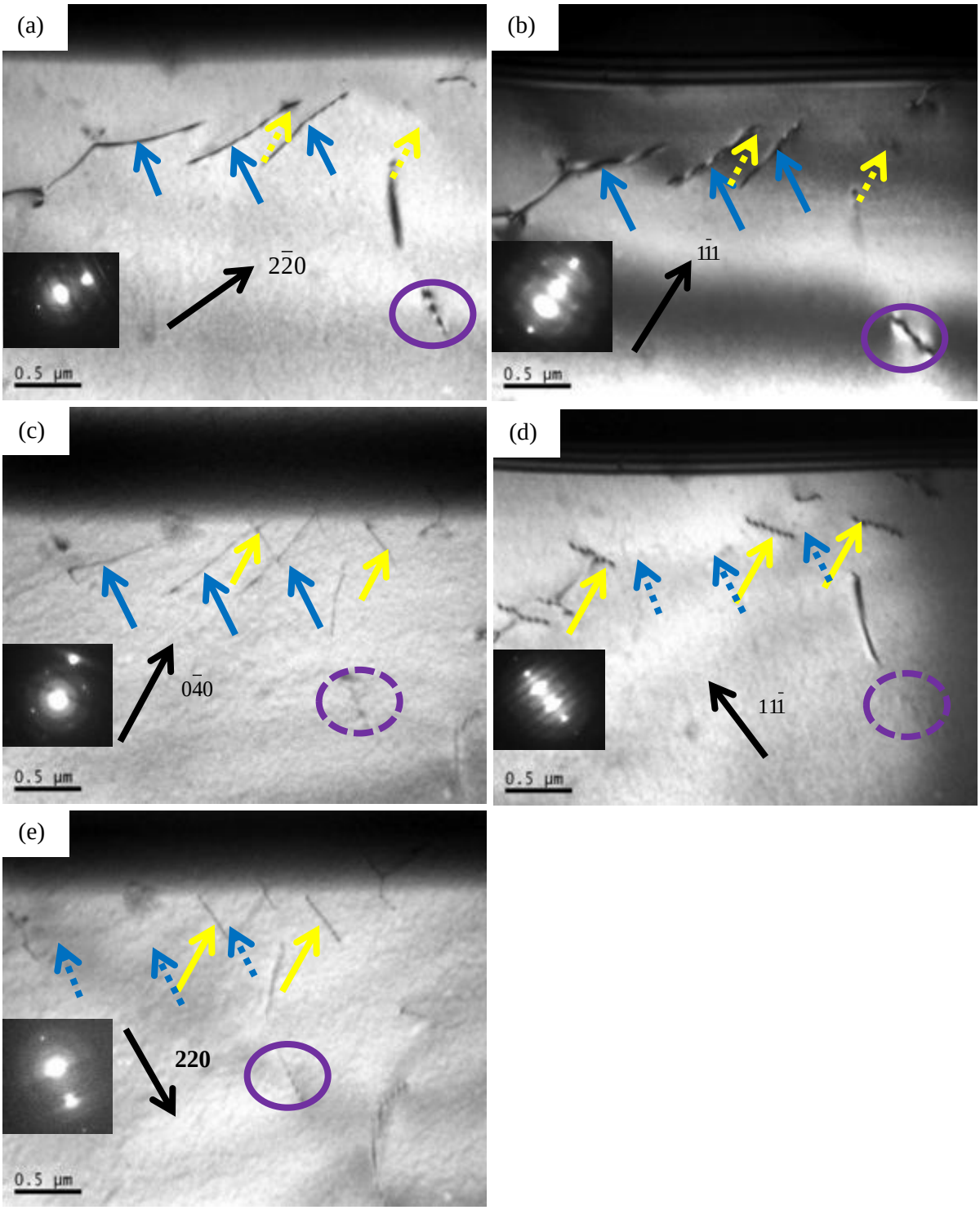


Figure 4.7 Bright field TEM micrographs imaged using different two-beam conditions to determine the Burgers vectors of dislocations in sample 3e (deformed at 1057 ˚C by 38 % and annealed at 1250 ˚C for 120 min): (a) **g** = ($2\bar{2}0$); (b) **g** = ($\bar{1}11$); (c) **g** = ($0\bar{4}0$); (d) **g** = ($1\bar{1}1$); (e) **g** = (220).

4.4.2 Deformation at 1068 ˚C by 36 % along [001] direction (4th deformation)

Concerning the reproducibility of the uniaxial compression of cube silicon sample and towards the interest of testing the furnace limit, a second deformation was conducted under similar conditions with slightly higher deformation temperature and average strain rate, which were 1068 ˚C and 1.25 x 10^{-5} s^{-1} respectively. The compression was also performed along [001] crystallographic direction and the total strain introduced was 36%. The deformed silicon sample was then subjected to subsequent annealing at 1250 ˚C for 120 min. The surface microstructures of as-deformed and subsequently annealed samples revealed by preferential etching and selective TEM configuration of bulk defects are presented in this section.

4.4.2.1 Microstructures of the as-deformed and annealed samples by SEM

It is evident that deformation with slightly higher temperature and strain rate produces similar deformation microstructure, however probably lower dislocation density. The as-deformed surface microstructure was comprised of relatively straight intersecting slip lines primarily lie in two different directions approximately perpendicular to each other (as highlighted by white lines) and constitute a network structure consisting of 5μm square cells. The dislocation etch pit density varies from cell to cell, ranging from approximately 1.0 x 10^{12} m^{-2} to 1.0 x 10^{12} m^{-2}. Certain cells (such as marked by ‘A’) contain a rather homogeneous etch pits distribution throughout the cell interior, whereas others possess very few etch pits located close to cell walls (marked by ‘B’). A remarkable microstructure change brought about by annealing was the curved cell boundaries and relatively irregular cell wall directions, indicating the occurrence of recovery process, as illustrated in Figure 4.8. The cell dimension was also increased

from 5 μm to approximately 10 μm after annealing. The dislocation density appeared more unevenly distributed across the sample surface. Certain high dislocation density area (marked by 'A') contains overlapping etch pits with a numerical density of approximately beyond 1.0 x 10^{13} m^{-2}, whereas certain lower dislocation density area (marked by 'B') featured by spatially scattered etch pits with an average density of 5.0 x 10^{11} m^{-2}.

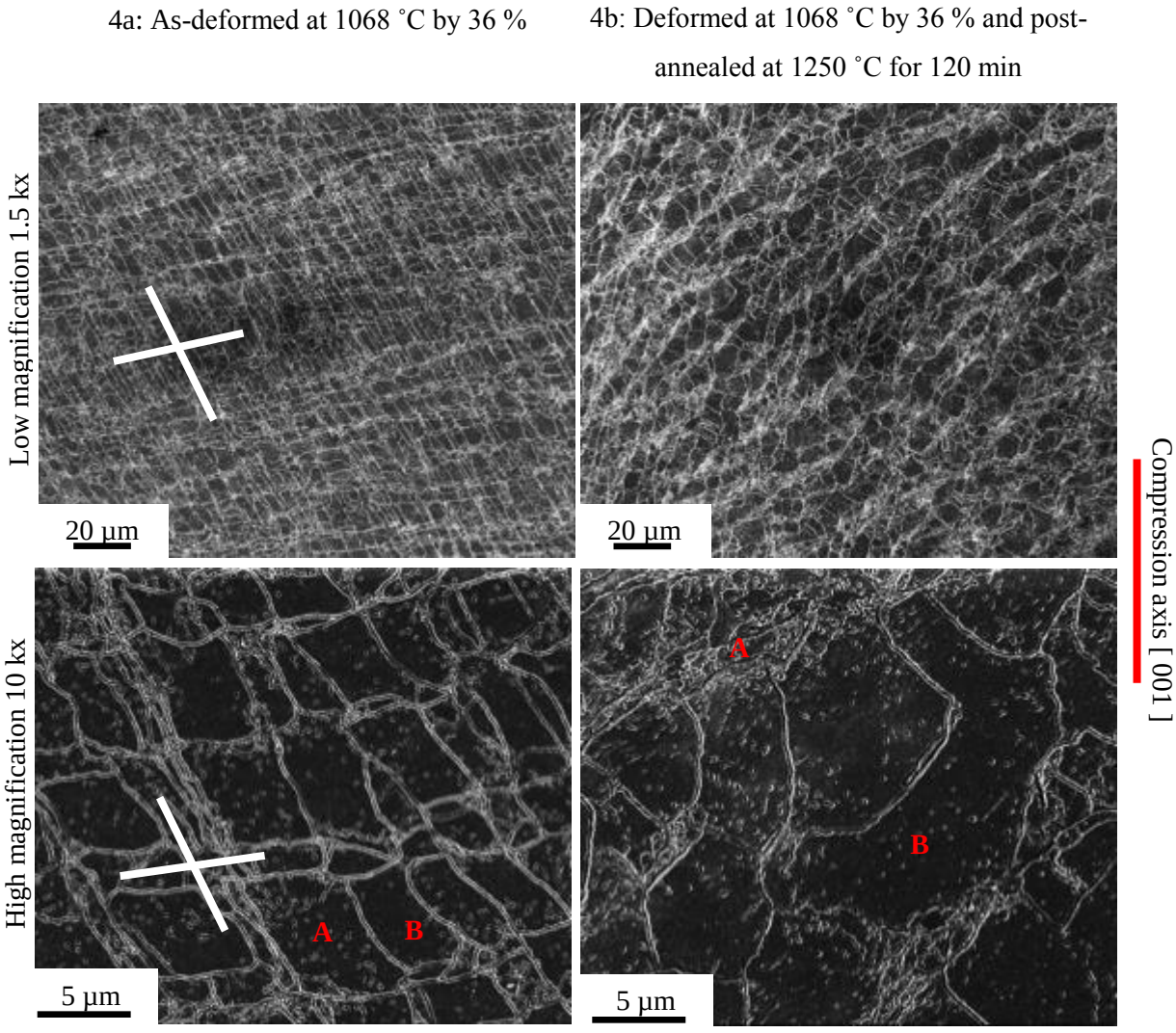


Figure 4.8 SEM micrographs of preferentially etched sample 4a (as-deformed at 1068 ˚C by 36 %) and sample 4b (deformed at 1068 ˚C by 36 % and annealed at 1250 ˚C for 120 min). Compression axis is vertical in these micrographs.

4.4.2.2 TEM investigation of defect morphology in as-deformed and annealed samples

Bulk defect morphologies were also examined in selected regions in the as-deformed and subsequently annealed samples, respectively. A piece of TEM foil was fabricated perpendicular to the compression axis across several subgrain boundaries from the as-deformed sample, as illustrated in Figure 4.9.

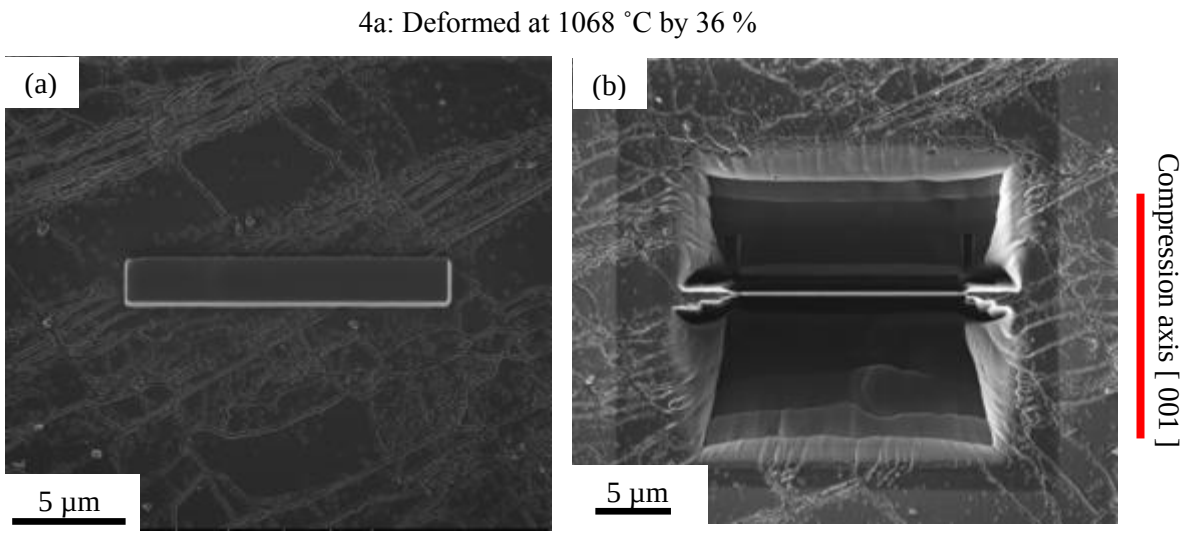


Figure 4.9 (a) TEM foil made from a representative region in sample 4a (deformed at 1068˚C by 36 %), (b) manufactured TEM foil in the ditch before lift out.

The as-deformed sample has a highly defective microstructure, as shown in Figure 4.10 (a). Higher magnification TEM bright field image displayed a distinct fragment of spatial dislocation network structure with dislocation lines 100 nm apart, believed to be introduced by plastic deformation, as highlighted by the red arrow in Figure 4.10 (b). Similar dislocation network was observed by previous researchers in plastically deformed germanium deformed at 720 ˚C by 5 % strain [218]. Since the foil normal was close to (001) pole and dislocations in silicon generally habit on the { 111 } slip planes, only short dislocation segments less than 500 nm in length were observed in this specimen as they are generally inclined with respect to the foil surface. Dislocation

tangles from pile-up of a large number of dislocations were also clearly observed in certain regions, as marked by the red arrow in Figure 4.10 (c). The complexity of this type of dislocation tangles make it unrealistic to identify individual dislocations and establish their configurations. However, it is estimated that this type of dense dislocation containing region has an average density higher than 1.0×10^{13} m^{-2}, which is in good agreement with the number measured by etch pit counting.

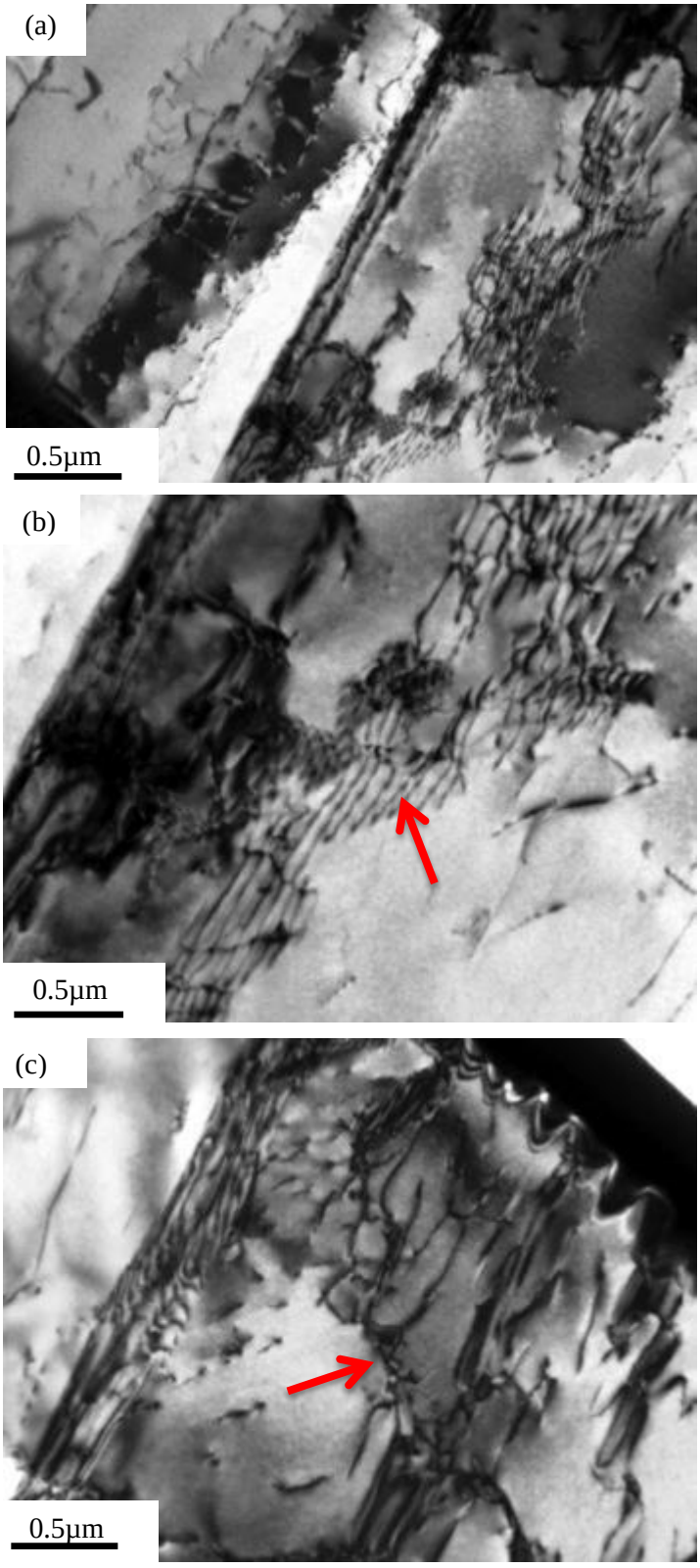


Figure 4.10 TEM bright field micrographs of sample 4a (As-deformed at 1068 ˚C by 36 %) viewed close to [001] zone axis using centre spot (000): (a) Low-magnification image of the specimen overview; (b) and (c) Higher magnification micrographs of typical dislocation network and dislocation tangles induced by plastic deformation.

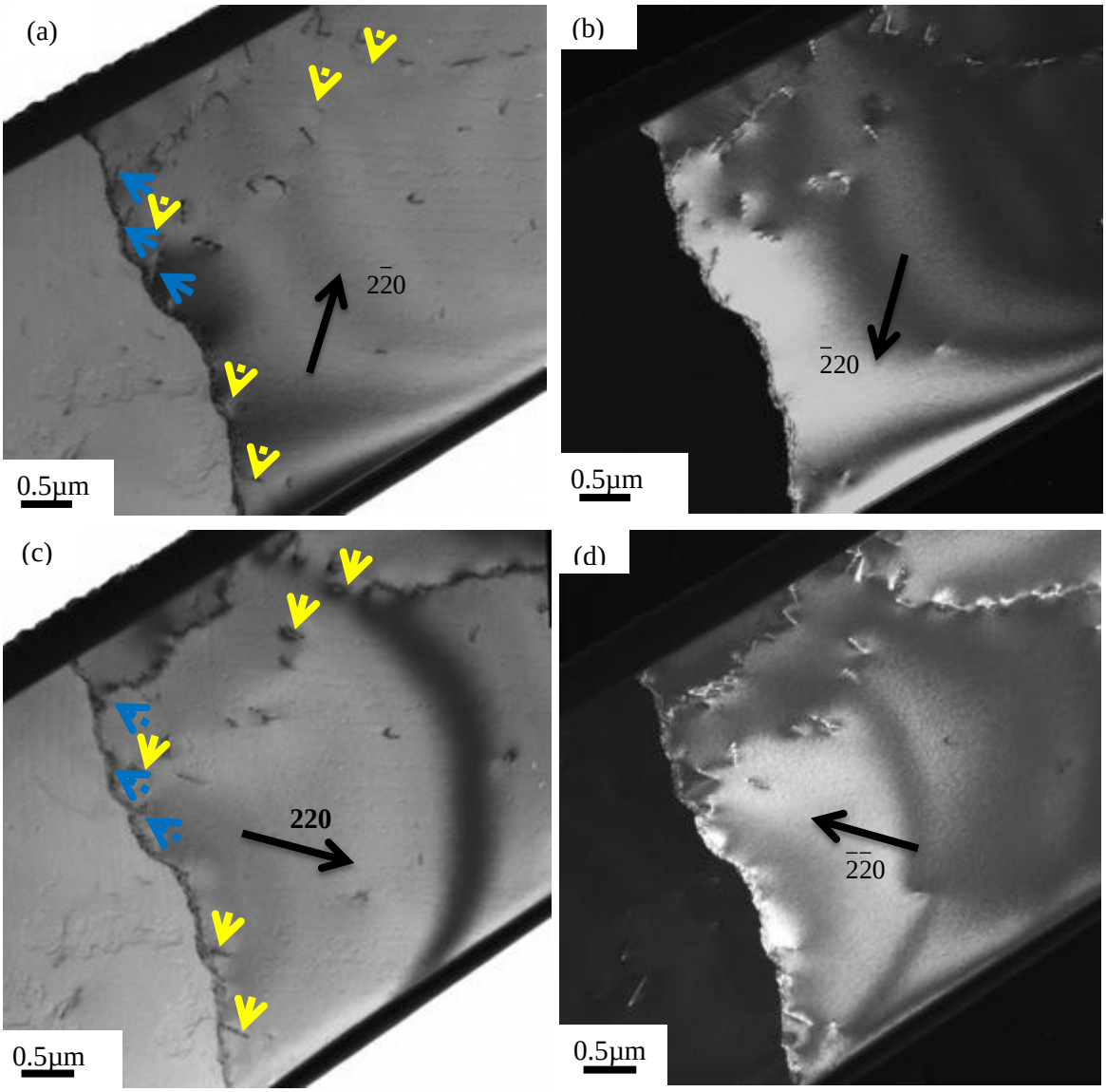


Figure 4.11 TEM foil made across a sub-grain boundary in sample 4b (deformed at 1068 ˚C by 36 % and subsequently annealed at 1250 ˚C for 120 min, TEM micrograph of this specimen imaged under different { 220 } two beam conditions: (a) Bright field image using centre spot (000), **g** = ($2\bar{2}0$); (b) Dark field micrograph using **g** = ($\bar{2}20$) reflection; (c) Bright field micrograph imaged using centre spot (000), **g** = (220); (d) dark field micrograph using **g** = ($\bar{2}\bar{2}0$) reflection.

In contrast, a TEM foil was made across a subgrain boundary from the subsequently annealed sample, as shown in Figure 4.11 (a). The specimen was then imaged under different { 220 } two-beam conditions. Dislocations lie parallel to the [$2\bar{2}0$] direction

appeared visible under the ($2\bar{2}0$) reflection and invisible under the (220) reflection, as marked by blue arrows in Figure 4.11 (b) and (d), henceforth are inconsistent with pure screw character with ½[$1\bar{1}0$] Burgers vector. Similarly, dislocations highlighted by yellow arrows in Figure 4.11 (b) and (d) behaved in the opposite manner, lying in the [220] direction and appeared visible under (220) reflection and vanished under ($2\bar{2}0$) reflection. This type of dislocations was defined as nearly pure ½[110] screw dislocations. The dislocation density in this specific specimen was estimated to be approximately 10^{12} m^{-2} magnitude in grain interior.

As illustrated in the present section, deformation of initial dislocation free single crystalline silicon at approximately 1050 ˚C by 38 % strain produces a distinguished plastic deformation microstructure featuring a large number of dislocations. Subsequent annealing at 1250 ˚C initiates recovery process however recovery is not completed within 120 min. The dislocation density was observed to decrease by approximately one order of magnitude in the recovered region. Therefore high temperature plastic deformation utilizing the apparatus available was undoubtedly proven feasible, but the annealing condition was inadequate for optimal microstructure alteration and required further evaluation.

4.5 Deformation of flat cube shape single crystalline silicon

As stated in Section 4.2, due to the limitation of the cube sample size, the deformed material obtained was insufficient to allow minority carrier lifetime measurement using the QSS-PC system available. Henceforth the sample size was modified into dimensions of 15 mm x 15 mm x 10 mm with the 10 mm side parallel to compression axis, in order to increase the possibility of obtaining deformed material with suitable dimensions for lifetime testing. The cross-section area was then 225 mm^2 compared to the initial 100 mm^2. Four compression experiments were carried out in total using this type of sample, with sufficiently higher deformation temperature (in the range from 1077 ˚C to 1150 ˚C). Besides, the subsequent annealing conditions were also adjusted for the purpose of enhancing the recovery process by means of significantly increase the annealing temperature. The detailed microstructure evolution investigated in three effective deformations by preferential etching/SEM and TEM is described in the present section.

4.5.1 Deformation at 1077 ˚C by 38 % along the [001] direction (5^{th} deformation)

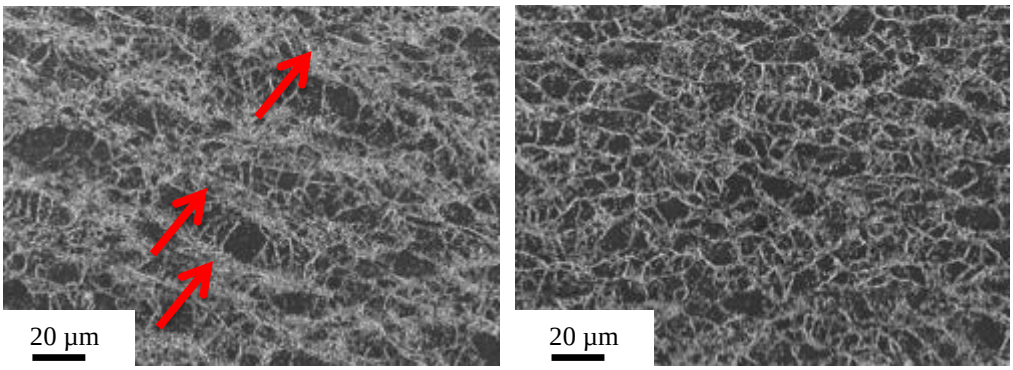
The first compression test of a silicon sample with a larger cross-sectional area was performed at 1077 ˚C along the [001] crystalline direction. The total strain induced into the sample during the deformation was 38 % and the average strain rate was 1.41 x 10^{-5} s^{-1}. However, the deformed silicon sample produced by this compression run contained many cracks presumably due to the high strain and relatively low deformation temperature. The silicon sample was sliced along the compression direction and the microstructures revealed by SEM micrographs were in the compression plane.

4.5.1.1 Microstructures of as-deformed and annealed samples by SEM

In common with previous deformation microstructure evaluation in Section 4.4, preferential etching revealed a profound dislocation etch pits cell structure in the as-deformed initially dislocation free Czochralski single crystalline silicon, as illustrated in Figure 4.12 (a). It is evident that 38 % plastic deformation gave rise to a highly defected microstructure. The major slip line traces generally form stripe shape lying 45˚ from the compression direction, as marked by red arrows in Figure 4.12 (a). The etch pit distribution was relatively heterogeneous in this as-deformed material, whereby certain areas contain undistinguishable overlapping etch pits whereas other slip line cells contain scattered etch pits. The cell size also has a remarkable variation across the sample surface, from less than 5 μm to approximately 20 μm. The as-deformed material was then subjected to subsequent annealing at 1375 ˚C for 30 min, 60 min, 90 min and 120 min, respectively. The corresponding SEM micrographs showing the surface microstructure evolution are displayed in Figure 4.12 (b)-(e). In interests of exploring higher annealing temperature and evaluating the consequential microstructure, annealing condition of 1400 ˚C for 120 min was selected and the SEM micrograph is shown in Figure 4.12 (f).

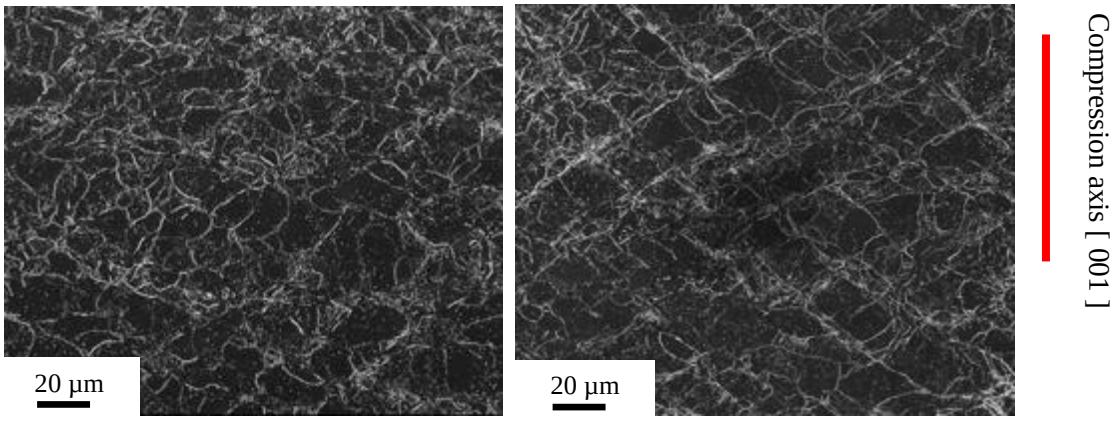
(a) 5a: As-deformed, 1077 ˚C by 38 %

(b) 5b: Deformed at 1077˚C by 38% and annealed at 1375˚C for 30min



(c) 5c: Deformed at 1077 ˚C by 38 % and post-annealed at 1375 ˚C for 60 min

(d) 5d: Deformed at 1077˚C by 38% and annealed at 1375˚C for 90min



(e) 5e: Deformed at 1077 ˚C by 38 % and post-annealed at 1375 ˚C for 120 min

(f) 5f: Deformed at 1077 ˚C by 38 % and post-annealed at 1400 ˚C for 120 min

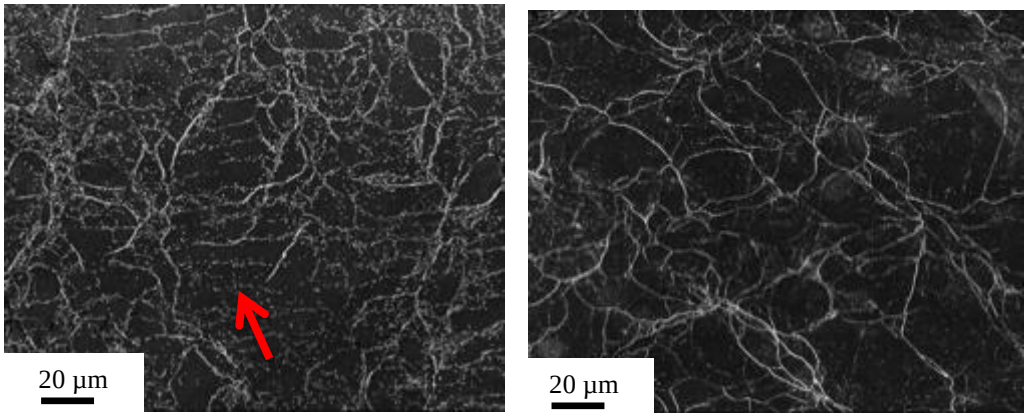


Figure 4.12 SEM micrographs of preferentially etched surface: (a) sample 5a (as-deformed at 1077 ˚C by 38 %); (b) sample 5b (deformed at 1077 ˚C by 30 % and annealed at 1375 ˚C for 30 min), red arrows mark the major slip line traces; (c) sample 5c (deformed at 1077 ˚C by 30 % and annealed at 1375 ˚C for 60 min); (d) sample 5d (deformed at 1077 ˚C by 30 % and annealed at 1375 ˚C for 90min); (e) sample 5e (deformed at 1077 ˚C by 30 % and annealed at 1375 ˚C for 120 min), the red arrow marks the polygon walls; (f) sample 5f (deformed at 1077 ˚C by 30 % and annealed at 1400 ˚C for 120 min). The compression axis is vertical in these micrographs.

Visual examination of the surface microstructural evolution with respect to annealing time at 1375 ˚C reveals a general trend of decreasing dislocation etch pit number with increasing annealing time length. Annealing at 1375 ˚C for 60 min exerts a considerable impact on the reduction of dislocation density. Microstructure after prolonged annealing displays an unambiguous characteristic alteration, featured by increased sub-grain cell dimensions and dislocation etch pit rearrangement. The most significant microstructure character brought about by high temperature annealing is the occurrence of polygon walls essentially in the form of relatively straight dislocation etch pits arrays, attributing to the mobility of dislocations at elevated temperatures, as indicated by red arrow in Figure 4.12 (e). This type of polygon walls was exclusively observed in the sample annealed at 1375 ˚C for 120 min and the spacing between neighbouring walls is generally approximately 10μm. By examining the microstructure of the sample annealed at 1400 ˚C for 120 min it is explicit that the sub-grain cell size is up to 50 μm, noticeably larger than the one annealed at 1375 ˚C for 120 min.

(a) 5a: As-deformed, 1077˚C by 38%

(b) 5f: deformed at 1077 ˚C by 38 % and post-annealed at 1400 ˚C for 120 min

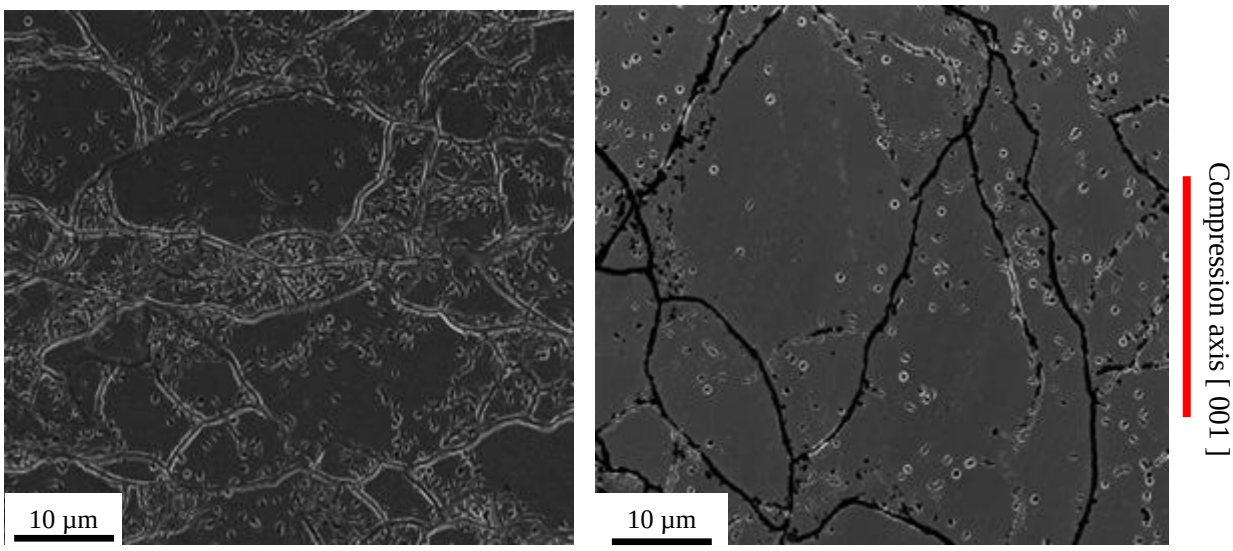


Figure 4.13 Higher magnification SEM micrographs of etched surface: (a) Sample 5a (deformed at 1077 ˚C by 38 %); (b) Sample 5f (deformed at 1077 ˚C by 38 % and annealed at 1400 ˚C for 120 min).

Direct comparison of the microstructure morphology of as-deformed and post-annealing 1400 ˚C for 120 min sample was accomplished by higher magnification SEM micrographs, as displayed in Figure 4.13. In consistent with the previous conclusion, the as-deformed sample maintains a considerable inhomogeneous microstructure, with varying dislocation etch pits density from cell to cell, and in the meanwhile the cell size also varies significantly across the sample surface, as shown in Figure 4.13 (a). The dense etch pits containing area has a density up to 10^{13} m^{-2}, whereas the low etch pit density area obtains an estimated value of 10^{11} m^{-2}, mostly in the interiors of large sub-grain cells. In contrast, the sample undergoing a subsequent annealing at 1400 ˚C for 120 min manifests a relatively homogeneous dislocation density distribution, see Figure 4.13 (b). The overall dislocation density was estimated to be 9.0 x 10^{11} m^{-2}, while the corresponding value of cell interiors was approximately as low as 5.0 x 10^{10} m^{-2}.

4.5.1.2 TEM investigation of defect morphology in annealed samples

In order to characterize further morphology of the bulk defects and verify the bulk dislocation density, a TEM foil specimen was fabricated across a sub-grain boundary in the sample annealed at 1400 ˚C for 120 min. The selected sub-grain boundary adjoined two sub-grains with evident dislocation etch pits density difference, numerically 1.0 x 10^{11} m^{-2} and 3.0 x 10^{11} m^{-2}, respectively. The fabrication location is shown in Figure 4.14.

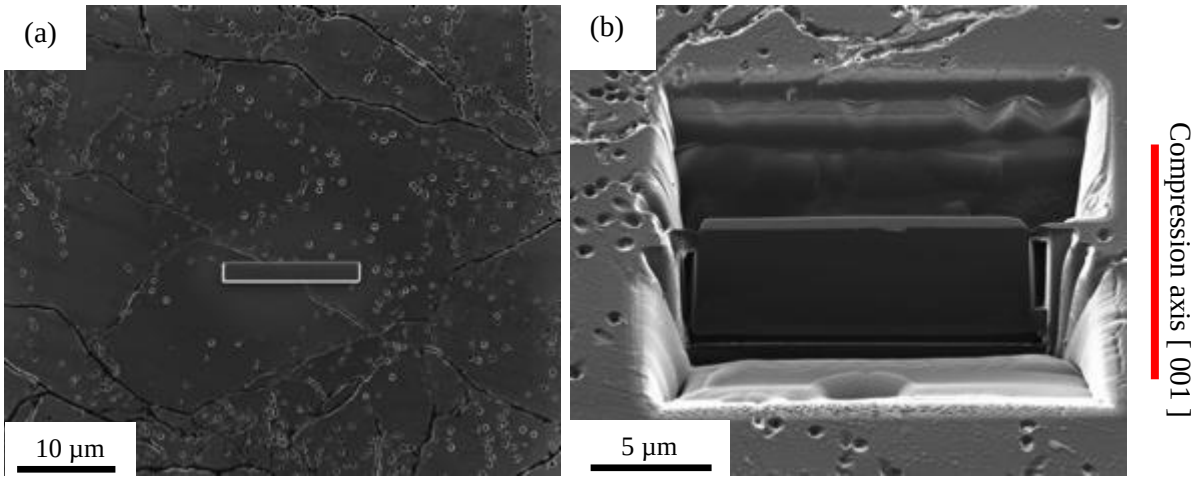


Figure 4.14 A piece of TEM foil was produced from a selected area in sample 5f (deformed at 1077 ˚C by 38 % and subsequently annealed at 1400 ˚C for 120 min): (a) The specimen was produced across a sub-grain boundary; (b) The nearly finished specimen in the ditch before lift out.

The foil normal was found to be close to the (001) pole by examination in TEM. It was then tilted to close to [111] zone axis in order to reveal all defects, the bright field image viewed along the (111) pole using central (000) spot with several strong reflections operating is illustrated in Figure 4.15. It is evident that the sub-grain boundary fabricated in the specimen showed a typical dislocation network structure, extending from the surface to the bulk in a 30˚ inclined direction. Scattered short

dislocation segments were observed on both sides of the sub-grain boundary. By means of counting the number of dislocation segment intersections with foil surface per unit area the dislocation density of the larger grain was calculated to be 3.0 x 10^{11} m^{-2} , which is in good agreement with the value obtained by surface etch pit counting.

Near sub-grain boundary area was then investigated by different { 220 } two-beam conditions close to [111] zone axis for detailed defects character analysis. The corresponding results are displayed in Figure 4.16. The short dislocation segments maintain strong contrast for three { 220 } **g** variants henceforth it was insufficient to determine their Burgers vectors. However, these dislocations were observed to arrange in arrays parallel to [$\bar{2}11$] direction and their line vectors were found to approximately coincide with [$01\bar{1}$] direction. Dark field micrograph imaged using ($0\bar{2}2$) reflection revealed an appreciable hexagonal arrangement of dislocations in the sub-grain boundary, as illustrated in Figure 4.16 (d), which appeared very similar to the hexagonal dislocation net sub-boundaries observed in steady creep stage of silicon under compression strain [32]. This type of dislocation network was also observed previously in deformed germanium by 5 % at 720 ˚C [218].

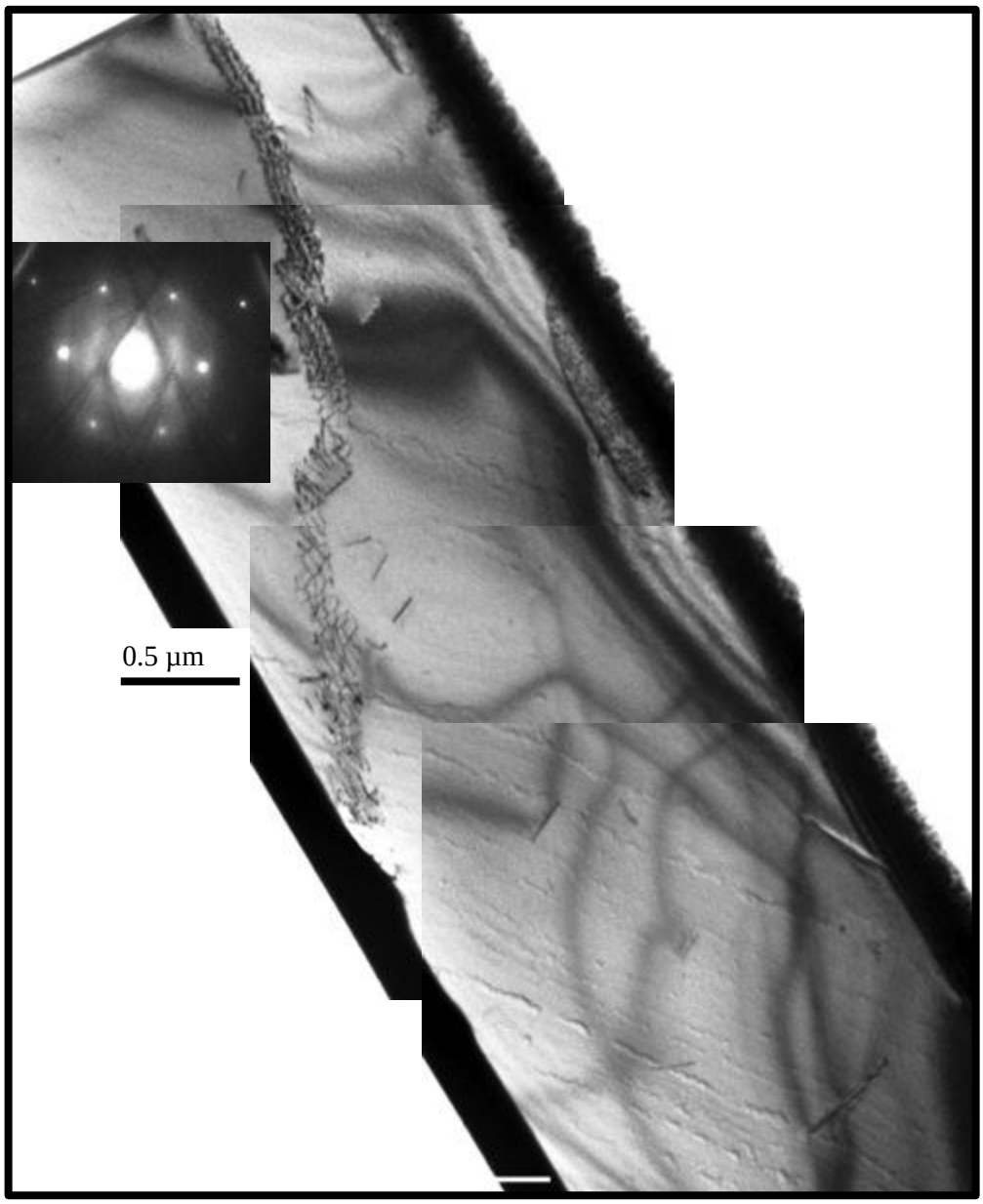


Figure 4.15 TEM bright field micrograph of defects morphology in the bulk of sample 5f (deformed at 1077 ˚C by 38 % and subsequently annealed at 1400 ˚C for 120 min), imaged using (000) spot close to [111] zone axis, with several strong reflections operating at the same time.

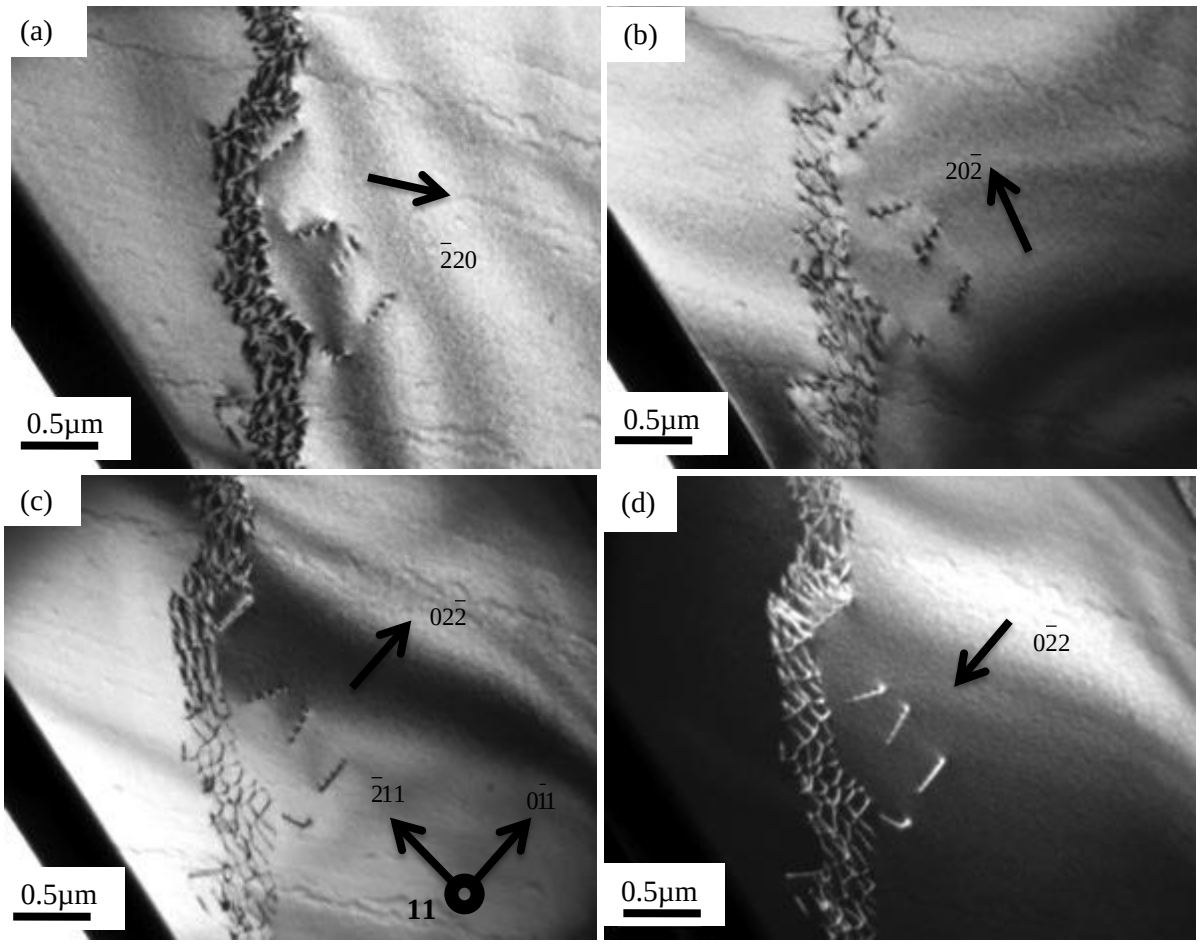


Figure 4.16 TEM micrographs of sample 5f (deformed at 1077 ˚C by 38 % and subsequently annealed at 1400 ˚C for 120 min), under different two-beams conditions close to the [111] zone axis: (a) Bright field micrograph **g** = $\bar{2}20$; (b) Bright field micrograph **g** = $20\bar{2}$; (c) Bright field micrograph **g** = $02\bar{2}$; (d) Dark field micrograph **g** = $0\bar{2}2$.

It was concluded from the above microstructure investigation that uniaxial compression at 1077 ˚C by 38 % induced a dislocation density of approximately 10^{13} m^{-2} into initially dislocation free single crystalline silicon. A recovery process effectively occurred and completed when the highly deformed sample was subjected subsequent annealing at 1400 ˚C for 120 min. The sub-grain cell size was essentially increase from 5 µm to more than 50 µm by high temperature annealing. At the same time, the average dislocation density was estimated to decrease from 10^{13} m^{-2} magnitude to 10^{11} m^{-2}. However, since the obtained as-deformed materials still contain a number of cracks it

was suspected that the deformation temperature was not sufficiently high which resulted in further exploration of higher temperature provided by the furnace.

4.5.2 Deformation at 1130 ˚C by 38 % along the [001] axis (7th deformation)

The deformation temperature was then increased to a higher value of 1130 ˚C. A uniaxial compression test was conducted at this temperature with an average strain rate of 2.64 x 10^{-5} s^{-1}. The total strain induced into the sample was 38 %. However, the obtained as-deformed sample was found to maintain small cracks, presumably due to the relatively higher strain rate applied during the compression process. Since the deformed sample failed to provide a sufficiently large size specimen for the minority carrier lifetime test, it was sliced along the compression axis for microstructure investigation. The as-deformed sample was subjected to annealing at 1375 ˚C and 1400 ˚C for 120 min, respectively. This section presents the corresponding microstructural evaluation results.

4.5.2.1 Microstructures of as-deformed and annealed samples by SEM

As illustrated in Figure 4.17, compression at 1140 ˚C induced a similar deformation microstructure as compression at 1057 ˚C, given the same strain rate and total strain. Dense dislocation etch pits were found to agglomerate along sub-grain boundaries, leaving relatively ‘clean’ sub-grain interior regions. Subsequent annealing at 1400 ˚C for 120 min exerted an appreciable effect on the sub-grain boundary arrangement, specifically altering relative straight sub-grain cell walls to curved ones. The average cell size was increased to more than 50 μm and the average dislocation density was estimated to be 10^{11} m^{-2}.

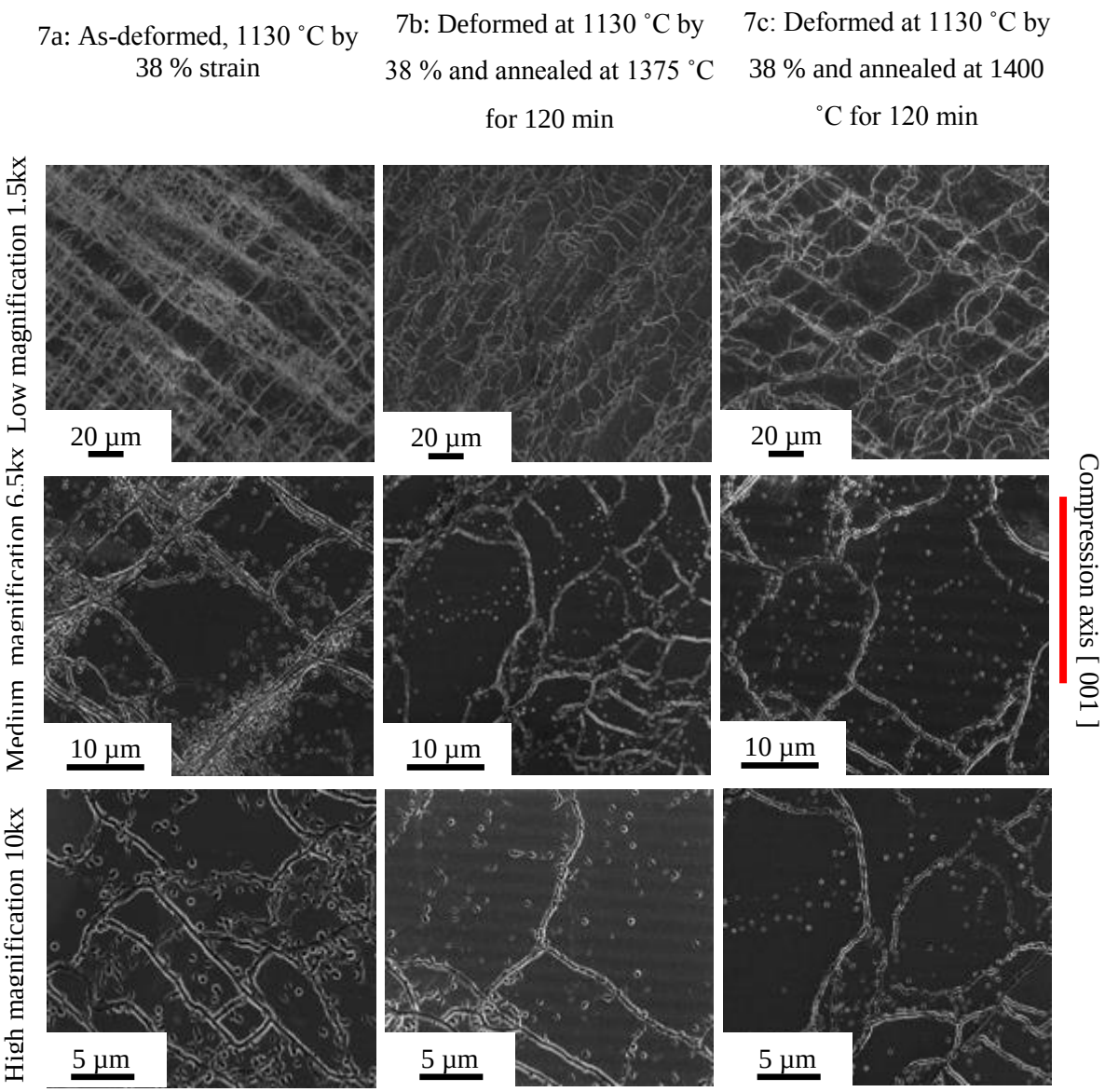


Figure 4.17. SEM micrographs of different magnification of sample 7a (as-deformed at 1130 ˚C by 38 %), sample 7b (deformed at 1130 ˚C by 38 % and annealed at 1375 ˚C for 120 min), and sample 7c (deformed at 1130 ˚C by 3 8% and annealed at 1375 ˚C for 120 min), respectively.

4.5.2.2 TEM investigation of defect morphology in as-deformed and annealed samples

A TEM specimen was fabricated from the as-deformed sample with the foil surface close to the (001) pole, hence TEM bright field images were recorded initially along the [001] zone axis. The overall defect morphology observed in the as-deformed material is consistent with that observed in the previous deformation microstructure investigation, comprising condensed dislocation segments and sub-grain boundaries, as shown in Figure 4.17 (a). Various dislocation structures were discovered, for instance dense dislocation dipole arrays as demonstrated in Figure 4.17 (b), severely defected sub-grain boundary regions appearing as moiré fringe pattern as indicated in Figure 4.17 (c), finally dislocation multipoles in the form of intersected dislocation segments as shown in Figure 4.1 (d). The average dislocation density was estimated as 10^{13} m^{-2} from TEM images.

In contrast, since annealing at 1400 ˚C for 120 min successfully facilitated the recovery process, the TEM sample fabricated from the annealed sample manifested a completely different morphology, as shown in Figure 4.18. Dislocation segments scattered in the grain interior and the corresponding density was estimated as 5.0 x 10^{11} m^{-2}.

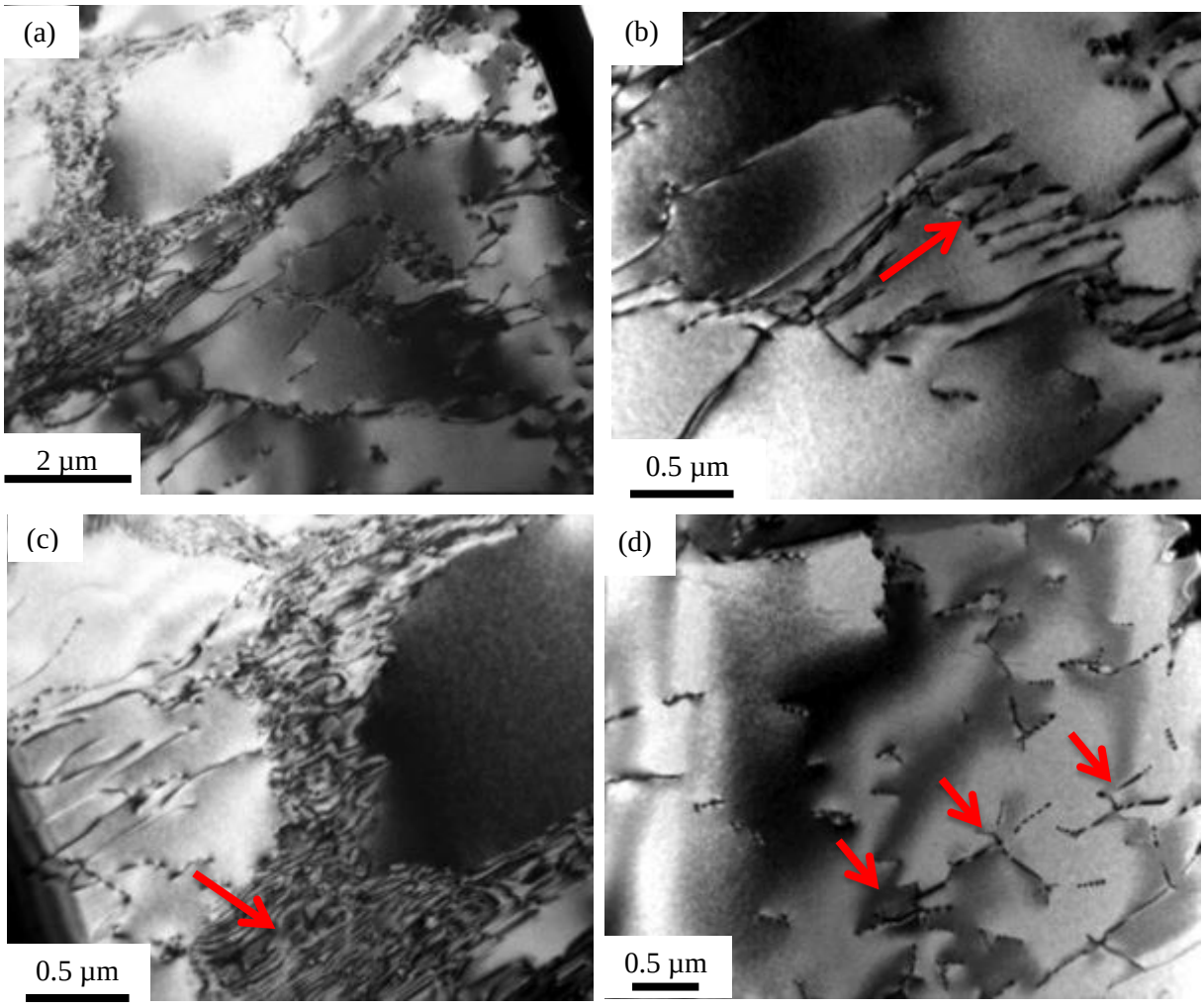


Figure 4.18. TEM bright field micrographs of sample 7a (deformed at 1130 ˚C by 38 %), imaged along the [001] zone axis using central spot (000): (a) Low magnification micrograph showing the general defects morphology; (b) High magnification micrograph demonstrating the dislocation dipole arrays, as indicated by the red arrow; (c) Moiré fringe pattern at highly defective sub-grain boundary region, highlighted by the red arrow; (d) Dislocation nultipoles comprising of intersected short dislocation segments, indicated by red arrows.

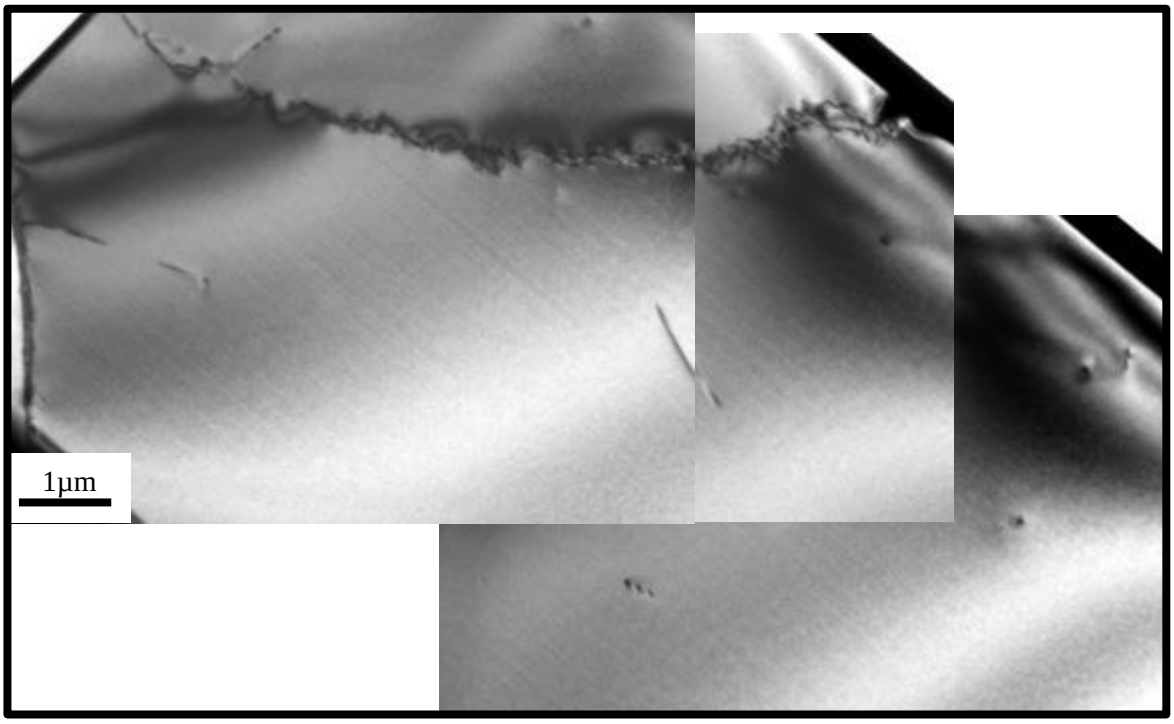


Figure 4.19. TEM bright field micrograph of sample 7c (deformed at 1130 ˚C by 38 % and post-annealed at 1375 ˚C for 120 min) imaged along the [111] zone axis using central spot (000).

The deformation temperature of 1130 ˚C was proved to be achievable and subsequent annealing condition of 1400 ˚C for 120 min was verified to be effective in terms of boosting recovery process resulting in not only sub-grain cell size augmentation but also significant dislocation density reduction. However, due to potentially excessive strain rate, the compression failed to produce a sufficiently large specimen required for the minority carrier lifetime examination. Henceforth, the final deformation was determined to be performed with an equivalently high temperature however with a lower strain rate.

4.5.3 Deformation at 1150 ˚C by 30 % along the [001] axis (8th deformation)

The final uniaxial compression experiment involving deformation of dislocation free single crystalline silicon was conducted at 1150 ˚C along the [001] axis. Total strain of 30 % was induced at an average rate of 1.67 x 10^{-5} s^{-1}. Attributing to the high deformation temperature and relative low strain rate, the as-deformed sample showed the most uniform structure macroscopically from visual evaluation. The deformed sample was then sliced in the direction perpendicular to the compression axis and was found to be satisfactory for lifetime tester. The as-deformed sample was then subject to routine annealing at 1400 ˚C for 120 min. Microstructure morphologies of as-deformed and annealed samples were also evaluated by SEM and TEM.

Viewing perpendicular to the compression axis, as shown in Figure 4.20, microstructure in the strain plane was found to differ from the microstructure in the compression plane with the absence of regular sub-grain cells formed by intersected straight slip lines. Curved sub-grain boundaries were observed predominantly. It is evident that the deformation was heterogeneous since both the sub-grain cell size and etch pits density distribution varied considerably across the sample surface. It was noticed that cell sizes ranged from less than 3 μm to 20 μm, with small cells containing agglomerated dense dislocation etch pits (more than 10^{13} m^{-2}) and large cells appeared much ‘cleaner’ (approximately 10^{11} m^{-2}). Subsequent annealing at 1400 ˚C for 120 min completely altered the surface microstructure, whereby sub-grain cell structures disappeared

completely and sub-grains more than 70 µm were observed. Etch pits counting method revealed an average dislocation density of 1.5 x 10^{11} m^{-2}.

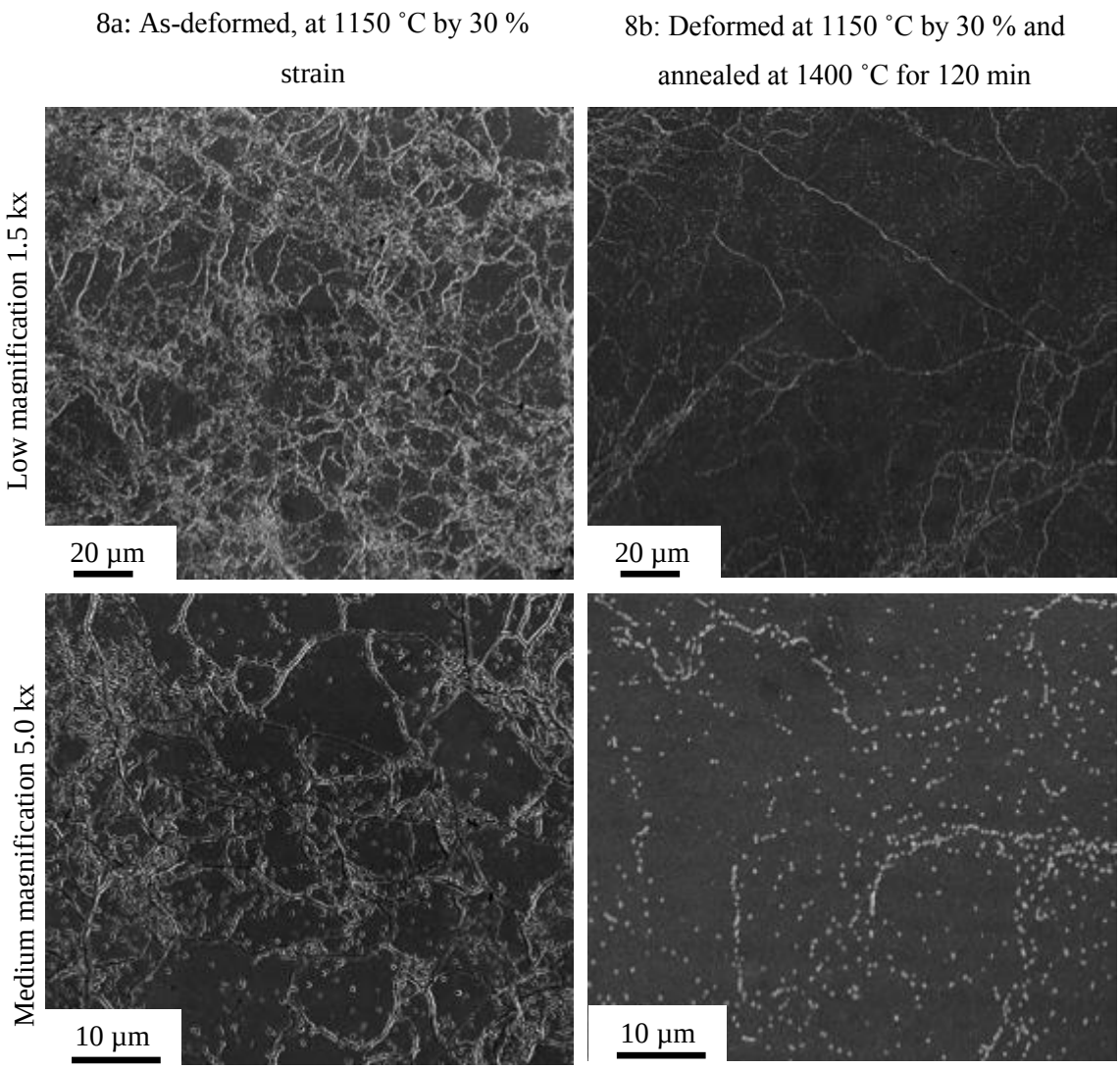


Figure 4.19. SEM micrographs of sample 8a (deformed at 1150 ˚C by 30 % strain) and 8b (deformed at 1150 ˚C by 30 % and annealed at 1400 ˚C for 120 min) surface after preferential etching, imaged perpendicular to the compression axis.

Bulk defects morphology investigated by TEM on the sample annealed at 1400 ˚C for 120 min reveals a low dislocation density configuration, as depicted in Figure 4.21. The dislocation density estimated in the sample is approximately 5.0 x 10^{10} m^{-2}.

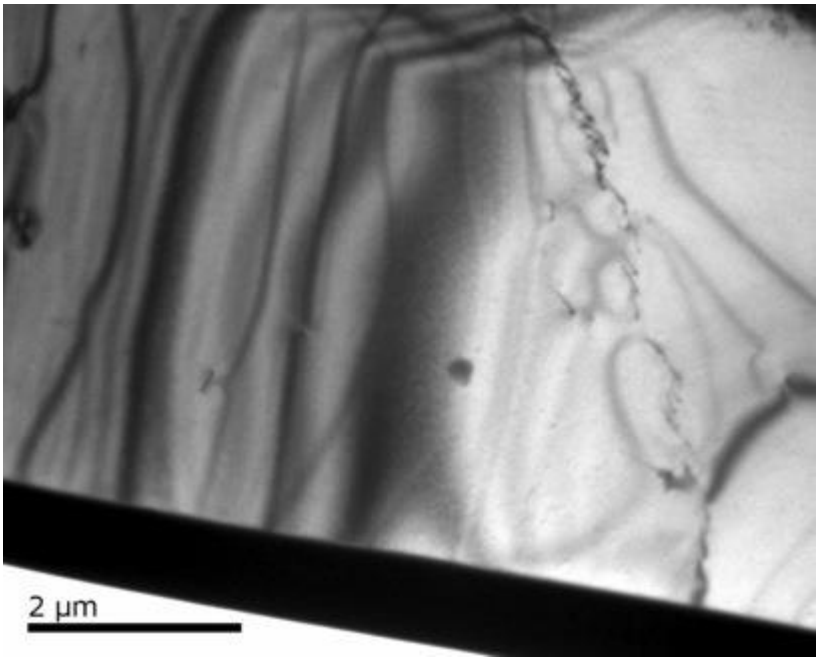


Figure 4.21. TEM bright field micrograph of sample 8b (deformed at 1150 ˚C by 30 % and post-annealed at 1400 ˚C for 120 min) imaged along the [111] zone axis using central spot (000).

It has been proven that the hot deformation of initial dislocation free single crystalline silicon with temperature of 1150 ˚C and 30 % strain was achievable using the available facility, under which condition uniaxial compression produced dislocation density in the order of 10^{13} m^{-2} magnitude. Subsequent annealing at 1400 ˚C for 120 min effectively reduced the dislocation density by two orders of magnitude, down to 10^{11} m^{-2}.

4.6 Discussion and conclusions

In the process of seeking for the optimal attainable deformation and annealing condition provided by the available apparatus, microscopic examination of relevant samples at both as-deformed state and post subsequent annealing state was selected to evaluate the effect of corresponding conditions. The primary observations of the series of deformation tests are as follows:

- Deformation temperature of up to 1150 ˚C and subsequent annealing temperature of 1400 ˚C are achievable by the facility available for this project.
- Initial dislocation free single crystalline silicon can be uniaxially compressed along the low index [001] crystallographic direction by more than 30 % at temperatures above 1050 ˚C at low strain rates in the order of 10^{-5} s^{-1}.
- Relatively uniform deformed sample without appreciable cracks was achieved at deformation temperature of 1150 ˚C and a strain rate of 1.67 x 10^{-5} s^{-1}. The total stress applied was 40.0 MPa and the corresponding strain induced was 30 %.
- Uniaxial compression at elevated temperatures produce characteristic deformation microstructure in the appearance of profound cellular patterns formed by intersecting straight sub-grain boundaries. These sub-grain boundaries are inclined at approximately 45˚ to the compression axis.
- 30 % deformation induced a dislocation density of order 10^{13} m^{-2} to the initially dislocation free single crystalline silicon. Heterogeneous microstructure was commonly observed in the as-deformed samples, appearing in sub-grain cell with varying sizes in the range of less than 5 μm to 20 μm and inhomogeneous dislocation density distribution across the sample ranging from 10^{11} m^{-2} to more than 10^{13} m^{-2} order of magnitude, depending on the specified region examined.
- Prolonged annealing at temperatures above 1250 ˚C successfully activated a recovery process which pronouncedly altered the microstructure, featured by the occurrence of polygon walls in the form of straight dislocation etch pits arrays. The recovered microstructure was associated with a considerable reduction of the average dislocation density by approximately two orders of magnitude and enhanced sub-grain cell sizes to more than 70 μm with an estimated dislocation

density of 10^{10} m^{-2}. The recovery process was found complete in 120 min at the temperature of 1400 ˚C.

- TEM bright field imaging revealed a complex defects morphology in the bulk of as-deformed samples. Dense dislocation kinks, tangles, bundles and distinct dislocation networks were commonly observed, together with closely spaced sub-grain boundaries. The sub-grain boundaries are in the form of dislocation arrays of parallel short dislocation segments. The dislocation morphology discrepancy is presumably due to the inhomogeneous plastic deformation throughout the sample.
- Dislocations with ½[$1\bar{1}0$] screw character were observed in both as-deformed and subsequently annealed samples.

4.6.1 Mechanical behaviour of dislocation free single crystalline silicon

The mechanical uniaxial compression behaviour of single crystalline silicon investigated in this study is found to be consistent with the research by Sylwestrowicz [27] which confirmed that dislocation-free single crystalline silicon can be strained up to 30 % at temperatures above 1100 ˚C. In contrast, Mardesich *et al.* [51] observed that during uniaxial compression along the < 001 > orientation, single crystal silicon material cracked at approximately 25 % strain at 1380 ˚C. The reason of this notable difference in fracture behaviour might be ascribed to the marked strain rates variations applied in these deformations, by several orders of magnitudes, numerically the former 3.3 x 10^{-4} s^{-1} and the latter 5.0 s^{-1}. The strain rates utilized in the present study are generally in the order of 10^{-4} s^{-1} to 10^{-5} s^{-1} magnitude, particularly for the compression conducted at 1150 ˚C by 30 % total strain, the average value of strain rate is 1.67 x 10^{-5} s^{-1}, which is comparable to the strain rate adopted in the study of Sylwestrowicz [27]. It

is postulated that the rate of straining has a pronounced effect on the rate of work-hardening [27], which is also verified by Kulkarni *et al.* [50] whose work performed on uniaxial compression of < 001 > oriented p-type single crystalline semiconductor grade silicon at the strain rates from 10^{-5} to 12 s^{-1} at temperatures ranging from 1100 ˚C to 1380 ˚C showed an extended range of no work hardening. The work of Kulkarni *et al.* [50] also provided evidence for recovery during compression process at low strain rate, which counteract the effect of strain hardening induced by accumulated internal stress. This might also contribute to the 30 % strain achieved at the relatively low temperature (1150 ˚C) in the present work. It could also deduced that with equivalent strain rates, the extent of plastic deformation increases prior to fracture with raised deformation temperature.

It was also observed in the study of Sylwestrowicz [27] that plastic deformation behaviour exhibits no correlation with the number of initial grown-in dislocations by means of comparing the deformation properties of initial dislocation-free samples and those with dislocation density of order 10^6 m^{-2}. This can be explained by the fact that, even at the very early stage of deformation, the nucleation of new dislocations is so large that the initial number of dislocations is not an important factor. The fact that dislocation-free samples deform plastically indicates that the Frank-Read mechanism is not the only possible source of dislocations. Also, clusters of vacancies may be considered as another source and the presence of impurities such as oxygen are a probable factor in the production of new dislocations. Dislocations slowed by oxygen can pile up against obstacles until at some point they break through. In the present work, as the deformations were conducted under clean environment, impurities such as transition metals might play a negligible role in the process. However, as the starting

material Czochralski single crystalline silicon contains an oxygen amount of 10^{18} atoms·cm^{-3}, it is reasonable to expect that the presence of oxygen, either in solution or in precipitated forms, would exhibit an effect on the dislocation induction during the plastic deformation.

4.6.2 Deformation microstructure

Characteristic deformation microstructure was observed in all deformation tests, primarily in the appearance of regular cellular structure constructed by straight intersecting lines after preferential etching. Further morphology configuration by TEM confirmed that these straight lines are essentially misoriented sub-grain boundaries. It was also noticed that these sub-grain boundaries extend relatively in a straight form into the bulk material by means of TEM examination.

Dislocation etch pit distribution was found generally heterogeneous throughout the sample, varying from cell to cell. In high dislocation density regions, etch pits overlap with each other that distinguish individual pits is unrealistic, where the density was estimated at least in the order of 10^{13} m^{-2} magnitude. On the contrary, some 'clean' cells contain few scattered etch pits across cell interiors, primarily in the vicinity of cell walls, the etch pits density was then estimated as approximately in the magnitude of 10^{11} m^{-2}. It is interesting to note that the dislocation distribution and the deformation cellular structure on the lateral faces of cube samples appeared more uniform than those of flat samples, irrespective of variations in deformation temperature, total strain and average strain rate. The cell size in the cube sample is approximately 5 μm while the size in the flat sample varies in the range from 3 μm to 20 μm. Although the individual sub-grain

cells in the cube sample contain various amount of the dislocation etch pits and the value may vary distinctly in adjacent cells, the dislocation density over any area which includes several cells tends to be constant. Whereas in the flat samples, rows of high dislocation density cells and 'clean' cells along the slip direction were clearly observed. This morphology difference might be attributed to the significant varied sample dimensions specifically the cross-section area, numerically 100 mm^2 in the former and 225 mm^2 in the latter. As a consequence the maximum applied stresses of the former is twice the value of the latter, respectively.

It has been widely observed that dislocation etch pits align along slip planes in diamond structure (both germanium and silicon) upon plastic deformation [24], [25], [28], [32], [34], [35], [37], [48], [218]. However, those structure are normally dislocation arrays formed by congregated individual dislocations but not distinguished slip line patterns, except the microstructure of silicon deformed by creep at 1300 ˚C [48] which resembles the deformed and annealed microstructure observed in the present work. One possible explanation is that almost all the previous work involved only a small amount of plastic deformation indicated by at the most 10 % strain, thereby the accommodated dislocations were not sufficient to construct concrete slip lines, but only dislocation arrays.

4.6.3 Subsequent high temperature annealing

Annealing to reduce dislocation density has long been a practice of metal workers and serves as an inspiration for the high-temperature annealing of multicrystalline silicon wafers [219]. It was suggested by Takeuchi and Argon [220] in their study of steady-state creep of single-phase crystalline matter at high temperature that temperatures

above 1100 ˚C were necessary for effective dislocation annihilation in silicon. Dislocations become significantly mobile at elevated temperatures and are able to move unconstrainedly out of glide planes henceforth dislocation of opposite signs annihilate pairwise. Hartman *et al*. [219] achieved a significant dislocation density reduction of > 95 % by high temperature annealing in commercial string ribbon multicrystalline silicon wafers at 1366 ˚C for 6 hours. Similarly, Xu *et al*. [221]conducted high temperature annealing at 1360 ˚C for 6 hours on as-grown upgraded metallurgical grade multicrystalline silicon wafers and noticed a reduction of dislocation density from 3.5 x 10^{12} m^{-2} to 0.5 x 10^{12} m^{-2}. Plastically deformed silicon does not only undergo a dislocation density reduction performance but a static recovery process upon subsequent high temperature annealing. Polygonization has been generally considered as a sign of recovery and it involves not only dislocation glide but also climb, henceforth a noticeable elevated temperature is required to initiate the process. In the present work, polygonization was widely observed in all annealing microstructure which signified the effective recovery process. It was also noticed that annealing at 1250 ˚C for 120 min was insufficient to facilitate appreciable microstructure alteration however annealing at 1375 ˚C and 1400 ˚C successfully completed static recovery within 120 min. Straight dislocation etch pits arrays in the as-deformed microstructure generally became curved after recovery process as well as an overall dislocation density reduction by two orders of magnitudes and sub-grain size growth by a factor of 5. These observations are in good agreement with previous experimental results. For instance, Patel [37] observed remarkable dislocation density reduction by a factor of 2 or 3 while annealing plastically bent single crystalline silicon sample at 1300 ˚C for 48 hours, in which long and straight polygon boundaries perpendicular to the slip planes appeared as a result of

dislocation rearrangement. In a similar study conducted on plastic compression of germanium [24] it was found that annealing a previously 1.5 % compressed germanium crystal for 16 hours at 900 ˚C decreased dislocation density by a factor of 5 and the straight rows of etch pits that fell along slip lines in as-deformed sample became curved after annealing.

In conclusion, with present accessible facilities of the present project, uniaxial plastic deformation on crystalline silicon was achievable at 1150 ˚C and subsequent annealing at 1400 ˚C. Relatively uniform deformed sample was obtained at deformation temperature of 1150 ˚C and strain rate of $1.67 \times 10^{-5}\ s^{-1}$. The total stress applied was 40.0 MPa and the strain induced correspondingly was 30 %. Subsequent annealing completed the recovery process in 120 min at the temperature of 1400 ˚C. Henceforth the ideal deformation condition was determined to be 1150 ˚C and strain rate in the order of $10^{-5}\ s^{-1}$, whereas subsequent annealing temperature was determined to be 1400 ˚C.

The suitable deformation and annealing condition was then applied to semiconductor grade polycrystalline silicon. The microstructural evolution and defect morphology of polycrystalline silicon after deformation and subsequent high temperature annealing was investigated systematically by SEM, TEM and EBSD. The relevant results are presented in Chapter 5 and Chapter 6.

Chapter 5

Investigation of the microstructure of polycrystalline silicon after deformation and annealing

5.1 Introduction

After determining a suitable deformation condition by conducting compression experiments on single crystalline silicon, a polycrystalline silicon sample was sawn from the bulk starting material and deformed at the same deformation temperature, namely 1150 ˚C. It is the purpose of this chapter and Chapter 6 to describe the microstructural evolution of the polycrystalline sample during pre-annealing (for different lengths of time), after deformation, and during subsequent annealing (for different lengths of time).

In this chapter part of the experiments to investigate the microstructural evolution of polycrystalline silicon during deformation and annealing are reported and discussed. The chapter begins by presenting the microstructural examination of the as-received polycrystalline material and its recrystallization behaviour during high temperature annealing before deformation, mainly by preferential etching and scanning electron microscopy (SEM), electron backscatter diffraction (EBSD), and transmission electron microscopy (TEM). These characterization techniques allow the sample surface microstructure, grain size, crystal orientation, grain boundary type, and crystallographic defect configuration (such as dislocation density and morphology) to be ascertained. The main body of the results summarises the investigation of microstructural evolution during deformation at elevated temperatures and upon subsequent high temperature

annealing. The thermal evolution of the crystalline structure and defects morphology is described and discussed in relation to results published by others [50], [51], [54]–[61], [65], [66], [222]. It will be shown that annealing at temperatures close to the melting point (1414 ˚C for silicon) after deformation by 10 % for a relatively short period of time results in significant recrystallization. The resultant recrystallized microstructure consists of large grains up to several hundred microns with low concentration of crystallographic defects (dislocation density of approximately 10^{10} m^{-2}), comparable to standard, commercially available multicrystalline silicon wafers and silicon sheets produced by the ribbon growth technique. Detailed crystallographic information of microstructures and geometrically necessary dislocation (GND) density at each thermal processing stage was also investigated by the high resolution electron backscattered diffraction (HR-EBSD) cross-correlation method, and these results will be presented separately in Chapter 6.

5.2 Investigation of the as-received polycrystalline silicon microstructures

The starting material used in this study is electronic grade, high purity polycrystalline silicon produced by the standard commercial Siemens process [186]. The material was manufactured and provided by SunEdison. The production process involves the decomposition of tricholorosilane at 1100 ˚C or with silane at 800 ˚C with hydrogen on silicon surfaces [223]. The reaction formulas are shown below:

$$3SiHCl_3 + H_2 \xrightarrow{yields} 2Si + 5HCl + SiCl_4 \qquad \text{Equation 5-1}$$

$$SiH_4 + H_2 \xrightarrow{yields} Si + 3H_2$$ Equation 5-2

In this process, polycrystalline silicon is chemical vapour deposited on hot single crystalline silicon, slim, rods in the bell bar shaped so-called Siemens reactor. The schematic is illustrated below in Figure 5.1.

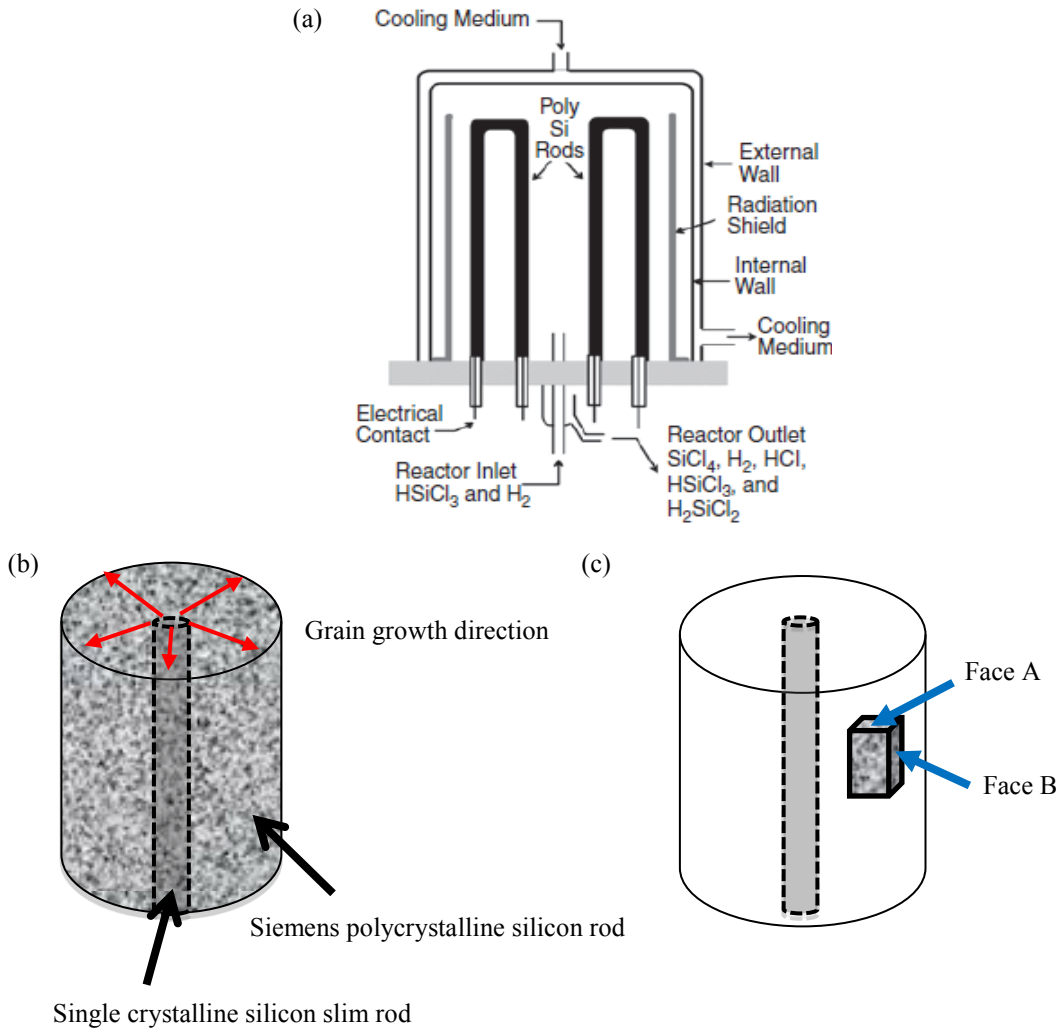


Figure 5.1. Schematic diagrams: (a) Traditional Siemens reactor [14]; (b) Siemens polycrystalline silicon rod, red arrows mark the grain growth direction; (c) How Face A and Face B were defined in this study, pointed by blue arrows.

The grain growth direction of polycrystalline silicon is radially outwards from the central single crystal rod, as depicted in Figure 5.1 (a) by red arrows. Samples used in this study were cut by ceramic sawing into dimensions of 20 mm x 20 mm x 10 mm (see Chapter 2). The microstructures of the two most representative sample surfaces were chosen to be examined, referred as Face A and Face B respectively, as illustrated by the blue arrows in Figure 5.1 (b). Face A represents the surface perpendicular to the long axis of the "polylog" but parallel to the grain growth direction, whereas Face B represents the surface parallel to the long axis of the "polylog" but perpendicular to the grain growth direction. The microstructure investigation of these two surfaces will be discussed in the following sections.

5.2.1 Microstructure revealed by preferential etching and SEM

The microstructures of Face A and Face B were examined after standard metallographic preparation followed by etching for 30 s in a Sirtl etch solution (see Section 2.5.2 for details). The SEM image of Face A illustrates a clearly visible coarse tree-stem-like texture elongated in the radial grain growth direction, as shown in Figure 5.2 (a) with the main tree stem marked by the blue arrow. The various grains in a cluster are separated by straight grain boundaries. Furthermore, the growth direction seems to change for a number of times during the deposition procedure. Upon further growth new nuclei are formed at discrete locations and growth continues in this tree-like structure. In general, the structure of the as-received material is non-uniform. While viewed perpendicular to the growth direction of the polycrystals the preferential etch reveals few large grains of up to 40 μm in diameter with low etch pit densities (approximately at the magnitude of 10^{11} m^{-2}) on a rough background, marked by blue arrows in Figure 5.2 (b). These large grains correspond with the main tree stems in the

grain growth direction. The radial lines in the lightly etched grains indicate the growth direction of the crystals and their common origins locate at the nucleation points. These large grains are believed to be the primary stems of the tree-like structure. Most of the material comprises much smaller grains for which SEM micrographs fail to reveal more details (marked by red arrows in Figure 5.2b). The crystallographic information was further verified by EBSD. The microstructures of as-received polycrystalline silicon material are in good agreement with earlier results for this kind of material in the literature [58].

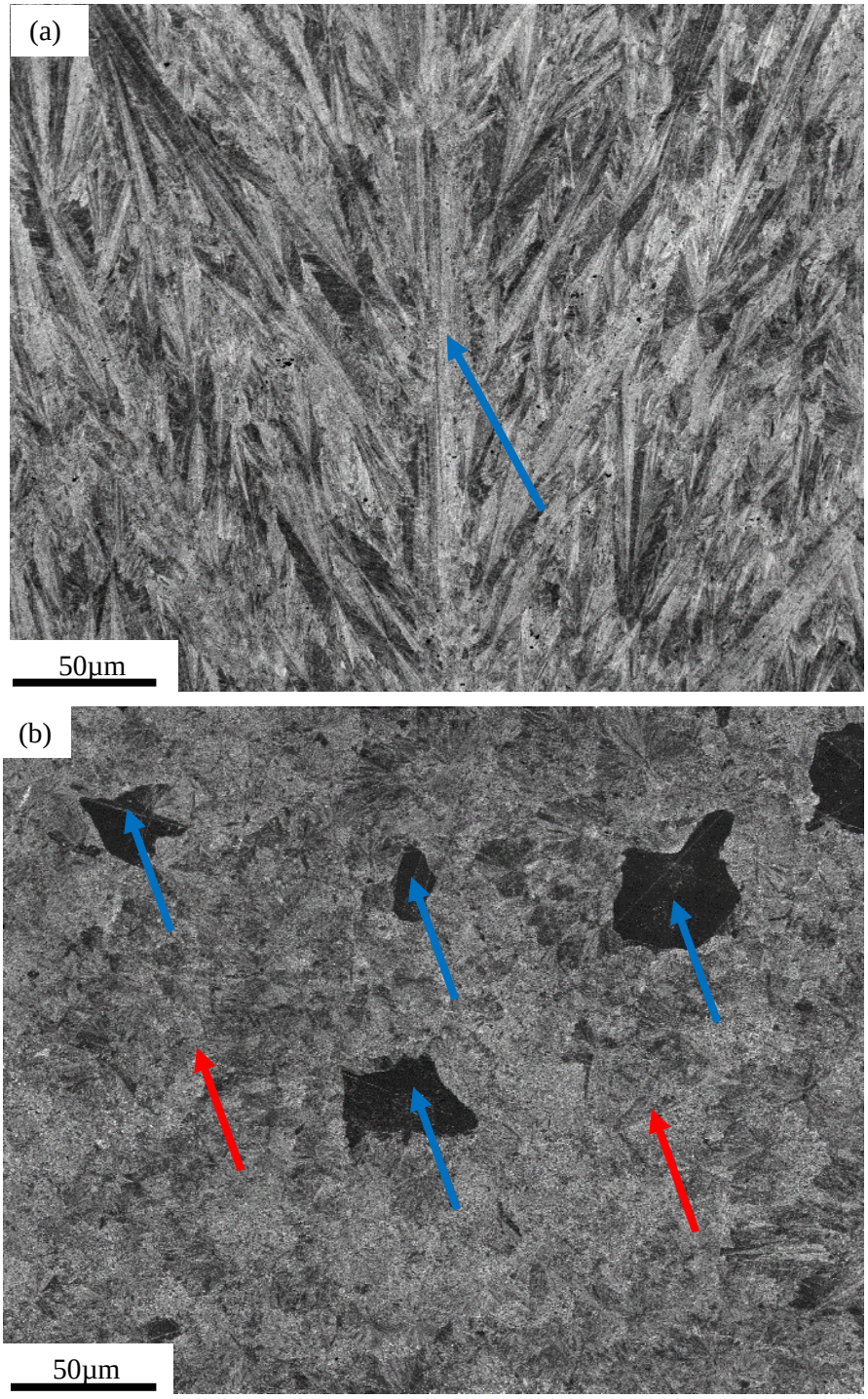


Figure 5.2 SEM micrographs of etched surfaces: (a) Face A with a higher magnification micrograph showing the closed packed dislocation etch pits; (b) Face B. The grain growth direction is vertical in (a) and outwards in (b). Blue arrow mark the locations of crystal 'tree stems'. Red arrows mark small grains.

Despite the fact that preferential etch is generally capable of revealing the crystallographic defects, it is impractical to estimate the dislocation density by conventional etch pit counting on this specific as-received polycrystalline silicon material. A higher magnification SEM micrograph of Face A gives the impression that etch pits are extremely close packed, as depicted in Figure 5.3. It was therefore proven nearly impossible to distinguish them apart. Thus dislocation density measurement by etch pit counting was not possible. Therefore the geometrically necessary dislocation (GND) density of as-received material was evaluated by means of cross-correlation based high resolution EBSD (HR-EBSD) analysis, which is the subject of Chapter 6.

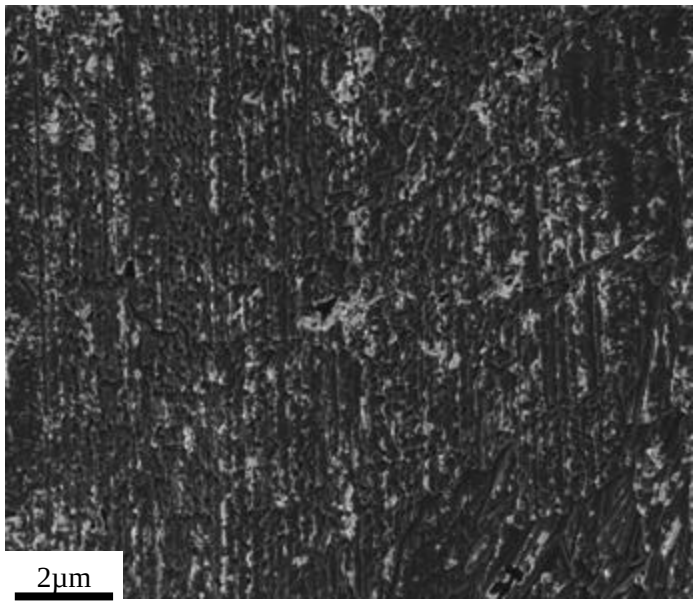


Figure 5.3. Higher magnification SEM micrograph of etched surface from Face A reveals a microstructure of extremely close-packed etch pits. The vertical lines are genuine etched structure rather than polishing scratches.

5.2.2 Crystallographic information from EBSD

In order to gain insight into the crystallographic configuration of the as-received material, EBSD was employed to gather information on microstructural properties from

various aspects such as grain size, grain boundary characteristics and local grain orientation distributions, as well as integral crystal textures.

Samples of the radial section (Face A) and axial section (Face B) of as-received material were sliced from the bulk into small pieces by traditional mechanical sawing. The samples were firstly polished by 6μm and 1 μm diamond paste, then with 50nm colloidal silica slurry to a mirror finish. Finally plasma cleaning was utilized to produce an ultra-clean sample surface. During this process Nitrogen atoms are ionized and interact with organic contaminants residing on the sample surface.

EBSD maps with the size of 100μm x 100μm were captured from typical areas on Face A and Face B (as shown in Figure 5.4 and Figure 5.5, respectively) using OIM DC v5.3 (TSL-EDAX) EBSD system in a JEOL 840A with accelerating voltage of 20 kV and ~ 30 nA probe current. The space between neighbouring points was 0.5 μm and at each point an EBSD pattern was recorded.

As regards to EBSD maps, pattern quality maps give direct account on the quality of specimen preparation as well as on positions of grain boundaries, while orientation distribution maps represent the local orientation of each grain (with respect to a reference coordinate system). EBSD maps (Figure 5.4a and 5.4b) of Face A (viewing along the grain growth direction) reveal a microstructure with inhomogeneous grain sizes varying from 3 ~ 30 μm in length and 1 ~ 3 μm in diameter. It is evident that all the small grains nucleated at certain sites during grain growth and grew outwards radially resulting in large twin grains which impinge with each other (marked by blue arrows in Figure 5.4a). The large twin grains are generally elongated in the grain growth direction in various sizes. From the orientations of two neighbouring grains (*i.e.* the

corresponding point lattices), their misorientation can be calculated. The related symmetry of a grain boundary can be expressed by the sigma notation (Σ), which denotes the reciprocal density of coincidence sites [224] between two adjacent lattices. Σ 3 and Σ 9 grain boundaries were both observed in the big twin grains distributing in a regular lamellar form (Figure 5.4c, with Σ 3 grain boundaries highlighted by black lines and Σ 9 grain boundaries highlighted by red lines). The inverse pole figure (Figure 5.4d) reveals no preferential texture along the crystal growth direction.

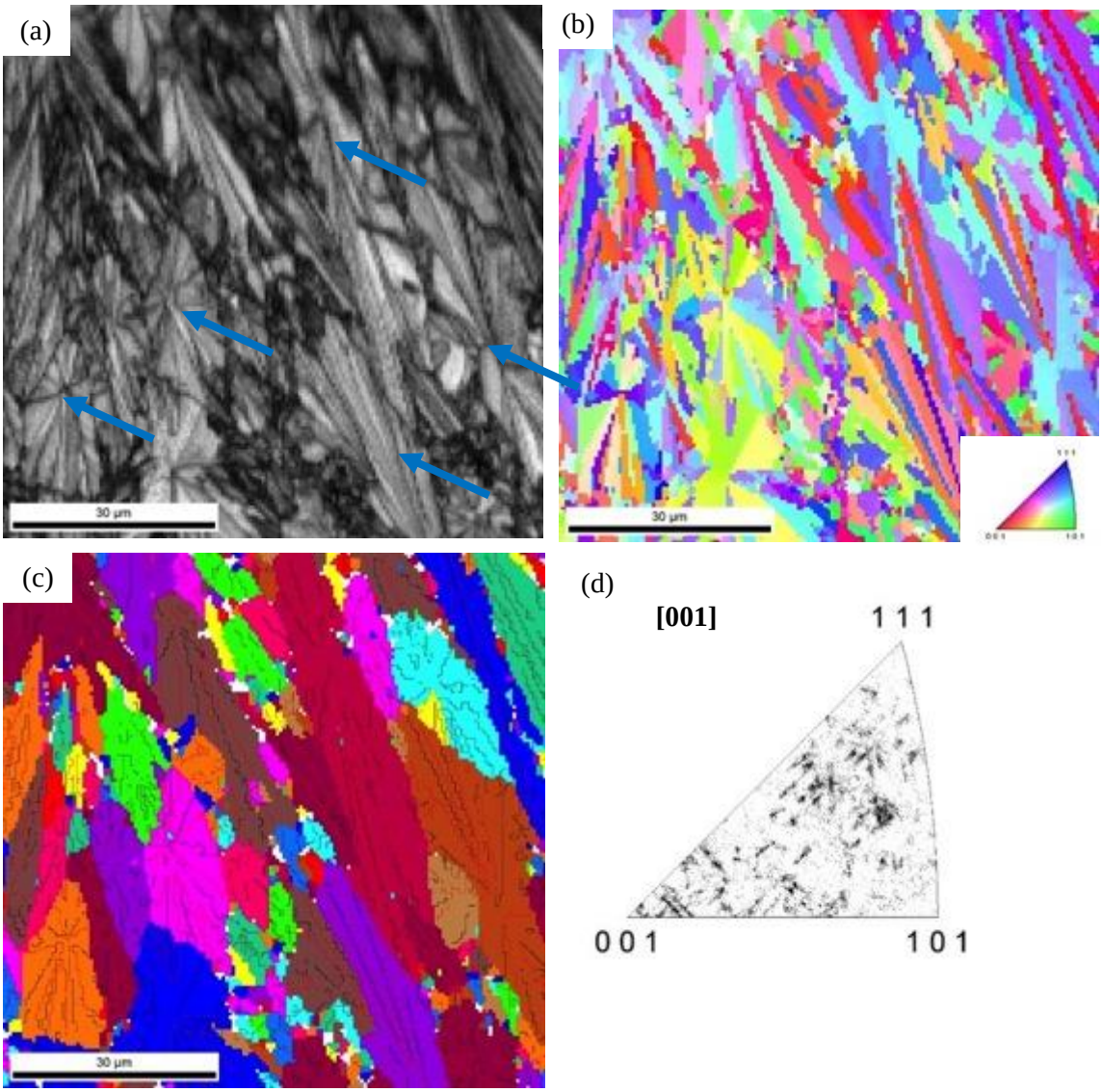


Figure 5.4 EBSD maps of Face A: (a) Pattern quality map, large twin grains are marked by blue arrows; (b) Grain orientation distribution map; (c) Grain map with Σ 3 and Σ 9 grain boundaries highlighted by black lines and red lines, respectively; (d) Inverse pole figure. Grain growth direction is vertical in these maps.

EBSD maps on Face B reveal a different microstructure from Face A, as it was viewed perpendicular to the grain growth direction. The pattern quality map (Figure 5.5a) shows that grains nucleated at discrete sites across the sample and nuclei grew outwards radially into large circular grains to form the primary matrix, with various sizes ranging from 5 µm to 30 µm (marked by blue arrows in Figure 5.5a). A large fraction of these large grains grow out along < 110 > directions according to the grain orientation map

(Figure 5.5b). Between these relatively large twin grains, the microstructure comprises small grains with more random orientations (marked by red arrows in Figure 5.5a), with an average grain size 1μm or smaller, presumably due to the fast deposition process which resulted in no further grain growth in these areas. Grain boundary characterization confirms that the twin grain boundaries within each big grain are Σ 3 and Σ 9 type (Figure 5.5c), similar to those in Face A. The inverse pole figure also verifies a sharp < 110 > fibre texture coinciding with the growth direction (Figure 5.5d).

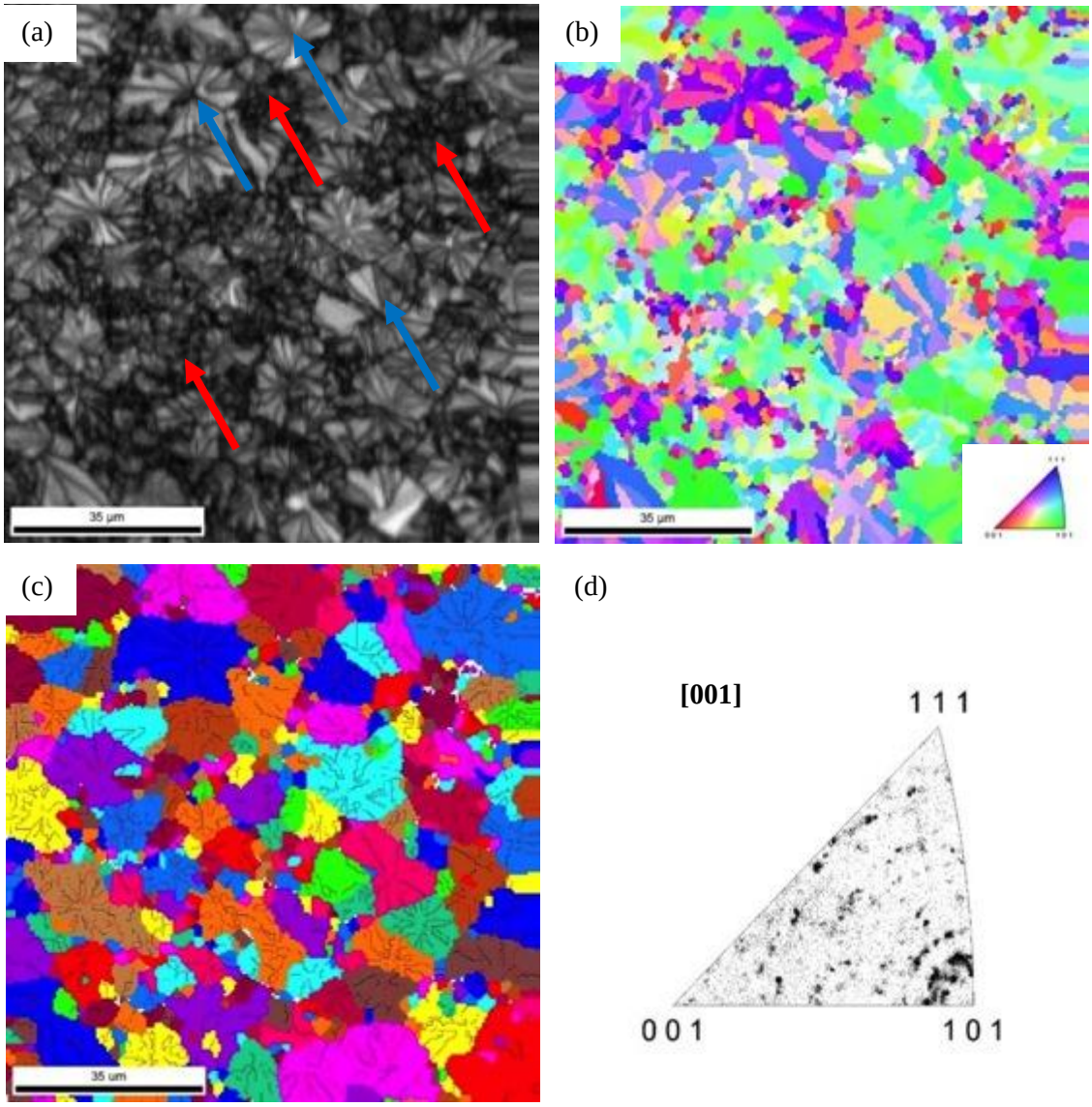


Figure 5.5. EBSD maps of Face B: (a) Pattern quality map, blue arrows mark large twin grains and red arrows mark small twin grains; (b) Grain orientation distribution map; (c) Grain map with Σ3 and Σ9 grain boundaries highlighted by red lines and black lines, respectively; (d) Inverse pole figure. Grain growth direction is outwards.

5.2.3 Defect morphology investigated by TEM

While preferential etching and SEM provide surface microstructure information and EBSD has proven effective in determining the crystallographic textures of the near-surface region, TEM was used to investigate the detailed defect morphology and obtain straightforward microstructural information on the bulk material. TEM specimens were generally prepared by FIB lift-out technique in this work. A specimen was cut from the centre region of a big twin grain on Face A. The foil surface is perpendicular to the grain growth direction. TEM bright field micrographs show a radial structure fanning out from the centre point, see Figure 5.6. The material also appears highly defective with straight twin grain boundaries.

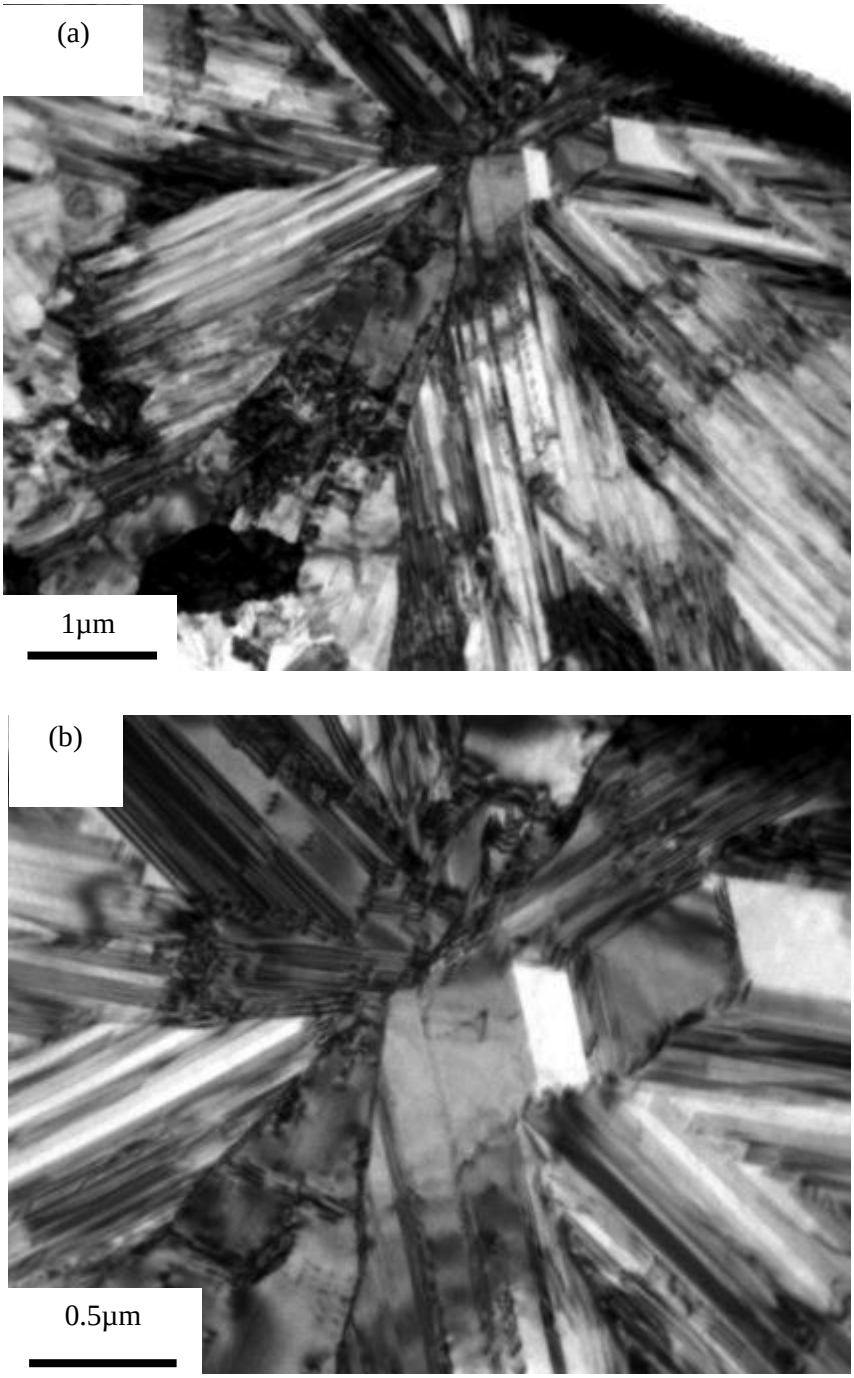


Figure 5.6. TEM micrographs of as-received material: (a) General view of the microstructure; (b) Centre area in higher magnification.

5.3 Pre-deformation annealing of the as-received materials

As the as-received material is so highly defected and potentially too brittle to be compressed directly, a series of experiments were assigned to investigate the microstructural evolution upon high temperature pre-annealing at 1400 ˚C for various time durations. This was to first of all verify the necessity of this procedure, and secondly, if possible, to determine the optimal pre-deformation annealing conditions. A set of samples were cut parallel to Face A and Face B and underwent annealing at 1400 ˚C for various lengths of time. All samples were sealed in evacuated quartz ampules to avoid oxidation (see Chapter 2 Section 2.4). After thermal annealing, samples were cooled down slowly in the furnace to room temperature (see Chapter 2 Section 2.4) and were prepared by standard polishing procedure followed by Sirtl etch for 30s before examination by SEM.

5.3.1 Microstructures of pre-annealed samples revealed by SEM

The samples with surfaces parallel to Face A were annealed for 30 min, 60 min, 90 min and 120 min at 1400 ˚C, separately. The SEM micrographs of typical areas in each sample are shown in Figure 5.7.

Annealing at 1400 ˚C for 30min significantly changed the microstructure of the as-received material, yielding a relatively homogeneous recrystallized matrix with average grains of 30 μm in diameter. 90 % of the as-received material recrystallized during the annealing process, whereas the tree-stem-like coarse-grained regions kept their geometrical shape, *i.e.* elongating in the original growth direction (marked by blue arrows in Figure 5.7a). However, prolonged annealing at 1400 ˚C did not seem to

improve the recrystallization to a further extent. The average grain size did not increase pronouncedly along with increasing annealing time, indicating that after initial recrystallization the grain structure was not strongly affected by further annealing. The coarse tree-stem-like regions and un-recrystallized left from the as-received material with extremely high dislocation content were present even after two hours isothermal treatment (marked by red arrows in Figure 5.7d).

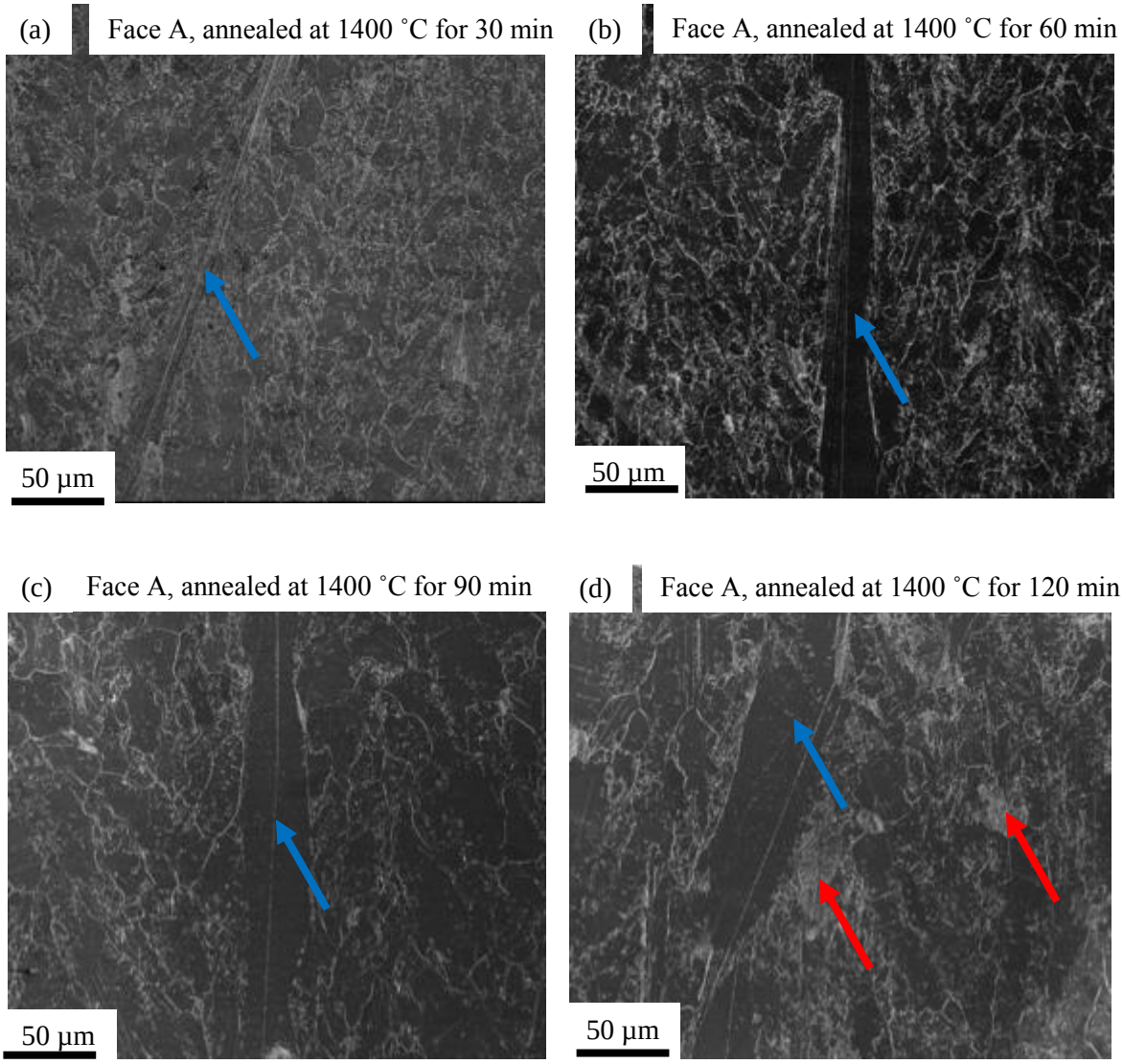


Figure 5.7. SEM micrographs of etched surface (Face A, original grain growth direction is vertical) of as-received materials after annealing at 1400 ˚C for (a) 30 min; (b) 60 min; (c) 90 min and (d) 120 min. Large twins are marked by blue arrows. Red arrows in (d) mark the high dislocation density un-recrystallized regions.

Examination of the microstructure using higher magnification SEM provides detailed information on grain size, grain boundary structure and dislocation etch pit distribution. It was observed that apart from the large tree-stem-like grains, the rest of the recrystallized microstructure after 30 min annealing at 1400 ˚C consists of newly nucleated and grown grains and a portion of un-recrystallized left from the as-received matrix, as marked by blue arrows and the red arrow in Figure 5.8(a), respectively. The

newly recrystallized grains have rather irregular shape and curved grain boundaries. Dislocation etch pits in these recrystallized grains have a density of at least 3 to 4 orders of magnitude lower than the un-recrystallized regions. However, the etch pit distribution, even within these recrystallized grains, appears rather inhomogeneous. Some relatively larger grains contain much fewer dislocations, especially at the centre region of the grain interior, than smaller grains. Stacking faults were found commonly present in most grains across the sample (marked by red circles in Figure 5.8). Annealing for an extended length of time (up to 120 min) at 1400 ˚C did not exert much influence on grain boundary morphology or defect density (as shown in Figure 5.8b).

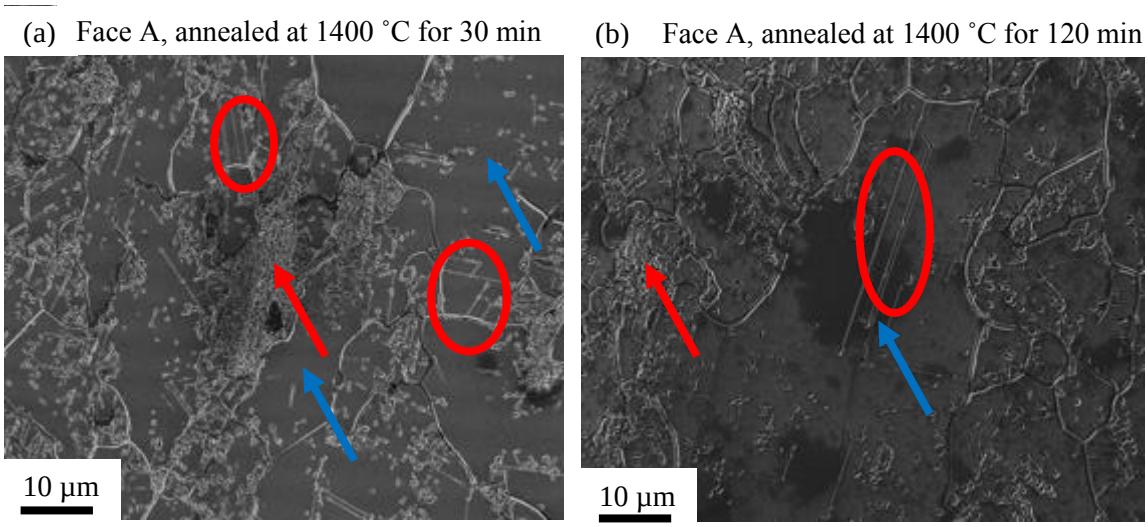


Figure 5.8 Higher magnification SEM micrographs of etched surface (Face A, original grain growth direction is vertical) of as-received materials after annealing at 1400 ˚C for (a) 30min and (b) 120min. Red arrows mark the high dislocation density un-recrystallized regions and blue arrows mark the recrystallized regions. Stacking faults are enclosed by red circles.

Although the microstructure research primarily focuses on Face A, a few samples from Face B were also cut and annealed under the same thermal conditions and subjected to the same preparation for SEM imaging. The representative regions in these samples

were imaged and are shown below. Figure 5.9 depicts the representative microstructures of as-received materials (Face B) annealed at 1400 ˚C for 30 min, together with micrographs from area of interests in higher magnification. It is clear that 30 min annealing drastically altered the microstructure of the as-received material as a result of recrystallization, which is in good agreement with the microstructure change observed in Face A. However, the recrystallized grains in Face B appear significantly more homogeneous than those in Face A, featuring almost equiaxed grain shape. The average recrystallized grain size is 30 μm in diameter, with a range between 3 μm and 40 μm. There is no apparent 'gigantic' long stem-like grain existing in this section, presumably due to the relatively more uniform structure of as-received material in this cross-section. 90 % of the material has recrystallized after 30 min annealing. While recrystallized grains with lower dislocation densities (approximately 2 x 10^{11} m^{-2}) impinge on each other, some new grains have nucleated from the grain boundaries of the recrystallized grains. Further annealing for another 30 min does not profoundly change the microstructure, apart from a slight grain growth.

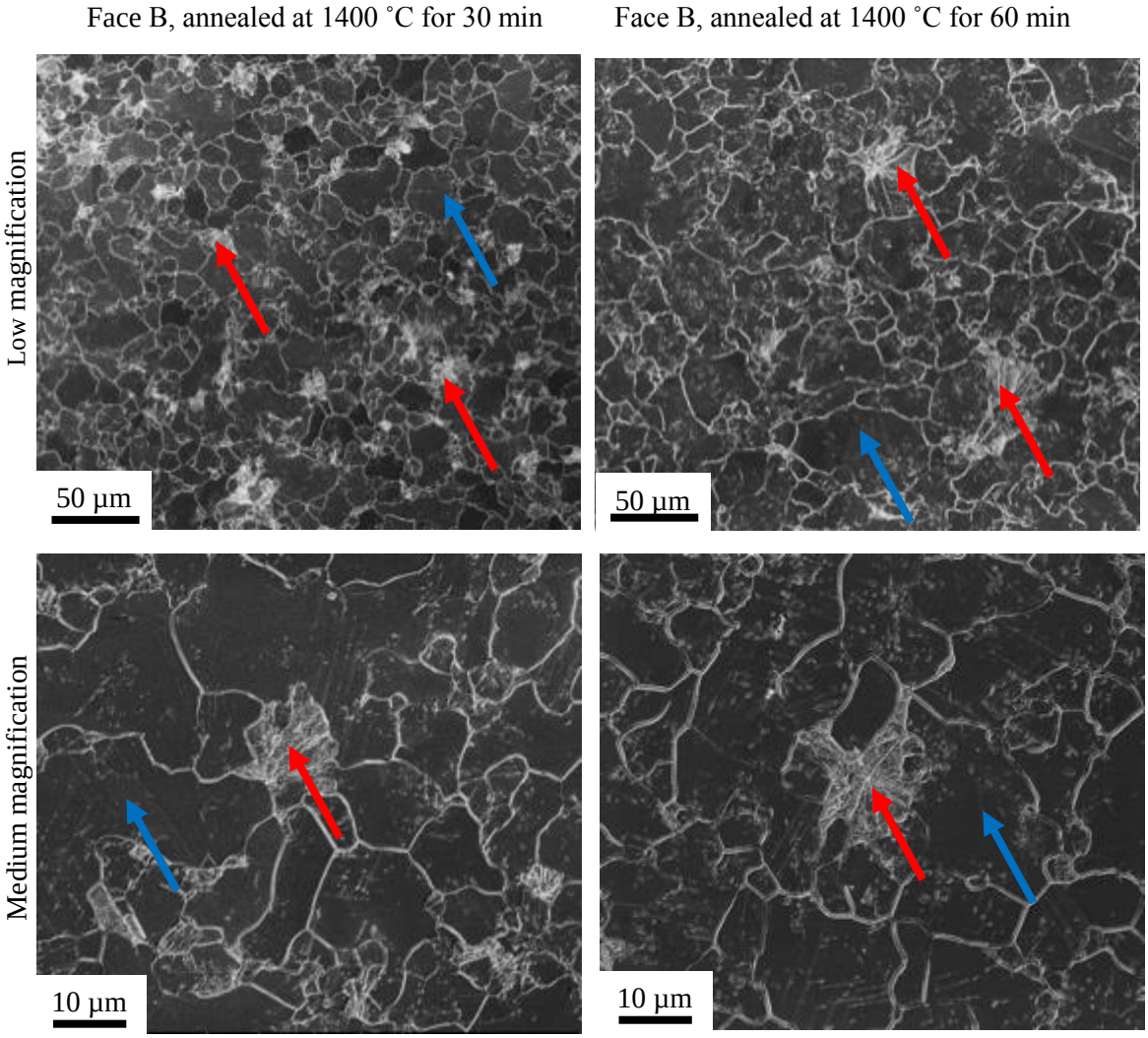


Figure 5.9. Representative SEM micrographs of etched surface (Face B, original grain growth direction is outwards) of as-received materials after annealing at 1400 ˚C for 30 min and 60 min, with specific areas at a higher magnification. Red arrows mark the un-recrystallized regions and blue arrows mark the recrystallized regions.

5.3.2 Crystallographic information of pre-annealed samples examined by EBSD

EBSD was used to characterize the texture change of the as-received material during the annealing process. The orientation distribution maps of Face A after annealing at 1400 ˚C for 30 min, 60 min and 90 min are shown in Figure 5.10 (b), (c) and (d), with the orientation map of Face A in the as-received state as reference (Figure 5.10a). The twin grain boundaries of Σ 3 and Σ 9 types are highlighted with black and red lines, respectively. It is evident that the as-received material has a highly twinned grain structure. Each large twin grain consists of small twins growing outwards from the centre point, with Σ 3 and Σ 9 grain boundaries separating each other. High angle grain boundaries exist between these big twin grains. The annealed sample has a completely different crystalline morphology, apart from a much larger grain size. Σ 9 grain boundaries completely disappear in recrystallized regions, while a small number of straight Σ 3 grain boundaries appear across some grains, presumably as annealing twins. In Figure 5.10 (d) a specific area was presented, which contains a part of a large stem-like grain (marked by the black arrow). EBSD crystal orientation map confirms that long straight grain boundaries in these large grains have Σ 3 character, constructing a highly symmetric twinning structure which does not disappear even after high temperature annealing for a long time.

The orientation maps of Face B in the as-received state, and after annealing at 1400 ˚C for 30 min and 60 min are presented in Figure 5.11 (a), (b) and (c), respectively. The initial as-received material is highly textured along the grain growth direction, whereas annealing and recrystallization completely changed the textured structure into a random

crystallographic orientation distribution. Similar to Face A, the recrystallized grains contain only Σ 3 grain boundaries from annealing twins.

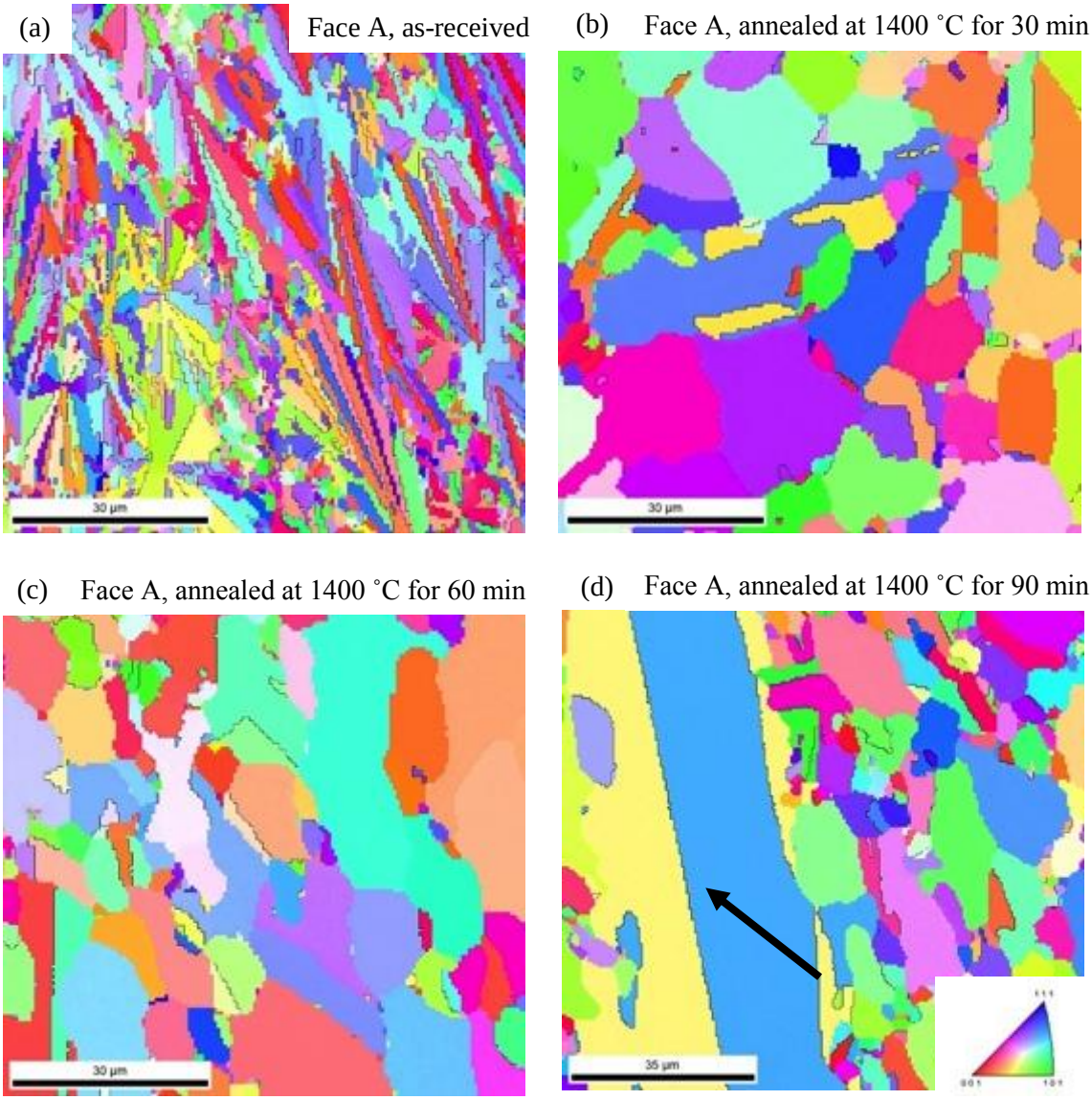


Figure 5.10. EBSD orientation maps of Face A: (a) As-received state; (b) Annealed at 1400 ˚C for 30 min; (c) Annealed at 1400 ˚C for 60 min; (d) Annealed at 1400 ˚C for 90 min, the black arrow marks the large stem-like grain. Red lines highlight Σ3 twin grain boundaries and black lines highlight Σ9 twin grain boundaries. The orientation colour map applied to all the sub-figures.

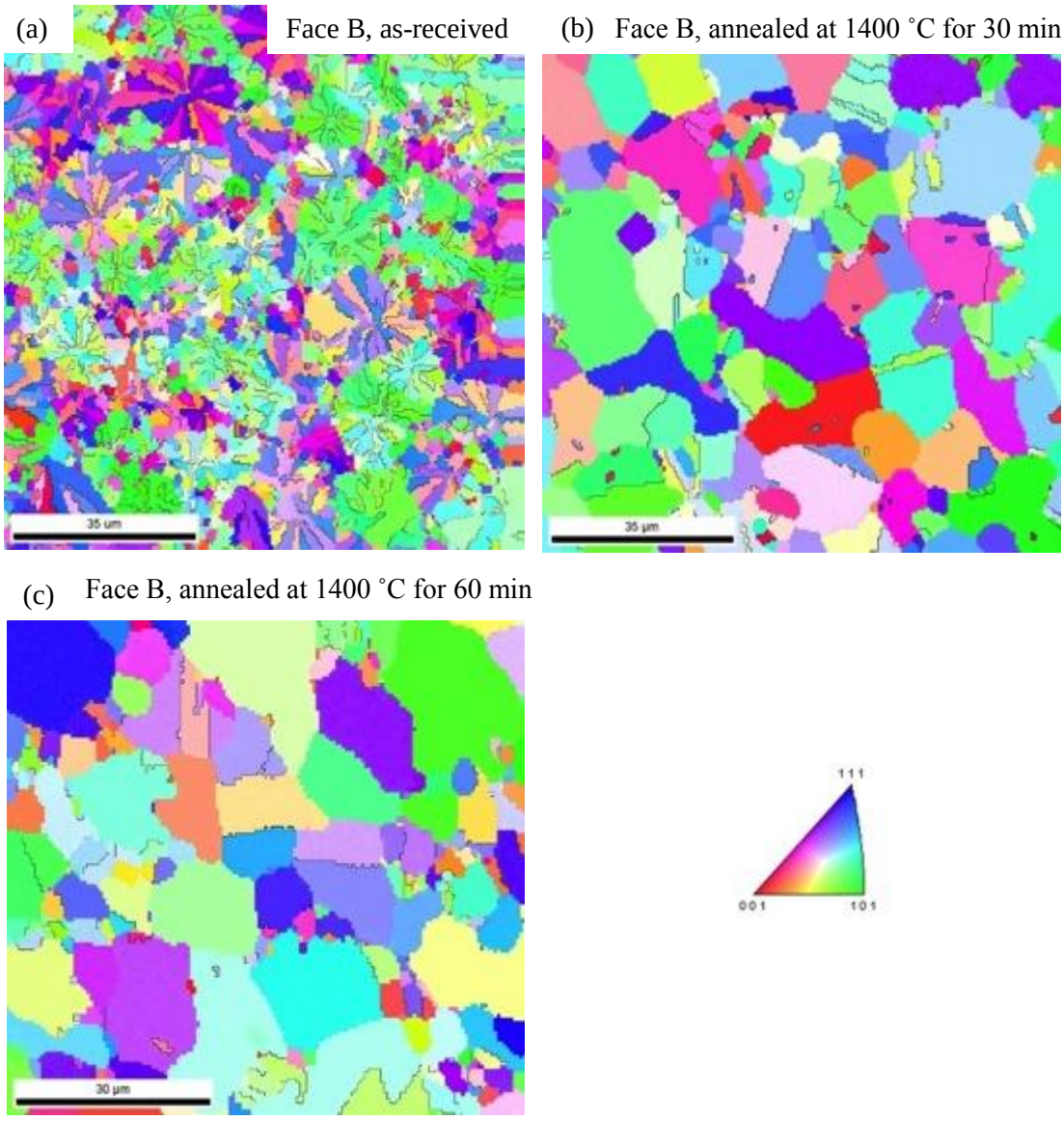


Figure 5.11. EBSD orientation maps of Face B: (a) As-received state; (b) Annealed at 1400 ˚C for 30 min; (c) Annealed at 1400 ˚C for 60 min. Red lines highlight Σ3 twin grain boundaries and black lines highlight Σ9 twin grain boundaries. The orientation colour map applied to all the sub-figures.

Preferential etching and EBSD reveal that the as-received material notably recrystallized after annealing at 1400 ˚C for 30 min in both cross-sections parallel and perpendicular to the grain growth direction. However, prolonged annealing has no noticeable effect regarding further altering the recrystallized microstructure. Therefore, an optimal pre-deformation annealing condition of 1400 ˚C for 30min was determined

to be satisfactory. This anneal was readily performed and no experiments were undertaken with shorter annealing time. Defect morphology characterization was performed using TEM on samples annealed for 30 min and 60 min, which will be described in the next sub-section.

5.3.3 Defect morphology investigated by TEM

In order that all defects in the bulk could be observed, cross-sectional TEM specimens were produced by a FIB lift-out technique from specific sites of interest on pre-annealed samples. Since the microstructure of both cross-sections did not appear to change remarkably after the initial recrystallization, samples from Face A annealed at 1400 ˚C for 30 min and 60 min, together with sample from Face B annealed at 1400 ˚C for 30 min were selected for bulk defect morphological investigation. The detailed TEM micrographs of each sample are presented and discussed in this section.

5.3.3.1 Defects in Face A annealed at 1400 ˚C for 30 min by TEM

Two representative types of regions were specifically chosen for TEM investigation: the un-recrystallized area with extremely high dislocation density (presumably un-recrystallized left from the as-received state); and the grain boundary area of the recrystallized grains with low dislocation density.

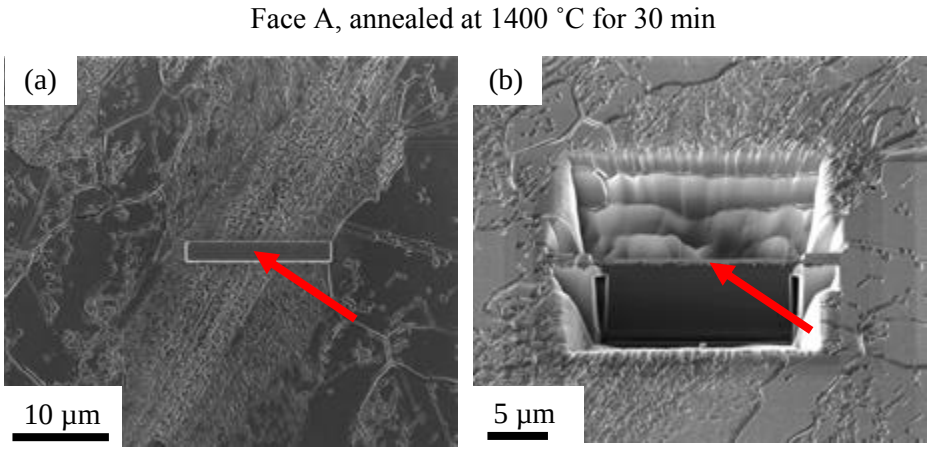


Figure 5.12. SEM image of TEM specimen preparation from a high dislocation density region in Face A, annealed at 1400 ˚C for 30 min (the surface is etched): (a) Plan view of the specimen post platinum deposition, the platinum layer is marked by the red arrow; (b) Side view of the specimen post final polishing, the relatively bright part is the platinum layer, marked by the red arrow.

Figure 5.12 shows the SEM images during specimen preparation by FIB from the un-recrystallized region. The deposited platinum layer indicates the specimen location and the roughness of the etched surface can be clearly seen from the side view of the specimen.

Figure 5.13 provides the low magnification overview of the specimen under TEM bright field condition. The platinum layer appears as a black stripe at the bottom left of the micrograph. It is evident that the specimen contains a significantly large number of crystallographic defects, predominantly condensed stacking faults and dislocation arrays, mainly in un-recrystallized grains, such as grain A and grain B (both taken near the [001] zone axis in this micrograph). Apart from the abundant un-recrystallized grains, there are present a few small recrystallized grains containing low defects content with the

average diameter of 2 μm, as pointed out by blue arrows in Figure 5.13. The whole specimen appears highly defective and the detailed crystallographic configuration of some representative defects in this specimen is shown in the following part of this section.

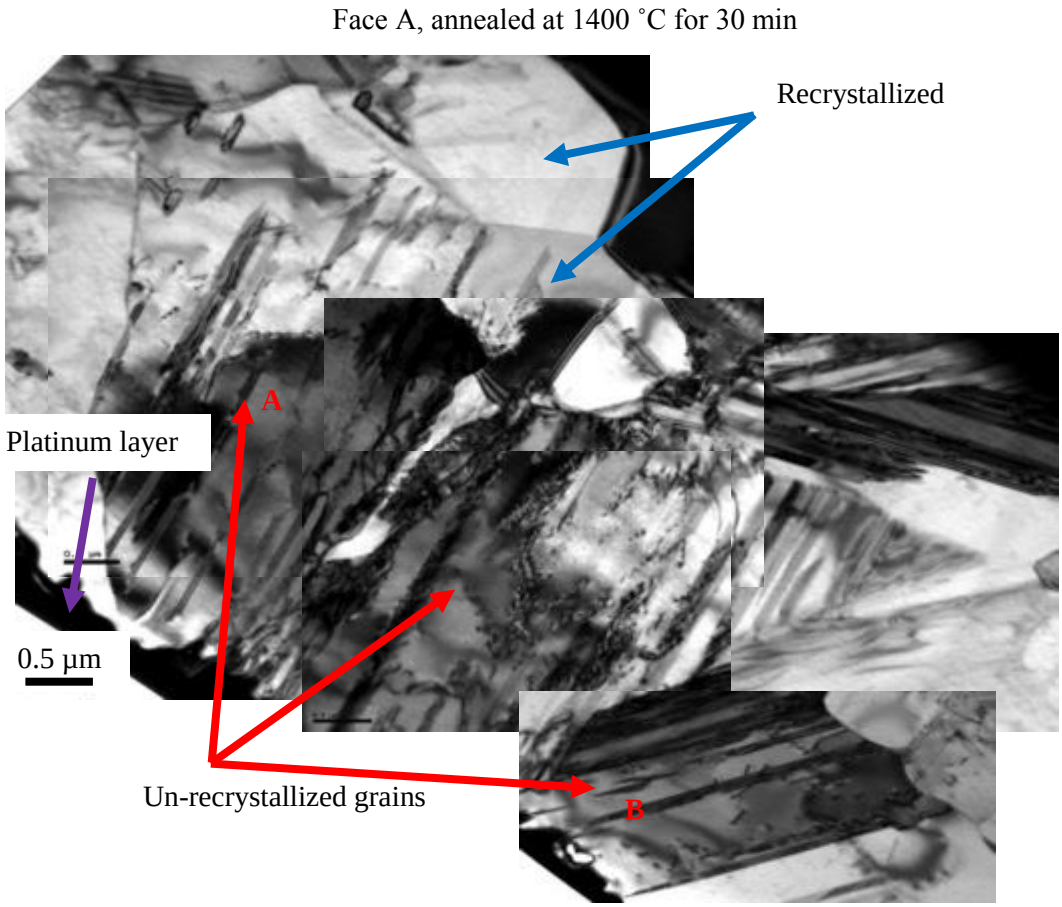


Figure 5.13. TEM bright field micrographs of the specimen overview (Face A, annealed at 1400 ˚C for 30 min), the dark stripe at bottom left is the platinum layer, marked by the purple arrow. Red arrows mark un-recrystallized grains and blue arrows mark recrystallized grains.

Representative high magnification TEM bright field micrographs of severely defective regions were taken near the [111] zone axis and presented in Figure 5.14, with the relevant crystallographic orientations denoted. The crystallographic orientations were

worked out from the corresponding diffraction patterns recorded together with the images, with image rotation corrected. It is unambiguous that, as viewed in the [111] beam direction, nearly all the stacking faults lie in $< 1\bar{1}0 >$ directions in the specimen (in all four images), while short straight dislocation segments inclined to the surface form different types of arrays with their ends lining up primarily in <211> directions. In Figure 5.14 (a), all the short dislocations lie in the $[\ \bar{2}11\ ]$ direction and the space between individual dislocation is approximately 300 nm in average. In Figure 5.14 (b), the dislocation array comprises five short segments. The projected dislocation line axis is approximately along the $[\ \bar{1}01\ ]$ orientation with a slight deviation between individual dislocations, whereas the dislocation array is nearly parallel to the $[\ \bar{1}\bar{1}2\ ]$ direction. The space in between individual dislocation in the array varies from 100 nm to 300 nm. In Figure 5.14 (c) another dislocation array with a different characteristic is shown. The short dislocation segments are notably close packed along the array direction, with the space between individual dislocations approximately 50 nm. The projected dislocation lines are in the $[\ \bar{2}11\ ]$ orientation, while the array is along the $[\ \bar{1}01\ ]$ direction. As marked by the red line in Figure 5.14 (d), this dislocation array consists of segments lying in the direction of $[\ \bar{2}11\ ]$, and the array stretch along the $[\ \bar{1}\bar{1}2\ ]$ direction. The short dislocation segments are separated by approximately 100 nm.

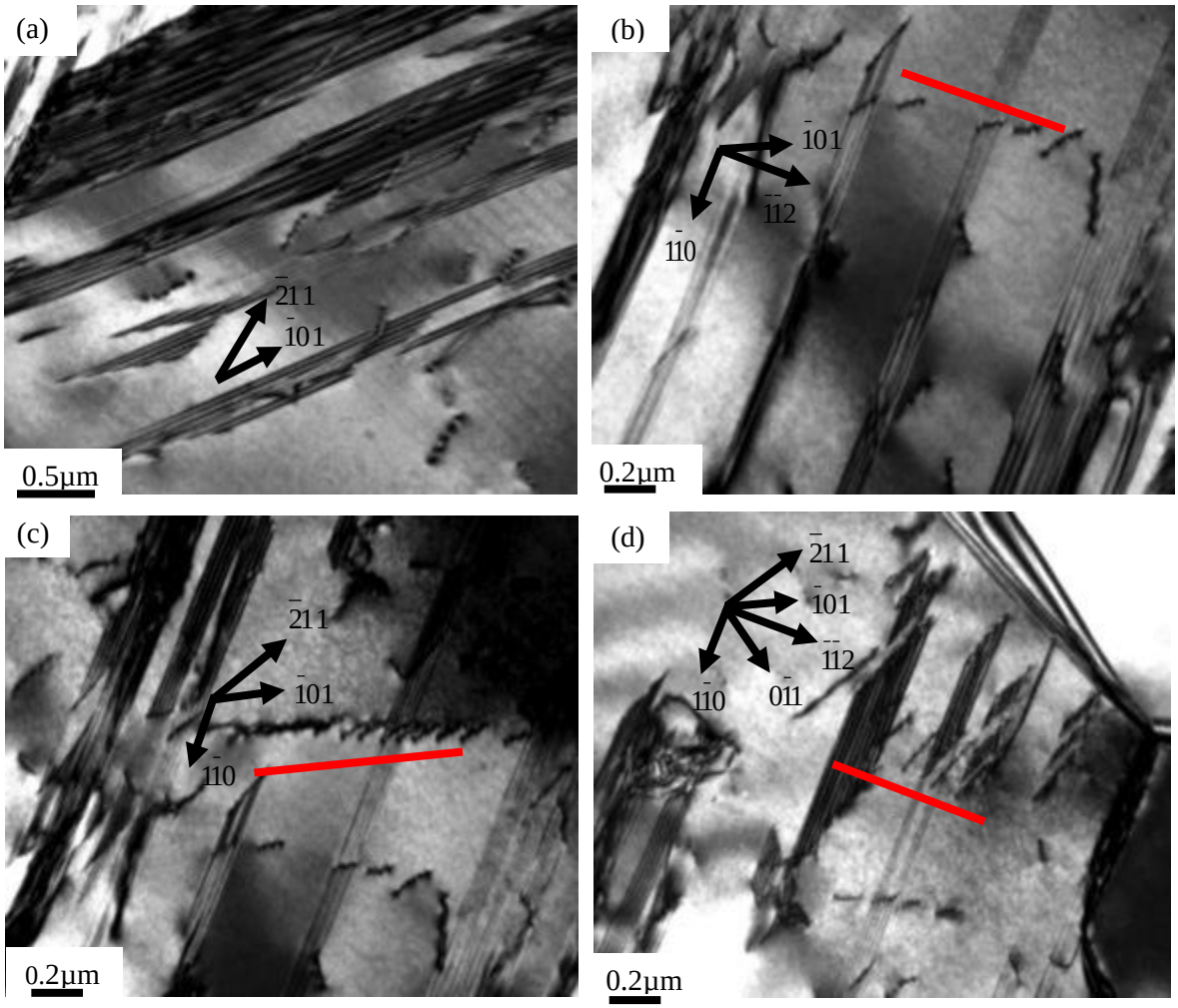


Figure 5.14. High magnification (111) pole bright field images of representative areas with high defect concentration from Face A, annealed at 1400 ˚C for 30 min. Red lines mark the direction of dislocation arrays.

The area containing dislocation arrays in Figure 5.14 (c) was analysed in two-beam diffraction conditions to characterize the stacking faults and dislocations. Bright field and dark field micrographs under different diffraction conditions are shown below in Figure 5.15, with diffraction vectors marked in individual micrograph. It is evident that most stacking faults give rise to strong contrast under diffraction vector [$\bar{2}02$] (Figure 5.15c) and out of contrast under diffraction vector [$\bar{2}20$] (Figure 5.15e). However, using ($02\bar{2}$) reflection (as in Figure 5.15a), some stacking faults are out of contrast (as marked by A) and some are in moderate contrast (marked by B). Due to the fact that the

foil surface was too close to the (111) pole, tilting to another low index pole was very difficult therefore detailed analysis was not possible. However, the character of the observed stacking faults is consistent with that in silicon, of 1/3 < 111 > type [106].

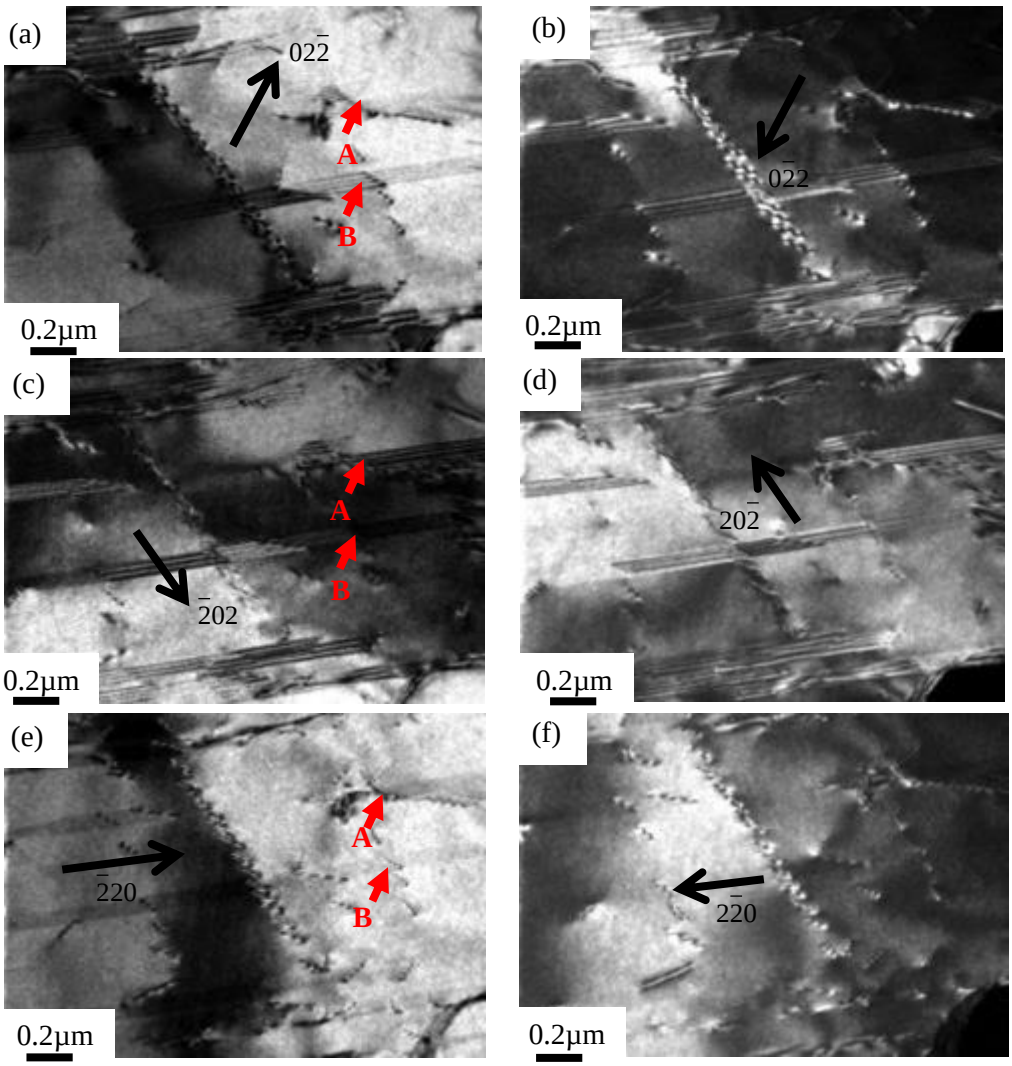


Figure 5.15. Representative area of interests (Face A, annealed at 1400 ˚C for 30 min) under different diffraction conditions: (a) Bright field image with diffraction vector **g** = $02\bar{2}$; (b) Dark field image with diffraction vector **g** = $0\bar{2}2$; (c) Bright field image with diffraction vector **g** = $\bar{2}02$, (d) Dark field image with diffraction vector **g** = $20\bar{2}$; (e) Bright field image with diffraction vector **g** = $\bar{2}20$; (f) Dark field image with diffraction vector **g** = $2\bar{2}0$.

Another representative TEM foil was made from the recrystallized region, with a single high angle grain boundary across the middle of the specimen, as shown in Figure 5.16. TEM micrographs from this sample provide insight into the defect morphology of the recrystallized grains.

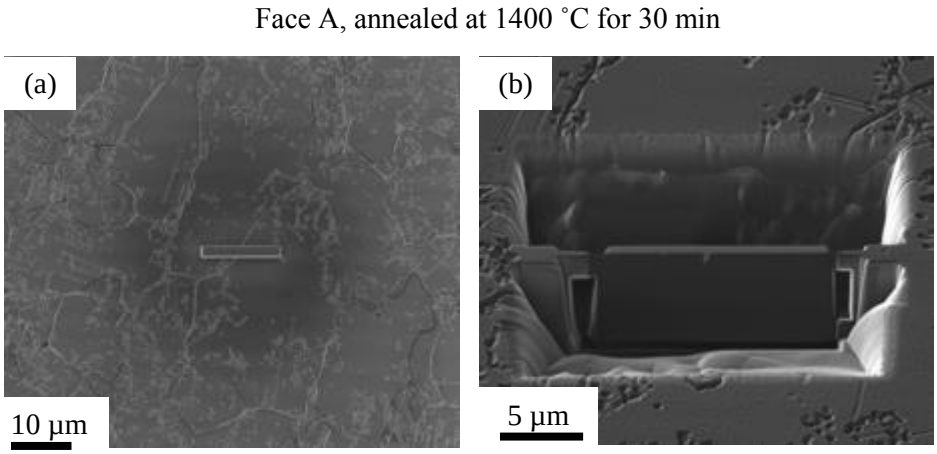


Figure 5.16. SEM image of sample preparation across a grain boundary in the recrystallized region from Face A, annealed at 1400 ˚C for 30 min (the surface is etched): (a) Post platinum deposition; (b) Pre final cut and sample lift-out (the bright stripe on top is platinum layer with a clear notch indicating the position of the etched grain boundary).

The recrystallized grains observed in TEM contain significantly lower defect contents, as illustrated in Figure 5.17. Very few short dislocation segments were observed, indicating that the foil normal is far away from the [111] zone axis. Defects in this specimen are mainly stacking faults and associated partial dislocations. All the defects appear out of contrast under diffraction vector [040] (Figure 5.17a). Stacking faults lying in $[\bar{2}\bar{2}0]$ orientation disappear when using $(\bar{2}\bar{2}0)$ reflection but appear when using $(2\bar{2}0)$ reflection. Similarly, stacking faults lying along $[2\bar{2}0]$ direction show

strong contrast under [$\bar{2}\bar{2}0$] diffraction vector but disappear under [$2\bar{2}0$] diffraction vector, as shown in Figure 5.17 (b) and (c). The partial dislocations all lie in the direction [010].

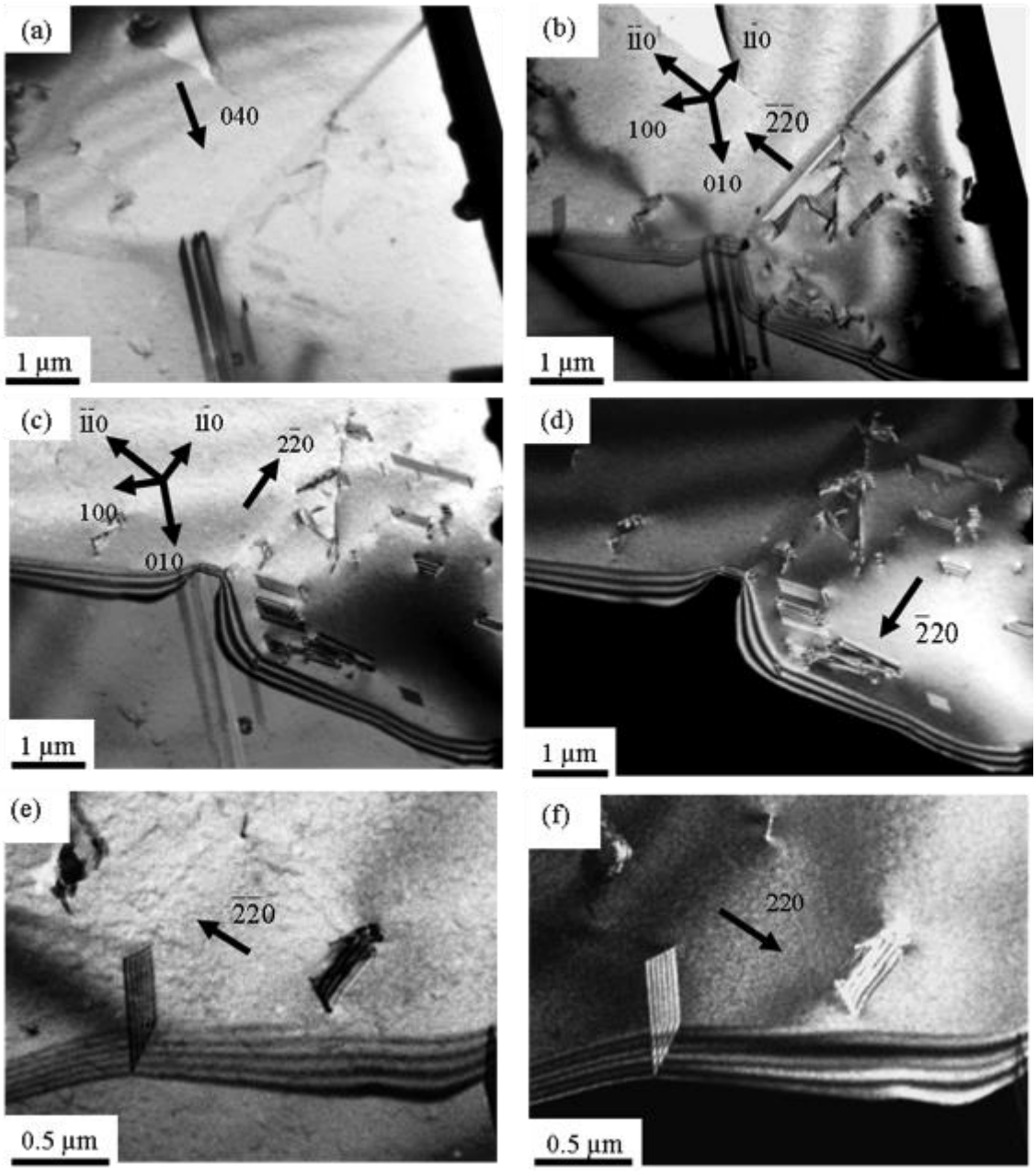


Figure 5.17. Low magnification TEM micrographs of defects: (a) Near (001) pole bright field image under diffraction vector **g**= (040), defects in the top grain show very weak contrast; (b) Near (001) pole bright field image under diffraction vector **g** = ($\bar{2}\bar{2}0$), all the stacking faults

along [$\bar{2}\bar{2}0$] orientation out of contrast; (c) Near (001) pole bright field image under diffraction vector **g** = ($2\bar{2}0$), all the stacking faults along [$2\bar{2}0$] out of contrast; (d) Near (001) pole dark field image under diffraction vector **g** = ($\bar{2}20$); (e) and (f) Bright and dark field images of a specific stacking fault interacting with the grain boundary under diffraction vector **g** = ($\bar{2}\bar{2}0$) and **g** = (220), respectively.

5.3.3.2 Defects in Face A annealed at 1400 ˚C for 60 min by TEM

A representative TEM specimen was made from the recrystallized region in the as-received sample (Face A) after annealing at 1400 ˚C for 60 min. The specimen was also specifically chosen across a high angle grain boundary (Figure 5.18a) to compare with the TEM specimen made in the same sample annealed for 30 min (as shown in Figure 5.16). Low magnification TEM micrograph indicates that the specimen contains remarkably low defect content, mainly in the form of stacking faults (as shown in Figure 5.18b). The stacking fault density is approximately 3 x 10^{9} m^{-2}, examined from TEM micrographs.

Representative stacking faults were examined under different diffraction conditions in order to characterize the nature of the defects. As indicated in Figure 5.19, stacking faults lying along the [$2\bar{2}0$] orientation disappear under ($2\bar{2}0$) reflection, while stacking faults lying along the [$20\bar{2}$] orientation show very weak contrast under ($20\bar{2}$) reflection and completely no contrast under ($1\bar{1}1$) reflection.

The second representative specimen was fabricated from the recrystallized region, across a high angle grain boundary which separates a high dislocation density grain and a low dislocation density grain, as shown in Figure 5.20. The TEM micrographs reveal

that the highly defective grain contains mainly stacking faults, but in relatively high concentration, while on the other side the grain is almost defect free.

In order to confirm the character of the long straight grain boundary locating in the middle of large stem-like grains, a thin TEM foil was made across one of these grain boundaries (Figure 5.21a) and examined by TEM. It is shown in TEM bright field micrograph (Figure 5.21b) that this type of grain boundary lies straight across the specimen. The diffraction pattern across the grain boundary verifies the twinned nature.

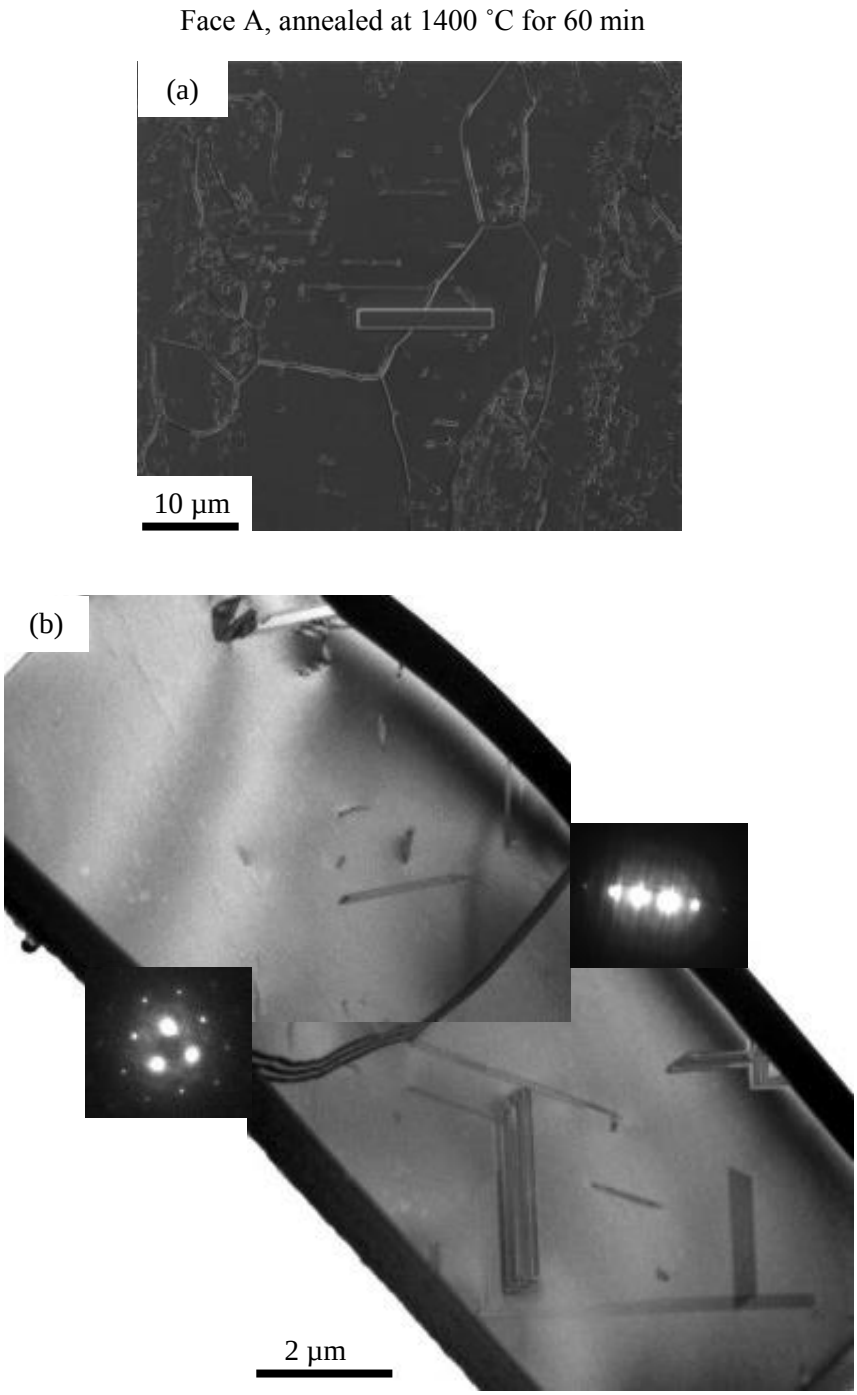


Figure 5.18. (a) SEM micrograph of the TEM specimen made across a grain boundary in the recrystallized region in Face A, annealed at 1400 ˚C for 60 min (the surface is etched); (b) Low magnification TEM micrograph of the specimen overview, revealing that the defects are primarily stacking faults. Diffraction patterns of each grain are attached.

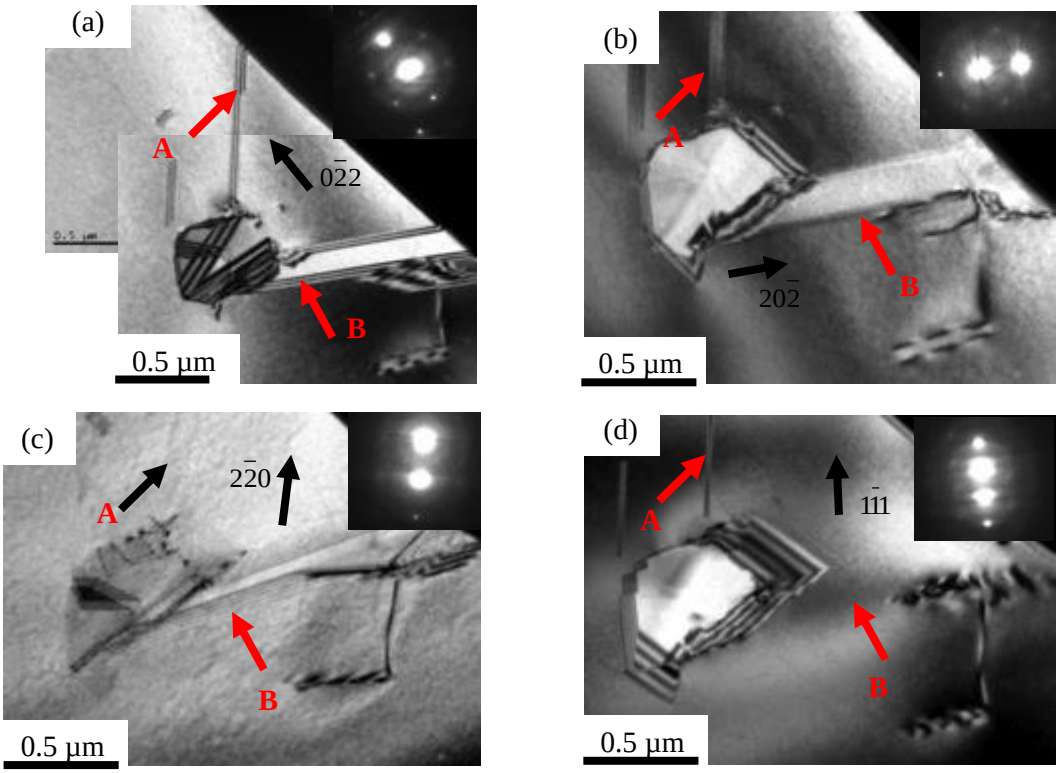


Figure 5.19. Representative stacking faults and twins in Face A, annealing at 1400 ˚C for 60 min, under different diffraction conditions: (a) [111] zone axis, **g** = ($0\bar{2}2$); (b) [111] zone axis, **g** = ($20\bar{2}$); (c) [001] zone axis, **g** = ($2\bar{2}0$), stacking fault A disappears; (d) [011] zone axis, **g** = ($\bar{1}11$), stacking fault B disappears.

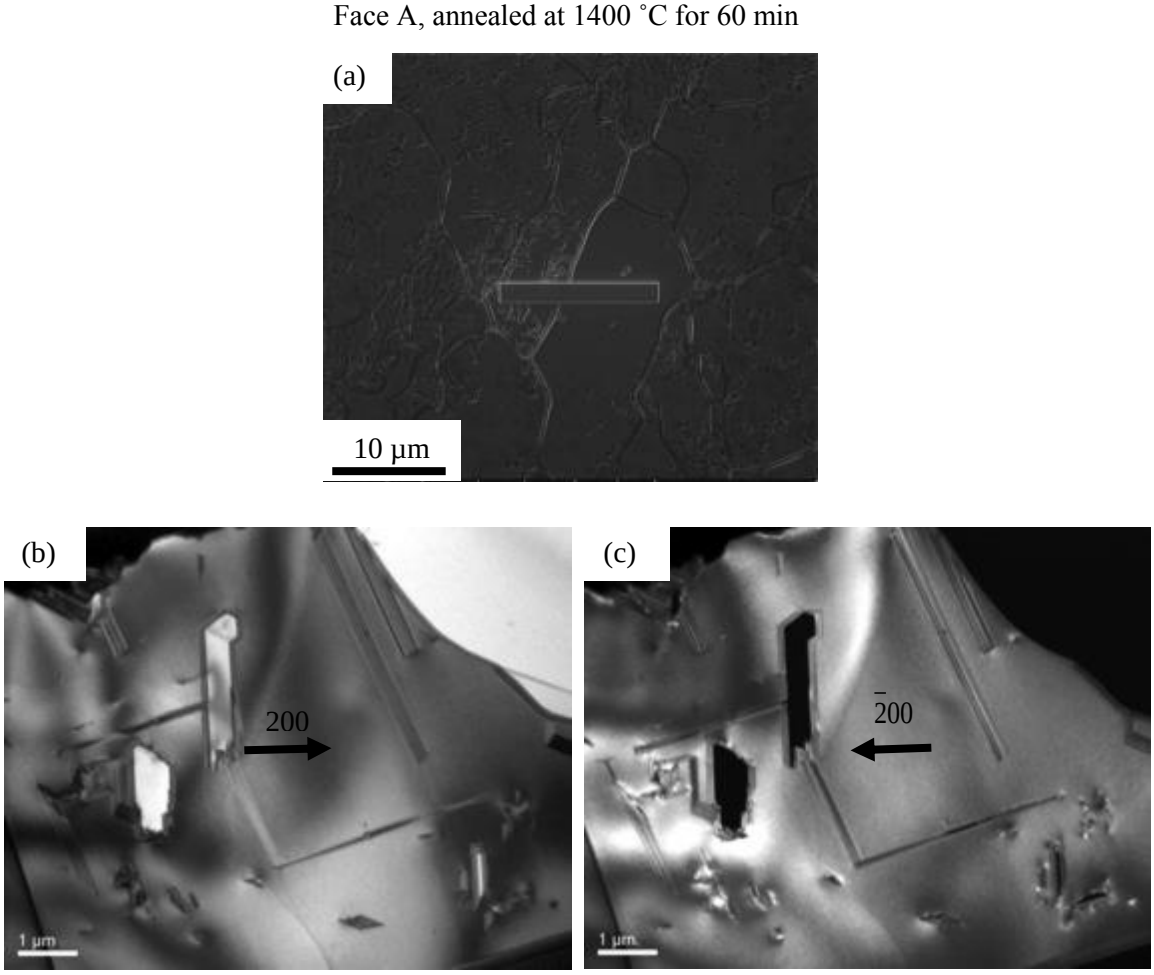


Figure 5.20. (a) SEM micrograph showing a TEM specimen made across a grain boundary separating a highly defective grain and a clean grain (the surface is etched) in Face A, annealing at 1400˚C for 60min; (b) Low magnification TEM bright field image and (c) dark field image show that the high dislocation etch pits grain contains mainly stacking faults and twins, whereas the low dislocation etch pits grain is almost defects free.

Face A, annealed at 1400 ˚C for 60 min

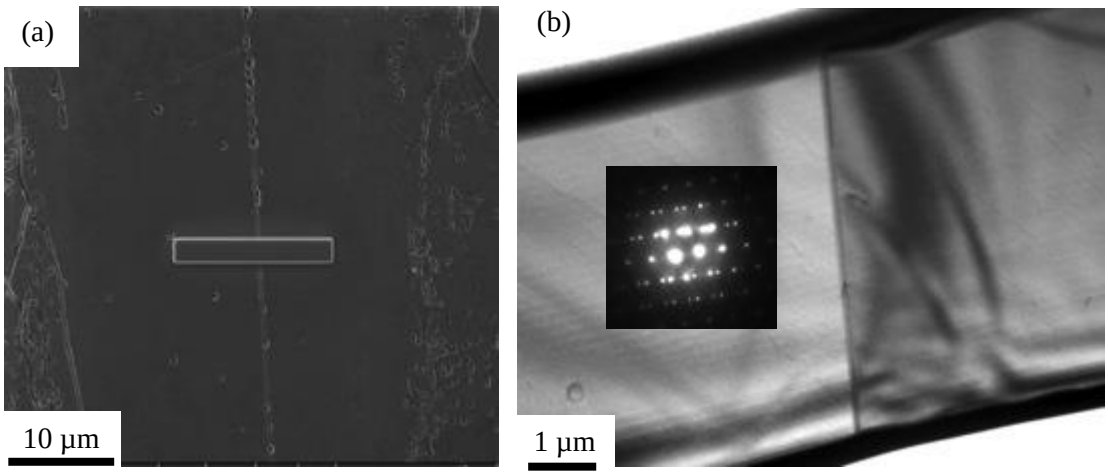


Figure 5.21. (a) A TEM specimen made across the long straight grain boundary in Face A, annealing at 1400 ˚C for 60 min (the surface is etched); (b) Low magnification bright field micrograph and diffraction pattern across the grain boundary confirming the twinned nature.

5.3.3.3 Defects in Face B annealed at 1400 ˚C for 30 min by TEM

A representative TEM foil was also fabricated across the grain boundary dividing the recrystallized region and the un-recrystallized un-recrystallized in Face B samples annealed at 1400 ˚C for 30 min. This enables the defect content in both types of microstructures to be directly compared in a single specimen. Specimen preparation is shown in Figure 5.22.

Face B, annealed at 1400 ˚C for 30 min

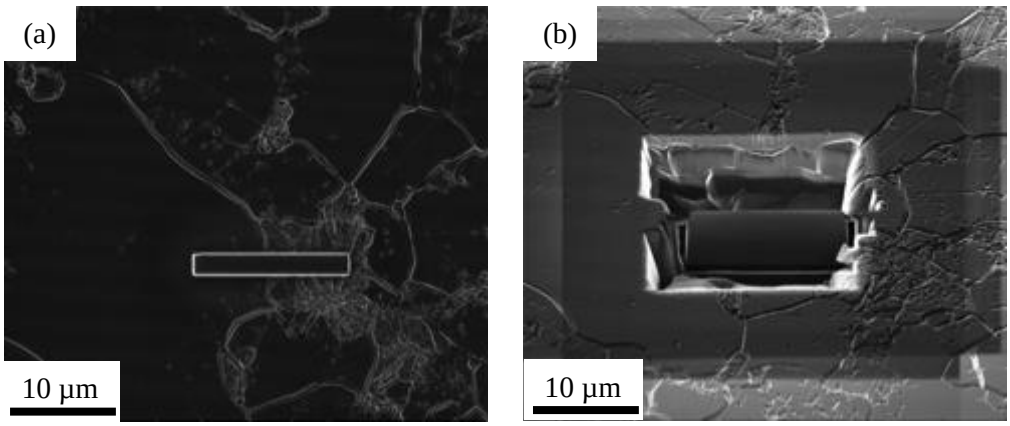


Figure 5.22. SEM micrographs of specimen preparation (the surface is etched): (a) Post platinum deposition; (b) Side view of the specimen before lift out.

Low magnification TEM micrographs illustrate the difference in defect contents from both sides of the grain boundary, with the recrystallized grain marked as grain A, and the un-recrystallized grains marked as B and C. Both bright field and dark field micrographs were taken under two-beam conditions with {111} reflections.

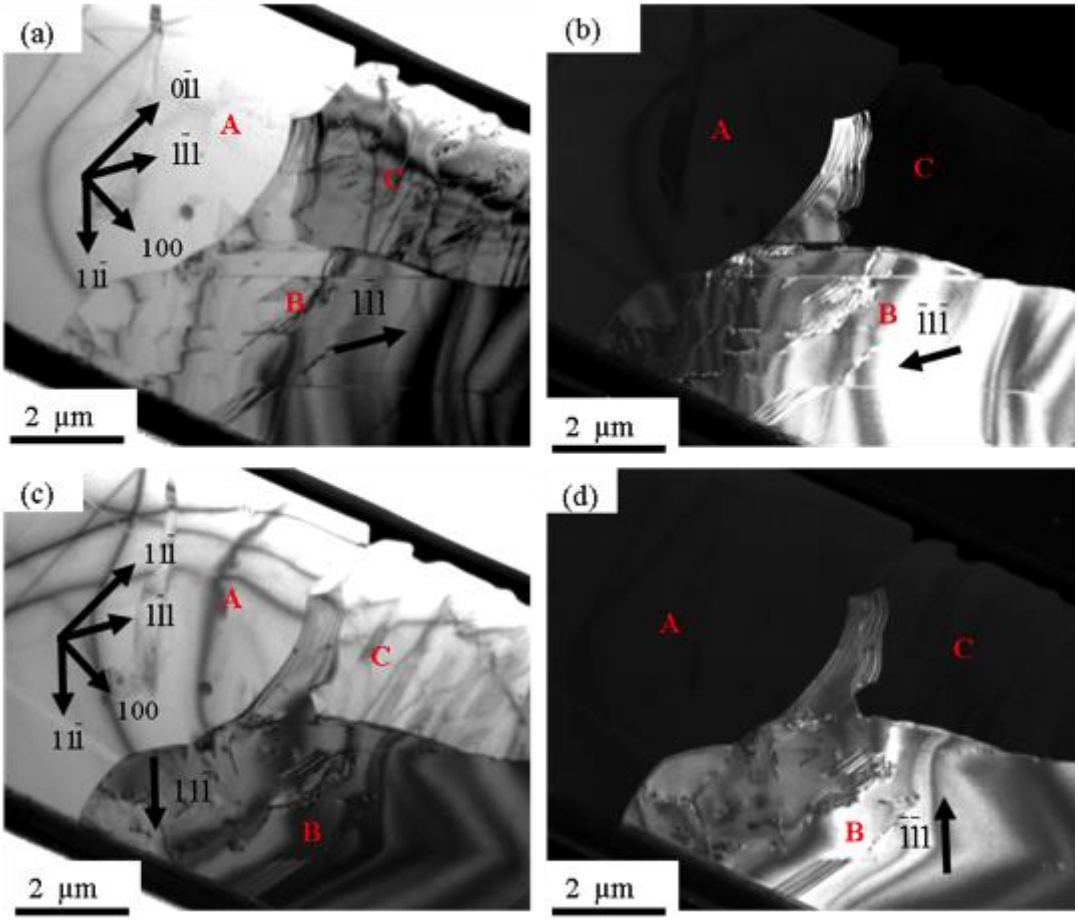


Figure 5.23. Low magnification TEM micrographs of the specimen: (a) and (b) Bright field and dark filed pair images, un-recrystallized grain B under diffraction vectors [$\bar{1}$11] and [$\bar{1}\bar{1}$1]; (c) and (d) Bright field and dark filed pair images, un-recrystallized grain B under diffraction vectors [1 1$\bar{1}$] and [$\bar{1}\bar{1}$1].

5.4 Deformation of polycrystalline silicon at 1155 ˚C for 4 hours

In the prior two sections, the effect of pre-deformation annealing on the microstructural evolution of the as-received polycrystalline material was described. As stated before, the defect examination reveals that the as-received highly defective materials recrystallized by around 90 % upon annealing at 1400 ˚C for 30 min. However, further

annealing up to 2 hours did not alter the microstructure to a lower defect content level. Therefore the cleaved polycrystalline silicon sample in dimension of 20 mm x 20 mm x 10 mm was then annealed in a vacuum furnace under clean conditions for 30 min at 1400 ˚C. The silicon sample together with other components including alumina push rods and high-purity alumina discs were then cleaned in the clean room using standard RCA procedure before being assembled in the deformation rig for the high temperature compression test. The compression was performed with the furnace temperature set as 1200 ˚C, while the true sample temperature was 1150 ˚C according to a thermal couple placed at the location of the specimen. The sample was compressed by 10 % in 4 hours under this isothermal condition. The maximum stress applied was 100 MPa and the average strain rate was approximately 6.94×10^{-6} s^{-1}. The compression axis coincides with the original grain growth direction in the material.

Thin slices of specimens of 1mm thickness were then mechanically sawn from the deformed sample for further microstructural examination and a post-deformation annealing process investigation.

5.4.1 Investigation of the as-deformed polycrystalline silicon microstructures by SEM

The microstructures of polycrystalline silicon after deformation were examined by SEM on both Face A and Face B after standard metallographic preparation followed by etching for 30 s in a Sirtl etch solution.

SEM micrographs of representative regions before and after deformation in the surface parallel to Face A are shown in Figure 5.24 for directly comparing the microstructures both globally and locally. It is clear that compression at 1150 ˚C by 10% did not bring

about a significant microstructural alteration in general, apart from introducing a large number of inner grain sub-grain boundaries and increased average dislocation density across the sample. One immediately apparent observation is that in large stem-like grains, which only had a single long straight twin grain boundary before deformation, cell structures composed of sub-grain boundaries were generated during the uniaxial compression process, as marked by red arrows in the top left and the top right subfigures in Figure 5.24. These cell structures have an average diameter of 15 μm. Higher magnification SEM micrographs also reveal that before deformation the grain interior is primarily comprised of a large number of stacking faults and associated partial dislocations (see the bottom left subfigure in Figure 5.24), while after deformation a remarkably large number of inner grain sub-grain boundaries appears in the form of dislocation arrays, although the average grain size (defined as the area enclosed by high angle grain boundaries) remains the same (see the bottom right subfigure in Figure 5.24). The average dislocation density was determined by conventional etch pit counting, yet it is worth noting that because of the inhomogeneous etch pit distribution it has proven difficult to produce reliable figures. The average dislocation density before deformation was estimated as 1.0×10^{12} m^{-2}, visually judging from the etch pit number in the red square from the bottom left micrograph of Figure 5.24. After deformation, the number of etch pits was increased to the level of 8.0×10^{12} m^{-2}, indicated by red square B from the bottom right micrograph of Figure 5.24, which is the relatively higher dislocation density area. The relatively lower dislocation density area marked by red square A in the same micrograph gave a density of 2.0×10^{12} m^{-2}.

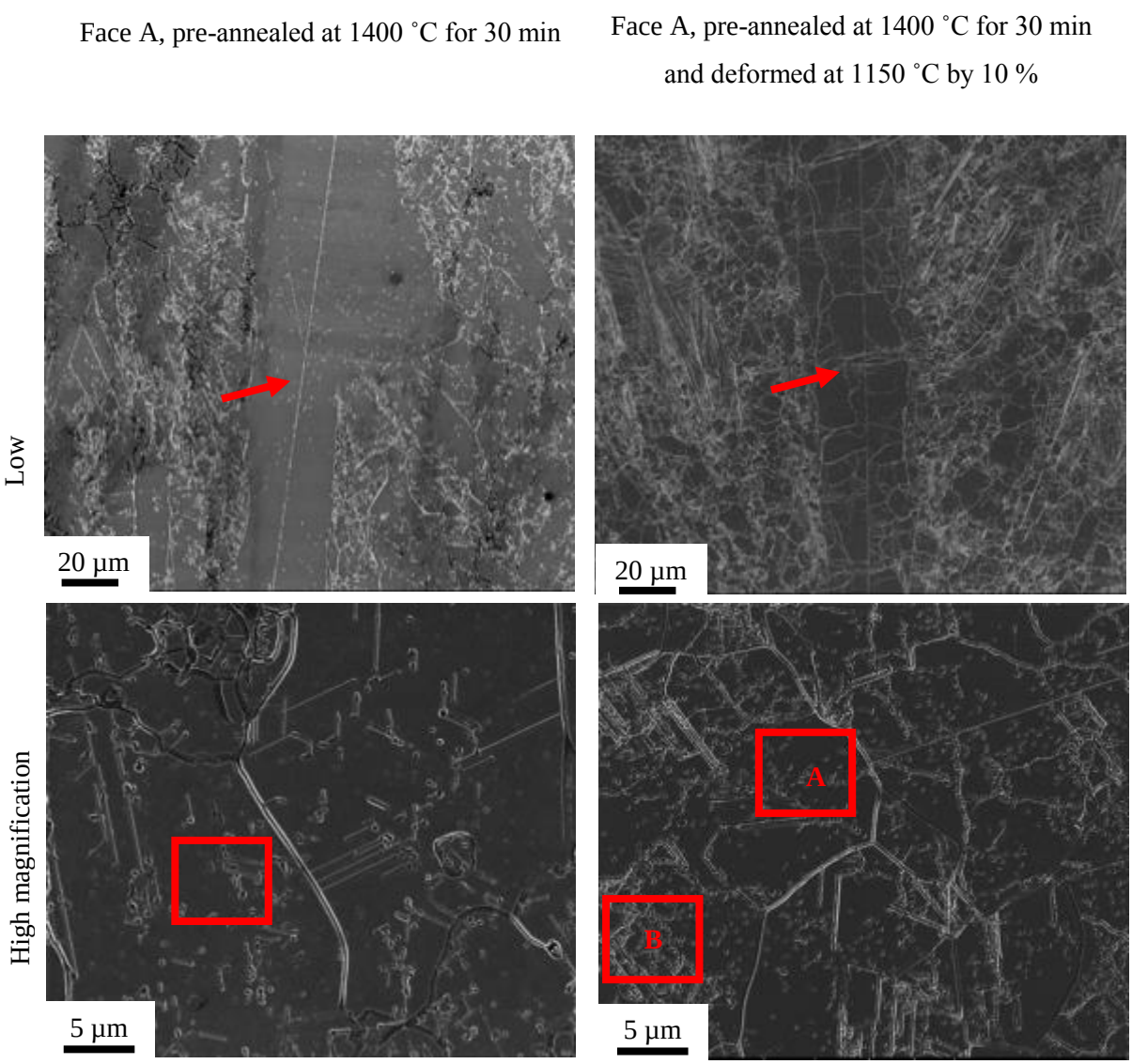


Figure 5.24. SEM micrographs of etched surface from Face A, pre-annealed at 1400 ˚C for 30 min, and after deformation at 1150 ˚C by 10 %. Red squares enclose selected areas for dislocation etch pit counting.

5.4.2 Crystallographic information of the as-deformed polycrystalline silicon by EBSD

In order to examine the crystallographic information of the as-deformed materials further, EBSD investigation was applied to both Face A and Face B on the deformed sample.

EBSD maps of 100 μm x 100 μm using step size 0.5 μm were acquired from both Face A and Face B, after standard diamond polishing followed by colloidal silica polishing. The pattern quality map, orientation distribution map, grain map with Σ 3 and Σ 9 grain boundaries highlighted by black lines and red lines respectively, and inverse pole figure are presented in Figure 5.25 and Figure 5.26. The images in Figure 5.25 are viewed along the compression plane and the original grain growth direction is vertical in these maps. Whereas the images in Figure 5.26 are viewed along the strain plane which is perpendicular to the compression axis and the original grain growth direction. EBSD maps reveal a similar grain microstructure compared to that before deformation. It is speculated that apart from some still existing residual structure of the as-received un-recrystallized, the general microstructure was not noticeably altered during the high temperature compression. This indicates that dynamic recrystallization is unlikely to occur under this deformation condition in polycrystalline silicon. However, dynamic recovery might have taken place during the deformation since the dislocation density introduced is lower than expected from a 10 % strain. This, however, requires further quantitative analysis. The inverse pole figure in Figure 5.26 reveals a more diverse grain orientation distribution compared to the strong texture in the as-received material.

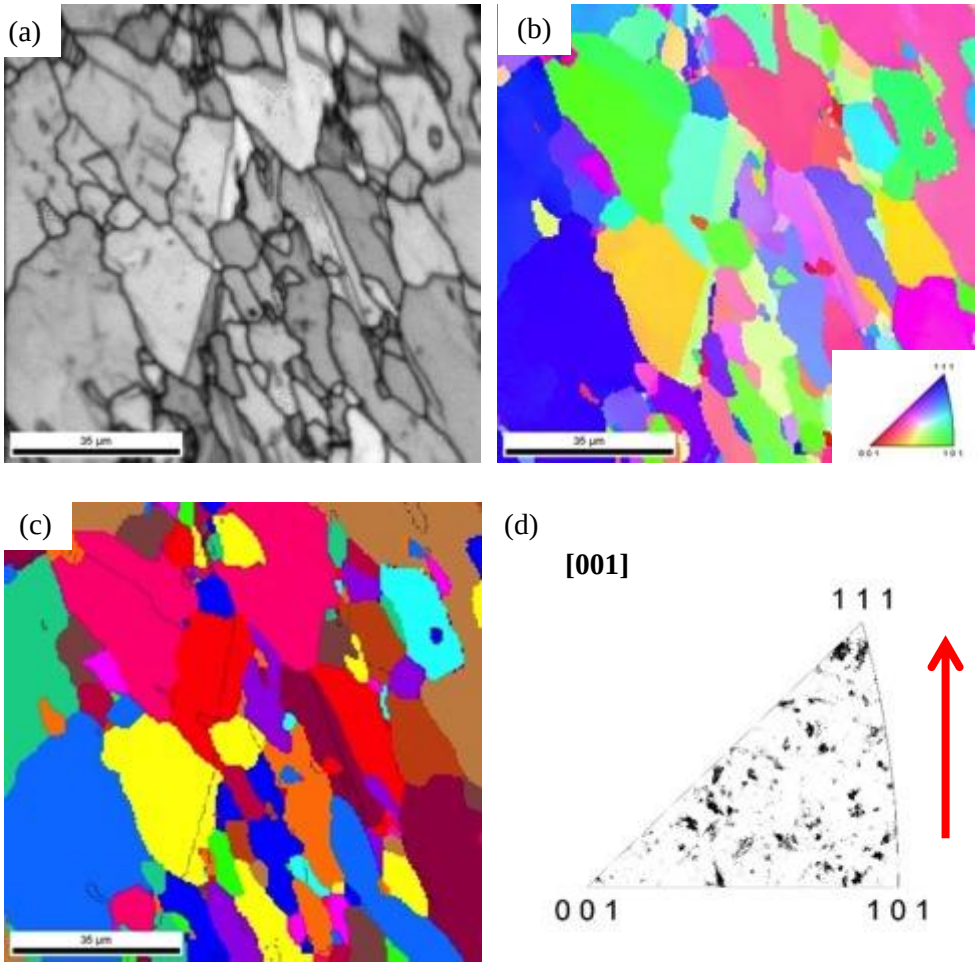


Figure 5.25. EBSD maps of Face A after deformation: (a) Pattern quality map; (b) Grain orientation distribution map; (c) Grain map with Σ 3 and Σ 9 grain boundaries highlighted by black lines and red lines, respectively; (d) Inverse pole figure. Initial grain growth direction and compression axis are vertical in these maps, as indicated by the red arrow.

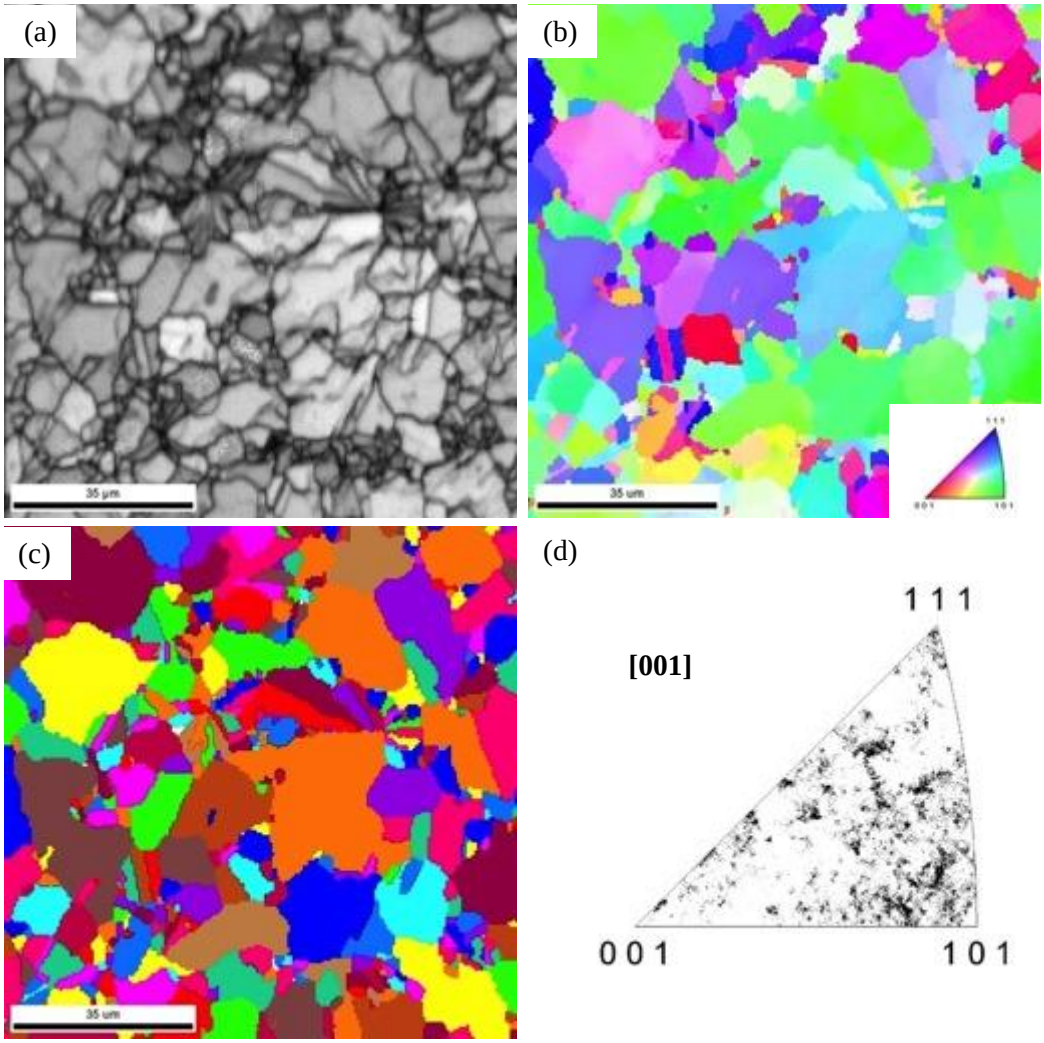


Figure 5.26. EBSD maps of Face B after deformation: (a) Pattern quality map; (b) Grain orientation distribution map; (c) Grain map with Σ 3 and Σ 9 grain boundaries highlighted by black lines and red lines, respectively; (d) Inverse pole figure. Initial grain growth direction and compression axis are outwards in these maps.

5.4.3 Defect morphology investigated by TEM

For the purpose of revealing the defect morphology in the deformed bulk material straightforwardly, some TEM foil specimens were fabricated using the FIB lift-out technique. A typical low magnification micrograph of such a foil is shown in Figure 5.27. It was noticed that plastic deformation induces sub-grain boundaries comprising closely spaced dislocations (marked by red arrows) and complex dislocation network

consisting of relatively long dislocation segments within these sub-grains. The dislocation morphology in the deformed material appears remarkably different from those before deformation (see Figure 5.14).

Some diffraction contrast work was conducted to characterize the dislocation characters in different grains, as shown in Figure 5.28. In both cases the specimen was tilted to near the [001] zone axis, as shown in Figure 5.28 (a) and (b). Two two-beam conditions were chosen for **g** · **b** analysis, **g** = [$\bar{2}\bar{2}0$] and [$\bar{2}20$], respectively. As marked by yellow circles, dislocations with Burgers vector ½[110] appear when **g** = [$\bar{2}\bar{2}0$] and disappear when **g** = [$\bar{2}20$], while blue circles highlight dislocations with Burgers vector ½[$1\bar{1}0$] which are out of contrast when **g** = [$\bar{2}\bar{2}0$] but in contrast when **g** = [$2\bar{2}0$], as depicted in Figure 5.28 (c)-(f). The dislocation line directions are are not coinciding with any distinguished crystallographic orientation, therefore they may have a mixed edge-screw character.

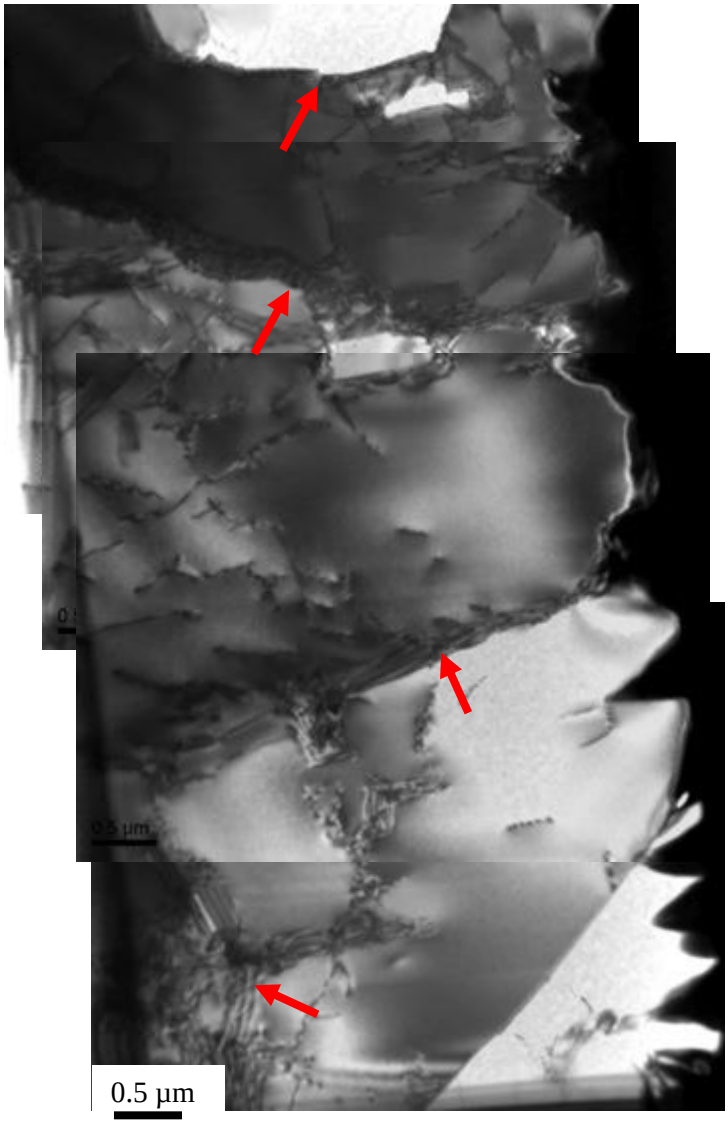


Figure 5.27. Low magnification TEM micrograph of as-deformed polycrystalline silicon compressed at 1150 ˚C by 10 % strain (specimen fabricated from Face A). Red arrows mark the sub-grain boundaries.

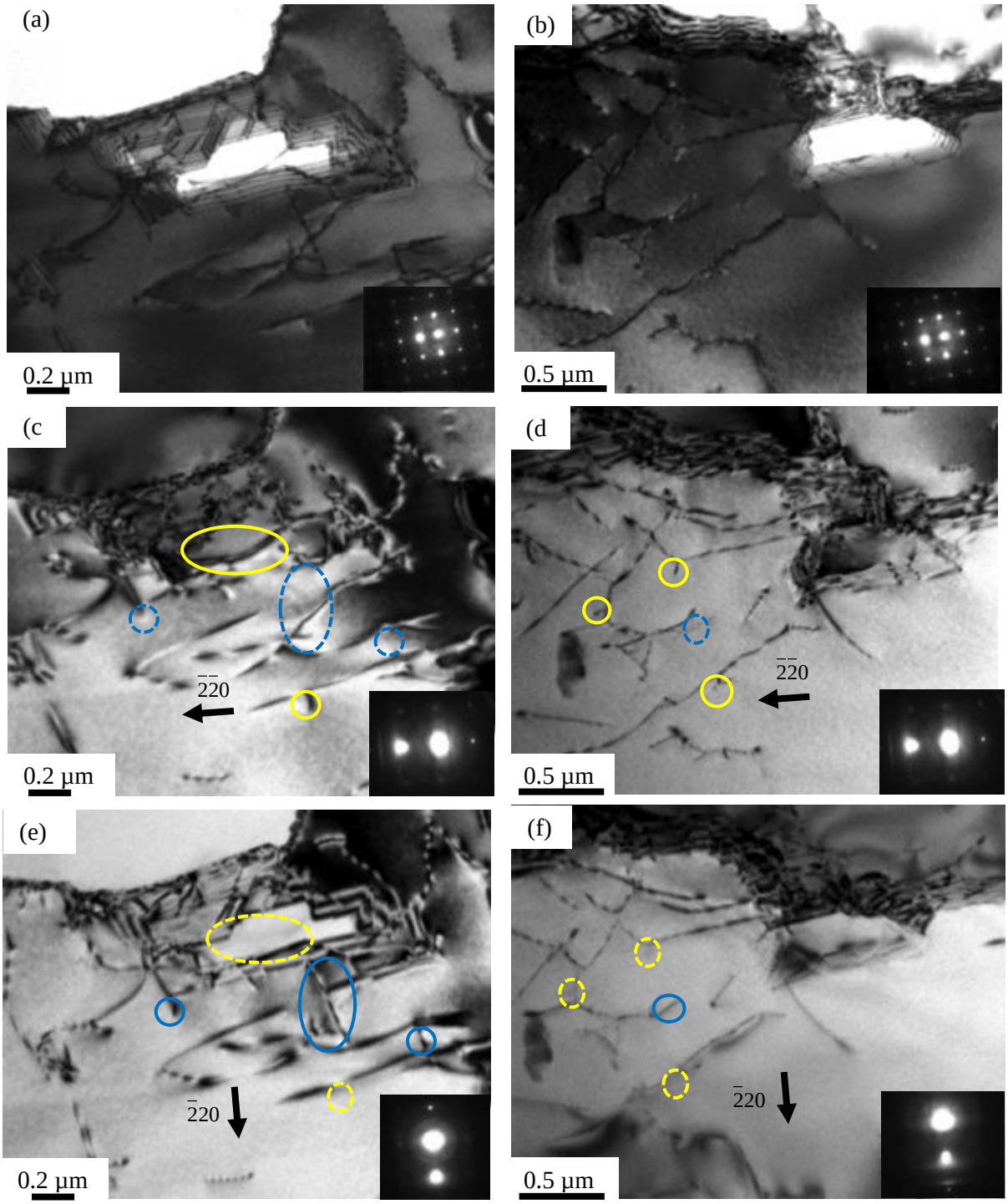


Figure 5.28. High magnification TEM micrographs reveal dislocation characters in the as-deformed polycrystalline silicon compressed at 1150 ˚C by 10 %: (a)-(b) near the [001] zone axis bright field image; (c)-(d) bright field image under two-beam condition, **g** = $\bar{2}\bar{2}0$, dislocations marked by yellow solid circles appear and marked by blue dash circles disappear under this condition; (e)-(f) bright field image under two-beam condition, **g** = $\bar{2}20$,

dislocations marked by blue solid circles appear and marked by yellow dash circles disappear under this condition.

5.5 Subsequent annealing effects on polycrystalline silicon microstructures

Plastic deformation generates a large number of crystallographic defects in the material, mainly in the form of dislocations. It is thus crucial to reduce the deformation-induced defect density in order to produce silicon material with potentially satisfactory electrical properties. Ultimately this material would need to have good performance in photovoltaic conversion efficiency.

High temperature annealing has been proven an effective approach towards dislocation annihilation in multicrystalline silicon as stated in various previous studies [37], [225]. This annihilation behavior strongly depends on the dislocation characters, *i.e.* their Burgers vectors and line vectors. Dislocations become mobile in silicon at elevated temperatures and dislocations with opposite Burgers vectors thus attract to each other and annihilate. Conversely, dislocations with the same Burgers vector will repel each other. It has been shown in the preceding section that uniaxial compression-induced dislocations obtain the morphology of tangles and kinks, and thus are likely to annihilate during high temperature isothermal treatments. Therefore it becomes interesting to examine the defects density and morphology evolution with respect to an annealing process after deformation, which will provide insights into the determination of the optimal subsequent annealing conditions after deformation.

The as-deformed samples were then subjected to annealing at a near melting point temperature of 1400 ˚C (silicon melts at 1414 ˚C) for various lengths of time. The microstructural evolution along the annealing duration was assessed by preferential etching, SEM, TEM and EBSD. Samples from Face A were annealed for 15 min, 30 min, 60 min and 120 min, respectively. For the purpose of comparison, samples from Face B were annealed for 30 min and 120 min. All the as-deformed specimens were mechanically polished by diamond paste and colloidal silica before annealing to ensure the elimination of sawing damage from the specimen preparation. No appreciable scratches were observed under optical microscope after polishing, indicating a completely damage-free surface. Therefore no sawing-induced dislocations will affect the microstructural evolution during annealing. The annealing was conducted by enclosing these thin as-deformed specimens into clean quartz tubes under an argon ambient. The capsules were then put into a box furnace and kept at 1400 ˚C for different time durations. The furnace ramping profile is shown in Section 2.4.

5.5.1 Investigation of the annealed microstructures by SEM

The subsequently annealed silicon samples underwent standard metallographic preparation and Sirtl etching for 30 s followed by close examination in the SEM, as shown in Figure 5.29.

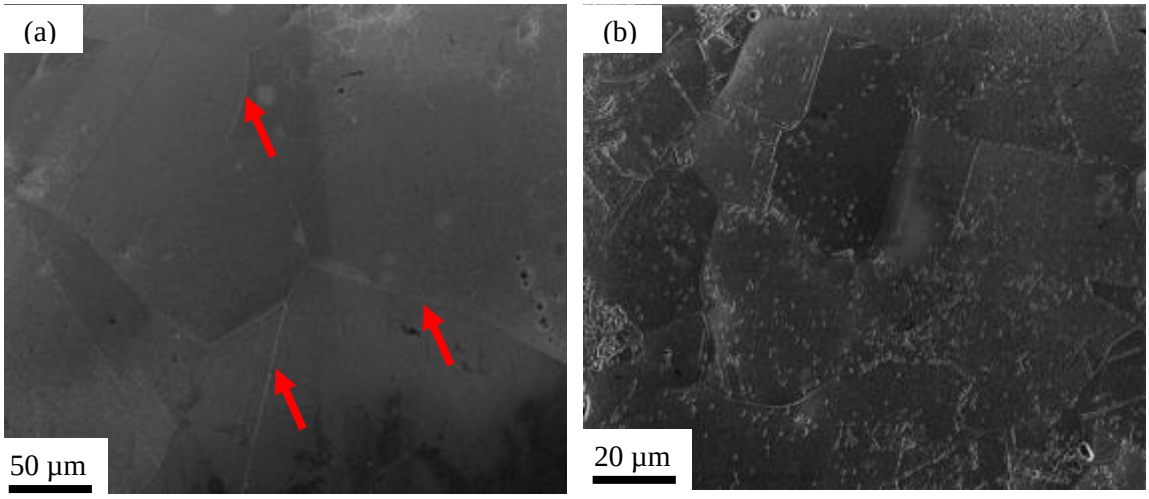


Figure 5.29. SEM micrographs of the etched second recrystallization regions in polycrystalline silicon deformed at 1150 ˚C by 10 % and annealed at 1400 ˚C for 15 min (Face A): (a) Low magnification, grain boundaries are marked by red arrows; (b) Relatively higher magnification.

It was observed that even just 15 min annealing at 1400 ˚C transformed 50 % of the deformed material into a completely different microstructure by static recrystallization, both in Face A and Face B, although only images from Face A are shown in Figure 5.29. This 'second recrystallization' microstructure comprises large grains with straight grain boundaries, revealed by Sirtl reagent etching, as shown in Figure 5.29 (a). The average grain size is several hundred microns, with a relatively inhomogeneous dislocation etch pit distribution. The representative higher dislocation density region in this second recrystallization microstructure is shown in Figure 5.29 (b) at a relatively higher magnification. The average dislocation density of this area calculated by etch pit counting is approximately 5.0×10^{10} m^{-2}.

Some partially-recrystallized grains were also found in the rest of the specimen. Typical microstructure is shown in Figure 5.30. It is revealed that large recrystallized grains with very low dislocation etch pit density and relatively straight grain boundaries are surrounded by small un-recrystallized grains with much higher dislocation content.

Apart from the remarkable difference in dislocation density, the most significant microstructural difference between the large recrystallized grain and the surrounding small grains are the absence of sub-grain boundaries in the recrystallized grain, indicating that they have gone through a recrystallization process, presumably via nucleation of new grains. In contrast, there still exist abundant sub grain boundaries consisting of aligned dislocation etch pits arrays in the surrounding microstructure, indicating no fundamental microstructural change in these regions during subsequent annealing from the as-deformed state. Quantitative analyses on GND (geometrically necessary dislocation) density distributions and evolution in polycrystalline silicon during subsequent annealing will be addressed in detail in the next chapter.

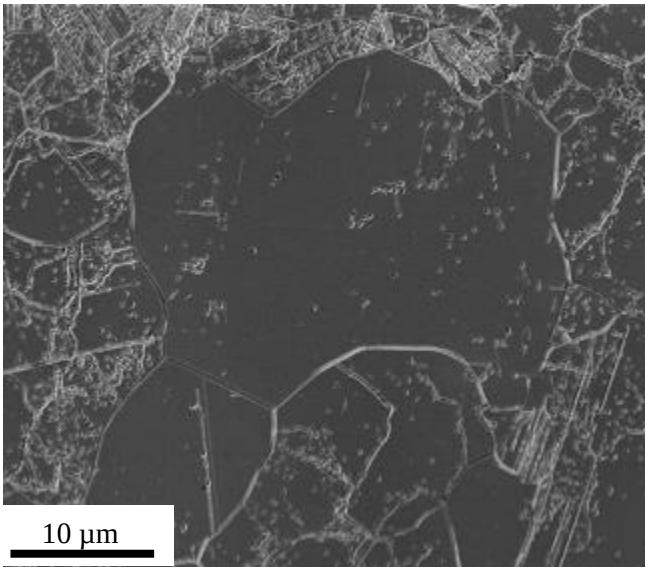


Figure 5.30. Typical etched partially-recrystallized region with a large low dislocation density grains surrounded by un-recrystallized microstructure, from polycrystalline silicon deformed at 1150 ˚C by 10 % strain and annealed at 1400 ˚C for 15 min.

One important factor to note relating to the compression process is that due to sample geometry the deformation is globally inhomogeneous. Hence even though all the specimens being annealed were cut from the same area of the as-deformed polycrystalline silicon bulk, their local deformation percentages remain notably

different. Therefore it does not seem to be possible to conclusively elicit the effect of annealing time on the percentage of second recrystallization in the as-deformed material, based on the observation of microstructure evolution in the as-deformed material undergoing subsequent annealing for 15 min, 30 min and 60 min. However, 120 min annealing at 1400 ˚C witnessed a completed recrystallization in both Face A and Face B. Henceforth the suitable subsequent annealing condition determined for the large deformed polycrystalline specimen is 1400 ˚C for 120 min.

5.5.2 Investigation of the annealed microstructures by EBSD

The crystallographic information of the annealed material was also investigated by EBSD mapping. A big EBSD map of 500 μm x 500 μm was scanned from a specimen (parallel to Face A) annealed at 1400 ˚C for 15 min and is presented in Figure 5.31. This map size was determined for the purpose of providing large scale information of grain orientation and grain size distribution. Two different types of grain structures were observed in this sample: the as-deformed microstructure occupying the upper part of the map and the second recrystallization microstructure in the lower part of the map. The grain orientation distribution (Figure 5.31a) is rather diverse, implying no strong texture in this sample. The pattern quality map (Figure 5.31b) suggests that the second recrystallization region provide good pattern quality thus it appears bright, inferring a lower defect density, while the as-deformed region appears dark due to the relatively more blurred patterns obtained, presumably due to a higher defect content.

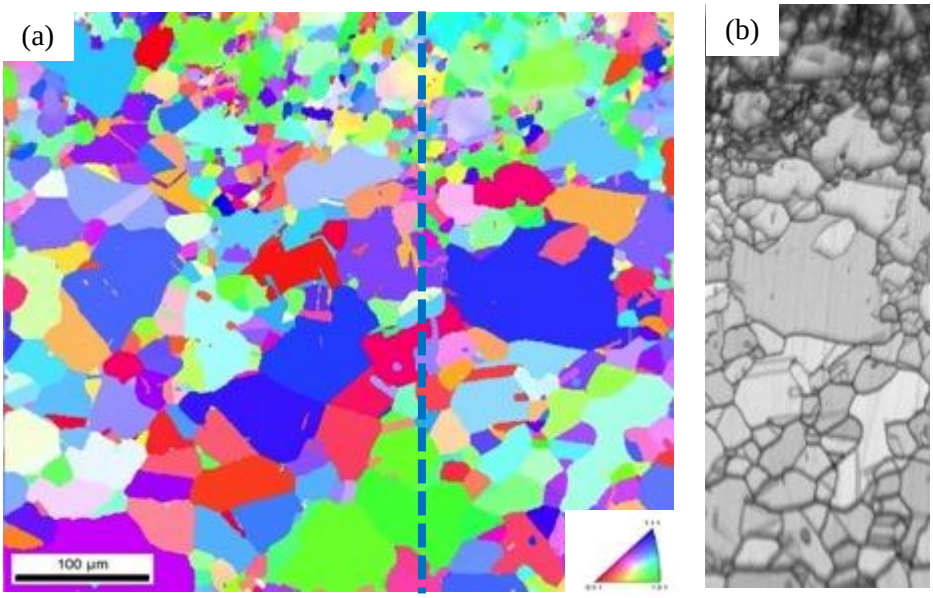


Figure 5.31. EBSD maps of polycrystalline silicon deformed at 1150 ˚C by 10 % and annealed at 1400 ˚C for 15 min (Face A): (a) Grain orientation map 500 µm x 500 µm; (b) Pattern quality map of the region marked by the blue dash line in (a). The compression axis is vertical in these maps.

5.5.3 Defect morphology investigated by TEM

In order to gather further information on the bulk defect morphology, a TEM foil was fabricated across two twin boundaries within a large grain, from the second recrystallization region in the polycrystalline silicon sample (Face A). The sample has been deformed at 1150 ˚C by 10 % strain and subsequently subject to isothermal annealing at 1400 ˚C for 15 min. As illustrated in Figure 5.32, bright field image recorded approximately along the [011] pole with multiple strong reflections operating reveals a distinctly clean bulk microstructure. The dislocation density was estimated below 10^{10} m^{-2}, which is in the same order of magnitude with the number obtained by etch pit counting. However, since the TEM foil only covers a small fraction of the microstructure and on the basis of the fact that dislocation density distribution in the recrystallized region is relatively heterogeneous, the dislocation density value obtained

by TEM examination could only be locally suggestive. This is also the reason that no more TEM work was conducted on the second recrystallization microstructure.

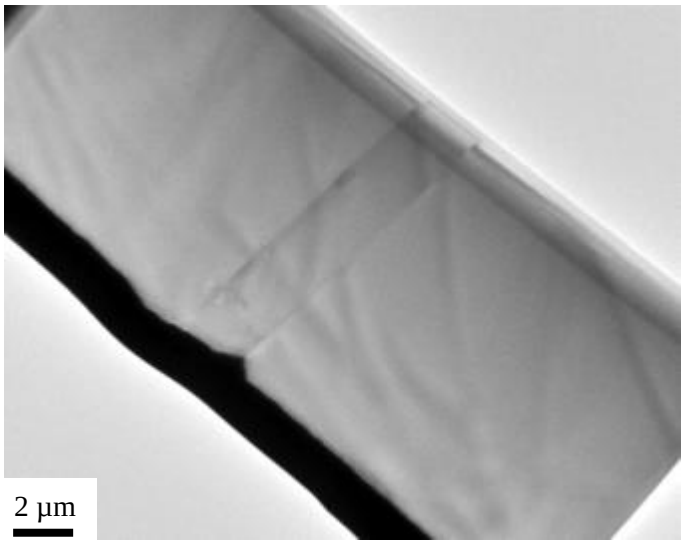


Figure 5.32. TEM bright field image viewed close the (011) pole from the second recrystallization region in polycrystalline silicon deformed at 1150 ˚C by 10 % and subsequently annealed at 1400 ˚C for 15 min.

5.6 Discussion

The aim of this chapter was to present a detailed microstructural investigation of polycrystalline silicon after high temperature pre-annealing, after deformation, and after subsequent post-deformation annealing. The microstructural examination was mainly performed by preferential etching, SEM, TEM and EBSD. The recrystallization behaviour of as-received polycrystalline silicon upon high temperature annealing was studied and a suitable pre-annealing condition (before the deformation) was determined to minimise material processing time. Deformation at elevated temperature (1150 ˚C) by 10 % introduced substantial strain to the polycrystalline material which activated a second recrystallization during the post-deformation annealing process. The change in dislocation density and grain size was analysed in different microstructures. The main

microstructural findings in this work are discussed and compared with the literature in this section.

5.6.1 Microstructure of as-received polycrystalline silicon

The microstructure of as-received polycrystalline silicon grown by the Siemens process in this study is found to have an inhomogeneous stem-tree-like structure (Figure 5.2). Small grains nucleate discretely at various locations and form large twin grains which are generally elongated in the grain growth direction, radially outwards from the centre single silicon log. Straight Σ 3 and Σ 9 grain boundaries are commonly present within the twin grains. The grain sizes vary from 3 ~ 30 μm in length and 1 ~ 3 μm in diameter (Figure 5.4). The as-received polycrystalline silicon has a sharp < 110 > fibrous texture aligned with the grain growth direction with random rotations around this axis (Figure 5.5). Preferential etching failed to reveal the average dislocation density since the etch pits are extremely close packed (Figure 5.3).

The major observation of the as-received polycrystalline silicon used in this work is in good agreement with previous results of this kind of bulk material [58], [65], [66]. In previous studies, the growth texture of polycrystalline silicon was investigated by the Schultz reflection method and found to be along <110> direction with no preferred orientation about this axis [4], which is consistent with the results obtained by EBSD in this project. Columnar grains elongated in the growth direction were observed with an average grain size of 0.1~1μm [2], which is comparable with the findings here. This type of <110 > growth texture was also observed in polycrystalline silicon films deposited by CVD method on different silicon substrates which confirms that nucleation of { 110 } islands is kinetically favoured [222]. This was suggested by the

high surface energy of the (110) planes which causes the crystallites to grow in the < 110 > direction.

However, the surface microstructures in previous studies [51], [58], [61], [65], [66] were only examined qualitatively by optical metallography and the growth twins were only suggested by the appearance of striated needle clusters but never confirmed by relevant technique. Dislocation density was not reported in the CVD grown polycrystalline silicon.

The defect morphology and crystallographic information acquired by modern TEM and EBSD techniques were reported in this work for the first time. Σ 3 and Σ 9 twin grain boundaries were confirmed by EBSD. TEM further examined the twinning configuration present in the polycrystalline material. Although the average dislocation density was found impossible to estimate by conventional etch pit counting, it was quantitatively studied by the HR-EBSD cross-correlation analysis (see Chapter 6) and the average GND density was calculated as approximately 10^{14} m^{-2}.

Although the shortest pre-annealing time in this work is 30 min, it is not clear that if the 90 % recrystallization of the as-received material could occur in a much shorter time, due to the lack of experimental data. The recrystallization might as well have completed by 90 % in 10 min or less, and is not affected by further annealing at 1400 ˚C.

5.6.2 Recrystallization of the as-received polycrystalline silicon

The as-received polycrystalline silicon was subjected to thermal annealing at 1400 ˚C in this work and it was found that 30 min heat treatment at this elevated temperature refined 90 % of the material into a relatively more homogeneous matrix, via recrystallization, with a 30μm average grain size (Figure 5.7 and Figure 5.9). The

recrystallization was confirmed by the significant change in texture and grain boundary type, examined by EBSD, for instance the strong < 110 > fibre texture completely disappeared after annealing. The recrystallized material has no apparent texture and mainly contains high angle grain boundaries together with a few Σ 9 twin grain boundaries (Figure 5.10 and Figure 5.11). During this procedure, internal stresses contained in the initial material was used to promote the recrystallization as a driving force. Σ3 twin grain boundaries were transformed into more energetically favourable Σ 9 grain boundaries. In the material pre-annealed at 1400 ˚C for 30 min, TEM examination reveals a heavily defective microstructure from the un-recrystallized region, consisting of densely spaced short dislocation arrays and intensive stacking faults (Figure 5.13). The dislocation segments are approximately 300 nm apart, aligned in the < 211 > crystallographic direction (Figure 5.14). In contrast, the recrystallized region in the same material contains significantly lower concentrations of defects, mainly very few stacking faults (approximately 3×10^{9} m^{-2}) and associated partial dislocations. The stacking faults in both regions primarily lie along the < 110 > orientation (Figure 5.17). Prolonged annealing at 1400 ˚C up to 120 min does not further increase the recrystallization fraction (Figure 5.8). This can be possibly attributed to the low migration velocity of high-angle grain boundaries in covalent bonded materials [59] and lack of driving force after the completion of primary recrystallization. Despite the recrystallization phenomena of the as-received polycrystalline silicon material, this work is generally in good agreement with that of previous studies, although specific findings remain in dispute. In addition, no published information was found on the detailed bulk defect configuration and dislocation density in the recrystallized material from as-received state in the preceding studies.

The recrystallization of polycrystalline silicon was first reported by Ouwens and Heijligers [56] who qualitatively studied the recrystallization behaviour of CVD grown polycrystalline silicon layers between 50 and 400 µm thick with grain size of the order of 0.1 ~ 1µm. The heat treatment was performed between 800 ˚C and 1400 ˚C. It was observed that 98 % of the material recrystallized within 30 min at about 1200 ˚C, resulting in a microstructure with average grain diameter of approximately 20 µm. No further microstructural change was observed even with annealing at 1200 ˚C up to 70 hours. A second recrystallization was activated by annealing at 1350 ˚C for a relatively short time, whereby big grains of 100 µm are found amidst smaller grains with size of around 20 µm. No texture change, however, was demonstrated in their study. Therefore it was argued by Lall *et al.*[66]that the microstructure change should be more appropriately called recovery and grain growth.

A similar study regarding the performance of polycrystalline silicon layers grown on a flat substrate by CVD method upon recrystallization was conducted by Schins *et al.* [58], with silicon sheets containing a predominant < 110 > crystallographic texture and thicknesses varying from 20 µm to 150 µm. Thermal treatment for 3 hours at temperatures between 1350 ˚C and 1400 ˚C resulted in recrystallization with grains in size of 50 µm to 100 µm and a sharp < 111 > texture. These results demonstrate the possibility of recrystallization in as-grown CVD polycrystalline silicon films. Even though it is known that the as-deposited thin film silicon has the same texture as that of the as-deposited bulk silicon material [57], [222], their recrystallization behaviors can still differ considerably due to certain variations in growth conditions (for instance growth temperatures and deposition rates).

A systematic investigation of the influence on recrystallization phenomena of parameters such as crystal orientation, specimen thickness and heating temperature was also undertaken by Schins *et al.* [58] on fine grained (0.1~10 μm) high purity CVD bulk polycrystalline silicon. It was found that the heat treatment between 1350 ˚C and 1400 ˚C for 3 hours converted the as-received primary < 110 > fibrous texture into a strong < 111> texture with free rotation around this axis. The recrystallized matrix consists of inhomogeneous oblong grains which are 20 μm ~2 mm in length and 20 ~100 μm in diameter. The starting material and the annealing condition in the present study are both comparable to those in [58], however a much shorter time (annealing at 1400 ˚C for 30 min) for recrystallization was used in the current work. In spite of the fact the recrystallization microstructure observed in the present work (elongated grains coinciding with the original grain growth direction in size of approximately 30 μm) appears very similar to that in [58] viewing parallel to the grain growth direction, no favored texture was confirmed in the recrystallized matrix. This might be attributed to the different grain growth profiles during the deposition processing.

The most similar recrystallization behaviour of bulk CVD polycrystalline silicon to the current work was observed by Lall *et al.* [66]. The starting material was also semiconductor grade polycrystalline silicon bars grown by CVD and the metallographic examination of the as-received material reveals a similar microstructure to that in this study, in both radial and axial sections of the 'polylog'. According to their reports, the polycrystalline silicon was annealed at 1380 ˚C for 24 hours which resulted in a more uniform microstructure with the removal of the small grains. It was also claimed that no texture change occurred during the annealing which indicated no recrystallization. However, their claim was disputable since it was made merely on the basis of an

assumption since no texture measurement of the annealed material was actually conducted in their study. In addition, the microstructure upon a shorter annealing time was not investigated in their work, therefore there exists a possibility that the recrystallization might complete within a much shorter period of time with no further microstructure change upon prolonged annealing time. However, it remains unknown that how short the annealing time could be provided a temperature up to 1380 ˚C.

5.6.3 Recrystallization of polycrystalline silicon after deformation and annealing

The deformation and annealing of bulk polycrystalline silicon was studied relatively more comprehensively by previous researchers [50], [51], [54], [55], [57], [59], [61], [66]in the interests of assessing the feasibility of manufacturing silicon sheets for photovoltaic application using traditional hot rolling process (for detailed literature coverage see Chapter 1). Recrystallization in polycrystalline silicon was widely recognized after high temperature plastic deformation and subsequent annealing, which is analogous to the behaviour of metallic materials. Recrystallization is a useful means of obtaining grains of favourable sizes, configuration and crystalline perfection. It was reported that a high annealing temperature is required in order to recrystallize deformed silicon [61].

In the present work, plastic deformation of CVD grown polycrystalline silicon at 1150 ˚C with 10 % compression strain at a strain rate of 6.94 $x10^{-6}$ s^{-1} was achieved. The microstructure was only slightly altered during the deformation, with the introduction of an appreciable large number of inner grain sub-grain boundaries (Figure 5.24). No change in average grain size was observed. The average dislocation density was

increased from 1.0 x10^{12} m^{-2} to approximately 8.0 x10^{12} m^{-2} after deformation as measured by visual etch pit counting. TEM examination manifests a typical plastic deformation microstructure after compression, in the form of a complex dislocation network and sub-grain boundaries (Figure 5.27). Dislocations with Burgers vector of ½[110] and ½[$1\bar{1}0$] were present (Figure 5.28). Thermal annealing at 1400 ˚C for 15 min transferred 50 % of the deformed material into a second recrystallization microstructure, featuring large grains of several hundred microns size separated by relatively straight high angle grain boundaries (Figure 5.29). No preferred texture was revealed by EBSD. The average dislocation density was estimated as 5.0 x 10^{10} m^{-2} by etch pit counting. The nucleation of new grains in the midst of the boundary between two adjacent grains were also observed. A prolonged annealing at 1400 ˚C for 120 min lead to a complete second recrystallization, in both sections parallel and perpendicular to the compression axis.

Other work regarding as-cast 'Silso' polycrystalline silicon [64], with varying grain sizes between 150 µm and 750 µm, showed recrystallization during the course of annealing material previously deformed by both tensile and compressing pre-strain. Kinoshita and Champier [54], [61] conducted tensile tests at temperatures between 800 ˚C and 1050 ˚C with following heat treatment at around 1400 ˚C. External 13 % tensile strain at 950 ˚C and subsequent annealing at 1395 ˚C for 4.5 hours led to approximately 50 % of the deformed material recrystallized. The resultant recrystallized microstructure contains irregular grains in sizes ranging from 80 µm to 1.8 mm. The etch pit density in the recrystallized regions was estimated as between 10^{7} m^{-2} and 10^{8} m^{-2}, significantly lower than that of as-received materials, which was between 10^{10} m^{-2} and 10^{12} m^{-2}. It was found qualitatively that the recrystallization fraction is proportional to the initial

deformation and to the temperature and time of annealing. Further quantitative study demonstrated that the recrystallization of this cast polycrystalline silicon material requires a critical global strain of 7 % and local strain of 10 %, irrespective of the strain rates. These results are fairly comparable to those obtained in the present work even though different materials and experimental methods were used. The recrystallization of 'Silso' cast polycrystalline silicon deformed at 1050 ˚C by 10 % took approximately 10 days to complete at 1396 ˚C. In comparison, thermal annealing at 1396 ˚C only took 2 hours to achieve complete recrystallization of CVD polycrystalline silicon deformed at 1150 ˚C by 10 %. The differences in the cast and bulk polycrystalline silicon should be taken into consideration as the major determining factor. For as-cast polycrystalline silicon, the internal strain is insufficient to initiate recrystallization from the as-received state, therefore an additional strain is necessitated to produce the driving force for recrystallization. Conversely, there exists sufficient intrinsic internal strain in the CVD grown polycrystalline silicon therefore the recrystallization could take place just by thermal treatment. Even though the grown-in defect content in as-cast polycrystalline silicon could be as high as 10^{12} m^{-2}, it is still 2 orders of magnitude lower than that in the as-received CVD material (as measured in this work).

The study of Schins and Radelaar [59] was conducted on similar CVD polycrystalline silicon starting material as that in this work. They demonstrated that uniaxial tension of by 5 % strain at 1140 ˚C followed by a subsequent thermal treatment at 1390 ˚C induces recrystallization which yielded large grain size in order of 1 mm. Their material was subjected to pre-annealing at 1350 ˚C for 3 hours to obtain a recrystallized microstructure before the deformation. This pre-annealing time is considerably longer than the one used in the present work (1400 ˚C for 30 min). For sample deformed by 5

%, the time required for a complete post-deformation recrystallization at 1390 ˚C varied from 20 to 34 hours. Their deformation and annealing temperatures are approximately equivalent to the parameters used in the present work. The difference in total deformation strain induced (10 % in this work) might account for the distinctly longer annealing time required for a complete recrystallization in their study. Their TEM examination revealed a dislocation concentration of 2 $x10^{13}$ m^{-2} inside sub-grains in a polycrystalline silicon sample compressed by 30 % at 1270 ˚C. This value, however, is about an order of magnitude lower than the one obtained in this work (even with only 10 % total strain). Another difference lies in the texture change, whereby in their work the texture inherently changed from the original < 110 > into < 111 > after recrystallization during pre-annealing. Upon compression along the original < 110 > direction at 1120 ˚C and 1280 ˚C by up to 30% the fiber texture was turned into a < 110 > deformation texture parallel to the compression axis. This type of texture change was not observed in the present work.

Pratt *et al.* [50], [55], [57], [66] carried out plastic compression of CVD polysilicon at 1380 ˚C with various strain rates both along and normal to the < 110 > fibre orientation. They found that the recrystallization completed after 10 min annealing at 1380 ˚C when the sample was compressed perpendicular to the original < 110 > direction by 30 % at 1380 ˚C with a strain rate of 0.08 s^{-1}. This finding is, to a certain extent, of similar timescale to the second recrystallization behaviour observed in this work. However, they claimed that a secondary texture was introduced by the compression which contains < 110 > axis parallel to the compression axis and a < 111 > axis parallel to the original < 110 > fibre axis. It is worth noting that their starting polycrystalline silicon material was first subjected to a pre-annealing at 1380 ˚C for 20 min before

compression, however, the texture was never examined after the pre-annealing and the possibility of primary recrystallization was never taken into account. It was speculated from their preliminary results that grain growth occurred without texture change during annealing the as-received polycrystalline silicon at 1380 ˚C for 24 hours. Since it is already known by several other studies together with the current work that CVD polycrystalline silicon does recrystallize upon annealing at temperatures close to the melting point in the order of several minutes, their so-called deformation texture could as well just be the pre-annealing texture.

A maximum stored energy is required to obtain the most rapid recrystallization. It is not clear that the very slow deformation at 1150 ˚C in this work would compare to a much more rapid deformation process at temperature close to 1400 ˚C. It is possible that a higher dislocation density could be induced to make recrystallization faster.

5.7 Conclusions

In summary, the following conclusions can be drawn from the deformation and annealing of polycrystalline silicon in the present work:

- CVD grown semiconductor grade polycrystalline silicon by Siemens process comprises a stem-tree like microstructure, heavily textured with a sharp <110> fibre texture aligned with the grain growth direction. The material consists of large twin grains elongating in the grain growth direction and contains primarily Σ 3 and Σ 9 grain boundaries. The grain sizes vary from 3 ~ 30 μm in length and 1 ~ 3 μm in diameter.
- Annealing at 1400 ˚C for 30 min effectively recrystallized 90 % of the as-received material, yielding an average grain size of 30 μm. The recrystallized

microstructure has no texture and contains mainly of Σ 9 twin grain boundaries and high angle grain boundaries. Prolonged annealing has no significant influence on the microstructure.

- In the material pre-annealed at 1400 ˚C for 30 min, the un-recrystallized region contains densely spaced short dislocation arrays and intensive stacking faults. The dislocation segments are approximately 300 nm apart, lying in the < 211 > crystallographic direction. Most stacking faults are arranged along the < 110 > direction. The recrystallized region contains significantly lower concentration of defects, mainly stacking faults lying along the <110> orientation with associated partial dislocations.
- Compression at 1150 ˚C for 4 hours along the original grain growth direction induced a total 10 % strain into the polycrystalline material, with a maximum stress of 100 MPa and an average strain rate of 6.94 x 10^{-6} s^{-1}. The plastic deformation gave rise to an appreciable large number of sub-grain boundaries in grain interiors, without altering the overall grain microstructure. The average dislocation density was increased from approximately 1 x10^{12} m^{-2} before deformation to 8 x10^{12} m^{-2} by visual etch pit counting.
- Defect morphology assessed by TEM confirmed a typical plastic deformation microstructure of the as-deformed material, featuring complex dislocation network and sub-grain boundaries in the form of intensive dislocation segments. Dislocations with Burgers vector of ½ [110] and ½ [$1\bar{1}0$] were configured.
- Subsequently annealing at 1400 ˚C for 15 min led to 50 % of the deformed material being recrystallized into a second recrystallization microstructure with large grains of several hundred microns scale and relatively straight high angle

grain boundaries. The average dislocation density was estimated as 5 x 10^{10} m^{-2} by etch pit counting.

- The second recrystallization was completed by prolonged annealing at 1400 ˚C for 120 min, in both sections parallel and perpendicular to the compression axis.

The GND density evolution of the polycrystalline silicon during pre-annealing, after deformation and during subsequent annealing was statistically evaluated by quantitative HR-EBSD cross-correlation method. The responding results are presented and analysed in the following chapter.

Chapter 6

Quantitative analyses on the microstructural evolution and GND density distribution in deformed and annealed polycrystalline silicon by HR-EBSD

6.1 Introduction

It was found extremely challenging to extract critical information concerning dislocation densities by preferential etching, especially in the case of as-received polycrystalline silicon in which the dislocation density is so high that visually resolving overlapping etch pits is nearly impossible. In addition, the dislocation etch pit density exhibit large variations across the polycrystalline material, after hot plastic deformation and subsequent annealing process, as demonstrated in the previous chapter. This causes difficulties in assessing the average dislocation density.

The most widely used technique in dislocation configuration investigation (such as grain boundaries, stacking faults and twinning [226]), TEM, was also proven to be less applicable in quantitatively determining the overall dislocation density at large scale in the bulk polycrystalline silicon. Several limiting factors of TEM need to be emphasized. First of all, qualitative rather than quantitative TEM observations are often made which prohibits statistical dislocation density studies in polycrystals where a large number of microstructure variables have to be considered and a limited number of areas can be examined [227]. In addition, in order to produce a TEM foil with electron transparency, ultra-thin (0.1 ~ 4 μm) specimens must be fabricated. During the preparation, dislocations migrate towards the free surfaces and thus their structure and density may

be altered significantly from bulk materials due to image forces [226]. Furthermore, both etch pits and TEM studies have not focused on the role of grain to grain interaction in polycrystalline crystals presumably because of the morphology and orientations of the neighbouring grains are either not available or difficult to measure by these two techniques.

As stated in Chapter 1, the rapid development of automatic Electron Backscatter Diffraction (EBSD) technique in the past few decades have successfully obtained not only high spatial resolution but also high angular resolution [228]. With ~ 20nm attainable spatial resolution (depending on materials), ~ 0.005° attainable angular resolution [229], the HR-EBSD cross-correlation technique (an off-line image processing method) enables the evolution of stored GND arrangements to be mapped at high resolution on the mesoscopic scale where the influence of overall microstructure on dislocation distribution can be clearly identified. Henceforth the HR-EBSD technique is a very suitable method to investigate both the microstructure and the GND content evolution in polycrystalline silicon in as-received state, prior deformation annealing, post plastic deformation and post subsequent annealing state.

It is, however, crucial to emphasize that TEM reveals the total dislocations present in the bulk material, whereas preferential etching elucidates all dislocations that intersect with surface. These dislocations could possibly maintain either SSD or GND characters (detailed definitions see Chapter 1). On the other hand, HR-EBSD cross-correlation method only recovers existing GND content in the examined region, whose value theoretically is lower than the one determined by TEM and preferential etching technique, which should be the sum of both SSDs and GNDs.

The principle of HR-EBSD cross-correlation method was already depicted in Chapter 1 and the basic equipment set up and condition employed has been illustrated in Chapter 2. Fundamental theories and the history of EBSD have been comprehensively reviewed and highlighted by several authors [195], [196], [228], [230]. This Chapter focuses on presenting the utilization of HR-EBSD cross-correlation method to recover the Geometrically Necessary Dislocation (GND) density in characterization of the plastically deformed polycrystalline silicon. The statistical study of GND density distribution, variation and accumulation with respect to the annealing conditions are described in the following sections in detail.

6.2 Experimental method

From a set of preliminary experiments, it was found that using 4 x 4 binned level and 0.5μm step size provides an excellent combination of spatial and angular resolution (~ 0.03˚) and the associated GND density noise level was estimated as ~5.6 x 10^{12} m^{-2}, which proves to recover adequate information for cross-correlation-based EBSD measurements of stored GND density [231]. Binning is a process to combine charges contained in adjacent pixels on a CCD camera into a single pixel, as illustrated in Figure 6.1. Pixel binning maintains the benefits of increasing image acquisition rate and improving signal to noise ratio (SNR) however reducing the angular resolution of the EBSD detector. 4 x 4 binning level enables statistically representative maps to be recovered with a reasonable scanning time and 0.5 μm step allows detailed dislocation structure to be revealed in the material, especially in the annealed microstructure where the average grain size is ~ 30 μm. EBSD maps with higher angular resolution were obtained by 1 x 1 binning at the expense of significantly longer collection time. The

corresponding GND density noise level of 1 x1 binning at 0.5 µm step size was calculated as approximately 2.8 x 10^{12} m^{-2}.

A series of EBSD scans were conducted on the polycrystalline samples at as-received state, pre-annealing state, as-deformed state and post-annealing state, respectively, in sections both parallel and perpendicular to the grain growth direction. For Face A (section parallel to the original grain growth direction and compression axis, see illustration in Chapter 5), 4 x 4 binning level and 0.5 µm step size were used. In comparison, as regards to Face B (section perpendicular to the original grain growth direction and compression axis), 1 x 1 binning level and 0.5 µm step size were employed. EBSD maps in size of 100 µm x 100 µm were collected in both sections. It is worth noting that although the collection conditions in different sections are different however in individual section the condition remains constant, henceforth the data calculated were directly comparable.

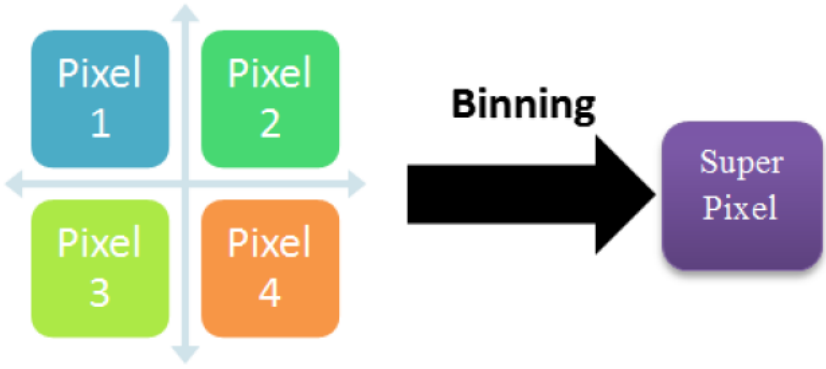


Figure 6.1. Schematic diagram of 2x2 binning process. The charge collected from pixel 1 to 4 are summed into the single super pixel (image courtesy to [8]).

6.3 Experimental results and discussion

6.3.1 GND density evolution of the as-received polycrystalline silicon (Face A) upon pre-deformation annealing by HR-EBSD

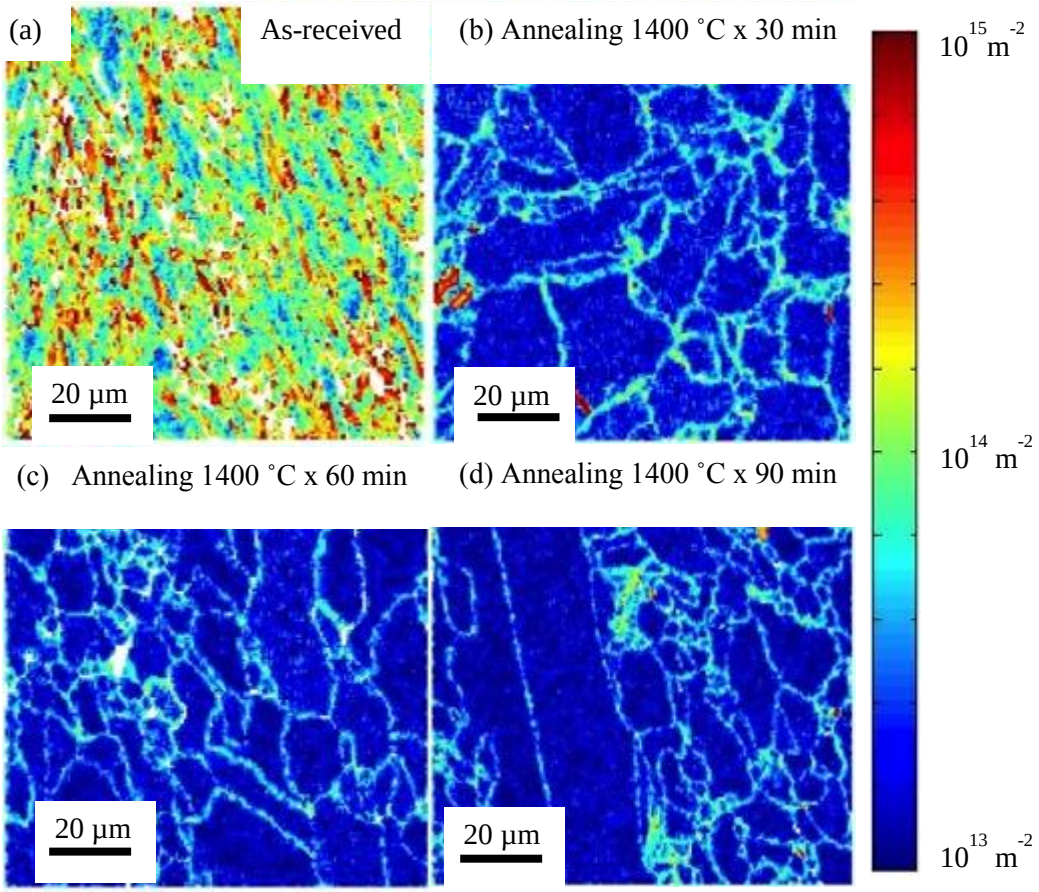


Figure 6.2. 100 µm x 100 µm HR-EBSD recovered spatial GND distribution maps of the as-received polycrystalline silicon (Face A) annealed at 1400 ˚C for (a) 0 min; (b) 30min; (c) 60min and (d) 90min, respectively. The scale bar is 20 µm and the used step size is 0.5 µm. The colour bar shows GND density in m^{-2} scale. White regions correspond to the rejected points by cross-correlation quality analysis with PH > 0.2 and MAE < 0.01 rads. The grain growth direction is vertical in all maps.

The lower bound estimates of stored GND density maps of section parallel to the grain growth direction at progressively increased annealing time at 1400˚C is shown in Figure 6.2. This series of data was collected from a JOEL JSM-840A using a tungsten filament cathode electron source with an applied voltage of 20 kV and a probe current of ~ 30 nA. The step size used is 0.5 μm and binning level is 4 x 4, and the collection time for each map was approximately 2 hours. The colour map scales used in this section is from 10^{13} m^{-2} to 10^{15} m^{-2} for the purpose of revealing the GND content to the optimal extent.

Visual assessment of Figure 6.2 (a) suggests that the as-received polycrystalline silicon is highly defected with a large amount of red GND density 'hot' spots, corresponding to local high dislocation content regions. There are relatively very few 'cold' spots present, representing low dislocation content area. It is clear that the dynamical recrystallization process during annealing at 1400 ˚C for 30 min not only remarkably altered the microstructural features (as depicted in Chapter 5) but also significantly decreased the quantitative GND density patterning, as shown in Figure 6.2 (b). The GND map displays an overall lower GND content with rare high dislocation density regions, presumably surviving from the as-received state. Further annealing at 1400 ˚C for 6 0min and 90 min did not induce further noticeable change in terms of GND content, as depicted in Figure 6.2 (c) and (d). It is worth noting that the residual high dislocation density regions from the as-received state in the GND map remains after annealing for 90 min at 1400 ˚C, in good agreement with the microstructure evolution revealed by preferential etching method in Chapter 5. It is likely that the white regions filtered by the thresholds criteria (PH > 0.2 and MAE < 0.01 rads) contain very high GND contents (resulting in severely deteriorated diffraction patterns). Removal of data in this way may provide a small bias in the statistics towards lower GND densities.

The overall evolution of the GND distributions without considering the location where dislocations are stored can be observed in the histograms presented in Figure 6.3, in which the GND density frequency is plotted as a function of $\log_{10}\rho_{GND}$. The general shape of the $\log_{10}\rho_{GND}$ histograms is very similar at each imposed annealing state, regardless of the difference in annealing time. Despite the distribution shape similarity, the average stored GND content clearly decreases. Assuming a log-normal form for the GND density distributions it is then sensible to report the geometric mean GND density which Figure 6.4 shows as a function of annealing time. Numerically from a mean value of 1.2×10^{14} m^{-2} at the as-received state rapidly decreased to 2.34×10^{13} m^{-2} after annealing at 1400 ˚C for 30 min, and then the rate of decrease slowed for further annealing, to 1.82×10^{13} m^{-2} after 60 min annealing and finally to 1.73×10^{13} m^{-2} after 90 min.

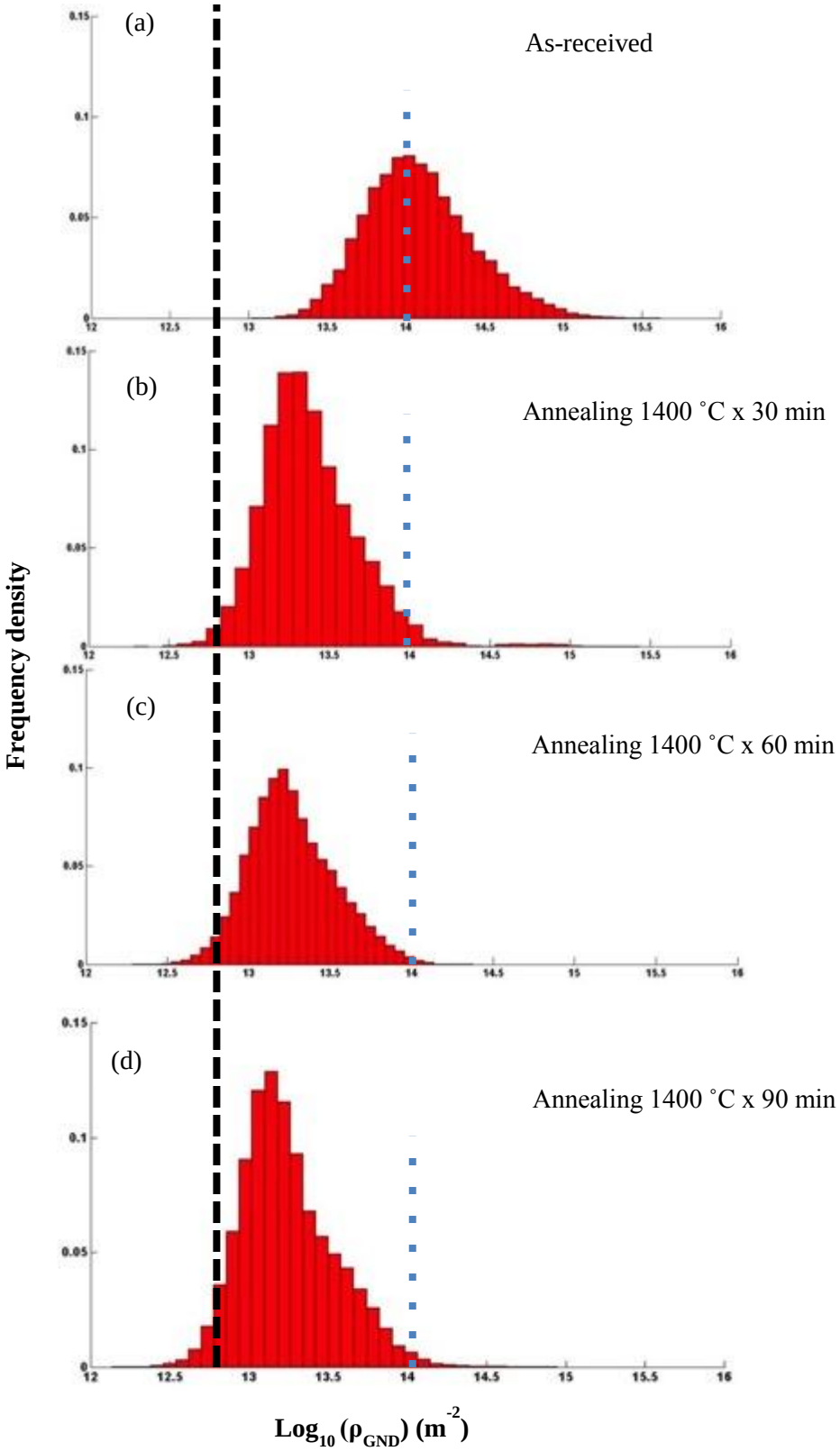


Figure 6.3. Histograms show the evolution of GND density distribution as increasing annealing time from the as-received state at 1400 ˚C for (a) 0min (as-received); (b) 30min; (c) 60min and (d) 90min. The blue dash lines mark the comparison line at GND density of 10^{14} m^{-2}. The black dash line denotes the sensitivity limit at 4 x 4 binning and 0.5 μm step size.

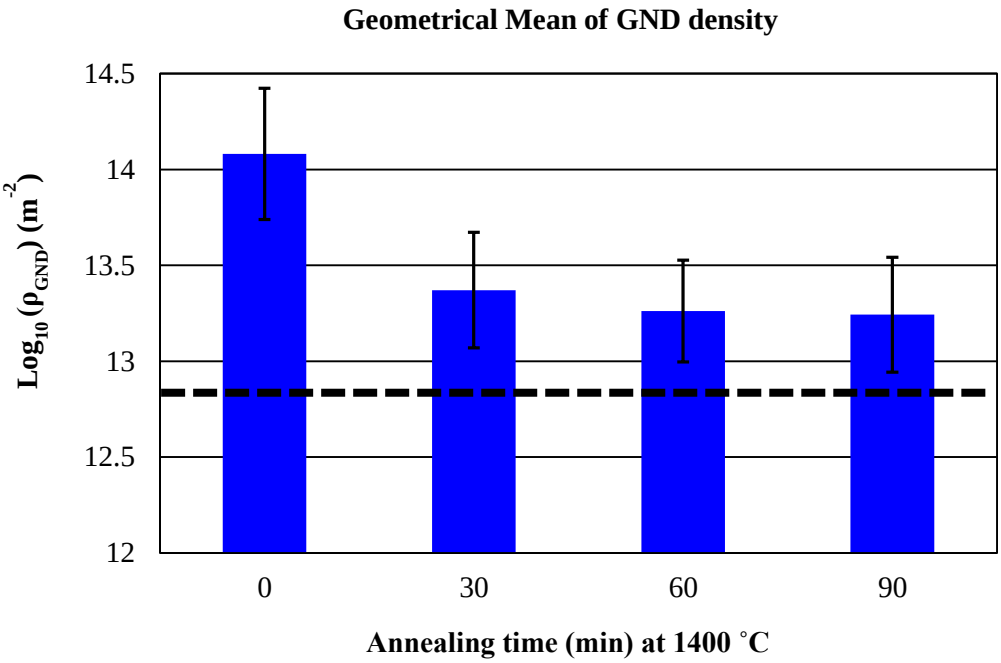


Figure 6.4 shows the relation of the imposed annealing time at 1400 ˚C from the as-received state and the geometrical mean of map-overall GND density. The black dash line denotes the sensitivity limit at 4 x 4 binning and 0.5 μm step size. The error bars represent standard deviation of the associated $\log\rho_{GND}$ distribution.

The grain size effect on the GND density was also explored in these samples in the as-received state and after pre-annealing at 1400 ˚C for 30 min, 60 min and 90 min, respectively. The corresponding diagrams were shown in Figure 6.5. Grain shapes were assumed to be circular therefore the grain diameter D was determined by counting the total area and finding the equivalent circle diameter using equation $D = 2 \times \sqrt{Area/\pi}$. The grain averaged GND density was also calculated for each grain. Grains along the edges of EBSD maps were excluded from analysis. For each map, the dataset with range of 0 ~ 15 μm was grouped into 5 ~ 10 bins and data in each bin were sorted in descending order. The points at 10 %, 50 % and 90 % of total points in each bin were identified and plotted as green, red and yellow dot lines which are used to describe the distribution and trends of datasets. The centile lines were only plotted when a minimum

20 grains was found within a bin. Figure 6.5 (a) for the as-received material, shows that the average GND density decrease very slightly as a function of the grain diameter, however, this is only made visible by the centile lines and there is considerable scatter covering orders of magnitude changes in GND density from grain to grain at a given size. The GND density is very high throughout the whole sample surface and the distribution is relatively homogeneous regardless of the small variation in grain size. On the contrary, the pre-annealed samples in general manifest a strong and approximately reverse non-linear correlation between the grain averaged GND density and grain diameter, with higher GND densities tending to be present in smaller grains. The relationship could be described by the following equation:

$$< \rho GND > \propto \frac{A}{D^{-\delta}} \qquad \text{Equation 6.1}$$

where A represents the grain area, D is the grain diameter and δ is a correction factor. However, since the D in the annealed material only varies over a factor of 10, it is difficult to judge the factor δ. These pre-annealed samples contain residual regions from the as-received state which are primarily composed of small grains with significantly higher GND density than the recrystallized region. The presence of such un-recrystallized debris possibly contribute to the high GND density plot in small grain diameter range. The annealed samples all show a trend that regions containing larger grains tend to have lower GND densities. The grain to grain variation in GND density is significantly smaller for these larger grains.

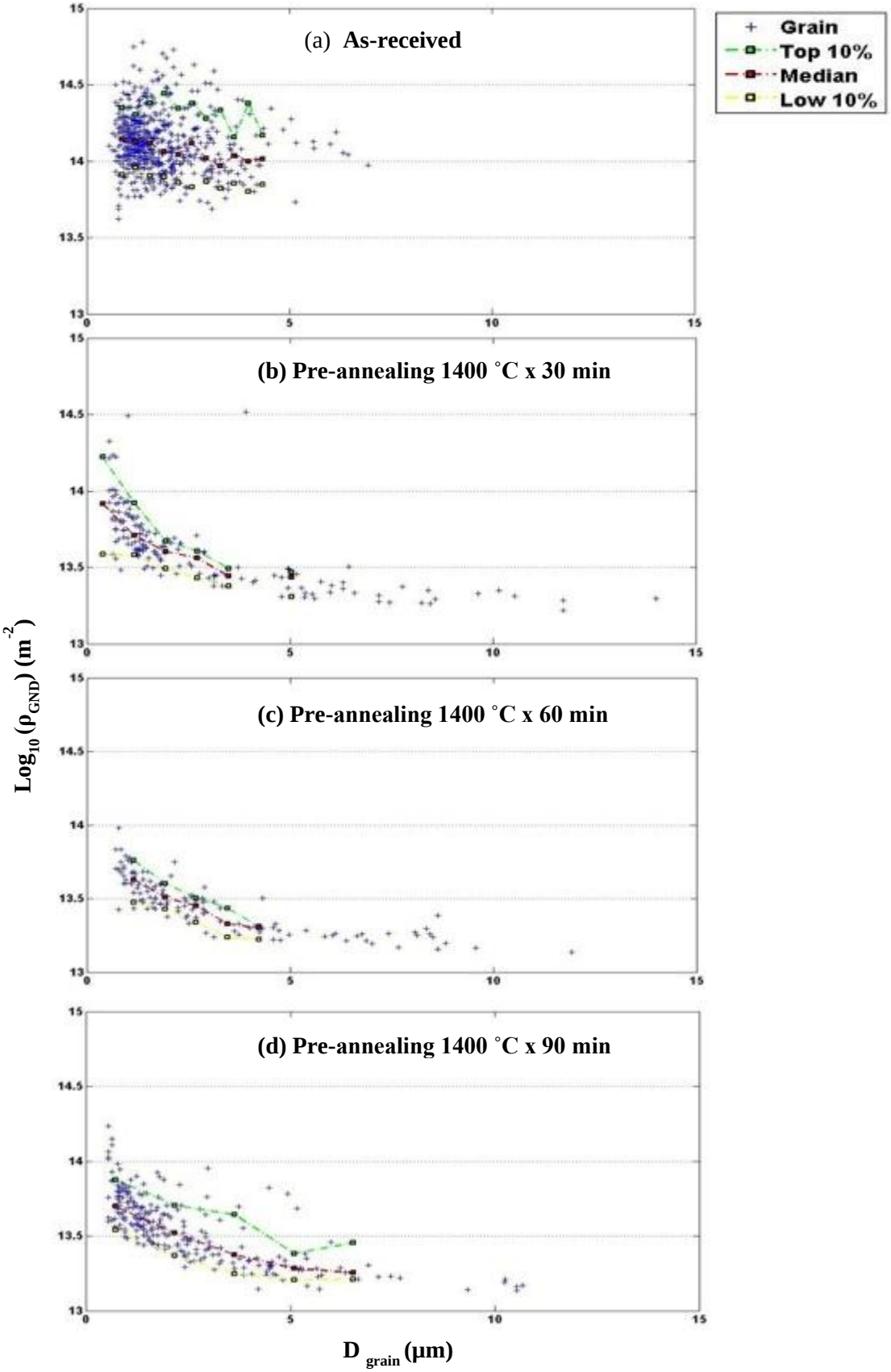


Figure 6.5. Scatter plot of grain average GND density as a function of grain diameters as increasing annealing time at 1400 ˚C from as-received state for (a) 0min (as-received); (b) 30 min; (c) 60 min and (d) 90 min. Marked are lines indicating the 10 %, 50 % and 90 % points in the distributions.

6.3.2 GND density evolution of as-received polycrystalline silicon (Face A) upon high temperature plastic deformation and subsequent annealing by HR-EBSD

As stated in the previous chapter, increasing the annealing time beyond 30min did not result in noticeable alterations in dislocation density nor microstructure of the recrystallized polycrystalline material. The optimal pre-annealing condition prior to plastic deformation was therefore determined as 1400 ˚C for 30 min, so to minimise the thermal budget. 100 µm x 100 µm EBSD maps were collected from cross sections parallel to the initial grain growth direction in polycrystalline samples before and after 10% plastic deformation at 1150 ˚C. The associated maps of spatial variating GND content recovered from cross-correlation EBSD method are shown in Figure 6.6.

Direct visual qualitative inspection of Figure 6.6 shows that significant heterogeneous deformation microstructures were developed during plastic deformation. It is clear that plastic deformation induces extra GND content in the microstructure. With high angle grain boundaries (misorientation between adjacent grains >10˚) highlighted, the relation between the high dislocation density features and high angle grain boundaries is made visually assessable at the microscopic scale. It is evident that before plastic deformation most high dislocation density features generally coincide with high angle grain boundaries, apart from some extremely high GND density features, corresponding to approximately 10^{15} m^{-2} GND density, presumably debris from the high dislocation density as-received state. Most of such features are linear and correspond to low angle sub-grain boundaries.

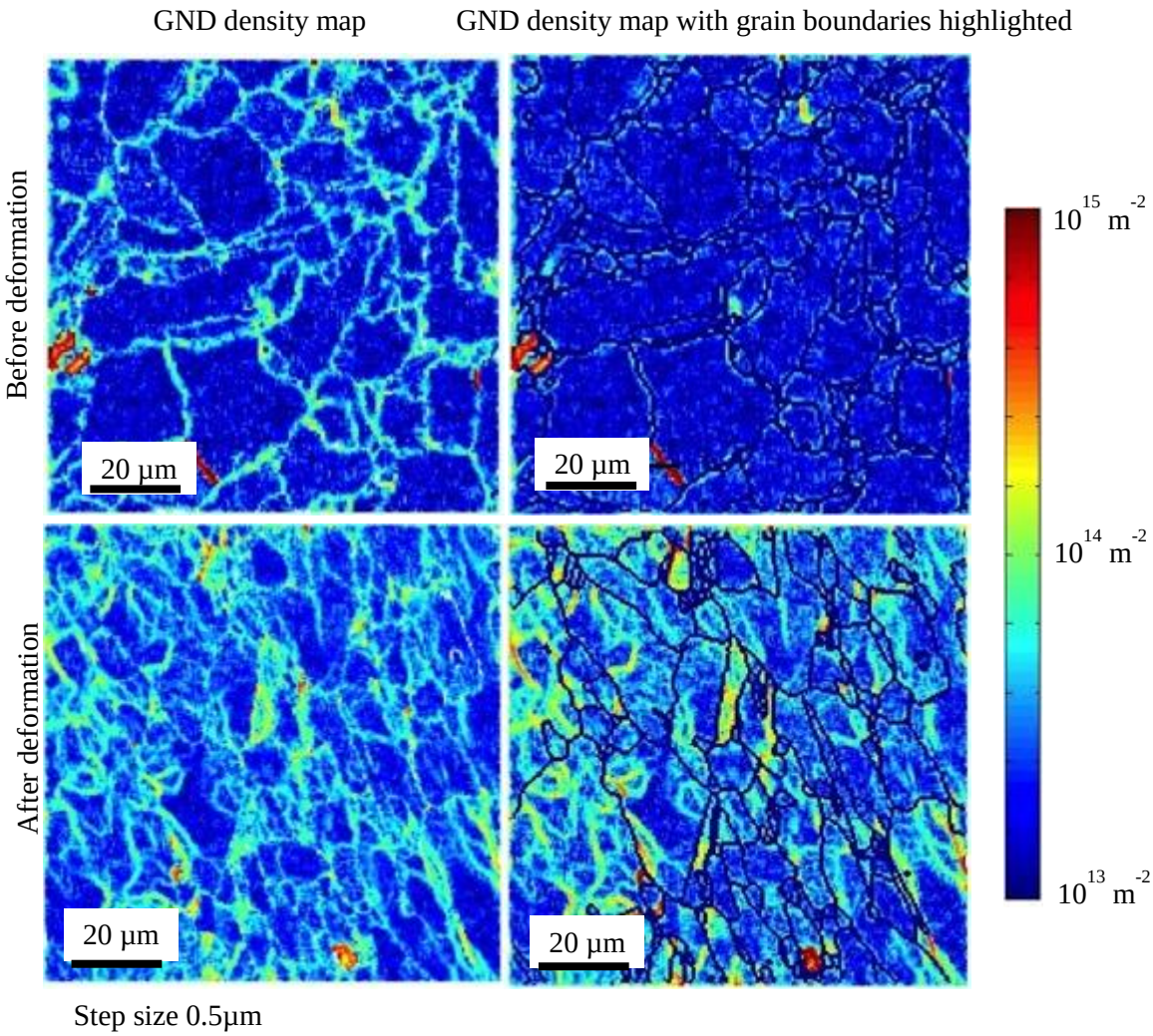


Figure 6.6. GND density maps illustrating the stored dislocation content before and after plastic deformation at 1150 ˚C by 10 % strain, with dark blue lines represent grain boundaries with minimum misorientation angle of 10˚ between adjoined pixels. The initial grain growth direction and the compression axis are both vertical in these maps.

Sub-grain boundaries at misorientations just below the threshold 10˚ (0.17 rad) arbitrarily used to define grain boundaries correspond to a GND density of 9.0 x 10^{14} m^{-2} ($\frac{\theta}{G \cdot \Delta x}$) at the 0.5 µm step size used in these maps. Sub-grain boundaries at the limiting GND density and lower can be seen in the undeformed sample. After plastic deformation, the GND network not only coincides with high angle grain boundaries, but also features the formation of continuous curved band-like dislocation structures

containing high dislocation content within the grain interiors at very few micron size and some long 'string-like' sub-grain features span across a grain from one grain boundary to another. Most of these bands are oriented in a range between 35 ~ 45˚ to the loading axis. These dislocation band patterns are observed in almost all grains. The GND density stored in dislocation band walls is estimated as ~10^{14} m^{-2}, whereas in band structure interiors the GND density is estimated as 5.0 x10^{13} m^{-2}. It is also worth noting that the formation of high dislocation content is rather heterogeneous, varying from grain to grain. However, in general these dislocations accumulate near grain boundaries rather than grain interiors.

The polycrystalline silicon deformed by 10 % plastic strain was then subjected to subsequent high temperature annealing at 1400 ˚C. As described in the previous chapter, the material started to develop a secondary recrystallization texture upon subsequent annealing for 15 min and the secondary recrystallization process was observed to complete within 120 min. In addition, individual low GND density recrystallized grains were observed to grow from the as-deformed texture in annealed samples. The representative areas from non-secondary recrystallized regions, partially secondary recrystallized regions and completely secondary recrystallized regions were selected and the corresponding GND information was recovered using HR-EBSD cross-correlation method. As indicated in Figure 6.7, even within the area where secondary recrystallization did not occur after subsequent annealing, it is clear that the general GND content decreased considerably from the as-deformed state. The overall amount of high dislocation density features within grain interiors decreased noticeably, resulting in relatively low density GND content grains of similar size to those in the as-deformed sample. Furthermore, the secondary recrystallization completely altered the general

microstructure morphology. The high dislocation density features in grain interiors almost entirely disappeared in this newly formed microstructure where the mean grain size is more than ~ 70 μm in diameter and the quantitative GND content map manifests a distinctively low dislocation density across the specimen, numerically ~ 3.2 x 10^{12} m^{-2}. This GND density is very close to the noise floor of the HR-EBSD measurement with the present settings and the real dislocation density may be lower than this in these regions. In addition, it is interesting to note that the partially secondary recrystallized region consists of individual recrystallized grains of low GND density surrounded by high GND density area. Presumably this is due to the large driving force required for recrystallization was sufficiently provided by significant local residual strain.

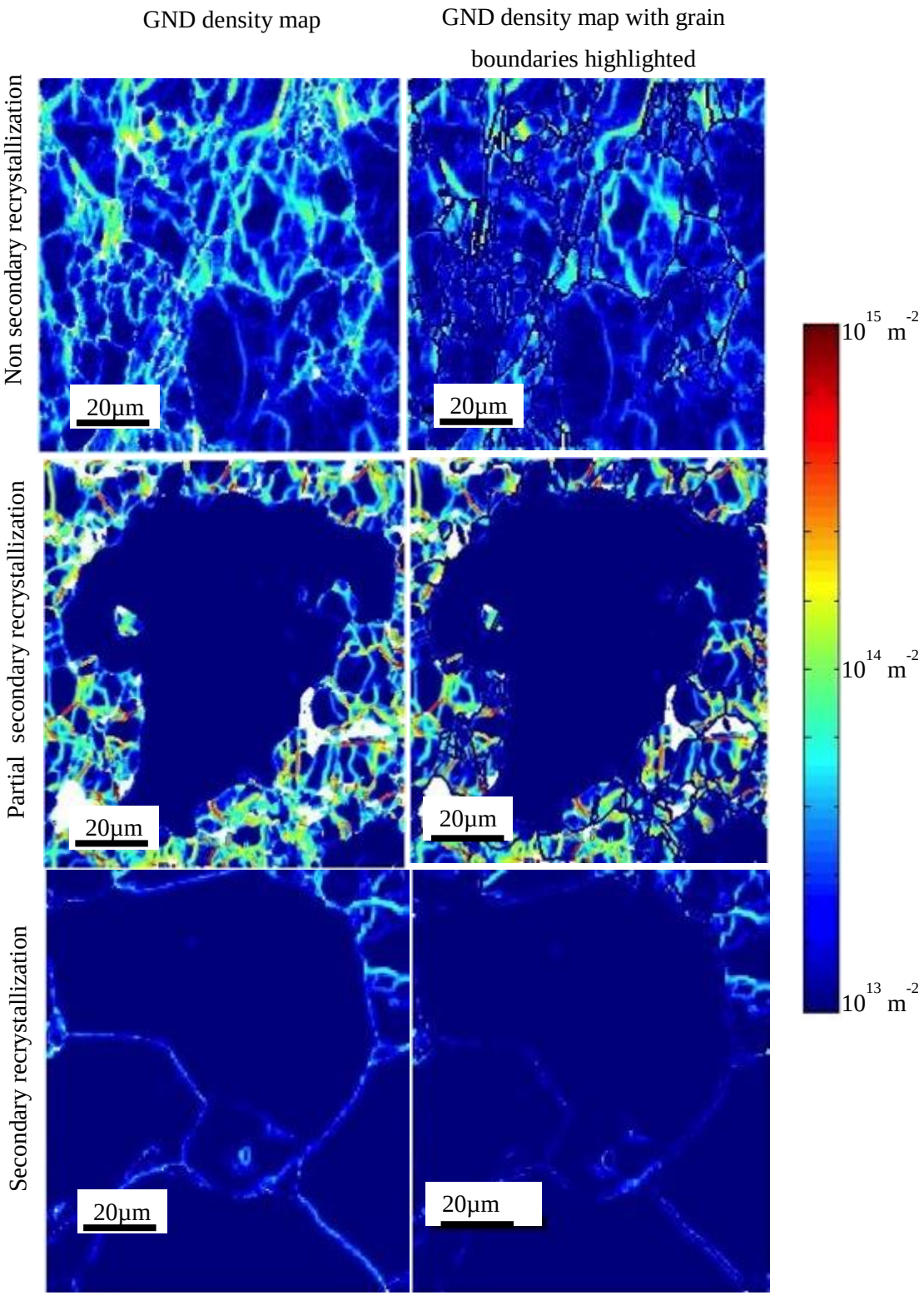


Figure 6.7 shows the GND content distribution maps exacted from regions of non-secondary recrystallized, partially secondary recrystallized and completely secondary recrystallized after subsequent annealing at 1400 ˚C for 15 min (Face A), with dark blue lines represent grain boundaries with minimum misorientation angle of 10˚ between adjoined pixels.

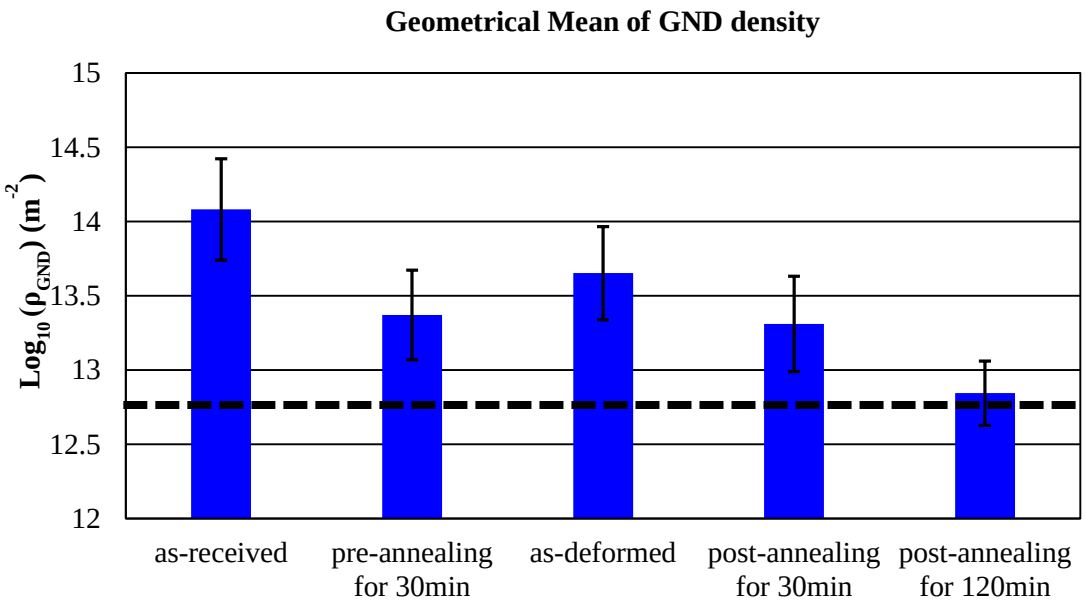


Figure 6.8. The average GND density evolution during pre-annealing at 1400 ˚C for 30 min, as-deformed at 1150 ˚C and subsequent annealing process at 1400 ˚C for 30 min and 120 min. The black dash line denotes the sensitivity limit at 4 x 4 binning and 0.5 µm step size. The error bars represent standard deviation of GND density distribution.

As shown in Figure 6.8, the overall GND density varies along the individual steps of the thermo-mechanical treatment. Recrystallization during pre-annealing step witnessed a remarkable GND density decrease while hot plastic deformation induces a marked increase in dislocation density. The GND density was further reduced by subsequent annealing treatment due to both dislocation annihilation and formation of secondary recrystallized microstructure. The lowest GND density was obtained in the completely secondarily recrystallized region which is two orders of magnitude lower than the as-received state, and is at a GND density very close to the noise floor of the measurements which may be limiting.

6.3.3 GND density evolution of as-received polycrystalline silicon (Face B) upon pre-deformation annealing by HR-EBSD

For the purpose of providing more comprehensive information of the statistical evolution of stored GND content with respect to annealing and the subsequent deformation process, quantitative GND analysis was also conducted on the cross-section perpendicular to the grain growth direction (Face B).

100 μm x 100 μm EBSD maps were scanned from samples of as-received state, after pre-deformation annealing at 1400 ˚C for 30 min and 60 min, respectively. The associated GND information was then determined by cross-correlation method, and is shown in Figure 6.9 (a)-(c). It is worth noting that due to the microscope access limitations, this series of data was obtained from a Field Emission-SEM JOEL JSEM-6500F. The step size was maintained at 0.5 μm and binning level is 1 x 1, hence the collection time for each map was approximately 14 hours. The colour map scales used in this section is from $10^{12}\,m^{-2}$ to $10^{15}\,m^{-2}$ for the purpose of revealing the GND content to the optimal extent. The noise floor for the GND density is somewhat lower, at 2.8 x $10^{12}\,m^{-2}$, than for the maps on Face A.

As shown in Figure 6.9 (a), the spatial GND content of the as-received state recovered is distinctly high (mostly beyond $10^{14}\,m^{-2}$) across the whole scanned area and the GND density distribution is also significantly heterogeneous. 90 % of the polycrystalline material recrystallized after 30 min annealing at 1400 ˚C and the associated recovered GND map indicates a low dislocation content microstructure, with very few residual high dislocation density areas as the debris of the as-received state (Figure 6.9b). The GND content morphology is broadly similar to the one recovered from the cross-section

parallel to the grain growth direction (Figure 6.2b), however the grain sections are more equiaxed in this section. Prolonged annealing for 60 min at 1400 ˚C did not seem to alter the dislocation content morphology to a noticeable extent, as visually demonstrated by Figure 6.9 (c). With high angle grain boundaries highlighted (see Figure 6.9d), it is noticeable that the high dislocation density features tend to coincide with the grain boundaries, apart from some debris from the as-received state. The grain interiors generally contain very small numbers of GNDs compared to the grain boundary vicinity.

The histograms of Figure 6.10 show that the GND density distribution of the as-received sample manifests a Gaussian-like distribution when plotted as a function of $\log_{10}(\rho_{GND})$, indicating a log-normal type distribution. Upon pre-annealing at 1400 ˚C for 30min, the mean GND value was found to shift very significantly towards the lower density side. However two major peaks coexist in the same histogram, corresponding to the recrystallized region and un-recrystallized debris. It is of interest to note that the lower GND density peak seems to fit well with the expectation of the noise floor. The histogram of pre-annealing for 60 min display similar shape and mean value. The evolution of mean GND density value with respect to the pre-annealing time is shown in Figure 6.11, which displays an evident decrease upon annealing for 30 min however prolonged annealing for 60 min only slightly further reduced the GND density.

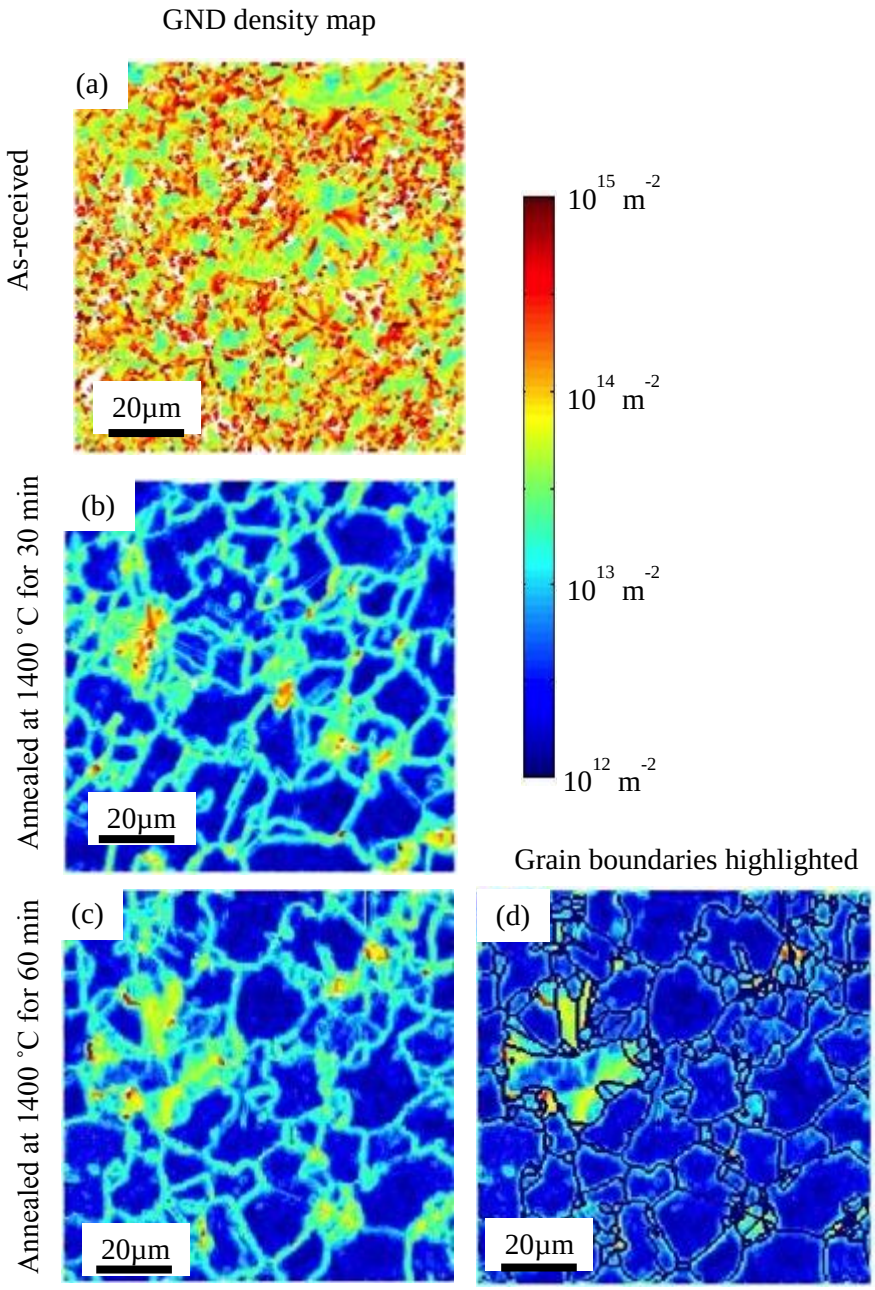


Figure 6.9. 100 µm x 100 µm HR-EBSD recovered spatial GND distribution maps of as-received polycrystalline silicon (Face B) annealed at 1400 ˚C for (a) 0 min; (b) 30min; (c) 60min; (d) a separate map with high angle grain boundaries indicated as dark blue lines of the sample annealed for 60min. The scanning step size is 0.5 µm. The colour bar shows GND density in m^{-2} scale. White regions correspond to the rejected points by cross-correlation quality analysis with PH > 0.2 and MAE < 0.01 rads.

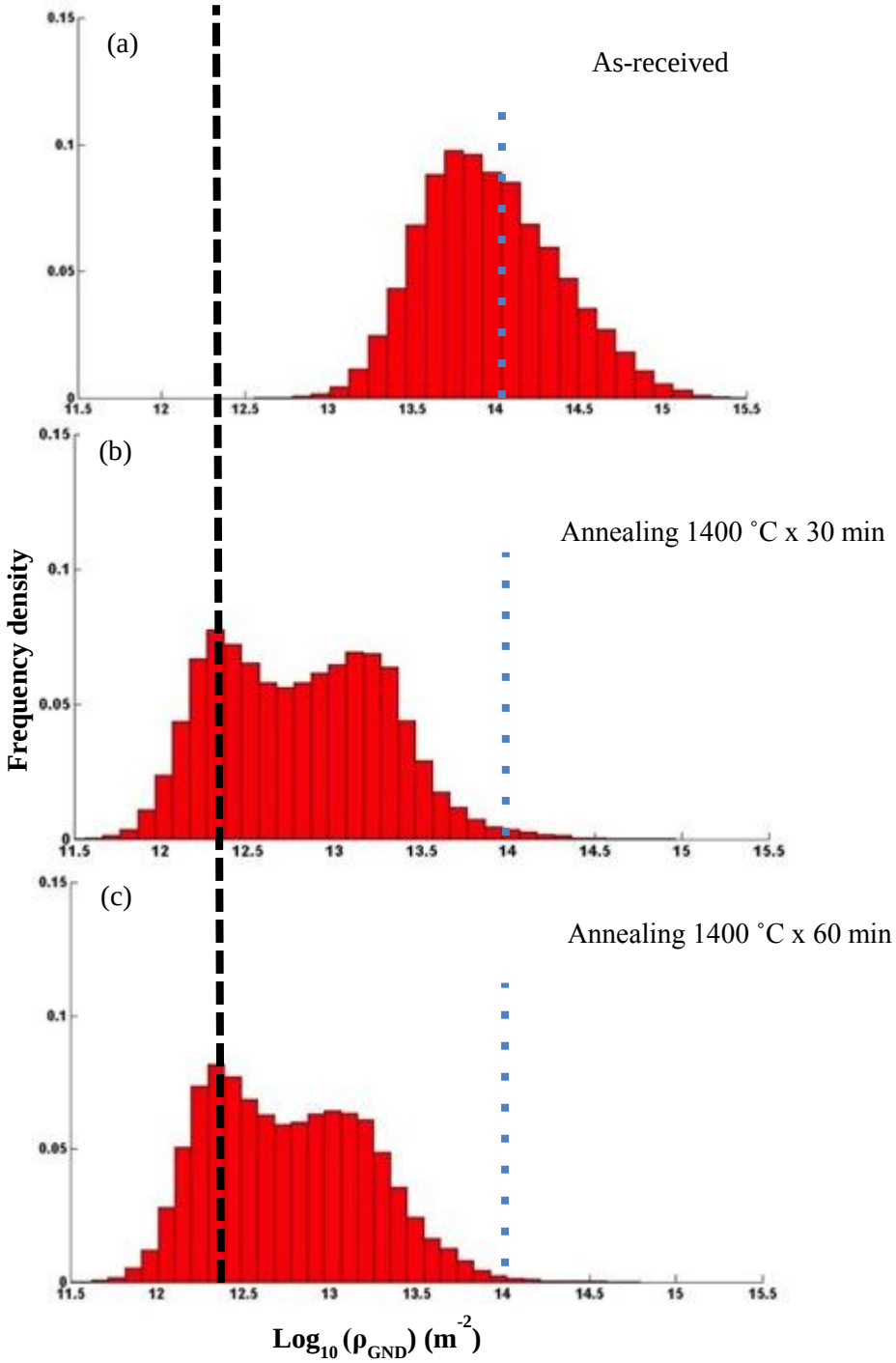


Figure 6.10. Histograms reveal the evolution of GND density distribution of polycrystalline silicon (Face B) for increasing annealing time at 1400 ˚C from as-received state (a) 0 min (as-received); (b) 30 min; (c) 60 min. The black dash line denotes the sensitivity limit at 1 x 1 binning and 0.5 μm step size. The blue dash lines mark the comparison line at GND density of 10^{14} m^{-2}.

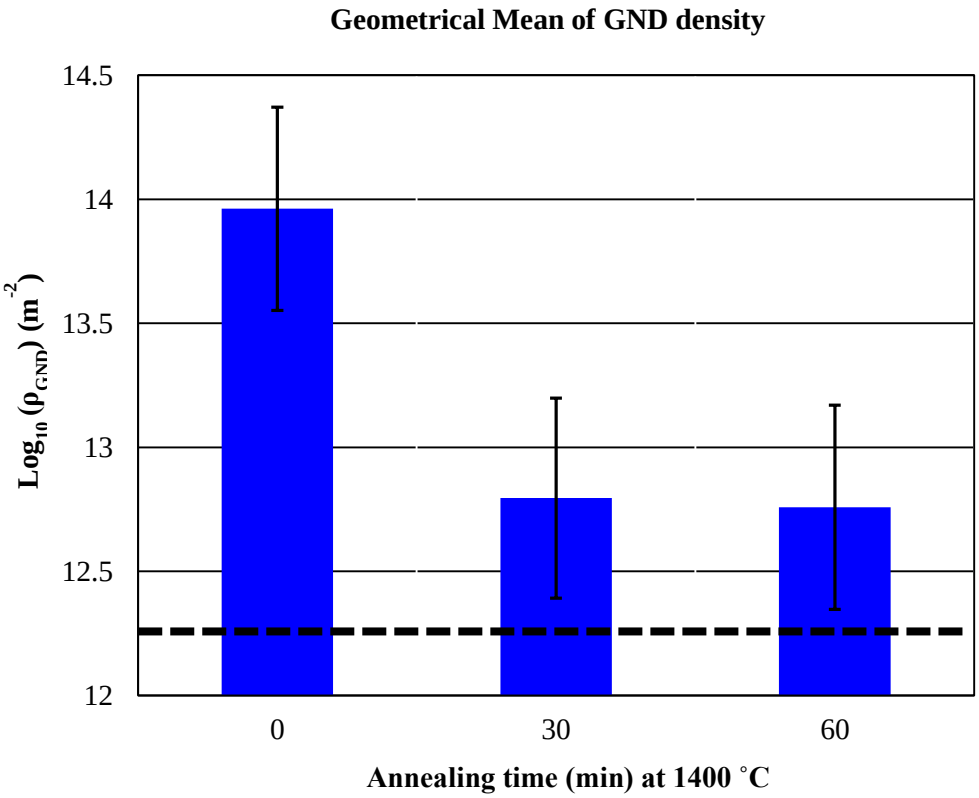


Figure 6.11. The relation of the imposed annealing time at 1400 ˚C from as-received state and the geometrical mean of map-overall GND density. The black dash line denotes the sensitivity limit at 1 x 1 binning and 0.5 µm step size. The error bars represent standard deviation of GND density distribution.

It is, however, possible that if the average GND density of the sample pre-annealed for 60min lies below the noise level, the results obtained by HR-EBSD cross-correlation method would essentially show the noise level rather than the genuine GND density. This is verified by etch pits counting the dislocation density in the recrystallized grains of samples pre-annealed at 1400˚C for 30 min and 60 min (Face B), see Chapter 5 Section 5.3.1. Preferential etching examinations of these regions reveal that the recrystallized grains in both samples show similar low dislocation etch pits density, approximately 2.0 x 10^{11} m^{-2}.

6.3.4 GND density evolution of as-received polycrystalline silicon (Face B) upon high temperature plastic deformation and subsequent annealing by HR-EBSD

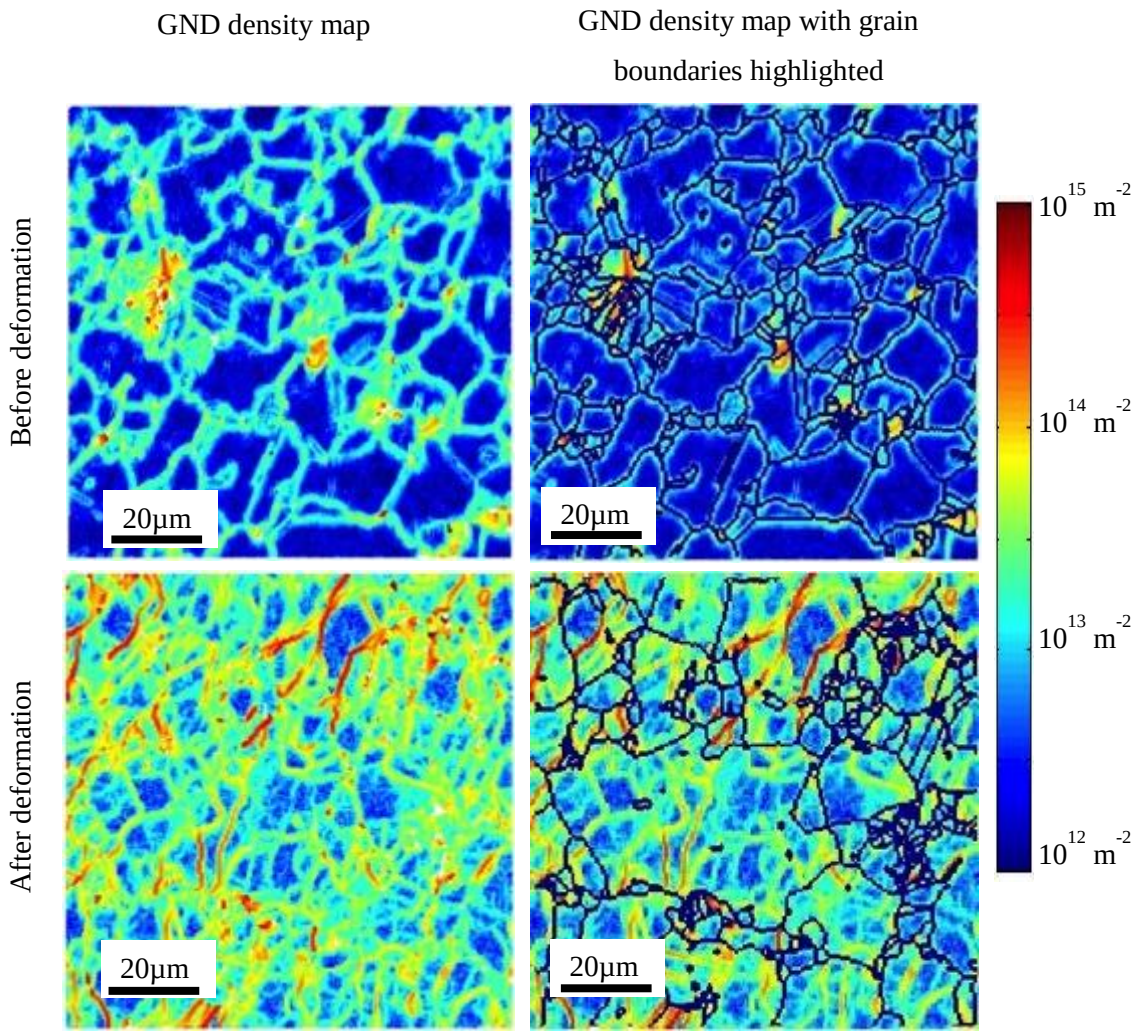


Figure 6.12. Spatial GND density maps illustrates the stored dislocation content before and after plastic deformation at 1150 ˚C by 10 % strain, with dark blue lines representing grain boundaries with minimum misorientation angle of 10˚ between adjoined pixels. The initial grain growth direction and the compression axis are both outwards in these maps.

Similar to the GND density evolution after plastic deformation in Face A, the deformation microstructure obtained in Face B evidently reveals the induction of extra GND content by plastic deformation from direct visual qualitative assessment in Figure

6.12. It is clear that plastic deformation induces extra GND content into the microstructure, especially with high angle grain boundaries highlighted. The overall GND density appears to be raised by one order of magnitude comparing to the sample before plastic deformation. Subsequent annealing examination indicated similar microstructure evolution as Face A. Henceforth the relevant results are not included in this subsection.

6.4 Direct comparison of HR-EBSD cross-correlation method and preferential etching on the determination of dislocation density in partially recrystallized polycrystalline silicon

A specific area containing an individual recrystallized grain in the sample (Face A) annealed at 1400 ˚C for 15 min post plastic deformation was selected to provide direct comparison between HR-EBSD cross-correlation method and conventional preferential etching technique. Such a sample contains both high and low dislocation density regions which could cover a large comparison range. The specimen was firstly polished by standard procedure for EBSD mapping, after the EBSD scan the sample was submerged in Sirtl etch for 30 s followed by examination in SEM. The EBSD mapping was undertaken on FEG-SEM at 0.5 μm step size and 1 x 1 binning of the EBSD detector.

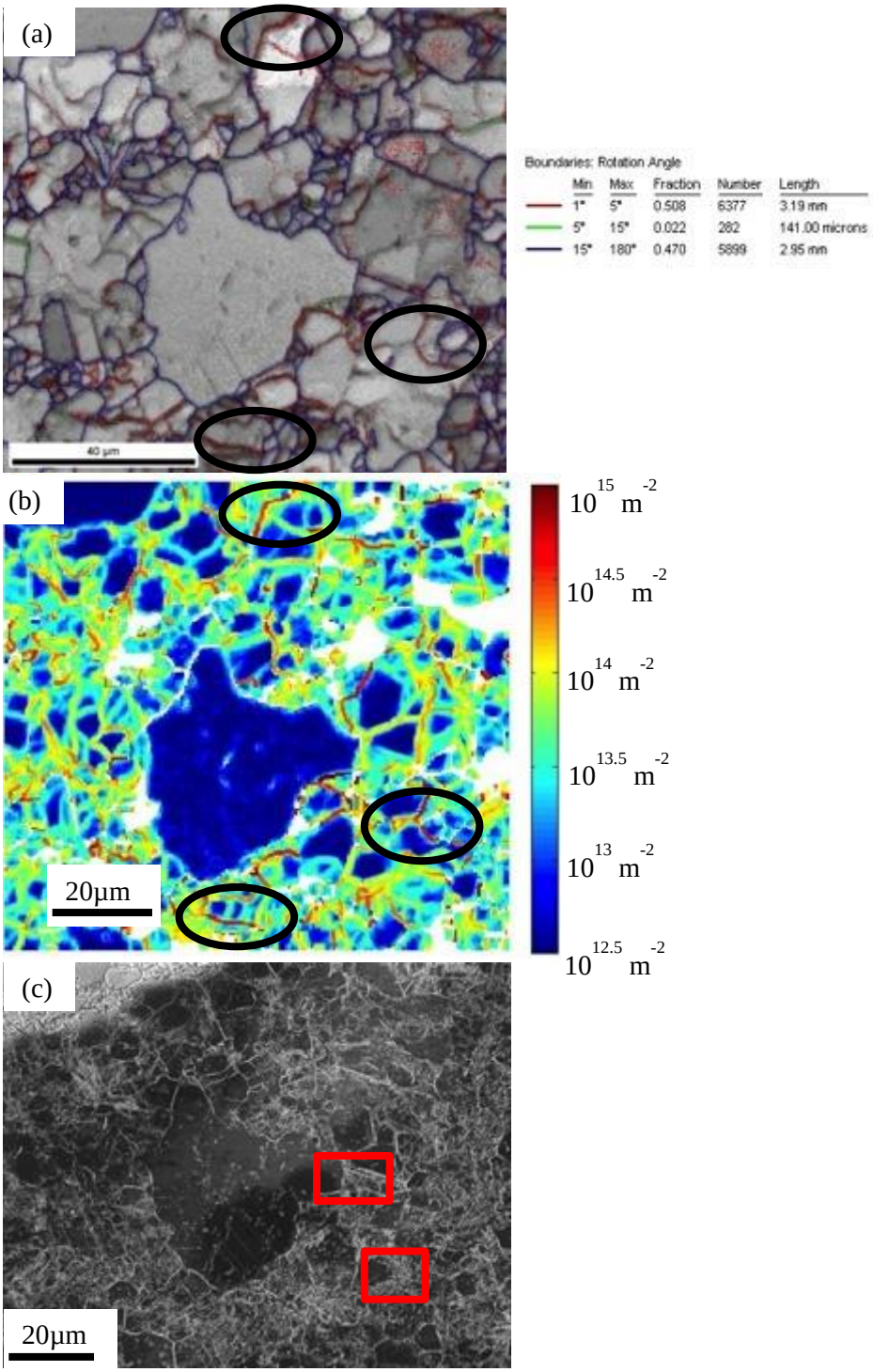


Figure 6.13. Representative partial secondary recrystallized region with one single individual recrystallized grain from Face A deformed and subsequently annealed at 1400 ˚C for 15 min: (a) Image quality map with grain boundary type marked as red, green and blue lines; (b) Spatial GND density map; (c) SEM micrograph post preferential etching by Sirtl etch solution for 30s. Black circles in (a) highlighted the regions containing low angle grain boundaries (misorientations between 1˚ and 5˚) and the corresponding area in spatial GND content map recovered by HR-EBSD cross-correlation method. Red rectangles marked in (c) indicate regions shown in higher magnification in Figure 6.14.

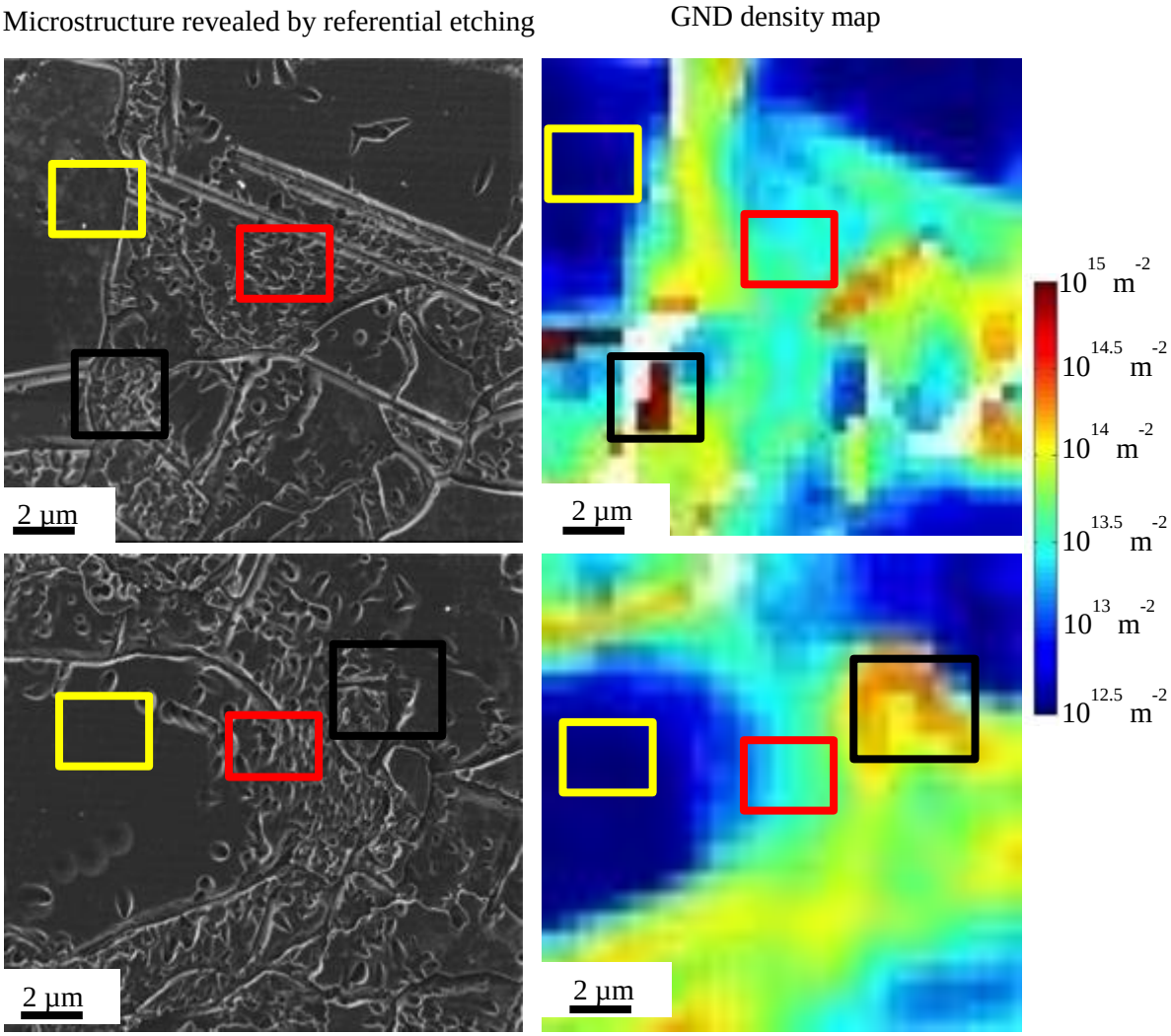


Figure 6.14. High magnification SEM micrographs and corresponding GND density maps of the same region, with specific low GND density area highlighted by yellow rectangles, medium GND density area marked by red rectangles and high GND density features marked by black rectangles.

The image quality map with grain boundary type highlighted (as shown in Figure 6.13a) reveals the newly formed recrystallized grain is separated from the surrounding microstructure by high angle grain boundaries. The un-recrystallized regions contain large amount of grain boundaries with rotation less than 5˚.

The recrystallized grain and an area in the surrounding microstructure were then selected for detailed comparison at higher magnification, as shown in Figure 6.14. Red

rectangles highlight the medium GND density area, etch pits counting reveals the dislocation density in the order of $10^{13}m^{-2}$ which is approximately in the same order of magnitude as indicated by cross-correlation method. However, while examining the low GND density regions (enclosed by the yellow rectangles), an average GND density of approximately $10^{12.5}\ m^{-2}$ was generated the calculated GND density map, which deviate considerably from the value obtained by etch pits counting which is virtually less than $10^{11}\ m^{-2}$. In regions showing high GND density in the EBSD data (black rectangles) the features are typically linear with densities up to ~$10^{15}\ m^{-2}$, and correspond to sub-grain boundaries which etch as continuous features in the 30s Sirtl etch. In order to gain a deeper insight of the mean dislocation density, a thin foil specimen was fabricated using FIB from the recrystallized grain and examined in TEM. The foil before and after lift-out is illustrated in Figure 6.15, with twin grains marked by red arrows. TEM bright field micrograph reveals a low dislocation content microstructure and the dislocation density estimated is in the order of $10^{11}m^{-2}$ which is consistent with the value obtained by etch pits counting. The numerical dislocation densities measured by HR-EBSD, etch pit counting and TEM from representative regions are shown in Table 6.1.

Table 6.1. Direct comparison of dislocation densities measured by HR-EBSD cross-correlation method, etch pit counting and TEM

	Low dislocation density	Medium dislocation density	High dislocation density
GND measured by HR-EBSD cross-correlation method	$10^{12.5}\ m^{-2}$	$10^{13}\ m^{-2}$	$10^{15}\ m^{-2}$

Etch pit counting	Less than 10^{11} m^{-2}	10^{13} m^{-2}	Subgrain boundaries
TEM	10^{11} m^{-2}	Nil	Nil

The probable explanation of the significantly higher GND density recovered by cross-correlation method is the lower bound GND content noise level, which was estimated as ~$2.8x10^{12}$ m^{-2} [207]as stated earlier in the present chapter. The cross-correlation method fails to reveal the genuine GND content and is inapplicable to assess GND density content when it is lower than the noise level. This is the case within the recrystallized grains in the present samples.

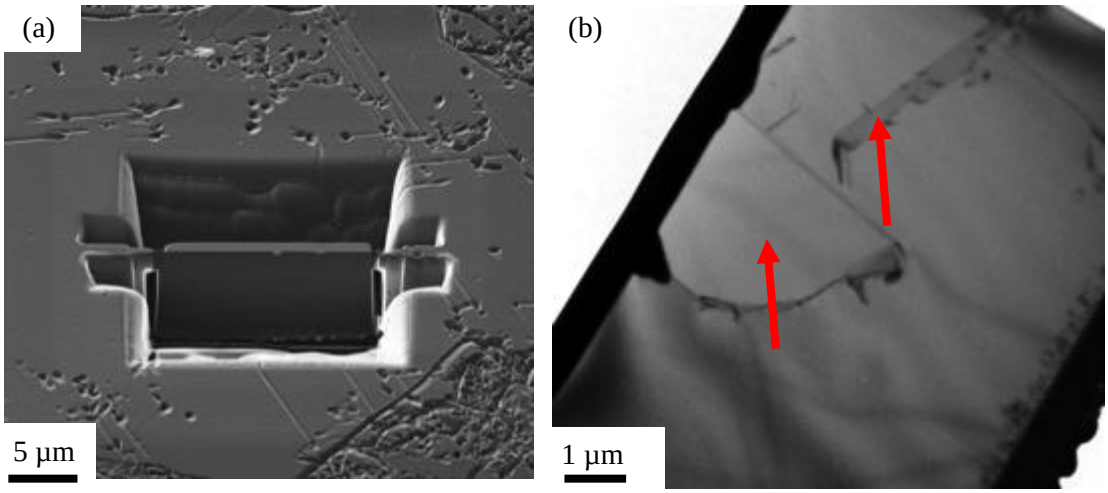


Figure 6.15. (a) TEM specimen fabricated from the recrystallized region by FIB lift-out technique; (b) TEM bright field image taken using (000) spot near [111] zone axis. Red arrows mark twin grains.

6.5 Investigation of the effect of polishing process on the GND density

It is well accepted that mechanical polishing introduces surface damage, in the form of dislocations, which can affect the corresponding GND content recovered by HR-EBSD cross-correlation method. Therefore a control experiment was conducted to assess the effect of polishing technique used in the present work.

Two pieces of p-type dislocation free Czochralski single crystalline silicon (sc-Si) wafer samples were prepared, in the size of real polycrystalline silicon sample (10 mm x10 mm) to maximally reproduce the polishing procedure. One piece of silicon wafer sample was selected and polished sequentially using 6μm and 1μm diamond paste before the final polishing step by colloidal silica solution (Syton liquid). Examination under optical microscope confirmed that all visible surface damage was removed after the complete polishing process. The other piece of silicon wafer sample functioned as the control sample on which no polishing treatment was conducted. Both samples then underwent EBSD scanning on JEOL JSM-6500F microscope using the same conditions as the polycrystalline silicon samples. EBSD maps of 20 μm x20 μm were scanned using binning level 1 x 1 and step size 0.5 μm, therefore approximately 1680 data points were collected in each map. The GND densities of both samples were subsequently recovered by cross-correlation method. The histograms of GND density distribution of both samples are shown in Figure 6.16.

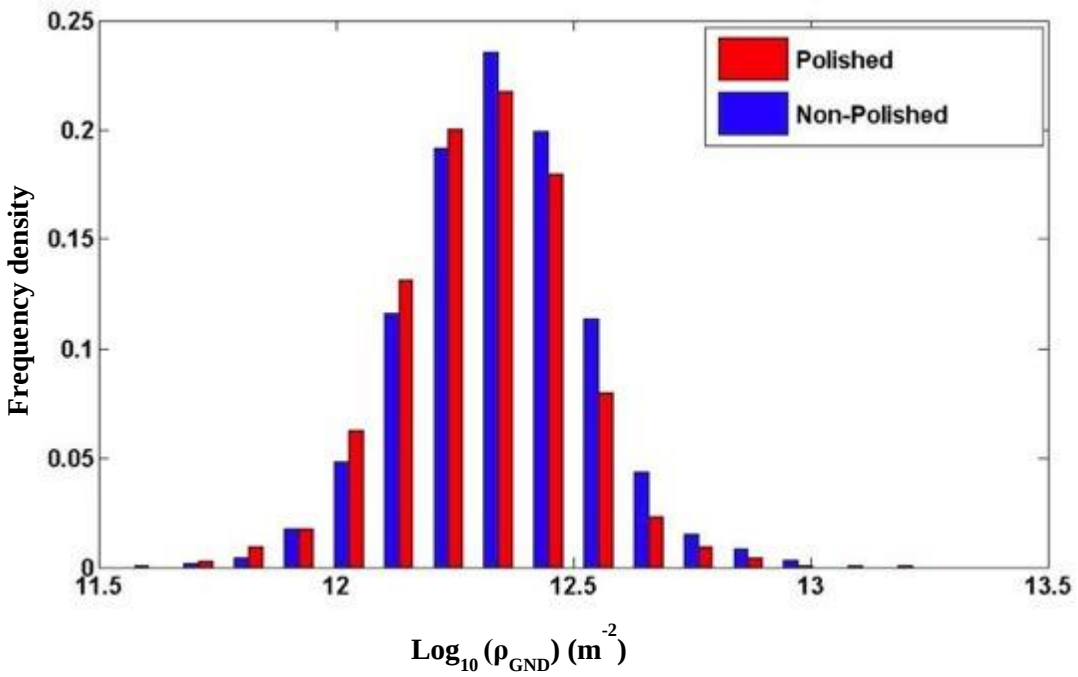


Figure 6.16. Histograms of GND density distribution of polished sc-Si sample and non-polished dislocation-free sc-Si samples.

The mean GND density value of unpolished sc-Si sample is $10^{12.38}$ m^{-2}, whereas the corresponding value of polished sc-Si sample is $10^{12.36}$ m^{-2}. It is known that the unpolished silicon sample is essentially dislocation free. The GND density value calculated by cross-correlation method therefore refers to the noise level of the specific scanning conditions selected and equipment utilized. The histogram of unpolished sc-Si also coincides well with the lower GND density peak in the histograms of Figure 6.10 (b) and (c), which suggests the left peak in those histograms is caused by the noise level. By comparing the mean GND density value of polished sc-Si with the one of unpolished sc-Si, it is clear that polishing process employed in the present work does not introduce excessive dislocations beyond the detection limit of HR-EBSD cross-correlation method, henceforth it is confident to claim that the GND density values of polycrystalline silicon obtained by this method are genuine.

6.6 Conclusions

HR-EBSD cross-correlation technique has been proven effective for statistically investigating the evolution of both microstructure and GND content of polycrystalline silicon samples prior and post hot plastic deformation and subsequent annealing. Lower bound GND density maps for representative areas of 100 µm x100 µm have been generated from each sample. For sections parallel to the initial grain growth direction and compression axis (Face A), fast pattern capture with 4 x 4 pattern binning and step size 0.5µm were used. This binning level is likely to obtain a noise level of ~ 5.6 x 10^{12} m^{-2}. Sections perpendicular to the initial grain growth direction and compression axis (Face B) were mapped at 1 x 1 pattern binning and step size 0.5 µm were selected for which a noise level of ~$10^{12.38}$ m^{-2} was established. The noise levels are remarkably lower than the average GND density recovered from the as-received state and as-deformed state but not the secondary recrystallized regions in the subsequently annealed samples.

The following conclusions can be drawn:

- The as-received polycrystalline silicon has an average GND density beyond 10^{14} m^{-2} in both sections parallel and perpendicular to the initial grain growth direction, as quantitatively recovered by HR-EBSD cross-correlation method. A large amount of red GND density 'hot' spots, referring to local high GND content regions beyond $10^{15}m^{-2}$, were observed in both sections.
- Pre-annealing at 1400 ˚C for 30 min not only profoundly altered the microstructure but also significantly reduced the statistical GND density to approximately 10^{13} m^{-2}. However, prolonged annealing did not seem to further

decrease the GND density noticeably. Most high GND density features generally coincide with high angle grain boundaries in the pre-annealed sample.

- Plastic deformation at 1150 ˚C by 10 % strain produced continuous curved 'string-like' high GND content structures within the grain interiors, presumably in the nature of sub-grain boundaries which are essentially dislocation arrays. These high GND density features form dislocation band patterns. The GND density stored in dislocation bands is estimated as ~ 10^{14} m^{-2} whereas the inner band regions have an approximate GND density of 5 x 10^{13} m^{-2}.
- Subsequent annealing at 1400 ˚C for 15 min post plastic deformation facilitated secondly recrystallization from the as-deformed state. The average GND density of the secondary recrystallized regions was measured as ~ $10^{12.5}$ m^{-2}, which is close to the noise level. The real dislocation density in these secondarily recrystallized regions may be lower.
- Direction comparison of HR-EBSD method and preferential etching was conducted on a partial secondary recrystallized region from the sample post-annealed at 1400 ˚C for 15 min. The GND density value and etch pits revealed by preferential etching from the high GND density (noticeably beyond the noise level) un-recrystallized regions are in good agreement. On the other hand, in the low GND density recrystallized grains preferential etching obtained an etch pits density below 10^{11} m^{-2} whereas the HR-EBSD cross-correlation method assessed a GND density of $10^{12.5}$ m^{-2}. The HR-EBSD method failed to reveal the genuine GND content in the secondary recrystallized grains which contain GND density lower than the noise level.

- Control experiment of polished dislocation free sc-Si verified that the polishing process selected in the present work did not introduce excessive GND density beyond the noise level.

The next chapter will present the electrical properties investigation of the deformed and post-annealed sample with applied gettering and passivation process.

Chapter 7

Investigation of the electrical properties of deformed and annealed polycrystalline silicon after gettering and passivation

7.1 Introduction

Inspired by previous studies of deformation of silicon at elevated temperatures [50], [51], [57], [66] , this work was initiated to revisit the hot compression of polycrystalline silicon. In contrast to earlier work, the deformation was performed in a clean environment using very high purity components to minimize contamination. The ultimate aspiration is to produce silicon sheets for photovoltaic applications using such hot compressed silicon. Therefore it is of vital importance to evaluate the electrical properties of the silicon material obtained in this approach. Gettering is a technique to remove or relocate harmful metallic impurities, whereas passivation is a process to inactivate defects. Both are standard procedures commonly integrated in modern solar cell fabrication and enhance electrical performance, and so were applied to the deformed and annealed polycrystalline silicon materials in this work (for detailed literature review see Sections 1.4 and 1.5). Minority carrier lifetime, as an effective indication of carrier diffusion length, is probably the most important figure of merit for solar grade silicon. In this work minority carrier lifetime is measured on the polycrystalline sample produced (see Section 2.12 for a description of the lifetime measurement technique).

The deformation and annealing experiments of polycrystalline silicon together with investigation of microstructural evolution over the corresponding processing steps are described in Chapter 5 and Chapter 6. Gettering and passivation were subsequently applied to the deformed (at 1150 ˚C by 10 %) and post-annealed (at 1400 ˚C for 120 min) polycrystalline silicon, for the first time. Details of such treatments employed in this work and the trend of measured minority carrier lifetime after each processing step are described and the possible explanations of this trend and related physical mechanisms such as surface recombination and trapping effects are discussed in this chapter.

7.2 Gettering and passivation processing

The recombination of minority charge carriers at defects can limit the overall conversion efficiency of photovoltaic solar cells. It has been widely recognized that the minority carrier recombination activity is closely related to structural defects and impurities present in the crystal. The dominant minority carrier lifetime limiting defects in polycrystalline silicon are grain boundaries and intra-granular defects (*i.e.* dislocations and micro-defects) decorated by harmful metallic impurities [146]–[151], [232]. An effective method to remove the unfavorable metal impurities is ***gettering*** [69], [168]–[174]. The specific gettering process used in this work is phosphorus diffusion gettering (PDG) using $POCl_3$ as the gaseous source [173]. During the PDG process, a heavily doped layer of phosphorus is deposited on the sample surface and impurities diffuse out of the bulk of the sample into the phosphorus layer via various potential mechanisms (see Section 1.4).

In addition, non-saturated bond defects, present at surfaces and interfaces in silicon material, also play a detrimental role in the electrical performance by introducing a large density of intermediate band-gap energy levels at which unwanted recombination of photo-generated carriers occur. This can be a major limiting factor in cell efficiency. These bond defects, however, can be electrically passivated to some extent [184]. Two passivation schemes are employed in this work, namely a hydrogen bulk passivation (H-passivation) and silicon nitride (SiNx) surface passivation. During H-passivation, a H plasma was created to produce H ions. These positively charged H ions rapidly diffuse into the specimen bulk and attach to non-saturated dangling bonds, resulting in the removal of their inner band energy states[233]. The experimental procedure including thermal profiles used in this work is described as follows:

(1). The polycrystalline silicon sample obtained by uniaxial compression at 1150 ˚C by 10 % measured approximately 15 mm x 15 mm. This was mechanically sawn into slices which were approximately 1.2 mm thick to produce sample of sufficient dimensions for the QSS-PC lifetime tester used. The sample was subsequently encapsulated in a clean quartz ampule and sealed in Argon ambient and annealed at 1400 ˚C for 120 min (Stage I). The sample was slowly cooled down to 200 ˚C by approximately 4 to 5 ˚C min^{-1} and then to the room temperature by 1 to 2 ˚C·min^{-1}. Minority carrier lifetime was measured after annealing. The sample was subsequently subjected to a series of passivation and gettering processes

(2). First of all, bulk hydrogen passivation was applied to the sample at 350 ˚C for 1 hour in an Oxford Instruments PlasmaLab 80+ PECVD system and the corresponding minority carrier lifetime was measured (Stage II). The passivation temperature was set to 350 ˚C with pure ammonia gas (NH_3) at a flow rate of 100 sccm (detailed experiment

setting see [234]). The processing time was selected as 1 hour as a preliminary pioneering experimental attempt. Since the sample was placed horizontally in the chamber only the top surface was exposed to the gas flow. Lifetime measurements were conducted with the passivated side up as well as with the passivated side down.

(3).When the first 1 hour H-passivation was found effectively to improve the bulk minority carrier lifetime, another hour of hydrogen in-diffusion was applied to the sample with the same surface up as the first step under the same conditions. Effective minority carrier lifetime was measured (Stage III). However, as shown later, the second 1 hour H-passivation treatment was not effective in further improving the measured lifetime, so no further H-passivation steps were applied.

(4). In the next step, the silicon sample was subjected to phosphorus diffusion gettering (PDG). The gettering was conducted by Mr Abu Siddique at Tetreon ®. The sample was loaded on a SiC boat horizontally in the furnace. $POCl_3$ in the gas stream flowed over the top sample surface for 20 min at 875 ˚C. According to Mr. Siddique, this step deposited a ~30 nm thick layer of rich phosphorus silicate glass (PSG) on the sample surface and formed a heavily doped thin emitter (approximately 200 to 250 nm) in the silicon. The sample was turned over and the same treatment was applied to the other surface. Upon the completion of the diffusion steps, the sample was cooled down to 800 ˚C in approximately 10 min in a small amount of oxygen flow. After an isothermal treatment at 800 ˚C for 25 min in nitrogen ambient, the sample was quenched to 300 ˚C in approximately 10s. The emitters fabricated in the sample were subsequently removed by planar etch which removed approximately 10 µm from both sides.

(5). SiNx surface passivation was then applied to the sample at 350 ˚C in the Oxford Instruments (OI) PlasmaLab 80+ PECVD system. A 70±5 nm thick silicon nitride layer was deposited in 4 min onto both side of the sample using a gas mixture of silane/nitrogen (5% SiH_4/95%N_2-400 sccm), ammonia (NH_3-20 sccm) and nitrogen (N_2-600 sccm) as precursor gas. The chamber pressure was 650 mTorr. The passivation was undertaken by Mr George Martins. The associated minority carrier lifetime was measured both before (Stage IV) and after the removal of the SiNx layers by HF (Stage V). The processing steps are summarised in Table 7.1.

Table 7.1. Series of processes applied to the single sample studied with QSS-PC lifetime measurements.

Stage	***Process***
Stage I	Deformation at 1150 ˚C by 10 % and subsequent annealing at 1400 ˚C for 120 min. Sliced into thinner sample.
Stage II	1 hour H-passivation at 350 ˚C
Stage III	Additional 1 hour (i.e. 2 hour total) H-passivation at 350 ˚C
Stage IV	$POCl_3$ gettering and SiNx surface passivation
Stage V	SiNx layer removed from Stage IV

7.3 Experimental results

7.3.1 Minority carrier lifetime of polycrystalline silicon

Effective minority carrier lifetime of the silicon sample was measured after each step using the QSS-PC technique (see Section 2.12). These measurements were mostly

conducted by Dr J. D. Murphy at University of Warwick. It is noted that the optical constant used for lifetime measurements was generally 0.7, but was 0.9 for the measurement of Stage IV. The optical constant is necessary for determining the light absorption into the sample in the QSS-PC mode. Thus the higher value accounts for the higher absorption in the SiNx cases as it is an anti-reflection coating. $POCl_3$ gettering and SiNx surface passivation were applied to both surfaces of the sample (arbitrarily denoted as the top side and bottom side), whereas H-passivation was only applied to the top surface. Minority carrier lifetime tests were conducted on both surfaces, except that only the top side was measured at Stage I. The obtained apparent minority carrier lifetime τ subscript as a function of excess minority carrier concentration with either sample side up is plotted in Figure 7.1 and Figure 7.2, respectively. The measured minority carrier lifetime (at the injection level of 1.0×10^{12} cm^{-3}) at each stage from the top side and the bottom side is compared quantitatively and depicted in Figure 7.3. The measured excess carrier lifetime with either sample side up of Stage IV and Stage V is plotted at a zoomed scale in Figure 7.4.

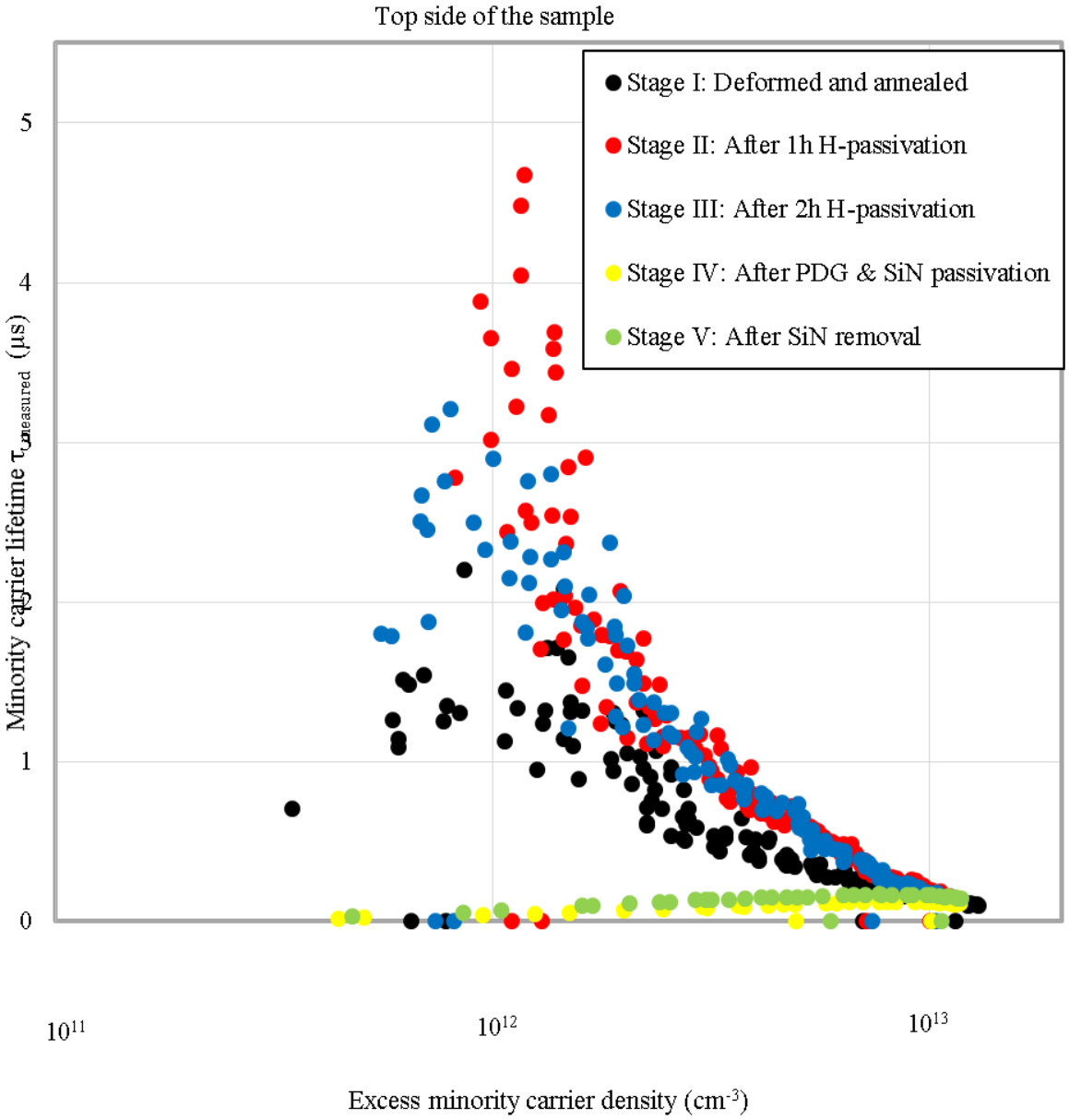


Figure 7.1. Measured minority carrier lifetime versus excess minority carrier density at each processing stage from the top sample surface.

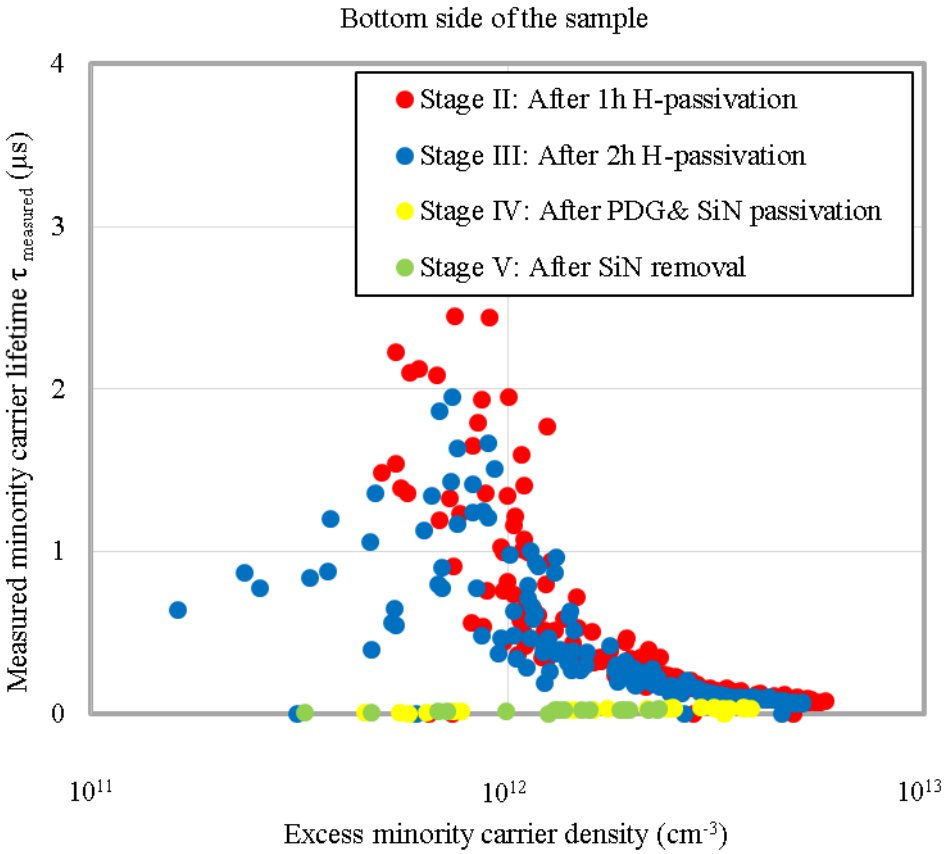


Figure 7.2. Measured minority carrier lifetime versus excess minority carrier density at each processing step from the bottom sample surface.

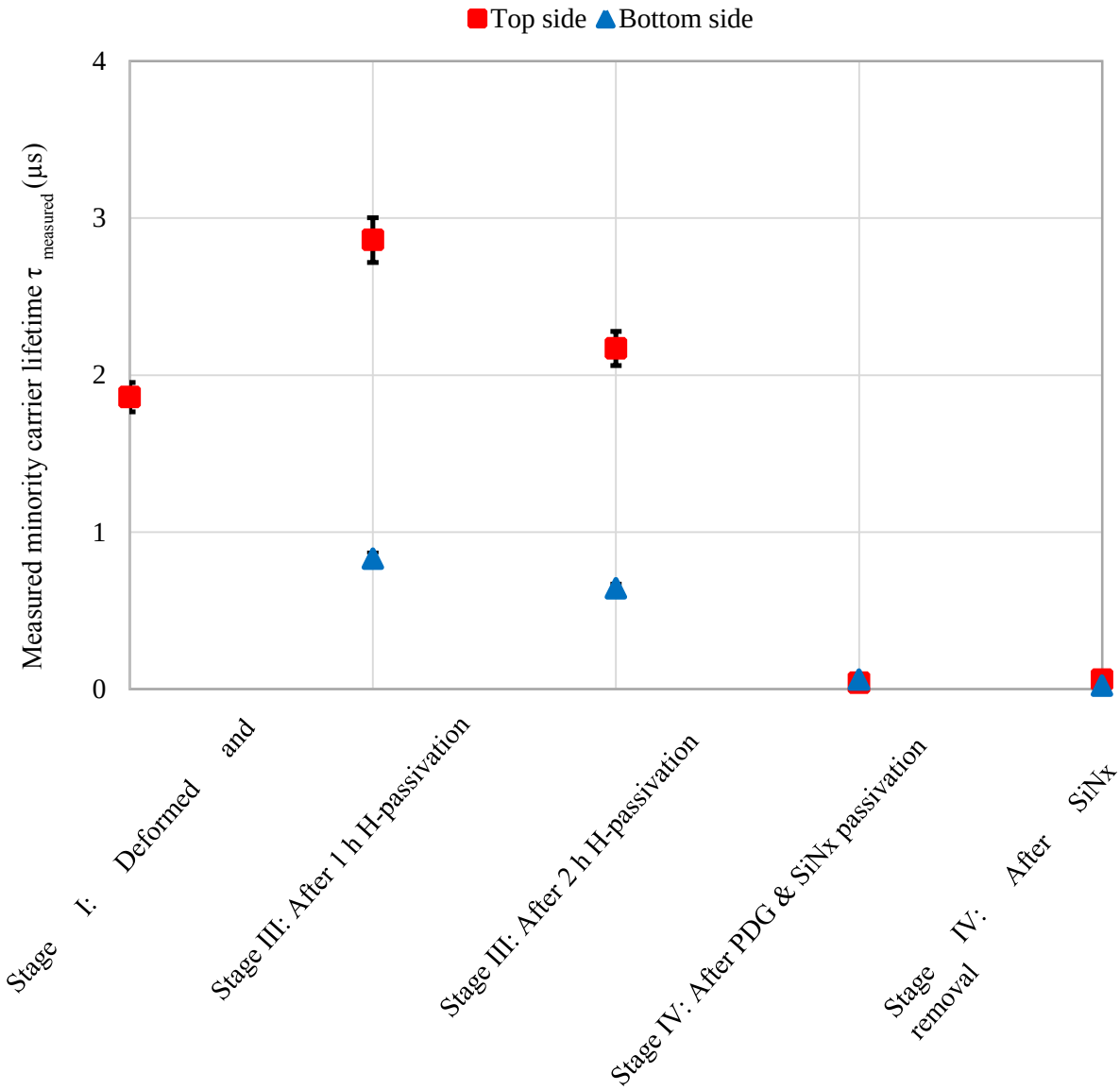


Figure 7.3. Measured minority carrier lifetime at different stages at the injection level of 1 x 10^{12} cm^{-3}. Error bars represent standard error, ±4 % for eddy-current measurement of excess-carrier lifetime for bulk sample [255]. Some errors are in absence as the values are too small to show at the current scale.

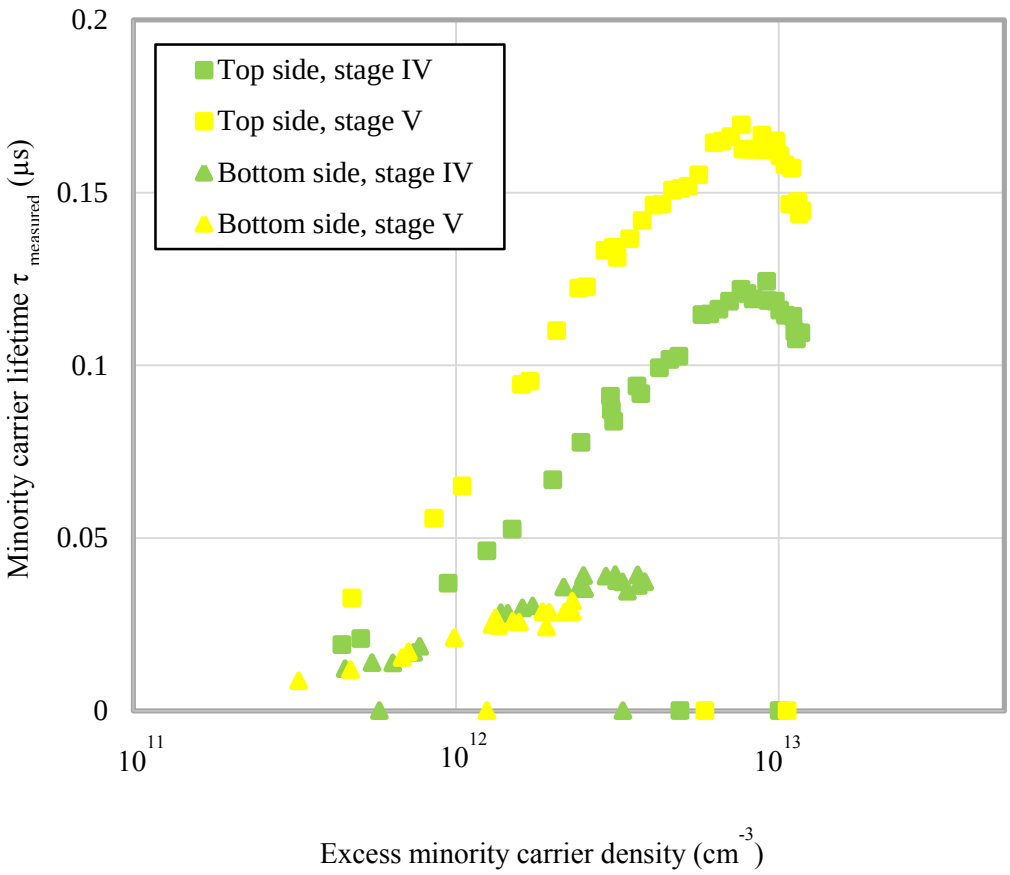


Figure 7.4. Measured minority carrier lifetime versus excess minority carrier density at Stage IV and Stage V from both sides of the sample.

In is evident that the measured effective minority carrier lifetime in the polycrystalline silicon sample at each stage is generally very low and strongly injection dependent. Standard single crystalline silicon wafers have minority carrier lifetime of 1ms or above [235]and standard mc-Si the order of tens of microseconds[236]. At low minority carrier densities, the apparent high minority carrier lifetime measured might arise from trapping effects, which will be discussed in the following section. In spite of the low lifetime measured, it was readily surprising that the polycrystalline silicon sample deformed at 1150 ˚C by 10 % and annealed at 1400 ˚C for 120 min obtained a

measurable minority carrier lifetime (1.9 μs at a minority carrier density of 1 x 10^{12} cm^{-3}), even without any further treatments for electrical properties improvement. In comparison, the as-received polycrystalline silicon yielded no attainable lifetime data. H-passivation for 1 hour effectively increased the excess minority carrier lifetime by 1 μs comparing to the non H-passivation state at a minority carrier concentration of 1.0 x 10^{12} cm^{-3}, however, an additional 1 hour H-passivation noticeably decreased the value at the same concentration level. The following $POCl_3$ gettering and SiNx surface passivation treatments unexpectedly deteriorated the minority carrier lifetime, to a nearly unmeasurable level of 0.04 μs at a minority carrier concentration of 1.0 x 10^{12} cm^{-3}. After the removal of the SiNx layer, this value was measured as 0.06 μs at injection level 1.0 x 10^{12} cm^{-3}, as shown in Figure 7.4. Possible mechanisms for this are discussed later.

Minority carrier lifetime with the bottom side up was only measured for reference. Since no measurement was performed on this surface of the deformed and annealed sample (Stage I), the dataset is incomplete. It should be noted that during the two H-passivation processes, the sample was placed in a way that only the top surface was exposed to the H-plasma, therefore the bottom surface was probably not passivated. However, this surface was treated by both $POCl_3$ gettering and SiNx passivation. Although it is impossible to justify the trend critically, qualitative inspection infers that the measured minority carrier lifetime was degraded significantly after $POCl_3$ gettering and SiNx surface passivation.

7.3.2 Minority carrier lifetime of smashed single crystalline silicon

It was also speculated that the polycrystalline silicon sample contains a large number of cracks after 10 % deformation at 1150 ˚C as observed by naked eyes. These cracks might affect the measured minority carrier lifetime as providing additional surface areas as well as measurement artefacts. This consideration stimulated an experiment to validate numerically the influence of internal sample cracks on acquired minority carrier lifetime measured by the QSS-PC technique. In this experiment, cracks were intentionally introduced progressively and the minority carrier lifetime was measured at each step. The experiment procedure can be described as follows: A piece of 30 mm x 30 mm n-type dislocation free Czochralski sc-Si wafer sample (resistivity 48.63 Ω·cm and thickness 200 μm) was selected as the starting material and the sample was not surface passivated. It was gradually broken into pieces by exponential number with even dimensions but was always reassembled into one piece for lifetime measurements. The sample was broken into 32 pieces eventually and the measured minority carrier lifetime as a function of sample pieces is plotted in Figure 7.5.

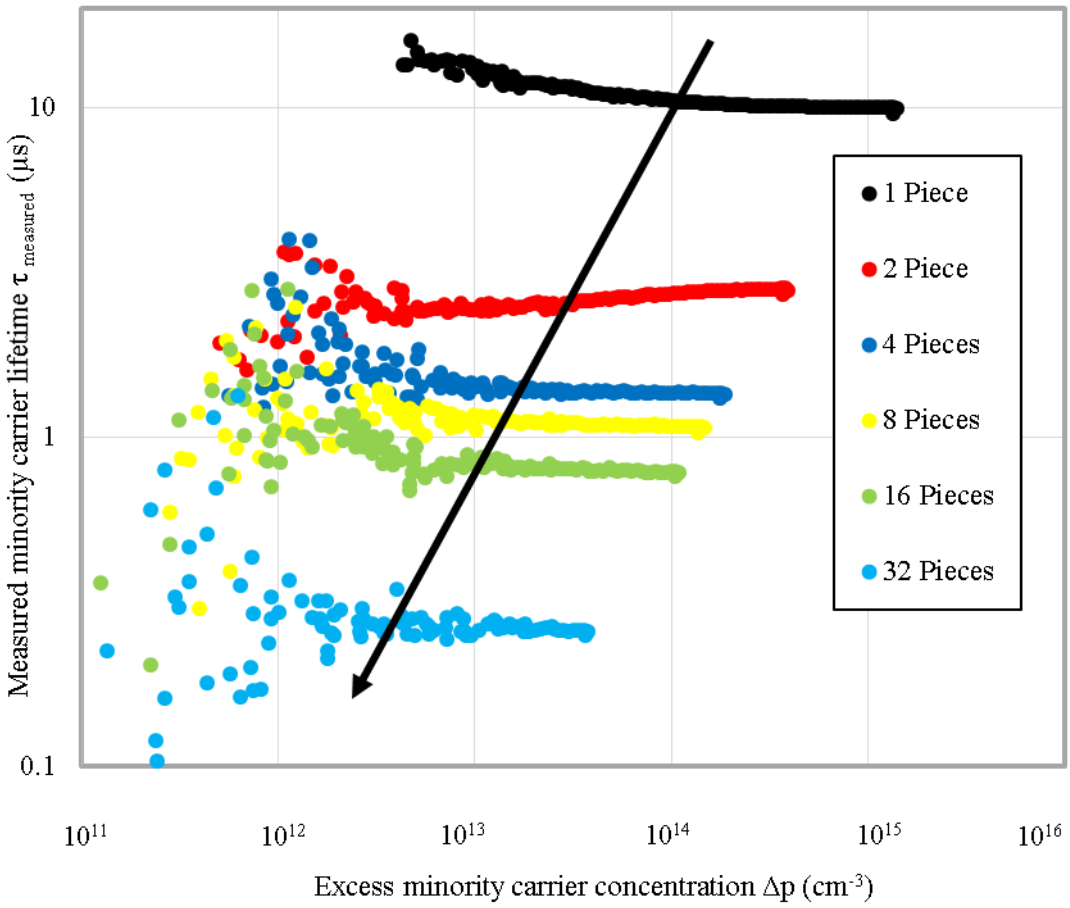


Figure 7.5. Measured minority carrier lifetime as a function of excess minority carrier density of a 30 mm x 30 mm n-type Czochralski sc-Si sample broken into various numbers of pieces exponentially. The general trend is marked by the black arrow.

It is surprising that the measured effective excess carrier lifetime is severely deteriorated even just by introducing one major crack across the sample, if one compares the effective lifetime curves of 1 piece and 2 pieces. The effective lifetime is further degraded by progressively introduced cracks. However, it is interesting to note that the measured lifetime of 4 pieces, 8 pieces and 16 pieces appears relatively comparable, approximately 1 µs at injection level of 1.0 x 10^{14} cm^{-3}. The lifetime of the sample broken into 32 pieces is effectively only measurable at injection level lower than

5.0 x 10 ^{13} cm^{-3}. It can therefore elucidate that internal cracks play a detrimental role in measured excess carrier lifetime.

7.4 Discussion

7.4.1 Comparison of electrical properties with that of previous work

In previous work conducted by Mardesich *et al.* [51], who also attempted to correlate the minority carrier lifetime with microstructure of deformed silicon, it was reported that minority carrier diffusion length of their as-received CVD polycrystalline silicon was near zero whereas the value of their deformed sample was unmeasurable. It is worth noting that their silicon material underwent a different thermo-mechanical treatment. In their work, CVD grown polycrystalline silicon was firstly annealed at 1380 ˚C for 24 hours and then compressed at 1380 ˚C at strain rates of 5.0 to 8.5 s^{-1} until a total 50 % strain was accommodated by the material. Even though no texture change was observed during the pre-annealing process, the material appeared to dynamically recrystallize during the deformation, resulting in some almost dislocation free recrystallized grains up to 500 μm in diameter across 70 % of the material. An additional 10 min annealing at 1380 ˚C boosted 95 % of the material to be recrystallized, eventually. The obtained microstructure, however, is comparable to that observed in this present work, both featuring large recrystallized grains decorated with dislocations and twin boundaries. Therefore the completely different electrical properties attained may not be attributed to the microstructure. The biggest difference in experimental conditions is probably that their thermal and mechanical treatments were conducted in a standard metallurgical apparatus in the absence of any intentional control of potential metallic contamination during the hot deformation. In comparison, the

present work was performed in a clean environment using high purity elements. It can, therefore, be postulated that the measurable minority carrier lifetime in this work is likely to benefit from the clean conditions used by all treatments. It is also worth noting that the initial polycrystalline silicon material of this work was undoped, however, it might become doped during processing due to contaminants introduced. Given the investigation conducted at the current stage, the possible doping level and contaminant varieties have not been fully recognized and this provides potential for future work. In addition, one important point of all the measurements conducted on the present polycrystalline silicon specimen is that it is wrong to assume that the full thickness of the specimen has been fully 'sampled'. This highest measured minority carrier lifetime (approximately 1.9 μs at injection level of 1.0 x 10^{12} cm^{-3}) corresponds to a minority carrier diffusion length of approximately 100 μm for electrons and 50 μm for holes, which is significantly shorter than the specimen thickness 1.2 mm. The following subsections discuss the effect of H-passivation, $POCl_3$ gettering and SiNx passivation, together with potential effects of trapping and cracks on the QSS-PC measurement.

7.4.2 The effective lifetime and trapping effects

Minority lifetime measurement of the deformed and annealed polycrystalline silicon was performed without any surface passivation on the sample, therefore arises a question if the measured lifetime is genuine indicative of the effective bulk lifetime. This section focuses on discussing the physical mechanism of the photo-generation and photo-conductance measurements measurement, aiming at providing insights into the nature of the measured minority carrier lifetime.

One important factor arises as the sample thickness (1.2 mm) is remarkably larger than normal silicon wafers (usually less than 1mm thick). It is not clear whether the lifetime tester coil could detect the signal throughout the sample thickness. According to Dr. R. Sinton (whose company manufacture's the QSS-PC systems used), the coil has a 'sense depth' of about 2 mm[237], although the signal will be reduced by the distance of the photo-conductance from the coil, so this should be a relatively minor effect.

The other factor to consider is the electron-hole pair generation depth. The standard configuration for the WCT-120 is a 700 nm infra-red-pass filter. Via applying a simulator created by R. Sinton and A. Cuevas (for simulation details see [238], [239]) with the spectrum of the flash lamp and filter and the sample characteristics in this work[237], the photo-generation was found to be uniform throughout the sample thickness (as shown in Figure 7.6) and relatively insensitive to surface recombination. 26], [27]

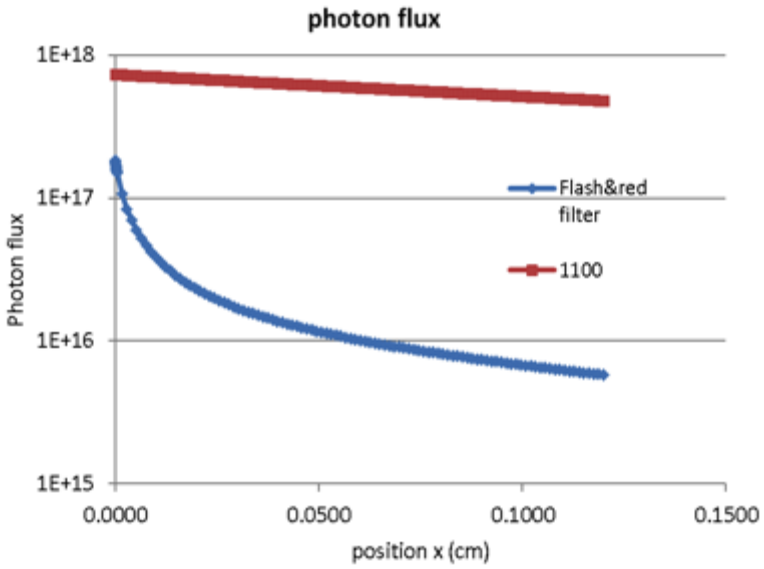


Figure 7.6. Photon flux throughout the polycrystalline sample in this work based on simulation[238], [239].

It is found in all lifetime measurement datasets that the maximum minority carrier concentrations do not exceed approximately 10^{13} cm^{-3}. This is because in the QSS-PC mode, the excess carrier concentration is essentially in steady state, with carrier generation and recombination in balance. The total carrier population is simply the photo-generation rate G multiplied by minority carrier lifetime τ. The G is fixed by the illumination intensity of the flash lamp and filter used in the Sinton lifetime tester, due to the extremely low carrier lifetime that the maximum excess carrier concentration is limited.

The next factor to consider is whether the measured effective lifetime is a true measure of the bulk lifetime. It is known that the effective lifetime τ_{eff} measured by a lifetime tester is composed of two components. One arises from the recombination in the volume of the sample and is characterized by the bulk lifetime τ_b which is a

combination of various types of recombination occurring in the bulk. τ_{eff} is also influenced by recombination that occurs at sample surfaces. It is characterized by surface lifetime τs and is a strong function of the surface recombination velocity $S1$ and $S2$ at either surface of the sample, the sample width W and the minority carrier diffusivity D[240]. The relation of the effective lifetime, the bulk lifetime and the surface lifetime can be described using the following equation:

$$\frac{1}{\tau eff} = \frac{1}{\tau b} + \frac{1}{\tau s} \qquad \text{Equation 7.1}$$

The photo-generation of the present sample using infrared light is relatively uniform throughout the sample thickness and surface recombination is large since no surface passivation was applied. Carriers were generated in the bulk and diffuse to both surfaces, therefore the surface recombination is similar for both front and back surface. The current sample has a thickness W of 0.12 cm and the surface recombination velocity S of bare surface is more than 10^5 cm/s [241]. Since the sample is not doped, the minority carrier type is unknown and should be classified as ambipolar, therefore the diffusivity constant is calculated as 18 cm^2/s according to a simulation of mobility model developed by Klassen[242]. When these parameters satisfy a boundary condition $S \times \frac{W}{D} > 100$, according to a normalized formula developed by Sproul [240]:

$$\tau_s = \frac{1}{D}\left(\frac{W}{\pi}\right)^2 \qquad \text{Equation 7.2}$$

where D is the diffusion constant of the minority carriers and W is the sample width. It can be calculated that for uniform photo-generation (produced by infrared light), the minimum effective surface lifetime is $\tau_s = \frac{1}{18}\left(\frac{0.12}{\pi}\right)^2 s =$ 81 µs. So for the present sample, the effect of the surface recombination could have accounted for about 81 µs,

which is significantly higher even than the highest measured lifetime in the present sample, 1.9 μs at the injection level of 1.0 x 10^{12} cm^{-3}. The surface-limited lifetime is determined by the relatively slow diffusion mechanism of carriers towards the surface in order to recombine, which indicates the carrier density at the surfaces is negligible compared to the carrier density within the sample bulk. Therefore the surface recombination lifetime is a function of the bulk lifetime. It is then a reasonable approximation that the measured lifetime is indicative of the real bulk lifetime.

However, given the unusual shape of minority carrier lifetime as a function of excess minority carrier concentration at low injection levels, another important factor to consider is the so-called trapping effects, which is a well-known phenomenon in measuring minority carrier lifetime at low illumination levels using photo-conductance-based lifetime measurements[243]–[245]. Trapping related artifacts have been widely observed in solar-grade multicrystalline silicon wafers[246]as well as in polycrystalline silicon films[247] and polycrystalline compound semiconductors under low injection conditions[247]. Unlike deep-lying recombination centers within the energy band gap, trapping centers usually exist as shallow states that temporarily hold minority carriers before releasing them back into the band[245]. In the QSS-PC measurement, at excess carrier concentrations comparable to or below the trap density, the presence of minority carrier traps causes a relatively significant excess of the majority carriers, consequently leading to a massively distorted photo-conductance. This effect appears as excessively high apparent lifetime at low injection levels, which does not represent the recombination lifetime. In Figure 7.1 and Figure 7.2, the anomalously high lifetime data points at low injection levels around 1.0 x 10^{12} cm^{-3} and the marked increase in

apparent lifetime with decreasing apparent excess carrier concentration are strong indicative of the presence of minority carrier trapping centers in the current sample.

7.4.3 Effect of H-passivation on lifetime

During H-passivation, H-ions diffuse into the silicon sample. Hydrogen has been known for a long time to saturate dangling bonds at surfaces, vacancies, and grain boundaries, and to passivate deep-level defects, such as those due to transition metal impurities[248]. Many of the electrical levels introduced in silicon by contaminating metal-related centers can be neutralized by reaction with atomic hydrogen. The apparent lifetime measured after 1 hour H-passivation is distinctly higher than the one before at low injection levels, which confirms the effectiveness of H-bulk passivation. This 1 hour passivation was undertaken as a proof of principal experiment. However, a second 1 hour H-passivation fails to further improve the measured lifetime. Provided a simple estimation based on $Ld = \sqrt{Dt}$, where Ld is H diffusion length into crystalline silicon, D is the H diffusion co-efficient at 350 ˚C which is a constant value in this case, t is the diffusion time, after 1 hour H passivation, the diffusion length is $60\sqrt{D}$ and in 2 hours the value is $85\sqrt{D}$, which is not pronouncedly increased from the 1 hour process. In addition, the process might be more complicated as H diffuses into the silicon material and gets trapped by defect sites. It also exists the possibility that a prolonged diffusion process may noticeably improve the passivation effect as the diffusion length would be much larger. However, due to the experiment schedule restraint, this work has not been conducted.

H-plasma might also have a hard radiation damage on the sample surface[249], however, this effect is still under investigation and the amount of damage introduced during the 2 hours 350 ˚C plasma diffusion is unclear at the moment.

7.4.4 Effect of $POCl_3$ gettering and SiNx passivation on lifetime

The measured lifetime deterioration after $POCl_3$ gettering and SiNx passivation might be attributed to the fast cooling profile of the $POCl_3$ gettering. The cooling rate after $POCl_3$ gettering is approximately from 875 ˚C to 800 ˚C in 10 min, followed by an isothermal treatment at 800 ˚C for 25 min, the sample was then quenched to 300 ˚C in approximately 10s. This is a significantly more rapid than normal treatment after deformation and annealing, which is cooling at the rate of 1˚C/min. The gettering process puts impurities back into solution at high temperature and the fast cooling process afterwards could possibly have quenched existing metal impurities in the bulk where they are more recombination active. The measured lifetime value shows no substantial change before and after the SiNx layer removal. This is not surprising that if the bulk lifetime is so low that surface passivation will not have appreciable effect on the measured lifetime value. In addition, no subsequent annealing was applied to the sample after the SiNx deposition, this could also affect the passivation performance. It is also worth noting that gettering at 875 ˚C counter-produced the effect of H-passivation since H-ions bonded at the defect states become thermally active during this process and tend to break off from the passivated sites. The difference in the optical constants (0.9 for measurement before SiNx removal and 0.7 for measurement after SiNx removal) might have a slight impact on the measured lifetime difference, however, since the

change is so small that this might be negligible. Restrained by limited project time allowance, detailed investigation on gettering and surface passivation mechanism on this specific polycrystalline sample has not been conducted and need to be left to future work.

7.4.5 Effect of cracks on photo-conductance measurement

It is probable that the interfaces (*i.e.* caused by internal cracks) contained in the deformed polycrystalline silicon in this work have a considerably deleterious effect on measured lifetime, making it difficult to infer the true 'bulk' lifetime in the deformed material. In this work, the cracked introduced have two main impacts, introducing extra surface area and reducing the size of eddy-current generated during the lifetime measurement. Although internal cracks generate extra surface, however this value is almost negligible comparing to the large surface area, provided that the sample surface area is calculated as $1.8 \times 10^{-3}\ m^2$ whereas the surface area introduced by cracks is only $6.0 \times 10^{-5}\ m^2$. Therefore the effect of eddy-current size might be the main cause accounting for the deteriorated measured lifetime. Analogous observations [250], [251] have been recently reported, specifically a pronounced dependence of the carrier lifetime measured on Al_2O_3 -passivated n-type silicon wafers on the sample size primarily due to the damages near cleaved sample edges. However, the quantitative analysis of this effect remains infeasible for the time being since it requires extra experiments beyond the scope of this thesis.

Alternative characterization methods such as photoluminescence (PL) mapping and microwave-detected photo-conductance decay (μW-PCD) could be useful to overcome

the disadvantages of photo-conductance measurement and therefore extract more genuine information of the true bulk recombination lifetime. In comparison to QSS-PC methods which only measures the sum of excess electron and hole concentrations, the measured PL intensity is proportional to the product of the total electron and hole concentrations[252], [253], consequently PL measurement is negligibly affected by neither trapping artifacts nor excess carriers accumulated in space charge regions[254]. In contrast to QSS-PC, μW-PCD method obtains the benefit of providing more reliable lifetime data under low injection conditions. It illuminates the sample using a short laser pulse on top of a steady-state bias light which generates additional electron-hole pairs within the sample, the time constant of the declination of this additional photo-conductance due to electron-hole recombination is subsequently measured by the detection of reflected microwaves whose reflectance changes based on the conductivity of the sample[254]. These lifetime measurement methods should be considered for application to the present sample in future work.

7.5 Summary

The deformed (at 1150 ˚C by 10%) polycrystalline silicon was subsequently annealed under clean conditions at 1400 ˚C for 120 min. The excess carrier lifetime measurement yielded a value of approximately 1.9 μs at injection level of 1 x 10^{12} cm^{-3}. It corresponds to a minority carrier diffusion length ($\sqrt{Dt}$) of approximately 100 μm for electrons and 50 μm for holes. However, the measured minority carrier lifetime appears abnormally high at low injection illuminations around 10^{12} cm^{-3} and decreases as the increasing minority carrier concentration, which strongly indicates the presence of minority carrier trapping centers in the sample. The sample was subsequently subjected to H-passivation, $POCl_3$ gettering and SiNx surface passivation. It was notified that 1

hour H-passivation effectively increased minority carrier lifetime by 1 μs at injection level of 1 x 10^{12} cm^{-3}. However, the $POCl_3$ gettering and SiNx surface passivation significantly reduced the measured lifetime to a nearly unmeasurable level. Despite that the real causes remain unknown, it is suspected that this might be attributed to the fast quenching profile of the gettering process during which the potential metallic contaminants were unable to diffuse or precipitate. A comparison experiment was conducted on n-type sc-Si wafer sample to numerically evaluate the effect of cracks on measured minority carrier lifetime. It confirms that cracks in the internal structure of the deformed polycrystalline have a remarkable deleterious effect on measured lifetime, which makes it challenging to infer the true 'bulk' lifetime. In summary, detailed analysis and discussion of lifetime datasets shows that it is highly possible that the actual bulk recombination lifetimes are higher than the ones indicated by Sinton QSS-PC measurements and the actual excess minority carrier concentrations are larger due to trapping effects and the restraint of the QSS-PC measurements. Nevertheless, further experiments are required to obtain more quantitative results.

Chapter 8

Summary, conclusions and suggestions for future work

8.1 Summary

This thesis has revisited polycrystalline silicon deformation at elevated temperatures, however, unlike previous investigations, clean conditions and high purity components were used. The introduction of potential harmful contaminants was carefully controlled during all thermal treatments. Subsequent gettering and passivation processes were applied in an attempt to improve the electrical properties for suitability in solar cell fabrication. The aim of this project is to answer the question: is it feasible to manufacture silicon wafers, cost-effectively, via conventional hot rolling using clean conditions?

Firstly, due to the finite resources available, uniaxial compression was used as a proxy for the process of rolling. As described in Chapter 3, a special compression apparatus was designed and manufactured to enable the deformation to be undertaken in a clean environment. Various practical challenges were encountered and overcome during the rig construction, for instance component dimension modification and component material selection. After 18 months, the system was finally tested and verified to be adequate for hot deformation experiments. The deformation cleanliness was subsequently characterized by monitoring the electrical properties of a control single crystalline silicon sample undergoing a thermal cycle in the rig. It is speculated that the cleanness of deformation conditions is at an acceptable level, in which the impurity

concentration introduce is approximately 3 orders of magnitude lower than the solubility (at 1150 ˚C) in silicon should the impurity be iron.

In Chapter 4, the optimum realistic deformation and annealing conditions were investigated by deformation of bulk dislocation-free single crystalline silicon. Compressions were undertaken along the low index [110] axis using different temperatures (1020 ˚C~1150 ˚C) and average strain rates ($1.67 \times 10^{-5}\ s^{-1} \sim 1.00 \times 10^{-4}\ s^{-1}$) under clean conditions. The deformed samples were subjected to various post-annealing conditions. The surface microstructures were examined by preferential etching and SEM, whereas the bulk defect morphology was studied using the TEM diffraction contrast technique. Deformation temperatures of up to 1150 ˚C and subsequent annealing temperature of up to 1400 ˚C are achievable using the available facilities. The initial dislocation-free single crystalline silicon can be uniaxially compressed by more than 30 % at temperatures above 1050 ˚C at low strain rates of $10^{-5}\ s^{-1}$ without severe fractures. The most uniform deformed sample was obtained at 1150 ˚C by 30 % strain using an average strain rate of $1.67 \times 10^{-5}\ s^{-1}$. The maximum stress applied was 40 MPa. Uniaxial compression produces a characteristic deformation microstructure with the appearance of profound cellular structures with intersecting 45˚ inclined straight sub-grain boundaries. 30 % deformation gives rise to a dislocation density of order $10^{13}\ m^{-2}$ and sub-grain cells with varying sizes in the range of less than 5 μm to 20 μm. Recovery was found complete after a prolonged annealing at 1400 ˚C for 120 min, resulting in an enhanced sub-grain cell size up to more than 70 μm and an estimated dislocation density of $10^{10}\ m^{-2}$. A complex defect morphology was revealed by TEM bright field imaging in the bulk of as-deformed samples. Dense dislocation kinks, tangles, bundles and distinct dislocation networks were commonly observed, together

with closely spaced sub-grain boundaries. The sub-grain boundaries are in the form of arrays of parallel dislocation segments. Dislocations with ½[$1\bar{1}0$] screw character were found in both as-deformed and subsequently annealed samples. A suitable deformation condition for polycrystalline silicon was determined to be 1150 ˚C and an average strain rate of order 10^{-5} s^{-1}. A suitable post-deformation annealing temperature, in order to reduce the concentration of extended defects, was determined to be 1400 ˚C.

In Chapter 5, semiconductor grade polycrystalline silicon produced by the Siemens process was deformed at 1150 ˚C at an average strain rate of 6.94 x 10^{-6} s^{-1} under clean conditions. The total strain accommodated was 10 % and the maximum stress applied was 100 MPa. Before the deformation, the polycrystalline silicon was pre-annealed at 1400 ˚C for 30 min to reduce internal stress. The as-deformed polycrystalline silicon was subjected to isothermal annealing at 1400 ˚C for 120 min to provide a fully recrystallized microstructure. The microstructural evolution of polycrystalline silicon during pre-annealing, after deformation and after post-annealing were investigated by preferential etching, SEM, TEM and EBSD. It was found that the as-received polycrystalline silicon comprises a stem-tree like microstructure, heavily textured with a sharp < 110 > fibre texture aligned with the grain growth direction. The material consists of large twin grains elongating in the grain growth direction and containing primarily Σ 3 and Σ 9 grain boundaries. The grain sizes vary from 3 ~ 30 μm in length and 1 ~ 3 μm in diameter. Annealing at 1400 ˚C for 30 min effectively recrystallized 90 % of the as-received material, yielding an average grain size of 30 μm. The recrystallized microstructure has no texture and contains mainly Σ 9 twin grain boundaries and high angle grain boundaries. Prolonged annealing at 1400 ˚C for up to 120 min was found to have no significant impact on the microstructural alteration. In the material pre-

annealed at 1400 ˚C for 30 min, the un-recrystallized region contains densely-spaced short dislocation arrays and stacking faults. The dislocation segments are approximately 300 nm apart, lying in the < 211 > crystallographic direction. Most stacking faults are arranged along the < 110 > direction. The recrystallized region contains significantly lower concentrations of defects, mainly stacking faults lying along the < 110 > orientation with associated partial dislocations. The plastic deformation gave rise to an appreciably large number of sub-grain boundaries in grain interiors, without altering the overall grain microstructure. The average dislocation density was increased from approximately 1 $x10^{12}$ m^{-2} before deformation to 8 $x10^{12}$ m^{-2} as measured by SEM etch pit counting. Defect morphology assessed by TEM confirmed a typical plastic deformation microstructure of the as-deformed material, featuring a complex dislocation network and sub-grain boundaries in the form of closely spaced dislocation segments. Dislocations with Burgers vector of ½ [110] and ½ [$1\bar{1}0$] were found. Subsequent annealing at 1400 ˚C for 15 min led to 50 % of the deformed material recrystallized for a second time. The observed microstructures have large grains of several hundred microns scale and relatively straight high angle grain boundaries. The average dislocation density was estimated as 5 x 10^{10} m^{-2} by etch pit counting. The second recrystallization was completed by prolonged annealing at 1400 ˚C for 120 min, in both sections parallel and perpendicular to the compression axis.

In Chapter 6, HR-EBSD cross-correlation method was employed to quantitatively investigate the GND density evolution of the polycrystalline silicon during pre-annealing, after deformation and after post-annealing. It was found that the as-received polycrystalline silicon has an average GND density in excess of 10^{14} m^{-2} in both sections parallel and perpendicular to the initial grain growth, with some local high GND content

higher than 10^{15} m^{-2}. Pre-annealing at 1400 ˚C for 30 min significantly reduced the statistical GND density to approximately 10^{13} m^{-2}, however, prolonged annealing did not seem to further decrease the GND density significantly. Most of the high GND density regions coincide with high angle grain boundaries in the pre-annealed sample. Plastic deformation at 1150 ˚C by 10 % strain produced continuous, curved, high GND content band patterns within the grain interiors, presumably in the nature of sub-grain boundaries. The GND density present in the dislocation bands is estimated as ~ 10^{14} m^{-2} whereas the inter band regions have an approximate GND density of 5 x 10^{13} m^{-2}. After the second recrystallization (performed after deformation) by annealing at 1400 ˚C for 15 min, the recrystallized regions had an average GND density as measured by HR-EBSD of ~ $10^{12.5}$ m^{-2}. This value is around the noise level of the technique. Therefore the real dislocation density in these regions may be lower. Direction comparison of the HR-EBSD method and preferential etching was conducted. It was found that the GND density value and etch pits revealed by preferential etching from the high GND density (noticeably above the noise level) regions are in good agreement. On the other hand, in the low GND density recrystallized grains preferential etching obtained a “true” etch pit density below 10^{11} m^{-2} whereas the HR-EBSD cross-correlation method assessed a GND density of $10^{12.5}$ m^{-2}.

In Chapter 7, minority carrier lifetime measurements using the QSS-PC method were conducted on the polycrystalline silicon deformed at 1150 ˚C by 10 % and post-annealed at 1400 ˚C for 120 min. The lifetime measurement yielded a value of approximately 1.9 μs at injection level of 1 x 10^{12} cm^{-3} which corresponds to a minority carrier diffusion length of approximately 100 μm for electrons and 50 μm for holes. The sample was subsequently subjected to H-passivation, $POCl_3$ gettering and SiNx surface

passivation. It was found that the minority carrier lifetime was increased to 2.9 μs at injection level of 1 x 10^{12} cm^{-3} after 1 hour H-passivation. However, the $POCl_3$ gettering and SiNx surface passivation significantly reduced the measured lifetime to a nearly unmeasurable level. It is speculated that this might be caused by the fast cooling profile of the $POCl_3$ gettering, which could possibly have quenched existing metal impurities in the bulk where they are more recombination active. The effect of cracks on measured minority carrier lifetime was evaluated by breaking n-type single crystalline silicon wafer samples. It has been found that internal cracks play a significant role in reducing measured excess carrier lifetime.

8.2 Conclusions

The results presented in this thesis suggest that the deformed and annealed polycrystalline silicon may maintain a reasonable minority carrier lifetime. Therefore producing silicon sheets by conventional hot-deformation has potential for future investigation for photovoltaic. However, the work was severely limited by the facilities and resources available. The highest temperature that could be reached in the deformation rig with the present set up was 1150 ˚C, which also resulted in a very slow deformation process. However, the process was performed to produce a total deformation equivalent with that obtained by rolling processes. Therefore this material is a reliable indicator of the electrical characteristics of heavily rolled silicon. It has been shown from previous work that at around 1400 ˚C silicon has approximately the same mechanical properties as aluminium at room temperature with regard to rolling. It is thus expected that with a deformation rig or rolling apparatus that could work at sufficiently high temperatures, a fast rolling process might be possible. After rolling the following step is to perform a recrystallization of to reduce the internal stress. In the

present work, since it was difficult to set the furnace temperature accurately, the recrystallization was performed at about 14 ˚C below the melting point. Also due to time constraints experiments were not performed to investigate the possibility whether annealing for a much shorter time than 15minutes would produce a satisfactory structure. It thus remains unclear that how short the annealing could be if temperatures closer to the melting point of silicon were achieved. From a practical point of view the shorter the time the better. An additional point with regard to this step is that the effectiveness of the recrystallization process depends on the stored energy in the material. After deformation at 1400 ˚C this energy will be different from what is obtained at 1150 ˚C, just as in the present work. Nevertheless, it is expected that by increasing the speed of the deformation process at 1400 ˚C the same or higher stored energies would be achieved. Finally it is possible that at such high temperatures, the defects present in the starting material are much more mobile, which might lead to the avoidance of the pre-deformation annealing step. Thus, this work has not excluded the possibility that hot rolling of silicon sheet is commercially feasible. However, due to the limitations on the equipment available, it has been difficult to argue that this would possible but that was never the intention of this project. This project was set up to determine whether the electrical characteristics of heavily deformed silicon material could be made satisfactory for solar applications, provided sufficiently clean processing together with industry standard passivation techniques. The results attained are very encouraging with the 2.9 μs lifetime even though it is very likely limited by cracks present in the sample. Therefore this project has indicated that it might be possible to produce thin silicon sheets in a rapid and kerf-less way and the resultant material may be electrically satisfactory for solar cell fabrication.

8.3 Suggestions for future work

The obtained deformed polycrystalline material has a large number of micro-cracks, presumably due to the bad mechanical quality of the as-received polycrystalline material which was made for use in Czochralski silicon manufacturing. Such material is crushed after manufacturing and so cracks are unimportant for their future use. Cracks can be avoided by using high quality polycrystalline silicon that is grown specifically for the float zone process. In this case the material is crystallized directly from the polycrystalline ingot therefore it needs to be produced free from cracks. Unfortunately such material was not available for use in this project. Further work should thus be performed on the crack free polycrystalline material so that measurements of carrier lifetime in deformed material can be made without the influence of cracks.

Although the minority carrier lifetime was reduced after gettering in this work the reasons remain unknown for the time being, development of better gettering processes is still necessary for future lifetime improvement. In particular the effect of the speed of cooling on lifetime should be investigated. As mentioned above, in future work, a much higher deformation temperature (ideally close to 1414 ˚C) is required to enable a much faster deformation process and the possibility to eliminate pre-annealing process. A better quality deformed material will be achieved by using float zone Siemens polycrystalline silicon. In addition, secondary ion mass spectrometry (SIMS) will be helpful to obtain a quantitative analysis of the composition of polycrystalline silicon samples, thus to understand if the lifetime deterioration is due to metallic contamination.

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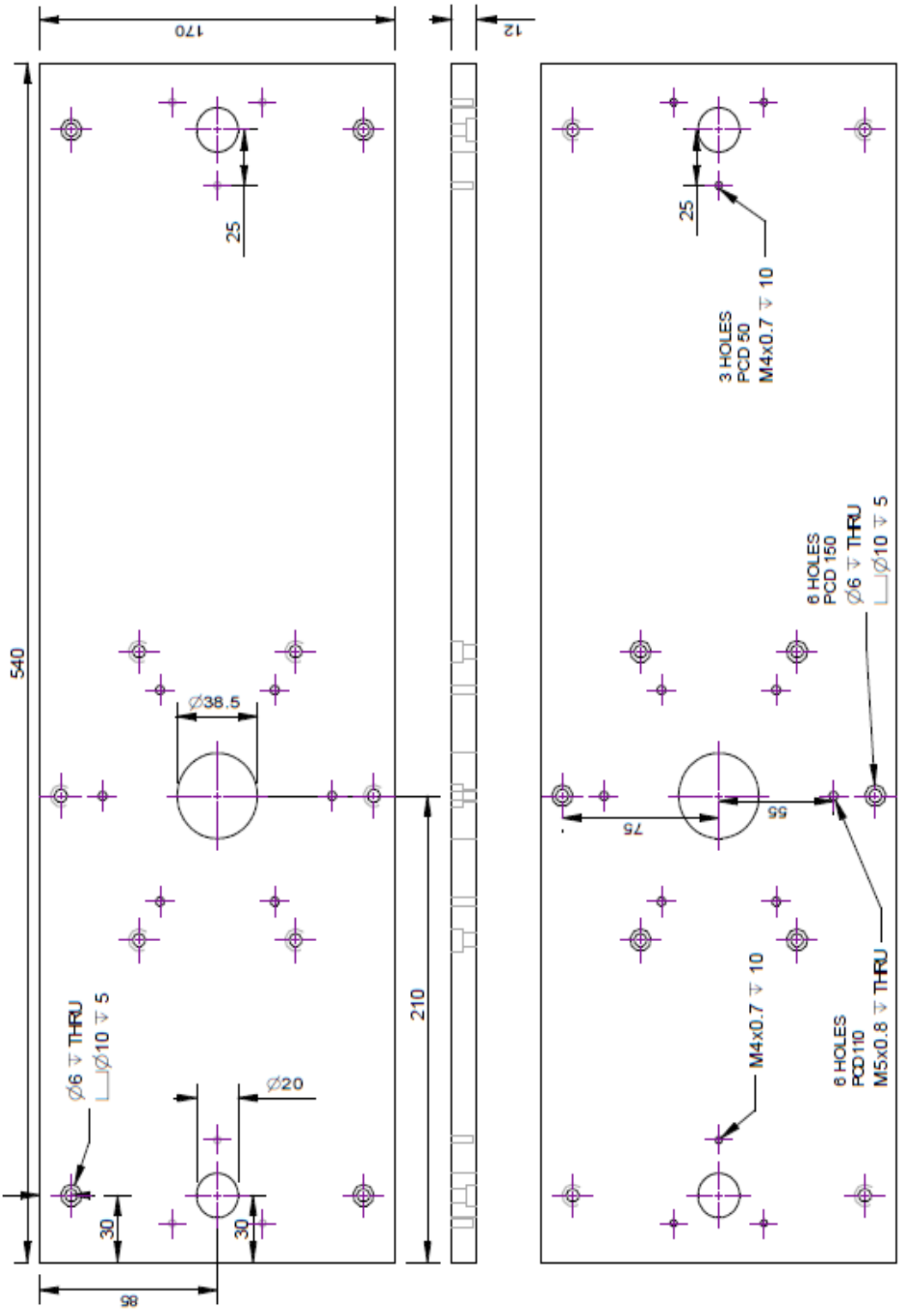
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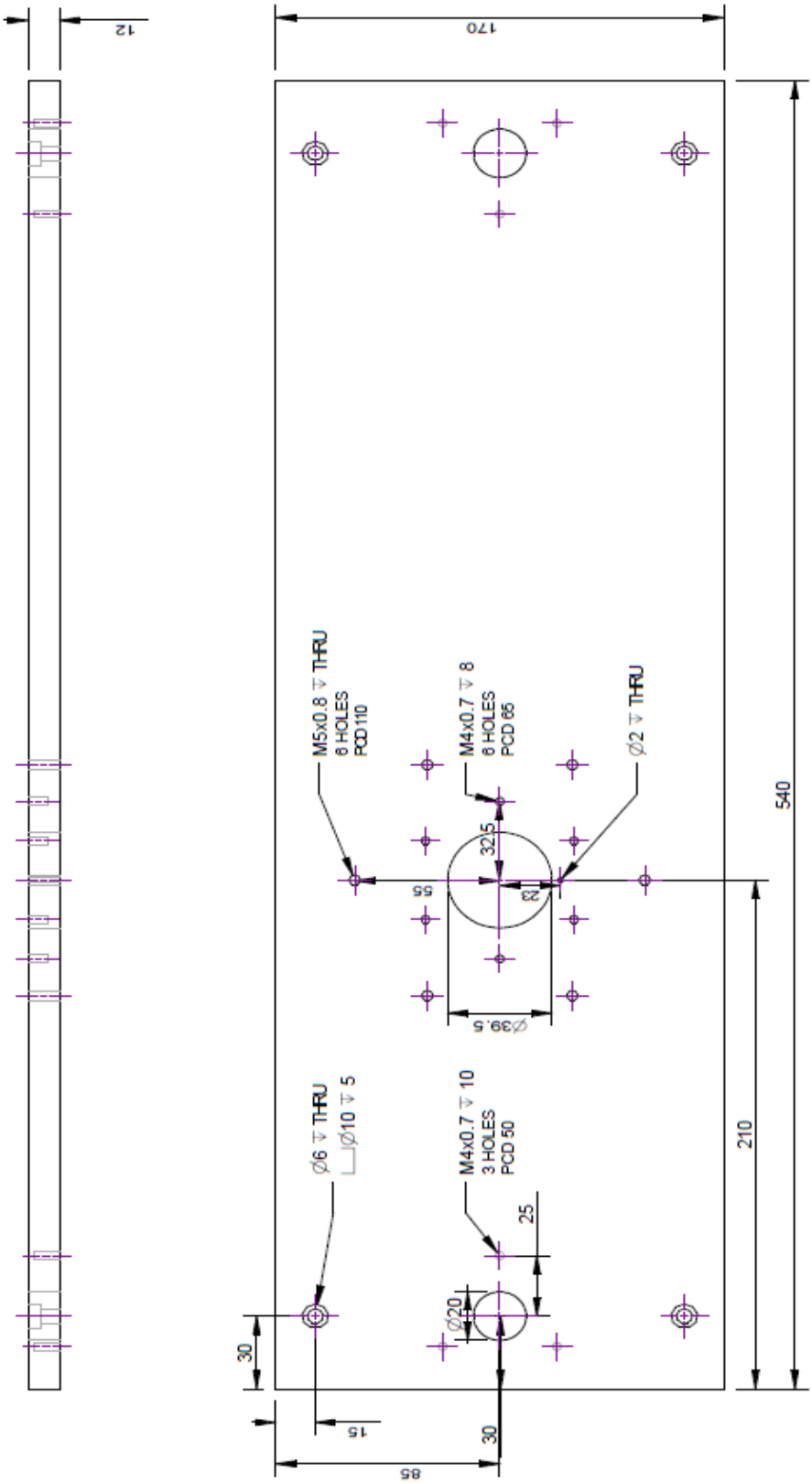
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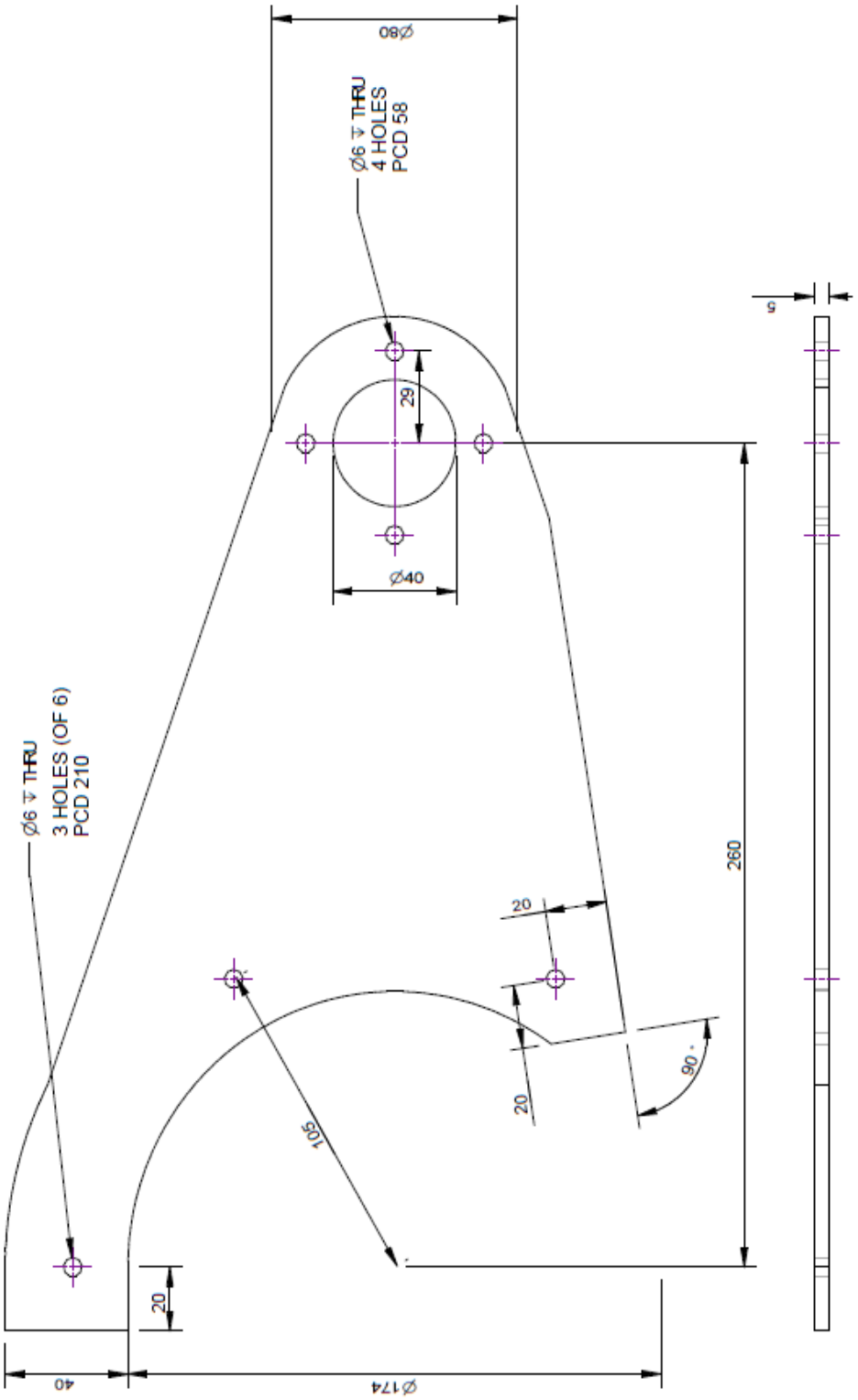
Appendix



Final design of the rig bottom plate



Final design of the rig top plate



Final design of the aluminium bracket