# Roll-to-Roll Processable Organic Thin Film Transistor based Circuits and their Sensory Application


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# Abstract

This thesis is trying to explore a possible routine to manufacture flexible sensor via vacuum-based processes. It starts with an exploration of a route to manufacture Organic Thin Film Transistors (OTFTs) and then a series of stabilization methods are discussed to reduce the probability of short circuit, current leakage and improve the performance of OTFTs, i.e., increasing mobility and decreasing threshold voltage. In addition, a possible mechanism of bias stress is investigated with a model and the relevant evolution of trapping state and trapping energy is plotted over time and distance from the dielectric/semiconductor interface. Next, a short-time bias scheme is demonstrated to reduce error of bias stress during strain tests. A first example of a strain sensor is based on the architecture of floating gate OTFTs, i.e., a PVDF coated floating gate that transfers the signal of charge imbalance from the ferroelectric effect to transistors, and then the OTFT will output the amplified signal. The advantage of floating gate structure is the separation of the transistor and sensor part to avoid interference between transistor and sensing reaction and giving the option for the transistor to be encapsulated from the environment. However, the bias voltage is a key parameter to control the floating gate sensor, with the sensitivity of the device dependant on it, i.e., it is very difficult to obtain both a sensitive signal at same time as one unaffected by bias stress. In order to obtain a sensitive and stable signal, a series of OTFT-based functional circuits are developed and a transimpedance converter is fabricated to convert nano-scale input current to a readable voltage output (0 – 3V). After encapsulation, the linear converting relationship is maintained and the mechanical flexibility is not affected. Finally, a series of sensors are built with the

OTFT-based signal conditioning circuit to detect arterial pulse from human body, pH, hydrogen peroxide and glucose from solution. Conclusively, this thesis demonstrates a new architecture of OTFT-based sensing system, and that can work as a versatile platform to integrate with different functionalized sensing electrodes to process signals to a readable level and visualized with smartphone via Bluetooth microcontroller.

*For father and mother*

*For Susan*

# Acknowledgement

Time flies by. It has been an incredible journey conducting research under the supervision of Dr Hazel Assender. I would like to extend my sincerest thanks to her, for her constant patience, encouragement, inspiration, and trust. I also thank Dr Thomas Cosnahan for training me to use Edward 306 and Oxford Web-coater and demonstrating fabrication and characterisation of organic thin film transistors. I am also grateful for Dr Bryan Stuart's demonstrating procedure to maintain vacuum devices and steps to develop polymer encapsulation. Gratitude is also given to Dr Ching-Mei Chen for her patient guidance on circuit layout design of flexible electronics and construction of wireless signal processing device. Thanks are also given to Dr Bruno G. Rosa, Dr Salzitsa Anastasove, Dr Benny P. L. Lo, and Prof Guang-Zhong Yang for sharing electronic facilities of sensor characterisation in Imperial College. Great thanks to Mr Botao Hao, Mr Daniel Gregory and Mr Xudong Tao for discussing with me on materials synthesis and characterisation. Moreover, I deeply appreciate the inspiring weekly talks organized by Dr Andrew Watt and Prof Nicole Grobert. I also extend my appreciation to Mr Richard Turner, Mr Greg Cock and Paul Warren for technical supports in the lab every day and IT support. Many thanks are also given to Mr Paul Pattinson for the fabrication of shadow masks in Department of Physics; to Dr Colin Johnston, Chris Salter and Nicola Flanagan for training me to use materials characterisation device in Begbroke; to Dr Vincent Tobin for his help about thesis writing and job hunting. I also thank my fellow rock-band players, Kuangdai Leng, and Jingyi Yang, and Zi Yin for our shared music time, as well as my friends at Wolfson College for our interesting dinner chats and coffee-

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# Declaration of Originality

This thesis is an account of work carried out by the author in the Department of Materials, University of Oxford under the supervision of Dr Hazel Assender. Any other work that has been addressed in the thesis is acknowledged in the text and lists of reference are presented at the end of each chapter. No part of this thesis has been submitted towards the completion of another degree at the University of Oxford or elsewhere. Parts of this thesis have been published in the following scientific journals or conference presentations:

**Kai Zhang**, Ching-Mei Chen, Salzitsa Anastasova, Bruno Gil, Benny Lo and Hazel Assender (2019) Roll-to-Roll Processable OTFT-based Amplifier and Application for Wearable Sensors. *Wearable and Flexible Technology 2019*. Poster Session and Oral Presentation

C.M. Chen, S. Anastasova, **K. Zhang**, B.G. Rosa, B.P.L. Lo, H.E. Assender and G.Z. Yang (2019) Towards Wearable and Flexible Sensors and Circuits Integration for Stress Monitoring. *Journal of Biomedical and Health Informatics*

**Kai Zhang**, Ching-Mei Chen, Salzitsa Anastasova, Bruno Gil, Benny Lo, and Hazel Assender (2019) Roll-to-Roll Procesable OTFT-based amplifiers and Application for pH Sensing. *2019 IEEE International Conference on Wearable and Implantable Body Sensor Network*

**Kai Zhang**, Ching-Mei Chen, Hazel Assender and Bhaskar Choubey (2018) Roll-to-Roll Rrocessable OTFT-based Amplifiers and Sensors. *AVS 65$^{th}$ International Symposium & Exhibition*. Oral Presentation

**Kai Zhang** and Hazel Assender (2018) Roll-to-Roll Manufacture of OTFT Sensors based on PVDF. *The 4th Annual Innovations in Large-Area Electronics Conference (innoLAE 2018)*. Poster Session

**Kai Zhang** and Hazel Assender (2017) Roll-to-Roll Manufacture of OTFT Sensors based on PVDF. *Wearable and Flexible Technology 2017*. Poster Session

# Contents

# Chapter I

# Introduction

## 1.1 Market Development of Flexible Electronics

Flexible electronics has become a more promising market for consumable electronic device during the recent decades and some successful commercial demonstrations, for example, foldable smartphones from Samsung, Huawei and Xiaomi, have attracted high attention from the public. It is forecast that the market for flexible electronics will increase from $ 41.2 billion in 2020 to $ 74 billion in 2030 and the distribution of technologies in 2019 is shown in figure 1, including flexible display, wearable sensor, simple logic processor, and flexible batteries [1].

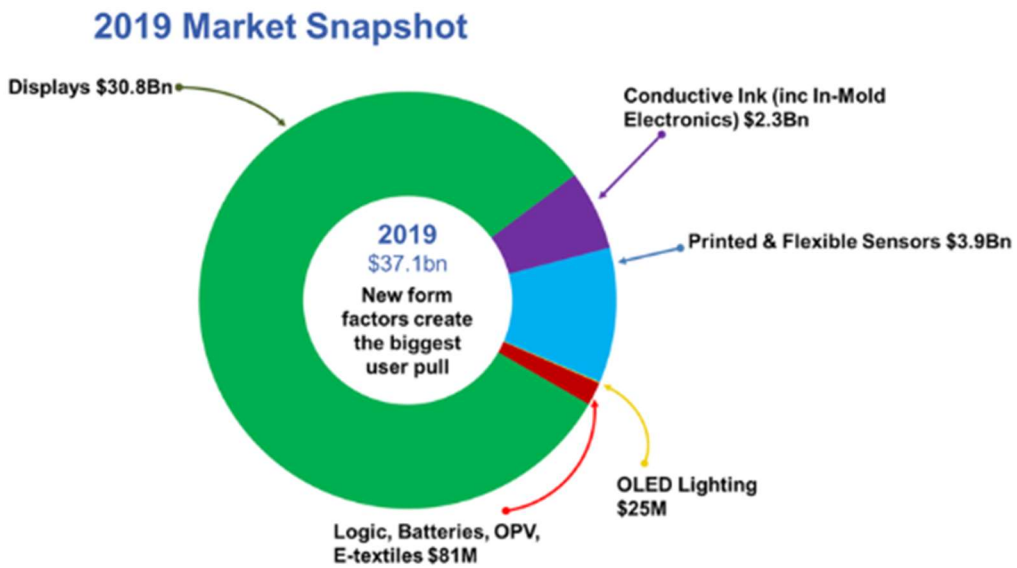



Figure 1.1. Market Distribution of Flexible Electronics in 2019 [1]

Particularly, with the development of a new generation of 5G communication and Internet of Things (IoT), flexible and wearable electronics, such as wearable sensor and flexible displays are anticipated to play a more important role in the market of smart devices. Although this market is dominated by flexible displays currently, the flexible sensor is expected to experience a significant growth in next decade because more applications, such as wearable health condition monitoring system and remote medical diagnosis will grow with increasing public expectation of personalized healthcare.

From the perspective of electronic engineering, fabricating flexible devices with commercial electronic components on a flexible substrate is a cost-effective method because there is already an advanced industrial community to supply basic electronic components, such as resistors, capacitors, inductors, transistors, and operational amplifiers with a low cost. However, all these standard components are not flexible, and the entire device gradually loses flexibility as more components are soldered onto a flexible substrate.

In order to fabricate fully flexible electronics, it is necessary to manufacture flexible basic electronic components directly onto a flexible substrate and for them to be connected into functional circuits. However, the manufacturing techniques, such as physical vapour deposition (PVD), chemical vapour deposition (CVD), screen printing, ink-jet printing and gravure printing for these functional components are still in development, e.g. there are few industrial lines to produce organic electronics, like OLED display, in large scale. In addition, the typical materials used in such flexible electronics exhibit instability when manufactured as thin films, which increase the uncertainties in the performance of devices. To bring flexible electronics into daily life,

a reliable manufacturing standard and a manufacturing technique are needed from the perspective of material research, and then electronic engineer can realize novel circuit design and device optimization, and finally, flexible electronics can be supplied to the market.

## 1.2 Objective of Thesis

This thesis is going to investigate the possibility to fabricate a flexible sensing system via vacuum processing. The sensing system is required to extract and process a signal to a readable level, and a series of examples are demonstrated with consideration of device stability, mechanical flexibility, different signal generating mechanisms, and signal processing mechanisms. In addition, in order to facilitate future scaling up manufacture, devices are designed with consideration of a technique that can be scaled up for high throughput production, for example, a roll-to-roll technique. Finally, sensitivity and selectivity of sensors are demonstrated and possible optimization ideas are discussed.

## 1.3 Thesis Outline

The fundamental principle of this research is firstly manufacturing single OTFTs and then integrating OTFTs with the sensing components to develop OTFT-based sensors. Chapter I is a brief introduction about the market of flexible electronics and background of this research. Chapter II is to review the recent development of organic electronics from the perspectives of materials, processing technique, system design and end sensor applications, afterward, there are four chapters to discuss experiments and results. The interconnection of the experimental chapters is shown in figure 1.2.

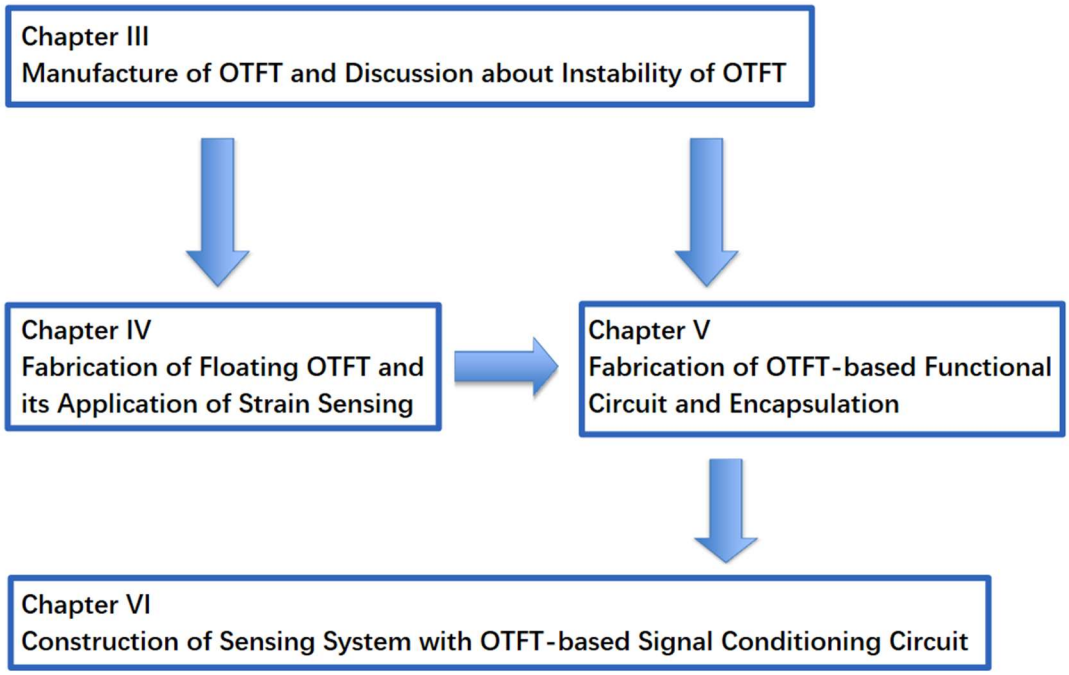



Figure 1.2. Outline of Thesis

The first experimental chapter (Chapter III) is to describe how to manufacture OTFT with vacuum process, and afterward, to discuss the possible reasons for the instability of OTFT when it is biased; a stabilization method is introduced. The second experimental chapter (Chapter IV) starts from the sensing principle of a floating gate device. After treatment optimization of a ferroelectric polymer, ferroelectric polymer coupled floating gate OTFT is fabricated for strain sensing application. Next, a strain measurement model is demonstrated and a novel testing method is discussed to extract the strain signal with less error from the instability of the OTFT. The third experimental chapter (Chapter V) is to describe the procedure to fabricate functional circuit with OTFT, from layout design to manufacturing, and the performance evaluation of each circuit. Afterward, a signal conditioning circuit is fabricated and encapsulated to work as an independent unit in the construction of a flexible sensing system. After that, Chapter VI introduces the procedure to build a flexible sensor based

on the signal conditioning circuit made in the last chapter, and there are four sensing applications developed to extract signals from mechanical strain and chemical reactions in solution.

Finally, Chapter VII concludes all findings in this doctoral research, from materials development, fabrication of flexible integrated circuit, to construction of sensing system. In future work, materials advancement is a key factor to develop a stable OTFT, and the processing technique needs to be further developed to scale up production of thin film electronics. Furthermore, system optimisation is indispensable to build a fully connected sensing system and the flexible sensors will be an important part of Internet of Thing (IoT).

# Chapter II

# Literature Review

## 2.1 Introduction

In the future era of Internet of Thing (IoT), sensors will play a very important role, and flexible sensors will be more advantageous than Si-based sensors for some applications. Firstly, the mechanical flexibility makes it possible to apply such devices on curved surfaces with less risk of brittle failure. Secondly, it is usually printed on a plastic substrate, i.e. the light-weight characteristic enable more wearable and portable applications. Thirdly, the roll-to-roll technique is helpful to scale up production of flexible electronics and reduce overall cost of single products, the flexible sensor will exhibit more price advantage for mass-production application.

From the perspective of sensory applications, organic thin film transistors are required because they can work as a signal processing unit independently or used to fabricate a signal processing circuit to convert the sensory signal to a readable level for human or machine. Therefore, fabrication of a flexible sensor is not only a case of developing a sensitive detector to extract a signal, but also including development of flexible OTFT and its functional circuit for signal processing.

Conventional OTFT-based sensors are designed to exploit directly the sensitivity of the semiconductor. However, this is not a sustainable way for OTFTs because of the unstable properties exhibited by the organic semiconductor when it directly reacts with

analytes, which will discussed in the following sections. Therefore, the development of OTFT-based sensors should be divided into two aspects, the first is to develop stable signal output with OTFTs and the second is to improve sensitivity and selectivity. To achieve signal processing function, some simple integrated circuits based on OTFTs have been fabricated, such as logic circuits and amplification circuits [2-8]. With a stable signal processing unit, more sensing reactions can be used on flexible sensor, for example, some enzymatic reaction in the human body that will be described in the sections on sensory review. In other words, OTFTs are a bridge to connect the development of sensing mechanism and optimisation of functional circuits.

The roll-to-roll technique, which provides a manufacturing capability for large area thin film materials with high throughput, is helpful to realize a cost-effective fabrication of OTFTs. A roll-to-roll production line can realize the multiple layer structure required for OTFT, illustrated in figure 2.1. With help of a suitable patterning technique, large areas of OTFT and OTFT-based circuits can be manufactured with a low cost.

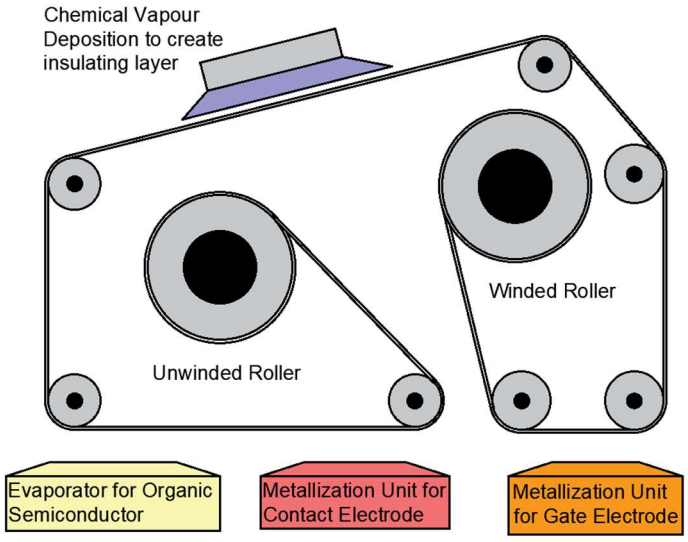



Figure 2.1. Schematic of Roll-to-Roll Production Line for OTFT

The objective of this chapter is to give a comprehensive introduction to the development of an OTFT-based sensor, starting from the working principle and manufacture of a single OTFT. Next, a series of conventional OTFT-based sensor applications and approaches are introduced and compared. Afterward, some developments on OTFT-based sensors are reviewed, including the floating gate structure, building signal conditioning circuits and electrode functionalization for selectivity in sensing. Finally, novel sensors integrated with OTFT-based circuit are described.

## 2.2 Working Principle of Organic Thin Film Transistors (OTFT)

In this section, the working principle and manufacture of OTFTs will be introduced firstly, and then research about stability of OTFT will be discussed, in particular to consider the phenomenon of bias stress, including possible mechanisms to explain why bias stress occurs and how to reduce it.

### 2.2.1 Working Principle and Structure of OTFT

A transistor is a three-terminal device that can be used as a switch or amplifier. In a thin film transistor, current through a conductive channel is dependent on the density of charge carrier, induced by an applied voltage at the gate, near the semiconductor/dielectric interface (Figure 2.2).

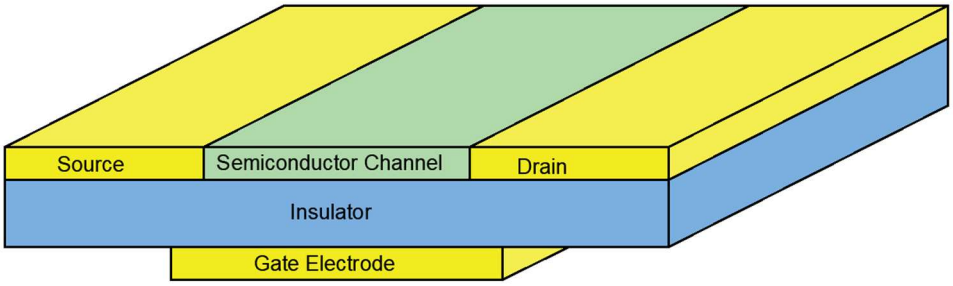



Figure 2.2. Schematic Structure of a Field-Effect Transistor

The gate/drain pair or gate/source pair can be considered as a structure of Metal-Insulator-Semiconductor (MIS), similar to Metal Oxide Semiconductor Field Effect Transistor (MOSFET), and there are four different working modes in which charge carrier density is exponentially dependent on energy difference from Fermi level, shown in figure 2.3.

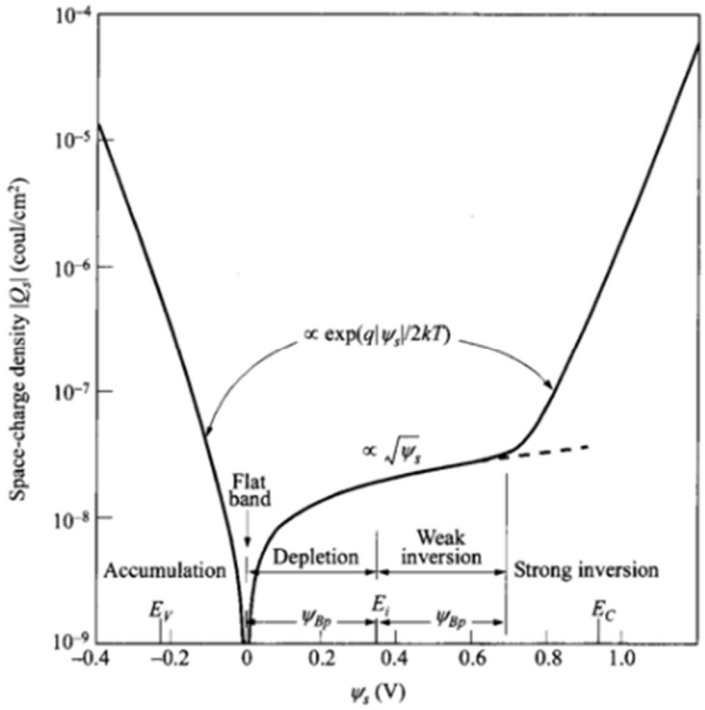



Figure 2.3. Density of Charge Carrier in Semiconductor as a Function of the Surface Potential [9]

Without bias voltage, the MIS structure keeps a flat band condition, shown in figure 2.4, in which the Fermi level of the gate electrode aligns with that of the semiconductor in same energy status. As a result, there is no current in the channel, i.e., the transistor is off. For organic semiconductors, the Highest Occupied Molecular Orbital (HOMO) and the Lowest Unoccupied Molecular Orbital (LUMO) are respectively equivalent to the valence band and conduction band in a conventional semiconductor, such as Si and GaAs. Doping is a method to alter the Fermi level of a semiconductor, and most semiconductors that are widely used today can be divided into p-type and n-type. The Fermi level of the former is close to the valence band (HOMO) and that of latter is close to conduction band (LUMO).

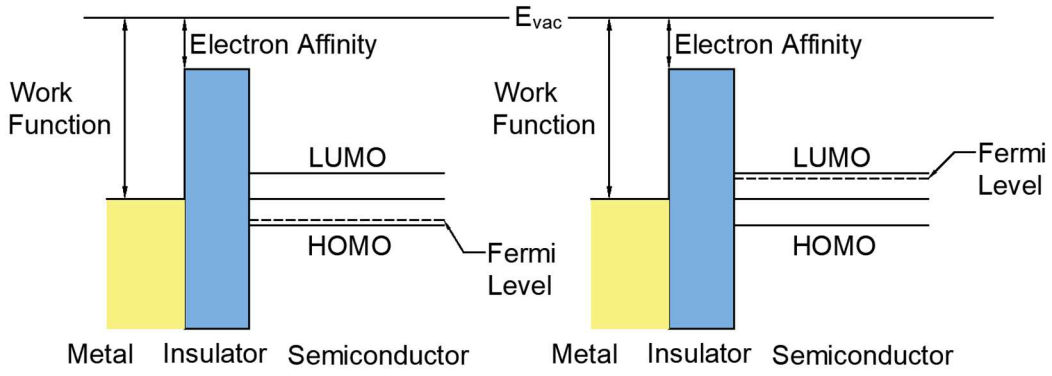



Figure 2.4. Flat Band Energy Diagram for p-type and n-type organic semiconductor [9]

For a p-type semiconductor, a negative bias voltage on the gate electrode leads to an upward bending of the LUMO and HOMO due to the electric field generated across the MIS (Figure 2.5). When the HOMO level at the insulator/semiconductor interface is above the Fermi level of the OSC, charge carriers (holes) will be localized at this interface and this is the accumulation mode. For an n-type semiconductor, the reverse is true, with electrons accumulating at the interface. Under this condition, the channel

is switched on because the charge carriers accumulated at the interface can flow under a driving electric field between source electrode and drain electrode.

In contrast, when the MIS is biased in the opposite direction, i.e., the valence band (HOMO) in p-type MIS or conduction band (LUMO) in n-type moves away from Fermi level, the density of charge carriers is reduced; this is called depletion mode. Consequently, the density of charge carrier is too low to generate current flow at the insulator/semiconductor interface, and transistor is off.

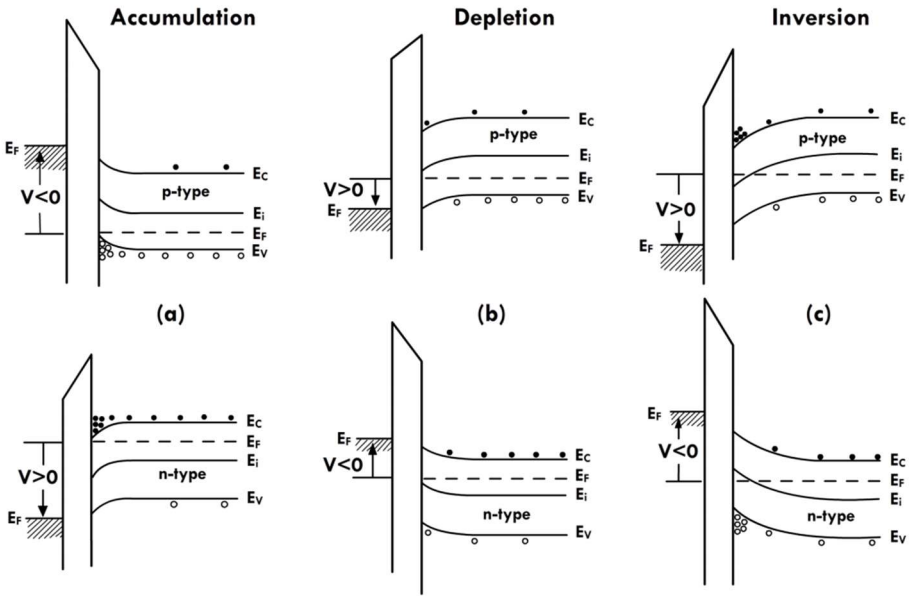



Figure 2.5. Metal Insulator Semiconductor (MIS) Energy Band Diagram [9]

However, if the opposite bias voltage is high enough, it is possible to move the conduction band of the p-type semiconductor downward until it lies below the Fermi level, and as a result, minority charge carriers (electrons) are harvested at the insulator/semiconductor interface. For an n-type semiconductor, holes are harvested. This condition is called inversion mode, and transistor is switched on.

Flat band, accumulation and depletion often occurs in OTFTs, while inversion mode rarely occurs due to the low density of minority charge carriers and large band gap [10]. Thus, inversion mode is not often used in OTFTs. In this project, all transistors are used in the range depletion mode, flat band, to accumulation with the transistor turned on in accumulation mode [9, 11-13].

### 2.2.2 Structure and Manufacturing of OTFT

OTFTs are often manufactured with the layer-stacking principle, and there are four main architectures of OTFT, as shown in figure 2.6, bottom-gate top-contact (BGTC), bottom-gate bottom contact (BGBG), top-gate bottom contact (TGBC) and top-gate top contact (TGTC). There are two major classes of fabrication process to print OTFT, solution methods and vacuum methods.

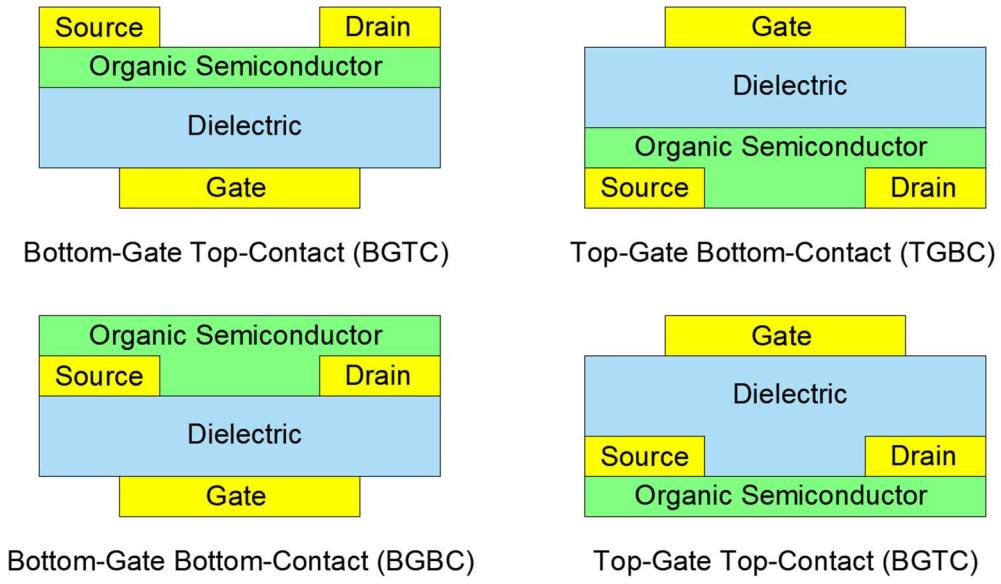



Figure 2.6. Architectures of OTFTs

#### 2.2.2.1 Solution-based Process

Solution processes include drop-casting, spin-coating, ink-jet printing, screen printing and gravure printing. Both small molecule semiconductors and polymer semiconductors can be printed by solution processing under ambient environment. Because the morphology of the semiconductor is solvent-dependent, the resulting semiconductors exhibit various performances. To control the performance of OTFTs made from solution process, there are a series of parameters that need to be controlled precisely, such as solvent polarity, viscosity, temperature and inter-layer penetration. More importantly, synthesis of conductive ink for solution processing is very expensive, consequently, high cost of parameter controlling and materials preparation with low yield makes this method less cost-effective [14, 15].

#### 2.2.2.2 Vacuum-based Process

Vacuum processes, such physical vapour deposition (PVD), chemical vapour deposition (CVD) and pulsed laser deposition (PLD) are often used to create thin film semiconductors for organic electronics. The mechanism of vacuum deposition is to transfer objective materials directly from source solid or liquid to the substrate in a vacuum chamber. Compared with parameters in solution-based processes, critical parameters to determine the morphology of semiconductors in vacuum-based process are simpler: deposition rate, vacuum degree, and overall thickness of semiconductor layer. However, the requirement for vacuum degree is high, usually less than $10^{-5}$ mbar, and the deposition rate needs to be sufficiently slow to guarantee uniformity, and, these characteristics increase the production cost [16, 17].

### 2.2.3 Characterisation of OTFT and Parameter Estimation

The behaviour of OTFT can be described by Horowitz's model [18]. The details of the model assumptions and derivations are described in the Appendix, and the relationship between bias gate voltage and output current is illustrated by equation 1,

$$I_D = \frac{W}{L}\mu C_i\left[\left(V_G - V_{FB} + \frac{n_0 qt}{C_i}\right)V_D - \frac{V_D^2}{2}\right] \ldots\ldots (2.1)$$

where, $I_D/A$ is Drain Current

$W/mm$ is width of channel, i.e. the distance between source and drain

$L/\mu m$ is length of channel

$\mu/cm^2V^{-1}s^{-1}$ is field-effect mobility of charge carrier

$C_i$ $/nF.cm^{-2}$ is capacitance in unit area

$V_G/V$ is gate voltage

$V_{FB}/V$ is flat band potential that represent the difference of work function between semiconductor and gate metal

$n_o/\mathrm{cm}^{-3}$ is the density of free charge in materials

$t/nm$ is thickness of semiconductor

$V_D/V$ is drain voltage

The threshold voltage ($V_{TH}$) is defined as $V_{TH} = V_{FB} - \frac{n_o q}{C_i}$, so the equation can be simplified:

$$I_D = \frac{W}{L}\mu C_i\left[(V_G - V_{TH})V_D - \frac{V_D^2}{2}\right] \ldots\ldots (2.2)$$

When $|V_D| \ll |V_G - V_{TH}|$, i.e. in the linear regime, and equation (2.2) can be approximated as:

$$I_D = \frac{W}{L}\mu C_i(V_G - V_{TH})V_D \ldots\ldots (2.3)$$

When $|V_D| \geq |V_G - V_{TH}|$, i.e., in the saturation regime, equation (2.2) can be approximated as:

$$I_D = \frac{W}{L}\mu C_i(V_G - V_{TH})^2 \ldots\ldots (2.4)$$

Plotting $I_D^{1/2}$ against $V_G$, a straight line can be obtained over some range of voltage in the saturation regime. The slope value can be used to calculate the mobility of charge carriers and extrapolating this line to the intersect with axis of gate voltage, this intersection indicates the threshold voltage, shown in Figure 2.7.

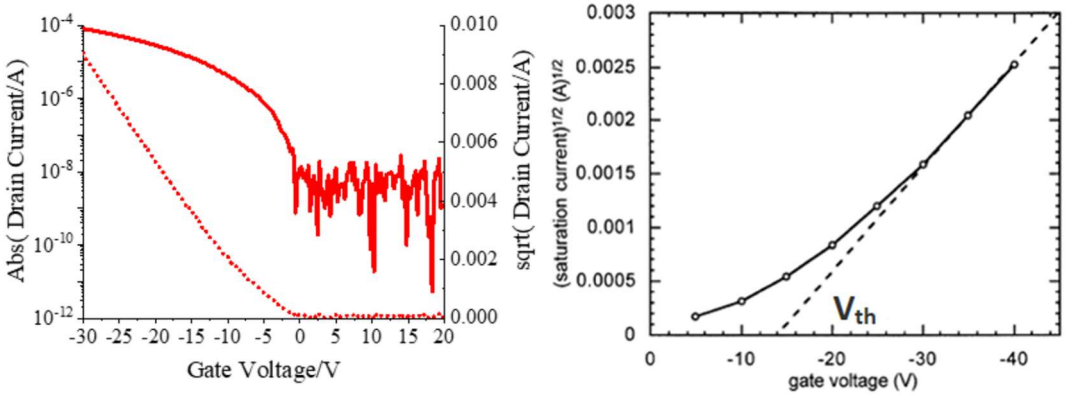



Figure 2.7. Transfer Curve of OTFT (left) and Relationship of $I_D^{1/2}$ against $V_G$ (right) [18]

Compared with inorganic transistors, for example, Si MOSFET, OTFTs, fabricated with dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT), exhibit a large band gap, a lower mobility, a higher threshold voltage, and smaller On/Off ratio [19], displayed in table 2.1.

Table 2.1. Band Gap Comparison for Inorganic Semiconductor and Organic Semiconductor

| | Inorganic Semiconductor [20-24] | | | Organic Semiconductor [25-30] | | |
|---|---|---|---|---|---|---|
| Name | Si | GaAs | Ge | P3HT | Pentacene | DNTT |
| Band Gap/eV | 1.14 | 1.43 | 0.67 | 1.9 | 1.84 | 3.2 |
| Mobility/ ($cm^2$/Vs) | 450 (Electron) | 400 (Hole) | 1900 (Hole) | 0.1 (Hole) | 5 (Hole) | 2.1 (Hole) |
| On/Off Ratio | $10^8$ | $10^7$~$10^8$ | 2 x $10^6$ | $10^3$~$10^5$ | $10^5$ | $10^6$ |

### 2.2.4 Stabilization and Degradation of OTFT

The stability of organic semiconductors is a limitation to the application of OTFT due to the sensitivity of OSC to temperature, illumination, oxygen and moisture.

In an ambient environment, the effect of oxygen is an important factor for the performance of an OTFT. When p-type semiconductors (pentacene or DNTT) are exposed to air, oxygen can diffuse along the grain boundaries of the poly-crystalline semiconductor and reach the dielectric/semiconductor interface close to which is the conducting channel when the device is switched on. When oxygen adsorbs onto grains of the semiconductor, electrons in the semiconductor are extracted because oxygen atoms have a high electron affinity, and as a result, the concentration of holes is increased. Equivalently, oxygen acts as a p-type dopant and reduces the distance

between the valence band and the Fermi level. Notably, the doping effect is physically reversible, i.e. there is no chemical reaction with the materials. After an exposure to high vacuum or inert atmosphere, oxygen dissociates from the semiconductor without deteriorating the chemical structure of the semiconductors [31]. Consequently, in the transistor manufactured by e.g., pentacene or DNTT, for a short period of oxygen exposure, mobility increases and threshold voltage decreases. It has been shown that in pentacene-based transistors, there is also a permanent, long-term oxidation that is a detrimental factor for their performance and lifetime. It has been shown that oxidation creates defects by formation of carbon-oxygen double bond, i.e., deteriorating conjugated structure of pentacene. As a result, the activation energy to create free holes increases and mobility decreases [32, 33]. However, the degradation of DNTT in air is significantly slower than pentacene due to its more stable chemical structure, so DNTT is more reliable than pentacene in the long term, as shown in figure 2.8. In contrast, n-type semiconductors will tend to exhibit a substantial instability because their LUMO energy is not sufficiently low to prevent the reaction of $O_2(H_2O)_n$ complexes, which act as traps in the semiconductor. Thermodynamically, improving the electron affinity of the semiconductor above 3.6 eV can address the instability, while this instability can be reduced or limited by improving crystallinity, i.e., reducing grain boundary to avoid diffusion of oxygen [34, 35]. Currently, the instability of n-type organic semiconductors hinders their application. As a result, circuit design is also affected because optimal signal processing circuits often combine multiple p-type and n-type transistors.

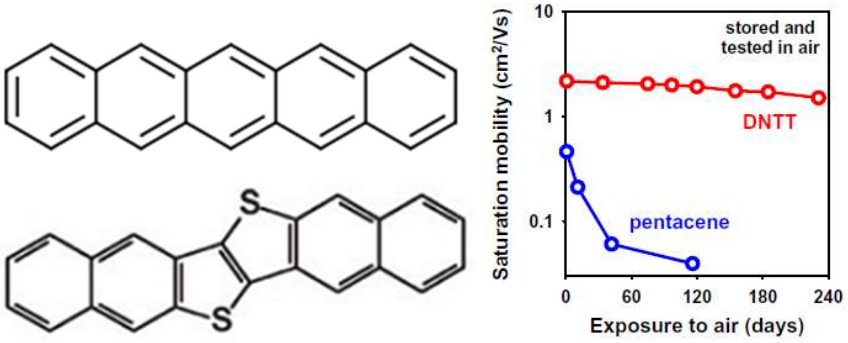



Figure 2.8. Structure (left) and Degradation (right) of pentacene and DNTT [29]

For an oxidation-resistant organic semiconductor, the effect of humidity on the semiconductor is reversible, and this character is often used in humidity sensors, which will be discussed in section 2.3.1 [36]. Under negative bias voltage, the contact-gate electric field helps polar water molecules to diffuse to the dielectric/semiconductor interface, and water molecules align themselves along the direction of electric field, i.e., with a positive dipole toward the insulator and negative dipole toward the semiconductor. For a p-type OTFT, when holes pass through the conducting channel, they are attracted by the negative dipoles of the water molecules. On reducing the gate voltage ($|V_G| \rightarrow 0$), conductive holes are released and the current increases. With the presence of water molecules, the current is determined by the balance between binding and releasing of water molecules to charge carriers under different gate voltage or water concentration, shown in figure 2.9 [37, 38]. In this project, a p-type semiconductor, DNTT, is used, and it exhibits a reversible response to moisture [16]. When the OTFT is in a dry environment, water molecules can be released from the dielectric/semiconductor interface, and as a result, performance of the OTFT recovers. However, for an organic semiconductor that is unstable in oxygen, for example, n-type organic semiconductor, $N,N' - bis(2,2,3,4,4,4 - heptafluorobutyl - 1,7 - dicyano - perylene - (3,4:9,10) - tetracarboxylic\ diimide$ (PDI-$FCN_2$),

humid air is detrimental due to its irreversible reaction route, $O_2 + 2H_2O + 4e^- \rightarrow 4OH^-$ in which hydroxide ions act as traps for electrons. Consequently, electron mobility decreases irreversibly, and the threshold voltage shifts toward a more positive region [39].

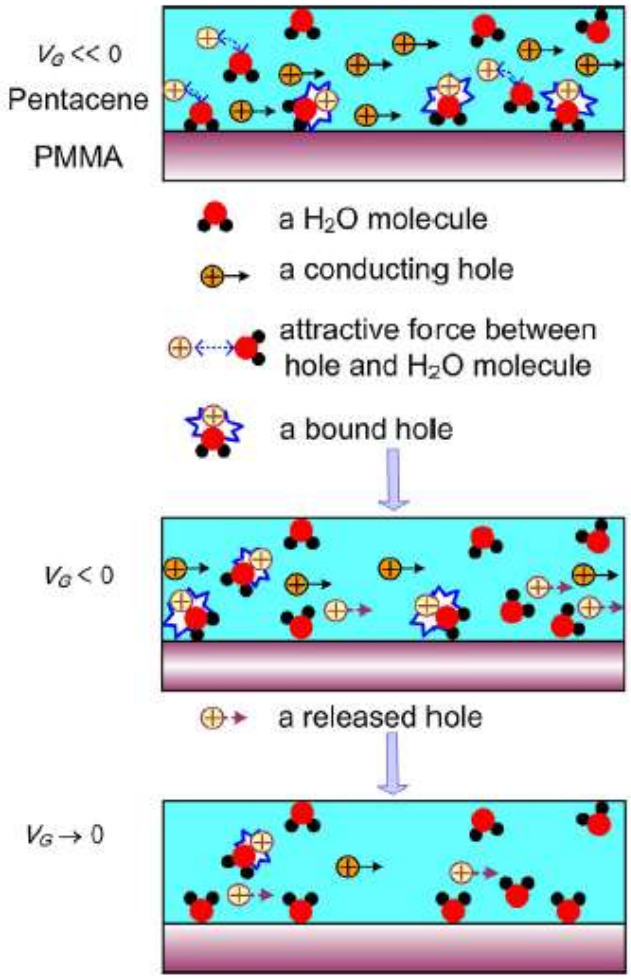



Figure 2.9. Schematic of Water Adsorption and Release on Dielectric/Semiconductor Interface [37]

Response to illumination is an intrinsic property for semiconductors. The extra photocurrent can help a device output a higher current, however, in the development of OTFT, this is considered as a source of instability. Photons from a light source

introduce electron-hole pairs in the semiconductor and then electrons and holes are separated under the electric field. For a p-type semiconductor, holes contribute to the drain current, and electrons accumulate at the semiconductor/dielectric interface. As a result, the extra holes lead to photoconductive effect and accumulated electrons leads to photovoltaic effect [40, 41]. However, organic semiconductors are relatively insensitive to a range of wavelengths, and photocurrent disappears when the light source is removed. In addition, the increment of photocurrent is non-linearly correlated to increase of luminance. Overall, this effect can be alleviated by keeping the OTFT in a dark environment and by using short-time bias with sufficient time for recovery [42].

### 2.2.5 Bias Stress on Thin Film Device

Bias stress is an intrinsic property of thin film transistors, which leads to an instability in output current. Although this instability is a recoverable process, it still limits the application of OTFTs under high voltage and long-time bias. When thin film transistors are biased, the threshold voltage of devices starts increasing, and as a result, drain current decay occurs.

A general description of the bias stress mechanism is that of charge carrier trapping, however, the details of the mechanism are not clearly concluded. Currently, there are some possible mechanisms identified: interaction at the back-channel region, intrinsic acceptor-like deep traps in the semiconductor, and trapping effects at the dielectric/semiconductor interface. In figure 2.10, the possible interaction at the back-channel region is demonstrated, however, the effect is less significant than the charge trapping effect [43].

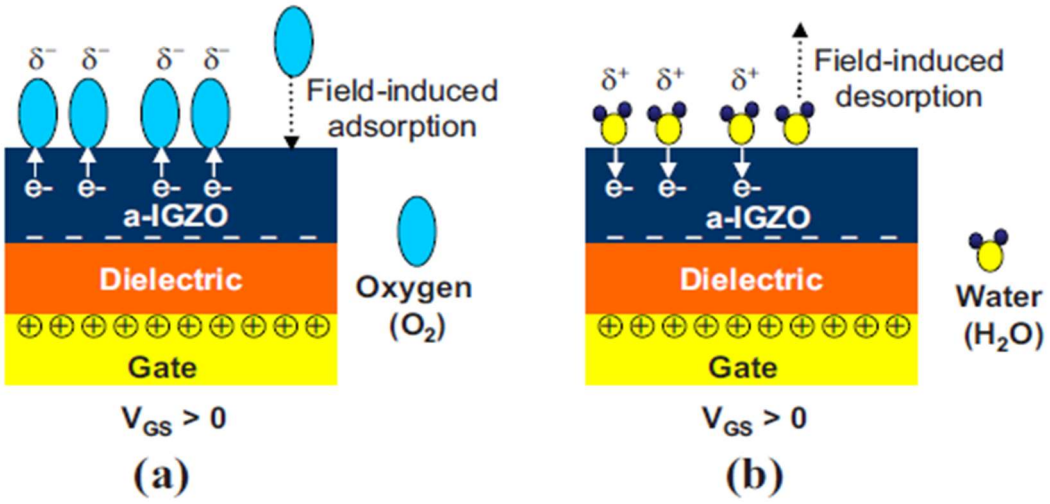



Figure 2.10. Schematic displaying the electric-field-induced adsorption of oxygen (a) and water (b) molecules from ambient environment under positive gate bias stress [43]

For poly-crystalline semiconductors in a thin film transistor, trapping states often exist widely, and can be divided into shallow traps and deep traps in which charge carries exhibit very low mobility. In the case of InGaZnO transistors, it is thought that shallow traps are associated with crystal defects, such as vacancies and grain boundaries, and can be removed by annealing. Deep traps are described as acceptor-like traps that combine with charge carriers, but the source of acceptor-like traps is still under exploration. A general conclusion is that both shallow traps and deep traps cause a threshold voltage shift under short-time and low voltage bias but deep traps dominate the threshold voltage shift with increasing bias voltage and time [44].

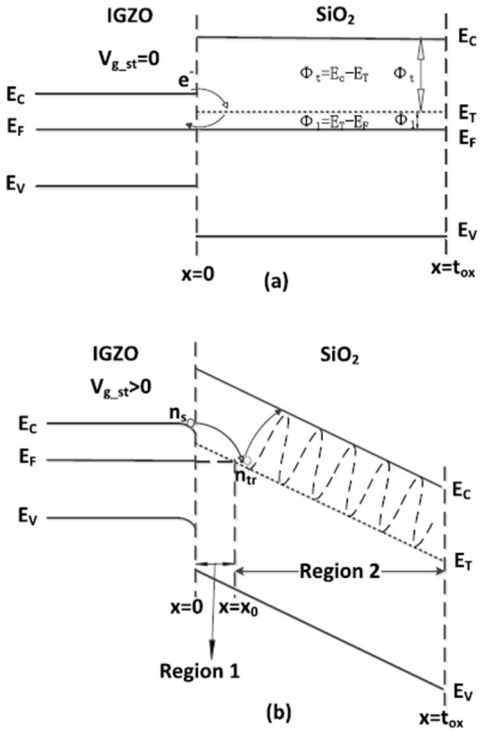



Figure 2.11. Energy band diagram for amorphous based InGaZnO thin film transistor under (a) zero bias and (b) positive bias [45]

By contrast, charge trap states in the dielectric materials are shown in some research to be the major reason for current decay [45-48]. When transistors are biased for a long time, the electric field between source/drain and gate drives charge carriers to tunnel into dielectric materials close to the interface and then into deeper positions by Poole-Frankel (PF) conduction. In the dielectric materials, there are two trapping regions, the first region close to semiconductor interface is called shallow region, in which trapped charge carriers can revert to the semiconductor, while in the second, deep region, further from the interface, it is not possible for charge carrier to tunnel back, illustrated in figure 2.11. Although this model is still in debate, a novel method to reduce charge carrier tunnelling effect was published in [47], showing that adjusting thickness of the buffer layer that passivates the polar group in dielectric materials is helpful to alleviate

current decay. It is a convincing support for the mechanism of charging trap states in dielectric materials. Although the electric field between source/drain and gate is dominant for bias stress, the electric field from source to drain is also shown to contribute to the current decay as the injection of charge carriers at contact/semiconductor is observed to exhibit time-dependent variance [49].

## 2.3 Introduction to Conventional OTFT-based Sensors

With the growing market for health care and personal monitoring products, the demands for portable and wearable sensors is increasing. Compared with conventional sensors, OTFT-based sensors exhibit several advantages, such as flexibility and low cost. This section will introduce the developments to date of OTFT-based sensors and analyse the limitations of the most recent OTFT-based sensors. Afterwards, a novel sensing structure, based on a floating gate approach and its application with different functionalization materials will be discussed.

Conventional OTFT sensing design is dependent on the reaction of the organic semiconductor with target analytes. Organic Field Effect Transistors (OFETs) and Organic Electrochemical Transistors (OECTs) can be transformed to ion sensitive sensors and electrochemical sensors respectively. The output current signal is affected by a shift of the effective bias voltage caused by the interaction between the semiconductor and analytes, for example shown in figure 2.12.

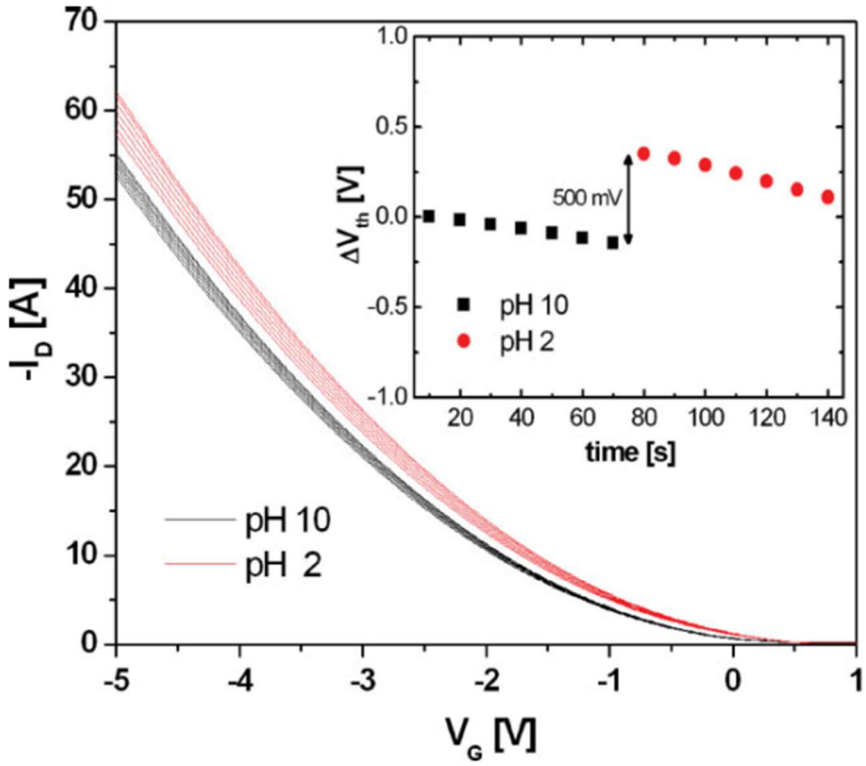



Figure 2.12. Transfer Curve shift before (redo circle) and after Sensing Reaction (green triangle) [50]

### 2.3.1 Ionic Interaction Mechanism of OFET

The architecture of a typical OFET sensor is shown in figure 2.13. The ionic interaction occurs on the organic semiconductor, directly trapping charge carriers by polar interactions or hydrogen bonding with the semiconductor, and the consequent change in overall conductivity in the channel affects output current [36]. Alternatively, ionic interactions occurring at the interface between the dielectric material and a testing solution modifies the dielectric materials. When the concentration of analytes varies, the overall dielectric constant is changed as well, and as a result, the actual bias voltage is shifted and output current is altered [51, 52].

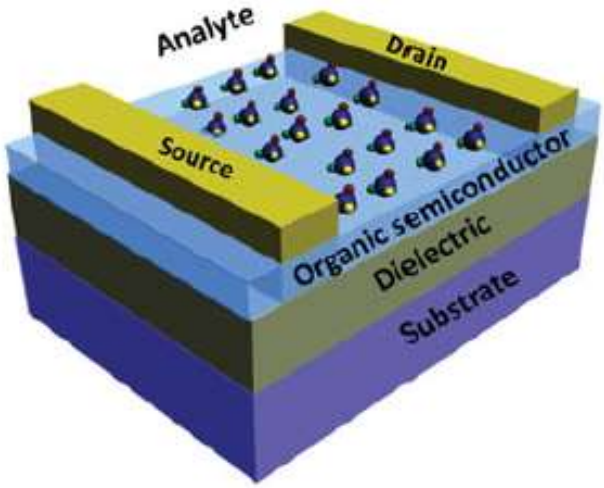



Figure 2.13. Architecture of OFET based sensors [36]

For p-type organic semiconductors, their intrinsic sensitivity to water enables their application as a humidity sensor. Although adsorption of water molecules is reversible in OTFTs, there is a limited range of humidity for the sensor; for example, P3HT is available for humidity from 0 – 40 % and pentacene works well for humidity from 30 – 75 %. When moisture in the environment is too high, some irreversible reaction, for example, electrolysis of water, occurs and deteriorates the semiconductor, finally, leading to failure of devices [53-55]. However, any polar species in the analyte that interacts with the semiconductor would also contribute to the signal, making selectivity of the sensor limited.

Detection of ionic reactions by OFET usually uses a principle of charge redistribution, with the analyte solution directly contacting the dielectric materials, shown in figure 2.14, and the device is often fabricated with a top gate bottom contact structure. When a reference electrode is used to apply a driving voltage to the solution, the output drain current is expected to vary with concentration of solution on the dielectric materials [50, 56-59]. However, it is difficult to achieve high selectivity because most ionic

analytes exhibit a quick response under driving voltage. Although application of a Langmuir – Blodgett (LB) film on dielectric materials achieve selectivity to hydrogen ion and enabled a pH sensing function in the range 3.5 – 5.5 [51, 52], it is difficult to realize ionic selectivity to many ions.

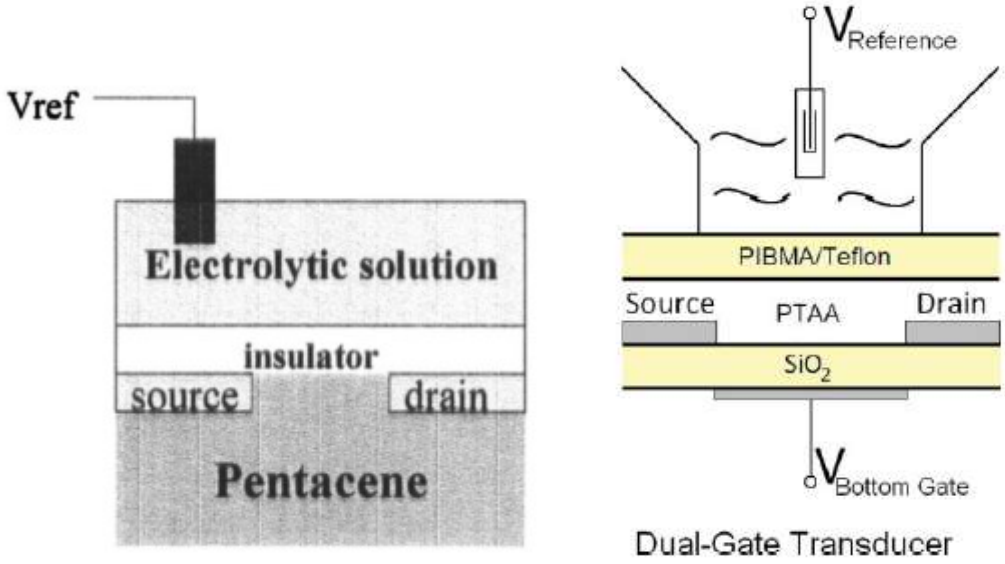



Figure 2.14. Structure of Hydrogen Sensor based Pentacene (L) [59] and Dual-Gate Hydrogen Sensor (R) [50]

Glucose detection is important for diabetics, and a glucose sensor can be fabricated with functionalization of the gate dielectric with the enzyme glucose oxidase. The catalytic reaction of glucose can produce gluconic acid or release hydrogen ions altering the overall ionic conductance of the solution. Consequently, the output drain current of the OTFT will be altered due to the shift of effective bias voltage (described above) [56].

Electrolyte gated OFETs have a similar structure to the OFET sensor with functional materials coated on dielectric materials, or functional materials applied directly on organic semiconductor to realize higher selectivity. It is shown that coating a layer of

anti-C-reactive protein (CRP) monoclonal antibody onto the surface of P3HT by physical adsorption is helpful to detect the concentration of CRP in solution, shown in figure 2.15 [60], because the antibody is capable to selectively recognize the CRP, i.e. realizing a selective electronic transduction.

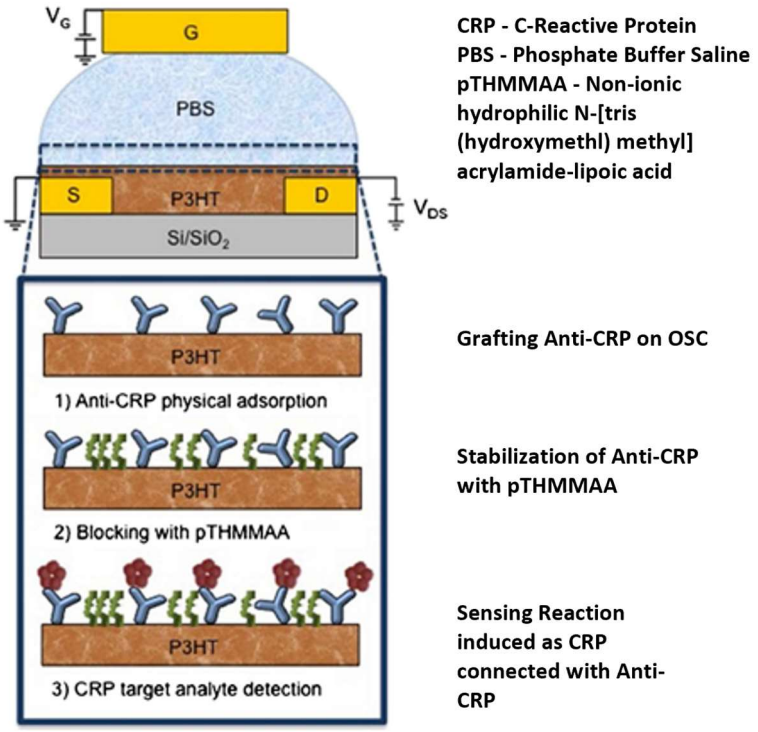



Figure 2.15. Structure of CRP-antibody Coated P3HT OFET [60]

The advantages of OFET sensors are the sensitivity from the rapid current response of transistor to gate voltage, which usually has a significant increment when the device is switched on and the direct contact architecture which is easy to fabricate. However, the stability of the organic semiconductor limits the sensitivity to ionic reactions because it causes less damage to the OSC than electrochemical reactions. In addition, the selectivity is limited due to the difficulty to functionalize the OSC while maintaining good electronic properties and the lifetime of OSC will be reduced over time because no encapsulation can be applied.

### 2.3.2 Electrochemical Mechanism on OECT

OECT-based sensors are fabricated with a structure of direct contact between the electrolyte and the organic semiconductor, shown in figure 2.16. When there is no bias voltage, there is a highly conductive channel between the source and drain electrodes, and high current can pass through the active materials, i.e., device is switched "ON". However, when the gate electrode is positively or negatively biased, anions or cations can diffuse towards the semiconductor under the electric field, therefore, the density of charge carriers in semiconductors is changed by a doping/de-doping mechanism or redox reaction, altering its conductivity in the channel region. As a result, an appropriate bias on the drain electrode can make the device work as a transistor on which drain current varies with concentration of analytes [61, 62].

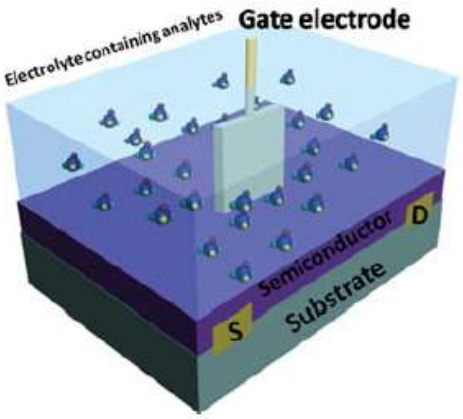



Figure 2.16. Architecture of OECT based sensors [36]

PEDOT: PSS is often selected as the sensitive material on OECT because the reversible electrochemical reaction, $PEDOT{\cdot}PSS + e^- + M^+ \Leftrightarrow PEDOT + M{:}\ PSS$. Without bias voltage, PEDOT: PSS is a good conductor (electrode), while semiconducting behaviour is exhibited after application of a bias voltage.

An OECT-based humidity sensor was developed when PEDOT: PSS was combined with Nafion film. The state of the PEDOT: PSS depends on the cation migration rate through the Nafion film; thus, variance of humidity will be transduced by the OECT measured by the variance of drain current [62-65]. In addition, the reaction of free ions in solution can act as a dopant for PEDOT: PSS to alter its mobility and the output drain current, shown in figure 2.17. To obtain selectivity to specific ions, PEDOT: PSS can be functionalized with a selective membrane, for example, potassium ionphore I (valinomycin), calcium ionphore II and silver ionophore can be used to detect concentration of $K^+$, $Ca^{2+}$ and $Ag^+$ respectively [66].

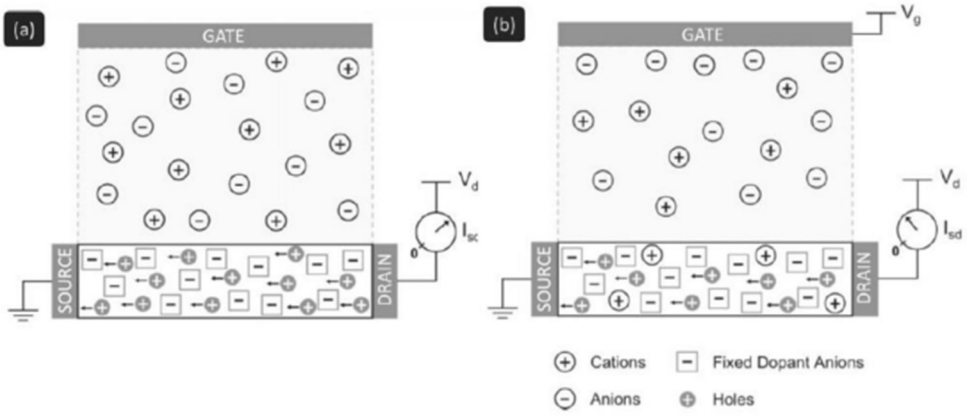



Figure 2.17. Sensing Mechanism of OECT before (a) and after bias (b) [67]

Due to the redox reaction of PEDOT: PSS, an integrating mechanism of electrochemical reaction can be realized, for example, the oxidisation of ascorbic acid occurs on PEDOT: PSS and alters the doping condition of PEDOT: PSS, finally reflected by the variance of drain current [68].

Although OECT is capable to sense electrochemical reactions, as with OFET, the direct contact structure and stability of OSC still limits the accuracy and lifetime of sensor.

## 2.4 Floating Gate Structure and Sensor Application with Ferroelectric Polymer

A floating gate (FG) is an additional electrode on a transistors that is electrically isolated by insulating materials from the bias gate (BG) electrode and contact electrodes. In this way, the FG and BG form a capacitor, and any charge variance inside this capacitor can indirectly alter the output of devices. In this section, the structure of FG-OTFT will be illustrated and a simple ferroelectric sensing mechanism with FG-OTFT will be discussed. Compared with the direct contact structures described above, the advantage of the FG-OTFT sensor is that damage to the OSC can be avoided, indeed the transistor element can be encapsulated from contact with the air or analyte and the structure gives more options for functionalization of floating gate instead of needing to functionalize the active components (OSC) to realize selectivity. However, the structure of FG-OTFT is more complex than the normal single OTFT, increasing the difficulty of fabrication.

### 2.4.1 Structure and Working Principle of a Floating Gate Transistor

A comparison of the structure of a conventional Metal Oxide Semiconductor Field Transistor (MOSFET) with a Floating Gate Metal Oxide Semiconductor Field Transistor (FG-MOSFET) is displayed in figure 2.18 (a) and (c). The floating gate acts as charge storage component on FG-MOSFET. As the total amount of electrical charge on the FG varies, it will be indicated by a change of output current through the transistor. There are two fundamental physical phenomena behind the FG structure, hot carrier injection and Fowler-Nordheim (F-N) tunnelling [69]. When a floating gate is initially biased under high voltage, hot carrier injection from the control gate (bias

gate) to floating gate occurs and the energy state of the floating gate is shifted due to charging. As a result, FG-MOSFET is switched to a charged state without losing any charge as long as there is no external electric field to allow discharge. In fact, charge leakage is unavoidable over time even it is very slow. The presence of F-N tunnelling enables FG-MOSFET to be reprogrammable, i.e., the energy state of FG can be altered by an external electric field [70, 71]. In the electronic market, the floating gate structure is widely used in non-volatile memory, such as flash memory and electrically erasable and programmable read-only memory (EEPROM). Usually, the charged state of FG-MOSFET is named as “Programmed” state or “ONE” state, and the discharged state is named as “Erased” stated or “ZERO” state. As a result, each FG-MOSFET can be fabricated as simple storage device, for example, a single-level cell, i.e., flash memory with one floating gate transistor can store one bit of information.

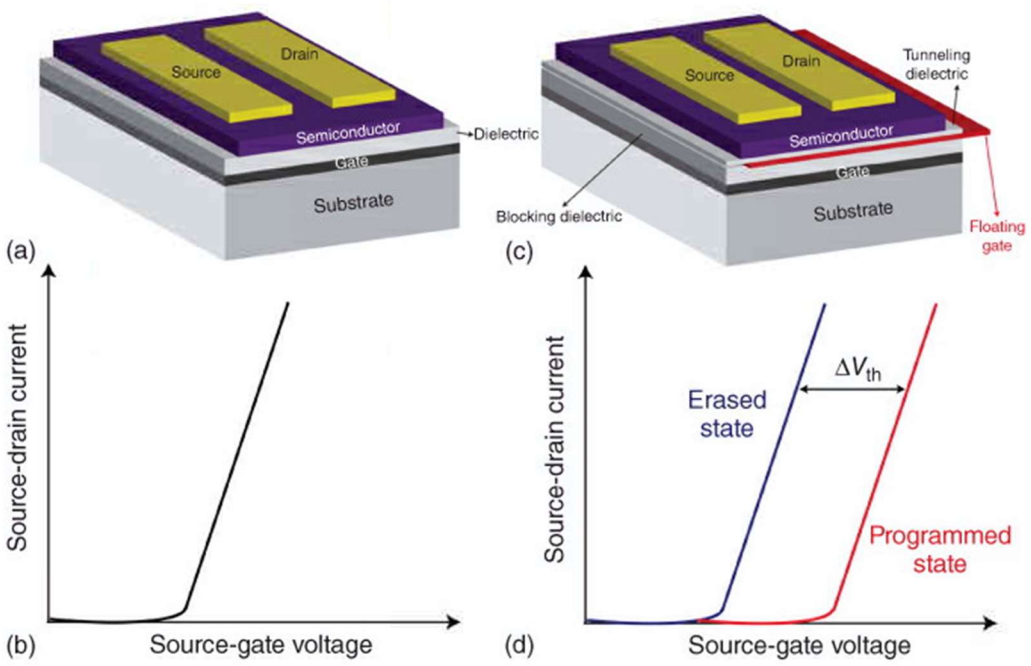



Figure 2.18. Comparison of MOSFET and FGMOSFET [70]

Because the output drain current of FG-transistors is dependent on the total amount of charge stored on the floating gate, shown in equation (4),

$$V_T^{FG} = \frac{C_{OX} + C_{FG}}{C_{FG}} V_T^{CG} - \frac{Q_{FG}}{C_{FG}} \dots\dots (4)$$

where, $V_T^{FG}$ and $V_T^{CG}$ are threshold voltage on floating gate and control gate, $C_{OX}$ and $C_{FG}$ are oxide capacitance on MOSFET and on floating gate, and $Q_{FG}$ is amount of electrical charge on floating gate, the bias voltage shift that affects the output drain current can linearly vary with change of total charge on floating gate, shown in figure 2.18 (b) and (d). Thus, with the charge sensitivity of FG-MOSFET, any charge generating, or charge-consuming reaction can be used to give signal on the FG-MOSFET, and it can be fabricated as an Ion Sensitive FET (ISFET), as shown in figure 2.19. The floating gate is under a solution and any ionic reaction leads to a shift of bias voltage on the transistor. With functionalization of the floating gate electrode with a selective membrane, it can be transformed to an ionic sensor, such as pH sensor with hydrogen ion selective materials [72], DNA sensor with functionalization of special biotinylated probe DNA [73], and cell monitor with functional materials sensitive to $Na^+$, $K^+$, and $Ca^{2+}$ [74].

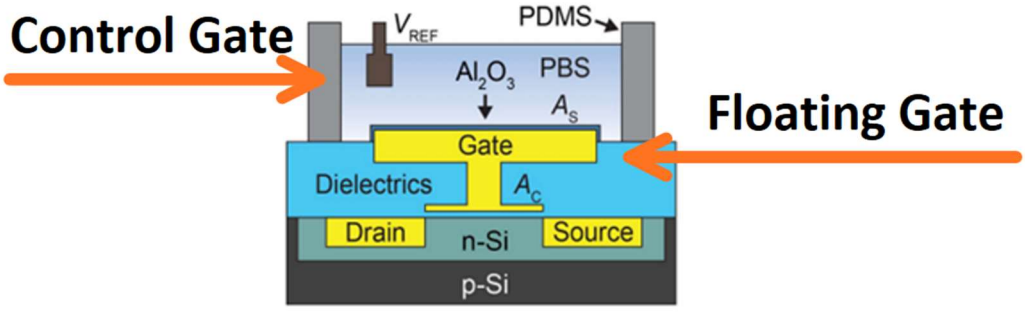



Figure 2.19. Ion Sensitive Sensor based on FG-MOSFET [73]

In this thesis, this principle of a FG-OTFT is used with the floating gate electrically coupled to the transistor but spatially displaced from it to allow the unstable organic semiconductor to be isolated from the analyte. Shown in figure 2.20, it allows maximum flexibility in modifications to the gate material to control selectivity of the device, without any such treatments affecting the transistor itself and encapsulation on OTFT can increase stability and lifetime.

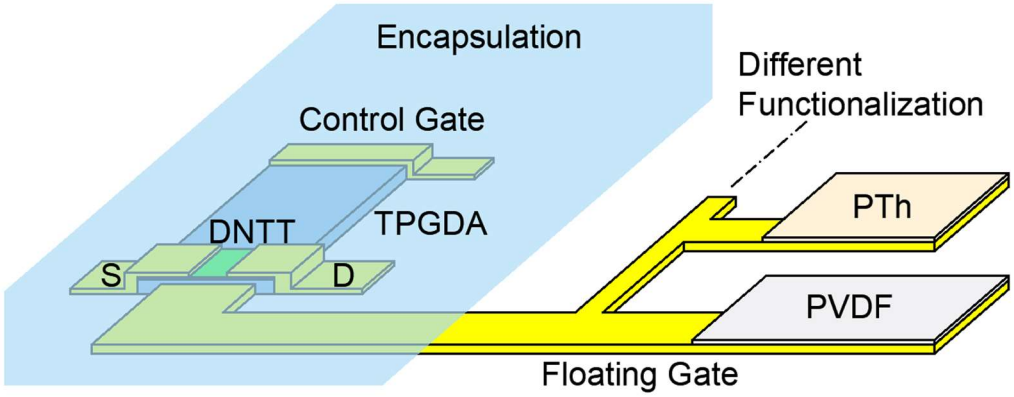



Figure 2.20. Schematic of FG-OTFT with Different Functionalization

### 2.4.2 Fabrication of a Ferroelectric Polymer Sensor

Due to the robust spontaneous electrical polarization of ferroelectric materials, they are widely applied in various fields, such as sensors and actuators. Poly-(vinylidene fluoride) (PVDF) is a promising ferroelectric polymer that can be fabricated as a thin film for sensor applications [75].

#### 2.4.2.1 Harvesting Ferroelectric Phase for PVDF

The source of ferroelectricity of PVDF is the phase with an all-trans conformation, i.e., β-phase, shown in figure 2.21.

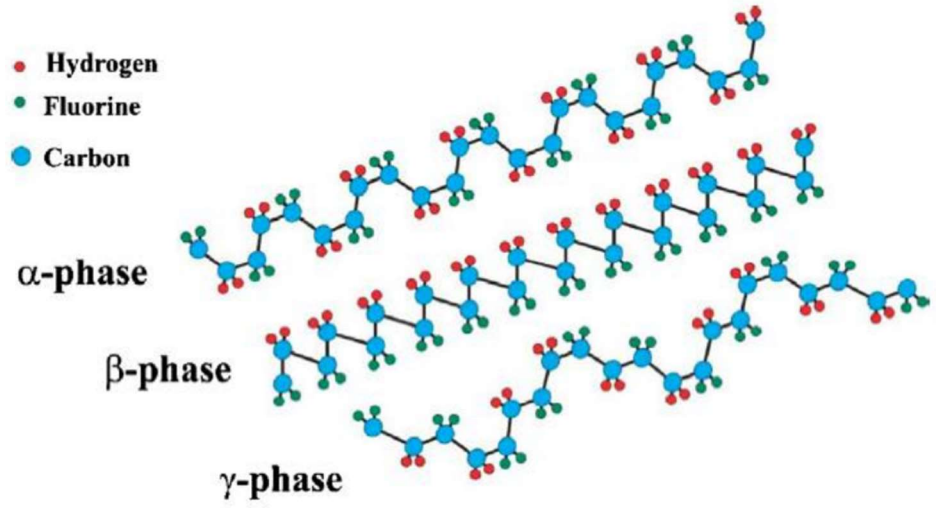



Figure 2.21. Structure of α-phase, β-phase, and γ-phase in PVDF [76]

Thermodynamically, the α-phase is a very stable phase at ambient temperature and pressure. It often forms when PVDF crystallises from the melt or solution because the α-phase has very low conformational energy, thermodynamically. However, the α-phase, with conformation TGTG' (T – trans, G – gauche$^{+}$ and G' – gauche$^{-}$), cannot exhibit piezoelectric properties, as the dipolar moment of successive chain units align antiparallel, leading to zero net dipolar moment in the crystal unit [77]. In contrast, the all-trans conformation has higher steric hindrance on the polymer chain, but it can be kinetically stabilised in ambient environment via stretching or poling, and the resulting β-phase PVDF crystals exhibit a ferroelectric effect because all polar groups are aligned to same direction [77, 78]. In addition, there are three less common phases (γ, δ, and ε) in PVDF. Thermodynamically, they are less stable than the α-phase, but can be stabilised kinetically by electrical pulses. The polarity of these three phases is less than the β-phase but higher than α-phase due to different arrangements of the polymer chains. Table 2.2 display a rough comparison of polarity for the different phases in PVDF.

Table 2.2. Comparison of Different Phase in PVDF under Ambient Environment

| Crystal Phase | Conformation | Polarity |
|---|---|---|
| α – Phase | TGTG'TGTG' | Low |
| β – Phase | TTTTTTTT | High |
| δ – Phase | TGTG'TGTG' | Intermediate |
| γ – Phase | TTTGTTTG' | Intermediate |
| ε – Phase | TTTGTTTG' | Intermediate |

There are two major routes to optimise the content of ferroelectric phase in PVDF. The first route is to encourage preferential formation of β-phase from the α-phase, for example, by mechanical stretching [77] [79]. The second route is to promote β-phase to form directly from the non-crystalline phase, i.e. amorphous phase or molten phase, e.g. by rapid quenching [80-83] and solution casting [84-90]. Based on these mechanisms, a series of methods to harvest β-phase have been investigated.

Mechanical stretching can directly transform the α-phase to β-phase. Li *et al*. demonstrated the detailed stretching mechanism of transformation, shown in figure 2.22, α-spherulites are gradually extended to β-crystals [77]. It is found that stretching at low temperature is helpful to form β-crystals due to the low mobility of polymer chains slowing down the recovery rate of polymer chains in this temperature region [79].

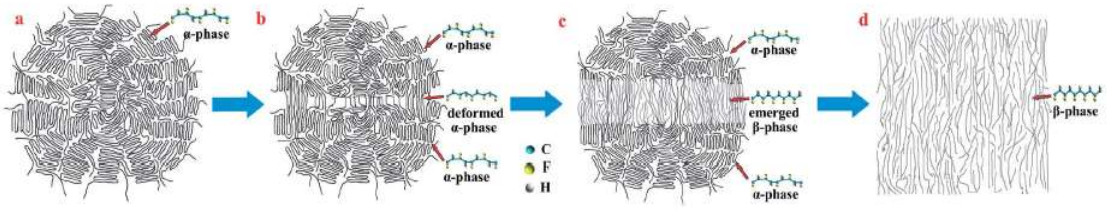



Figure 2.22. Formation of β-phase by stretching [77]

Rapid quenching under high pressure can induce direct formation of β-phase when molten PVDF is cooled down to low temperature. The content of β-phase increases with increasing quenching rate and decreasing quenching temperature [80, 81]. Hattori *et al*. indicated that high pressure, is helpful to form β-crystals that are resistant to the reverse transformation from β to α at elevated temperature [82, 83].

Solution casting can directly create β-phase by drop casting, spin-casting and dip coating techniques. It is demonstrated that solvent with higher dipole moment can facilitate formation of β-phase or γ-phase [84], and heated spin coating is helpful to promote more β-phase when drying spin-coated thin film [85, 86]. Electrospinning is helpful to directly produce β-phase and achieve polarisation during formation of a thin film [87, 88]. Langmuir-Blodgett deposition can produce PVDF nanofilm with high content of β-phase and achieve self-poling of PVDF without an electric field (Figure 2.23), repeating it to obtain film with sufficient thickness [89, 90].

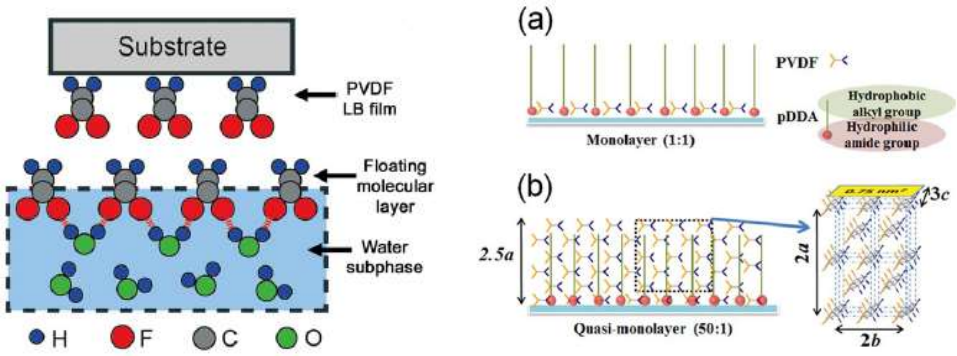



Figure 2.23. Deposition of PVDF nanofilm [89, 90]

Composition control is the modification of the structure of polymer chains to increase thermodynamic driving force to form β-phase. Copolymerisation with Trifluoroethylene (TrFE) [91-93] or chloride trifluoride ethylene (CTFE) [76, 94, 95], shown in figure 2.24, is beneficial to form β-phase from solution or amorphous phase.

However, regularity of the molecular chain is reduced as more TrFE or CTFE units are added, leading to lower crystallinity and lower Curie temperature, hence there is a critical to compromise between content of β-phase and crystallinity.

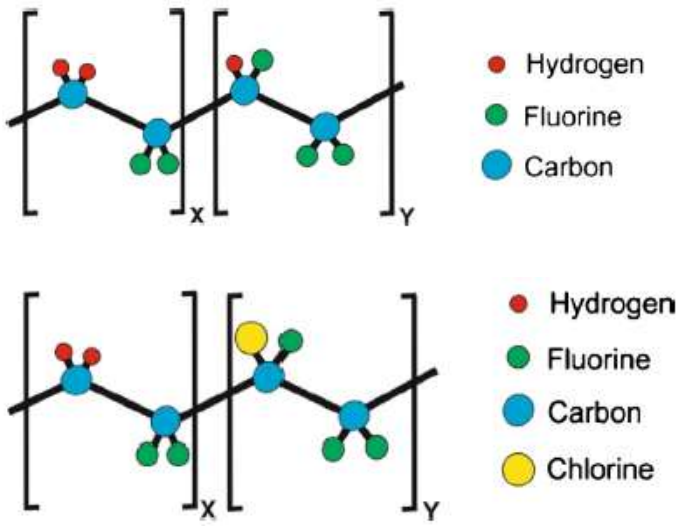



Figure 2.24. Structure of Poly-(VDF-TrFE) and Poly-(VDF-CTFE) [76]

#### 2.4.2.2 Activation of Ferroelectric Phase

For most ferroelectric materials, polar vectors are distributed randomly when it is initially made, and an overall ferroelectric property is activated after polarisation under high electric field. Differently from ferroelectric ceramics, in which the alignment of polar vector is dependent on lattice distortions, polarisation of PVDF takes place via a cooperative diffusion process of lamella crystals surrounded by amorphous phase material, i.e., conformational changes in the amorphous phase allows motion of crystal lamellae, with most domains along a direction close to the direction of poling electric field. In terms of poling technique, electric poling is a widely used method [96-99], and sometimes mechanical stretching or elevated temperature accompanies the electric poling [91, 100-102].

Electric poling is the application of a strong electric field on PVDF materials to align the orientation of polar vector. A simple method to achieve this is by applying a thin film electrode on either side of the PVDF and applying a constant voltage across the electrodes [97]. Alternatively, poling can be achieved by placing PVDF materials under a Corona field or high voltage plasma [98, 99].

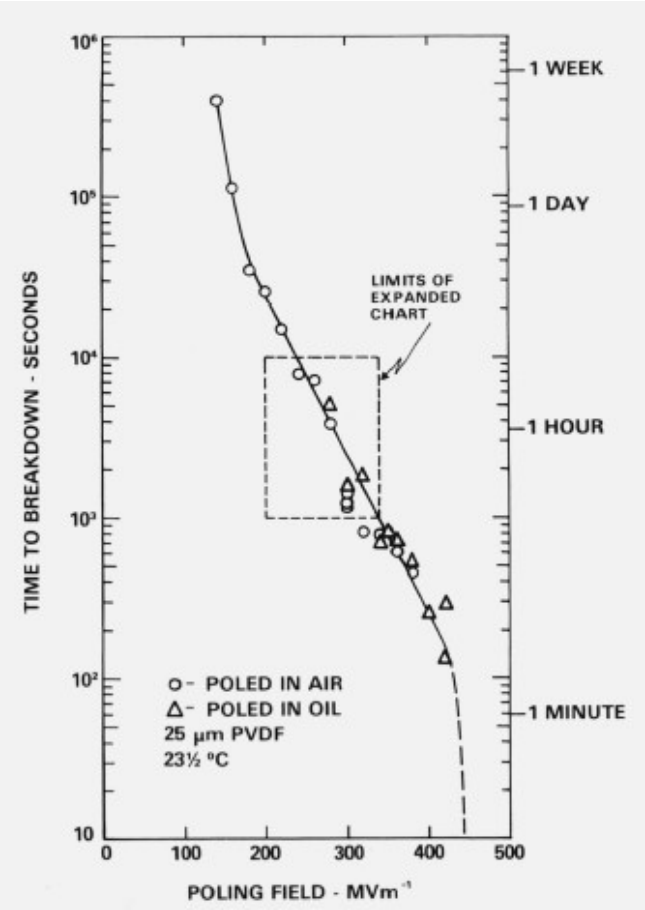



Figure 2.25. Relationship between Poling Field and Poling Time [97]

In figure 2.25, a relationship between poling electric field and poling time is displayed. Based on this relationship, polarisation can be optimised to obtain materials of high ferroelectricity with low risk of damage. During electric poling, applying suitable mechanical stress and temperature is helpful for the cooperative diffusion of PVDF lamella, and facilitating orientation of polar vector [100, 101].

### 2.4.3 Sensor Application of PVDF on OTFT

Because of ferroelectricity, PVDF or P(VDF-TrFE) is often directly fabricated as a capacitor, and the electrodes on the top and bottom of PVDF are connected to signal processing devices. Due to compatibility with thin film processing techniques, a PVDF capacitor is often made as a flexible sensor to detect mechanical strain, especially in the field of health care, for example, it is used as skin-touch sensor to extract heart rate signal [103], shown in figure 2.26.

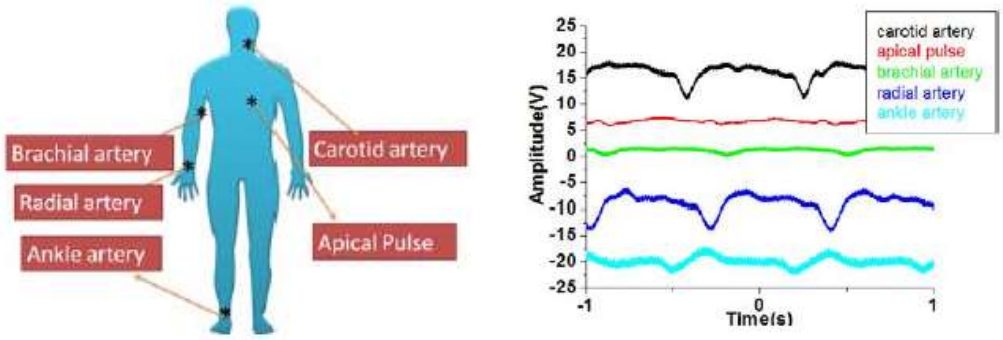



Figure 2.26. Pulse Sensor location and generated signal [103]

In addition, ferroelectric PVDF can be processed as a fibre that contains an inner electrode for polarisation. Fibres are poled and woven into fabric with a conductive electrode. It can achieve detection of heart rate when it is attached to the chest [104].

Because of the highly sensitive response of PVDF to micro mechanical motion, the sensing application of PVDF can be extended by coupling with coating materials which exhibit a volume response. For example, when hydrogen gas adsorbs onto palladium, the micro-strain caused by the resulting significant volume expansion results in ferroelectricity on PVDF and then the signal can be captured by a signal processing device [105]. In a similar way, modification of PVDF with hydrogel is

helpful to transform it to a humidity sensor, but detecting the strain induced by the expansion of the hydrogel by water [106].

Due to the small output signal from the PVDF sensor, a high-accuracy signal processing device is required to cooperate with PVDF sensor to build a sensing system. Although a conventional signal processing device, for example, signal amplifier, is accurate, it is often based on a Si chip without any flexibility making it difficult to integrate with a fully-flexible wearable device. With the development of OTFT, it is a worthwhile trial to integrate PVDF with OTFT to amplify the signal in order to achieve a flexible and wearable sensing system.

Because a single OTFT can be used as a signal amplifier, a direct way to connect OTFT with PVDF is to use the PVDF as part of the dielectric materials in OTFT, shown in figure 2.27. When mechanical strain induces a ferroelectric reaction on PVDF, the charge imbalance will lead to a bias voltage shift, which then alters the output current [106-108]. Because ferroelectric PVDF is sensitive to temperature, i.e., pyroelectric effect, this thin film sensor can also be used as a temperature sensor on the human body.

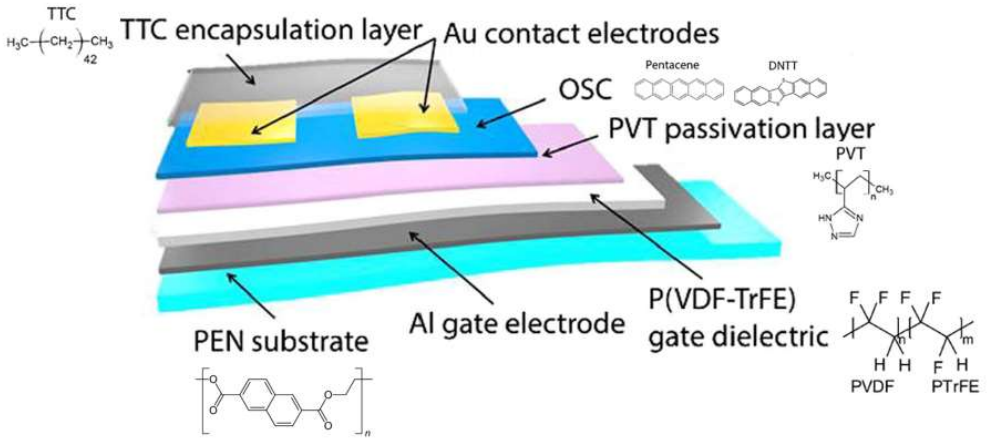



Figure 2.27. Structure of P(VDF-TrFE) gated strain sensor [106]

Another architecture to integrate PVDF and OTFT is a floating gate structure, as the output current of a FG-OTFT is sensitive to the charge on the FG, so PVDF thin film deposited on the FG is a direct way to transfer the charge imbalance from PVDF to the OTFT. One electrode of the PVDF capacitor is connected to the floating gate of FG-OTFT, and the electrode is kept floating to air. When a dynamic cyclic mechanical stress is applied on the PVDF sensor, the output signal exhibits signal variance with the same frequency, i.e. a signal of mechanical strain variance is extracted [109]. In a similar way, applying a temperature variance on PVDF, FG-OTFT can detect the signal of temperature variance as well [110].

## 2.5 Design and Fabrication of OTFT-based Signal Conditioning Circuit

With development of organic thin film transistors, circuits based on OTFTs have been fabricated to achieve different signal processing functions. Signals can be analogue or digital. An analogue signal is a continuously varying signal, whereby most physical signals are analogue, for example, encoded radio waves. However, it is often convenient to discretize it to digital signal which describes any signal in a binary representation, i.e., discretize signal into state “ZERO” and state “ONE”. Depending on the nature of the physical signal, analogue and digital circuits are fabricated to process and visualize signals. Analogue circuits are often used to operate directly on an original continuous signal and achieve different processing, such as voltage-to-voltage amplification, current-voltage conversion and analogue-to-digital conversion. However, digital circuits can only operate on discrete signals and work as a processor to finish logical or mathematical calculation [111].

### 2.5.1 Review of OTFT-based Functional Circuits

Because the signal processing capability of a single OTFT is limited (voltage input and current output), an integrated circuit enables more functions, such as current-to-current amplification, voltage-to-voltage amplification, and current-to-voltage conversion. A functional integrated OTFT circuit is developed by building-up of basic sub-circuits and modelling the behaviour of digital circuit and analogue circuit.

#### 2.5.1.1 OTFT-based Digital Circuits

An inverter is the simplest logic circuit that is capable of inverting an input signal, which usually requires a p-type and an n-type MOSFET connected in a complementary way, shown in figure 2.28. There is a threshold for each inverter, when an input signal is above the threshold, it outputs "ZERO" while input signal is below threshold, and it outputs "ONE", shown in truth table [112]. Because the output signal is heavily dependent on the threshold value, the inverter is also capable of transforming a continuous analogue signal to discrete digital signal.

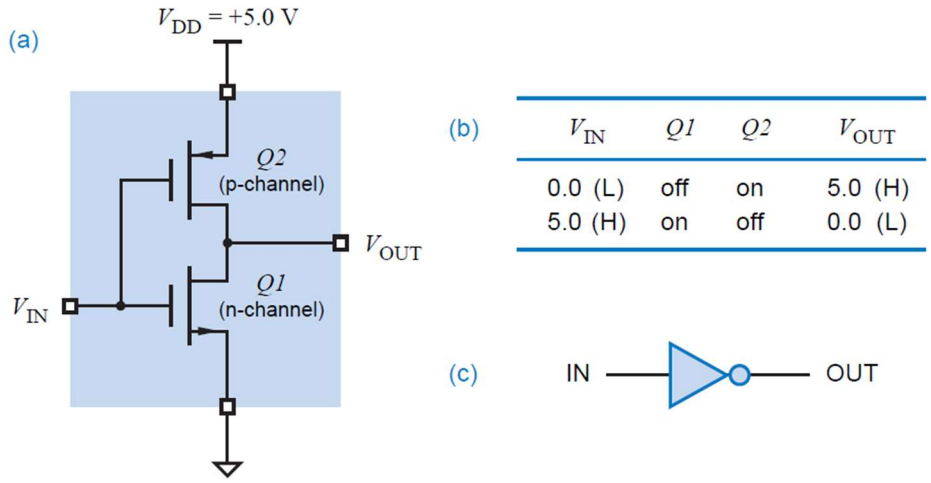
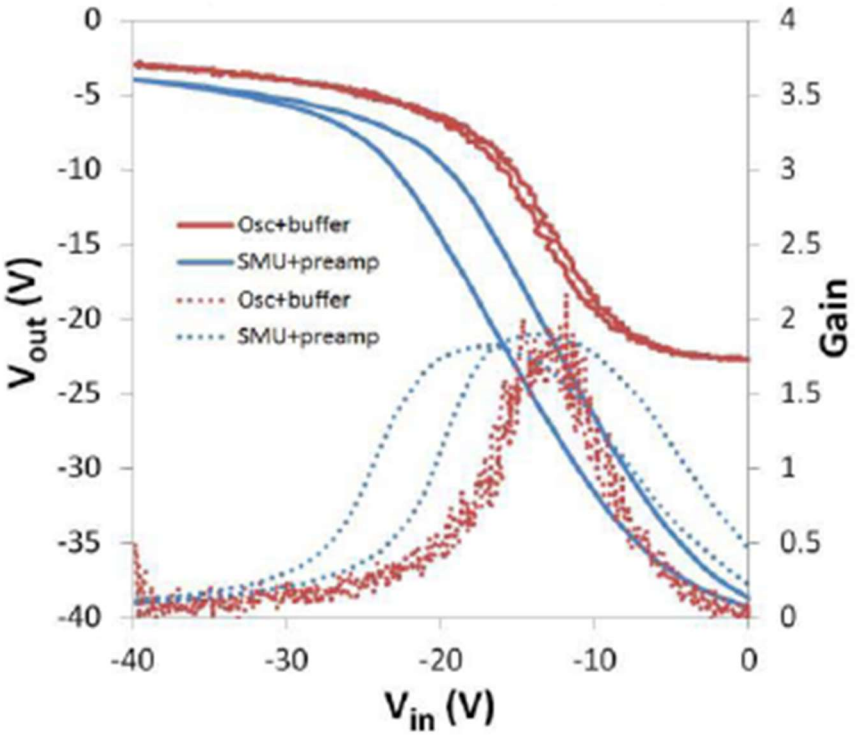
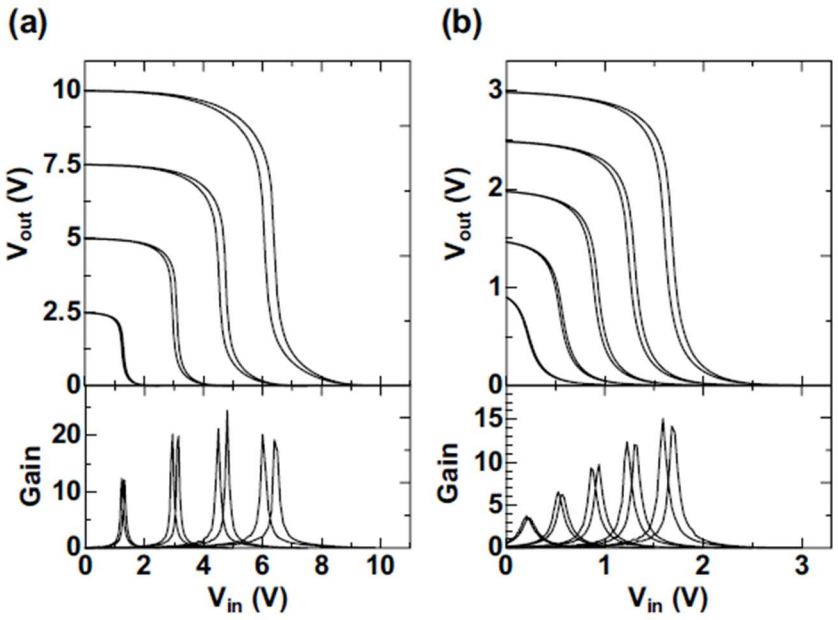



Figure 2.28. (a) Circuit diagram, (b) functional performance and (c) logic symbol of a CMOS inverter [112]

OTFT-based inverters have been widely explored recently because they are relatively simple, as shown in figure 2.28 above. For example, they have been manufactured with vacuum process that is compatible with roll-to-roll techniques, and tested with a square wave (400 Hz, 40 V) input signal [113]. The performance of the simple inverter is compared with the predicted result from simulation, and it exhibits high similarity, but the uncertainty from parasitic capacitance causes a faster voltage response, suggesting that the simple inverter needs to work with a frequency higher than 1 kHz. In contrast, complementary inverter circuits have been fabricated by solution-processing with p-type and n-type OTFT [6]. These invertors exhibited a more rapid switching of the output signal than vacuum processed OTFT because the higher subthreshold slope of a single transistor, shown in figure 2.29, but it exhibits hysteresis issues due to the threshold voltage shift caused by bias stress.




(I)




(II)

Figure 2.29. Transfer Characteristics of Vacuum-Processed Inverter with p-type OTFT (I) [113] and Solution-Processed Inverter with p-type and n-type OTFT (II) [5]

With stable performance of a simple inverter, some complex digital circuits can be created, such as diode-load logic (DDL) and zero-$V_{gs}$-load logic (ZVLL) circuits, shown in figure 2.30. In this case, the ZVLL configuration exhibits higher gain and higher noise margin than DDL, but it is still limited. The dual gate design on an inverter enables more possibilities to adjust the bias voltage on the transistor, and thus, it is helpful to increase gain and expand output voltage swing. In addition, optimizing the inverter structure with a bootstrapping technique can further increase gain and make the output voltage response more rapid [6].

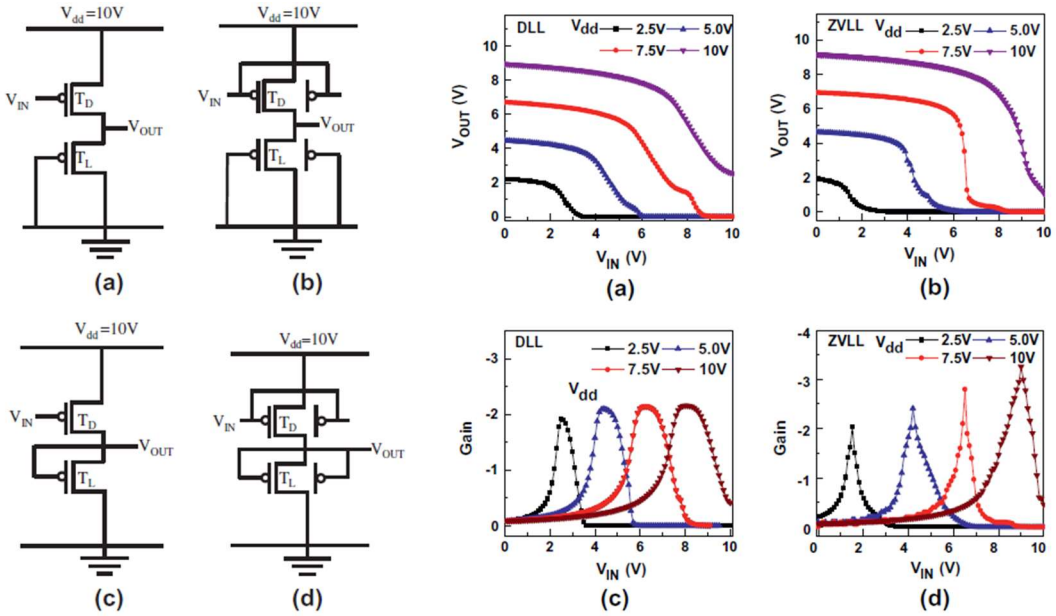



Figure 2.30. Schematic of Single Gate DLL and Dual Gate DLL (Left (a) and Left (b)) and Single Gate ZVLL and Dual Gate ZVLL (Left (c) and Left (d)) and Transfer Characteristics for DLL and ZVLL (Right (a) and Right (b)) and the Gain for DLL and ZVLL (Right (c) and Right (d))

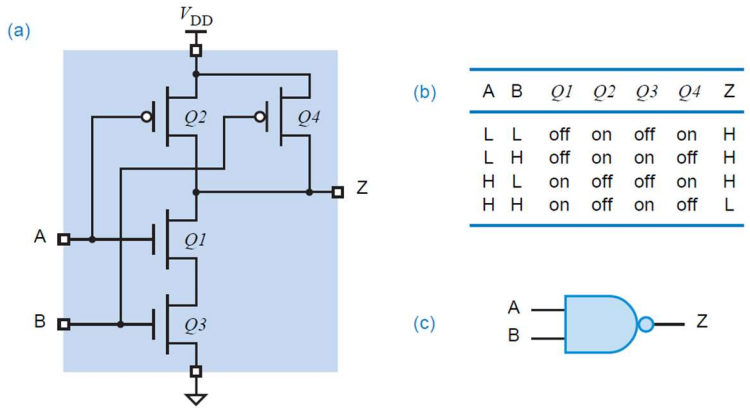



Figure 2.31. (a) Circuit diagram, (b) functional performance and (c) logic symbol of a NAND [112]

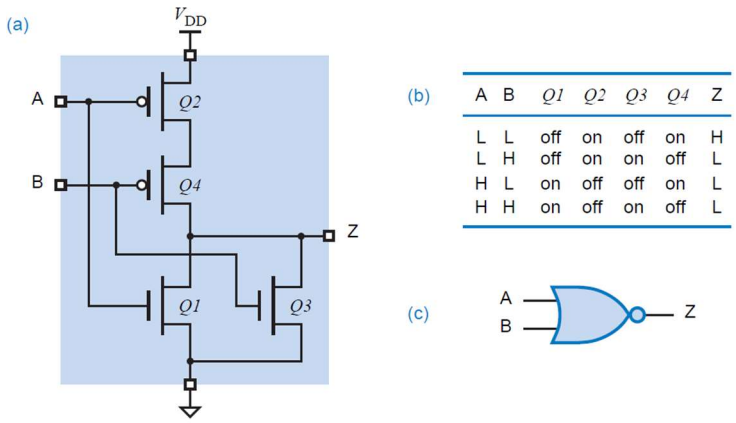



Figure 2.32. (a) Circuit diagram, (b) functional performance and (c) logic symbol of a NOR [112]

NAND and NOR logic elements are often constructed with inverters, and the functionality of NAND and NOR are displayed by the truth table, shown in figure 2.31 and 2.32 [112]. After obtaining stable OTFT-based inverters, a series of logic gate circuits, such as NAND and NOR gate circuit has been fabricated with all-evaporation technique, and then tested under two different input frequencies, 200 Hz and 400 Hz [113]. The results show that the output signal from the logic gate follows the truth table in figures 2.31 and 2.32, and it matches the predicted result from simulation, shown in figure 2.33, but the output voltage swing is still limited to half the range of the input signal. Based on the reliable performance of OTFT inverters, a multi-stage oscillator has been fabricated with vacuum process and solution process. Compared with a RO fabricated with an ink-jet printing technique, the vacuum-processed five-stage RO exhibits a higher frequency under the same rail voltage. However, the vacuum-processed seven-stage RO, shown in figure 2.34, exhibits a lower frequency than the five stage under high rail voltage, deviating from the model. This might be attributed by the non-zero off-current and error in the estimation of parasitic capacitance [2, 3, 113, 114].

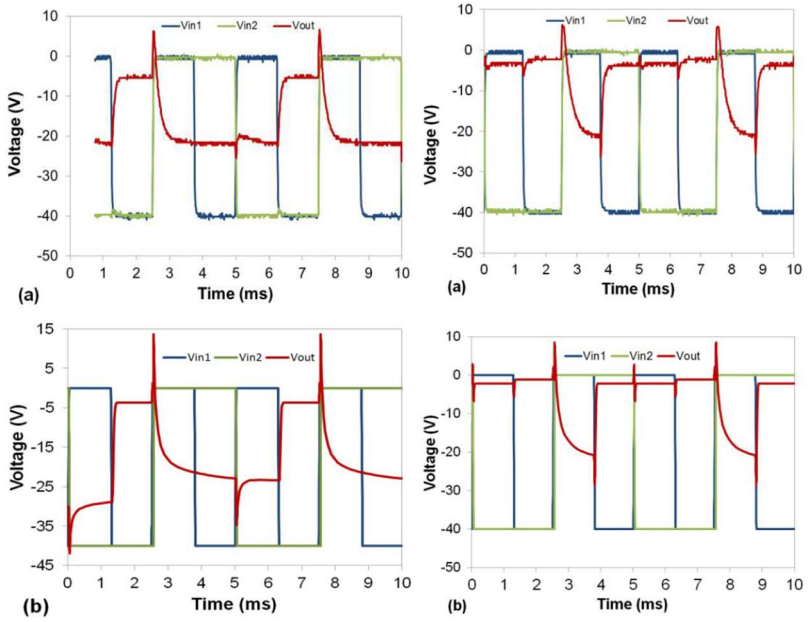



Figure 2.33. Actual Output and Simulated Output for NAND (Left) and NOR (Right) circuit [113]

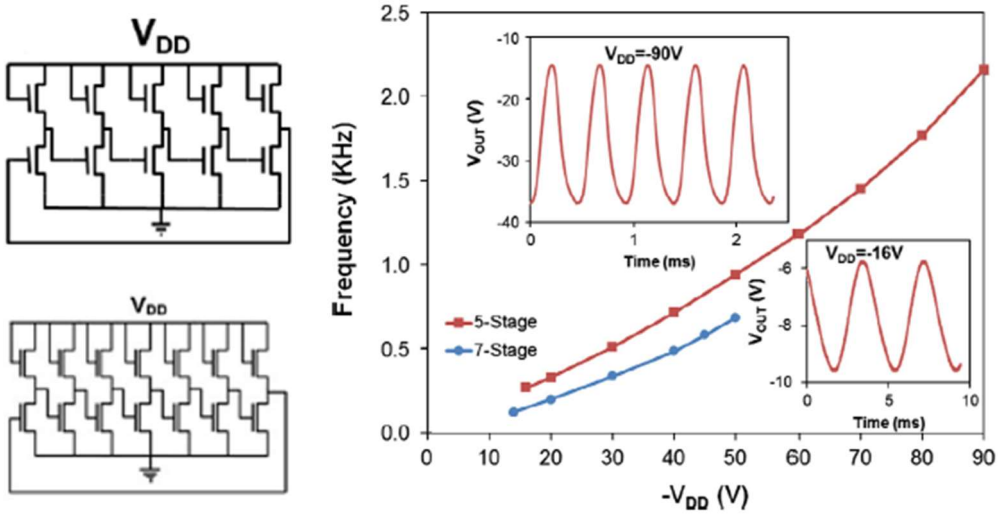



Figure 2.34. Five-Stage and Seven-Stage Ring Oscillator and Output Frequency [3, 4]

### 2.5.1.2 OTFT-based Analogue Circuits

A current mirror is a very basic building block in integrated circuits, and it is often used to build current sources and current-steering circuits. The basic structure of a current mirror is shown in figure 2.35, and for an ideal current mirror, the output should produce a stable current that is a copy of the reference current without being affected by the external load variance. By adjusting the overall width/length ratio of transistors on the mirror side, it is possible to control the current gain of a current mirror [115].

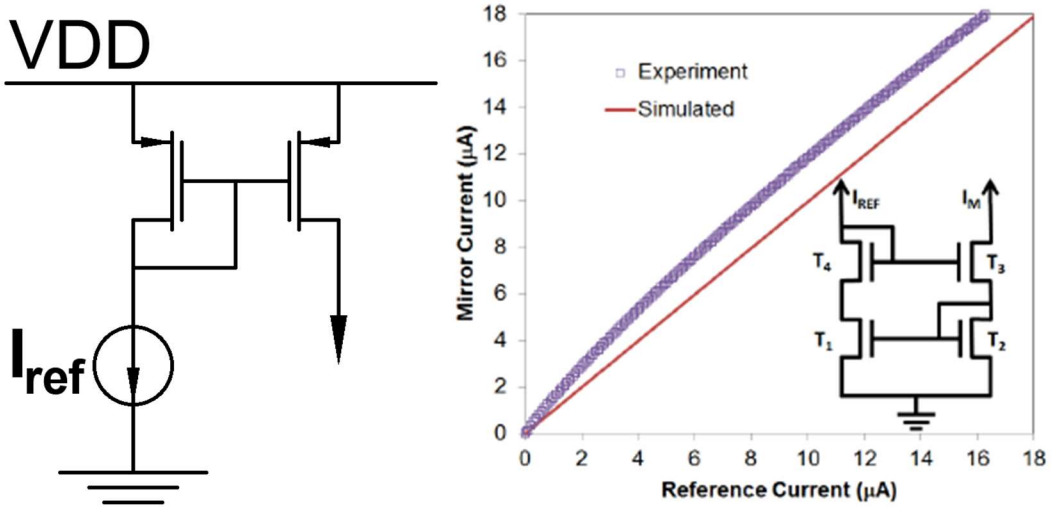



Figure 2.35. Circuit Diagram of Simple Current Mirror and OTFT Wilson Current Mirror with its response [113]

An OTFT Wilson current mirror has been fabricated with a vacuum-deposition process, shown in figure 2.36 [113]. It is assumed that all transistors in the current mirror are nominally identical and the ideal response is linear. However, the actual response exhibited deviation from linear behaviour due to minor differences between the transistors. The results reveal a mismatch between the reference transistor and the mirror transistor, i.e., the channel conductivity of the reference transistor might increase with higher reference current.

An operational amplifier (op-amp) is a very important basic component in most electronics. It can be used to fabricate integrators, differentiators, and current-voltage converters. In terms of structure, shown in figure 2.36, an op-amp is fabricated by integration of a multiple stage amplifier, including current mirror (MB and M6 or MB and M7), differential stage (M1 and M2), gain stage and output stage (M5 and M6). The current mirror is used as a current source to supply constant and stable current. The differential amplifier is used to output an amplified signal which is the difference between two input terminals. A circuit diagram of a differential pair is shown in figure 2.37 (a). A basic assumption for an ideal differential is that transistors M1 and M2 exhibit exactly the same properties, and both are operated in the saturation region. With these assumptions, an ideal gain can be calculated, and the amplification curve of the differential pair can be plotted, as illustrated in figure 2.37 (b). The output stage is the last stage of the op-amp. It is often used to provide the amplifier with a low output resistance, and as a result, it can output a signal to an external load without loss of gain [116].

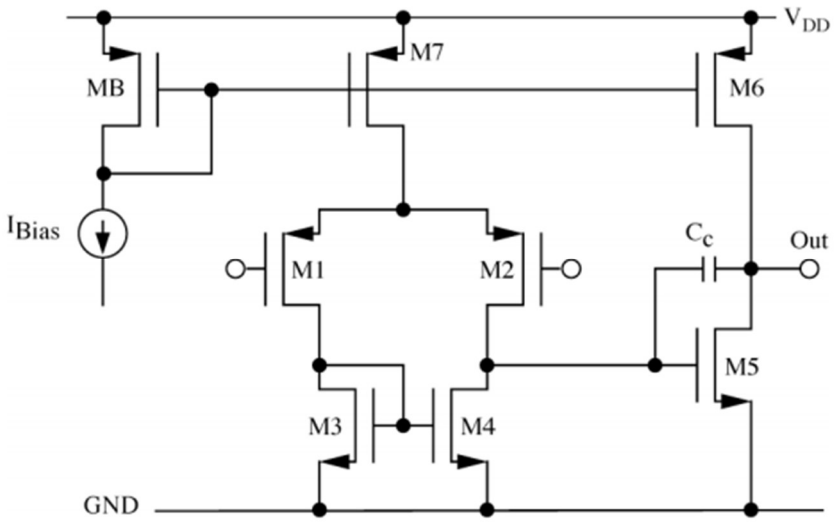



Figure 2.36. Schematic of Two-Stage CMOS Op-Amp

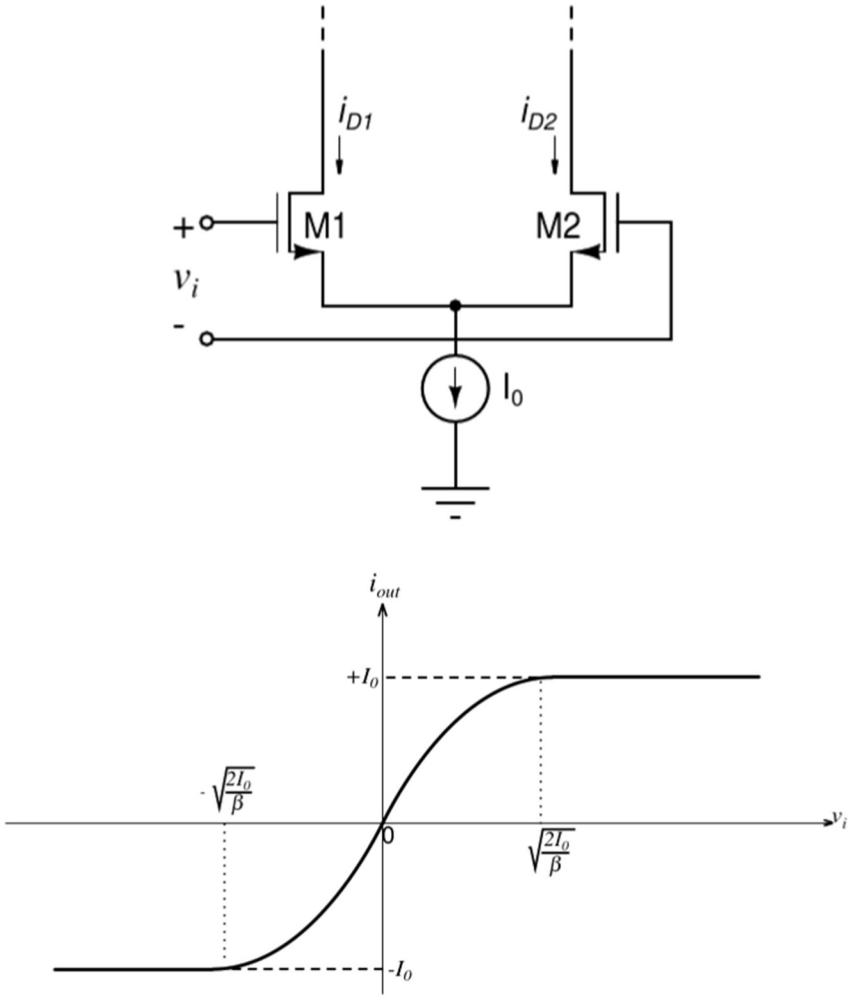



Figure 2.37. Schematic Diagram of Differential Pair and Amplification Curve [116]

An OTFT-based pseudo-CMOS amplifier has been developed, shown in figure 2.38. All OTFTs were manufactured on a PEN substrate and then interconnected. The feedback resistor ($R_0$) and input dc-cut capacitor ($C_0$) were connected to the OTFT-based circuit with screen-printed conductive adhesives. The assembled amplifier was tested with various AC voltage signals as input and then the amplification gain was calculated from the ratio of peak-to-peak amplitude of the output waveform to the input waveform. Plotting gain against input frequency, gain is shown to peak at approximately 1 Hz [117].

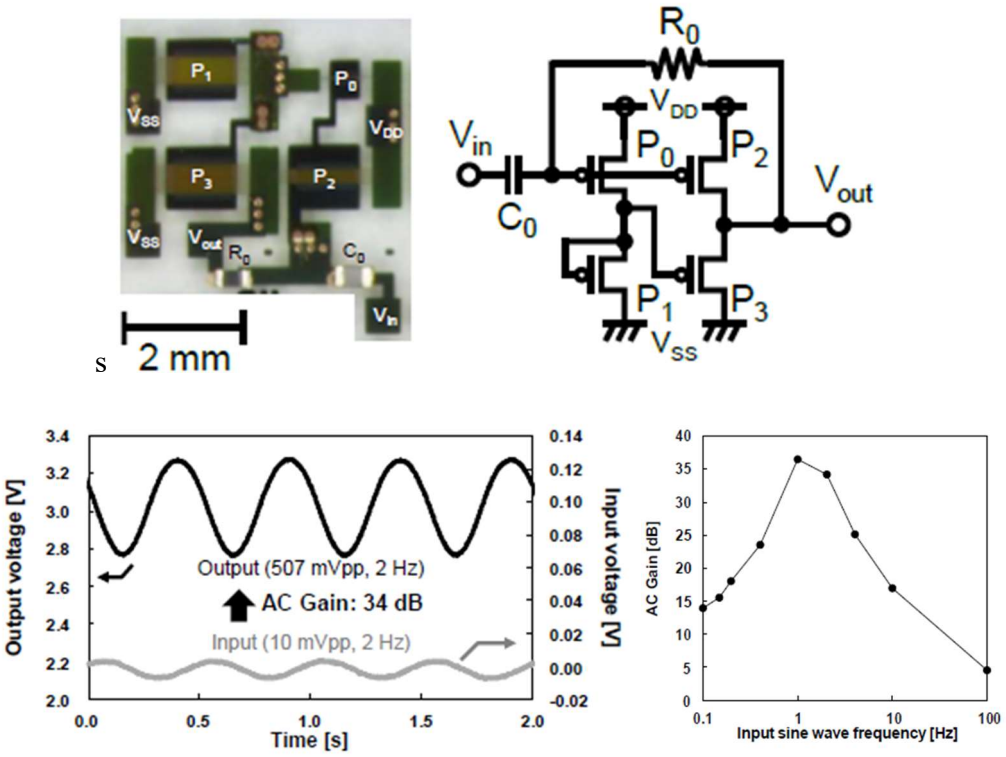



Figure 2.38. Pseudo-CMOS amplifier and Amplification Test Result [117]

An OTFT-based op-amp was fabricated as complementary circuits with solution-processed p-type and n-type OTFTs, shown in figure 2.39, including current mirror, differential pair and output stage [8]. Closed-loop DC characteristics and open-loop DC characteristics were demonstrated, and the circuits exhibited hysteresis in both cases. In the open-loop condition, the dual gate structure exhibited less hysteresis than the single gate, and for closed-loop condition, the hysteresis was reduced by a small feedback resistor. Dynamic characterisation of the organic op-amp reveals the frequency dependence of the open-loop gain, and the amplification gain is stable at low frequency and decreases with increasing frequency. The dynamic response differs from the result in figure 2.39, but the working frequency range is similar, at 1 – 10 Hz. Based on the stable OTFT op-amp, an integrator, differentiator, transimpedance

amplifier and oscillator were fabricated subsequently by connecting it with external resistor and capacitor, and the output signals were close to simulated results.

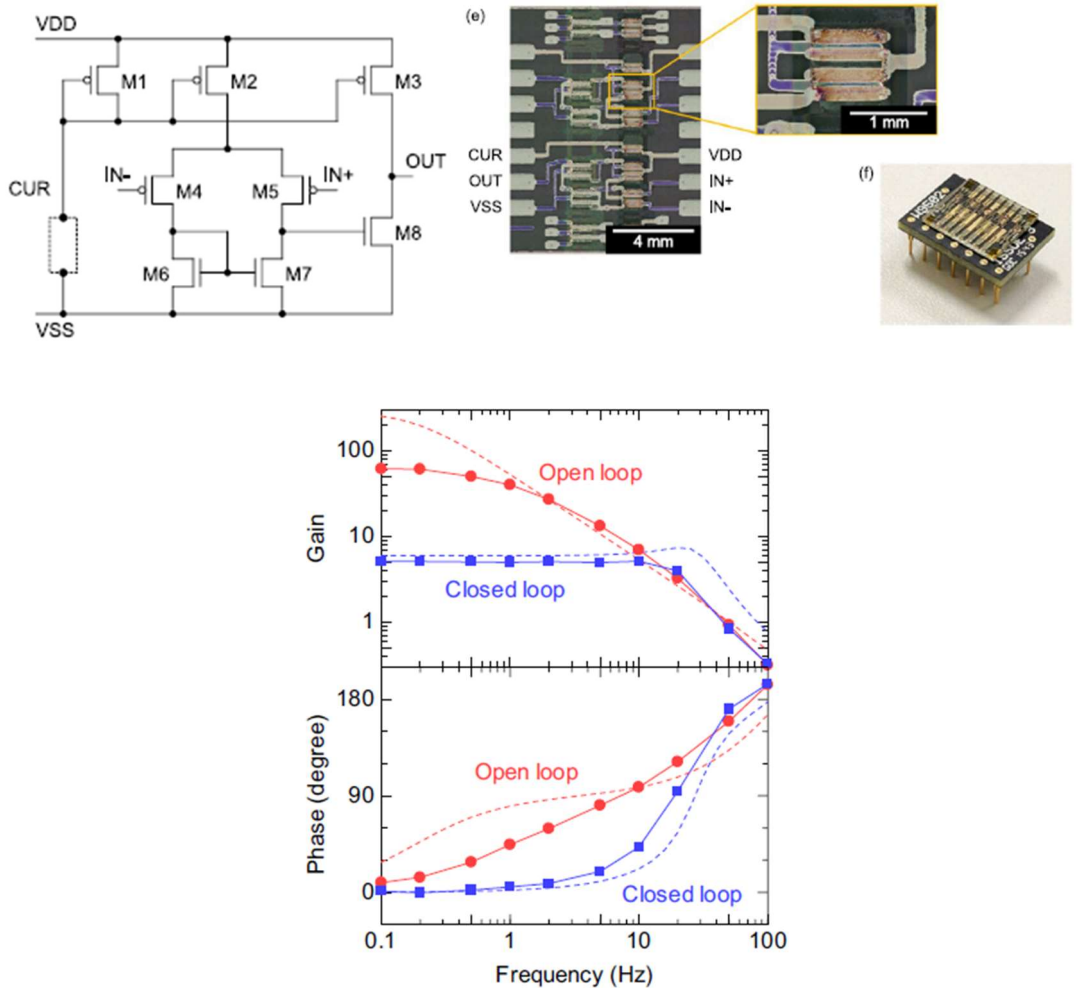



Figure 2.39. OTFT-based Operational Amplifier and Dynamic Frequency response [8]

To enhance the gain of an OTFT amplifier, the width/length ratio of a single transistor needs to be increased. A single stage with large width/length ratio differential pair was fabricated and it realized high amplification gain at 1 kHz and higher cut-off frequency at 1.2 kHz [118].

After developing an OTFT op-amp, it is possible to create a complex signal processing system for sensors. A sensing system employing p-type OTFTs as PMOS was created with integration of a differential stage, current source and inverter chain to process signals from an electrode in an electrochemical cell, shown in figure 2.40 [7]. Although the differential pair exhibits high gain, an inverter chain is needed to improve the overall gain of the entire circuit for signal conversion from electrochemical cell to a display.

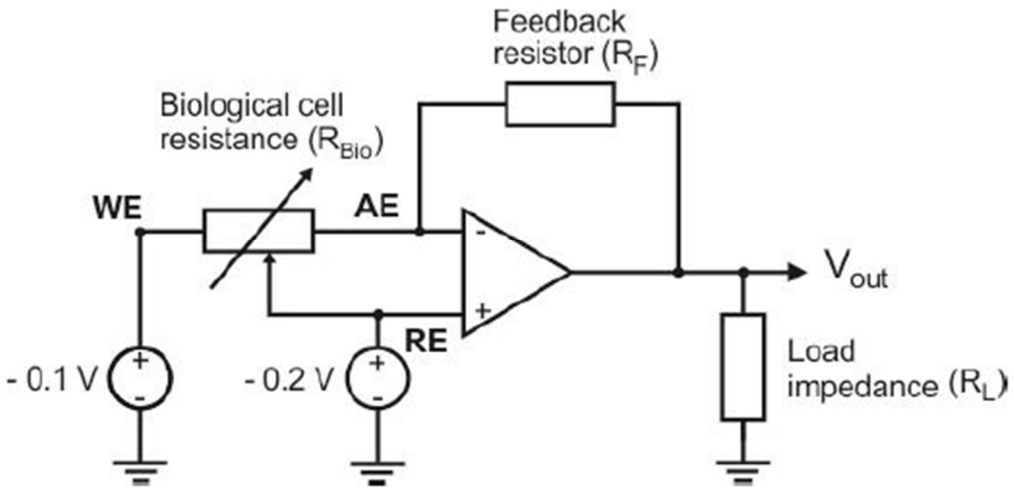



Figure 2.40. OTFT-based Signal Conditioning Circuit for Electrochemical Reaction [7]

### 2.5.2 Encapsulation and Protection for OTFT-based Circuit

Because of the vulnerability of organic semiconductors, protection and encapsulation is very important for OTFT, especially for small molecule n-type OTFTs. The degradation mechanism of OTFT has been reviewed in section 2.2.4, based on these mechanisms; the encapsulation must block the passage of oxygen and moisture.

Plastic substrates used in manufacture of flexible circuits are an insufficient barrier to the diffusion of oxygen and water molecules, in order to protect OTFTs from water vapour and oxygen, the ideal water vapour transmission rate (WVTR) and oxygen transmission rate (OTR) should be in range of $10^{-3}$~$10^{-6}$ $g.m^{-2}day^{-1}$ and $10^{-3}$~$10^{-5}$ $cm^3.m^{-2}day^{-1}atm^{-1}$ respectively. Table 2.3 below displays WVTR and OTR for different polymeric materials and oxide coated plastic films. An oxide film, such as $Al_2O_3$ or $SiO_2$, applied as a coating to the flexible polymer has tightly bound atoms and can be an effective barrier to oxygen or moisture permeation, with the micro or nano defects populations in the oxide film controlling the rate of permeation [119].

Table 2.3 WVTR and OTR for different polymeric materials [120-122]

| Materials | WVTR/($g.m^{-2}day^{-1}$) | OTR/($cm^3.m^{-2}day^{-1}atm^{-1}$) |
|---|---|---|
| HDPE (25.4 μm) | 4.7 – 7.8 (38 ºC) | 2300 – 3100 (23 ºC) |
| LDPE (25.4 μm) | 16 – 23 (38 ºC) | 7000 – 8500 (23 ºC) |
| Cast PP (25.4 μm) | 9.3 – 11 (38 ºC) | 2300 – 3100 (23 ºC) |
| Biax PET (25.4 μm) | 16 – 20 (38 ºC) | |
| Orientated PET | | 31 – 93 (23 ºC) |
| $SiO_x$ (40 nm) coated PET (125 μm) | 0.5 (40 ºC) | 0.7 (40 ºC) |
| $AlO_x$ (360 nm) coated PET (12 μm) | 0.04 (23 ºC) | <0.005 (23 ºC) |

HDPE – High Density Polyethylene
LDPE – Low Density Polyethylene
PP – Polypropylene

Current protection film is often made of a hybrid of inorganic/organic film. With nano-laminates, nano-fillers mixed into the polymer have the effect to increase the diffusion path for oxygen and water, and these barriers exhibit higher toughness than a continuous inorganic oxide coating, for example, the OTR can be reduced further to 0.1 $cm^3.m^{-2}day^{-1}atm^{-1}$ with thinner oxide layer [123]. For the highest barrier, continuous, coating, a multi-layer laminate structure is helpful to inhibit propagation of defects

between successive oxide layers [124]. It is shown that WVTR can be reduced into range of $10^{-4}$ g/m$^2$/day if multi-layer organic/inorganic encapsulation is applied [125].

## 2.6 Electrochemical Sensing Mechanism and Electrode Functionalization

The deterioration of organic semiconductors due to contact with the atmosphere and analytes, and the selectivity limitation of OSC, means that the direct-contact architecture of OTFT sensor has limited application. A novel method is to separate the signal generating unit and the processing unit, like FG-OTFT sensor, described in section 4.1, and with this new architecture, it is possible to encapsulate the vulnerable organic semiconductor with chemically inert materials and then achieve multiply functional sensing work on an extended electrode. Meanwhile, functionalization of electrodes for selectivity is well developed in electrochemical research, in which the sensing signal is processed by the PCB-based amplification circuit. In this project, OTFT-based signal conditioning circuits are fabricated, to replace the PCB-based amplifier and electrodes are functionalized with different materials.

The key requirement for electrode functionalization is to realize a strong bonding between the electrode and the objective sensing materials without prohibitively reducing electrical conductivity across this interface. Because of the strong bonding between gold and sulphur, some sulphur containing molecule, such as cysteamine and thiophene derivatives are used as a binder to connect gold electrode and sensing materials.

### 2.6.1 Cysteamine Coating

Adsorption of thiols on gold surfaces has been researched and shown to form self-assembled monolayers (SAM). A high coverage of cysteamine on a gold surface, shown in figure 2.41 (a) can be achieved by immersing a gold electrode in cysteamine aqueous solution or ethanoic solution for a short time [126]. Because of the strong bonding between gold and cysteamine SAM and short coating formation time, this can be the basis of multiple different functionalization on gold electrodes.

Because of the interaction between hydrogen ions with the amine group of cysteamine, a cysteamine/Au electrode can be transformed to a pH sensor with floating gate structure. The output curve of FGOTFT with hydrogen ion bonded floating gate exhibits a lower current response, shown in figure 2.41.(b) [127], but this sensing response is dependent on the instantaneous reaction between ions under electric field, and the output current signal decays with time.

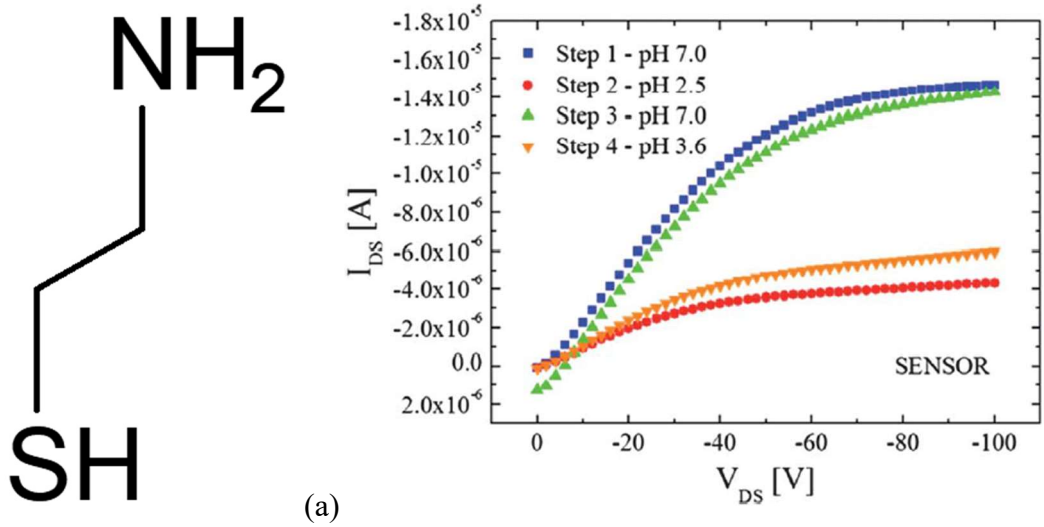



Figure 2.41. Drain Current Response of FGOTFT under Different pH [119]

In addition, more research focuses on enzyme functionalization on electrode with cysteamine due to the selectivity offered by different enzyme. Enzymatic reactions often produce $H_2O_2$ that decomposes under catalysis of noble metal or oxides [128], thus, $H_2O_2$ sensors are widely developed to detect the product of specific enzymatic reactions, for example, decomposition of glucose [129].

With help of cysteamine and its derivatives, horseradish peroxidase (HRP) can be bonded to a gold electrode for detection of $H_2O_2$, shown in figure 2.42. However, there are some limitations to this $H_2O_2$ sensor. Firstly, the sensing signal is dependent on the redox reaction of the mediator, which occurs after oxygen is produced from decomposition of $H_2O_2$. In addition, the chain structure, shown in figure 2.42, increase the distance between the gold electrode and the sensing materials, i.e. the effective sensitivity is reduced [130].

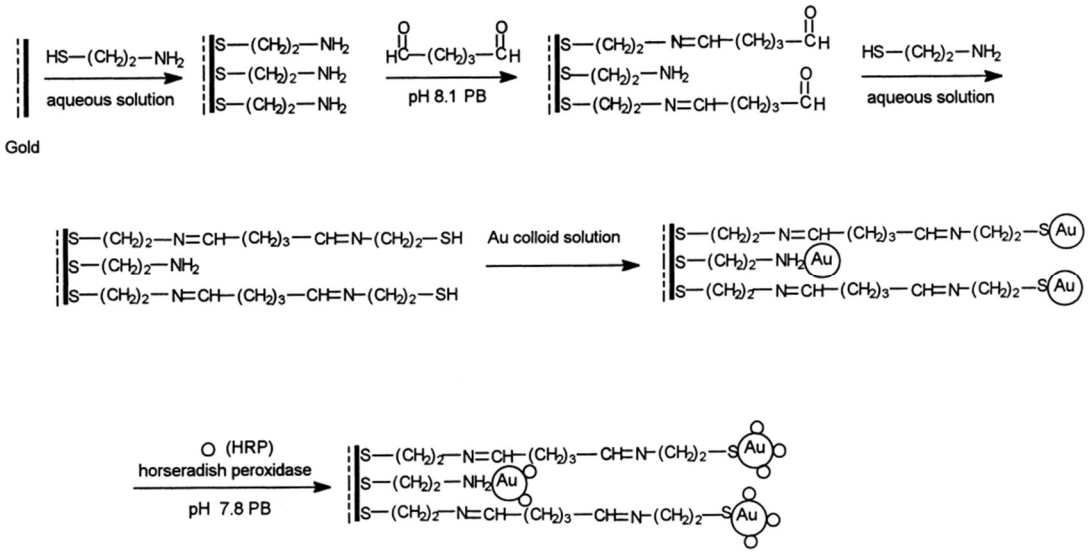



Figure 2.42. Schematic of Preparation Process of $H_2O_2$ Sensor [130]

In order to shorten the charge transfer distance or to make the binder more conductive, some composite structures have been investigated. A novel nano-composite formed by

grafting Ag nano particles onto a cysteamine-coated gold electrode with a chitosan-graphene oxide composite was fabricated to realize a mediator-free $H_2O_2$ sensor; it demonstrated a low detection limit and wide linear range [131]. In addition, a urea biosensor was developed with a binder of PAMAM-grafted multi-wall carbon nano-tubes, on which urease is constrained. The binder forms strong bonding with cysteamine-coated Au electrode. Shown in figure 2.43, this complex structure exhibits high stability in aqueous solution with high selectivity and sensitivity to urea [132].

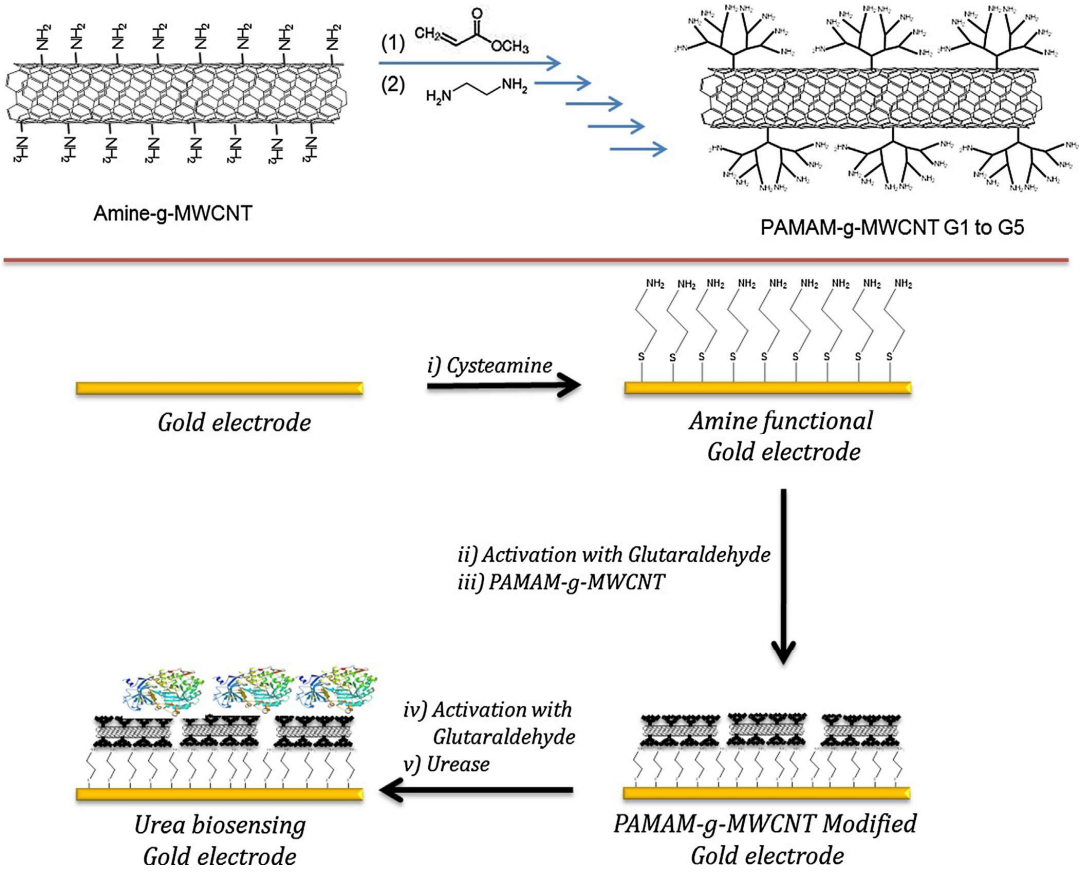



Figure 2.43. Schematic of PAMAM-MWCNT binding for Urea Sensor on Cysteamine coated Gold Electrode [132]

The reusability or reproducibility of a cysteamine coated electrode is usually dependent on the bonding strength between functional materials and cysteamine,

therefore, a permeable coating is needed to immobilize the functional materials. A composites of multi-wall carbon nanotubes and Nafion was used for protection of cysteamine-coated Au electrode and myoglobin. Consequently, it gave a higher selectivity to $H_2O_2$ in solution without losing stability [133].

In addition, chitosan can be used to protect materials on an electrode. As shown in figure 2.44, a cysteamine/glucose oxidase (GOx or GOD) pair can be immobilized on a gold electrode in aqueous solution because the chitosan limits the diffusivity of GOx. It is illustrated that this functionalized electrode can detect the concentration of glucose in the presence of ferrocenemethanol as a mediator which generate a sensing signal when it is oxidised by the oxidant produced by decomposition of glucose [134].

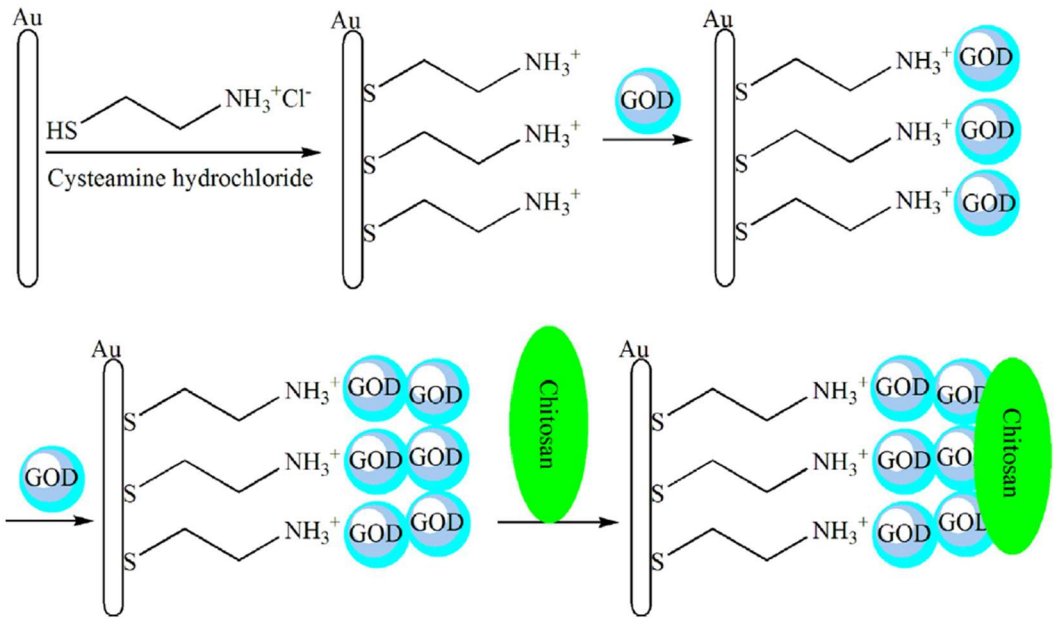



Figure 2.44. Schematic of Glucose Sensor Fabricated by Cysteamine Coating and Chitosan immobilizer [134]

### 2.6.2 Coating of Thiophene-based Polymers

Thanks to a conjugated π-structure, poly-thiophene (PTh) and its derivatives exhibit high electrical conductivity and versatility to grafting functional groups, so it is often used in fabrication of OLED, OTFT, sensors and batteries. However, because it is capable of self-assembly on a gold surface or gold nano-particles [135, 136], it also makes a wide range of sensing functionalization on an electrode possible, and research often focuses on the bonding strength between PTh functional materials and objective materials and improvement of binding capability.

Electrochemical polymerisation of Th on a glassy carbon electrode (GCE) is a straightforward way to encapsulate a target molecule in a polythiophen matrix to enable sensing function. For example, gold particles can be loaded in a PTh matrix during electrochemical polymerisation of Th in the presence of gold colloid [137] and it can be used to detect the presence of $H_2O_2$ in solution due to the intrinsic catalytic property of gold to decomposition of $H_2O_2$. In addition, an anesthetics sensor was created with this mechanism, that exhibited high sensitivity to procaine, benzocaine, and procainamide with differential pulse voltammetry (DPV), but only the sensing signal from procainamide hydrochloride was of acceptable strength [138]. In addition, electrochemical polymerisation of thiophene monomer or bithiophene monomer in the presence of GOx can be used to create a glucose sensor [139], and cyclic voltammetry scanning is helpful to trap GOx in the nano-pores of a PTh matrix, shown in figure 2.45, after which a linear sensory response was exhibited. However, the incompatibility of GOx to organic solvents makes it difficult to immobilize more GOx molecules onto the electrode without damage [140].

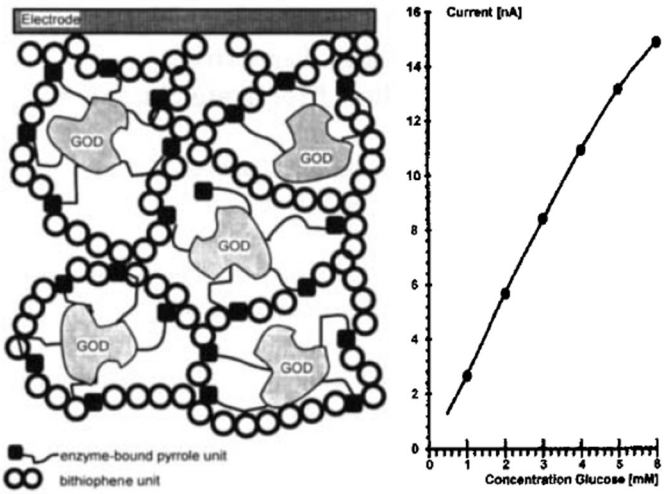



Figure 2.45. Entrapped GOx in PTh Matrix and its Sensory Response to Glucose [140]

To immobilize an enzyme more stably on the electrode, a copolymer of thiophene and its derivative is helpful. Poly (3, 4-ethylenedioxythiophene) (PEDOT) is an important PTh derivative that is often used as an electrode due to its high electrical conductivity. After functionalization with GOx, it can be used as glucose sensor, but a water permeable immobilizer (Nafion membrane in figure 2.46) was required to strengthen the bonding between PEDOT and GOx, shown in figure 2.46 [141]. Alternatively, electro-spun poly-acrylonitrile was used to create nano-fibres on top of a PEDOT/GOx structure as protection without reducing the activity of GOx. In contrast, a copolymer of 3-thiophene acetic acid and 3-hexylthiophene was synthesized as a shell structure to contain urease covalently by interaction between the carboxylic group on the polymer and the amino group on urease. The functionalized electrode exhibited a stable potentiometric response to variance of urea activity in aqueous solution, but the concentration range that could be detected was limited [142].

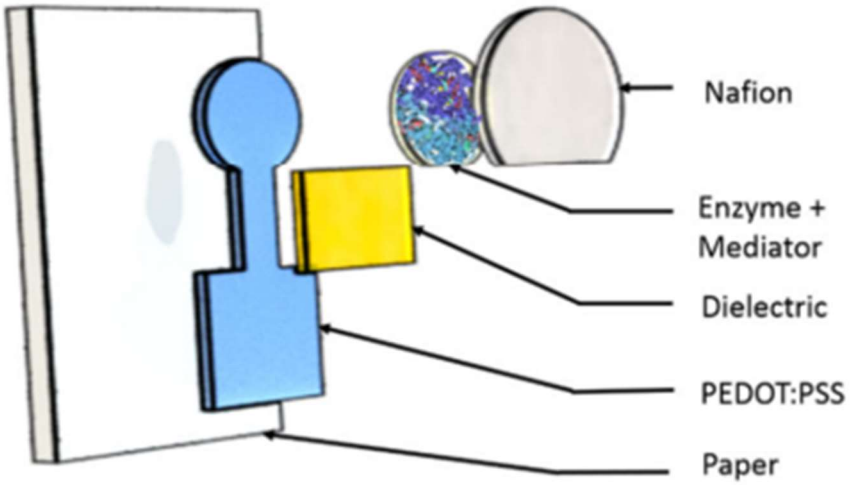



Figure 2.46. Stabilization of Enzyme on PEDOT: PSS Electrode [141]

Nanocomposites of PTh and objective materials are attractive for sensor research because of higher loading capability to target molecules. Polymers of alkyl thiophene, such as poly-(3-methylthiophene) (P3MT) and regioregular poly-(3-hexylthiophene-2,5-diyl) (P3HT), can be used for fabrication of nano-composites. The former was used to encapsulate gold nano-particles and bind on GCE that exhibited electro-catalytic activity to nitrite and iodate [143] and the latter was used with dithiobissuccinimidyl propionate (DTSP) to immobilize glucose oxidase on the gold electrode for detection of glucose [144]. Because of the limited conductivity of thiophene-based polymer, conductive carbon materials, for example carbon nanotubes are used to alleviate the overall resistivity of the nanocomposites; a functionalized ITO glass electrode with gold-PTh-CNT nanocomposites, shown in figure 2.47, exhibited high sensitivity and selectivity to dopamine under differential pulse voltammetry (DPV).

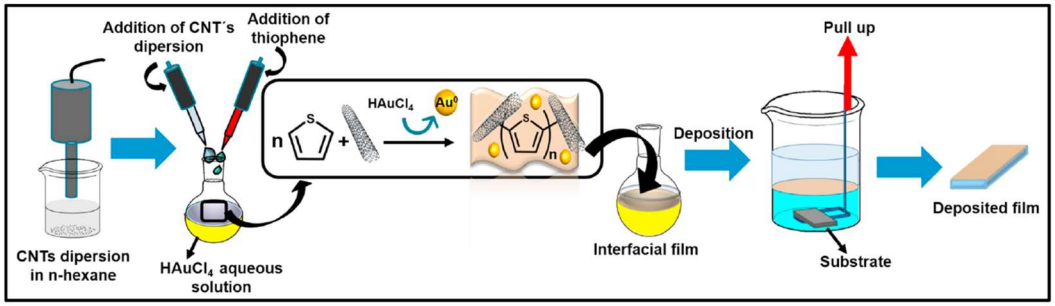



Figure 2.47. Synthesis of Au-PTh-CNT nano-composites for Electrochemical Sensor [145]

### 2.6.3 Integration of a Functionalized Electrode with OTFT

In electrochemical research, a commercial workstation is very accurate and reliable means to process any small signal generated from the reaction, and it's very helpful for development of novel sensors. However, for a fully flexible device, an integrated flexible circuit to process the small signal from the electrochemical reaction should be employed. Because of this gap between electrochemical sensor study and electronic device study, only a few research papers have focussed on the development of flexible and wearable sensing systems.

Because of high stability and reliability, conventional transistors, for example, MOSFETs are widely used in research for an integrated flexible sensing system. The key challenge of such research is to reduce the overall size of the device as much as possible, allowing it to be embedded onto a flexible substrate. The floating gate structure provides a platform for deposition of sensing materials and FGMOSFETs are often transformed into a sensor, for examples as shown in figure 2.48. The sensitivity is determined by the shift of the effective bias voltage under the charge transfer reaction and selectivity is determined by the functional coating on top of the floating

gate. Based on this mechanism, FGMOSFET has been transformed to a series of sensors, such as humidity, pH and DNA [146-148].

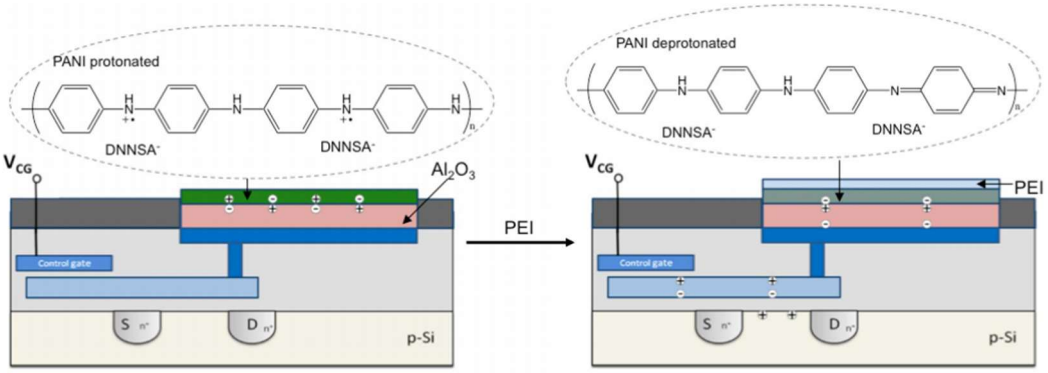



Figure 2.48. FGMOSFET Sensor to Detect Polyethyleneimine [146]

Similarly, the floating gate structure can be transferred to an OTFT system. A pressure sensor and a strain sensor have been fabricated with a compressible capacitor and ferroelectric polymer. The capacitor and PVDF can generate an instantaneous charge imbalance on the floating gate to shift the effective bias voltage and then alter the output signal [109, 149]. With a functional layer of cysteamine, FGOTFT can be used to detect pH variance due to selective adsorption of hydrogen ions on the cysteamine surface. When the floating gate is coated with single-strand DNA molecules, it can be used to detect hybridization of the DNA strands on the floating gate because of the instantaneous charge imbalance, however because the signal generated by charge imbalance cannot be kept on the floating gate for a long time and the overall output signal is very small [150-153]. An innovative testing method with high frequency AC voltage from source to drain, with measurement of the frequency shift when cells are deposited onto a floating gate was used to examine activity of cells and their ionic reaction, i.e., FGOTFT was transformed into a cell sensor [154].

Although the signal processing system for electrochemical reactions is complex in conventional devices, the basic circuits are well developed. In figure 2.40 above, an integrated system based on p-type OTFT has been built. Although the simulation results give a very linear signal conversion relationship between concentration of cholesterol and output voltage, such an integration needs to be demonstrated experimentally [7].

## 2.7 Prospects

Today, it is possible to manufacture OTFTs and some simple integrated circuits with OTFTs via high throughput roll-to-roll techniques. By integrating functionalized thin film electrodes with an OTFT-based signal conditioning circuit, it should be possible to achieve a fully wearable sensing system. Compared with a conventional OTFT sensor, the integrated sensing system is expected to exhibit a more stable performance and longer lifetime, and to allow greater options for control of selectivity to specific analytes.

However, the sample-to-sample variation of organic electronics is still a limitation for the future application. To overcome the sample dependency, a large scale manufacturing technique is need to obtain more organic electronics, where a series of standard procedures and tight process control can be created to optimize the properties of device and reduce the sample variability. With the standard procedures, the waste of materials and overall cost of manufacturing can be reduced, making the wearable device more accessible and cheap for the end customer. Finally, an Internet of Things (IoT) can be constructed after the customized wearable electronics distributed around the world to collect massive health condition data from the public and achieve high-

efficient and high-accurate medical service, e.g., remote diagnosis and continuous monitoring of chronic conditions.

# Chapter III

# Manufacture of Organic Thin Film Transistors with Roll-to-Roll Process and Model Validation for Study of Bias Stress

## 3.1 Introduction

Organic Thin Film Transistors (OTFTs) are very promising component for flexible electronics due to their inherent mechanical flexibility, and ease of large-area manufacture. In terms of manufacturing, layer stacking is the basic principle of manufacturing OTFTs for any architecture of OTFTs, BGTC, BGBC, TGBC, and TGTC and OTFTs are usually manufactured by vacuum deposition or solution deposition, as introduced in literature review (section 2.2.2). In this project, all OTFTs are manufactured with thermal evaporation and vacuum flash evaporation.

The properties of the dielectric and semiconductor layers are very important for the performance and stability of OTFTs. An ideal dielectric insulator between gate and semiconductor should exhibit a high dielectric constant and zero leakage current with very low thickness because a high electric field facilitates localization of charge carriers and leakage would interfere with the output signal. However, it is difficult to

realize uniform and defect-free insulating thin films in large area; the variance of thickness and uncontrollable defect distribution often leads to a short circuit issue and current leakage in OTFT. Compared with Si-based transistors, the stability of organic semiconductors is a determining factor for the performance of an OTFT; the susceptibility to an oxidising environment limits the stability of the output signal and the lifetime of transistors.

Different from CMOS, OTFTs exhibit a time-dependent output signal when they are switched on, which is called the bias stress. From the perspective of circuit design, the time-dependent current decay resulting from bias stress will cause uncertainties for electronic systems on chip (SoC) and limit the application of OTFTs for complex circuits. The basic understanding of the bias stress is in terms of charge trapping states; however, the source of trapping states is complex to understand and still in exploration. As introduced in literature review (section 2.2.4), grain boundaries of the semiconductor and polar functional groups in dielectric materials might be possible sources of trapping states, but the principal origin of the charge trapping effects that lead to the observed bias stress is not yet well established and may vary from system to system.

In this chapter, a manufacturing technique based on vacuum processing will be introduced, and OTFTs are made in the architecture of top-contact and bottom-gate with this technique. Next, the electronic behaviour of the transistors are characterised using a Keithley 2400 source meter. Multiple batches of transistors are made, and the properties of these transistors are compared, and parameters of manufacturing are adjusted to optimize performance of transistors. After that, modification of the transistors to reduce the probability of short circuit and current leakage will be

described. Next, use of OTFTs with similar performance to explore the air aging stabilization and oxygen-doping effect will be described. Finally, the bias stress effect of OTFTs is investigated by extracting time-dependent drain current with a model of charge trapping in dielectric materials.

## 3.2 Experiments

### 3.2.1 Manufacture of OTFT in Roll-to-Roll process

The OTFTs in this work are manufactured in a bottom-gate top contact architecture due to lower contact resistance and higher charge carrier density generated by a top contact structure [155, 156], shown in figure 3.1, via vacuum evaporation techniques on 125 um Poly (ethylene naphthalate) (PEN) (DuPont Teijin Films) because of its thermal stability in PVD process and low surface roughness. In this project, aluminium or copper gate electrodes, dinaphtho[2,2-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) semiconductor and gold contacts are deposited in an Edward 306 vacuum thermal evaporator (E306) (details described in Appendix) shown in figure 3.2 (a), through a shadow mask. The deposition rate was monitored using a Quartz Crystal Microbalance (QCM). Deposition and curing of Tripropylene glycol diacrylate (TPGDA) insulator was carried out using the Oxford Web-coater (details described in Appendix), shown in figure 3.2 (b). The chemical structures of TPGDA and DNTT are shown in figure 3.3. A buffer of Polystyrene (PS), which reduces the polarity of TPGDA surface, is deposited on TPGDA layer by spin coating and evaporating residual solvent by heating [16]. The operating parameters of E306, Oxford Web-coater and spin coater are shown in table 3.1.

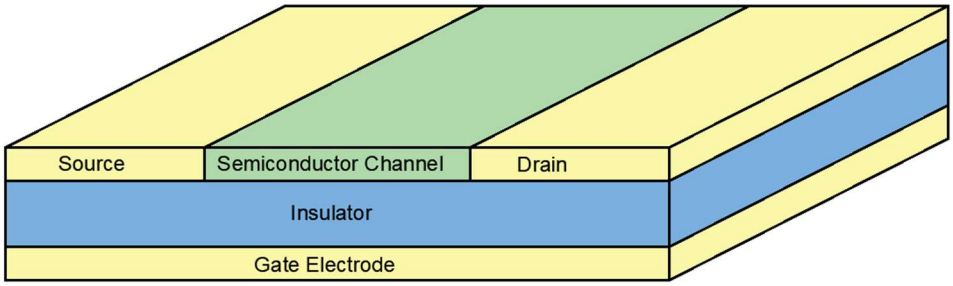



Figure 3.1. Structure of Bottom-Gate Top-Contact OTFT

Figure 3.2. E306 Evaporator (Left) and Oxford Web-coater (Right)

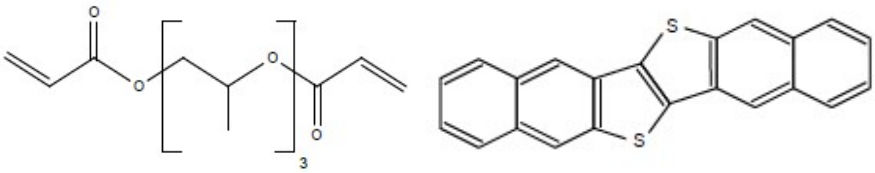


Figure 3.3. Structure of TPGDA (left) and DNTT (right)

Table 3.1. (A) Operating Parameter of Web-coater

| Operating Parameter | Value |
|---|---|
| Rotating Speed of Drum/m.min$^{-1}$ | 25 |
| Working Pressure/mbar | $1.0 \times 10^{-4} - 2.0 \times 10^{-4}$ |
| Temperature of Tank/ $^{o}$C | 270 ± 3 |
| Temperature of Tank Door/$^{o}$C | 285 ± 3 |
| $O_2$ Flow Rate/sccm | 5 |
| Ar Flow Rate/sccm | 200 |
| MDX Voltage/V | 250 ± 20 |
| MDX Current/A | 5.9 ± 0.05 |

Table 3.1. (B) Operating Parameters of E306

| | Aluminium Gate | DNTT Semiconductor | Gold Contact |
|---|---|---|---|
| Deposition Rate/nm.s$^{-1}$ | 4 – 5 | 0.003 – 0.005 | 1 – 2 |
| Working Pressure/mbar | 5.0 x $10^{-5}$ | < 3 x $10^{-5}$ | 7 x $10^{-5}$ |
| Thickness (QCM)/nm | 40 – 50 | 30 – 40 | 30 |

Table 3.1. (C) Operating Parameter of Spin Coater

| Parameter | Value |
|---|---|
| Concentration of PS solution/wt% | 0.6 |
| Spinning Rate/rpm | 1000 |
| Spinning time/s | 30 |
| Post heating temperature/$^{o}$C | 95 |
| Post heating time/min | 5 |

### 3.2.2 Measurement of thickness

Although the QCM can indicate thickness and deposition rate, the accuracy is very low. The thickness of a reference sample of each layer materials deposited on silicon wafer is measured in Dektak profile-meter and thickness is measured at three different points at a masked edge on each film. The table 3.2 displays the average thickness value.

Table 3.2. Thickness of each layer on OTFT

| Batch | Gate/nm | Insulator (TPGDA)/nm | Semiconductor (DNTT)/nm | Contact (Au)/nm |
|---|---|---|---|---|
| 1 | 191 ± 21 | 244 ± 67 | 163 ± 19 | 104 ± 17 |
| 2 | 97 ± 12 | 564 ± 18 | 200 ± 48 | 60 ± 12 |
| 3 | 70 ± 13 | 725 ± 27 | 100 ± 21 | 59 ± 9 |
| 4 | 95 ± 17 | 160 ± 20 | 51 ± 8 | 133±21 |
| 5 | 57 ± 8 | 398 ± 40 | 75 ± 17 | 90 ± 23 |
| 6 | 79 ± 29 | 642 ± 16 | 75 ± 16 | 47 ± 10 |
| 7 | 30 ± 12 | 725 ± 11 | 30 ± 6 | 30 ± 5 |

### 3.2.3 Characterisation of Transistors

All transistors are characterised by two Keithley 2400 source-meters, shown in figure 4, to extract transfer and output diagrams for each transistor. The testing parameters are controlled by Labtracer 2.0 software.

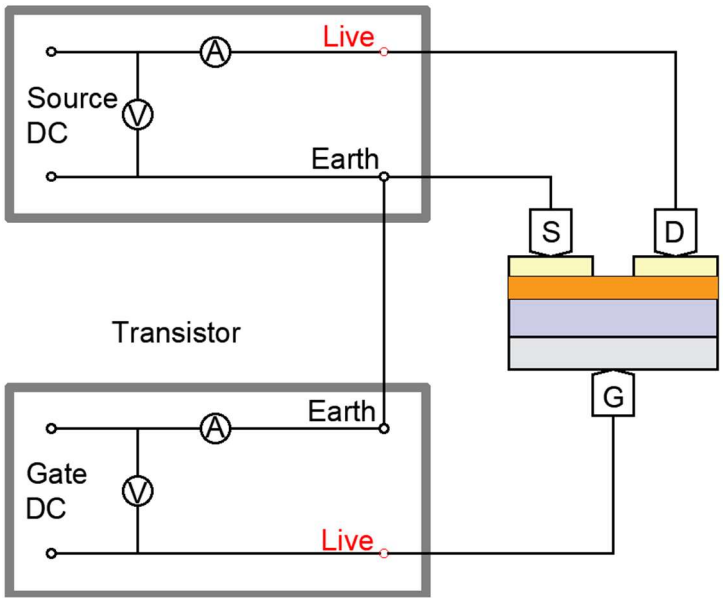



Figure 3.4. Circuit connection of Transistor Characterisation

Before characterisation of the transistor, source/drain short, source/gate short and drain/gate short-tests in voltage ranges of 0 – 40 V are carried out to assess the quality of semiconductor and insulators respectively. Any transistors with a shorting problem will be eliminated directly, and transistors without a shorting problem will be sent to the next stage for characterisation of transfer property and output property.

The transfer curve under high voltage is firstly measured. The gate voltage ($V_G$) varies from 20 V to –30 V, and drain voltage ($V_D$) is fixed at –30 V. If the drain current is very low at this voltage range, an alternative is to set $V_G$ in range of 10 to –40V and

$V_D$ to be fixed at –40V. For output measurement, $V_G$ varies from 0 to –40 V in steps of of –5V, and $V_D$ varies from 0 to – 40 V continuously.

### 3.2.4 Aging Tests of Transistors

All OTFTs are stored in the dark in a dry box immediately after fabrication. In the black dry box, the storage temperature is about 20 ºC and humidity is in the range of 5 – 10%. Transistors were tested in the dark repeatedly in a clean room after various times to test the aging behaviour of the transistors. The testing environment in the clean room was 15 – 25 ºC with humidity range from 30% to 60%. The total testing period was 15 days.

### 3.2.5 Bias Stress Test

Transistors in the same batch with similar performance were selected for long time bias tests. Due to the humidity variance between the storage box and the testing environment, transistors are conditioned in the testing room overnight (about 12 hours) prior to testing. Because the bias stress test applies a long-time test on transistors, and to avoid potential damage of the transistor during testing, a relatively low bias voltage (-10 V) and driving voltage (-10 V) are used instead of the typical testing parameters in characterisation of the transfer curve or output curve. Therefore, a transfer curve (from 5V to -10V) is tested to extract threshold voltage ($V_{th}$) before applying the bias voltage. After that, a constant gate bias voltage and a source-drain driving voltage are applied to the OTFT sample at the same time, shown in figure 4, and then the signal decay of drain current is monitored over time (about 1000s). Finally, the drain current decay curve can be used to estimate the shift of threshold voltage.

## 3.3 Results and Discussion

### 3.3.1 Performance Evaluation of OTFT

The shorting test is the first step to evaluate a batch of OTFTs, and problems usually arise from source/drain, source/gate or drain/gate. A source/drain short can be caused by the shadowing effect of the mask which can bend under the high temperature of the evaporation process, as illustrated in figure 3.5, source and drain are connected in the region of shadow effect, i.e., leading to short circuit. This issue can be alleviated by stronger fixation of shadow mask on substrate and by reducing the pressure of chamber to the range of $10^{-6}$ mbar because the evaporation temperature of materials in the boat is lower at lower pressure and so the shadow mask bending degree can be reduced.

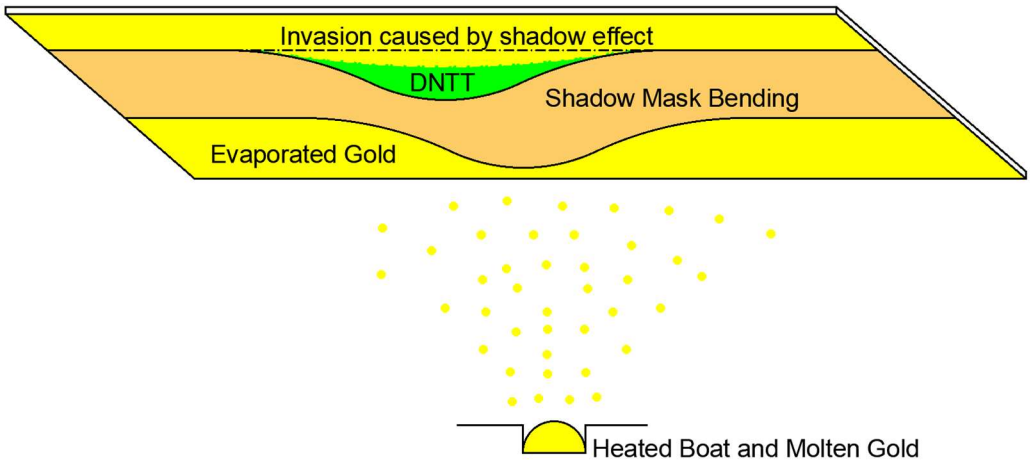



Figure 3.5. Shadow Effect caused by the deformed shadow mask

Because the manufacturing process is completed in four separate vacuum processes, contaminant deposits from the air onto the surface of the sample substrate are unavoidable. A contact/gate short is most likely caused by contaminants, which leads

to breakage of the thin film and thus contact between the top electrode and bottom electrode.

A series of batches of transistors were manufactured with various gate electrode and dielectric layer thicknesses to investigate the effect of these parameters on the yield of non-shorting transistors. From the results, presented in table 3.3 and figure 3.6, it is demonstrated that thickening the dielectric layer is helpful to reduce the probability of contact/gate shorting. However, in batch 6, the yield is still low despite a thick dielectric as the underlying gate electrode is thick as well, which might cause breakage of the dielectric layer at the electrode edge, leading to short circuit. Batch 7 has highest yield rate because its gate electrode is very thin and the dielectric layer is thick.

Table 3.3. Yield of transistors and thickness

| Batch | Gate Layer Thickness/nm | Insulator Thickness/nm | Yield (No. of Working transistors/Total production) |
|---|---|---|---|
| 1 | 191 ± 21 | 244 ± 67 | 17/108=15.7% |
| 2 | 97 ± 12 | 564 ± 18 | 54/63=85.7% |
| 3 | 70 ± 13 | 725 ± 27 | 50/57=87.8% |
| 4 | 95 ± 17 | 160 ± 20 | 1/18=5.6% |
| 5 | 57 ± 8 | 398 ± 40 | 8/18=44.4% |
| 6 | 78 ± 29 | 641 ± 16 | 14/27=52.2% |
| 7 | 30 ± 10 | 725 ± 10 | 384/418 = 91.8% |

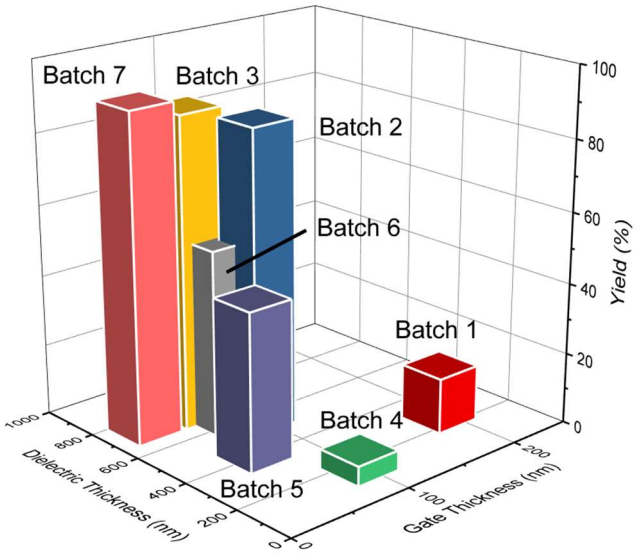



Figure 3.6. Comparison of Transistor Yield

Thus examination of the quality of several batches of transistors, suggested that thickness of gate electrode should be kept below 50 nm and thickness of insulator should be greater than 600 nm to make the insulator layer uniform at the edge of the gate and to reduce the shorting incidence. Because the evaporation of the aluminium has to be very fast to avoid oxidation of the aluminium during deposition, it is difficult to control thickness of aluminium lower than 50 nm on this static substrate, therefore, it was decided to use copper as the bottom gate electrode materials, as this can be evaporated more slowly, and hence make a more controllable thin layer.

In addition to shorting, another problem associated with a thin insulator layer is leakage of gate current, inducing some interference to output current. On the output curve of transistors, the starting point of the output curve deviates from the origin, leading to errors when it is fabricated in a circuit. Figure 3.7 displays a comparison of transistor output curve with and without current leakage.

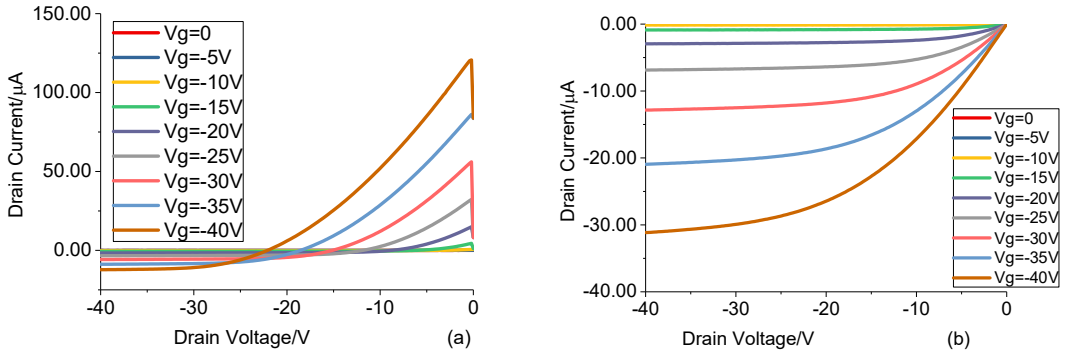



Figure 3.7. Comparison of Output Current from OTFT with (a) and without (b) leakage

When transistors are biased under -40V, and the drain voltage ($V_D$) is varied from 0 to –40V, the potential difference between drain contact and gate electrode varies from 40V to 0V. The leakage behaviour can be revealed by plotting Gate Current ($I_G$) against Drain Voltage ($V_D$). Shown in figure 3.8, for a stable transistor (right), the $I_G$ should not change and keep a very low level ($10^{-7}$ A) with continuous variation of $V_D$, while the $I_G$ of an unstable transistor (left) often exhibits a dependence on the $V_D$, and this dependence determines the deviation of $I_D$ on the output diagram.

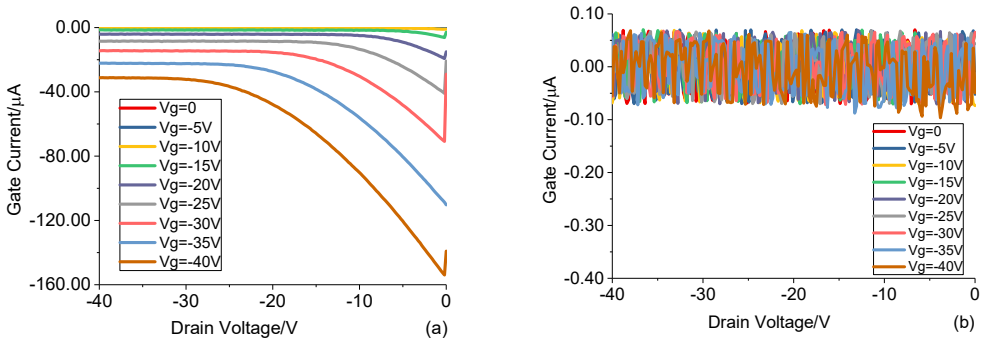



Figure 3.8. Comparison of Gate Current with and without leakage

In order to investigate the current leakage site, the current through the gate is extracted and plotted against drain voltage, and it can be divided into Source-Gate leakage (S/G), Drain-Gate leakage (D/G) and double leakage, i.e., gate current passing through source and drain at same time.

When leakage occurs, S/G leakage has only a small influence on the output performance of transistors. The gate current is a constant as bias voltage ($V_D$) increases because the potential difference between source and gate is a constant. As the gate voltage increase, the gate current increases. The internal circuit of the Keithley 2400, shown in figure 3.4, it is notable that leakage current between source and gate flows from gate to earth of the device directly without interference with the source/drain circuit. As a result, the output curve is associated with very low deviation even if the gate current is very high, shown in figure 3.9 (a) and (b).

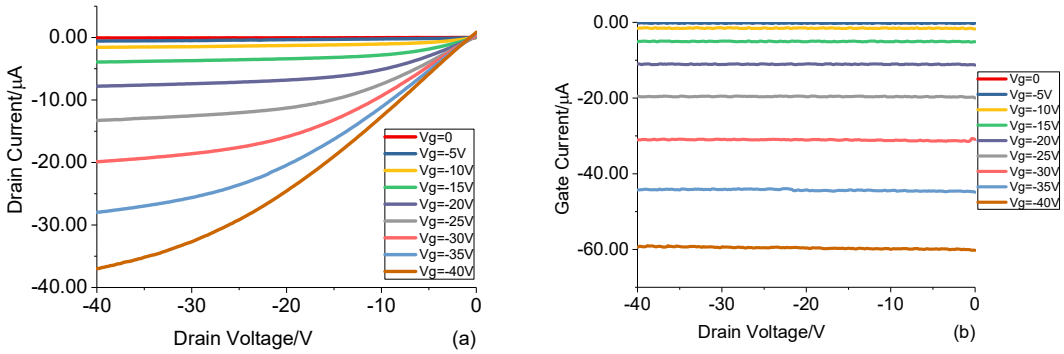



Figure 3.9. Output Current (a) and Gate Current (b) of transistor with S/G leakage

By contrast, D/G leakage has a very significant influence on the output performance of transistors. The potential difference between drain and gate varied from a maximum to zero as drain current increases, as a result, gate current exhibits a gradual decline when the device is on. From the internal circuit of the testing system, it is found that leakage current will flow into Source/Drain circuit when Drain/Gate leakage occurs

and the direction of Drain/Gate leakage is in the opposite direction to the Source/Drain current, therefore, interfering with the output current, i.e., resulting in deviation on the output curve of transistors, shown in figure 3.10.

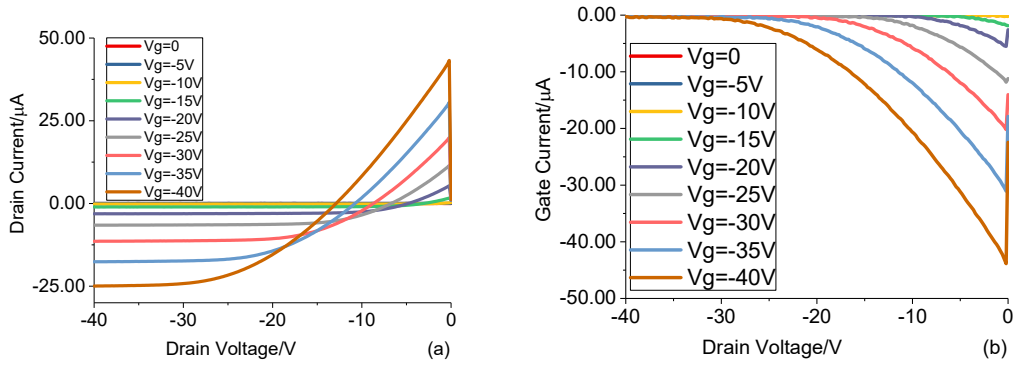



Figure 3.10. Output Current (a) and Gate Current (b) of transistor with D/G leakage

However, double leakage that means both Source/Gate leakage and Drain/Gate leakage occur at same time, which often leads to significant deviations on the output curve of transistors. Figure 3.11 displays the output curve of transistors with double leakage. On the diagram of $I_G$ – $V_D$, these curves have similar shape, the movement of the baseline indicates source/gate leakage and the gradual decline of gate current with increasing drain voltage indicates drain/gate leakage. To solve this problem, it is less effective to remove the influence of leakage current by simply switching the source and drain electrodes and the quality of dielectric layer must be improved to avoid double leakage.

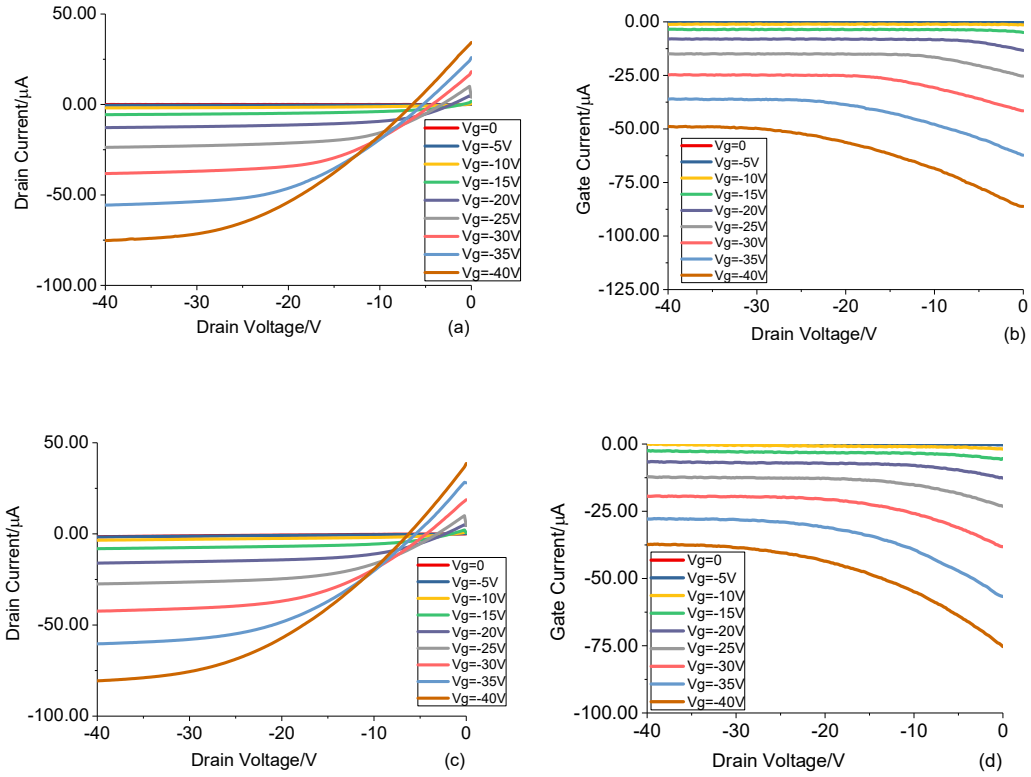



Figure 3.11. Output of Transistors with S/G and D/G Leakage

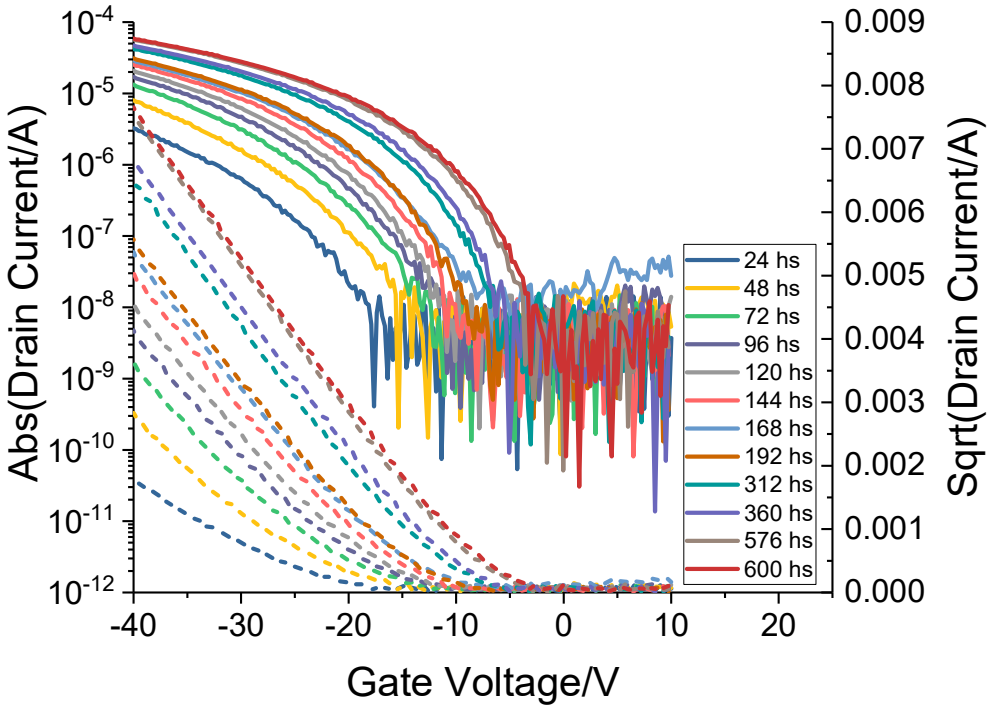
Thickening the TPGDA layer is a method to reduce leakage current to a negligible level, but this is dependent on the drain current level, i.e., this method is effective when the drain current is much higher than the leakage current. For transistors exhibiting a small output signal, the effect of leakage current cannot be neglected. In addition, surface contaminants are possible leakage site, and surface cleaning that is carried by spraying with isopropanol followed by air duster drying is very helpful to reduce the probability of current leakage.

Although the single side leakage has a very small effect on the output current, it still increases the difficulty and cost of manufacturing because the leakage site must be avoided when it is fabricated in a circuit. In production, the leakage current should be tested from each contact electrode before characterisation of the transistor because S/G

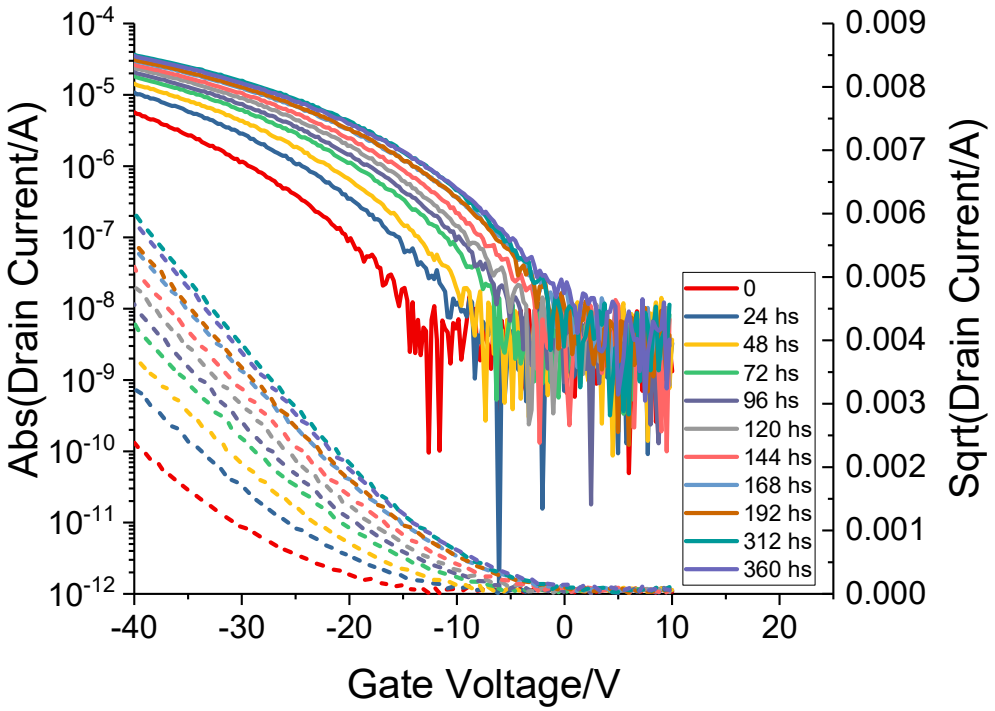
leakage is not easily recognizable from the transfer and output curves. By this means, the uncertainties in circuit fabrication can be reduced.

### 3.3.2 Stabilization of OTFT in Ambient Environment

It has been found that OTFTs often exhibit a poor performance when first fabricated, and a certain time of aging is helpful to stabilise the performance of the OTFT. In the previous research [157], it was shown that the performance of OTFTs can be stabilized after 48 hours aging treatment in an ambient environment, but the relationship between stability and aging time has not been investigated in detail for these devices.




(A)




(B)

Figure 3.12. Variance of Transfer Curve over Time for single transistor (Sample A and Sample B)

In figure 3.12, comparisons of transfer curves and output curves over time are given. It is noticeable that the drain current increases significantly over the first several days of storage. Applying the square law equation, described in the literature review (Section 2.2.3), on these transfer curves, the mobility and threshold voltage can be extracted. Even within the same batch, each OTFT exhibit different mobility and threshold voltage. In the batch under study here, mobility varies in range from 0.2 $cm^2/(Vs)$ to 1.1 $cm^2/(Vs)$ with a mean of 0.58 $cm^2/(Vs)$ and standard deviation of 0.21, and threshold voltage varies in range of -6V to -14V with mean of -11V and standard deviation of 1.9V.

Plotting mobility and threshold voltage against aging time for each of the transistors, stabilisation diagrams are obtained, shown in figure 3.13 and 3.14. It is noticeable that mobility increases during the initial aging stage and become less dependent on the aging time after a while. Generally, after approximately two weeks (about 300 hours), the mobility of most transistors has levelled off and stays almost unchanged with time.

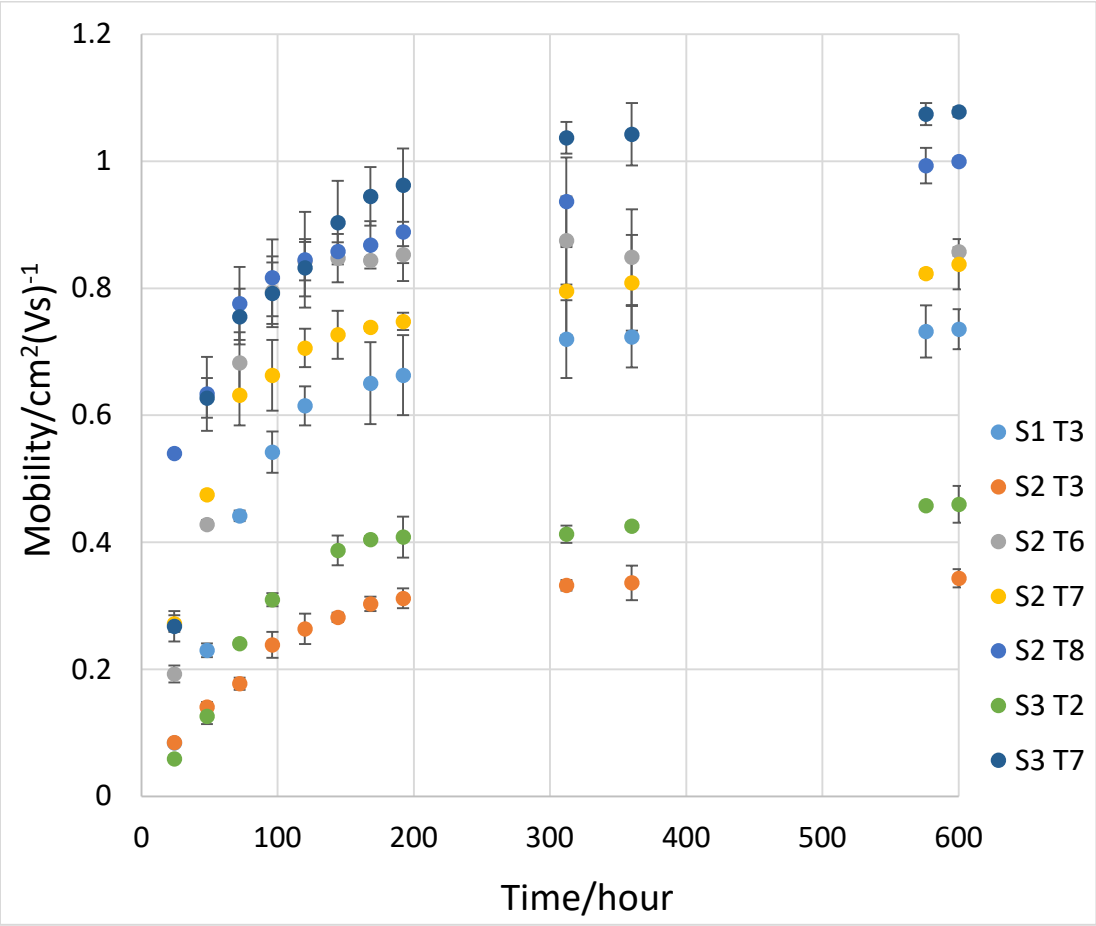



Figure 3.13. Variance of Mobility against Time

The variance of threshold voltage exhibits a longer dependence on aging time, i.e., the threshold voltage can decrease with time even once the mobility has stabilised. In the aging period of 600 hours, the threshold voltage decreases significantly and there is no obvious stabilisation phenomenon until 600 hours for most of the OTFTs.

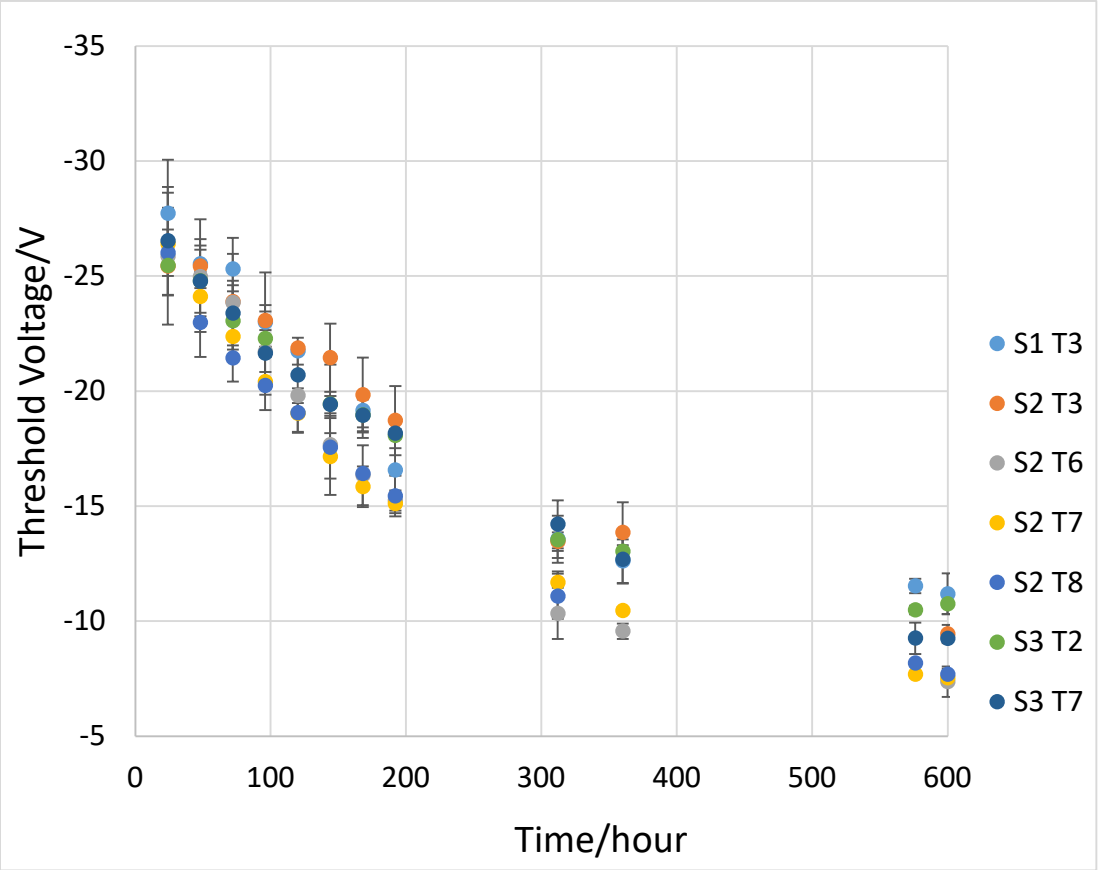



Figure 3.14. Variance of Threshold Voltage against time

The mechanism of the stabilisation is still in debate, and there are two possible mechanisms after oxygen doping; extra charge carriers created by p-type doping and enhanced injection of charge carriers.

In the researches of Nayak *et al*., the oxygen doping mechanism demonstrates that electrons in the semiconductor grains are extracted by oxygen adsorbed onto the grains due to high electron affinity of oxygen [31]. Although the research of Nayak is based on pentacene, this mechanism is likely suitable for DNTT due to the structural similarity between pentacene and DNTT. When DNTT is exposed in dry air, oxygen can diffuse into the DNTT semiconductor along the grain boundaries and reaches the dielectric/semiconductor interface. As a result of electron extraction, the concentration of holes in the bulk DNTT grain is increased, facilitating the transport of electric

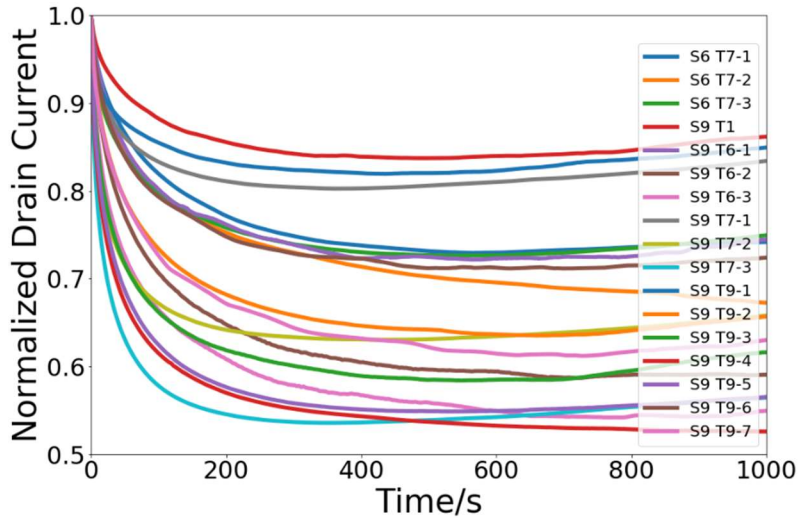
charge, and gradually saturates at the dielectric/semiconductor interface, i.e. further improvement of mobility becomes limited. Another mechanism is a reduction of the energy barrier for injection of charge carriers. The extra p-type dopant (oxygen) alters the activation energy barrier for injection of charge carries and as a result, more holes are supplied, i.e., the threshold voltage is decreasing under exposure to the ambient environment over time. A possible reason is that diffusion path to the interface of the electrode/semiconductor is more difficult than the path to conductive channel. Oxygen saturation occurs at the conductive channel firstly and oxygen-doping still occurs at the electrode/semiconductor interface, as a result, threshold voltage keeps decreasing over longer time. However, the longer-term stabilization of threshold voltage has not been investigated.

### 3.3.3 Model Validation for Bias Stress

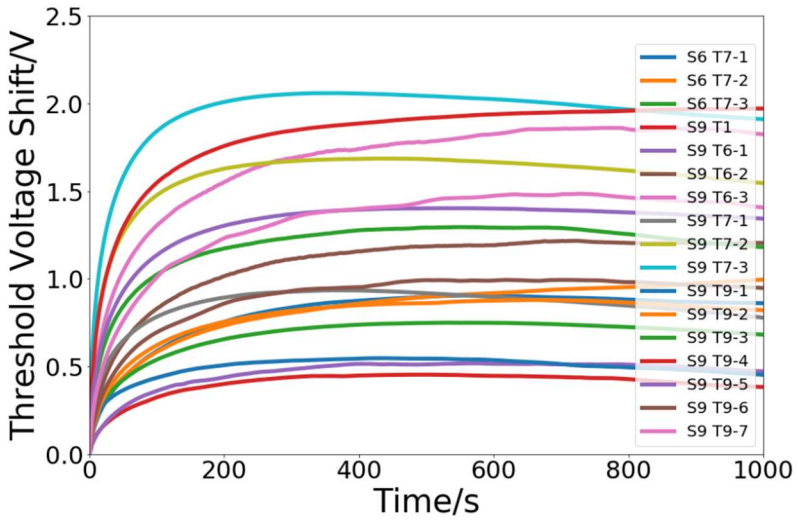
In order to investigate the instability against time, there are two methods to extract data, and Za'abb and Taylor suggested that there are two methods to build up the relationship between threshold voltage shift and bias time. The first method is to immediately measure $\Delta V_{th}$ from the transfer curve after a bias of constant voltage, and the second method is to estimate it from the decay curve of drain current ($I_d$). Because relaxation occurs after the bias voltage is removed, there is an error associated with measurement of $\Delta V_{th}$ from the transfer curve. In addition, the repeated operation in first method is more time-consuming than the second method, which is capable to continuously collect more data points. Thus, threshold voltage is converted from continuous current decay with equation 3.1 shown below [158],

$$\Delta V_{th}(t)^2 - 2\big(V_G - V_T(0)\big)\Delta V_T(t) - \big(V_G - V_T(0)\big)^2 \frac{\Delta I_D(t)}{I_D(t)} = 0 \ldots\ldots (3.1)$$

Example decay curves of drain current are plotted in figure 3.15 (a). For most of the transistors, a rapid current decay occurs in the initial 300s, after which the decay becomes slow. Although the results are similar to the current decay from previous research [158], some transistors exhibit a slight increase in the current after long times. The slight current improvement is possibly contributed by a variance in the humidity of the testing environment because the adsorption of moisture facilitates the transport of charge.




(a)




(b)

Figure 3.15. (a) Decay of Drain Current over Time (b) Shift of Threshold Voltage over Time calculated from Equation (3.1)

After solving equation (1), the shift of threshold voltage can be plotted, shown in figure 3.15 (b), which starts with a rapid change which then gradually slows down. To describe the shift of threshold voltage, a stretched-exponential time dependence model is widely applied in recent years on thin film transistors, introduced in literature review (Section 2.2.5), in which charge trapping initially occurs in shallow traps where de-trapping can occur, and then is transferred to deep trap sites where de-trapping is difficult. However, the source of trapping is still unclear from the perspective of the materials. Defect trapping in the semiconductor and at the semiconductor/dielectric interface are widely investigated mechanisms [159]. Recently, a mechanism of charge tunnelling was explored in amorphous Silicon (a-Si) and InGaZnO thin film transistors [48, 160] but not used to study OTFTs, and this model will be adapted to the experimental results to study the possible dominant trapping mechanism for OTFTs under research in this chapter.

In this model, tunnelling and back-tunnelling of charge carriers is assumed as the dominant mechanism of charge carrier trapping. As shown in figure 3.16, there is a trapping energy ($E_T$) between the HOMO and the Fermi level, and $E_T$ is bent through the TPGDA insulator. It is assumed that the energy difference ($\phi = E_T - E_F$) decreases as one moves away from dielectric/semiconductor interface to the bulk insulator [160] and there is a critical distance from the interface ($x_0$), beyond which charge carriers that have tunnelled into the insulator cannot easily tunnel back to the semiconductor.

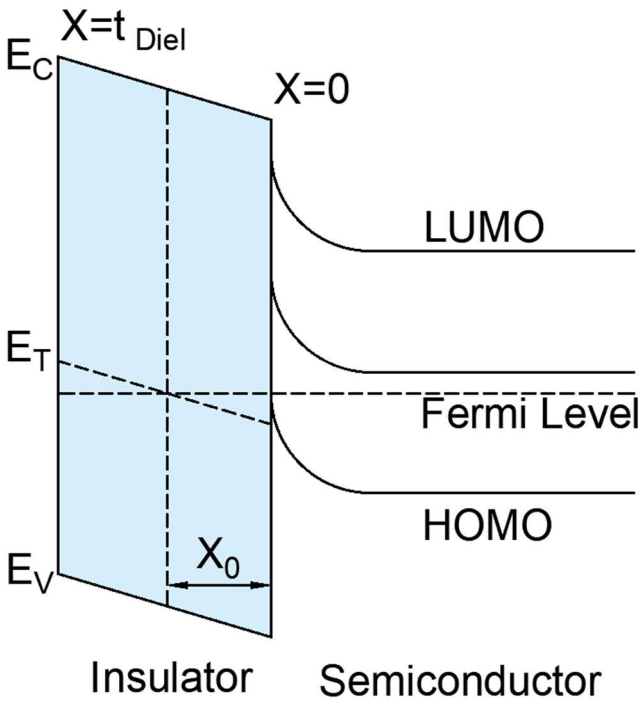



Figure 3.16. Energy Band Diagram of TPGDA/DNTT Interface

The value of critical distance is dependent on the energy difference, gate voltage, and thickness of the insulator. It can be estimated by equation (3.2),

$$x_0 = \frac{\phi}{q * {V_G}/{t_{Diel}}} \dots\dots (3.2)$$

where, $q$ is elementary charge, $V_G$ is gate bias voltage and $t_{Diel}$ is thickness of the dielectric materials. Usually, $x_0$ is a static distance. When bias voltage is applied, the actual charge carrier distribution evolves with increasing bias time. The distribution of trapped charge carrier ($n_{tr}$) and the dynamic transfer front ($x_1$) are described by equation (3.3) and (3.4),

$$n_{tr} = \frac{N_T}{1 + \frac{1}{1 + \exp\left(-\frac{\phi\left(1 - \frac{x}{x_0}\right)}{V_{nt}}\right)}} \left\{1 - \exp\left[-\exp\left(-a(x - x_1)\right)\right]\right\} \dots\dots (3.3)$$

$$x_1 = \frac{1}{a}\ln\left[S_0 v n_s t\left(1 + \frac{1}{1 + exp\left(-\frac{\phi\left(1-\frac{x}{x_0}\right)}{V_{nt}}\right)}\right)\right] \ldots\ldots (3.4)$$

where $N_T$ is the intrinsic trap concentration in the insulator, $S_0$ is the capture cross-section at the interface, usually assumed to be $1 * 10^{-17} cm^2$ and $a$ is a decay parameter which can be described by equation (5),

$$a = \frac{2}{h}\sqrt{2m^* E_t\left(1 - \frac{qFx}{2E_t}\right)} \ldots\ldots (3.5)$$

where $h$ is Planck constant ($6.626 * 10^{-34}\ m^2 kgs^{-1}$),

$m^*$ is equivalent mass of electron, which is usually assumed that $m^* = 0.6m_e = 5.466 * 10^{-31}\ kg$,

$E_t/eV$ is height of energy barrier,

$F/(V/m)$ is the electric field across insulator,

$x/m$ is the tunnelling distance, and it is usually less than 15 nm, therefore, the electric field-dependent term $\left(\frac{qFx}{2E_t}\right)$ can be ignored, and decay parameter is only dependent on the height of energy barrier.

In equation (4), $v$ is thermal velocity of electron ($1.168 * 10^7\ m/s$),

$t/s$ is total bias time,

$n_s$ is density of charge carrier trapped at interface, which is described by equation (3.6),

$$n_s = \frac{C_i^2 V_i^2}{q\varepsilon\alpha V_{therm}} \dots\dots (3.6)$$

where, $C_i$ is gate capacitance per unit area,

$V_i$ is the potential drop across insulator, i.e., voltage difference between $V_G$ and $V_{th}$ $(V_G - V_{th})$,

$\varepsilon/(F/m)$ is dielectric constant,

$V_{therm}$ $/V$ is thermal voltage (0.0257 V under ambient temperature),

$\alpha$ is a constant can be estimated by equation (3.7), under the assumption of that the potential drop by contact resistance is much lower than the driving voltage ($V_{DS}$),

$$\alpha = \frac{V_{GS} - V_T}{\frac{\int_0^{V_{GS}} I_{DS,sat}(v_{gs}) dv_{gs}}{I_{DS,sat}(V_{GS})}} \dots\dots (3.7)$$

where, $V_{GS}, V_T, I_{DS,sat}$ are gate voltage, threshold voltage, and drain current respectively,

After obtaining the constant $\alpha$, the characteristic slope ($V_{nt}$) can be estimated by equation (3.8),

$$V_{nt} = \alpha * \frac{V_{therm}}{2} \dots\dots (3.8)$$

Extracting $I_{DS} - V_G$ data from the transfer curve of each transistor, the trapped charge carrier density can be approximated, and plotted against distance and time.

Over a fixed time, the density of trapped charge carriers can be determined and the shift in voltage at this moment can be approximated by an integration of trapped charge

carriers over distance from the semiconductor/dielectric interface across the entire insulator, shown in equation (3.9),

$$\Delta V_{th}(t) = \int_{x_0}^{t_{Diel}} \frac{q n_{tr}(x) S_e}{\varepsilon_{Diel} S_i / (t_{Diel} - x)} dx \ldots\ldots (3.9)$$

where $\varepsilon_{Diel}$ is dielectric constant of insulating material, and $S_e, S_i$ are gate electrode area and gate insulator area respectively, and these two areas are same for the BGTC architecture.

The trapping density of OTFTs has been measured in previous research [161, 162], however, there is not specific research focusing on the measurement of trapping density and trapping energy of the insulator, so as a result, these two parameters need to be estimated.

Because the threshold voltage shift is not a linear function with trapping density and trapping energy level, a numerical analysis has to be applied instead of conventional linear regression analysis. After obtaining the transfer curve from each transistor, parameters, such as $x_0$, $n_s$ and $V_{nt}$ can be extracted, and then trapping density and trapping energy value are initialized in a specific range from $10^{15}$ to $10^{22}$ /cm$^3$ and from 0 to 0.5 eV, estimated from previous research [162] to reduce the parameter searching space. In the limited range, the threshold voltage shift curve is simulated at each point and then a cost function is calculated by the absolute value between experimental and simulated threshold voltage shift curve. After intensive iterative computing, a minimum of cost function is detected in the limit space and the simulated threshold voltage shifting curve is defined as the most similar curve to the experimental result, shown in figure 3.17.

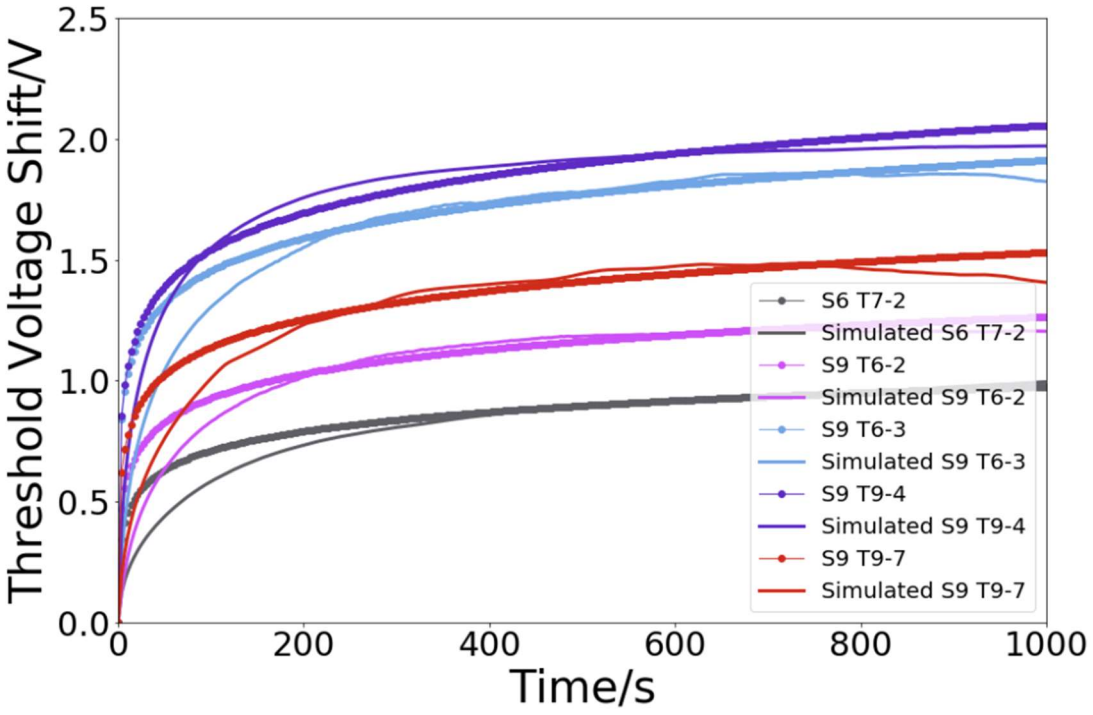



Figure 3.17. Experimental and Simulated Threshold Voltage Shift

Consequently, the trapping density and trapping energy levels are approximated. After that, a density function of trapped charge carriers can be plotted against distance from interface and time, shown in figure 3.18. An evolution of the transfer front can be visualized on each curve, and it increases with longer bias time.

Because the varying performance of different individual OTFTs, the estimated trapping density and trapping energy level varies within a limited range. The evolution trends are similar, trapped charge carriers are close to a constant near the interface and then experience a rapid decrease over distance from the interface when bias time is very short. With prolonged bias time, the profile of trapped charge carriers start to moving forward deep region of insulator and exhibit an increment before rapid decrease.

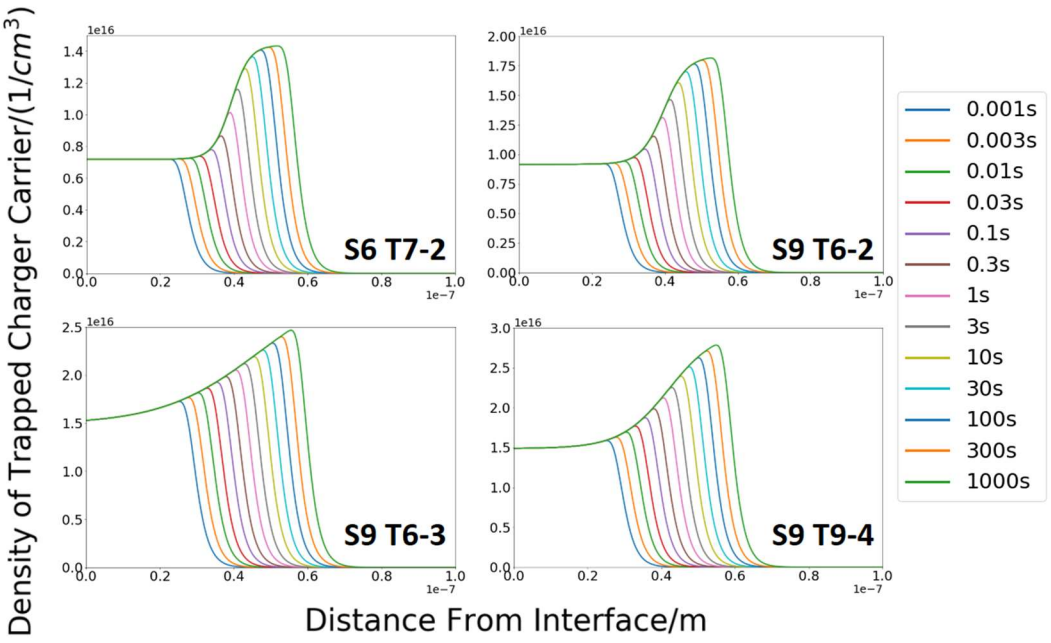



Figure 3.18. Density Evolution of Trapped Charge Carrier over Distance from Interface under Different Bias Time

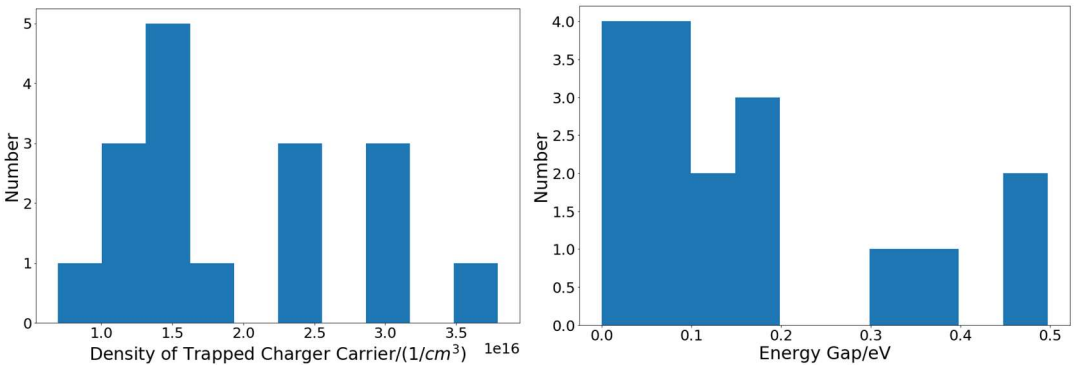



Figure 3.19. Histogram of Trapping Density and Trapping Energy for all the transistors in Batch 7

From the histogram in figure 3.19, the trapping density is distributed in the range of $6.95 \times 10^{15}$ cm$^{-3}$ to $3.79 \times 10^{16}$ cm$^{-3}$ with mean of $1.93 \times 10^{16}$ cm$^{-3}$ and trapping energy is distributed in the range from 0 to 0.5 eV with mean of 0.166 eV. In previous research [161, 162], trapping density is a function of interfacial voltage, and it is distributed in

the range from $10^{17}$ to $10^{22}$ /cm$^3$ which is much higher than the estimated intrinsic trapping density in the insulator here. Therefore, charge traps in the dielectric material is probably not the dominant mechanism for the threshold voltage shift in the OTFT in this project. The traps caused by defects in the semiconductor and at the semiconductor/interface might be dominant, but this needs to be studied separately in future. Alternatively, as the number space for parameter estimation is limited due to computing capability, there might be an optimum that has not been found in the limited space explored. To explore possible parameters in a wider space, a fast optimisation algorithm and more computing capability are needed. From the perspective of manufacturing, the number of tested samples in this section is not enough to provide statistical support, and more samples need to be tested to provide a more statistically confident estimation of parameters, i.e., intrinsic trapping density and trapping energy.

## 3.4 Summary

The thickness of the gate electrode and dielectric layer are very important for reliable manufacture of OTFTs in a large scale. A thinner dielectric layer is favourable for transistors to keep the threshold voltage low, but micro-particles on surface of the substrate might lead to breakage of dielectric layer, and the edge of the gate electrode can lead to shorting with a thin insulator. As a result, it was found that the thickness of the TPGDA layer should be greater than 600 nm and thickness of gate electrode should be less than 50 nm. Additionally, short circuit between source and drain electrodes can be avoided by lowering the chamber pressure to have a lower evaporation temperature leading to less mask distortion and hence shadow effect. Gate current leakage is a significant problem for OTFTs, and the leakage can be limited by

thickening the TPGDA layer above 600 nm approximately. In order to avoid the potential error caused by leakage current, it is needed to measure the leakage current from source and drain electrode of each single OTFT before circuit fabrication.

Aging in oxygen is a relatively effective and easy way to increase mobility and reduce threshold voltage of OTFTs. Current data indicate the rate of increment in mobility is very small after 144 hs for most OTFTs, although some OTFTs may need an aging treatment of 192 hs. However, threshold voltage displays a continuous decline over a longer time, and only begins to stabilize after 500 hs. In the industrial application, a customized aging scheme considering optimization of temperature and oxygen content is needed to reduce overall aging time.

Finally, bias stress is an intrinsic property for thin film transistors that are affected by complex mechanisms of charging trapping states. In this chapter, the charging of dielectric trapping states is considered as a potential source of bias stress and a model which is used to simulate threshold voltage shift is used to estimate the trapping states density. However, the estimated trapping density is much smaller than the reported data, indicating that charging dielectric materials is probably not the dominant contribution for the bias stress in DNTT-based OTFTs.

# Chapter IV

## 4.1 Introduction

A floating gate (FG) is a particular structure that may be placed between the gate dielectric layer and the control gate, isolated by insulating materials, as shown in figure 4.1. As discussed in the literature review (section 2.4.1), a floating gate can be used to store electric charge inside the transistor. It can be used not only as a memory device, but also an electrode for sensing.

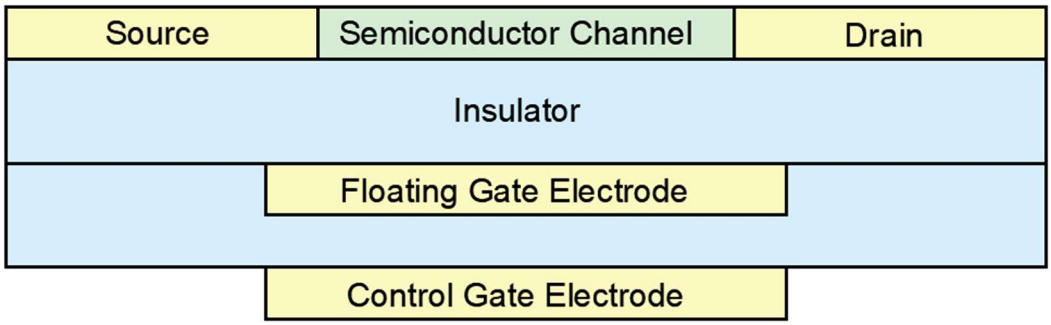



Figure 4.1. Schematic of Floating Gate Transistor

The basic mechanism of floating gate field effect transistors, such as MOSFET and OTFT is to detect variance in charge on the floating gate where the effective bias voltage of the transistor is shifted to induce a significant change of channel current from source to drain [163]. It is described by equation (4.1),

$$V_T^{FG} = \frac{C_{OX} + C_{FG}}{C_{FG}} V_T^{CG} - \frac{Q_{FG}}{C_{FG}} \dots\dots (4.1)$$

where, $V_T^{FG}$ and $V_T^{CG}$ are threshold voltage on the floating gate and control gate, $C_{OX}$ and $C_{FG}$ are the capacitance per unit area between channel and floating gate and

capacitance per unit area between control gate and floating gate on the MOSFET and the floating gate respectively, and $Q_{FG}$ is the amount of electrical charge on the floating gate. From this equation, it is seen that the threshold voltage shift is linearly related to the charge variance, but the channel current is not strictly linear to gate bias voltage. The transistor is usually pre-biased to the region where channel current exhibits a quasi-linear response to bias voltage, and then altering the amount of charge on the floating gate achieves a linear sensory response.

As a ferroelectric polymer, poly-vinylidene fluoride (PVDF) is able to convert mechanical strain to a potential difference between top and bottom surface of a thin film of the material. As a result, strain sensors are often fabricated as a capacitor with PVDF with an accurate voltage meter to detect micro-scale strain changes.

In this chapter, ferroelectric PVDF created by a spin-coating with heated-substrate is described firstly, and the PVDF produced in this way is examined with FTIR. After a series of annealing treatments under different temperatures and times, a complete process from original PVDF pellet to ferroelectric PVDF film to obtain highest ferroelectric phase in PVDF is described. Afterward, a simple example of PVDF-integrated FGOTFT sensor is created and tested to demonstrate the response to strain variance. To measure strain change on a thin film, a buckling test device is built up based on the buckling strain model which is capable to estimate the variance of surface strain with displacement distance. Next, a PVDF-coated floating gate is placed on the buckling test device to establish the relationship between strain and the output current of the FGOTFT. Due to the presence of bias stress in the OTFTs, continuously testing with long time bias introduces and extra error with longer testing time, so a novel testing method using a series of short-time biases followed by an interval of no bias is

described. A trade-off between length of bias and length of interval, is used to measure the output signal when the floating gate is stressed. Finally, a series of linear relationships is built up between input strain level and output drain current signal under different bias voltages.

## 4.2 Experiments

### 4.2.1 Thin Film Processing for PVDF

In the literature review (section 2.4.2), multiple methods to fabricate ferroelectric PVDF thin films, such as mechanical stretching, molten quenching and solution casting were described. In this chapter, spin-coating, which is an example of solution casting is employed to create a PVDF thin film. Because of the polar groups of the PVDF molecule, a polar solvent, dimethyl sulfoxide (DMSO) is used to dissolve PVDF pellets into solution. In previous research, DMSO has been shown capable to facilitate formation of ferroelectric phase in PVDF (β-PVDF) [84, 86, 164-166].

The PVDF pellets (Sigma-Aldrich) used in this project have a number average molecular weight of 107000 g/mol. Dimethyl Sulfoxide (DMSO) purchased from Sigma-Aldrich, was used as a solvent to make 10wt%, 15wt% and 20wt% solution. Because the high molecular weight and pellet state of PVDF, the PVDF is dissolved in DMSO by stirring for 2 hours at 150 $^{o}$C under magnetic stirring and a reflux condenser. Each pellet starts to dissolve within the first 30 mins. A relatively long time of dissolution is helpful to remove any residual crystals of PVDF because any residual α-crystals may induce formation of undesirable α-crystals during spin coating as the PVDF films are produced [167].

Due to the high viscosity of the PVDF/DMSO solutions, they are initially heated in a water bath to a temperature in the range from 90 ºC to 95 ºC to reduce viscosity and enable good fluidity of solution during spin coating. In addition, the cold surface of the substrate has been found to deteriorate the film quality [165], therefore, the chuck of the spin coater and glass slide are initially heated to 90 ºC or above to facilitate the spreading of the viscous solution. In the work of Cardoso *et al*., a relationship between spinning rate and content of β-phase is revealed, indicating that high spinning rate is helpful to produce more β-phase, however, as expected, the thickness of the film is reduced at high spinning rate [168]. In this chapter, a Laurell WS-650-SZ-6NPP/LITE spin coater is used with a range of spinning speed from 1000 rpm to 8000 rpm. When the plastic (PEN) substrate is fixed on spin coater, a glass substrate is required because the PEN substrate is deflected when it is directly fixed on the spin coater by the vacuum chuck, shown in figure 4.2.

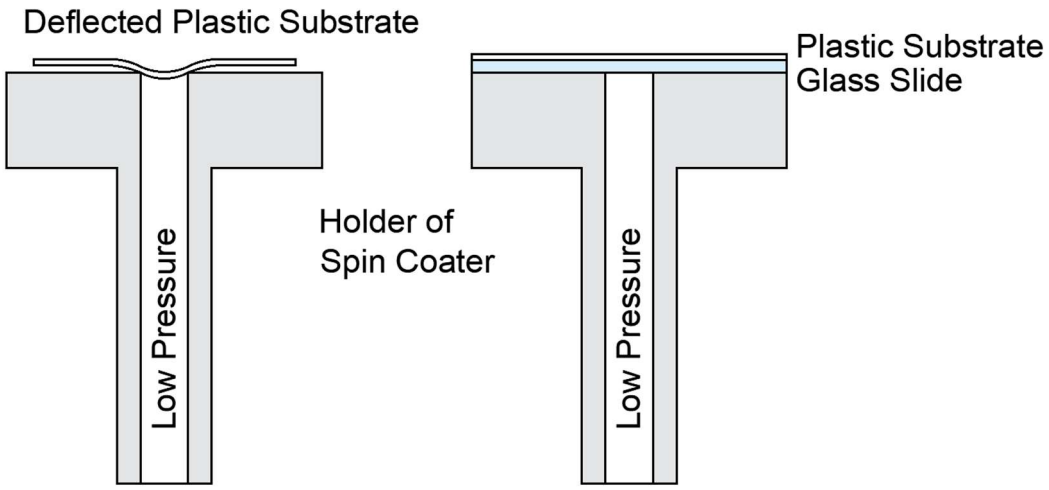



Figure 4.2. Schematic of Fixation of Substrate on Spin Coater Holder

After spin coating, PVDF is annealed under different temperatures between 60 ºC and 150 ºC and different times, between 1 h and 24 hours, to promote formation of the β-

phase and to evaporate residual DMSO solvent. Afterwards, Vecco Dektak is used to measure the thickness of the PVDF thin film and Varian Excalibur Fourier-Transform Infrared (FTIR) spectrometer with attenuated total reflectance (ATR) instrument is used to examine the conformational character of the molecular chains of PVDF, with wavenumber ranging from 700 $cm^{-1}$ to 3500 $cm^{-1}$ and 64 scans on each sample.

### 4.2.2 Fabrication of Floating Gate OTFT with PVDF

The structure of the PVDF-coupled FG-OTFT is shown in figure 4.3. The fabrication process of the FGOTFT is similar to the process to manufacture OTFT (section 3.2.1); following the sequence of floating gate, dielectric layer (TPGDA), buffer layer (PS), semiconductor (DNTT) layer and contact electrodes and finally, deposition of the control gate on top of the dielectric materials. However, before making the semiconductor layer, PVDF needs to be deposited on the functional area of the floating gate because the annealing temperature of the PVDF might introduce extra oxidation of organic semiconductor. Because the solution during the spin coating process will flush over all the sample area, to avoid any organic solvent damage to the gate electrode that will be used to build the OTFT, a protective film is fixed at the edge of functional area, shown in figure 4.4. Next, the PVDF thin film is created on the area of floating gate by spin coating, and then annealed with optimized temperature and time.

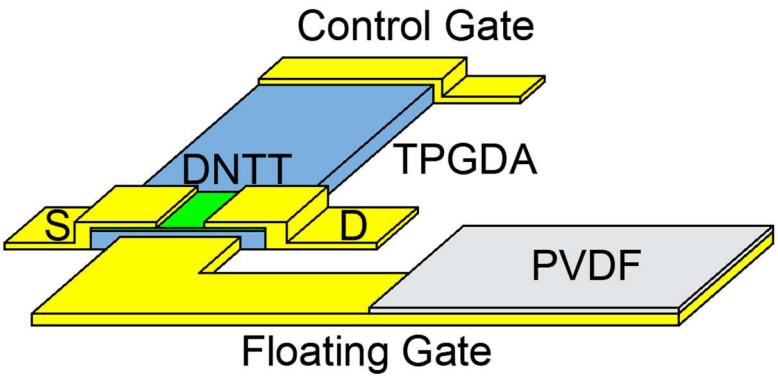



Figure 4.3. Schematic of Floating Gate OTFT coupled with PVDF

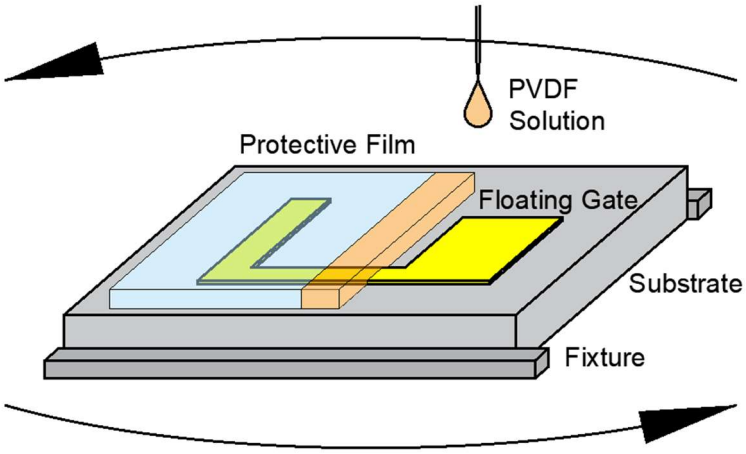



Figure 4.4. Schematic of Selective Spin-coating on Floating Gate

After annealing, the sample is transferred to a custom-built Corona poling system which consisted of a sharp needle connected to high voltage source (10 – 30 kV) and positioned 5 – 20 cm above ground electrode [169]. In the work reported in this chapter, three different strong electric fields were generated with voltage of 20 kV with various distance (5 cm, 10 cm and 15 cm) between sample and tip, shown in figure 4.5. The PVDF coated sample is placed in this system for 30 mins under an optimized temperature at which β-crystal is promoted. Finally, the OTFT can be directly constructed on floating gate with E306 and Oxford Web-coater with parameters (section 3.2.1).

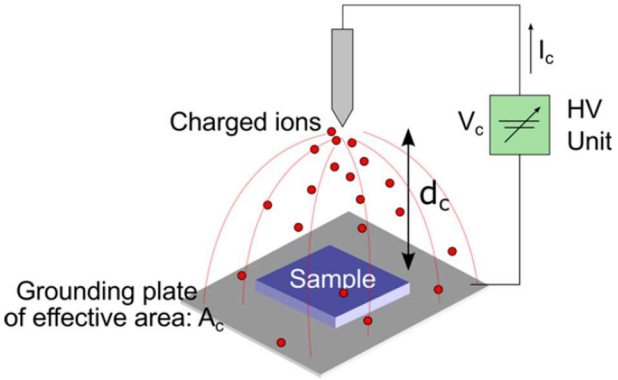



Figure 4.5. Schematic of Corona Poling System [169]

### 4.2.3 Optimization of Bias Voltage and Time

As discussed in the last chapter, the current decay in the drain current – time curve is caused by the bias stress which is an intrinsic property for OTFTs. Although it is difficult to avoid this problem, the current decay is reversible after removing the bias stress. The continuous bias scheme can be replaced by a series of short-term biases with a fixed recover time after bias. In this scheme, to explore a suitable bias-relaxation condition, there are three factors to be controlled separately, bias voltage, bias time and recover time.

In a first series of experiments, the FGOTFT is biased under the same voltage with varied bias time. In a second series of experiments, the transistors were biased for the same period time with varied bias voltage. After short time bias, a fixed length of recovery time is set to 30s. After that, the decay percentage under different bias voltage will be compared with fixed bias time and that under different bias time will be compared in fixed bias voltage.

### 4.2.4 Construction of Buckling Bending Strain Measurement

The buckling bending machine was developed with one fixed clamp and one mobile clamp controlled by a motor, shown in figure 4.6. Two steel rulers are fixed to form a track along which a mobile clamper can move forward and backward. The thin film sample is fixed in the clamps, and the mobile clamp is moved toward the fixed clamp with a constant speed (about 1 mm/s) by adjusting the controlling current from a Keithley 2400. Based on the buckling model which is discussed in next section, the surface strain of sample can be estimated.

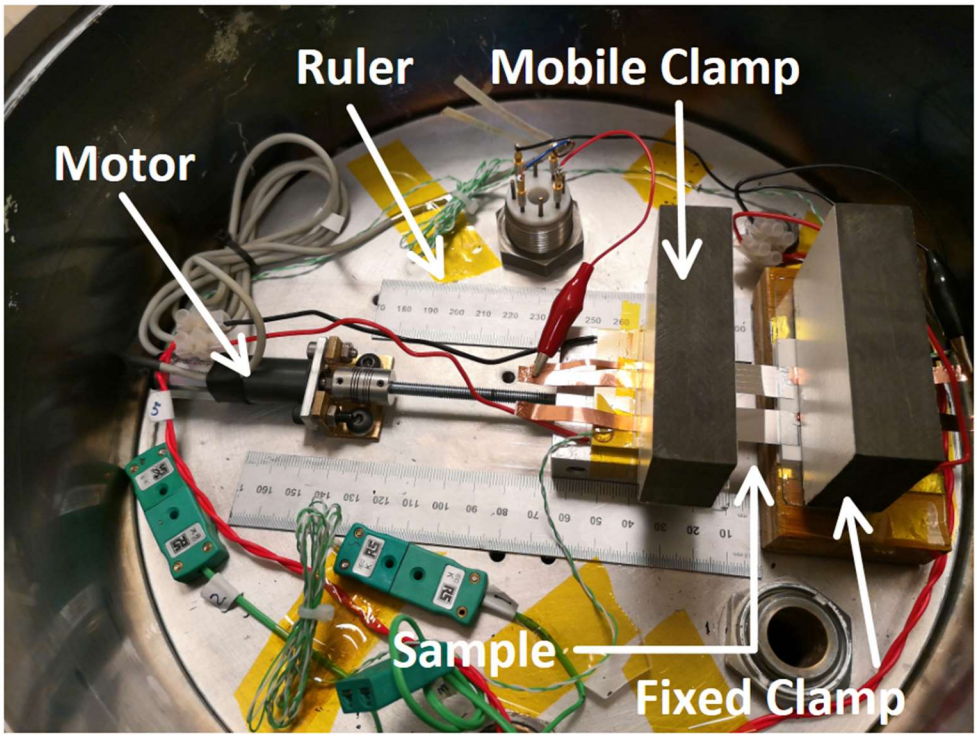



Figure 4.6. Schematic of Buckling Bending Strain Machine

### 4.2.5 Measurement of Sensory Response under Different Strain

To reduce errors from the bias stress, a series of short time biases is used to measure drain current before applying strain on the floating gate. Because electric charge can

be stored on the floating gate, bending strain is applied to a flexible PVDF coated floating gate and then the device is switched on for a short time to read out the drain current under this condition. After each measurement, an increased strain is applied to the PVDF-coated floating gate and the drain current measured, until finally, the drain current against strain level can be plotted to obtain a calibration curve for strain sensing. In this case, a commercial PVDF thin film with controlled properties and quality, rather than the spin-coated layers is connected to the floating gate to demonstrate sensory response and signal transducing capability of FGOTFT.

## 4.3 Discussion

### 4.3.1 Harvesting a high content of ferroelectric phase

Spinning speed is a very important factor affecting the β-phase content of PVDF because a higher spinning speed promotes stronger shear stress in molecular chains to align them into the lattice of the β-crystal, hence, spinning speed should be as fast as possible. However, in this work, fixing the substrate on the spin coater is not very stable when spinning speed is above 5000 rpm, with the glass substrate tending fall, damaging the sample film. In addition, the viscosity of the polymer solution is very significant for the formation of thin films. Although a 20wt% PVDF/DMSO solution can be made, it exhibits very high viscosity even when heated to 90 $^{o}$C, such that it cannot be dropped onto the coater with a normal pipette, hence, only solutions of 10 wt% and 15wt% were finally used to produce PVDF thin film by spin coating.

From Dektak, the thickness of PVDF spin-coated from 10wt% and 15wt% solution has similar thickness, 1.1 ± 0.2 μm. The FTIR spectrum of PVDF is displayed in figure

4.7 (a), and the spectrum range from 740 $cm^{-1}$ to 860 $cm^{-1}$ has been shown in figure 4.7 (b). The peak absorbance at 766 $cm^{-1}$ and 840 $cm^{-1}$ can be used to calculate the relative content of β-phase in crystal phase by the equation below [170, 171]:

$$F(\beta - phase) = \frac{A_\beta}{\frac{K_\beta}{K_\alpha}A_\alpha + A_\beta} \dots\dots (4.2)$$

where, $A_\alpha$ and $A_\beta$ are absorbance at 766 $cm^{-1}$ and 840 $cm^{-1}$ respectively.

$K_\alpha = 6.1\ x\ 10^4$ and $K_\beta = 7.7\ x\ 10^4$ are absorption coefficient at 766 $cm^{-1}$ and 840 $cm^{-1}$ respectively measured in previous research [171]. In this work, it is assumed that the crystallinity of PVDF is not changed significantly during annealing [172], the relative content of β-phase will be used to indicate the effect of annealing.

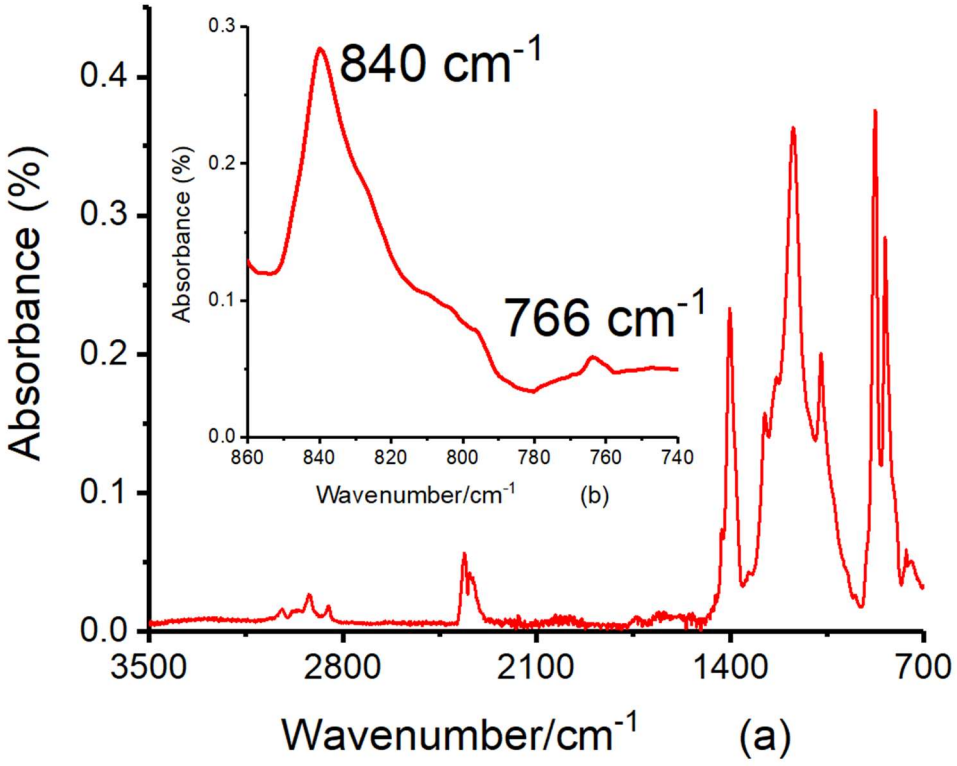



Figure 4.7. FTIR Spectrum of PVDF annealed under 60 °C for 6h

From initial annealing at 60 ºC for 1 h, it is noticeable that PVDF film from 10wt% solution exhibits a higher content of β-phase (73 %) than PVDF film from 15wt% solution (60 %), which is probably due to the lower viscosity in 10wt% solution, which is helpful for formation of the polar phase. Therefore, only the PVDF film produced from 10wt% solution was subject to further annealing tests to optimize the β-phase formation. After a series of annealing treatments, high temperature annealing was found not to be helpful to promote more β-crystals, and in contrast, samples annealed under high temperature and long annealing time exhibit a higher content of α-crystals (Figure 4.8). When PVDF thin film is created by spin-coating, molecular chains are arranged in the crystal phase in a short time, and there is some solvent remaining in materials. Although the crystallinity was initially assumed to be unchanged during annealing, secondary crystallization might occur from the remaining amorphous phase due to presence of residual solvent and the elevated temperature during annealing. In figure 4.7, there is a small increment in relative content of β-phase under 60 ºC and 90 ºC initially. This is possibly caused by the formation of β-phase during secondary crystallization, but the increment is relatively small and cannot be kept with increasing annealing time. With increasing annealing temperature and time, most polymer chains prefer transforming to α-crystal due to high thermodynamic stability, discussed in literature review. Consequently, the relative content of β-phase decreases with increasing annealing temperature and time. Therefore, for optimal β-phase spin-coated PVDF should be annealed at 60 ºC for 1h before polarization treatment.

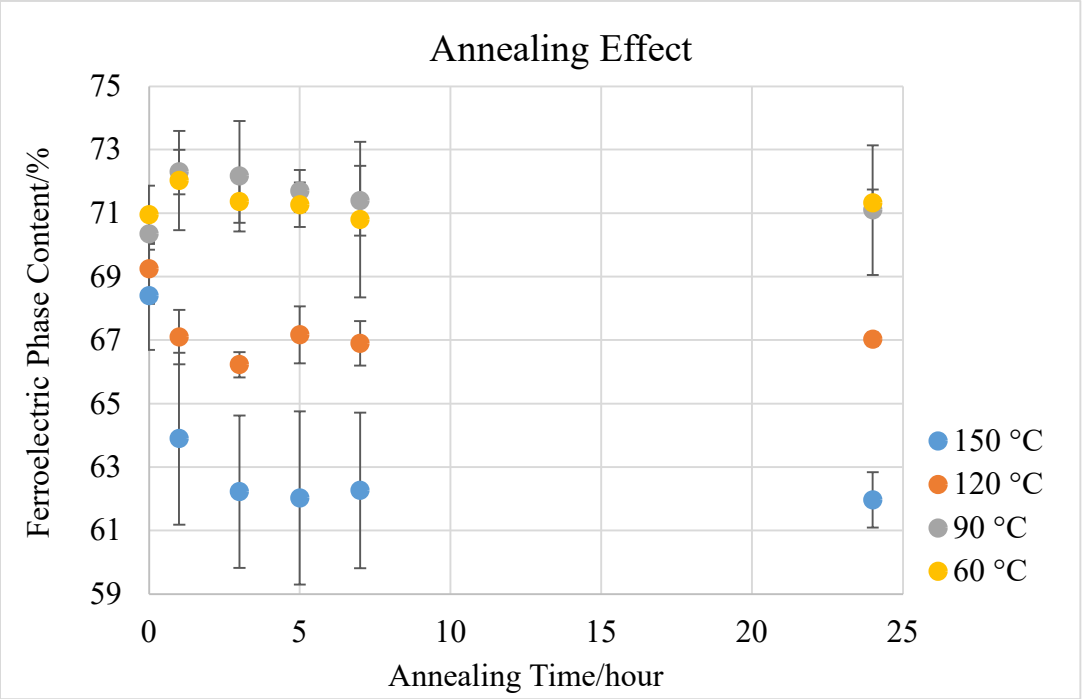



Figure 4.8. Variance of β-Phase against annealing time at different annealing temperature

### 4.3.2 Polarization of PVDF Thin Film

After obtaining the routine to harvest β-phase in PVDF thin film, samples are treated under Corona charging treatment. To obtain a stronger ferroelectric effect, a shorter distance between the tip and samples is preferable, however, samples are damaged when the distance is less than 10 cm, shown in figure 4.9. In order to avoid damaging the sample, only the electric field generated by 20 kV with distance of 15 cm between sample and tip is used to polarize FGOTFT sensor, shown in figure 4.10.

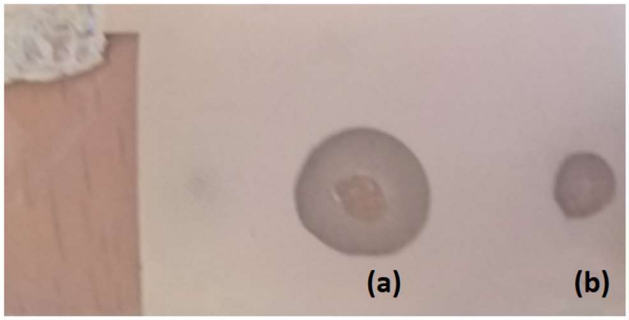



Figure 4.9. Damaged sample under Corona Charging Treatment (a) 20 kV and 5 cm (b) 20 kV and 10 cm

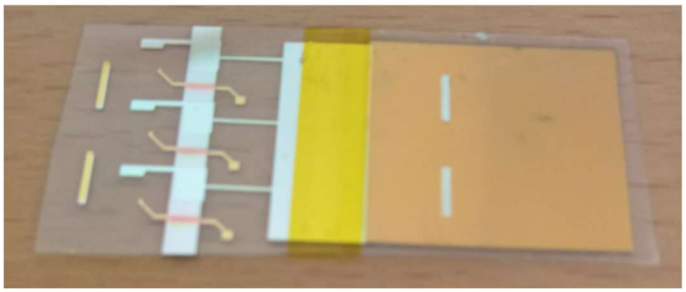


Figure 4.10. PVDF integrated OTFT sensor (The left side is connected to the probe pins and the right side covered by PVDF which is polarised under electric field of 20 kV and 15 cm)

### 4.3.3 Demonstration of Sensory Response to Buckling Strain

The initial sensory response was demonstrated by manually bending the PVDF coated area, with the results shown in figure 4.11. There are four different protrusions induced in the drain current – time curves which correspond to each time the bending strain was applied. However, there are two problems associated with this response curve; firstly, the sensory response is smaller than the initial decay when device is switched on, i.e. the current decay caused by bias stress, and secondly, the manual strain is not accurately controlled. In order to solve these problems, the bias voltage should be

reduced and the continuous bias scheme replaced with short pulsed bias, furthermore, a strain controlling device needed to be built.

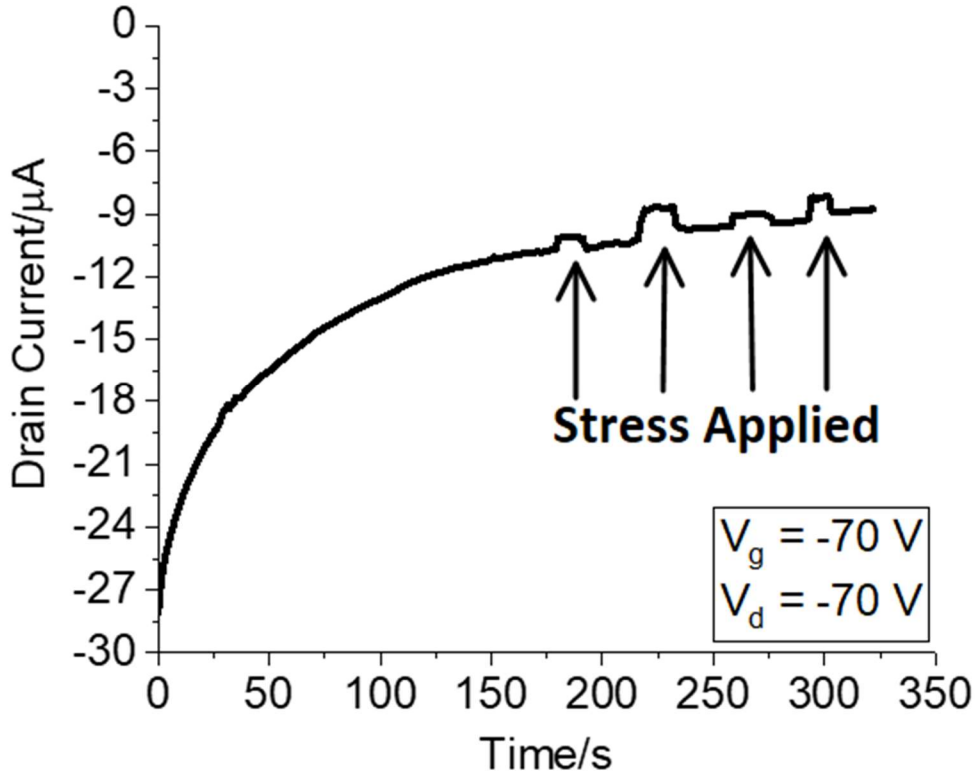



Figure 4.11. Sensory response of PVDF coupled OTFT sensor

To reduce the error from current decay, the bias voltage, bias time, and recovery time needs to be balanced to obtain accurate measurement of strain. The results of short time bias (without strain applied) have been collected and the measured drain current data is scaled into a range from zero to one respectively based on the minimum and maximum value of each curve, and plotted against time, shown in figure 4.12, and the current decay percentage can be directly visualized.

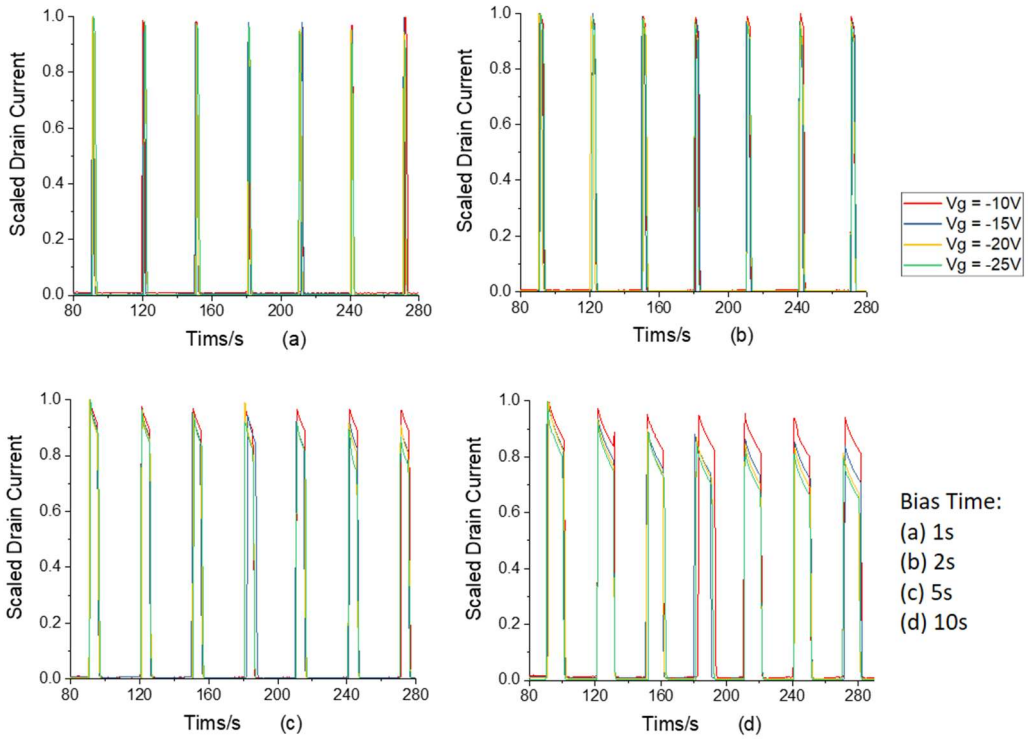



Figure 4.12. Scaled Drain Current against Time

When the bias time is relatively short, the current decay is comparable between the low voltage biased device and the high voltage biased device. To clearly demonstrate this decaying effect, peak values of drain current when device is switched on have been read out and plotted against time in figure 4.11. For devices biased for only 1s, it can be indicated that normalized drain current when device is switched on exhibits variance from 0.9 to 1, for test under 2s bias, 10V-biased device exhibits the small variance because small current decay is superimposed with random error, but high voltage (-20V and -25V) biased device exhibits a larger decay. Furthermore, with increasing the bias time, only the lowest 10V-biased device can exhibit a small current decay. To visualize the relationship, drain current, for different bias voltage is plotted under different bias time. The data are grouped by the bias voltage, shown in figure 4.13.

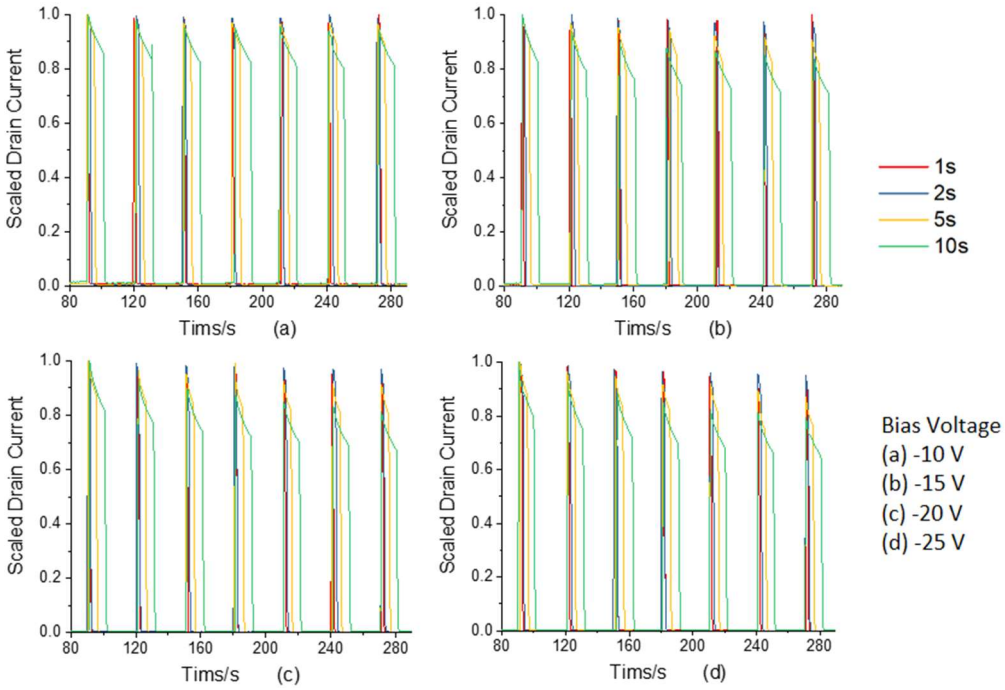



Figure 4.13. Scaled Drain Current against Time under constant voltage

To analyse the comprehensive effect of bias voltage and time, a series of heat maps are plotted in figure 4.14. It can be noticed that at the bottom-right region, i.e., low bias voltage and short bias time, the relative signal strength compared with maximum level (strength of first bias) is still maintained even after seven bias pulses. In contrast, in upper-left region, i.e., high bias voltage and longer bias time, the current signal decays to a lower level as more bias applied. In the buckling strain measurement, the bias condition should be kept in the bottom-right region.

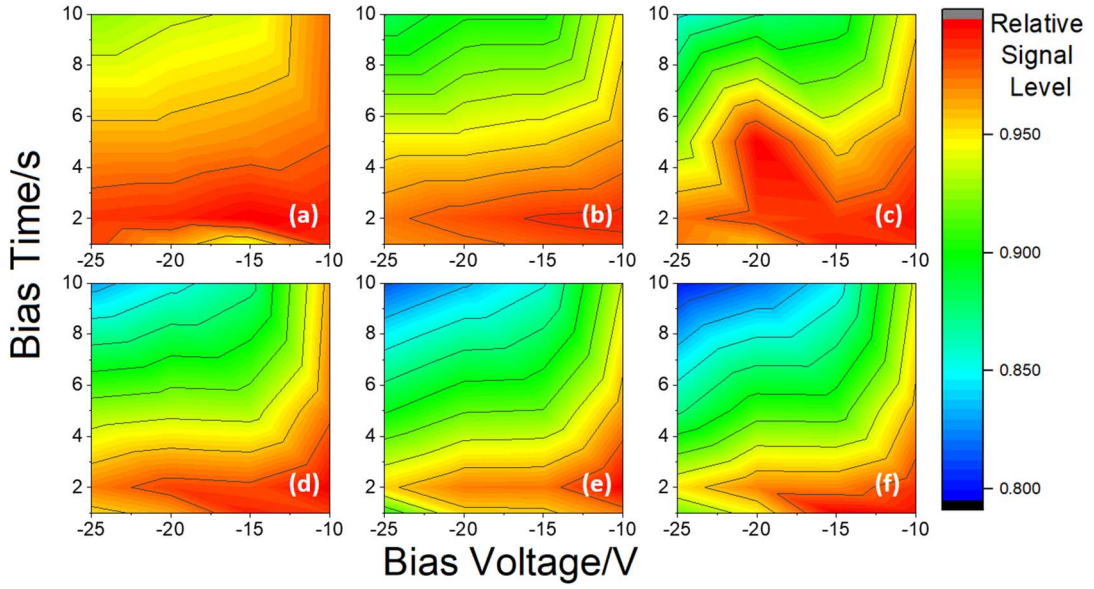



Figure 4.14. Heat Map of Decay Percentage during discrete bias at (a) 120s – Second Bias, (b) 150s – Third Bias, (c) 180s – Fourth Bias, (d) 210s – Fifth Bias, (e) 240s – Sixth Bias, and (f) 270s – Seventh Bias

The model to measure buckling bending strain with displacement of a free end is illustrated in figure 4.15 [173], which assumes that the substrate is much thicker than thin film on the top surface and therefore the strain of thin film is approximately equal to the geometrical strain. By this model, the measurement of strain will be easier, and it is convenient way to establish the relationship between strain and output signal.

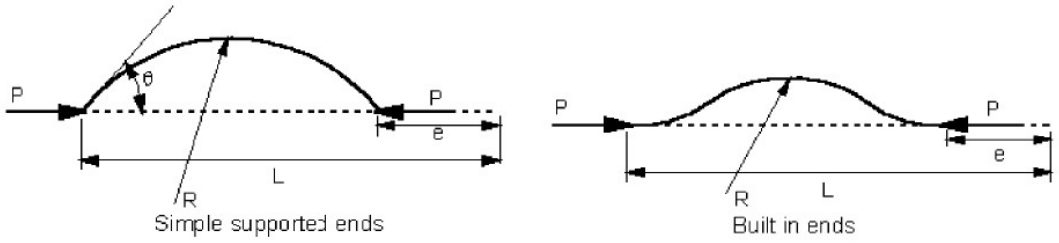



Figure 4.15. Buckling Strain Model that estimating strain level by measuring the displacement of free end in (a) Simple Support scheme and (b) Built-in scheme

$$\varepsilon = \frac{t_{substrate} + t_{film}}{2R} \dots\dots\dots (4.3)$$

In equation (4.3), $t_{substrate}$ and $t_{film}$ are the thickness of the substrate and thin film sample respectively, and $R$ is radius of curvature, which can be numerically calculated by the equation (4.4), (4.5) and (4.6),

$$\lambda = \frac{e}{L} \dots\dots\dots (4.4)$$

$$\lambda = 2\left[1 - \frac{E(k)}{K(k)}\right] \dots\dots\dots (4.5)$$

$$\frac{l}{R} = 4K(k)k \dots\dots\dots (4.6)$$

where $L$ is total length of substrate,

$e$ is the displacement of free end,

$\lambda$ is contract ratio,

$E(k)$ and $K(k)$ are elliptic integral

$l$ is the equivalent length, $l = L$ for simple support end and $l = 0.5 * L$ for built-in end Connecting equation (3) and (4), $k$ can be calculated numerically with Matlab built-in function (code in appendix), after that, the radius of curvature ($R$) can be calculated. By substituting the geometrical parameters ($L = 20\,mm$, $t_{total} = 0.5\,mm$ and $t_{film} \approx 1\,\mu m$) of the PVDF thin film sample into the equation above, the relationship between displacement and strain level can be obtained, shown in figure 4.16 below, it is noticeable there exists a linear relationship ($R^2 = 0.9999$) between displacement of the free end and the calculated buckling strain when displacement is

relatively small ($\leq 5\,mm$). With further increasing displacement, the strain level increases and deviates from the linear relationship. Therefore, the actual buckling strain can be approximately calculated by measuring displacement of free end when it is sufficiently small. For all experiments reported here, the strain was kept below 0.05.

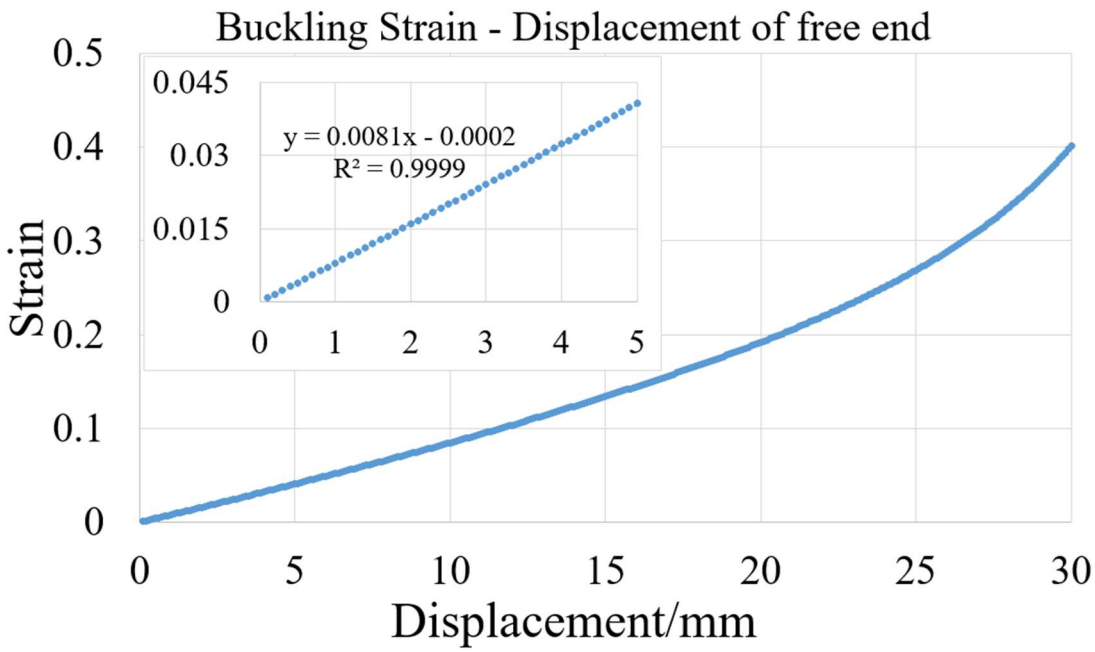
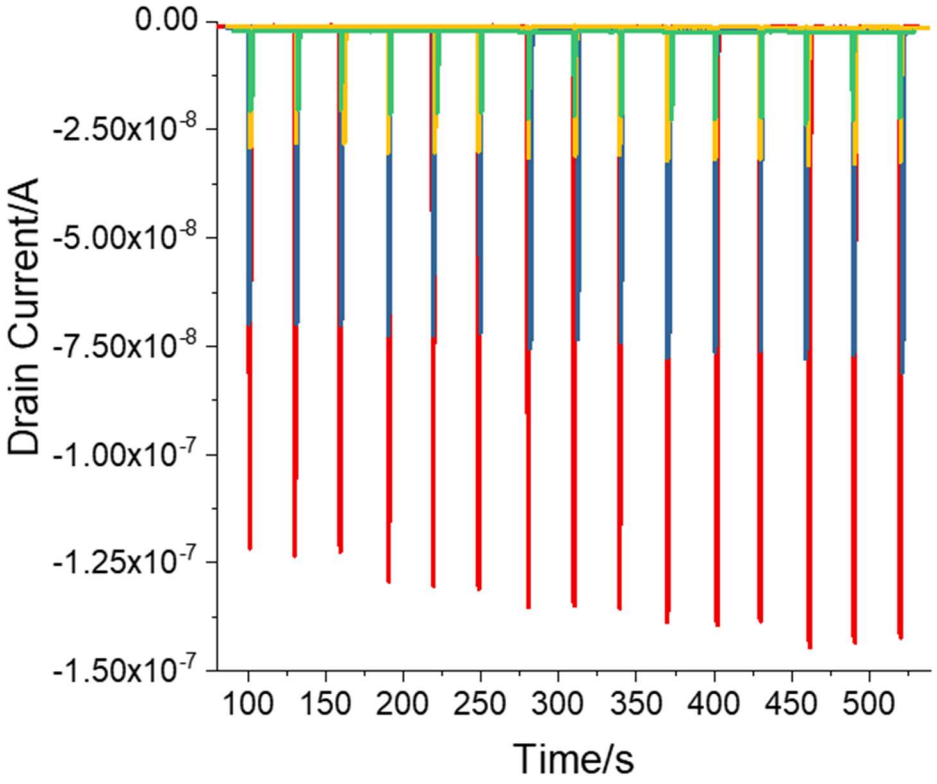



Figure 4.16. Linear relationship between buckling strain and displacement free end and it gets worse with increasing displacement

With the short time bias experiments in the previous section, a scheme of 1s bias and 30s recovery and four bias voltages, -10V, -15V, -20V, and -25V are used to switch transistors on to extract signal.

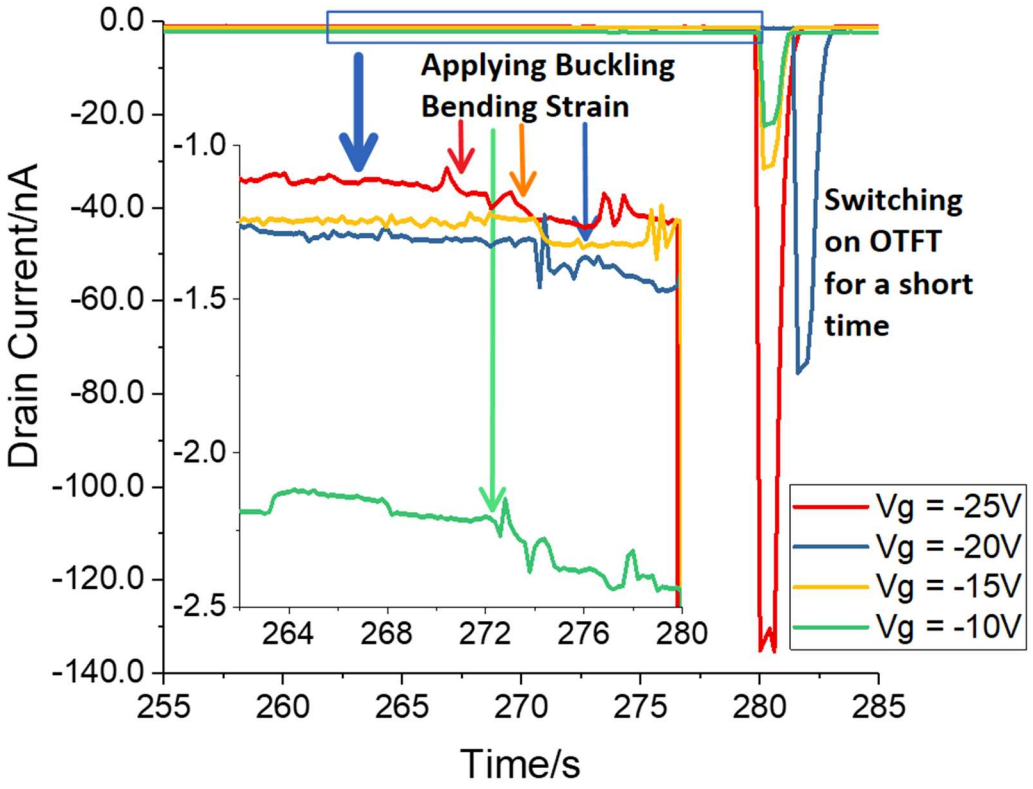
Initially, the device was turned on repeatedly to record the current without the effect of strain change on the floating gate. Then, stepwise the free end of the substrate was moved to increase the strain on the PVDF to change the voltage on the floating gate. At each strain level, the device is turned on three times to record the current level under each specific strain level. Finally, the average change of drain current, i.e., turn-on

current minus initial current level, for each strain level is calculated and plotted against strain level, shown in figure 4.17 (a).




| Strain Level | | | | | |
|---|---|---|---|---|---|
| -25 V | 0 | 0.68% | 1.4% | 2.2% | 3.3% |
| -20 V | 0 | 0.69% | 1.5% | 2.4% | 3.3% |
| -15 V | 0 | 0.66% | 1.3% | 2.2% | 3.1% |
| -10 V | 0 | 0.66% | 1.6% | 2.5% | 3.6% |

(a)




(b)

Figure 4.17. (a) Sensory Response under four different Bias Voltages (b) Drain current variance under strain level of 1.5 % approximately (the inner figure is the current variance without bias voltage on control gate and the signal is very small)

To measure the change in potential on the floating gate, the variance of drain current before and after applying the strain is used as a signal. When the transistors are off, the current change caused by the extra charge generated on the floating gate is very small, nearly close to baseline, shown in figure 4.17 (b) because the device is working in the region where gate voltage is close to zero, and output drain current is in the noise level ($10^{-10}$ $A$). It is difficult to distinguish signal from the baseline. After switching on the device, the FGOTFT is shifted to the region where a small variance on the floating gate can linearly induce a change on output drain current. When strain level is about 1.5%, the signals are 1.4 $nA$, 2.5 $nA$, 3.9 $nA$, and 12.8 $nA$ for FGOTFT biased under

-10V, -15V, -20V and -25V respectively, i.e. the signal is amplified to a recognizable level.

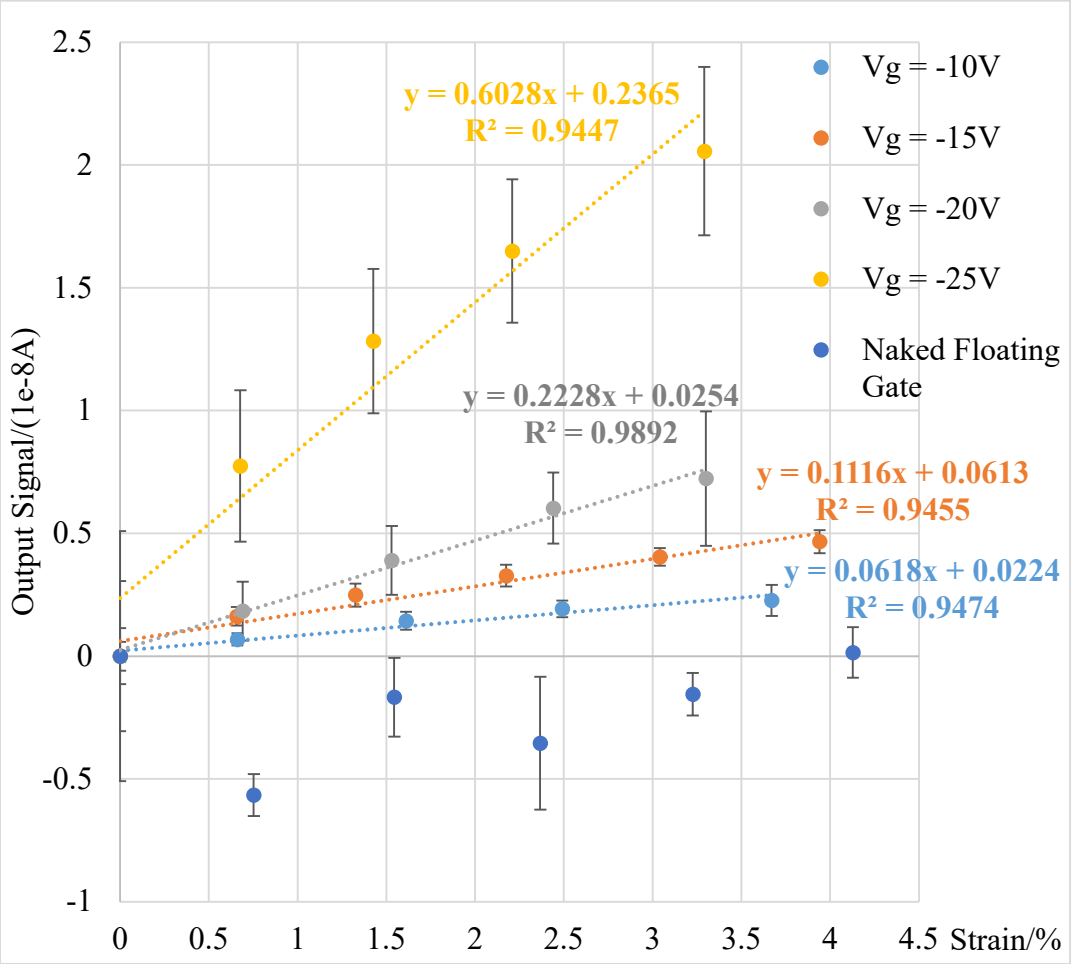



Figure 4.18. Calibration of strain sensor under different bias condition

After extracting the sensory response from the FGOTFT, a relationship between output signal and strain can be plotted. Shown in figure 4.18, the slope of the fitted line increases with increasing bias voltage, i.e., the amplification effect is improved, and sensitivity is improved. As a control, a naked floating gate is bent and the response from the FGOTFT is collected. For all voltages, the current is low and shows no trend, suggesting that it is scatter in the experiment. However, higher bias voltage induces more bias stress effect, and the range of error bar increases with improving bias voltage.

As discussed in the previous chapter, bias stress is an intrinsic property of OTFT, and charger carriers are trapped when transistors are switched on. A shorter bias time is helpful because of less charge trapping, therefore, a fast or high frequency bias, for example, in 1 MHz level, might be useful to reduce error from bias stress significantly.

## 4.4 Summary

In this chapter, a process of making thin film PVDF with a relatively high content of ferroelectric phase is developed by spin coating. When this PVDF sensor is combined with an OTFT, it is possible to read out the signal of strain from the continuous current – time curves under a relatively high bias voltage. However, the bias stress effect induces a current decay under high bias voltage or long-time bias.

To reduce the effect of bias stress, the current drifting and recovery conditions were investigated to develop suitable bias voltage and bias time. Afterwards, a testing method of multiple short-time bias is applied to extract the signal of strain change. In the buckling test, a linear relationship is extracted between buckling strain the actual change of drain current. The signal is still too low to read or transmit with commercial devices, and high signal output is often associated with strong effect of bias stress. To obtain a sensitive and accurate sensory response, a trade-off of bias voltage and bias time is needed.

The amplification of single transistor is limited and increasing bias voltage will increase the risk of dielectric materials breakdown. To have greater amplifying effect, an integrated circuit based on OTFTs might be an option for small signal processing, and this is investigated in the next chapter.

# Chapter V

## 5.1 Introduction

In the field of flexible and wearable electronics, there are two main streams. One route is to reduce the size of a Si-based chip capable of achieving signal collection, processing and transmission, to make it fit on the curved surface, although the mechanical rigidity will still limit the wearable properties [174-176]. An alternative approach, in contrast, is to use organic electronics which are much more flexible and have the promise to be manufactured in large area with high throughput [16, 17, 177].

In terms of signal processing capability, Si-based chips are well developed, but the OTFT-based signal processing circuit is less developed because of the instability of OTFT over time and the variation in properties of single transistors. As discussed in the literature review (section 2.5), single components, such as transistors, resistors, capacitors and inductors can be manufactured, exhibiting controllable properties, but the uncontrollable sample dependency of the components often leads to errors when complex circuits are fabricated. Therefore, simple circuit structure, such as single transistor or floating gate single transistor has been the main approach in the development of OTFT sensors. However, the signal amplification of a single OTFT is limited. As discussed in section 4.3.3, higher sensitivity can be obtained with higher bias voltage, but the bias stress is also more significant under high bias voltage, so the intrinsic error increases as well. To enable an accurate and sensitive signal processing capability, fabricating OTFT-based circuits becomes more worthwhile to achieve good signal processing [7, 8, 117, 118].

In this chapter, OTFTs with different geometrical properties are manufactured with methods suitable for a high-throughput roll-to-roll technique and then characterised by the methods described in section 3.2.3. With the help of high throughput techniques, it is possible to manufacture a large number of OTFTs in the same batch, i.e., there are sufficient transistors for selection in circuit fabrication. Next, transistors with similar performance are selected for fabrication of sub-circuits, such as current mirror and differential pairs. After validation of sub-circuit performance, the current mirror and differential pairs are used to build a transimpedance amplifier to convert nano-scale input current to a readable voltage output. There are two batches of transistors manufactured. The first batch is designed to include more single transistors on the same substrate to explore the solution to make transimpedance converter, and circuit is fabricated using the selected transistors. The second batch is designed with intensive layout; the positions and geometry of all transistors are fixed using the parameters of sub-circuits explored with first batch, i.e., to directly fabricate multiple transimpedance converters in same batch. Finally, the relationship between input and output signal is characterised and transimpedance converters are encapsulated with PDMS. As a comparison, devices are tested before and after encapsulation to explore the effect of encapsulation.

## 5.2 Experiments

### 5.2.1 Circuit layout and Design of Shadow Mask

The layout of the first batch of samples is designed in 6 areas, shown in figure 5.1. Transistors in areas I and II are used to fabricate current mirrors, transistors in areas III and IV are used as differential pairs because of their larger width, and transistors in

area V and VI work as pseudo-resistors to adjust the overall impedance of the circuit. Because of symmetry, the functions of area I, II, V and VI can be reversed based on the performance of the transistors. In terms of geometry, the width/length (W/L) ratio of transistors in area I, II, V and VI are $2.5mm/0.1mm$ and that in area III and IV are $25mm/0.1mm$. With the transistor layout in figure 5.1, the shadow mask pattern for evaporation were designed and fabricated, shown in figure 5.2. In this batch, each sample substrate includes 54 transistors in total, and each transistor on the substrate is characterised individually and then selected for fabrication of functional sub-circuits.

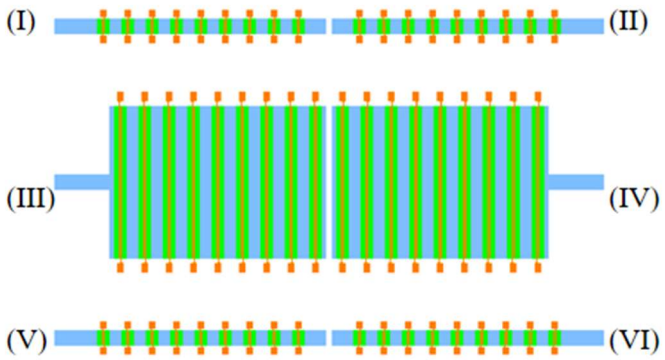



Figure 5.1. Transistor Layout of First Batch

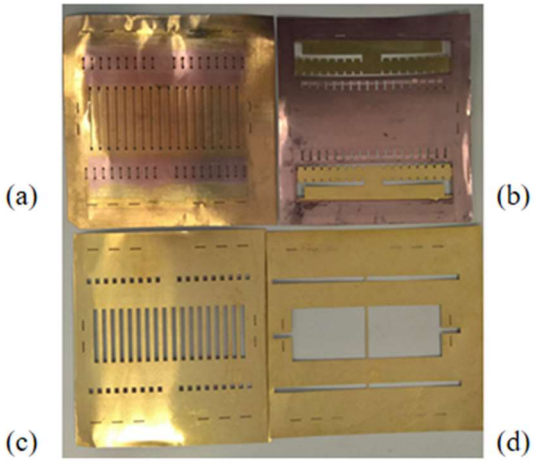



Figure 5.2. Shadow Mask for (a) Contact Electrode Source/Drain (b) Inter-connection (c) Semiconductor and (d) Gate Electrode

### 5.2.2 Manufacture of OTFT

Polyethylene naphthalate (PEN) substrates for OTFTs were pre-cleaned with isopropanol (IPA) and then cut to $10 * 10\, cm^2$. Gate materials (Cu or Al) are thermally evaporated through the shadow mask onto the plastic substrate and the TPGDA as dielectric materials is deposited on the gate electrode with Oxford Web-coater followed by a spin-coating of PS buffer material. Finally, the organic semiconductor, dinaphtho [2,3-b:2',3'-f] thieno[3,2-b]thiophene (DNTT) and gold top electrodes are deposited. The operating parameters are same as experiments in section 3.2.1.

After the OTFTs have been fabricated, all OTFTs were stored in a dark environment at 20 $^{o}$C and humidity of 5% – 10% for approximately for 96 hours for oxygen doping (Chapter III). Afterward, each transistor is characterised in turn using Keithley 2400 source meter, as described in section 3.2.3 to extract transfer and output characteristics.

### 5.2.3 Fabrication and Characterisation of Functional Sub-circuits

In the first batch, functional sub-circuits are fabricated using silver ink to make connections between transistors. The circuit diagram of the current mirror is shown in figure 5.3. A series of current mirrors are designed to explore the current duplicating effect, and the overall power consumption. An ideal current mirror is capable to exhibit a controllable current duplicating effect with lowest power consumption.

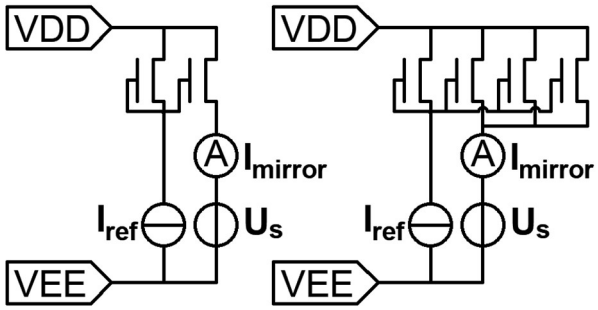



Figure 5.3. Simple CM (1:1) (left) and (1:3) (right)

Current mirrors are tested with fixed VDD (25 V) and VEE (0 V), voltage source ($U_s$) output a varied voltage from 25 V to –35 V under different output current ($I_s$), from $10^{-7}$ A to $10^{-6}$A with step of $10^{-7}$ A, and from $10^{-6}$ A to $10^{-5}$ A with step of $10^{-6}$ A. The measured current is plotted against input voltage. After that, the current transfer ratio ($I_o/I_r$) is calculated under different output voltages and plotted against $I_r$.

A differential pair is built following the current mirror, shown in figure 5.4. The current mirror (T1 and T2) works as a current source to provide constant current through T2 and current is adjusted by T1 and the pseudo-resistor (T7). T3 and T4 work as an amplifier pair to process the signal, meanwhile, T5 and T6 work as pseudo-resistor to adjust the impedance of the circuit.

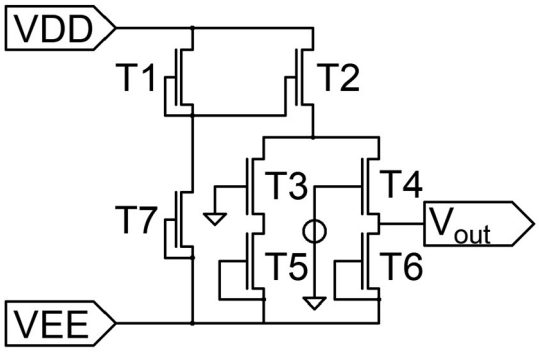



Figure 5.4. Circuit Diagram of Differential Pair (T3 and T4) constructed with 1:1 Simple Current Mirror (T1 and T2)

The differential pair is tested with three different current mirrors, 1:1, 1:2, and 1:8. The input voltage sweeps from 40 V to –40 V and the output voltage is plotted against input voltage with different VDD/VEE bias. The slope at 0 V and the slope maximum are extracted to demonstrate the amplifying effect.

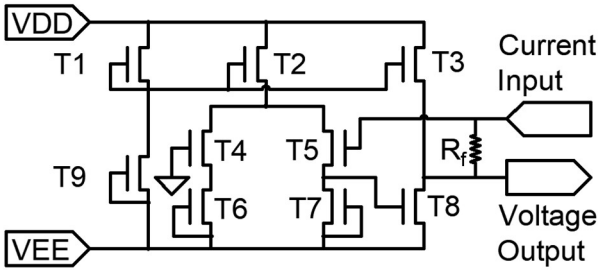



Figure 5.5. Circuit Diagram of Transimpedance Amplifier (Designed by Dr Ching-Mei Chen [178])

A transimpedance amplifier is directly built on the differential pair described above, shown in figure 5.5. An output stage is created following the differential pair and then a fixed-value resistor is constructed between the input end and output end of the circuit.

The transimpedance amplifier is placed in a shielding box and biased under condition of VDD = 5V and VEE = -5V, with input current sweeps from 0.1 μA to 3 μA by increments of 0.1 μA, while at same time, the output voltage is recorded by an oscilloscope. Afterward, a plot of output voltage against input current obtains the converting relationship.

### 5.2.4 Miniaturization and Encapsulation of OTFT-based Transimpedance Amplifier

After obtaining the key parameters of the transimpedance amplifier, it is important to optimize the size and performance because the I-to-V converters in the first batch that

were printed on a 10 x 10 $cm^2$ substrate is not easy-access for wearable applications. A new layout of the OTFT transimpedance amplifier was designed by author on an area of 3.7 x 2.3 $cm^2$, shown in figure 5.6 and manufactured with all-evaporation process through shadow mask following the sequence of Cu gate electrode, TPGDA dielectric insulator, PS buffer layer, DNTT semiconductor layer and Gold source/drain contact electrode. Afterward, the transistors on each sample are tested and the sample without any short-circuiting transistors is selected for interconnection. Finally, a thin layer of Cu is evaporated through a shadow mask to connect the transistors according to the circuit design as described in figure 5.6.

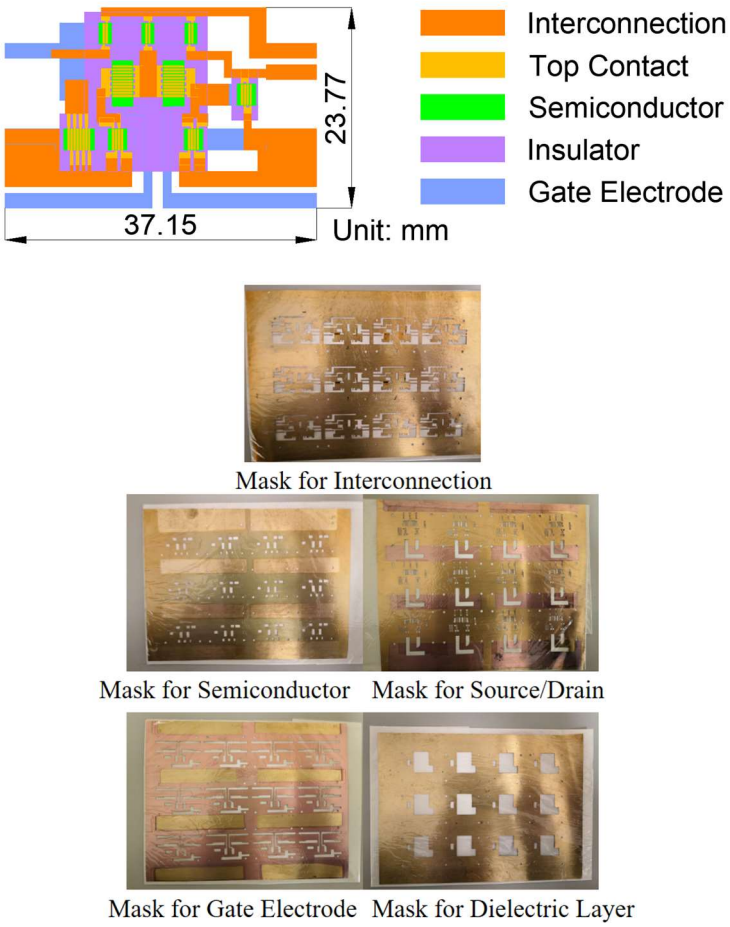



Figure 5.6. Pattern (Top) and Shadow Mask (Bottom) of Small-size OTFT Transimpedance Converter

In addition, a resistor with interdigitated structure is printed on PET. A pair of interdigitated electrodes with thickness of 30 nm is firstly evaporated via shadow mask, shown in figure 5.7, and then each pair of electrodes is tested to avoid any short-circuited devices.

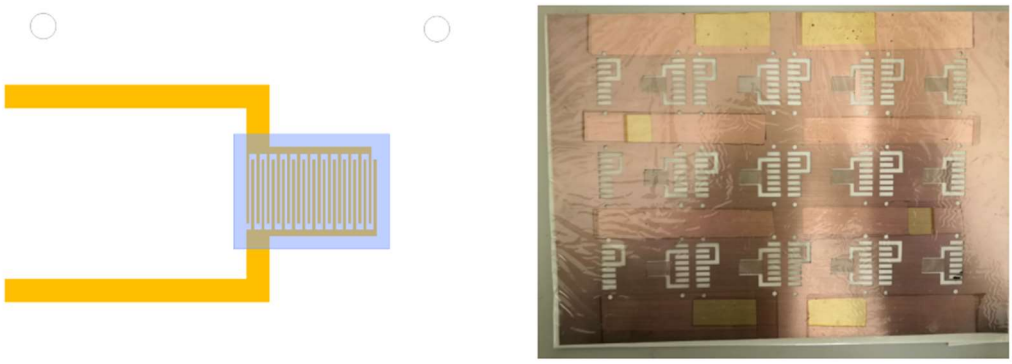


Figure 5.7. Thin Film Resistor based on interdigitated electrode

Next, a thin layer of Cu is evaporated on the interdigitated electrode, shown in figure 5.7. Adjusting the thickness of the Cu layer can control the resistance of this resistor. In this work, the thickness of the Cu layer was varied from 1 nm, 3 nm, 5 nm, 7 nm and 9 nm, monitored via QCM. Due to oxidation of Cu over time, the resistance is finally determined after aging for several days. Afterward, the resistance of the thin film resistor is tested with the Keithely 2400.

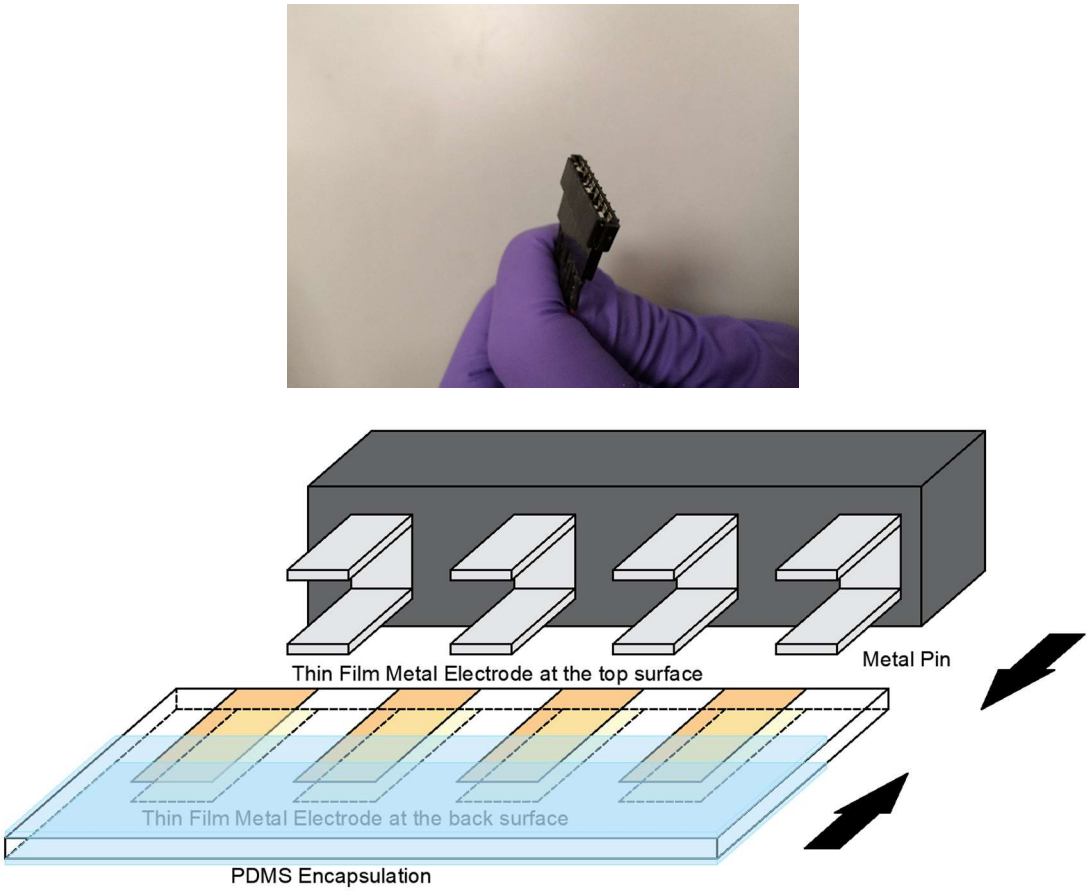



Figure 5.8. FFC/FPC Board Connector (Top) and Cross-Section of a PDMS Encapsulated OTFT Circuit at the Edge (Bottom)

Afterwards, silver paint is added on the edge of the electrode as a protective material to avoid the metal pin of the connector (FFC/FPC Board Connector) scratching the thin conductor. Finally, the FFC/FCP Board Connector, shown in figure 5.8, fixes the OTFT-TIA and thin film resistor.

Before encapsulation, OTFT-TIA and thin film resistor are fixed by matching the connection track of the resistor to the input and output trace of OTFT-TIA, and then parafilm is used to cover the edge of sample which is to contact with connector.

Encapsulation materials are prepared with 10 g of PDMS and 1 g of silicon elastomer curing agent (hardener), the mixture is manually stirred for 5 mins and then put into a

vacuum chamber for degassing for about 45 mins. After removing all bubbles inside the polymer mixture, it is poured into a mould and then the parafilm-protected sample is carefully placed into this solution for curing over 24 hs at 30 ºC. When the encapsulation materials are fully cured, a blade is used to gently remove the parafilm and the PDMS on that was over the parafilm to reveal the contact electrodes. Finally, the connectors on OTFT-TIA are installed and the sample is located into the shielded test box.

## 5.3 Results and Discussion:

### 5.3.1 Performance Evaluation of Functional Circuits

The function of the current mirror is to supply a constant current or to work as a current-regulating circuit. The current transfer ratio (M) is a key parameter to evaluate the performance of a current mirror. It is described by Equation (1), assuming that each transistor used to build current mirror exhibits same output,

$$\mathrm{M} = \frac{I_{output}}{I_{reference}} = \frac{(W/L)_{mirror}}{(W/L)_{reference}} \dots\dots (1)$$

where $W$ and $L$ are width and length of the conductive channel respectively. In this project, the geometrical property is designed to be the same for each transistor, thus, the current transfer ratio can be expressed as Equation (2),

$$\mathrm{M} = \frac{I_{outp}}{I_{reference}} = \frac{Number\ of\ Transistors\ on\ the\ Mirror\ Side}{Number\ of\ Transistors\ on\ the\ Reference\ Side} \dots\dots (2)$$

The number ratio of the simple current mirrors in this chapter are 1:1, 1:2, and 1:8. On the reference side, a constant current is supplied at each step and then voltage source

($U_s$) varies from 25 V to -35 V to alter the actual current passing through the mirror side. The $I_o - U_s$ relationship has been plotted in figure 5.9. As the source voltage varies from 25V to -35V, the output current initially increases and then gradually saturates.

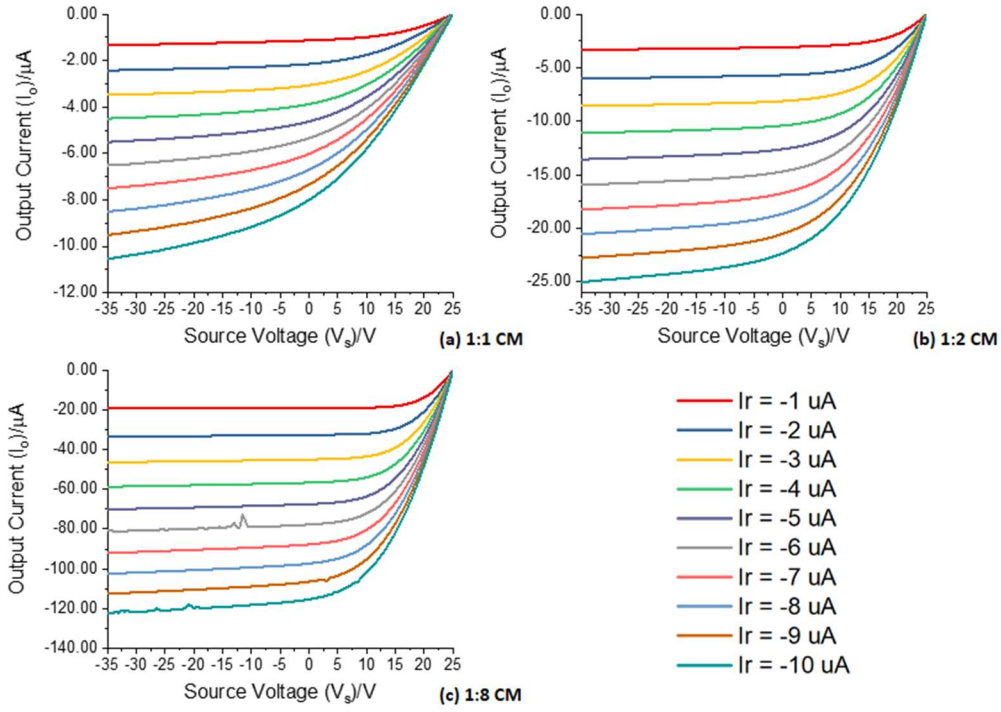



Figure 5.9. $I_o - U_s$ Curves for Simple Current Mirror with number ratio of (a) 1:1, (b) 1:2, and (c) 1:8

After obtaining the $I_o - U_s$ curves, reading out the output current under fixed voltage and compared it with the reference; the current transfer ratio can be calculated with equation (2). Plotting current transfer ratio against the reference current, we can obtain the variance of M as the reference current is varied, shown in figure 5.10.

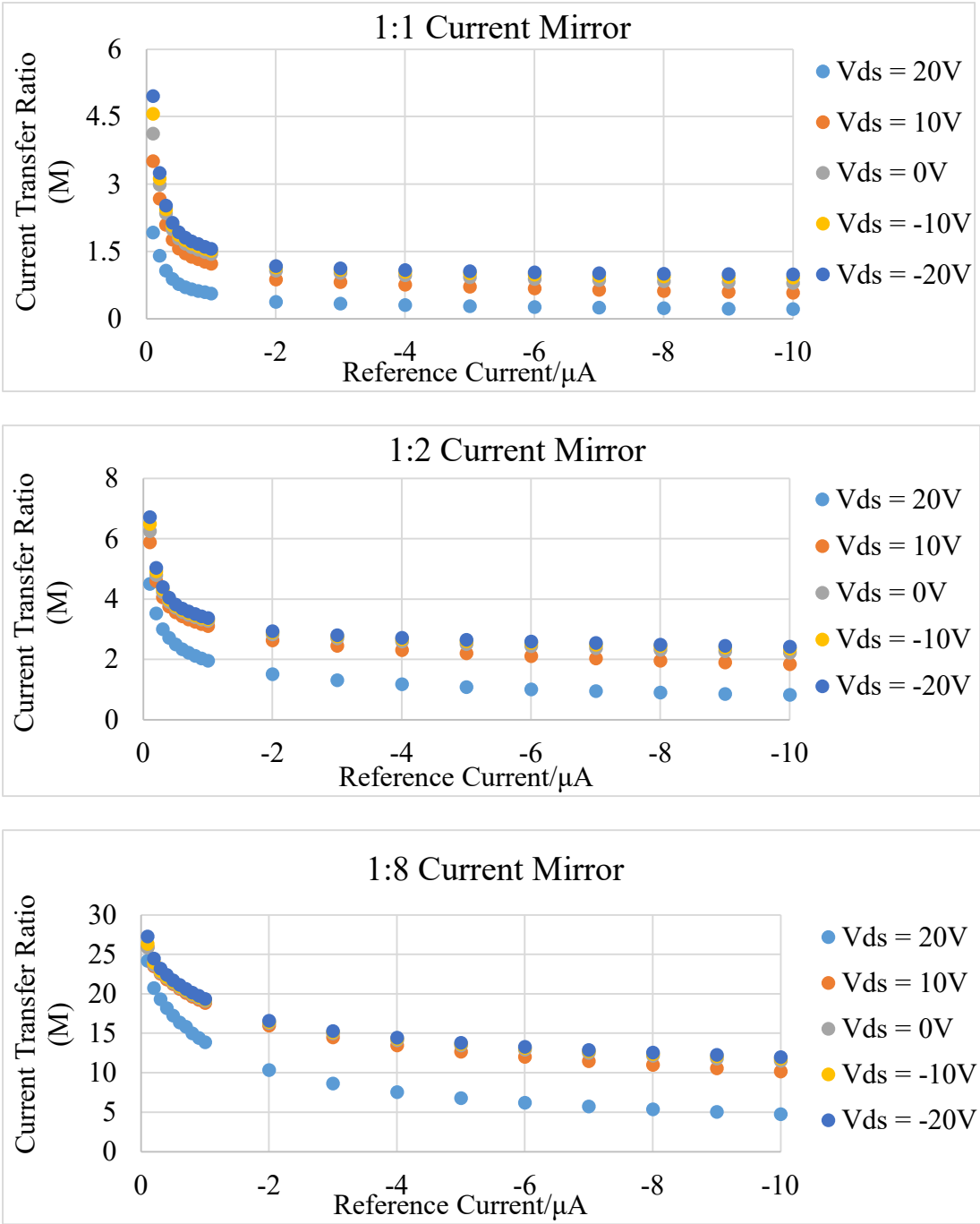



Figure 5.10. Current Transfer Ratio for simple current mirror and cascade current mirror

Current transfer ratio decreases with reference current varying from 0 to -10V and then gradually approaches a constant. Ideally, the current transfer ratio is expected to be equal to the number ratio described in equation (2); however, the conductivity variance

in transistors leads to a deviation of the measured current transfer ratio. In addition, current transfer ratio varies in a range as source voltage varies, and this range is dependent on the number of transistors on the mirror side. As shown in figure 5.10, 1:8 simple current mirror exhibits a wide variance of current transfer ratio, and its current transfer ratio is higher than the number ratio when it works in the saturation region (source voltage range from 0 to -20V). In contrast, the 1:1 and 1:2 current mirror exhibits a smaller variance in current transfer ratio, from 0.2 to 1.17 and from 0.8 to 2.95 respectively when the reference current varies between -2 μA and -10 μA.

Considering the current duplicating effect, the 1:8 current mirror is capable to supply a high current for the sub-circuit, for example, the differential pair, however, in terms of current transfer ratio, a small variance is favourable. The 1:1 current mirror and 1:2 current mirror, with smaller variance, are more able to be controlled and exhibit less error caused by mismatch of the transistors.

Next, a differential pair based on each of the preferred 1:1 and 1:2 current mirrors is built based on the circuit diagram in figure 5.4. The circuit layout is illustrated in figure 5.11. The transistors in areas III and IV are the key component to adjust the current in the circuit, followed by two pseudo-resistors.

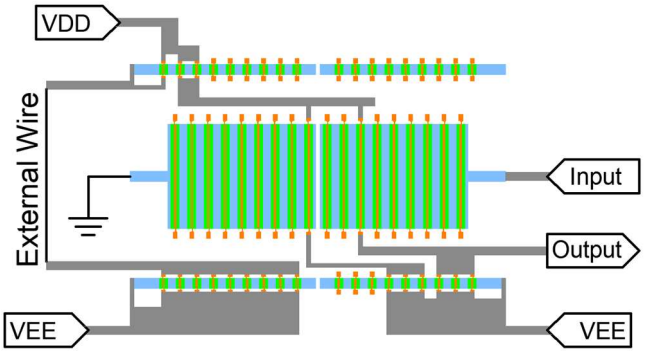



Figure 5.11. Differential Pair based on 1:2 Current Mirror

The results of a voltage sweep of the differential pair is shown in figure 5.12, and the characteristic slope is extracted in table 5.1 and figure 5.13.

The slope of the voltage output curve represents the amplifying effect**.** As VDD/VEE bias voltage varies from ±5 V to ±25 V, the slope of the amplification curve increase, and with more transistors built into the current mirror, the amplification range within which the slope experiences a significant variance, is slightly widened under the same bias voltage.

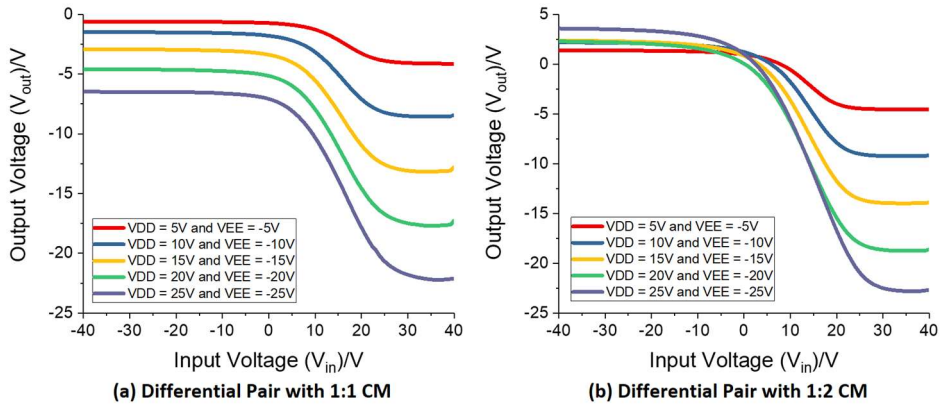



Figure 5.12. Voltage to Voltage Amplification from Differential Pair connected to different Current Mirrors

Ideally, the amplification curve is expected to be centrally symmetrical around the origin, i.e., output voltage is zero because transistors are off and circuit is open when input voltage is zero and exhibits a significant change when input voltage varies to positive or negative region and then gradually approaches a saturation platform, shown in figure 2.37. However, ohmic conductivity in the channel provides a path for current even when transistors are off, leading to a vertical shift in the curve. In table 5.1, an amplification effect (i.e., when the maximum slope is greater than 1) can be seen in the differential pair built with 1:2 current mirror when VDD/VEE is greater than 20V.

However, the results in figure 5.12 shows that the slope is relatively small when the input voltage swings around the origin, and the maximum amplification effect is exhibited when input voltage is approximately 15V. A positive voltage bias is needed to obtain a higher amplification effect and reducing the threshold voltage might be helpful to reduce the horizontal shift of the curve. Therefore, the differential pair is not good for direct use as signal amplifier because the sensor signal is usually varying less than 1V and the bias voltage (VDD/VEE) is too high (±20) to be acceptable for biomedical application.

Table 5.1. Slope of voltage output under different VDD/VEE voltage

| | Bias (VDD/VEE Voltage) | Absolute Slope at zero Input | Max Absolute Slope | Input Voltage at Max Slope |
|---|---|---|---|---|
| Differential Pair Based on 1:1 Current Mirror | ±5 | 0.02 | 0.23 | 15.2 V |
| | ±10 | 0.05 | 0.44 | 16.0 V |
| | ±15 | 0.07 | 0.59 | 16.0 V |
| | ±20 | 0.09 | 0.72 | 15.2 V |
| | ±25 | 0.11 | 0.82 | 16.0 V |
| Differential Pair Based on 1:2 Current Mirror | ±5 | 0.06 | 0.40 | 13.61 V |
| | ±10 | 0.13 | 0.69 | 14.41 V |
| | ±15 | 0.20 | 0.88 | 14.41 V |
| | ±20 | 0.28 | 1.02 | 14.41 V |
| | ±25 | 0.34 | 1.16 | 16.0 V |

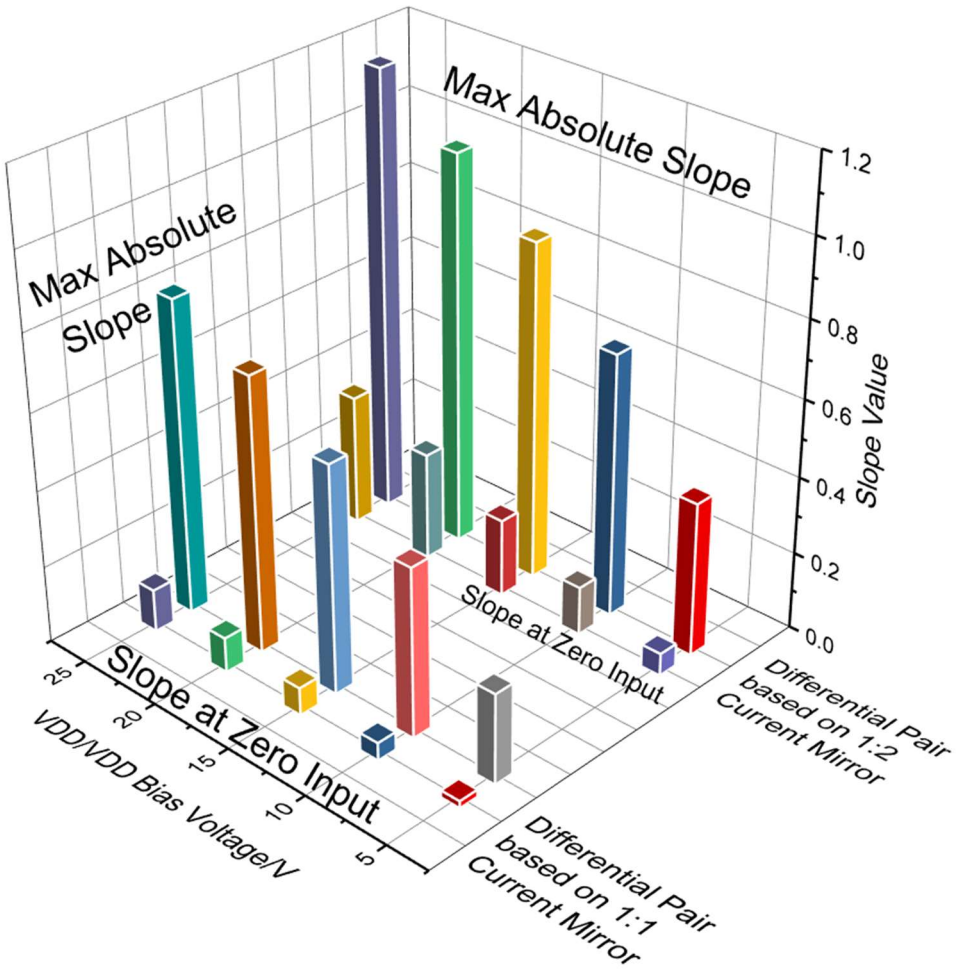



Figure 5.13. Comparison of Amplification Effect of Differential Pair

Although the differential pair cannot be directly used to amplify a sensor signal, it can be used to build a transimpedance amplifier, which converts an input current signal to a voltage signal as output. The circuit layout of the first transimpedance converter is shown in figure 5.14. Based on the differential pair, an output stage, which includes two transistors from Area I and three transistors from Area II is added following the differential pair because the output stage is helpful to reduce the impedance mismatch. Theoretically, the gain of a transimpedance amplifier is the ratio of output signal level over input signal level, and it is supposed to have similar value to the feedback resistor in this case.

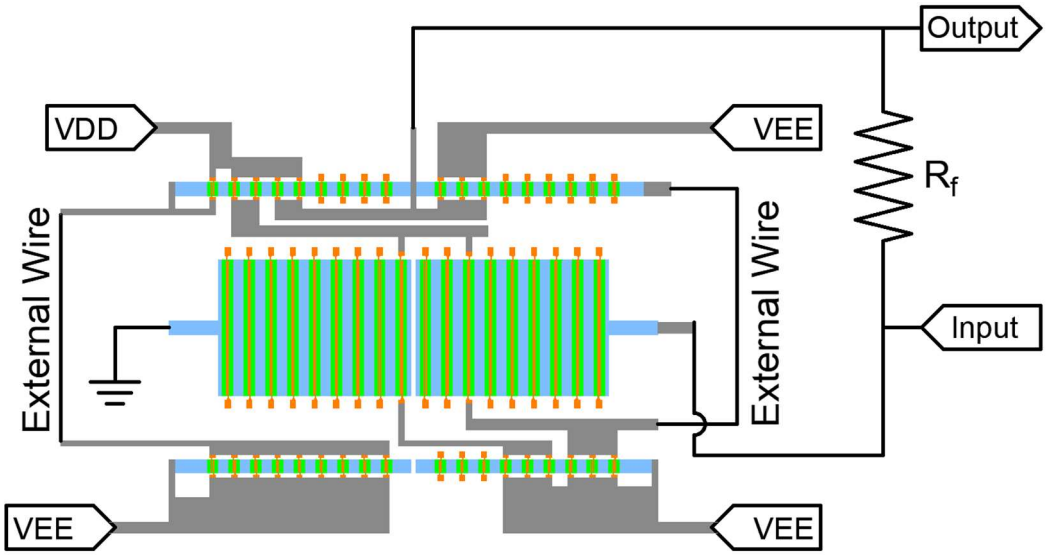



Figure 5.14. Circuit Layout of Transimpedance Amplifier

After the testing under VDD/VEE of ±5V, a relatively linear relationship can be obtained when the input current is positive, shown in figure 5.15. It enables the conversion of nano-scale current to a readable voltage output. However, there is still a voltage offset when the input current is zero. Because the current in the circuit is not absolute zero even when the transistors are off, the current under off-condition causes a potential drop from VDD to VEE. The gain, calculated from the linear fit, is approximately 820k, which is higher than the value of the feedback resistor in this circuit (620 kΩ). In order to solve the mismatch problem, more optimizations are needed in terms of geometrical structure of each transistor, impedance variance of transistors and circuit layouts from the perspective of electronic technology. Due to lack of available software to support simulation of OTFT-based circuit, more efforts should be made in the development of OTFT-based simulation tool and optimization algorithm of OTFT system in future.

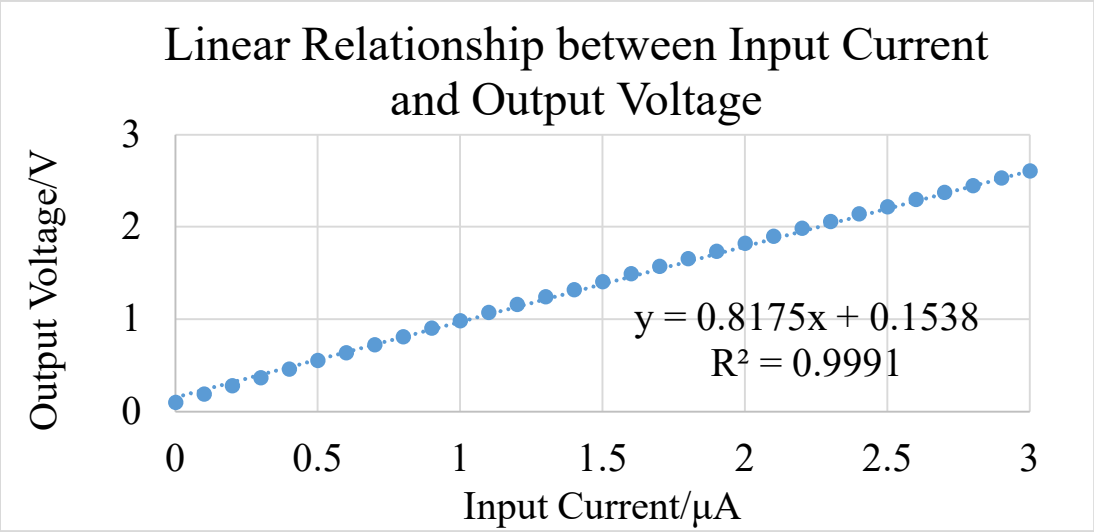



Figure 5.15. Linear conversion from I to V

### 5.3.2 Characterisation of Miniaturized OTFT-based Signal Conditioning Circuits

In the first batch, the usage rate of transistors is very low, i.e., only a few of the transistors are used to fabricate the circuit, and the layout needs to be optimized after obtaining the number of transistors for current mirror, differential pair, and output stage. Hence, the layout of second batch is more compact, shown in figure 5.6, and it is capable to produce 12 transimpedance converters at the same time. Each single transistor is characterised before interconnection, and a sample without any short circuits is selected for the final signal conditioning circuit.

Compared with first batch, long-channel transistors are designed with an interdigitated structure to save more space on the substrate, and these are found to exhibit lower current leakage from source to drain when transistor is off compared to the long channel structure of the first batch, shown in figure 5.16.

On the shadow mask with long channel, the long strip feature is constrained at both ends, and the mask tends to buckle when it is heated during evaporation. However,

with the interdigitated structure, each short strip of the mask is constrained at only one end, i.e., there is more space for expansion when it is heated, and the mask does not tend to buckle. Thus, the interdigitated mask is less likely to deform to move away from the sample under high temperature, whereas the mask in first batch is more susceptible to bending under high temperature. When the shadow effect occurs with a deformed mask, the actual distance between source and drain electrode is shortened, and hence the resistance in the channel becomes less, in the worst case, leading to short circuit issue. The shadow effect of interdigitated structure is less than the long-strip structure and off-current of the former is much lower.

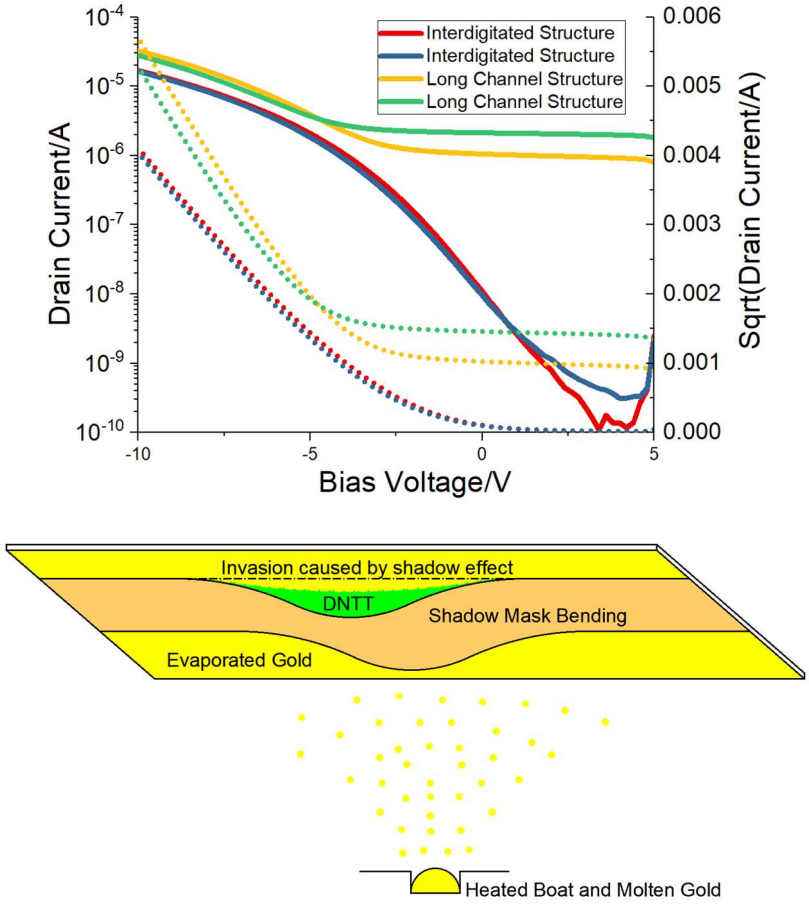



Figure 5.16 Transfer Curve Comparison of Long Strip and Interdigitated Structure (Top) and Shadow Effect caused by Mask Bending (Bottom)

The thin film resistor exhibits a thickness-dependent resistance, shown in figure 5.17. The resistance is extremely high, i.e., it exceeds the effective range of the resistance meter when thickness is less than 2 nm, and it starts to decrease rapidly with thicker metal layer, so the resistance can be controlled to a specific value. After making a series of thin film resistors, a resistor that exhibits a resistance value about 620 kΩ (close to the resistor in used in figure 5.14) is selected to integrate with OTFT signal conditioning circuit.

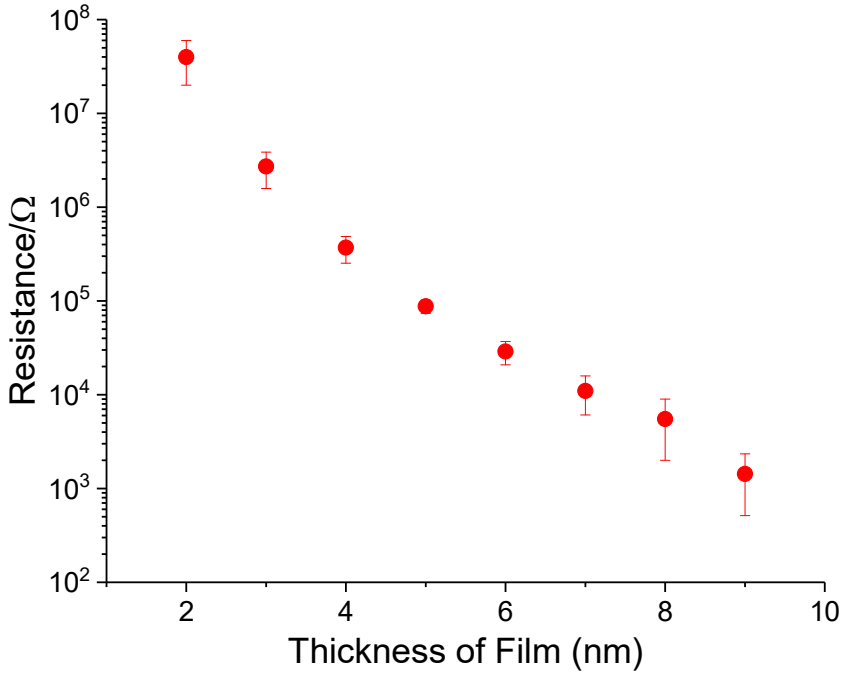



Figure 5.17. Relationship between Resistance and Film Thickness on the Interdigitated Electrode (The error bar shows batch-to-batch variance)

An image of the transimpedance converter is shown in figure 5.18. The linear conversion of the small size transimpedance converter is characterised with the same method described above, and the linear traces before and after encapsulation are shown in figure 5.19. The encapsulated device exhibits a slightly higher gain and lower offset

voltage due to the presence of encapsulation, but the linearity is not changed significantly.

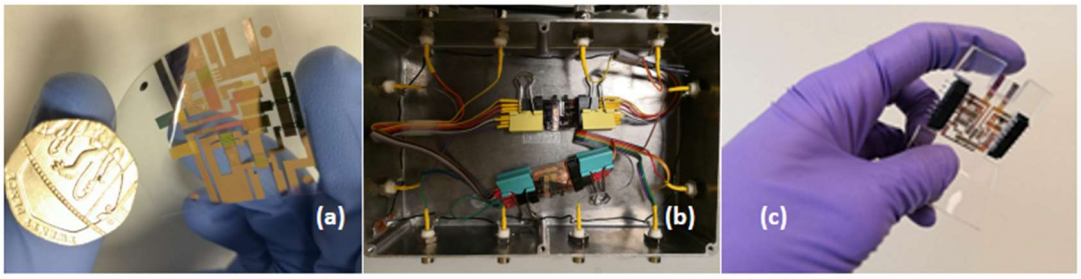



Figure 5.18. Transimpedance Converter (a) Sample Made from Evaporator, (b) Testing in Shielding Box and (c) Encapsulated by PDMS

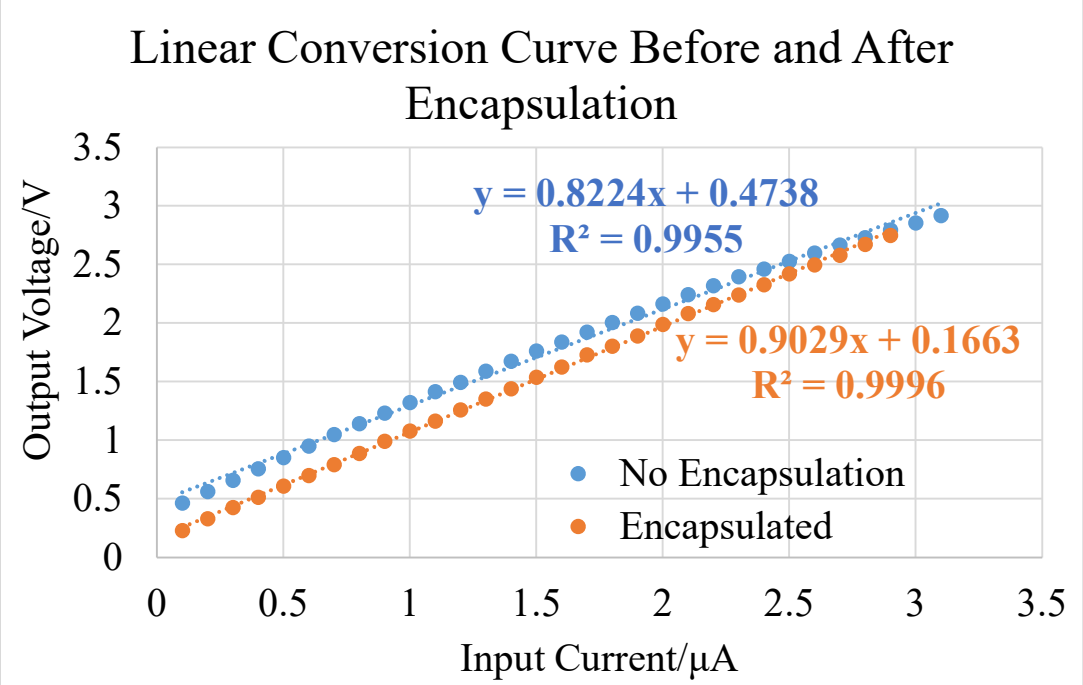



Figure 5.19. Linear Conversion Relationship before and after Encapsulation

## 5.4 Summary

In this chapter, it is demonstrated that flexible OTFT-based functional sub-circuits can be manufactured by an all-vacuum process with Oxford Web-coater and Edwards 306.

After characterisation of the functional sub-circuits, a transimpedance amplifier was created with the functional circuits to realize a linear conversion from a nano-scale current input signal to an output signal of several volts. Next, the geometrical properties and layout of transistors for fabrication of functional sub-circuits were optimized to reduce the overall size of a single transimpedance converter to print more devices in a limited area. It is possible to manufacture 12 transimpedance converters at the same time in the small Edwards Evaporator. In addition, a series of thin film resistors were manufactured via evaporation and the resistance can be controlled within a limited range by adjusting thickness of metal deposited between interdigitated electrodes. After integration and encapsulation, a flexible transimpedance converter can be obtained with a linear converting capability to process nano-scale current input to a readable voltage output of several volts. In the next chapter, this signal conditioning circuit will be used to process sensing signal.

# Chapter VI

## 6.1 Introduction

In a broad definition, sensors are a sub-system to convert physical change in their environment to a signal that can be recognized by human or machine, such as a colour change or a change in electric current. Generally, fabrication of a sensing system is associated with a signal detector, transducer, processor and visualizer. As discussed in the literature review (section 2.3), a conventional OTFT-based sensor directly uses the sensitivity of semiconductor to detect concentration of analytes, i.e., the signal detector and processor are formed from same OTFT, but the instability of organic semiconductor limits the sensing application [65, 179, 180]. To enable versatile sensing application with OTFT, a sensing system is needed on a flexible substrate, i.e., signal detector and OTFT-based signal processor can be manufactured separately to prevent OTFT damage in the analyte environment.

In Chapter IV (section 4.3.3), a PVDF-coupled FGOTFT was shown to detect strain change on a thin film, and this will be developed to an arterial pulse sensor in this chapter with the functional signal conditioning circuit demonstrated in Chapter V (section 5.3.2). The nano-scale current signal generated by the PVDF is converted to a readable signal through the OTFT-based transimpedance converter, and the signal is read out by a smart phone via a wireless micro-controller.

Electrochemical sensing is well developed and it has been used as a biochemical sensor for pH, glucose concentration and lactic acid in body fluids [181-183] because the electrochemical reaction in solution often occurs with a significant transfer of

electrical charge, i.e. the electrochemical reaction is very sensitive to concentration change. In addition, use of enzymes is helpful to improve sensitivity and make the electrochemical reaction occur selectively. However, electrochemical sensors are generally dependent on a glassy-carbon working electrode, Ag/AgCl reference electrode and Pt counter electrode, which are not flexible. Some research focuses on the functionalization of thin film electrodes and makes them compatible with flexible devices [184]. In this chapter, a flexible electrode will be manufactured via an evaporation process and modified with different functional sensing materials to detect pH variance and glucose concentration in solution. Finally, the signal will be processed by the OTFT-based signal conditioning circuit to output a linear calibration relationship.

## 6.2 Experiments

### 6.2.1 Fabrication of Arterial Pulses Sensor:

A PVDF strain sensor is capable of converting mechanical strain to a current signal; connecting the OTFT-based transimpedance amplifier with the thin film PVDF strain sensor enables a detection of arterial pulses and a conversion from nano-scale current to a readable voltage output, displayed by micro-controller or oscilloscope, shown in figure 6.1. Based on this circuit diagram, there are two versions of an arterial pulse sensor developed. The first version of the sensor is based on the 10 x 10 $cm^2$ flexible patch, and second version is based on the smaller size transimpedance converter that has optimized layout and encapsulation. Although the structures of the two sensors are based on the same circuit, different output signals from them are exhibited either to a micro-controller followed by smart phone wirelessly, or to an oscilloscope.

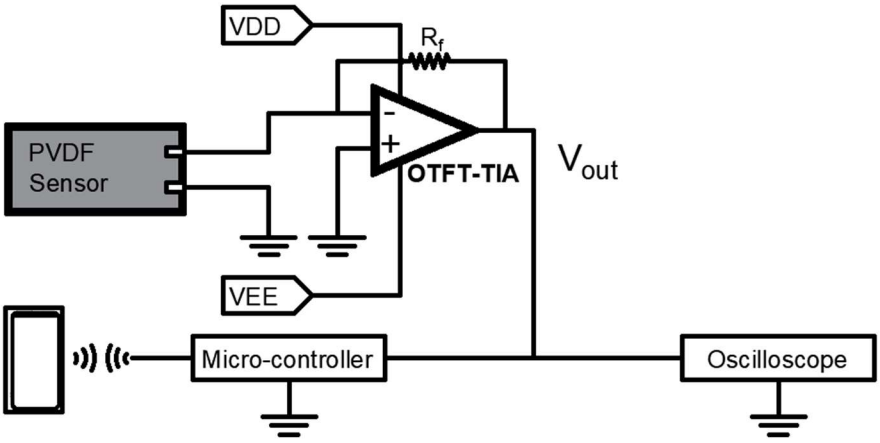



Figure 6.1. Schematic of PVDF arterials pulses sensor

### 6.2.2 Manufacture of Thin Film Electrode:

Thin film gold electrodes are manufactured using the E306 evaporator with a vacuum of 2 x $10^{-5}$ mbar. Because the purchased PET substrate is covered by a protective film, this protective film can act as a shadow mask. An initial pattern of the electrodes is created on the protective film before evaporation by cutting through the protective film layer with a scalpel. The protective films in the objective area are removed manually to expose the substrate. Next, samples are placed on the holder of the E306 and gold is evaporated onto the substrate to cover all areas of the sample, with an evaporation rate of 1 nm/s and total thickness of 30 nm. Finally, the protective film covering the marginal areas is removed, hence removing extra gold in the marginal areas as well. As a result, only the objective area is coated with gold. After the thin film gold electrodes are prepared, a layer of silver paint is applied onto the areas where the electrical contacts will be made as protection from damage by the contacts for measurement. Shown in figure 6.2, epoxy insulating materials are coated on the top part of the surface area of the electrodes to ensure each sample has similar active area

(1 x 2 $cm^2$) when immersed in solution without needing to control carefully the depth of immersion.

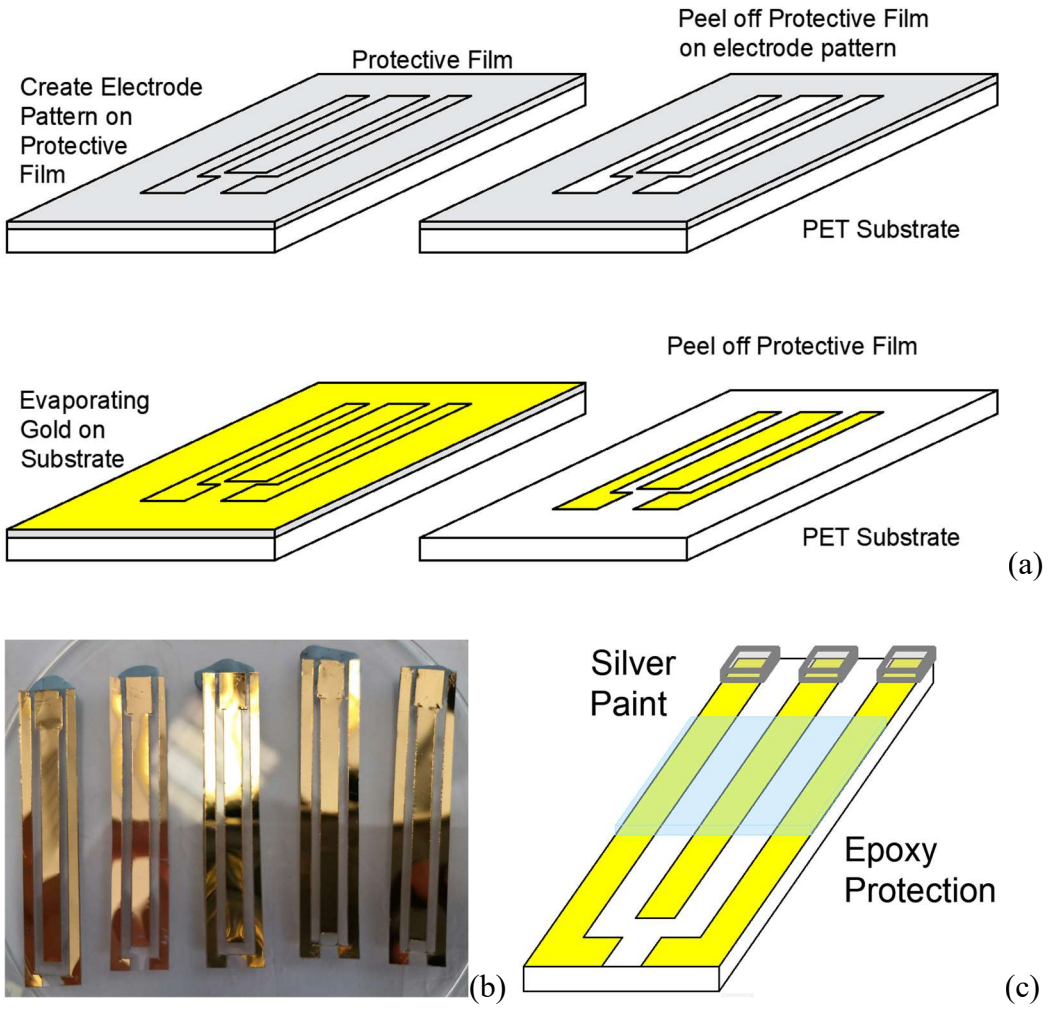



Figure 6.2. Schematic of Manufacturing Thin Film Gold Electrode

### 6.2.3 Cysteamine Functionalized Thin Film Gold Electrode and pH sensor

Initially, a non-flexible hydrogen ion detector was created and provided by Dr Salzitsa Anastasova, who is a collaborator in this project. The needle electrode is functionalized with hydrogen ion selective material, iridium oxide ($IrO_x$) as described in [185] and then connected to a voltage buffer (LMP7721, Texas Instruments) followed by a 1 kΩ resistor in series to generate the current signal. By connecting this pH detector to the

OTFT-TIA, it is possible to convert the nano-scale current to a readable voltage output signal on an oscilloscope, shown in figure 6.3. After obtaining the current output under different pH environments, a calibration curve can be plotted as output voltage against pH.

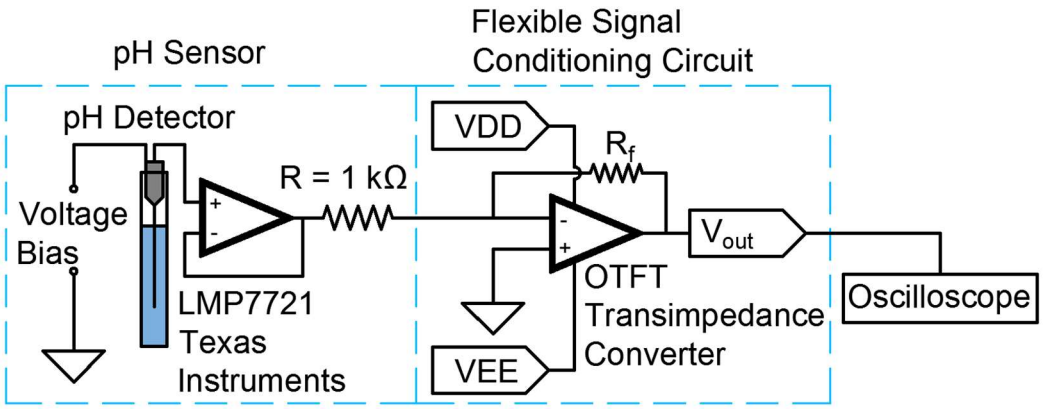



Figure 6.3. Structure of Customized Needle-type Sensor

In order to create a flexible pH sensor, a thin film gold electrode on a PET substrate is a suitable option. Cysteamine is a compound, structure shown in figure 6.4, which is chosen as it can interact with gold with strong bonding through the sulphur atom and the amino group on it can interact with hydrogen ions in solution to form an $–NH^{3+}$ cation at the surface of gold electrode. The thin film gold electrode is firstly immersed into an 80 mM aqueous solution of cysteamine for 24 hours and then dried in an ambient environment. In cyclic voltammetry measurements, dynamic voltage scans from 0 to 1.2V with four scanning rate, 2.5 mV/s, 5 mV/s, 10 mV/s and 20 mV/s were carried out. After that, chronoampermetry is used to monitor variance of pH over time.

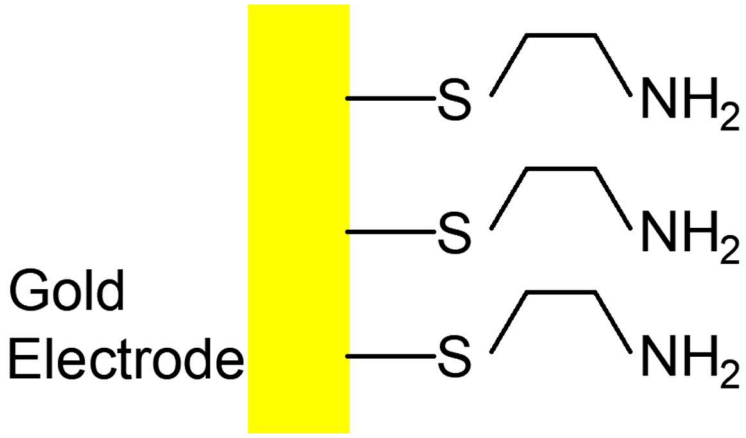



Figure 6.4. Structure of Cysteamine and interaction with Gold

### 6.2.4 Detection of Hydrogen Peroxide with bare gold thin film

Because gold can catalyse the decomposition of $H_2O_2$, the bare thin film gold electrode is directly used as sensor head in solution. The electrochemical testing system is built as figure 6.5. Initially, the Keithley 2400 is used to provide a dynamic voltage bias and records a current in cyclic voltammetry. In this test, two pairs of electrodes are tested. The first pair consists of thin film gold as working electrode, a Ag/AgCl reference electrode and a Platinum wire as the counter electrode. The second pair has thin film gold as the working and counter electrodes with Ag/AgCl as the reference electrode. Voltage scanning is from 0 to 1.2V with scanning rate of 5 mV/s with increasing concentration $H_2O_2$ in phosphate-buffer saline (PBS). Afterward, Keithley 2400 and OTFT-TIA are combined in chronoampermetry, the middle electrode is connected to the bias source, and the left and right electrodes are connected each of the OTFT-TIA and Keithley 2400 for current recording. The bias voltage is set at the position where a current peak shows up in voltammetry. In this way, a real time sensing monitoring system is built to obtain sensing current – time curve. During testing, a magnetic stirrer is used with a spinning rate of 100 rpm to promote mixing of solute in solution.

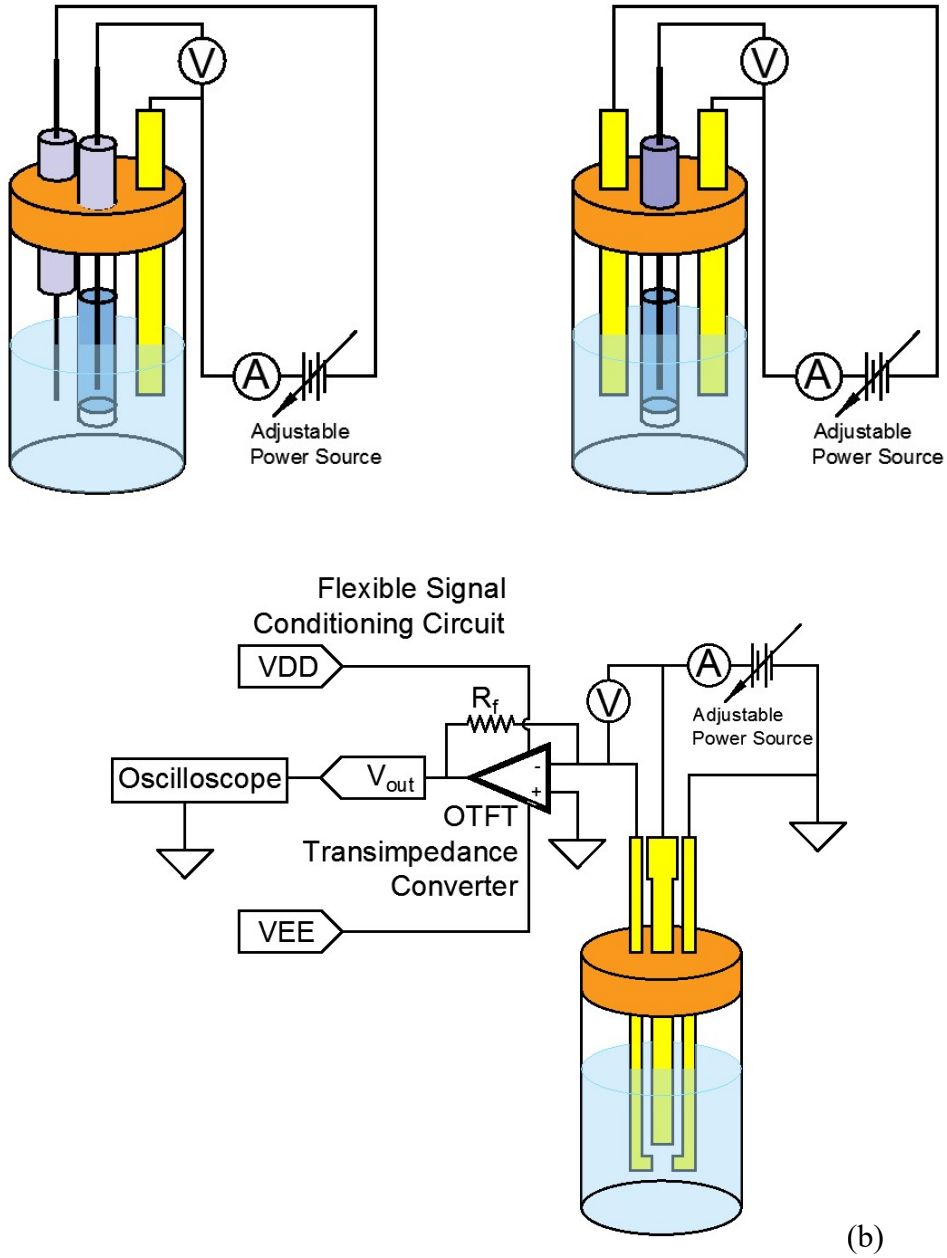



Figure 6.5. Electrode setup for (a) Cyclic Voltammetry and (b) Chronoampermetry

### 6.2.5 Glucose Oxidase Functionalized Thin Film Gold Electrode as Glucose Sensor

To fabricate a flexible sensor for glucose detection, using glucose oxidase allows us to exploit the high selectivity of enzymatic reaction to create a glucose-specific sensor. A product of the enzymatic reaction, hydrogen peroxide, can be electrochemically

detected by the thin film gold electrode. Due to the weak bonding between gold electrode and glucose enzyme, a binder molecule is needed to constrain the glucose oxidase (GOx) to the thin film gold electrode, where the reaction products can then be detected. Thiophene-based polymers can be used because the sulphur atom can directly interact with gold atom, whilst another functional group, such as hydroxyl and carboxylic group on the enzyme can bind to the polymer. In this work, a copolymer of thiophene and 3-thiophene carboxylic acid, shown in figure 6.6, is synthesised and used as binder between the surface of the thin film gold electrode and GOx. This polymer is chosen as the thiophene units can react with the gold surface and the carboxylic group can connect the amide group on glucose oxidase to achieve functionalization of the enzyme on the gold electrode.

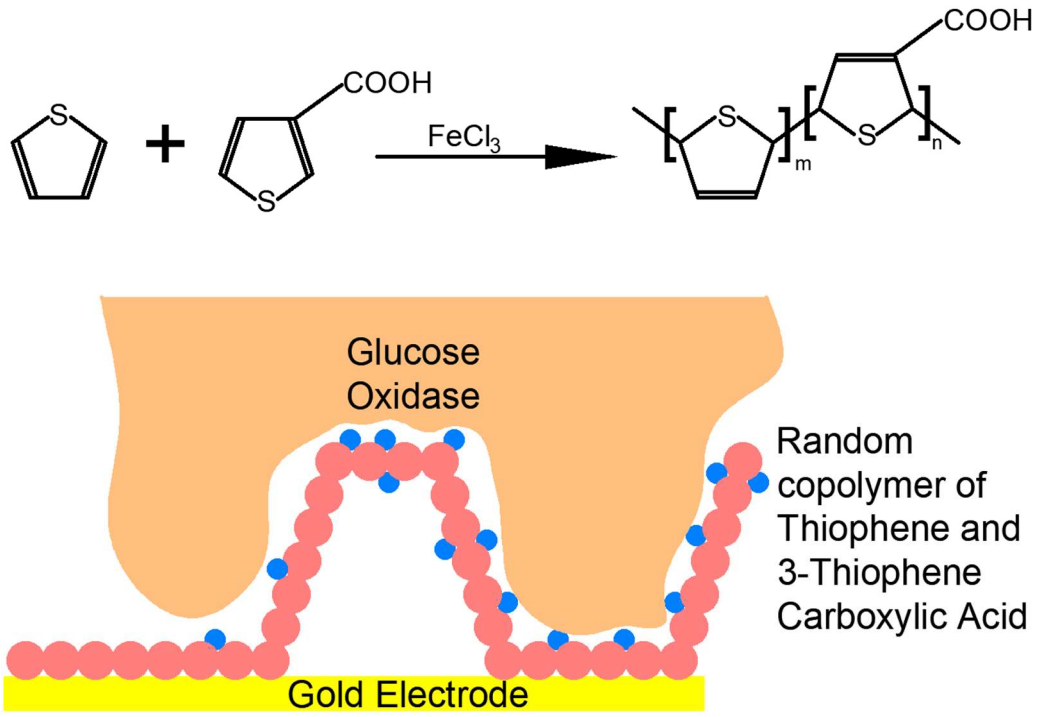



Figure 6.6. Polymerisation of Thiophene and 3-Thiophene carboxylic acid (upper) and binding interaction with gold and GOx (lower)

Copolymers of Thiophene (Th) and 3-Thiophene carboxylic acid (3TCA) are created in $CHCl_3$ solution with $FeCl_3$ as a catalyst [186]. Three different molar ratios of Th and 3TCA were used, listed in table 6.1. The copolymerisation occurs in an $N_2$ environment over 24 hours under ambient temperature around 25 $^oC$. The experimental set up is shown in figure 6.7. Afterward, the remaining solid deposit of $FeCl_3$ is removed by filtering, and the liquid phase is transferred to a separating funnel. Because $FeCl_3$ exhibits a higher solubility in the aqueous phase than that in the chloroform phase, extra DI water is added into a separating funnel, to wash out $FeCl_3$ from chloroform phase by shaking. The washing is repeated until the colour of the chloroform phase is light yellow. Finally, the organic phase is separated and all the organic solvent evaporated under 50 $^oC$ to obtain the polymer.

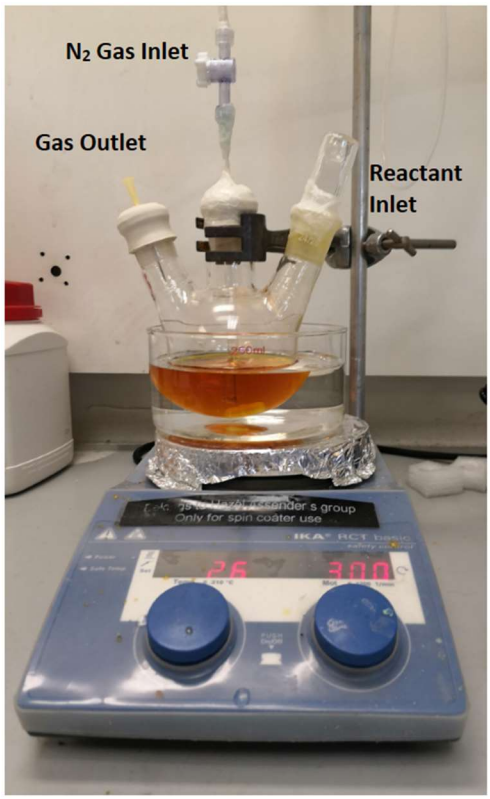



Figure 6.7. Synthesis device for Poly-(Thiophene)-(3-Thiophene Carboxylic Acid)

Table 6.1. Concentration ratio of Thiophene and 3-Thiophene Carboxylic Acid

| Solution | 10:1 | 1:1 | 1:10 |
|---|---|---|---|
| Thiophene | 20 mM | 10 mM | 2 mM |
| 3-Thiophene Carboxylic Acid | 2 mM | 10 mM | 20 mM |

The presence of the carboxylic group is helpful to build a bridge between the copolymer and GOx, however, it increases the solubility of the copolymer in water, making the copolymer less stable against detaching from the substrate in aqueous solution. In order to optimize the concentration of carboxylic groups, copolymers with different ratios of Th/3TCA are sampled for solubility and bonding tests.

In the solubility test, samples with similar, known mass, are mixed with DI water to the same weight concentration and allowed to dissolve quiescently for 1h. After that, 95% of the volume of solution is removed using a fine pipette without disturbing the polymer deposited on the bottom and then the residual water is evaporated to leave the residual copolymer. The weight difference before and after the dissolution can indicate how much of the material dissolved.

After selection of a copolymer with suitable ratio of Th/3TCA, a mixture of copolymer and GOx is made. To enable connection between GOx and copolymer, an intermediate mixture of $H_2O/CH_3CN$ with water content of 50% is used to dissolve both copolymer and GOx. This has been shown possible without damage to the GOx over a period of hours [140]. In this work, poly-(Th)-(3TCA) and GOx are dissolved into acetonitrile ($CH_3CN$) and water respectively, and then the two solutions are mixed with volume ratio of 50%/50%.

To immobilize GOx on the surface of thin film gold, the mixture of GOx/Poly-(Th)-(3TCA) is applied on top of the copolymer by drop-casting and then dried under

reduced pressure for 10 minutes. The coating and drying steps are repeated 10 times to immobilize sufficient functional materials onto the gold surface. To prevent oxidation and further damage of GOx, the functionalized electrode is tested in PBS solution immediately after coating.

The electrochemical testing method is similar to that of the $H_2O_2$ sensor. For cyclic voltammetry, the dynamic voltage was scanned from 0 to 1.2 V with four different scanning rates 2.5 mV/s, 5 mV/s, 10 mV/s and 20 mV/s. Afterwards, chronoampermetry is used for testing glucose content variance under a fixed bias voltage, at which the current response of CV curve exhibits a peak. In this test, glucose concentration is increased in steps, and then at each step bias voltage is switched on to record the current response until steady. The mean value of the stable current is plotted against concentration of glucose to obtain the calibration diagram. To demonstrate selectivity of sensor, the sensory response is tested in a PBS solution with continuously increasing concentration of uric acid, finally, the sensory response to uric acid is compared with that to glucose.

## 6.3 Results and Discussion

### 6.3.1 Performance of Arterial Pulse Sensor

The first arterial pulse sensor is based on the OTFT-TIA fabricated with silver-ink interconnections. The extracted heart rate is displayed in figure 6.8; signals are collected from each of oscilloscope and smart phone. The blue curve is directly collected from the oscilloscope which has more noise than orange curve that is collected from smart phone and filtered via Fast Fourier Transform algorithm to

remove the 50 Hz noise [187]. The second arterial pulse sensor is based on the small-size integrated OTFT-TIA which has same circuit diagram but different layout and more encapsulation or protection package, and its sensory response (from oscilloscope) is displayed in figure 6.8(b).

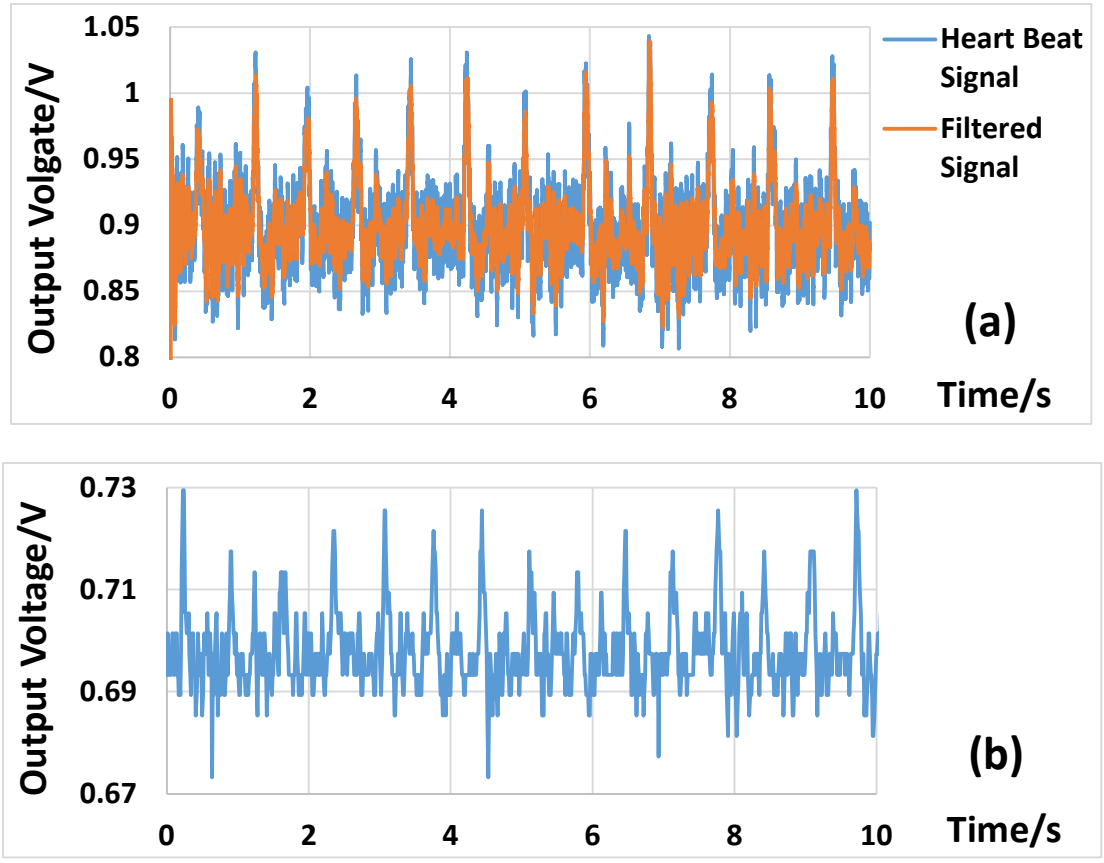



Figure 6.8. Heart Rate recorded by the OTFT-based Sensing System (a) Sensor – 1 (Blue curve is visualized by oscilloscope and Orange curve is visualized by Smartphone and (b) Sensor – 2 visualized by oscilloscope

Comparing the performance of these two sensors, signals are normalized by equation (6.1), where X represents the voltage signal of each data point, $\mu$ and $\sigma$ are mean value and standard deviation of signal. Thus, the standard score that has no unit will be used to represent strength of signal against the mean value of signal.

$$Standard\ Score = \frac{X - \mu}{\sigma} \ldots\ldots\ldots (6.1)$$

It is noticeable that the first sensor exhibits a higher strength of signal than the second sensor, and the signal/noise ratio of each sensor are extracted separately, shown in table 6.2.

Table 6.2. Comparison of Signal and Noise

| | Mean Strength of Signal | Mean Strength of Noise | Signal/Noise Ratio |
|---|---|---|---|
| Sensor-1 | 3.33 | 1.20 | 2.78 |
| Sensor-2 | 3.04 | 0.73 | 4.16 |

As discussed in the Chapter V (section 5.3.2), the mask with an interdigitated structure exhibits less shadowing effect, i.e., it is helpful to reduce the off current. Therefore, second sensor exhibits higher signal/noise ratio, which is dependent on the on/off ratio of transistor in the differential pair. In additional to the geometrical issue, encapsulation might be a reason for the different signal/noise ratio, the second sensor is tested in a metal shielding box due to small size while first sensor is tested in an Al-foil covered plastic box, which has a worse shielding effect and so the noise level is relatively high.

Although the signal processing capability of OTFT-based circuit is still limited compared with a commercial, non-flexible, amplifier, the power consumption of the OTFT-based circuit is estimated in range of $10^{-6}$ W by product of overall current in circuit and the rail-to-rail voltage (difference between VDD and VEE) [188]. It is much smaller than the power consumption of commercial amplifier ($10^{-3}$ W), which is important for the market of wearable devices.

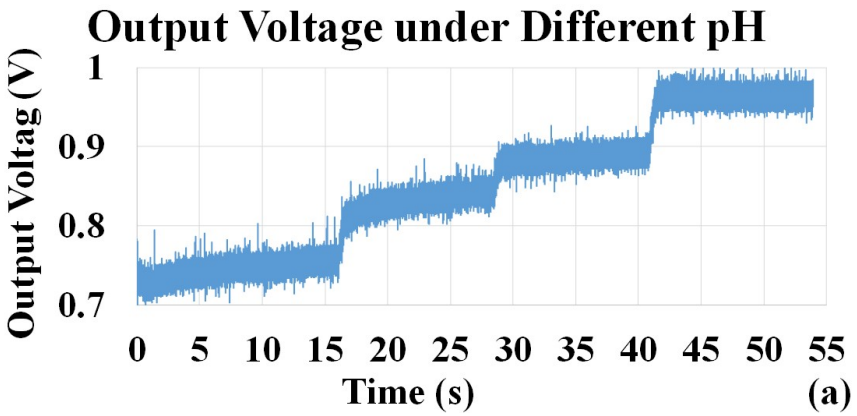
### 6.3.2 Performance Analysis of pH Sensor

The first needle-type pH sensor was used to detect hydrogen ions with following reaction and its Nernst Equation,

$$2[IrO_2(OH)_2 2H_2O]^{2-} + 3H^+ + 2e^- \leftrightarrow [Ir_2O_3(OH)_3 3H_2O]^{3-} + 3H_2O \ldots\ldots (6.2)$$

$$E = E_0 - \frac{2.3RT}{2F} log\left[\frac{[Ir_2O_3]}{[IrO_2]^2[H^+]^3}\right] \ldots\ldots (6.3)$$

The activity of hydrogen ion ($H^+$) and oxidation state of $IrO_x$ determines the thermodynamic equilibrium, and hence determines the sensing signal. On a change of ion concentration, the sensing electrode generates a voltage signal firstly (Nernst equation) and it is converted to current signal after the voltage buffer followed by a resistor. After that, the OTFT-based signal conditioning circuit converts the current sensing signal to a readable level for the oscilloscope and displayed in figure 6.9 (a). There is a noticeable step wise increase of output voltage with increasing pH. After plotting output sensing signal with the pH, a linear calibration curve can be obtained, shown in figure 6.9 (b).



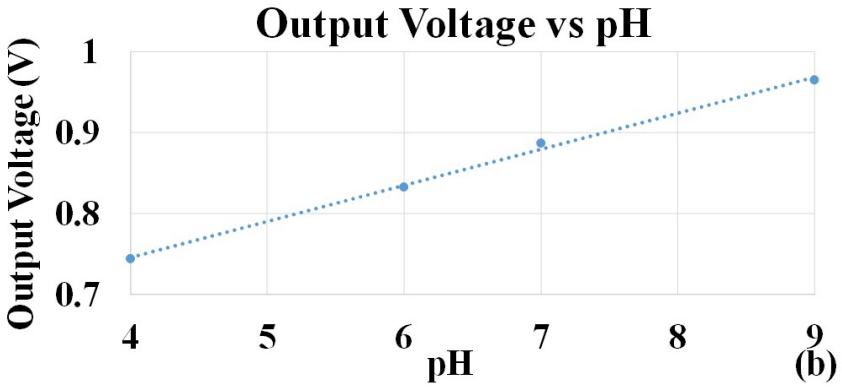



Figure 6.9. (a) Real-time monitoring of pH and (b) Calibration curve for pH sensor collected from sensing system consists of needle-type detector and OTFT-based Converter

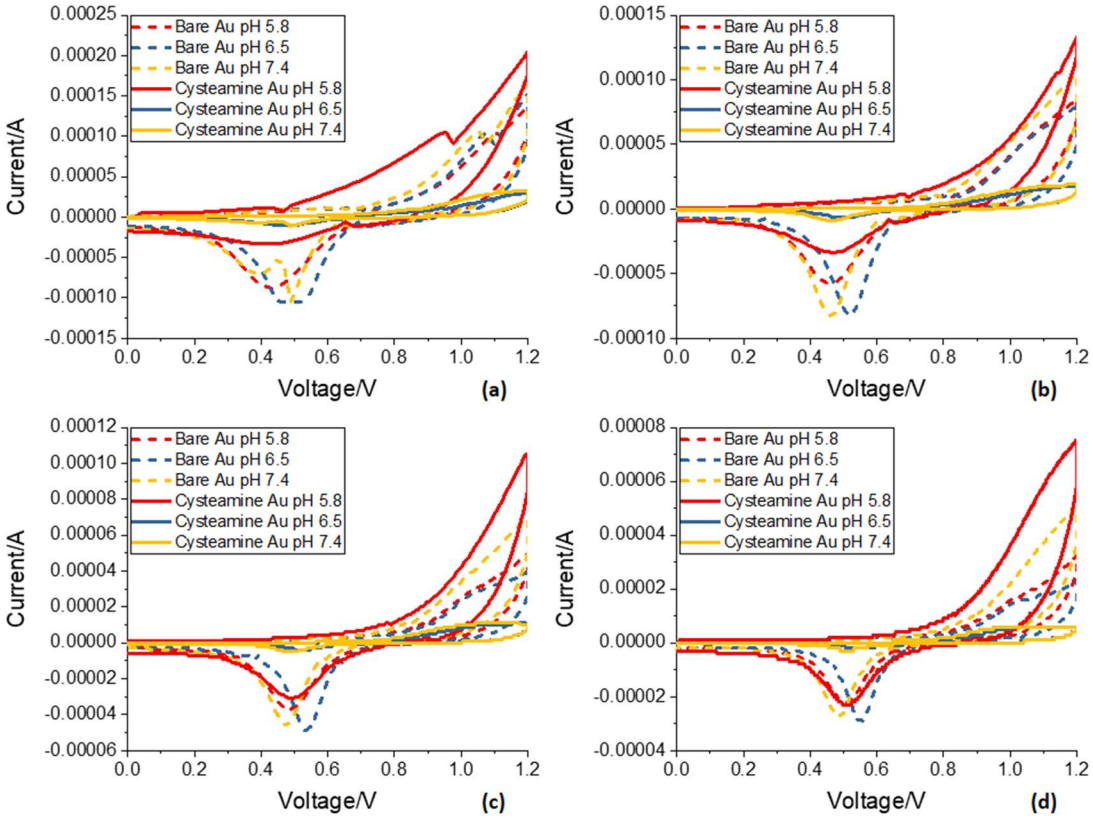



Figure 6.10. Cyclic voltammetry of bare Au electrode and cysteamine coated Au Electrode in solution of pH 5.8, 6.5 and 7.4 with scanning rate of (a) 20 mV/s, (b) 10 mV/s, (c) 5 mV/s, and (d) 2.5 mV/s

In addition, a thin film cysteamine coated gold electrode is used to detect pH variance in solution. Because the $–NH_2$ group on cysteamine can form $–NH_3^+$ with hydrogen ions in solution, the cysteamine coated electrode is expected to exhibit a higher current response when a redox reaction occurs than for the case of the naked gold electrode. The cyclic voltammetry scanning results are shown in figure 6.10. They show that the cysteamine coating can reduce the current response at approximately 0.5 V to close to zero in a quasi-neutral solution (pH 7.4 and 6.5). When the solution pH is decreased to 5.8, i.e., activity of hydrogen increases, although cysteamine coated electrode decreases current response at 0.5 V, the current response of bare Au electrode is similar to that of cysteamine coated electrode when scanning rate is slow.

Because the thin layer of cysteamine on gold surface is only able to separate the hydrogen ions from gold electrode for a short time, when there is insufficient time for hydrogen ions to diffuse to the gold surface, i.e., fast scanning, the response current is low at close to neutral pH due to there being less hydrogen ion participating in the charge transfer process. However, charge transfer is not an issue when the scanning rate is slow, and the active hydrogen ion can pass through cysteamine thin film to react with the gold electrode, reducing the sensitivity of the system to pH.

In the chronoampermetry test, a rapid change of current response can be found, shown in figure 6.11, when the electrode is transferred to solutions with different pH causing a transitory signal. When cysteamine coated Au electrode is initially transferred into a new, lower pH, solution, a local in-equilibrium is established rapidly between the electrode surface and bulk solution. After that, hydrogen ions to diffuse into the cysteamine gold electrode the overall solution quickly revert to its original equilibrium, i.e., the current response declines quickly. Because the transitory current change is too

short to generate a stable signal for pH sensing, it is not suitable for application of monitoring pH variance in body fluids.

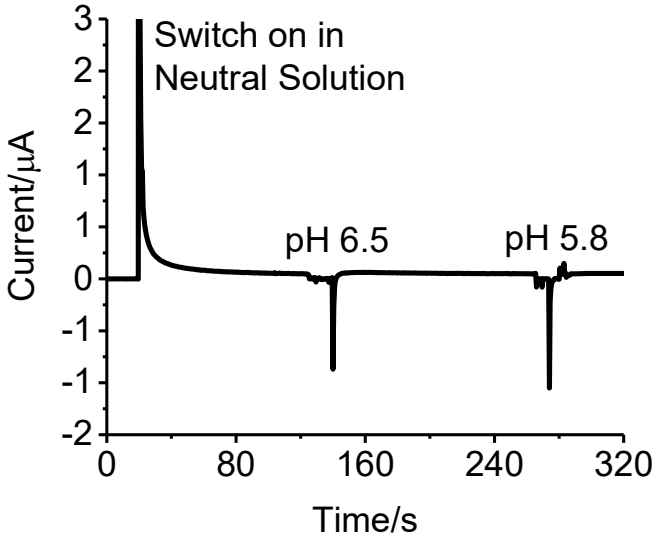



Figure 6.11. Transitory signal generated by cysteamine coated gold electrode in solution with different pH

### 6.3.3 Performance Analysis of an $H_2O_2$ Sensor

The equilibrium for $H_2O_2$ in acidic solution is described by the reaction below,

$$H_2O_2 + 2H^+ + 2e^- \rightarrow 2H_2O \ldots\ldots (6.3)$$

$$E = E_0 - \frac{2.3RT}{2F}\log\left[\frac{1}{[H_2O_2][H^+]^2}\right] \ldots\ldots (6.4)$$

In this electrode half reaction, the thermodynamic state before and after reaction is determined by activity of $H_2O_2$, and $H^+$. The cyclic voltammetry of $H_2O_2$ in PBS solution of pH 7.4 is displayed in figure 6.12, on which a series of peaks exist at around 0.5 – 0.6 V. As the concentration of $H_2O_2$ in solution increases, the peak height increases as well because more conductive species are generated from reaction and the

current increases. There is a peak shift (about 0.08 V) from the Au – Au pair to the Au – Pt pair that might be induced by the work function difference between Au (5.47 eV) and Pt (5.6 eV), because the current response is actually determined by the potential drop between the working and counter electrodes, but the voltage reading is the difference between working and reference electrodes. For the Au – Pt pair, a higher voltage is needed to compensate the work function difference to initiate same current response initiated with an Au – Au pair.

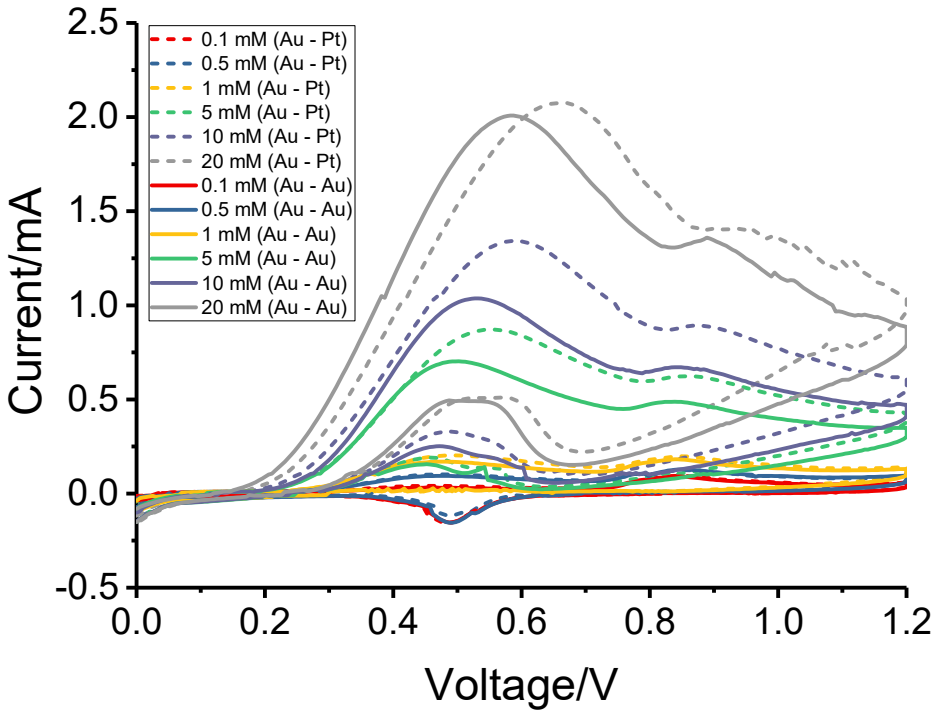
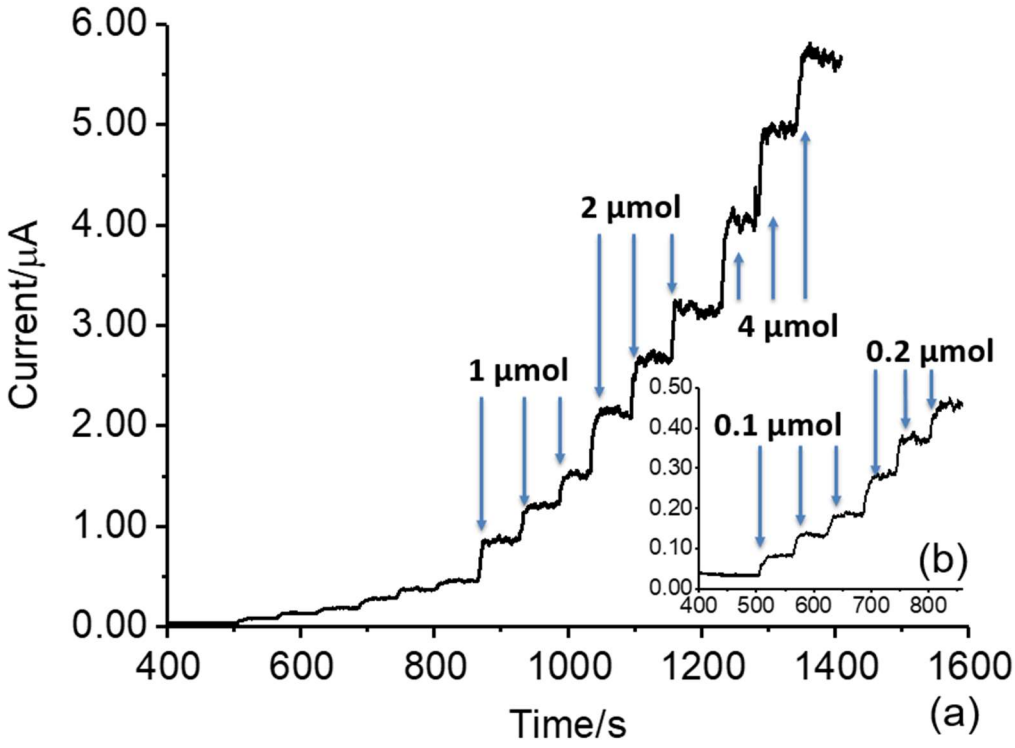


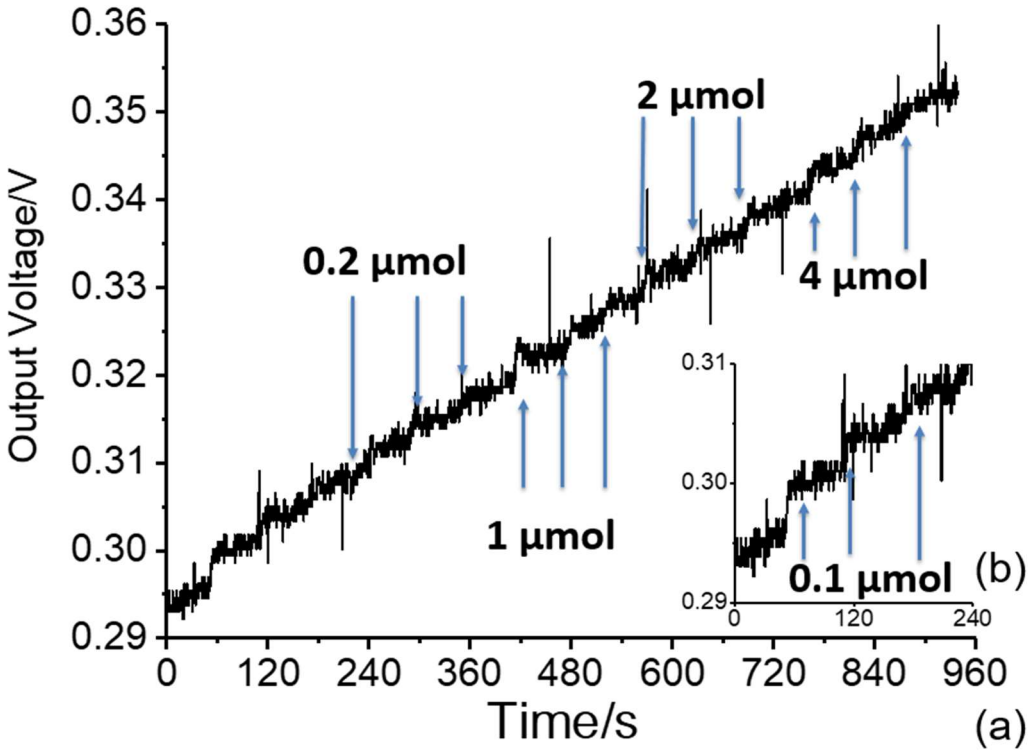

Figure 6.12. Cyclic Voltammetry of $H_2O_2$ in PBS (pH = 7.4) with Au – Au Electrode Pair and Au – Pt Electrode Pair (from the Nernst equation as concentration of $H_2O_2$ increases driving force, as observed here)

Based on the cyclic voltammetry curves, a bias voltage of 0.6 V is fixed in chronoamperometry test, and the current response is recorded with increasing concentration of $H_2O_2$ in PBS, by adding small additional amounts of $H_2O_2$ to the

solution, shown in figure 6.13. The current signal measured directly with the Keithley 2400 exhibits an increasing current with the stepwise increases in concentration. When the sensor element is coupled to the flexible OTFT signal conditioning circuit, a small stepwise increase in signal (output voltage) can be observed after a percentile filtering algorithm (removing data outlier over a specific percentile) provided by Origin. After reading the output signal and plotting it against concentration of $H_2O_2$, the calibration curve can be obtained in figure 6.14.




(I) Figure (a) demonstrates sensory response from 400s to 1600s and figure (b) demonstrate sensory response from 400s to 900s




(II) Figure (a) demonstrates sensory response from 0 to 960s and figure (b) demonstrate sensory response from 0 to 240s

Figure 6.13. Real-time Sensing Current from Keithley 2400 (I) and OTFT based Transimpedance Converter after filtering (II)

It is noticeable that the current signal recorded directly with the Keithley 2400 exhibits a linear relationship between current response and $H_2O_2$ concentration, while a linear relationship is exhibited between output voltage and log concentration of $H_2O_2$ from OTFT-based circuit. Ideally, the output signal from OTFT-based converter should exhibit similar trend in voltage scale with the signal from Keitheley 2400 because the Keithley 2400 which has a transimpedance amplifier inside for processing of small signal. A possible reason under the difference of curve trending is that overall impedance of the Keithley 2400 is much smaller than the OTFT-based circuit; as a

result, the current in the path of OTFT-based circuit is much smaller than that measured by the Keithley 2400.

Using the Keithley 2400, the current response is principally determined by the concentration of $H_2O_2$, and the signal is proportional to the variance of concentration. However, using the OTFT-based circuit, the circuit impedance is larger than the resistance of solution, i.e., the output signal becomes less sensitive to variation of $H_2O_2$ concentration. According to ohms law, signal variance can be obtained by increasing electric driving force, shown in equation 6.4, therefore, the current in this path is proportional to $\log[Conc[H_2O_2]]$. Thus, output current vs concentration and output voltage vs logarithmic concentration are plotted to obtain a linear calibration curve for each sensor.

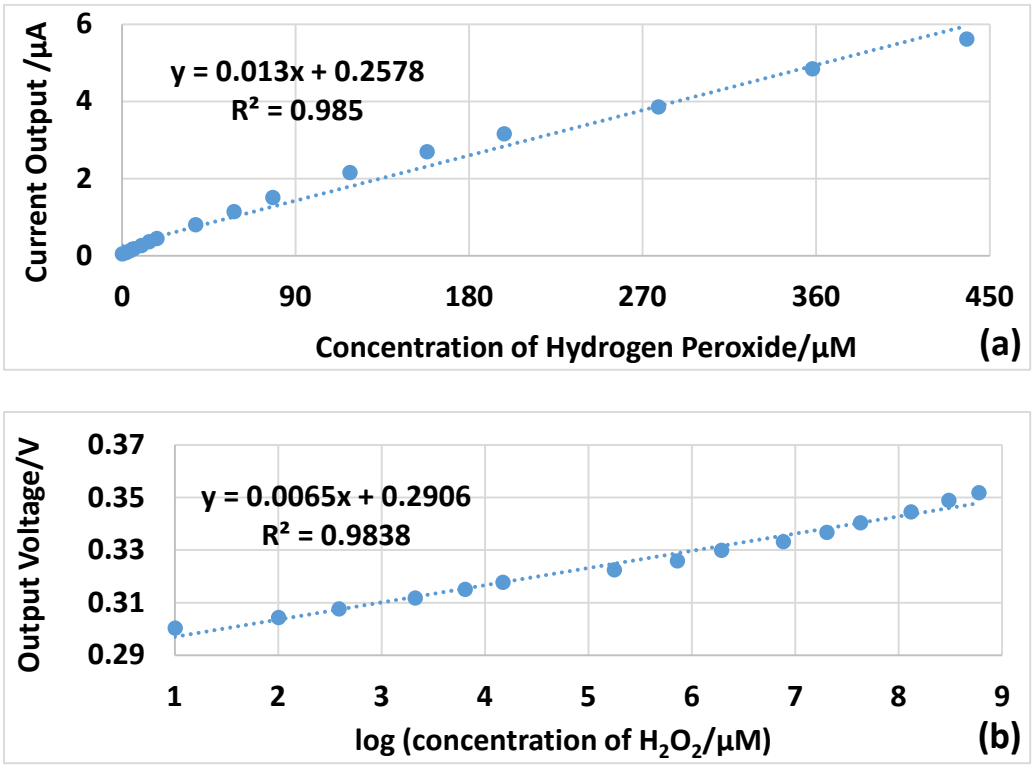



Figure 6.14. Calibration for $H_2O_2$ Sensing for (a) Keithley 2400 and (b) OTFT-based Signal Conditioning Circuit

### 6.3.4 Performance Analysis of a Glucose Sensor

The results of the solubility test of the synthesised copolymers are shown in figure 6.15. All samples exhibit a significant weight loss during the first hour of immersion, and then for the greater acid content samples, there is further weight loss after the second hour, so a long exposure to aqueous solution should be avoided. The trends indicate that water solubility of the copolymer increases with higher content of 3TCA in the polymer chain, and in next experiments in aqueous solution, testing time should not be long. Because Poly-$(Th)_n$-$(3TCA)_n$ and Poly-$(Th)_{10n}$-$(3TCA)_n$ have lower water solubility, they are selected as possible linkers to bind the glucose oxidase to the gold electrode.

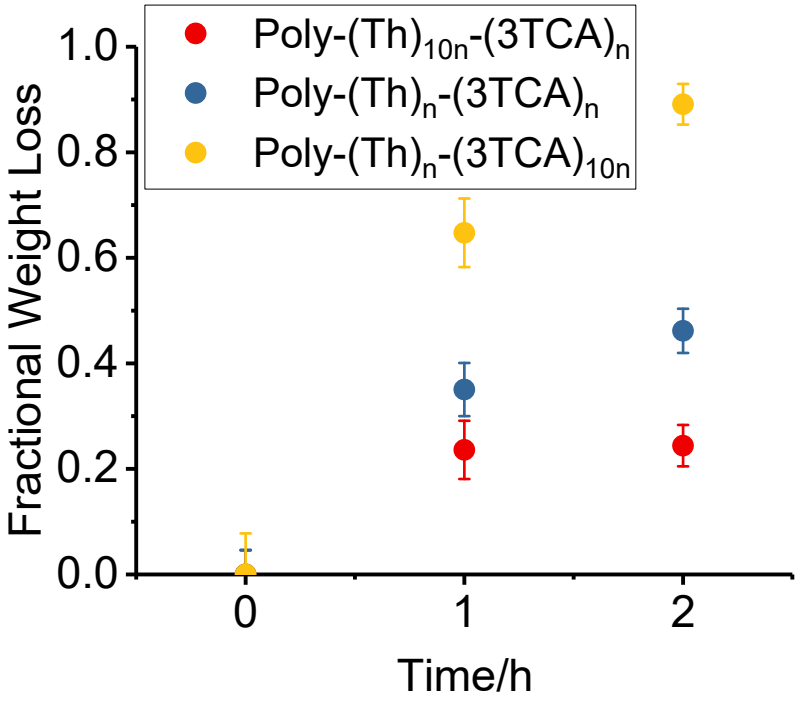



Figure 6.15. Fractional Weight Loss of different polymer immersed in water for specific hours (0 means the mass of dried materials is equal to the initial mass, i.e., no solubility)

To demonstrate the interaction between the copolymer and glucose oxidase, a mixture of GOx and Poly-$(Th)_n$-$(3TCA)_n$ or Poly-$(Th)_{10n}$-$(3TCA)_n$ is examined by FTIR. The results are shown in figure 6.15. The absorbance peak of nitrogen-hydrogen (N-H) bonds of the amino group in GOx is in the range of 3100 – 3500 /$cm^{-1}$. The GOx/Poly-$(Th)_n$-$(3TCA)_n$ sample exhibits a reduced peak in the range of 3100 – 3500 /$cm^{-1}$, i.e. lower absorbance strength indicates less N-H bonds, and might result from the formation of an amide group between GOx and the carboxylic group of the copolymer. On the other hand, there is a peak (–COOH group) at the range of 1670 – 1690 /$cm^{-1}$ on the FTIR of poly-$(Th)_n$-$(3TCA)_n$, shown in figure 6.16, and this peak is shifted to the range of 1640 – 1660 /$cm^{-1}$, while the peak of the amide group on GOx is in range of 1630 – 1650 /$cm^{-1}$. This peak shift indicates formation of amides between GOx and poly-$(Th)_n$-$(3TCA)_n$. In contrast, the GOx/Poly-$(Th)_{10n}$-$(3TCA)_n$ exhibits a similar spectrum to the GOx, i.e. there is little evidence of bonding interaction. As a result, GOx/Poly-$(Th)_n$-$(3TCA)_n$ is selected as the functional materials on the thin film gold electrode.

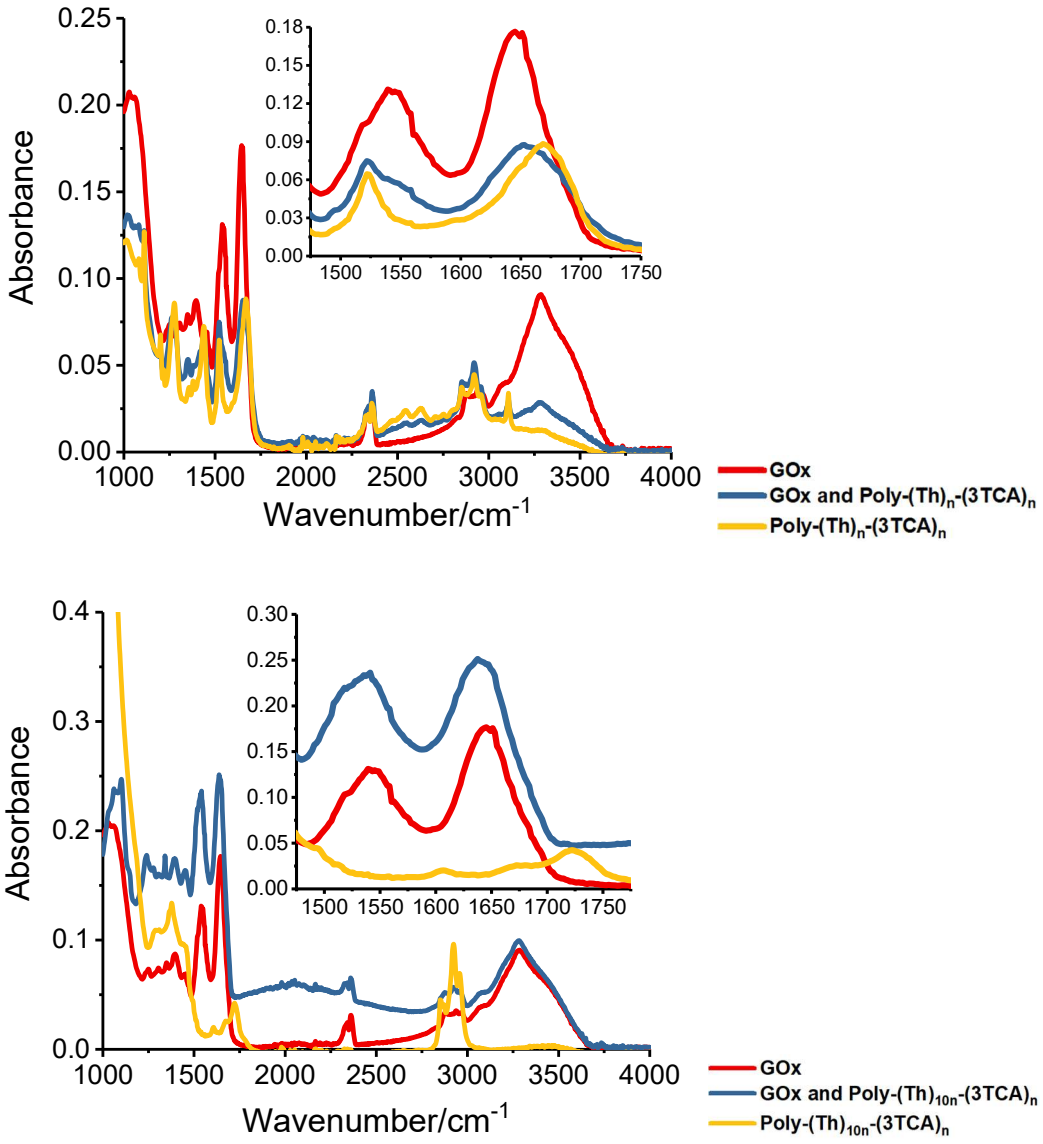



Figure 6.16. FTIR of GOx/Poly-$(Th)_n$-$(3TCA)_n$ (Top) and GOx/Poly-$(Th)_{10n}$-$(3TCA)_n$ (Bottom)

After obtaining the GOx-decorated thin film gold electrode, cyclic voltammetry is used to inspect the electrochemical reaction of glucose decomposition with the presence of GOx, and the results are displayed in figure 6.17. It can be found that a peak is forming at 0.7 V as more glucose is added into the solution when GOx is directly added into solution. In addition, the GOx-decorated thin film gold electrode, although not

demonstrating a distinct peak, exhibits a shoulder in the range of 0.7 – 0.8V forming on the larger peak at 1V with increasing concentration of glucose.

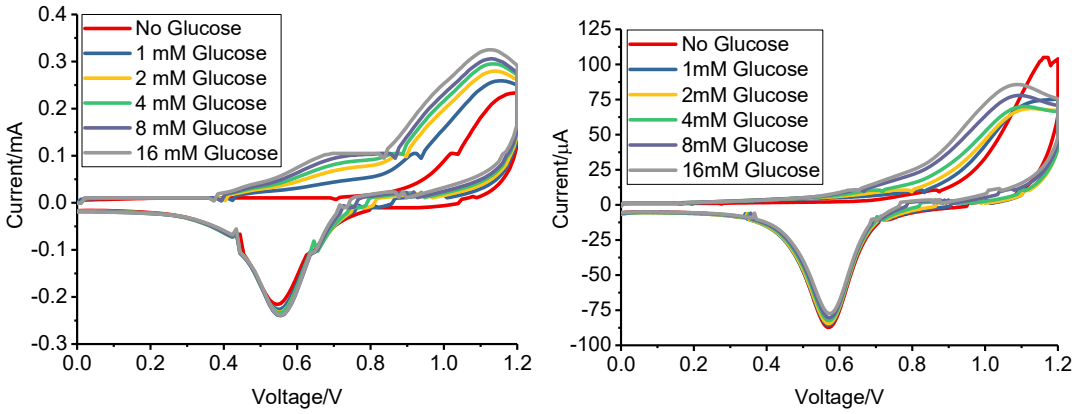



Figure 6.17. Cyclic voltammetry of Glucose with presence of 0.25 U/ml GOx (Left) and Electrochemical Reaction of GOx (0.0125 U/ml) decorated Thin Film Gold Electrode in in PBS (pH = 6) with scanning rate of 5 mV/s (Right)

In figure 6.17, the peak position, about 0.65V – 1.1V, differs from that of $H_2O_2$, 0.6V – 0.7V in figure 6.11, because the polymer/GOx layer increases the resistance of the cell Therefore, the GOx decorated thin film gold electrode is capable to detect the variance of glucose concentration, and then a calibration curve for sensor will be investigated.

A series of single-bias measurements [189] for each concentration of glucose is applied to the sensing system with a gold electrode decorated by 0.0125 U/ml GOx. The current response from the Keithley 2400 and the OTFT-based signal conditioning circuit have been shown in figure 6.18 after a percentile filtering algorithm (removing data outlier over a specific percentile). When the bias voltage is applied, there is a significant increment initially, and then the signal experiences a decay because an equilibrium of mass exchange is gradually established between the near-electrode

region and bulk solution as the local $H_2O_2$ generated by the enzyme before the bias was applied becomes depleted. The signal stabilizes at a current commensurate with the $H_2O_2$ being generated by the action of the enzyme. Because of a lack of a filter unit on the circuit, the OTFT-based device collects a noisy signal, but the overall output level can be read out by taking the mean value of output voltage when it becomes stable, e.g. from 80s to 100s in figure 6.17.

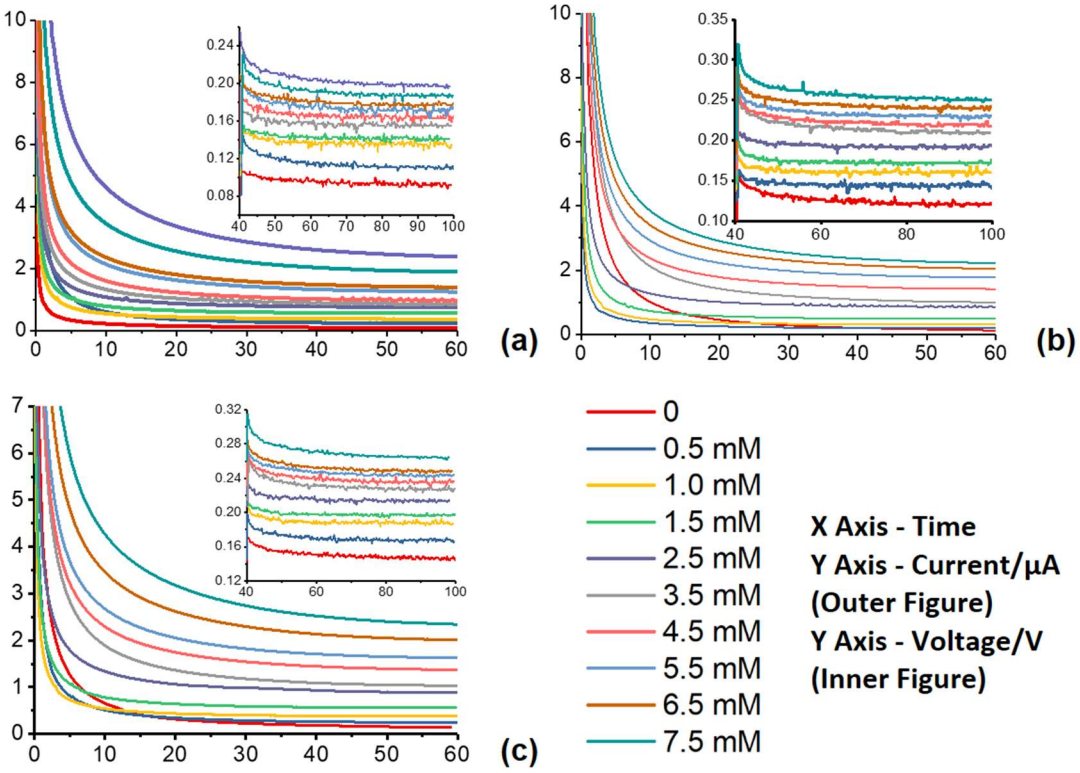



Figure 6.18. Sensory Response from Keithley 2400 (a) and OTFT-base Signal Conditioning Circuit (b)

The calibration curves for the GOx/Poly-$(Th)_n$-$(3TCA)_n$ decorated sensors have been plotted in figure 6.19. The data collected by the Keithley 2400 exhibits a linear relationship between output current and concentration of glucose, whereas data from OTFT-based circuit exhibits linear relationship between output voltage and log

concentration because of the impedance difference described previously. The slope value of linear curve can be used to demonstrate the sensitivity of sensor.

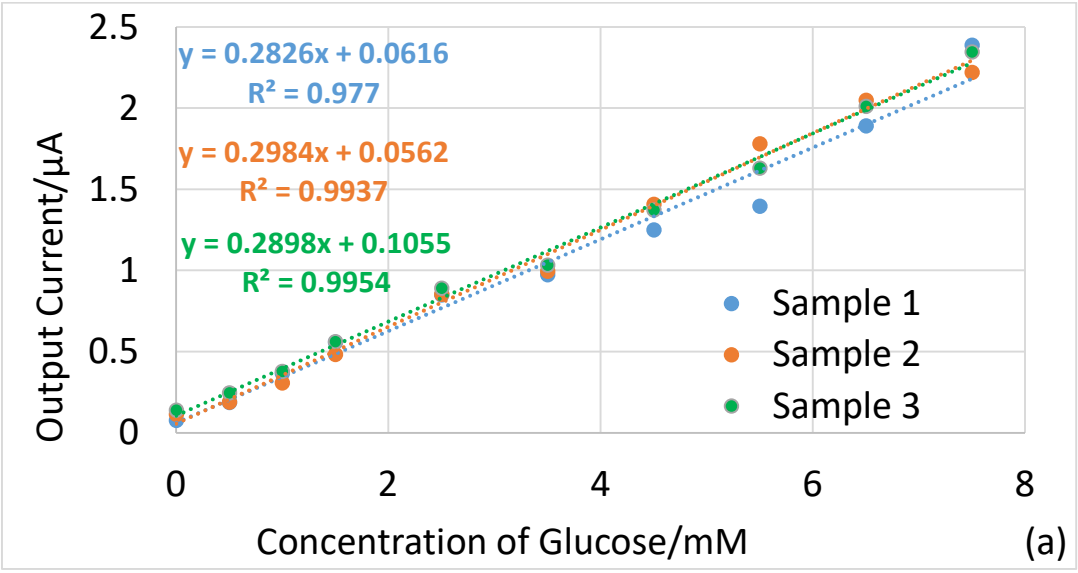



Figure 6.19. Calibration curve for Glucose Sensors (a) Signal from Keithley 2400 in Linear Scale and (b) Signal from OTFT-based circuit in Log Scale

To demonstrate the selectivity of the sensor, a series of uric acid solutions, which is a common species in body fluids, is used, and the relationship between output voltage

and concentration of uric acid has been shown in figure 6.20. It demonstrates that the sensor is less sensitive to uric acid, i.e., the slope value of sensory response to uric acid, about 0.0111 V/log(μM), is much less than that of sensory response to glucose, from 0.068 to 0.091 V/log(μM), i.e., the sensory signal to uric acid is lower. Therefore, the sensory exhibits selectivity to glucose.

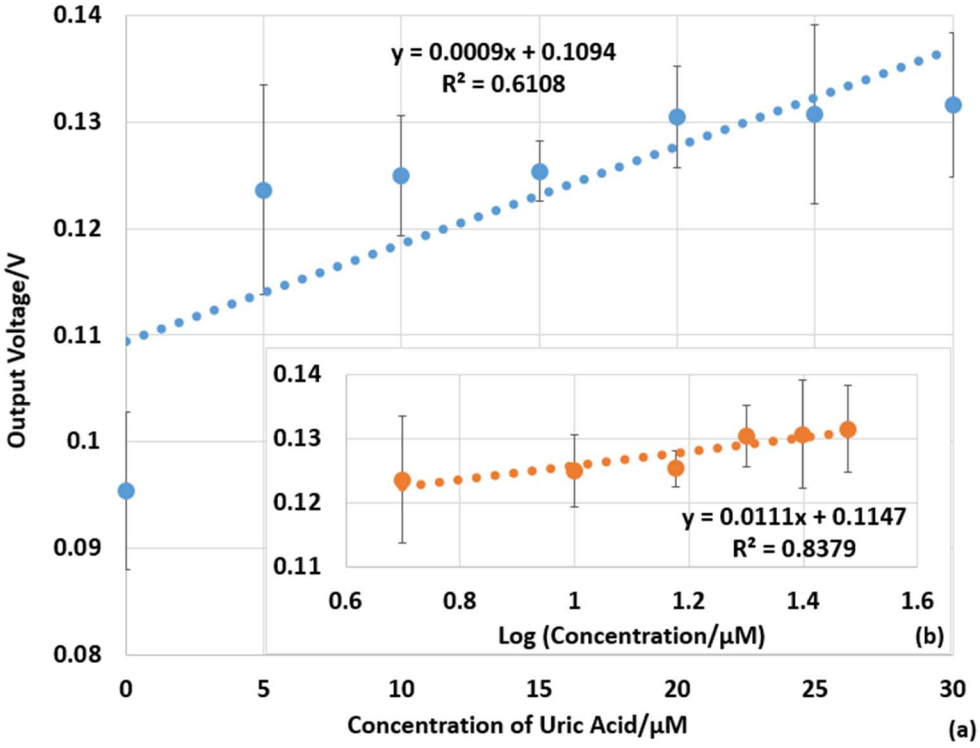



Figure 6.20. Sensory Response to Uric Acid (a) Linear Scale and (b) Log Scale

However, the sensor exhibits very weak reusability, i.e., the response becomes very small when the functionalized sensing electrode is used a second time. A possible reason is that gradual loss of glucose enzyme from the electrode surface when it is immersed in aqueous solution. In order to investigate the cause of the weak reusability, the Poly-$(Th)_n$-$(3TCA)_n$ the sample is characterised by NMR, and the $^1$H-NMR spectra has been shown in figure 6.21. Ideally, the peak around 8.2 ppm which is exhibited by the proton of carbon b on 3TCA is expected to be reduced significantly and peaks are

in the range from 7 ppm to 7.5 ppm possible aggregate for Poly-$(Th)_n$-$(3TCA)_n$. However, in figure 6.20 (III), peaks around 7.6 ppm and 7.45 ppm indicate the presence of a monomer. Comparing the peak area around 8.15 ppm (carbon c on 3TCA) and peak area around 7.6 ppm (carbon a on 3TCA), 3TCA is possibly placed at the end of the molecular chain. In addition, the peak area around 8.15 ppm, 7.5 ppm and 7.25 ppm are very similar, i.e., no dominant peak and no long-chain molecule, therefore, the product is probably a mixture of oligomers. When it reacts with the gold surface, the entanglement of the molecular chain is not strong enough to immobilize enzyme near the electrode and then enzyme glucose gradually dissolves away from the electrode surface in aqueous solution overtime.

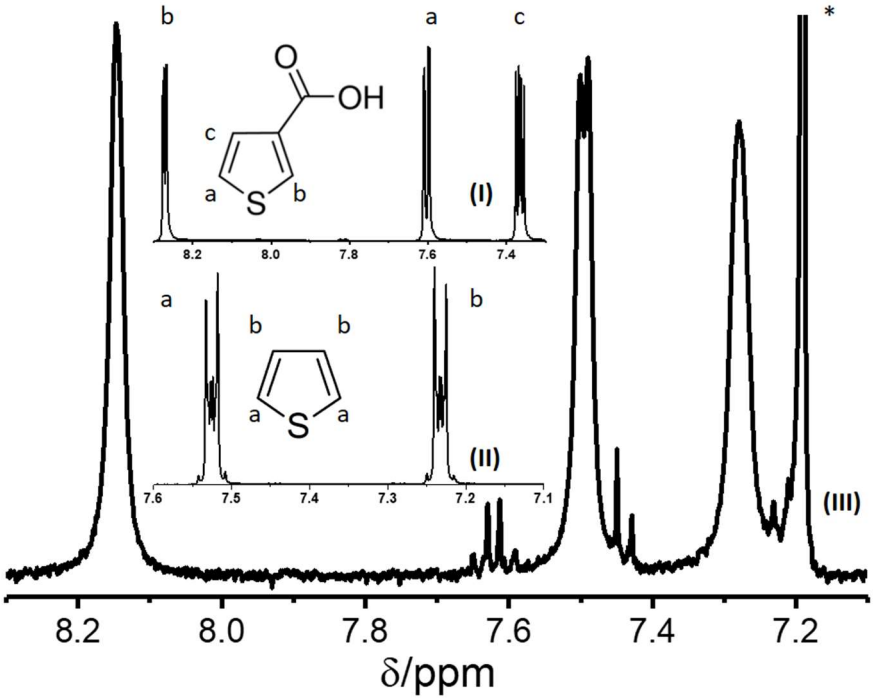



Figure 6.21. $^1$H-NMR spectra of (I) 3-Thiophene Carboxylic Acid, (II) Thiophene and (III) Poly-$(Th)_n$-$(3TCA)_n$ (Asterisk denotes the signal from residual $CDCl_3$)

## 6.4 Summary

In this chapter, two arterial pulse sensors have been created with different transimpedance converters. Although both sensors can successfully visualize an arterial pulse signal, the sensor with the interdigitated structure exhibits a higher ratio of signal to noise because of lower off-current through conductive channel. Furthermore, visualization with a smart phone demonstrates that the signal obtained by the flexible sensor is acceptable for a micro-controller due to low power consumption. In addition, two pH sensors were created with a conventional rigid electrode and flexible electrode, respectively. They demonstrate that the cysteamine coated flexible electrode exhibits a rapid signal decay which makes it difficult to obtain a stable signal for sensing. Afterward, the sensory response to hydrogen peroxide is demonstrated with a flexible gold electrode and transimpedance converter, which implies that enzymatic reaction is detectable, and then glucose oxidase decorated electrodes are fabricated with a thiophene-based copolymer binder. Finally, the sensitivity and selectivity to glucose are demonstrated, and the possible reason for the electrode's low reusability is discussed.

# Chapter VII

# Conclusion and Future Work

In this thesis, a series of OTFT and OTFT circuits have been manufactured, i.e. demonstrating that large scale vacuum processes, based on thermal evaporation are capable to produce flexible electronics with high yield. In addition, there are different sensors developed with the OTFT-based signal conditioning circuit, and the performance of sensors is evaluated in terms of sensitivity and selectivity respectively.

Firstly, the OTFTs fabricated with vacuum process to manufacture OTFT with roll-to-roll suitable techniques has been characterised, and the background mechanisms causing short circuits and current leakage have been explored, therefore, the manufacturing processes have been optimized to alleviate these problems. Next, a post aging process in ambient environment, employing oxygen doping mechanism, has been investigated to stabilize the properties of OTFT with improving mobility and reducing threshold voltage. Afterward, the effect of bias stress is investigated using a model that had previously been proposed to understand the stability of Si-based transistors. With this model, it is possible to estimate the trapping energy and the trapping density for each OTFT, and the evolution of parameters have been discussed as well. To develop a high-performance OTFT, surface cleaning of each layer is very necessary to reduce the defects that lead to short circuit and current leakage, and then thinner dielectric materials can be used to improve the performance of OTFT. In addition, the oxygen doping effect could be extended to study the effect of temperature and pressure because the doping effect in this thesis is very slow under ambient

environment, and faster process would be preferable for industrial production. The on-test instability caused by bias stress for thin film electronics is a very difficult problem, and the model in this thesis needs to be modified according to performance of OTFTs, and the parameter estimation process should be modified to improve accuracy and reducing cost of time to estimate parameters. Furthermore, more research should focus on the fundamental mechanism of charge trapping and optimization of materials or processes to reduce the overall density and distribution of charge traps.

The floating gate structure provides a solution to separate the sensing area and transistor area in order to avoid interference between the two, in other words, the fabrication of OTFT-based sensor can be modularized to two parts, manufacturing of OTFT and functionalization of floating gate. The advantages of this structure are the stabilization of the organic semiconductor with the possibility of separated encapsulation, and versatile functionalization of the floating gate electrode. An example of a strain sensor is fabricated with a floating gate structure, and it was shown to demonstrate a sensory response to mechanical bending, but the signal decay caused by bias stress introduces difficulties to read the signal. To reduce this effect, a short time and low voltage bias scheme is proposed, and it is shown that this method is helpful to reduce error, although the output signal is reduced at same time, to a level that is difficult to read with a digital current meter in daily life. In future, the floating gate structure OTFT could be optimized in two aspects, one is to improve the performance of single transistors with a thinner dielectric layer, and electrode with low contact resistance, or to optimize the structure of the floating gate to alter the charge harvesting capability and the transducing capability. In addition, ferroelectric properties of the thin film polymer can be amended to generate a stronger signal and

the thin film processing technique can be modified to be compatible with the OTFT fabrication.

In order to obtain a stable and readable signal from the sensing reaction, a single transistor is not enough, and it is very beneficial to build a signal processing circuit. In this thesis, different functional circuits have been fabricated using a vacuum process, and developed to convert the nano-scale current signal to a readable range with a linear converting relationship. After layout optimization, the signal conditioning circuit can be fabricated onto a 3 x 4 $cm^2$ area and 12 transimpedance amplifiers are made at same time. Encapsulating the converter with PDMS, it can be protected and facilitate wearable application. In future, a large-area manufacturing technique, for example flexographic technique, should be developed to produce OTFT with stable output signal and then a customized model for this technique can be created based on the property distribution of the OTFTs. In this way, the design of a circuit layout can be simulated and optimized before manufacturing to reduce potential errors in the circuit, and models of sub-circuits can be modularised as an independent object for fabrication of more complex circuits and end application. With the OTFT circuits, it is helpful to improve the reproducibility and reduce cost of manufacturing further. In addition, encapsulation materials and technique can be optimized and integrated with the manufacturing process for more stable products.

After obtaining a stable signal processor, a versatile sensing system can be constructed by integrating the OTFT-based signal conditioning circuit with different sensing electrodes. First, a strain sensor that employed a PVDF layer as the active material to detect arterial pulses works well and the signal can be visualized on smart phone via a Bluetooth micro-controller. This is very promising for application as a skin-contact

monitoring system for patients with chronic heart disease or for patient stress monitoring. In addition, chemical sensors were developed to detect concentration changes in species in solution. pH sensors are fabricated with a solid electrode and thin film flexible electrode respectively, and the rigid electrode exhibits a linear converting relationship between pH and output signal, while the flexible pH sensor still needs more optimization of the materials to have stable output. As a product of enzymatic reaction, the content of hydrogen peroxide in body fluids is an excellent indicator to reflect health condition, and a flexible hydrogen peroxide sensor is developed based on an evaporated gold electrode. Based on the sensitivity to hydrogen peroxide, a glucose sensor is developed by immobilizing glucose oxidase with copolymer of thiophene and 3-thiophene-carboxylic acid on gold electrode. Both exhibit a linear relationship between log concentration of analytes and output signal, and the functionalized gold electrode exhibits a selectivity to glucose. In future, the technique to directly integrate ferroelectric materials onto thin film electrode needs to be developed for the wearable arterial sensor. For the flexible pH sensor, it needs to transfer the redox sensing mechanism of rigid electrode onto thin film electrode and modify the materials to be compatible with biological systems. Although the glucose oxidase is helpful to detect the presence of glucose, the sensitivity still needs to be improved by loading more enzyme onto the electrode with an improved conductive polymer. In addition, the versatility of this sensing system can be extended to detect other chemical species in body fluids, such as lactic acid and cortisol in future.

The impact of flexible sensors on the construction of IoT will be very significant in future, especially in the biomedical service. From a marketing perspective, it requires more efforts to introduce the benefits of wearable sensor to the public and link the

industry of hardware manufacturing, software developing, and AI algorithm study together to build a fully connected and digitized system serving public daily life.

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# Appendix

1. Introduction of Instruments

Edward 306A is a vacuum deposition system that include thermal evaporation unit, sputtering unit, plasma generator, and a flexographic printing unit for versatile application. Each unit can work independently and coordinatively to obtain thin film materials. In addition, the embedded pinning gauge and quartz crystal microbalance (QCM) can realize in-line monitoring of pressure and film thickness as well as deposition rate.

Oxford Webcoater is a large-scale vacuum thin film processing system. Integrated with multiple coating unit, include thermal evaporator, sputtering unit, plasma generator, electron-beam generator, gasification unit, and flexographic printing unit and roll-to-roll processing unit, it is capable to realize metallization, physical vapour deposition, chemical vapour deposition with plasma or e-beam to produce thin film coating with high throughput. For example, passing speed can be within the range of 1 to 5 m/s with film width of 350 mm.

2. Introduction of Horowitz Model

The Horowitz Model describes the relationship between bias voltage and the output drain current. After applying a bias voltage, a region of charge accumulation is established at the dielectric/semiconductor interface, the distribution of charge accumulation can be described by equation (1):

$$Q_a = C_i\left(V_g - V_{FB} - V(x)\right) \ldots\ldots (1)$$

where, $Q_a$ is the accumulated charge,

$C_i$ is capacitance of insulator,

$V_g$ is the gate voltage,

$V_{FB}$ is flat-band voltage, i.e. counteract the potential difference between work function of metal and Fermi level of semiconductor,

$V(x)$ is the potential difference at position

For bulk materials, charge per unit area across the conductive channel is described by equation (2):

$$Q_0 = n_0 qt \ldots\ldots (2)$$

where, $n_0$ is the density of free charge,

$q$ is elementary charge,

$t$ is thickness of insulator,

Assuming elemental resistance $dR$ at elemental segment $dx$ of the conductive channel is inversely proportional to the width of channel, mobility of charge carriers ($\mu$) and total amount of free charges ($Q(x)$), it can be expressed in equation (3):

$$dR = \frac{dx}{W\mu|Q(x)|} = \frac{dx}{W\mu|Q_0 + Q_a(x)|} \dots\dots (3)$$

Therefore, the potential drop over the element is in equation (4):

$$dV = I_d dR = \frac{I_d dx}{W\mu|Q_0 + Q_a(x)|} \dots\dots (4)$$

Substituting equation (1) in to equation (4) to obtain equation (5)

$$I_d dx = W\mu|Q_0 + Q_a(x)|dV = W\mu Q_0 + C_i\left(V_g - V_{FB} - V(x)\right)dV \dots\dots (5)$$

After integration, equation (6) is obtained,

$$I_d = \frac{W}{L}\mu C_i\left[\left(V_g - V_{FB} + \frac{n_0 qt}{C_i}\right)V_d - \frac{V_d^2}{2}\right] \dots\dots (6)$$

The term $\left(V_{FB} - \frac{n_0 qt}{C_i}\right)$ can be defined as threshold voltage ($V_{th}$), and equation (6) can be expressed as:

$$I_d = \frac{W}{L}\mu C_i\left[(V_g - V_{th})V_d - \frac{V_d^2}{2}\right] \dots\dots (7)$$

3. Python Code to optimize Trapping Energy and Trapping Density

https://github.com/woshizk/Thesis_Appendix

4. Matlab Code for Strain Measurement

https://github.com/woshizk/Thesis_Appendix