Fast Switching of High Current WBG Power Devices

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Abstract

Wide-band-gap power devices, such as Gallium Nitride High Electron Mobility Transistors and Silicon Carbide Field-effect Transistors, offer impressively fast switching performance compared to their traditional Silicon counterparts. However, Si designs have not stood still, and new generations of these devices offer good switching performance at competitive prices. This paper makes a comparative study between a representative selection of 650 V SiC MOSFET, GaN HEMT, and Si IGBT power switching devices. The devices are switched as fast as possible using a low inductance PCB design and no external gate resistors. A mathematical analysis of switching energy losses is presented, along with SPICE simulation and experimental test results for comparison.

1 Introduction

Today, Wide Band-gap (WBG) devices offer superior switching performance but are yet to match Silicon (Si) devices in terms of price and availability. A new generation of Si devices offer switching that is satisfactory for many applications, at competitive prices. It is therefore not a clear-cut engineering design decision as to which devices will be best for a particular application. The motivation for this paper is to help switched-mode circuit designers make an informed choice, by presenting a like-for-like comparison of performance between different types of devices when they are switched as fast as they will go.

We present an experimental study of switching performance comparing the latest silicon and WBG power transistors. These are 650V devices with approximately 30 mΩ on-state channel resistance. The tests are carried out at a junction temperature of 100 °C and so are representative of real-world operation. The authors have gone to considerable lengths to ensure highest switching performance as measured by edge-rates (rate-of-change of drain current and drain-source voltage) for each power device: The Printed Circuit Board (PCB) design uses SMD packages for the power devices and associated key power circuit components to minimise stay inductance. The switching losses are measured using embedded measurement circuits that have been designed for high accuracy (2% at DC) and high bandwidth (approximately 500 MHz). Experimental test results are presented for both manufacturer-recommended gate resistor values and zero-ohm external-gate-resistor drives.

The main contributions of this paper are as follows:

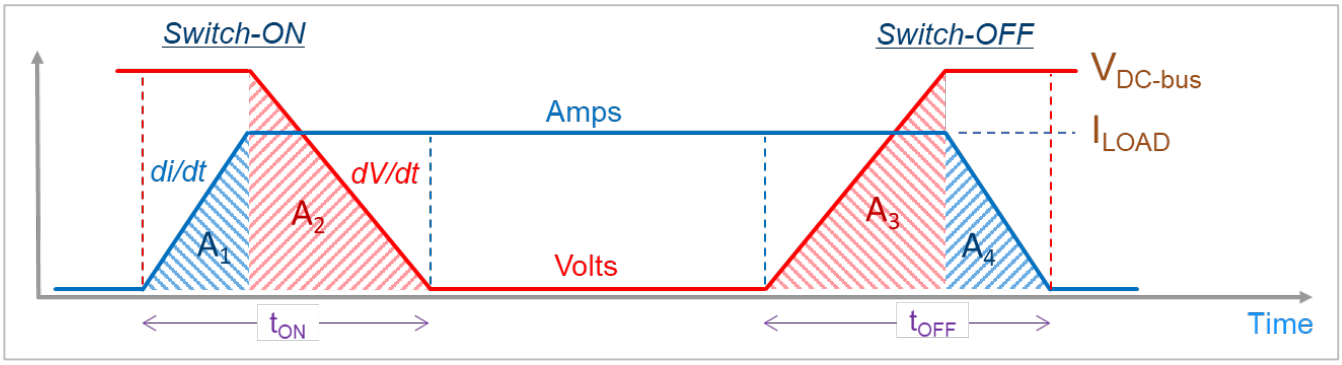
1. The latest and best-in-class Silicon and WBG devices are compared using a half-bridge test circuit with a 400 V-DC bus voltage and a 40 A switched inductive load current. An elevated operating temperature of 100 °C is used to mimic real-world use conditions.
2. A comparison between experimentally measured and SPICE-derived switching losses for Si and WBG devices.
3. A demonstration of the switching performance achieved by using zero external gate resistance.
4. An example of a circuit layout optimized for switching speed using non-conventional PCB construction methods.

This work is motivated by the desire to achieve fast edge-rates and low switching losses. With careful PCB layout, a favourable balance between switching losses, voltage overshoot and power throughput can be achieved.

2 Switching Theory

There are two contributions to MOSFET switching loss – one is due to the stored charge in the output capacitance of the device and other capacitances at the output node, and the other is due to the overlap between voltage and current during the switching transition. The first part should be minimised with careful PCB layout that pays attention to the switched-node parasitic capacitance. The second part depends on how quickly the device is turned on or off. Both losses can be largely eliminated using soft-switching techniques, but that is not the subject of this paper.

Fastest switching results in the shortest possible overlap region between the device voltage and current, *Figure 1*. However, parasitic inductances in the device package and layout of the circuit can cause oscillation and voltage overshoot, which



$$P_{LOSS} = (½ \times V_{DC} \times I_{LOAD} \times [t_{ON} + t_{OFF}] \times f_{SW}) + (½ \times C_{OUT} \times V_{DC}^2 \times f_{SW}) + (R_{DS(ON)} \times I_{LOAD}^2)$$

Figure 1: Switching diagram shows integration of area under idealized current and voltage switching transitions as a way to calculate energy dissipation in a single switch cycle. The power loss equation adds output capacitance discharge energy loss; These per cycle energy losses are multiplied by the switching frequency to give power loss. The addition of a conduction loss term completes this assessment of power loss in a half-bridge switch stage to a first order approximation.

increases the switching loss and can lead to device failure by over-voltage. For these reasons manufacturers typically recommend using external gate resistors to slow down switching to reduce drain-source overshoot and damp gate-source voltage oscillation, but at the cost of increased switching loss. Once again, careful layout and choice of low inductance packages is essential when aiming to minimise the required gate resistance.

An approximation of the losses in a half-bridge switching circuit is shown in *Figure 1*. The product of the idealized current and voltage waveforms is integrated to calculate energy dissipation in a single switch cycle. The power loss equation adds output capacitance discharge energy loss [1]. These 'per cycle' switching energy losses are multiplied by the switching frequency to give power loss. The addition of an I^2R conduction loss term completes the loss assessment. The governing factors are switch edge-rate, parasitic switch node capacitance, and on-state channel resistance. There are also parasitic loss mechanisms, such as body-diode reverse recovery charge Q_{rr}, non-linear Miller and output capacitances, along with inductance shared between source-pin on the power device and gate-drive current return path; all of which tend to increase losses, especially when switching at fast edge-rates.

2.1 Switching Loss Numerical Model

A more sophisticated numerical approach is presented in this section. The following equations [4] are used to calculate the rise (r) and fall (f) times of current (i) and voltage (v) of the device during turn-on and turn-off events.

$$t_{ir} = R_G C_{iss}(V_{DS}) \times \ln\left(\frac{V_{GS+} - V_{TH}}{V_{GS+} - V_{gp}}\right) \quad (1)$$

$$t_{vf} = R_G \times \frac{Q_{GD(D)}}{V_{DS(D)}} \times \frac{V_{DS}}{V_{GS+} - V_{gp}} \quad (2)$$

$$t_{on} = t_{ir} + t_{vf} \quad (3)$$

$$t_{vr} = R_G \times \frac{Q_{GD(D)}}{V_{DS(D)}} \times \frac{V_{DS}}{V_{gp} + V_{GS-}} \quad (4)$$

$$t_{if} = R_G C_{iss}(V_{DS}) \times \ln\left(\frac{V_{gp} + V_{GS-}}{V_{TH} + V_{GS-}}\right) \quad (5)$$

$$t_{off} = t_{vr} + t_{if} \quad (6)$$

Here, R_G is the total gate resistance, C_{iss} is the effective input capacitance as seen by the gate drive circuit, and is a function of V_{DS}; V_{GS+} and V_{GS-} are the relative values of the positive and negative bias voltage applied between gate and source. V_{DS}, V_{TH}, V_{gp} are drain-source, gate-threshold, and gate-plateau voltages respectively. $Q_{GD(D)}$ is the datasheet-specified gate-drain charge at the datasheet test condition with drain-source of $V_{DS(D)}$.

Using the above equations, the switching energies during turn-on and turn-off can be calculated:

$$E_{on} = \frac{1}{2} V_{DC} I_{LOAD} t_{on} + \frac{1}{2} C_{OUT(D)} {V_{DC}}^2 \quad (7)$$

$$E_{off} = \frac{1}{2} V_{DC} I_{LOAD} t_{off} \quad (8)$$

Note that the $½CV^2$ component of switching loss occurs only during the turn-on of the device. A charge-equivalent output capacitance [5] at the drain-source voltage of V_{DC} is calculated from manufacturers' datasheet plots.

These equations do not consider additional losses due to the parasitic mechanisms previously mentioned. However, as shall be shown in later sections, with appropriate packaging and PCB layout, these parasitic effects have only a modest effect on the waveforms.

3 Circuit Parasitics

At high switching frequencies, a successful converter design needs to minimise the negative effects of the following parasitic elements:

1) *Common Source Inductance (CSI)* is the inductance shared between the gate-drive and power circuit, both inside the device package and externally on the PCB.
2) *Gate Loop Inductance (GLI)* is related to the area enclosed by the gate-drive current path to the switching die and the return path from the source connection back to the gate-drive 0 V pin. If this inductance is too high, critical damping may not be achieved, resulting in switching instability and device failure [8].
3) *Switched Current Commutation Loop Inductance (SCCLI)* is related to the area enclosed by a circular current path through both upper and lower switching devices in a half-bridge topology and any local decoupling capacitance. If this inductance is too high, it can result in significant over-voltage spikes at switch-off and oscillations at the switching-node during fast transitions.
4) *Switch-Node Capacitance (SNC)* is the capacitance across the two power devices in their off-state, plus the capacitance from the switching node copper traces to ground through the board.

All of these parasitic elements primarily operate to slow down switching and increase losses.

4 SPICE Simulation

Circuit simulation has been conducted in LT Spice. The simulations place a device model within a circuit that is representative of the experimental system. The transistor models have been downloaded recently from the device manufacturers' websites. Three parasitic elements were added to the SPICE simulation circuits, based upon measurements taken with a VNA (Vector Network Analyser) on a test PCB:

1. *Switched Current Commutation Loop (SCCL) inductance:* A value of 0.6 nH was measured around the commutation loop, containing both power devices and local DC-bus capacitors.
2. *Gate-drive loop inductance:* A value of 8 nH was measured between the gate drive IC and power device, including both gate trace and return current path.
3. *Switched node capacitance:* A value of 90 pF was measured at the switch node copper to the power ground plane underneath. Note that this value is for the board only and does not include the output capacitance of the power devices.

In each case, a single lumped value inductor or capacitor component was added to the simulation circuit to represent this parasitic element. The simulations all used L3 models with 100 °C junction temperature or a global temperature setting.

5 Test Platform Design

The authors have developed a high-performance test platform (*Figure 4*) to achieve the fastest possible switching edge-rate from the power devices. The parasitic circuit inductances have been minimised with careful PCB layout and the use of a thin (25 µm) polyimide dielectric in a between the top two copper layers *(Figure 2).*

To accurately measure switching loss, voltage and current measurement circuits are embedded on the PCB to avoid high-frequency noise artifacts typically introduced by traditional voltage and current probes and to minimise their contribution to circuit parasitics.

A very low SCCL inductance is achieved using a multi-layer PCB that puts the current return path directly under the main switching components, with the thin polyamide layer between these two opposing current paths.

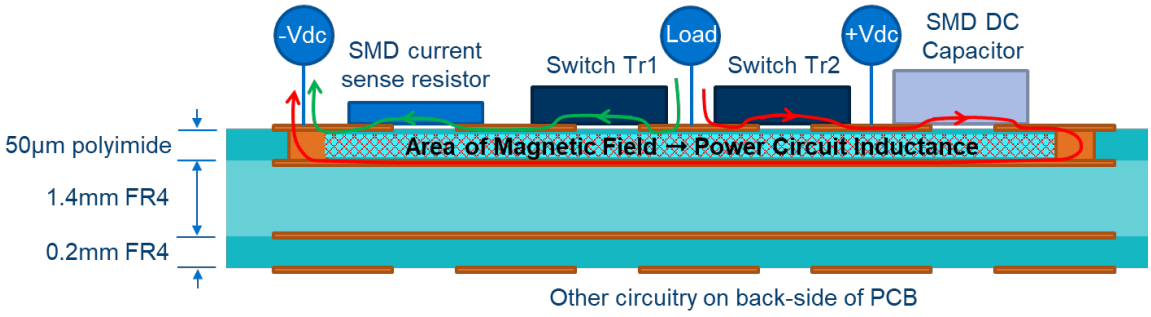


Figure 2: Hybrid circuit board construction achieves low inductance layout using multi-layer construction with a polyimide dielectric between the switching traces on the top layer and current return path directly underneath. In this way the opposing current directions cancel a magnetic field that would otherwise cause switching inductance.

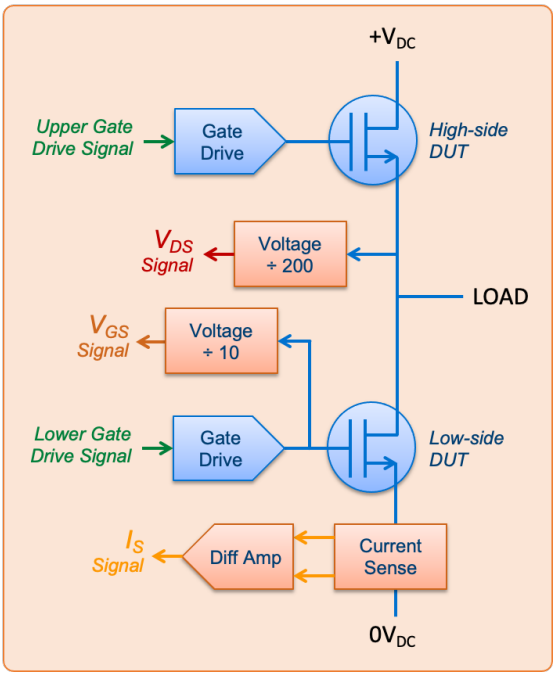


Figure 3: Schematic diagram of the embedded measurement and gate-drive circuits, with the power transistors in a half-bridge configuration.

Key advantages of polyimide are:

1. High break-down voltage per unit thickness of material (> 100kV/mm).
2. Homogeneous material that is free of defects and voids, to ensure that the voltage can be supported reliably across the area of material.

Such a thin layer would be difficult to achieve reliably with conventional FR4 material. Clearly there is a trade-off between achieving low inductance, using a thin dielectric and high overlap of the commutation current path with the power ground return trace, and creating undesirable capacitance at the switch node to power ground through this same thin dielectric material. This is unavoidable but can be managed by keeping the power devices close together to reduce the interconnect copper area.

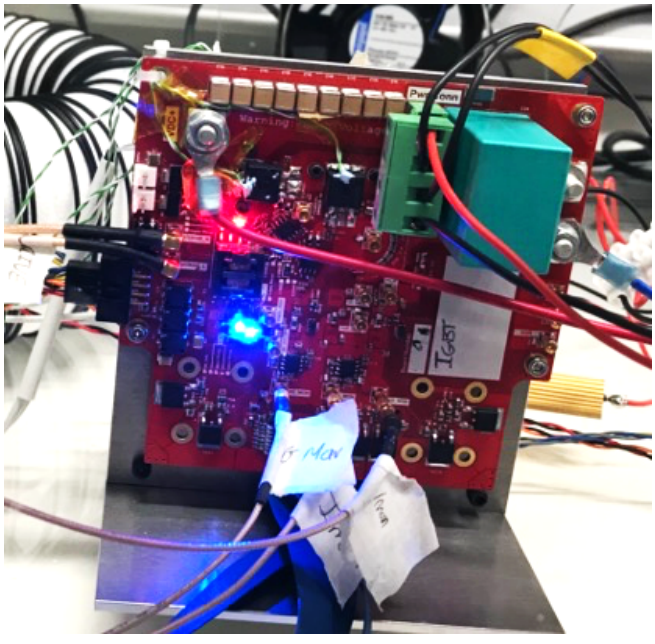


Figure 4: Photograph of authors' test platform PCB, showing power stage and measurement systems.

The measurement circuits were designed to minimise insertion effects on the switching devices and circuit being tested [3-5]. The measured signals are switched-node voltage, gate-voltage of the lower device, and switched current in the lower device, *Figure 3*. The latter measurement is normally difficult to obtain due to the added inductance of the current transducer in this critical position in the circuit. This design uses parallel-connected low-inductance sense resistors coupled to local amplifier circuit (total 3.3 mΩ & <100 pH). Using on-board measurements ensures the signal path delays are matched, allowing for accurate calculation of the switching losses.

Identical PCBs are used for each device type to ensure that a fair comparison of the performance for the three different device technologies (SiC MOSFET, GaN HEMT, Si IGBT) is made in their respective packages (all are surface-mount).

6 Experimental Results

The experimental switching results for this paper were obtained using double pulse tests [3] and are set out in *Figure 5*. The current is ramped up through a load inductor and the device under test is then switched off and back on under full voltage and current. This approach is particularly important for the Si IGBT to allow it to reach a stable conductivity modulated on-state. The inductor is air cored, with a low turn-to-turn capacitance. As the test is only repeated 4 times per second, there is no significant heat generation in any of the components. Therefore, the power devices are pre-heated to 100 °C by an external heater. In the tests the devices are switched with or without an external gate resistor.

6.1 Switching Waveform Comparison

Switching waveforms from the experimental tests with zero external gate resistances are set out in *Figure 5 (a-f)*. The measurements are obtained using a 350MHz LeCroy MDA8000 12-bit Oscilloscope. The waveforms are free from large amounts of ringing. No shoot-through currents are observed.

At turn off, *(d-f)* the switching shows minimal overshoot voltages, suggesting the SCCL is as small as expected. Turn-on therefore proceeds as expected *(a-c)*, with a small initial voltage dip during the high *di/dt* due to the small residual stray

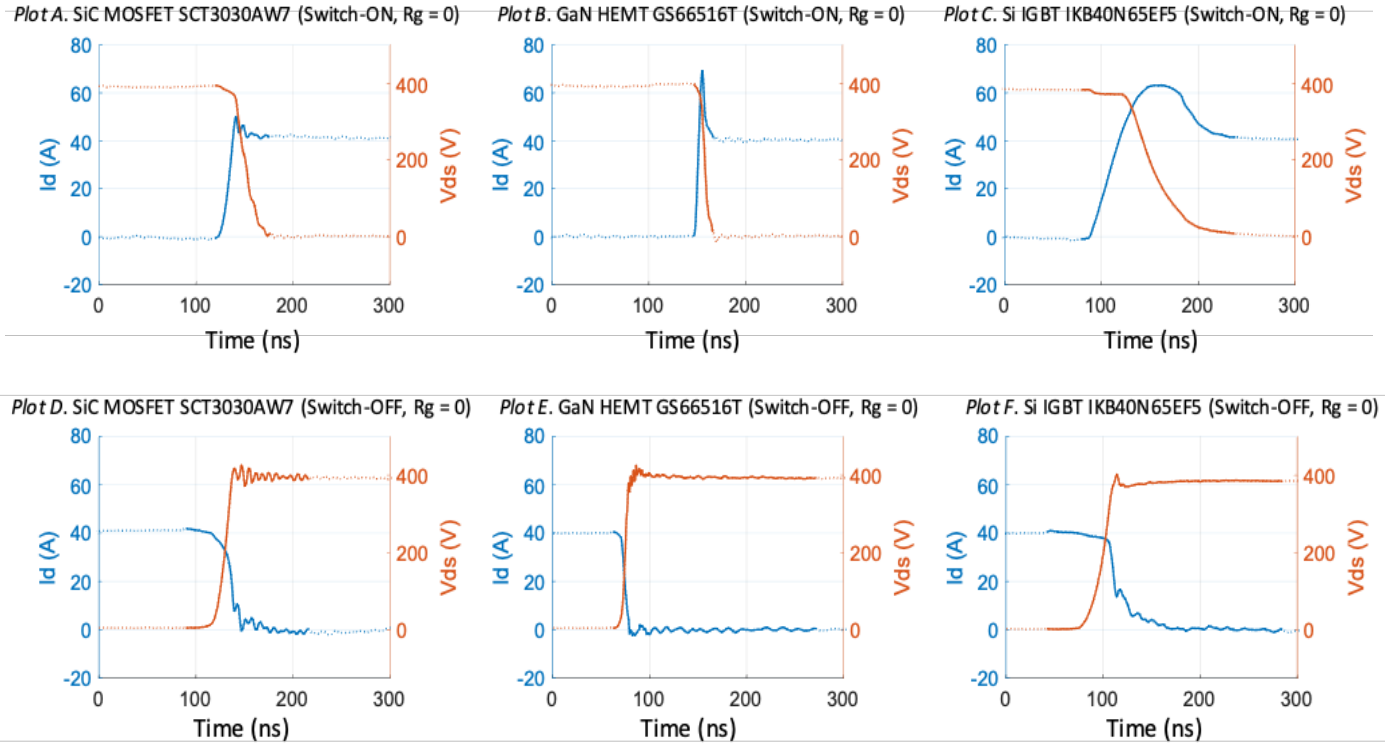


Figure 5: Switching waveforms at zero-ohms external gate resistance, for both switch-on and switch-off, shows the difference in switching performance between these three different types of power devices. The combination of fast transitions and wire-bonded package for the SiC device results in ringing after the switch-off event, but is not sufficient to cause reliability issues or significant additional losses. The GaN device achieves very fast switching transitions and therefore can be used at high switching frequencies. The IGBT switching is much slower than the other two devices, but this may be sufficient to achieve low overall losses for many lower frequency applications.

inductance. Each turn-on waveform shows a current overshoot. In *(a),* the upper SiC MOSFET body-diode reverse recovery and C_{OUT} discharge current is observed as a modest current peak. A larger overshoot current is seen in the GaN HEMT waveforms *(b),* but the total switching time is greatly reduced compared to that for SiC, at around 25 nsec.

Clearly the GaN HEMT device switches the quickest and with lowest losses, both at turn on and turn off. It is notable that the GaN waveforms are nearly ideal, with well-defined on and off periods and step changes to the di/dt and dv/dt, while the SiC MOSFET current and voltage waveforms have significant curvature and some lower frequency ringing noticeable at turn off.

The Si IGBT turn on is relatively slow, although the turn off is surprisingly rapid, close to that for the SiC MOSFET. Despite the large overshoot current at turn on, the IGBT switching is well controlled. At turn off, it shows the typical IGBT characteristics, with a steep initial current fall followed by a significant current 'tail'. There are pronounced device stray inductance effects at turn on, with a noticeable drop in the voltage during the relatively slow current rise.

6.2 Estimation of Switching Losses from Experimental Waveforms

The recorded voltage and current waveforms have been processed to find switching losses by trapezoidal integration of the voltage-current product over each sampling interval, over a time window covering the switching event. The start of the time window is defined by the point at which the gate voltage, V_{gs}, has increased above 10% of $V_{gs(on)}$, or fallen below 90% of $V_{gs(on)}$, for turn-on and turn-off respectively. The end of the window is the point at which V_{ds} falls and stays below 2% of V_{DC} or I_{ds} falls below 0.5% of the inductor current I_L, for turn-on and turn-off respectively. In this way we ensure any oscillations are included in our estimation of switching energy. These are plotted in *Figure 6*.

It should be noted that for SiC MOSFET, zero gate resistance is recommended by the manufacturer. In the other cases the losses are reduced with zero Ohm switching. As can be expected from the waveforms, the SiC MOSFET losses are around 30% of those for the Si IGBT (switched with zero Ohms). Similarly, for the GaN HEMT, the reduction in losses is nearly 40%. In all cases the turn on losses are greater than the turn off losses. In the

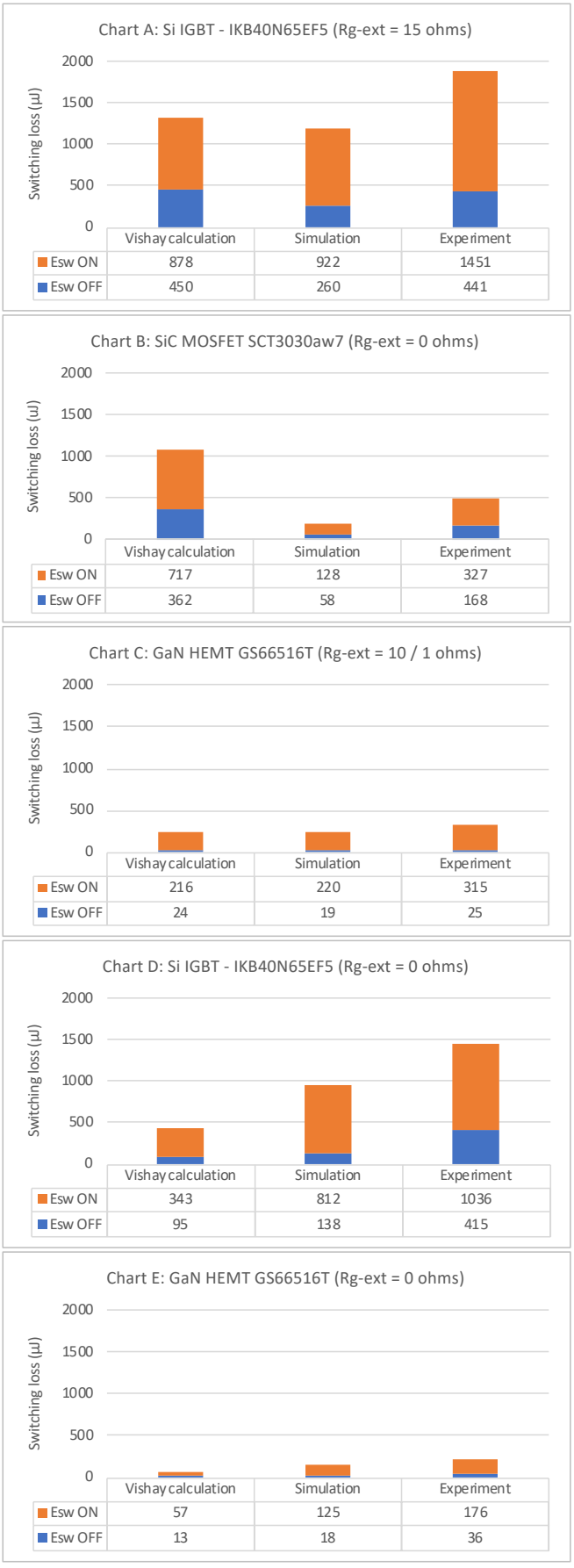


Figure 6: A comparison between switching energy loss evaluation methods and experimental test results from the switching circuits developed by the authors, in relation to accuracy.

SiC MOSFET case they are similar, but in the case of the GaN HEMT, the turn off losses are a very small proportion of the total switching losses. This would allow approximately a 60% higher switching frequency for the same total losses.

6.3 Estimation of Switching Losses from Datasheet Parameters and Simulation

The datasheet losses are all obtained at 25 °C. These are almost double those measured for the SiC MOSFET. The datasheet losses for the GaN HEMT are less than those measured with the recommended value of gate resistance (this is likely due to the higher SCCL inductance of the manufacturer's test setup compared to that used in the experiments here). But at the higher switching speed the experimental losses are lower. The Si IGBT datasheet losses are less than the measured losses for both values of the gate resistance.

In *Figure 6*, the simulations are conducted in LT Spice using the parasitic element values from the experimental setup. The results for the SiC MOSFET are relatively close to those measured. The results for GaN and the Si IGBT are more significant underestimates.

7 Discussion

An important observation is that spurious turn-on was not observed even when switching at elevated temperatures with zero gate resistance and a very low inductance circuit.

When comparing the losses, the effect of the parasitic inductance is important, as illustrated in the datasheet conditions. The GaN HEMT datasheet test circuit has 2 nH of SCCL inductance (compared to just 0.6 nH for the circuit used by the authors). However, the datasheet also has an output capacitance stored energy at 400 V of 17 uJ. Here the author's test PCB parasitic output node capacitance of 90 pF adds just 7 uJ to this. However, the capacitance also affects the waveforms in the form of a turn off snubber, shifting losses from turn off to turn on (when the capacitance is discharged by the switching device).

One further aspect which arises is related to the turn on, where the output capacitance of the off-device in the inverter leg contributes to the switching device current, both as an increased current [2] at turn on and as a reduced current during the voltage rise at turn off. This effect is in addition to that discussed previously for the parasitic PCB switch-node capacitance. In both cases, the energy retained in the capacitance during turn-off is subsequently lost in the switching device at turn-on.

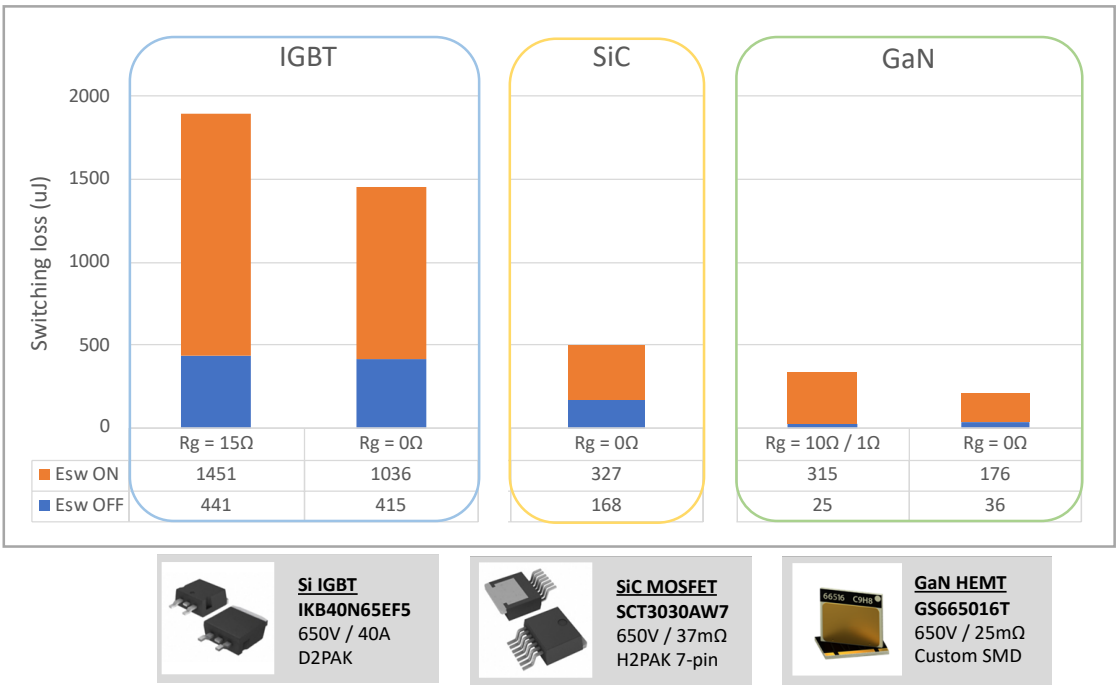


Figure 7: Switching loss comparison using experimental test results. The tests were all carried out at 100 °C, with both manufacturer recommended gate resistances and zero-ohms. The Rg value shown here is an externally fitted gate resistor. The gate-driver and switching device have their own internal resistance that is not indicated here or changed during these tests. The on-state resistances indicated here are from the manufacturer's datasheets (at 25 °C). Comparable on-state channel resistance is achieved in all three devices at 100 °C. GaN and Silicon on-state channel resistances change significantly with temperature, whereas SiC does not. The SiC MOSFET datasheet recommends zero-ohm external gate resistance.

When considering the SCCL inductance, this also affects the waveforms, as noted in the waveforms for turn on, and acts as a turn on snubber. Therefore, the use of higher values of stray inductance, as found in the datasheets, is likely to reduce the turn on losses and in concert with the capacitances may reduce the overall losses.

Clearly, it is extremely difficult for the device manufacturers to fully parameterise their simulation models and perform extensive testing, including the many conditions that could be seen in the field, in terms of board layout and parasitic elements. Device users also have some difficulty parameterising their circuits as it requires accurate measurements of very small inductances and capacitances.

In the case of the SiC MOSFET, considerable effort has been made by the manufacturer to provide E_{ON} and E_{OFF} curves against current, providing the user with a degree of confidence. The SiC device waveforms also have 'textbook' MOSFET features, which result from the structure being directly extrapolated from the classic power MOSFET. Furthermore, the high internal gate resistance helps with the modelling, as very fast switching is impossible to achieve (in contrast to the GaN HEMT device).

The IGBT simulation and extrapolation is known to be challenging regarding losses due to the internal stored charge, and only models which account for this in a careful manner can achieve good accuracy. Indeed, IGBT circuit simulations also need an excellent diode model [8], given the significant diode recovery time seen here in *Figure 5 (c)*. Indeed, as it appears diode behaviour is a major limiting factor on IGBT performance it may be anticipated that a SiC Schottky diode could be co-packaged with the Si IGBT die to achieve significant improvements in overall performance.

Regarding the GaN HEMT device, the authors believe that the gate drive circuit is now the limiting factor in this design. A further speed-up may be possible if this were to be improved. The GaN device also offers remarkably clean switching waveforms, most likely due to low gate-to-drain capacitance and very low inductance package. This low capacitance results in negligible ringing, and the corresponding gate-to-source capacitance of the GaN HEMT indicates there is little danger of shoot-through currents due to Miller switch-on effects.

A summary of the experimental results is given in *Figure 7*, and shows a comparison of switching energy losses between the three different devices.

8 Conclusions

The experimental assessment of the switching performance for three comparable devices reveals the state of the commercial 650 V power device market in early-2022. In summary:

1. The GaN HEMT and IGBT devices show a significant decrease in switching energy losses with zero-ohm gate resistance, compared to manufacturer recommended gate resistance. Particularly, the GaN switching losses are reduced by one-third (and this may be reduced further with a different driver). However, reliable operation with zero-ohm gate resistance is only possible because of the ultra-low inductance circuit design used for these tests.
2. The GaN and SiC devices offer much lower switching losses compared to the Si IGBT. The GaN HEMT can achieve about half the switching losses of the SiC MOSFET.
3. The Si IGBT switch-on current peak due to the Q_{RR} reverse-recovery of the opposing silicon diode, and translates into higher switching losses, particularly at 100 ^{o}C; the diode appears to be the limiting factor on IGBT performance.
4. The SiC MOSFET device offers good switching performance, but speed appears is limited by the high internal gate resistance.
5. Shoot-through current should not be expected in well a crafted GaN circuit, even when switching at around twice the datasheet voltage and current slew rates. The GaN HEMT has been shown here to have an exemplary diode-like reverse conduction and fast, low loss switching in hard-switched half-bridge circuits.

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9 References

[1] International Rectifier application note AN-1001 “A More Realistic Characterization of Power MOSFET Output Capacitance Coss”, published 1999.

[2] Shelton, Edward, et al. "Low inductance switching for SiC MOSFET based power circuit." 2017 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 2017.

[3] Shelton, Edward, et al. "Design and measurement considerations for WBG switching circuits." 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe). IEEE.

[4] Palmer, Patrick, et al. "An experimental comparison of GaN, SiC and Si switching power devices." IECON 2017-43rd Annual Conference of the IEEE Industrial Electronics Society. IEEE, 2017.

[5] Shelton, Edward, et al. “Comparison of Fast Switching High Current Power Devices” PCIM 2021.

[6] Vishay application note AN608A “Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance”, published 2016.

[7] Yang. X, et al., “An Improved Fourier-Series-Based IGBT Model by Mitigating the Effect of Gibbs Phenomenon at Turn on”, IEEE Transactions on Electron Devices, Volume: 68, Issue: 7, July 2021

[8] Bryant, A.T., et al. “A Compact Diode Model for the Simulation of Fast Power Diodes including the Effects of Avalanche and Carrier Lifetime Zoning”, IEEE 36th PESC Conference, June 2005

[9] Siliconix, Vishay. "Power MOSFET basics: Understanding gate charge and using it to assess switching performance." Application Note (2016).