

Silicon-on-Insulator Membrane SIS Mixers for Africa Millimeter Telescope Band 6+7 Operation

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Abstract—We present the design, simulation, fabrication, and initial characterization efforts toward a broadband superconductor-insulator-superconductor (SIS) mixer covering ALMA Bands 6 and 7 (211–373 GHz) on a single chip. The mixer employs a twin-junction SIS architecture integrated on a 10 μm -thick silicon-on-insulator (SOI) membrane substrate and is intended as a building block for future sideband-separating and dual-polarization receivers. To support the fabrication of these devices, front-side SIS circuit processing, SOI membrane release techniques, and gold beam-lead integration have been developed and refined. Initial device-release trials have successfully produced mixer chips with intact membranes and beam leads, while experimental setup for cryogenic mixer characterization has also been completed.

Index Terms—Millimeter and sub-millimeter, heterodyne receiver, silicon-on-insulator, superconductor-insulator-superconductor mixer, nano-fabrication, deep reactive ion etching

I. INTRODUCTION

Almost all deployed millimeter- and sub-millimeter (mm/sub-mm) wave telescopes, such as the Atacama Large Millimeter/submillimeter Array (ALMA, [1]) and the Herschel Space Telescope [2], employ superconductor-insulator-superconductor (SIS) receivers to perform high-spectral-resolution observations below 1.5 THz. Although these established astronomical observatories have been conducting highly successful observation campaigns and producing significant scientific results, there is a strong desire to further improve the performance of SIS receivers to enable even more ambitious science goals. One example is ALMA's Wideband Sensitivity Upgrade (WSU) program [1], which aims to broaden the intermediate-frequency (IF) bandwidths of the heterodyne receivers. Furthermore, upcoming mm/sub-mm telescopes, such as the Africa Millimetre Telescope (AMT, [3]) and the Atacama Large Aperture Synthesis Telescope (AtLAST, [4]), are expected to be equipped with the next generation of heterodyne instruments offering improved performance. One such advancement is the capability for ultra-broad radio-frequency (RF) observations.

In this manuscript, we describe our effort to combine adjacent ALMA-defined bands on a single SIS mixer chip.

In particular, we focus on a Band 6+7 mixer, which has immediate applications for the planned expansion of the Event Horizon Telescope (EHT, [5]) network through the construction of the AMT station in Namibia.

II. MIXER DESIGN

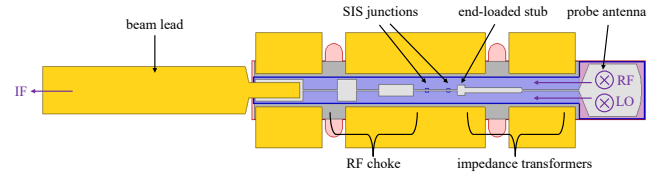


Fig. 1. Layout of the B6+7 DSB SIS mixer comprising a pair of tunnel junctions. The RF and LO signals are coupled to the chip via a probe antenna positioned across the cross section of a full-height rectangular waveguide. The down-converted IF signal is coupled to the IF matching board (not shown) through a gold beam lead.

Fig. 1 shows the layout of a double-sideband (DSB) SIS mixer design targeting ALMA Bands 6+7 (B6+7: 211–373 GHz), forming the basis of the mixer chips required for subsequent sideband-separating (2SB) and/or dual-polarization (dual-pol) configurations. The choice of these particular bands is motivated by the AMT's need to perform simultaneous observations in both bands. Consequently, the same receiver design can be readily duplicated to provide this simultaneous observing capability.

A detailed description of the mixer design has been presented previously [6]. Here, we briefly summarize the methodology for completeness. Our mixers employ 1 μm^2 Nb/AlOx-Al/Nb junctions with a critical current density of $J_C = 8\text{--}10 \text{ kA/cm}^2$, a normal resistance of $R_N = 20 \Omega \cdot \mu\text{m}^2$, and a capacitance of $C_J = 80 \text{ fF}/\mu\text{m}^2$. To achieve broad RF operation, we make use of the twin-junction architecture [7], comprising a pair of near-identical tunnel junctions separated by a short microstrip transmission line that tunes out the parasitic junction capacitance, which would otherwise short high-frequency RF signals.

A top-down rectangular waveguide guides the radio-frequency (RF) and local-oscillator (LO) signals to a probe antenna, aligned such that the flat surface of the antenna is perpendicular to the propagation direction of the incoming RF waves carried by the waveguide. This configuration readily facilitates future implementation in 2SB and dual-pol receiver architectures.

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The remaining on-chip RF circuitry uses microstrip transmission lines. We match the impedance of the probe antenna to that of the SIS junctions using a two-step Chebyshev transformer, followed by an RF choke that acts as a low-pass filter to minimize RF and LO leakage into the IF circuit. An end-loaded stub at the end of the Chebyshev transformer enables tuning of the mixer chip across the desired operating bandwidth. With this basic layout in place, we optimize the dimensions of the on-chip circuit components using Ansys® High Frequency Structure Simulator (HFSS) to achieve optimal performance across the target bandwidth.

III. MIXER SIMULATIONS

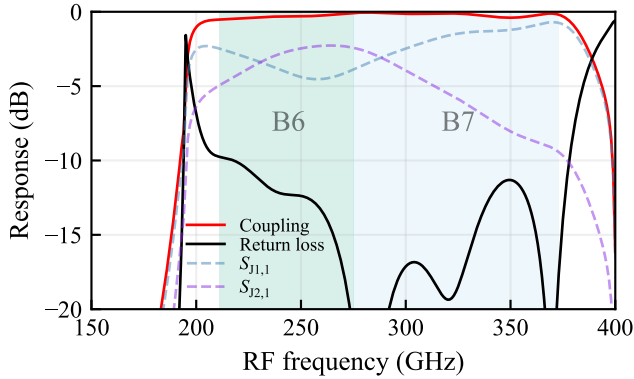


Fig. 2. The predicted RF performance of the B6+7 twin junction design, as simulated in Ansys HFSS. The coupling to each junction is shown in dashed lines, and the total RF coupling is in solid red. The return loss is represented with a solid black line.

The predicted scattering-parameter performance of the Band 6+7 mixer is shown in Fig. 2. The return loss is maintained below -10 dB across both the Band 6 and Band 7 frequency ranges, corresponding to an RF bandwidth of 55.5%. This bandwidth is considerably broader than the $\sim 26\%$ bandwidth of the current ALMA receivers. The total RF power coupled to both junctions is also close to 0 dB across the entire frequency range. The predicted heterodyne performance is presented in the following section.

A. IF considerations and receiver performance

The RF and IF heterodyne performance of the presented mixer chip is simulated using a combination of HFSS and the quantum mixing simulation code SuperMix [8]. To extend the IF bandwidth (IFBW), we incorporate a six-step Chebyshev transformer board, shown in Fig. 3, fabricated using Rogers Duroid® RO3210 material and placed directly after the mixer chip [9], [10]. The IF board was designed to achieve a 16 GHz IFBW for the presented mixer chip.

To illustrate the anticipated RF performance of the mixer, we present the receiver performance for fixed LO tuning frequencies and the anticipated IF operational bandwidth, rather than plotting the RF heterodyne performance directly (i.e., assuming an infinitesimally small IF bandwidth). Fig. 3 shows the predicted noise-temperature performance of the complete

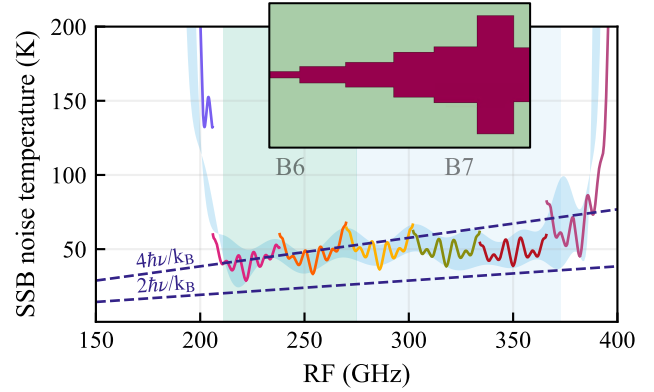


Fig. 3. The 2SB noise temperature performance of the B6+7 design with a 16 GHz impedance-matched IF transformer board (shown in the overlaid frame). The filled regions in each plot refer to the general range of noise temperatures the receiver can be expected to perform at, depending on the LO tuning. The receiver noise temperature includes contributions from the low noise amplifier (3.5 K), optics (3%), and mixer chip itself. In solid lines are the noise temperature performances for individual LO tunings. We show multiples of the quantum noise limit in dashed lines for reference. The LO tunings sit at the center of each colored line, with each sideband extending to either side. The effects of passive components combining or splitting signals are not included here.

2SB receiver. In simulation, the DSB mixer components are duplicated and process each sideband separately. We do not account for the effects or losses from passive components splitting or combining signals. We assume a 3% loss in the room-temperature optical components and a cryogenic low-noise-amplifier (LNA) noise contribution of 3.5 K. The shaded blue region is bounded by the approximate maximum and minimum noise temperatures across the RF bandwidth, depending on the LO tuning frequency. The colored curves demonstrate that the entire Band 6+7 frequency range can be covered within approximately four times the quantum noise limit using only six to seven LO tuning settings.

IV. NANO-FABRICATION PROCESS

The presented mixer design is intended to be fabricated using silicon-on-insulator (SOI) substrate technology instead of the more commonly used quartz, sapphire, or high-resistivity silicon substrates, owing to its mechanical and electromagnetic advantages over conventional thick substrates [11]. SOI technology also enables the fabrication of irregular chip geometries, including the semicircular alignment tabs incorporated in our design (see Fig. 1). However, the use of an SOI substrate introduces additional complexity to the device fabrication process, as discussed below.

For the mixer design presented in this manuscript, we employ a 10 μm -thick SOI substrate. As shown in Fig. 1, we also incorporate gold beam-lead technology alongside the SOI membrane technology to simplify device mounting, improve thermal contact, and minimize parasitic effects associated with traditional wire bonds. These gold beam leads are deposited around the edges of the mixer chip to form the grounding path, while a separate elongated beam lead is incorporated at the end of the mixer chip to couple the down-converted IF output to the IF transformer board. Again, the use of

beam-lead technology in conjunction with the SOI membrane increases the complexity of device fabrication compared with conventional quartz or silicon substrates.

A. Front-side mixer circuit fabrication

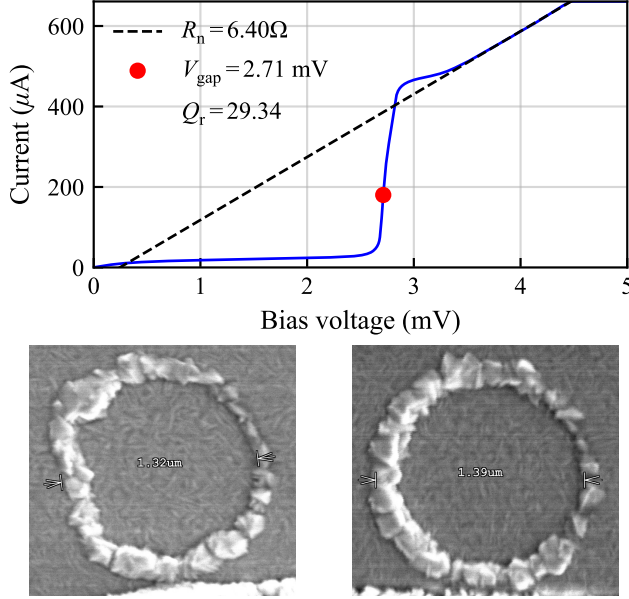


Fig. 4. *Top*: The measured IV curve for an example of a B6+7 twin junction device with $1.5 \mu\text{m}^2$ junctions. The smoothed and corrected curve is shown in solid blue. The measured normal resistance is fitted with a dashed black line. We mark the calculated gap voltage with a red marker. The plot shown that we have achieved a critical current density of 14 kAcm^2 with a quality factor $Q_r = R_N/R_{\text{subgap}} = 29$. *Bottom*: SEM images of the twin junctions.

Before delving into the intricacies of processing SOI devices with deposited gold beam leads, we first needed to demonstrate that standard Nb-junction mixer circuits could be successfully fabricated on these membranes. We have since refined our front-side fabrication recipe and screening procedures to produce wafers with a high device yield. To date, we have fabricated 15 batches of SOI wafers, primarily varying the Al oxidation time and photoresist processing procedure to achieve the target critical current density. For each batch, we bias multiple devices (located within a small subsection of the wafer) and measure their IV characteristics at 4 K to assess the quality of the fabricated tunnel junctions.

An example of a recently tested B6+7 device is shown in the upper panel of Fig. 4. This device was intentionally fabricated with a larger-than-design junction area of $1.5 \mu\text{m}^2$. To expedite the analysis, we use the QMix package [12], [13] to smooth the measured IV curves and extract key figures of merit, such as the gap voltage and normal-state resistance.

B. Back-side mixer chip processing

Successful fabrication of an SIS mixer circuit on an unprocessed SOI substrate represents only the first half of the challenge. The second half involves successfully releasing these membrane devices from the bulk wafer, which consists

of a thick silicon handle layer and an intermediate buried oxide (BOX) layer.

Our initial approach follows conventional SOI backside-processing techniques [11], [14]. First, the SOI wafer is bonded to a carrier wafer, after which the handle layer is thinned by polishing it from 450 to $100 \mu\text{m}$. Deep reactive ion etching (DRIE) is then used to remove the remaining handle layer down to the BOX layer. As our laboratory does not possess a DRIE system, this step was performed in collaboration with an external facility. After patterning the exposed BOX layer with photoresist to define the desired chip geometry, we etched through both the BOX layer and the device layer (i.e., the membrane), stopping at the beam-lead interface.

Concurrently, we are also exploring an alternative method for releasing SOI chips from the bulk wafer without the need for a DRIE system. The details of this process are beyond the scope of the present manuscript. Briefly, we are investigating a wet-etching approach using potassium hydroxide (KOH) as the etchant to replace the DRIE process.

V. RELEASED SOI MIXER CHIPS

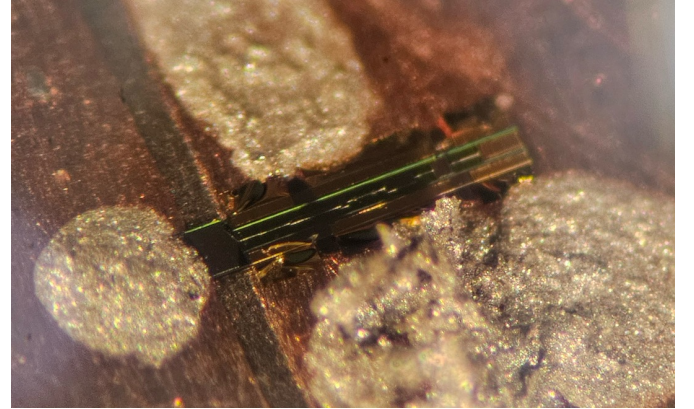


Fig. 5. The device mounted to a biasing board with conductive silver paint and bonded gold beam leads.

To date, using the conventional SOI device-release process described above, the first of two release attempts (at the time of writing) resulted in cracks in the silicon membrane and was therefore deemed unusable. The second attempt, however, achieved partial success. Of the 10 released chips, two mixer chips retained all required ground and IF beam leads, while the remaining devices preserved only part of the vulnerable gold beam leads, particularly the grounding but not the IF-connection beam lead.

For all devices, we successfully achieved the target membrane thickness of $\sim 10 \mu\text{m}$, and the intended chip geometry was clearly defined. We believe that microscopic cracks in the silicon, introduced during an imperfect polishing process, may have caused the gold beam leads to fracture. However, further investigation is required to confirm this hypothesis.

With these released chips, preliminary IV measurements are currently underway to verify that the quality of the tunnel junctions remains well preserved after the aggressive backside

processing. To reduce risk and preserve the fully intact SOI devices for subsequent mixer characterization, we initially mounted chips with partially missing beam leads onto a biasing board for these tests.

This exercise also provides an opportunity to explore optimal techniques for handling and mounting these ultra-thin and fragile devices. As shown in Fig. 5, we found that the most effective procedure is to secure the chips with a small amount of crystal bond and then apply small dabs of conductive silver paint to establish both mechanical and electrical connections between the chip and the board. The gold beam leads are subsequently pressed onto the board using a manual wire bonder (without wire) to ensure good electrical contact.

VI. EXPERIMENTAL SETUP

In parallel with refining the SOI device-release and mounting processes, we have prepared the experimental setup for characterizing these broadband SIS mixer chips. We finalized the design of the mixer block, as shown in Fig. 6. The RF and LO signals are directed into the block through a rectangular waveguide. The circular recess surrounding the rectangular waveguide forms the interface required to accommodate the feed horn with a WR4 Flann UG387/U flange.

The magnetic field required to suppress unwanted Cooper-pair tunneling is applied to the junctions using a coil mounted on the left side of the block. The coil current can be controlled externally using a dedicated current supply. The IF signal is routed through the PCB-based IF board within the block and is extracted through an SMA connector, shown on the right side of Fig. 6, for transmission to the remainder of the IF chain.

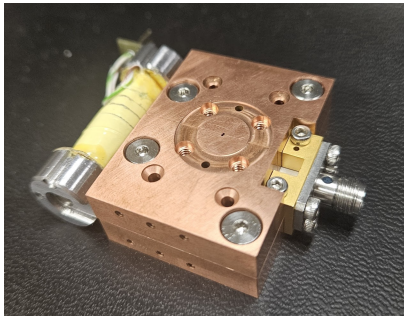


Fig. 6. The mixer block housing individual B6+7 mixer chips. A magnetic coil is set on the left side, and the SMA output on the right side directs the mixer output to the rest of the IF chain.

For full device characterization and noise-temperature measurements, the mixer block will be mounted in a cryostat dedicated to SIS mixer experiments.

VII. CONCLUSIONS

We have presented the design and development of a broadband ALMA Band 6+7 SIS mixer based on a twin-junction architecture fabricated on an SOI membrane substrate. Simulations predict good RF coupling across 211–373 GHz and indicate that the receiver can achieve low noise temperatures over the full operating bandwidth with a limited number of LO tuning settings. In parallel with the mixer design

effort, fabrication processes for SOI membrane devices and integrated gold beam leads have been established, resulting in the successful release of several mixer chips. Experimental infrastructure, including a dedicated mixer block and cryogenic test facility, has also been prepared for device characterization. Ongoing work focuses on DC-IV curve characterisation of the released devices and subsequent heterodyne measurements.

REFERENCES

- [1] J. Carpenter, C. Brogan, D. Iono, and T. Mroczkowski, "The ALMA Wideband Sensitivity Upgrade," in *Physics and Chemistry of Star Formation: The Dynamical ISM Across Time and Spatial Scales*, V. Ossenkopf-Okada, R. Schaaf, I. Breloy, and J. Stutzki, Eds., Feb. 2023, p. 304.
- [2] A. Karpov, D. Miller, F. Rice, J. A. Stern, B. Bumble, H. G. LeDuc, and J. Zmuidzinas, "Development of 1.25 THz SIS mixer for Herschel Space Observatory," in *Millimeter and Submillimeter Detectors and Instrumentation for Astronomy III*, J. Zmuidzinas, W. S. Holland, S. Withington, and W. D. Duncan, Eds., vol. 6275, International Society for Optics and Photonics. SPIE, 2006, p. 62751U. [Online]. Available: <https://doi.org/10.1117/12.684534>
- [3] M. Backes, C. Müller, J. E. Conway, R. Deane, R. Evans, H. Falcke, R. Fraga-Encinas, C. Goddi, M. Klein Wolt, T. P. Krichbaum, G. MacLeod, V. A. R. M. Ribeiro, F. Roelofs, Z. Q. Shen, and H. J. van Langevelde, "The Africa Millimetre Telescope," in *The 4th Annual Conference on High Energy Astrophysics in Southern Africa (HEASA 2016)*, Jan. 2016, p. 29.
- [4] P. D. Klaassen, T. K. Mroczkowski, C. Cicone, E. Hatziminaoglou, S. Sartori, C. D. Breuck, S. Bryan, S. R. Dicker, C. Duran, C. Groppi, H. Kaercher, R. Kawabe, K. Kohno, and J. Geach, "The Atacama Large Aperture Submillimeter Telescope (ALAST)," in *Ground-based and Airborne Telescopes VIII*, H. K. Marshall, J. Spyromilio, and T. Usuda, Eds., vol. 11445, International Society for Optics and Photonics. SPIE, 2020, p. 114452F. [Online]. Available: <https://doi.org/10.1117/12.2561315>
- [5] A. W. Raymond, D. Palumbo, S. N. Paine, L. Blackburn, R. Córdova Rosado, S. S. Doeleman, J. R. Farah, M. D. Johnson, F. Roelofs, R. P. J. Tilanus, and J. Weintraub, "Evaluation of New Submillimeter VLBI Sites for the Event Horizon Telescope," *Astrophys. J.*, vol. 253, no. 1, p. 5, Mar. 2021.
- [6] J.-H. Kim, F. Boussaha, C. Chaumont, A. Baryshev, and B.-K. Tan, "Band-combining sis mixer designs for the africa millimetre telescope." National Radio Astronomy Observatory, 2025.
- [7] J. Zmuidzinas, H. G. Leduc, J. A. Stern, and S. R. Cypher, "Two-junction tuning circuits for submillimeter SIS mixers," *IEEE Transactions on Microwave Theory Techniques*, vol. 42, no. 4, pp. 698–706, Apr. 1994.
- [8] J. Ward, F. Rice, G. Chattopadhyay, and J. Zmuidzinas, "SuperMix: A Flexible Software Library for High-Frequency Circuit Simulation, Including SIS Mixers And Superconducting Elements," in *Tenth International Symposium on Space Terahertz Technology*, T. W. Crowe and R. M. Weikle, Eds., Mar. 1999, p. 268.
- [9] B.-K. Tan, G. Yassin, and P. Grimes, "Ultra-wide intermediate bandwidth for high-frequency sis mixers," *IEEE Transactions on Terahertz Science and Technology*, vol. 4, no. 2, pp. 165–170, 2014.
- [10] J. Garrett, "A 230 GHz Focal Plane Array Using a Wide IF Bandwidth SIS Receiver," Ph.D. dissertation, University of Oxford, UK, 2018.
- [11] N. Scott Barker, M. Bauwens, A. Lichtenberger, and R. Weikle, "Silicon-on-insulator substrates as a micromachining platform for advanced terahertz circuits," *Proceedings of the IEEE*, vol. 105, no. 6, pp. 1105–1120, 2017.
- [12] J. D. Garrett and G. Yassin, "QMIX: A Python package for simulating the quasiparticle tunneling currents in SIS junctions," vol. 4, no. 35, p. 1231, Mar. 2019. [Online]. Available: <https://doi.org/10.21105/joss.01231>
- [13] J. D. Garrett, B.-K. Tan, F. Boussaha, C. Chaumont, and G. Yassin, "Simulating the Behavior of a 230-GHz SIS Mixer Using Multitone Spectral Domain Analysis," vol. 9, no. 6, pp. 540–548, Nov. 2019. [Online]. Available: <https://ieeexplore.ieee.org/document/8822760/>
- [14] A. B. Kaul, B. Bumble, K. A. Lee, H. G. LeDuc, F. Rice, and J. Zmuidzinas, "Fabrication of wide-if 200–300ghz superconductor-insulator-superconductor mixers with suspended metal beam leads formed on silicon-on-insulator," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 22, no. 5, p. 2417–2422, 08 2004.