# Study of *Mixed Mode* electro-optical operation of $Ge_2Sb_2Te_5$


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*Dedicado a mis padres, Gerardo y María Cristina*

# DECLARATION

This thesis is the result of my own work and includes nothing, which is the outcome of work done in collaboration except where specifically indicated. It has not been previously submitted, in part or whole, to any university of institution for any degree, diploma, or other qualification.

In accordance with the Department of Materials guidelines, this thesis does not exceed 40,000 words.

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# ABSTRACT

Chalcogenide based Phase Change Materials are currently of great technological interest in the growing field of optoelectronics. $Ge_2Sb_2Te_5$ (GST) is the most widely studied phase change material, and it has been commercially used in both optical and electronic data storage applications, due to its ability to switch between two different atomic configurations, at high speed and with low power consumption, as well as its high optical and electrical contrast between amorphous and crystalline states. Despite its well-known optical and electrical properties, the operation in combination of optical and electrical domains has not yet been fully investigated.

This work studies the operation of GST nano-devices exposed to a combination of optical and electrical stimuli or *mixed mode* by asking, is it possible to electrically measure an optically induced phase change, or vice versa? If so, how do the optical and electrical responses relate to each other, and is it possible to operate GST with a combination of optical and electrical signals? What are the technical constraints that need to be considered in order to fabricate GST devices that could be operated either optically or electrically?

In order to answer these questions, experiments that characterized the optical and electrical responses of GST based nano-devices were performed. It was found that different crystallization mechanisms may have influence in the response, and that the thermal and optical design characteristics of the device play a key role in its operation. Finally a proof of principle, of an opto-electonic memory device that can be read electrically, reset optically and write electrically, is presented. This opens up possibilities for the development of new opto-eloectronic applications such as non-volatile interfaces between future photonics and electronics, high speed optical communication detectors, high speed cameras, artificial retinas and many more.

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# LIST OF ABBREVIATIONS AND ACRONYMS

ADC: Analog to Digital Converter

AFM: Atomic Force Microscope

CMOS: Complementary metal–oxide–semiconductor

FR-4: Fire Retardant 4

GST: $Ge_2Sb_2Te_5$

GRIN: Gradient Refractive Index lens

IPA: Isopropyl alcohol, Isopropanol

ITO: Indium Tin Oxide

I/V: Current / Voltage

LVDT: Low Voltage Differential Transformer

MEK: Methyl ethyl ketone

MIBK: Methyl isobutyl ketone

NSOM/SNOM: Near-field Scanning Optical Microscopy

PCM: Phase Change Memory

PMMA: Polymethyl methacrylate

PSF: Point Spread Function

PZT: Lead Zirconate Titanate

RF: Radio Frequency

RIE: Reactive Ion Etching

SEM: Scanning Electron Microscope

STDP: Spike Time Dependant Plasticity

TEM: Transmission Electron Microscope

XAFS:X-Ray Absorption Fine Structure

XANES: X-Ray Absorption Near Edge Structure

XRD: X-Ray Diffraction

# 1 INTRODUCTION

The highly technological world we live in keeps progressing at a constantly increasing speed. Since the end of the 20th century, information technologies have been the main driver of innovation by providing novel tools for data analysis as well as connectivity. The advance in the use of such technologies depends on an increasing supply of computational power and communications bandwidth. Moore's law predicted in 1975 that the number of components per integrated circuit doubles every 18 months[1]. This means that the level of integration in electronics is just a couple of generations away from reaching the atomic limit. At the same time, micro-processor clock speeds as well as data transfer rates have reached a plateau. The combination of these circumstances has motivated the search for new technologies that could satisfy the computing demands of the near future.

Different approaches to tackling these problems have emerged, but two of them have attracted attention by showing real potential. Firstly the development of Non-Von-Neumann computer architectures and secondly the increasing use of photonics in high speed processing and communications. The development of the former depends on the creation of new components capable of integrating memory and processing capabilities

to overcome the so-called Von-Neumann bottle neck [2]. The creation of such new components in turn, depends on new materials capable of having multiple levels of non-volatile memory. Likewise, the advance of photonics processing also depends on the development of new materials with the required optical properties, in particular a tuneable refractive index. One group of materials with the potential to fulfil these criteria are the chalcogenide based *phase change materials*.

Chalcogenide glasses are compounds made up of an element from the chalcogen group (Sulphur, Selenium and Tellurium, with the exception of Oxygen) combined with an element that enhances network formation (As, Ge, Sb, Ga, Si or P) [3]. Chalcogenide-based phase change materials have been the subject of scientific interest since Ovshinksy observed electronic switching behaviour and memory effect in a thin film of a chalcogenide compound in the 1960's [4]. To date, research into phase change materials has shown that due to their unique phase transformation dynamics, they are able to reversibly switch between two different atomic configurations or phases (amorphous and crystalline) for many cycles at high speed and with low power consumption, making them ideal for data storage technologies.

During the last three decades there has been a significant interest in finding the most suitable material for data storage applications. Such applications require high switching speeds and reduced power consumption. Figure 1 shows different ternary compounds used in the evolution of optical data storage technology. To date the one of the most broadly studied phase change materials is $Ge_2Sb_2Te_5$ (GST). It was originally developed as the active material for high speed non-volatile optical data storage media (DVD-RAM) because the difference in reflectivity between amorphous and crystalline phases allowed the storage of optically distinguishable bits of information by writing dots in an optical disk [5][6] at high speeds.

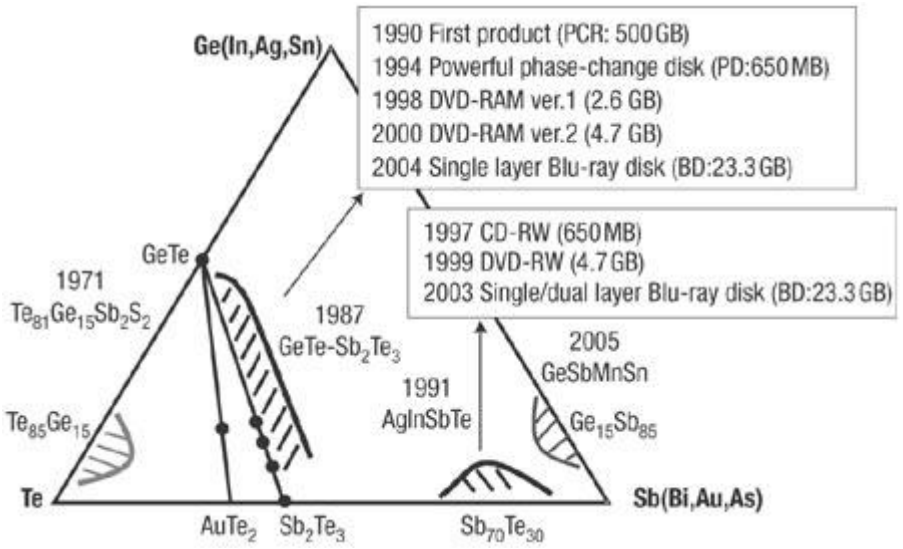


**Figure 1 Phase Change Material ternary compounds explored for optical data storage. Reprinted by permission from Macmillan Publishers Ltd. Nature Materials 6, 824 - 832 (2007), copyright 2007.**

Subsequently, GST has also been used in electronic phase change memories (PCM)[7][8] because, in addition to the change in reflectivity, GST experiences a change in electrical resistivity between the amorphous and crystalline phases. Recently, PCM's have been considered as a potential replacement for non-volatile solid state memories, succeeding flash memory technology [9]. The technological relevance of GST has attracted the interest of the scientific community, which has studied the origin of the switching mechanism that gives GST its remarkable properties. In this thesis GST was used due mainly to two reasons, primarily it is a recognized and widely studied material, which makes it an ideal candidate for a bench mark study case in the exploration of new applications, and secondly because it was easily accessible.

## 1.1 $Ge_2Sb_2Te_5$ Phase Change Material

Analytical studies using Differential Scanning Calorimetry (DSC) and X-Ray Diffraction (XRD) data, have shown that GST has three atomic configurations or phases; amorphous, metastable rock salt (face center cubic, fcc) and hexagonal [8]. Each phase possesses different optical and electrical properties [10], with three orders of magnitude difference in resistance between the amorphous and crystalline states (kΩ– MΩ), which makes it ideal for electrical memory. The technologically important transition is between the rock salt and amorphous phases, because of the speed of this transition and the high optical and electrical contrast between these two phases. For instance, a GST optical media with 20% reflectivity contrast between amorphous phase and crystalline fcc has been reported to amorphize in 1ns and crystalize in 13ns [11].

GST is a p-type semiconductor [12], with 20% vacancies in the crystalline state [5]. It exhibits high endurance of up to $10^{12}$ cycles [13], can remain in any specific state for over 10 years at room temperature [14], and it is compatible with CMOS standard manufacturing processes [15]. It also requires low switching power; recent research has shown experimentally devices which operate at powers of the order of 100 femto-Joules [16].

GST-based electronic PCM has been commercialized by Numonyx (now part of Micron Technology Inc.) and Samsung Electronics and is currently under active research by Intel, ST microelectronics and IBM among others. Nonetheless, the study of the material properties and the switching mechanism of GST, as well as the exploration of new applications, are still areas of active research.

## 1.2 Switching Mechanisms

### 1.2.1 Optical switching

Optical switching is the basis of current rewritable optical data storage technology. It has also provided a mechanism to study the properties of GST and represents a source of potential new applications in photonics.

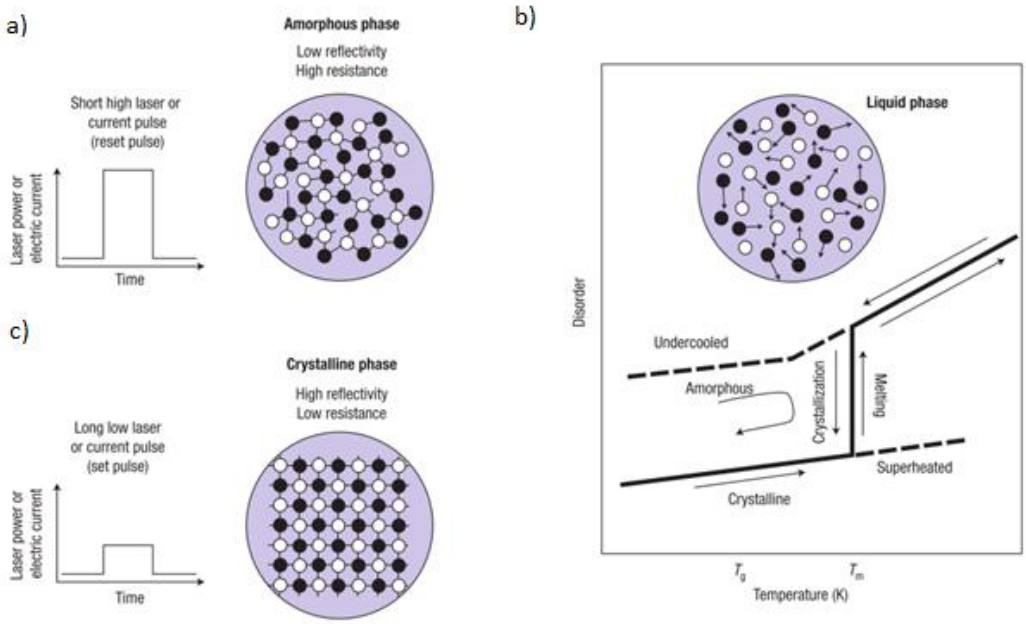


**Figure 2 Traditional thermal switching mechanism of phase change materials. "a) A short pulse of a focused, high-intensity laser beam locally heats the phase change material above its melting temperature. b) Rapidly cooling at rates higher than $10^9$K/s quenches the liquid state into a disordered, amorphous phase. c) To induce crystallization, a laser pulse with intermediate power is used. The laser locally heats the phase change material above the crystallization temperature. At temperatures above $T_g$ the atoms become increasingly mobile and can rearrange to the energetically favourable crystalline state"** [17]**. Reprinted by permission from Macmillan Publishers Ltd. Nature Materials 6, 824 - 832 (2007), copyright 2007.**

The switching mechanism for optically-induced phase change is based on the exposure to localized heat in the form of a laser pulse, is described in Figure 2. Based on early studies [18], it has been assumed that to induce the phase change from amorphous to crystalline state it is required to apply a laser pulse with the correct fluence to heat up the material above the glass transition temperature ($T_g$). On the other hand, to transform it from crystalline to the amorphous phase, a different pulse is applied such that it heats the material above the melting temperature ($T_m$). The molten material is then super-cooled by thermal diffusion thorough the substrate, and the liquid phase disorder is retained in the amorphous phase after the thermal quench [17].

#### 1.2.1.1 Early Characterization Experiments

What makes GST interesting is the fast crystallisation speed in comparison to other materials. Differential scanning calorimetry experiments have identified GST as a marginal glass former with a small reduced glass transition temperature ($T_g/T_m$) and high fragility[19]. These properties have been presented as the reasons for the fast crystallization and amorphization characteristics of GST. A small reduced glass transition temperature implies that the crystallization occurs rapidly at high temperature [17], as can be seen in Figure 3. Fast crystallization is assisted by the high fragility via crystal growth [20]. During amorphization, the molten GST is thermally quenched at a high rate of $10^{10}$ K/s; due to the high fragility, the material becomes increasingly rigid as the temperature decreases. Once the glass transition temperature $T_g$ is passed, crystallisation has been avoided due to reduced atomic mobility inhibiting structural reorganization [20]. Since amorphization depends on a high rate thermal quenching, the heat dissipation characteristics of the underlying substrate are important in the optimization of switching speed [11].

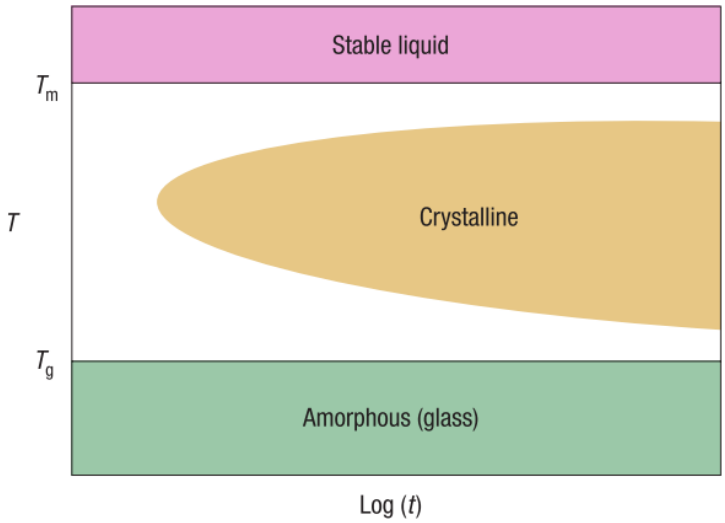


**Figure 3 "Time-temperature-transformation diagram of an undercooled liquid. t = time, $T_m$ = melting temperature, $T_g$ = glass transition temperature. The crystalline region depicts schematically that the minimum time for crystallization strongly depends on temperature"**[17]**. Reprinted by permission from Macmillan Publishers Ltd. Nature Materials 6, 824 - 832, copyright 2007.**

1.2.1.2 Further studies about the atomic structure.

Studies of the phase change phenomena mentioned so far are based on the classic kinetics theory proposed by Turnbull [17]. However, later studies have focused on the analysis of the atomic structure for better understanding about the nature of the phase transformation of GST.

A work presented by Kolobov *et al* [21] analysed X-ray absorption fine-structure spectroscopy (XAFS) measurements of GST, and proposed a model for the atomic structure that can provide an explanation for GST switching properties. According to this model [21], the atomic structure of GST is composed of a periodic set of atoms in the sequence Sb-Te-Ge-Te-Te-Ge-Te-Sb-Te (Figure 4).

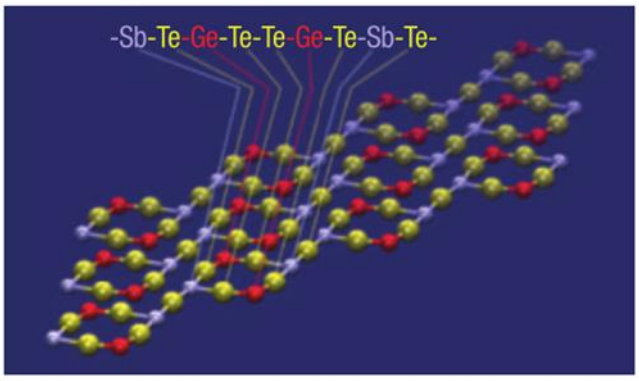


**Figure 4 Sematic of the -Sb-Te-Ge-Te-Te-Ge-Te-Sb-Te- building block proposed by the Kolobov model. Reproduced by permission from Macmillan Publishers Ltd. Nature Materials 3, 703 -708, copyright 2004.**

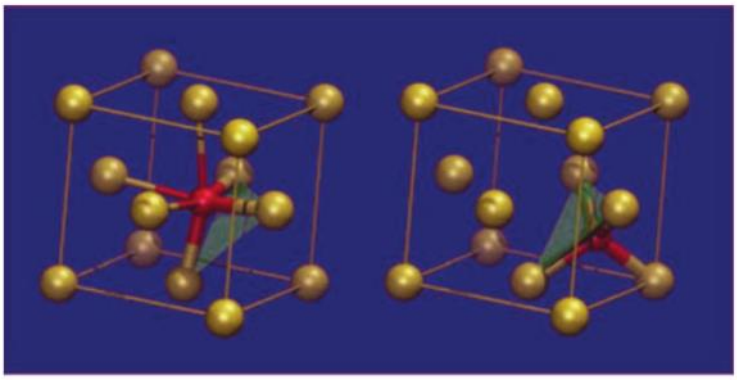

**Figure 5 Umbrella flip effect. The Tellurium atoms (big spheres) form a rock salt sub-lattice. The Germanium atom (small sphere) shifts from the tetrahedral position (left) to the octahedral position (right). (Sb atoms are not shown). Reproduced by permission from Macmillan Publishers Ltd. Nature Materials 3, 703 -708, copyright 2004.**

The stacking of this sequence generates a rock salt sub-lattice formed by covalently bonded Te atoms; this Te sub-lattice remains unchanged in both amorphous and crystalline phases. During the crystalline to amorphous transition, the Ge atoms migrate from an octahedral to a tetrahedral configuration named by the authors as *umbrella flip*

(Figure 5). Throughout this change, the strong covalent bonds of Ge to Te are maintained, implying that only weaker resonant bonds between Ge and Sb atoms are required to break in order to induce a structural change. This suggests that the change could be achieved just by electronic excitation without the need for melting. Therefore, the optical pulse itself could excite charge carriers, softening the lattice and inducing a collapse of the crystalline structure without necessarily passing by the liquid phase.

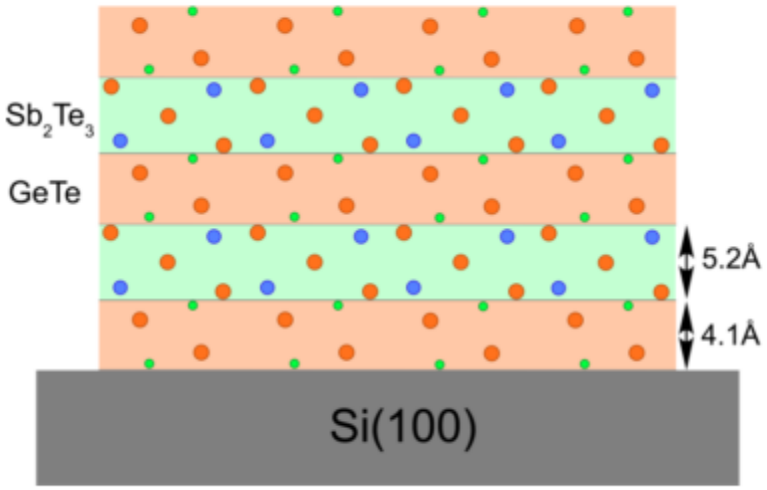


**Figure 6 Schematic structure of the Ge2 Sb2 Te5 interfacial configuration. Image reproduced with permission from: Kotaro Makino, Junji Tominaga, and Muneaki Hase, "Ultrafast optical manipulation of atomic arrangements in chalcogenide alloy memory materials," Opt. Express19, 1260-1270 (2011).**

One of the limitations of this model is the assumption of homogeneity in the long range structure of the material. However, the model holds for areas where the layered structure proposed is homogeneous, or near interfaces were Ge atoms can flip. Following this idea, Simpson *et al* [22] proposed a structure where an artificially enhanced lattice effect is generated by alternatively depositing layers of GeTe and

$Sb_2Te_3$. In this type of structure (Figure 6), the phase change occurs just in the boundaries between layers following the *umbrella flip* effect (Figure 5).

Optical excitation of this interfacial configuration have also provided experimental evidence of athermal switching in the pico-second pulse range [23]. Such experiment demonstrated the possibility of inducing a crystalline to amorphous transition just by electric excitation. It is also explained that athermal effects are not observable above pico-second range excitation, because at these time scales thermal effects dominate and traditional melting quenching amorphization occurs [23]. This observation coincides with a similar previous study [24] on the thermal-athermal response to a variety of optical pulses at different time scales, performed on semiconductors (Figure 7).

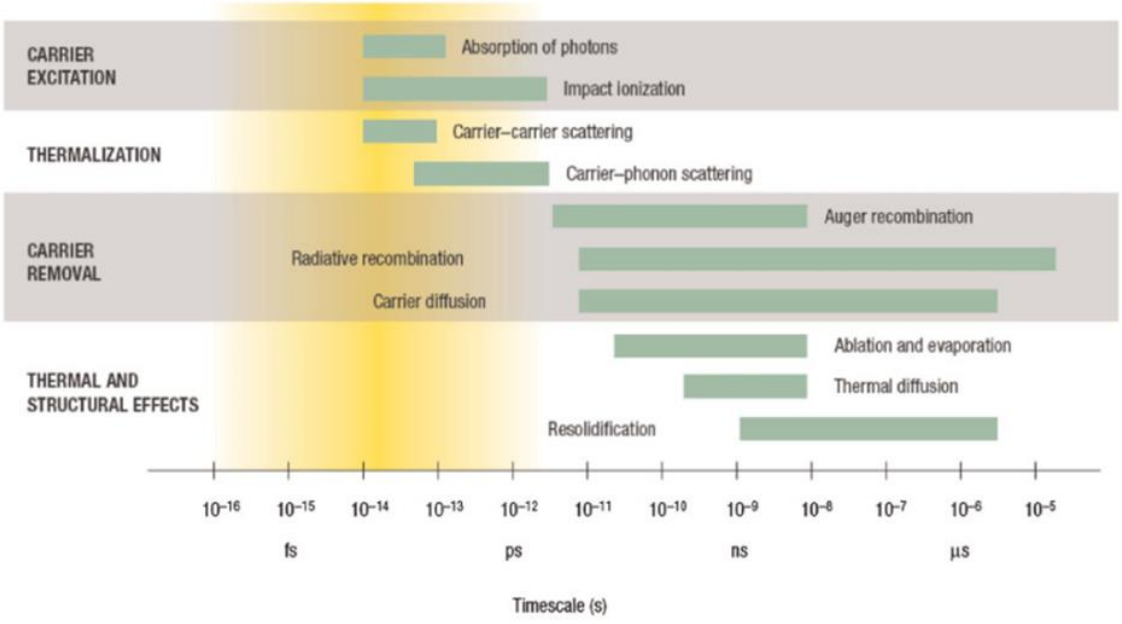


**Figure 7 Time evolution of different electronic and lattice events for semiconductors after femtosecond laser exposure. Reproduced by permission from Macmillan Publishers Ltd. Nature Materials 1, 217-224, copyright 2002.**

A subsequent, experiment presented by Fons *et al* [25] studied the structural change of GST during the crystalline to amorphous transition by measuring the evolution of the

time-resolved x-ray absorption near-edge structure (XANES) while simultaneously applying a 600 pico-second optical pulse. By following the evolution of the white-line intensity, they observed that in the amorphization transition the GST does not melt, because the intensity never goes through the value of the molten state (Figure 8). The authors argued that the rupture of weaker sacrificial (resonant) bonds by means of electronic excitation is enough to collapse the ordered metastable crystalline structure in an athermal process.

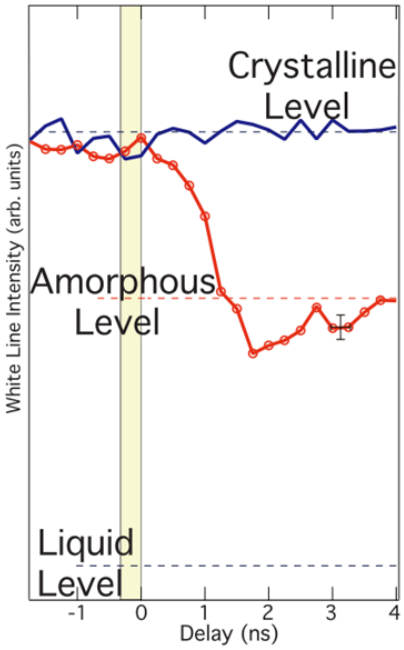


**Figure 8 Evolution of white line intensity of XANES during amorphization of GST. Dashed lines correspond to static crystalline, amorphous and liquid level. Greyed rectangle indicates the optical pulse** [25]**. Reprinted figure with permission from P. Fons et al, Physical Review B, 82, Pages 041203 2010. Copyright 2010 by the American Physical Society.**

More recently, Waldecker *et al* [26] presented a different study of the optically induced amorphization, by using a combination of single shot electron diffraction and optical

spectroscopy measurements, while applying a femto-second laser pulse. In this study the authors claim that:

"The dielectric function [of the GST] changes by 30% within 100fs owing to a rapid depletion of electrons from resonantly bonded states. This occurs without perturbing the crystallinity of the lattice, which heats with a 2-ps time constant" [26].

They also report that there is a minimum threshold of intensity of the laser to induce crystallization, and that the change in the dielectric function occurs below and above the threshold. They claim that this provides evidence that the amorphization occurs due to thermal melting of the crystalline lattice as the photo excited carriers decay in the pico-second range. This study clarifies that both thermal and athermal phenomena occur, but at different time scales.

#### 1.2.1.3 Origin of Optical contrast

In agreement with the last mentioned study by Waldecker *et al* [26], other research also indicates that the reflectivity change is due to the existence or absence of resonant bonds, as the dielectric function of GST changes according to the atomic structure transition between the metallic and non-metallic phases [27][28][29][30].

### 1.2.2 Electrical switching

Electrically induced phase change operates in an analogous way to the optically induced phase change, but in this case electrical pulses are applied instead of optical pulses. The electrical pulses through the material produce heat by the Joule Effect. Similarly to optically induced phase change, electrically induced phase has classically depended on two different pulses; a long pulse of low power that heats up the material above the glass transition temperature allowing crystallization, and a shorter but higher power

pulse that induces enough heat to melt the crystalline material. After melting, fast thermal quenching cools the material, that then becomes amorphous[17].

Phase change materials are attractive as electronic memory devices, not only because of the high contrast in resistance between the amorphous and crystalline states, but also because of their electrical response[4]. Figure 9 illustrates the characteristic I/V response of a GST phase change memory device. Starting in the amorphous state when a small voltage bias is applied, the device has a linear high resistance response, but if the bias voltage is increased over certain threshold, the high resistance of the material will yield to a conductive state without experiencing electric breakdown. At this point a sudden increase in current heats up the material which is quickly crystalized. Understanding of threshold switching is essential for the optimization of the response time and energy consumption of memory devices [17].

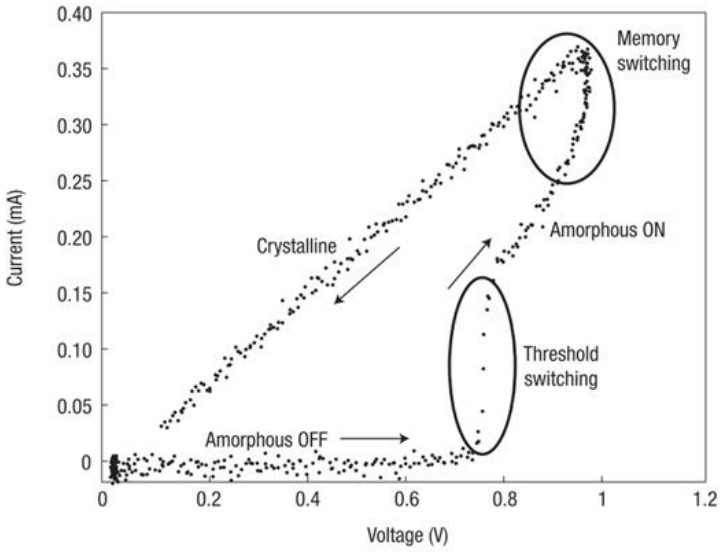


**Figure 9 Characteristic I/V curve of a GST Phase Change Memory starting from the amorphous state. Reprinted by permission from Macmillan Publishers Ltd. Nature Materials 6, 824 - 832, copyright 2007.**

### 1.2.3 Threshold switching

Threshold switching, or O*vshinksy effect*, occurs when a voltage is applied through the phase change material in the amorphous state. After a certain critical threshold value $V_{th}$, the resistance of the material suddenly decreases and it becomes conductive, generating a region of negative differential resistance. This state is sustained while a minimum holding voltage $V_{hd}$ is maintained through the material. Threshold switching is responsible for the nonlinear behaviour preceding the phase change, as shown in the characteristic I/V of a PCM (Figure 9).

Early analytical models described the threshold switching as a consequence of different solid state phenomena [31]. In the Adler model [32], initially the current depends on the mobility of holes, assuming the p nature of the material. According to such model, at low voltages and therefore low electric fields, hole mobility is limited by traps and lone pair electrons that occupy the conduction band. With an increase of voltage, the field concentrates and creates a depletion region near one of the electrodes (Shottky barrier) limiting the conduction. At a higher voltage, charges start to tunnel the barrier. The flow of charges starts filling the traps until saturation, increasing the mobility through the material. The increased mobility yields to Poole-Frankel emission [33], a further current increase and finally threshold switching occurs. Adler model also assumes the creation of a highly conductive filament, associated with threshold switching. When the holding voltage is removed, the transition to low conductance (OFF state) occurs due to diffusion of the charges forming the filament and eventual recombination of carriers in the surrounding media [34]. Recently, new models have been created motivated by the development of the Phase Change Memory [34] [35] [36], such models will be described next.

1.2.3.1 Pirovano Model

Similar to the Adler model, Pirovano uses traps and lone pair electrons. However instead of a Poole-Fenkel emission, this model uses impact ionization as the mechanism to produce an exponential increment in current. Before switching, when a collision occurs the resulting electrons fill in the traps increasing the mobility of generated holes. Ultimately the increase of generated carriers saturates the traps producing threshold switching [34].

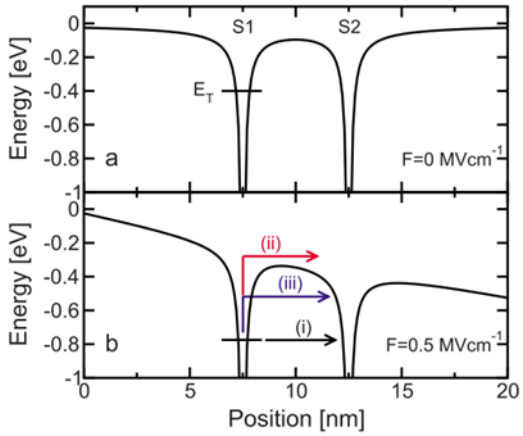


**Figure 10 Profile of the electron potential energy in Ielmini modelalong the minimum path between localized states S1 and S2, with electric field F =0 (top) and 0.5 MV cm−1 (bottom). Schematic for the electron transport processes via localized states: (i) tunnelling through the energy barrier at ET, (ii) thermal (PF) emission over the energy barrier and (iii) thermally assisted tunnelling through the energy barrier at an energy E>ET** [35]**. Reprinted figure with permission from D. Ielmini, Physical Review B, 78, Pages 035308, 2008. Copyright 2008 by the American Physical Society.**

1.2.3.2 Ielmini Model

Similar to previous models, the Ielmini model [35] uses trap limited conduction, but introduces a new mechanism to explain the threshold switching. This mechanism

combines tunnelling with Pole-Frenkel emission[33]. With an increment of voltage, electrons starting near the Fermi level find it successively easier to tunnel to higher energy traps, because of the *thermally assisted* tunnelling (Figure 10). As the electrons populate the traps, starting from the lower energy towards higher energy ones (closer to the conduction band), the average mobility rises with a subsequent exponential current increase, characteristic of threshold switching [34].

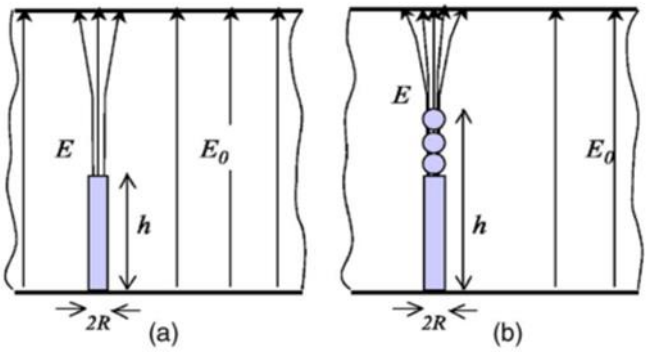


**Figure 11 Nucleation of conductive (crystalline) phase in a host of resistive (amorphous) GST material starts with nucleation of a long cylinder embryo (a) followed by nucleation of spherical particles at the cylinder edge (b). Reprinted from: Applied Physics Letters 90, 12, pages 123504, 2007 with the permission of AIP Publishing.**

1.2.3.3 Karpov Model

Karpov, *et al* [36] proposed a model which assumes that the threshold switching is not just a conduction effect but actually implies a structural change. Based on the early nucleation hypothesis of Ovshinsky [4], this model suggests that threshold switching occurs due to the formation of a conductive crystalline filament across the material. Initially a cylindrical crystallite is formed by the influence of the electric field. Further, this conductive filament creates a region of concentrated electric field where unstable spherical crystalline regions are formed by field induced nucleation [37]. Threshold

switching occurs due to percolation, when the filament connects both electrodes (Figure 11).

### 1.2.4 Crystallization

Crystallization phase change has been traditionally thought to occur by heating due to the Joule effect, when the current rises after threshold switching. However, the idea of the electric field influence during the phase transformation has increasingly been accepted, as more studies and evidence have been presented.

For example, it has been shown [38] that when an electric field is applied simultaneously with a thermally induced crystallization (annealing), an increment in the dimensions of nucleated crystallites is observed, providing evidence of the influence of the electric field enhancing crystallization [38].

Another study [37] reported observations of the characteristic change in resistance corresponding to crystallization by applying a sub-threshold voltage bias. This crystallization response was orders of magnitude slower compared to normal threshold switching. The explanation provided for the slower response suggests the growth of a conductive filament by field induced nucleation. Further, in this study it is shown that by increasing the temperature, the crystallization time can be reduced [37].

Similar interpretations have been provided by simulation based work [39] that studied the role of the electric field during the crystallization process. The result of the simulations show that the combination of temperature and electric field defines the dominance of nucleation or growth crystallization mechanisms [39].

## 1.2.5 Amorphization

Nam *et al* [40] have provided evidence of the electrical nature of amorphization. In their study, they followed the crystalline to amorphous transition of a GST nanowire by *in situ* TEM observations while applying a series of electrical pulses of increasing voltage. The first pulses induced the appearance and growth of dislocations (Figure 12, B-F). Once the applied pulses exceeded a certain threshold value, the dislocations became mobile and travelled in the same direction as the holes by the *carrier wind force* (Figure 12 G-H). A transient decrease in resistance was observed just before the amorphization. The author's analysis attributed this response to threshold switching Figure 12 A-Insert, Figure 13 B-C). Finally, amorphization occurred when mobile dislocations jammed at a certain point of the wire (Figure 12, I).

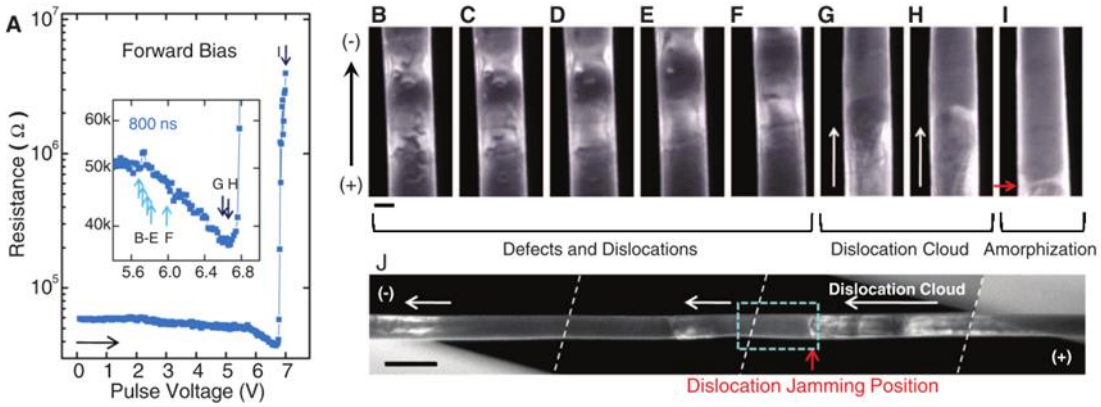


**Figure 12 Electric amorphization switching via in situ TEM measurements. Images reproduced from: S. Nam et al, "Electrical wind force-driven and dislocation templated amorphization in phase-change nanowires". Science, 2012, Vol 336, Pages 1561-1655. Reprinted with permission of AAAS.**

This response was further demonstrated by another experiment in which a notch added to the GST nanowire functioned as a constriction region for the dislocations displaced

by the *carrier wind force.* Amorphization was observed in the constrained area (Figure 13, d), confirming that amorphization occurs by accumulation of dislocations.

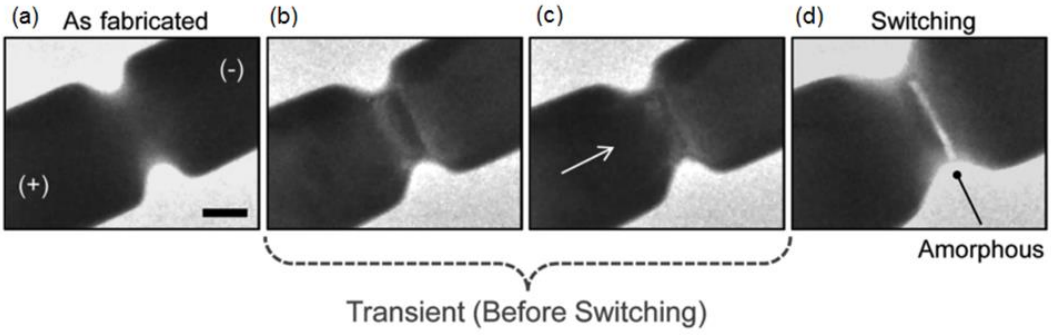


**Figure 13 Amorphization switching in a device with a notch. Images reproduced from: S. Nam et al, "Electrical wind force-driven and dislocation templated amorphization in phase-change nanowires". Science, 2012, Vol 336, Pages 1561-1655. Reprinted with permission of AAAS.**

## 1.3 Thesis outline

The changes in optical and electrical properties upon phase change make GST an ideal material for the development of opto-electronic applications that have the potential to contribute towards the solution of the technological challenges of the present. Additionally it has been widely studied and is already used in a number of commercial applications [41]. However, the use of GST by combining the optical and electrical responses upon phase change is an area that has not yet been completely explored.

Therefore, a number of questions can be posed:

- Is it possible to electrically measure an optically induced phase change, or vice versa?
- If so, how do the optical and electrical responses relate to each other?

- Is it possible to operate GST with a combination of optical and electrical signals?
- What are the technical constraints that need to be considered in order to fabricate GST devices that could be operated either optically or electrically?

The aim of the present work is to add new information to the scientific discussion in order to contribute towards the answers to these questions, and specifically to describe in detail the challenges faced and the techniques utilized during the process of fabrication and characterization of GST nano-devices. The idea was originally conceived by Prof. Harish Bhaskaran, and further refined during the progression of the research in collaboration with Dr. Peiman Hosseini.

Chapter 2 presents a review of our current state of knowledge as reported in the literature, including a survey of different PCM device architectures, a summary of the potential new applications of this phase change material and a descriptive compilation of relevant works that preceded the present research.

Chapter 3 presents the early results obtained after performing a set of preliminary experiments. It explains the fabrication process developed to produce the first set of nano-devices, using a planar design, and then describes the testing methodology created to characterize such devices by applying a series of optical pulses and measuring the optical and electrical response. It concludes by summarizing a series of technical challenges faced which need to be addressed in order to complete the experiments to characterize the *mixed mode electro-optical operation* of GST nano-devices.

Chapter 4 describes the design and construction details of a second experimental set-up. This new setup is a custom-made laser scanning microscope assembled specifically to

overcome the limitations of the set-up used to perform the preliminary experiments of Chapter 3.

Chapter 5 explains the details about the process of nano-fabrication to produce a second set of GST nano-devices, using a vertical design with transparent electrodes. The second design was used in order to overcome the limitations encountered during the preliminary experiments performed with planar devices. The MatLab library used for the transfer matrix method calculations was developed by Carlos Rios Ocampo. XRD measurements were performed by Dr. Lesley Wears at the University of Exeter facilities.

Chapter 6 goes on to present the experimental results obtained by testing the second set of nano-devices in the custom-built setup. The results include optically inducing the crystallization of a device by a series of accumulative pulses, as well as electrically induced crystallization. In both cases, the evolution of the reflectance and resistance was simultaneously measured. The analysis of the results is then presented, showing how partial crystallization within the GST thin film of the device plays a significant role in the optical and electrical response. Finally, a proof of concept of an opto-electronic memory device that can be written electrically and erased optically is presented. The COMSOL thermal model used in this chapter was developed in collaboration with Santiago Garcia-Cuevas Carrillo, from the University of Exeter.

To conclude, Chapter 7 summarises the main results of this work, which is the experimental demonstration of an opto-electronic memory device, and outlines how it represents a step forward towards the development of opto-electronic applications based on GST. These include fast telecommunications or interfacing between photonic and electronic circuits, as well as ultra-high resolution nano-displays or artificial retinas.

The original contributions of this doctoral thesis are:

- Designed an experiment and the required methodology to characterize the optical and electrical response of GST in nano-devices.
- Designed and built of a custom made experimental setup to perform *mixed mode* experiments.
- Presented the first experimental study on the relationship between optical and electrical response of GST in nano-devices.
- Provided a proof of concept of a novel non-volatile optoelectronic memory based on GST a nano-device.

# 2 LITERATURE REVIEW

## 2.1 Phase Change Memory Device architectures

The use of GST for the development of PCMs requires in addition to the study of the material characteristics, the realization of functional structures or devices that can be operated by applying controlled electrical pulses. Such devices need to be easy to manufacture, reliable and ultimately minimize the power required by the GST to change phase. In this section, a non-exhaustive compilation of some architectures reported in the literature is presented, providing a brief description of the fabrication process which is the relevant aspect for the present work.

### 2.1.1 Bridge

Krebs *et al* [42] fabricated a type of bridge device using lithographic processes. First the bottom electrodes were built, followed by a planarization process with $SiO_2$, then a thin strip of GST was deposited, as shown in Figure 14.

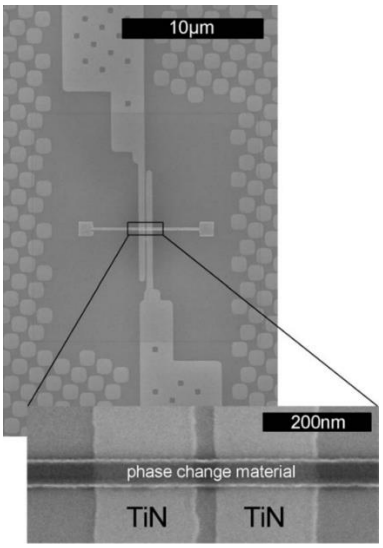


**Figure 14 SEM image of a bridge device. A thin strip of GST was sputtered across two planarized electrodes build previously. Insert shows the Phase Change material in contact with the electrodes over the dielectric gap. Reprinted from Applied Physics Letters 95, pages 082101, with the permission of AIP Publishing.**

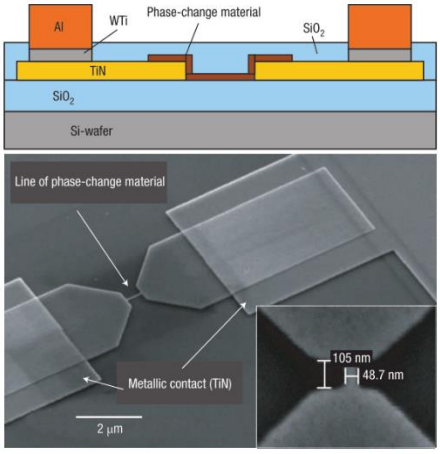


**Figure 15. Top, schematic diagram of the low cost planar device. Bottom, SEM image of the device fabricated, the phase change material region was patterned with high resolution electron beam lithography. Reprinted by permission from Macmillan Publishers Ltd. Nature Materials 4, 347 - 352, copyright 2005.**

### 2.1.2 Planar

Lankhorst et al [43] presented a low cost planar device built by depositing a lithography patterned phase change material region between two large electrodes. The pattern of the device caused the phase change material to switch in the narrower line region. A schematic and SEM images can be observed in Figure 15.

### 2.1.3 Cross-bar

Hosseini *et al* [41] fabricated a cross-bar device by first constructing a planarized bottom electrode, then the GST and top electrode layers were deposited in the same run in such a way that a small GST region was confined between the crossing of the electrodes.

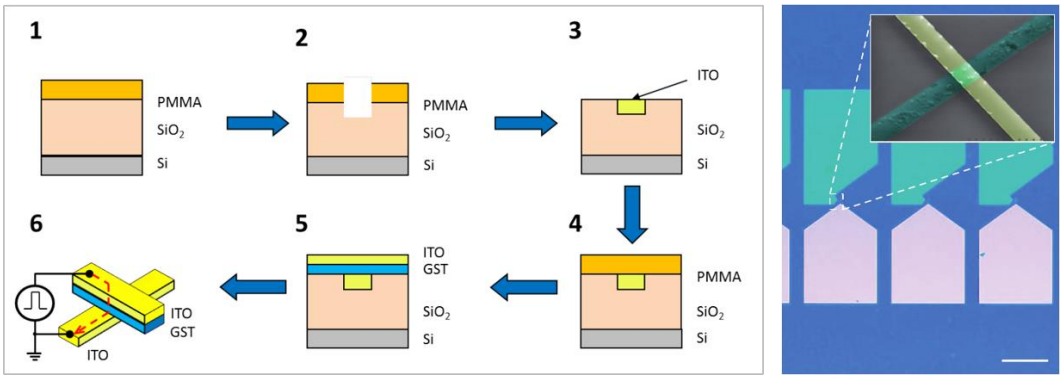


**Figure 16. Schematic representation of the cross-bar devices. Reprinted by permission from Macmillan Publishers Ltd. Nature 511, 206 - 211, copyright 2014..**

Figure 16 shows the fabrication process: 1) Spin coat PMMA resist on an oxidized silicon wafer. 2) e-beam patterning and etching of a trench in the $SiO_2$. 3) Indium Tin-Oxide (ITO) was deposited to fill in the trench in order to fabricate a planarized bottom electrode. 4) A second e-beam lithography was performed on PMMA resist, to pattern the top electrode. 5) GST and ITO were deposited using the same pattern. 6) Cross-bar

device created by confining a small GST region between ITO electrodes. Figure 16 right, optical microscope of a line of devices scale bar is 100µm. Insert contains a coloured SEM picture of the cross-bar area.

### 2.1.4 Mushroom Cell

This was the first scalable PCM architecture, developed by S. Lai and T. Lowrey at Intel corp. [7]. Originally called Ovonic Universal Memory (OUM), it was later commonly known as *mushroom cell*, because of the mushroom-like shaped dome created by the amorphous GST as it changes phase during the operation of the PCM. This vertical architecture was built by first depositing a bottom electrode, followed by a dielectric layer. Then a hole was patterned in the dielectric layer and filled with a conductive heater material (commonly TiN). Later, a thin film of GST was deposited, followed by the top electrode layer. Figure 17 shows a schematic diagram of the mushroom cell architecture.

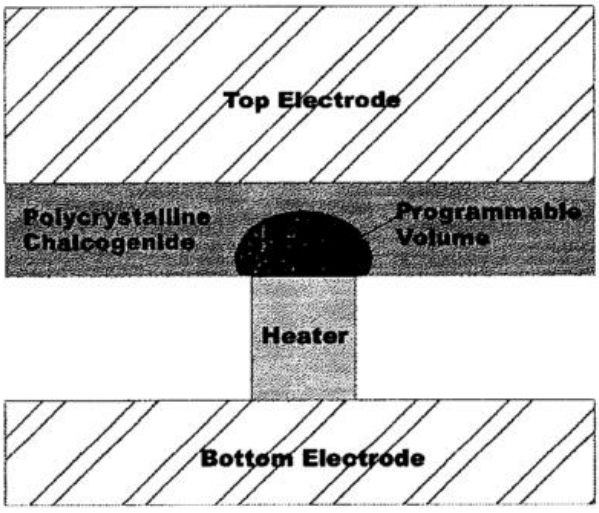


**Figure 17 Schematic Diagram of a mushroom cell PCM. Image reproduced from [7], (2001) IEEE.**

The importance of the mushroom cell architecture was that it showed a way to produce scalable CMOS compatible vertical devices. It also showed the need for thermal management and established the relationship between efficiency of the cell and the contact area between the GST layer and the heater.

### 2.1.5 Micro-trench

Developed by Pellizer *et al* [44] at ST Microelectronics, the µ-trench architecture was created with the intention of reducing the programming current by minimizing the contact area of the GST with the electrodes. This was achieved by "reducing the heater thickness and by a sub-lithographic GST trench" [45]. This process was scalable and used a bipolar junction transistor (BJT) as access device. The architecture included a semi-metallic heater which thickness was defined by film deposition and the µ-trench itself, fabricated by sub-lithographic techniques. Further the GST was then sputtered resulting in a very small contact area. A schematic of this architecture is shown in Figure 18.

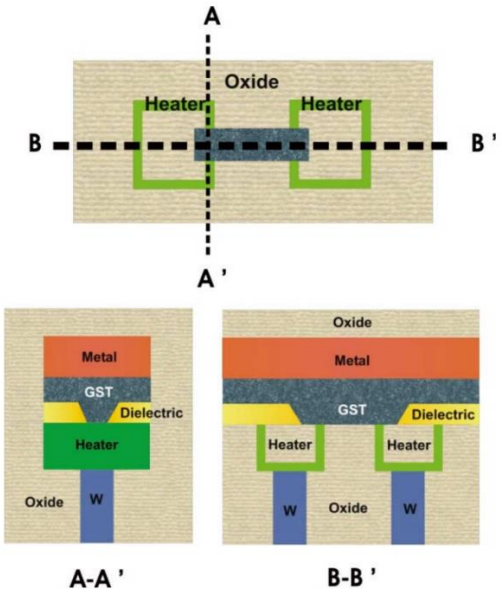


**Figure 18 Schematic view of a µ-trench PCM. Adapted from** [44]**, (2004) IEEE.**

### 2.1.6 Pore

Another approach to reduce the contact area between GST and the bottom electrode was by creating a nano-pore that could achieve sub-lithographic size. This process was presented by Breitwisch *et al* [46] and started with a previously created bottom electrode covered by SiN, $SiO_2$ and SiN layers. A lithographic process created an aperture on the top SiN layer, then $SiO_2$ was wet-etched to produce a recess in respect to the top SiN layer. Then a layer of poly-Si layer was deposited. A pinch in the poly-Si was created by the effect of the recess on the SiN top layer. Later, the poly-Si was etched so that the pore opening was transferred to the bottom SiN, which was then selectively etched using the poly-Si as a mask. Then, the $SiO_2$ was removed, leaving the pore exposed. Finally, GST and the top electrode materials were deposited to complete the PCM. Schematic of these steps are shown in Figure 19. The pore size reported by this process was of 43nm fabricated using 180nm CMOS technology.

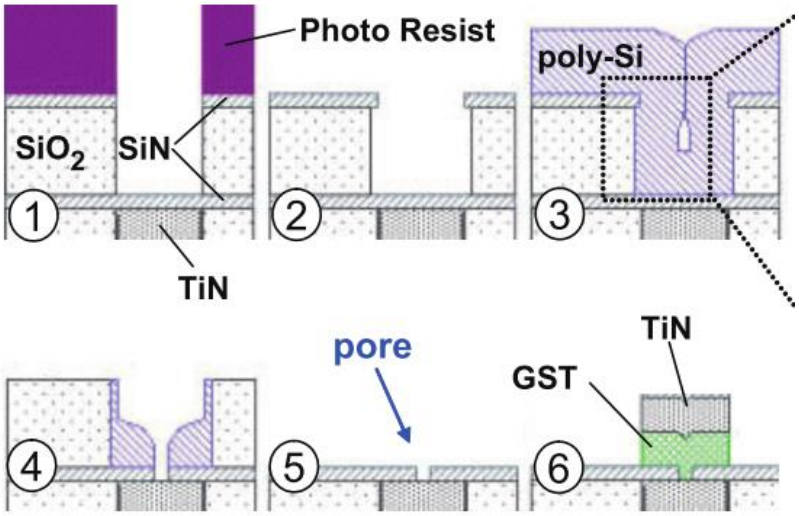


**Figure 19 Schematic diagram of the pore PCM process. Adapted from**[46]**, (2007) IEEE.**

## 2.1.7 Edge

A different alternative architecture also following the sub-lithographic feature size concept, was the Edge Contact PCM, introduced by Ha *et al* [47]. This process started by constructing the bottom electrode (M0 or Metal connection), on top of it a Bottom Electrode Connector (BEC) was formed. Then the Bottom Electrode (BE) made of a 20nm TiN layer was deposited followed by a dielectric film that covered the BE. Next a trench was created in the bottom dielectric layer and in contact with the BE. This trench was then filled with GST and a Top Electrode capping material (TE). Finally the Top Electrode Contact (TEC) and the top Metal Connection (M1) were built. A schematic of this device architecture is shown in Figure 20. By creating a trench in contact with the BE, a small volume region by the edge of the trench that worked as a PCM was created. The size of the PCM was defined by the depth of the trench and the thickness of the BE, both of such parameters can achieve sub-lithographic dimensions.

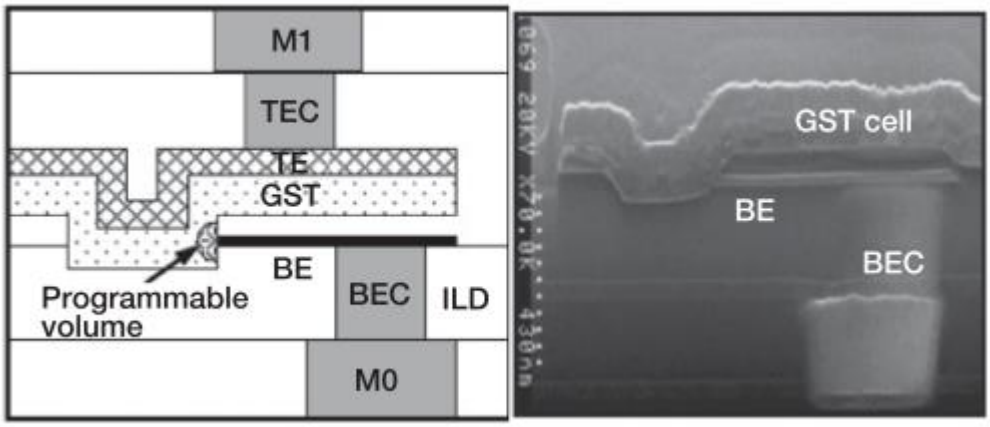


**Figure 20 Left, Schematic diagram of an Edge contact PCM. Right, SEM picture of the cross sectioned device. Adapted from** [47]**, (2003) IEEE.**

## 2.2 Potential New applications

### 2.2.1 Multi-level data storage

One of the features of PCM that is currently under research is the development of multi-level data storage. This is achieved by storing intermediate values between the amorphous and crystalline states of the GST allowing the PCM to store more than one bit per cell. A study presented by IBM Research [48] analyzed different aspects of multi-level data storage using PCM. The multi-level logic programming used starts with the device in low resistance state (SET), then a series of successively increasing current pulses are used for writing. These pulses melt part of the crystalline region in such a way that a section of the GST area is incrementally amorphized. The reading is done by measuring the increase in resistance after applying a low voltage pulse. It is explained that the SET to RESET transition is preferred to achieve multiple level storage in order to facilitate the reading. In another case, reading from a high resistive state (RESET) would require higher voltages that may induce threshold switching, and the high current after threshold switching could alter the state previously stored.

This study also analyzes the problem of variability between devices, which is one of the main factors that limit the scalability of multi-level PCM. Small fabrication variations can cause resistance levels to deviate from the expected ranges, reducing multi-level reliability. In order to overcome this problem, the study proposes an iterative write-read method and compares different control procedures that lead to the convergence of the expected resistive value.

Currently, the main problem that limits multi-level data storage in PCM is the resistance drift [49] because the stored values drift to a potentially different value, limiting the amount of intermediate resistance steps that can be stored and differentiated at reading.

Approaches to compensate for the resistance drift include the creation of measurement techniques less subjective to resistance drift [50], as well as the creation of devices that minimize the residual stress experienced by the GST volume when the phase change occurs [51]. This is because resistance drift is "due to the material structural relaxation and stress release"[49].

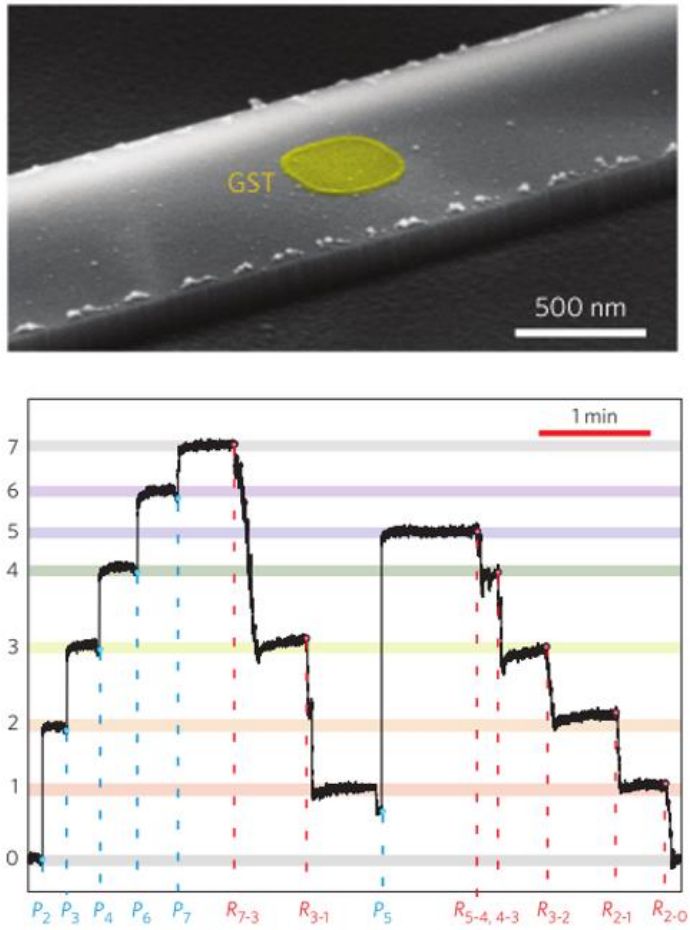


**Figure 21 SEM picture of the all photonic multi-level memory (TOP), that consists on a GST region deposited on top of a photonic waveguide. Bottom, diagram of multi levels achieved by partially crystallizing the GST by Appling laser pulses of different powers, thru the waveguide. Reprinted by permission from Macmillan Publishers Ltd. Nature Photonics 9, 725 - 732, copyright 2015..**

### 2.2.2 Integrated Photonics

One of the most promising potential new applications for GST is its use in multi-level photonic memories. This was experimentally demonstrated by Rios *et al* [52]. By depositing a small GST region on top of a photonic waveguide (Figure 21 Top), the light coupling between the GST and the waveguide changes depending on the refractive index of the GST, which can be altered by inducing a phase change. As a consequence, the attenuation of the transmitted signal in the wave guide can be controlled in discrete steps by partially crystallizing the GST region of the device (Figure 21 Bottom).

### 2.2.3 Computing using PCM

Recently, Wright et al [53] have shown the possibility of using the multi-level property of PCMs as a processing element, unveiling a promising way to construct computing systems beyond the Von-Neumann paradigm. This work uses phase change material as an accumulator to perform arithmetic operations. The accumulation property occurs in the RESET (amorphous) to SET (crystalline) transition due to partial crystallization. When a pulse is applied, the current through the PCM induces the creation of crystalline nuclei in the amorphous media. Subsequent pulses cause the growth of existing nuclei as well as the nucleation of new ones. After a specific number of pulses, the percolation limit is reached, which yields to a low resistance state. By carefully selecting the characteristics of the pulses, it is possible to divide the RESET-SET transition into a defined number of steps that are used as the base for the operation. This system is different from the previously proposed multi-level storage in the way that it does not depend on individual internal states, but only on two highly differentiable ones, a high resistance accumulative state and a low resistance one. The latter is reached after the specified number of pulses have been applied starting at the high resistive state, or, in

other words, after the number of pulses applied have taken the resistance value beyond the decision level (Figure 22)

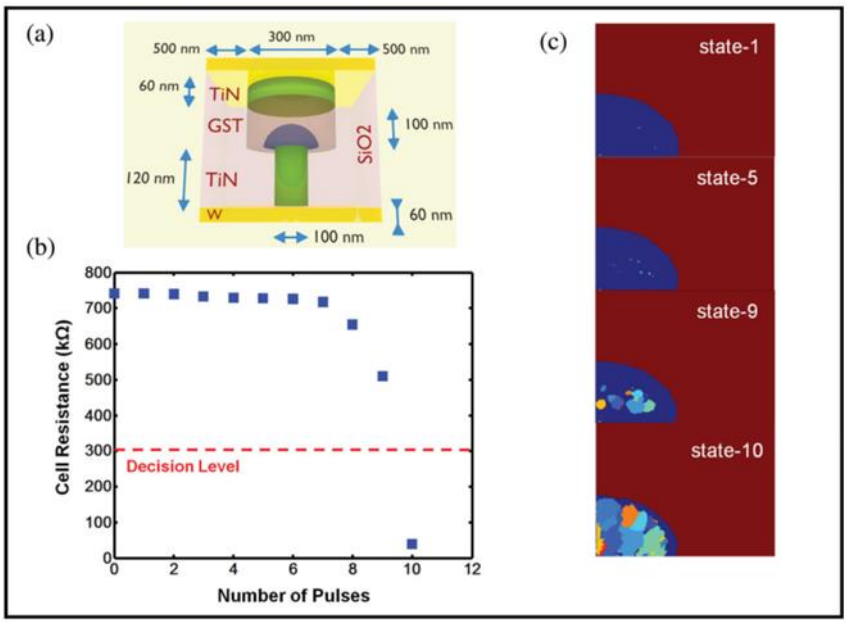


**Figure 22 a) Schematic of the PCM mushroom-type cell used for simulation of the phase-change base-10 accumulator response. b) The resistance of the PCM cell in (a) after the application of each of 10 input pulses with each input pulse having an amplitude of 1.085V and being of 60 ns duration. This is the basic accumulator response, in this case operating in base-10. c) Shows the simulated structure of the active region after the first, fifth, ninth and tenth pulses (i.e., state-1, state-5, state-9 and state-10): Lighter regions are crystallites inside the amorphous dome. The area surrounding the amorphous dome is crystalline. Reproduced from** [53] **with permission of Wiley (2013).**

In order to perform an addition operation, for example, a successive number of pulses are applied to the cell. The result is stored as the complement number of pulses to reach the decision level. An example provided in this work is the operation ($3_{10}$+$1_{10}$ ). This operation requires applying 3 and then 1 pulse to a PCM. The result is stored as internal

state 4, and the answer is the complement to the base of pulses required to take the cell to the decision level. Therefore, further application of pulses indicates that 6 pulses are required to reach the decision level ($10^{th}$ state), consequently the answer is 4. The authors present similar algorithms to perform subtraction and, interestingly, factorization. They also stated that the required logic for the operation can be implemented using PCM, (i.e. calculation of complements) offering a full set of operations to create non Von-Neumann architectures[53].

The accumulation property has also been demonstrated in the optical domain [54] by using a successive series of laser pulses to perform arithmetic operations. Calculations are performed in a similar way by defining a decision level and tuning the fluence of the pulses to define the operation base (Figure 23).

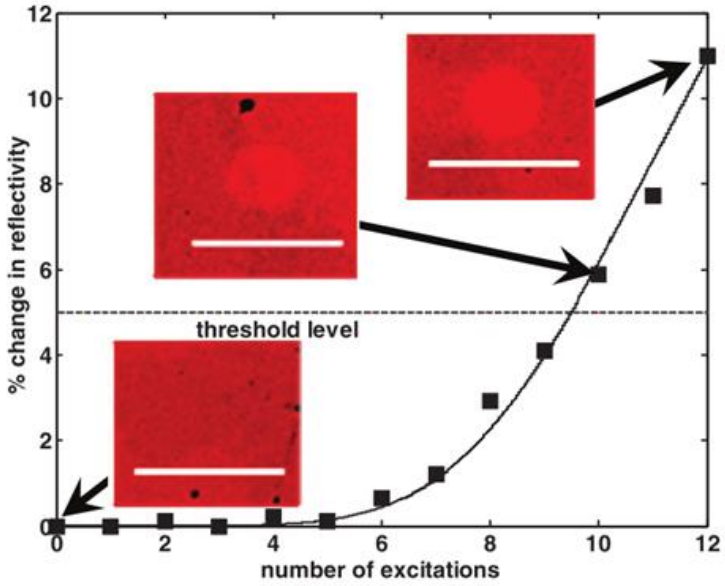


**Figure 23 Example of accumulation property used in arithmetic processing in the optical domain. A consecutive number of conveniently selected pulses define the base for the calculation. Reproduced from** [54] **with permission of Wiley (2011).**

### 2.2.4 Neuromorphic computing

Probably the most exciting application of PCMs is their use for neuromorphic processing. This means the creation of hardware architectures that mimic the way neurons and synapses compute in the brain. Neuromorphic processing has received great interest in recent years, after the invention of the memristor [55].

However, memristors have not yet been able to fulfil the expectations due to their complex fabrication process, low yield, and very short cyclability. For these reasons, PCM's have been considered as a potential alternative for neuromorphic computing architectures.

The human brain possess $10^{11}$ neurons and $10^{15}$ synapses. Synapses are thought to be responsible for how information is stored and processed in the brain [56]. Therefore they have been the main focus of interest in the research of neuromorphic systems.

Kuzum *et al* [56] have demonstrated a scheme to implement Spike Time Dependent Plasticity (STDP) using a PCM as a synapse. STDP is a learning rule found in biological neural systems. It states that the synaptic connection between neurons that fire simultaneously is strengthened (potentiation), whereas if neurons fire separately their connection is weakened (depression). According to this work, it is possible to imitate the potentiation and depression behaviour of a synapse by inducing intermediate resistance levels starting from the SET (crystalline) state towards RESET (amorphous), similar to the multi-level data storage discussed earlier [48].

The pulsing scheme of this approach depends on two sets of pulses the – pre-synaptic and the post-synaptic – which are applied to each electrode of the PCM. The pre-synaptic pulse is in fact a series of ramping up voltage depression pulses, followed by a decreasing amplitude series of potentiation pulses. The post-synaptic pulse is a normal

squared pulse. When such pulses coincide, their amplitudes are added and a current passes through the PCM modifying the internal state. (Figure 24). This scheme requires a complex set of pulses to achieve the potentiation and depression on a single PCM. Such a complex programing scheme requires as a consequence a complex control logic, which presents a scalability barrier.

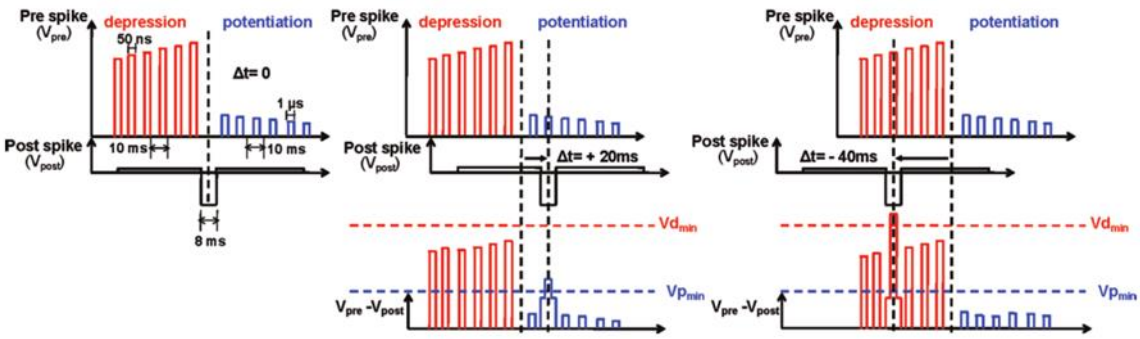


**Figure 24 Pulse scheme used to implement STDP. Reproduced from D. Kuzum et al, "Nanoelectronic Programmable Synapses Based on Phase Change Materials for Brain-Inspired Computing" Nano Letters, 12, Pages 2179-2186. Copyright (2011) American Chemical Society.**

A different approach by Suri *et al*,[57] combines two PCMs to create a synapse capable of supporting STDP. One PCM is used to store the current status of potentiation and the other one the depression. In this case, each PCM starts in the RESET (amorphous) state and moves towards the SET (crystalline) after every pulse. Although this approach claims to be more energy efficient than the previous one, and the pulsing scheme is simpler, the control logic is not. This is because pre- and post- synaptic neurons on either side of the synapse have to add the contribution coming from each PCM to determine the appropriate weight of the connection. Also as both potentiation and depression depend on just one direction (RESET to SET) of each PCM, the system saturates once the conductive state is reached, hence an extra resetting control is

required. Despite these difficulties, simulations of an architecture based on this "two PCM synapse" [57] have proven to perform object recognition in video sequences [57].

Both alternatives explained so far depend on the change in resistance of the PCM by creating intermediate levels between SET and RESET states. Recently, Li *et al*. [58] have suggested a new approach to implement STDP based on their findings of memresistive properties of crystalline GST. In their study, they observed a polarity dependent change in resistance. They attribute this behaviour to Space Charged Limited Conduction (SCLC). In their analysis, the authors state that:

"During the application of external negative voltage bias in this experiment, the injection electrons were captured by the vacancies, filling the deep-level traps. The conduction behaviour in the positive bias region indicated the transition from trap-filled to trap-unfilled SCLC associated with charge emission." [58].

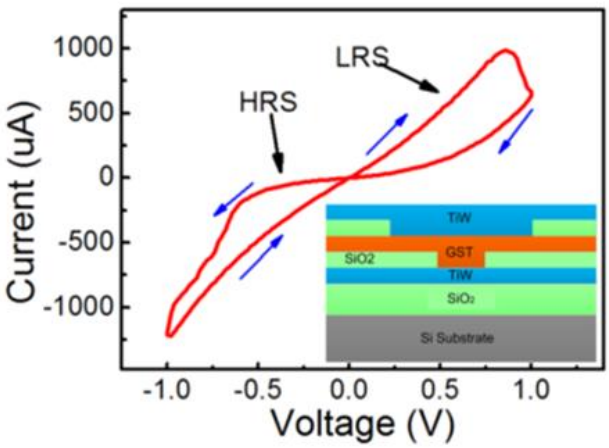


**Figure 25 I/V Plot showing the memresistive response of crystalline GST by applying positive and negative bias. Insert is a schematic of the device. Reprinted by permission from Macmillan Publishers Ltd. Scientific Reports 3, Article 1619, copyright 2013.**

A change in the value of the device capacitance was also observed while measuring the I/V response. According to the authors, this is the indication of change in the charge distribution.

By using this bipolar response, (Figure 25) it is possible to implement a simpler STDP pulse schema compared to the previous approaches mentioned. In this case both potentiation and depression are obtained by a series of pulses of increasing amplitude. (Figure 26)

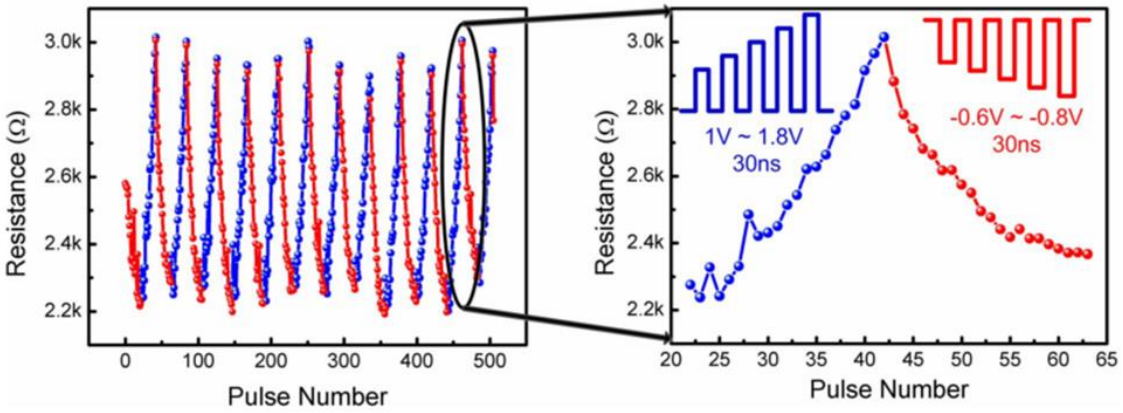


**Figure 26 Pulse-driven memristive behaviour. The conductance increases or decreases in response to negative or positive pulses, respectively, representing synaptic weight modulation due to potentiating or depressing pulses. The pulse amplitudes vary with identical 30-ns widths and 1-s pulse intervals. Reprinted by permission from Macmillan Publishers Ltd. Scientific Reports 3, Article 1619, copyright 2013.**

All approaches mentioned so far have looked into the possibility of emulating potentiation and depression behaviours of the biological synapses using PCM. However, another key element in the neuromorphic architectures is the leaky integrate

and fire neuron. Toma *et al* from IBM research have demonstrated that the stochastic integration and firing behaviour of the neurons can also be reproduced using a PCM device by pairing the "conductivity of the PCM with the membrane potential of a neuron" [59]. A series of pre-synaptic accumulative pulses are added up in the PCM neuron, gradually increasing the conductivity of the device. Then when it reaches certain threshold, a pulse is emitted and the device is automatically reset. This approach has been shown to be scalable, as the authors provide a demonstration with 500 neurons.

### 2.2.5 Opto-electronics

Recently, there has been growing interest in the development of opto-electronic applications using GST after Hosseini *et al* [41] showed that it is possible to create colour tunable pixels that can be switched electrically. By encapsulating a thin film of GST between two transparent electrodes, these transparent electrodes create an optical nano-cavity. The resonance of the nano-cavity can be designed by varying the thickness of the different layers. Then, by crystallizing the GST, it experiences a change in refractive index which produces a change in the optical response of the cavity. This is perceived as a change in colour. Figure 27 shows the schematics of this concept and a demonstration of this technique to produce super high-resolution images, by electrically inducing a phase change in the pixels.

Subsequently, following a similar idea, Rios *et al* have demonstrated that it is also possible to obtain colour gradients by partially crystallizing the GST layer when signals of different voltages are applied [60].

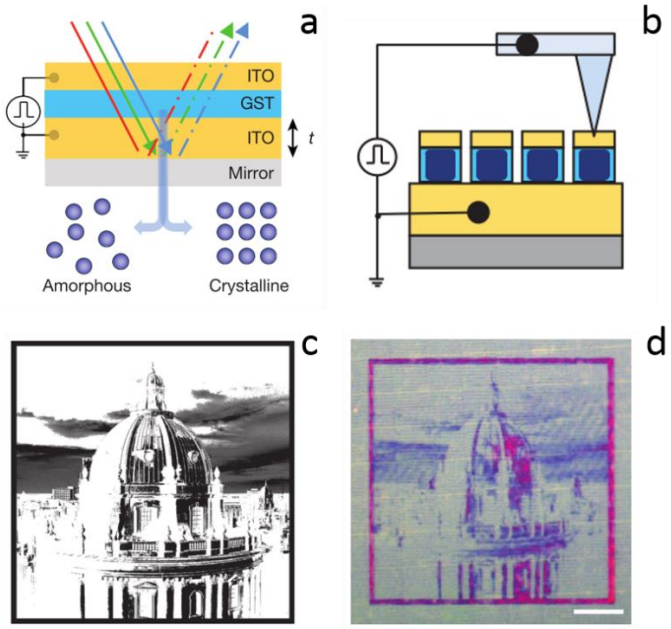


**Figure 27 Colour tuneable nano-pixels. a) Colour of the pixel is tuned by adjusting the thickness of the GST film and the top and bottom transparent electrodes. b) Using an atomic force microscope tip, individual pixels were switched electrically, so their colour changed. c) Black and white high contrast digital image, d) same image as c but written by switching a series of 300x300nm pixels with 200nm pitch. Scale bar is 10µm. Reprinted by permission from Macmillan Publishers Ltd. Nature 511, 206 - 211, copyright 2014..**

### 2.2.6 Mixed Mode

In addition to the emerging display applications, another types of opto-electronic devices that combine optical, electrical, memory and processing functionalities have been suggested [61][54]. One of the most interesting research opportunities in this respect, is to explore the GST capabilities in a combination of electrical and optical domains; or *mixed mode operation*. To do this, it is necessary to understand the relation between the evolution of optical and electrical responses. Some previous work has

measured the combined electrical and optical responses in order to characterize a variety of GST properties. Although these properties provide useful clues about how to interoperate in both domains, the use of *mixed mode* for memory or computation has not yet been explored as such. Following there is a summary of previous works that have performed some sort of optical and electrical measurements to characterize different properties of GST.

2.2.6.1 Transient responses to optical excitation

Lee *et al* [62] studied the photoconductivity and absorption coefficient of GST in amorphous and crystalline phases. In their study, they used ellipsometry for the absorption coefficient and a tungsten lamp with a monocromator for the photoconductivity. By combining the data of electrical and optical measurements, they were able to infer the optical bandgap of the amorphous, FCC and hexagonal phases, and explain its correspondence to the photoconductivity behaviour. This was presented as a corresponding increase in the absorbance and photoconductivity while varying the illumination photon energy. The study also characterized how the crystalline phases changed in conductivity at low temperatures, concluding that GST is a degenerated semiconductor because "the fermi level is within the valence band"[62].

One interesting property of degenerated semiconductors is that they present the band filling effect. As the name indicates, low energy states get "filled" while increasing the concentration of carriers. Band filling effect has been proposed as the cause of saturable absorption detected in crystalline GST in a work presented by Lee *et al* [63]. In this study, saturable absorption was observed by exposing crystalline GST to a pulsed laser of variable power. As the power of the laser pulse increased, the absorption coefficient decreased together with a corresponding increase in transmittance. The association of this behaviour with the band filling effect derives from a measurement of electrical

resistance performed simultaneously. In this case, the electrical resistance decreased as the power of the laser increased. This finding was interpreted by the authors as a consequence of the increment of free carriers. It is important to remember that this study analyzed just the transient response of crystalline GST upon optical excitation without actually inducing a phase change.

Later, another study by Liu *et al* [64] presented similar observations, but in this case the determination of electrical response was not obtained experimentally but by first principle simulations.

2.2.6.2 Electrical and optical response during crystallization.

Kim *et al*[65], studied the differences between electrical and optical responses during the crystallization of GST by simultaneously measuring the change in reflectivity and resistivity. These measurements were performed on a GST thin film while it transitioned from the amorphous to crystalline phase by the effect of an isothermal heat source. In their results, they notice that the change in reflectivity occurred later in time than the change in resistivity. Based on a theoretical analysis, they subsequently determined that there is a linear relationship between the reflectivity and the crystallinity of the material. A comparison of the evolution of the change in resistance against the crystallinity produced a non-linear response that they explain by using the predictions of the Wiener percolation model. This model explains the behaviour of the electrical resistance in the case when conductive (crystalline) seeds are within a dielectric (amorphous) media. Interestingly, it is explained in Kim *et al's* analysis that by performing numerical calculations for different conditions of the Weiner model, the evolution of the resistance better fits a particular case of the Weiner model when crystallization occurs in a layer by layer fashion starting from the top of the material. This situation can be seen in Figure 28a.

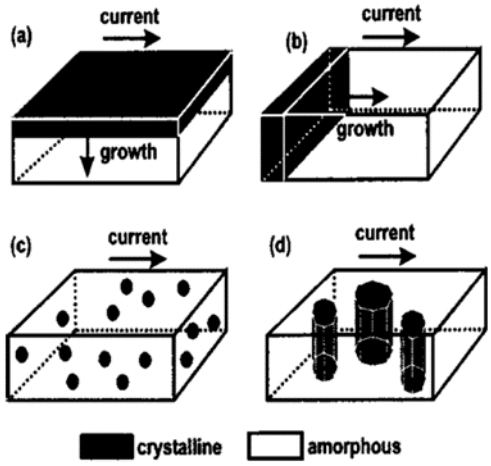


**Figure 28 Different crystallization behaviours obtained by numerical simulations, using specific cases of the Wiener percolation model. Case (a) was choose as the better fit for the data obtained** [65]**. Reprinted from Journal of Applied Physics 97, Pages 083538, 2005.**

Subsequent work presented by Choi *et al* [66] implemented a similar experiment. They also measured the evolution of the electrical resistivity and optical conductivity simultaneously during the amorphous to crystalline transition of GST. However, this experiment used halogen lamps as a fast heating source and performed two different measurements, one with isothermal heating and another one with an incremental temperature ramp. The experiment of isothermal heating is technically the same as the one from the work by Kim *et al*, mentioned previously. However, in this case they observed the opposite behaviour: there was a delay in the change of electrical resistivity compared with the reflectivity. They nevertheless again associated the origin of this behaviour with percolation, explaining that crystalline nuclei start to grow in the amorphous material producing the change in reflectivity but is not until such nuclei form a conduction path that the resistivity drops, and at this point the evolution of reflectivity is almost complete. A possible explanation for the discrepancy of results

would require considering the position of the sample in respect to the heat source, and how heat is distributed within the GST layer. This discrepancy highlights the importance of the thermal characteristics in the evolution of optical and electrical responses during crystallization.

A more recent experiment was implemented by Liang *et al* [67], observing simultaneously the electrical and optical response of the transition of the GST from as-deposited amorphous to crystalline phase. In contrast with previous studies, the phase change was induced optically by a single nano-second laser pulse. The reflectivity was measured by a different laser source in a pump-probe configuration. Moreover, in this experiment, other considerations were taken into account such as monitoring the voltage used to measure the resistance. It is important to mention that this experiment follows the phase transition in a time frame significantly shorter than in previous studies, observing the response while the system was relaxing after the pulse. In the results, the authors report a delay in the response of the reflectivity compared to the evolution of the resistivity, similar to the observations mentioned previously in the work of Kim *et al*. [65].

Also similar to previous studies, the analysis provided is based on the percolation phenomena, but in this case a 2D model of percolation is provided. This 2D model explains that crystalline nuclei start to grow in the surface of the material up to a point when a conduction path is reached and the resistivity starts to decrease, but these crystalline nuclei do not yet produce a significant change in reflectivity. Further, the crystalline nuclei grow on the surface of the material forming a conductive strip; at this point, the change in reflectivity starts to be perceptible. Finally, the crystalline layer grows from the surface into the material, completing the change in reflectivity once the absorption depth limit is reached. However, the evolution of resistivity has been almost

completed by the time the crystalline layer is formed on the surface of the material. A schematic of this explanation can be seen in Figure 29.

The crystallization behaviour of this 2D model is qualitatively similar to the one previously mentioned in the work of by Kim *et al*. [65]

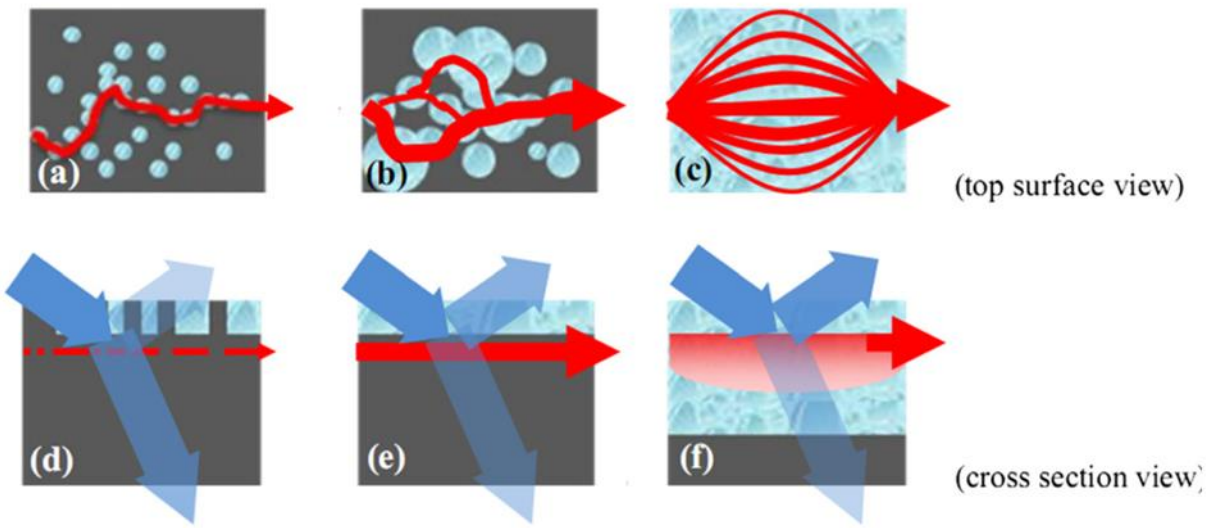


**Figure 29 Schematic diagram of the evolution of reflectivity and conductivity of GST upon irradiation by a single nanosecond laser pulse. (a)(d) Crystalline nuclei reach the percolation threshold and a conduction path is created. Not perceptible change in reflectivity occur yet. (b)(e) Nuclei grow to form a conductive layer in the top of the material. The change in reflectivity starts to be observed. (c)(f)Crystallization proceeds into the material, change in reflectivity is completed when the crystallization reaches the absorption limit depth. Reprinted from Chemical Physics Letters 507, G. Liang et al, "Comparison of optical and electrical transient response during nanosecond laser pulse-induced phase transition of Ge2Sb2Te5 thin films", Pages 203-207, Copyright (2011), with permission from Elsevier.**

It is clear from what has been shown above, that the evolution of the crystallization of GST behaves differently in the electrical and optical domains, and that the differences can be explained in the light of percolation. However experiments to date have only explored the electrical response by measuring the change in resistance without considering the potential of combining optical excitation with voltage bias. This combination offers an interesting possibility for the mixed mode operation, considering the non-linear electronic response of GST associated to threshold switching. This idea comes to mind following recent investigations that demonstrate the influence of the electric field in the crystallization dynamics. For example, the application of an external electric field has been used in combination with a thermally-induced crystallization process. Arciniega *et al* [38] have observed an increment in the dimensions on the rock salt crystalline domains by thermally annealing a GST sample assisted by an electric field. They also observed that these domains are ferroelectric and their shape and orientation was influenced by the electric field.

Similarly, Karpov [68] has presented a model that explains how the electric field induced by optical pulses can affect the shape of the crystalline nuclei, and suggests the possibility of controlling the orientation of the crystallites by using polarized light.

2.2.6.3 Mixed mode approaches

A possible approach for *mixed mode* operation is to induce a phase change electrically and measure the change optically. This approach presents some challenges, mainly because of the difference in contrast between both domains (20% optical contrast vs. a change of three orders of magnitude in resistance). Also there is a size trade-off; minimum optically observable dimensions are defined by the diffraction limit, whilst efficiency and speed of electrical switching are improved by reducing the dimensions. Nonetheless, some application ideas have been suggested.

For instance, Mu *et al* [69] have presented simulations of an electrically controlled optical latch. The stability of the states of GST allows the device to retain a specified ON/OFF state (latch) when power is removed, hence improving energy efficiency. The device consists on a plasmonic waveguide made of gold electrodes with a thin layer of GST in between them. The operation depends on the variation of the absorption coefficient. In the OFF state (crystalline), the higher absorption increases the coupling loss compared to the ON state (amorphous). The authors claim a theoretical 10dB difference between the ON and OFF states. By using plasmon transmission, this configuration overcomes the optical diffraction limit. A schematic is shown in Figure 30.

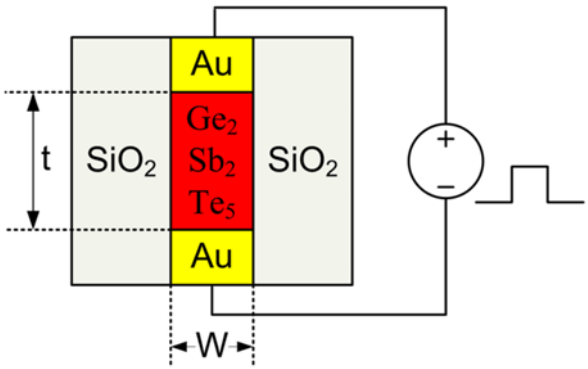


**Figure 30 Schematic of a GST based plasmonic latch. Gold terminals function as electrodes to switch the GST as well as plasmonic waveguides. Reprinted from Applied Physics Letters, 103, 4, Pages 034115, 2013 with the permission of AIP Publishing.**

Another early example of a potential *mixed mode* realization was previously exposed by Gholipour [70] with the intention of creating opto-electronic gates. This was done by creating two small GST regions electrically arranged in series. It was found that when the GST regions were crystalized optically, the value of the resistance of the

series circuit decreased. A threshold level corresponding to a logical 1 was achieved when both GST regions were crystalized, corresponding to the AND logic. Figure 31 shows optical microscope images of this device.

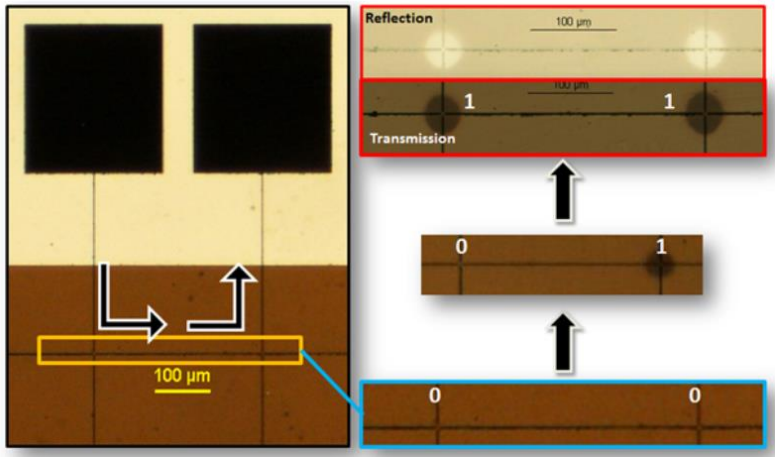


**Figure 31 an opto-electronic AND gate using GST. Image taken from** [70]

## 2.3 Conclusion

GST is a very versatile material that has excellent properties for electronic and photonic memory. Moreover, those properties have recently been inspiring the development of new applications in emerging fields like neuromorphic computing and opto-electronics. In particular, *mixed mode* or the combined operation of optical and electrical domains, offers the potential for the creation of applications like ultra-fast opto-electronic memories, memflectors[61] and ultimately artificial retinas. However, notwithstanding the existing studies on opto-electronic applications, further research is still necessary to address challenges like the design and operation parameters of GST devices operated in *mixed mode*.

Therefore, in this thesis, the aim is to further look into the relation of the optical and electrical responses in nano-devices when the phase change is induced either optically

or electrically, in order to advance the development of the emerging opto-electronic applications, based on GST. The next chapter will describe a first attempt to characterize the optical and electrical response of GST on planar devices, by adapting a previously existing experimental setup.

# 3 PRELIMINARY EXPERIMENTS

## 3.1 Introduction

The absence of previous work that specifically studies GST under *mixed mode* electro-optical operation conditions made it necessary to develop a characterization methodology that included the fabrication of GST nano-devices as well as the configuration of an experimental setup. This chapter presents the evolution of an initial set of *mixed mode* experiments performed using an already existing experimental setup as well as previously produced substrates sputtered with GST. The intention of these experiments was to validate the testing approach and feasibility of observing an optical and electrical crystallization response of GST under optical and electrical stimuli.

There were several steps in adapting the pre-existing experimental set-up. Firstly, it was necessary to fabricate suitable nano-devices. Section 3.2. describes how the this was undertaken. Then, Section 3.3 outlines the experimental set-up which was subsequently developed, and Section 3.4 presents the results which were obtained. The results were sufficiently promising to establish the feasibility of operating GST nano-devices in *mixed mode*. However several limitations related to the device design and experimental

setup made it clear that it would be necessary to build an experimental system from scratch, as well as a different type of device, in order to definitively demonstrate the *mixed mode* approach.

## 3.2 Devices

The first challenge was the fabrication of the nano-devices. The materials available to make the devices were a series of $Si/SiO_2$ wafers, sputtered with GST of different thicknesses, and a variety of capping layers, provided by Polarion technologies. The inventory of available wafers is shown in Table 1.

| Wafer Code | GST225 thickness (nm) | Capping layer material | Capping layer thickness (nm) | Substrate |
|---|---|---|---|---|
| D | 20 | ZSO | 5 | $SiO_2$ |
| E | 50 | ZSO | 5 | $SiO_2$ |
| F | 10 | ZSO | 5 | $SiO_2$ |
| G | 50 | ZSO | 5 | $SiO_2$ |
| H | 10 | $SiO_2$ | 5 | $SiO_2$ |
| J | 50 | $SiO_2$ | 5 | $SiO_2$ |

**Table 1 Inventory of GST225 prepared substrates available for the device fabrication process**

As mentioned previously in Chapter 2, a variety of phase change memory cell designs have been reported in previous papers (see Section 2.1). However, not all of them were suitable for a fabrication process which commenced with a GST substrate like the wafers available for these experiments. The structure chosen for the present

experiments, in terms of nano-manufacturing facilities and materials available, was a planar device design similar to those presented by Krebs *et al* [71] or Lankhorst *et al* [43]. Neither of these planar devices were fabricated from substrates with GST already deposited; instead the researchers first created electrodes and then sputtered GST. Therefore, for this project the fabrication process had to be redesigned entirely. It was necessary to still follow a planar design that would allow the creation of a windowed GST area optically accessible through the top transparent capping layer, and electrically connected to the GST area by adding an electrode at each side of the device. In order to do that, the capping layer had to be removed prior to depositing metal to fabricate the electrodes.

### 3.2.1 Process design

The planar design aimed for consisted of a GST region confined between two lateral electrodes. The processes of fabrication were organized in two stages. During the first stage, the initial substrate was patterned by electron beam lithography and then processed by Reactive Ion Etching (RIE) to remove the capping layer material in the areas where the electrodes would be allocated, exposing the underlying GST. Later, still using the same mask, an adhesive layer followed by a metal layer was deposited to form the electrodes. During the second stage, a second e-beam lithography step was used to pattern a gap around the electrodes. This gap was then produced by a plasma etching step, with the intention of isolating the small GST device area between the electrodes from the rest of the substrate. The schematics of the planned fabrication process can be seen in Figure 32.

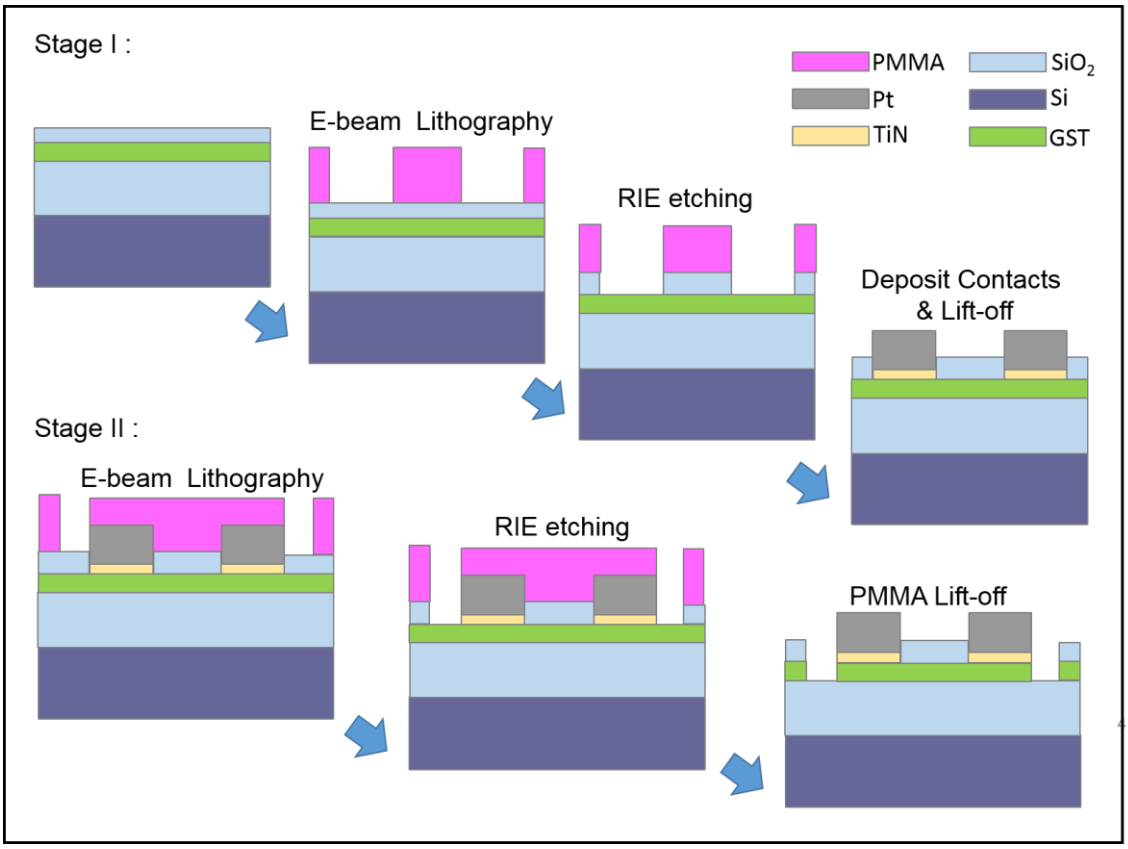


**Figure 32. Schematic of the nano-devices fabrication process. Stage I constrained a small region of GST between electrodes, Stage II etched away the surrounding GST so only the device area was isolated from the substrate**

### 3.2.2 Chip design

After creating the plan for the fabrication process, the next step was to design the masks for the electron beam lithography steps. Masks for both fabrication stages were designed in Autodesk AutoCAD®. During the process of mask design, certain constrains needed to be taken into account, mainly in relation to the electrical access to the devices. Firstly, in order to connect the devices to the measurement equipment, the chip was wire bonded to a custom-made carrier. This meant that bonding pads and connecting lines between such pads and the devices needed to be added to mask design. Secondly, given that the amorphous-to-crystalline transition requires fast falling edges

(nano-second range), the lines were designed to minimize electronic reflections. Thirdly, a constraint came from the need for optical access. This was achieved by a microscope objective with high numerical aperture. As a consequence of the high numerical aperture, the working distance was short (in the order of tens of μm); thus, the integrity of the wire bonds was in danger of accidentally touching the microscope objective. In order to avoid this, long lines between the devices and bonding pads were added so there would be enough space for the microscope objective to move at a safe distance from the bonding pads and the bonded wires. Figure 33 shows the design of the CAD mask used in the fabrication process. The chip design contained 25 devices of five different dimensions in order to test the performance of devices of different sizes. Table 2 shows the dimensions of the devices included in the design.

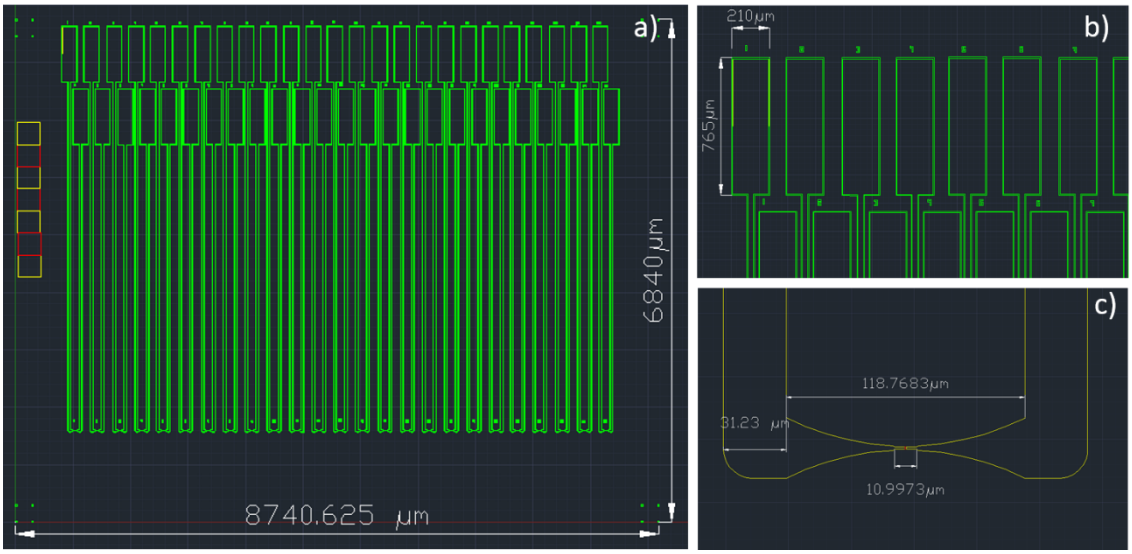


**Figure 33 Nanofabrication chip design. a) Entire chip pattern including alignment markers, b) detail of the bonding pads from the top of the chip, c) detail of the device region. The device is the red square between the lateral electrodes**

| Device | Length (distance between the electrodes) | Width |
|---|---|---|
| 1 | 1μm | 1μm |
| 2 | 500nm | 500nm |
| 3 | 500nm | 100nm |
| 4 | 200nm | 100nm |
| 5 | 100nm | 20nm |

**Table 2 Dimensions of different devices included in the design**

### 3.2.3 Nano fabrication

Prior to fabrication, the most suitable substrates were selected from the ones available listed in Table 1. Substrates with $SiO_2$ capping layer were chosen over those capped with ZnS-$SiO_2$ with the intention of minimizing current leakage between the electrodes through the capping layer, which may affect the resistance measurements of the GST device area. This is because ZnS is a semiconductor and ZnS co-sputtered with $SiO_2$ tends to form connected nuclei within the $SiO_2$ matrix[72].

*E-beam lithography optimization*

The devices used for the preliminary experiments were processed in a Nano Beam NB4 electron beam lithography system. In order to obtain the best possible resolution, expose dose tests were performed on samples spin coated with 400nm of Poly-Methil-Meta-Acrylate (PMMA), since this was the e-beam resist layer used for chip patterning. During the expose dose characterization process, it was found that the edge correction software of the e-beam depended on a set of parameters to properly account for the

electron scattering properties of the sample. Therefore, it was necessary to adjust the software settings according to the electrical characteristics of the GST substrates used because they differed from the standard $SiO_2$ on Silicon. After these tests, the smallest obtained feature was in the order of 100nm.

*Plasma etching recipe optimization*

As mentioned previously, plasma etching was included in the process design as a method to remove the capping layer of the initial wafer. This was one of the most challenging steps in the fabrication process because a very precise etching rate was required in order to minimize over-etching the GST layer underneath. Therefore, fine tuning of the plasma etching recipe was required.

First fabrication attempts were made with samples taken from wafer H (10nm GST, 5nm $SiO_2$, as listed in Table 1). The standard $SiO_2$ plasma etching recipe uses a combination of $CHF_3$ and $O_2$. However, it has been shown that processing in the presence of oxygen causes oxidation of the GST layer[73]. So in order to avoid oxidation, a custom recipe without oxygen was developed. In the standard recipe, the function of oxygen is to help to remove organic build-up from the surface during the etching process[74]. If oxygen was not used, another mechanism to remove build-up was required. The alternative mechanism selected was ion bombardment achieved by adding Ar in order to sustain the plasma and decreasing the pressure of the reactive chamber in comparison with the standard recipe. This recipe allowed non-reactive Ar ions to collide energetically against the surface, producing a mechanical etching effect. The drawback of this combination was an observed increment in the etching rate of the PMMA mask, as well as increased sensitivity to temperature variations. Additionally, it was found that during etching characterization tests, that the etching rate of GST compared to $SiO_2$ was significantly higher (GST = 3.5nm/s, $SiO_2$ = 0.1nm/s). This

turned out to be problematic, because due to the natural thickness variations on the wafer, certain areas of the GST were etched away before the capping layer was completely removed from other areas, resulting in a very rough surface with peaks of $SiO_2$/GST and pits into the etched GST. Figure 34 shows an optical microscope image taken after a flat etching test on a sample made from wafer H. Irregular etching can be clearly observed.

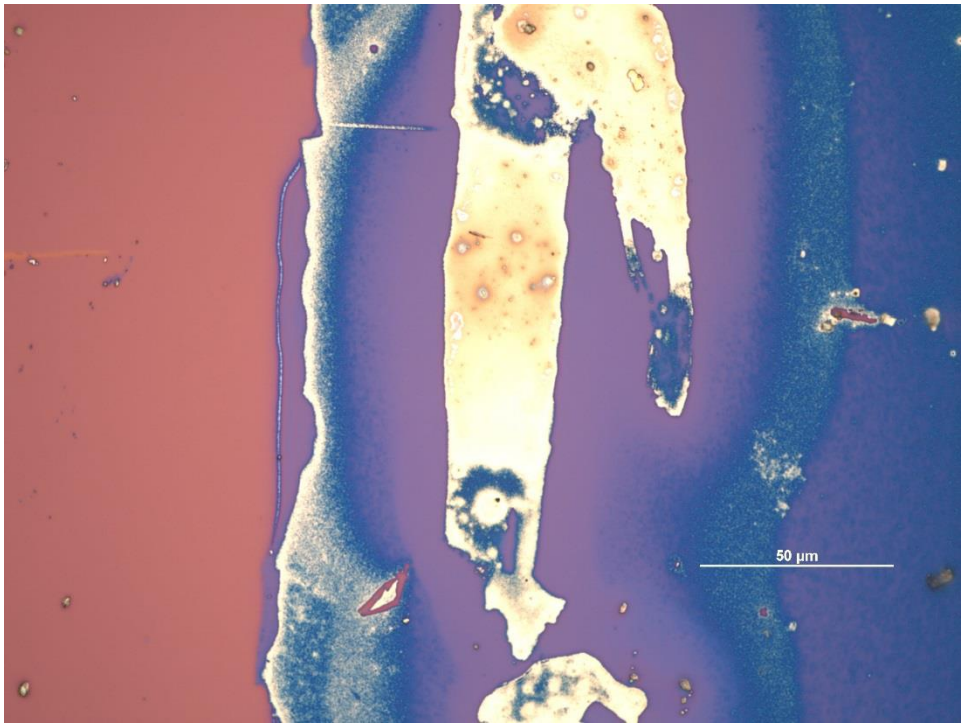


**Figure 34 Irregular etching of GST on a flat sample of wafer H. White metallic areas correspond to initial GST+SiO2, blue corresponds to exposed GST areas. Doted areas show where the SiO2 capping layer was partially removed exposing GST regions to etching**

After trying several combinations of parameters to optimize the recipe, it was discovered that it is not possible to obtain a continuous GST exposed area on samples taken from wafer H, removing just the top 5nm of $SiO_2$ without completely etching the

5nm GST in certain areas. The solution to this problem was to use a different substrate. As a consequence, further experiments were performed with samples from wafer J (see Table 1). Table 3 shows the final optimized recipe used to etch 8nm into the initial substrate (5nm $SiO_2$ + 3nm GST), compared to a standard plasma etching recipe for $SiO_2$. As mentioned previously, this recipe was sensitive to temperature, so in order to obtain repeatable results, a dry run without any samples in the chamber was carried out prior to the etching process starting from the RIE machine at room temperature.

| | Standard $SiO_2$ etching recipe | Optimized $SiO_2$ etching recipe without $O_2$ |
|---|---|---|
| Chamber pressure | 37.5 mTor | 15 mTor |
| RF Power | 100 W | 50 W |
| Ar | 0 sccm | 5 sccm |
| $CHF_3$ | 100 sccm | 5 sccm |
| $O_2$ | 2.5 sccm | 0 sccm |
| Etching rate | 36 nm/min $SiO_2$ (thermally grown) | 48s for 5nm $SiO_2$(sputtered) + 3nm GST |

**Table 3 Comparison of standard SiO2 RIE etching recipe vs. custom developed recipe without Oxygen. (sccm, standard cubic centimetre per minute).**

*Metal sputtering*

The next step after removing the capping layer was to deposit a metal to form the electrodes. Initial fabrication trials used a combination of 3nm Cr as an adhesive layer, followed by 30nm Au, both deposited by thermal evaporation. Later, it was found

during electrical testing of the devices that the increase of temperature in the surroundings of the device melted down the electrodes, as can be seen in Figure 35a. Although the melting point of GST is lower than the Au, which suggests than the GST was also overheated and melted if the Au electrodes were destroyed. Another problem was the potential oxidation of the GST when exposed to air while being transferred between the RIE and the thermal evaporator vacuum chambers, as it has been shown that GST oxidizes in contact with air, starting by forming $GeO_2$ [73]. The solution to those problems was to use Pt instead of Au, because it has similar noble properties but a higher melting point that would survive overheating, and to replace thermal evaporation with RF sputtering.

In the case of RF sputtering, deposition is made by plasma. The plasma present in the sputtering machine allows for a technique called *back etching*, which is in principle similar to the RIE etching technique. The final set of devices were fabricated using this procedure, as follows. The sample was back etched in order to remove a possible layer of GST oxidized during the transport between the RIE and sputtering chambers. Finally, 40nm of titanium nitride was used as an adhesive layer and 70nm of platinum were sputtered on the device. Titanium nitride is commonly used in PCM fabrication as a conductive electrode (30-70 μΩ/cm) that blocks electro-migration[42]. The subsequent lift-off process of the metallic layer involved a bath in hot acetone and ultrasonic cleaning. Figure 35b shows an optical microscope image of a device completed up to Stage I of the fabrication process. It is important to mention that only devices of type 1, 2 and 3 from the ones listed in Table 2, were manufactured successfully. Devices of types 4 and 5 were short-circuited, due to the very small gap of the device area.

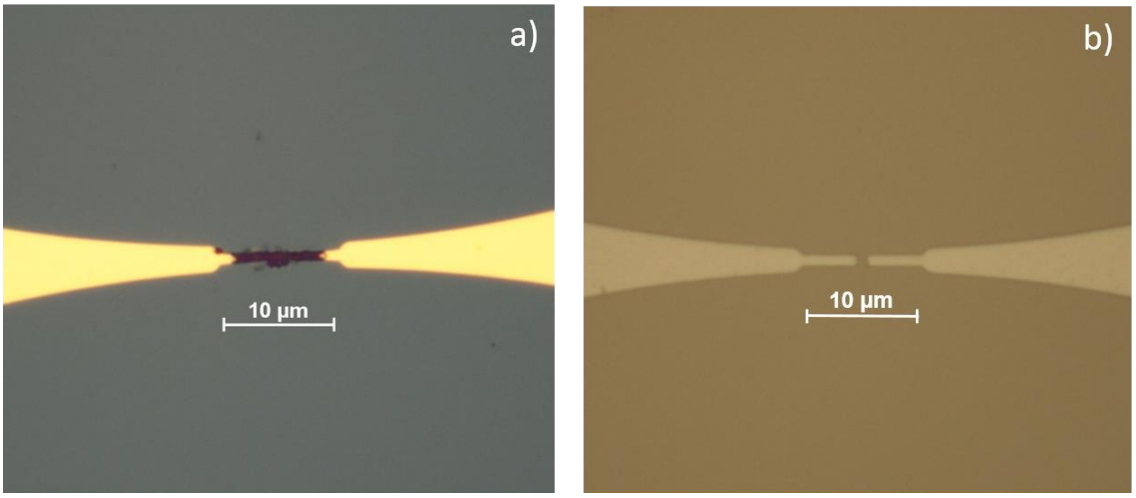


**Figure 35 Optical Microscope Image of a) Melted Au electrodes after I/V measurement, b) 1µm device fabricated up to Stage 1 using Pt electrodes.**

## 3.3 Experimental setup

### 3.3.1 Optical system

In order to perform *mixed mode* experiments, it was required to develop an instrument capable of shining laser pulses on the devices to optically induce a phase change of the active material. The instrument used for the preliminary experiments was a legacy laser system used by a previous research group. It was built on a modified microscope by adding a combination of semi-transparent and dichroic mirrors in order to align a laser and the visualization elements to the same optical axis, allowing visualisation of the laser spot on the target via the optical microscope. It was also possible to integrate an optical power meter to measure the power reflected by a certain area of the target while being illuminated by the laser. The setup used a low cost 25mW 405nm laser diode; such laser diodes are easily accessible due to the mass adoption of Blu-ray® technology. The laser diode was fixed to the body of the microscope by a custom-made fixture that contained a collimating lens (ThorLabs C671TME-405) as well as X, Y

displacement and kinematic mounts. All these elements permitted the precise alignment of the laser to the optical axis of the microscope. The objective used was a dry 0.9na 100x; the coarse focus was controlled with the mechanical mechanism of the microscope and the fine focus (100µm range) with a microscope objective piezo actuator. The reflected intensity of the sample was measured by coupling the photo-detector of an optical power meter (Newport NP1830C) to the body of the modified microscope. Figure 36 shows the optical setup as well as a schematic of its configuration.

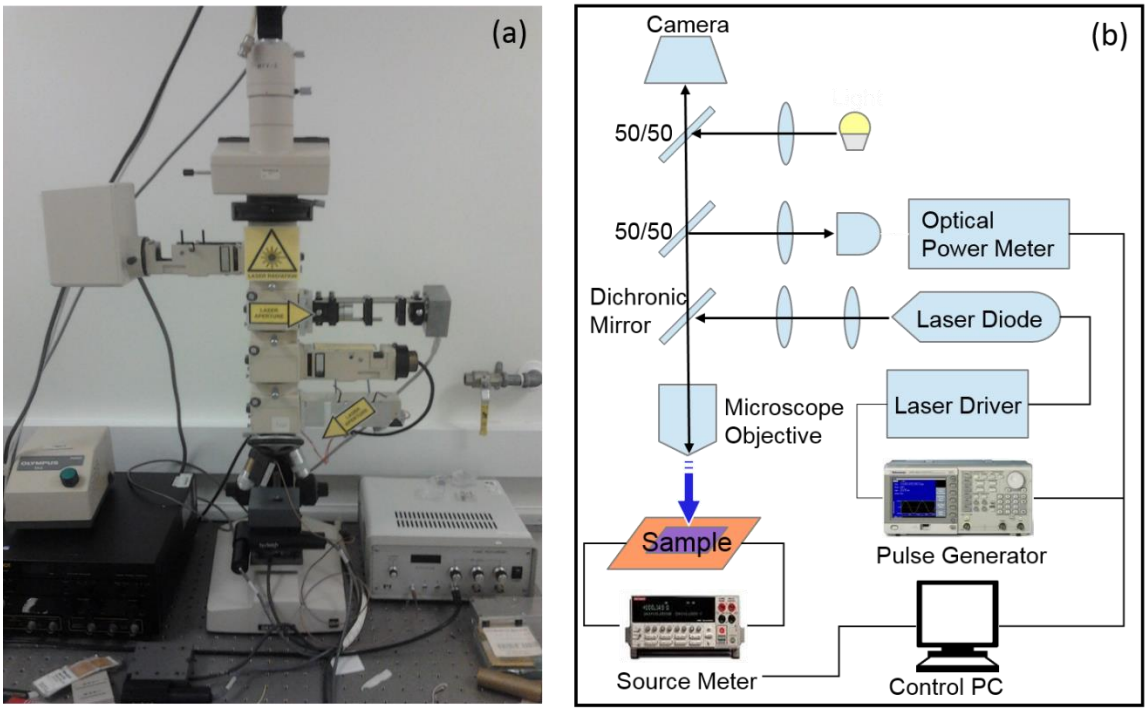


**Figure 36 Initial set-up. (a) Initial Optical Set-up built from a modified Microscope. (b) Schematic of the Optical and Electronic components used for the measurements**

*Optical system characterization*

The first activity performed prior the experiments was to characterize the amount of optical power, in terms of the current applied to the laser diode, at the same time

considering the internal losses of all optical elements of the setup. To do this, the optical power meter was located under the microscope objective and a series of measurements of current vs. effective optical power were obtained. This information is shown in Figure 37.

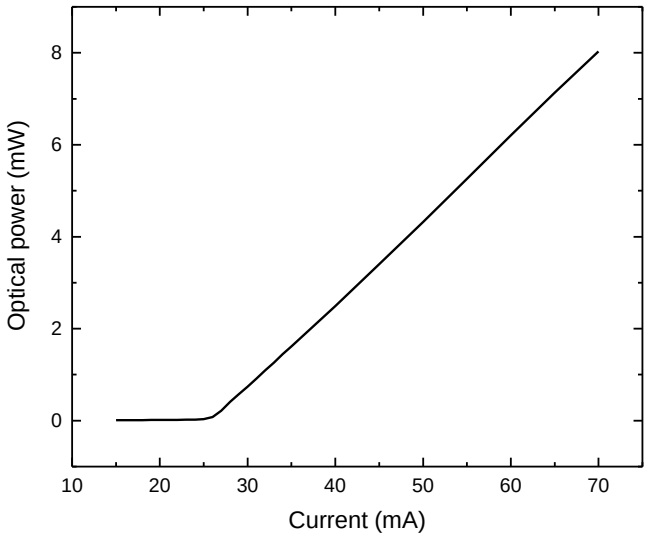


**Figure 37 Optical power vs. applied current**

## 3.3.2 Electrical System

Another key part of the set-up was the electronics system required to perform electrical measurements on the devices and also to control the optical components. The resistance measurements were performed with a source meter (Keithley 2400) which accessed the devices via SMA connectors located in a custom made PCB where the chip was glued and connections between devices and circuit pads were made by wire bonding. The laser was controlled by a limited capability Melles Griot laser diode driver which sourced a selectable DC current used for polarization, and also provided modulation to a higher pre-set current value via an external signal. This external signal, which was used to control the pulse width, was sourced by an Arbitrary Function Generator (Tektronix

AFG3102) operating in the pulse feature. It is important to mention that due to the response time of the laser diode driver, it was able to produce a minimum edge of 1µs, limiting the pulse length to 2µs. This limit is important, because it is known that re-amorphization occurs by fast melting-quenching the material with pulses of maximum duration of 200ns[75] with ns range falling edges. Therefore, it was not possible to achieve reamorphization with this equipment, limiting the optically induced phase change experiments to just amorphous to crystalline transition. This was one of the main factors which prompted the need to build a new system.

### 3.3.3 Mechanical design and other components

The X, Y motion of the target was performed by a pair of linear stages actuated by legacy Burleigh pico-motors. This configuration allowed the laser to be aimed at the device, move between devices and perform raster scans of an area of interest. The minimum discrete step of the pico-motors in combination with the stages was of 100nm over a displacement range of 25mm. All instruments were coordinated and remotely operate by a PC running a custom made LabView® program specific for the *mixed mode* experiment.

## 3.4 Experimental results

In order to promptly test the viability of the *mixed mode* electro-optical operation, experiments were performed with devices fabricated up to Stage I. Doing this made it possible to evaluate the feasibility of the devices before proceeding with Stage II of the fabrication process. This approach also followed early unsuccessful fabrication attempts that proved the patterning and etching processes of the Stage II to be challenging.

### 3.4.1 Electrical characterization

The first step to identify the operational characteristics of the devices was to perform electronic testing. This was done by obtaining I/V traces using a Keithley 2400 source meter running a custom made acquisition program written in LabWiew®. The electrical testing confirmed a typical GST crystallization I/V response, shown in Figure 38a. However, 60V were required to switch a device of 1x1μm dimensions. The need for such a high voltage was mainly a consequence of the device geometry, since a threshold field of 56V/μm[42] is necessary to induce switching of GST.

Additionally, from the I/V curve shown in Figure 38a, it is possible to extract the amorphous and crystalline resistive values before and after switching. Such values correspond to 15.5MΩ in amorphous state and 4.8MΩ in crystalline. Such resistance change is significantly smaller than the conventional $10^3$ factor [76] expected. A possible cause for this could be that the device is intrinsically highly resistive. In such a case, the resistance of the electrodes, in addition to the contact resistance between the electrodes and the GST, accounted for a large part of the total device resistance in contrast to the resistance of the GST area between the electrodes. Hence, the change of resistance due to the phase change of GST was dominated by the greater resistive value of the overall device.

After the I/V testing, the switched device was inspected in an optical microscope. It was found that the electrically induced crystallization occurred not only in the device area confined between the electrodes, but also in the surroundings, as shown in Figure 38b.

Additionally, dendritic formations were observed in the crystallized region, which agrees with existing models of electrical conduction in GST. Those models state that the effect of electric field enhances crystallization[37][39] and can produce dendritic

structures[77]. Hence, due to the large crystallised area and the high voltage required to induce the crystallization, it was not possible to electrically reverse the devices to the amorphous state. Therefore, further electrically induced phase change experiments were unfeasible.

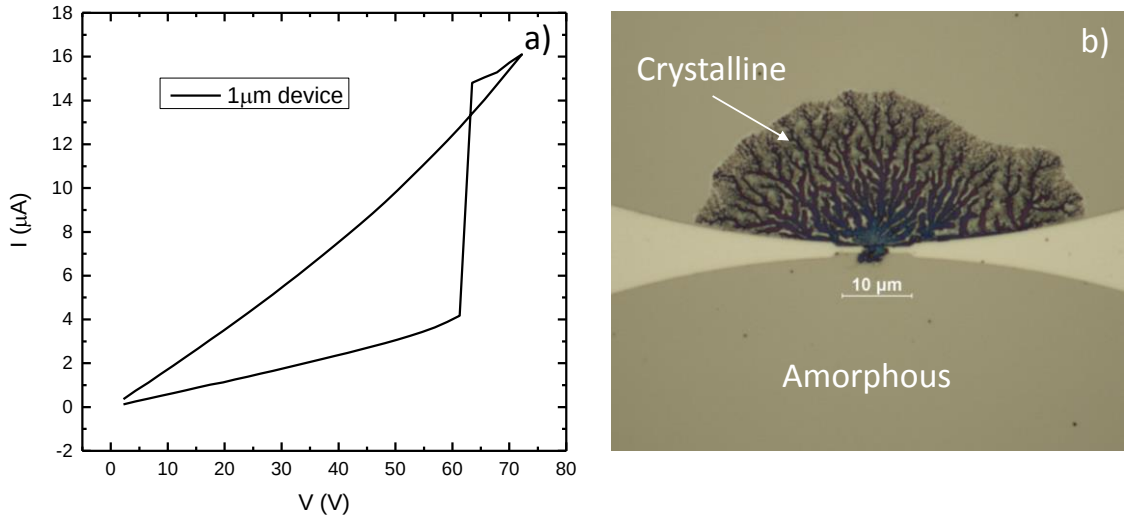


**Figure 38 Switching response. a) I/V curve of a 1μm device. Threshold switching occurred near 60V due to the high resistance of the device. b) Optical microscope image of the device after I/V switching, GST area around the device was also crystallized with a dendritic pattern.**

## 3.4.2 Optical Characterization

The next experiment performed was the study of GST upon optically induced crystallization. It was necessary to first identify the power required to produce accumulative crystallization. By varying the amount of current and the pulse length, a matrix of writing areas was created on a sample of the same substrate used for the device's fabrication. Figure 39 shows the effect of different powers and time pulse combinations on a sample of J wafer substrate. An increment in reflectivity indicates areas being crystallized. It can be seen that there is no significant difference between

1μs pulses and shorter ones, due to the time response limit of the laser driver explained previously. This characterization method was an adaptation from the one used by Weidehhof [75] but explored only low powers to identify a set of parameters that would produce partial crystallization.

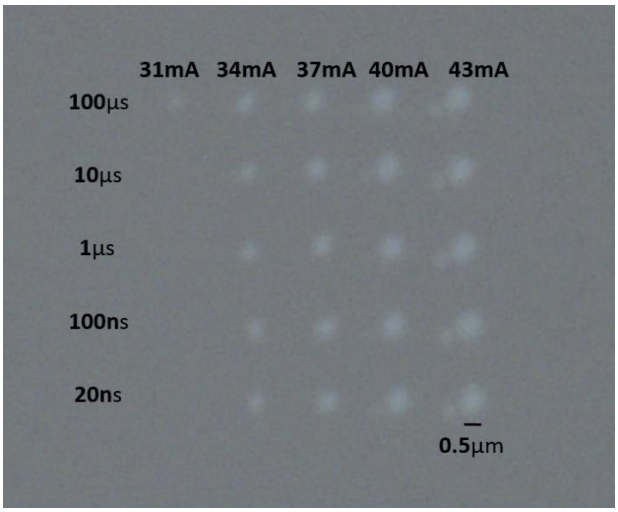


**Figure 39 Laser power calibration on substrate J. Columns indicate different currents applied to the laser diode, rows pulse duration.**

### 3.4.3 Mixed mode experiment, optically induced crystallization.

Despite all previously identified limitations, it was nevertheless possible to use the experimental system to study one combination of mixed mode electro-optical operation by optically inducing crystallization of the GST while measuring the change in resistance as well as the intensity change of the reflected power. This experiment was performed on a 500x100nm (size 3) device because it was the smallest successfully manufactured type. Although better observations of the change in reflectivity could be made with larger devices, this holds only if the crystallization occurred homogeneously across the device area. In this case however, the laser spot size was in the order of 500nm (as shown in Figure 39).

Therefore, using a device smaller than the laser spot size increases the chances of homogeneous laser exposure. So, in order to crystalize the GST, various series of 20 identical 1μs optical pulses were applied to the device. The power of each series of pulses monotonically increased between 0.5 to 5.5m. Given that pulse accumulation depends on the power applied (as was shown by Wright et al [54]), increasing the amount of power of the pulses allowed for the exploration of different partial crystallization conditions in a short period of time. The aim of reducing the time required to run the experiments was to minimize the effect of the mechanical drift of the stage, which was observed to accumulate over time. Reflectivity measurements were obtained by illuminating the device, with the laser operating in continuous mode at low intensity (0.3mW) to avoid further crystallization which would alter the experiment. Resistance measurements were performed by obtaining a low voltage (1V) I/V curve. Each I/V was linearly fitted and the resistance value was extracted as the reciprocal of the slope for each curve.

Figure 40 shows the obtained results. An increment in reflected power can be observed simultaneously with a decrement in the electrical resistance, whilst different series of accumulative pulses were consecutively applied to the device [78]. This result shows a clear correspondence in the response of the optical and electrical domains when the GST changes from amorphous to crystalline. Regarding the change of reflectivity, two raster scans were acquired before and after applying optical pulses to the device additionally to single point measurements performed after every pulse. As can be seen in the reflectivity scans shown in Figure 41, an increment in the reflected power in the area of the device is assumed to be due to crystallization. However, given that the device fabrication was only completed until Stage I, the GST film of the substrate was still present around the area of the device confined between the electrodes. Therefore, it

is reasonable to assume that crystallization of the area adjacent to the device also occurred. This explains the increment in reflected power also in the area surrounding the device shown on Figure 41b.

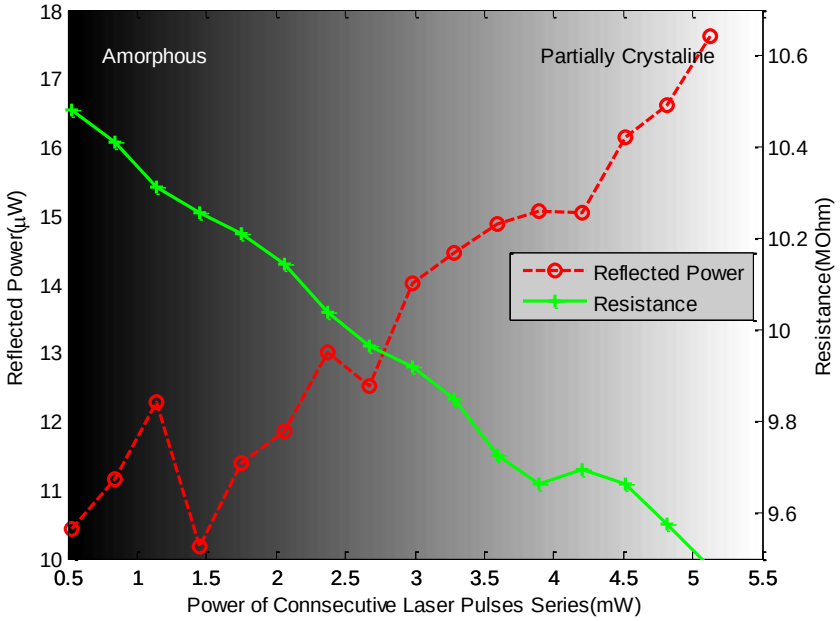


**Figure 40 Result of Preliminary Mixed Mode experiment, optical excitation optical and electrical measurements, applying a series of laser pulses of monotonically increasing power** [78]**.**

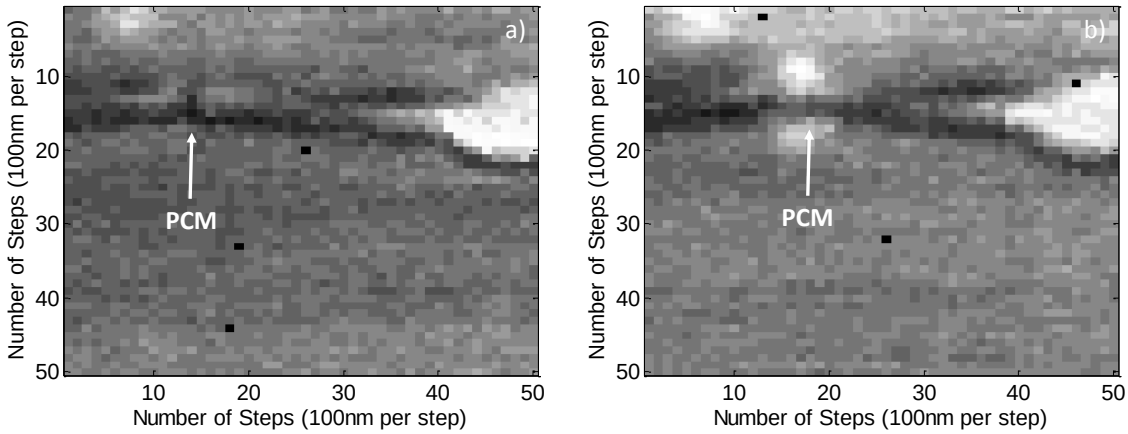


**Figure 41 Reflectivity maps obtained by raster scanning the area around the device a) before and b) after the experiment.**

These observations on the evolution of reflectivity versus electrical resistance, agree with a similar experiment previously reported by Liang *et al* [67] and represents a step forward in the realization of opto-electronic devices in comparison to what has been reported in the literature, by showing the feasibility of using GST as an active material for the fabrication of opto-electronic devices.

## 3.5 Conclusion

During the stage of preliminary experiments, the principal research question addressed was: Is it possible to electrically measure an optically induced phase change, or vice versa? In order to address this question, it was necessary to design and fabricate nano-devices while simultaneously designing the *mixed mode* experiment using the limited optical system available. This system needed to be characterized and updated and, a custom-made code was developed for the automation of the measurements.

With the fabricated devices and experimental setup, it was possible to test one of the *mixed mode* combinations, optical excitation and optical - electrical measurements. The results of this experiment showed a clear correlation between the change of electrical resistance and reflectivity on the amorphous to crystalline transition, proving viable the possibility of operating GST nano-devices in optical and electrical *mixed mode* operation.

However, several limitations were encountered. The designed architecture proved difficult to fabricate because of the small tolerance to misalignments between lithographic steps. Hence attempts to fabricate devices to the Stage II of the process were not successful and the experiments were performed with devices completed until Stage I. In addition, the devices were too resistive to operate electrically without

experiencing electric breakdown. This was caused by a combination of high contact resistance and high resistance of the GST device area itself; this confirms Lankhorst *et al*'s prediction that GST planar devices would have a maximum limit gap of 50nm to be electrically operable [43]. As a consequence, it was only possible to perform optically-induced phase change experiments. Moreover, the frequency response limit of the laser diode driver impeded the possibility of investigating the amorphous-to-crystalline transition because temperature quenching required pulses with sharp (nano-second range) falling edges that were impossible to obtain.

All the previously mentioned limitations, in addition to extra ones, including: mechanical drift, low-step resolution of the stage, sensitivity of the setup to vibration due to the vertical configuration and astigmatism of the laser beam; pointed to the need for a complete redesign of the optical setup, as well as the fabrication of the nano-devices in order to further study the response of the GST based opto-electronic devices in both optical and electrical domains. Having done the preliminary experiments described in this chapter, this could be undertaken in the confidence that a clear correlation between optical and electrical domain exists.

# 4 EXPERIMENTAL SET-UP

## 4.1 Introduction

As described in Chapter 3, preliminary experiments made it evident that the set-up used had several limitations with respect to mechanical, electrical and optical operation properties. Therefore, in order to continue with the study of *mixed mode* electro-optical operation of GST, a new experimental set-up with better characteristics was required. The following features were identified. In order to aim the laser accurately on the device, a raster reflectivity scan was necessary. This, in turn, called for the improvement in reproducibility of the stage position, as well as a reduction of the drift due to thermal expansion and mechanical relaxation of the components. Additionally, by reducing mechanical drift, the time available to perform the test would also increase, allowing for better focusing and aiming into the area of interest. Improvement in the scan step resolution was also required, in comparison to the 100nm step resolution provided by the pico-motors of the former setup. Also, nano-second range optical and electrical pulses were needed to induce amorphization of GST devices. All of the before

mentioned requirements were subsequently incorporated into new experimental setup in a way which is described in detail in this chapter.

The requirements for the optical component of the experimental setup corresponded closely to a laser-scanning microscope. Such an instrument produces images by raster scanning a focused laser beam on a given sample and acquiring the intensity of the reflected signal at every point during the scan. However, higher power than that required to simply acquire reflectance scans (3mW) was also needed to optically induce phase changes of GST (~60mW). One important decision in the current design was the use of fibre-coupled optical components. Such components allow a reduction of the setup footprint, simplify the alignment and improve the sensitivity to vibration. Figure 42 shows a simplified schematic of the custom-made laser scanning microscope.

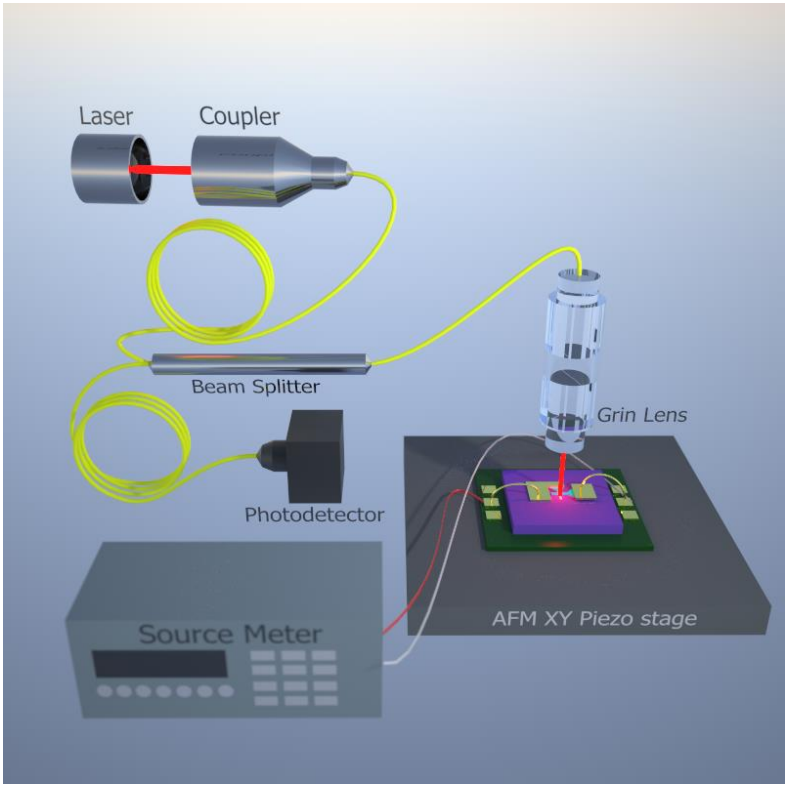


**Figure 42 Simplified schematic of the experimental set-up, including the core elements of the custom-made laser scanning microscope.**

## 4.2 Optical components

After deciding the use of fibre-coupled optics, the next design decision focused around the operating wavelength. GST has the advantage of being absorptive in a very large spectrum, from UV to IR in the telecommunication bands (~1550nm) and beyond. However, the resolution of the laser-scanning microscope depends on the optical probe, or in practical terms, the laser spot size used for the raster scanning process. The spot size in the far field is diffraction limited and depends on the wavelength selected. The logical decision then would be to select of the shortest available wavelength. Low cost 405nm laser diodes have recently become easily accessible due to their use in Bluray® disk technology. However, near UV optics, and in particular fibre-coupled components associated with this wavelength, are significantly more expensive and sometimes unavailable due to higher absorbance near the UV of commonly used glasses. The alternative was to use a 660nm. Low cost laser diodes of this wavelength are also easily accessible due to their use in DVD® technology. Likewise, a variety of fibre-coupled components for this wavelength are available. For these reasons, the optical components of the system were built considering a 660nm wavelength choice.

### 4.2.1 Laser

In order to reversibly switch GST, nano-second length pulses are required. To produce such short pulses there are two alternatives; one is to use a continuous laser coupled to a shutter mechanism, and the other to electronically pulse a laser diode. The first alternative was found to be significantly more expensive and complex than the second one, specifically when working with wavelengths in the visible range because most of the shooters and amplifiers available were designed for telecom bands. Moreover, the

second alternative was compact and economical, and it only required the control electronics and a fast response laser diode.

The laser diode chosen for this experimental setup was therefore a 658nm ROHM RLD65PZB5 with rise time of 50ps, maximum pulsed power 250mW at 80ms pulse width, according to the specifications. The laser diode was electronically driven by a combination of a DC polarization bias and nano-second pulses. Such a combination allowed the diode to remain continuously in the linear lasing region during the pulsing operation. The mixing of both signals was achieved by a custom-made bias tee, fabricated using a Minicircuits PBTC-1GW+ bias tee integrated circuit, with operation frequency range of 100 KHz to 1GHz for the RF port. Figure 43 shows an image of the custom-made bias tee.

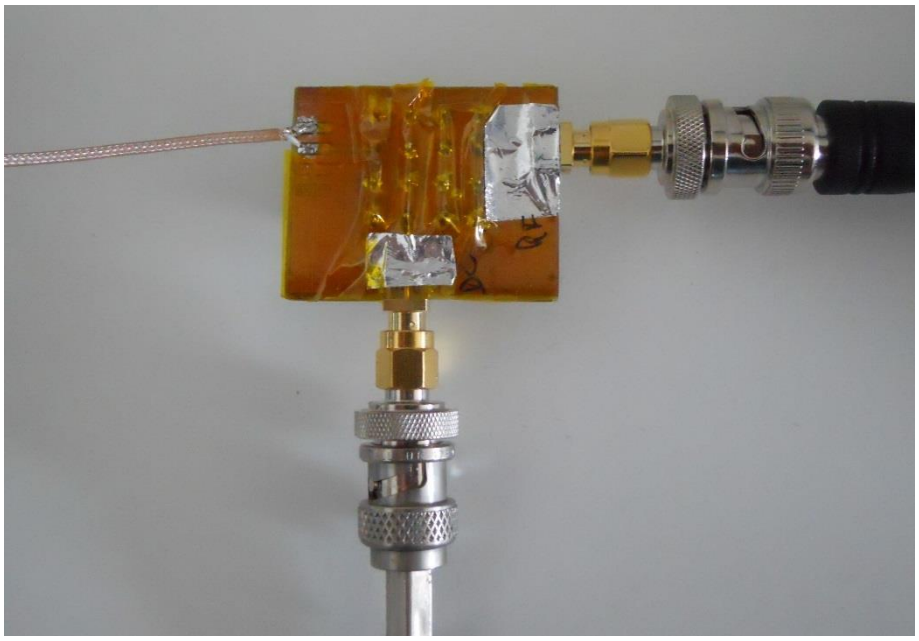

**Figure 43 Custom-made bias tee, showing both DC and RF ports, and the coaxial output connected to the laser diode.**

The laser diode was then mounted on a low-cost diode housing (OFL153) which also contained a plastic moulded aspheric lens for beam collimation. Next, the laser beam

was coupled to a single mode optical fibre (Thorlabs SM600) by means of a free space to fibre laser coupler (Thorlabs F280APC-B). This coupler belonged to a family of products designed to work at 633nm central wavelength. It was selected from other couplers of the same the product line because it allowed coupling to larger beam sizes, which was required in this case due to the laser beam diameter being approximately 3mm after collimation. Figure 44 shows the schematic of the different optical components that comprise the system.

In addition to the advantages mentioned before about the use of fibre-coupled optics, coupling to a single mode fibre corrected various common problems related to the quality of a laser beam obtained by a laser diode. Those problems were mainly eccentricity of the beam and astigmatism, but also other beam related aberrations caused by the quality and alignment of the optics were compensated. Coupling the laser to a single mode optical fibre allowed the use of a low cost laser source (diode) and low cost collimation optics whilst still obtaining a high quality Gaussian beam in the output side of the optical fibre. It is also important to mention that commercially available fibre-coupled laser diodes exist. However, none of the analysed options fulfilled the requirements of power, speed and cost for the development of the present experimental setup.

### 4.2.2 Coupling mount

The laser diode module and the laser coupler were aligned by a 5-degrees of freedom custom-made holding mount that is shown in Figure 45. The diode housing was mounted on a combination of two linear stages to align X and Y positions. The laser fibre coupler was supported by a kinematic mount to correct for rotational misalignment.

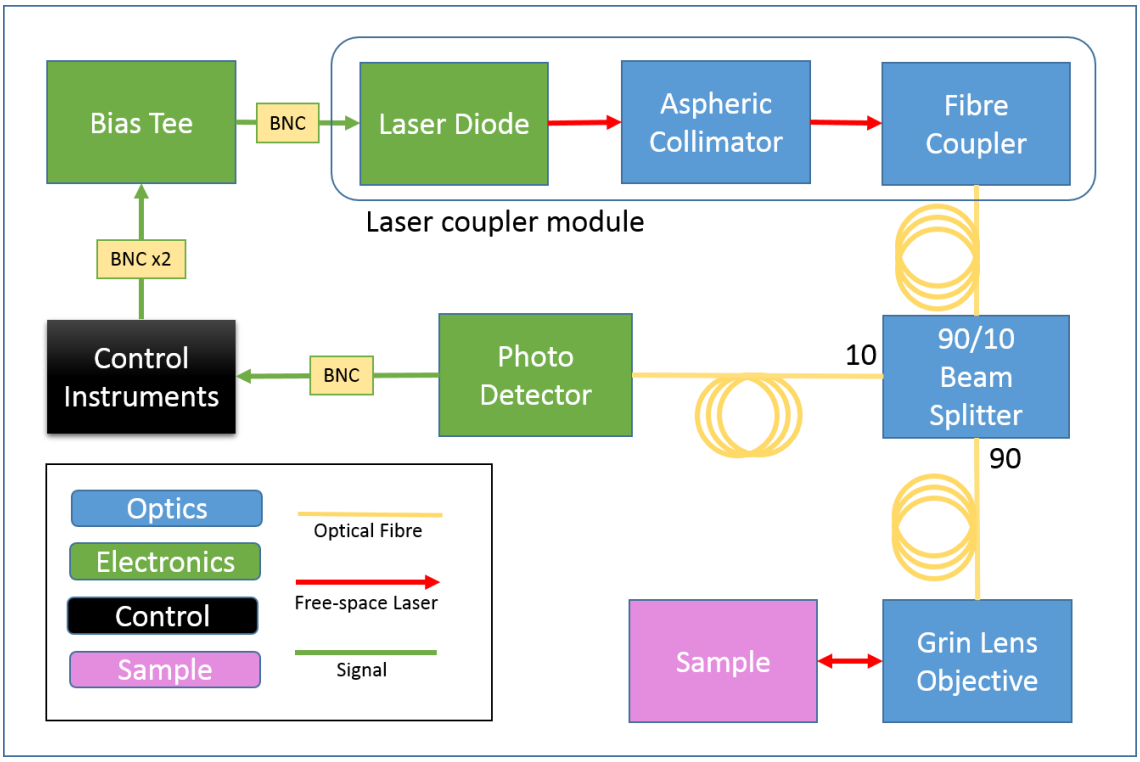


**Figure 44 Schematic diagram of the optical components of the experimental setup.**

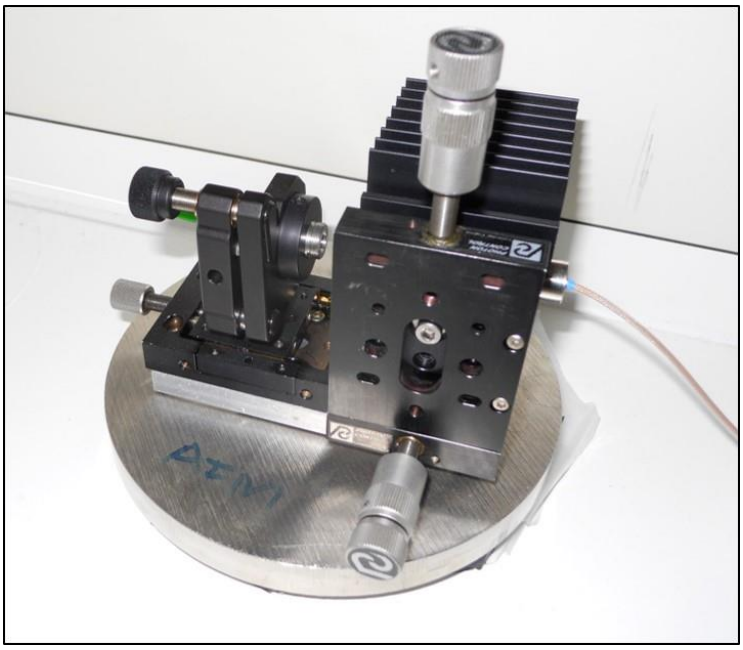

**Figure 45. 5 Degrees of freedom custom-made laser coupler module.**

### 4.2.3 Beam splitter

After coupling the laser to the optical fibre, the fibre was connected to a 90:10 beam splitter (Thorlabs FC632-90B-APC). The 90% transmission path was connected to the laser output and the 10% output of the reflected signal was connected to the photo detector (Figure 44). This arrangement caused the reflected signal to be attenuated by 90% by the beams splitter, but it provided the best possible combination to maximize the amount of power transmitted to the objective. Despite the attenuation, the reflected signal was still measureable by the photodetector.

### 4.2.4 Confocal GRIN lens objective

The laser coming from an optical fibre is divergent, therefore it was required to implement a way to illuminate the sample with enough power to induce the phase change as well as to couple the reflected signal back into the fibre in order to measure the reflectance and construct an image during the raster scan. One possible set-up, the 'near field', would have avoided the use of additional optics by positioning the optical fibre in closed proximity to the sample, the same way as found in the Near-field Scanning microscopy (NSOM) technique. However, a long working distance was also a requirement to allow space between the fibre and the sample to access the devices electrically by wire bonding. Additionally, given that this technique only works in the near field, the fibre would need to be positioned nano-metres away from the sample; achieving positioning with such precision would require a sophisticated closed-loop controller and a way to accurately sense the position of the fibre. Those requirements make the near field alternative unviable. Hence, it was necessary to implement a 'far field' set-up, and this required the addition of extra optic elements to focus the laser beam from the optical fibre into the sample.

One of the far field options was to use a commercial microscope objective with a long working distance and high numerical aperture; this would minimize the laser spot size and consequently, increase the resolution of the laser scanning microscope. However, commercially available long working distance and high numerical aperture objectives were found to be uneconomical and bulky, and so this alternative was rejected.

The next option was to use a grin lens and couple it to the optical fibre. A grin lens is a cylindrical piece of glass, with a radial Gradient Refractive Index (GRIN). Such a refractive index gradient allows this type of lens to behave like a normal thin lens by bending the light as it traverses through the lens. GRIN lenses have a small footprint, are economical and can collimate light to diffraction limited spot. For these reasons they are commercially used as the optical element in fibre coupled laser diodes.

In contrast with normal thin lenses which optical power depends on the curvature, the power of GRIN lenses depends on the pitch, which is a function of the gradient constant (k) and the length of the lens. One pitch is the equivalent to a $2\pi$ rotation of the incident light beam as it is shown in Figure 46.

Due to the small footprint and low cost, the GRIN lens alternative was chosen to focus the laser beam from the optical fibre on the sample. From the variety of lenses commercially available, the one chosen was Thorlabs GRIN2906, in combination with a ferrule terminated single mode optical fibre (Thorlabs SMPF0206-APC). Technical characteristics of those components are shown in Table 4.

The GRIN lens and ferrule terminated optical fiber were assembled using a borosilicate glass sleeve (Thorlabs 51-2800-1800) that would provide support for axial alignment, the components prior assembly are shown in Figure 47.

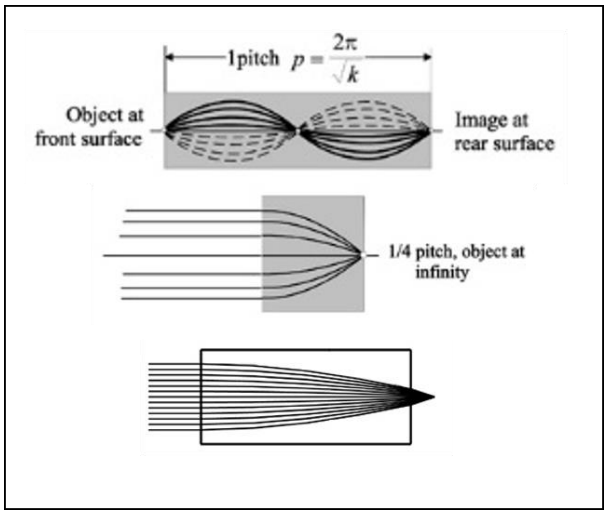


**Figure 46 Grin lenses. Top: Description of pitch in a GRIN lens. Centre: 0.25 pitch commercially traded as Selfoc®. Bottom: 0.3 pitch lens. Images adapted from: "Optical Design Fundamentals for Infrared Systems, Second Edition", Max Riedl, SPIE press (2001).**

| **GRIN lens GRIN2906** | **Optical Fiber SMPF0206-APC** |
|---|---|
| Wavelength: 650nm | Wavelength: 633-780nn |
| Pitch: 0.29 | Central Mode size: 5.3µm |
| Length: 5.380mm | Core refractive index: 1.46147 |
| Central refractive index ($n_g$): 1.6073 | |
| Grin lens gradient: 0.339mm$^{-1}$ | |

**Table 4. Selected GRIN lens and optical fibre characteristics**


**Figure 47 GRIN lens objective components prior assembly. Image reproduced from https://www.thorlabs.com.**

When using the GRIN lens, the working distance and spot size values depend on the distance between the fiber and the lens. So it was required to carefully select the position on the assembly to optimize the trade-off between working distance and spot size. Additionally, physical limitations of the components also needed to be considered. The glass sleeve length was 10mm and the diameter of the grin lens and ferrule terminated optical fiber were 1.8mm. Thus in order to keep the lens and ferrule aligned, a minimum of 1.8mm was required on each side to hold the components in place. This limited the maximum possible distance to 6.4mm. The optimum position was chosen from different combinations of spot size and working distance values, calculated by a transfer matrix model created by Jung *et al* [79]. Figure 48.a shows the model equations and how they relate to the layout of the components. The optimum values for working distance and spot size selected were 328 µm and 2.24 µm respectively, for a back separation of 4mm (Figure 48.b-d). One advantage of this configuration was that the single-mode optical fibre acted as a pinhole in the path of the reflected signal, effectively creating a confocal configuration [80].

### 4.2.5 . Photo detector

Once acquired by the confocal objective, the reflected laser signal was transformed into a voltage signal by a Newport 2001-FC Photodetector. This Silicon photo-detector operates in the visible spectrum (300-1050nm) and has a wide input power range (1pW–10mW). It also includes an integrated trans-impedance amplifier with multiple gain settings (Max. $3x10^4$). However, the maximum frequency response is 100 KHz and rise time of 2µs, limiting the acquisition only to information obtained while performing raster scans with a continuous wave (CW) laser illumination. Detection of pulses used to induce phase change was not possible with this photo detector.

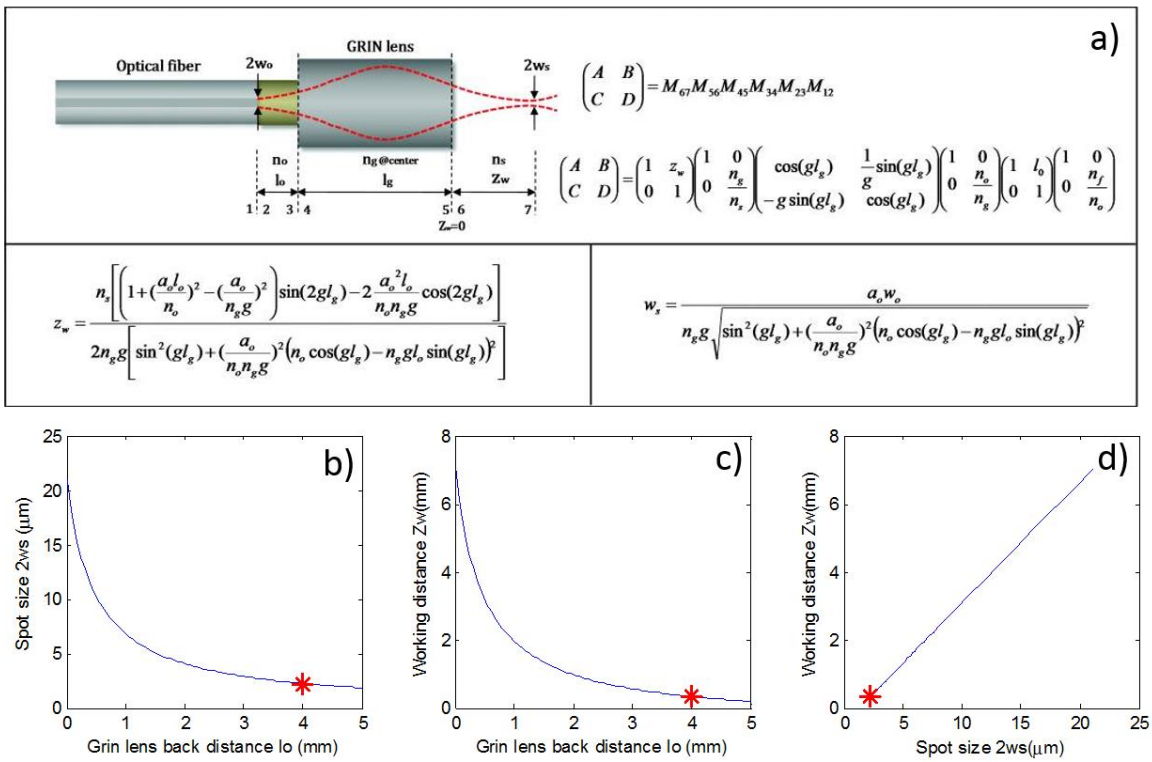


**Figure 48 Grin Lens Objective Calculations. a) Transfer matrix model used to calculate the laser spot size and working distance as function of the space between the grin lens and the optical fibre, adapted from** [79]. **b,c) Calculated values for the spot size and working distance applying the model to the selected components, d) working distance vs spot size trade plot. Red stars represent the values selected, in function of the chosen back distance of 4mm.**

## 4.3 Mechanical components

### 4.3.1 XY Piezo stage

In order to improve the resolution and repeatability of the laser scans in comparison to the experimental set-up used in the preliminary experiments, this experimental setup used the XY piezo stage of an existing Asylum MFP-3D Atomic Force Microscope (AFM). The accuracy of this instrument is excellent due to a closed loop positioning control system sensed by high precision Low Voltage Differential Transformers

(LVDT). Resolution was also greatly improved, because the AFM piezo stage performs continuous displacements in contrast to the prior setup with minimum discrete step size of 100nm. By having continuous displacements across the scan area, the maximum resolution of the scan then depended on the sampling frequency of the reflectance, which in turn depended on either the speed of the photo-detector or the Analogue to Digital Converter (ADC) of the AFM used to acquire the photo detector signal, whichever was the slowest. In addition, by using the AFM ADC to acquire the photo detector signal, the synchronization between the reflectance value and the XY position was resolved by the AFM software, providing high accuracy while aiming the laser on the device area. Additionally, the AFM thermal and acoustic isolation hood helped to reduce thermal drift.

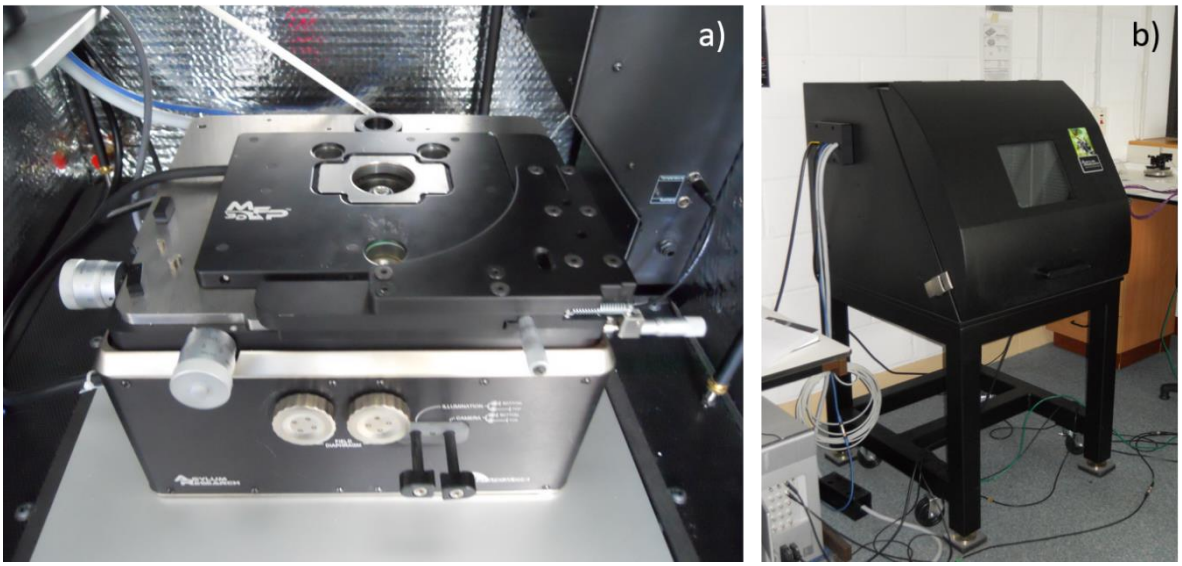


**Figure 49 AFM XY piezo stage, a)showing the three grove contact points. b) AFM hood to provide thermal and acoustic isolation**

### 4.3.2 AFM Laser scanning head accessory

The design of the Asylum MFP-3D AFM uses a scanning head that contains the cantilever and the Z piezo, and is mounted on top of the XY piezo stage by a three-groove kinematic clamp. For that reason, the laser scanning microscope was designed as an accessory that was mounted on the XY piezo stage instead of the original AFM scanning head. This allowed for ease of use, and quick setting up of the experiment, minimizing the time required to operate this highly demanding instrument.

The AFM laser scanning head accessory (Figure 50a) was composed of three different parts; the central base plate, the objective mount and the legs (Figure 50 b,c,e). The central base plate was machined from a 10mm thick block of titanium, a material chosen because of its low thermal expansion coefficient (~9μm / m·K). The base plate was held in place on top of the XY piezo stage by three legs, each build by coupling a custom-made steel rod with a semi-spherical termination to a rotational micrometre. The micrometres were used to adjust the height of the base plate and to provide correction for tilt. The central base plate provided support for the objective mount which was assembled by an angle bracket (Thorlabs DT12A) and a linear translation stage (Thorlabs DT12/M) used for the coarse focus adjustment of the GRIN lens objective. The linear stage held a custom-machined adapter plate which in turn held a kinematic mount (Thorlabs KM05T/M) used to correct the inclination of the objective, so the laser beam would have normal incidence over the sample. The complete objective mount moved up and down from the sample via an opening, machined in the centre of the base plate. Both the original AFM scanning head and the former experimental setup used for the preliminary experiments used a video camera aligned to the same optical axis as the laser beam. With these cameras, it was possible to search

the sample and aim the laser via the microscope objectives. However, in the current setup it was found to be impossible to add a camera in the same optical axis as the laser beam; therefore in order to provide visual aid to coarsely aim the laser, a USB microscope camera was mounted by the side of the objective.

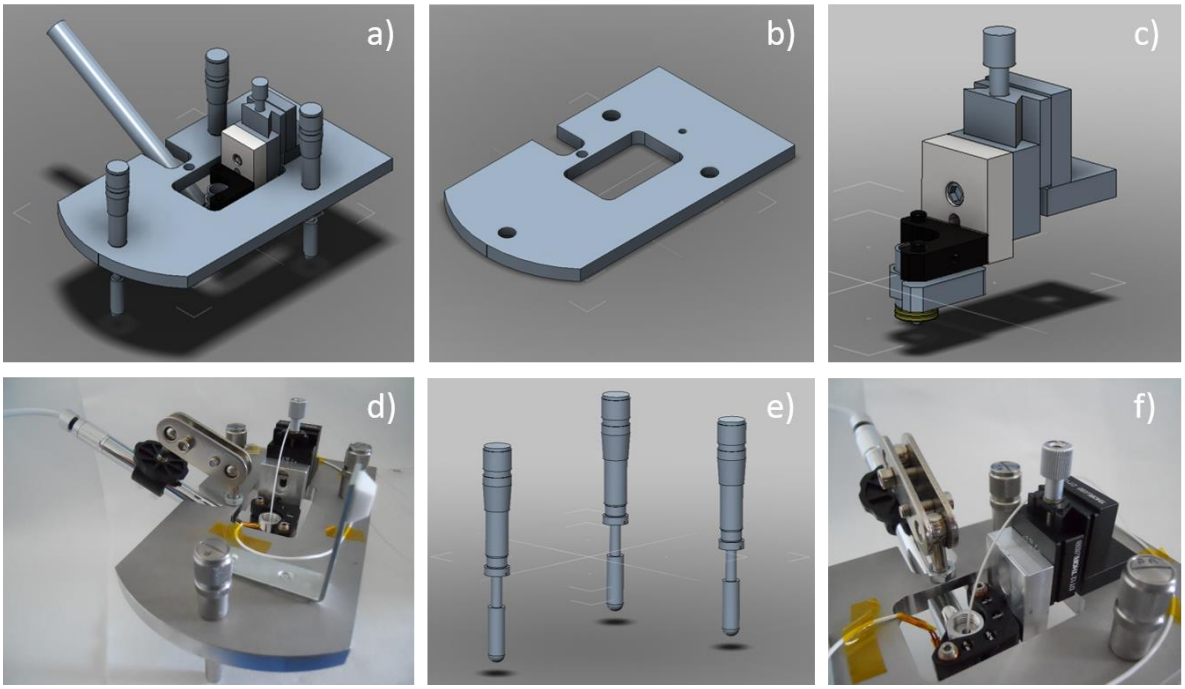


**Figure 50 Laser scanning microscope accesory. a) laser scanning head CAD design render, b) 3D render of the base plate, c) 3D render of the objective mount, d) Image of the laser scanning head assembled the USB camera is vissible on the left, e) 3D rendering of the micrometer legs, f) Detail image of the assembled objective mount.**

### 4.3.3 Z Axis Piezo

The fine adjustment of the focus of the laser beam on the sample was performed by a custom-made piezo stage, added to the objective mount. This extra piezo stage was required for two reasons. Firstly, the coarse adjustment performed with a linear stage in the objective mount was not sensitive enough to repeatedly provide displacements

smaller than 10µm Secondly, manual fine adjustments proved to be extremely unreliable since the forces applied to the mount while manipulating the stage were large enough to bend the mount and displace the laser beam off target.

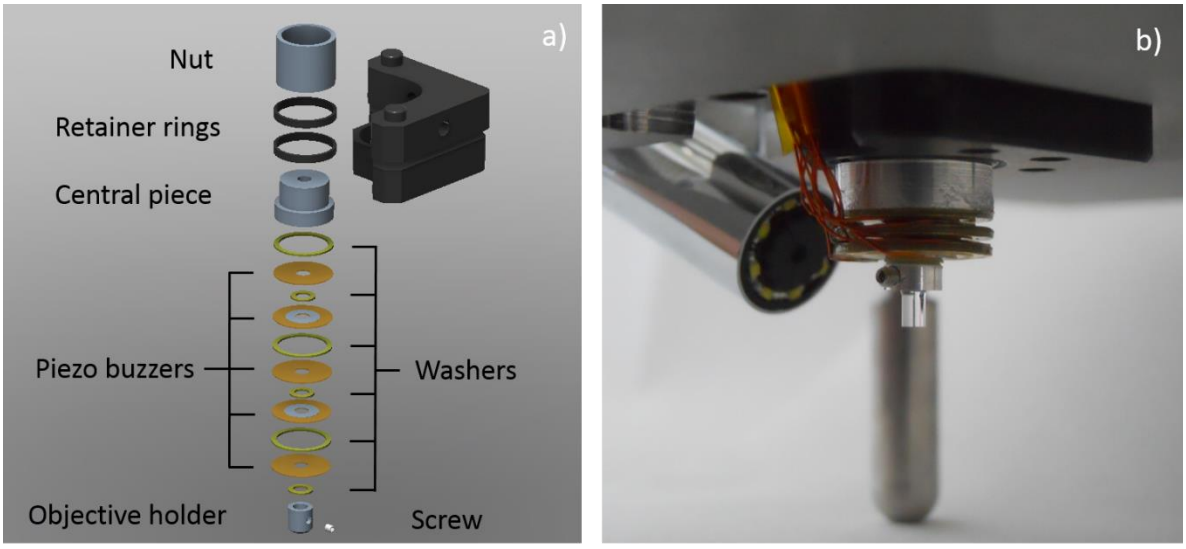


**Figure 51 Custom made Z Piezo. a) Assembly diagram of the Z piezo stage used for fine focussing. The combination of piezo buzzers and washers structure added up the displacement of each individual piezo b) Z piezo in the mount with objective installed.**

The custom construction of the Z piezo stage was based on low cost piezo buzzers. These are built as a bilayer disk; the larger disk acts as a diaphragm and it is made of brass and a smaller disk made of PZT as the piezoelectric material. When a voltage is applied to the piezo electric disk, it expands or contracts depending on the polarity. The strain produced by the piezo electric disk produces a deformation of the bilayer arrangement, effectively causing the disk to become concave. Wang *et al* demonstrated the possibility of fabricating low cost piezo electric actuators with piezo buzzers by building a 3-axis AFM stage [81]. In the present case, the requirement was a linear actuator with a minimum displacement range of 10µm. For that, an array of five piezo

buzzers was constructed by stacking them in a bellows-like configuration, so that the individual expansions or contractions added up to the displacement of the whole linear array. Figure 51a shows a CAD render of the individual elements of the assembly. A circular opening in the centre of each piezo buzzer allowed the fitting of the GRIN lens objective, which was held in place by a specially machined holder piece located at the edge of the assembly. The washers used to join the piezo buzzers were fabricated from a 0.4mm sheet of FR4 material. FR4 is a glass reinforced epoxy laminate that it is commonly used in the manufacturing of printed circuit boards (PCB) for the electronics industry. The different pieces were cemented together with epoxy resin and aligned with the aid of a machined assembly that kept all the parts in place during the curation of the resin. The piezo buzzers were electronically accessed by sticking coil wires to each terminal with silver paste and then adding a layer of cyanoacrylate to improve adhesion. Figure 51b shows the assembled Z piezo array mounted on the scanning head accessory with the GRIN lens objective installed.

## 4.4 Electronic components

Different electronic components of the experimental set-up served a variety of purposes; the first was the electrical characterization of the nano-devices, and the second, to electrically induce phase changes in the GST nano-devices. Thirdly, electronics were used to control and acquire data from the optical part of the system as well as to operate the mechanical components. Figure 52 shows a schematic diagram of the electronics part of the experimental set-up and their interconnections. Figure 53 shows images of the different electronic components of the experimental set-up built.

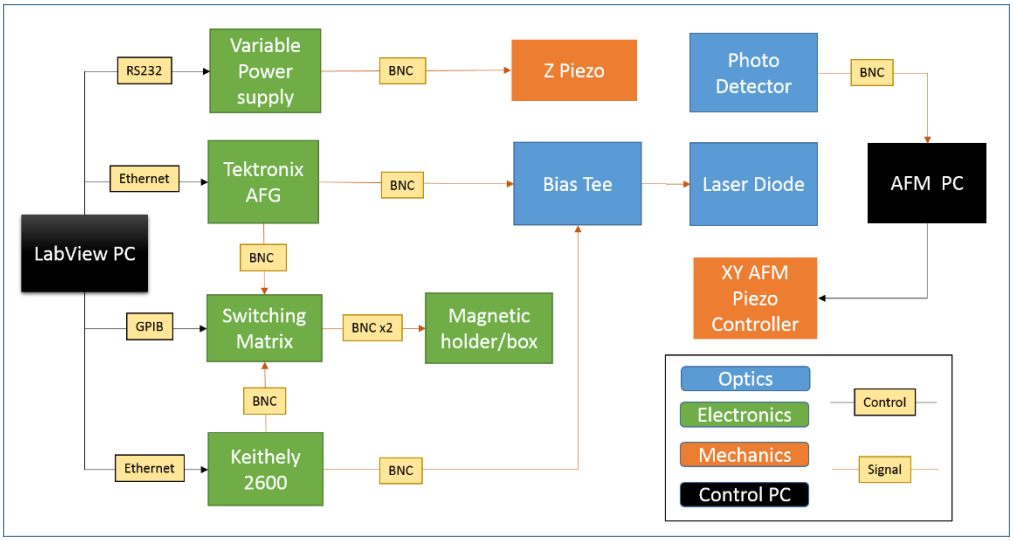


**Figure 52 Schematic diagram of the experimental set-up, showing the electronic components and connections.**

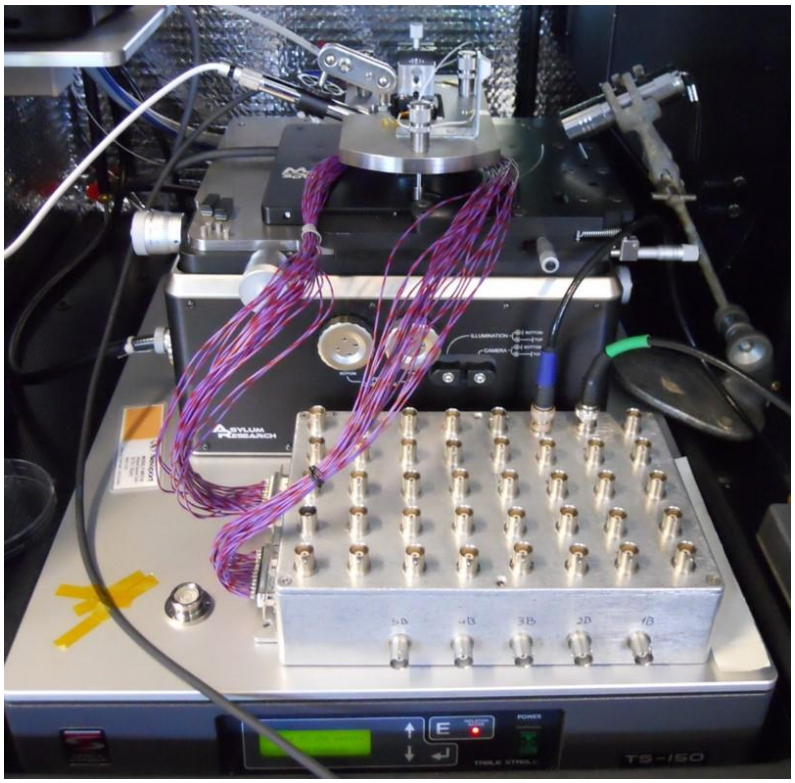

**Figure 53 Experimental set-up AFM assembly. The image shows the laser scanning head accessory mounted on the XY AFM piezo stage, the magnetic holder and the connections box used to access the devices electronically.**

### 4.4.1 Source Meter

The source meter used was a Keithley 2614B. This programmable instrument has two channels than can be used independently. In this case, Channel A was used as a precision current source to provide a DC bias current to the laser diode, via the low frequency port of a bias tee (see section 4.2.1). Channel B was used to perform electrical characterization of the GST nano-devices by performing I/V curves and resistance measurements.

### 4.4.2 Arbitrary Function Generator (AFG)

The function generator used was a 100MHz Tektronics 3021B with pulse mode. The shortest pulse possible to obtain was 20ns that included 5ns rising and falling edges minimum times. This instrument has two channels. Channel 1 was used to drive the optical pulses of the laser diode via the RF port of the bias tee (see section 4.2.1). Channel 2 was used to generate pulses to electrically phase change the GST of the nano-devices.

### 4.4.3 Switching Matrix

The electrical characterization process required iteratively measuring the resistance of the devices and then applying electrical pulses. These two actions were performed by different instruments, in order to combine the high sensitivity of the Source Meter for resistance measurements, and the high speed of the pulse generator to induce the phase change. Therefore, it was necessary to automate the constantly alternating connections between the devices and the instruments. The solution was to add a switching matrix to the setup. In this case, the model used was Keithley 7001 with two Keithly 7062 relay cards.

### 4.4.4 AFM magnetic holder

In order to accurately point the laser to a desired position on the sample, it was necessary to firmly hold the sample to the AFM XY piezo stage. In addition, the holding mechanism needed to allow electrical access to the devices. The solution to both requirements was the construction of a custom-build magnetic holder. The holder was designed to be thin (8mm high) in order to fit under the laser scanning accessory while accommodating a DIP48 chip carrier.

### 4.4.5 Variable voltage supply

A computer-programmable variable voltage supply was used to control the voltage applied to the Z piezo. The model used was a Precision BK9124, which provided a range of 0-60V, which was sufficient to produce a displacement of approximately 10μm.

### 4.4.6 Computer Control

The control of the different elements of the system was performed by two computers. The AFM computer controlled the XY AFM piezo stage via the Asylum Research AFM software. The output signal of the photo detector was digitized by one of the general purpose ADC's of the AFM controller. By doing this, the signal of the reflectance was synchronized with the position of the XY piezo in order to produce the scan image in real time. The rest of the electronics were controlled by a second computer running a specially designed LabVIEW® program that provided an orchestrated control of the instruments and produced log recording of every measurement taking of any given experiment.

## 4.5 Characterization

Once the experimental set-up was build, testing was required. In the next section, there is a description of some characterization measurements performed to assess the operation of the instrument.

### 4.5.1 Laser spot size

In order to verify the operation of the laser scanning microscope, in particular the GRIN lens objective, some test scans were performed. Figure 54 shows the Point Spread Function of the laser probe obtained by scanning a sub-spot size feature. Measured laser beam size was 2.2µm in accordance with the design parameters.

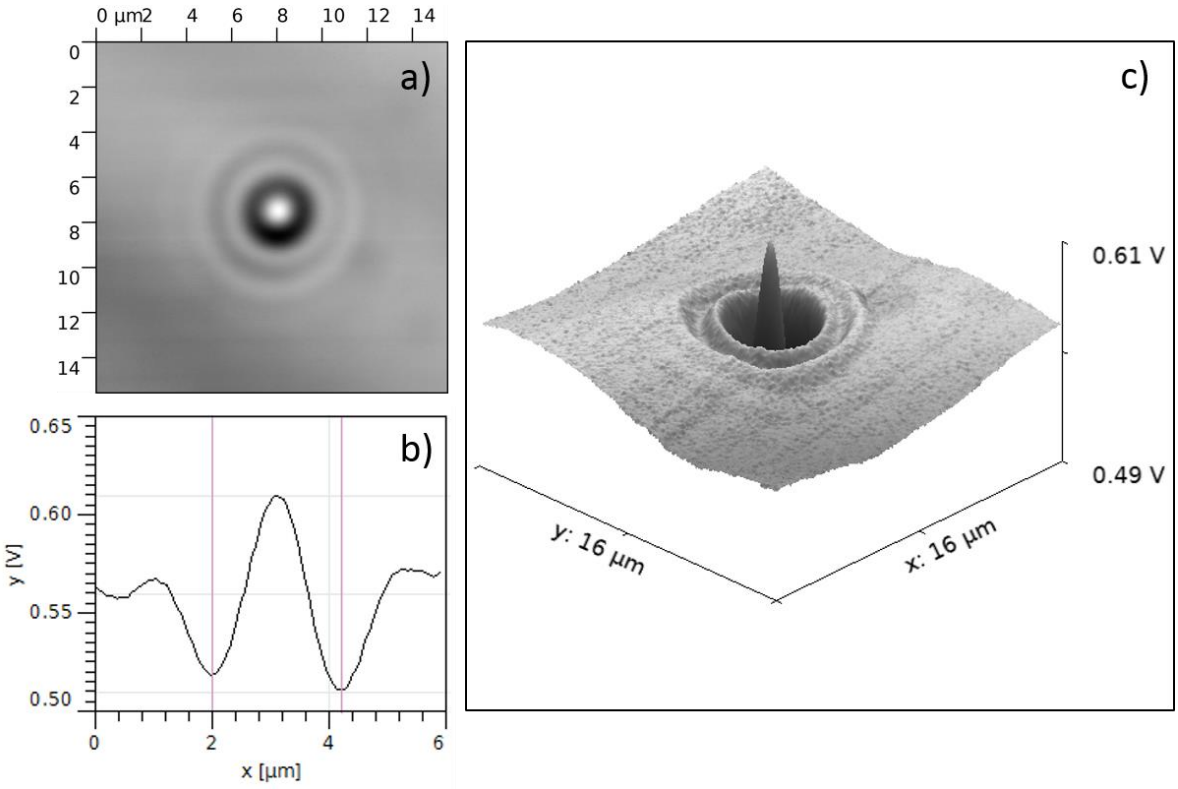


**Figure 54 Point Spread Function. a) Reflected scan image of the PSF, b) cross section that shows gausian profile of the spot, distance between lines is 2.2µm, c) 3D render that shows the airy disk pattern of the PSF.**

### 4.5.2 Laser power characterization

Laser power measurements were necessary to establish the limits of the system and the inserted power losses. To do that, a variety of measurements were performed using a free space Optical Power Meter. The first measurement involved the characterization of the laser module (combination of the laser diode and the collimation aspheric lens) while varying the DC current of the laser diode. Figure 55a shows the laser module response. It is possible to observe the characteristic linear lasing region starting at about 55mA. Therefore, 60mA was chosen as the lowest stable operation bias value within the lasing region.

Knowing the optical power per current bias response (Figure 55a), it was the possible to characterize the whole assembly insertion loss. This was done by measuring the optical power output at the objective, and comparing it with the power of the laser module (Figure 55b). The complement of the slope of the linear trend indicates that the set-up insertion loss is 76.66%. The main sources of loss are the laser to fibre coupling (50% insertion loss), 10% power drop at the beam splitter, in addition to standard APC fibre connections losses. The next graph (Figure 55c) shows the I/V curve of the laser diode. This measurement was required to calculate the diode resistance in the linear region. With this information together with the Optical power vs Current bias (Figure 55a) and knowing the insertion loss of the system, it was possible to calculate the amount of optical output power per volt of the electrical pulses used to drive the laser diode biased at a constant current of 60mA. The result of these calculations is shown in Figure 55d.

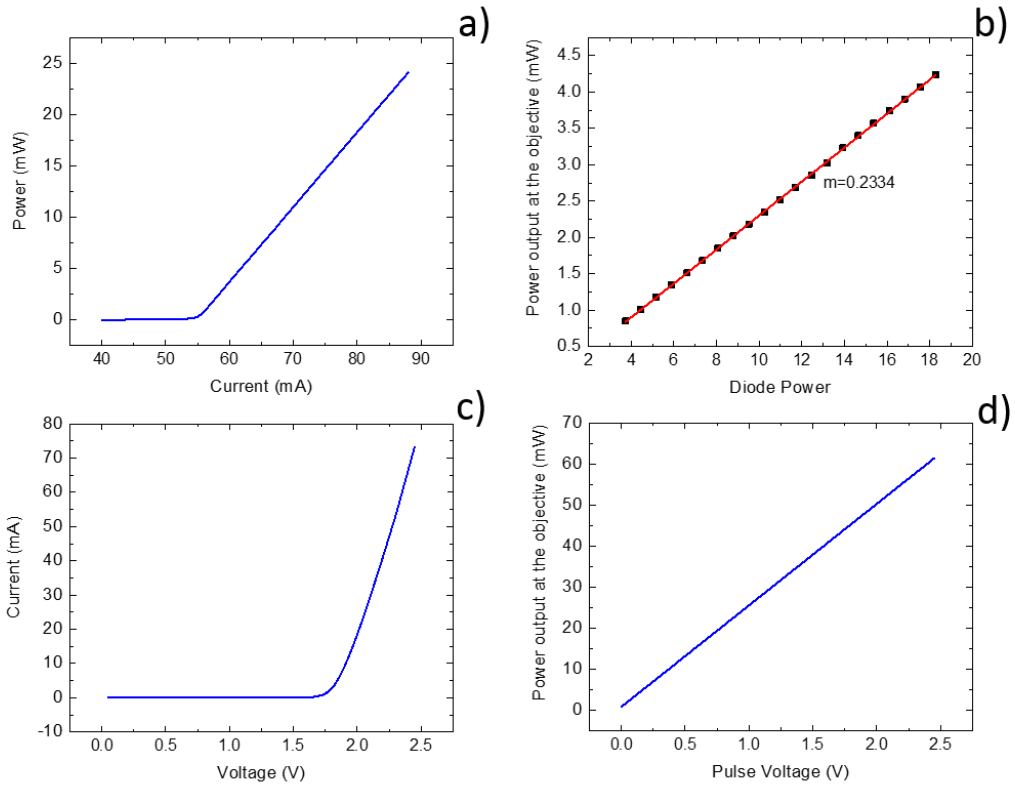


**Figure 55 Laser setup power output characterization. a) Optical power vs. DC bias applied to the laser diode, b) Calculation of system efficiency 23.34% by linearly fitting the power output at the laser objective, against the laser diode power output, c) I/V curve of the laser diode, d) Calculated optical power output from the objective, for given pulse voltages (assuming 60mA DC bias) considering setup insertion loss, this graph was using during the experiments to modulate the output laser power by controlling the voltage of the electrical pulse applied to the laser diode.**

### 4.5.3 Optical limitations

During the long run operation of the setup, it was found that ambient temperature variations induced variations of the optical output power due to a well-known drop in efficiency with the increase of temperature of laser diodes. In order to mitigate this, a large heat sink was attached to the laser diode module. Also to enhance stability,

measurements were performed at night, and a warm up cycle was performed prior to every experiment by turning on the laser for 30min at 60mA DC bias before the measurements.

The system presents a very high insertion loss (76.6%), most of it caused by the laser to fibre coupling (50%). This is assumed to be caused by the bad quality laser beam obtained from low cost diodes, in combination with the typically high (50%) insertion loss while coupling to single mode optical fibres. Another important limitation was the lack of optical isolation in the reflection path. Back reflections could accelerate diode ageing, and might under certain circumstances cause output power instability. Despite these drawbacks, the current experimental set-up represents a significant improvement in terms of power, accuracy, position, repeatability sensitivity and foot-print compared to than the previous setup used for the preliminary experiments.

### 4.5.4 Low current measurements considerations

Due to the typically high resistance value of the devices (GΩ) and to the low voltages used for I/V curves and resistance measurements (<1V), current signals were very small (nA) and subject to noise. In addition, the 7062 switching matrix boards were not specifically designed for low current measurements and were not ground isolated. So small perturbations from the power line were induced in the measurements. In order to compensate for this, the integration time for each point of the I/V trace or resistance measurement was set to 1 Power Line Cycle (PLC) or 20ms.

## 4.6 Conclusion

This chapter has described the construction of a new experimental set-up consisting in a laser scanning microscope accessory that has a small foot-print, is compatible with the existing AFM XY piezo stage, has a low cost and is capable of performing the *mixed mode* experiments. Once this set-up was built and characterized, the next chapter describes how the complementary nano-devices were designed and fabricated.

# 5 NANO-FABRICATION

## 5.1 Introduction

As it was explained in Chapter 3, the preliminary experiments showed that the planar devices of the original specification were unsuitable to be operated electrically unless the device length were less than 50nm. However, this would make the phase change optically undetectable. Thus, it was evident that a different type of device was necessary. The architecture chosen was a cross-bar vertical device with transparent electrodes made of Indium Tin Oxide (ITO). ITO is commonly used in the consumer electronic industry for the elaboration of LCDs and touch pads. By confining a thin film of GST between transparent electrodes, it was possible to maximize the optical access area while keeping the length of the GST region to a minimum, thus reducing the voltage threshold required to operate the devices electrically. The concept and fabrication process used follows the one presented previously by Hosseini *et al* [41]. A conceptual idea of the vertical devices fabricated is shown in Figure 56.

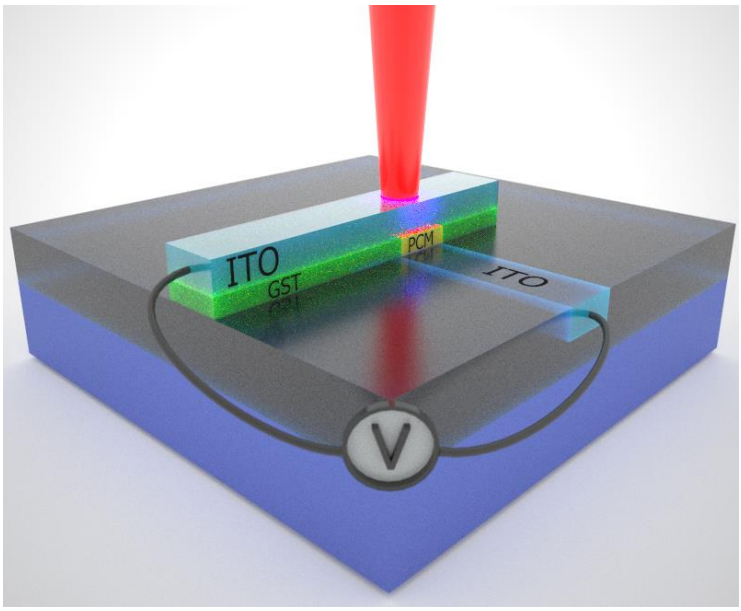


**Figure 56 Conceptual schematic of the cross-bar vertical devices, fabricated by containing a thin film of GST between two ITO transparent electrodes.**

## 5.2 Optical properties optimization

The specification of the devices requires a large window to allow for observation of the phase change, but at the same time, a GST thickness of max 50nm is needed to allow the devices to be operable electrically. In addition, it is desirable to maximize the optical contrast between amorphous and crystalline phases in order to observe partial crystallization states. Traditional GST-based optical data storage achieves a 20% contrast in reflectance with layers of 50nm. However, in this case, it proved possible to achieve a similar optical contrast with a significantly thinner layer of GST by tuning the response of the optical cavity created when GST is contained between ITO electrodes, as described by Hosseini *et al* [41]. The tuning was achieved by varying the different thicknesses of the top, bottom and GST layers. Optimization was performed by doing simulations using a transfer matrix method as described in the next section.

## 5.2.1 Matrix transfer method for reflectance calculation

The optical properties of the stack were modelled with a transfer matrix model, developed by Macleod [82]. This model allowed the calculation of the reflectance of the optical nano-cavity based on the refractive index, thickness and order of the layers that comprise the stack. The way the model works is by considering the continuity conditions of the incident tangential electric (*E*) and magnetic (*H*) fields as they propagate through the layers of the stack. The intensity and phase of the fields get transformed as a function of the thickness and complex refractive index of every layer. The combination of all transformations is represented as a transfer matrix of the form:

$$\begin{bmatrix} E_{air}/E_{substrate} \\ H_{air}/H_{substrate} \end{bmatrix} = \begin{bmatrix} B \\ C \end{bmatrix} = \left\{ \prod_{r=1}^{q} \begin{bmatrix} \cos\delta_r & (i\,sin\delta_r)/\eta_r \\ i\,\eta_r sin\delta_r & cos\delta_r \end{bmatrix} \right\} \begin{bmatrix} 1 \\ \eta_m \end{bmatrix} \quad (1)$$

- $E_{air}$ , $H_{air}$ :Amplitudes of the incident Electric and Magnetic fields at the top interface
- $E_{substrate}$ , $H_{substrate}$ : Amplitudes of the transmitted Electric and Magnetic fields through the bottom interface towards the substrate
- r=1 : Initial media (air)
- q : Number of layers of the stack
- $\delta r = 2\pi N d \cos\vartheta/\lambda$ : Changes of phase introduced by a layer of thickness d
- $\eta_r$ : Optical admittance of each layer
- $\eta_m$ : Substrate admittance

The total reflectance of the stack is then given by the expression [82] :

$$R = \left(\frac{\eta_0 B - C}{\eta_0 B + C}\right)\left(\frac{\eta_0 B - C}{\eta_0 B + C}\right)^* \quad (2)$$

Where $\eta_0$ is the admittance of the incidence medium (air).

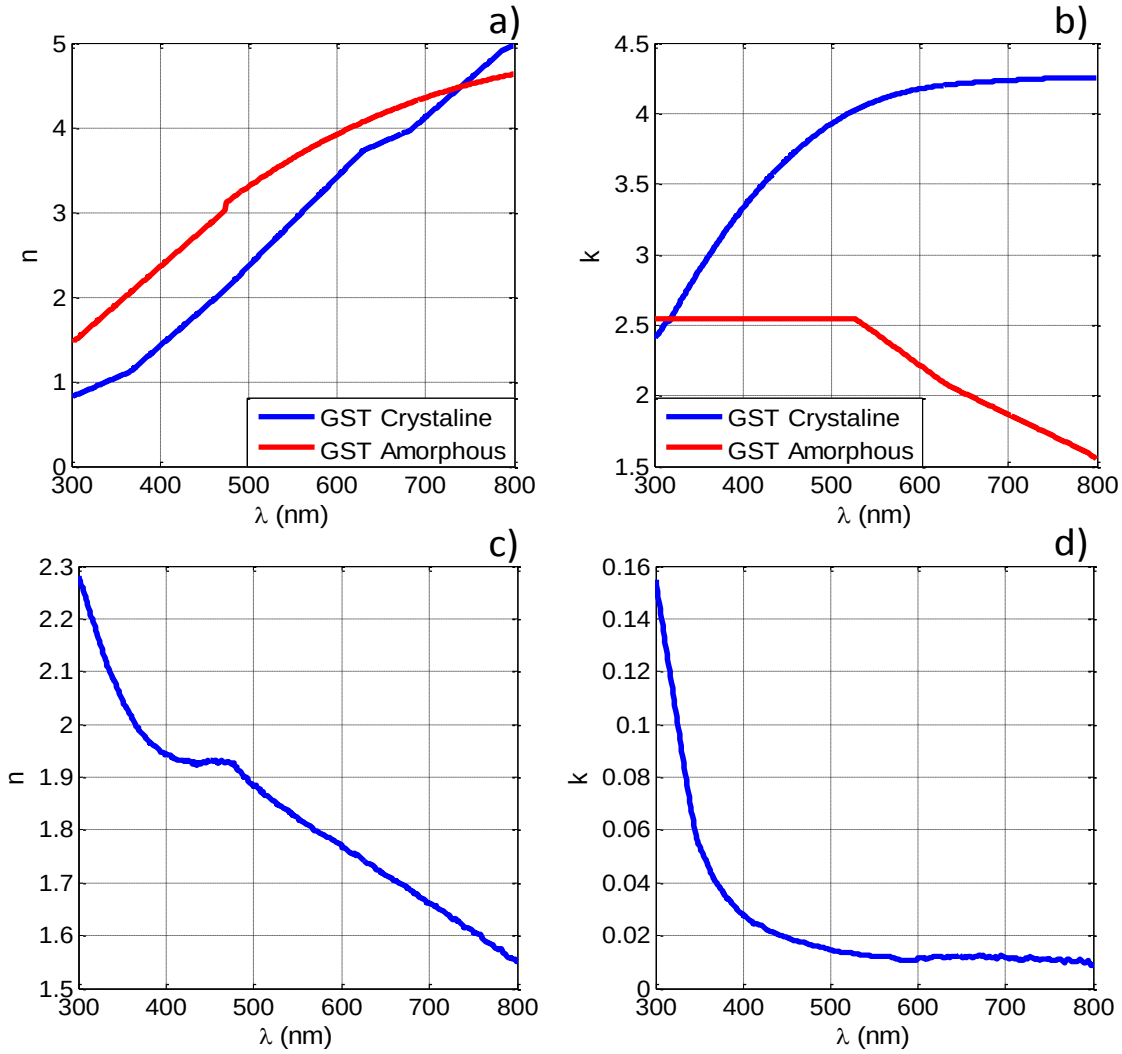


**Figure 57 Complex refractive indexes used in the model. a) GST n values, b) GST k values, c) ITO n values, d) ITO k values.**

This model has also been used by Rios *et al* [60] to model colour change in AgInSbTe (AIST) films. By feeding the data of the refractive indexes of GST and ITO (Figure 57) into the model, it was possible to test the optical contrast between amorphous and crystalline of several different combinations of layer thicknesses. Ultimately the combination chosen was 20nm of ITO top electrode, 15nm of GST and 20nm of ITO bottom electrode, deposited on top of a $Si/SiO_2$ substrate. Estimated optical response can be seen in Figure 58. It is important to point out that an increment of 20% in

reflectance from the amorphous to the crystalline states was obtained with only 15nm of GST. Different sizes of devices were fabricated, but in order to reach a balance between the device fitting into the laser spot to be exposed as homogenously as possible, and on the other hand being large enough to be measured by the laser scanning microscope, two sizes were the main focus of the experiments, 500nmx500nm and 1µmx1µm.

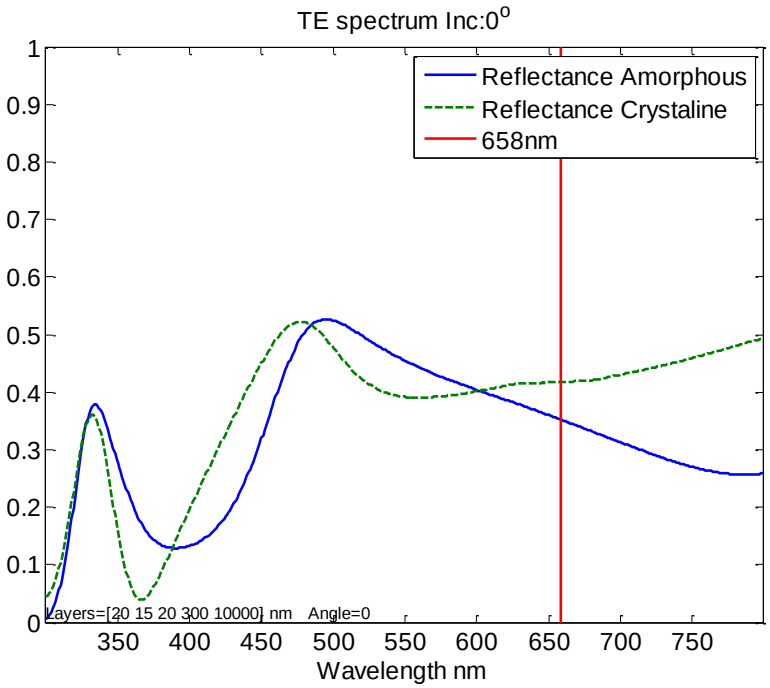


**Figure 58 Theoretical optical response of the chosen stack in the visible range. The red line indicates the response at the wavelength of the laser scanning microscope.**

## 5.3 Nano fabrication process

In order to fabricate the cross-bar nano-devices, four lithographic steps were necessary. The first step was the creation of reference markers. Those markers were then used for alignment of the successive lithographic steps. Then, the next step was the fabrication of the bottom ITO electrode, followed by the top electrode that contained the GST thin

film. Finally, gold access electrodes were added. A detailed description of each of the processes is provided below.

### 5.3.1 Reference markers

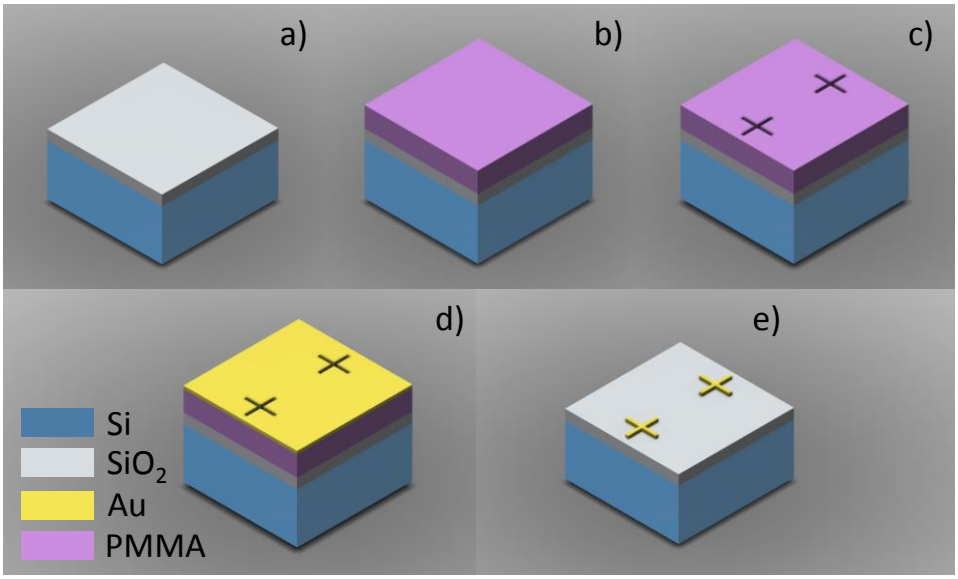


**Figure 59 Reference markers process.**

The markers process, as the first lithographic step, started with a clear substrate. The substrate used was a 10mmx10mm diced piece from a thermally oxidized Si/$SiO_2$ wafer (320nm $SiO_2$) (Figure 59a). Before the lithographic process, the sample was cleaned by a sequence of ultrasonically agitated hot baths of acetone, MFCD26 stripper, acetone, and isopropanol (IPA), to finally be dried by $N_2$ flow. Then a bi-layer Polymethyl methacrylate (PMMA) electron beam resist was spin-coated (Figure 59b). PMMA495 + PMMA950 were used for the bilayer. These two electron-beam resists have different molecular weights, which causes different sensitivity to the electron radiation. The effect of spin-coating the more sensitive, low molecular weight in the bottom (PMMA495) is that the exposed pattern will be slightly concave within the resist layer, avoiding adhesion of any deposited material in the walls of the PMMA mask. This

helps to create clean edges around the patterned features, and increases the production yield by improving the quality and ease of the lift-off process. After spinning each layer, they were reflowed in a hot plate at $160^0$C for 5 minutes.

After the PMMA mask was deposited, the sample was exposed to an electron beam writing process that created the marker's design. The expose dose used was 650μC/cm$^2$ using a 10nA electron beam. After exposure, the sample was developed by submerging it in a mix of 15:5:1 parts of IPA, MEK, and MIBK respectively, for 30 seconds, after which it was sequentially rinsed in IPA, $H_2O$ and dried by $N_2$ blow. The development process removed the PMMA resist exposed to the e-beam lithographic process, effectively creating a mask with the markers pattern (Figure 59c). Then a combination of 30nm Cr and 50nm Au was deposited by thermal evaporation from a Cr rod and Au wire on a tungsten crucible, respectively. The deposition rate was set at 0.1nm/sec, measured by a piezo-electric deposition monitor, at a base pressure of $1x10^{-6}$ mbar (Figure 59d). Finally the PMMA mask was removed by a lift-off process by submerging the sample in acetone at $50^0$C for 12 hours, followed by 1 minute sonication in acetone at 10% power and 1 minute sonication in IPA at 10% power. A final IPA rinse and $N_2$ blow completed the marker's lithographic step (Figure 59e).

### 5.3.2 Bottom electrode

The second lithographic step created the bottom electrode of the cross-bar devices. The process started by spin coating a bi-layer PMMA (PMMA495+PMMA950) each layer was reflowed in a hotplate for 5min at $160^0$C (Figure 60a). Then the bottom electrode pattern was created by e-beam lithography, with an expose dose of 600μC/cm$^2$, and an electron beam current of 1nA. Then the mask was developed (Figure 60b) with a 15:5:1

mix of IPA, MEK, and MIBK respectively, followed by a rise in IPA, $H_2O$ and dried by $N_2$ blow, equal to the development process used in the markers step.

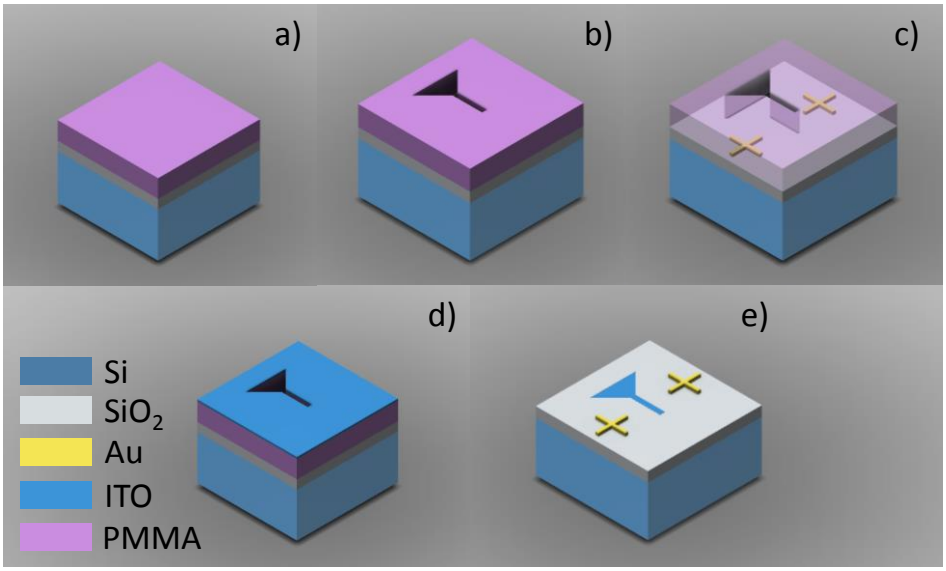


**Figure 60 Bottom electrode process.**

Next followed the planarization mechanism. In order to avoid a short circuit between the electrodes, the bottom electrode was planarized by creating a trench in the $SiO_2$ substrate of a depth equal to the thickness of the deposited ITO that formed the electrode. The trenches were created by etching 20nm of $SiO_2$ by Reactive Ion Etching (RIE). The recipe started with a base pressure of $5x10^{-6}$mTor, a gas mix of 25sccm $CHF_3$ + 25sccm Ar, reached an operating pressure 30 mTor, then applied 200W of RF power for 1 minute.

After the trenches were competed (Figure 60c) the ITO that would fill them to form the bottom electrode was sputtered using the same PMMA mask (Figure 60d). The ITO RF-Sputtering process required significant amount of characterization. During several repetitions of the process, it was found that there was a significant variability in the quality of the deposited thin film in terms of appearance and electrical resistance. Low quality films presented very high sheet resistance (MΩ range) and brown coloration.

These characteristics corresponded to oxygen deprived ITO [83]. A correlation was also found between the quality of the films and the base pressure used during the sputtering process; lower base pressures (~$1x10^{-7}$mbar) yielded better quality films, which suggests that oxygen provided by the stoichiometrically balanced ITO target was reacting with contaminants in the sputtering chamber. A common solution to this problem is to perform RF sputtering in an oxygen-rich gas mixture. However this solution was forbidden due to safety reasons, associated to limitations of the sputtering system available for the present nano-fabrication process. The sputtering system achieves a high vacuum by means of a cryogenic pump, which accumulates the absorbed gases in an internal container until a pump regeneration process is performed. Therefore the accumulation of oxygen creates a risk of explosion.

Working around this limitation consisted of adopting a two-part methodology. Firstly, the system was allowed to pump for 24 hours before sputtering ITO, thus reducing the base pressure value. Secondly, after sputtering and lift-off, the sample was annealed at 300°C in air for 30min. This process has been reported to improve the conductivity of the ITO by increasing the crystallinity of the thin film[84].

The ITO was sputtered from a 2in target (Testbourne, UK) under the following conditions: base pressure of $1x10^{-7}$mbar, operating pressure of $7x10^{-3}$ mbar, 100 sscm Ar, RF Power 30 W, for 9 min 30 secs. The lift-off process was the same as in previous steps. Annealing, was performed after lift-off to complete the fabrication of the bottom electrode (Figure 60e).

## 5.3.3 Top electrode

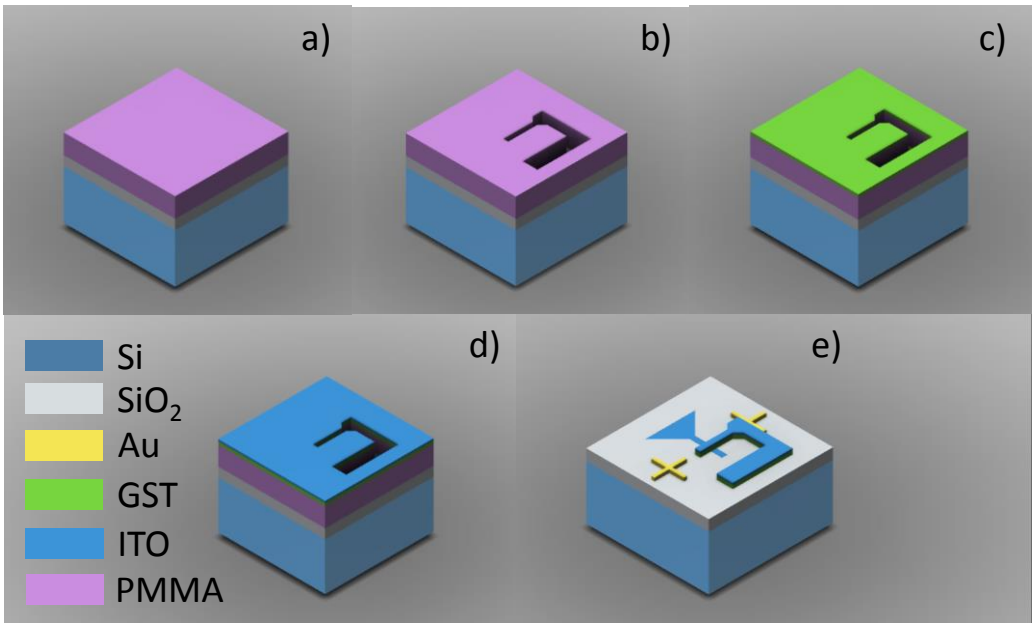


**Figure 61 Top electrode process.**

The third lithographic step was used to build the top electrode of the cross-bar nano-devices. As in previous steps, a bi-layer PMMA495+PMMA950 was spin coated and reflowed at 160°C for 5 minutes (Figure 61a). Then, the pattern of the top electrode was created by electron-beam lithography, with an expose dose of 650μC/cm$^2$ and beam current of 1nA. The development process used was the same as in previous lithographic steps. After development the PMMA mask was completed (Figure 61b). The top electrode was composed of two layers, GST and ITO. The materials were deposited one after the other without breaking the vacuum in order to avoid exposure to air and potential oxidation of the GST layer. 15nm of GST were sputtered from a 2 inch target (Super Conductor Materials, USA) (Figure 61c) with a base pressure of 1x10$^{-7}$ mbar, chamber pressure of 7x10$^{-3}$ mbar, 100 sccm Ar, 30W for 4 min 10 secs. Then 20nm ITO were sputtered immediately after (Figure 61d), using the same recipe as for the bottom electrode: operating pressure was 7x10$^{-3}$ mbar, 100 sscm Ar, RF Power 30 W,

for 9 min 30 secs. It is important to mention that in order to avoid crystallization of the GST, the ITO top electrode was not thermally annealed as the bottom one was. Another important observation is that it was found that the adhesion of the GST layer to the ITO/$SiO_2$ substrate was poor, therefore the lift-off process was performed with extreme care to avoid the top electrodes detaching from the substrate. For the lift-off process, the sample was submerged in acetone at room temperature for 72 hours, then it was exposed to 10% power ultrasonic bath cleaning for 1 minute in acetone, rinsed in fresh acetone, sonicated at 10% power in IPA for 1minute, rinsed in fresh IPA and dried by $N_2$ blow. After lift-off, the cross-bar devices were fabricated (Figure 61e).

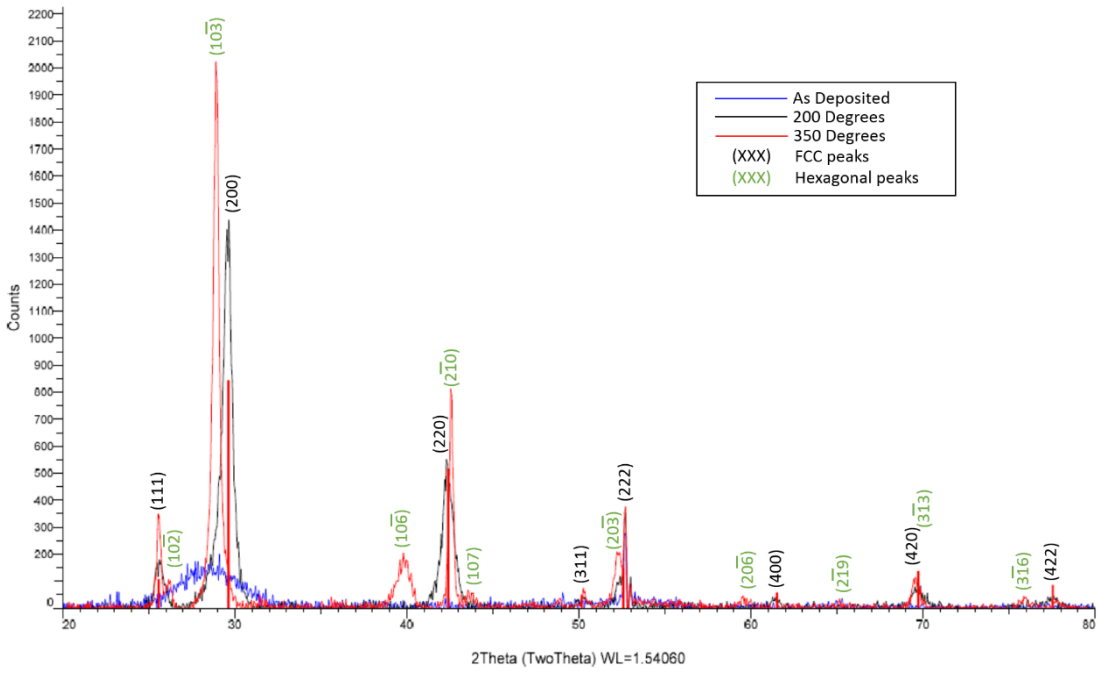


**Figure 62 XRD pattern of sputtered GST layer as deposited (blue) and after crystallization by thermal annealing.**

In order to verify the crystallinity of the GST films after the sputtering process, a control sample with GST deposited on it was analysed by XRD. Results from the measurements are shown in Figure 62. It is possible to observe the as-deposited-

amorphous state at room temperature and the phase transitions, first to fcc and then to a mixed fcc and hexagonal state as the sample was thermally annealed inside the diffractometer.

### 5.3.4 Contact electrodes

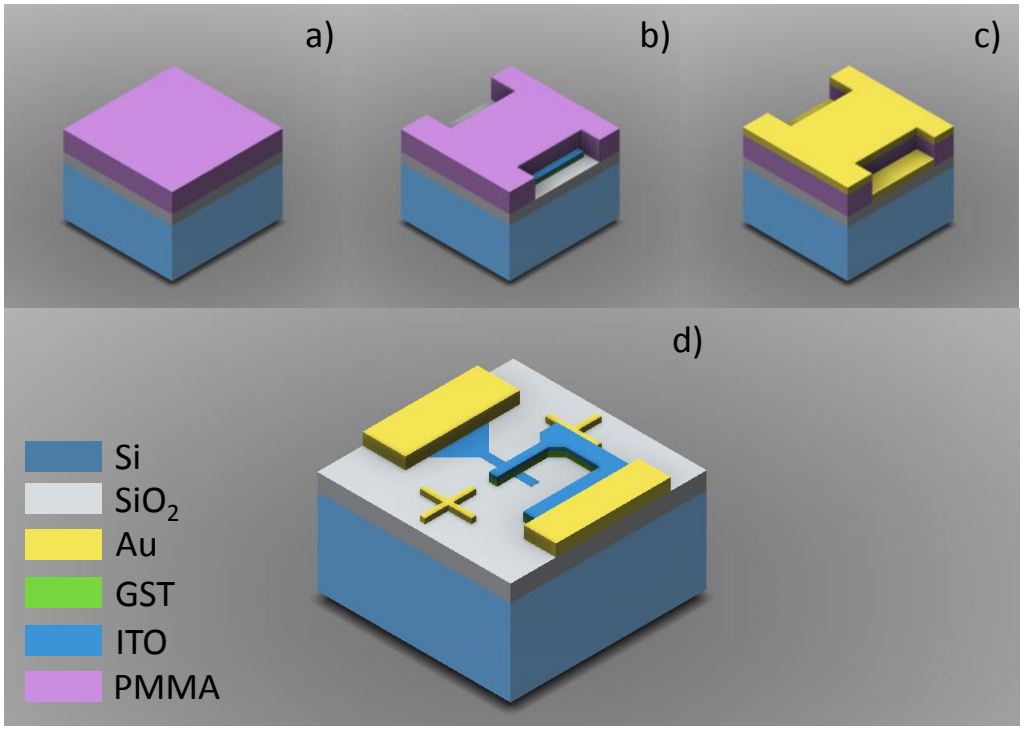


**Figure 63 Access electrodes process.**

The last lithographic step was used to create large (105µm x 105µm) gold electrodes so the device was accessible via wire bonding. The purpose of creating a different lithographic step for the access electrodes, additionally to the top and bottom steps mentioned before, was to reduce e-beam writing time. The e-beam system used did not have the option to dynamically set the writing-beam current. As a consequence, if the large access electrodes and small device features were to be written in the same job, a small writing current would be needed to achieve the resolution required for the

devices, causing the large access electrodes to be written by a small beam current, dramatically increasing the writing time and cost of the entire process.

The process started by applying a bi-layer PMMA495+PMMA950. In order to avoid crystallization of the devices, the PMMA resists layers were not reflowed, but only heated to 95°C for 15min in a hot plate – this was with the intention of letting the solvent evaporate to leave a solid PMMA coating layer (Figure 63a). The side effect of this was an increase in sensitivity of the resist to e-beam radiation. Therefore the e-beam patterning process was performed with an expose dose of 500μC/cm$^2$ and a beam current of 10nA. For the development process, the same solvent development mix as in previous steps was used. However, in this case the development time had to be adjusted to 45 seconds, followed by rinse in IPA and $H_2O$ and finally being dried with an $N_2$ blow to complete the pattern in the PMMA mask (Figure 63b).

Next, 30nm Cr used as adhesive layer followed by 60nm Au were thermally evaporated to form the access electrodes (Figure 63c). Evaporation base pressure was 2x10$^{-6}$ mbar and deposition rate 0.1nm/sec. It is important to mention that the large thickness of the Cr layer, in comparison with standard adhesive layers that usually require only a few nm, was designed to improve electric contact between Cr/Au electrodes and ITO. When a very thin layer of Cr is used, Cr attempts to oxidize in contact with the ITO, causing the remaining metallic Cr to diffuse into the Au, leaving a CrOx layer that is not electrically conductive[85]. This causes a highly resistive contact or a faulty memresistive behaviour.

Lift-off of this process was also gentle to avoid destroying the devices. The sample was submerged in acetone at room temperature for 72 hours, followed by sonication at 10%

power for 1 min in acetone, then rinsed in fresh acetone, IPA, $H_2O$ and dried by $N_2$ blow. At the end of this step, the nano-devices were completed (Figure 63d).

### 5.3.5 Sample dicing

Ten different batches of 24 devices each were fabricated per sample. Therefore in order maximize the availability of the devices, the sample was cut with a diamond dicer in ten different parts. Before dicing, the sample was protected by a dual layer of spin-coated PMMA495, and dried in a hot plate after each layer at 75°C for 20min. After dicing, every batch was cleaned individually by a 3 minute sonication in $H_2O$ 50% power, then rinsed in $H_2O$ to remove Silicon particles produced by the diamond saw.

Next, in order to remove the resist, the piece was rinsed in acetone, and then sonicated in an acetone bath at 10% power for 1 min, followed by another fresh acetone rinse, then rinsed in IPA, and dried by $N_2$ blow. After this process, the samples were kept in a vacuum container to avoid any potential oxidation of the GST by the edges of the nano-devices.

### 5.3.6 Chip carrier mount and wire bonding

Finally every individual diced batch of 24 devices was fixed to a Spectrum Semiconductor CSB04838 DIP48 chip carrier using silver paste. Then each device was wire bonded to be accessed individually. Figure 64 shows the completed devices chip assembled.

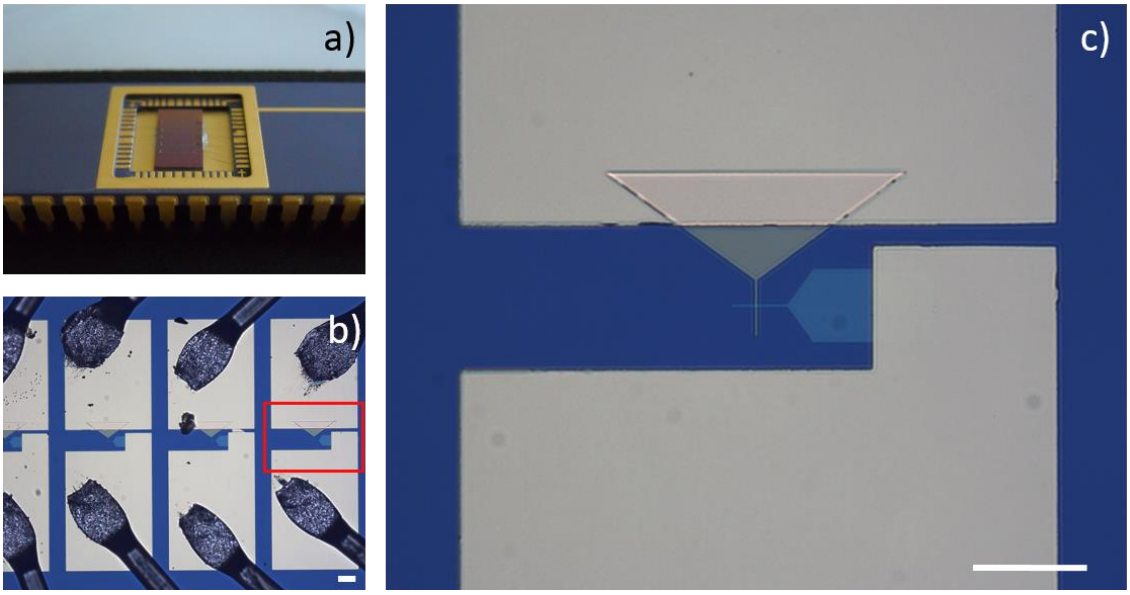


**Figure 64 Completed, nano-devices chip mounted in chip carrier and wire bonded**

**a) Diced row with 24 devices fixed to chip carrier, b) detail of wire bonding to Au contact electrodes. c) Detail of the red squared area, showing a 1µm device. Scale bars are 20µm.**

### 5.3.7 Conclusion

In this chapter, the processes followed to fabricate of the cross-bar nano-devices used for the *mixed mode* experiments have been presented. The cross bar vertical architecture with transparent ITO electrodes was selected because it maximizes the device area, allowing optical access to the GST layer in the device, while at the same time reducing the threshold voltage required to electrically switch the GST. It has also been explained how different challenges during the fabrication process were solved, including conductivity and contact issues with the ITO transparent electrodes. Additionally, it has been explained how the chip was fixed to a chip carrier to fit into the experimental setup described in Chapter 4. The next chapter will describe how the *mixed mode* experiments were performed and provides an analysis of the results obtained.

# 6 MIXED MODE EXPERIMENTS

## 6.1 Introduction

Previous chapters have explained the construction of an experimental set-up with the capability to perform the planned experiments, in addition to the fabrication process used to produce vertical nano-devices. With this new combination of setup and devices, it was possible to perform the *mixed mode* experiments. This chapter presents the results obtained by measuring the evolution of the reflectance and resistance of the devices while subjected to different optical and electrical stimuli to induce the phase change.

Section 6.2 describes the methodology adopted, whilst Sections 6.3 and 6.4 present the results of initial testing by electrical and optical measurements respectively. Sections 6.5 and 6.6 present the results of the *mixed mode* experiments, firstly with electrical excitation and secondly with optical excitation. The chapter culminated (6.7) by experimentally demonstrating a proof of principle of a GST based opto-electronic memory.

## 6.2 Methods

### 6.2.1 Laser focusing

In order to perform the optical part of the *mixed mode* experiments, it was required to accurately point the laser at the devices, as well as to focus the laser spot on the device. The process to locate the devices was as follow. First with the laser turned on, at low power (60mA DC bias) and the sample loaded in the magnetic holder, the height of the objective was adjusted until the objective was at approximately the working distance (~300μm) from the sample, and until the laser spot was visible on the optical microscope camera. Secondly, the XY micrometres of the AFM piezo stage were used to move the sample until the laser was located under the device area. This step was necessary to coarsely align the device of interest with the laser beam, due to the short displacement range of the AFM piezo stage (100μm). Thirdly, the coarse focus of the laser was adjusted by maximizing the intensity of the reflected signal. Fourthly, the laser-scanning microscope was set to a continuous scan mode, and by observing the image acquired by the laser microscope, the position of the scan area of interest was re-adjusted by using the XY micrometres. Once the scanning are of interest was roughly located, then the final fine positioning was performed by adjusting the offset scan values within the 100μm range of the XY Piezo. Finally the fine laser focus was performed with a special case of a knife-edge technique. This was achieved by performing a series of line scans perpendicular to the top electrode, while simultaneously, the voltage that controlled the position of the Z-piezo was adjusted.

Due to the contrast difference between the background substrate and the top electrode, a step in intensity was observed. The correct focus was achieved when the position of the Z-piezo minimized the slope of the step. This was an iterative process because the Z-piezo had no position sensor or feedback mechanism, in addition to non-characterized hysteresis.

### 6.2.2 Reflectance measurements

The reflectance of the device during the *mixed mode* experiments was extracted by post-processing a series of images captured by the laser-scanning microscope. The images files were generated by the Asylum AFM software, and contained the intensity of the reflected signal, as measured by the photo detector. Figure 65 contains a flow chart with the algorithm for reflectivity data post processing. In order to extract the reflectance value at the device, two factors were required to be corrected in order to compensate for variations of the system; first of all, the drift of the XY piezo stage, which may be up to 2μm during the duration of the experiment, and secondly, variations in the intensity of the laser caused by temperature fluctuations of the laser diode.

The drift of the images was compensated by the algorithm by centering the images before data extraction. In order to find the centre, four line scans at different pre-defined positions in every image were extracted (Figure 66, cross sections 1-4). Then. by identifying the central position of each electrode in the line scan, it was possible to accurately determine the center of the crossbar that corresponded to the center of the device. Once the central region was identified, a horizontal cross-section over the area of the device was extracted taking the central value of this cross section as the reflectance value of the device at the moment when the image was captured. The cross marker of Figure 66 indicates the center of the device area identified by the program.

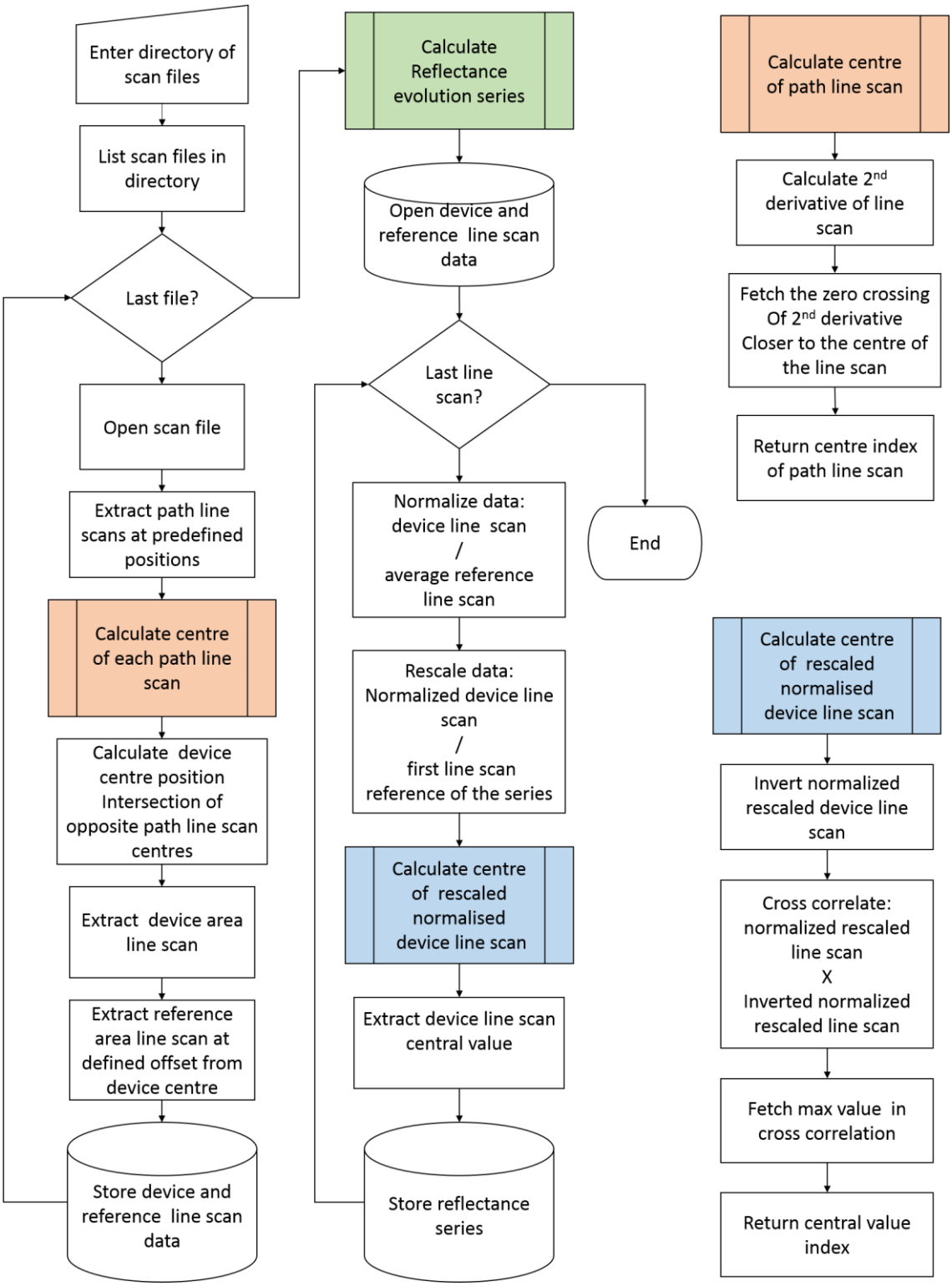


**Figure 65 Post processing algorithm for reflectance extraction from laser scans.**

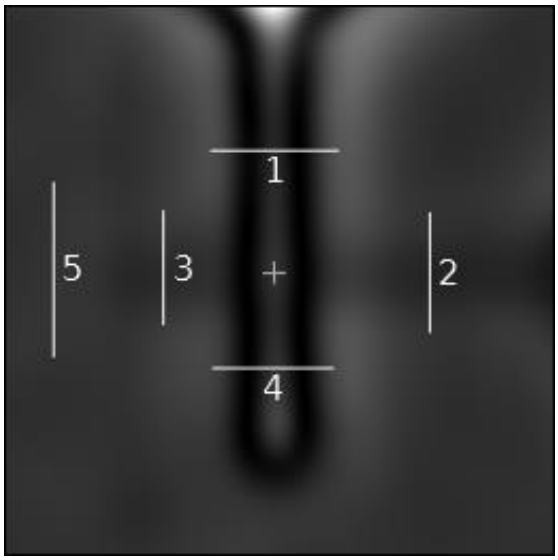


**Figure 66 Schematic of the linear scans for reflectance data post processing.**

To compensate for the temporal variations of the laser intensity, an additional cross section was extracted (Figure 66, cross section 5). However, in this case it corresponded to a substrate area located at a fixed distance from the device center where there were no features. It was assumed that the reflectance of this reference area did not vary during the experiment compared to the change of reflectance of the device. As a consequence, any change in the reflectance value of this reference area accounted for variations of the laser intensity. Further data processing re-scaled the extracted cross sections of the device areas, with the values obtained from the reference areas at every image.

To analyze the evolution of the reflectance during the experiment, the intensity of each image was further re-scaled, taking the reflectance of first image of the series as a reference for the subsequent images of the same experiment. Lastly, the cross-sections of the device areas were re-centered and the central value of each section was extracted. This produced a series in which each data point corresponded to the reflectance extracted from an individual image, with the whole series showing the evolution of the

reflectance of the device during the experiment. Figure 67 shows the before-mentioned steps for post-processing of the change of reflectance of a typical device.

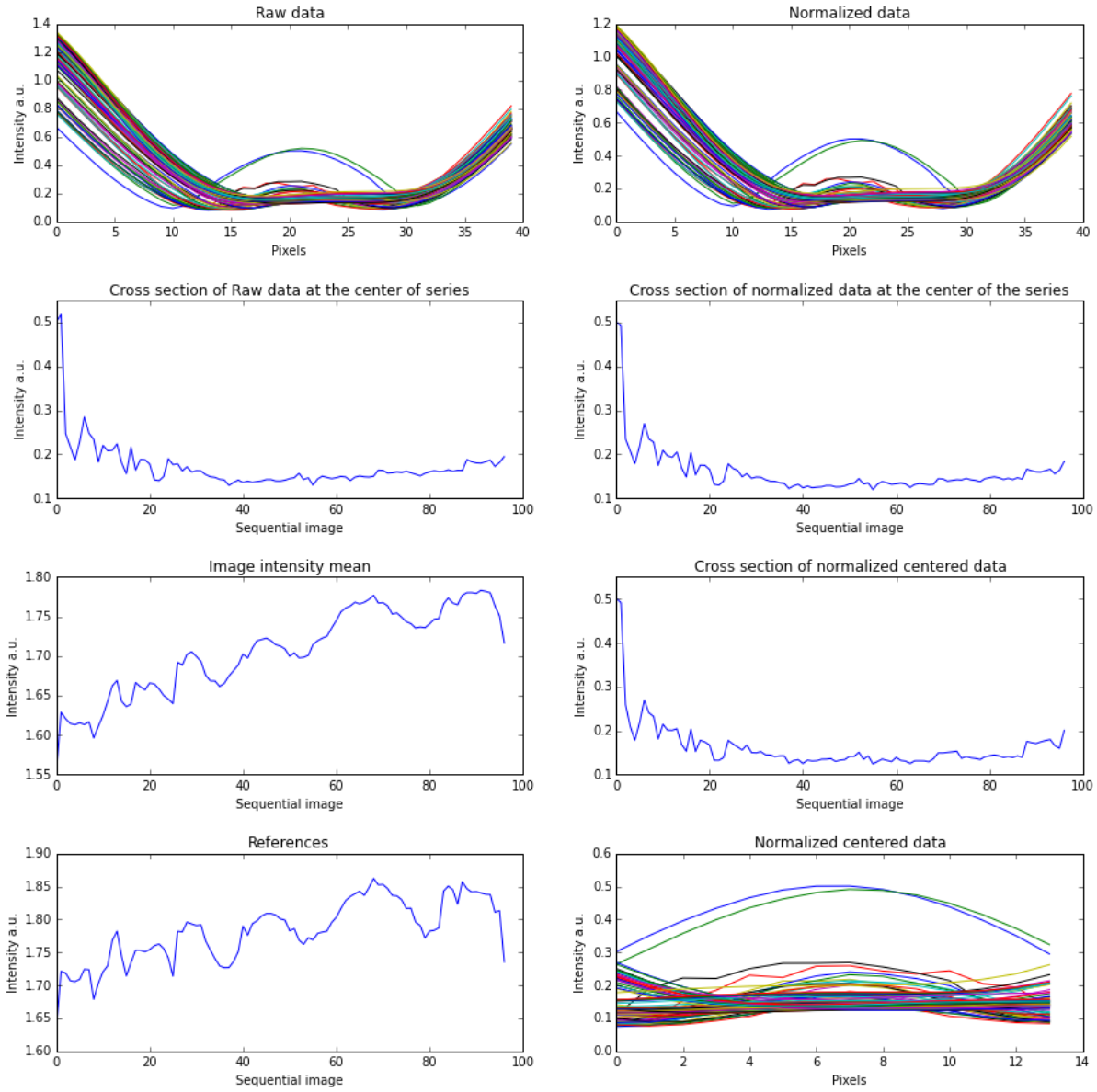


**Figure 67 Reflectance extraction post processing steps. The raw data is first re-scaled, considering the variations of laser intensity of the references and the first measurement of the series, then al the series are re-centered and the central data of the re-scaled, centered data is extracted.**

### 6.2.3 Single point resistance measurements

During the *mixed mode* experiments it was required to regularly measure the electrical resistance of the device in order to monitor its evolution as the GST changed phase. The resistance measurements were performed by a single point acquisition at a pre-defined voltage. Such voltage was selected to be low enough to avoid perturbing the state of the device. The measurement was performed with the source meter (Keithley2614B) and consisted of applying the selected measuring voltage to the device while simultaneously measuring the current to calculate the resistance. The resistance calculation was internally performed by the source meter. The integration period of the single point resistance measurement was 20ms, or one Power Line Cycle as explained previously in section 4.5.4.

### 6.2.4 Thermal model

In order to estimate the amount of optical power required to optically switch the nano-devices, a COMSOL® Multiphysics model was used. The model consisted of two parts. The first one was a simplified 2-D abstraction that represented the layers of different materials that formed the nano-device. By simulating the way an incident electromagnetic wave of the same wavelength as the laser beam propagated through the geometry, it was possible to quantify the energy losses due to absorption within the device. Figure 68 shows the solutions obtained for the first part of the model, and the profile of the energy losses due to absorption.

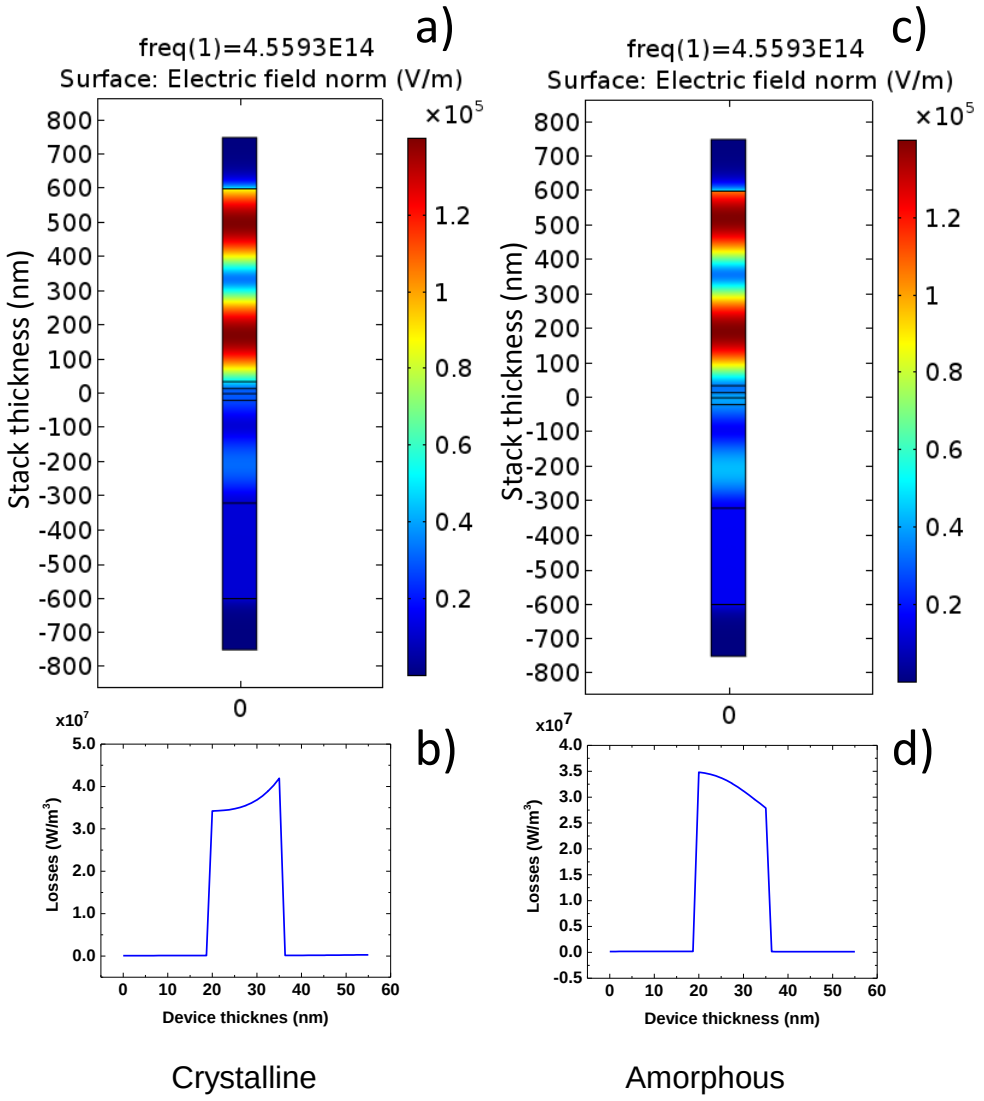


**Figure 68 Calculation of optical losses, equivalent to the power turned into heat. a) Electric field distribution of a normal incident beam of 658nm on the optical stack with crystalline GST layer, b) representation of the optically absorbed power for crystalline GST. c) Electric field distribution of a normal incident beam of 658nm on the optical stack with amorphous GST layer, d) representation of the optically absorbed power for amorphous GST**

The second part of the model was a 3-D heat transfer simulation that represented the geometry of the crossbar nano-device (Figure 69a). The heat source utilized was calculated based on the energy losses obtained from the first part, therefore assuming that the energy lost due to optical absorption was transformed into heat (Figure 68b, d) and dissipated through the device geometry. One important consideration for the reliability of the solutions obtained by Finite Element Analysis is the selection of the appropriate mesh size. For this model, the mesh used was a free tetrahedral with element sizes automatically assigned between 7.5 and 175nm. Given that the smallest feature in the model was the 15nm GST layer, 7.5nm minimum element mesh size provided enough resolution to obtain a reliable solution. Figure 69b shows a schematic of the meshing of the geometry, Figure 69d shows a detail of the meshing in the device area.

The temperature distribution across the cross-bar structure, obtained by applying 65mW optical power to a crystalline device is shown in Figure 69c. It can be seen that the heat is sourced from the top electrode that contains the GST, which is the most optically absorptive element of the geometry. Figure 69e shows a 2-D cross section corresponding to an XY plane at the interface between the ITO bottom electrode and the GST film. In this figure is possible to observe that the heat flows out of the device through the ITO bottom electrode. As a consequence, a temperature gradient is created within the device. Then, according to the simulation, there is a temperature difference of approximately 200K between the edges at the bottom electrode, and the central region, as can be seen in the cross section of the temperature gradient shown in Figure 69f.

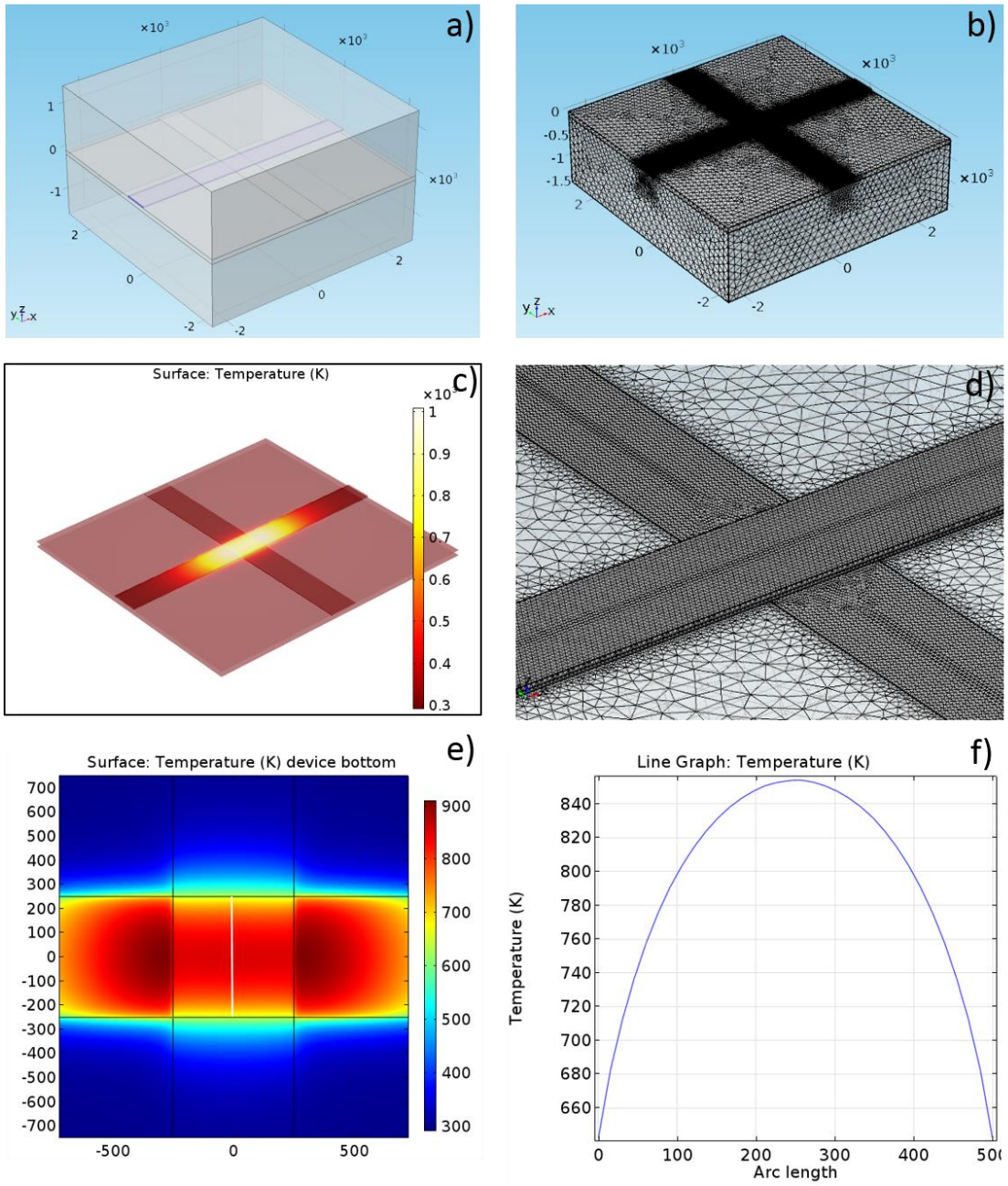


**Figure 69 COMSOL thermal model. a) 3D geometry of the heat transfer model. b) Mesh used in the FEA solver. c) Thermal response obtained by optically heating the device with a laser beam of 65mW of power. d) Detail of the meshed geometry. e) 2D cross section at the bottom of the GST thin film that shows a temperature gradient due to heat dissipation via the bottom electrode. f) Cross section of the temperature gradient inside the device, obtained from line insert in figure e).**

By using this model, it was estimated that the minimum optical power required to reach the crystallization temperature across the device was approximately 20mW. The list of parameters used for the second part of the model are shown in Table 5. It is important to mention that this is a static model that does not consider transient dynamics between phases of the GST.

| **Material** | **Thermal conductivity (W/m·K)** | **Density (kg/m³)** | **Heat capacity (J/Kg·K)** |
|---|---|---|---|
| ITO | 11 | 7160 | 340 |
| $SiO_2$ | 1.4 | 2650 | 733 |
| GST (cry) | 0.53 | 5995 | 218 |

**Table 5 Material parameters used for the COMSOL heat transfer model.**

## 6.3 Electrical testing

The first step prior the *mixed mode* experiments was to verify that the devices were working electrically. Electrical testing was necessary to confirm that there were no short circuits between the electrodes and that the layer of GST showed the characteristic switching behaviour. This was verified by performing an I/V measurement in one of the devices of the chip. By analysing the I/V response, it was also possible to identify the threshold voltage in order to operate the device in the non-linear region before the threshold switching, as well as to select the voltage level used to perform resistance measurements without perturbing the state of the GST. Figure 70 shows the I/V curve obtained from one devices of the chip. The characteristic switching behaviour can be

observed. From this measurement, the selected value for resistance measurements was set to 1V, because the sub-threshold non-linear region starts at approximately 3.5V and the threshold switching occurred at approximately 6.5V.

It is important to notice that although the threshold voltage of these devices is sufficiently low to operate them with the instruments available in the experimental setup (10V pulse generator maximum output), it is still about one order of magnitude higher than standard operational PCM voltages (<1V). This may be attributable to the sub-standard conductivity of the ITO used in the electrodes, as discussed in section 5.3.2. Highly resistive contact pads generate parasitic voltage drop in the paths, increasing the threshold voltage of the entire device. However, the cross-bar devices fabricated, present significant improvement over the planar devices fabricated previously and discussed in section 3.4.1.

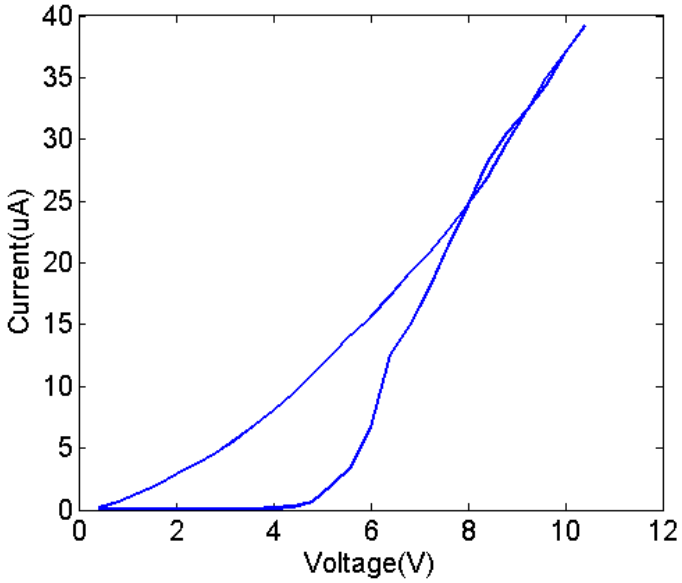


**Figure 70 Characteristic I/V curve of a 500x500nm device**

## 6.4 Optical excitation, electrical measurements

The first *mixed mode* experiment performed was to demonstrate how optical pulses would modulate the resistance of the as-deposited-amorphous GST in the nano-devices. In this experiment, the nano-devices were subjected to a series of optical pulses to induce crystallization by accumulation, as demonstrated by Wright *et al* [54].

Accumulation occurs by controlling the energy of the optical pulse in such a way that subsequent pulses increase the crystallinity of the GST. The optical pulses applied were 50ns in duration and 13mW in power. This combination allows for a steady progression from the initial, as-deposited amorphous state to the crystalline one. After each optical pulse, a single point resistance measurement was performed. Figure 71 shows the evolution of the resistance for two devices of dimensions 500 nm x500 nm and 1 µm x1 µm. As can be seen, the resistance value in both devices gradually drops by approximately three orders of magnitude in response to the optically induced crystallization. The change in magnitude of the resistance corresponds to the characteristic change of as-deposited amorphous to crystalline states of GST. This result clearly shows that by changing the phase of the GST nano-devices by optical pulses, a corresponding change in resistance occurs. This experiment confirms the findings of the experiment performed previously and explained in Chapter 3.

Another observation obtained from Figure 71 is that the 500x500nm device reached the lowest resistive value with significantly less pulses than the larger 1µmx1µm device. A possible explanation for such response could be in terms of heat dissipation. As mentioned previously in section Thermal model6.2.4, after the optical pulse is applied, the heat dissipates mainly through the ITO electrodes. Given that the thickness of the GST layer of both devices is the same (15nm), the ratio of device area vs. electrode

contact varied by a factor of two, increasing the heat dissipation of the device and causing as a consequence the observed decrease in the rate of progression towards crystallization.

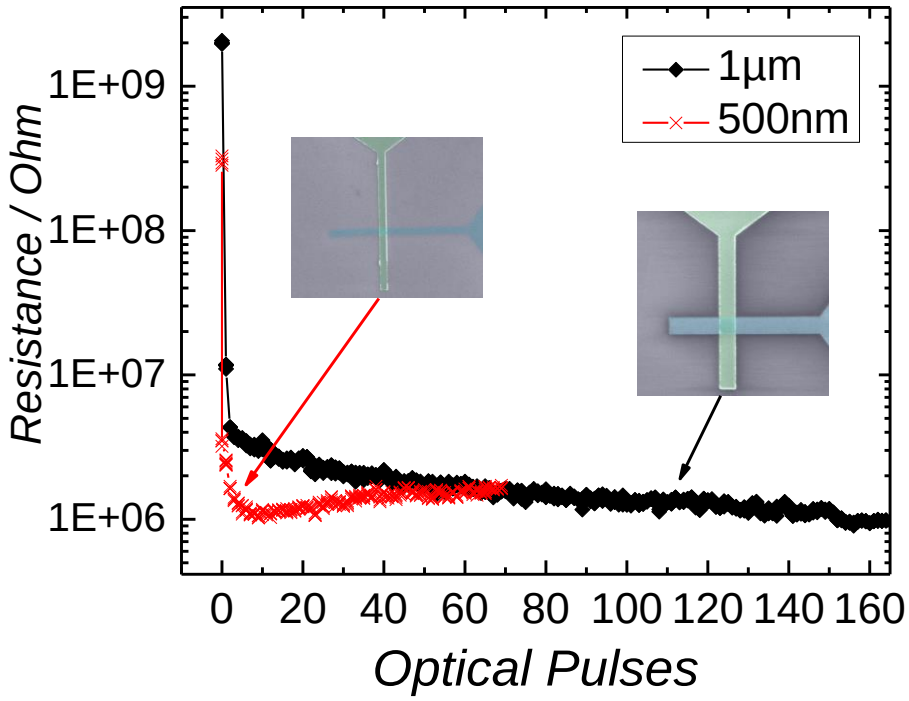


**Figure 71 Evolution of resistance of the nano-devices against consecutive optical pulses.**

## 6.5 Electrical excitation, optical and electrical measurements

Having shown that the optically induced phase change in the nano-devices can be observed electrically, the next experiment was to demonstrate the relationship of the reflectance upon electrically-induced crystallization. This experiment consisted of applying a series of electrical pulses to a 500x500nm device and measuring its resistance and reflectance after each pulse. The selected pulses applied were 2.5V and 100ns duration, which allowed for a steady accumulative transition, following the

procedure demonstrated by Wright *et al* [53] . According to such a procedure, it is possible to achieve accumulative crystallization of GST by applying voltage pulses selected below the sub-threshold switching region (see Figure 70).

It is important to note that this experiment was expected to be the more challenging, given the nucleation-dominated crystallization mechanism of GST. It is known that when electrically switched, GST would tend to form conducting crystalline filaments. Such filaments would then form highly conducting paths that would appear electrically as if the GST had switched, but the change may not be observable optically.

The reflectance measurements were performed by acquiring sequential images with the laser microscope by scanning with a low intensity laser beam of 1mW. These images were then post-processed following the method described in section 6.2.2. Capturing images served two purposes. Firstly, after every scan it was possible to re-aim the laser before applying the next pulse in order to compensate for stage drift. Secondly, it meant that enough information was acquired to compensate for drift and laser intensity variations between images.

Figure 72 shows the evolution of the reflectance and resistance while electrical pulses were applied. Noise from the reflected power data was removed by a sliding window average filter with a window size of 5. It can be seen that as expected, the resistance decreases as more pulses are applied. However, the reflectance also decreases as number of applied pulses is increasing. This behaviour is counter-intuitive, given that the reflectance of the bulk GST increases upon crystallization for wavelengths in the visible spectrum[86]. In this case, however, such response can be explained if it is considered as a consequence of a shift in the resonance of the optical nano-cavity, formed by stacking the different layers that comprise the device. Figure 73 shows the

calculated reflectance response of the GST device as it experiences partial crystallization, measured at 658nm (wavelength of the laser-scanning microscope).

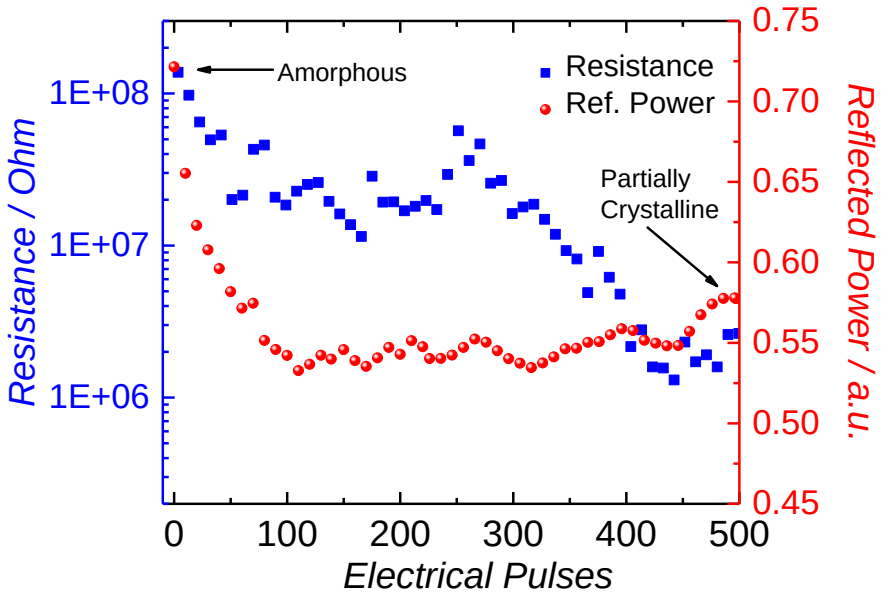


**Figure 72 Evolution of the resistance and reflected power as a function of the number of electrical pulses applied to a single 500nm device.**

The response shown in Figure 73 was calculated using the transfer matrix model described in section 5.2.1, and assumes that the partial crystallization of the GST layer occurred homogeneously within the material. From Figure 73 one can observe that while the GST transitions from amorphous to the crystalline state, a non-linear and non-monotonic response is expected, starting with a decrement in the reflectance. This response resembles the behaviour obtained experimentally and shown in Figure 72. However, the range of crystallinity measured optically during the experiment was only partial and corresponded to approximately 65% crystallinity as indicated by the grayed area of Figure 73.

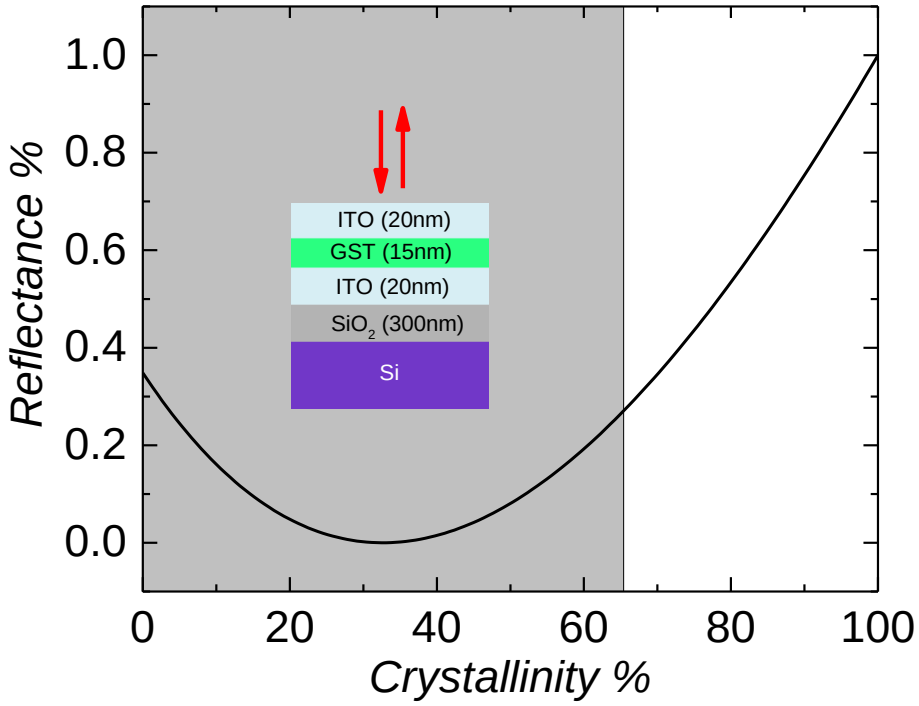


**Figure 73 Calculated optical response of the optical nano-cavity of the device per decree of homogeneous crystallization.**

The shift in the resonance of the optical nano-cavity is produced by the change of the refractive index of the GST upon crystallization[41]. Therefore, the response obtained suggests that the phase change is occurring to an extent that is optically detectable, despite the current understanding that the evolution of both optical and electrical responses depend on different crystallization mechanisms (percolation for the electrical case, and heterogeneous nucleation for the optical case, according the dual percolation model of Kim *et al* [65] ). The results shown in Figure 72 also oppose the idea of a non-observable optical change when the phase change is induced electrically caused by the formation of a conductive filament.

A possible explanation for the unexpected observation of optical response could be that no conductive path was formed immediately, because the voltage of the electrical pulses was selected to be in the sub-threshold region, so no electrical switching would occur.

However, the pulses may provide enough energy to induce heterogeneous nucleation, especially given the large area to thickness ratio of the device (~1:1600). This explanation is in agreement with the analysis provided by Kim *et al* [65], who suggested that in their observations heterogeneous nucleation dominated the crystallization process.

Another observation that can be made from Figure 72 is that an eventual drop of the resistance confirms electrically that the GST has been crystallizing, however the resistance change is not the expected 3 orders of magnitude, which suggests that the device is only partially crystalline, in accordance with the optical measurement.

More so, the evolution of the reflectance occurs before the final resistance drop. The fact that both measurements evolve differently in time suggests that the crystallization of the GST within the device may not occur homogeneously. These findings are similar to the ones observed previously by Liang *et al* [67] in an experiment where crystallization was induced optically. However, in the case of the experiment performed by Liang *et al*, a delay in the evolution of the reflectance in respect to the resistance was reported, contrary to the present observations. Their explanation was based on an extension of the dual percolation model of Kim *et al*, suggesting that when an optical pulse is applied on a horizontal region, heterogeneous nucleation produces a conductive path before the optical transition is observed. The results presented here show the opposite response, and it is suggested that this is due to the different device configuration. The device used in the presented experiments had a vertical configuration, with the electrodes located at the top and bottom of the GST thin film. Thus far, it seems reasonable to assume that time trends are opposite to the one of Liang *et al*, although the dual percolation model is able to describe both situations.

## 6.6 Optical excitation, optical and electrical measurements

Thus far, it has been shown that subjecting the GST nano-devices to optical pulses produced an observable change in resistance, and that by applying electrical pulses it was possible to induce an observable change in reflectance. In order to better understand the relationship between the changes in the evolution of these two physical properties, an additional experiment was performed by applying a series of 13mW optical pulses of 50 ns duration with 5ns falling edge, to a 500 nm x 500 nm device, similar to the experiment shown in section 6.4. However, in this case, both resistance and reflectance were monitored, and most importantly, the pulses were continuously applied after the device reached the lowest resistance value in order to provide further evidence of the crystallization dynamics of the nano-devices.

It can be seen that by continuously applying optical pulses, the device response becomes apparently erratic. However, a correlation between optical and electrical signals can be observed. In order to understand such correlation, it is required to look at the optical response of the device in terms of partial crystallization, shown in Figure 75. The reflectance in terms of crystallinity has been divided in two regions. Region (I) occurs when the GST is between 0 and ~35% crystalline. When in this region, changes in reflectance and resistance follow the same trend, i.e. decreasing as the crystallinity increases. By contrast, in Region (II) when the GST is over ~35% crystalline, the reflectance and resistance have opposite trends. Following this logic, Figure 74 has been divided into sections. Each section highlights how the trends of the reflectance and resistance are either opposite or follow each other, corresponding to the regions (I) or (II) shown in Figure 75.

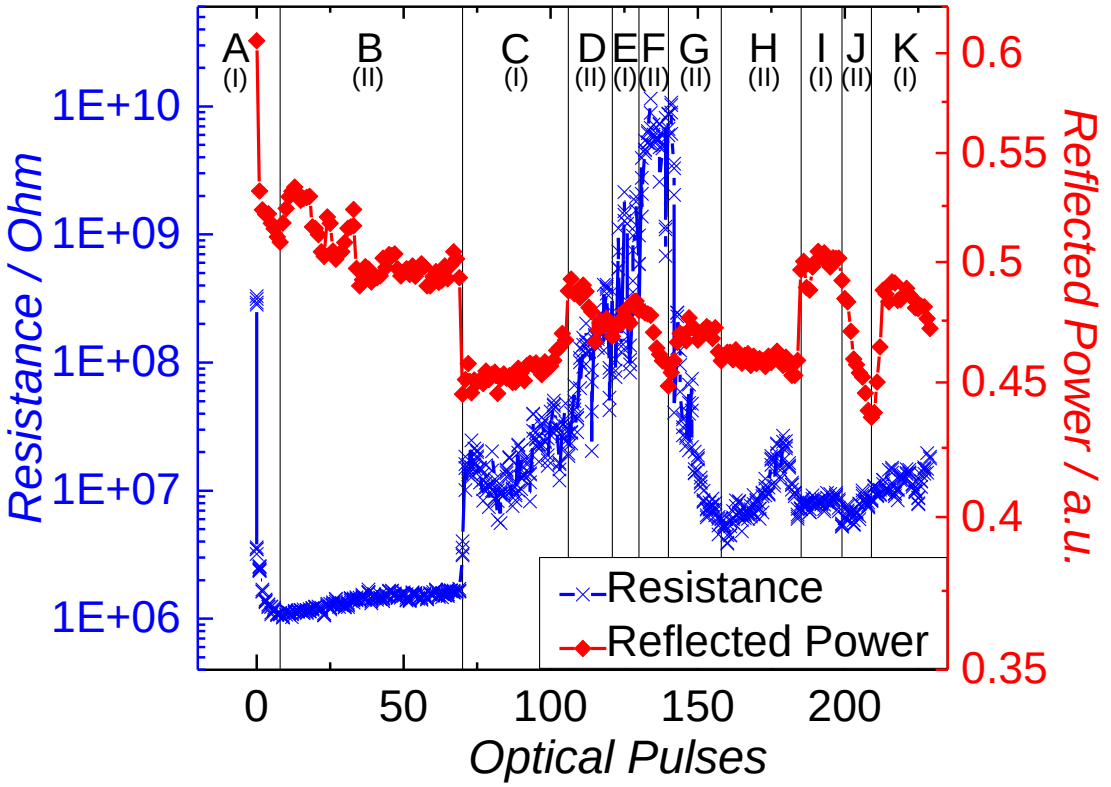


**Figure 74 Evolution of Resistance and Reflectance by applying optical pulses, divided by regions where trends either correspond or opose each other.**

Region (A) in Figure 74 shows the expected response as the GST crystallinity increased monotonically. However, after more optical pulses were applied, the device responded differently. In region (B) for instance, the trends are opposite, which indicates a transition to the Region (II) of Figure 75. In addition, the increment in resistance and decrease in reflectance of region (B) suggests that the crystallinity of the GST decreased in comparison to region (A). The occurrence of amorphization, then, is the best hypothesis to explain the apparent erratic behaviour of subsequent regions, but it only occurs after GST had reached certain crystallinity level, achieved during Region (A). The reason for this is that as the GST becomes more crystalline, the absorbance increases (See Figure 57) and consequently the amount of heat generated by an optical

pulse, despite the pulse being identical to the ones applied previously that induced crystallization. As it was mentioned earlier, optical pulses selected for the experiment had sharp falling edges of 5ns so they could induce amorphization of the GST.

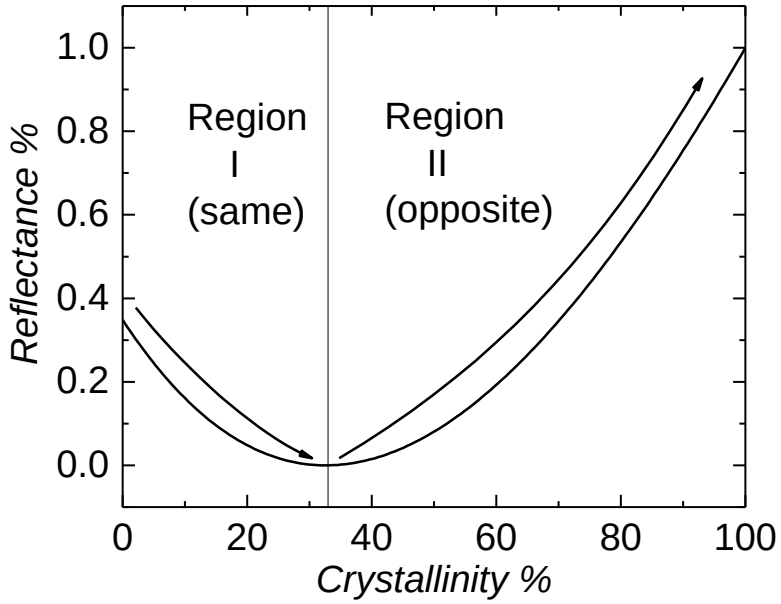


**Figure 75 Calculated optical response the device vs. degree of homogeneous crystallization divided in two regions according to the reflectance trend.**

Correspondingly, when partial amorphization occurs, the absorbance of the device decreases, so subsequent pulses would more likely induce crystallization of the GST, causing the device to traverse back and forward between Regions (I) and (II) of the nano-cavity's optical response shown in Figure 75.

Another important observation that can be made from Figure 74 is that transitions between Regions (I) and (II) do not always occur at the same levels of resistance and reflectance. This suggests, similarly to the previous electrically induced phase change experiment, that the crystallization within the device is not homogeneous. The inhomogeneity of the crystalline region within the device, could have a layered

structure similar to the one observed by Putero *et al* [87], which also implies the possibility of regions where phase segregation occurs. However, independently from the organization at the nanometer range, the possibility of operating the device at different degrees of partial crystallization exists.

One important disclaimer regarding the data of this particular experiment is the fact that the value of the resistance series in Figure 74 Region F, is higher than the initial value shown in Region A, this may be caused by the electrical testing of the device. Before mixed mode experiments, each device was tested electrically, without switching it but to verifying that the characteristic nonlinear resistance in the pre-threshold switching region existed. This test may have partially crystalized the device, in such a way that when amorphization occurred, the resistance reached a higher value than the initial one of the mixed mode series, as shown in the data.

## 6.7 Opto-electronic memory

Up to now, it has been shown that despite different mechanisms being responsible for the resistance and reflectance responses, when crystallization occurs, whether it is induced optically or electrically, it is possible to observe a correspondence between both measurements. Therefore, the next experiment consisted in a demonstration of *mixed mode* electro-optical operation by alternating optical and electrical stimuli.

For this experiment, the device was first conditioned optically until it reached the lowest resistance state, followed by a 4V I/V curve (Figure 76a). Hence, it was assumed that the device started in crystalline state. Different combinations of optical pulses, powers and durations were attempted to re-amoprhize the device. It was found experimentally that four series of 50 optical pulses (200 pulses in total) of 85ns at 66mW was the

combination that better partially re-amorphize the device in a repeatable way. Figure 76b shows the schematic electrical pulse used to drive the laser diode and produce a single optical pulse, of the series.

For each iteration of the *mixed mode* experiment, the device was crystallized (SET) electrically by an I/V curve as the schematic shown Figure 76a, and partially re-amorphized (RESET) by the series of optical pulses described previously. Figure 77 shows the result of 10 iterations of the *mixed mode* experiment. It can be seen that after the application of the optical RESET pulses, the value of the resistance increases. On the other hand, after the electrical excitation, the resistance decreases again, indicating that the crystallinity of the GST has increased.

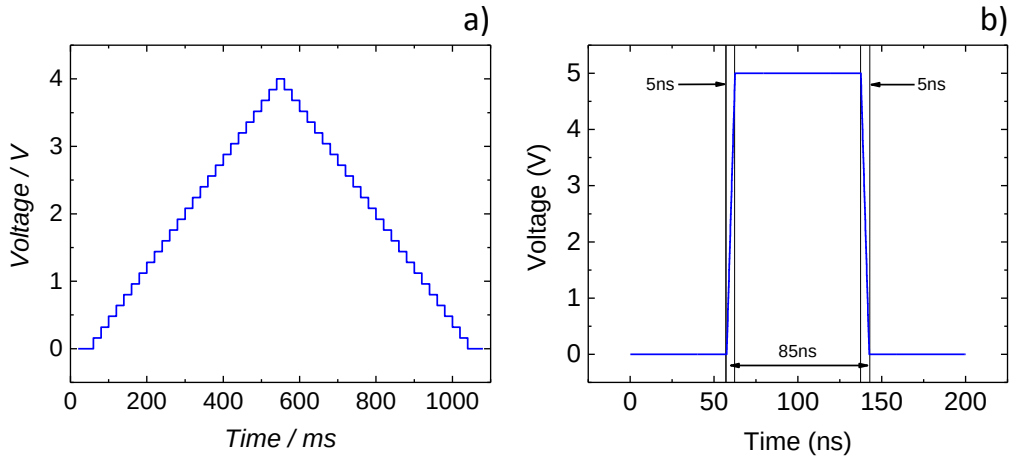


**Figure 76 Schematic of mixed mode stimuli. a)SET 4V ramp. b) Schematic of electrical pulse used to drive the laser diode to generate the RESET optical pulses. Pulse width is 85nm with 5nm at the edges; Amplitude of 5V produced 66mW optical power output from the objective.**

It should be noted from Figure 77 that resistance changes approximately by a factor of three, which is significantly less than the 1000x times change observed in the first transition from as-deposited amorphous to crystalline demonstrated previously in

Section 6.4. Previous studies have shown that the contrast resistance from the first as-deposited-amorphous to crystalline transition is larger than from further re-amorphized to crystalline transitions, due to the creation of super-critical nuclei in the material, that remain after melting-quenching re-amortization [88]. However, such an effect is not enough to account for the observed reduction in resistance contrast.

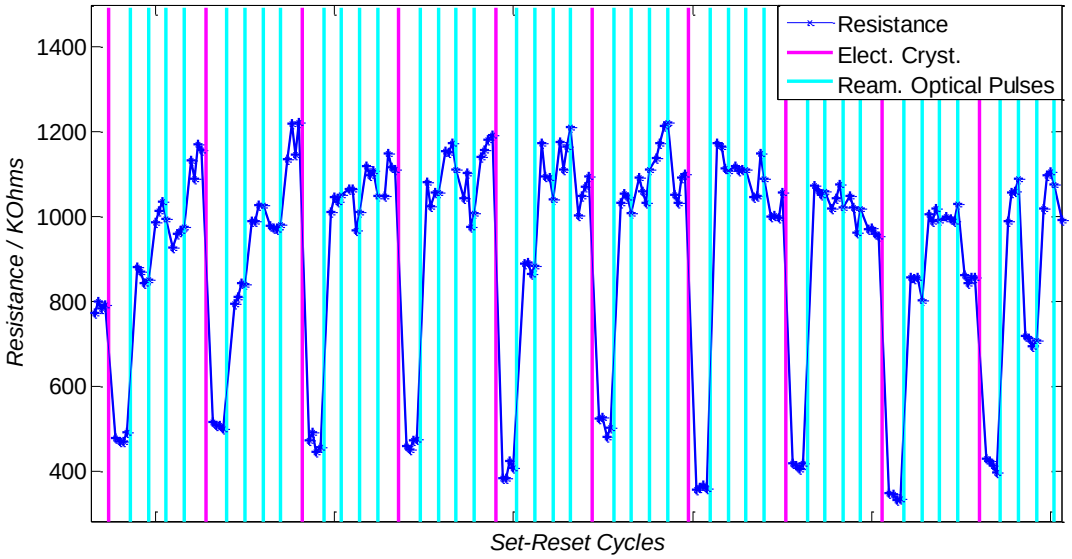


**Figure 77 Evolution of the resistance during 10 iterations of electrically induced crystallization and optical reamorphization.**

A possible explanation for the reduced resistance change comes from the observation that the low resistance level (SET state) corresponds to the lowest resistance measured. According to the device conditioning assumption that the initial state of the device was crystalline, it can be suggested that the change in resistance observed during *mixed mode* operation occurred between the assumed fully crystalline state and a partially re-amorphized state. As explained previously in section 6.6, it is expected that the device will be operable under different partial crystallization states. Also, given that the crystalline state is thermodynamically favorable, it is reasonable to assume that the

stability observed between SET and RESET stimuli in the *mixed mode* experiment was a consequence of the predominant crystalline state.

Despite requiring 200 pulses of 66mW, the device crystallized only partially. This could be explained by the information obtained from the thermal simulation presented in section 6.2.4. Due to the thermal properties of the device, a temperature gradient was created within the GST thin film during optical heating (Figure 69c,d). Such a temperature gradient suggests that certain areas in contact with the bottom electrode did not reach the melting temperature, making it impossible to re-amorphize the device entirely. Nevertheless, enough partial re-amorphization has occurred that resistance was sufficiently modulated to demonstrate *mixed mode* electro-optical operation in GST-based nanoscale devices.Finally, in order to demonstrate that the device was not subject to damage by ablation or electrical breakdown, a SEM image was captured and it is shown in Figure 78.

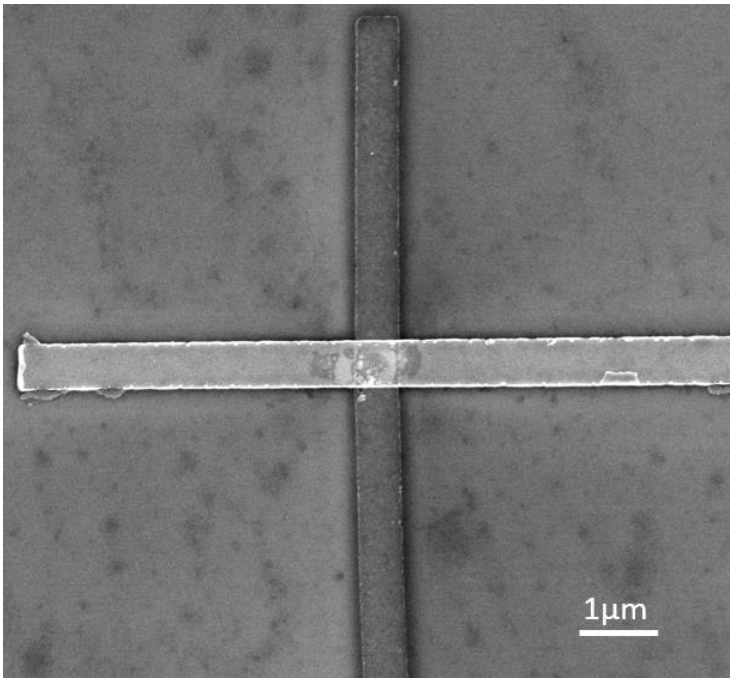


**Figure 78 SEM image of the 500x500nm device after mixed mode experiment. Sings of crystallization are visible, but no ablation damage occurred.**

## 6.8 Conclusion

In this chapter, a series of experiments have been presented which show for the very first time in GST-based nanoscale devices that a complex relationship exists between the resistance, reflectance and crystallinity. It has been demonstrated that such relationship exists irrespective of the means used to induce the crystallization (i.e. electrical or optical pulses). An optically induced phase change can produce a change in the device resistance, while an electrically induced phase change can be observed as a change in reflectance. Different mechanisms have been suggested for each case according to the results obtained and their interpretation in relation to previous studies. For the electrically induced phase change, heterogeneous nucleation is the proposed cause for the optical response. On the other hand, partial crystallization is responsible for the electrical response due to optical pulses. For these experiments accumulative pulses have been used.

It has been suggested that that partial crystallization of the GST within the device is not homogeneous due to differences in absorbance and intrinsic thermal properties of the device. However, it was not possible from the results obtained to confirm whether phase segregation occurs within the device, and the locations of crystalline/amorphous regions. It is important to mention that it is known that GST experiences a volumetric contraction of approximately 7% when it crystalizes. This contraction was taken into the account while developing the model of the optical response upon partial crystallization, because thin films optical stacks are commonly highly sensitive to thickness variations. However in this case no significant difference was found between optical models with or without contraction compensation. Additionally, volumetric contraction has been associated to the resistance drift phenomena in PCM, however in

the case of this study, the effect of the residual strain in the device due to GST contraction has not been taken into account, due to the long time scales of the resistance drift that are significantly larger than the duration of the experiment, so the effects are in this case, neglected.

To conclude, a proof-of-concept GST based opto-electronic memory nano-device capable of mixed *mode* electro-optical operation, has been presented. This has been achieved by crystalizing it electrically and re-amorphizing optically while the resistance values show two different repeatable states. These results represent a stepping stone towards the realization of the memflector [61] as well as other opto-electronic devices for future applications that require a memory element capable of operating electrically and optically. Such applications include opto-electronic interfaces for integrated photonic circuits[89][52], in addition to potential new technologies like accumulative optical pulse detectors or synthetic retinas. These will be considered in more detail in Chapter 7.

# 7 CONCLUSIONS AND FUTURE WORK

## 7.1 Thesis summary

The aim of this Doctoral Thesis was to investigate the potential use of the phase change material $Ge_2Sb_2Te_5$ in the realization of opto-electronic memory devices. In order to do that, an experiment was conceived to measure the change in optical and electrical properties of GST nano-devices. Such experiment included the fabrication of nano devices, and the construction of an experimental setup to perform the measurements. Chapter three describes in detail the way initial experiments were performed by adapting a previously existing laser system based on a modified optical microscope that allowed to focus a 405nm laser beam into a 500nm spot. Custom designed planar nano-devices were fabricated following a bow tie design that allowed optical and electrical access to the GST layer. Electrical access was achieved by contacting the GST layer by two Pt lateral electrodes; optical access was obtained via a transparent window made of $SiO_2$ capping layer material. However, it was found that due to manufacturing challenges and the intrinsic limitations of the design, such planar devices were not

suitable to be operated electrically, because of their high resistance, which was a direct consequence of the length of the GST device region (1μm). Nevertheless, it was possible to perform one experiment of the different mixed mode electro-optical operation combinations. Such experiment observed the change of electrical resistance when the phase change of as-deposited amorphous to crystallize was induced by accumulative optical pulses. The result of this experiment was sufficient to confirm a correlation between the evolution of reflectance and resistance, demonstrating the feasibility of the *mixed mode* electro-optical operation of GST based nano-devices.

However, after performing the preliminary experiments, it was clear that an alternative experimental setup with better specifications in terms of position repeatability and stability was required. Additionally a different type of device was necessary in order to verify the response of the devices to both different combinations: optical and electrical induced crystallization, as well as *mixed mode* operation. A new experimental setup was designed and built from scratch. The new experimental setup was designed as a laser scanning microscope accessory that fitted into an Asylum AFM. The XY precision piezo stage of the AFM was used by the laser scanning microscope to perform the raster scans. A compact and lightweight fibre coupled laser objective was fabricated by using a GRIN lens as the focusing element, coupled to an optical fibre. The combination of the GRIN lens with the optical fibre allowed for long working distance, as well as a confocal configuration that improved the quality of the raster scan images reducing the spurious reflections by using the optical fibre as the pinhole element of the confocal setting. The fine displacement of the Z axis used to focus the laser on the sample was achieved by a custom made piezo-buzzer linear actuator that hold the laser objective. All the details of the experimental setup built for this experiment are detailed in Chapter 4 of this thesis.

In addition to the new experimental setup, a new type of cross-bar vertical nano-devices were manufactured, by encapsulating a GST thin film between transparent ITO electrodes which allowed the nano-devices to be operable optically and electrically. By using vertical devices, the resistance value of the device was reduced to crossed section of the GST think film (15nm) in comparison with 1μm of the planar devices used in the preliminary experiments. However using a very thin film of GST reduced the optical contrast. In order to maximize the optical contrast and make the phase change optically observable a tuneable optical nano-cavity effect caused by the combination of the transparent electrodes, the GST and bottom substrate was used during the nano-devices design. Making small adjustments to the thicknesses of each layer it was possible to tune the resonance peak of the reflectance response, to maximize the contrast between amorphous and crystalline states, achieving ~20% contrast change, similar to a 50nm film used in optical data storage media. The fabrication process required to overcome a series of nano-manufacturing challenges, including the process characterization to optimize the conductivity of ITO thin films, and how to contact the ITO electrodes with metallic electrodes. All the details about the vertical nano devices were described in Chapter 5.

Further *mixed mode* experiments using the custom made optical set-up described in Chapter 4 in combination with the cross-bar vertical devices described in Chapter 5, were presented in Chapter 6. Such experiments showed that crystallization induced by accumulative optical pulses can be measured electrically, further confirming the preliminary results described in Chapter 3. Additionally, it was shown that electrically-induced crystallization by means of accumulative pulses produces an optically detectable response. It was also found how different degrees of partial crystallization occur within the device, suggesting that it is possible to operate the devices under

different partial crystallization conditions. By studying the change of reflectance in combination with the change of resistance, considering the non-monotonic optical response caused by the optical nano-cavity, it was possible to demonstrate the direct correlation between optical and electrical responses, and explain the way crystallization occurred within the nano-device, according to the dual percolation model, described previously in the literature.

With the understanding of the crystallization dynamics of the nano-devices, gained by the different sets of experiments, a proof of concept of an opto-electronic memory that operates in *mixed mode,* was demonstrated by crystallizing the GST based nano-device electrically, and partially re-amorphizing it optically while a repeatable three fold change in resistance was observed. Thermal simulations suggested that the way heat was dissipated around the device created thermal gradients internally, causing non-homogeneous crystallization/amorphization of the GST within the device limiting the change of resistance to a factor of three instead of the expected thousand.

It was concluded based on the observations that the crystallization of the GST material within the device is not homogeneous, and the possibility of phase segregation exists, as it has been reported before in the literature. The analysis performed in this work, provided enough understanding to be able to effectively demonstrate *mixed mode* operation. However, future works would benefit from adding TEM studies to further understand the evolution of the material at the atomic level in order to verify the hypothetical occurrence of phase segregation.

The present work is the first that studies the operation of GST based opto-electronic memory devices, and has, within its limits, demonstrated the potential that exists in the development of opto-electronic applications using GST. The main limitation of the

present work is derived from the limitations of the instruments used for data acquisition. Such instruments were designed for low speed measurements (KHz range), therefore, the study of the transient phenomena was not considered in this thesis. Gradual crystallization was instead achieved by the used accumulation techniques demonstrated in GST, caused by its nucleation dominated nature. Nevertheless, the laser scanning microscope built as part of this work could potentially be overhauled by adding high speed electronics equipment to perform transient phase change experiments. (i.e. semiconductor analyser, pico-second laser, picosecond photodetector, etc.).

## 7.2 Future work

The present methodology and experimental set-up provides a stepping stone for further research into the opto-electronic response and applications of GST. Future directions continuing the work presented in this thesis could include the following:

- Perform capacitive measurements to provide further evidence towards the occurrence of phase separation of GST within the device during crystallisation. Additionally such study could provide more information towards the understanding of the way the GST crystalline region grows within the device, as this was not possible to be determined in the present Thesis.
- Comparative study of GST with other phase change materials. GST was selected in this Thesis because it is the most widely studied phase change material. However, the present work could be expanded by using it as a bench mark to study mixed mode operation of other phase change materials. One potential candidate for comparison could be the binary compound GeTe. This compound has also been widely studied, and possess similar characteristics to GST. However, opposite to GST, GeTe crystallisation mechanism is growth

dominated. By comparatively studying these two different phase change materials, it could be possible to further understand the role of the intrinsic crystallisation dynamics of the material in the mixed mode operation.

- Transient mixed mode measurements. As mentioned before, it could be possible to extend the capabilities of the experimental set-up, by incorporating high speed electronics. This will enable the system to detect the transient phenomena of the mixed mode operation in order to explore the contribution of different sources of excitation (optical or electrical) in the crystallisation of the GST, without relying on the accumulation techniques used in this Thesis.
- The creation of a new device architecture with improved thermal properties. As it was shown in Chapter 6, the cross-bar devices used in the *mixed mode* experiments, suffered from uneven heat distribution, which limited the stability and operational range of the devices. Therefore, a new device design, with more homogeneous heat distribution characteristics that also maintains the tuneable contrasts provided by the optical stack configuration, could be envisioned.
- Combination of optical signals with electrical bias and vice-versa. It has been shown in the literature[39][38][90] that the presence of an electric field influences the crystallization behaviour of the GST. Therefore, it should be possible to tune the sensitivity of the opto-electronic devices by electrically modulating the crystallization threshold.
- New type of photo detectors. Given that the GST has a broad absorption spectra, it should be possible, by carefully choosing the optical stack characteristics, to produce devices with spectral selectivity to the point of achieving narrow-band, low power, large dynamic range, ultra-fast, electrically-readable non-volatile photo detectors that could have many applications. Such applications include,

future interfacing between photonics and electronics, high speed optical communication detectors, high speed cameras, artificial retinas and many more.

## 7.3 Main contributions

In summary, it is claimed that the present thesis further advances the state of the art by the following contributions:

- Designed an experiment and the required methodology to characterize the optical and electrical response of GST in nano-devices.
- Designed and built of a custom made experimental set-up comprised of two parts, a laser scanning microscope which allowed optical access to the nano-devices and provided sufficient optical power to induce phase change; and the electronics assembly required to perform resistance measurements and induce the phase change by electrical pulses.
- Presented the first experimental study on the relationship between optical and electrical response of GST in nano-devices. By using partial crystallization via accumulation, it was possible to obtain insights on the different crystallization mechanisms. Evidence is provided of the electronically observable phase change induced optically and vice versa. It is proposed that the crystallization within the devices may not be homogeneous due to the intrinsic thermal properties of the device and differences in absorbance.
- Provided a proof of concept of a novel non-volatile opto-electronic memory based on GST a nano-device. The device was operated in *mixed mode*, SET electrically, RESET optically, with electrical readout.

# 8 LIST OF PUBLICATIONS

## Conference presentations:

C. David Wright, Harish Bhaskaran, **Gerardo Rodriguez-Hernandez**, Peiman Hosseini, Jorge A. Vazquez Diosdado and Wolfram H P Pernice. "Beyond von-Neumann Computing with Phase-change Materials and Devices", MRS Spring Meeting, San Francisco, 1st - 5th Apr 2013

C. David Wright , Yat-Yin Au , Mustafa M Aziz , Harish Bhaskaran , Rosie Cobley , **Gerardo Rodriguez-Hernandez** , Peiman Hosseini , Wolfram H P Pernice and Lei Wang, "Novel Applications Possibilities for Phase-Change Materials and Devices". European \ Phase Change and Ovonics Sympsium 2013.

**G. Rodriguez Hernandez**, P. Hosseini, C. D. Wright, W. H. P. Pernice, H. Bhaskaran, "Mixed-Mode Electro Optical Properties of $Ge_2Sb_2Te_5$", ISOM 2013, Seoul (South Korea).

P. Hosseini, C. Rios, **G. Rodriguez Hernandez**, Y.Y. Au, W. Pernice, C.D. Wright and H. Bhaskaran, "Phase Change Memories, Memristors and Memflectors", CIMTEC 2014, Montecatini Terme (Italy).

Wright C.D., Au Y, Bhaskaran H., **Rodriguez-Hernandez G.**, Hosseini P., Rios C., Agarwal R., Pernice W.H.P. "'Mixed-Mode' Optoelectronic Applications Possibilities using Phase-Change Materials and Devices", MRS Spring Meeting, San Francisco, 6th - 10th Apr 2015.

**G. Rodriguez Hernandez**, P.Hosseini, C.Rios. C.D. Wright and H.Bhaskaran, "Phase change material based non-volatile optoelectronic interface for optical systems") CIMTEC 2016, Perugia (Italy).

## Poster presentations:

**G. Rodriguez-Hernandez** P. Hosseini and H. Bhaskaran, "Study of $Ge_2Sb_2Te_5$ properties for opto-electronic applications" American Ceramic Society, Electronic Materials and Applications (EMA) 2016, Orlando Florida, USA. (2nd Place best poster award).

## Papers:

**G. Rodriguez-Hernandez**, P.Hosseini, C.Rios, C.D. Wright, and H.Bhaskaran "Mixed-mode electro-optical operation of $Ge_2Sb_2Te_5$ nanoscale crossbar devices." Advanced Electronic Materials 2017, 1700079.

Syed Ghazi Sarwat, Pascal Gehring, **Gerardo Rodriguez Hernandez**, Jamie H. Warner, G. Andrew D. Briggs, Jan A. Mol, and Harish Bhaskaran. "Scaling Limits of Graphene Nanoelectrodes" Nano Letters, 2017, 17, 3688-3693.

## Patents:

Carlos A. Ríos Ocampo, Matthias Stegmaier, **Gerardo Rodríguez-Hernández**, Wolfram H.P. Pernice, and Harish Bhasakaran. Photonic Device (Tunable photonic circuits based on GST). PCT application number: PCT/GB2016/052871. Filed in Oct. 2014.

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