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Development of scalable electronics for the TORCH time-of-flight detector

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ABSTRACT: The TORCH detector is proposed for the low-momentum particle identification upgrade of the LHCb experiment. It combines Time-Of-Flight and Cherenkov techniques to achieve charged particle separation up to 10 GeV/c. This requires a time resolution of 70 ps for single photons. Existing electronics has already demonstrated a 26 ps intrinsic time resolution; however the channel count and density need improvements for future micro-channel plate devices. This paper will report on a scalable design using custom ASICs (NINO-32 and HPTDC). The system provides up to 8×64 channels for a single micro-channel plate device. It is also designed to read out micro-channel plate tubes with charge-sharing technique.

KEYWORDS: Cherenkov detectors; Instrumentation and methods for time-of-flight (TOF) spectroscopy; Particle identification methods; Photon detectors for UV, visible and IR photons (vacuum)

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1 Introduction

The Time Of internally Reflected Cherenkov light detector (TORCH) [1] is proposed for the low-momentum particle identification upgrade of the LHCb experiment [2]. In this detector, Time-Of-Flight (TOF) and Cherenkov techniques are combined to achieve positive $\pi/K/p$ separation up to 10 GeV/c. Cherenkov photons are generated from a 1 cm-thick quartz plate, which is segmented into small identical modules as shown in figure 1.

These photons propagate by total internal reflection to the edge of the plate. Subsequently, they are focused to an array of Micro Channel Plate (MCP) photon detectors at the periphery of the detector which time their arrival. In order to achieve effective π/K separation, a time-of-flight resolution of 15 ps per track is required at a distance of approximately 10 meters from the interaction region. This requires a 70 ps time resolution per single photon.

This paper will report on the recent development of such a TOF measurement system based on existing ASICs, both custom and commercial MCPs.

2 Background

2.1 Photon detectors

The TORCH detector will use Micro Channel Plate (MCP) as photon detectors. The final MCP device needs to provide a stable gain up to at least 5 C/cm², a physical granularity equivalent to 8×128 pixels and a 53×53 mm² active area with 60×60 mm² physical dimension, as shown in figure 2. Such a MCP is under development by Photek, U.K. [3]. The final device will use a 64×64 -channel physical layout. The channels are grouped together by 8 along the coarse direction, while

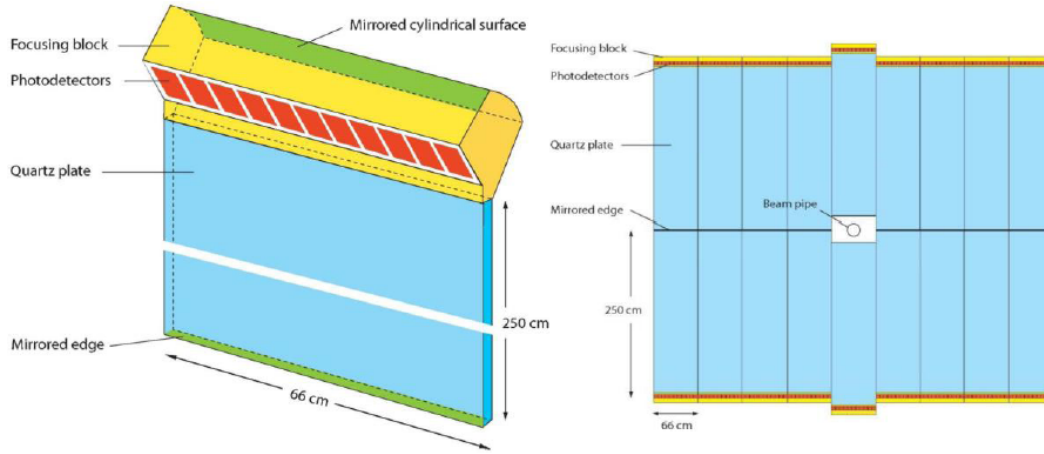


Figure 1. TORCH detector (left), segmented quartz plate (right).

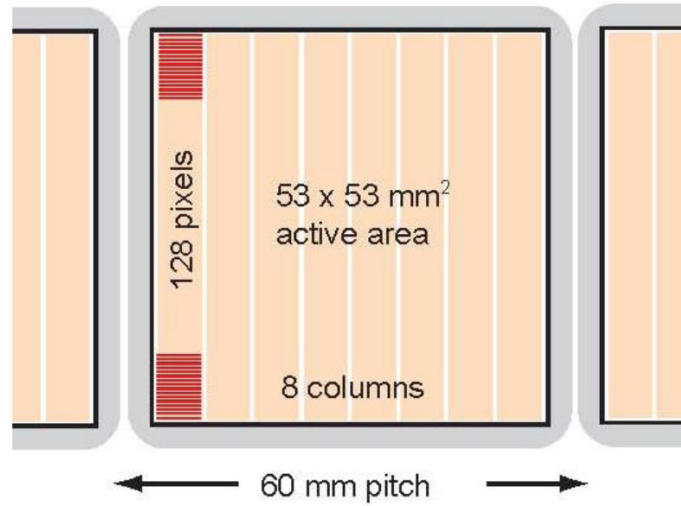


Figure 2. Proposed final MCP layout.

charge sharing technique between two adjacent channels will be applied along the fine direction, in order to achieve the 8×128 -channel equivalence. The current prototype is a quarter size model with 32×32 -channels. This gives a layout equivalent to 4×64 channels. Commercial 32×32 -channel Planacon devices [4] from Photonis, U.S.A are also being investigated. In this case, 4 channels are grouped along the coarse direction to form an 8×32 layout. In comparison to the previous 8×8 -channel Planacon that was used [5], the new photon detectors require at least 4 times higher channel density in electronics and more bandwidth in readout.

2.2 Previous electronics

In the past, a Time-Of-Flight system based on an 8×8 channel Planacon was developed for the proof of the TORCH concept [6]. The system used 8-channel NINO and HPTDC ASICs. It has provided an intrinsic time resolution of 26 ps with electrical test pulse [6]. With the above MCP, a 77 ps time resolution was measured, when tested with a pulsed laser system [7]. The readout

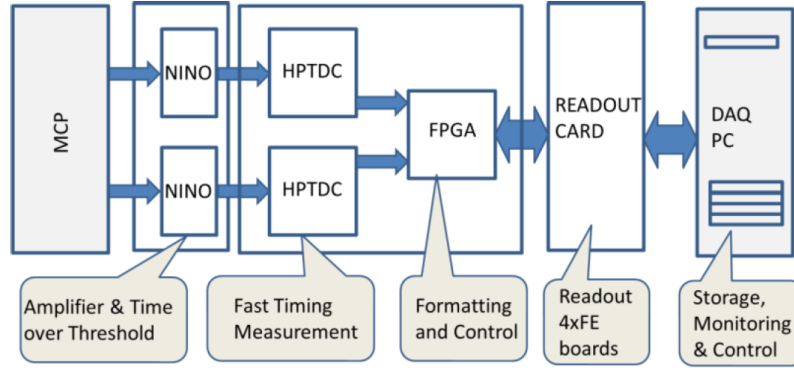


Figure 3. Main data flow.

system was based on a Xilinx SP605 development board connected to the front end boards via an adaptor PCB. It provided 64-channel TOF measurements for a single MCP tube. However, due to the requirement of higher channel count and density of new MCPs, a new system is being developed as described in the following sections.

3 Electronics development

3.1 System overview

Figure 3 shows the main data flow in the developed system. Firstly, the 32-channel NINO chips amplify the signals from the MCP and measure the Time-Over-Threshold (TOT) according to a user-defined threshold [8]. Its outputs are LVDS pulses whose width is proportional to the time over threshold. The HPTDCs are used in High Resolution Mode, which offers a maximum 34 ps (RMS) resolution [9] (with calibrations in place). In this mode, a HPTDC can still provide 32-channels. HPTDCs digitise the arrival time of the rising and trailing edge of the output pulses from the corresponding NINO. The HPTDC data are buffered in the on-board FPGA and are subsequently transmitted to the readout board and sent to a DAQ PC.

The system is a modular and scalable design, up to 8 NINO/HPTDC boards can be used for a single MCP within the $60 \times 60 \text{ mm}^2$ envelope. Using 64-channel NINO and HPTDC boards, the system can have 8×64 -channels in order to fulfil the final requirement. The electronics does not protrude sideways as shown on figure 4. Hence, MCPs can also be placed next to each other without increasing the dead area between two MCPs. The modular design also gives flexibility to instrument different photon detectors throughout the development stages. Separating the readout board allows using a readout framework of an experiment, for example LHCb, in a later stage of the project.

3.2 Analogue front end – NINO board

As shown in figure 5, a NINO board is equipped with two 32-channel IRPICS2 (NINO) ASICs [8], which are wire-bonded to the PCB. The NINO chips perform TOT measurements according to a threshold value that can be set by an on-board DAC. Alternatively, this threshold can be set by potentiometers for quick adjustment. The NINO also has an output pulse stretcher that can be set

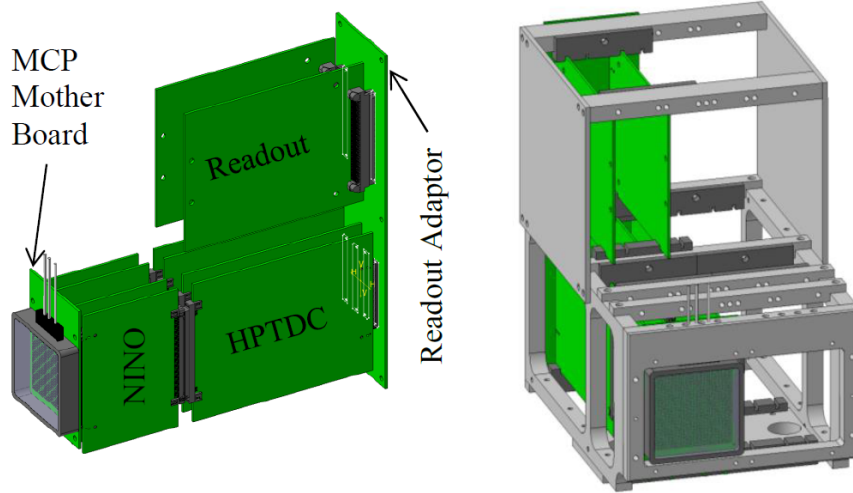


Figure 4. (a) 3-D model of the system. A MCP is connected to 4 NINO boards followed by 4 HPTDC boards. Two readout boards are used via an adaptor board. (b) The MCP and PCBs are supported by aluminum frames and comb structures.

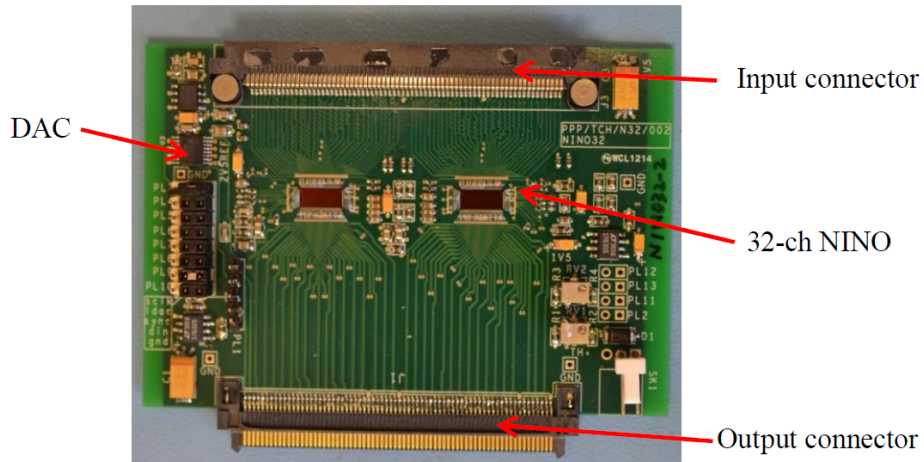


Figure 5. NINO board.

to suit the HPTDCs' input requirements. The SPI-DAC can be programmed either by on-board headers for standalone testing or via the edge connector at the bottom of the board. When mated with the HPTDC board, the FPGA on HPTDC board can control the threshold.

The NINO board was tested with an electrical pulse coupled through a 10 pF capacitor. The pulse is split in two channels on the NINO board, one with added cable delay as shown in figure 6. The distribution of the time difference measured between the output of these two channels is shown in figure 6. It can be seen from the histogram the sigma of the Gaussian fit is 38 ps. Since the two signals are uncorrelated, the timing resolution is $38/\sqrt{2} = 26.8$ ps.

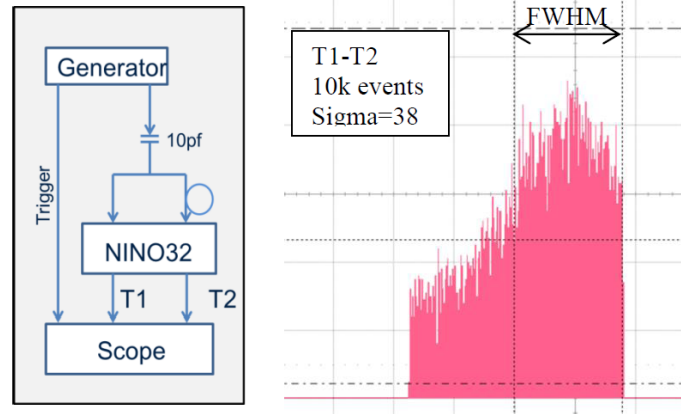


Figure 6. NINO Test setup (left) and results (right).

3.3 Time to digital conversion

As shown in figure 7, the HPTDC board consists of two HPTDC ASICs that provide 64-channel fast timing measurements for up to 34 ps RMS resolution [9]. The inputs are 64 LVDS pairs on the connector on the top side as shown. These signals are split in the two HPTDC chips, where the digitization is taking place. Subsequently, a Xilinx Spartan 3AN FPGA [10] reads and buffers the output from the HPTDCs. The FPGA also provides the following functions: command decoding (control and configuration), HPTDC configuration, data formatting and NINO threshold control.

The control commands are transmitted from the readout board and decoded on this FPGA. The configuration register for the HPTDCs can be loaded through the readout board and programmed in to the corresponding HPTDC via a JTAG interface. The HPTDC start up sequence will also be performed automatically by the FPGA each time a new configuration is loaded. The NINO threshold can also be loaded through the readout board, and then decoded in the FPGA. The FPGA will program the DAC on the NINO board using a SPI interface.

Once the HPTDC operation is started, data are read out by the FPGA and temporarily buffered locally. In some cases, the data are formatted to be compatible with other components in the experiment, for example to work with a telescope in a test beam.

3.4 Readout and control board

A compact readout and control board is designed to replace the SP605 development board in the old system. As shown in figure 8, the readout board consists of a Xilinx Spartan 6 LX45T FPGA [11], a Gigabit Ethernet PHY chip, a 1 G-bit DDR3 RAM and low-jitter clock fan out ASICs. It uses a single 5 V power supply, and all required voltages are regulated locally. The I/O connector shown on the top of the board provides the following LVDS signals: 4 fan-out clocks, 4 fan-out triggers and 52 I/O pairs for data and control. It also provides 2.5 V and 3.3 V at maximum 2.5 A. The fan-out clock and trigger are received from the HDMI connector shown on the bottom side of the board. The connector is pin compatible with the AIDA Trigger logic Unit [12], which is used in a number of experiments and telescopes, including the Timepix 3 telescope [12]. This allows the use of the telescope data in test beams. The readout board is designed to drive up to 4 HPTDC boards

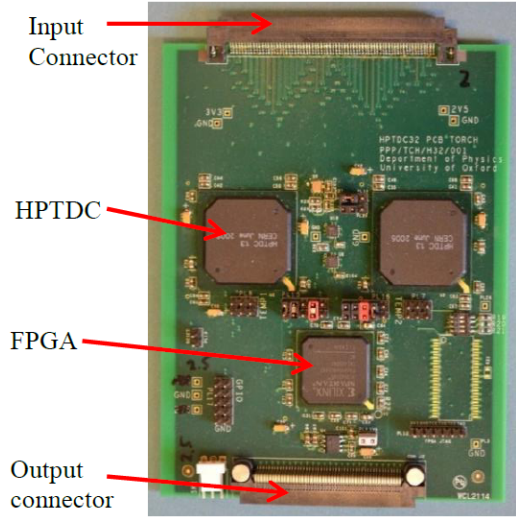


Figure 7. HPTDC board.

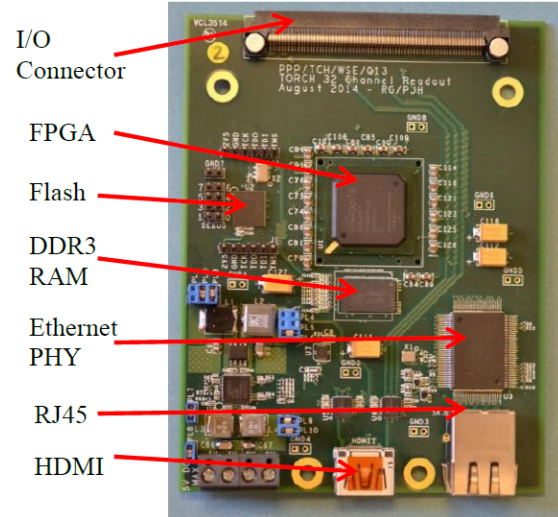


Figure 8. Readout board.

without additional clock fan-out. Gigabit Ethernet is used to communicate with a PC in both ways. Raw Ethernet protocol is implemented to achieve the best efficiency. Up to 800 Mbps downstream are recorded in our tests.

In order to read out data from a number of HPTDC boards, a block-based readout scheme is used. In normal operation, the HPTDC data are held in FIFOs in the FPGA on a HPTDC board until they are read out by the readout board. The readout board reads a fixed number of bytes from one HPTDC board, and then switches to the next one. If the HPTDC board being read out has no data, zero padding will be used.

3.5 Mother boards for different MCPs

An MCP mother board provides contact pads on one side to connect to an MCP and on the other side connectors for the NINO boards. In this way, we only need to design different mother boards for different MCPs through the development stages. Two examples are shown in figure 9. On the left it shows a mother board designed by Photek for their prototypes. The picture on the right is a mother board designed for 32×32 Planacons. The Photek MCP uses Anisotropic Conductive Film (ACF) [13] together with a mechanism that applies pressure on the mother board to achieve the connection. The Planacon is connected to the mother board by conductive glue.

3.6 Readout adaptor board

The readout adaptor board simply routes the output of the HPTDC board to readout boards. The connector layout is compatible with both Photek and Planacon mother boards. It uses length matched tracks for fanning out clock and trigger signals to the HPTDC board. Finally, power regulators are added to the adaptor board to supply 2.5 V and 3.3 V for HPTDC and NINO boards. It provides up to 9 A for both voltages.

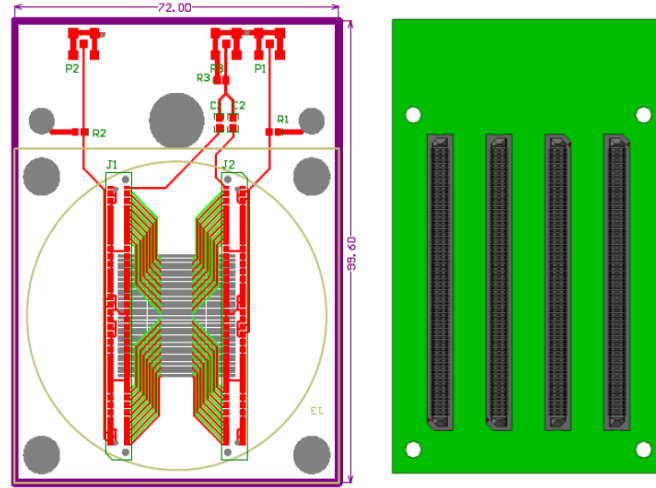


Figure 9. MCP mother boards Photek (left) Planacon (right).

4 Conclusion and future work

A beam test is planned at CERN in near future. Both Photek prototype MCP and the commercial Planacon MCP will be used. The TORCH prototype will include a radiator plate, sized $1 \times 12 \times 35 \text{ cm}^3$, and a focusing prism. MCPs will be instrumented with 4 NINO boards and 4 HPTDC boards, providing a total of 256 channels. The readout of an 8×64 -channel MCP is in preparation. This final MCP is expected to be delivered in two years' time.

Acknowledgments

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