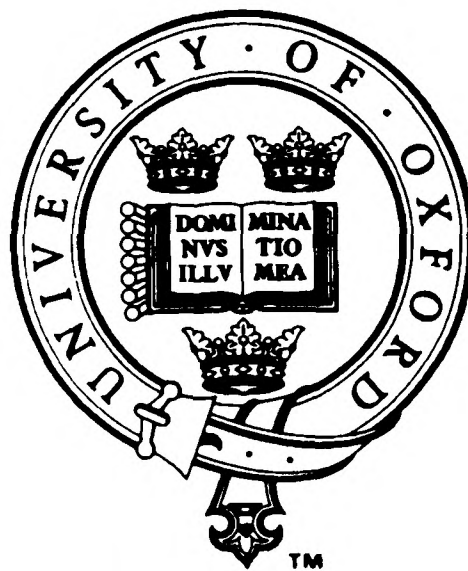


Floating-Gate Based Trimmable Current Sources

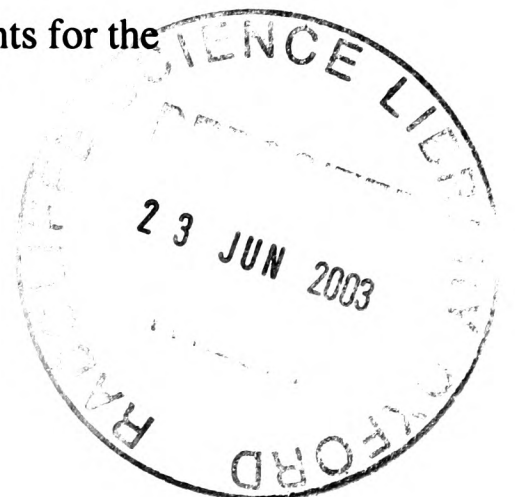
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Floating-Gate Based Trimmable Current Sources

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One of the most crucial building blocks of an electronic system is the digital-to-analogue converter (DAC) which forms the interface between the digital and analogue component parts. In order to achieve the high performance required by many systems, particularly communications systems, the DAC requires careful, time consuming and expensive design and layout which increases the cost of the entire system.

This design process is required to minimise the mismatches between the current sources in the current steering DAC. Trimmable current sources, based on floating-gate devices, are therefore proposed in order to simplify the design of a DAC. A floating-gate device is a form of an analogue non-volatile memory which can be programmed to control the threshold voltage of a MOSFET.

Four different current sources are designed to use a floating-gate device in three distinct ways: as a trimmable current source, as a trimmable voltage source and as a trimmable resistor. All the current sources have a sufficient trimming range to correct for any process and parameter variations. However, a major concern about floating-gate devices is their ability to retain a programmed voltage. It is shown that these current sources can be biased so that they retain a programmed floating-gate voltage over several days of normal operation. Even with this characteristic, a variation in the operating temperature of the current sources will cause a significant variation in the output current. Therefore, the temperature characteristics of the current sources are investigated to determine the impact of temperature variations. A distinct biasing condition is identified in all the current sources which causes the output current to be insensitive to temperature variations. Furthermore, one design is identified which is temperature insensitive over a significant trimming range.

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Chapter 1

Introduction

The recent technological revolution has been driven by the demand for cheaper, smaller and faster products. The cost and size of these products can be reduced by integrating entire systems on a single chip (SoC). Since the major part of any system is digital, the technology usually chosen for SoC integration is CMOS. This integration requires the design of both digital and analogue parts on a single substrate, which has proven difficult. Problems of integration are compounded by the growing demand for wireless products, which require the integration of RF systems. Wireless communications systems typically consist of a digital signal processor, which performs the computation, an analogue transceiver with an interface between these two, consisting of an analogue-to-digital (ADC) and a digital-to-analogue converter (DAC).

The DAC is one of the most crucial building blocks in this system. It is increasingly required by each new generation of communications standards to operate at faster conversion rates and higher data resolutions. For example, the recent Bluetooth standard requires a rate of conversion of up to 200MS/s with data resolutions of 10-14 bits. To achieve this level of high performance, CMOS current steering DACs have been favoured because of their good high speed performance. However, to achieve the required resolution, careful design and layout is required to eliminate the problem of mismatches between the current sources. This increases the cost of the system, both in terms of the design time and silicon area. Therefore, there is need for an alternative strategy to meet the strict design criteria of the DACs.

In this thesis, the use of floating-gate technology, implemented in a standard $0.35\mu m$ double poly CMOS process, to design novel trimmable current sources is explored. These current sources, which can be trimmed to minimise the mismatches, will simplify the design of current steering DACs considerably.

1.1 Current Steering DACs

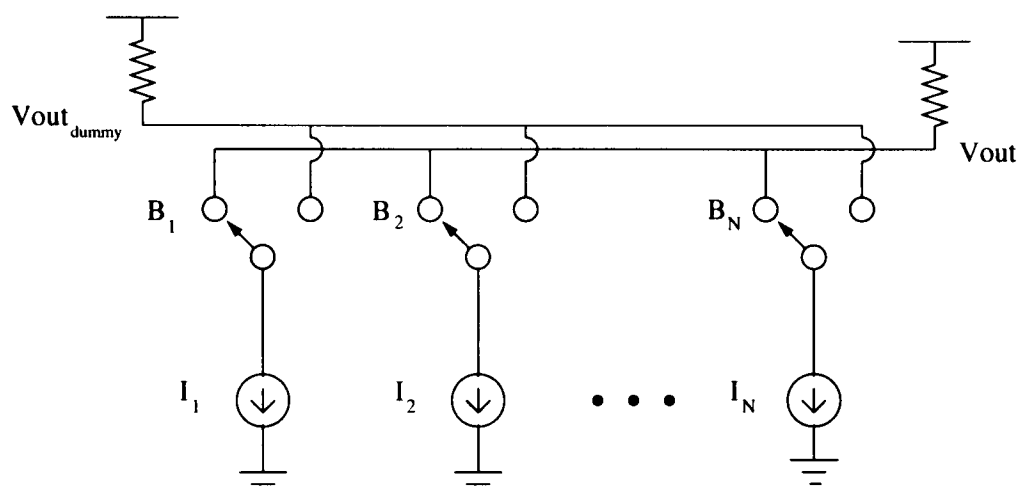


Figure 1.1: *Conventional Current Steering DAC Architecture*

Current steering DACs consist of a bank of current sources with switches controlled by the digital input as shown in Figure 1.1. The simplest architecture consists of binary weighted current sources which can be switched directly by the binary input [1,2]. The number of current sources is therefore the same as the number of input bits. However, there are two disadvantages associated with this simple architecture. The first is that it requires accurate matching between different sized current sources. In effect the most significant bit current source must be accurate to within 0.5 LSB (least significant bit). This is difficult to achieve for a resolution of greater than 8-bits. The second problem with this architecture is that during any transition, several current sources which are expected to switch simultaneously, sometimes do not. This can cause transient errors, glitches, which can introduce non-linear signal components [3]. For example, during the mid-code transition, (for example $0111 \Rightarrow 1000$ in a 4-bit system), the largest glitch is caused if the current sources switch such that an intermediate state of 1111 arises.

An alternative to the binary weighted current source architecture is the unary weighted (or

thermometer coded) architecture [4]. In this architecture, an N-bit system will contain 2^N current sources. The switch of each current source is controlled by one output from a binary-thermometer decoder which is designed to convert the binary input code into a thermometer code. This architecture minimises the number of transitions and at any one time, the transitions are all either rising or falling, thereby reducing the transient glitches significantly. One of the disadvantages of the thermometer coded DAC is that the complexity of the design increases rapidly with each extra bit. This not only increases the size of the design but also results in more cross-talk and substrate noise.

The problems with thermometer coded DACs mean that a compromise between the two architectures is often used. In a segmented architecture, binary weighted current sources are used for the LSBs and unary weighted current sources for the MSBs. This architecture therefore combines the advantages of both binary and unary weighted architectures to obtain a small area together with low glitch noise [3, 5–9].

The main static performance limitation of both DAC architectures is the mismatch between the current sources which introduces errors in the output current [10, 11]. These mismatches are caused by the variations in the threshold voltage, V_{th} , and the transconductance parameter, β , between each transistor and the nominal parameter values. These parameter variations arise from a combination of the inherent stochastic variations of the parameters, which are technology dependent, and the variations due to process, mechanical strain and temperature gradients, all of which can have a significant effect on the mismatch in large arrays [12, 13]. A critical aspect of the design of any DAC is to determine the amount of mismatch that can be tolerated and then ensure that this level is never exceeded.

1.1.1 Matching Requirements

The random variations of V_{th} and β in a MOSFET that degrade the performance of a DAC, have been investigated by Pelgrom et al. [12]. This group found that these variations are related to

the device size, in particular

$$\frac{\sigma_{\beta}^2}{\beta^2} = \frac{A_{\beta}^2}{WL} \quad (1.1)$$

$$\sigma_{vt}^2 = \frac{A_{vt}^2}{WL} \quad (1.2)$$

where σ_{β} and σ_{vt} both represent the standard deviations of β and V_{th} , A_{β} and A_{vt} are process related constants and W and L are the device dimensions. It can be seen from these definitions that the standard deviations of β and V_{th} are inversely proportional to the MOSFET area. Therefore, a model is needed to determine the size of a device required to achieve specific matching conditions.

For a MOSFET operating in the saturation region with a constant gate-source voltage, V_{gs} , the output current is

$$I = \frac{\beta}{2}(V_{gs} - V_{th})^2 \quad (1.3)$$

Assuming that the two types of parameter variations are independent, then the variance of the output current is given by [14]

$$\sigma_I^2 = \left(\frac{\partial I}{\partial \beta} \sigma_{\beta} \right)^2 + \left(\frac{\partial I}{\partial V_{th}} \sigma_{vt} \right)^2 \quad (1.4)$$

where

$$\frac{\partial I}{\partial \beta} = \frac{1}{2}(V_{gs} - V_{th})^2 \quad (1.5)$$

$$\frac{\partial I}{\partial V_{th}} = -\beta(V_{gs} - V_{th}) \quad (1.6)$$

The normalised current standard deviation is therefore given by [14]

$$\frac{\sigma_I^2}{I^2} = \frac{\sigma_{\beta}^2}{\beta^2} + \frac{4\sigma_{vt}^2}{(V_{gs} - V_{th})^2} \quad (1.7)$$

Using Equations 1.1 and 1.2, the current mismatch is then given by [15]

$$\left(\frac{\sigma_I}{I}\right)^2 = \frac{\left[A_\beta^2 + \frac{4A_{vt}^2}{(V_{gs}-V_{th})^2}\right]}{WL} \quad (1.8)$$

It can be seen from this equation that there are two contributions to the overall current mismatch. Both terms reduce with increasing device area but only one term depends upon the gate voltage. Therefore, specific matching requirements can be met by a combination of selecting the device size and gate overdrive voltage, $(V_{gs} - V_{th})$. A convenient compromise is to make the two mismatch contributing terms equal. For a $0.35\mu\text{m}$ technology with $V_{th} = 0.5\text{V}$, $A_\beta = 1.1\%\mu\text{m}$ and $A_{vt} = 9.6\text{mV}\mu\text{m}$, this gives a gate bias, V_{gs} , of 2.3V for a NMOS transistor.

Figure 1.2(a) shows the mismatch as a function of the gate overdrive voltage for different transistor sizes. It can be seen that as $V_{gs} - V_{th}$ decreases, the mismatch deteriorates for a given transistor area. However, an improvement is obtained with increasing transistor size. Figure 1.2(b) shows the variation of the transistor area with the gate overdrive voltage for 0.3% mismatch (which is sufficient to achieve 99% yield for 12-bit matching accuracy [15]). This figure demonstrates the need to increase the transistor area at lower overdrive voltages in order to meet the matching requirements. For a target mismatch of 0.3% at the optimum bias voltage, the minimum transistor size is $26.1\mu\text{m}^2$. For lower mismatch requirements, the minimum transistor size becomes unacceptably large. For example for 0.2% mismatch, $(WL) = 58.7\mu\text{m}^2$ and for 0.1% mismatch, $(WL) = 235\mu\text{m}^2$.

Large transistors are required to achieve tolerable mismatch even with large gate overdrive voltages. However, to operate a current source transistor in the saturation region, it must be biased so that $V_{ds} > V_{gs} - V_{th}$, this is equal to 1.8V at the optimum gate bias. This MOSFET must be cascoded by a switch. In this situation, the lack of voltage headroom can limit the maximum V_{ds} to less than 1.8V . In order to increase the available voltage, the source transistor should be biased at a lower gate voltage. However, without increasing the device size, the mismatch will increase.

The results of Equation 1.8 represent the variations between neighbouring devices. They

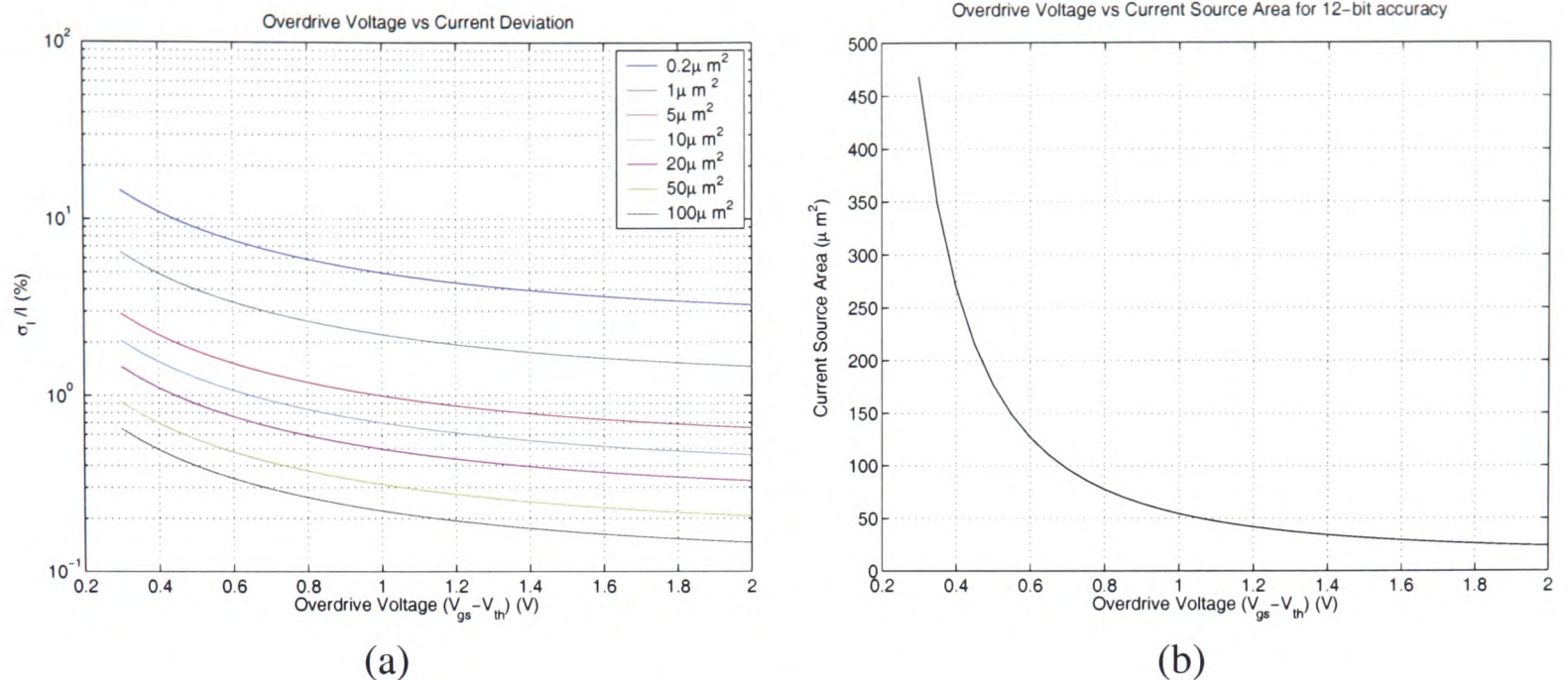


Figure 1.2: *Matching properties of a MOSFET. (a) shows the mismatch variation with gate overdrive voltage for constant transistor area. Mismatch is decreased by either increasing the overdrive voltage or the transistor area. (b) shows the variation of area with overdrive voltage for 12-bit matching.*

do not take into account the parameter gradients. These variations are caused by oxide thickness gradients, mechanical stress and temperature gradients across the die, which affect widely spaced transistors. Several layout rules have been suggested in order to minimise the effects of these gradient variations [16, 17].

- Transistors which form identical current source should have the same structure, shape, size, orientation and surroundings.
- Common-centroid layout schemes should be used to compensate for parameter gradients. However, this increases design complexity and hence design time.
- Transistors should be placed in an area of low mechanical stress gradients in the centre of the die. This may be possible in a specific DAC chip but, is very difficult in a SoC.
- Transistors should be placed well away from power sources to minimise the effect of temperature gradients. This may be difficult to achieve in a SoC.

The use of large devices and very careful centroid layout of the current sources in [9, 15, 18] increases the circuit area as well as the design time. In addition, these techniques can be very application specific. Special switching schemes have also been used to minimise the effect of

mismatch [4, 19]. These require extra decoding logic which increases the area and power consumption. Despite all of these techniques, it is still difficult to achieve high resolution by design. Therefore, calibration schemes [2, 20, 21] which can dynamically correct the mismatches at the expense of increased control circuitry and power consumption have been used. The current sources can also be laser trimmed after fabrication, however, this is expensive and not available on standard CMOS processes. All of these techniques aim to improve the matching between the current sources at the cost of increased complexity, design time and silicon area.

The ideal current source for a DAC should be easily trimmed to overcome the device mismatches and be robust to temperature changes. The novel approach taken in this thesis is to design these circuits has been to employ floating-gate devices to create programmable current sources, voltage sources and resistors¹.

1.2 Review of Applications of Floating-Gate Devices

In the past thirty years, floating-gate devices have been mainly used as digital non-volatile memories. The foundation for the development of these devices was the work done by Kahng and Sze [23] and Lenzlinger and Snow [24]. This led to the first commercial digital memory product in 1971, that used a Floating-Gate Avalanche-injection MOS (FAMOS) which later became known as an EPROM [25, 26], and is a structure still used today in digital memory devices.

Following the development of digital memory devices, the early nineties saw growing research into using floating-gate devices as analog storage elements, primarily in silicon neural network architectures. This led to the first commercial neural network chip [27]. However, the rapid growth in digital computation throughout the 1990's made the hardware implementation of neural networks uncompetitive.

Commercial use of floating-gate devices for analogue applications is still limited to applications which do not require high accuracy such as analogue voice storage [28]. One such product, manufactured by Information Storage Devices (ISD) uses EEPROM technology for

¹Work by Diorio et al. has also concluded independently that floating-gate devices could be used in DACs to trim the current sources [22].

non-volatile analogue storage. Another chip consisting of a few individual floating-gate devices is available for use as an analogue voltage source [29], however, this design cannot be used as a generic module that can be inserted into an integrated circuit.

Commercially successful applications of floating-gate devices have been those that use specialised EEPROM technology to implement the floating-gate devices. However, it is expensive to integrate this technology into a standard CMOS process which is the most widely used technology for large scale integration. Research in analogue applications of floating-gate devices, has shown that floating-gate devices can be implemented in a standard CMOS technology. Examples of applications which use these devices range from low-power, low-voltage digital computation circuits [30–34] to low power analogue circuits such as analogue multipliers [35], amplifiers [36–39] and filters [40, 41]. Floating-gate devices have also been used as analogue weight storage elements in silicon learning systems [42–47]. Work reported by Diorio et al. has shown some promise in the use of floating-gate devices in a large analogue memory array in a single chip similar to the equivalent use of EEPROM technology for digital memory [48–52].

1.3 Floating-Gate Devices in Standard CMOS Technology

A floating-gate device implemented in a standard double poly CMOS technology consists of a MOSFET (which can be either N or P-type) whose gate is electrically isolated by silicon dioxide (SiO_2) surrounding the floating-gate. As in a standard MOSFET, the floating-gate is formed from the first polysilicon layer (poly1). This is coupled to a second polysilicon layer (poly2), known as the control gate, by a capacitance, C_{fg} , formed by the two polysilicon layers together with the intermediate SiO_2 layer. This control-gate, which has an input voltage, V_{cg} , applied to it, is used to achieve control over floating-gate voltage. Figure 1.3(a) shows the symbol and capacitive equivalent circuit of the floating-gate device and Figures 1.3(b) and (c) show a typical layout and fabrication layers of the device implemented in a standard double poly digital CMOS process.

Floating-gate devices can be implemented in CMOS technologies which do not offer a sec-

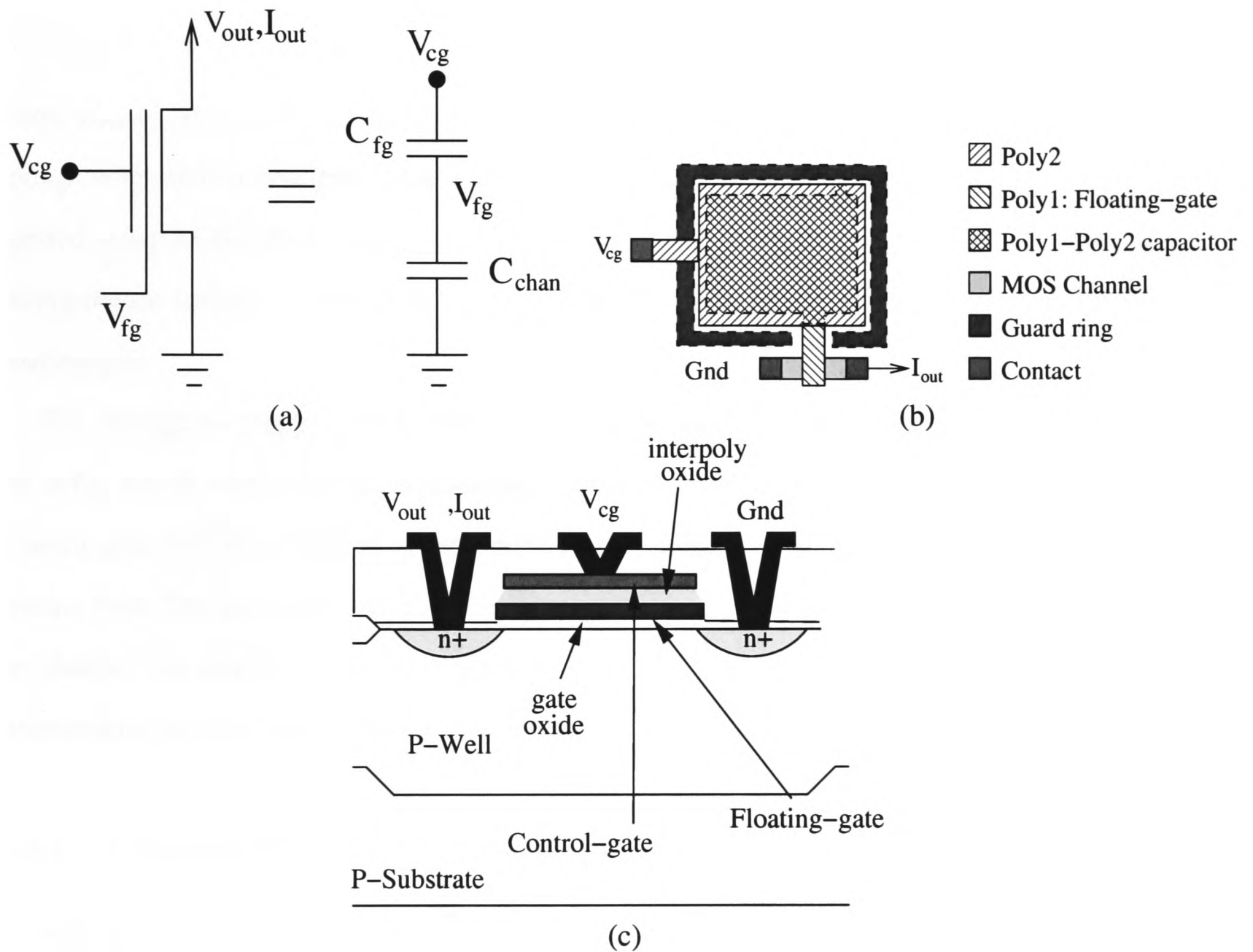


Figure 1.3: *Floating-Gate MOSFET. (a) shows the symbolic view of the MOSFET together with the equivalent capacitor circuit of the MOSFET. (b) and (c) show a typical layout and fabrication layers of the device respectively.*

ond polysilicon layer [53, 54], however, a large well structure has to be used as a control node, which increases the silicon area.

From the equivalent capacitor circuit it can be seen that the floating-gate voltage, V_{fg} , is dependent upon the control-gate voltage, V_{cg} .

$$V_{fg} = \frac{C_{fg}}{C_{tot}} V_{cg} + V_{fg|V_{cg}=0} \quad (1.9)$$

where C_{tot} is the total capacitance seen by the floating-gate and $V_{fg|V_{cg}=0}$ is the floating-gate voltage when the control-gate voltage is zero. V_{fg} can therefore be varied using V_{cg} which is applied using an external voltage source. This is a quick and convenient way of varying V_{fg} during device testing. Alternatively, $V_{fg|V_{cg}=0}$ can be controlled by varying the charge on the floating-gate.

The storage of charge on the floating-gate relies upon the good insulating properties of the SiO_2 which surrounds the floating-gate. Hence, in order to force charge on or off the floating-gate, the SiO_2 must be subject to extreme conditions such as UV radiation or a high electric field. The particular techniques that have been used to create trimmable current sources are channel hot electron injection (CHEI) or Fowler-Nordheim Tunneling (FNT). These two mechanisms are described in the following sections.

1.3.1 Channel Hot Carrier Injection

In short channel devices, large lateral fields occur at the drain end of the channel. If this field is sufficiently high, then the electrons in NMOS (holes in PMOS) can gain more energy than that expected in equilibrium. Research into the effects of these high energy carriers has concentrated on the degradation they cause in normal MOS transistors when they enter the gate oxide [55–73]. To enter the oxide, the carriers must surmount the energy barrier which occurs at the $Si - SiO_2$ interface, which is approximately 3.2eV for electrons and 4.8eV for holes [74, 75]. Therefore, hot carrier degradation effects are expected to occur when a sufficiently large electric field is applied to provide the carriers with enough energy to cross the barrier. These hot carriers

are then injected into the oxide, some becoming trapped in the oxide and whilst others traverse the oxide and form an unexpected gate current. It is the trapped carriers, both hot holes and electrons, which degrade the performance of the device by introducing a shift in the threshold voltage and the transconductance parameter, β . The charge trapping occurs in localised energy levels at the $Si - SiO_2$ interface [63] and in defects within the oxide itself. These traps affect the number of carriers which are able to traverse through the oxide to form the gate current. Holes are 3-4 orders of magnitude more effective at producing interface states than electrons and their trapping rate is about 5 orders of magnitude higher than those of electrons [67]. In a floating-gate device, the gate current due to the hot carriers flows on to the floating-gate. This mechanism can therefore be used to program a floating-gate device.

In an NMOS transistor, both types of carriers, holes and electrons, are able to become “hot” [74, 75]. A high lateral electric field exists at the drain end when the drain voltage, V_d , is high. This allows the electrons to become hot. A high floating-gate voltage attracts these hot electrons towards the floating-gate. This phenomenon is known as channel hot electron injection (CHEI). Hence in a floating-gate device with an NMOS transistor, CHEI can be used to inject electrons into the floating-gate. The effect of this injection is to reduce the floating-gate voltage, $V_{fg|V_{cg}=0}$, in Equation 1.9.

If on the other hand, the initial condition of the floating-gate is such that $V_{fg} \ll V_d$, then the injection of hot holes is observed (CHHI). These hot holes are created through impact ionisation of electrons as they accelerate towards the drain. Under this biasing condition, it is the holes that are attracted to the gate. However, the magnitude of the hot hole current is significantly smaller than that due to electron injection because of the higher energy required by the holes to cross energy barrier at the $Si - SiO_2$ interface.

In PMOS devices, at low-gate voltages, hot-hole injection is observed and at high-gate voltages, it is the hot electrons that are injected. These electrons are generated by the impact ionisation of holes. CHEI in PMOS devices has been reported by Diorio et al. [42] and used for the dynamic programming of the weights of a silicon synapse. These floating-gate devices are designed to operate in the subthreshold region. However, one of the problems with using

PMOS devices for programming is that the injection current is lower than in NMOS devices. More importantly, CHEI in PMOS devices suffers from positive feedback. For example, when CHEI occurs in a PMOS device, electrons are injected on to the gate. This reduces the floating-gate voltage which in turn increases the channel current. This positive feedback means that this mechanism is unstable and requires to be treated carefully. Floating-gate devices implemented by Diorio et al. therefore use a special cascode device to stabilise the injection process [44].

One of the advantages of using NMOS devices for programming with CHEI is that the programming mechanism is self-limiting. The effect of CHEI injection is to reduce the floating-gate voltage, V_{fg} , as given by Equation 1.9. In an NMOS device, a reduction in the floating-gate voltage, reduces the channel current which reduces the electron injection. This injection process in NMOS transistors is thus self-limiting and therefore stable.

It is therefore expected that CHEI can be used in NMOS devices to add electrons on to the floating-gate. CHHI could be used to add holes, but this damages the oxide more than CHEI does. An alternative mechanism that can be used to increase the floating-gate voltage is Fowler-Nordheim tunneling (FNT).

1.3.2 Fowler-Nordheim Tunneling

Fowler-Nordheim tunneling (FNT) is a mechanism by which electrons tunnel through an energy barrier in the presence of a high electric field [76]. The tunneling of electrons through Si to SiO_2 was first shown by Lenzlinger and Snow [24]. The energy band diagram showing the floating-gate, the surrounding SiO_2 and a polysilicon tunneling node is shown in Figure 1.4. Under normal bias conditions, the electrons on the floating-gate are isolated by an energy barrier of 3.2eV whose thickness is the thickness of the SiO_2 layer. When the bias voltage of the tunneling node is increased, the thickness of the SiO_2 barrier as seen from the floating-gate decreases. With the barrier sufficiently reduced, the electrons are able to tunnel through the SiO_2 . The tunneling current density is therefore a function of the electric field, ε , across the

oxide and is given by [77]

$$J = C_1 \varepsilon^2 e^{-\frac{\varepsilon_0}{\varepsilon}} \quad (1.10)$$

where C_1 and ε_0 are material constants.

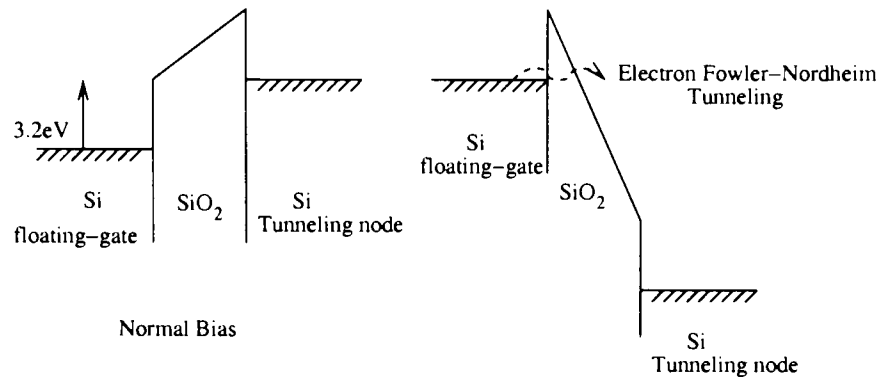


Figure 1.4: *Energy band diagram showing the Fowler-Nordheim tunneling mechanism.*

Digital memory devices which use this mechanism to program require the use of ultra-thin floating-gate oxides or a textured-surface polysilicon to enhance programming rates [27, 78–80]. However, both of these techniques require a special process which is expensive to integrate into a standard CMOS process.

The first floating-gate device to use a tunneling structure designed on a standard CMOS process was reported by Carley [81]. The tunneling node consisted of a p-well in a n-type substrate. When a high voltage is applied to the p-well, tunneling occurred at the edge of the floating-gate polysilicon which overlapped the p-well. This structure however, resulted in very different charging and discharging rates. A similar structure has also been used recently by Diorio et al. [42] to remove electrons from a floating-gate. An alternative structure proposed by Thomsen and Brooke uses a second polysilicon layer which overlaps the floating-gate polysilicon in a small area to form the tunneling node [82]. Electron injection in poly-oxide layers has been found to occur in small areas around the tunneling node which causes large variations in the injection current [83]. However, this structure is smaller than the well structure used by Carley and Diorio et al.

FNT can be used to remove electrons from the floating-gate by applying a positive voltage

on the tunneling node. This mechanism thus complements CHEI which is used to add electrons on to the floating-gate. The floating-gate voltage can therefore be decreased using CHEI and increased using FNT.

1.4 Thesis Statement

This thesis sets out to examine the hypothesis that floating-gate devices can be used to create current sources for use in high precision current steering DACs which are both trimmable as well as temperature insensitive. It examines their retention properties.

1.5 Thesis Overview

Chapter 2 describes a floating-gate device designed in a $0.35\mu\text{m}$ double poly CMOS process. This device can be programmed using both CHEI and FNT. However, these mechanisms vary from process to process and therefore, both need to be characterised for this process. Another aspect of these devices is their ability to retain charge once they have been programmed to a specific voltage. This is not only important during the storage of the device but also during normal operation. The operating conditions required to achieve this are investigated in this chapter.

Chapter 3 describes four different trimmable current sources which employ floating-gate devices in three different forms. The first current source uses the floating-gate as a programmable current source. In the next two current sources, the trimming is achieved by using a floating-gate device as a programmable voltage source to bias a MOSFET and in the final current source, the floating-gate device is used as a trimmable resistor which is used to modulate the output current. It is expected that these current sources will be trimmed after fabrication. It will be shown that small variations in the operating temperature can cause a larger change in the output current than the change caused by charge loss from the floating-gate. Therefore, the effect of temperature on each of the current sources is investigated in Chapter 4. A particular operating point

is identified at which the output currents are insensitive to variations in temperature. It will be shown that when biased around this operating point, the current source that uses a floating-gate device as a programmable resistor, gives an output current that is both temperature insensitive and trimmable over a significant range.

Chapter 5 presents the conclusions and future work.

Chapter 2

Floating-Gate Technology

2.1 Introduction

Floating-gate devices are required to trim current sources suitable for high speed current steering DACs in RF systems. It is therefore essential to implement these devices in a technology that is able to support operation at hundreds of MHz. Floating-gate devices also require a double poly process together with support for high voltage devices that are required for both CHEI and FNT programming. The AMS $0.35\mu m$ double poly CMOS process was thus identified as a suitable technology to implement floating-gate devices.

In this chapter, a floating-gate device implemented in this technology is presented. This floating-gate device can be programmed using both CHEI and FNT. The characteristics of these programming mechanisms are explored to determine the current injection rates. It will be shown that both mechanisms can be modelled empirically. If the floating-gate device is to be used as a trimmable current source, then the long term charge retention characteristics, both during operation and in storage, are crucial in determining the viability of this technology.

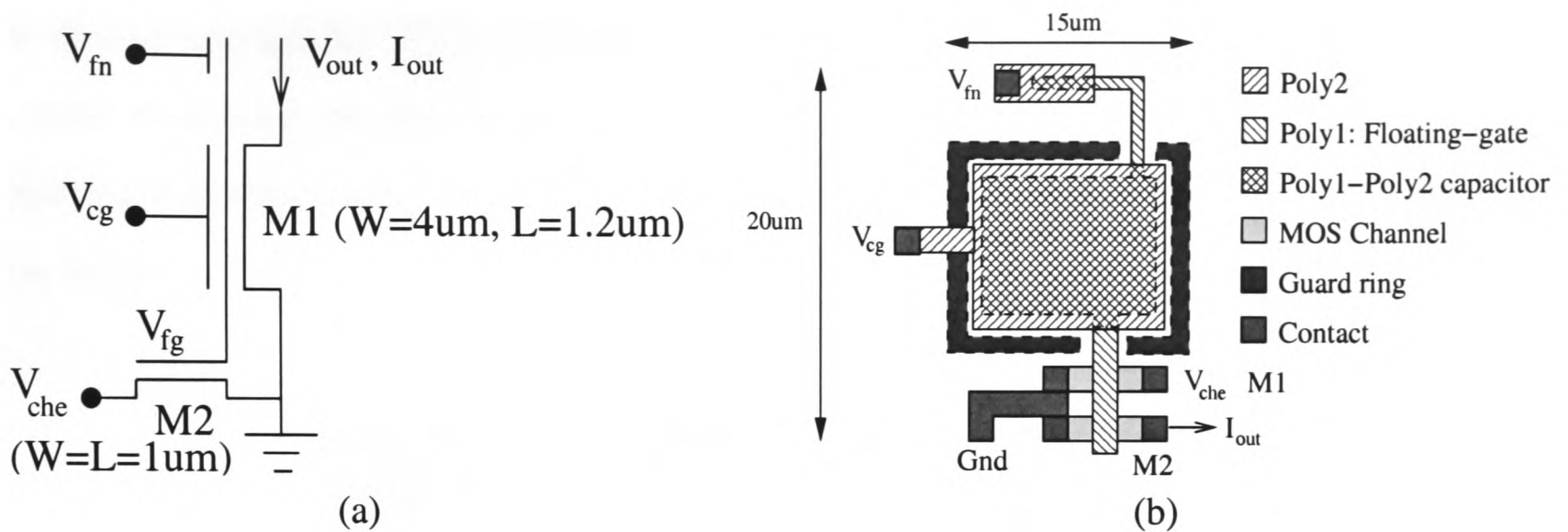


Figure 2.1: *Floating-Gate MOSFET. (a) shows the symbolic view of the designed device. (b) shows the layout of the device. A grounded metal shield which covers the circuit is not shown.*

2.2 Floating-Gate MOSFET

The designed floating-gate device, shown in Figure 2.1(a), consists of two n-MOSFETs, M1 and M2, the floating-gate capacitor and the Fowler-Nordheim tunneling node. M1 is the sense transistor which is used to read the stored floating-gate voltage. The programming of the floating-gate is done through M2 which is used for CHEI programming whilst FNT occurs at the tunneling node which has a voltage V_{fn} applied to it.

As shown in the layout of the device in Figure 2.1(b), the floating-gate, poly1, is enclosed within poly2 to protect it from any noise. Furthermore, the substrate under the floating-gate is surrounded by a guard ring to reduce fluctuations due to variations in the substrate potential. The figure also shows that the dominant structure in this device is the floating-gate capacitor. The floating-gate capacitor can be made smaller, however, since no characterisation data exists for such devices fabricated on this $0.35\mu m$ technology, the floating-gate has been designed to be large to reduce the impact of capacitor mismatch and more importantly charge leakage. The result is a total area of $300\mu m^2$.

The floating-gate voltage of this device is decreased using CHEI. Transistor M2 is used for this purpose by applying a sufficiently high voltage, V_{che} , to the drain of the MOSFET to enable the generation of hot electrons. On the other hand, to increase the floating-gate voltage, FNT is used to remove the electrons from the floating-gate through the inter-poly oxide between

the floating-gate and the FNT poly2 node. The tunneling voltage, V_{fn} , is applied to this node in order to decrease the width of the energy barrier sufficiently to induce electron tunneling. Figures 2.2(a) and (b) show the locations of CHEI and FNT in cross-sections of the floating-gate device.

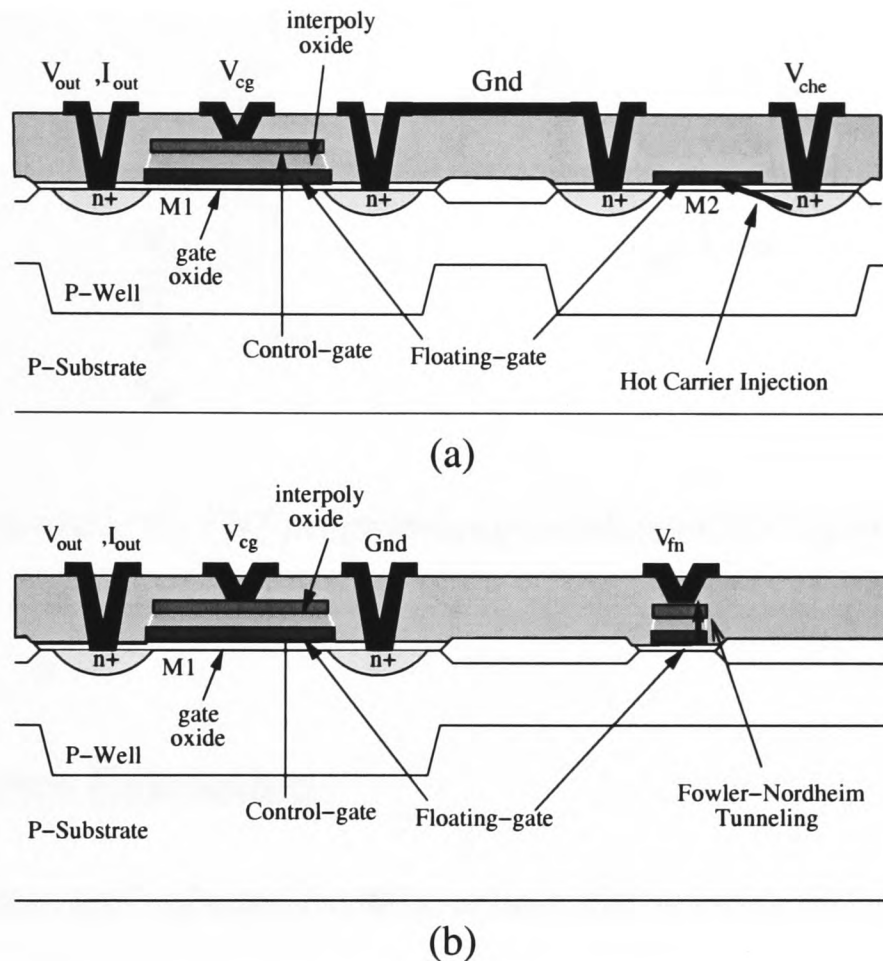


Figure 2.2: Cross-section of the floating-gate device. (a) shows the CHEI mechanism. (b) shows the FNT mechanism.

The FNT node adds to the capacitance of the floating-gate. The equivalent capacitor circuit of the device, shown in Figure 2.3, now includes this capacitance, C_{fn} . Thus the floating-gate voltage is given by

$$V_{fg} = V_{fg|V_{cg}=0} + \frac{C_{fg}V_{cg} + C_{fn}V_{fn}}{C_{tot}} \quad (2.1)$$

where $V_{fg|V_{cg}=0}$ is the floating-gate voltage when the control-gate voltage is zero, C_{fg} is the floating-gate capacitance, C_{fn} is the tunneling node capacitance and $C_{tot} = C_{fg} + C_{fn} + C_{chan}$. It is clear from the layout of the device that C_{fn} is significantly smaller than C_{fg} . However, it will still have a finite effect on V_{fg} when a high voltage is applied during FNT programming.

Removing this high voltage at the end of programming will cause a small change in V_{fg} . This disturbance will be significant when precise programming is required. To determine the extent of this disturbance, the values of various capacitors need to be determined.

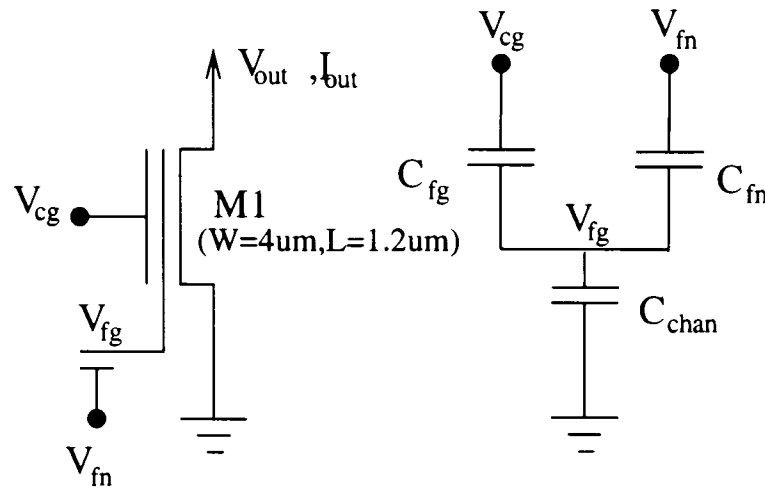


Figure 2.3: The schematic of the FNT programming circuit is shown together with the equivalent capacitor circuit.

2.2.1 Capacitance Extraction

The device capacitances are evaluated from the extracted simulation data of the floating-gate element. The extracted parameters are shown in Table 2.1. The total capacitance for the floating-gate element, C_{tot} , with a sense transistor of dimensions $W = 4\mu m$ and $L = 1.2\mu m$, is $126fF$. Therefore the capacitance ratios are $\frac{C_{fg}}{C_{tot}} = 0.79$ and $\frac{C_{fn}}{C_{tot}} = 0.0079$. This suggests that less than 1% of V_{fn} will be coupled on to the floating-gate. Thus for example, when a 15V programming voltage is applied to the tunneling node, the disturbance on the floating-gate will be approximately 150mV. This level of disturbance is not acceptable for accurate programming.

C_{fg}	$101.1fF$
C_{fn}	$0.939fF$
C_{chan}	$5fF/\mu m^2$
C_{tot}	$102fF + 5fF/\mu m^2$

Table 2.1: Extracted Programming Cell Parameters

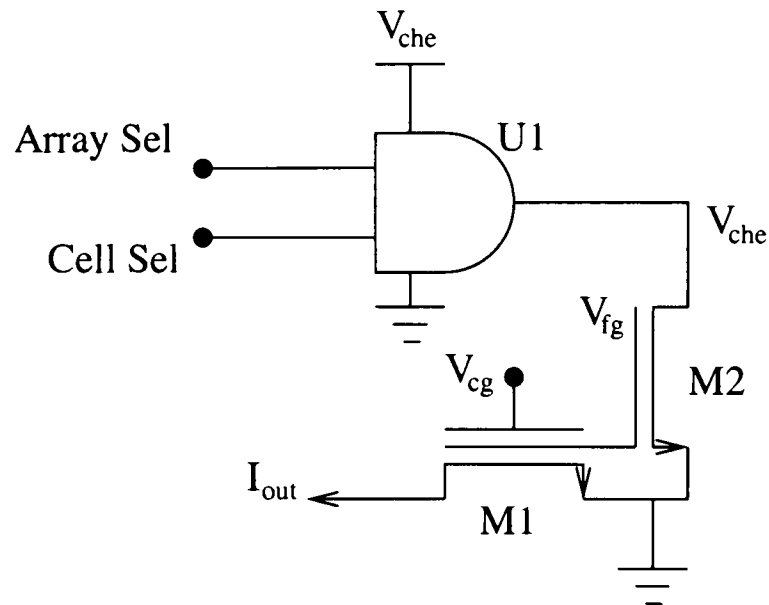


Figure 2.4: *CHEI Programming Selection Circuit*

2.2.2 CHEI Programming Selection Circuit

If the floating-gate circuit is to be used as an element in a DAC, then a circuit is required to select a particular element for programming. For CHEI programming, this selection circuit must supply voltages larger than the nominal $V_{dd} = 3.3V$. Therefore, 5V transistors, which are available in this process, are used. The selection circuit, shown in Figure 2.4, consists of an AND gate, U1. This circuit has two input signals, *ArraySel* and *CellSel*. *ArraySel* signal is high when any element in an array is to be programmed using CHEI and *CellSel* is only high if the particular element in the array is to be programmed. The AND gate is powered by the CHEI programming voltage, V_{che} . The programming starts when both selection signals are high. The output of the AND gate provides the drain of the programming MOSFET, M2, with the programming voltage, V_{che} . M1 is the sense NMOS transistor.

An advantage of this circuit is that it is very simple. However, each floating-gate element requires this selection circuit which adds an area of $242\mu m^2$ to each device. The total area of the floating-gate element is now $542\mu m^2$.

2.2.3 FNT Programming Selection Circuit

As in the case of CHEI programming, in order to be able to select a specific floating-gate element in a large matrix for FNT programming, a selection circuit is required to handle large

voltages. The circuit used, first suggested by Mann [84] and shown in Figure 2.5(a), consists of 2 digital gates, U1 and U2, and 6 transistors, M1-M6. M1-M4 are 5V PMOS transistors and M5-M6 are special high voltage n-channel transistors available on this process. The high voltage transistors are available as predefined cells. Since these standard cells were too large, a device with reduced dimensions was created.

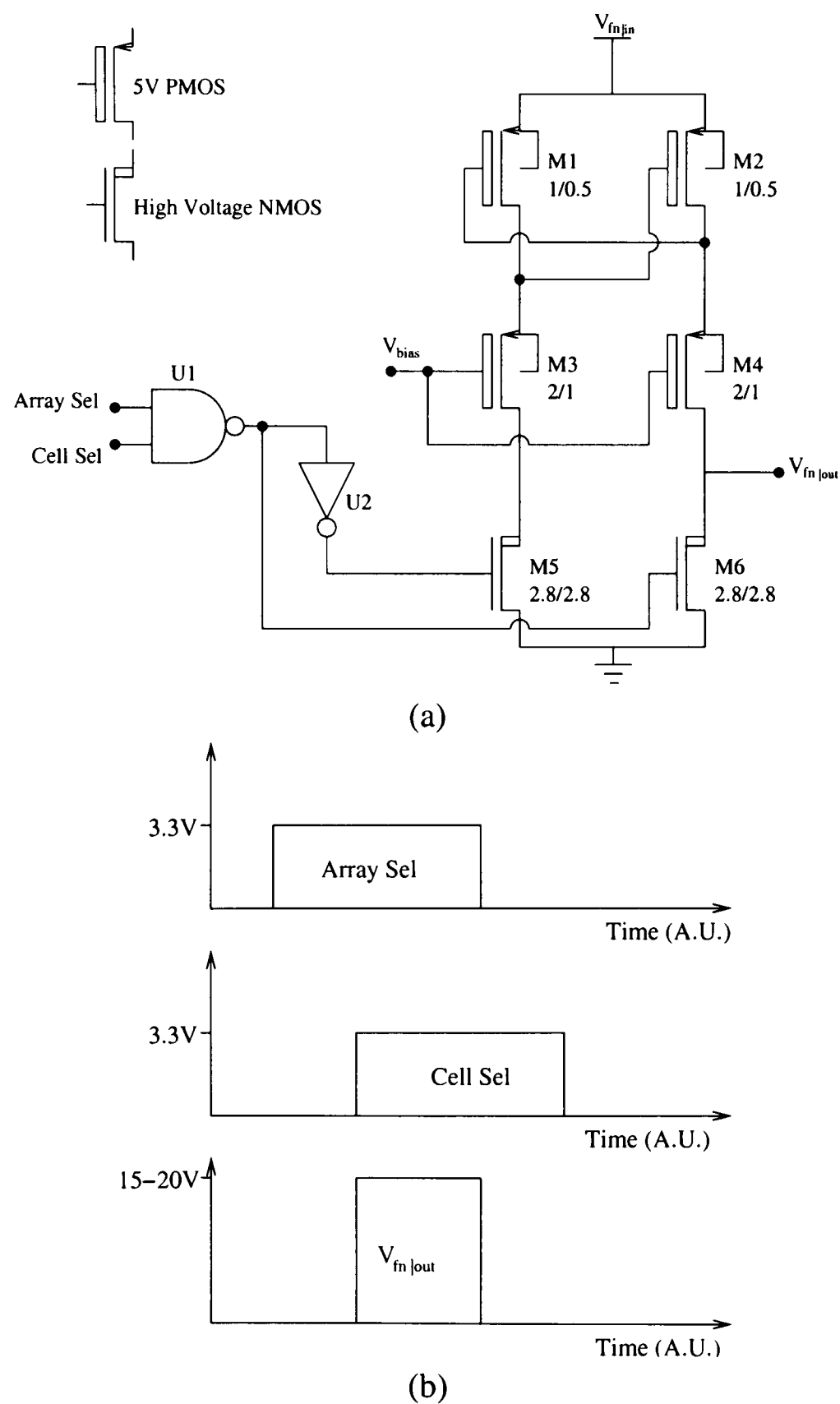


Figure 2.5: *FNT Selection Circuit and Simulation Results*

The supply voltage of the circuit is $V_{fn|in}$ with the output voltage, $V_{fn|out}$, tapped at the drain of M6. V_{bias} is set at 7V. The two digital input selection signals, $CellSel$ and $ArraySel$, determine which floating-gate element in a specific array is to be programmed using FNT. As shown in the simulation results in Figure 2.5(b) when either signal is low, the output is 0V. The output is $V_{fn|out} \approx V_{fn|in}$ only when both signals are high. The layout area of this circuit is $1350\mu m^2$. With this selection circuit added to the floating-gate element consisting also of the CHEI selection circuit, the total area is $1892\mu m^2$.

2.3 Channel Hot Carrier Programming Characteristics

The programming mechanisms rely upon the behaviour of a MOSFET which is not characterised by the manufacturer. Therefore in order to be able to model this behaviour, it is necessary to characterise the programming mechanisms in this process. To achieve this, several samples of the floating-gate devices have been manufactured with all the nodes of this circuit externally accessible.

Hot carrier injection occurs when the drain bias conditions of the programming transistor are extreme. In this process, the recommended V_{dd} is 3.3V therefore larger drain voltages are expected to generate “hot carriers” which are injected on to the gate. The programming voltage, V_{che} , which is applied to the drain of M2 must therefore be sufficiently large to enable the generation of these “hot carriers”. To observe both injection mechanisms, CHHI and CHEI, the first experiments are started with the floating-gate voltage just above threshold. As expected, at this low gate voltage, CHHI is observed. This mechanism injects positive charge on to the floating-gate which increases the floating-gate voltage and hence the sense transistor output current. To characterise this mechanism, both V_{cg} and V_{out} are fixed and I_{out} is measured for several V_{che} voltages until no noticeable change in the output current is detected. To determine the CHEI characteristics, a second set of experiments is required with the floating-gate voltage initiated at around 5V. With a sufficiently high V_{che} , the CHEI mechanism will inject electrons on to the floating-gate. This will reduce V_{fg} and hence I_{out} . Once again the experiment stops

when the rate of change of I_{out} is small.

The hot carrier injection characteristics are described in terms of the gate current due to the hot carrier injection as a function of the bias conditions. Therefore the measured variation in the output current of the sense transistor due to CHHI and CHEI needs to be translated into a gate current. The relationship between I_g and V_{fg} is

$$I_g = C_{tot} \frac{\partial V_{fg}}{\partial t} \quad (2.2)$$

where C_{tot} is the total capacitance of the floating-gate. From Figure 1.3(a) it can be seen that C_{tot} is the sum of the floating-gate capacitance, C_{fg} , and the total channel capacitance, C_{chan} , and the FNT injection capacitance, C_{fn} . From the device layout, C_{fg} , C_{fn} and C_{chan} are estimated to be $101 fF$, $0.9 fF$ and $24 fF$ respectively. The rate of change of V_{fg} can be determined from the rate of change of I_{out} using the I-V characteristics of M1 as a mapping function. However, since the exact floating-gate voltage is not known, a standard MOSFET, identical to M1 and placed close to M1, is used to provide the I-V characteristics.

$$V_g = f(I)|_{experiment} \quad (2.3)$$

$$\left. \frac{\partial V_{fg}}{\partial t} \right|_{estimate} = \frac{\partial f}{\partial I} \left. \frac{\partial I_{out}}{\partial t} \right|_{experiment} \quad (2.4)$$

Hence, using the measured rate of change of I_{out} and the above equations, I_g is estimated for several V_{che} conditions.

Figure 2.6 shows the variation of the derived I_g with V_{fg} as V_{che} is varied from 5V to 6V. As expected, at low floating-gate voltages ($V_{fg} < 1.5V$) CHHI is observed during the experiments. The data in Figure 2.6(a) shows that the maximum gate current ranges from $0.75 \times 10^{-16} A$ with $V_{che} = 5V$ to $12 \times 10^{-16} A$ with $V_{che} = 6V$. For higher floating-gate voltages, $V_{fg} > 1.5V$, CHEI is observed. Figure 2.6(b) shows the variation of the electron gate current on a logarithmic scale with floating-gate voltage. As expected, the electron injection current is found to be orders of magnitude larger than the hole injection current [74, 75]. It can also be seen from this figure that the gate current has an exponential relationship with the floating-gate voltage.

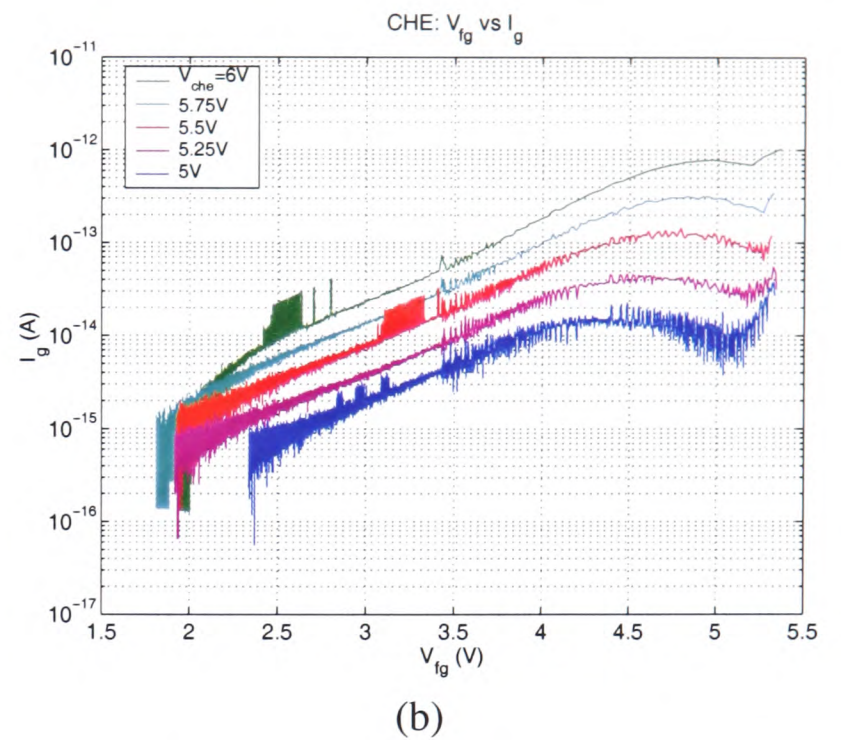
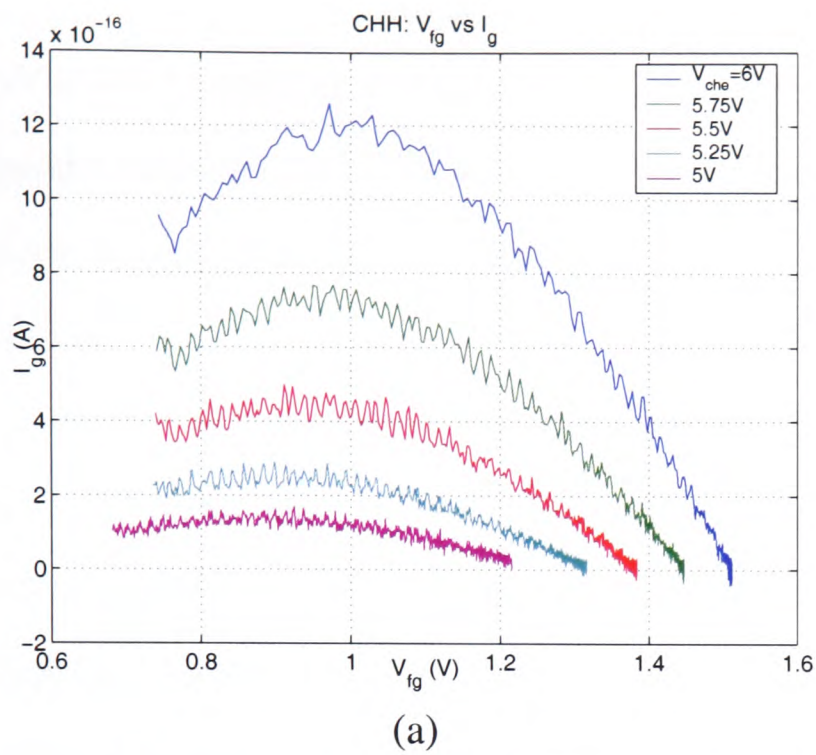


Figure 2.6: *Floating-gate MOSFET Hot Carrier Injection Programming Characteristics.* (a) shows the hot hole injection current derived from the measured rate of change of V_{fg} for $V_{fg} < 1.5V$. (b) shows the variation of the hot electron injection current derived from the measured rate of change of V_{fg} for $V_{fg} > 1.5V$. The noise in both plots is due to the numerical differentiation of the V_{fg} data.

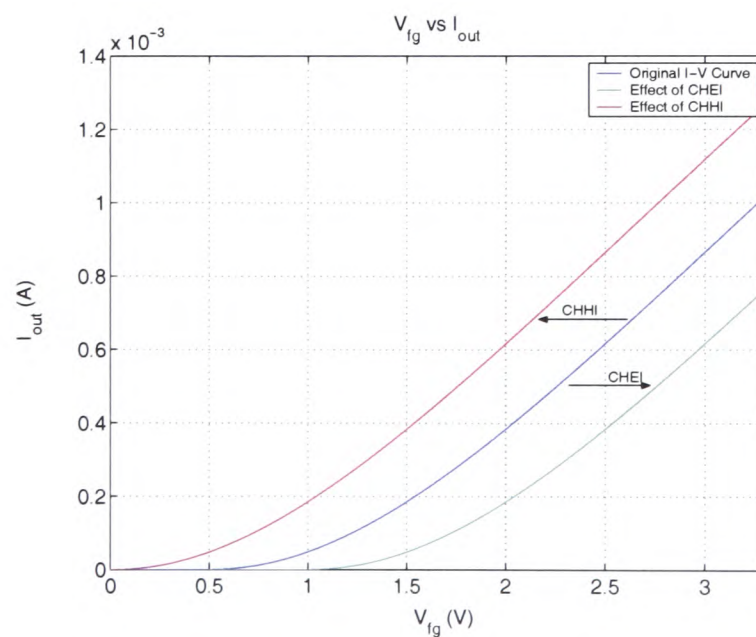


Figure 2.7: *Effect of Hot Carrier Injection.* CHEI increases the threshold voltage and CHHI decreases it.

These measurements suggest that V_{fg} can be both increased and decreased using channel hot carrier injection. Figure 2.7 shows the effect of the CHHI and CHEI programming on the I-V characteristics of a floating-gate device. As expected, holes injected on to the floating-gate using CHHI has the effect of decreasing the threshold voltage of the sense MOSFET. On the other hand, CHEI has the effect of increasing the threshold voltage and hence reducing the current.

Ideally, all charge carriers injected into the SiO_2 should be able to escape on to the floating-gate. However, carrier transport through the SiO_2 is far from ideal. In particular, the gate oxide which insulates the floating-gate from the channel contains defects that traps charge. Charge trapping and interface state generation within the gate oxide reduces the predictability of hot carrier injection. In standard MOSFETs, hot hole injection has been associated with an increase in interface trap generation and oxide trap charging [69, 85, 86]. These mechanisms also occur with hot electron injection, however, the damage due to electrons is less severe. The increased damage and low injection rates of holes suggest that CHHI should not be used to increase the floating-gate voltage. Therefore, only hot electron injection is considered as a viable hot carrier mechanism for floating-gate programming.

2.3.1 Empirical Modeling of CHEI

In order to be able to predict the CHEI characteristics, a model of the mechanism is required. Previous work by Diorio et al. [44, 87] uses a simple exponential model, given by Equation 2.5, to fit the CHEI data. In this model, the gate current, I_g , is a function of the programming channel current, I_{ds} , and the programming MOSFET drain-source voltage, V_{che} .

$$\frac{I_g}{I_{ds}} = Ae^{\frac{V_{che}}{V_{inj}}} \quad (2.5)$$

where both A and V_{inj} are empirical model parameters derived for a particular constant channel programming current and floating-gate voltage. This model was developed to explain the programming of p-channel programming MOSFETs operating in subthreshold. It also does not

take into account the dependence of the floating-gate voltage on the injection current. Therefore an alternative flexible model is required to predict the CHEI behaviour of an n-channel floating-gate MOSFET.

Inspection of the data suggested that a useful model would assume that the normalised gate current is an exponential function of the floating-gate voltage and programming drain voltage.

$$\frac{I_g}{I_{ds}} = N e^{(AV_{fg})} e^{(BV_{che})} \quad (2.6)$$

where N , A and B are empirical fitting constants. Taking the natural logarithm of Equation 2.6 gives a first order linear function.

$$\log_e \frac{I_g}{I_{ds}} = \log_e N + AV_{fg} + BV_{che} \quad (2.7)$$

To fit the model, the CHEI data, shown in Figure 2.6(b), represented as a normalised gate is shown on a logarithmic scale in Figure 2.8. For a constant V_{che} condition, Equation 2.7 can be re-written as a first order linear equation with gradient A and y-intercept $\log_e N$ as shown in Equation 2.8.

$$\log_e \frac{I_g}{I_{ds}} - BV_{che} = \log_e N + AV_{fg} \equiv Y = C + MX \quad (2.8)$$

A is therefore the gradient of each of the different V_{che} curves in Figure 2.8. It can be seen from this figure that the gradients of the curves are constant between $3 < V_{fg} < 3.75\text{V}$ for all 5 V_{che} conditions. Therefore, evaluating A as the average gradient of the 5 curves in this region gives $A = 1.4$. Using the y-intercept from Equation 2.8, N is found to be $e^{(-41.425)}$. Re-writing Equation 2.7 for a constant V_{fg} condition gives

$$\log_e \frac{I_g}{I_{ds}} - AV_{fg} = \log_e N + BV_{che} \equiv Y = C + MX \quad (2.9)$$

Therefore, in order to determine the remaining constant, B , vertical intercepts of the curves in

Figure 2.8 are taken at various V_{fg} values between 3V and 3.75V . These intercepts give the variation of $\frac{I_g}{I_{ds}}$ with V_{che} at constant V_{fg} as required by Equation 2.9. Evaluating the average gradient of these lines gives $B = 2.35$. The result is an overall model

$$\frac{I_g}{I_{ds}} = e^{(-41.425)} e^{(1.4V_{fg})} e^{(2.35V_{che})} \quad (2.10)$$

that is compared to the measured data in Figure 2.8. The model curves are a good fit to the experimental data in the evaluated range. However, the model cannot explain the peak in the gate currents seen at high floating-gate voltages.

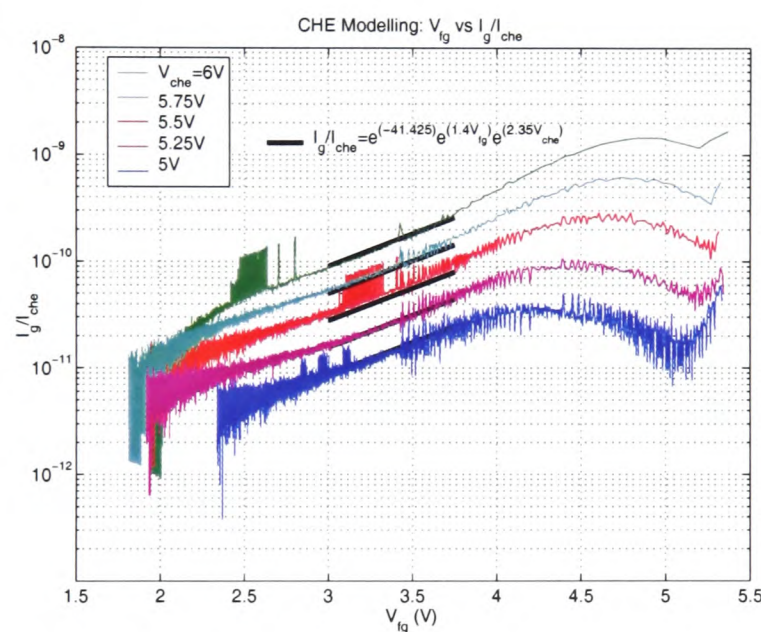


Figure 2.8: *fg-MOS CHEI Model 1*

Since the programming channel current is a function of the floating-gate voltage, a second model which evaluates the gate current as a function of only the programming current, I_{ds} , and V_{che} was also investigated.

$$I_g = K(I_{ds})^n e^{(CV_{che})} \quad (2.11)$$

where K , n and C are fitting constants. Re-writing this equation in a logarithmic form gives

$$\log_e I_g = \log_e K + n \log_e I_{ds} + CV_{che} \quad (2.12)$$

In order to evaluate the model parameters, I_g is plotted against I_{ds} for several V_{che} conditions ranging from 5V to 6V in Figure 2.9. From Equation 2.12, it can be seen that for constant V_{che} , the gradient of the curves gives n , which was found to be 4.1. The constant C was evaluated as the average gradient of the curves formed by taking the vertical intercepts at various I_{ds} and found to be 1.9. The y-intercept of the linear curves gave $\log_e K = -9.01$. The overall model is therefore given by

$$I_g = e^{(-9.01)} I_{ds}^{4.1} e^{(1.9V_{che})} \quad (2.13)$$

This equation is shown for the 5 V_{che} conditions in Figure 2.9. As with the previous model, this model also gives a good fit to the experimental data over the same gate current range. However, this model also does not explain the gate current peaks observed at high gate voltages.

Both models can however be used to predict the injection gate currents for higher programming voltages. For similar channel currents, the gate current increases by an order of magnitude as V_{che} is increased to 7V and a further order of magnitude increase is expected with a programming voltage of 8V.

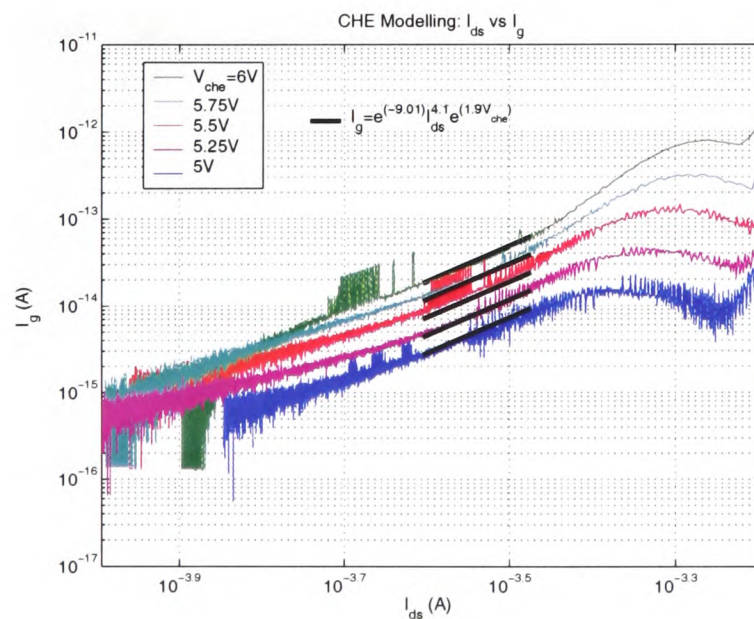


Figure 2.9: *fg-MOS CHEI Model 2*

Both of these models can be used to predict the programming conditions required to program the floating-gate voltage to a specific voltage. However, this approach is only possible if CHEI

programming is consistent from one device to another on the same chip.

2.3.2 CHEI Programming Variations

To estimate the variability of CHEI, the injection gate currents for seven different floating-gate elements on the same chip were evaluated. The results, plotted in Figure 2.10, show that the gate current in different devices is consistent to within a factor of two for floating-gate voltages greater than 2V. These variations arise because of the different field conditions at the drain of the programming MOSFET. These differences are due to stochastic variations of the parameters which affect the drain field. The variations in the gate current mean that some form of feedback mechanism must be used in order to program a precise floating-gate voltage.

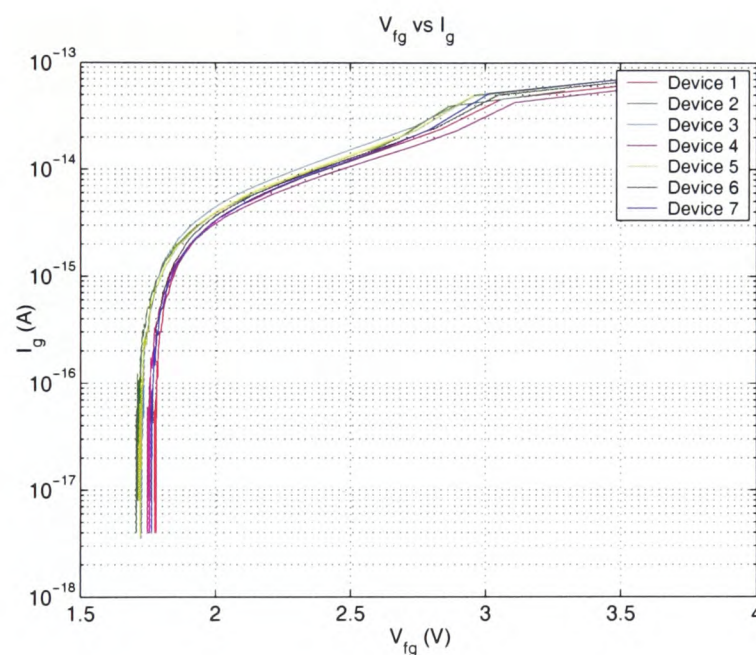


Figure 2.10: *CHEI Programming Variation Across the Die.*

Another problem with achieving a precise voltage on the floating-gate is the disturbance caused by the coupling of the programming voltage via the gate-drain overlap capacitance. The estimated overlap capacitance is 0.25 fF which means that the coupled voltage is $0.002 \times V_{che}$. Thus for example, with a programming voltage of 6V, the disturbance is 12mV. This disturbance therefore needs to be taken into account whilst programming using a feedback mechanism.

2.4 Fowler-Nordheim Tunneling Programming Characterisation

The maximum programming voltage that can be applied to induce FNT is limited to the breakdown voltage of a poly1-poly2 capacitor which is at least 15V and typically 30V. This programming mechanism removes electrons from the floating-gate, therefore, V_{fg} increases during programming. The effective tunneling voltage is therefore reduced and the output current of the sense transistor is increased. Programming characteristics of a device can therefore be evaluated by monitoring changes in the sense transistor output current whilst a specific programming voltage is applied to the tunneling node.

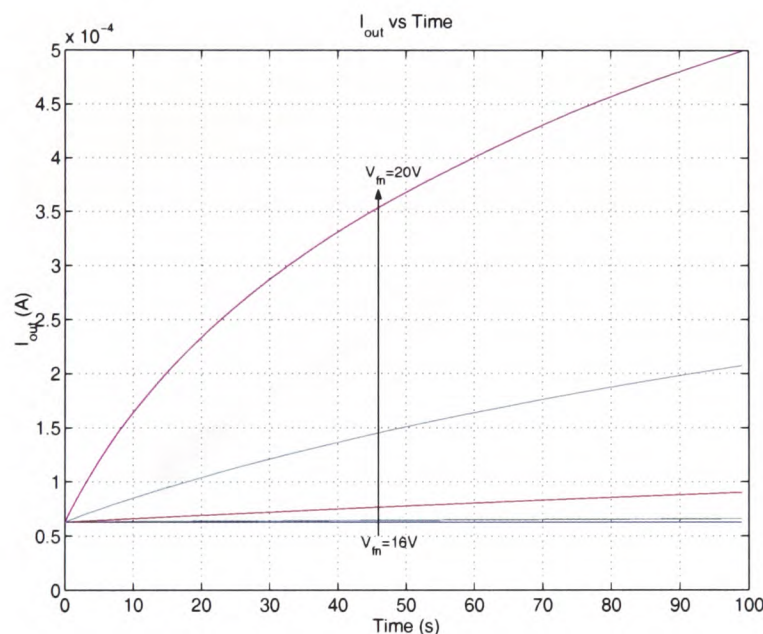


Figure 2.11: *FNT programming at various tunneling voltages over 100s. The rate of change of the sense transistor output current increases as V_{fn} increases from 16V to 19V.*

Figure 2.11 shows the variation of the sense transistor channel current over a period of 100 seconds for several values of V_{fn} ranging from 16V to 19V. For all the experiments, the channel current is initialised to an arbitrary value of $60\mu A$ which corresponds to an initial floating-gate voltage of approximately 1V. In addition, V_{out} is set to 2V to minimise the effect of CHEI in the sense transistor. As expected, the rate of change of channel current increases significantly as V_{fn} increases from 16V to 19V. For voltages lower than 16V, no change in the output current was observed over the 100 seconds. The device is then damaged irreversibly by applying a V_{fn}

of 21V. This damage is due to the breakdown of the tunneling poly1-poly2 capacitor which has a breakdown rating between 15V to 30V.

As with CHEI, the tunneling current is derived from the rate of change of the measured output current by using the measured I-V characteristics of a MOSFET identical to the sense transistor as a mapping function. Hence, the tunneling current is given by

$$V_g = f(I)|_{\text{experiment}} \quad (2.14)$$

$$\left. \frac{\partial V_{fg}}{\partial t} \right|_{\text{estimate}} = \left. \frac{\partial f}{\partial I} \frac{\partial I_{out}}{\partial t} \right|_{\text{experiment}} \quad (2.15)$$

$$\Rightarrow I_{tun} = C_{tot} \frac{\partial V_{fg}}{\partial t} \quad (2.16)$$

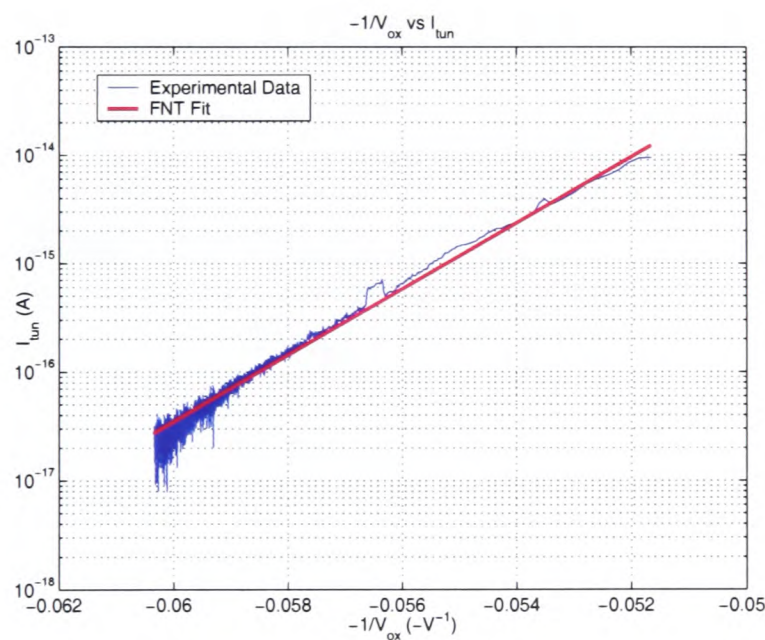


Figure 2.12: The derived FNT current shown together with the simple FNT model.

The model for FNT injection current is [24, 77]

$$I_{tun} = \varphi V_{ox}^2 e^{-\frac{V_f}{V_{ox}}} \quad (2.17)$$

where φ and V_f are fitting parameters and V_{ox} is the tunneling oxide voltage which is the difference between V_{fn} and V_{fg} . This expression can be simplified if it can be assumed that the exponential term dominates. The validity of this assumption can be demonstrated from the

logarithms of Equation 2.17.

$$\log_e I_{tun} = \log_e \varphi + 2\log_e V_{ox} - \frac{V_f}{V_{ox}} \quad (2.18)$$

From the experimental data, $\log_e I_{tun}$ has a range from -38 to -32.3 and $2\log_e V_{ox}$ varies from 5.63 to 5.91. These values show that the variation of the second term in the above equation does not make a significant contribution to the tunneling current variations. Equation 2.18 can be re-written by letting $x = \frac{1}{V_{ox}}$ and $y = \log_e I_{tun}$

$$y = \log_e \varphi - 2\log_e x - V_f x \quad (2.19)$$

It can also be assumed the variation of x is small. The second term in Equation 2.18 is then given by

$$2\log_e x = 2\log_e(x_0 + \Delta x) \quad (2.20)$$

$$= 2\log_e \left(x_0 \left[1 + \frac{\Delta x}{x_0} \right] \right) \quad (2.21)$$

$$= 2 \left[\log_e x_0 + \log_e \left(1 + \frac{\Delta x}{x_0} \right) \right] \quad (2.22)$$

$$\approx 2 \left[\log_e x_0 + \frac{\Delta x}{x_0} \right] \quad (2.23)$$

Substituting this approximation into Equation 2.19 gives

$$y \approx \log_e \varphi - 2 \left[\log_e x_0 + \frac{(x - x_0)}{x_0} \right] - V_f x \quad (2.24)$$

$$y \approx (\log_e \varphi - 2\log_e x_0 + 2) - \left(\frac{2}{x_0} + V_f \right) x \quad (2.25)$$

This leads to a simplified model

$$\log_e I_{tun} = \log_e \varphi' - \frac{V_f'}{V_{ox}} \quad (2.26)$$

$$I_{tun} = \varphi' e^{-\frac{V_f'}{V_{ox}}} \quad (2.27)$$

where the relationships between the original and modified constants, φ' and V_f' , are given by

$$\log_e \varphi' = \log_e \varphi - 2\log_e x_0 + 2 \quad (2.28)$$

$$V_f' = 2V_{ox|_0} + V_f \quad (2.29)$$

where $V_{ox|_0}$ is the first value in the V_{ox} data. This simplified model has been used previously by Diorio et al. [44, 87] to describe FNT injection between the floating-gate and an n-well. The parameters for Equation 2.27 can be extracted by plotting the variation of $\log_e I_{tun}$ against $\frac{-1}{V_{ox}}$ on a logarithmic scale as shown in Figure 2.12. This gives the simple FNT model

$$I_{tun} = 72.24e^{-\frac{703}{V_{ox}}} \quad (2.30)$$

This model is also shown in Figure 2.12 together with experimental data. Using the relationships between the fitting constants of the two models, the parameters of the original model are also evaluated. This gives

$$I_{tun} = 0.0264V_{ox}^2 e^{-\frac{664.5}{V_{ox}}} \quad (2.31)$$

The two FNT models are compared in Figure 2.13. It can be seen from this comparison that the simple model is a very good approximation of the original model. This suggests that the assumptions made in deriving the simple model are valid.

2.4.1 FNT Programming Variations

The FNT models in the previous section were derived from a single device. In order to be able to use Equations 2.30 and 2.31 confidently, it is necessary to determine the variation of the FNT programming mechanism from one floating-gate element to another on the same chip. Five devices on a single chip were programmed using FNT to determine the variation of the FNT current with the oxide voltage. These tunneling currents are shown in Figure 2.14. It can be seen that the programming rate varies by up to an order of magnitude from one element to

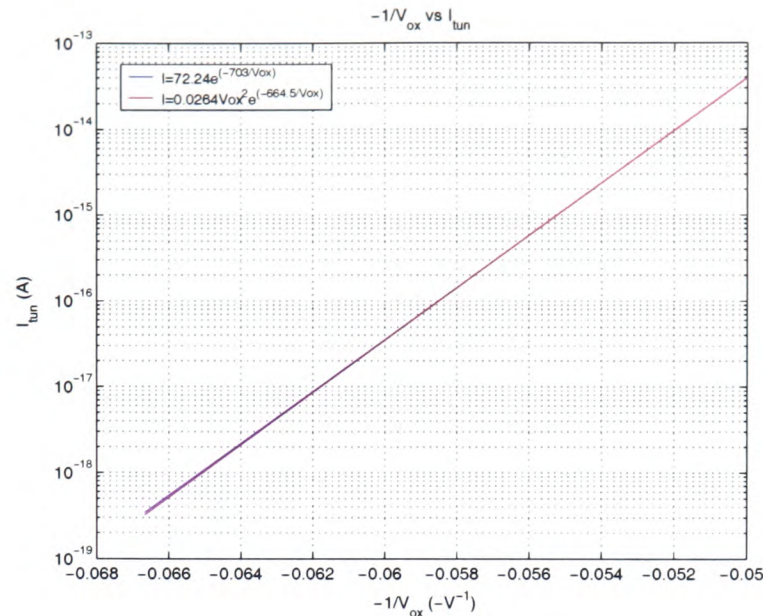


Figure 2.13: *Comparison of the two FNT models.*

another. These variations are however consistent with previous measurements of FNT through inter-polyoxide that suggested that the injection current is dominated by conduction in small areas, thus causing large variations [83]. These results therefore suggest that it will be very difficult to predict the FNT characteristics of a specific floating-gate element in a single chip. Thus, some form of a feedback system will be required to monitor the current changes during the programming of each element.

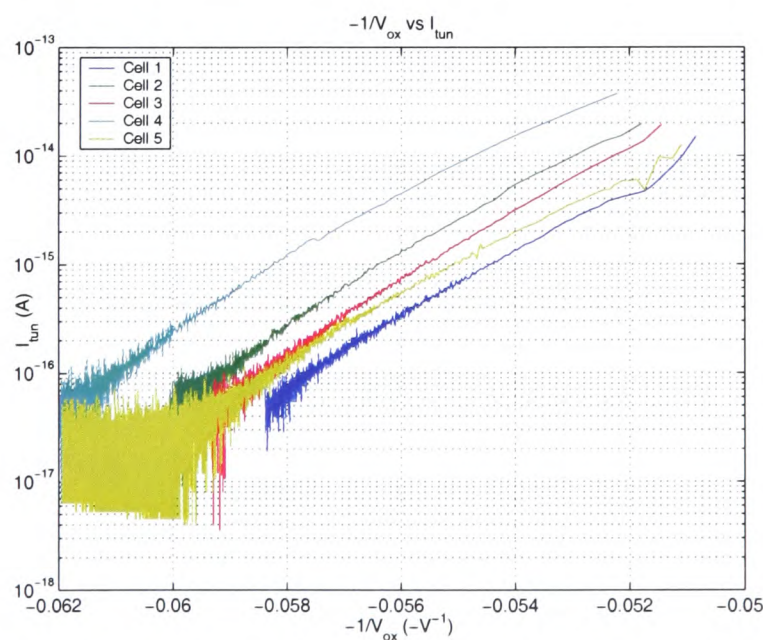


Figure 2.14: *FNT Programming Variation*

However, even with a feedback system, this programming mechanism has a problem. As explained earlier in Section 2.2.1, when V_{fn} is applied to the element, an instantaneous increase

in the output current is observed due to C_{fn} . The feedback system would therefore not be able to determine the static state of the floating-gate since the voltage change due to C_{fn} is significant. In order to eliminate this problem, another coupling capacitor can be added, which has a negative voltage applied to it during programming to compensate for the increase in current due to V_{fn} . The compensating capacitor would be required to perfectly match the FNT capacitor which is difficult to achieve. This is because the FNT injector is of minimum geometry and therefore likely to be extremely variable.

2.5 Charge Retention

Once a device is programmed, it will be required to retain the data. The retention characteristics fall into two categories. The first is the long term retention of the charge whilst the chip is stored. More importantly for programmable analogue memories is charge loss from the floating-gate during normal operation.

2.5.1 Long Term Charge Retention in Storage

The floating-gate is surrounded by SiO_2 which is a very good insulator. Therefore, the charge on the floating-gate does not have any mechanism to leak away if the device is stored in a static free environment. It is therefore surprising that experimental data presented by Millard et al. [88] suggested that these devices suffer from charge leakage whilst in storage.

In order to investigate the stability of charge on the designed devices, the I-V characteristics of a device were measured before and after a 7 day interval. During this interval, the test chip was placed in an anti-static environment. The variation of I_{out} with V_{cg} before and after the interval, shown in Figure 2.15, is similar to that obtained by Millard et al..

During these experiments normal electro-static discharge (ESD) precautions were taken. An anti-static arm band was always worn. In addition, the bond-pad connecting to the control-gate of all the floating-gate devices was protected by a conventional ESD protection circuit. Despite these precautions, it became apparent during various experiments that the floating-gate devices

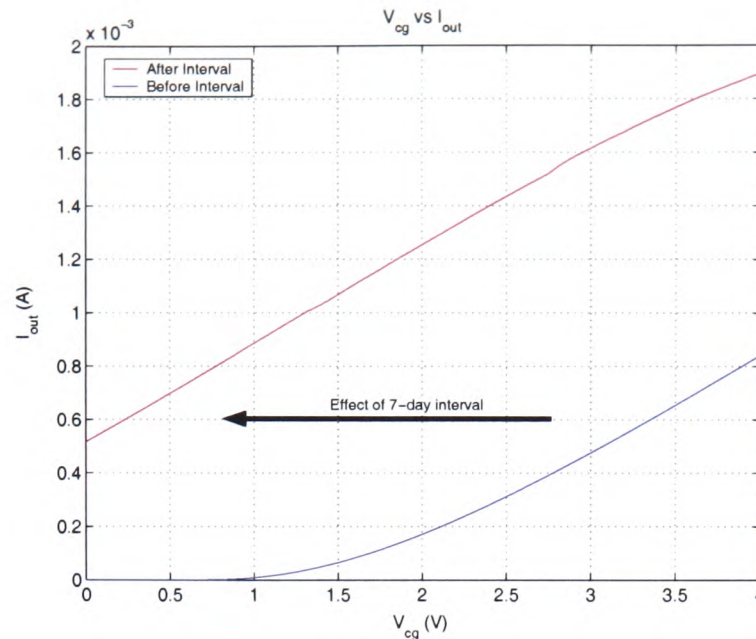


Figure 2.15: *Effect of a 7-day interval on the variation of I_{out} with V_{cg} . Significant charge loss is observed.*

were vulnerable to sudden, small but measurable changes in floating-gate voltage. This raised the possibility that the loss of charge on the floating-gate observed in the data in Figure 2.15 was caused by the handling of the device during the experiment rather than during storage.

To test this possibility, the device was characterised, removed from its socket, as if to place it in storage, and then immediately replaced in the socket and re-characterised. During these experiments a similar level of charge loss to that shown in Figure 2.15 was observed. These results lead to the conclusion that the floating-gate devices are more vulnerable to ESD than conventional digital devices. On reflection it is unwise to assume that protection mechanisms that are sufficient to prevent a gate current which is large enough to cause permanent damage to the gate of a MOSFET to be sufficient to prevent a measurable charge loss from a floating-gate.

With the level of ESD protection implemented on the test chip it has been impossible to clearly demonstrate the long term storage capability of the floating-gate devices.

2.5.2 Charge Retention during normal operation

All previous experiments have characterised the loss of data from a stored floating-gate device caused by charge leakage. A more important situation for analogue memory devices is its ability to retain data during normal operation.

With a higher than usual drain voltage, in the range 5V to 6V, it is possible to program a floating-gate device using CHEI. This mechanism relies upon creating a high lateral field close to the drain that gives rise to hot carriers. When these carriers have an energy of greater than 3.2eV they can be injected into the gate oxide. It is therefore expected that the gate current caused by CHEI should reduce to zero once the source-drain voltage is less than 3.2V. However, results reported by Ghetti et al. [89, 90] for EEPROM devices, show gate-currents at drain voltages as low as 1V. At these low voltages, Ghetti et al. concluded that the generation of hot carriers arises from carrier-carrier interactions in the channel and not due to energy gained by the electric field in the drain. These interactions transfer energy between carriers with the result that some of them have more energy than the maximum expected with a particular source-drain voltage. Therefore, in the designed floating-gate device, CHEI is expected to occur in the sense transistor, whose V_{ds} is always less than 3.3V. This means that even during normal operation, there is a mechanism that has the potential to change the charge on the floating-gate.

To determine the CHEI characteristics at normal operating drain-source voltages, the rate of change of the output current of the sense transistor was monitored at three different V_{ds} voltages ranging from 3V to 1V. Figure 2.16(a) shows change in the output current for the 2V and 3V conditions over 300000s (3.47 days). The initial V_{fg} for all experiments is set to approximately 3V.

The first observation, shown in a close-up view of these results in Figure 2.16(b), is a relaxation phenomenon lasting approximately one hour. In both V_{ds} cases, the initial output current decays by $6\mu\text{A}$ from initial currents of $701\mu\text{A}$ for $V_{ds} = 3\text{V}$ and $696.5\mu\text{A}$ for $V_{ds} = 2\text{V}$. The floating-gate voltage for each experiment was increased from an arbitrary value to 3V. It has been suggested by Kirton et al. [91] that this change in voltage, moves some carrier traps at the $\text{Si} - \text{SiO}_2$ interface to an energy below the Fermi energy of the device. Once the device is switched on, these traps attract electrons from the channel and thus reduce the channel current.

This initial transient was followed by a slower change in the output current caused by changes in the floating-gate voltage. The measured fractional change in the output current over 300000s gives $\frac{\Delta I}{I}|_{V_{ds}=3\text{V}} = 1.34\%$ and $\frac{\Delta I}{I}|_{V_{ds}=2\text{V}} = 0.19\%$. These variations are not ac-

ceptable for floating-gate devices which are programmed after fabrication to achieve a specific accuracy. Furthermore, a gate current has been observed for $V_{ds} = 2V$, a voltage at which the drain electric field is not high enough to be able to generate any electrons with energy greater than the $3.2eV$ required to cross the $Si - SiO_2$ barrier.

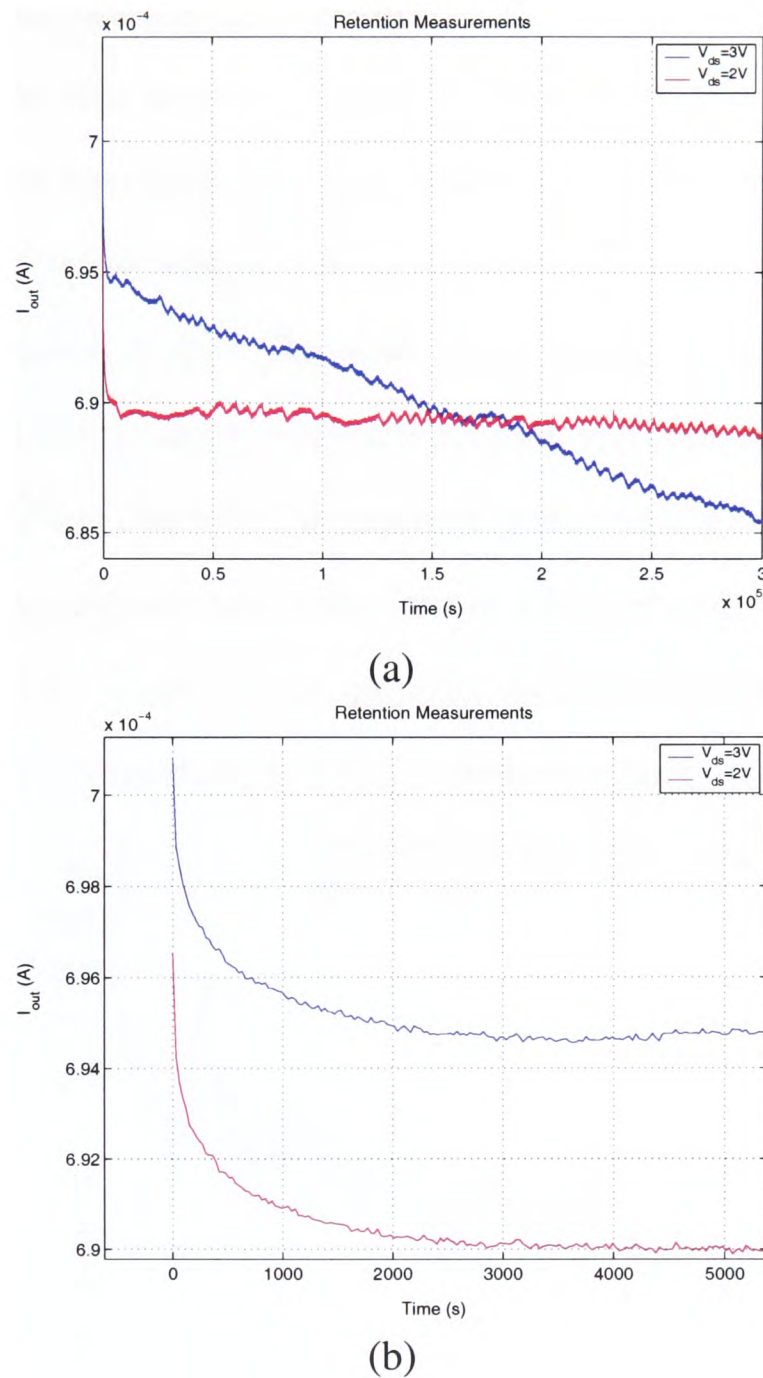


Figure 2.16: Charge retention in a floating-gate MOSFET with $V_{ds}=2V$ and $3V$.(a) shows the change in the output current over 300000s. (b) shows the initial relaxation phenomenon which stabilises after 3000s.

The measured results for $V_{ds} = 1V$, taken over 600000s (6.94 days), are shown in Figure 2.17. A current change of $\frac{\Delta I}{I}|_{V_{ds}=1V} = 0.1\%$ is observed which corresponds to 0.05% for the same timescale as the experiments for $V_{ds} = 2V$ and $3V$. These results confirm that CHEI can occur at drain-source voltages as low as $1V$, as predicted by Ghetti et al..

The observed results cannot be predicted from the CHEI models described earlier since the models were derived for injection currents from hot electrons which are excited by a high electric field at the drain of the MOSFET. As reported by Ghetti et al., the gate currents observed for $V_{ds} < 3.2\text{V}$, are due to electrons gaining enough energy through interactions with other electrons in the channel and drain of the MOSFET.

It is also clear from the data shown in Figure 2.17 that the output current also suffers from a periodic oscillation of an amplitude of $0.1\mu\text{A}$ which represents a variation of approximately $\pm 0.02\%$. Nearly 7 peaks in the current can be seen over a period of 7 days which suggests the period of the oscillation is 1 day. The most likely source of these variations is the daily oscillation of the ambient temperature. From temperature variation simulations of a MOSFET, a change in temperature of less than 0.5°C is required to observe the current variation seen in the experimental results. These experiments were done at a temperature of 40°C in an oven with a temperature tolerance of 1°C . Therefore, the periodic oscillation of the output current observed can be attributed to a daily variation of up to 0.5°C in the operating temperature of the test chip.

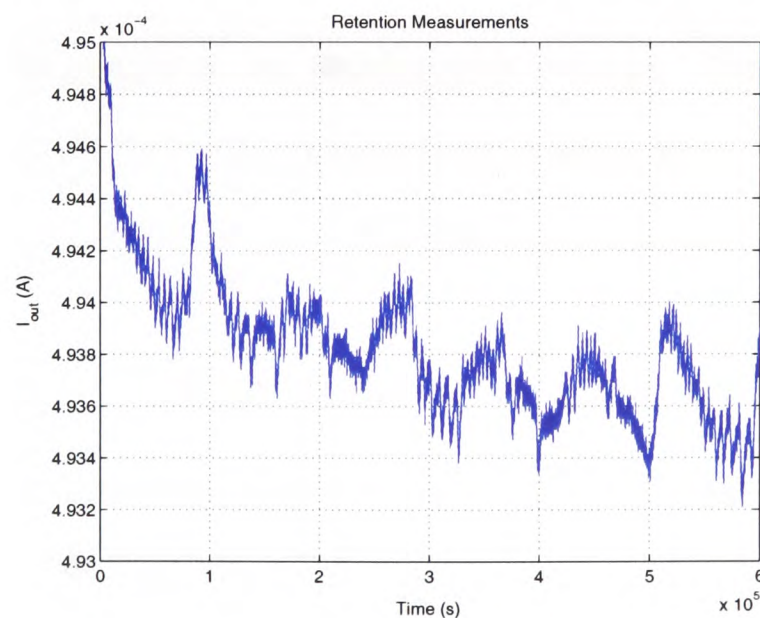


Figure 2.17: Charge retention in a floating-gate MOSFET with $V_{ds} = 1\text{V}$. A periodic oscillation of the output current can also be seen.

The results in Figure 2.17 suggest a slow change in the floating-gate voltage even with a low V_{ds} . However, the most striking feature of this data is that temperature variations of less than 1°C have a larger effect than this slow change in the floating-gate potential. The impact of temperature variations must therefore be investigated.

2.6 Conclusion

A floating-gate device designed to be fabricated on a standard double poly $0.35\mu m$ CMOS technology has been described. The device consists of two n-channel MOSFETs which share the floating-gate. One transistor is the CHEI programming transistor and the other one is the sense/read transistor. The floating-gate is capacitatively coupled to a control-gate and a tunneling node. The charge on this floating-gate device, which has an area of $300\mu m^2$, can therefore be changed using either CHEI or FNT.

In addition to the floating-gate device, programming selection circuits for both CHEI and FNT have also been described. These circuits are required to be able to select any floating-gate element in a matrix for either CHEI or FNT programming. Therefore, both of these circuits must be able to handle the high voltages required for CHEI ($> 5V$) and FNT ($> 15V$). A consequence of adding these circuits to the floating-gate element is that the total area is increased to $1892\mu m^2$.

CHEI characteristics of the floating-gate device are investigated for several values of the programming voltage. As expected, the injection current is found to be a function of this programming voltage and the instantaneous floating-gate voltage. Two novel empirical models describing the CHEI characteristics are shown to be a good fit to the experimental data for floating-gate voltages ranging from $3V$ to $3.75V$ and programming voltages ranging from $5V$ to $6V$.

The CHEI characteristics of several devices on the same chip have been measured. As shown in Figure 2.10, the injection currents from all of the devices vary by less than a factor of 2. The model for CHEI can therefore only be used to specify the conditions required to achieve acceptable programming rates. Accurate programming will only be possible if a feedback mechanism is employed to stop programming once the desired output is achieved.

FNT is observed when a voltage greater than $16V$ is applied to the tunneling node. This mechanism is used to complement the CHEI mechanism by removing electrons from the floating-gate. The derived tunneling current, shown in Figure 2.12, is found to be consistent with the tunneling current model described by Equation 2.17. This model has been simplified to a model

used previously by Diorio et al. [87].

The FNT current of several different nominally identical floating-gate devices on the same chip are found to vary by as much as an order of magnitude. These differences are due to variable nature of the asperities in the poly-oxide layer which is used for tunneling. Therefore, as with CHEI, this mechanism can only be used for precise programming using some form of a feedback system.

The floating-gate is surrounded by SiO_2 which is a very good insulator. Thus under normal operating conditions charge should remain on the gate permanently. Unfortunately, observations during various experiments showed charge loss from the floating-gate which occurred during the handling of the test chips. It was therefore concluded, that the loss of charge that has previously been thought to occur during storage is actually due to electrostatic transients, small enough to pass through conventional ESD protection used on the control-gate pad. With these problems, it has not been possible to determine the long term storage capability of the floating-gate devices.

Despite these concerns, a more important property of the devices is their ability to store charge during normal operation. Several experimental results have shown that the floating-gate suffers from charge loss due to CHEI from the sense MOSFET in normal operation. The injection was observed at drain-source voltages as low as 1V. At these low voltages, the electric field at the drain is not high enough to generate hot electrons. An alternative mechanism, suggested by Ghetti et al. [90] that might explain these observations is carrier-carrier interactions that can create “hot” electrons at low drain voltages. At low drain voltages, the rate of charge loss is strongly voltage dependent. Therefore, to minimise the loss of charge from the floating-gate, the V_{ds} of the sense MOSFET must be reduced to less than 1V. At this low drain voltage, small variations in temperature cause larger variations in the output current than the loss of charge from the floating-gate over a period of several days. The trimmable current source should therefore be insensitive to temperature variations after programming.

Chapter 3

Trimmable Current Sources for Current Steering Digital-to-Analogue Converters

3.1 Introduction

To achieve the performance demanded by communications standards from DACs, careful design and layout is required. The main limitation of current steering DACs is the mismatch between the current sources. Several techniques for improving these matching properties have been published [4, 9, 15, 18, 20, 92–94]. These include using large area devices and centroid layout schemes [15, 18], complex switching [4, 9, 92] and dynamic calibration [20, 94]. All of these techniques increase the cost by increasing the design time and/or silicon area. It is therefore proposed to use a floating-gate device as a trimming element in current sources.

It has been shown in the previous chapter that the floating-gate voltage can be increased or decreased using either FNT or CHEI respectively. These programming mechanisms could therefore be applied to trim a floating-gate device in a current source to achieve the required output current. Using a programmable current source will avoid the need for careful layout and device sizing. Furthermore, it reduces design times and also avoid the power consumption required in dynamic calibration.

In this chapter, four different trimmable current sources, which have been designed and

tested, are presented. An array of 16 current sources is implemented for each trimmable current source design. In order to selectively program each floating-gate element, the CHEI and FNT programming circuits, described in Chapter 2, are also included in each current source.

The four designs use a floating-gate device in three distinct ways. The first architecture uses the floating-gate element as a trimmable current source. The next two designs use the floating-gate device as a trimmable voltage source to provide a trimming voltage to the current sources. The final design uses the floating-gate element in the linear operating mode to create a programmable resistor to trim the output current.

3.2 Trimmable current sources - TCS1

The most direct approach to creating a trimmable current source is to simply use a floating-gate transistor as the current source. The floating-gate device must therefore be programmed to a target accuracy and retain this level of accuracy throughout operation. However, a major concern about this design is the retention of charge on the floating-gate.

For a floating-gate MOSFET current source, the rate of change of output current from the floating-gate device is given by

$$\frac{\partial I_{out}}{\partial t} = g_m \frac{\partial V_{fg}}{\partial t} \quad (3.1)$$

where I_{out} is the trimmable output current, V_{fg} is the floating-gate voltage and g_m is defined as

$$g_m \approx \sqrt{2\mu_o C_{ox} \frac{W}{L} I_{out}} \quad (3.2)$$

where μ_o is the electron mobility and C_{ox} is the capacitance per unit area of the gate oxide. The rate of change of current can be minimised by either minimising g_m or the rate of change of floating-gate voltage. In order to minimise g_m the MOSFET width can be reduced. However, this will reduce the output current unless the overdrive voltage on the floating-gate is increased. The ability to increase this voltage is however limited by the need to keep the device in satura-

tion.

An alternative circuit, shown in Figure 3.1, which reduces the current through the floating-gate MOSFET whilst maintaining the overall output current level is proposed. This current source consists of three NMOS transistors. Two of the transistors are M2 and M3. M2 is a standard NMOS transistor with a bias voltage, V_{bias} , supplied by a bias generating circuit. M3 is a floating-gate NMOS transistor which provides a trimmable current. Both M2 and M3 are designed to operate in the saturation region so that neither transistors' output current is affected by any change in the drain-source voltage. In a high-speed DAC, the current source output is usually switched by a differential switch which minimises the transient switching glitches. However, in order to simplify the trimmable current source only a single transistor switch, M1, is implemented here.

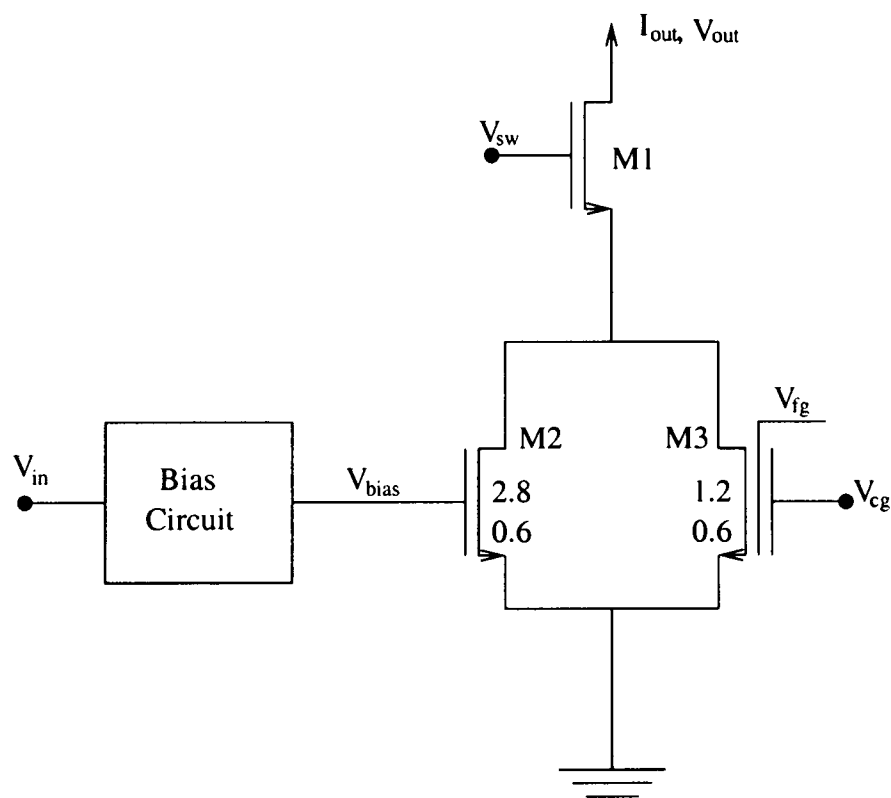


Figure 3.1: *TCS1 consists of two branches: A fixed output current (M2) and a trimmable output branch (M3). M1 is a simple single transistor switch.*

The source transistor of the current source requires a bias voltage which can be supplied by either an off-chip source or an on-chip biasing circuit. All of the implemented current sources are biased using an on-chip circuit shown in Figure 3.2. M4 in the circuit is used to convert the input voltage, V_{in} , into a current which is mirrored by 16 locally placed transistors such

as M6-M7. The transistors shown within the dotted box are all placed close to each other to minimise mismatch. The mirrored current is converted into a bias voltage for each current cell using transistors such as M8-M9. To minimise mismatch these transistors are local to each current cell. This approach is used to generate multiple copies of a bias voltage which are robust to large mismatches between widely separated transistors. The simulated relationship between V_{in} and V_{bias} is shown in Figure 3.3. As can be seen from this figure, the output voltage saturates at 2.7V. However, this does not limit the performance of the current source since higher bias voltages are not typically required because of the limited voltage headroom.

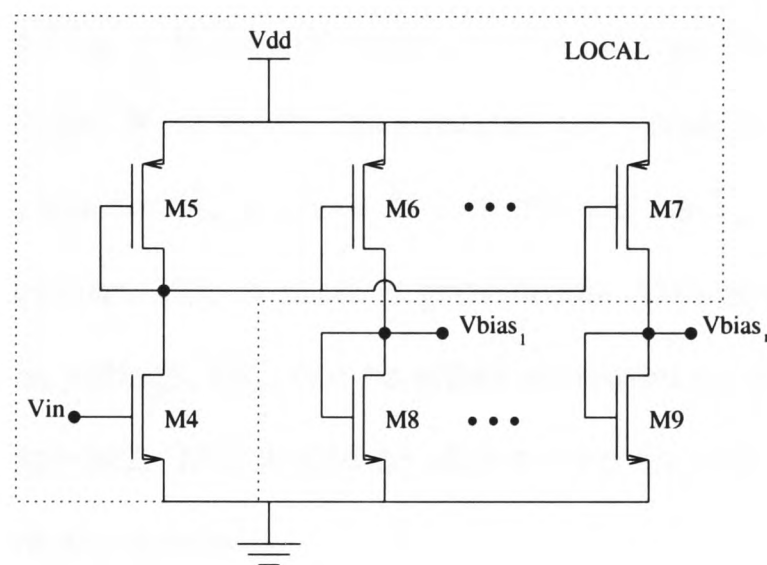


Figure 3.2: *Bias voltage generating circuit*

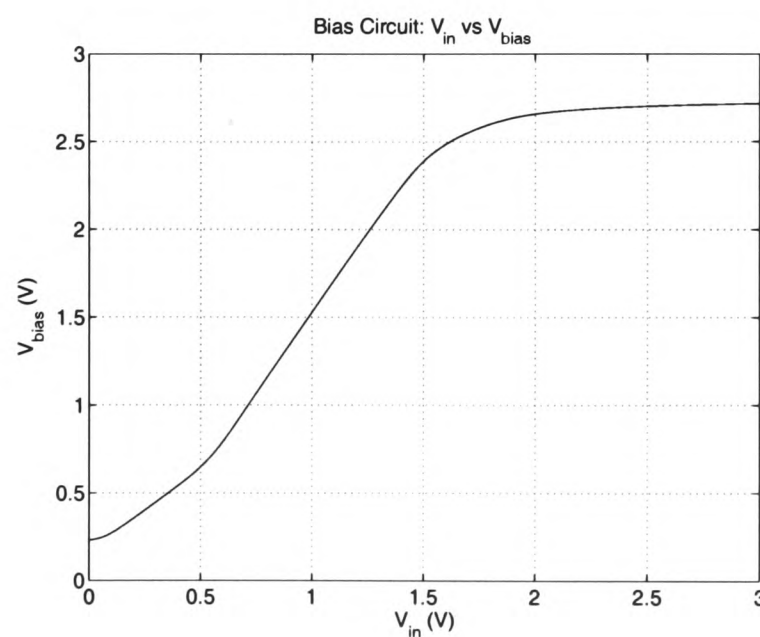


Figure 3.3: *Bias voltage circuit output: Simulation*

A typical current steering DAC has a full scale output current of 20mA. This gives a max-

imum output voltage swing of 1V when the current drives a 50Ω load. Therefore, the lowest voltage at the output node of each current source will be 2.3V when $V_{dd} = 3.3\text{V}$. Since the size of the transistor is no longer a mismatch determining factor, M2 can be of minimum length as long as it is able to give a suitable output current range. M2 is therefore designed to have an output range of up to $320\mu\text{A}$ which is a typical range for a 6-bit thermometer coded current source in a 12-bit segmented current steering DAC. Monte Carlo simulation results for the variation of the current through M2 due to mismatches for three bias conditions are shown in Figure 3.4. The mismatch data used during the simulation is supplied by AMS. When M2 is biased at a relatively low voltage ($V_{in} = 0.7\text{V}$) the mean current through the device is $51.4\mu\text{A}$ with a standard deviation of $3.3\mu\text{A} \equiv \frac{\sigma_I}{I} = 6.4\%$. As expected the standard deviation decreases with increasing bias voltage so that for $V_{in} = 1\text{V} \Rightarrow \frac{\sigma_I}{I} = 2.9\%$ and for $V_{in} = 1.5\text{V} \Rightarrow \frac{\sigma_I}{I} = 1.1\%$.

The floating-gate transistor, M3, is used to provide the trimming current for the current source. The trimming bias voltage, V_{fg} , can be either increased or decreased depending upon the current flowing through M2. M3 should be able to compensate for mismatches of up to $\pm 3\sigma$, which covers 99% of all variations.

The dimensions of M2 and M3, shown in Figure 3.1, have been chosen to give 70% and 30% of the total output current respectively when both transistors have similar bias conditions. These dimensions were chosen to meet the worst case requirements. For example, assume both, M2 and M3, are biased at the same but relatively low potential, say 0.7V. Then because of parameter variations, the fixed branch output current could be $1 + 3\sigma = 1.19$ times the expected value. This suggests that a split of 80:20 would be sufficient, however to be robust to ΔW variations between devices of different widths, the floating-gate device was designed to supply a larger fraction. If the output current is greater than expected, the trimming transistor bias can be reduced to achieve the desired current. Since the trimming branch is designed to supply 30% of the total current, it never completely switched off even after compensating for the worst case mismatch. If on the other hand, the total current is less than expected, the floating-gate voltage can be increased in order to increase the total current to the desired value. The amount by which the floating-gate voltage can be increased is limited to a voltage that ensures that the device

remains in saturation. Thus with this architecture both mismatch cases can be compensated for easily.

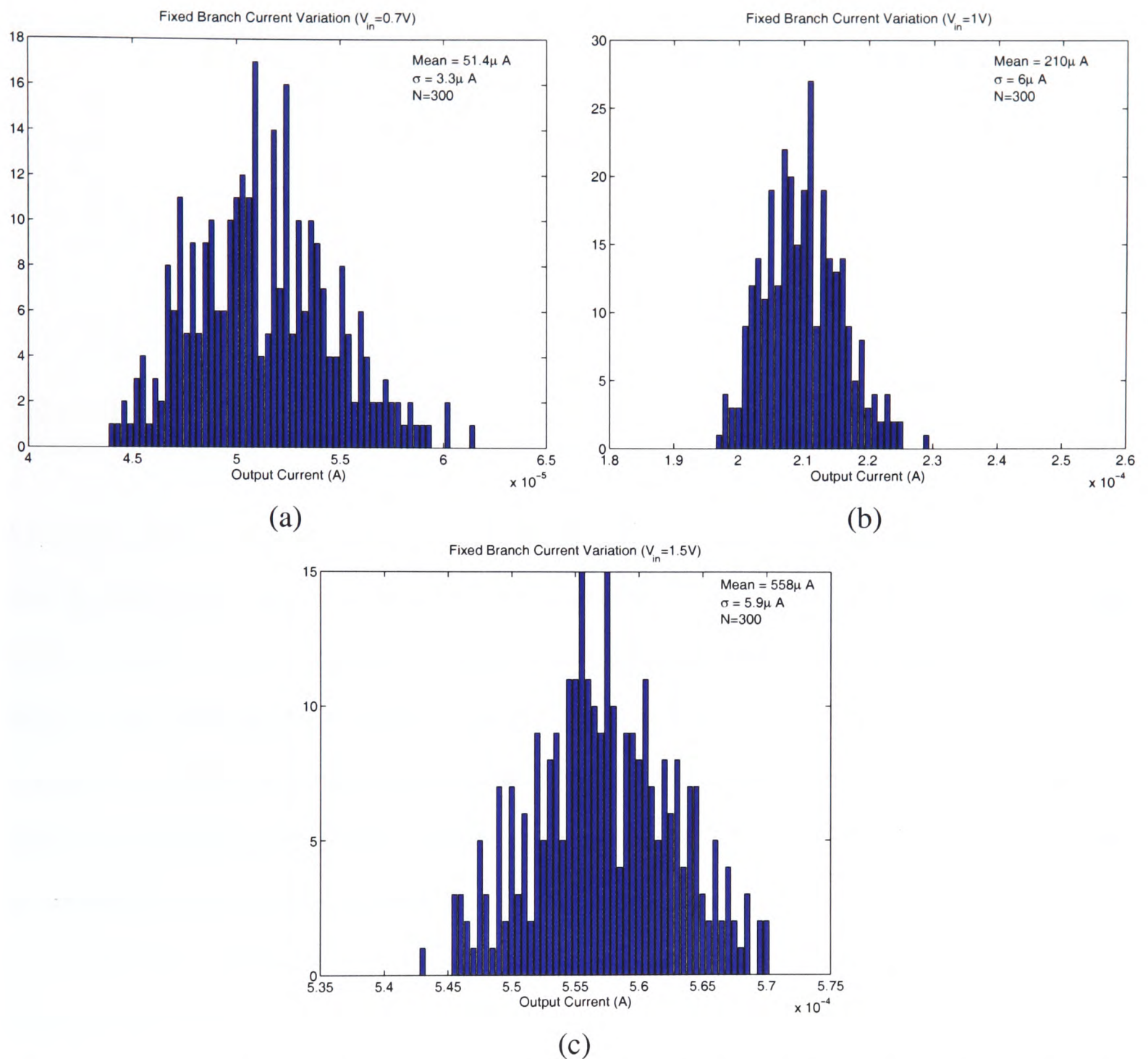


Figure 3.4: Monte Carlo simulation results for the variation of the current through M2 for $V_{in} = 0.7V$, $1V$ and $1.5V$. The simulations were done for 300 runs using the data supplied by AMS.

The functionality of the fixed branch is tested by measuring the total output current whilst sweeping the bias voltage, V_{in} , from 0V to 3.3V and holding V_{cg} at 0V and V_{out} at 2.3V. Both the simulation and experimental results, shown in Figure 3.5, confirm the increase in I_{out} with increasing V_{in} . Both results also show a saturation of the output current at $V_{in} \approx 2V$. When compared to the response of the bias generating circuit shown in Figure 3.3, it is clear that this effect is caused by the saturation of the output voltage from the bias circuit. There is a difference

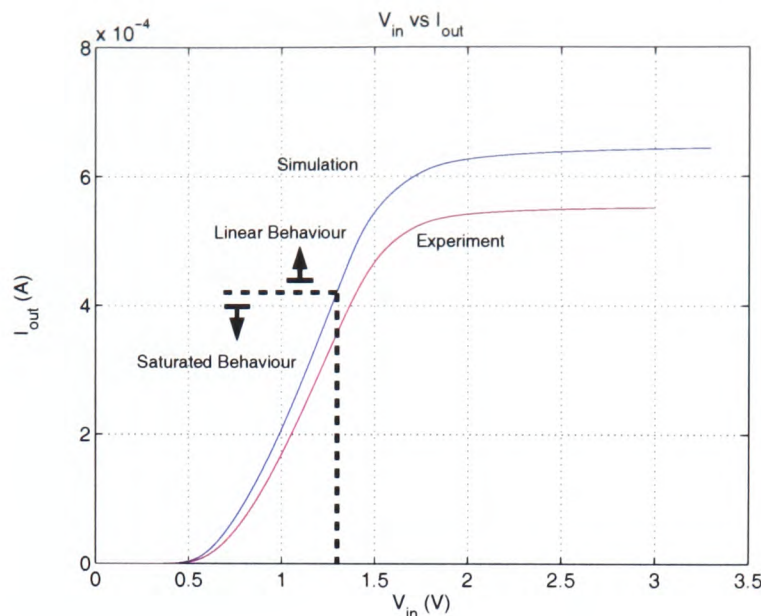


Figure 3.5: *TCS1 - Fixed branch output current vs Bias Voltage: Simulation and Measurement. The saturation of both curves at $V_{in} \approx 2.15V$ is due to the output response of the biasing circuit.*

of 15% between the simulation and measurement results in the saturated region. During simulations the transistor is modelled with typical parameters, however, these parameters vary significantly from one chip to another. These process variations affect only the absolute accuracy of output current and not the matching between transistors on the same die. If however, absolute accuracy is required, then the trimming range should be increased to reflect the increased mismatch due to process variations. Process mismatches are significantly larger than mismatches between neighbouring devices. Monte Carlo simulations of process variations found that with $V_{in} = 0.7V$, $\frac{\sigma_I}{I} = 50\%$ and with a bias of $V_{in} = 1.5V$, $\frac{\sigma_I}{I} = 9.7\%$. The difference between the measured and simulated results is therefore due to process variations.

The simulation results are also used to determine the operating regime of the source transistor. For M2 to remain saturated, the maximum input voltage, V_{in} , is 1.3V with a corresponding maximum output current of $430\mu A$. The maximum current range from the measured data for this bias range is $380\mu A$. Despite process variation the output range is acceptable for use in a segmented DAC.

The trimming range of the circuit is evaluated by first determining the saturation operating region of the floating-gate transistor. Since the drain voltage of the floating-gate transistor is not externally accessible, the circuit is simulated to determine the variation of the V_{ds} of M3 with V_{fg} . The simulation results, plotted in Figure 3.6, show the V_{ds} of the floating-gate transistor

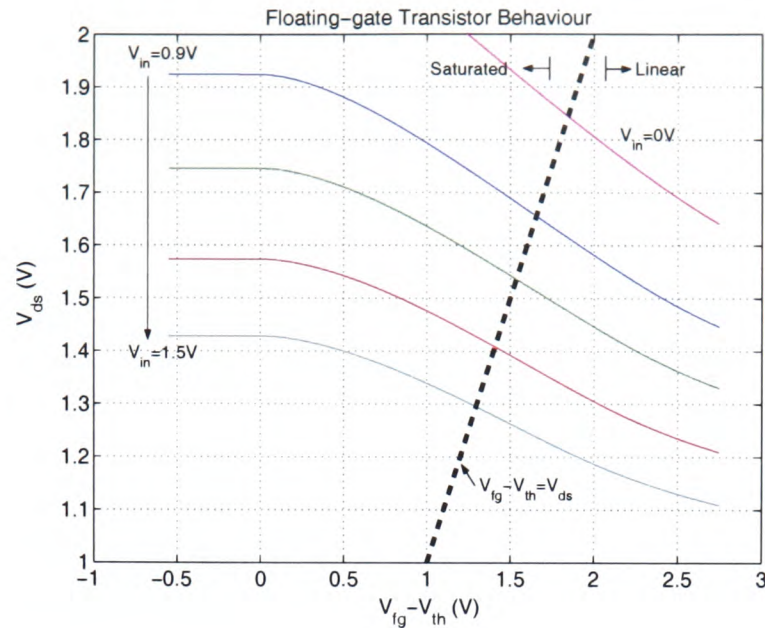


Figure 3.6: Simulated floating-gate voltage range for saturated operation. The linear and saturation operating regions are shown. For operation in the saturation region, V_{fg} should be less than 2.35V for all fixed branch bias voltages.

as a function of the floating-gate overdrive voltage, $V_{fg} - V_{th}$, for several fixed branch bias conditions. The two operating regions, saturated and linear, are marked on the figure with the $V_{fg} - V_{th} = V_{ds}$ line defining the boundary. The maximum floating-gate voltage to ensure saturated behaviour depends upon the fixed branch bias voltage which affects the drain node voltage of the floating-gate transistor. Figure 3.6 shows that the maximum V_{fg} ranges from 2.35V for $V_{in} = 0V$ to 1.8V when $V_{in} = 1.5V$.

The trimming branch current variation can be measured by varying the floating-gate voltage using either one of the two programming mechanisms (CHEI or FNT described in Chapter 2) or by using the control-gate node to capacitatively couple the control-gate voltage, V_{cg} , on to the floating-gate. For simplicity, the output current is measured by sweeping V_{cg} from 0V to 3V for several bias conditions. The measurement results plotted in Figure 3.7 show that, as expected, the total output current increases with an increase in V_{fg} as well as V_{in} . The initial output current for the $V_{in} = 0V$ curve is $4\mu A$ which suggests an initial floating-gate voltage of 0.7V for this particular current source.

The figure also shows the designed operating locus, $V_{bias} = V_{fg}$, of the circuit. Under this condition it is expected that the ratio of the currents from the fixed and trimmable branches will be 70:30. The current ratios are found to be : $V_{in} = 0.8V \Rightarrow I_{fix} = 70\mu A, I_{trim} =$

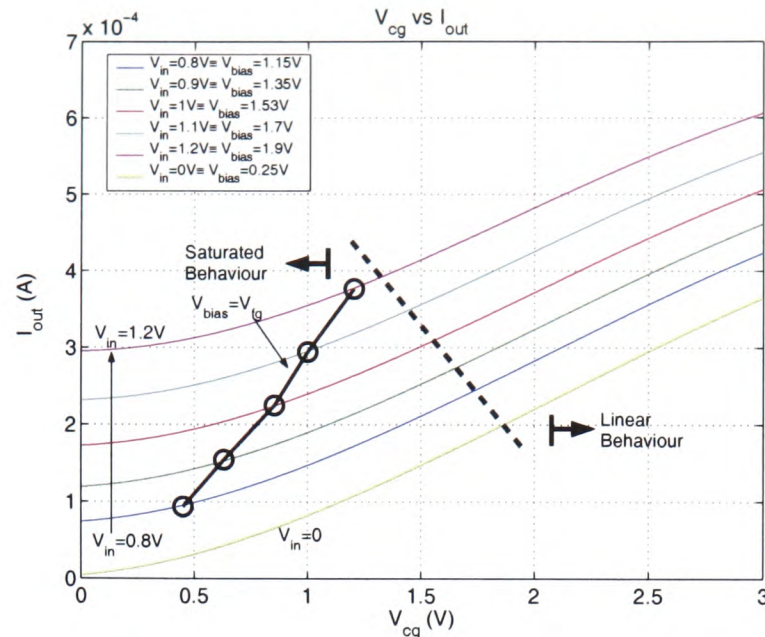


Figure 3.7: TCS1 - Control-Gate Voltage vs Output Current for various Bias Voltages: Measurement. Note the output current rises immediately at 0V. This is due to an initial positive voltage on the floating-gate.

$25\mu A$, Ratio = 74 : 26; $V_{in} = 1.2V \Rightarrow I_{fix} = 290\mu A$, $I_{trim} = 90\mu A$, Ratio = 76 : 24.

These ratios are different from the expected ratio of 70:30 because the ideal ratio is based upon the drawn dimensions of the source transistors and the floating-gate capacitor. The variation from the ideal ratio is due to ΔW variations of the transistors. In conventional design, this problem is overcome using multiple copies of the same geometry device. However, this increases circuit area and since the circuit can be trimmed after manufacture, this variation is not a problem for this circuit.

The trimming branch must be able to compensate for fixed branch currents which are both lower and higher than the expected value by either decreasing or increasing the floating-gate voltage. After trimming, both current source transistors must continue to operate in the saturation region. For low bias voltages on the fixed branch, this condition is met easily. For example, consider a transistor biased at $V_{in} = 0.8V$, which will have a worst case mismatch, $\pm 3\sigma$, of $\pm 17\%$. Therefore the trimming branch may be required to increase or decrease the total output current by up to $\pm 17\%$ of the mean fixed branch current. For this case, the required trimming range is $\pm 11\mu A$ which is smaller than the nominal trimming branch operating current, $32\mu A$, for this bias point. In fact as the output current can be decreased until the trimming branch is switched off and increased by $148\mu A$ until the trimming branch operating point reaches linear

region giving a trimmable range of $-32\mu\text{A}$ to $+148\mu\text{A}$. Therefore, I_{trim} can be easily decreased or increased by $11\mu\text{A}$.

As V_{in} increases, the mean operating trimming branch current moves closer to the saturation-linear operating boundary. Therefore, the amount by which this current can be increased is restricted. For example, the case of $V_{in} = 1.2\text{V}$, I_{trim} can be increased from its mean value of $90\mu\text{A}$ by only $12.5\mu\text{A}$ which is an increase of 4.3% relative to the mean fixed branch current of $290\mu\text{A}$. However, the required trimming range, determined from Monte Carlo simulations for this bias voltage, was found to be $\pm 6\%$. Therefore, if this bias voltage is used, the yield will be less than 99%. It is therefore suggested that bias voltages less than 1.2V ($V_{bias} < 1.9\text{V}$) are used for this current source. If these high bias voltages are required by a particular application then the geometry of the source and switch transistors can be modified to accommodate this requirement.

3.3 Trimmable current sources - TCS2

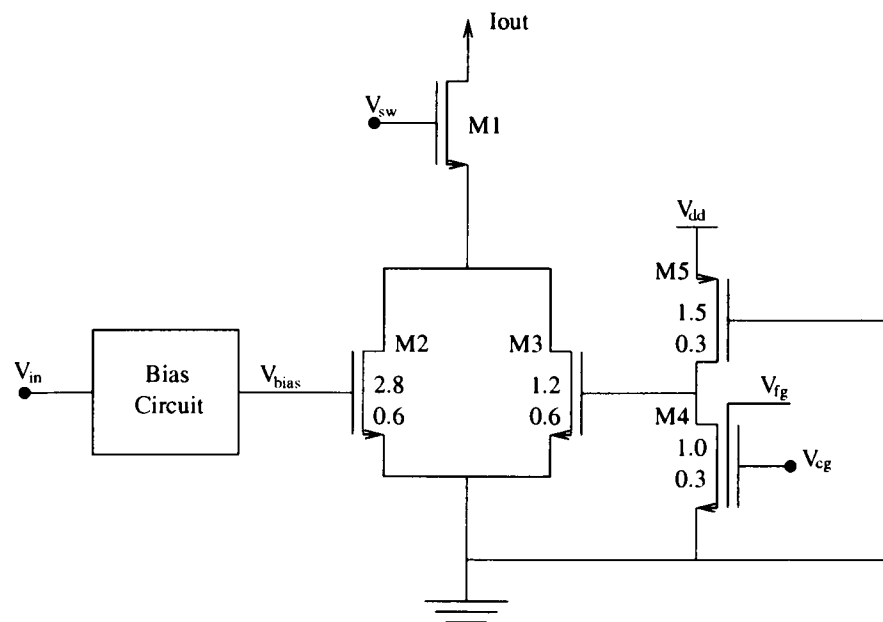


Figure 3.8: TCS2 consists of two branches: a fixed output current branch (M2) and a trimmable output current branch (M3). The trimmable branch source MOSFET is biased with a floating-gate inverter.

The programming speed of the trimmable branch of the previous circuit is limited to the programming speed of a single floating-gate transistor. This speed may not be sufficient for

some applications. If the current sources are to be programmed immediately after fabrication then a slow programming speed will increase the manufacturing cost by increasing the time required to trim a device after manufacture. In order to increase the programming speed, an alternative circuit could be used. This current source architecture, shown in Figure 3.8, also consists of two branches, a constant current output section, M2, and a trimmable output branch, M3. M2 is again biased with the biasing circuit shown in Figure 3.2. However in this circuit, M3 is a standard NMOS transistor which is biased by the voltage generated from the output of an inverter consisting of a floating-gate NMOS transistor, M4, and a PMOS transistor, M5. The rest of the inputs to the circuit, V_{sw} , V_{in} and V_{cg} are the same as in the previous circuit. The two current source transistors, M2 and M3 are again designed to operate in the saturation region with the total output current split 70% and 30% when both transistors have similar bias conditions.

The transfer characteristics of the inverter, shown in Figure 3.9(a), show that the circuit has a gain of 2 for input voltages between 2 and 2.5V. This ensures that the output current is more sensitive to changes in the floating-gate voltage compared with the previous circuit which therefore increases the programming speed of the floating-gate transistor.

Since the fixed branches of this circuit and TCS1 are the same, the transfer characteristics are expected to be the same. The simulated and measured trimmable output currents in Figure 3.9(b), show that as the floating-gate voltage increases the output current decreases. Both the experimental and simulated curves show good agreement in the saturation region. A noticeable difference is the mismatch at low floating-gate voltages which is due to non-typical process parameters for this chip-run. Process variations only affect the absolute accuracy of transistors. A slight relative shift in the measured curve is also observed due to an initial negative voltage of approximately 75mV on this particular floating-gate. Without an external connection to the drain of M3, the current range for which the trimming branch transistor remains saturated can only be estimated from simulation. The maximum bias voltage of the trimming branch transistor was estimated in the previous section to be 2.35V which corresponds to a minimum floating-gate voltage of 1.85V from Figure 3.9(a). Using this voltage range, the current range

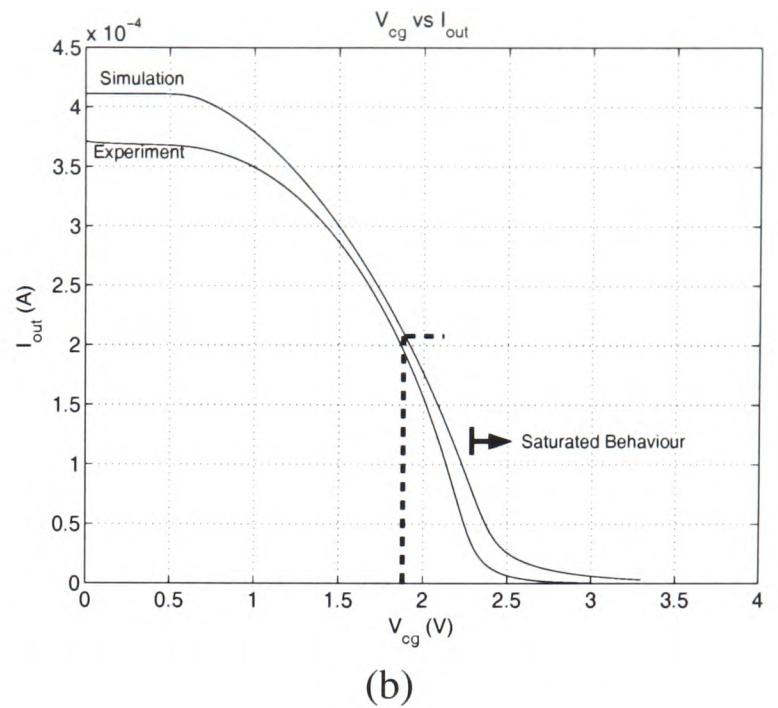
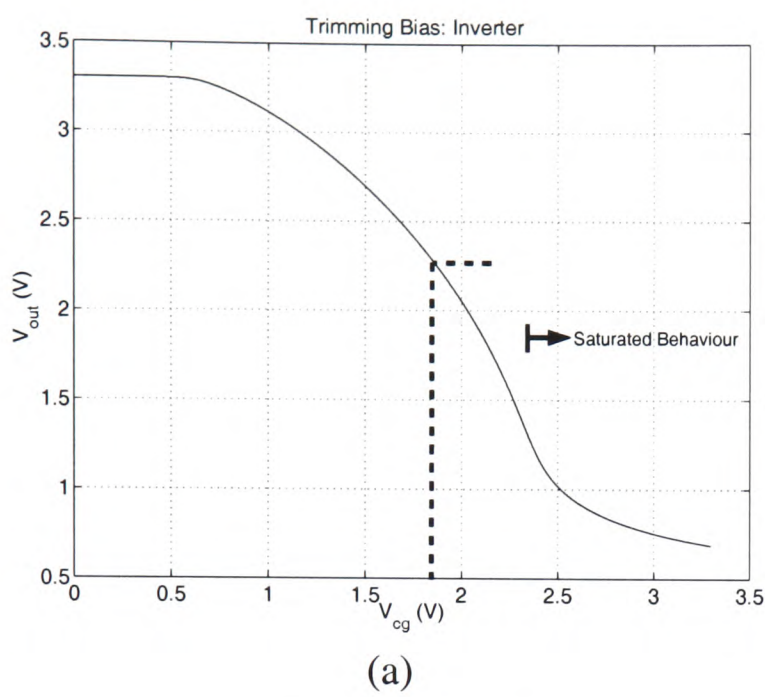


Figure 3.9: TCS2 - (a) shows the simulated inverter transfer characteristics. For the trimming branch to remain saturated the output voltage of the inverter is required to be less than 2.35V which therefore gives $V_{cg} > 1.85V$. (b) shows the measured and simulated output characteristics of the trimming branch with $V_{in} = 0V$. The simulated trimming range is found to 210 μA with the trimming transistor saturated and the fixed branch switched off. The corresponding range from the measured results is 200 μA .

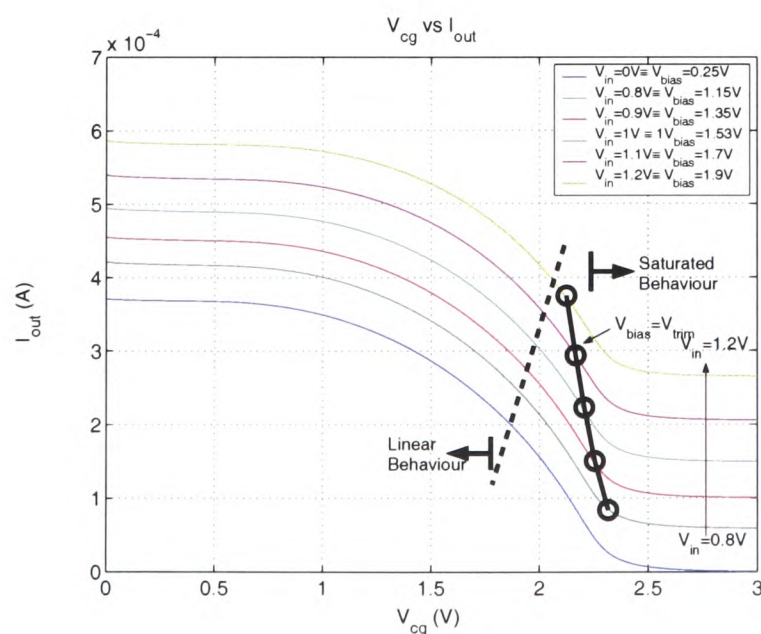


Figure 3.10: TCS2 - Measured trimmable branch output current variation with control-gate voltage for several fixed branch bias conditions. The saturation/linear region boundary is also shown together with the designed operating locus.

of the trimmable branch from the measurement results is found to be $200\mu\text{A}$ when the fixed branch bias is 0V . Figure 3.10 shows the measured trimmable branch response for several other fixed branch bias conditions. It can be seen from the results that the trimming range decreases as the fixed branch bias voltage increases because of the requirement to operate the trimmable branch in the saturation region. As the current flowing through the switch transistor increases, the common drain-source voltage of M2 and M3 decreases. The maximum gate voltage of M2 and M3 required to keep the devices in saturation also decreases.

For example the trimming range with $V_{in} = 0\text{V}$ is found to be $\Delta I_{trim} = 200\mu\text{A}$ compared with a range of $\Delta I_{trim} = 150\mu\text{A}$ with $V_{bias} = 1.2\text{V}$. When biased at $V_{in} = 1.2\text{V}$, the trimmable branch current can only be increased by $12\mu\text{A}$ from the designed operating point, which is not enough to compensate for mismatches. This trend is similar to that found for TCS1. For lower bias voltages, the trimming range is sufficient for mismatch compensation. Therefore this current source should be biased at voltages less than $V_{in} = 1.2\text{V}$.

In order to confirm the effect of the inverter gain on the output current, the gradient of the output response is determined. The average gradient of the measured curve between $V_{cg}=2.05\text{V}$ to 2.55V is found to be $290\mu\text{A/V}$ compared with a gradient of $140\mu\text{A/V}$ in the previous circuit (Figure 3.7) over the same bias range. This increased gradient, which is due to the gain of the inverter, will reduce the programming time of the floating-gate but also make the circuit more sensitive to charge loss.

3.4 Trimmable current sources - TCS3

The third trimmable current source, shown in Figure 3.11, uses an NMOS source follower circuit (a floating-gate NMOS, M4, and a standard NMOS, M5) to provide the bias voltage to the trimming transistor instead of the inverter used in TCS2. As before, M2 and M3 are designed to generate 70% and 30% of the total output current respectively with both transistors operating in the saturation region.

The source-follower is designed to have a gain less than unity in order to reduce the sensi-

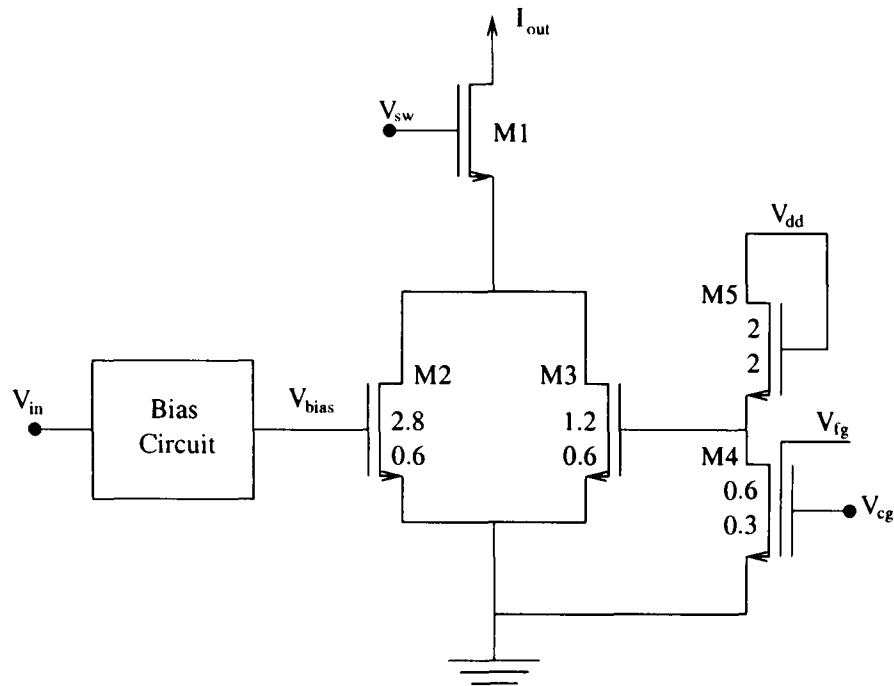


Figure 3.11: *TCS3 consists of two branches: a fixed output branch (M2) and a trimmable output branch (M3) which is biased with a floating-gate source-follower*

tivity to any charge loss from the floating-gate. This architecture therefore has the advantage of reducing the impact of long term charge loss, however, it has the disadvantage of a reduced programming speed of the floating-gate. Figure 3.12 compares the simulated output response of the source-follower with the response of the inverter from the previous circuit and a unity gain line. The difference in gain between the two circuits is clear from the figure. The gradient of the inverter response is 2 between $V_{cg}=2V$ to $2.5V$ whereas the gradient of the source-follower response is 0.5 between $V_{cg}=2V$ to $2.5V$.

The source-follower curve is used to determine the minimum floating-gate voltage required to ensure that the trimming branch transistor, M3, always operates in saturation. Since the bias voltage of M3 must always be less than $2.35V$, V_{fg} must be greater than $0.5V$.

The trimmable branch response is measured by sweeping V_{cg} from $-1V$ to $4V$ whilst monitoring the output current. As expected, both the simulation and measured results plotted in Figure 3.13(a) show that increasing V_{cg} , decreases the total output current. A shift in the measured curve is observed because of an initial positive voltage of $1V$ on the floating-gate transistor of this particular current source. At low control-gate voltages, the difference between the measurement and simulation results is again due to process variations. With $V_{in} = 0V$ and transistor M3 saturated, the maximum output current from the trimming branch is $210\mu A$. Figure 3.13(b)

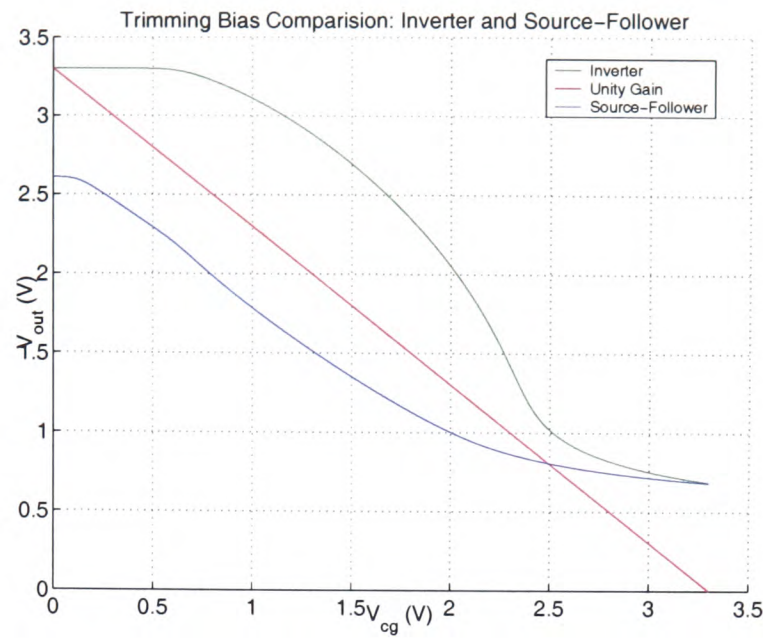


Figure 3.12: Comparison of the source-follower and inverter output responses. The inverter has a gain greater than unity compared with a gain of less than unity for the source-follower.

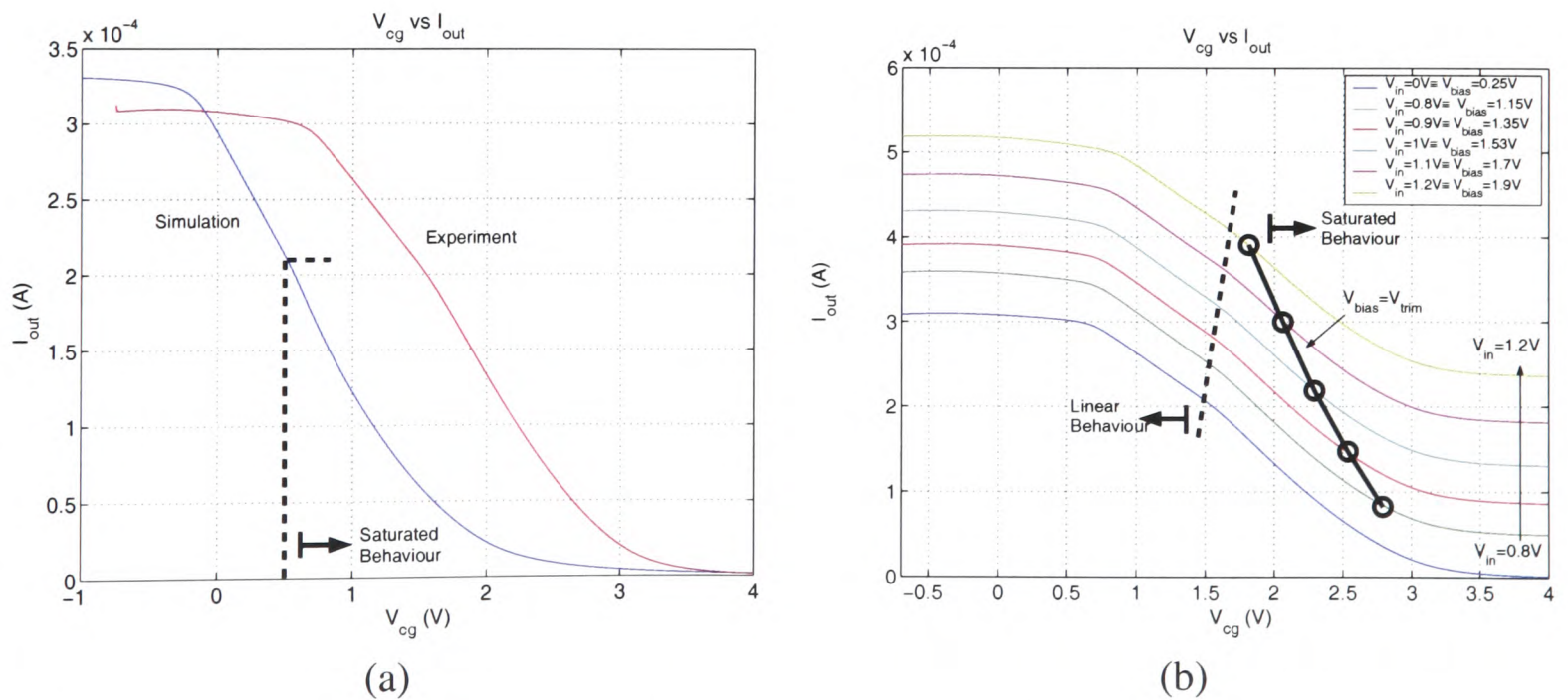


Figure 3.13: TCS3 - Control-gate voltage vs output current. (a) shows the simulated and measured response with the fixed branch switched off, $V_{in} = 0$. The positive shift of the measured plot is due to a positive voltage of approximately 1V on the floating-gate of the measured device. (b) shows the measured response for several fixed branch bias conditions together with the designed operating locus.

shows the measured response for several fixed branch bias conditions. The boundary between the saturation and linear operating regions is also plotted together with the designed operating points for each bias. Both of these loci occur at the same output currents as those found for the previous two designs. Therefore, the trimming range for this circuit is the same as TCS1 and TCS2 for all the fixed branch bias conditions shown.

The main difference between this and the previous circuits is the current gain. From the experimental data for $V_{in} = 0V$, the current gain between $V_{cg}=2.5V$ to $3.5V$ is $60\mu A/V$ compared with $140\mu A/V$ for TC1 and $290\mu A/V$ for TCS2 which suggests that TCS2 will have the fastest programming rate but TCS3 will be the least sensitive to any charge loss from the floating-gate.

3.5 Trimmable current sources - TCS4 and TCS5

The previous three architectures used a floating-gate device as a trimmable current source (TCS1) and as a trimmable bias source (TCS2, TCS3). Two other designs, TCS4 and TCS5, are based upon a circuit first proposed by Bugeja et al. [20, 94] and use the linear behaviour of MOSFETs to trim the output current. As in the original design in [94], TCS4, shown in Figure 3.14, consists of two parallel current sources, transistors M2 and M3 which are both biased with the same gate voltage. M4 is the trimming transistor which operates in the linear region. Bugeja first used off-chip potentiometers, to bias M4 in order to trim the output current, which was inconvenient [94]. A later design therefore relied upon constantly refreshing capacitors to hold the charge which was more convenient to the user but increased the complexity of the design and added to the power consumption of the system [20]. To avoid these problems, a floating-gate transistor based programmable voltage source can be used instead. In TCS4, M4 is thus biased with a trimmable floating-gate source-follower similar to that used in TCS3.

As shown in Figure 3.14 the two current source transistors in TCS4, M2 and M3, are the same size. However, for a specific V_{in} , the output current from each transistor will be different because the channel resistance of M4 modulates the source voltage of M3. As the floating-gate voltage increases, the bias voltage of M4 decreases and therefore its channel resistance

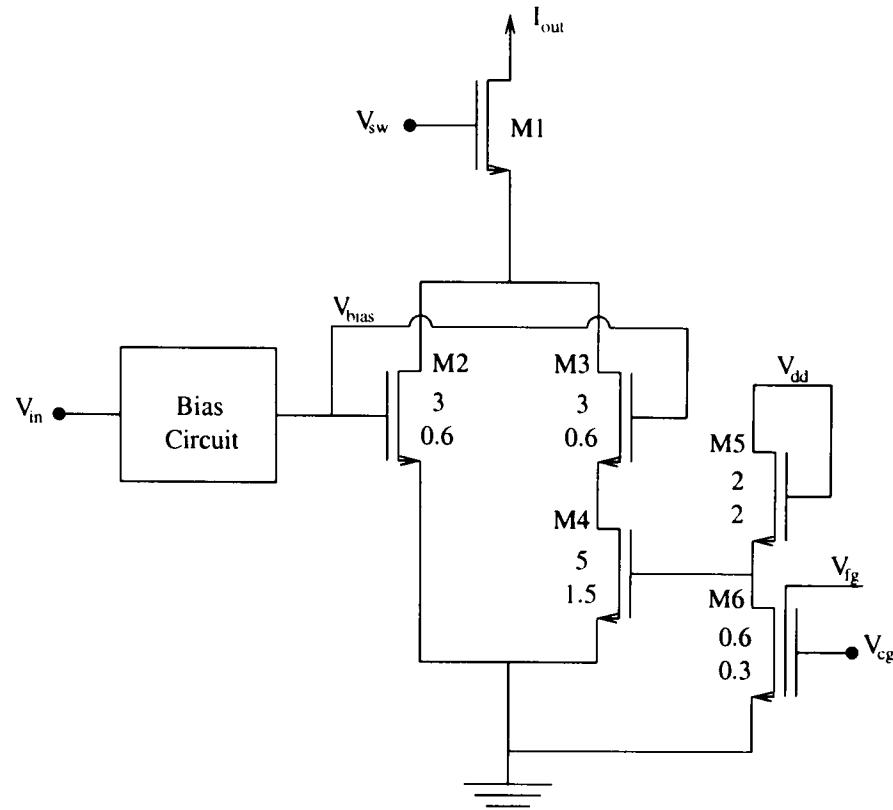


Figure 3.14: *TCS4 consists of fixed and trimmable output branches. M2 and M3 are biased at the voltage. M4 is a linear MOSFET which is used to modulate the trimmable branch current. A floating-gate source-follower is used to bias M4.*

increases. This increase in the resistance increases the source voltage of M3 which causes a reduction in the overdrive voltage of M3 and hence the output current. Ideally, when the channel resistance of M4 is zero, the current through M2 and M3 will be equal ($I_{M2} = I_{M3}$) and when the channel resistance tends towards infinity, $I_{M3} \Rightarrow 0A$. The current through M3, I_{M3} , can therefore be varied by simply changing the bias condition of the floating-gate transistor. Since M2 operates in saturation, its output current is not affected by changes in the trimming branch current which will change the current through M1 and hence modulate the drain voltage of M2.

An alternative mechanism to modulate the source voltage of M3 is to replace M4 with a floating-gate device. This alternative circuit, referred to as TCS5 and shown in Figure 3.15, has fewer transistors and is expected to consume less power than TCS4. TCS5 is therefore preferred over TCS4.

The measured variation of the output current of TCS5 with the control-gate voltage is shown in Figure 3.16(a) for several bias conditions ranging from 0.8V to 1.2V. As expected the data shows that the output current increases as V_{cg} (and V_{fg}) increases. However, the measured output current increases at $V_{cg} \approx 1V$ compared with $V_{cg}=0.5V$ in the simulated data, plotted in

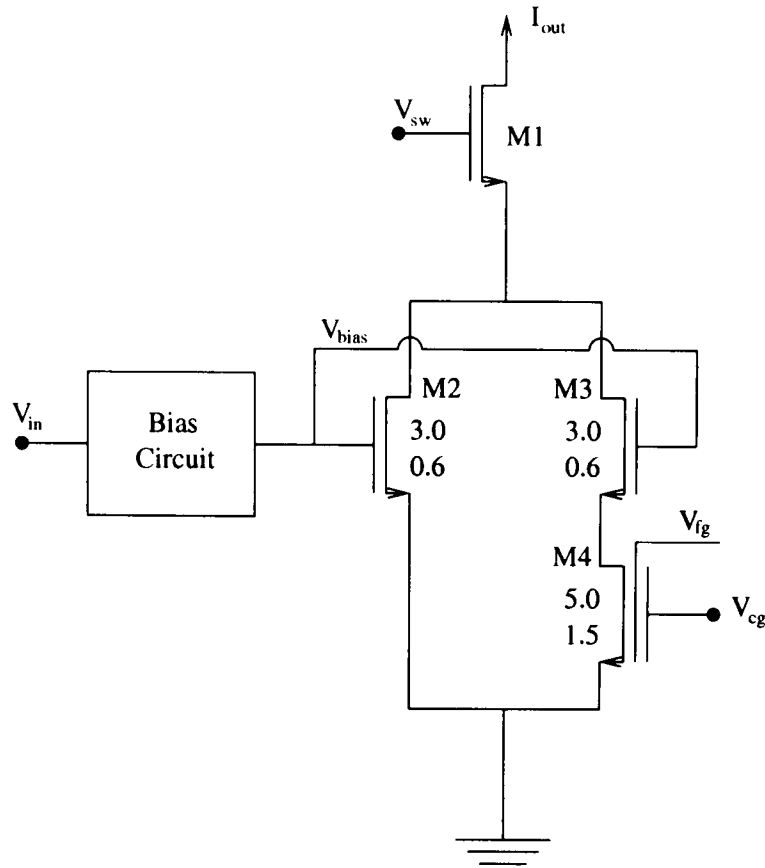


Figure 3.15: *TCS5 is a simplified version of TCS4. The linear MOSFET, M4, is a floating-gate NMOS which is used to modulate the trimmable branch output current.*

Figure 3.16(b). This discrepancy is due to an initial negative voltage of approximately 0.5V on the floating-gate. A comparison of the two sets of results shows that the absolute values of the current at various bias voltages are different. Again this is due to non-typical process parameters which can result in significant deviation from typical conditions. For example, variation of the output current from the fixed branch due to process variations is $\frac{\sigma_I}{I} = 33.6\%$ with $V_{in}=0.8V$ and $\frac{\sigma_I}{I} = 15.4\%$ with $V_{in}=1.2V$. The observed differences between the measured and simulated data fall within the $1 \pm 3\sigma$ boundary.

The boundary between saturation and linear regions of the floating-gate transistor, drawn in Figure 3.16(b), is used to determine the trimming range of the circuit. At a bias of 0.8V the output current can be trimmed from $110\mu A$ to $166\mu A$ which is a range of 51%. When biased at 1.2V, the trimming range is reduced to 35%. This reduction in the trimming range is due to an increase in the minimum floating-gate voltage required for linear behaviour. However, this reduction does not affect the trimming capability of the current source since the mismatches are lower at the higher bias voltages.

The programming rate of this current source is likely to depend upon the bias voltage, V_{in} .

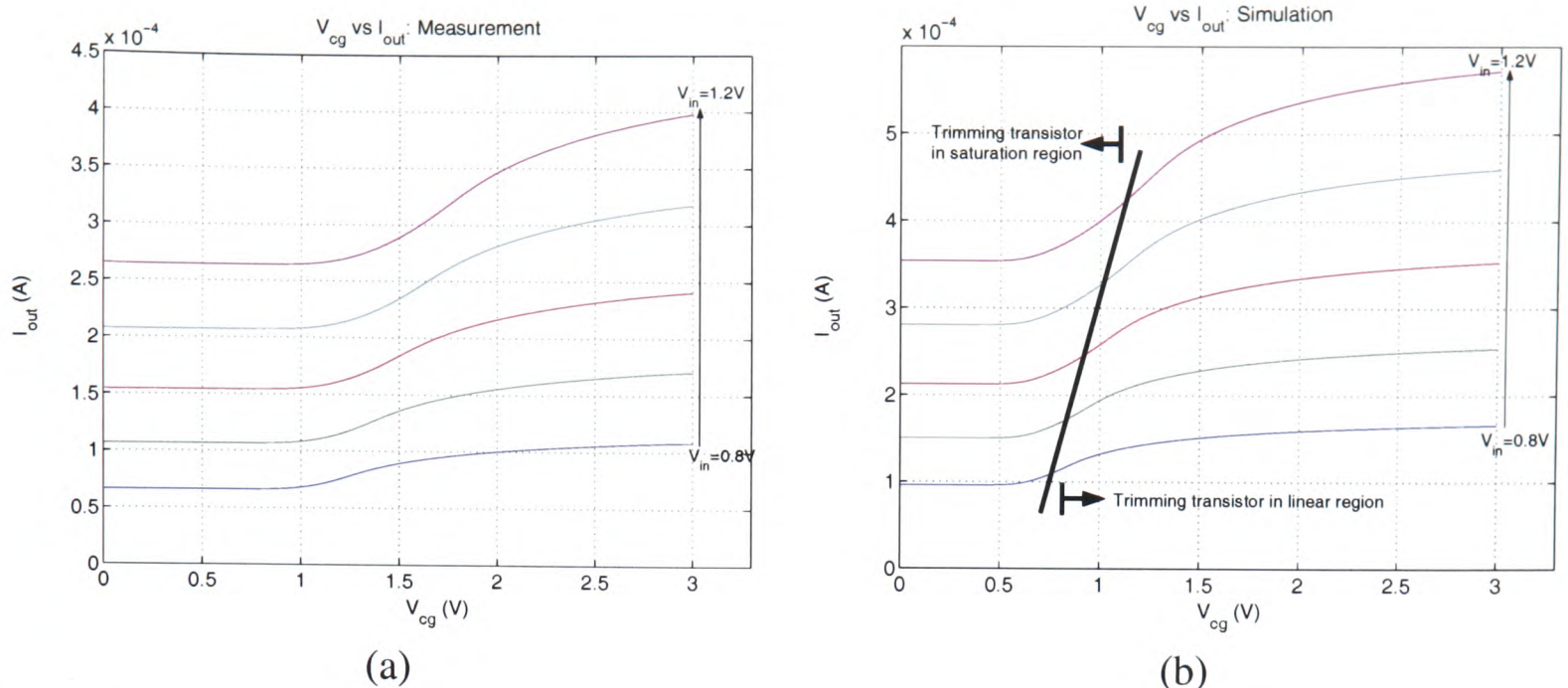


Figure 3.16: *TCS5 Control-gate voltage vs output current for several bias voltages. (a) shows the measurement results. The output current begins to increase at $V_{cg} \approx 1V$. This suggests that the floating-gate has an initial negative voltage of approximately 0.5V. The simulation results plotted in (b) shows the simulated linear and saturation operating regions of the trimming transistor, M4.*

The current gain from approximately, $75\mu A/V$ at $V_{in} = 0.8V$ to $100\mu A/V$ at $V_{in} = 1.2V$. Therefore the programming rate of this current source is expected to be in between the programming rates of TCS1 and TCS3.

3.6 Comparison of Retention Characteristics

All the current sources were designed prior to knowing any retention characteristics for this process. It was concluded in Chapter 2, that the retention of charge on the floating-gate during normal operation depends critically upon the bias conditions of the sense transistor. Floating-gate charge loss has been observed with V_{ds} as low as 1V. In addition, Ghetti et. al [90] predict charge loss for V_{ds} lower than 1V.

In TCS1, the V_{ds} of the sense transistor is in the range of 1.5V to 2V. Based on the results of Chapter 2, it can be predicted that the floating-gate device in the current source will suffer from electron injection from the sense transistor. These electrons gain their energy through carrier-carrier interactions in the sense MOSFET channel. This current source is therefore not ideal for applications which require matched current sources over a long time.

The V_{ds} of the sense MOSFET in TCS2 is always less than 2.35V in order to ensure that the trimming branch MOSFET always operates in saturation. However, depending upon the floating-gate voltage, the V_{ds} can be set to less than 1V. At this voltage, the charge loss is significantly reduced. However, this advantage may be offset by the increased sensitivity of the output current to any change in the floating-gate voltage due to the gain of the trimming inverter.

The sense MOSFET in TCS3 has a similar V_{ds} range to the MOSFET in TCS2. Using the floating-gate voltage, V_{ds} can also be set to less than 1V. However, an advantage of this current source over TCS2 is that the gain of the source-follower is approximately a fifth of that found for the inverter. This means that with similar drain-source conditions, the floating-gate in TCS3 will retain charge five times as long as the TCS2 floating-gate.

To determine the charge retention ability of the linear mode floating-gate device in TCS5, it is necessary to determine the variation of its V_{ds} with V_{fg} . The results, plotted in Figure 3.17, show that the maximum V_{ds} of the floating-gate transistor is 0.5V for bias voltages (V_{in}) between 0.9V and 1.5V. The floating-gate transistor of this circuit thus operates with a much lower V_{ds} compared with the other designs (TCS1-TCS3). This circuit will be able to retain the programmed voltage for significantly longer times than the other circuits.

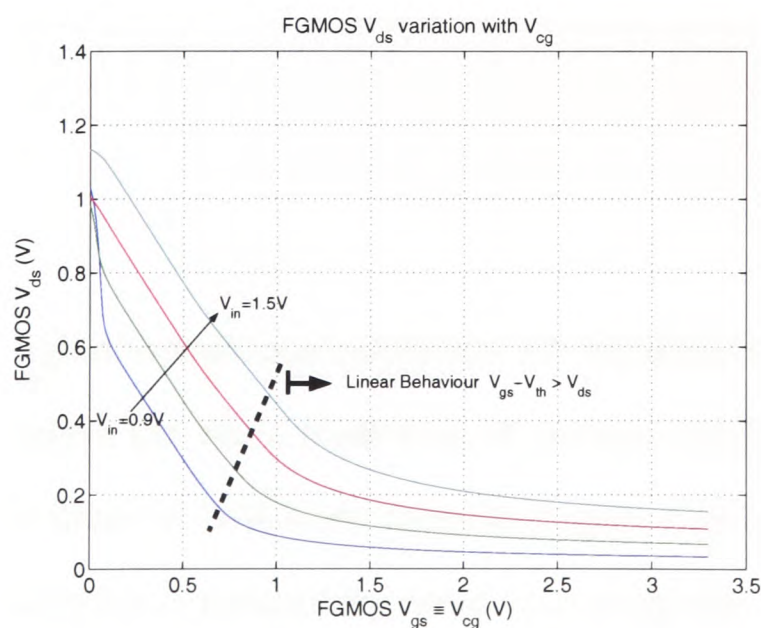


Figure 3.17: TCS5 Simulated floating-gate transistor V_{ds} variation with V_{cg} . When the transistor is in linear operation, the V_{ds} is below 0.5V for all bias voltages (V_{in}) between 0.9V and 1.5V.

To confirm the charge retention capability of this circuit, the output current was measured

for approximately 7 days. The experimental time was limited by the measurement instruments. The results, plotted in Figure 3.18, show that with the circuit biased at around 0.9V, the output current remains at a mean value of $141.5\mu\text{A}$ for the entire measurement period. These results confirm that TCS5 has the best charge retention capability compared with the other current sources. However, it can also be seen that the output current suffers from oscillations with a period of approximately 1 day. This variation is attributed to the oscillation of the operating temperature.

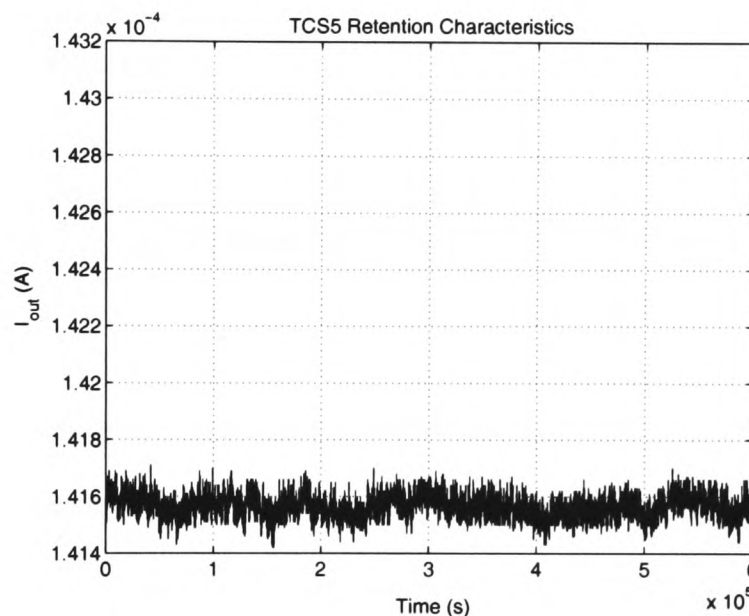


Figure 3.18: *Retention characteristics of TCS5 at an arbitrary output current.*

3.7 Conclusion

Current sources used in digital to analogue converters are required to meet strict matching requirements in order to achieve the static resolution of current steering DACs. The matching properties of the current sources in DACs are dependent upon their bias conditions as well as the devices sizes. This mismatch is reduced by either increasing the bias voltage, which introduces voltage head room problems, or by increasing the device size, which increases the area cost. Further constraints are introduced by parameter variations caused by oxide thickness variations, mechanical stress and temperature gradients across the die. The effect of these variations can be minimised by using complex and time consuming common-centroid layout schemes. To

avoid these issues, trimmable current sources based on floating-gate device technology have been designed and tested.

The designed current sources use a floating-gate in three distinct ways: a programmable current source, a programmable voltage source and a programmable resistor. Table 3.1 summarises the characteristics of the four current sources.

Current Source	Floating-gate Mode	Programming Speed	Retention Characteristics
TCS1	Current Source	2	4
TCS2	Voltage Source	1	3
TCS3	Voltage Source	4	2
TCS5	Resistor	3	1

Table 3.1: *Summary of the characteristics of the current sources. The relative scores shown for the programming speed and charge retention range from 1 for the best current source to 4 for the worst one.*

TCS1, is a two branched circuit consisting of fixed and trimmable output current branches which are designed to supply 70% and 30% of the total output current respectively. The trimmable branch consists of a floating-gate MOSFET which acts as a programmable current source. The floating-gate voltage can be increased or decreased using either FNT or CHEI as described in Chapter 2. However, the programming rate is limited to the injection rate of the floating-gate device itself. The trimming range of this current source is sufficient to correct mismatches for bias voltages of up to $V_{in} = 1.2V \equiv V_{bias} = 1.8V$ which is sufficient to correct for any mismatches. With this bias range, the V_{ds} on the floating-gate device is between 1.5V and 2.3V which is likely to cause charge loss from the floating-gate during normal operation.

TCS2 uses a floating-gate based inverter to bias the trimming transistor. The trimming range of this current source is the same as TCS1. With the gain of the inverter greater than unity, an increased programming speed is expected from this circuit. One of the benefits of this increased speed is a lower manufacturing cost since more devices can now be programmed within a specific time. This circuit also has a lower V_{ds} on the floating-gate compared with TCS1 which can lead to better charge retention characteristics. However, one of the disadvantages of a faster programming time is an increased sensitivity to charge loss which can negate the

advantage of a lower operating V_{ds} .

TCS3 uses a floating-gate source-follower to bias the trimming branch MOSFET instead of the inverter used in TCS2. The source-follower has a gain of less than unity which reduces the sensitivity of the output current to changes in the floating-gate voltage. One of the expected benefits of this circuit is likely to be an improved retention period during normal operation compared with TCS1 and TCS2 if the floating-gate MOSFETs of the current sources have the same V_{ds} .

The final current source described, TCS5, is based upon a circuit first proposed by Bugeja et al. [94]. It uses a floating-gate MOSFET in the linear region of operation to modulate the source voltage of a saturated MOSFET to generate the trimming branch current. The trimming range of this circuit is between 35% to 51% depending upon the bias conditions. This is a sufficient range to correct for any mismatches. Since the floating-gate device is operating in the linear region, the V_{ds} of the device is less than 0.5V. Retention results of this current source have shown that the floating-gate device does not suffer from charge loss over a period of at least 7 days. However, it is also clear from these results that a variation in the output current due to temperature variations is larger than any change in the output current due to charge loss. Therefore, the effect of temperature variations on these current sources must be investigated.

Chapter 4

Temperature Effects

4.1 Introduction

The recent trend towards integration of complete systems on a single chip has forced designers to analyse the effects of temperature gradients caused by components with a large power dissipation [95, 96]. For example, a communications system will contain large power devices, such as power amplifiers, that dissipate enough power to create temperature gradients that can affect the performance of a matched array of current sources in a DAC. These temperature gradients make accurate analogue design challenging. Particularly, when the power dissipation and therefore the temperature gradients may be time dependent.

The aim is to develop a trimmable current source that can be trimmed after manufacture. Temperature gradients across an array of current sources can affect the relative accuracy of the output currents which leads to a deterioration in the performance of the DAC. If the trimmable current sources are to be used in large integrated systems then it is important to understand the effect of temperature on each of the four trimmable current sources.

The basis of all the current sources is a MOSFET. The effect of temperature on a MOSFET has been well understood [97]. In particular, Filanovsky et al. [98, 99] has highlighted the fact that there is an operating region in a saturated MOSFET on some processes where the output current is independent of temperature. The exact bias conditions required to achieve this region

are technology dependent. Therefore, this chapter begins with an analysis of the first order MOSFET temperature model. The conditions required to achieve the temperature independent output current are identified for the $0.35\mu m$ technology. These are then used to determine the stability of this operating region to variations in the bias conditions. Finally, these models are then used to explain the temperature response of the current sources.

4.2 MOSFET Temperature Model

In saturation, the first order model of the drain current in a transistor is given by

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_{th})^2 \quad (4.1)$$

$$\beta = \mu C_{ox} \frac{W}{L} \quad (4.2)$$

where V_{gs} is the gate-source voltage, V_{th} is the threshold voltage, μ is the effective mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of the transistor respectively. Assuming both V_{th} and β are temperature dependent, the variation of I_{ds} due to temperature is therefore given by [97]

$$\frac{\partial I_{ds}}{\partial T} = \frac{1}{2} \frac{\partial \beta}{\partial T} (V_{gs} - V_{th})^2 - \beta \frac{\partial V_{th}}{\partial T} (V_{gs} - V_{th}) \quad (4.3)$$

The temperature dependence of the threshold voltage at an arbitrary temperature T is [97]

$$V_{th} = V_{th0} + \alpha_{vt}(T - T_0) \quad (4.4)$$

where V_{th0} is the threshold voltage at a reference temperature T_0 and α_{vt} is the process dependent threshold voltage temperature coefficient. Simulation results for threshold voltage variation with temperature for NMOS and PMOS transistors for the $0.35\mu m$ process are plotted in Figure 4.1. From the gradient of the two curves, the threshold voltage temperature coefficient, α_{vt} , for this $0.35\mu m$ process, is found to be $-1.1\text{mV}/^\circ\text{C}$ and $1.9\text{mV}/^\circ\text{C}$ for NMOS and PMOS

transistors respectively.

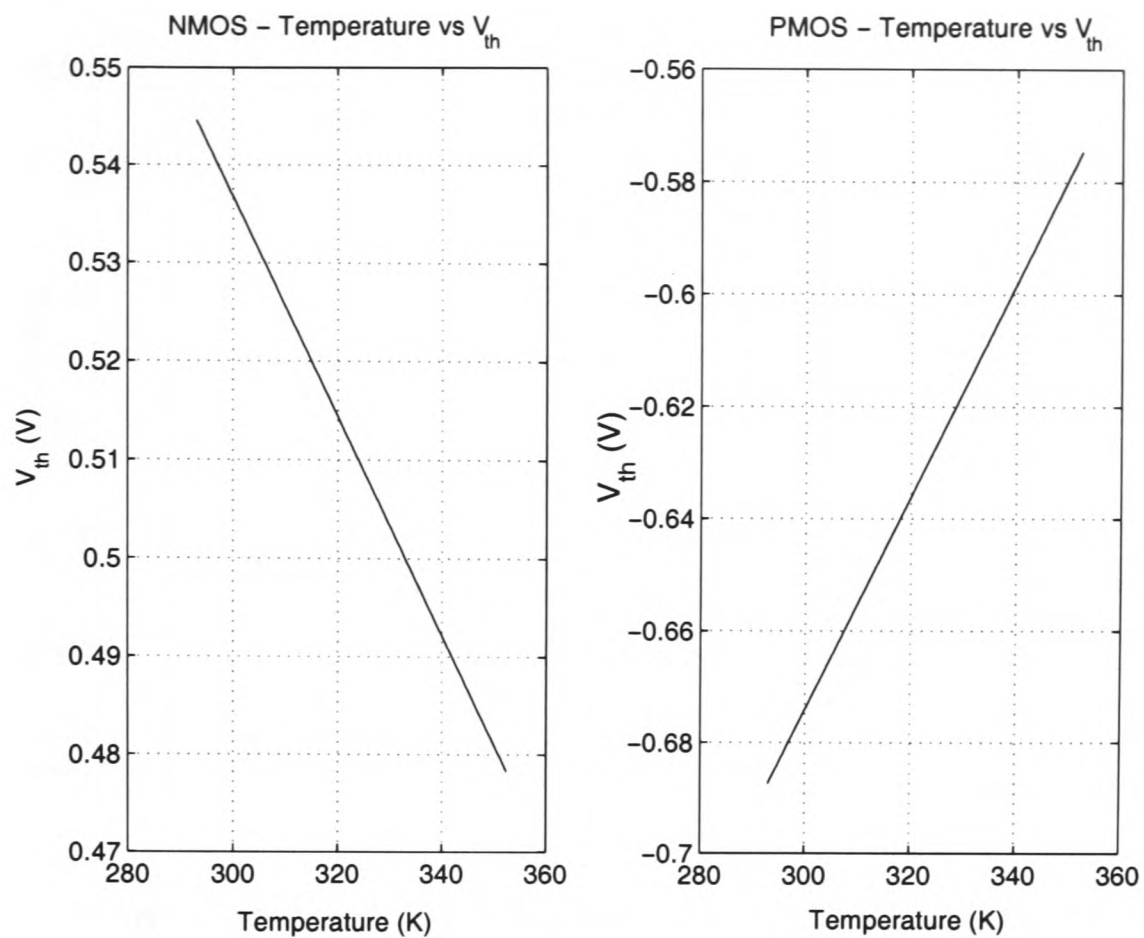


Figure 4.1: *Threshold voltage variation with Temperature, $T_0 = 293K$ - NMOS and PMOS*

The temperature dependence of β arises from the temperature dependence of the mobility [97], hence

$$\mu = \mu_0 \left(\frac{T}{T_0} \right)^{\alpha_\mu} \quad (4.5)$$

$$\beta = \mu_0 C_{ox} \frac{W}{L} \left(\frac{T}{T_0} \right)^{\alpha_\mu} \quad (4.6)$$

where μ_0 is the carrier mobility at temperature T_0 and α_μ is the process dependent mobility temperature exponent. Simulation results showing the variation of β with temperature are shown in Figure 4.2 for NMOS and PMOS transistors. The gradient of this data has been used to extract the mobility exponent, α_μ for this $0.35\mu m$ process. For NMOS transistors the exponent is found to be -1.8 whilst for PMOS transistors, $\alpha_u = -1.29$.

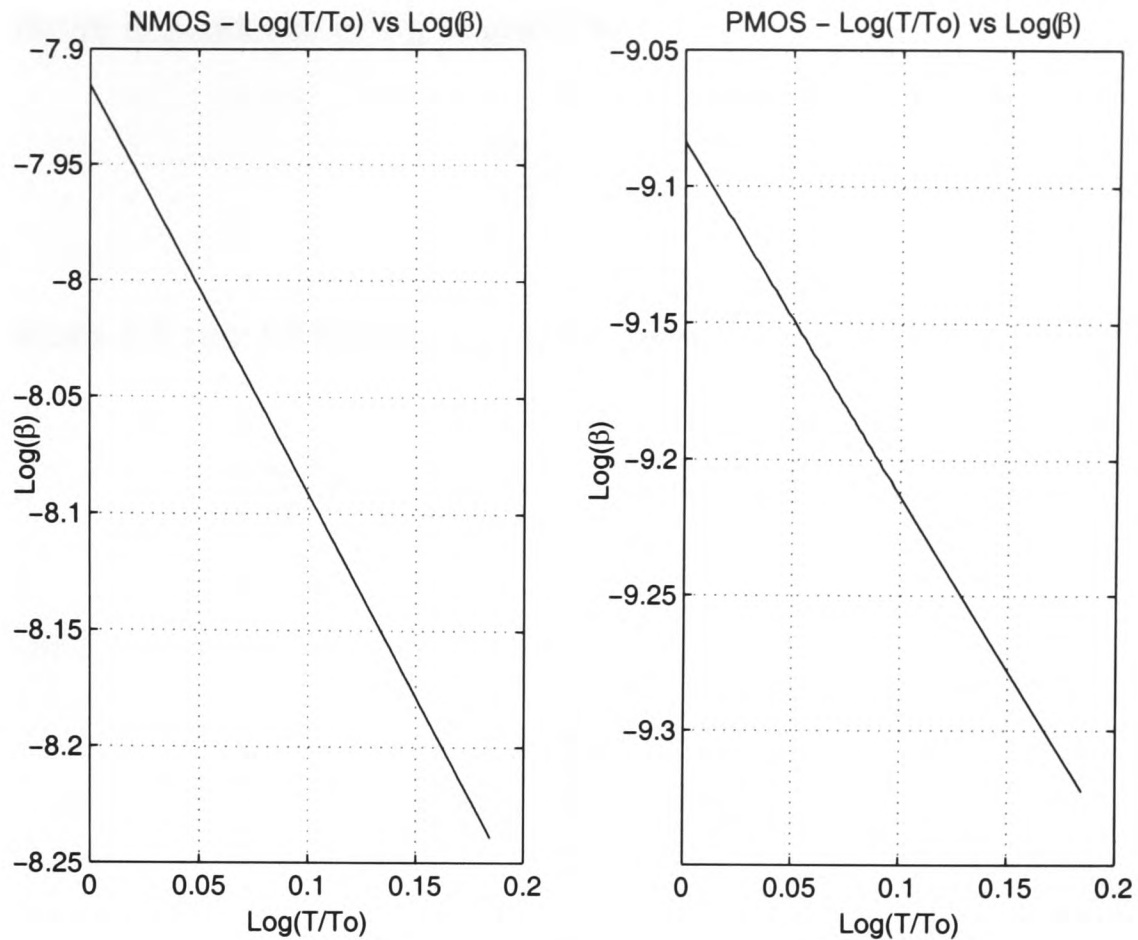


Figure 4.2: *Beta variation with Temperature, $T_0 = 293K$, NMOS and PMOS*

4.2.1 Zero Temperature Coefficient Point

Once a current source in a DAC has been trimmed to a specific current after manufacture, it can still suffer from mismatches due to temperature gradients arising during operation. It is therefore desirable to bias the current source at a point which minimises the effect of these temperature variations. This bias point, known as a zero temperature coefficient (ZTC) point, can be determined analytically for a MOSFET.

For a ZTC point to exist, $\frac{\partial I_{ds}}{\partial T} = 0$, therefore Equation 4.3 becomes

$$\frac{1}{2} \frac{\partial \beta}{\partial T} (V_{gs} - V_{th})^2 - \beta \frac{\partial V_{th}}{\partial T} (V_{gs} - V_{th}) = 0 \quad (4.7)$$

The temperature dependence of β is given by differentiating Equation 4.6 with respect to T

$$\frac{\partial \beta}{\partial T} = \mu_0 C_{ox} \frac{W}{L} \frac{\alpha_\mu}{T_0} \left(\frac{T}{T_0} \right)^{\alpha_\mu - 1} = \frac{\alpha_\mu \beta}{T} \quad (4.8)$$

and the temperature dependence of V_{th} is given by

$$\frac{\partial V_{th}}{\partial T} = \alpha_{vt} \quad (4.9)$$

Inserting Equations 4.8 and 4.9 into Equation 4.7 gives

$$\frac{1}{2} \frac{\alpha_u \beta}{T} (V_{gs} - V_{th})^2 - \beta \alpha_{vt} (V_{gs} - V_{th}) = 0 \quad (4.10)$$

which reduces to

$$\frac{\alpha_\mu}{2T} (V_{gs} - V_{th}) = \alpha_{vt} \quad (4.11)$$

The ZTC gate voltage, $V_{gs|ZTC}$, is then determined by substituting Equation 4.4 into Equation 4.11 to give

$$\begin{aligned} V_{gs|ZTC} &= V_{th0} + \alpha_{vt}(T - T_0) + \frac{2T\alpha_{vt}}{\alpha_\mu} \\ &= V_{th0} + \alpha_{vt} \left[T \left(1 + \frac{2}{\alpha_\mu} \right) - T_0 \right] \end{aligned} \quad (4.12)$$

The corresponding ZTC drain-source current, $I_{ds|ZTC}$, is therefore give by

$$\begin{aligned} I_{ds|ZTC} &= 2\beta \left(\frac{\alpha_{vt}T}{\alpha_\mu} \right)^2 \\ &= 2\mu_0 C_{ox} \frac{W}{L} \left(\frac{T}{T_0} \right)^{\alpha_\mu} \left(\frac{\alpha_{vt}T}{\alpha_\mu} \right)^2 \\ &= 2\mu_0 C_{ox} \frac{W}{L} \left(\frac{\alpha_{vt}}{\alpha_\mu} \right)^2 \frac{T^{\alpha_\mu+2}}{T_0^{\alpha_\mu}} \end{aligned} \quad (4.13)$$

It has been previously highlighted [98, 99] that if $\alpha_u = -2$, then the predicted $V_{gs|ZTC}$ and

NMOS Parameters	Value
C_{ox}	$4.604 \times 10^{-3} \text{Fm}^{-2}$
α_{vt}	$-1.1 \text{mV}/^\circ\text{C}$
α_μ	-1.8
μ_0	$0.0385 \text{m}^2/\text{Vs}$
Drawn W	$4 \mu\text{m}$
Drawn L	$1.2 \mu\text{m}$
T_0	300K

Table 4.1: $0.35 \mu\text{m}$ Technology Parameters

$I_{ds|ZTC}$ values are

$$V_{gs|ZTC} = V_{th0} - \alpha_{vt}T_0 \quad (4.14)$$

$$I_{ds|ZTC} = \frac{\mu_0 C_{ox}}{2} \frac{W}{L} (\alpha_{vt}T_0)^2 \quad (4.15)$$

Thus when $\alpha_\mu = -2$, the ZTC gate voltage and current shows no temperature dependence and therefore a single ZTC point exists for all temperatures. For the $0.35 \mu\text{m}$ technology used, the NMOS mobility exponent (-1.8) is close to the ideal value (-2). The NMOS devices are expected to be less temperature dependent around the ZTC point compared with PMOS devices and therefore further discussion is limited to NMOS devices.

Using the NMOS parameters summarised in Table 4.1, $V_{gs|ZTC}$ and $I_{ds|ZTC}$ for the devices are

$$V_{gs|ZTC} = 0.862 + 122 \times 10^{-6}T \quad (4.16)$$

$$I_{ds|ZTC} = 12.69 \times 10^{-6}T^{0.2} \quad (4.17)$$

This ZTC point is dependent upon the device width and length. As expected, both of the above expressions show slight temperature dependence. By substituting the temperature models of V_{th} and β into Equation 4.1, I_{ds} is evaluated around the ZTC region for various temperatures and plotted in Figure 4.3. Points A-F in the figure show where the 293K curve intercepts the 303K-353K curves. It is clear that a single ZTC point does not exist for all temperatures.

However, the current curves tend to converge into “bottle neck”. For example, a $60K$ change in temperature, the voltage and current spread around the “bottle neck” region is $\Delta V_{gs|ZTC} = 4mV$ and $\Delta I_{ds|ZTC} = 600nA$.

The simple first order mathematical model of the ZTC region has been confirmed using the BSIM3 model simulated using Cadence. These results, also plotted in Figure 4.3, show a ZTC voltage spread of $5mV$ and a corresponding current change of $600nA$ which is similar to that found using the simple model. However, the absolute values of the currents and voltages are slightly different which highlights the fact that the first order model is only an approximation.

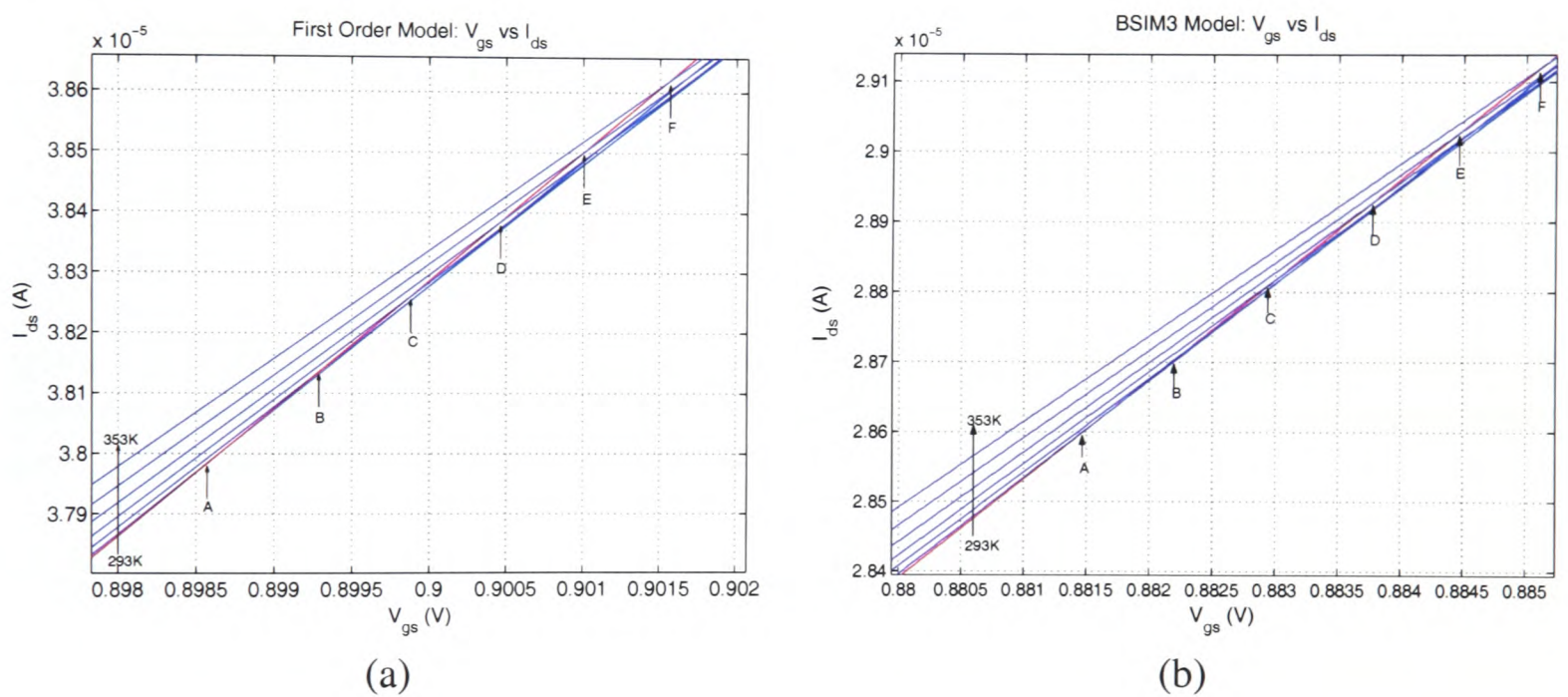


Figure 4.3: ZTC Simulations. (a) shows the first order model using Equations 4.16 and 4.17. (b) shows the BSIM3 model. Points A-F represent the points at which the 293K curve intercepts the curves for 6 other temperatures between 303K and 353K.

4.2.2 Experimental Results

A test NMOS transistor with $W = 4\mu m$ and $L = 1.2\mu m$ and the drain, source, gate and bulk nodes all externally connected was used to confirm the temperature dependence of the drain-source current, I_{ds} . This current is monitored at various temperatures as the gate voltage, V_{gs} , is swept from 0-3.3V whilst holding the drain-source voltage, V_{ds} , fixed at 3.3V. Figure 4.4(a) shows the measured results. From the close-up of the response, shown in Figure 4.4(b), regions in which $\frac{\partial I_{ds}}{\partial T} > 0$ and $\frac{\partial I_{ds}}{\partial T} < 0$ can be seen. More interestingly, there is a point in between these

two regions where a ZTC “point” is observed at a bias voltage of 0.915V and an output current of $34\mu\text{A}$. The difference between the experimental results and the simulations is consistent with process parameter variations.

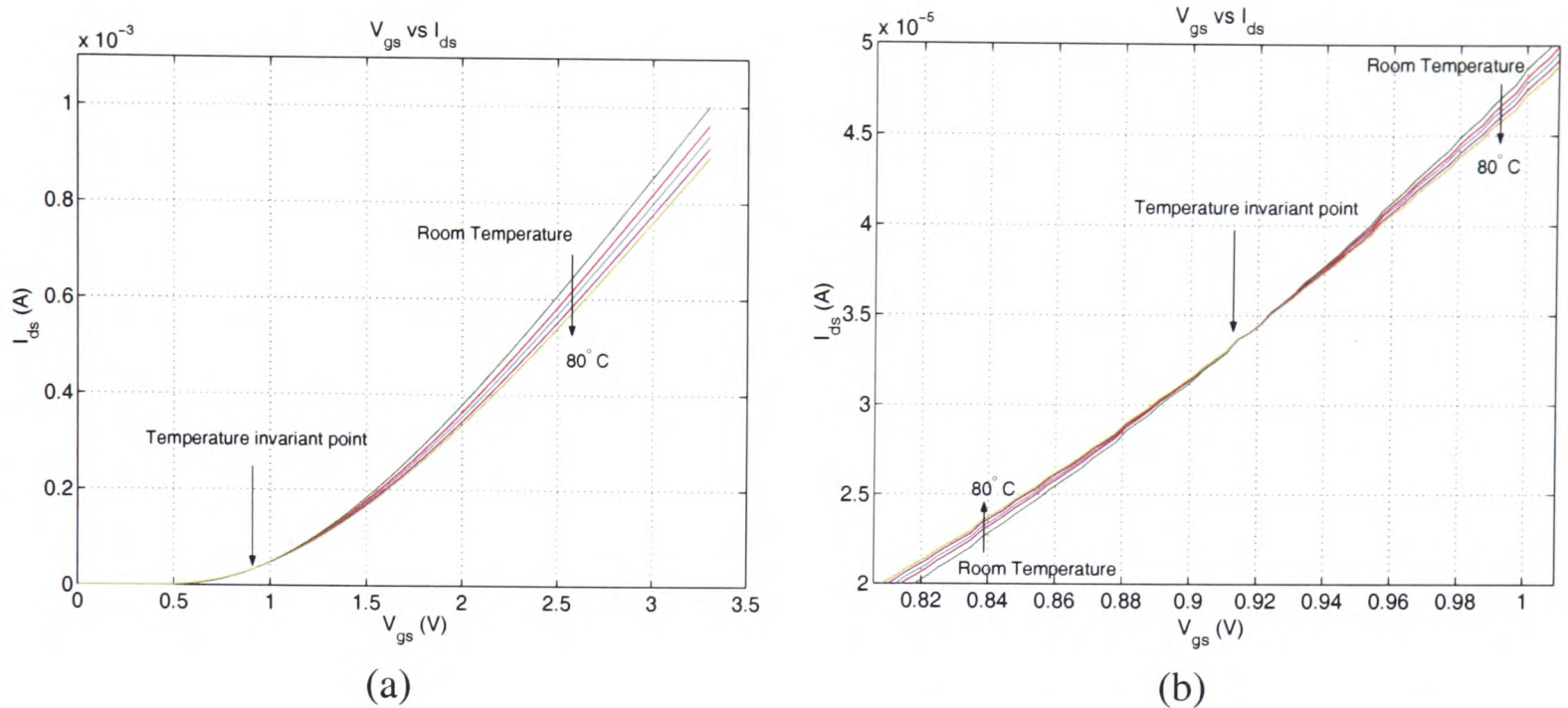


Figure 4.4: *Effect of temperature variations on the output current of a NMOS transistor. (b) shows the close-up view of the ZTC “point”. The temperature is varied between room temperature, 27°C, and 80°C.*

As can be seen from the measured and simulation data, in order to be biased at the ZTC “point”, the gate voltage must be set accurately. In practice, it may not be possible to provide a bias with the required accuracy. Therefore, it is necessary to determine the sensitivity of the temperature variations of the output current for bias voltages around the ZTC “point”.

4.3 Gate Bias Sensitivity around the ZTC “point”

The tolerance of the gate bias voltage of a MOSFET that is required to be temperature insensitive needs to be analysed in order to determine the accuracy and drift of the required voltage source. Assume a current source is formed by a n-channel MOSFET with a fixed gate voltage. The variation of I_{ds} with temperature for voltages around $V_{gs|ZTC}$ is evaluated in order to determine the sensitivity of the ZTC “point”. Substituting Equation 4.16 into Equation 4.1 leads to

Equation 4.18 which gives the variation of I_{ds} with temperature.

$$I_{ds} = K \left(\frac{T}{T_0} \right)^{\alpha_{\mu}} (0.322 + 122 \times 10^{-6} T_1 + 1.1 \times 10^{-3} (T - T_0))^2 \quad (4.18)$$

where $K = \mu_0 \frac{C_{ox}}{2} \frac{W}{L}$ and T_1 is the temperature that is used to give the ZTC bias voltage using Equation 4.16.

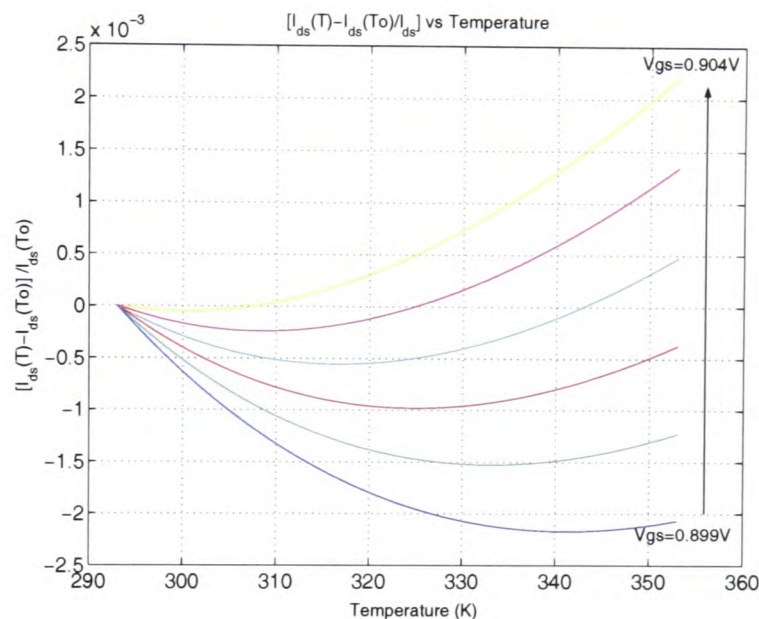


Figure 4.5: Fractional change in current around the ZTC region

The results of Matlab simulations, evaluated for a single NMOS transistor with $W = 4.2\mu\text{m}$ and $L = 1.2\mu\text{m}$, for six different gate voltages are plotted in Figure 4.5 and show I_{ds} variations relative to the initial current at $T=293\text{K}$. With V_{gs} increasing by only 5mV, 0.899V to 0.904V, the maximum variation of I_{ds} changes from -0.2% to $+0.2\%$. The smallest change in the output current is obtained at $V_{gs} = 0.902\text{V}$ where a variation of only $\pm 0.05\%$ relative to the initial current is obtained despite a 60°C change in temperature.

It is clear that the temperature dependence around the ZTC “point” is very sensitive to the gate voltage. Hence, there is a need to set V_{gs} accurately. This means that effects not included in the simple first order model of MOSFET behaviour also need to be analysed to ensure that the transistor is correctly biased. Therefore, using a modified model, the impact of V_{ds} variations is determined.

4.4 Drain-Source Voltage Modulation

A modified saturation current model which takes into account the V_{ds} dependence of the channel current of a MOSFET is [97].

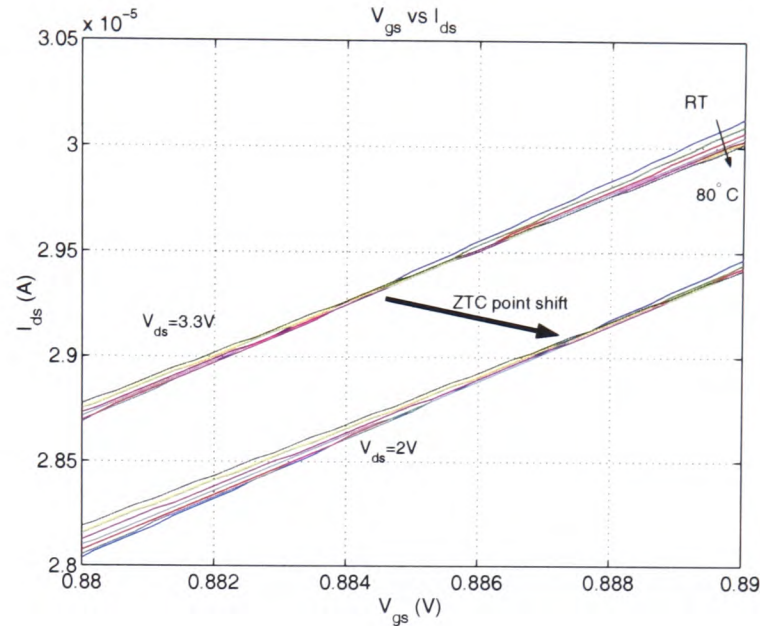


Figure 4.6: Effect of V_{ds} variation on the ZTC “point”: Simulation. The temperature is varied from room temperature, 27°C , to 80°C .

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_{th})^2(1 + \lambda V_{ds}) \quad (4.19)$$

where λ is the V_{ds} dependence factor. Simulation results around the ZTC “point” for a MOSFET with $V_{ds} = 3.3\text{V}$ and $V_{ds} = 2\text{V}$ are shown in Figure 4.6. The ZTC voltage and current are observed to have shifted from 0.884V to 0.887V and $29.3\mu\text{A}$ to $29\mu\text{A}$ respectively with a decrease in V_{ds} from 3.3V to 2V .

This shift can be explained by first evaluating the temperature dependence of the modified I_{ds} expression, Equation 4.19.

$$2\frac{\partial I_{ds}}{\partial T} = \left[\frac{\partial \beta}{\partial T}(V_{gs} - V_{th})^2 - 2\beta \frac{\partial V_{th}}{\partial T}(V_{gs} - V_{th}) \right] (1 + \lambda V_{ds}) + \beta V_{ds} \frac{\partial \lambda}{\partial T}(V_{gs} - V_{th})^2 \quad (4.20)$$

Since a ZTC “point” exists, $\frac{\partial I_{ds}}{\partial T} = 0$,

$$(V_{gs} - V_{th}) \left[\frac{\partial \beta}{\partial T} (1 + \lambda V_{ds}) + \beta V_{ds} \frac{\partial \lambda}{\partial T} \right] = 2\beta \frac{\partial V_{th}}{\partial T} (1 + \lambda V_{ds}) \quad (4.21)$$

$$V_{gs|ZTC} = V_{th} + \frac{2\beta \frac{\partial V_{th}}{\partial T} (1 + \lambda V_{ds})}{\frac{\partial \beta}{\partial T} (1 + \lambda V_{ds}) + \beta V_{ds} \frac{\partial \lambda}{\partial T}} \quad (4.22)$$

Substituting $\frac{\partial \beta}{\partial T}$ and $\frac{\partial V_{th}}{\partial T}$ from Equations 4.8 and 4.9 gives

$$V_{gs|ZTC} = V_{th} + \frac{2\alpha_{vt}(1 + \lambda V_{ds})}{\frac{\alpha_{\mu}}{T}(1 + \lambda V_{ds}) + V_{ds} \frac{\partial \lambda}{\partial T}} \quad (4.23)$$

For the case, $\frac{\partial \lambda}{\partial T} = 0$, Equation 4.23 reverts to the original ZTC expression, Equation 4.12. In this situation, the ZTC gate voltage is not a function of V_{ds} however, $I_{ds|ZTC}$ is dependent on V_{ds} . Since a shift in $V_{gs|ZTC}$ with V_{ds} has been observed, it must be assumed that $\frac{\partial \lambda}{\partial T} \neq 0$. The change in $V_{gs|ZTC}$ with V_{ds} must be associated with the temperature dependence of λ . This can be determined using the BSIM3 saturation region current model [100].

$$I_{ds} = I_{dsat} \left(1 + \frac{V_{ds} - V_{dsat}}{V_A} \right) \quad (4.24)$$

where I_{dsat} is the saturation current, V_{dsat} is the saturation drain-source voltage and V_A is the Early voltage. V_A is extracted from simulation and is found to approximately vary linearly with temperature

$$V_A \approx 0.0529T + 24.495 \quad (4.25)$$

At room temperature, V_A is approximately 40V. Therefore, at a low V_{gs} , typically 0.9V, $V_{dsat} =$

V_{ds}	$V_{gs ZTC}$	$I_{ds ZTC}$
3.3V	0.893V	23.8 μ A
2V	0.896V	23.4 μ A

Table 4.2: *Effect of V_{ds} variation on $V_{gs|ZTC}$*

0.4 and $\frac{V_{dsat}}{V_A} = \frac{0.4}{40} \ll 1$. Equation 4.24 can then be simplified to

$$I_{ds} = I_{dsat} \left(1 + \frac{V_{ds}}{V_A} \right) \quad (4.26)$$

$$\Rightarrow \lambda = \frac{1}{V_A} \quad (4.27)$$

From Equation 4.25 this gives

$$\frac{\partial \lambda}{\partial T} = -0.0529 \lambda^2 \quad (4.28)$$

Substituting Equation 4.28 into Equation 4.23 gives

$$V_{gs|ZTC} = V_{th} + \frac{2\alpha_{vt}(1 + \lambda V_{ds})}{\frac{\alpha_{\mu}}{T}(1 + \lambda V_{ds}) - 0.0529 \lambda^2 V_{ds}} \quad (4.29)$$

Equation 4.29 is evaluated using Matlab at T=293K for various values of V_{ds} . This is then substituted into Equation 4.19 to determine $I_{ds|ZTC}$. The results, summarised in Table 4.2, show a similar trend in the shift of the ZTC “point” to that observed in Figure 4.6. If a MOSFET is to be biased at the ZTC “point”, its drain voltage must be known in order to determine the optimum gate bias voltage. Fortunately for the trimmable current sources, the devices are cascoded by a switch and therefore variations in V_{ds} will be small.

4.5 Bias Source Temperature Dependence

The above analysis assumes that the gate bias voltage supplied to a MOSFET is temperature independent. In practice, this voltage will be supplied by a bias circuit whose output is likely to be temperature dependent. For the current sources described in Chapter 3, the bias voltage of

all of the fixed branch MOSFETs is supplied by the bias circuit described in Figure 3.2. Taking the temperature variation of the bias voltage into account, the temperature dependence of the output current is now given by

$$\frac{dI_{ds}}{dT} = \left. \frac{\partial I_{ds}}{\partial T} \right|_{MOS} + \frac{\partial I_{ds}}{\partial V_{gs}} \frac{\partial V_{gs}}{\partial T} \quad (4.30)$$

where $\left. \frac{\partial I_{ds}}{\partial T} \right|_{MOS}$ is temperature response of MOS with a fixed bias and $\frac{\partial I_{ds}}{\partial V_{gs}} \frac{\partial V_{gs}}{\partial T}$ is the response due to the temperature variations of the gate voltage. This suggests that the temperature dependence of output current of a MOSFET will depend critically upon the temperature dependence of the bias circuit.

4.5.1 Fixed Branch Bias Circuit

The bias voltage for the fixed branches of TCS1-TCS5 is supplied by a bias generator circuit shown in Figure 3.2. In order to determine the effect of this circuit on the output current, the simulated temperature responses of the fixed branch with and without the bias circuit are compared in Figure 4.7. The ZTC “point” for the MOSFET connected to the bias circuit is at a much higher output current, $126\mu\text{A}$, than that found for the MOSFET with a constant gate bias, $41.5\mu\text{A}$.

To explain this difference, consider the temperature response of the bias circuit determined from simulations, shown in Figure 4.8. It can be seen from this data that at an input voltage of approximately 0.9V, which is the input voltage at which the ZTC “point” is observed, the temperature gradient of the output voltage is positive.

$$\frac{\partial V_{bias}}{\partial T} > 0 \quad (4.31)$$

where V_{bias} is the output voltage from the bias circuit. Since a ZTC “point” has been observed,

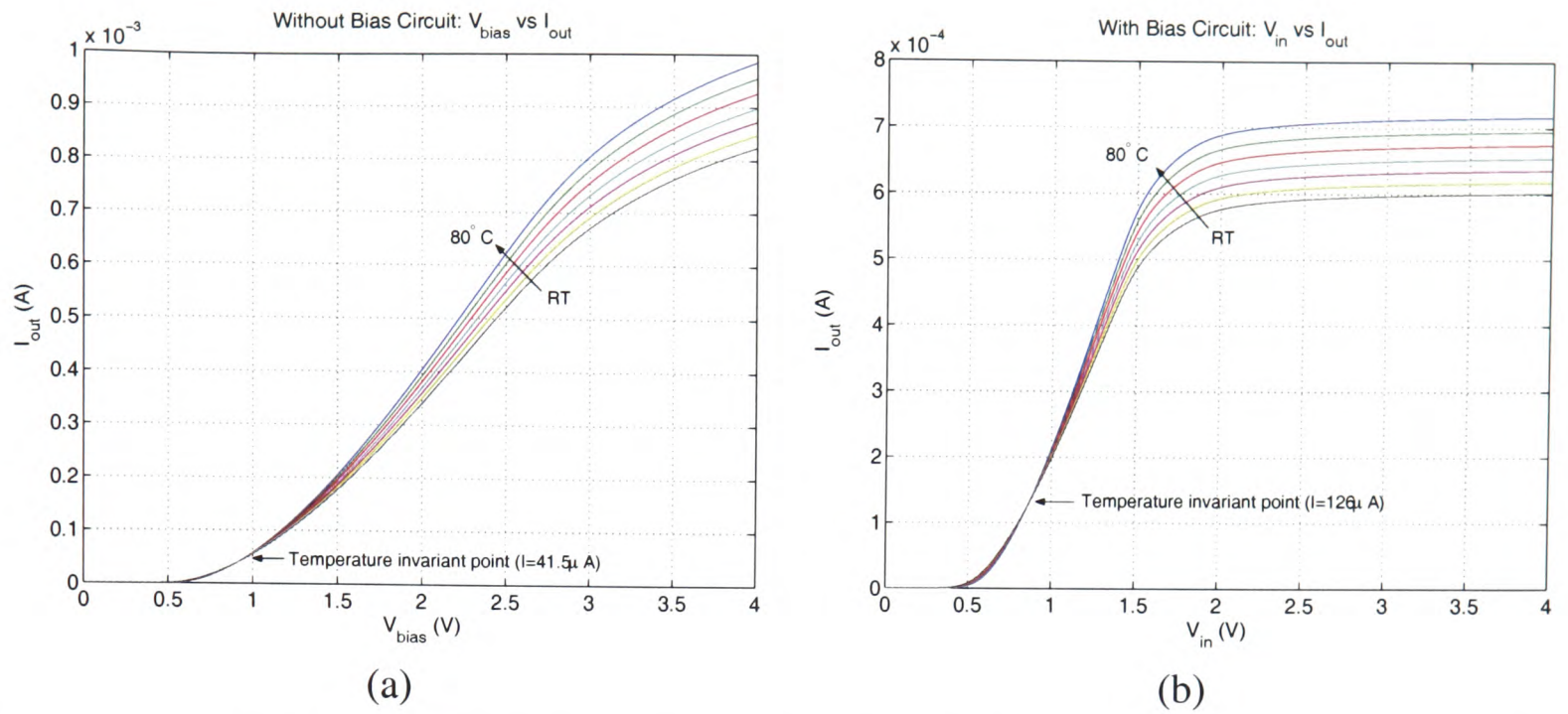


Figure 4.7: Effect of Bias Circuit as the temperature is varied between room temperature, 27°C , to 80°C . (a) shows the response without the bias circuit. V_{bias} is the bias voltage applied to the fixed branch transistor. (b) shows the response with the bias circuit. V_{in} is the input voltage of the bias circuit. The saturation effect is due to the bias circuit output.

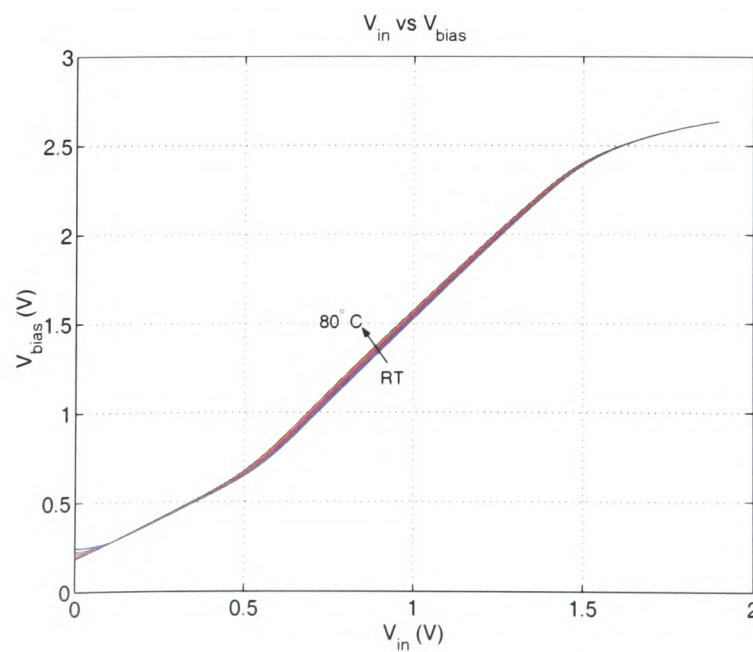


Figure 4.8: Temperature response of the bias circuit

Equation 4.30 must equal to zero. In this case

$$\left. \frac{\partial I_{ds}}{\partial T} \right|_{MOS} + \frac{\partial I_{ds}}{\partial V_{bias}} \frac{\partial V_{bias}}{\partial T} = 0 \quad (4.32)$$

The second term in the above equation is positive since at this bias condition

$$\frac{\partial I_{ds}}{\partial V_{bias}} > 0 \quad (4.33)$$

and therefore for a ZTC “point”

$$\left. \frac{\partial I_{ds}}{\partial T} \right|_{MOS} < 0 \quad (4.34)$$

This condition is met when the bias voltage is greater than $V_{gs|ZTC}$ of a MOSFET as shown in Figure 4.4. Therefore, the ZTC output current with the bias circuit is greater than that found for the MOSFET without the bias circuit since the MOSFET with the bias circuit has to be biased at a higher voltage at the ZTC “point”. These results show that a ZTC point still exists with the bias circuit, only its position has moved.

The MOSFETs of the trimming branches of TCS2 and TCS3 are biased with a floating-gate MOSFET based inverter and source-follower respectively as shown in Figure 4.9. It is therefore expected that the temperature response of these branches will be dependent upon the temperature response of the inverter and source-follower bias circuits.

4.5.2 Inverter Bias Circuit

To determine the temperature dependence of the inverter bias circuit on the output current of the trimming branch of TCS2, the temperature response of the inverter is determined from simulations. These results are shown in Figure 4.10. At output voltages of less than 2V, a positive temperature gradient is observed, $\frac{\partial V_{out}}{\partial T} > 0$, for a fixed input voltage. For a ZTC

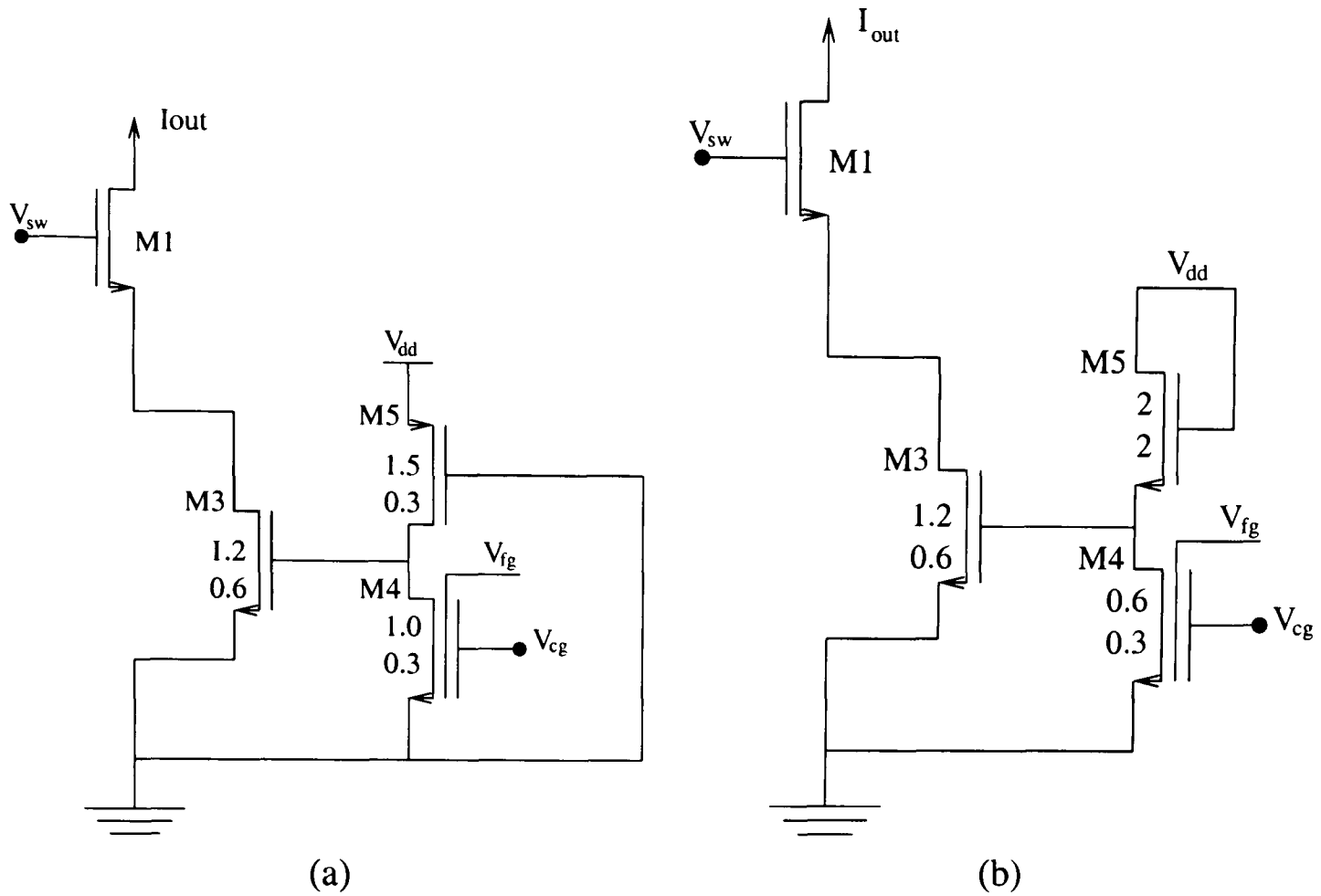


Figure 4.9: *TCS2 and TCS3 Trimming Branch Bias Circuits (a) shows the TCS2 trimming branch with the floating-gate MOSFET based inverter bias. (b) shows the TCS3 trimming branch with the corresponding source-follower bias.*

“point” to exist, Equation 4.30 must equal zero. Therefore

$$\left. \frac{\partial I_{out}}{\partial T} \right|_{MOS} + \frac{\partial I_{ds}}{\partial V_{out}} \frac{\partial V_{out}}{\partial T} = 0 \quad (4.35)$$

Since for inverter output voltages of less than 2V

$$\frac{\partial I_{out}}{\partial V_{out}} \frac{\partial V_{out}}{\partial T} > 0 \quad (4.36)$$

$$\Rightarrow \left. \frac{\partial I_{out}}{\partial T} \right|_{MOS} < 0 \quad (4.37)$$

As with the case of the TCS1-TCS3 fixed branch MOSFETs, a ZTC point is expected to be at a higher output current than for a MOSFET biased with an ideal voltage source in order to meet the MOSFET temperature response requirements set by Equation 4.37.

The experimental temperature responses of the trimming branches of TCS2 and TCS1 are compared in Figure 4.11. The ZTC “point” for the floating-gate inverter biased MOSFET is as

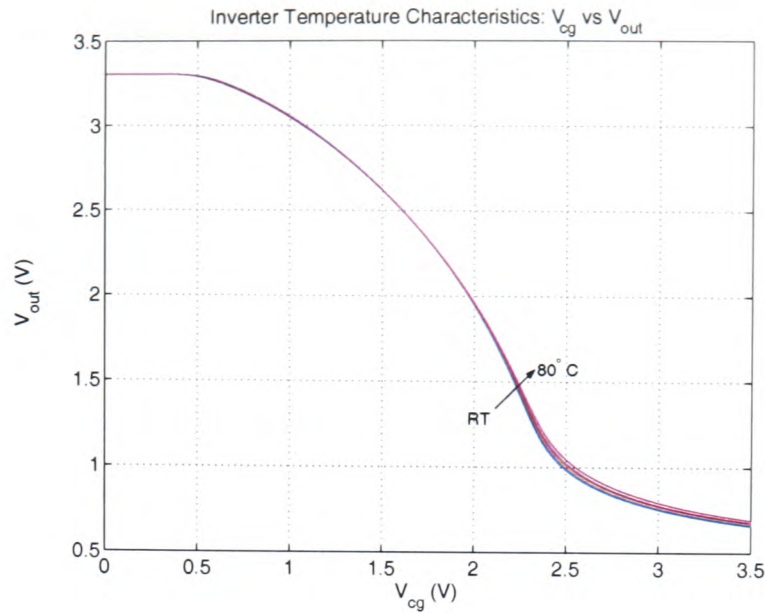


Figure 4.10: *Simulated inverter temperature response: Room temperature to 80°C*

expected found to be at a higher current, $80\mu\text{A}$, than that found for the trimming branch which consists of only a floating-gate MOSFET, $17\mu\text{A}$. These results show that a ZTC “point” still exists with this bias circuit, once again it has simply moved to a higher current value.

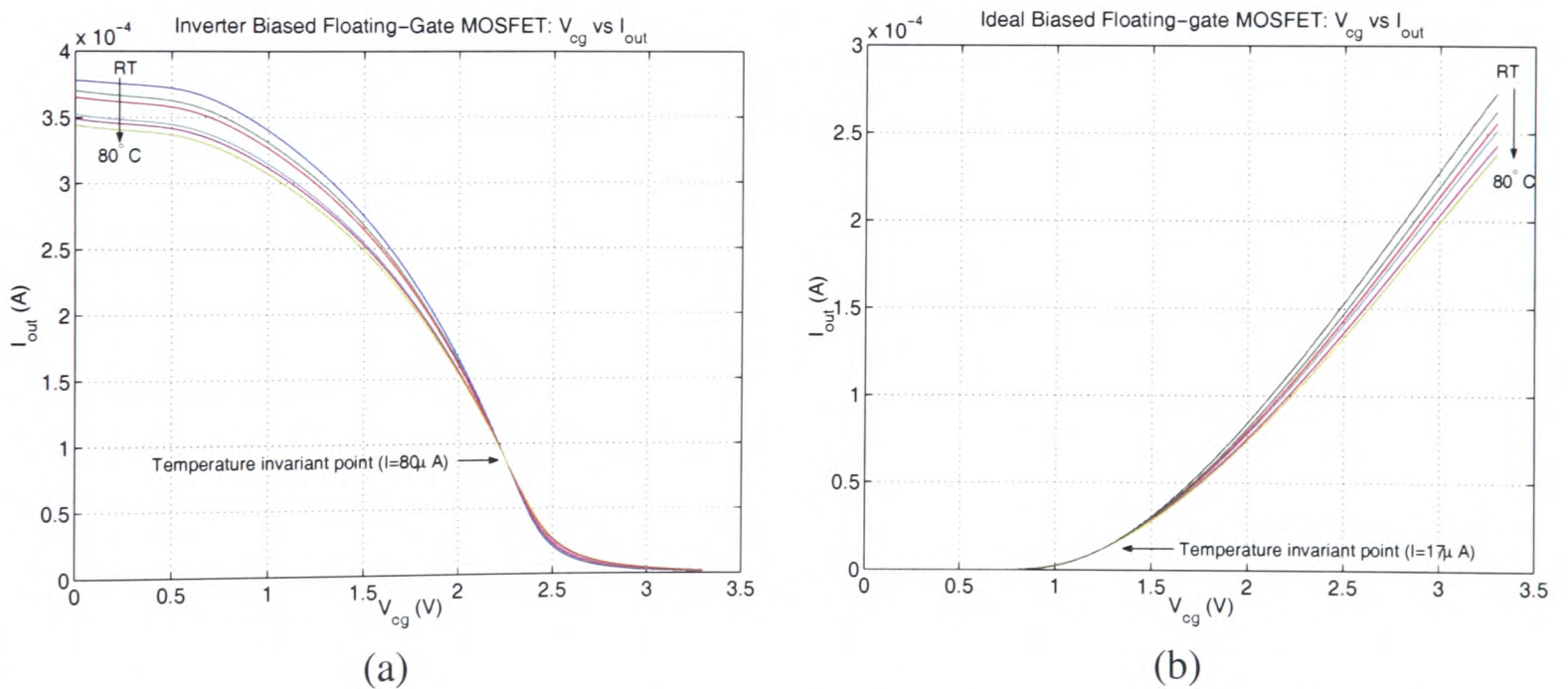


Figure 4.11: *Experimental response of the trimming branches of TCS1 and TCS2 as the temperature is varied between room temperature and 80°C. (a) shows the effect of the inverter bias in TCS2. (b) shows the temperature response of the trimming branch of TCS1 which has no bias circuit. Note the high threshold voltage due to an initial negative charge on the floating-gate.*

4.5.3 Source-Follower Bias Circuit

Similar to the inverter bias of TCS2, the source-follower bias circuit in TCS3 will affect the temperature response of the trimming branch of TCS3. The temperature response of the output current of the trimming branch, which depends upon the response of the source-follower, is given by Equation 4.30. Again the source-follower has no external connections therefore, the temperature response of the source-follower is determined from simulation. These results are shown in Figure 4.12 for temperatures ranging from room temperature to 80°C.

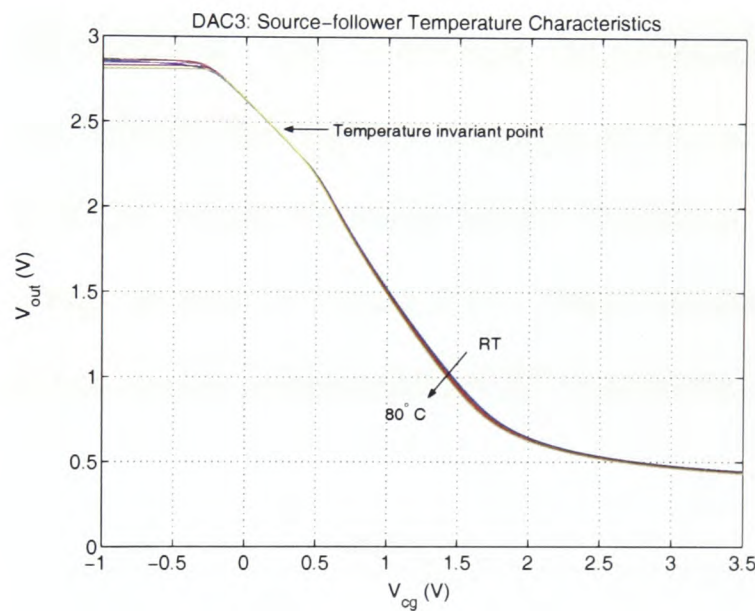


Figure 4.12: *Simulated source-follower bias circuit temperature response: Room temperature to 80°C*

A temperature independent output voltage region is shown at an output voltage of approximately 2.5V. At lower output voltages

$$\frac{\partial V_{out}}{\partial T} < 0 \quad (4.38)$$

Therefore

$$\frac{\partial I_{ds}}{\partial V_{out}} \frac{\partial V_{out}}{\partial T} < 0 \quad (4.39)$$

For a ZTC “point” to exist, Equation 4.30 must equal zero. Hence, following from Equation

$$\left. \frac{\partial I_{out}}{\partial T} \right|_{MOS} > 0 \quad (4.40)$$

In order to meet the condition set by Equation 4.40, V_{out} must be less than the $V_{gs|ZTC}$ of a MOSFET. Therefore, the expected ZTC current for the MOSFET biased with a source-follower is lower than that found for the circuit without the source-follower.

The measured temperature response of the trimming branch of TCS3 is shown in Figure 4.13. No ZTC “point” is observed. This is because the temperature response, $\left. \frac{\partial I_{out}}{\partial T} \right|_{MOS}$, is never positive enough to balance the negative response of the source-follower, $\frac{\partial I_{out}}{\partial V_{out}} \frac{\partial V_{out}}{\partial T}$. The temperature gradient of the whole trimming branch therefore remains negative for entire floating-gate voltage range as seen in Figure 4.13. These results suggest that this source-follower bias circuit would not be able to bias a MOSFET to achieve a temperature independent current source.

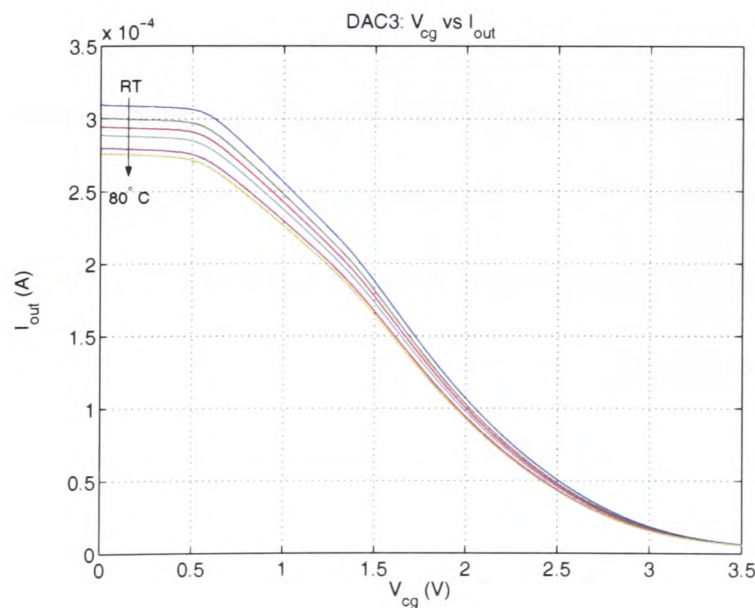


Figure 4.13: Experimental temperature response of the trimming branch of TCS3 as the temperature is varied from 27°C to 80°C. No ZTC “point” is observed.

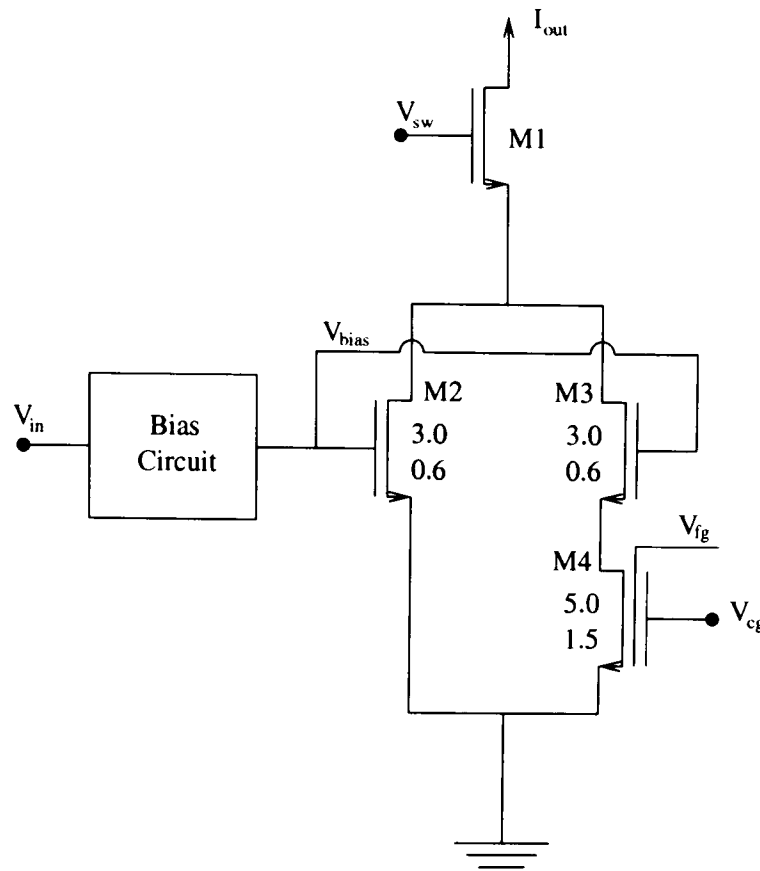


Figure 4.14: TCS5 showing the two branches. The trimming branch consists of floating-gate MOSFET which is used to modulate the output current.

4.6 Temperature Response of TCS5

The final current source, shown again in Figure 4.14, consists of two branches which are biased by the bias circuit described in Figure 3.2. One branch is a MOSFET similar to the fixed output branches of TCS1-TCS3 whilst the second branch consists of 2 MOSFETs in series, with one acting as a trimming resistor. Since the two branches are always on, the overall temperature response will be a combination of the response of both halves.

$$\frac{\partial I_{out}}{\partial T} = \frac{\partial I_{fixed}}{\partial T} + \frac{\partial I_{trim}}{\partial T} \quad (4.41)$$

Therefore, for a ZTC “point” to exist

$$\frac{\partial I_{out}}{\partial T} = 0 \quad (4.42)$$

$$\Rightarrow \frac{\partial I_{fixed}}{\partial T} + \frac{\partial I_{trim}}{\partial T} = 0 \quad (4.43)$$

The temperature response of the fixed output branch will be the same as that obtained for the

previous current sources. The variation in the overall ZTC region is therefore governed by the temperature response of the trimmable branch of the current source.

4.6.1 Temperature Dependence Model of the Trimming Branch of TCS5.

The trimmable branch without the switch is shown in Figure 4.15. In this circuit transistor M1 operates in the saturation region and the trimming transistor, M2, in the linear region ¹. The output current, I_{out} , of the circuit in Figure 4.15 is given by two simultaneous equations describing currents through M1 and M2

$$I_{out} = \frac{\beta_1}{2}(V_G - V_S - V_{th1})^2 \quad (4.44)$$

$$I_{out} = \beta_2(V_{fg} - V_{th2})V_S \equiv \frac{V_S}{R_{eff}} \quad (4.45)$$

where V_G is the gate voltage of M1, V_S is the source voltage of the same device and R_{eff} is the effective channel resistance of the trimming transistor. Eliminating V_S from the two equations leads to a relationship between V_G and I_{out}

$$\frac{2I_{out}}{\beta_1} = V_G^2 + (I_{out}R_{eff})^2 + V_{th1}^2 - 2V_GI_{out}R_{eff} - 2V_GV_{th1} + 2I_{out}R_{eff}V_{th1} \quad (4.46)$$

This equation can be simplified into a quadratic equation in I_{out}

$$(I_{out}R_{eff})^2 + 2I_{out} \left[R_{eff}V_{th1} - V_GR_{eff} - \frac{1}{\beta_1} \right] + (V_G - V_{th1})^2 = 0 \quad (4.47)$$

which has two possible solutions

$$I_{out} = \frac{1}{R_{eff}} \left[V_G - V_{th1} + \frac{1}{R_{eff}\beta_1} \right] \pm \frac{1}{R_{eff}^2\beta_1} \sqrt{2R_{eff}\beta_1(V_G - V_{th1}) + 1} \quad (4.48)$$

The modelled behaviour of a device in saturation is $I_{out} = 0$ when $V_G = V_{th1}$, therefore the

¹In Appendix A, this circuit model is simplified further by replacing the linear MOSFET with a resistor.

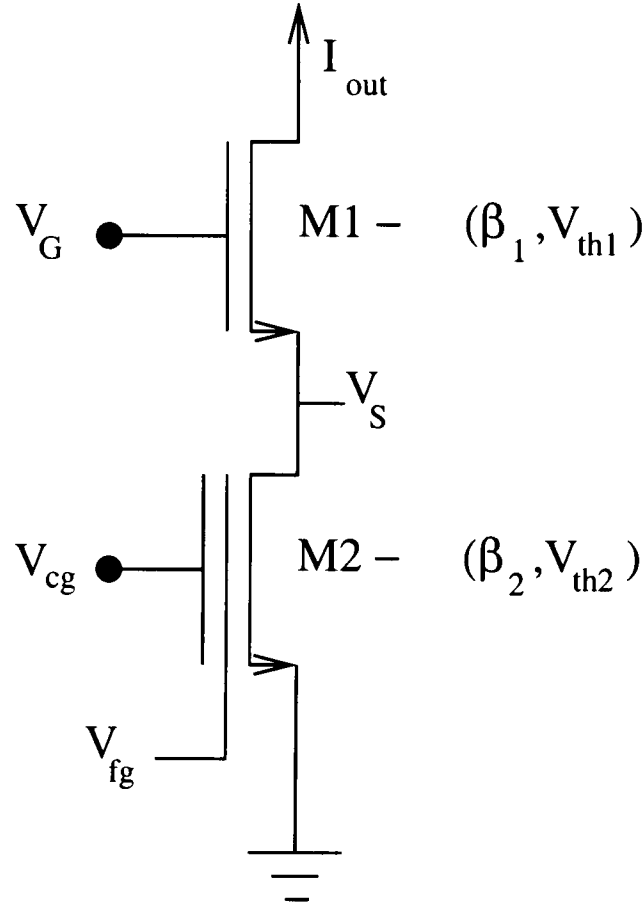


Figure 4.15: A simple version of TCS5

valid solution is

$$I_{out} = \frac{1}{R_{eff}} \left[V_G - V_{th1} + \frac{1}{R_{eff}\beta_1} \right] - \frac{1}{R_{eff}^2\beta_1} \sqrt{2R_{eff}\beta_1(V_G - V_{th1}) + 1} \quad (4.49)$$

where $R_{eff} = \frac{1}{\beta_2(V_{fg} - V_{th2})}$. Figure 4.16 shows how this current varies as a function of V_G around the ZTC “point” at two different temperatures and various values of floating-gate voltages. A turning point in the locus of the ZTC points is observed near $I_{out|ZTC} = 32\mu A$.

The locus can be determined by re-writing Equation 4.30

$$\frac{dI_{out}}{dT} = \frac{\partial I_{out}}{\partial T} \Big|_{MOS} + \frac{\partial I_{out}}{\partial V_{GS}} \frac{\partial V_{GS}}{\partial T} = 0 \quad (4.50)$$

From Equation 4.3, the MOSFET temperature dependence is given by

$$\begin{aligned} \frac{\partial I_{out}}{\partial T} \Big|_{MOS} &= \frac{1}{2} \frac{\partial \beta_1}{\partial T} (V_{G|ZTC} - V_S - V_{th1})^2 - \beta_1 \frac{\partial V_{th1}}{\partial T} (V_{G|ZTC} - V_S - V_{th1}) \\ &= \frac{\alpha_u \beta_1}{2T} (V_{G|ZTC} - V_S - V_{th1})^2 - \beta_1 \alpha_{vt} (V_{G|ZTC} - V_S - V_{th1}) \end{aligned} \quad (4.51)$$

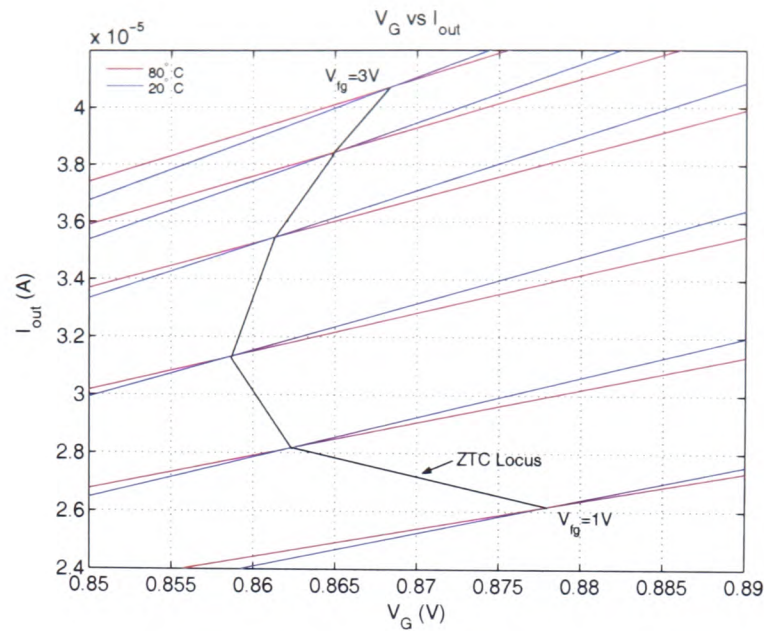


Figure 4.16: Close-up of V_G vs I_{out} at different V_{fg} and temperatures. A locus of the ZTC “points” is also shown.

and the latter terms in Equation 4.50 are

$$\frac{\partial I_{out}}{\partial V_{GS}} = \beta_1 (V_{G|ZTC} - V_S - V_{th1}) \quad (4.52)$$

$$\begin{aligned} \frac{\partial V_{GS}}{\partial T} &= -\frac{\partial V_S}{\partial T} \\ &= -I_{out|ZTC} \frac{\partial R_{eff}}{\partial T} \end{aligned} \quad (4.53)$$

The overall temperature dependence is then

$$\frac{\alpha_u \beta_1}{2T} (V_{G|ZTC} - V_S - V_{th1})^2 - \beta_1 (V_{G|ZTC} - V_S - V_{th1}) (\alpha_{vt} + I_{out|ZTC} \frac{\partial R_{eff}}{\partial T}) = 0 \quad (4.54)$$

which can be simplified to

$$\frac{\alpha_u}{2T} (V_{G|ZTC} - V_S - V_{th1}) - \alpha_{vt} - I_{out|ZTC} \frac{\partial R_{eff}}{\partial T} = 0 \quad (4.55)$$

where the temperature dependence of the effective resistance, R_{eff} is given by

$$\frac{\partial R_{eff}}{\partial T} = R_{eff} \left[\frac{\alpha_{vt}}{V_{fg} - V_{th2}} - \frac{\alpha_u}{T} \right] \quad (4.56)$$

Equation 4.55 can then be re-arranged to

$$V_{G|ZTC} - V_S - V_{th1} = \frac{2T}{\alpha_u} \left[\alpha_{vt} + I_{out|ZTC} \frac{\partial R_{eff}}{\partial T} \right] \quad (4.57)$$

Substituting $V_{G|ZTC} - V_S - V_{th1}$ from Equation 4.44, gives

$$I_{out|ZTC} \frac{\partial R_{eff}}{\partial T} - \frac{\alpha_u}{T\sqrt{2\beta_1}} \sqrt{I_{out|ZTC}} + \alpha_{vt} = 0 \quad (4.58)$$

This quadratic equation in $\sqrt{I_{out|ZTC}}$ can be solved to give

$$\sqrt{I_{out|ZTC}} = \frac{\alpha_u}{2T \frac{\partial R_{eff}}{\partial T} \sqrt{2\beta_1}} + \frac{1}{2 \frac{\partial R_{eff}}{\partial T}} \sqrt{\frac{\alpha_u^2}{2T^2 \beta_1} - 4\alpha_{vt} \frac{\partial R_{eff}}{\partial T}} \quad (4.59)$$

This equation can be solved for various values of V_{fg} to determine $I_{out|ZTC}(V_{fg})$. Each of these values can be substituted into Equation 4.45 to determine the corresponding value of V_S . Finally, the values of V_S and $I_{out|ZTC}$ can then be used in Equation 4.44 to determine the corresponding $V_{G|ZTC}$. The resulting ZTC “points”, $(V_{G|ZTC}, I_{out|ZTC})$, plotted in Figure 4.17(a), show a curve with a turning point at approximately (0.862V, 32μA).

This data suggests that, by biasing the circuit at a voltage, V_G higher than this turning point voltage, it should be possible to vary the output current over a finite range of values whilst remaining temperature insensitive. Using Equation 4.49, the variation of the output current with the floating-gate voltage can be determined for bias conditions around the ZTC turning point. Figure 4.17(b) shows the current variation between two temperatures (20°C and 80°C) for several values of V_G between 0.858V and 0.87V as V_{fg} and hence I_{out} is varied. These results show that if the current source is biased between these voltages, then a trimmable current source can be designed with a weak temperature dependence. Thus for example, when biased at $V_G = 0.865V$, the output current can be trimmed between 27μA and 37μA and still be temperature insensitive to within 0.3% as the temperature increases from 20°C to 80°C which is equivalent to 0.005%/°C.

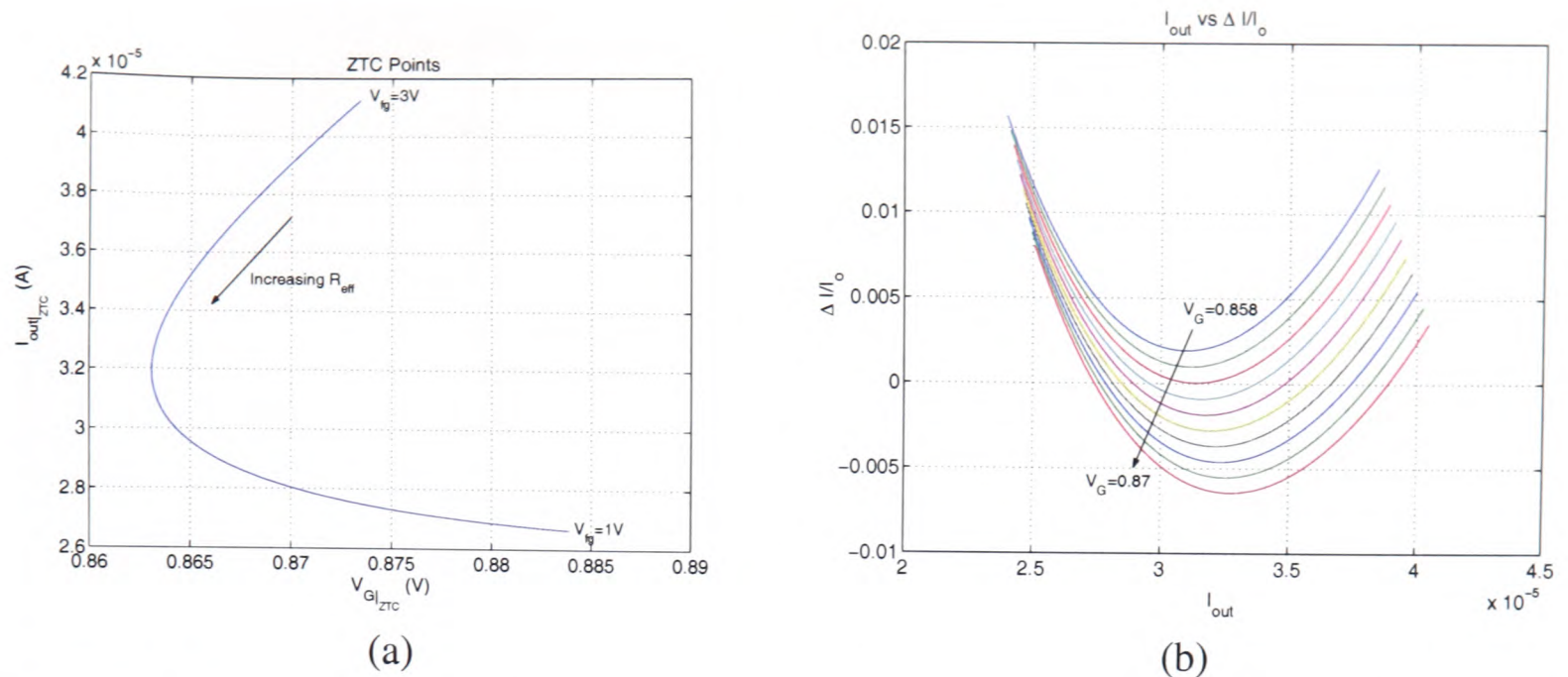


Figure 4.17: (a) shows the locus of ZTC “points” R_{eff} and hence V_{fg} is varied. (b) shows the variation of the output current with the current source biased close to the ZTC turning point.

4.6.2 TCS5 Experimental Results

To confirm the model results, the output current of TCS5 is measured as a function of the bias voltage at several temperatures and floating-gate voltages. These results, plotted in Figure 4.18, clearly show a ZTC “point” for each group of currents measured at the same floating-gate voltage. Critically, these ZTC points appear to lie on a curve similar to that predicted by the model in Figure 4.16. Since the fixed branch only gives a single ZTC “point”, the overall ZTC “point” variation seen in this figure is only due to the temperature response of the trimming branch.

Using these experimental results, one value of V_G which will create a current source with a low temperature sensitivity over a significant current range is 0.885V. Measurement results showing the variation of output current with the floating-gate voltage at several bias voltages around 0.885V and temperatures ranging from room temperature to 80°C are plotted in Figure 4.19. The results for 0.85V show that the output current changes by up to 30% as the temperature is increased from room temperature to 80°C. The change in the current is monotonic. The maximum change reduces rapidly with increasing bias voltage until a bias voltage of 0.88V where a maximum change of only 0.4% is observed. The maximum change at 0.89V is -0.5% and therefore the optimum bias voltage is expected to be in between these two voltages which

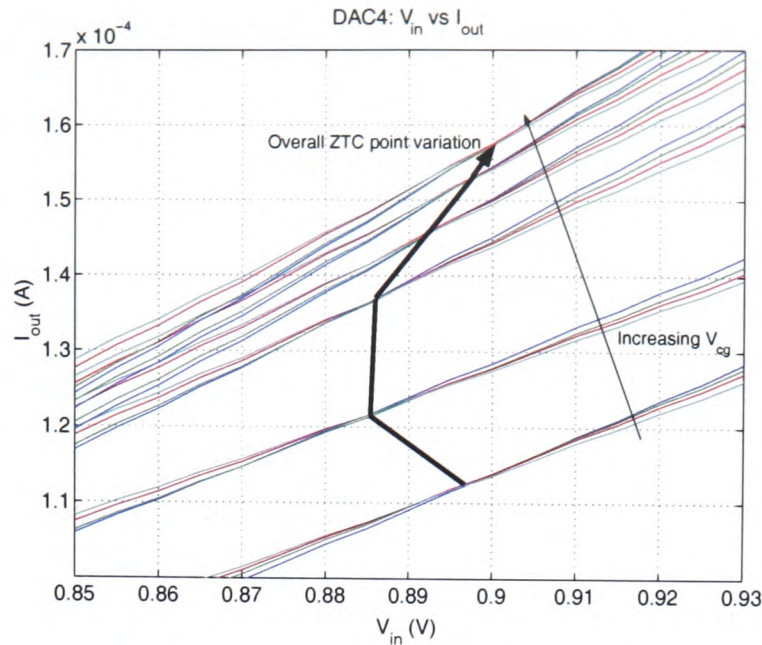


Figure 4.18: *TCS5: Measured variation of the output current at various floating-gate voltages. The locus of the ZTC “points” is also shown.*

gives the minimum temperature sensitivity over a trimmable current range of 17%. The change in current is also no longer monotonic. Therefore, by biasing the circuit at around 0.885V, a trimmable current source with a weak temperature dependence is obtained.

Charge retention experimental results of this current source, shown previously in Figure 3.18, confirmed the ability of this circuit to retain charge during operation over at least 7 days. The bias conditions of the current source during that experiment were in fact set around a ZTC “point”. Results of retention experiments at three different temperatures, 40°C, 60°C, 80°C, with the current source biased around the ZTC “point”, are shown in Figure 4.20. As expected, the output current varies only slightly ($0.2\mu\text{A}$) as the temperature is varied from 40°C to 80°C. Furthermore, as expected the floating-gate does not show any sign of leakage for all three temperatures.

4.7 Conclusion

The trimmable current sources described in Chapter 3 are designed to eliminate the mismatch between elements in a large array. Ideally, the current sources will be trimmed once immediately after fabrication. This means that the current sources must remain matched throughout their

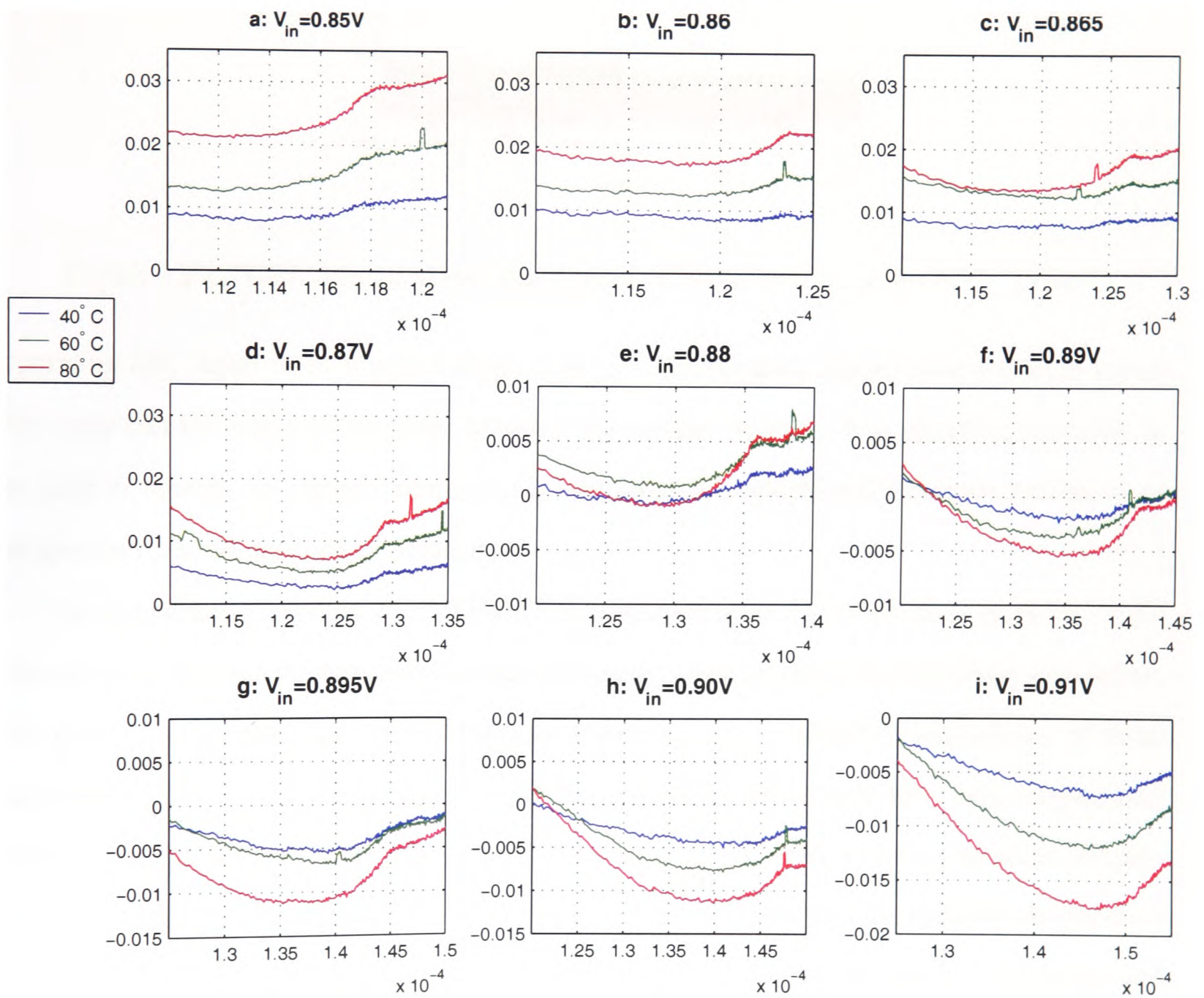


Figure 4.19: TCS5 Effect of Bias voltage variation - experiment. The x-axes of the graphs are the output currents at room temperature, I_{rt} , and the y-axes is the change in current relative to the room temperature current, $\frac{I_T - I_{rt}}{I_{rt}}$ where I_T is the current at temperature T .

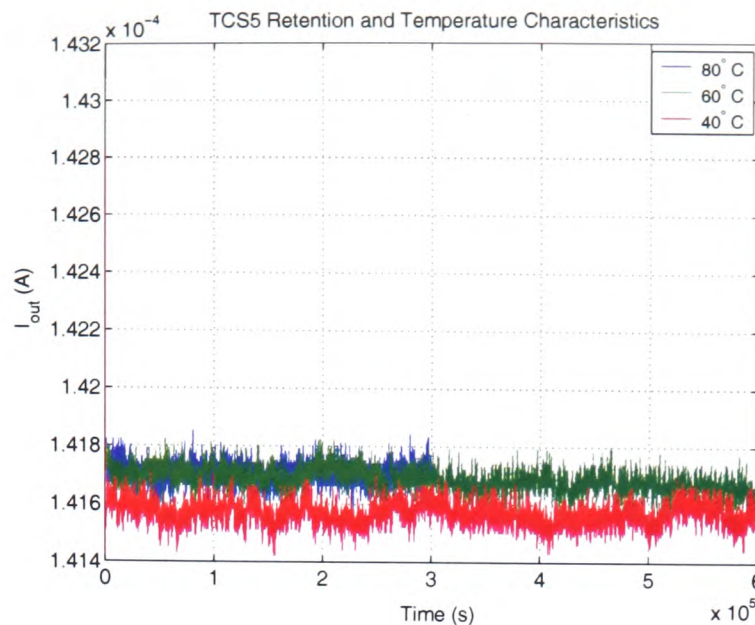


Figure 4.20: *TCS5: Retention and Temperature Characteristics at the ZTC “point”*.

operating life. Apart from charge leakage from the floating-gate, temperature gradients across the array can introduce mismatches between the current sources. It is therefore desirable to be able to operate the current sources at a bias condition which will minimise the effect of temperature variations during operation.

The temperature response of a MOSFET is dependent upon the temperature response of the threshold voltage and the transconductance parameter, β which are both technology dependent. For the $0.35\mu m$ technology used, it has been shown that the temperature dependence of these parameters causes a MOSFET operating in the saturation region to have a zero temperature coefficient (ZTC) point. When biased at this point, the output current has a very weak temperature dependence. In order to achieve true temperature independence, the mobility temperature exponent is required to have a value of -2, which is not the case for this process. Experimental results of the variation of the output current with temperature, shown in Figure 4.4, confirm the existence of a ZTC point. These results are also consistent with the simple first order model used to predict the ZTC “point”. This model is also used to show that the ZTC “point” is very sensitive to the MOSFET gate and drain bias conditions. The ZTC “point” characteristics of each of the designed current sources are summarised in Table 4.3.

The fixed branch MOSFETs of all the current sources are biased with a bias generator circuit shown in Figure 3.2. The temperature response of the output current depends upon

Current Source	Floating-gate Mode	Programming Speed	Retention Characteristics	Temperature Response
TCS1	Current Source	2	4	Single ZTC point
TCS2	Voltage Source	1	3	Single ZTC point
TCS3	Voltage Source	4	2	No ZTC point
TCS5	Resistor	3	1	Locus of ZTC points

Table 4.3: *Summary of the characteristics of the current sources. The relative scores shown for the programming speed and charge retention range from 1 for the best current source to 4 for the worst one. The temperature response of each current source is described in terms of the ZTC points as the current source is trimmed.*

the variation of this bias voltage due to temperature. The position of the ZTC current can either increase or decrease relative to the MOSFET ZTC current depending upon the temperature gradient of the bias voltage. Simulation results of the bias circuit show that the bias voltage has a positive temperature gradient which has the effect of increasing the ZTC output current compared to a MOSFET with a fixed bias voltage. Therefore the ZTC “point” in TCS1 is a single “point” which is governed by response of the fixed branch MOSFET and the trimmable branch MOSFET.

Similarly, the MOSFET of the trimmable branches of TCS2 and TCS3 are biased with an inverter and a source-follower respectively. Therefore, the temperature response of these branches will depend upon the temperature response of these bias circuits. In the case of the inverter, the trimming bias voltage has a positive temperature gradient which increases the ZTC current relative to an ideal biased MOSFET. On the other hand, the temperature response of the source-follower shows a negative temperature gradient. This has the effect of lowering the ZTC current. Unfortunately, this temperature dependence is so strong that no ZTC “point” is observed for this current source.

The final current source, TCS5, consists of a fixed branch, whose temperature response is the same as the other current sources, and a trimmable branch with two MOSFETs in series. The temperature dependence model of this branch, derived from first principles, shows that the ZTC “point” moves along an arc as the trimming voltage is varied as shown in Figure 4.16. An operating point is identified from simulations which results in the trimmable output cur-

rent having a weak temperature dependency ($0.005\%/^{\circ}\text{C}$) over significant current range (17%). These results are confirmed by the measured temperature response of output current as shown in Figure 4.18. Additionally, experimental results have confirmed the long term retention ability of the floating-gate MOSFET in this circuit. TCS5 can therefore be used as a trimmable current source in a current steering DAC whilst maintaining the required matching requirements in the presence of temperature gradients during operation.

Chapter 5

Summary and Conclusions

This thesis has presented a floating-gate device, implemented in a $0.35\mu m$ double-poly CMOS process, as a trimming element in current sources suitable for a current steering DAC.

5.1 Floating-Gate Technology

The designed floating-gate device consists of two n-channel MOSFETs which share a floating-gate. One transistor is the CHEI programming transistor and the other one is the sense/read transistor. The floating-gate is capacitatively coupled to a control-gate and a tunneling node. The charge on this floating-gate device, which has an area of $300\mu m^2$, can therefore be changed using either CHEI or FNT.

The two programming mechanisms can be selected via the CHEI and FNT selection circuits which allow a floating-gate element in a matrix to be programmed using either one of the two mechanisms. These circuits however, increase the area of the element considerably to $1892\mu m^2$.

CHEI characteristics of the floating-gate device, investigated for several values of the programming voltage, show that the injection gate current is a function of this programming voltage and the instantaneous floating-gate voltage as shown in Figure 2.6(b). Two new empirical models describing these characteristics are shown to be a good fit to the experimental data for floating-gate voltages ranging from 3V to 3.75V and programming voltages ranging from 5V

to 6V.

The derived models can only be used in predicting the programming conditions required to achieve a specific output current if the model is independent of programming variations from one device to another. Unfortunately, CHEI programming experiments on different elements have shown that the injection current can vary by up to a factor of two from one device to another on the same chip. This means that the models could be used to predict an approximate programming rate and with the use of some form of feedback this rate can be adjusted to achieve the precise floating-gate voltage.

FNT is observed when a voltage greater than 16V is applied to the tunneling node. This mechanism forces the electrons off the floating-gate which increases the floating-gate voltage. This is therefore a complementary programming mechanism to CHEI. The tunneling current, derived from experiments and shown in Figure 2.12, is found to be consistent with the original Fowler-Nordheim tunneling current model described by Equation 2.17. By analysing the experimental data, this model is simplified to one which fits the experimental tunneling current over five orders of magnitude. However, the FNT current of several different floating-gate elements on the same chip are found to vary by as much as an order of magnitude. Previous FNT experiments through inter-polyoxide have suggested that the injection current is dominated by conduction in small areas, thus causing large variations. Therefore, as with CHEI, this mechanism can only be used for precise programming using some form of a feedback system. Considering these large variations, another option would be to use FNT as a blanket erase mechanism and therefore use only CHEI in conjunction with feedback for precise programming.

It had been expected that with the floating-gate surrounded by a very good insulator, SiO_2 , the programmed charge would remain on the floating-gate permanently whilst the device is kept in storage. However, it has not been possible to prove this. Despite various attempts to determine the long term retention ability of these devices, experimental results have shown that these devices suffer from severe charge loss when stored. Evidence is presented that leads to the conclusion that this loss of charge was due to electrostatic transients small enough to pass through conventional ESD protection circuits used on the control-gate pad and not due to charge

loss during storage. A more important characteristic is the charge storage capability of these devices during normal operation. Results have been presented that show that the floating-gate device suffers from charge loss due to charge injection from the sense MOSFET even with drain-source voltages at which electrons are not expected to gain the energy required to cross the $Si-SiO_2$ barrier. This is thought to arise from a mechanism, suggested by Ghetti et al. [90], in which carrier-carrier interactions are responsible for the generation of hot electrons. These results suggest that to minimise the charge loss from the floating-gate, the sense MOSFET must be designed to operate with a low V_{ds} . Measurement results for a MOSFET operated with a V_{ds} of 1V over a period of 7 days showed that temperature variations of less than 0.5°C has a larger effect on the output current than charge loss from the floating-gate.

5.2 Application of Floating-Gate Devices in Current Sources

Current sources used in DACs are required to meet strict matching conditions in order for the DAC to achieve its static linearity performance. For a MOSFET being used as a current source in a DAC, its matching properties are dependent upon the gate bias conditions as well as its size. Conventionally, the mismatch between neighbouring devices is reduced by either increasing the gate bias voltage, which introduces voltage head room problems, or by increasing the device size, which increases the area cost. However, additional problems are caused by parameter variations due to oxide thickness, mechanical stress and temperature gradients across a die. The effect of these variations can be minimised by using complex and time consuming common-centroid layout and special switching schemes. These expensive design solutions can be avoided by using a trimmable current source based on floating-gate technology. Since the output current of such a current source can be trimmed to the required level, the layout of the current sources of a DAC is no longer critical.

Four different trimmable current source architectures have been designed and tested. These current sources use a floating-gate device in three distinct ways: as a programmable current source, as a programmable voltage source and as a programmable resistor. The first current

source, TCS1, has two parallel branches consisting of a fixed and a trimmable output current branch. The trimmable branch consists of a floating-gate MOSFET which acts as programmable current source that is used to trim the output current. The fixed and trimmable branches of the current source are designed to supply 70% and 30% of the total output current respectively. This split was determined by analysing Monte Carlo statistical simulation of the fixed branch current source. Depending upon the level of mismatch, the trimming branch current can be either increased or decreased to achieve the required output current. Measurement results have shown that this current source has a sufficient trimming range to correct for mismatches with bias voltages up to $V_{bias} = 1.8V$. However, the drain-source voltage on the floating-gate device varies between 1.5V and 2.3V, which is likely to cause charge loss from the floating-gate voltage over time during normal operation.

TCS2 and TCS3 use the floating-gate MOSFET in an inverter and a source-follower respectively to create a trimmable voltage bias source to control the gate voltage of a MOSFET. Both of these current sources have the same trimming range as TCS1. With the gain of the inverter greater than unity, an increased programming speed is achieved from this circuit. One of the benefits of this increased speed is a lower manufacturing cost since more devices can now be programmed within a specific time. However, a disadvantage of a faster programming time is an increased sensitivity to charge loss which can negate the advantage of a operating the floating-gate MOSFET at a lower V_{ds} than TCS1.

The source-follower of TCS3 on the other hand has a gain of less than unity which reduces the sensitivity of the output current to changes in the floating-gate voltage. A disadvantage of this low gain is a slower programming rate. However, this circuit will have a longer charge retention period compared with TCS2.

The final current source described, TCS5, is based upon a circuit first proposed by Bugeja et al. [94]. This uses a floating-gate MOSFET in the linear region of operation to modulate the source voltage of a saturated MOSFET to generate the trimming branch current. The measured trimming range of this circuit is between 31% and 50% which is sufficient to correct for the expected mismatches. The drain-source voltage of the floating-gate MOSFET is always less

than 0.5V. Results have been presented which show that with this bias condition, the floating-gate does not suffer from any charge loss over a period of at least 7 days of normal operation. However, these results also show that effect of small temperature variations is more important than charge loss in this current source.

5.3 Effect of Temperature Variations

All the trimmable current sources are designed to eliminate the mismatch between current sources in an array. Ideally, the current sources will be trimmed only once immediately after fabrication. This means that the current sources must remain matched throughout their operating life. Apart from charge leakage from the floating-gate, any variation of temperature can introduce mismatches between the current sources. It is therefore desirable to be able to operate the current sources at a bias condition which will minimise the effect of temperature variations during operation.

The temperature response of a MOSFET is dependent upon the temperature response of the threshold voltage and the transconductance parameter, β which are both technology dependent. It has been shown that any MOSFET can have a zero temperature coefficient (ZTC) bias point. However, to achieve true temperature independence, the mobility temperature exponent is required to have a value of -2. For the $0.35\mu\text{m}$ technology used, this exponent is -1.8 which resulted in a ZTC bottle neck around a gate voltage of 0.88V instead of a single point. These results are consistent with the simple first order model used to predict the ZTC “point”. This simple model is also used to show that the ZTC “point” is very sensitive to the MOSFET gate and drain bias conditions. Since a MOSFET is the main component of a current source, these results are used as a basis for the analysis of the effect of temperature variations on the trimmable current sources.

The MOSFET temperature experiments used a gate bias source that was temperature independent. However, all the fixed branch MOSFETs of the trimmable current sources are biased by a bias generator circuit shown in Figure 3.2 and the trimmable branches of TCS2 and TCS3

are biased with floating-gate based inverter and source-follower. The output of all of these bias circuits is temperature dependent. The effect of temperature on the output current is therefore a combination of the temperature response of a MOSFET with a fixed bias source and temperature variation of the gate voltage of the MOSFET. The position of the ZTC current can therefore either increase or decrease relative to the MOSFET ZTC current depending upon the temperature gradient of the gate bias voltage. Simulation results of the bias circuit of the fixed branch MOSFETs have shown that the bias voltage has a positive temperature gradient, which has the effect of increasing the ZTC output current of the fixed branch. Similarly, in the case of the inverter, the trimming bias voltage also has a positive temperature gradient, which increases the ZTC current relative to a MOSFET with a fixed input. On the other hand, the temperature response of the source-follower of TCS3 shows a negative temperature gradient which is so strong that no ZTC “point” is observed. By biasing TCS1 and TCS2 at the ZTC “point”, a temperature insensitive current source can be obtained. However, this temperature insensitivity is not maintained over a range of currents. These current sources are therefore either trimmable or temperature insensitive.

The final current source, TCS5, consists of a fixed branch, whose temperature response is the same as the other current sources, and a trimmable branch with two MOSFETs in series with one acting as a programmable resistor. The temperature dependence model of the trimmable branch, derived from first principles, has shown that the ZTC “point” moves along an arc as the trimming voltage is varied. An operating point has been identified from simulations which results in the trimmable output current having a very weak temperature dependency ($0.005\%/^{\circ}\text{C}$) over current trimming range of 17%. This is equivalent to a maximum temperature increase of 60°C in order to remain within a mismatch of 0.3%, which corresponds to a resolution of 12-bits. These results are confirmed by the measured temperature response of output current of TCS5 as shown in Figure 4.18.

TCS5, therefore, combines the advantages of a floating-gate device biased at a very low V_{ds} with the ability to maintain a weak temperature dependency over a large trimming range that is required to eliminate device mismatches.

This thesis has shown that a trimmable current source designed using floating-gate device technology can be used to simplify the design process of a current steering DAC. With a sufficient trimming range to correct for any device mismatches, the trimmable current source with a linear mode floating-gate device (TCS5) is also able to retain the programmed output current over a period of at least several days of continuous operation as well as being insensitive to variations in operating temperature. These characteristics make it suitable for use in a DAC implemented in a SoC.

5.4 Future Work

The floating-gate devices implemented in a $0.35\mu\text{m}$ CMOS process have shown that they have the potential to be used as a trimming element in a current source. However, several problems, which need to be resolved before this technology can be confidently used, have been identified in this thesis.

Experimental results have shown that the floating-gate can lose charge during handling. It was concluded that conventional ESD protection of the control-gate is not sufficient to stop this leakage from the floating-gate. It is therefore necessary to investigate better protection circuits. One possibility is to use a source-follower as a buffer between the bond-pad and the control-gate of the floating-gate. This source-follower would absorb any transients which are able to pass through the conventional ESD protection of the bond-pad.

The long term retention experiments showed a relaxation phenomenon over a period of approximately an hour. This relaxation is thought to be caused by the charge carriers filling carrier traps at the $\text{Si} - \text{SiO}_2$ interface left vacant due to the shift in the floating-gate voltage. In order to verify this hypothesis, further experiments are required to determine the relationship between the magnitude of the shift in the floating-gate voltage and the amount of relaxation. If this hypothesis is correct, then the amount of relaxation will be proportional to the shift in the floating-gate voltage. By being able to predict this shift in the floating-gate voltage, a programming scheme can be devised to take into account the effect of the relaxation. This will

avoid the need to re-program a floating-gate device.

Another critical issue with using this technology in trimming applications, is the retention characteristics of the floating-gate device during operation. Several experiments have shown that the floating-gate can gain electrons by CHEI even when the sense MOSFET is biased at a V_{ds} less than 3.2V, which is the minimum voltage required by the electrons to gain enough energy to cross the $Si - SiO_2$ energy barrier. This phenomenon, thought to be caused by hot electrons gaining energy through carrier-to-carrier interactions, has been observed at V_{ds} as low as 1V. Further experiments at lower V_{ds} are required to develop a model for charge loss at low drain bias voltages. This model could then be used to design the optimum operating conditions of the floating-gate device in order to minimise charge loss from the floating-gate.

The CHEI selection circuit consists of an AND gate whose output provides the programming voltage. However, the output voltage from this simple circuit is reduced if too much current is drawn by the programming transistor. Therefore, an alternative programming circuit which can guarantee the level of the programming voltage is required.

Furthermore, the area of the implemented floating-gate element is dominated by the two programming selection circuits which are included in each element. A global programming scheme which can apply either programming voltage to a particular floating-gate element is required. The size of the element can be reduced further by reducing the size of the floating-gate capacitor since the device does not suffer from charge leakage if biased appropriately. As well as offering a simple design flow for a DAC, this smaller floating-gate device could offer a significant reduction in silicon area.

TCS5 is a current source that is trimmable over a temperature insensitive range of 17%. A larger range would make this current source more versatile. The results in Appendix A show that the temperature coefficient of a linear trimming resistor needs to be $-0.003/K^{-1}$ to achieve a temperature insensitive current range of almost 100%. To increase the trimming range of TCS5 further, the temperature response of the linear MOSFET must be modified to that of a linear resistor. The temperature model developed for TCS5 assumed that the floating-gate voltage is independent of temperature. One way of changing the temperature characteristics of

the linear MOSFET is to provide a temperature dependent voltage to the control-gate. Therefore a modified model is required to predict the necessary temperature response of this voltage in order change the temperature response of the linear floating-gate MOSFET.

The original aim of these trimmable current sources was to simplify the design of conventional high speed current steering DACs. Another similar application which is suitable for a trimmable current source is a current steering non-linear DAC which is part of a low power direct digital frequency synthesis (DDFS) system [101]. A DDFS system is ideal for integration into a communications system. This introduces the possibility of variations in the DAC output due to temperature gradients. The size of the current sources of the DAC varies non-linearly with each input bit. This requirement makes it very difficult to create matched current sources out of identically sized MOSFETs. A trimmable temperature invariant current source which has a large programmable output range would simplify the design and layout of the non-linear DAC considerably.

5.5 Conclusions

This project sets out to examine the hypothesis that floating-gate devices can be used to create current sources, for use in high precision current steering DACs, which are both trimmable as well as temperature insensitive. It is also expected that these devices can be operated such that they are able to retain the programmed output current during normal operation.

The trimmable current sources are programmed to output a specific current using n-channel floating-gate devices. The programming characteristics of these devices were investigated. Experimental results showed that CHEI and tunneling can be used to decrease and increase the floating-gate voltage respectively. As expected the tunneling current was shown to be consistent with FNT. Previous work on electron injection by Diorio et al. had suggested a model for impact ionisation channel hot electron injection in a p-channel floating-gate device. This model has been extended in this thesis to include an exponential variation in the gate current due to the floating-gate voltage observed in the data, but, not included in the Diorio model.

An alternative new model was also investigated that matched the data over a similar range of bias conditions. However, neither model can account for the peak in the gate-current at high floating-gate voltages. Further work is therefore required to improve these models. However, observed variability in the CHEI and FNT characteristics mean that programming must be done in feedback, which limits the usefulness of any model. The proposed models can be used to estimate the programming rates that can be achieved with specific bias conditions. In addition, the programming characteristics of the floating-gate device are also useful in determining the operating range of a floating-gate device in any circuit.

The data retention characteristics of programmed devices were investigated. During these experiments, sudden changes in floating-gate voltages were observed when a device was handled. It is believed that this previously unreported behaviour explains previous results reported by Millard et al., who assumed that any charge loss observed after storing a device for several months was due to gradual loss from the floating-gate. Further work is required to investigate and eliminate this behaviour.

When the current through a floating-gate device is monitored continuously over several days good charge retention characteristics are observed. However, these results were observed with low drain-source voltages on the floating-gate device. These results are consistent with soft-programming characteristics in EEPROM devices as reported by Ghetti et al.. Previous claims about good retention characteristics of floating-gate devices implemented in sub-micron technologies have relied on the assumption that with a V_{dd} of 3.3V, the electrons can never gain enough energy to be able to leave or enter the floating-gate via the SiO_2 barrier. Ghetti et al. and the experimental results reported in this thesis have shown that this assumption is invalid. Therefore, in order to minimise the charge loss, the floating-gate device must be biased with a very low V_{ds} .

With the floating-gate device biased with a low V_{ds} during retention experiments, the effect of temperature fluctuations of less than 1 degree were observed. The importance of the effect of small temperature variations on the accuracy of a trimmable current source has been recognised for the first time.

Several different circuit designs which use a floating-gate device to trim the output current were compared. Each design consists of a trimmable and a non-trimmable branch in order to reduce sensitivity to charge leakage from the floating-gate. The current source which uses the floating-gate device as a programmable resistor has been shown to have the required bias conditions for the retention of charge on the floating-gate. With good data retention possible, the accuracy of the trimmable current sources is therefore limited by the sensitivity to variations in temperature.

The temperature sensitivity of each design was analysed. It was shown that in one of the designs, as the current source is trimmed, the previously reported single ZTC point of a MOS-FET was transformed into a locus of ZTC points. A bias condition is thus identified which can be used to create a temperature insensitive current source over a significant current range.

This thesis has shown that floating-gate devices can be used to create trimmable current sources that are both trimmable and temperature insensitive. The trimmable current sources can be operated under conditions which enable the retention of the programmed output current under normal operation.

Appendix A

Resistor Model

The trimmable branch of TCS5 can be modelled as a MOSFET in series with resistor instead of the trimmable MOSFET operating in the linear region. The output current equation is therefore

$$\begin{aligned} I_{out} &= \frac{\beta}{2} (V_G - V_S - V_{th})^2 \\ &= \frac{\beta}{2} (V_G - I_{out}R - V_{th})^2 \end{aligned} \quad (\text{A.1})$$

The temperature dependence of the output current is given by

$$\frac{dI_{out}}{dT} = \left. \frac{\partial I_{out}}{\partial T} \right|_{MOS} + \frac{\partial I_{out}}{\partial V_{gs}} \frac{\partial V_{gs}}{\partial T} \quad (\text{A.2})$$

where $\left. \frac{\partial I_{out}}{\partial T} \right|_{MOS}$ is the temperature dependence of MOSFET with a fixed bias and $\frac{\partial I_{out}}{\partial V_{gs}} \frac{\partial V_{gs}}{\partial T}$ is the response due to temperature variations of the gate-source voltage. The temperature dependence of the resistor is modelled as [97]

$$R = R_0(1 + \alpha_r(T - T_0)) \quad (\text{A.3})$$

where α_r is the temperature coefficient of the resistor and R_0 is the resistance at a reference

temperature T_0 .

$$\begin{aligned}\frac{\partial V_{gs}}{\partial T} &= -\frac{\partial V_S}{\partial T} \\ &= -\alpha_r R_0 I_{out}\end{aligned}\tag{A.4}$$

From Equation 4.52

$$\frac{\partial I_{out}}{\partial V_{gs}} = \beta(V_{gs} - V_{th})\tag{A.5}$$

The overall temperature dependence is therefore

$$\frac{\partial I_{out}}{\partial T} = \frac{\alpha_u \beta}{2T} (V_{gs} - V_{th})^2 - \beta \alpha_{vt} (V_{gs} - V_{th}) - \beta \alpha_r R_0 I_{out} (V_{gs} - V_{th})\tag{A.6}$$

At the ZTC point, $\frac{\partial I_{out}}{\partial T} = 0$, $V_G = V_{G|ZTC}$ and $I_{out} = I_{out|ZTC}$. Simplifying Equation A.6

$$\frac{\alpha_u}{2T} (V_{gs|ZTC} - V_{th}) - \alpha_{vt} - \alpha_r R_0 I_{out|ZTC} = 0\tag{A.7}$$

$$\frac{\alpha_u}{2T} (V_{G|ZTC} - I_{out|ZTC} R - V_{th}) - \alpha_{vt} - \alpha_r R_0 I_{out|ZTC} = 0\tag{A.8}$$

$$\begin{aligned}\alpha_u V_{G|ZTC} &= I_{out|ZTC} (\alpha_u R + 2T \alpha_r R_0) + \alpha_u V_{th} + 2T \alpha_{vt} \\ &= I_{out|ZTC} [\alpha_u R_0 + \alpha_u \alpha_r R_0 (T - T_0) + 2T \alpha_r R_0] + \alpha_u V_{th} + 2T \alpha_{vt}\end{aligned}\tag{A.9}$$

Simulation of the circuit showed that for a particular α_r , $V_{G|ZTC}$ is independent of $I_{out|ZTC}$ as the resistance changes. Therefore, $\frac{\partial V_{G|ZTC}}{\partial I_{out|ZTC}} = 0$;

$$\alpha_u R_0 + \alpha_u \alpha_r R_0 (T - T_0) + 2T \alpha_r R_0 = 0\tag{A.10}$$

The temperature coefficient which satisfies this condition is

$$\alpha_r |_{\frac{\partial V_{G|ZTC}}{\partial I_{out|ZTC}}=0} = \frac{-\alpha_u}{2T + \alpha_u (T - T_0)}\tag{A.11}$$

Using the technology parameters in Table 4.1, the temperature coefficients are evaluated for

$(T - T_0)$	$\alpha_r (10^{-3} K^{-1})$
0	3.00
10	2.99
20	2.98
30	2.97
40	2.96
50	2.95
60	2.94

Table A.1: *Temperature Coefficient Variation*

various temperatures which are shown in Table A.1. Over a $60K$ change in temperature, the temperature coefficient does not change significantly.

The constant ZTC gate voltage can also be determined from Equation A.9.

$$\begin{aligned}
 V_{G|ZTC} &= V_{th} + \frac{2T\alpha_{vt}}{\alpha_u} \\
 &= V_{th0} + \alpha_{vt}(T - T_0) + \frac{2T\alpha_{vt}}{\alpha_u} \\
 &= V_{th0} - \alpha_{vt}T_0 + \alpha_{vt}T \left(1 + \frac{2}{\alpha_u}\right)
 \end{aligned} \tag{A.12}$$

This equation is exactly the same as that found for a stand alone MOSFET, Equation 4.12. The above analysis does not take in to account the back-gate effect. Therefore in practice the ZTC gate voltage will tend to be slightly greater than the expected voltage determined from the above equations.

Equation A.12 is substituted into Equation 4.1 to determine $I_{out|ZTC}$ variation with resistance.

$$V_{G|ZTC} - V_{th} = \frac{2T\alpha_{vt}}{\alpha_u} \tag{A.13}$$

$$I_{out|ZTC} = \frac{\beta}{2} \left[\frac{2T\alpha_{vt}}{\alpha_u} - I_{out|ZTC}R \right]^2 \tag{A.14}$$

$$\frac{2I_{out|ZTC}}{\beta} = \frac{4\alpha_{vt}^2 T^2}{\alpha_u^2} - \frac{4T\alpha_{vt}}{\alpha_u} I_{out|ZTC}R + I_{out|ZTC}^2 R^2 \tag{A.15}$$

$$I_{out|ZTC}^2 R^2 - I_{out|ZTC} \left(\frac{2}{\beta} + \frac{4T\alpha_{vt}}{\alpha_u} R \right) + \frac{4\alpha_{vt}^2 T^2}{\alpha_u^2} = 0 \tag{A.16}$$

This quadratic equation can be solved to give

$$I_{out|ZTC} = \frac{1}{\beta R^2} + \frac{2T\alpha_{vt}}{\alpha_u R} \pm \frac{1}{\beta R^2} \sqrt{1 + \frac{4T\alpha_{vt}\beta R}{\alpha_u}} \quad (\text{A.17})$$

By setting $R \rightarrow 0$, the solution is

$$I_{out|ZTC} = \frac{1}{\beta R^2} + \frac{2T\alpha_{vt}}{\alpha_u R} \pm \frac{1}{\beta R^2} \sqrt{1 + \frac{4T\alpha_{vt}\beta R}{\alpha_u}} \quad (\text{A.18})$$

This solution describes a ZTC output current which is independent of the ZTC gate voltage. For the general case, $\frac{\partial V_{G|ZTC}}{\partial I_{out|ZTC}} \neq 0$ and $\alpha_r|_{\frac{\partial V_{G|ZTC}}{\partial I_{out|ZTC}}=0} \neq \alpha_r$; the gate voltage from Equation A.1 is

$$V_{G|ZTC} = I_{out|ZTC} R + \sqrt{\frac{2}{\beta} I_{out|ZTC}} + V_{th} \quad (\text{A.19})$$

Substituting $V_{G|ZTC}$ from Equation A.19 into Equation A.7

$$I_{out|ZTC} \alpha_r R_0 - \frac{\alpha_u}{2T} \sqrt{\frac{2}{\beta} I_{out|ZTC}} + \alpha_{vt} = 0 \quad (\text{A.20})$$

Solving this quadratic equation gives

$$\sqrt{I_{out|ZTC}} = \frac{\alpha_u}{2\alpha_r R_0 T \sqrt{2\beta}} - \frac{1}{2\alpha_r R_0} \sqrt{\frac{\alpha_u^2}{2\beta T^2} - 4\alpha_{vt}\alpha_r R_0} \quad (\text{A.21})$$

The variation of the ZTC point with the temperature coefficient is simulated in Matlab using Equations A.19 and A.21 and is plotted in Figure A.1 for resistance increasing from $1k\Omega$ to $5k\Omega$. When $\alpha_r = 0$, the ZTC current is constant whilst the ZTC gate voltage increases with increasing resistance. However, as expected, as the temperature coefficient increases to $3e - 3$, the ZTC current is seen to be independent of the gate voltage, $V_{G|ZTC} = 0.899V$, and therefore only dependent on the resistor value. This gate voltage is predicted by Equation A.12. When biased at this gate voltage, this circuit can be used generate a temperature invariant current which is dependent only on a resistor with a temperature coefficient of $3e - 3$.

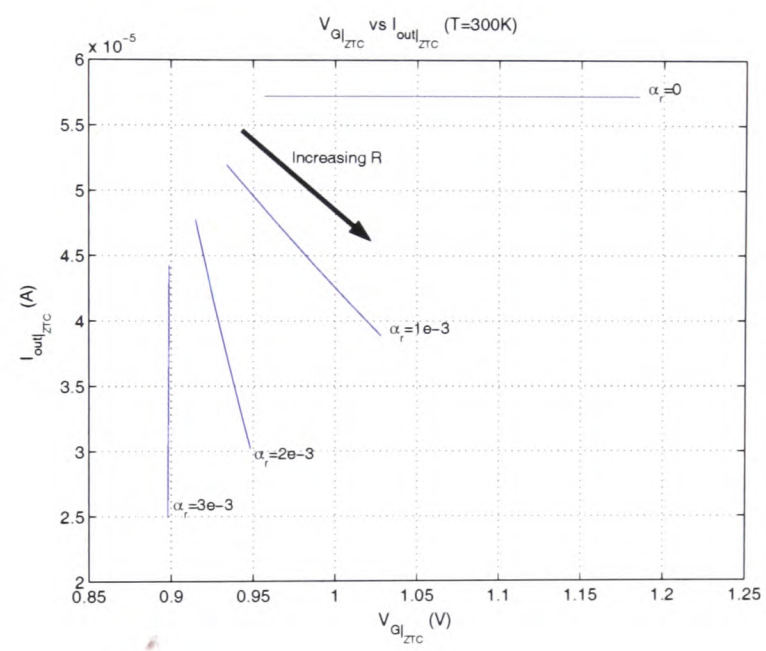


Figure A.1: ZTC point variation with α_r

Bibliography

- [1] Alessandro Cremonesi, Franco Maloberti and Gino Polito, "A 100-MHz CMOS DAC for Video-Graphic Systems," *IEEE J. Solid-State Circuits*, vol. 24, no. 3, pp. 635–639, June 1989.
- [2] Mika P. Tiilikainen, "A 14-bit 1.8-V 20-mW 1-mm² CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1144–1147, July 2001.
- [3] Chi-Hung Lin and Klaas Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6mm²," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1948–1958, December 1998.
- [4] Yonghua Cong and Randall L. Geiger, "Switching Sequence Optimization for Gradient Error Compensation in Thermometer-Decoded DAC Arrays," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 7, pp. 585–595, July 2000.
- [5] Nianxiong Tan, Ellie Cijvat and Hannu Tenhunen, "Design and Implementation of High-Performance CMOS D/A Converter," in *IEEE International Symposium on Circuits and Systems*, June 1997, pp. 421–424.
- [6] Tien-Yu Wu, Ching-Tsing Jih, Jueh-Chi Chen and Chung-Yu Wu, "A Low Glitch 10-bit 75-MHz CMOS Video D/A Converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 1, pp. 68–72, January 1995.
- [7] Jose Bastos, Michel S. J. Steyaert, Anelia Pergoot and Willy M. Sansen, "Influence of Die Attachment on MOS Transistor Matching," *IEEE Transactions on Semiconductor Manufacturing*, vol. 10, no. 2, pp. 209–219, May 1997.
- [8] G. Van der Plas, J. Vandebussche, W. Daems, A Van den Bosch, G. Gielen, M. Steyaert and W. Sansen, "Systematic Design of a 14-bit 150-MS/s CMOS Current-Steering D/A Converter," in *Proceedings of Design Automation Conference*. IEEE, 2000, pp. 452–457.
- [9] Anne Van den Bosch, Marc A. F. Borremans, Michel S. J. Steyaert and Willy Sansen, "A 10-bit 1 GSample/s Nyquist Current-Steering CMOS D/A Converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 315–324, March 2001.
- [10] J. Jacob Wikner and Nianxiong Tan, "Modeling of CMOS Digital-to-Analog Converters for Telecommunications," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 5, pp. 489–499, May 1999.

- [11] J. Jacob Wikner and Nianxiong Tan, "Influence of Circuit Imperfections on the Performance of DACs," *Analog Integrated Circuits and Signal Processing*, vol. 18, no. 1, pp. 7–20, January 1999.
- [12] Marcel J. M. Pelgrom, Aad C. J. Duinmaijer and Anton P. G. Welbers, "Matching Properties of MOS Transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1440, October 1989.
- [13] Michael Mojal, "Multi Bit DAC with corrective gate to drain voltage for optimum matching under Gradient Temperature effects," in *IEEE International Conference on Electronics, Circuits and Systems*, 1998, vol. 1, pp. 139–142.
- [14] Eric Felt, Amit Narayan and Alberto Sangiovanni-Vincentelli, "Measurement and Modeling of MOS Transistor Current Mismatch in Analog IC's," in *Proceedings of IEEE/ACM International Conference on Computer Aided Design*, 1994, pp. 272–277.
- [15] Jose Bastos, Augusto M. Marques, Michel S. J. Steyaert and Willy Sansen, "A 12-bit Intrinsic Accuracy High-Speed CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1959–1969, December 1998.
- [16] Alan Hastings, *The Art of Analog Layout*, Prentice Hall, 2001.
- [17] G. Van der Plas, J. Vandebussche, A. Van den Bosch, M. Steyaert, W. Sansen and G. Gielen, "MOS Transistor Mismatch for High Accuracy Applications," in *Proceedings of the 10th ProRISC/IEEE Workshop*, 1999, pp. 529–534.
- [18] J. Vandebussche, G. Van der Plas, A. Van den Bosch, W. Daems, G. Gielen, M. S. J. Steyaert and W. Sansen, "A 14b 150MSample/s update rate Q^2 random walk," in *ISSCC Dig. Tech. Papers*, 1999, pp. 146–147.
- [19] Yasuyuki Nakamura, Takahiro Miki, Atsushi Maeda, Harufusa Kondoh and Nobuharu Yazawa, "A 10-b 70-MS/s CMOS D/A Converter," *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 637–642, April 1991.
- [20] Alex R. Bugeja and Bang-Sup Song, "A Self-Trimming 14-b 100-MS/s CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 25, no. 12, pp. 1841–1852, December 2000.
- [21] Shu-Yuan Chin and Shung-Yu Wu, "A 10-b 125 MHz CMOS Digital-to-Analog Converter (DAC) with Threshold-Voltage Compensated Current Sources," *IEEE J. Solid-State Circuits*, vol. 29, no. 11, pp. 1374–1380, November 1994.
- [22] Miguel Figueroa, John Hyde, Todd Humes and Chris Diorio, "A Floating-Gate Trimmable High-Resolution DAC in Standard $0.25\mu\text{m}$ CMOS," in *Proceedings of the Nonvolatile Semiconductor Memory Workshop*, 2001, pp. 46–47.
- [23] D. Kahng and S. M. Sze, "A floating-gate and its application to memory devices," *The Bell System Technical Journal*, vol. 46, no. 4, pp. 1288–1295, 1967.
- [24] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim tunneling into thermally grown SiO_2 ," *J. of Appl. Phys.*, vol. 40, no. 6, pp. 278–283, 1969.

- [25] D. Frohman-Bentchkowsky, "A fully decoded 2048-bit electrically programmable FAMOS read-only memory," *IEEE J. Solid-State Circuits*, vol. 6, no. 5, pp. 301–306, October 1971.
- [26] D. Frohman-Bentchkowsky, "Memory behaviour in a floating-gate avalanche-injection MOS (FAMOS) structure," *Applied Physics Letters*, vol. 18, no. 15, pp. 332–334, April 1971.
- [27] Mark Holler, Simon Tam, Hernan Castro and Ronald Benson, "An Electrically Trainable Artificial Neural Network," in *International Joint Conference on Neural Networks*, 1989, pp. 191–196.
- [28] Frank Goodenough, "Single IC Stores And Plays Back 4 Minutes Of Voice," *Electronic Design*, pp. 67–76, 22 July 1996.
- [29] Advanced Linear Devices, Inc, <http://www.aldinc.com>, *Electrically Programmable Analog Device (EPADTM)*.
- [30] T. Shibata and T. Ohmi, "A functional MOS Transistor featuring gate-level weighted-sum and threshold operations," *IEEE Transactions on Electron Devices*, vol. 39, pp. 1444–1455, 1992.
- [31] T. Shibata and T. Ohmi, "Neuron MOS binary-logic integrated circuits-Part I: design fundamentals and soft-hardware-logic circuit implementation," *IEEE Transactions on Electron Devices*, vol. 40, pp. 570–576, 1993.
- [32] T. Shibata and T. Ohmi, "Neuron MOS binary-logic integrated circuits-Part II: simplifying techniques of circuit configuration and their practical applications," *IEEE Transactions on Electron Devices*, vol. 40, pp. 974–979, 1993.
- [33] Werner Weber, Stefan J. Prange, Roland Thewes, Erdi Wohlrab and Andreas Luck, "On the Application of the Neuron MOS Transistor Principle for Modern VLSI Design," *IEEE Transactions on Electron Devices*, vol. 43, no. 10, pp. 1700–1708, October 1996.
- [34] Katsuhisa Ogawa, Tadashi Shibata, Tadahiro Ohmi, Motomu Takatsu and Naoki Yokoyama, "Multiple-Input Neuron MOS Operational Amplifier for Voltage-Mode Multivalued Full Adder," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 45, no. 9, pp. 1307–1311, September 1998.
- [35] Koichi Tanno, Pkihiko Ishizuka and Zheng Tang, "A 1-V, 1-V_{p-p} Input Range, Four Quadrant Analog Multiplier Using Neuron-MOS Transistors," *IEICE Trans. Electron.*, vol. E82-C, no. 5, pp. 750–757, May 1999.
- [36] Massimo Lanzoni, G. Tondi, P. Galbiati and Bruno Ricco, "Automatic and Continuous Offset Compensation of MOS Operational Amplifiers Using Floating-Gate Transistors," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 287–290, February 1998.
- [37] Paul Hasler, Bradley A. Minch and Chris Diorio, "An Autozeroing Floating-Gate Amplifier," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 48, no. 1, pp. 74–82, January 2001.

- [38] Y. Berg, O. Naess, M. Hovin and H. Gundersen, "Ultra Low-Voltage Floating-Gate (FGUVMOS) Amplifiers," *Analog Integrated Circuits and Signal Processing*, vol. 26, pp. 63–73, January 2001.
- [39] Y. Berg, T. S. Lande, O. Naess and H. Gundersen, "Ultra Low-Voltage Floating-Gate Transconductance Amplifiers," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 48, no. 1, pp. 37–44, January 2001.
- [40] Miguel Figueroa, David Hsu and Chris Diorio, "A mixed-signal approach to high-performance, low-power linear filters," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 816–822, May 2001.
- [41] M. Kucic, P. Hasler, J. Dugger and D. Anderson, "Programmable and adaptive analog filters using arrays of floating-gate circuits," in *Proceedings of the Conference on Advanced Research in VLSI*, 2001, pp. 148–162.
- [42] Chris Diorio, Paul Hasler, Bradley A. Minch and Carver A. Mead, "A Single-Transistor Silicon Synapse," *IEEE Transactions on Electron Devices*, vol. 43, no. 11, pp. 1972–1978, November 1996.
- [43] Chris Diorio, Paul Hasler, Bradley A. Minch and Carver Mead, "A Floating-Gate MOS Learning Array with Locally Computed Weight Updates," *IEEE Transactions on Electron Devices*, vol. 44, no. 12, pp. 2281–2289, December 1997.
- [44] Chris Diorio, "A p-Channel MOS Synapse Transistor with Self-Convergent Memory Writes," *IEEE Transactions on Electron Devices*, vol. 47, no. 2, pp. 464–472, February 2000.
- [45] Chris Diorio, David Hsu and Miguel Figueroa, "Adaptive CMOS: From Biological Inspiration to Systems-on-a-Chip," *Proceedings of the IEEE*, vol. 90, no. 3, pp. 345–357, March 2002.
- [46] Paul Hasler, Chris Diorio and Bradley A. Minch, "A Four-Quadrant Floating-Gate Synapse," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, 1998, vol. 3, pp. 29–32.
- [47] Paul Hasler and Jeff Dugger, "Correlation Learning Rule in Floating-Gate pFET Synapses," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 48, no. 1, pp. 65–73, January 2001.
- [48] Chris Diorio, Sunit Mahajan, Paul Hasler, Bradley Minch and Carver Mead, "A High-Resolution Nonvolatile Analog Memory Cell," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, 1995, vol. 3, pp. 2233–2236.
- [49] Paul Hasler, Bradley A. Minch and Chris Diorio, "Floating-Gate Devices: They are not just for Digital Memories Anymore," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, 1999, vol. 2, pp. 388–391.
- [50] Reid R. Harrison, Julian A. Bragg, Paul Hasler, Bradley A. Minch and Stephen P. De-weerth, "A CMOS Programmable Analog Memory-Cell Array Using Floating-Gate Circuits," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 4–11, January 2001.

- [51] Chris Duffy, Ethan Farquhar and Paul Hasler, “Practical Issues using E-Pot Circuits,” in *Proceedings of the IEEE International Symposium on Circuits and Systems*, 2002, vol. 5, pp. 493–496.
- [52] Paul D. Smith, Matt Kucic and Paul Hasler, “Accurate Programming of Analog Floating-Gate Arrays,” in *Proceedings of the IEEE International Symposium on Circuits and Systems*, 2002, vol. 5, pp. 489–492.
- [53] Leland Chang, Charles Kuo, Chenming Hu, Alexander Kalnitsky, Albert Bergement and Pascale Francis, “A CMOS-Compatible Single-Poly Cell for Use as Non-Volatile Memory,” in *Proceedings of the International Semiconductor Device Research Symposium*, 1999.
- [54] Scott A. Jackson, Jacob C. Killens and Benjamin J. Blalock, “A Programmable Current Mirror for Analog Trimming Using Single-Poly Floating-Gate Devices in Standard CMOS Technology,” *IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing*, vol. 48, no. 1, pp. 100–102, January 2001.
- [55] Boaz Eitan and Dov Frohman-Bentchkowsky, “Hot-Electron Injection into the Oxide in n-Channel MOS Devices,” *IEEE Transactions on Electron Devices*, vol. 28, no. 3, pp. 328–340, March 1981.
- [56] Nelson S. Saks, Paul L. Heremans, Luc Van Den Hoven, Hereman E. Maes, Roger F. De Keersmaecker and Gilbert J. Declerck, “Observation of Hot-Hole Injection in NMOS Transistors Using a Modified Floating-Gate Technique,” *IEEE Transactions on Electron Devices*, vol. 33, no. 10, pp. 1529–1533, October 1986.
- [57] Vei-Han Chan and James E. Chung, “The Impact of NMOSFET Hot-Carrier Degradation on CMOS Analog Subcircuit Performance,” *IEEE J. Solid-State Circuits*, vol. 30, no. 6, pp. 644–649, June 1995.
- [58] Roland Thewes, Martin Brox, Karl F. Goser and Werner Weber, “Hot-Carrier Degradation of p-MOSFET’s Under Analog Operation,” *IEEE Transactions on Electron Devices*, vol. 44, no. 4, pp. 607–617, April 1997.
- [59] Roland Thewes and Werner Weber, “Effects of Hot-carrier Degradation in Analog CMOS Circuits,” *Microelectronic Engineering*, vol. 36, pp. 285–292, 1997.
- [60] Yu-Sheng Tang, Yue Hao and Ming-Yu Wang, “Analytic Models of Drain, Substrate and Gate Current Distributions in the Drain Section of MOSFETs,” *IEEE Transactions on Electron Devices*, vol. 48, no. 10, pp. 2279–2291, October 2001.
- [61] David Esseni, Luca Selmi, Andrea Ghetti and Enrico Sangiorgi, “Injection Efficiency of CHISEL Gate Currents in Short MOS Devices: Physical Mechanisms, Device Implications and Sensitivity to Technological Parameters,” *IEEE Transactions on Electron Devices*, vol. 47, no. 11, pp. 2194–2200, November 2000.
- [62] Rudi Bellens, Guido Groeseneken, Paul Heremans and Herman E. Maes, “Hot-Carrier Degradation Behaviour of N- and P-Channel MOSFET’s Under Dynamic Operation Conditions,” *IEEE Transactions on Electron Devices*, vol. 41, no. 8, pp. 1421–1428, August 1994.

- [63] J. F. Zhang, H. K. Sii, Guido Grieseneken and Robin Degraeve, "Hole Trapping and Trap Generation in the Gate Silicon Dioxide," *IEEE Transactions on Electron Devices*, vol. 48, no. 6, pp. 1127–1135, June 2001.
- [64] K. Michael Han and Chih-Tang Sah, "Positive Oxide Charge from Hot Hole Injection During Channel-Hot-Electron Stress," *IEEE Transactions on Electron Devices*, vol. 45, no. 7, pp. 1624–1627, July 1998.
- [65] D. Vuillaume, "Hot-Carrier Injections in SiO_2 ," *Microelectronics Reliability*, vol. 38, no. 1, pp. 7–22, 1998.
- [66] H. E. Maes, G. Groeseneken, R. Degraeve, J. De Blauwe and G. Van den bosch, "Assessment of oxide reliability and hot carrier degradation in CMOS technology," *Microelectronic Engineering*, vol. 40, pp. 147–166, 1998.
- [67] Alexandre Acovic, Guiseppe La Rosa and Yuan-Chen Sun, "A Review of Hot-Carrier Degradation Mechanisms in MOSFETs," *Microelectronic Reliability*, vol. 36, no. 6/7, pp. 845–869, 1996.
- [68] Paul Heremans, Rudi Bellens, Guido Groeseneken and Herman E. Maes, "Consistent Model for the Hot-Carrier Degradation in n-Channel and p-Channel MOSFET's," *IEEE Transactions on Electron Devices*, vol. 35, no. 12, pp. 2194–2209, December 1988.
- [69] Helmuth Gesch, Jean-Pierre Leburton and Gerard E. Dorda, "Generation of Interface States by Hot Hole Injection in MOSFET's," *IEEE Transactions on Electron Devices*, vol. 29, no. 5, pp. 913–918, May 1982.
- [70] G. Groeseneken, R. Bellens, G. Van den bosch and H. E. Maes, "Hot-carrier degradation in submicrometre MOSFETs: from uniform injection towards the real operating conditions," *Semicond. Sci. Technol.*, vol. 10, pp. 1208–1220, 1995.
- [71] Karl R. Hofmann, Christoph Werner, Werner Weber and Gerhard Dorda, "Hot-Electron and Hole-Emission Effects in Short n-Channel MOSFET's," *IEEE Transactions on Electron Devices*, vol. 32, no. 3, pp. 691–699, March 1985.
- [72] D. Goguenheim, A. Bravaix, D. Vuillaume, F. Mondon, M. Jourdain and A. Meinertzhagen, "Stress induces leakage currents in N-MOSFETs submitted to channel hot carrier injections," *Journal of Non-Crystalline Solids*, vol. 245, pp. 41–47, 1999.
- [73] R. Thewes, R. Brederlow, C. Schulunder, P. Wiczorek, B. Ankele, A. Hesener, J. Holz, S. Kessel and W. Weber, "MOS Transistor Reliability under Analog Operation," *Microelectronics Reliability*, vol. 40, pp. 1545–1554, 2000.
- [74] Cheng T. Wang, *Hot carrier design considerations for MOS devices and circuits*, Van Nostrand Reinhold, 1992.
- [75] Eiji Takeda, *Hot-carrier effects in MOS devices*, Academic Press, 1995.
- [76] R. H. Fowler and L. Nordheim, "Electron Emission in Intense Electric Fields," *Proc. Roy. Soc. Lond.*, vol. 119, pp. 173–181, 1928.

- [77] S. M. Sze, *Physics of Semiconductor Devices*, Wiley, 1981, 2nd Edition.
- [78] E. Sackinger and W. Guggenbuehl, "An analog trimming circuit based on a floating-gate," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1437–1440, December 1988.
- [79] R. K. Ellis, "Fowler-Nordheim emission from non-planar surfaces," *IEEE Electron Device Letters*, vol. 3, pp. 330–332, 1982.
- [80] Chi-Kai Sin, Alan Kramer, V. Hu, Robert R. Chu and Ping K. Ko, "EEPROM as an Analog Storage Device, with Particular Applications in Neural Networks," *IEEE Transactions On Electron Devices*, vol. 39, no. 6, pp. 1410–1419, June 1992.
- [81] L. Richard Carley, "Trimming Analog Circuits Using Floating-Gate Analog MOS Memory," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1569–1575, December 1989.
- [82] Axel Thomsen and Martin A. Brooke, "A Floating-Gate MOSFET with Tunneling Injector Fabricated Using a Standard Double-Polysilicon CMOS Process," *IEEE Electron Device Letters*, vol. 12, no. 3, pp. 111–113, March 1991.
- [83] D. R. Brown, S. Collins and G. F. Marshall, "Carrier Trapping in inter-polysilicon charge injectors," *Electronics Letters*, vol. 31, no. 1, pp. 72–73, January 1995.
- [84] J. R. Mann, "Floating Gate Circuits in MOSIS," Tech. Rep., MIT Lincoln Laboratory, November 1990.
- [85] Eric M. Vogel, Monica D. Edelstein and John S. Suehle, "Defect generation and breakdown of ultrathin silicon dioxide induced by substrate hot-hole injection," *Journal of Applied Physics*, vol. 90, no. 5, pp. 2338–2346, September 2001.
- [86] S. Mahapatra, Chetan D. Parikh, V. Ramgopal Rao, Chand R. Viswanathan and Juzer Vasi, "A Comprehensive Study of Hot-Carrier Induced Interface and Oxide Trap Distributions in MOSFET's Using a NOvel Charge Pumping Technique," *IEEE Transactions on Electron Devices*, vol. 47, no. 1, pp. 171–177, January 2000.
- [87] Chris Diorio, Bradley A. Minch and Paul Hasler, "Floating-Gate MOS Learning Systems," in *Proceedings of the International Symposium on the Future of Intellectual Integrated Electronics (ISFIIIE)*, 1999, pp. 515–524.
- [88] W. P. Millard, Z. K. Kalyjian and A. G. Andreou, "Calibration and matching of floating gate devices," in *The Proceedings of the International Symposium on Circuits and Systems*. IEEE, 2000, vol. 4, pp. 389–392.
- [89] Luca Selmi, Andrea Ghetti, Roberto Bez and Enrico Sangiorgi, "Trade-offs between Tunneling and Hot-Carrier Injection in Short Channel Floating Gate MOSFETs," *Micro-electronic Engineering*, vol. 36, pp. 293–296, 1997.
- [90] Andrea Ghetti, Luca Selmi and Roberto Bez, "Low-Voltage Hot Electrons and Soft-Programming Lifetime Prediction in Nonvolatile Memory Cells," *IEEE Transactions on Electron Devices*, vol. 46, no. 4, pp. 696–702, April 1999.

- [91] M. J. Kirton, M. J. Uren, S. Collins, M. Schulz, A. Karmann and K. Scheffer, "Individual defects at the $Si : SiO_2$ interface," *Semiconductor Science and Technology*, vol. 4, no. 12, pp. 1116–1126, December 1989.
- [92] R. van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer Academic, 1994.
- [93] Henrik T. Jensen and Ian Galton, "A Low-Complexity Dynamic Element Matching DAC for Direct Digital Synthesis," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 45, no. 1, pp. 12–27, January 1998.
- [94] Alex R. Bugeja, Bang-Sup Song, Patrick L. Rakers and Steven F. Gillig, "A 14-b, 100-MS/s CMOS DAC Designed for Spectral Performance," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1719–1731, December 1999.
- [95] Wim Van Petegem, Ben Geeraerts, Willy Sansen and Benny Graindourze, "Electrothermal Simulation and Design of Integrated Circuits," *IEEE J. Solid-State Circuits*, vol. 29, no. 2, pp. 143–146, February 1994.
- [96] K. Lampaert, G. Gielen and W. Sansen, "Thermally Constrained Placement of Smart-Power IC's and Multi-Chip Modules," in *Thirteenth IEEE SEMI-THERM Symposium*, 1997, pp. 106–111.
- [97] Yannis Tsividis, *Operation and Modeling of The MOS Transistor*, McGraw-Hill, 1999.
- [98] I. M. Filanovsky and Ahmed Allam, "Mutual Compensation of Mobility and Threshold Voltage Temperature Effects with Applications in CMOS Circuits," *IEEE Transactions of Circuits and Systems-I: Fundamental Theory and Applications*, vol. 48, no. 7, pp. 876–884, July 2001.
- [99] I. M. Filanovsky, A. Allam and Su Tarn Lim, "Temperature Dependence of Output Voltage Generated by Interaction of Threshold Voltage and Mobility of an NMOS Transistor," *Analog Integrated Circuits and Signal Processing*, vol. 27, pp. 229–238, 2001.
- [100] Daniel Foty, *MOSFET Modelling with SPICE*, Prentice-Hall, 1997.
- [101] A. McEwan and S. Collins, "Analogue Interpolation Based Direct Digital Frequency Synthesiser," Submitted to the 2003 IEEE International Symposium on Circuits and Systems.

