Development of 230 GHz Finline SIS Mixers for Next-Generation Large Array Receivers and HARP Instrument Upgrade

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ABSTRACT

In pursuit of advancing large array receiver capabilities and enhancing the 16-element Heterodyne Array Receiver Program (HARP) instrument on the James Clerk Maxwell Telescope (JCMT), we have successfully fabricated 230 GHz finline superconductor-insulator-superconductor (SIS) mixers. These mixers are critical for assessing the potential and prospective for the HARP instrument's upgrade. Unlike HARP's mixer, we replace the probe antenna with an end-fire unilateral finline as the waveguide to planar circuit transition. The current mixer design operates in the range of 230 GHz , and the mixer chips' I-V curves have been characterized, showing promising results with a quality factor (Rsg/Rn) exceeding 9.3. Evaluation of the double-sideband (DSB) receiver noise temperature (Trx) is currently underway. Once successfully characterised, our immediate aim is to scale the mixer to operate at HARP's frequency range near 345 GHz. Ongoing simulations are currently being conducted for the design of the 345 GHz SIS mixer. This work marks a crucial step toward enhancing HARP receiver performance

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with better sensitivity and Intermediate Frequency (IF) bandwidth, enabling higher-frequency observations, and expanding the scientific potential of the JCMT and its collaborative partners.

Keywords: SIS mixers, large format array, heterodyne receivers, sub-millimetre astronomy, superconducting mixers

1. INTRODUCTION

The investigation of millimeter-wavelength spectral lines is crucial for advancing our understanding of the complex physical and chemical properties of the interstellar medium. However, conducting wide-field spectroscopic surveys of the Milky Way and nearby galaxies presents a significant challenge due to the time-intensive nature of these studies, even when using large single-dish telescopes. This difficulty is further compounded when using interferometers, which have inherently limited fields of view. Multibeam receivers can potentially increase a telescope's mapping speed by a factor proportional to the number of pixels in the array. Nevertheless, the mapping speed is also inversely proportional to the system noise temperature.[?]

$$Mapping\,Speed \propto \frac{N}{{T_{sys}}^2}$$

where N is the number of pixels in the array, and $T_{\rm sys}$ is the system noise temperature.

Thus, any increase in system noise temperature can rapidly negate the speed improvements provided by the array. Consequently, an array receiver system must incorporate additional pixels without compromising the state-of-the-art noise performance characteristic of modern single-beam systems. Key challenges include efficiently coupling each pixel to the main dish, managing the increased mechanical and electrical complexity, dividing and injecting the local-oscillator (LO) signal without interfering with the astronomical signal path, and processing the additional intermediate frequency (IF) signals. To expedite the mapping process, it is therefore logical to increase the number of pixels within the receiver. This expansion must occur without compromising the near quantum-limited performance of the superconductor–insulator–superconductor (SIS) mixers. A critical consideration for the next generation of large-format focal plane arrays is the probable reimaging of telescope optics. This reimaging is necessary to accommodate smaller feed horns and closer pixel spacing. Noteworthy constraints in this context include the size limitations of the SIS devices, the magnetic coils, and the immediate proximity of IF components to the SIS devices. Addressing these challenges is imperative to maximize pixel density and advance observational capabilities in millimeter-wavelength astronomy.[?,?]

The Heterodyne Array Receiver Program (HARP) is a 16-element heterodyne array receiver arranged in a 4×4 pixel configuration with a $2' \times 2'$ field of view. It has been installed at the James Clerk Maxwell Telescope (JCMT) on the summit of Maunakea, Hawai'i since 2007.[?,?] Over the years, observations made by this instrument have significantly contributed to astronomy. For instance, the Spectral Legacy Survey (SLS), one of its notable projects, produced a spectral imaging survey of all molecules detected in the 345 GHz atmospheric window (between 332 GHz and 373 GHz) toward a sample of five sources.[?] Utilizing HARP's rapid, wide-field mapping capability and its high angular resolution (14"), a high-resolution CO (3-2) survey of the galactic plane has been released.[?] Another major program that has employed HARP is the JCMT Nearby Galaxies Survey.[?]

The original design and development of HARP mixers were conducted by the Cavendish Astrophysics group at the University of Cambridge, while the mixer chips were fabricated by the Kavli Institute of Nanoscience at Delft.[?] A key technique involved using a radial probe to couple the signal from a full-height waveguide to a thin film microstrip.[?] Despite successful operation over many years, upgrading HARP presents a complication: the LO power required for operating the SIS mixers cannot be controlled individually due to the LO coupling design.[?] Only the overall incident power can be controlled by monitoring the average mixer current. Therefore, new mixer chips must operate effectively with the same LO power level as the previous mixers for any upgrades. To replace malfunctioning mixer chips in HARP and ensure a supply of replacement devices, a new design was developed incorporating a rectangular probe, previously used for planar dual-polarization applications in the same frequency range.[?] Since 2019, three new chips have been installed on HARP.[?] These new mixer chips were fabricated at the Superconducting Device Laboratory, Institute of Astronomy and Astrophysics, Academia

Sinica (ASIAA), Taiwan, which has produced many batches of SIS mixer chips for the Submillimeter Array (SMA) interferometer.[?,?]

To accelerate the upgrade program, we are considering a more immediate solution: developing a replacement array utilizing existing technology while incorporating several innovative features to significantly enhance performance. With adequate support, we can feasibly improve the array's sensitivity, expand the Radio Frequency (RF) and Intermediate Frequency (IF) bandwidth, and potentially simplify the optical system. In scenarios where resources are constrained, the array receiver can be designed to align with the existing optical architecture. This strategy would provide a minimal yet effective upgrade, enhancing JCMT operations while the broader development and deployment proceed.[?]

2. IMPLEMENTATION

2.1 Design

The initial step in designing new finline mixer chips for HARP involves conducting finite element electromagnetic simulations of the finline structure at RF using the High Frequency Structure Simulator (HFSS).[?] Fig. 1 illustrates the simulation model of the finline structure, including the tuning, coupling, and RF choke circuits. The design of the junction and matching circuit underwent simulation employing quantum mixer theory,[?] along with an analytical model for thin-film superconducting microstrip lines.[?] Additionally, numerical simulation methods were utilized to assess the SIS performance with multiple tones.[?,?,?]

Our first mask design has not implement variations in the design to to accommodate process variations and simulation errors. The next version will consider the advantage which has been demonstrated.[?]

Referring to Fig. 1 , the incoming signal travels through the finline antenna to the waveguide and is coupled to the microstrip. Beyond the feed point, the signal reaches the SIS junction through microstrip. The SIS matching circuit is a short inductive microstrip section followed by several rectangular stubs as RF chokes. The intermediate frequency (IF) signal produced by the SIS junction travels to the microstrip RF choke and then impedance matching microstrip to a SMA type connector, which has a characteristic impedance of 50 Ω.

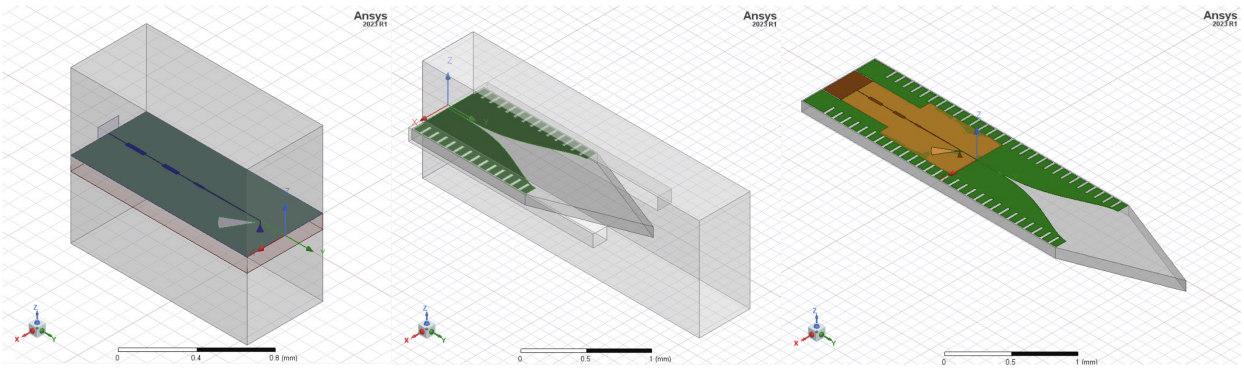

Figure 1. The HFSS electromagnetic model represents the finline mixer chip. From left to right, the model consists of the coupling and matching microstrip, the finline antenna structure, and the overlapping integration. The structure comprises a single crystal quartz substrate, finline structure, microstrips, crossovers, ground plate, and IF stub. The waveports were positioned at the ends of the waveguide.

2.2 Mixer Chip Fabrication

The SIS mixer chips were fabricated on 2-inch crystal quartz substrates of 300 μm in thickness. To implement the SIS junction, matching circuit, RF chokes, and ground plate, a five-layer mask set was conducted, as shown in Fig. 2. The first layer was SIS tri-layer which included the deposition, oxidation, and lift-off to produce Nb/Al/AlOx/Nb sandwich. The thicknesses involved are: bottom Niobium (Nb) 200 nm, aluminum 7 nm, and top Nb 100 nm. Then the SIS junctions were defined by patterned photoresist, top Nb etching, and the SiO_2

layer deposition as the DC electrical isolating layer and the part of 250nm of the total dielectric layer of 430nm for microstrip. The third layer is the other part of 190nm of the dielectric layer. The four layer is a thick Nb layer of 600nm for the wiring of the microstrip and RF choke structure. The fifth layer is the Au layer for the contact pads. The fabricated devices needed to be further diced and lapped to the specific dimension. We performed the dicing process first using a precision dicing machine. The depth of the diced grooves was about 150 μm . Then the wafer was mounted on a 5" quartz plate by wax for the lapping process. The targeted thickness is 100 μm. The thickness of chip was checked by a micrometer on a flat marble plate with an accuracy within 2 μm. Fig. 3 explains the detail process flow of the dicing and lapping for getting the chip with the targeted dimensions. The advantage of such process sequence is that the diced grooves can be filled with wax that improved the adhesion of individual chips on the quartz plate significantly and the chip survival yield is much enhanced.[?]

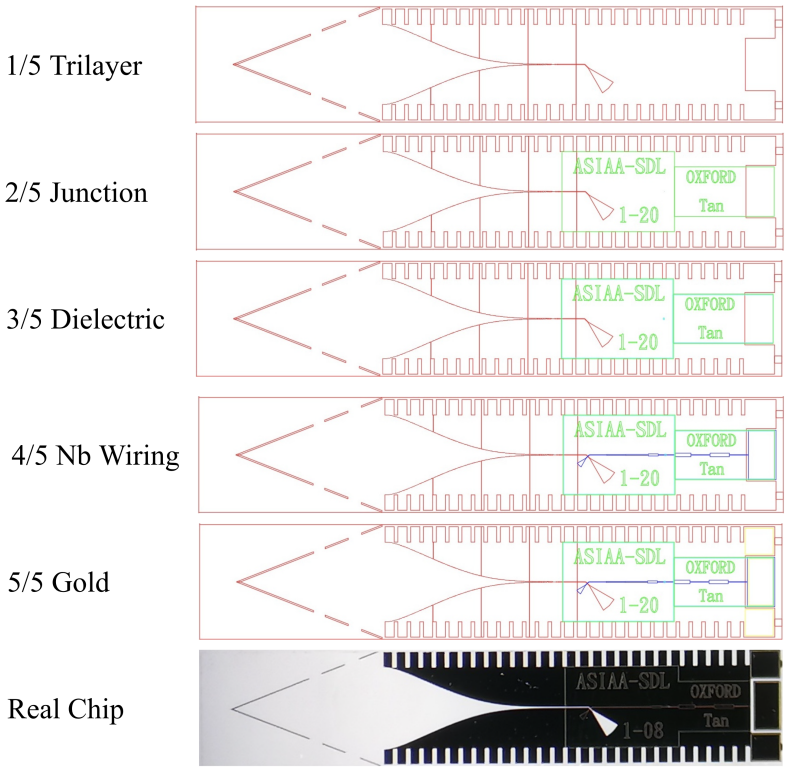

Figure 2. The layout of five layers mask set for the mixer patterns. They are trilayer, junction definition, dielectric, wiring, and the gold contact.

Table 1. The specifications of mixer fabrication

Mask	Type	Resist	Materials	Thickness(nm)	Note
Trilayer	Lift-off	AZ5214E	Nb/AlOx-Al/Nb	100/7/200	Jc = 9.0 kA/cm^2
Junction/SiO2	Etching	FH6400L	Nb	100	Dj = 1.4 μm Anodization (7V)
	Lift-off		SiO2	250	
Dielectric	Lift-off	AZ5214E	SiO2	190	Thick PR of 1.5 μm
Wiring Nb	Etching	FH6400L	Nb	600	RF clean before Deposition
Gold Contact	Lift-off	AZ5214E	Au/Ti	200/20	RF clean before Deposition

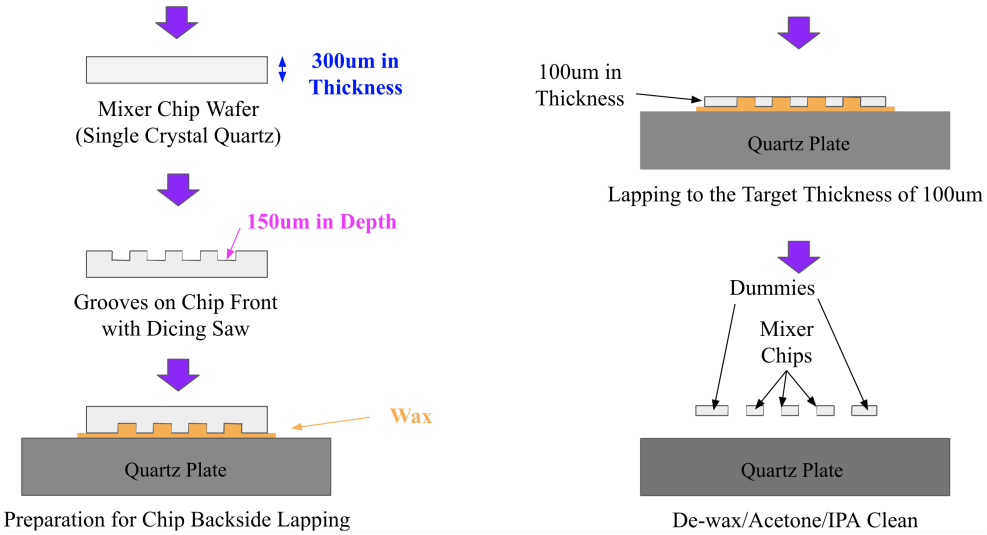

Figure 3. The schematic process flow of the dicing and lapping of the mixer chips. The original thickness of the wafer was 300 μm and the final thickness of chip is 100 μm.[?]

2.3 Mixer Block Assembly and Experimental Setup

The mixer block was composed of two split blocks made of oxygen-free copper (OFC) with gold plating. The design of the mixer blocks originated from the University of Oxford[?] and they were fabricated at the National Astronomical Research Institute of Thailand (NARIT). The IF transmission line was designed as a microstrip with a characteristic impedance of $\sim 50\ \Omega$. At the end, the microstrip-to-coaxial transition utilized a glass bead and sliding contact to a K connector. The mixer chip was carefully inserted into the slot, and its position was meticulously adjusted to optimize coupling, as shown in Fig. 4. Subsequently, aluminum wires with a diameter of 5 mil were bonded to bridge the IF stub and ground pads on the SIS mixer chip and the IF transmission line. Fig. 5 illustrates the current test setup at NARIT. On the left is the interior of the cryostat, where one mixer, serving as the Device Under Test (DUT), has been assembled and connected to the IF chain. This chain includes a bias-T, isolator, cryogenic Low Noise Amplifier (LNA), and then outputs to the room temperature measurement path. Surrounding this area, other mixer block assemblies are prepared to characterize the junction performance through I-V scans. The final goal will be build the test setup with an interal cold load of 4K and rotating mirror to switch the beam between the cold load and ambient load.[?]

3. RESULT AND DISCUSSION

Currently, some mixer block asseblies are under testing and the test setup is still under the development. To characterize the junction quality of the fabrication process, some test chips have been completed the I-V scan to estinate the junction performance. Fig. 6 is the result of I-V scan on a square junction with a dimention of 1.5 μm at operation temperature (4 K). The magnetic field was ulitized with a permanant magent. The gap voltage of the junction is 2.88mV while the normal resistance (Rn) is $\sim 6.5\ \Omega$. The quality factor (Rsg/Rn) exceeding 9.3, where Rsg is the junction resistance at 2mV. This result also another demonstrate of the junction capability for the HARP mixers have been developed and replaced in 2019.[?] Compare with the fabrication processes between the mixer design, the finline ulized thicker thickness of the dielectric in this manuscript and the HARP was the inverted microstrip. The two techniques of the device designs have been demonstrated by the fabrication capability.

4. CONCLUSION

We have designed and fabricated finline SIS mixers for the potential upgrating HARP instrument on JCMT. In laboratory tests the junctions of the mixers show good quality factor to lead the desing as high performance

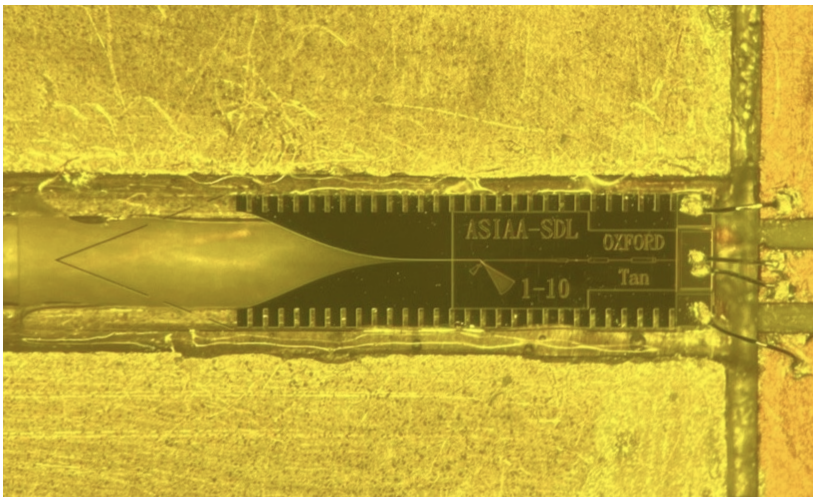

Figure 4. illustrates the optical microscope (OM) view of both the mixer chip and the IF transmission line within the mixer block. On the left, the mixer chip is seamlessly inserted into the designated slot within the mixer block.

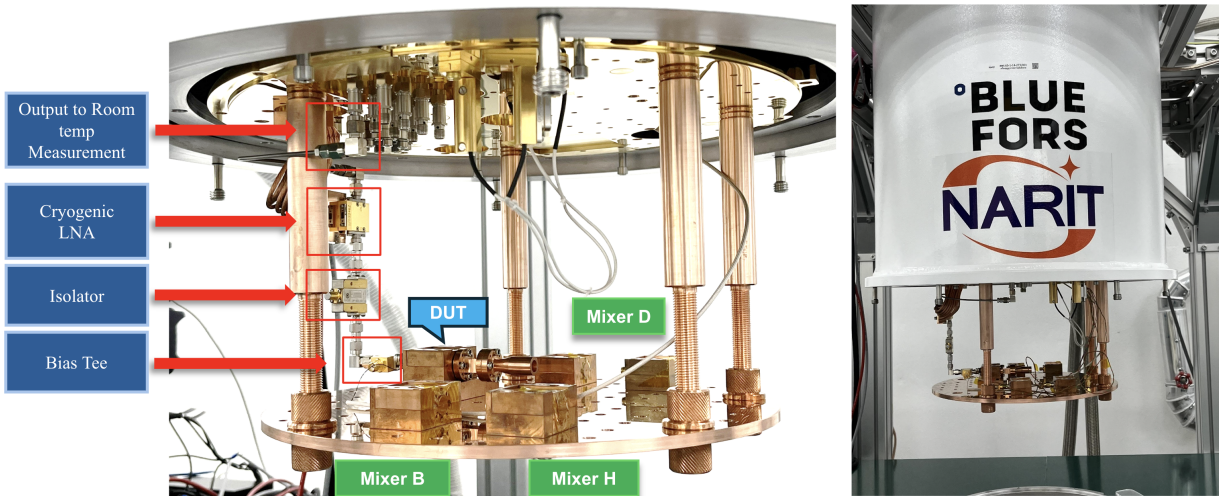

Figure 5. illustrates the current test setup at NARIT. On the left is the interior of the cryostat, where one mixer, serving as the Device Under Test (DUT), has been assembled and connected to the IF chain. On the right is the cryostat assembly, which is capable of cooling the devices to 4K using a pulse tube cooler.

SIS mixer. The development of the test setup in cryogenic fridge will able to further estimate the receiver performance. The progress lead the collatoration to continue outlining the concept for the realistic development of HARP upgrade in the near future.

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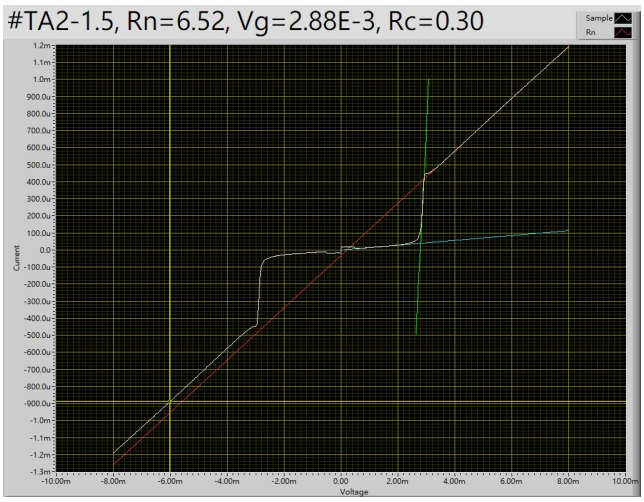

Figure 6. illustrates the current vesus voltage curve of the junction on the test chip.

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