

Quad-Module characterization with the MALTA monolithic pixel chip

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1. Introduction

The MALTA silicon pixel detector family combines a depleted monolithic active pixel sensor (DMAPS) with a fully asynchronous front-end and readout. The design features a high granularity pixel matrix with a 36.4 µm symmetric pixel pitch, low power consumption of <1 µW/pixel and low material budget with detector thicknesses as little as 50 µm. The detector achieves a radiation hardness to 100 MRad TID and more than 1×10^{15} 1 MeV n_{eq}/cm^2 with a time resolution of < 2 ns [1, 2, 3].

In order to cover large sensitive areas efficiently with a minimum of power and data connections the development of modules, comprising of up to 4 MALTA detectors, is studied. The chip features CMOS transceiver blocks together with most powering pads on its east and west sides. This allows for chip-to-chip data and power transfer in a module where 4 chips are arranged side-by-side [4, 5]. By choosing different wire bonding schemes a parallel or serial powered module can be assembled (see figure 1).

The serial powering scheme used for MALTA quad modules means that the power needed to operate 4 chips must be passed into chip 0 and transferred chip-to-chip from there. The on-chip power lines of MALTA are not optimized for this load and it is therefore assumed that losses in performance due to under-powering will be observed for chips further down the line (chips 2 and 3).

2. Module characterization in beam tests

Both, a serial and a parallel powered module, have been assembled and characterized at the SPS North Area with a 120 GeV/c pion beam using the MALTA telescope which is installed in the H6a beam line [6]. The parallel powered module was tested with an average detection threshold of 330 to 430 electrons (chip-to-chip thresholds on the module varied) while the serial powered module achieved thresholds of 450 to 610 electrons with a clear trend towards higher thresholds from chip 0 to chip 3. All thresholds were determined with the size of the capacitance in the injection circuit assumed to be 230 aF based on parasitic extraction from simulations.

The parallel powered module achieves a detection efficiency of > 98% on all chips with <1 % of pixels effectively masked. This indicates that the individual chips of the module do not interfere with each other in any significant way. Further, 97.1% of data are read out within a 25 ns window after signal travel time calibration. The results for the serial powered module are still preliminary and pending further investigation. However, the results so far show losses in efficiency with chip 3 only achieving ∼92% detection efficiency. Furthermore, only 71.9% of data is read out within 25 ns after signal travel time calibration. All calculated efficiencies include masked pixels (<1 % of each chip matrix). The efficiency maps for the fully enabled serial and parallel powered modules can be seen in Figures 2 and 3. Some low efficiency patterns are visible which are attributed to masked pixels on the matrix.

Two factors contribute to the loss in performance of the serial powered module. First, chip 1 of this module has two broken low voltage differential (LVDS) channels in the 40-channel parallel readout of the chip which where stuck "high" (MALTA is read out in 40 bit words that are transmitted in parallel). This is a known issue on the chip side and considered a yield issue. These channels correspond to pixel hit flags in the MALTA word and as a result, up to two additional pixel hits are read out from this chip with every MALTA word. Due to the high readout frequency,

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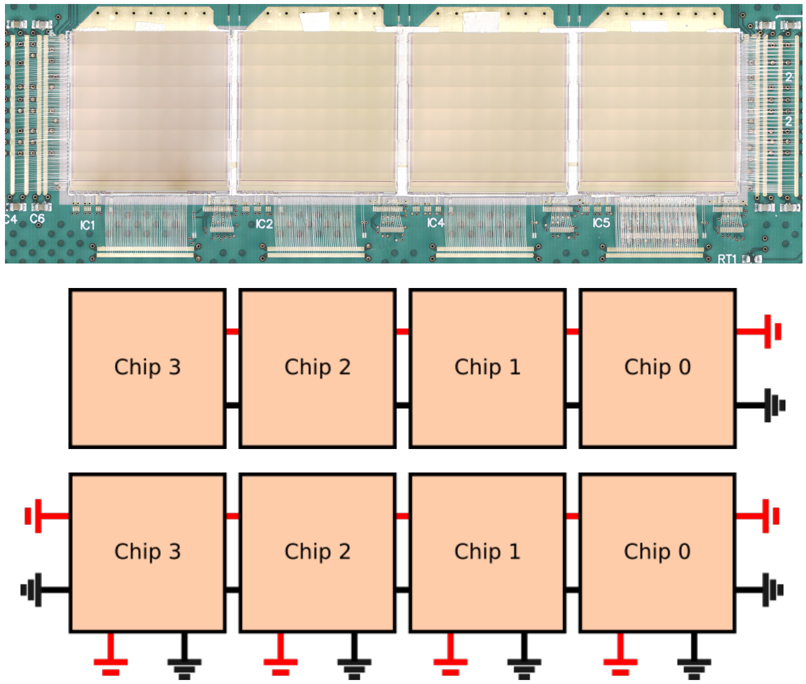
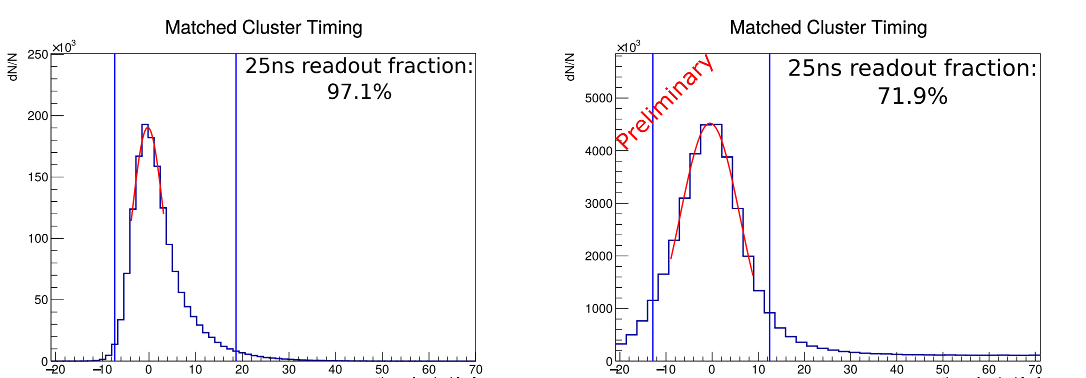


Figure 1: A quad-module with MALTA chips (top) can be wire bonded with a serial powering scheme (middle) or a parallel powering scheme (bottom).

this erroneous data had a higher chance of intercepting valid data at the module output and caused increased chip mis-identification. Since this issue is caused by a damaged chip it is not considered a performance loss due to serial powering.
However, even when ignoring chip mis-identification, the serial powered module still shows lower efficiency for chip 2 at ∼97 % and chip 3 at ∼96 %. This is attributed to the under-powered pixel front-end which is the result of dropping voltage levels along the module. A possible solution here is to enlarge the power transmission lines in the MALTA metal layers in future designs or to further reduce the power draw of the front-end through improvements to the analogue front-end. A fully powered front-end is also expected to recover the losses of in-time efficiency.

3. Conclusion

The MALTA monolithic pixel detector can be used for the assembly of modules with up to four chips. Using a wire bond scheme for parallel powering, a MALTA quad-module can achieve 98% overall detection efficiency with 97.1% of data read out within 25ns after signal timing calibration. For a fully enabled quad-module assembled



(a) In-time readout performance for a 25 ns time window with the parallel powered module.

(b) In-time readout performance for a 25 ns time window with the serial powered module.

Figure 2: In-time readout performance of the 4-chip module in with both powering schemes.

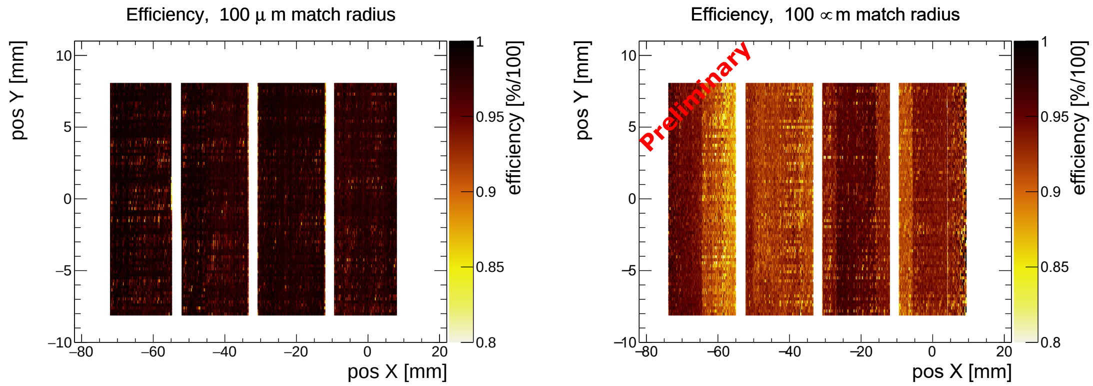


Figure 3: Efficiency maps for the parallel powered and fully enabled module (left) and the serial powered and fully enabled module (right).

with a serial powering wire bond scheme the detection efficiency drops to 92% on chip 3 of the module due to chip mis-identification caused by the faulty readout of a chip of that module and under-powering. Furthermore, only 71.9% of data is read out within 25 ns. Losses in efficiency are mainly attributed to a broken chip in the serial powered module while the reduced timing performance is attributed to an under-powered front-end.
These results verify the functioning of chip-to-chip data transmission on MALTA detectors. They are furthermore promising for serial powered modules with MALTA detectors of the next generations, MALTA2 and MALTA3, where further improvements were implemented for the detector's sensor design, slow control and power distribution.

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