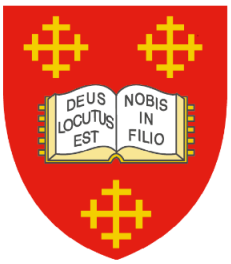


Development and testing of ATLAS ITk strip barrel stave components

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I dedicate this to my family, especially to the loving memory of my grandmother.

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Abstract

The LHC is planned to be upgraded to HL-LHC with a nominal luminosity of $5 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$ and an operational lifetime of over 10 years. The ATLAS (A Toroidal LHC ApparatuS) experiment, as a general purpose particle physics experiment at the LHC, is planning a major upgrade in its tracker part to ensure performance in higher radiation and data rate. The new all-silicon inner tracker (ITk) is planned to be replacing the current SCT during the long shut down in 2026.

This thesis is focused on the strip barrel part of the ITk. It discusses the performance testing of different components on a strip barrel stave and the overall performance studies of a single stave. Pre-irradiation effect and operational parameters of ABCStar chip set are tested. The performance of a prototype ABCStar module in test beam is studied. This thesis discusses the software and procedure developments of the tape tester robot, which is developed for measuring strip barrel bus tapes. The statistical analysis of pre-production tape test results is obtained. The reliability studies of VTRx+ optical transceivers are also presented. This thesis also includes various studies on the performance of a single barrel stave.

***Keywords*—** HL-LHC - ATLAS ITk - hardware upgrade

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Author's Contributions

I started working on ATLAS ITk in October 2018 and had participated in various projects to prepare for the final system tests planned in 2023.

I was responsible for validating the pre-irradiation solution with ABCStar chips and the related data analysis, the results of which are presented in Sec. 2.1.1. Sec. 2.1.1 also included my studies on the frequency and input voltage operation window for ABCStar chips. I was responsible for the data analysis for results shown and performed the shmoo tests as well as data analysis on another older chip set.

My work on module test beam studies is shown in Chapter 3. I performed data analysis on pedestal and beam data from Sept. 2019 test beam data and investigated the calibration issues. I was also responsible for the uncertainty studies and the S/N ratio calculations. I performed data analysis on Sept. 2019 pulse shape data and participated in theoretical pulse shape simulation. I also did uncertainty studies on the pulse shape data.

Chapter 4 covers my work on the tape tester robot. I have been responsible for software development and procedure updates since Oct. 2018. I participated in all performance validation campaigns since then until 2022 and was responsible for related data analysis. I was also responsible for setting up statistical data analysis software and developing test procedures.

I also participated in VTRx+ reliability studies, which results shown in Chapter 5. I was responsible for software development used in the tests and performed some performance validation tests, including LI (luminosity-current) scans. I also performed data analysis for data obtained.

I participated in several performance tests on staves at RAL and CERN. Related results are discussed in Chapter 6. I performed data analysis on cold noise studies and magnetic triggering studies. I was also responsible for data analysis on module performance comparison on-stave and standalone. I developed the software used for on-stave LI scans and analysed obtained data.

1 | Introduction

The Large Hadron Collider (LHC) installed at CERN is a large general-purposed high-energy hadron collider. [1] The LHC is composed of a 27 km long accelerating ring with multiple smaller rings. The protons are extracted from hydrogen sources and go through the pre-accelerating phase in several different accelerators, as shown in Fig. 1.1. Starting from the Linear Accelerator (LINAC) to the booster, onto the Proton Synchrotron (PS) then onto the Super Proton Synchrotron (SPS), the hadrons are injected in the LHC. The hadrons will only collide at certain collision points, where detectors are built to study the collision products. On the LHC ring there are four major detectors: A Large Ion Collider Experiment (ALICE), the Compact Muon Solenoid (CMS), Large Hadron Collider beauty (LHCb) and A Toroidal LHC Apparatus (ATLAS). The ALICE detector is focused on the study of heavy-ion processes generated by lead-lead collision, while LHCb mainly studies b-physics. The ATLAS and the CMS are two more general-purpose detectors, measuring the properties of the Standard Model and the Higgs boson, as well as searching for physics beyond the Standard Model. The LHC was first started up in 2008, and has been the largest high energy hadron collider since. As a general-purpose accelerator, research at the LHC ranges from precision measurements on standard model (SM) particles to search for new physics like dark matter beyond SM (BSM) as discussed for the four major detectors. The current luminosity is about $10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$ since 2017. Higher luminosity promises event rate for rare collisions and can open opportunities for more detailed Higgs studies and more BSM studies. It has been scheduled that the LHC is to be upgraded in luminosity during the long shut-down scheduled in 2026.

The LHC is going to be upgraded to the High-Luminosity LHC (HL-LHC) [3], with a nominal luminosity of $5 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$ and the peak luminosity of $7.5 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$. As one of the main detectors at the LHC, the ATLAS detector needs to go through a corresponding upgrade in order to adjust to the high luminosity future. The biggest update is planned for the tracking detector of the ATLAS experiment, which will be replaced with the new all-silicon inner tracker (ITk). A more granular detector to accommodate for the higher luminosity and increased radiation tolerance. Along with the high luminosity, the

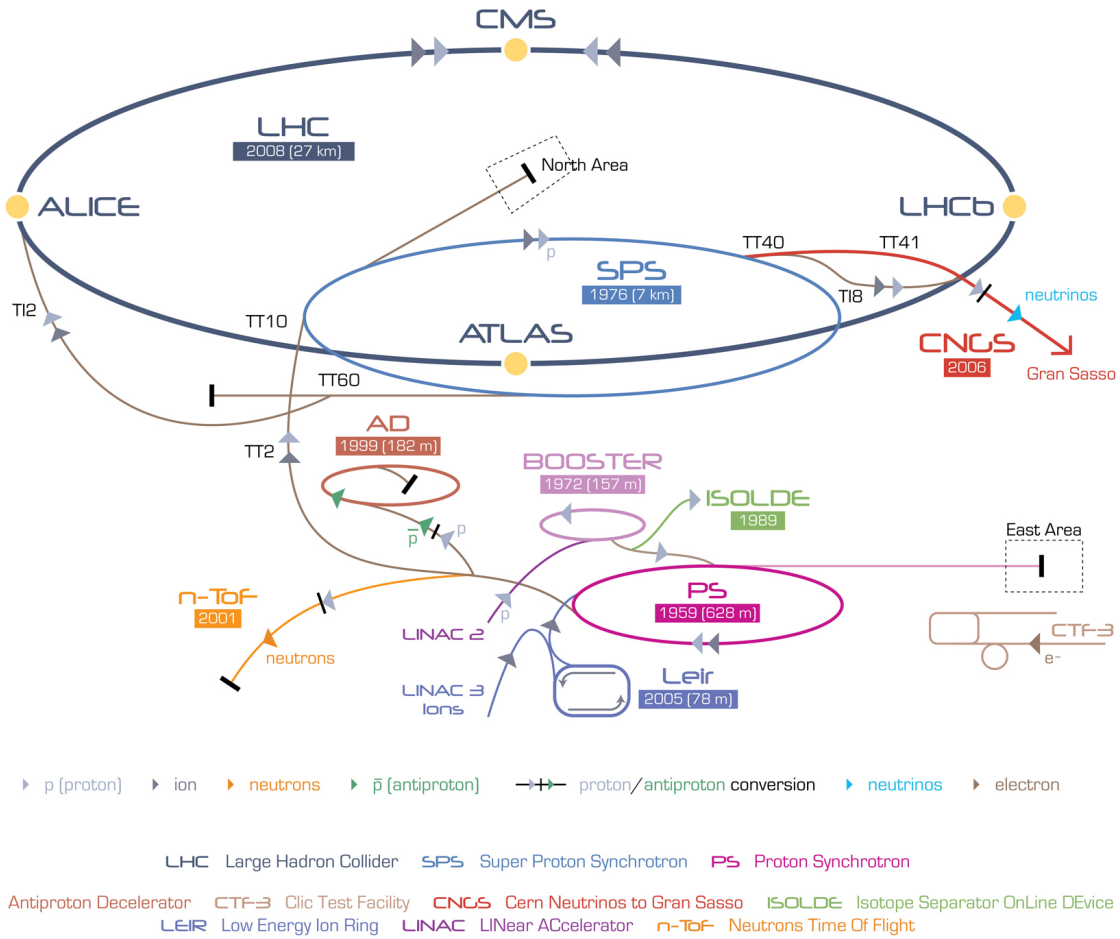


Figure 1.1: The LHC accelerator complex. Figure adapted from [2].

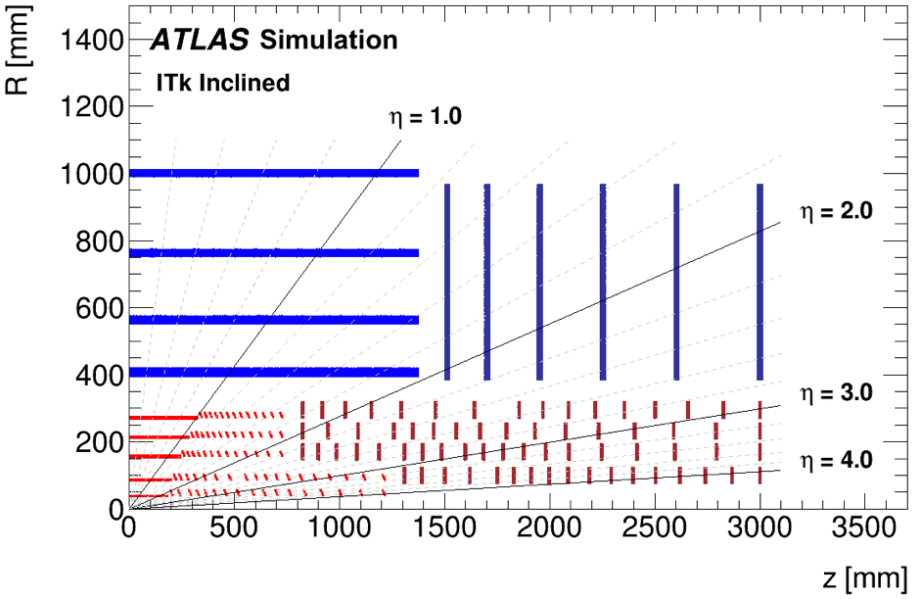


Figure 1.2: Schematic layout of one quadrant of the ATLAS ITk detector. The red color corresponds to the ITk pixel part, while the blue components represent the ITk strip detector. The horizontal axis goes along the beam line and the origin of axes lies in the interaction point. The vertical axis corresponds to the radius measured from the beam axis. [4]

technical requirements on the ITk include significantly increased radiation hardness of all its components, reduction of the amount of detector material leading to the lower energy losses in dead detector material, as well as improvement of data selection system, which will have to cope with one order of magnitude higher data rates [4].

Five concentric pixel barrel layers will be surrounded by four strip barrel layers. Both pixel and strip systems will also include their end-cap parts, represented by the pixel rings of different radii and six strip disks on each side of the pixel and strip barrel, respectively. A cross section of one quadrant of the ITk detector is shown in Fig. 1.2, while its computer simulated model is illustrated in Fig. 1.3. The focus of this thesis is on the upgrade of the silicon strip tracker part of the ITk.

As this thesis focuses on the development and testing of components and systems required for the new silicon strip tracker in ATLAS, there is a general discussion of signal and noise in silicon detector systems (as in Sec. 1.1 and Sec. 1.2). The ATLAS ITk design is briefly reviewed in Chapter 2. Chapter 3 discusses barrel module test beam data analysis

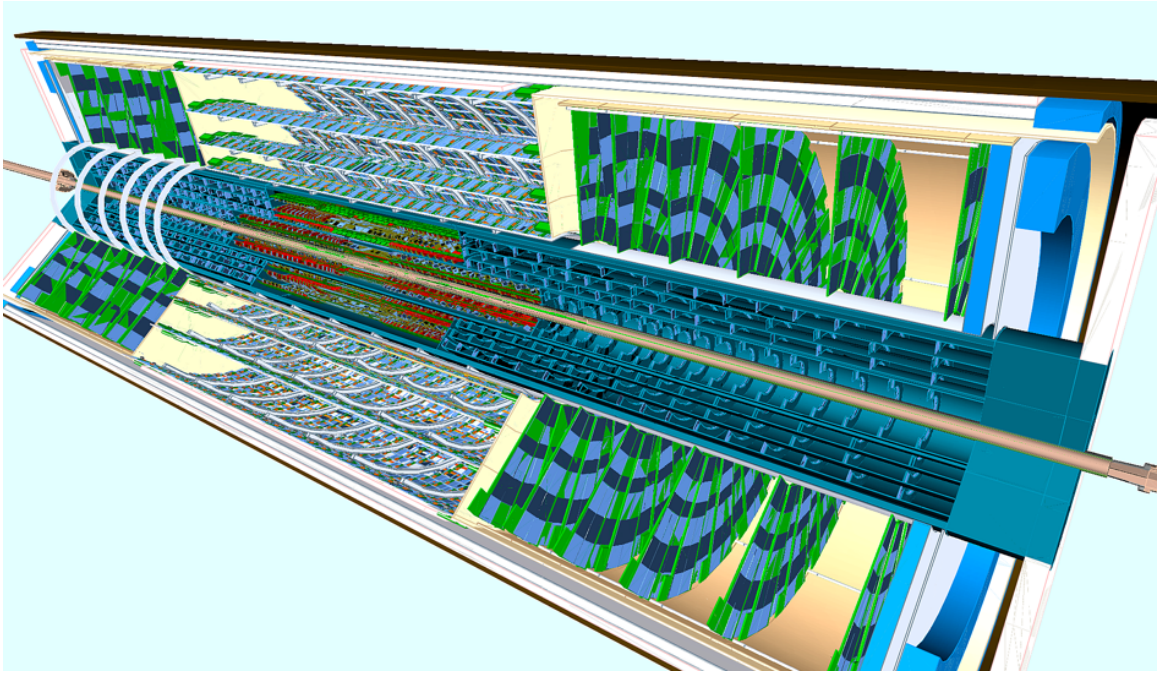


Figure 1.3: Simulated layout of the ATLAS ITk detector, with the inner pixel part surrounded by the strip detector [4]

results. Chapter 4 discusses the tape tester robot and the test results for pre-production tapes tested. Reliability studies on optical links used on ITk are discussed in Chapter 5. Chapter 6 discusses tests performed on ITk barrel staves and Chapter 7 gives a short conclusion of this work.

1.1 Signal Generation in Silicon Detectors

The fundamental idea behind silicon strip detector sensors is the ionisation chamber, as illustrated in Fig. 1.4. In the case of silicon sensors used for the strip tracker detector, particles and radiation go through the sensor region and generate mobile charges (electron and hole pairs) along the track. The charges move in the electric field and induce a current on the electrode. When the electric field is large and the sensor thickness is thin, the charges move fast so that the pulse is short. This pulse is then passed to the amplifier and shaper circuits. The pre-amplifier and the shaper part mostly focus on optimising the system for best signal-to-noise ratio (SNR).

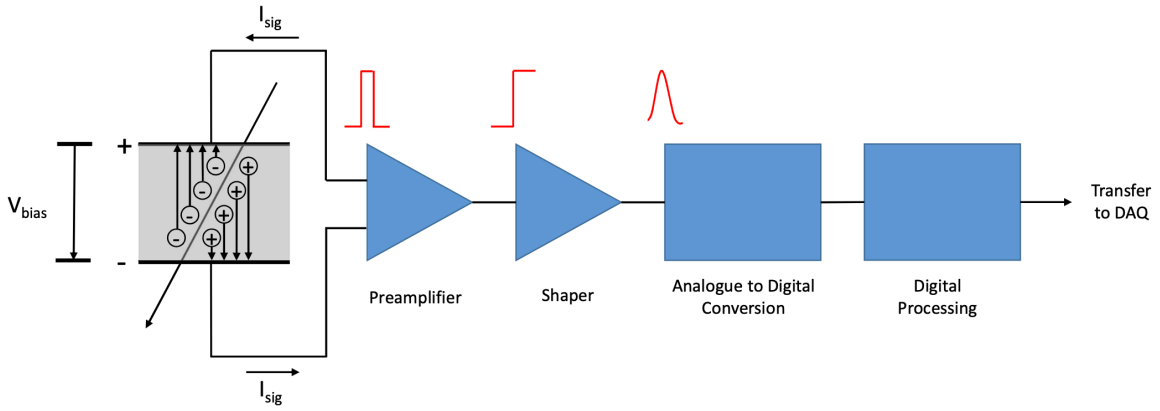


Figure 1.4: A generic semiconductor detector based on ionisation chambers. Radiation passes through the chamber, generating charge pairs (electrons and holes in the case of silicon) along the trajectory. The charges move towards the electrodes under the bias voltage applied across the sensor region and are collected by the collection electrodes. The charges induce a pulse in the circuit, which is passed to the pre-amplifier and the shaper to be amplified and shaped before being digitised. Then the outgoing signal could be sent to a buffer or further processed before being sent to data acquisition (DAQ). [5]

An additional constraint is to minimise detected hits in the wrong bunch crossing, which is usually described with pile-up. [5] There are two types of pile-ups, in-time and out-of-time pile-up. In-time pile-up means two events happen at the same time and are thus inseparable. Out-of-time pile-up happens when the electronics processing time is long. One event last several bunch crossing (BC) and later events are merged into it. A bunch crossing is the time interval between collisions of proton bunches in the LHC, which is approximately 25 ns. Even though this can be resolved with faster electronics, more noise comes with faster electronics, as will be discussed in Sec. 1.2. As a result, compromises are made and this is discussed in Sec. 1.2. The resultant pulse goes through digitisation and then is sent to be further processed or into a buffer awaiting a readout request. Then the data goes into data acquisition (DAQ) system.

A more detailed look into the sensor part of the detector is illustrated in Fig. 1.5. The sensor part is regarded as a p-n junction in silicon, as detailed in Sec. 2.2. A generic n-in-p silicon sensor is illustrated in Fig. 1.5. Due to thermal diffusion, electrons and holes move away from their original positions and into the other region at the junction. Their thermal diffusion forms a space charge region and the electric field it builds up limits the mobile charges from

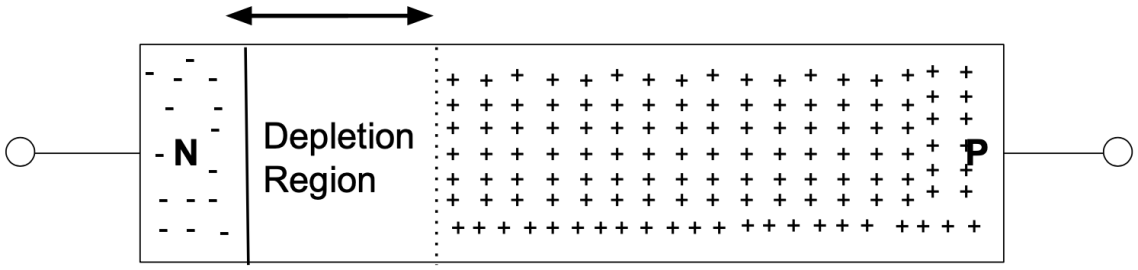


Figure 1.5: The sensor is a p-n junction in silicon. When an external potential is applied with positive polarity on the n-side and negative polarity on the p-side, the mobile charges are drawn away from the junction. This leaves a net space charge from atomic cores and builds up an electric field in the junction.

further movement. So all p-n junctions start with a depletion region where there are no mobile charges present and a "built-in" potential difference between p and n sides, V_{bi}. [6] Then the bias voltage is applied. When the negative polarity is applied to the p-side and positive polarity is applied to the n-side, it is called "reverse bias". The bias voltage works to increase V_{bi}. The depletion region is made larger in this way. The depletion region acts as an ionisation chamber mentioned above. In the silicon strip detector in ATLAS, the sensors are reversed biased.

The relation between the width of the depletion region and the reverse bias voltage V_b is described as

$$w_d = \sqrt{\frac{2\epsilon(V_b + V_{bi})}{Ne}} \tag{1.1}$$

in which N is the dopant concentration in the bulk and ϵ is the dielectric constant. When the depletion width extends fully to cover the thickness of the diode, the diode is fully depleted and the bias voltage at this point is called "depletion voltage". The strip tracker system is designed to achieve full depletion in sensors at the start of operation before radiation damage. After radiation damage, the detector will be operated under-depleted but the signal-to-noise ratio will still be acceptable. The signal-to-noise ratio is important to ensure good separation between signal and noise at the end of the detector life. Noise occupancy is required to be below 10^{-3} and efficiency above 99 $\%$. When the voltage is even higher than the depletion voltage, the field increases the speed of mobile charges.

When the sensor depletion region is considered as a flat plate capacitor between the two electrodes, its capacitance can be described as

$$C = \epsilon \frac{A}{w_d} = A\sqrt{\frac{\epsilon e N}{2(V_b + V_{bi})}} \tag{1.2}$$

When the built-in voltage is negligible compared to the applied bias voltage, the capacitance would be proportional to $\frac{1}{\sqrt{V_b}}$. When the sensor is fully depleted, the sensor capacitance is minimized and the signal that could be collected when a charged particle passes through is maximized [5].

When a charged particle passes through the sensor region, it loses energy according to the Beth-Bloch equation [7] as in Equ. 1.3,

$$-\frac{dE}{dx} = Kz^2 \frac{Z}{A}\frac{1}{\beta^2}[\frac{1}{2}ln\frac{em_e c^2\beta^2\gamma^2 W_{max}}{T^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}] \tag{1.3}$$

where:

- K is the constant $\frac{4\pi e^4}{c^2 m_e}N_A$
- e stands for electronic charge
- c stands for the speed of light
- m_e is the mass of the electron
- N_A is the Avagadro's constant
- z is the charge of the incoming particle
- Z stands for the atomic number of the material
- A is the atomic mass of the material
- β is the speed of the incoming particle
- γ is the Lorentz factor
- W_{max} is the maximum kinetic energy that can be transferred in a single collision

- I is the mean excitation energy
- $\delta(\beta\gamma)$ is the density effect correction to the ionization energy loss

The energy deposited in the sensor can create electron-hole pairs in the depletion region (also known as the sensitive region). The mean energy needed for generating an electron-hole pair is E_i, which is 3.6 eV in silicon. The number of electron-hole pairs created for a particle with deposited energy E is $\frac{E}{E_i}$ and thus the charge that can be collected between the electrodes is $\frac{E}{E_i}e$.

When the mobile charges (electron-hole pairs) are generated in the sensor, they start to drift towards the diodes under the electric field (V = V_{bi} +V_b) and are collected on the electrodes. The drift velocity can be described as

$$\vec{v} = \mu\vec{E}, \quad \mu = \frac{\mu_0}{[1 + (\frac{\mu_0 E}{v_s})^\beta]^{\frac{1}{\beta}}} \tag{1.4}$$

, where μ is the mobility of the mobile charge, μ_0 is the low field mobility, v_s is the saturation velocity of the carrier and β is an empirical constant used to fit the data. [6] Electrons and holes have different mobilities, 1350 and 450 cm^2/Vs respectively in silicon as low field mobilities μ_0 [6]. Electrons have higher mobility, thus signal arising from electrons being faster. This is detailed later in Sec. 2.2. The electrons and holes are the mobile charges that result in signals in silicon sensors. At the same time there is also thermal diffusion at play, though it only has a very small effect in the presence of the bias voltage. But it can be one source of noise, as will be discussed later.

Mobile charges moving in the sensitive volume of the sensor induce a signal current in the circuit. The current begins flowing once the charge is generated and starts moving. The induced current is based on the induced charge on the electrodes, which can be illustrated in Fig. 1.6. If a charge is generated near the upper plate and moves towards the lower one, it will initially induce most of its charge on the upper plate. Then as it moves to the lower plate, an increasing proportion of charge shifts to the lower plate. This is described quantitatively by the Shockley–Ramo theorem [8] [9]. The instantaneous current can be expressed in

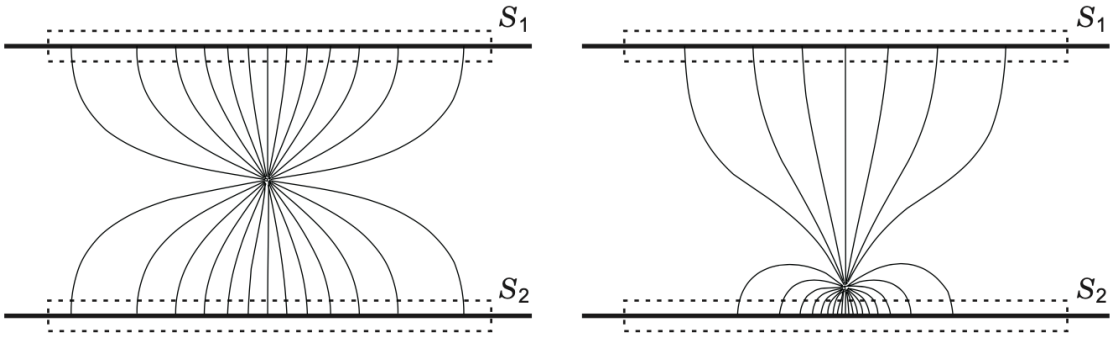


Figure 1.6: Left: A charge q positioned in the middle between two parallel plates induces equal amount of charge on each plate, yielding induced charge -q/2 on both S1 and S2. Right: When the charge is positioned close to the bottom plate, more field lines terminate on the lower panel than the upper one, so more charge is induced on S2 than on S1. [6]

$$i = -q\vec{v} \cdot \vec{E_Q} \tag{1.5}$$

in which $\vec{E_Q}$ is the weighting field and $\vec{v}$ is the instantaneous velocity of the charge. The weighting field is determined by applying unit potential to the measurement electrode and zero to others.

As the charge move from one plate to another, its velocity can be determined with Equ. 1.4 and the current it induces at a certain moment on a electrode can be deduced from Equ. 1.5. The time needed for collecting the mobile charge can be calculated with its velocity. As can be seen, since the electrons have higher mobility than holes, the collection time for electrons is shorter, resulting in a faster signal.

The mobile charges in the semiconductor sensors do not necessarily all reach the collection electrode. The sensor silicon can suffer from imperfections induced during manufacturing, device fabrication and radiation damage. [6] These kinds of defects can introduce states in the sensor that can trap charge. In the presence of trapping, the mobile charge will have a finite lifetime before it is trapped and may not make it to the collection electrode. This can cause charge loss in the signal. Trapping makes it advantageous to use a faster signal pulse as the possibility of trapping is reduced.

The examples in this part are based on the sensor electrodes are two parallel plates. If the detector structure is more complicated (like in strip or pixel detector systems), the electric

field remains similar but the weighting field is very different. Most of the charge comes from the charges moving near the collection electrode where the weighting field is large. Therefore, the signal in n-in-p sensors is mainly from electrons, resulting in a faster signal. A faster signal helps reduce charge trapping, thus increasing the sensor radiation tolerance.

1.2 Noise Charges During Signal Processing

The signal generated in the sensors is collected and passed down the circuit, as discussed in the previous section. But along with the signal, there is also noise collected and passed down. Three common noise sources present in a silicon strip detector are thermal (Johnson) noise, shot noise and $\frac{1}{f}$ noise. [6]

- Thermal noise is caused by velocity fluctuations from thermal excitation and is obviously dependent on environmental temperature. The spectral density of thermal noise is independent of frequency. So the noise is considered "white". The noise increases as the temperature goes up. The RMS voltage evolved in the circuit is described as

$$dV^2 = 4ZkTdf \tag{1.6}$$

, in which Z is the impedance of the circuit, k is the Boltzmann constant, T is the temperature and *df* is the frequency band considered. [10]

- Shot noise come from the number fluctuation when charge carriers are injected into a sample independent of one another. The thermionic current flow that pass through a p-n junction as a "dark current" or "leakage current" is a common example. Shot noise is also independent of frequency and dependent on temperature. The noise also increases as the temperature increases as described in the Arrhenius law [11],

$$I = I_0 exp(\frac{-E_g}{2k_B T}) \tag{1.7}$$

where I is the dark current, E_g is band gap energy (between valence and conduction bands) and k_B is the Boltzmann constant.

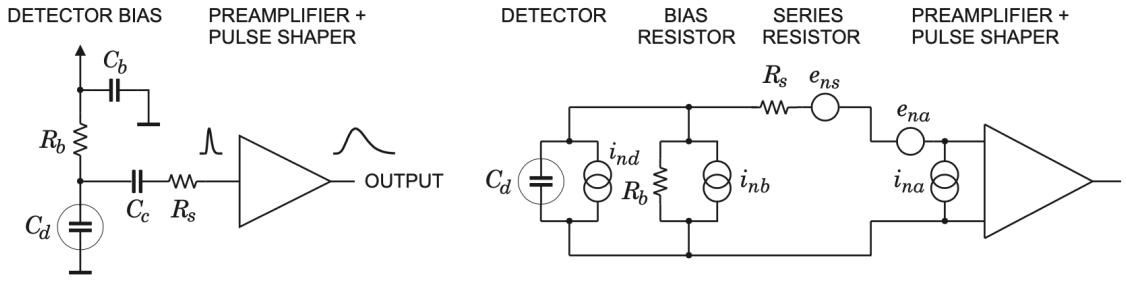


Figure 1.7: A typical detector front-end circuit and its equivalent circuit for noise analysis. [6] In the right plot, i_{nd} stands for the "shot noise" in the sensor. i_{nb} is the thermal noise current through R_b. e_{ns} is the voltage noise source introduced by R_s. e_{na} and i_{na} are respectively the voltage and current noise components of the amplifier and the shaper.

- $\frac{1}{f}$ noise has many sources. It generally is generated from a combination of process with different time constants giving an overall $\frac{1}{f^\alpha}$ behaviour with α approximately to 1. One of these process is caused by trapping in silicon sensors. The charge carriers are trapped and then released with a time constant. This effect is particularly obvious when the frequency is low. This noise is dependent on frequency.

The noise and the signal are both present in the detector circuit, which is illustrated in Fig. 1.7. In the left hand side detector front end circuit, the detector sensor is represented by the capacitance C_d and the bias voltage is applied through resistor R_b. The bypass capacitor C_b connects external interference coming through the bias supply lines to the ground. The coupling capacitor C_c blocks the sensor bias voltage from the amplifier input. R_s represents any resistance between the sensor and the amplifier input. On the right hand side, i_{nd} stands for the "shot noise" in the sensor. There is a thermal noise current i_{nb} through R_b and this generates a voltage over the capacitor C_b. As R_s is series resistor, it acts as a noise voltage source, e_{ns}. For the amplifier and the shaper, they have both voltage and current components of noise, e_{na} and i_{na}.

As the i_{nd} flows through the detector capacitance C_d, it introduces noise voltage on C_d as well and the "white" spectrum of shot noise become dependent on frequency. Thermal noise gives noise voltage to the series resistance R_s. Since the strip sensor is focused on charge collection, in the end, it is the noise charge we are interested in. With some calculations [6], the noise voltage can be converted to equivalent noise charge. The equivalent noise charge is

the signal charge when the signal-to-noise ratio is 1, which is also equivalent to the amount of noise charge.

Thermal noise is independent from frequency but now coupled with C_d, shot noise and $\frac{1}{f}$ noise are both dependent on frequency. The bandwidth of the signal is usually different from the noise bandwidth. The shaper is designed to select as much signal as possible and reject as much noise as possible in order to maximize the SNR. In the strip tracker system, the signal from the sensor and the response of the pre-amplifier are very fast compared to the shaping time needed in the shaper. So the selection of the bandwidth is realised in the shaper design. At the same time, the shaping time of the shaper has to limit the possibility that signal pulses overlap with each other and become indiscernible. There are other limiting factors on the shaping time as well, which will be discussed below.

The equivalent noise charge with can be summarised as

$$Q_n^2 = i_n^2 F_i T_S + e_n^2 F_v \frac{C^2}{T_S} + F_{vf} A_f C^2 \tag{1.8}$$

, in which $i_n^2 F_i T_S$ is the current part of the noise, $e_n^2 F_v \frac{C^2}{T_S}$ is the voltage part of the noise, $F_{vf} A_f C^2$ describe the $\frac{1}{f}$ noise,C is the sum of all the capacitance shunting the input, F_i, F_v and F_{vf} are the parameters determined by the frequency or time response of the shaper and T_S is the shaping time for the shaper. As some noise sources, e.g. thermal and shot noise, are dependent on the temperature, the total noise increases as the temperature goes up. In the case of the strip tracker, a $CR - RC^2$ shaper is used. The CR part works as a high pass filter and the RC part is a low pass filter to select the signal bandwidth. The RC^2 filter produces a sharper fall-off in frequency than a single RC.

As can be seen from Equ. 1.8, the current noise increases proportionally with the shaping time while the voltage noise decreases with shaping time, which relation is illustrated in Fig. 1.8 . The $\frac{1}{f}$ noise is independent of shaping time. As shown in Fig. 1.8, the minimal noise is achieved when current noise and voltage noise are the same. Here T_S is the optimal shaping time for minimizing the noise charge. Combined with bandwidth optimization and minimizing overlapping signal pulses, this provides a limitation on the shaping time design.

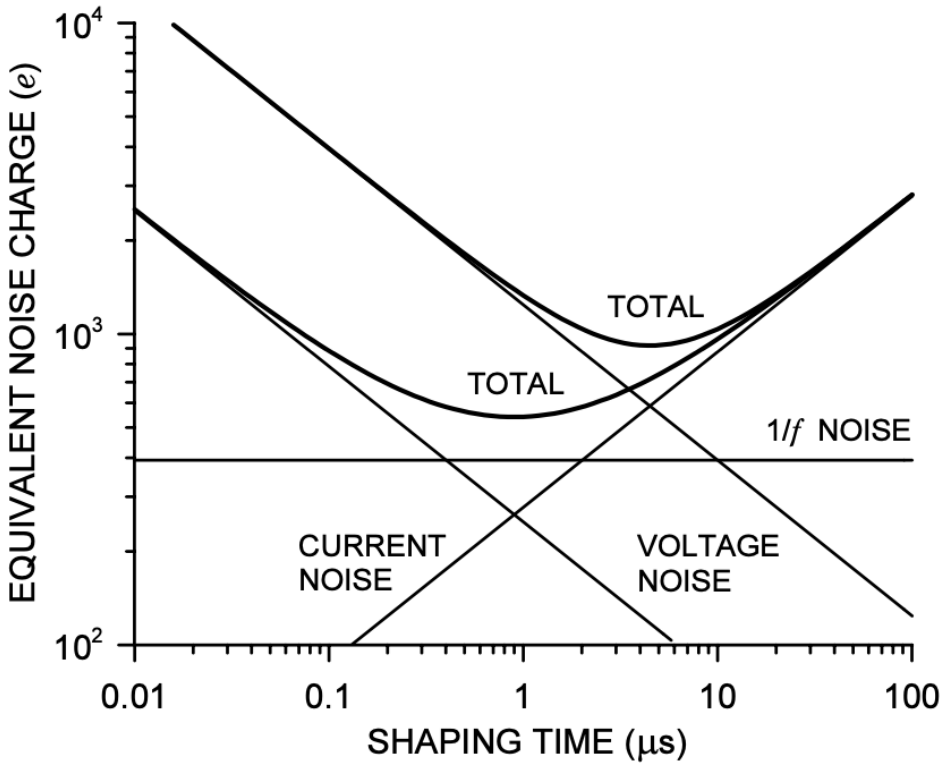


Figure 1.8: An example of equivalent noise charge relation with shaping time. The voltage noise increases with shaping time while the current noise decreases with shaping time. $\frac{1}{f}$ noise is constant. The total noise is at the minimum when the current and voltage noise are equal. If one of the three increases, the total noise also increases. Increased voltage noise is shown as an example. [6]

As discussed, the shaping time of the shaper is a key factor in the detector front end. In the strip tracker system, the signal pulse from the sensor and the pre-amplifier are both very fast. The pulse width received at the output mostly describes the shaper shaping time. The FWHM of the pulse is one way to describe the shaping time and adopted by the strip tracker. If the pulse lasts too long, the pulse will last for several bunch crossings (BCs) so that events in consequent BCs can be merged together, as mentioned as the out-of-time pile-up process in Sec. 1.1. This introduces more additional noise into the system. As a compromise from these limits, the shaping time in the ITk strip is limited to within two BCs, which is 50 ns. The data for the triggered BC is recorded together with that from the preceding and following BCs. The 01X run mode in ITk strip is when there is hit on a strip in the BC of interest, there needs to be no-hit on the strip in the BC before and there is no limit on the BC after. This approach can limit noise and also does not contribute significantly to pile-up with only a small loss of efficiency.

1.3 Threshold and Binary Output

As shown in Fig. 1.4, after the shaper the data is sent into the discriminator. As shown in Fig. 1.9, the shaper output signal goes into a threshold discriminator, with the other input the threshold. If the amplitude of the pulse is larger than the threshold, the output is 1 and if it is lower than the threshold the output would be 0. This leaves only 1 and 0 as the possible outcomes, which makes it a binary system. The ITk strip detector adopts the binary system as shown in Fig. 1.9.

It is obvious to see that if the threshold is set too high, even the signal can not pass through. The output will always be 0. If the threshold is set too low, even the fluctuation introduced by noise would be able to surpass the threshold. The output will be 1 almost all the time. In neither case the output represents the signal. The goal in setting the right threshold is to include as much signal as possible whilst rejecting as much noise as possible. As shown in Fig. 1.10, some noise will always be included. But if the noise rate is controlled well, the SNR can be optimised. The requirement of the strip tracker by the end of life is to make sure that the signal efficiency is above 99 % and keep noise occupancy below 0.1 %.

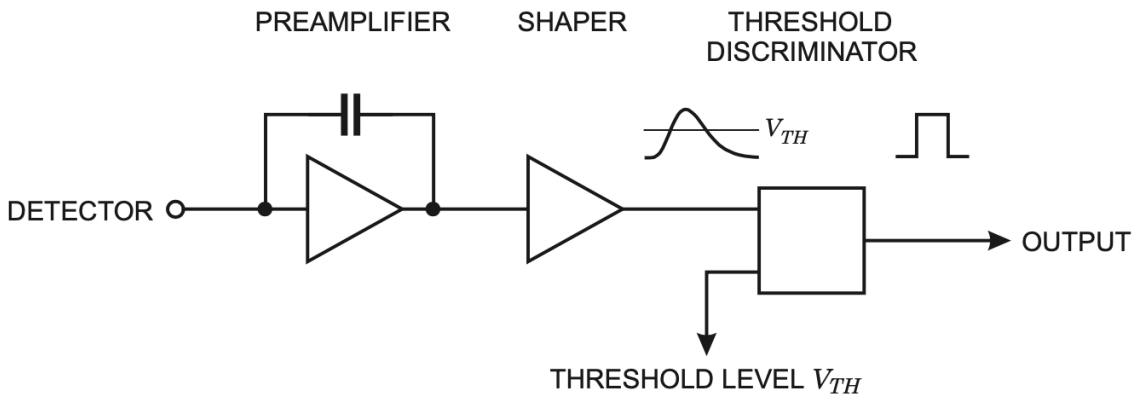


Figure 1.9: A threshold discriminator at the output of the shaper provides a digital output whenever the shaper output exceeds the threshold level. Instead of the detector, the charge can also come from a calibration circuit that can inject known amount of charges and calibrate the system. [6]

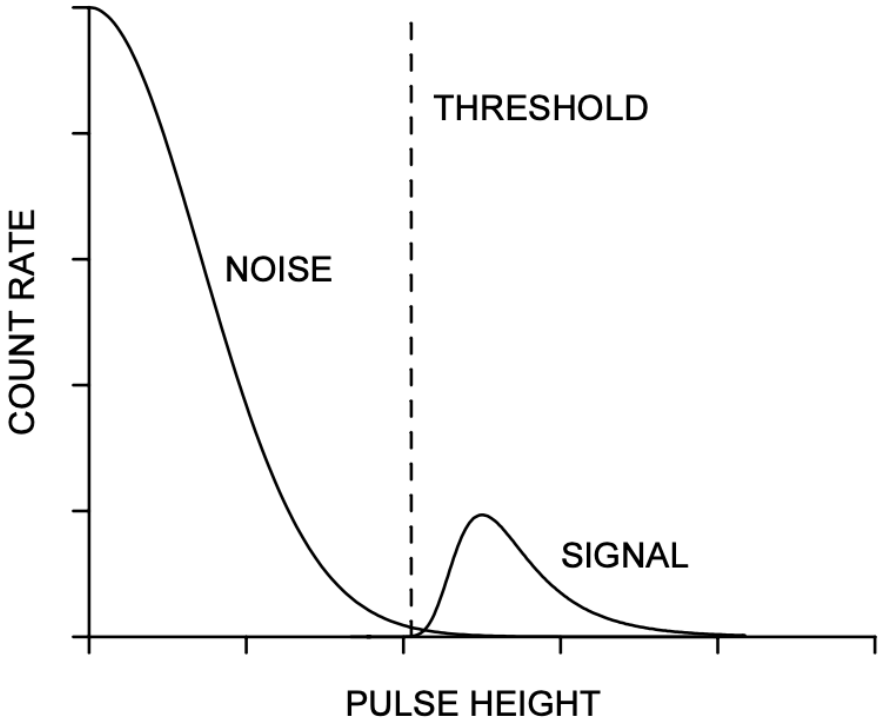


Figure 1.10: In a binary system the threshold must be set low enough to keep most of the signal but also high enough to reduce noise rate. The noise rate is usually much higher than the signal rate but the amplitude is lower. In this example the threshold setting the signal is beginning to get rejected but a noticeable rate of noise still surpasses the threshold. [6]

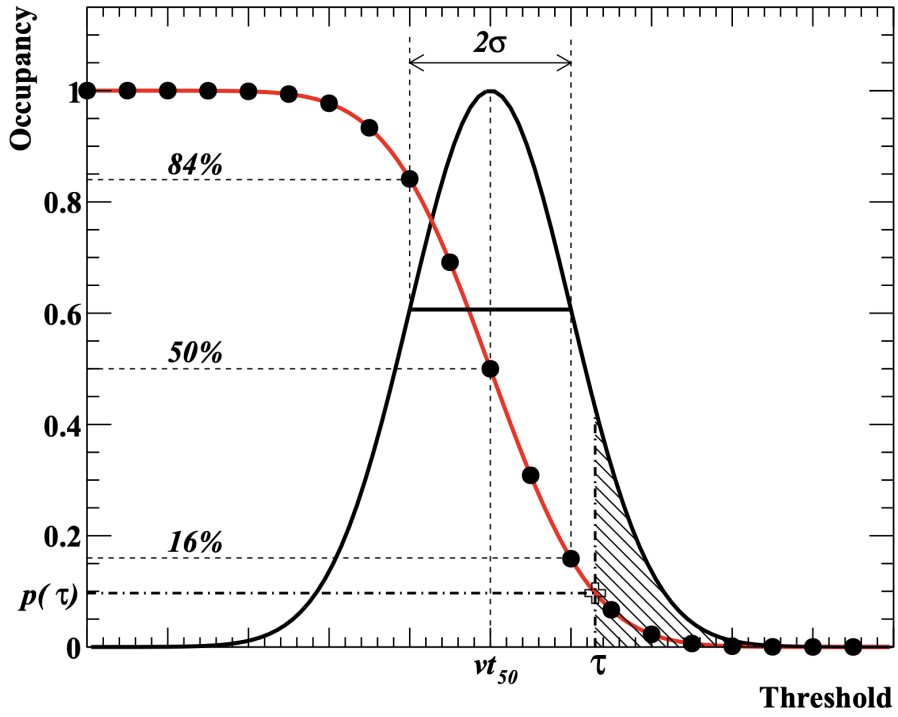


Figure 1.11: A threshold scan. Threshold τ is varied in steps and the signal pulse is convoluted with a Gaussian electronic noise. At a given threshold τ, the occupancy is described as p(τ) and corresponds to the dashed area. [12]

For a signal with fixed amplitude, in the case of no noise, the relation between occupancy and threshold distribution will be a step distribution from 1 to 0. But in the presence of noise, the distribution will be smeared. When a known calibration pulse is convoluted with a Gaussian-distributed electronic noise, as shown in Fig. 1.11, the probability of the signal being larger than the threshold should be proportional to the complementary error function, defined as

$$erfc(\frac{z}{\sigma}) = 1 - \frac{2}{\sqrt{\pi}} \int_0^z e^{-t^2} dt \tag{1.9}$$

[12]. The σ in Equ. 1.9 is $\sqrt{2}$ of the σ in the normal distribution. The σ is an estimate of the RMS of the electronic noise. The occupancy versus threshold distribution in Fig. 1.11 is called an S curve. The threshold where the occupancy is 50 % is the VT50 point when the threshold is measured in voltage. It corresponds to the input charge amplitude.

To calibrate each channel of the sensor strips, there are calibration capacitors for each channel. A pulse of known voltage is sent to each channel to provide a given charge. For

each value of charge injected, the threshold DAC is scanned to get the VT50 and output noise. Then the input charge is varied to get a VT50 and an output noise at each charge injection. The linear part of the curve between VT50 and input charge can be fitted to obtain the gain for this channel. [1] Then the output noise is divided by the gain to obtain the input noise of this channel.

[1] The gain of the pre-amplifier is designed to be linear in the low charge region, and be decreasing in the higher charge region (to save power consumption). For the separation of signal and noise, we are therefore interested in the gain in the low charge region (ie. the linear region).

2 | The ATLAS ITk Silicon Strip Detector Barrel

This chapter gives an overview of all the components on barrel staves of the ATLAS ITk Silicon Strip Detector. Results of studies on pre-irradiation of ABCStar chips and the frequency and voltage operation window of ABCStar chips are given in Sec. 2.1.1.

The ATLAS ITk Silicon Strip Detector [4] is composed of two major sections, the barrel part and the end-cap part. The ATLAS ITk strip detector, composed of four concentric barrel layers and one end-cap section with six disks on each of its barrel sides, covers the pseudo-rapidity range up to $|\eta| = 2.7$. Pseudo-rapidity is a spatial coordinate describing the angle of a particle relative to the beam axis. It is defined as

$$\eta = -ln(tan(\frac{\theta}{2})) \tag{2.1}$$

, where θ is the angle between the particle direction and the positive direction of the beam axis. The barrel layers are parallel with the beamline and range from -1400 mm to +1400 mm along the beam axis. Each barrel layer is built from staves, that provide mechanical, electrical and cooling services to the barrel modules. The inner two barrel layers accommodate the Short Strip (SS) modules, while the outer layers have Long Strip (LS) modules. The sensor size are the same, but short strip sensors are divided into strips half the size of the long strips. Therefore, there are four rows of strips for short strip sensors and two for long strip sensors. The total strip width is 96.4 mm.

The end-cap modules of six different kinds are mounted on the petals, where 32 petals compose one end-cap disk. Strips of the end-cap sensors are radially distributed and point to the beam axis center, with strip lengths varying from 19.0 mm to 60.1 mm. Stereo angles between the strips implemented in both the barrel and the end-cap systems provide the 2-dimensional information on the position of the particle track. In the barrel system, the modules on each side of the stave are rotated by ± 26 mrad with respect to the beam line resulting in the total rotation angle of 52 mrad between the strips. In the end-cap system the total stereo angle of 40 mrad is achieved by the implementation of 20 mrad stereo angle directly in the strip sensor design. The stave and petal populated by the barrel and end-cap

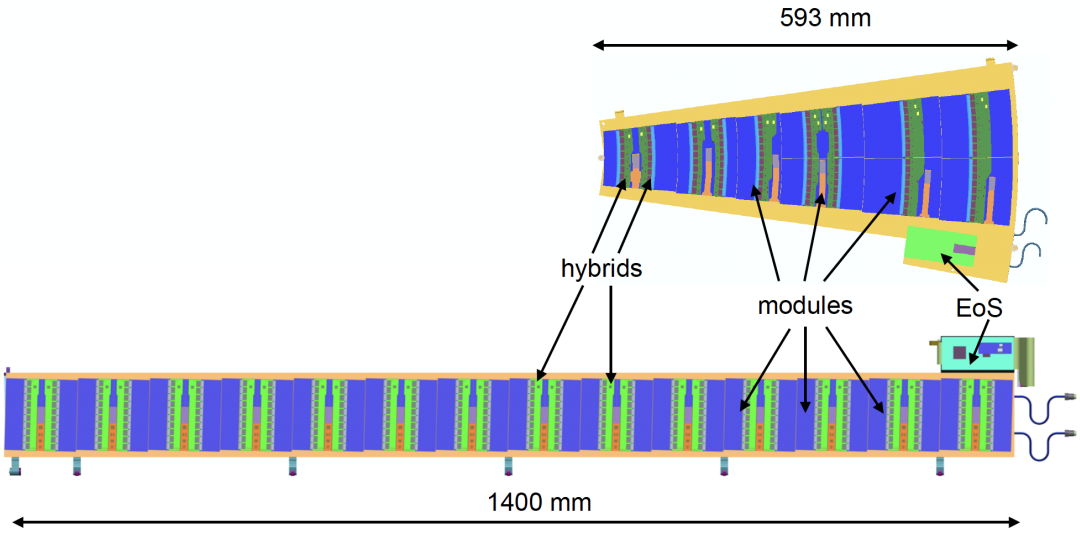


Figure 2.1: Layout of staves for both end-cap and barrel staves. The end-cap petal is on the top, and the barrel stave is the bottom one. EoS: end of stave card, which connects the stave with the off-detector electronics. The configuration of the barrel stave is a RHS one as the EoS card is on the right hand side. Figure source: [4].

modules, respectively, are shown in Fig. 2.1. The focus of this thesis is the barrel part of the strip tracker. The different parts of the barrel part are discussed in more details in the sections of this chapter.

2.1 ASICs

Four different application-specific integrated circuit (ASIC) chips have been designed and used for the silicon strip tracker. The ABCStar (ATLAS Binary Chip Star) chips' main purpose is to convert incoming charge signal from sensor strips into hit information. Other functionalities are detailed in Sec. 2.1.1. [13] The HCCStar (Hybrid Controller Chip Star) chips serve as the interface between ABCStar chips and the bus tape, eventually the off-stave world. [14] Ten ABCStar chips and one HCC chip are glued together to make a hybrid. The AMAC (Autonomous Monitor and Control Chip) and BPOL12V chips are on the power board of the module. [15] [16] [13] The AMACs provide monitoring and interrupt functionality and the BPOL12V chip takes input around 11V and has a DC-DC converter to provide output of 1.5 V for the hybrids. They will be detailed in Sec. 2.3.

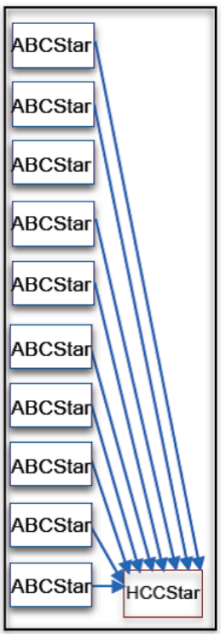


Figure 2.2: ABCStar and HCCStar communication scheme. [13]

The ABCStar and HCCStar chips are especially relevant in this thesis and are introduced in more detail in Sec. 2.1.1 and Sec. 2.1.2. The communication scheme between HCCStar and ABCStar is illustrated in Fig. 2.2, which is direct and shaped like a star , thus the "Star" in naming [13].

2.1.1 ABCStar Chips

The ABCStar chips serve all functions required to process signals from 256 strips of a sensor section to output a binary read-out. The data are sampled at the bunch crossing clocking rate (BC) and stored for 12.8 μs (equivalent to 256 events) in the "pipeline". There are two levels of triggers in the design. The L0 trigger is the global trigger, which works at 1 MHz. It serves as the event trigger and starts the readout of the detector hit information from the pipelines to the buffer memories on the front-end ASICs. [4] The event buffer can hold 128 events. There is another trigger, the PR trigger, which is a regional trigger with only regional data of interest. [1] The PR trigger is no longer in use in the ITk upgrade but the

[1] One option that was considered for the ITk trigger was to use a regional trigger. In this scheme, an L0 trigger initiates readout of the detector in the region around the triggered signal. This data is processed by the L1 trigger and if the trigger is satisfied, this initiates the full readout of the detector.

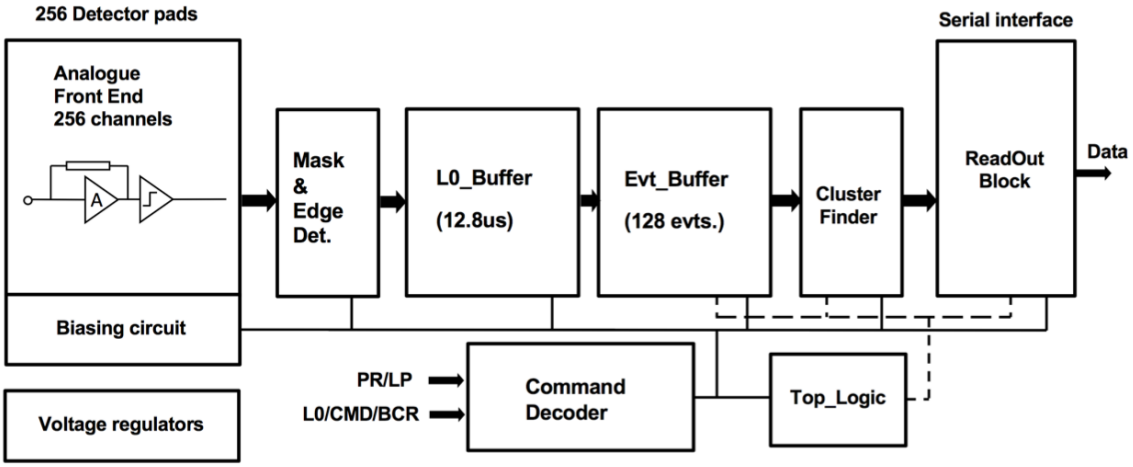


Figure 2.3: Block diagram of the ABCStar chip. [4]

design remains in the ABCStar chip, as shown in Fig. 2.3.

The main functionality blocks are: front-end including threshold and calibration controls, power regulation, command decoder, mask and edge detection, L0Buffer, EventBuffer, cluster finder and read-out logic. "Top_Logic" deals with PR and LP triggers. The front-end is optimized to have a noise level below 1000 electrons after irradiation. A resistor is used in the feedback of the pre-amplifier. The resistance feedback improves noise performance before and after irradiation. Even when the discriminator threshold changes from irradiation damage, the circuit can keep the current correct. [4] [17] The discrimination level is set to reject noise whilst keeping signal and after discrimination, the binary output for front-end channels are sampled and stored in L0Buffer at each bunch crossing. At each L0 trigger reception the event with the correct latency is transferred to EvtBuffer (event buffer) and maintained for 128 L0 (128 μs at 1 MHz L0 rate) and tagged. When a trigger requests a certain event with its event ID, the event is then processed through the cluster finder to obtain "clustering" information. "Cluster" is used in ATLAS to describe how many neighbouring strips record signal over discriminator threshold in one event. The readout block formats information into packets and ready for data transmission at a rate of 160 Mbps. The chips are delivered in wafers in the shape of circular disks before being diced into individual chips.

ABCStar chips adopt the CMOS technology and can be affected by irradiation. When a CMOS p-n junction with an oxide layer is irradiated (as featured in Fig. 2.4), electron-hole

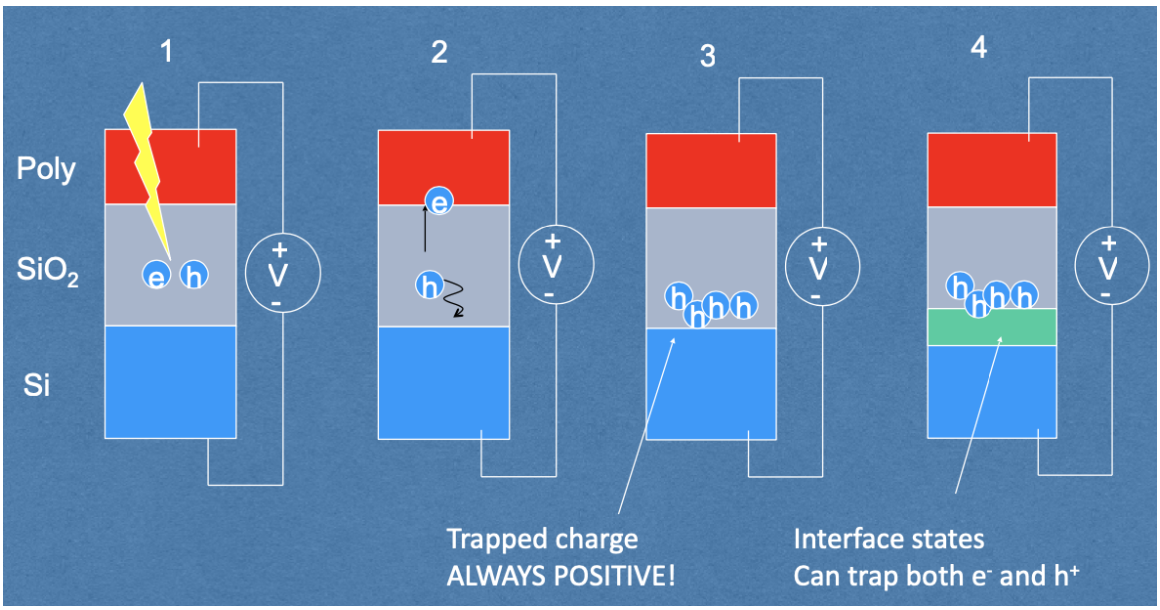


Figure 2.4: Illustration of irradiation damage in CMOS chips. [18]

pairs are created. As electrons have higher mobility than holes, they are removed much faster. The holes are trapped near the interface in oxide, thus in the oxide charges are always positive. The interface region is created due to radiation damage and both positive and negative charges can be trapped in the interface. For NMOS transistors, negative charges are trapped.

As shown in Fig. 2.5, for a typical NMOS transistor, positive charge accumulates with irradiation in the oxide region (STI region) whilst negative charge accumulates in the interface region in the p-bulk. Thermal energy would increase the charge movements, thus contributing to the removal of both oxide charge and interface charge. If not operating at high temperatures, the trapping times are significant, the oxide charge is faster to accumulate and also faster to dissipate. The oxide charge accumulation affects the chip performance as it increases leakage currents and in extreme conditions, open the gate at lower voltage than expected. The negative charge in the interface section helps reducing the leakage current, therefore improving for the chip performance.

Since the oxide charge is faster to accumulate and faster to dissipate, it is mostly dominant in the beginning of irradiation. As the dose goes up, the interface charge accumulation becomes more noticeable. Then the interface charge starts to overpower the oxide charge.

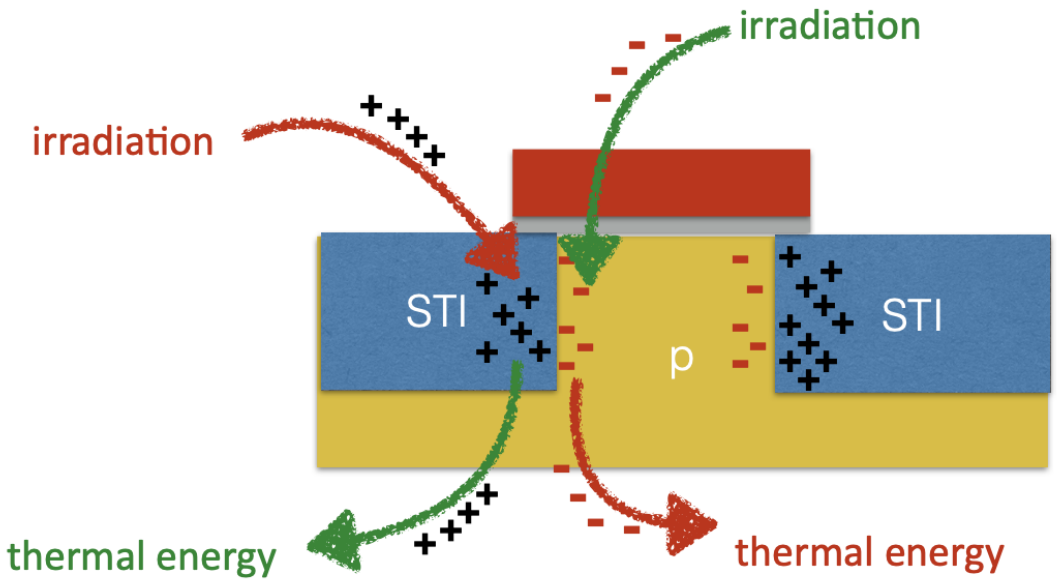


Figure 2.5: Illustration of oxide charge and interface charge in an example NMOS chip. STI stands for shallow trench isolation and is usually silicon oxide in this case. [18]

As a result, the leakage current across the gate should have a peak feature. The peak in the digital leakage current vs radiation dose is greatly suppressed during subsequent irradiation. Since the oxide charge is faster to dissipate, the interface charge will be more likely to reside when the irradiation stops. If the irradiation starts again, the oxide charge accumulates to the original level again fast. After an irradiation, in the subsequent irradiations the digital leakage current increases rapidly with the dose. However, it ends up following the same curve of leakage current vs dose as would have been obtained from a single dose irradiation, as shown in Fig. 2.6 for the digital part of ABCStar chips.

Leakage currents are dangerous to the ITk system because two main reasons. One is that the heat generated by leakage currents and it increases risks for thermal runaway [2], which is dangerous for the system. The temperature in the sensor increases the leakage current, which in turn increases heat dissipation in the sensor. If the thermal path to the cooling loop has too high a thermal impedance, then this can result in thermal runaway. The other reason is that the voltage drop along transmission will increase with leakage current. There

[2]Thermal runaway is an effect when one thermal effect triggers other process, resulting in an uncontrollable increase in temperature.

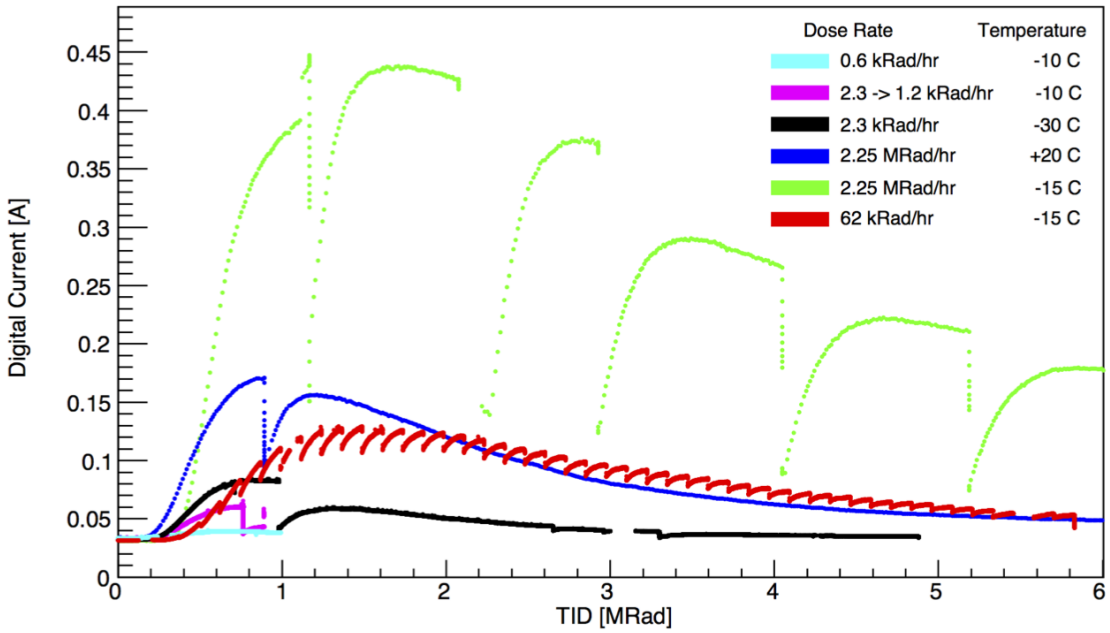


Figure 2.6: Digital current vs. TID for ABC130 chips during X-rays irradiations at different dose rates and temperatures. [4]

are two issues with voltage drops. The round trip voltage drop needs to be below 1 V to ensure the BPOL12V is operated with optimal efficiency. The voltage drop along the return (also called “ground”) side needs to be below 200 mV to ensure the signals remain safely within the common mode range of the receiver. The EoS card is detailed in Sec. 2.5. It communicates between the stave and the off-detector electronics.

It is also clear that once the chip has enough dose to pass the peak, the leakage current will cease to be a problem from Fig. 2.6. This effect prompts a way to suppress the size of the peak in the leakage current issue that chips should be pre-irradiated before mounting so that the accumulated dose has past the peak. It is planned that all chip wafers are pre-irradiated using ^{60}Co sources. The analogue leakage current is observed to be less affected by irradiation. As the analogue circuit is designed with "Enclosed Layout Transistors" (ELT) [19] to ensure radiation tolerance, the leakage current issue is under control. But the ELT design takes up too much space to be used in the digital circuit in the chip design.

To study the positioning of the peak and if different batches of chips show differences in the leakage current peak, 11 chips were irradiated at RAL with an X-Ray machine in Jan. 2022.

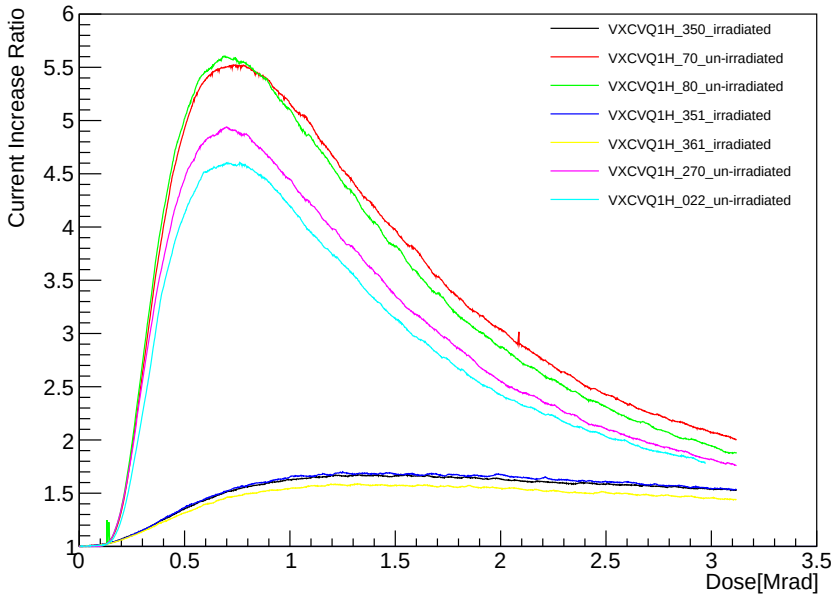


Figure 2.7: Dose versus digital current increase ratio for chips from the same wafer. Chip number 350, 351 and 361 have been previously irradiated in Taiwan to 8 MRad (SiO_2).

In Fig. 2.7, all chips are from the same wafer while in Fig. 2.8, the chips are from the same position on different wafers from the same batch. It can be seen that chips from the same position on different wafers have quite similar irradiation peaks while there are more variety of peaks when it comes to chips from different positions on the same wafer. There are three pre-irradiated chips in Fig. 2.7 as well. They have been irradiated to 8 MRad (SiO_2). The maximum expected lifetime dose for ITk strip is around 66 MRad (Si). This is still well below the lifetime dose. But if the dose is high enough to pass the current pulse, the leakage current will not be problematic.

There is also a leakage current rise with radiation dose with the pre-irradiated chips. But their peak magnitude is greatly reduced compared to the unirradiated chips. This result agrees with the theory of radiation damage on ABCStar chips and also shows that if the chips are irradiated past the peak region, they will not have a large irradiation peak. The peak position is around 0.8 MRad (SiO_2). As a result, pre-irradiation of chips should be introduced before mounting to avoid the leakage current issues.

The ABCStar chip is tuned to operate at 1.2 V for low voltage digital power and 160 Mbps

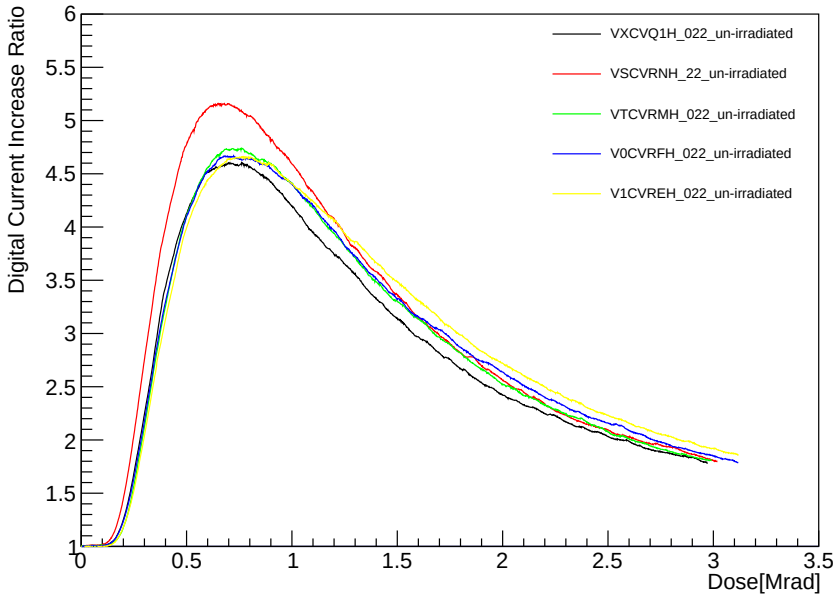
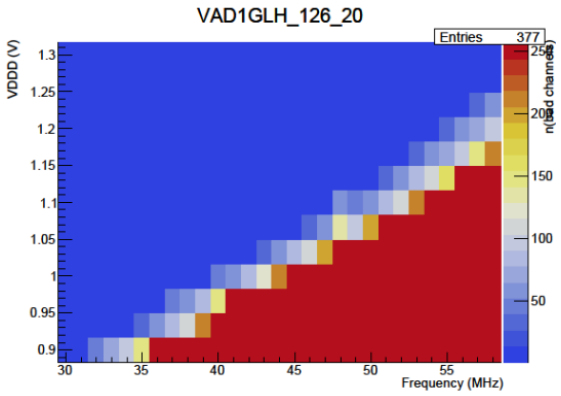


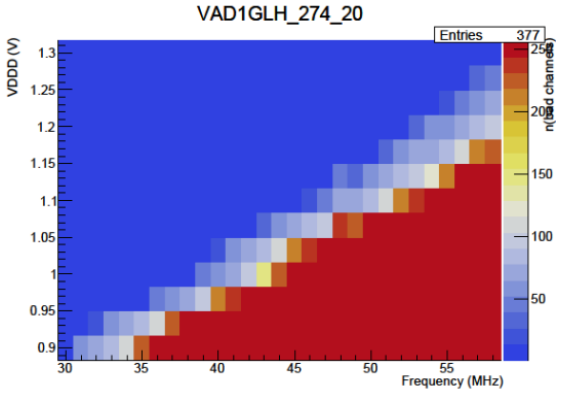
Figure 2.8: Dose versus digital current increase ratio for chips from the same positions on different wafers. They are all the 22nd chip on different wafers. These wafers are from the same lot.

data rate. The input voltage for the hybrid is at 1.5 V but locally regulated to be 1.2 V for ABCStar and HCCStar chips. During operation, there might be voltage and frequency drift for different reasons. It is useful to find out the voltage and frequency operation region. If a chip is operating outside the operational region, data transmission is likely to be faulty, resulting in digital errors. Any channel with such an error was defined to be bad. The frequency and voltage is illustrated in the "shmoo plots", which depict the relation between digital voltage, the frequency and the number of bad channels. In 2021 studies were performed at RAL for shmoo plots with the latest ABCStar chip design. As shown in Fig. 2.9, the X axis is the frequency, and the Y axis is the digital voltage. The chip is tuned to operated at 40 MHz clock for frequency and is tuned to 1.2 V for the digital voltage. The color scale describes how many channels are bad. There are 256 channels per chip and red means that they are all bad while blue means operating normally.

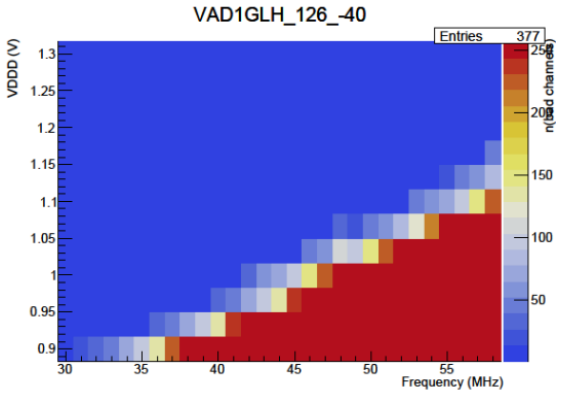
Fig. 2.9a compared with Fig. 2.9c as well as Fig. 2.9b compared with Fig. 2.9d show that the operational region is larger when the temperature is lower. Fig. 2.9a paired with Fig. 2.9b and Fig. 2.9c paired with Fig. 2.9d show that radiation damage shrinks the



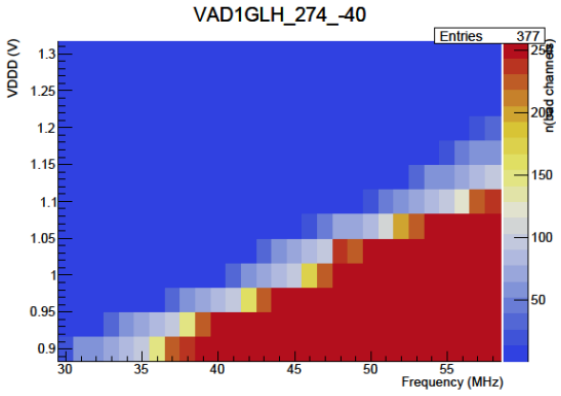
(a) The frequency and voltage vs bad channels relation with an unirradiated chip at 20 °C.



(b) The frequency and voltage vs bad channels relation with a chip irradiated to 50 MRad (SiO_2) at 20 °C.



(c) The frequency and voltage vs bad channels relation with an unirradiated chip at -40 °C.



(d) The frequency and voltage vs bad channels relation with a chip irradiated to 50 MRad (SiO_2) at -40 °C.

Figure 2.9: Shmoo plots at 20 °C and -40 °C with an unirradiated and a irradiated chip. The red region is all channels are bad while the blue region means no channels are bad and the chip is operating properly.

operational region. This agrees with our expectation that the ATLAS ITk operates with very low temperature and irradiation damages chip performances. The temperature has a larger effect on the chip performance while irradiation has smaller effects. In lower temperature, transistors operates faster, resulting in better performance thus larger operation window.

2.1.2 HCCStar Chips

The Hybrid Controller Chip (HCC) is the interface ASIC between the signalling on the stave and the front-end of ABCStar chips. There is one HCCStar per hybrid. [4] HCC has stave-side inputs for the bunch crossing clock and control signals including triggers, known as the CCR. CCR stands for Clock Control Reject, the control signals needed by a hybrid, including Trigger, Timing and Control (TTC) information. After HCCStar processing, the controls are sent to each ABCStar on the hybrid. Data coming from the ABCStars are sent through the HCCStar to be queued and sent to data lines on the stave.

The block diagram of the HCC is shown in Fig. 2.10. [4] The HCCStar receives a 160 MHz clock (which is synchronous with the 40 MHz bunch crossing clock). The CCR data are received in the HCCStar and then sent to ABCStar chips at 160 Mbps. Data packets from the ABCStar chips are sent to HCCStar and phase aligned to 160 Mbps. The output data rate from the HCCStar to the EoS in normal operation will be 640 Mbps.

2.2 Silicon Sensors

The sensors in the silicon strip tracker are AC-coupled with n-type implants in a p-type bulk (n^+-in-p). The design of a sensor strip is shown in Fig. 2.11.

Inter-strip isolation is achieved by p-stop implants, uniform p-spray or a combination of both. The p-stops prevent shorts between strips. The silicon thickness is between 300-320 μm and the radiation requirements are to withstand the simulated maximum fluence of $8.1 \times 10^{14} n_{eq}/cm^2$ [3] as well as an ionising doze of 33.3 MRad (Si) and to operate up to 500 V bias voltage. There is a 1.5 times safety scaling and the actual design can withstand the

[3] n_{eq}/cm^2 is the 1 MeV neutron equivalent fluence (NIEL) in Si.

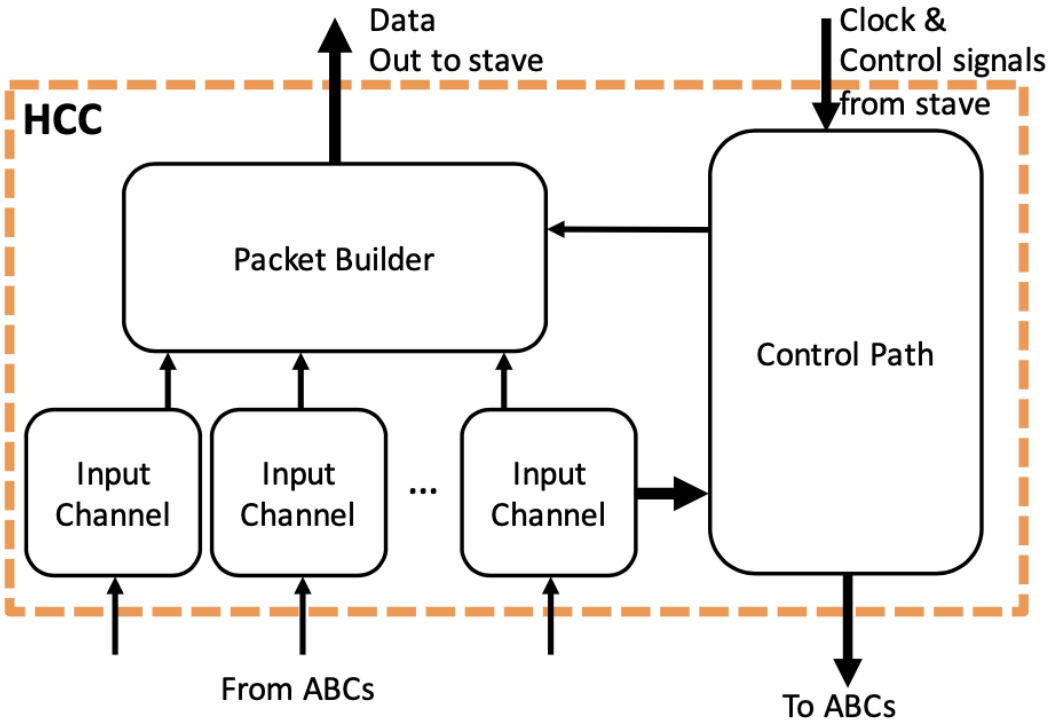


Figure 2.10: Block diagram of the HCCStar chip. Figure source: [4]

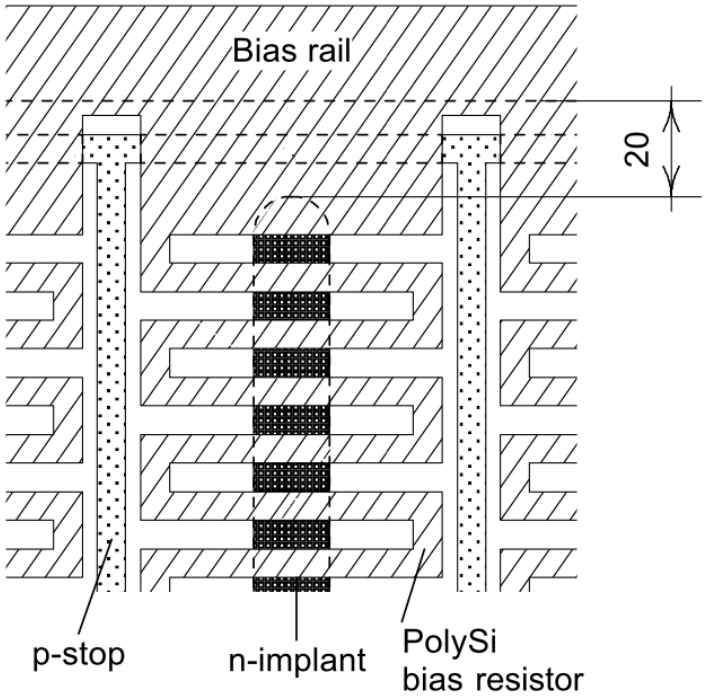


Figure 2.11: Design of a punch-through strip. The collecting electrode is connected to the bias rail via large resistor, which is connected to the back plane. The p-stop between the strips reduces charge trapped in interface between strips. Figure source: [20]

maximum fluence of $1.2 \times 10^{15} n_{eq}/cm^2$ and the doze of 50 MRad (Si). The sensor type is chosen based on no type-inversion as well as the amount of signal retained after irradiation. The electron has higher mobility than holes. Sensor type inversion happens for a p-in-n sensor after radiation damage. The formation of charged defects leads to a change in the effective doping concentration and the effective parts converts from p-in-n to n-in-p. [21] When electrons are the collected carrier, the signal loss due to charge trapping is reduced. As the irradiation accumulates, the bias voltage eventually fails to fully deplete the sensor. As explained with Ramo theorem in Sec. 1.1, the weighting field is the strongest near the collecting electrode. Since the n-in-p detectors do not type invert, high field region near the collection electrode will be maintained after radiation damage.

The barrel sensors cover an active area of 96.64 $\times$ 96.67 mm^2. There are 1280 read-out strips per bank that are wire-bonded to channels on ABCStar chips. The strip pitch is 75.5 μm. The strips are parallel to the edge of the sensor. When placed on the stave, the sensors on both sides are tilted each by ± 26 mrad with respect to the beam line resulting in the total rotation angle of 52 mrad between the strips as mentioned before. The inner two layers use Short Strip sensors to ensure higher granularity and therefore lower occupancy in the region of higher particle flux. The outer two layers use Long Strip sensors. Short Strip sensor strip length is 24.1 mm and Long Strip sensor strip length is 48.2 mm. The expected signal charge will decrease from 17300 to 11500 electrons with radiation damage for the sensors on the inner barrel which receive the maximum fluence of $8.1 \times 10^{14} n_{eq}/cm^2$. [22] [4]

2.3 Modules

A module is made up from one or two hybrids, a sensor and a power board. As discussed in Sec. 2.1, a hybrid is composed of ten ABCStar chips and one HCC chip glued on a flexible circuit. A short strip (SS) module has two hybrids and a sensor with four rows of short strips while a long strip (LS) module has one hybrid and a sensor with two rows of long strips. A schematic drawing of a SS module layout is shown in Fig. 2.12. ASICs on hybrids are introduced in Sec. 2.1 and the sensors are in Sec. 2.2. The last part of the module to discuss is the power board.

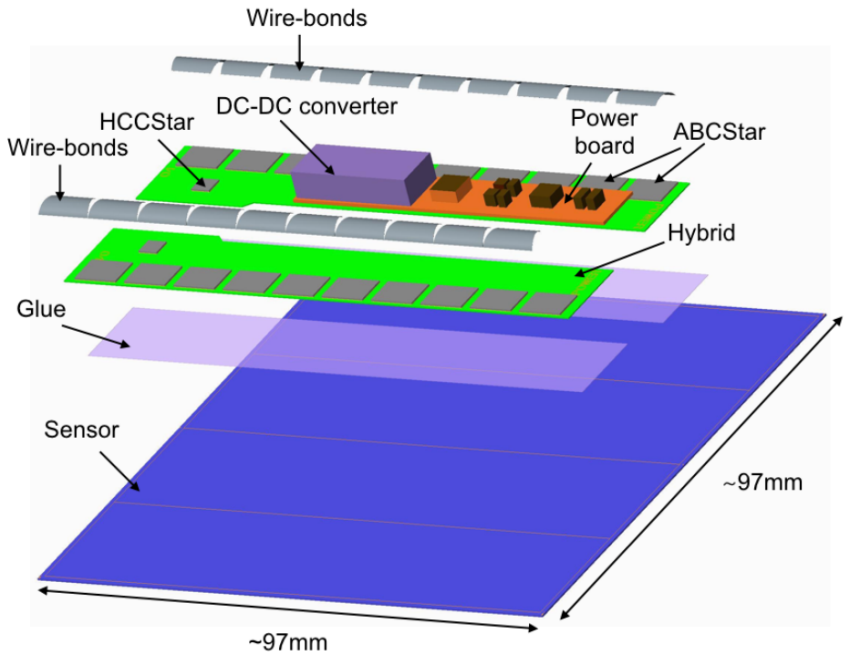


Figure 2.12: A scheme view of a SS module. [4]

The power scheme for the ITk strip tracker modules is DC-DC. [4] A DC-DC power scheme converts a direct current (DC) input supply to a DC output supply usually at a different voltage level. The DC-DC power scheme allows for transmission at higher voltages and therefore reduces the amount of passive material for the same voltage drop. Since it is on the detector, it is required to be irradiation hardened. The power board functions to provide all necessary power to ASICs and auxiliary on-detector electronics for monitoring, control and sensor high voltage (HV) biasing. The power board has four sections of electronics to serve its purpose: the control and monitoring ASIC AMAC, the sensor bias HV switch, the silicon sensor HV bias filtering circuit and the DC-DC power block using BPOL12V ASIC. A photo of a prototype power board is shown in Fig. 2.13.

The AMAC (Autonomous Monitor and Control Chip) ASIC provides both monitoring and interrupt functionality. It is connected to the lpGBT chip on the EoS card on the stave via differential transmission lines. The AMAC monitors voltages, temperatures and sensor bias currents on strip modules. It also provides control to switch bias potential "on" and "off" for sensors with a GaNFET [23] as well as controlling powering for ABCStar and HCCStar

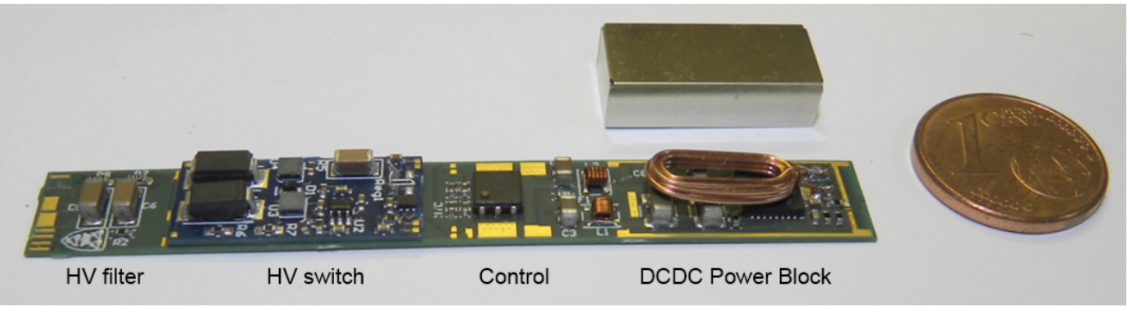


Figure 2.13: Prototype Barrel Power Board with coil and prototype shield box in the background. [4]

chips.

The DC-DC converter module is embedded with a buck converter ASIC, the BPOL12V chip. A buck converter (step-down converter) is a DC-to-DC converter that steps down voltage (while stepping up current) from its input to output. [24] The BPOL12V chip provides output voltages in the range of 0.6 to 5 V from an input voltage between 5 and 12 V. This is because we want to maintain high efficiency for the DC-DC converter. The output current can be up to 4 A. The switching frequency can be adjusted in the range of 1 to 3 MHz. Operation is tuned to be 1.8 MHz. The other part in the DC-DC converter module contains a custom toroidal air-core inductor needed for the high magnetic field in the experiment. It is sealed in a metal box that functions as a Faraday cage so that the magnetic field does not leak. Leaking magnetic field can introduce excessive noise in the sensor strips underneath, which will be discussed in Chapter 6.

The HV Multiplexer is a circuit that can connect and disconnect sensors from the sensor bias bus. [4] The HV Multiplexer is used here because there are up to four sensors connected to the same power supply. Without the HV Multiplexer, one sensor in breakdown will prevent the others from being operable. A gate voltage is used to control a GaNFET transistor that serves as a switch for the sensor bias voltage [23]. The transistor needs to operate with up to 500 V as the sensor bias voltage. So the transistor also needs to be radiation tolerant. GaNFET is adopted as the material in this case as it has been shown to be sufficiently radiation tolerant.

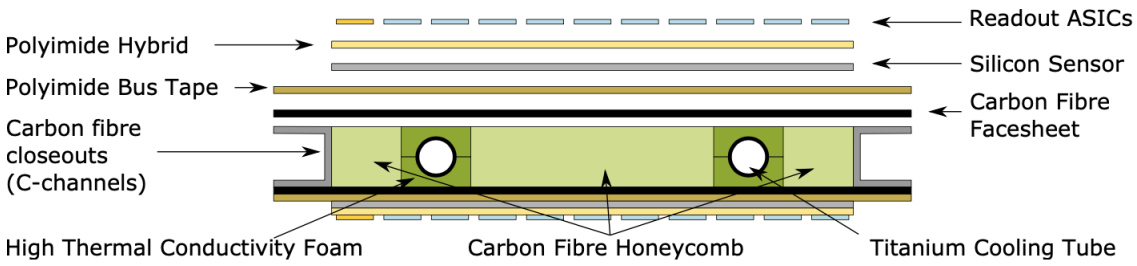


Figure 2.14: Schematic of the internal structure of the stave core, with the silicon sensors and ASICs added. Glue layers are not shown. Figure source: [4].

2.4 Bus Tapes

For the Silicon Strip Tracker, the detector will come in forms of end-caps and barrels composed of staves or petals. Staves consist of modules (as discussed in Sec. 2.3) and bus tapes. 14 modules are mounted onto a bus tape and a stave contains two bus tapes cocured to a carbon fibre skin. Then the two skins are combined with honeycomb and the cooling loop/thermally conductive foam to make a stave. The cross section is shown in Fig. 2.14. Since there are two bus tapes back-to-back on each side of the barrel stave, they are designed to be chiral, one left-hand-side (LHS) and the other right-hand-side (RHS). Fig. 2.1 shows the layout of one side of a core, the long rectangular one is a barrel stave while the top one is an end-cap pedal. The barrel part of the detector is the focus of this thesis.

Bus tapes [25] are integrated to provide functionalities from data transmission to power connection for the whole stave with modules mounted on top of them. They are the copper/polyimide circuits for the local support structures in barrels and end-cap petals. They distribute both low voltage (LV) DC (10-11 V) and HV DC (up to 550 V) from the EoS card to power boards on modules. They route control data to and from AMACs on power boards, electrical data from hybrids to the EoS card and CCR control signals from EoS to each hybrid.

2.4.1 Barrel Bus Tape

As shown in Fig. 2.1, the barrel bus is a long rectangular printed circuit board (PCB) unlike the end-cap ones. For the barrel part of the detector, there are two types of staves, long-strip (LS) and short-strip (SS), depending on the length of strips on them.

There are four HV lines serving three to four modules each, providing bias voltage for sensors on those modules. Four HV lines are to reduce the effect in case of single point failures. Differential pairs are used in the tape design to provide 640 Mpbs point-to-point data transport from hybrids to EoS. CCR is multi-drop at 160 Mbps, going from EoS to hybrids. A multi-drop bus is a bus in which all components are connected to the electrical circuit, the EoS in this case. A command is sent to all receivers on the bus but only the addressed device will respond. The other devices listen for the data they are intended to receive. The devices here are the modules. The muti-drop bus is adopted as a compromise. There need to be multiple sections in data transmission lines to reduce the influence of module signal reflection. But if there is one line per module, the stave will be unnecessarily wide and have excess dead areas. So the CCR is divided into four sections, each connected to five, four, four and one modules. For the module next to the EOS card, the data flow is in the opposite direction of the other modules and therefore has its own CCR section. There is a two-way communication between EoS and AMACs boards on power boards. The data rate is up to 4 Mbps. They end with small PCBs (terminal boards) which are loaded with termination resistors and are connected to the lines via wire-bonding.

There are also other lines on the tape, including the common calibration line from EoS to power boards and an OF line to transmit commands instructing the AMAC chip to turn off a module if needed. To provide grounding, screening and impedance control, a ground layer is beneath the CCR and data lines and accessible with bond pads.

For the lines on tapes, the copper thickness is very important. It determines the voltage drop along the LV and LV return lines. As discussed in Sec. 2.1.1, the voltage drop along the LV return lines needs to be lower than 200 mV and the total round trip voltage drop has to be below 1 V. Since the resistances along LV and LV return lines are very small and not easily

measurable, these resistances are indirectly indicated and monitored by resistance versus length for longer 100 μm wide lines like the data lines.

The general structure of a bus tape can be understood from Fig. 2.1. The modules and EoS card are mounted on the stave via glue and are wire-bonded to exposed conductive gold-plated pads on the tape. A tape has a double-sided copper/polyimide core and cover layers made from polyimide with a glue layer. Different vendors use different methods to access pads and bottom layers. The process adopted by Altaflex is using small openings cut in the top cover to access the pads on the copper layer. There are also openings in the base polyimide layer to allow access to pads on the bottom copper layer. These openings are made with laser ablation. A different approach is adopted by the CERN vendor. The connection between top and bottom layer is via vias but the cover layer openings are milled. The pads are plated with the ENIG (electroless nickel immersion gold) process. Information about the tape vendors are discussed in more detail in Sec. 4.4. This phase is defined as a bare tape. The bare tapes are co-cured with three layers of carbon fibre to allow the face sheet to become a co-cured tape and then two co-cured tapes are made into a stave.

To fulfill the purpose of bus tapes, detailed specifications come with the design in many aspects. For manufacturing factors, there can be a 10 % uncertainty on the copper thickness on the tape. This along with many other factors can influence the voltage and current values transmitted along the LV/HV power lines. The maximum and nominal voltages and currents are given in Table 2.1.

Name	Max/Nom V	Max/Nom for Voltage Source
LV (SS)	11/10	11.4/10.1 A
LV (LS)	11/10	5.5/4.9 A
HV	550	15-20 mA max

Table 2.1: Maximum and nominal voltages and currents for power lines. The maximum value is set to ensure safe operation of BPOL12V and the nominal value is an indicative number of voltage to be used.

Signal integrity is indicated with the impedance of the differential pair located on the sacrificial area of a tape. The allowed impedance should be between 90 and 110 Ω. The maximum attenuation at 1 GHz is 15 dB. There are pads used for wire bond pull tests to

determine the strength of wire bonds. Daisy chains are used for resistance measurements or for via reliability tests.

It is important to check the accuracy of the physical dimensions of the tape. Modules will be mounted at the nominal locations relative to precision plastic parts that will be used to mount staves to the cylinders. If the modules are not mounted in nominal positions relative to mechanical features on the core, there will be potential overlapping or gaps between modules. The gaps will introduce excess dead area on a stave. Therefore, if a tape is too short or too long, the bond pads on the tape will not be aligned well with the bonds pads on the hybrids and power boards. The X direction is defined as along the longitudinal direction, which is approximately 1400 mm long for a barrel tape in Fig. 2.1. The Y direction is perpendicular to the X direction in the tape plane. Z axis in later discussions is in the direction perpendicular to the X-Y plane. Distortion of features from the nominal positions along the X axis is required to be within 1 mm per meter over the full length of the tape. Especially the EoS region should have distortion within 150 μm in the X direction, as demonstrated in design plots in Fig. 2.16a. The location of bond pads compared to the tape center line in Y direction should be within 600 μm regarding the nominal position. Reception measurements of the tape dimensions are detailed in Chapter 4.

If there are distortions in the Y direction, the clearance will be compromised. Clearances from HV lines to the edge of the stave and clearance from the LV area to the sensor are important to maintain safe HV clearances. This is to avoid excessive HV leakage. The jig used for co-cure making process is shown in Fig. 2.15. There are slots in the sacrificial area of the tape that fit onto the circular dowel pins in the jig. The slots allow the tape to shrink or expand in the X direction but accurately control the distortion in the Y direction. The final pre-production tapes were deliberately made slightly too long so that the lengths after co-cure would come out close to nominal. The jig is made of carbon fibre with a very low coefficient of thermal expansion (CTE). The slots on the jig are made of invar [4].

The clearances are the distances from the sensor to the data lines on the bus tape, from the HV lines to the edge of the tape, as illustrated in Fig. 2.16b. Compromised clearances risk

[4]Invar, FeNi36, is a nickel–iron alloy with uniquely low CTE.

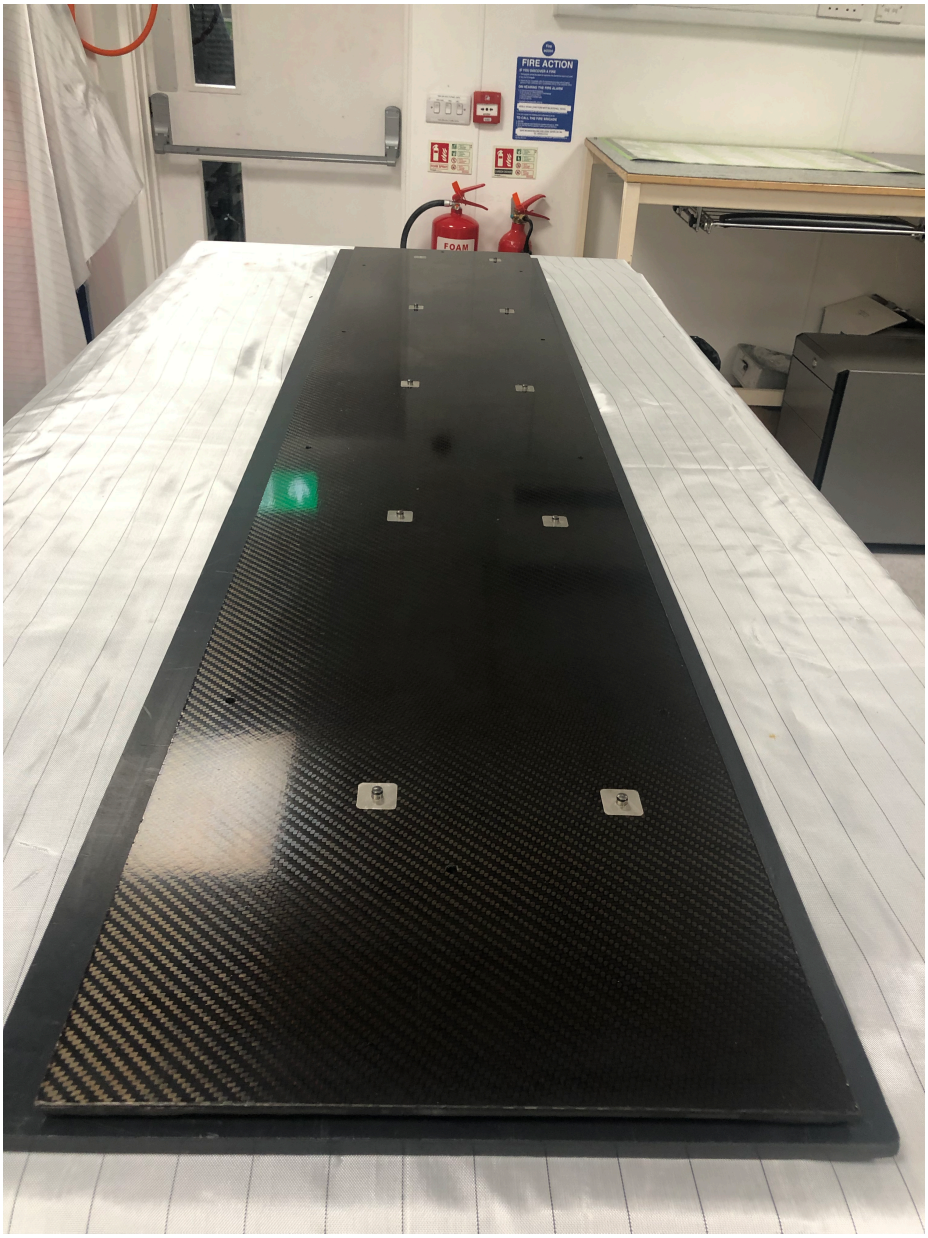
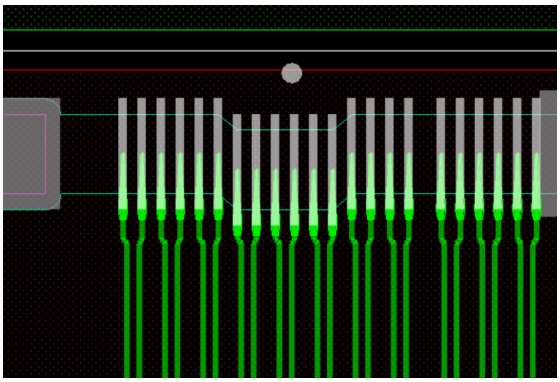
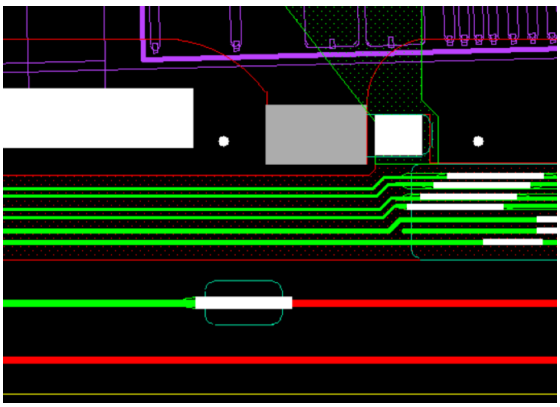


Figure 2.15: The co-cure making jig. The base plate is carbon fibre and rectangular invar pieces have been glued in. Precise 6-mm diameter holes have been drilled into the invar inserts. 6-mm dowel pins are located precisely at the centre of the invar inserts and these constrain the distortions of the tape in Y directions.



(a) Data lines in EoS region go in Y direction, the pad width in X direction is 150 μm. So the tape accuracy in X direction in the EoS region should be within 150 μm.



(b) Clearances of lines near a module. The distance from the bottom HV (bottom red line) line to the edge of a tape is 0.78mm. The distance from the exposed grounded pad (grey pad) to the sensor (region in purple lines) is 1.56 mm.

Figure 2.16: Bond pads locations in tape design files.

shorts and cuts on the lines, thus damaging the tape. Industry specifications for 500V from Underwriter Laboratories (UL) give clearance of 0.8 mm between two lines under cover layer and 1.8 mm for two exposed lines. These are shown to be conservative by previous tape manufacturing. The clearances are also studied. There are no significant leakage currents unless the clearance is below 100 μm. To validate the tapes, they are tested with HV at 1000 V, which is approximately double the maximum of 550 V that is planned for operation. The tape width is increased from 115 to 116 mm to increase clearances and all tolerances to be relaxed. This is to accommodate for larger distortions in the Y direction during co-cure (see Chapter 4).

The alignment between top and bottom copper layers of an Altaflex tape is required to be better than 350 μm. The alignment is checked by the positioning of a circle and a square as in Fig. 2.17. There is a square 1mm $\times$ 1mm on top copper and the circle on the bottom Cu layer is 300 um diameter. Misalignment can be identified easily. The thickness of the tapes can not differ from the nominal value by more than 10 %.

Left-hand-side (LHS) and right-hand-side (RHS) are used to define the chirality of tapes. As the tapes are arranged back to back in stave making, a LHS and RHS tape make a pair. There exist four configurations to serve different purposes, such as right-hand-side (RHS)

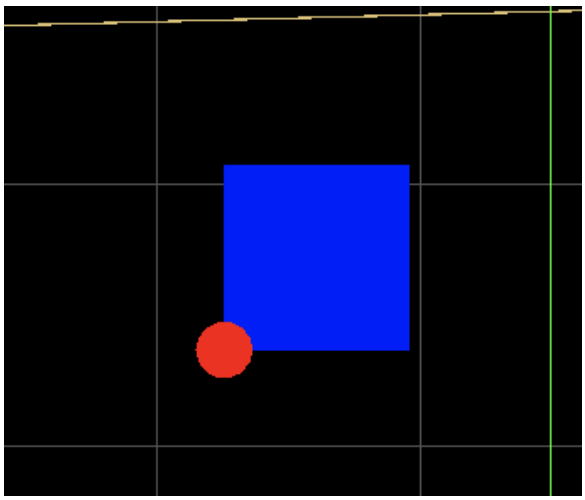


Figure 2.17: Visual inspection pattern for top-bottom layer copper alignment. The red circle is on top layer copper and the blue square is on bottom layer. If the circle is not on the corner of the square, the alignment is off.

or left-hand-side (LHS) short-strip (SS) or long-strip (LS) staves. Apart from the regions of interest, the tapes coming from manufacturers also have sacrificial areas. It means that the actual tape is part of the incoming product, with areas not of interest near edges. The main purpose of sacrificial areas is to minimise glue spillage onto bond pads but they are also used for test structures as well. Test structures are for wire bond pull tests, measuring impedance and attenuation of differential pairs and checking reliability of vias as discussed earlier.

Fig. 2.18 shows a bare tape, a co-cure tape and a stave put side-by-side.

2.5 Barrel Staves

14 modules are loaded on each side of a barrel stave as well as an end-of-stave (EoS) card on each side with links to the off-detector electronics. One side of a barrel stave is shown in Fig. 2.18 on the left. The modules are wire-bonded and glued to the tape. [4] The EoS card [26] handles all communication between the stave/petal and the off-detector electronics, and additionally also transfers the LV and HV from the power supplies to the stave/petal.

The EoS hosts up two lpGBTx (low power GigaBit Transceivers) high-speed serial communication ASICs [27] and an optical transceiver module VTRx+ (versatile transceiver) [28].

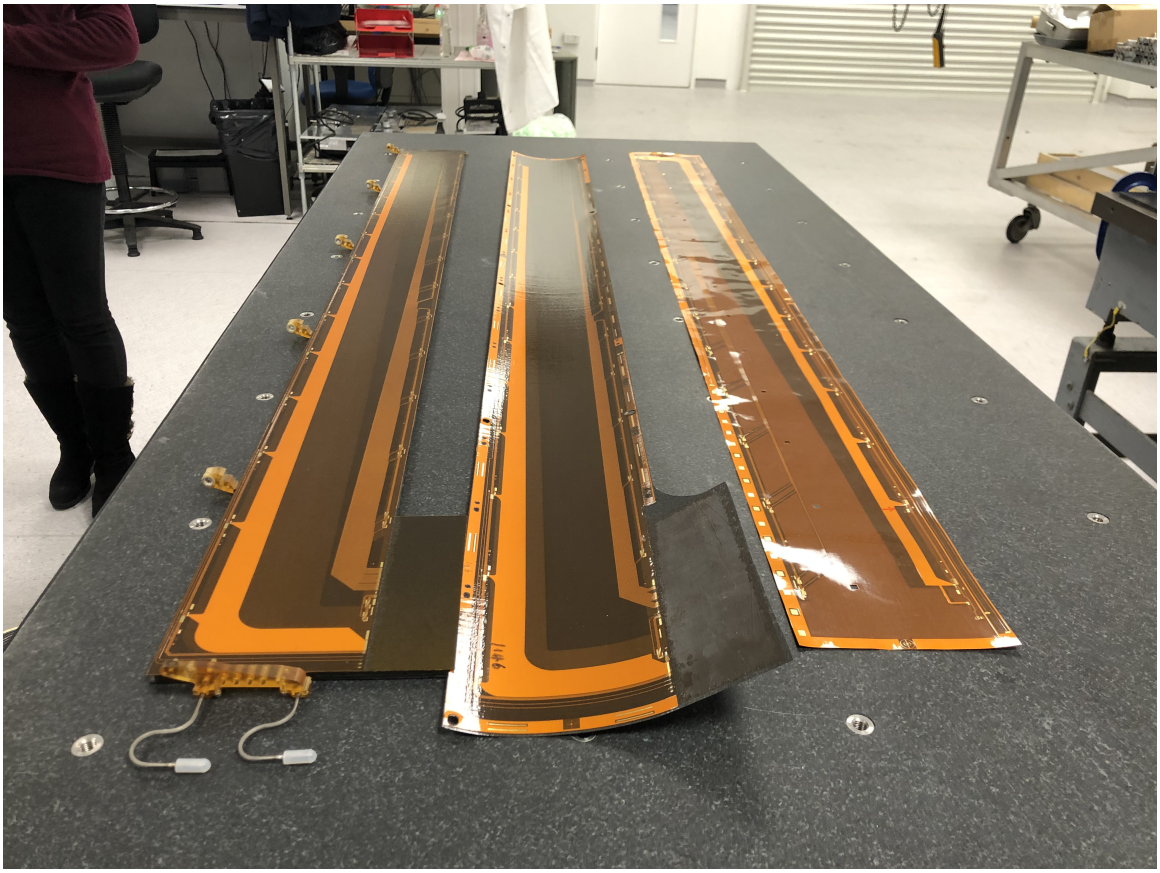


Figure 2.18: Three tapes placed by each other. The left one is a stave with a cooling pipe and lock points, which are captured in the brackets that are on the cylinder to locate the stave in the correct location. The middle tape is a co-cured tape. The EoS region carbon fibre sheet is in place. The tape is rigid in X-Y plane and a bit flimsy in the perpendicular direction. A co-cured tape is not flat after co-cure. During stave making, a co-cured tape is held flat on a vacuum jig. The right one is a bare tape. It is very flexible.

The lpGBTx is a high-speed, radiation-hardened Serializer/Deserializer (SERDES) chip that can do both serialising and de-serialising. For the uplink direction, it can multiplex up to 28 data lines at 640 Mbps to one output stream, which signal is then converted to optical on the VTRx+. For the downlink direction, 2.56 Gbps data is de-serialised to provide 160 MHz clock and 160 Mbps CCR data to the modules. The lpGBTx can also send commands and receive data from AMACs at a speed up to 4 Mbps. The lpGBTx also implements error correction to protect data from single event upsets (SEU). [29] [30]

The VTRx+ is a high-speed optical transceiver. The VTRx+ serves as opto-electronics for the data transmission between the EoS and the off-detector DAQ. [4] There are four channels of transmitters (Tx) and one channel of receiver (Rx). TRx is a transceiver. The Tx for ITk will operate at 10.24 Gbps and the Rx operates at 2.56 Gbps. The two ASICs on this transceiver is the GBTIA chip (Gigabit Trans-impedance Amplifier) [31] for receiving data and the LDQ10 chip [32] to drive the optical transmitter. The other parts of a VTRx+ are the Vertical Cavity Surface Emitting Laser diodes (VCSELs) and photo-diodes operating at a wavelength of 850 nm and multi-mode fibres.

The logical diagram is shown in Fig. 2.19. The CCR signals from off-detector are processed by the FPGA off-detector and sent through optical fibres to the EoS region on-detector. The incoming signal is optical, and all signals on staves are electrical. The optical to electrical conversion is performed by a photo-diode (PD) on the VTRx+. The now-electrical signal is then processed by the GBTIA and sent to a lpGBTx. The signal is then de-serialised and sent to HCCStars on hybrids. The HCCStar distribute CCR information to each ABCStar chip. In the other direction, the data from ABCStar goes to HCCStar. Then the data is sent to the lpGBTx on the EoS region and gets serialised. It is then sent to the LDQ10 chip and the photo-diode to be converted into optical signal. Then the optical data signal gets transmitted off-detector via optical fibres. There are also VSCELs and photo-diode arrays in the counting room to convert optical signals to or from electrical signals.

As there are two hybrids on each module for SS staves and only one for LS staves, the amount of data for SS staves is about twice as much as for the LS data. To transmit all the data from the stave, the SS stave has two Tx channels per stave side and the LS stave has

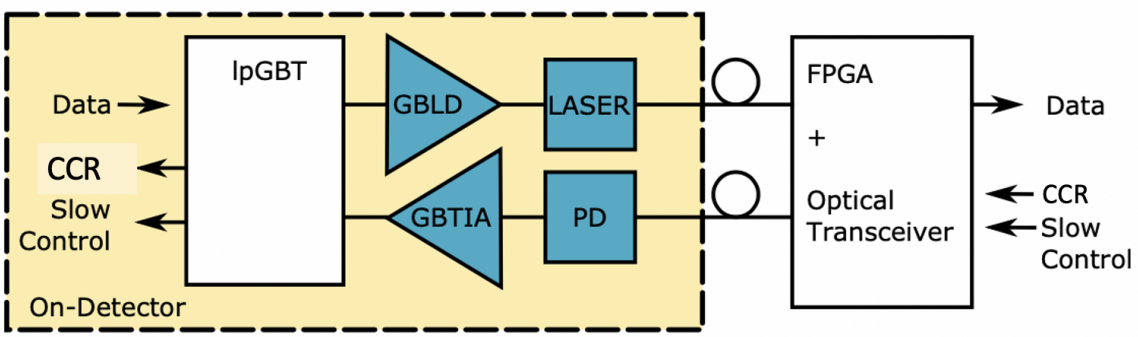


Figure 2.19: The opto-electronics read-out chain. The on-detector items are inside the dashed yellow box. PD is short for photo-diode. The functionality of the radiation tolerant ASICs is described in the text. The off-detector opto-electronics will use commercial off-the-shelf components. [4]

one Tx channel per side. There is one VTRx+ per sides of a stave (same for SS and LS). On a LS stave there is one lpGBTx per stave side. On a SS stave there are two lpGBTx to feed data into two channels of LDQ10. There is only one downlink (from off-detector to detector, also referred to as Rx) fibre per side. The secondary lpGBTx is configured by the main lpGBTx via the I^2C link. The high-speed data is passed through elinks. The downlink data transmission speed is 2.56 Gbps. Half of the bandwidth is taken up by error correction and the CCR data is sent to modules at 160 Mbit/s. In the uplink direction, there are 14 or 28 lanes (one differential pair per module for LS staves and two differential pairs per modules for SS staves) of 640 Mbit/s data from modules to the EoS card. The lpGBTx will be used to send data at 10.24 Gbps, which includes overheads such as error corrections. For SS staves, the physics data rate is 9.6 Gbps and for LS staves the physics data rate is 4.8 Gbps.

The input voltage for the EoS card is 11 V. It is converted to 2.5 V with the BPOL12V converter.An additional DC-DC converter is used to step down from 2.5 V to 1.2 V. The EoS card ASICs needs two input voltages, 2.5 V and 1.2 V. 2.5 V is needed for the VCSEL driver circuit in the LDQ10 and the GBTIA to bias the photo-diode. 1.2 V is needed for the digital logic in the LDQ10 and the lpGBT.

3 | Barrel Module Test Beam Data Analysis

Before the modules can be trusted to perform well on a stave in the LHC, they are first tested in beams with known particles and using a known tracking system to measure the efficiency of the module under test. Test beams can be used for controlled studies of performance of tracking detectors. For the ITk strip modules, there are several test beam campaigns designed and carried out to test different aspects of the module performance. Test beam tests allow detailed studies on performance parameters such as hit efficiency for charged particles.

A short-strip (SS) module was tested at the DESY (Deutsches Elektronen-Synchrotron) with 5.4 GeV electron beam in the Sept. 2019 test beam campaign, and the analysis of its data is the focus of this chapter. The main purpose of this test is to check and compare the module performance in cold (-30 °C) and warm (30 °C) environments. The ATLAS ITk will be operated at cold temperatures at around -35 °C. But the detector assembly and most of the initial testing is performed in room environment. So it is important to compare module performance at cold and warm temperatures.

This chapter will first introduce the experimental setup and theoretical background for the test beam experiment. Then it will include analysis results on pedestal, beam test and pulse shape related studies.

3.1 Experimental setup and theory background

The electrical performance of a module is tested by parameter scans, in which a certain parameter is varied and the system response is recorded. As discussed in Sec. 1.3, threshold scans are commonly used for the ITk strip tracker. The purpose of the test is to scan the module response at various threshold settings for ABCStar chips on the module. The signals from the sensors are amplified and then sent to the discriminator in the front-end (FE) of the channels in ABCStar chips.

The 5.4 GeV electron beam used is provided by the DESY electron synchrotron. [33] The

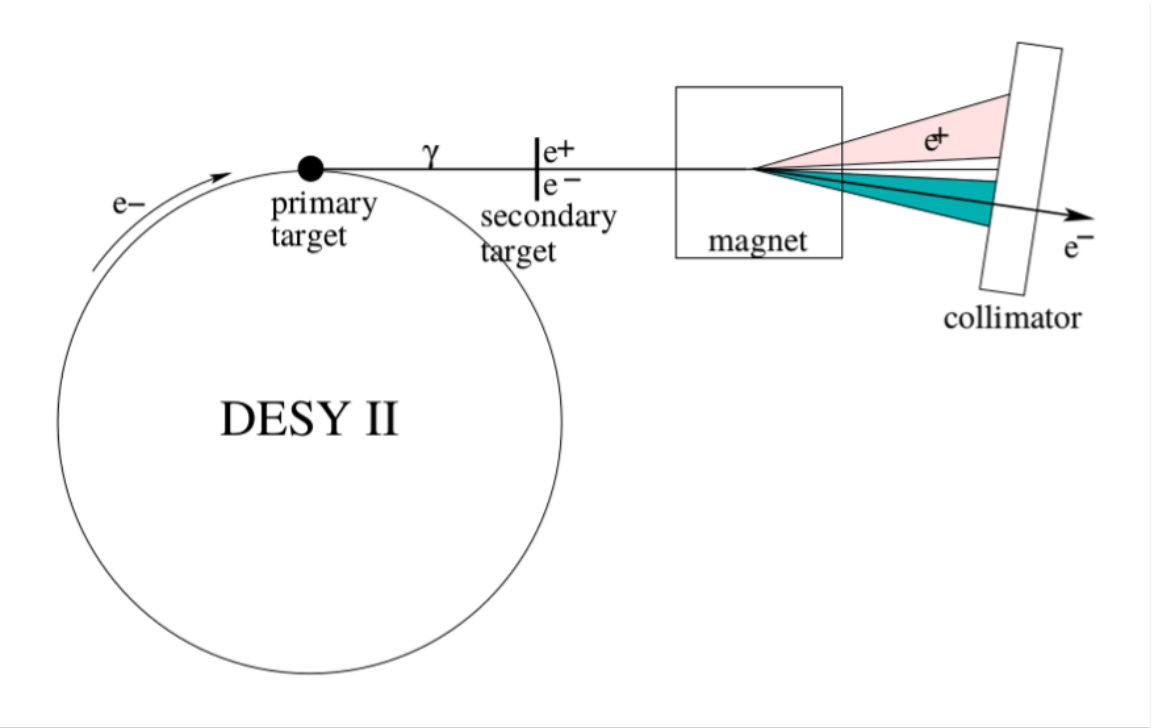


Figure 3.1: Electron generation for the test beam area 22 at DESY-II Testbeam Facility [33].

synchrotron circumference of 292.8 m and the synchrotron is also a pre-accelerator for the PETRA-III storage ring. Carbon fibres are moved into the beam to generate bremsstrahlhung photons, which leaves the line at a tangent. The photons are then directed at a secondary metal target to generate electrons. The beam is spread out by a dipole magnet and the beam with a certain energy is selected. The DESY beam generation is illustrated in Fig. 3.1. The maximum electron energy is 6 GeV from this synchrotron and the beam energy used in this study is 5.4 GeV as mentioned before.

As is shown in Fig. 1.11 and Equ. 1.9, in the presence of noise, the relation between signal occupancy and the threshold settings can be described by an S curve. The Digital-to-Analog Converter (DAC) is used to convert digital input signal to various amplitude of analog output. The threshold is set and varied in DAC counts from the outside world and then converted to voltage (usually in mV) inside the chips. The estimated conversion factors are calculated by simulations of the ABCStar ASIC.

The front-end is calibrated by injecting different charges into the circuitry. As discussed in Sec. 1.2, the calibration builds up a conversion between voltage and charge. With the DAC

and RC calibration that converts the voltage into charge, it is possible to know the charge equivalent for a given threshold in DAC settings. With this knowledge, it is possible to study the signal collection for each channel with a variable input.

The experimental setup is illustrated in Fig. 3.2. In this setup, the device under test (DUT), the SS module in this case, is placed in an EUDET-style [34] telescope system composed of Mimosa detectors [35] [36]. The telescope system consists of six Mimosa planes to provide tracking information, which counts from M0 to M5 in the illustration. As the module can only give a binary "hit" output, the trajectory of the incoming particle is given by the telescope system. Since the Mimosa telescope detectors record information on the scale of ms and the DUT operates in the scale of 25 ns, an extra fast timing plane is required for time matching. Both Alpide [37] and FEI4 [38] timing planes are placed in the system but in this analysis only FEI4 is used for timing information.

The square around the DUT represents a cooling box, in which the DUT is placed. The cooling box is cooled down with dry ice to reach about -30 °C for cold tests. The temperature is measured via a thermometer (thermocouple type K connected to a multimeter) located close to the module inside the cooling box. Then the module is placed in the test beam telescope structure facing the beam direction, with three Mimosa planes in the front and three behind, as shown in Fig. 3.2. Fig. 3.3 is a photo of the cooling box with the module inside.

In these studies, two sets of data regarding comparing cold and warm performances were taken with beam on. Dedicated runs without beam in the system, named pedestal runs [1], are used to obtain calibration information and to understand the electrical noises and other background performance. These data are used as the baseline compared to beam data. Pedestal data here were taken with beam off at both -30 and 30 °C. For data reconstruction, EUDAQ [40] and EUTelescope [41] were used. EUDAQ transfers the raw data files from the data acquisition into LCIO [42] formatted files. Then for pedestal data, the LCIO files are directly analysed. For beam data, EUTelescope is used to combine individual hits into

[1] "Pedestal" is used in ATLAS runs that are performed with no beam on and no charge injection to get background and calibration information.

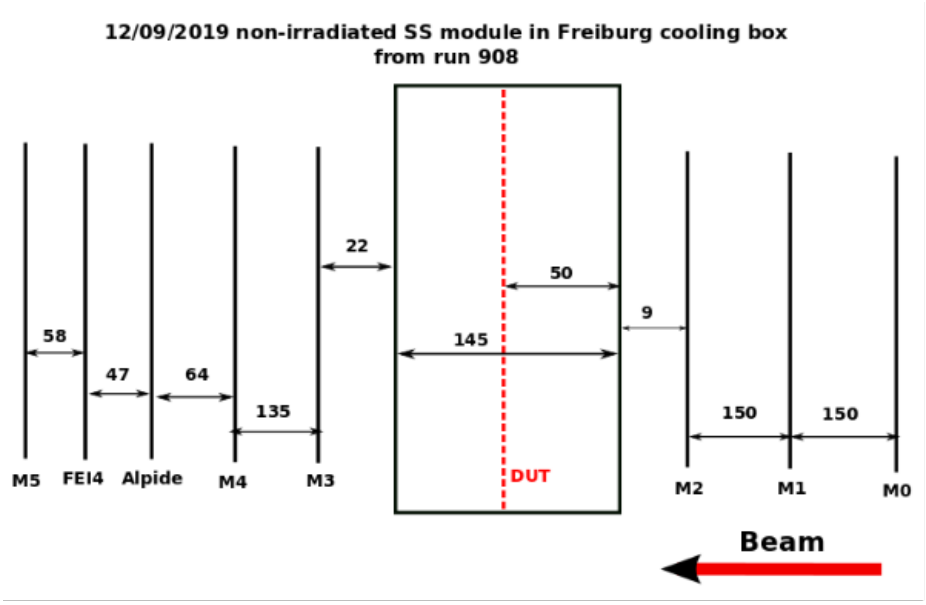


Figure 3.2: Sept. 2019 SS module test beam experimental setup. The EUDET telescope planes with Mimosa26 pixel detectors are labelled from M0 to M5. The numbers are the distances between planes in mm. In addition there are scintillator planes upstream and downstream of the DUT, which provide external triggers to the DUT. [39]

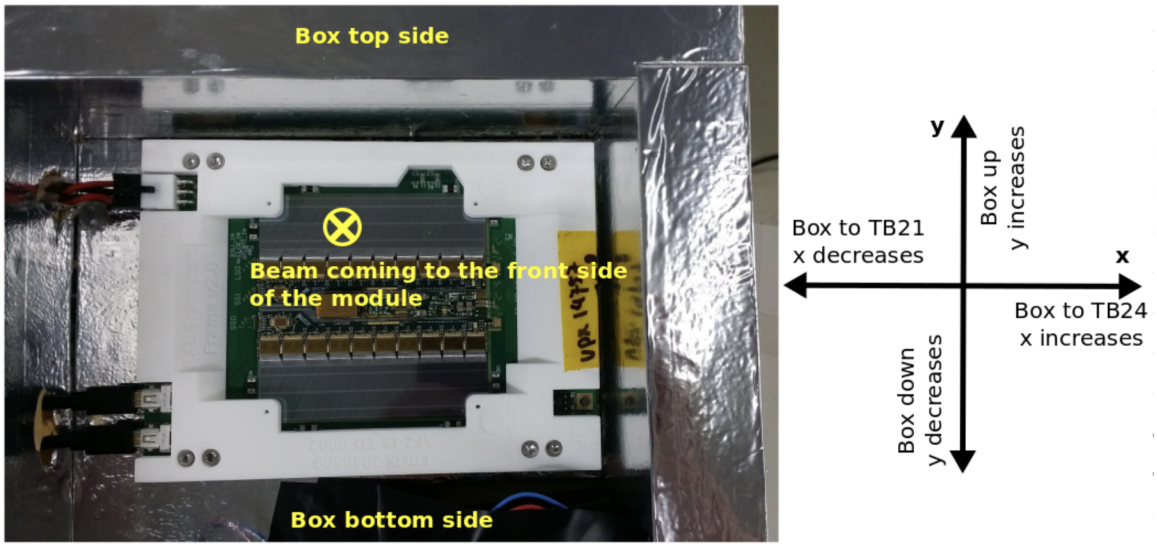


Figure 3.3: ITk Short Strip module installed in the polystyrene cold box, which has been tested in September 2019. The beam was centered on chip 4 as indicated by the cross. The beam profile covered a width equivalent to 123 strips. [39]

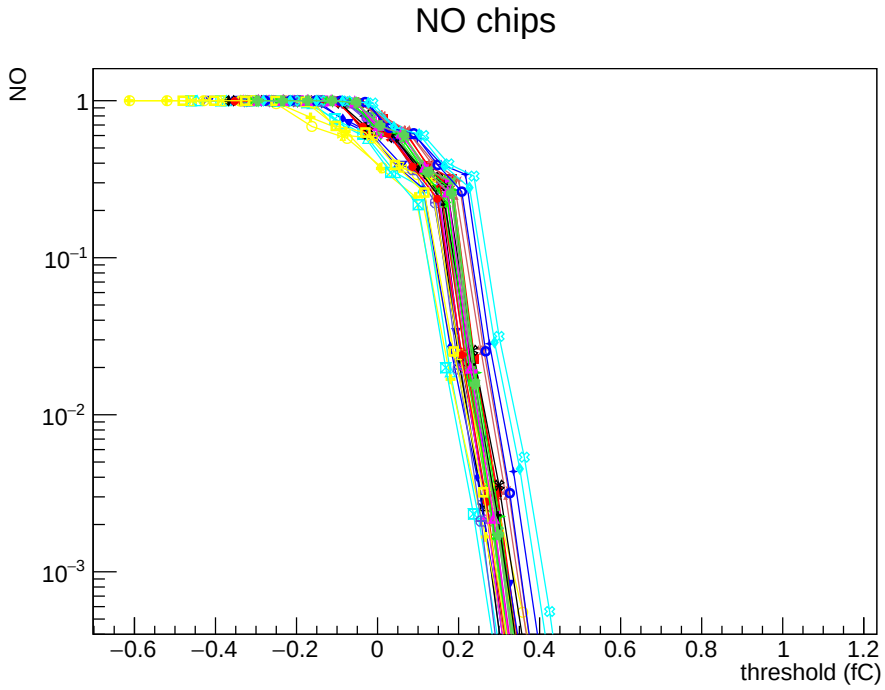
tracks with tracking information from Mimosa planes and timing cuts based on FEI4. The reconstruction uses a broken line fit, which allows for a single large scatter on one plane.

3.2 Pedestal

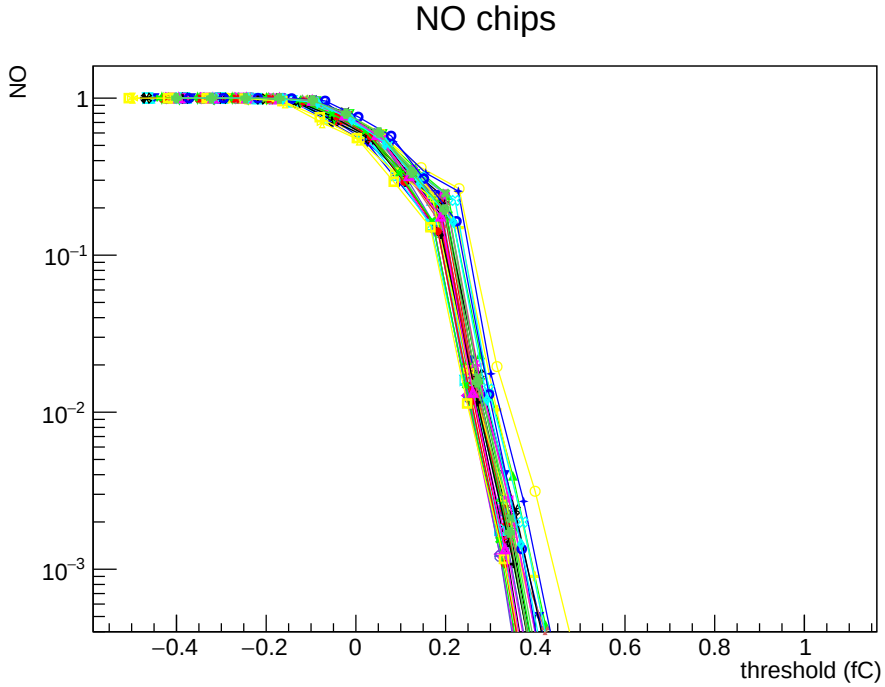
Pedestal data, taken with beam off, represents the level of noise when there is no charge input from sensors. Two sets of data, one taken at -30 °C and the other at 30 °C, were taken from the Sept. 2019 test beam campaign. The threshold region scanned is 0 to 40 in DAC settings, corresponding to around -0.6 to 0.4 in fC in this case. The negative charges are an artifact, coming from the RC calibration. The part of interest is the falling curve of the S curve instead of the plateau so the negative charge does not affect the final results. This measures the overall noise charge from the sensors along with the electric noise inside the circuit. The sources of noise are discussed in Chapter 1. The occupancy where only noise is present vs the threshold is the noise occupancy (NO) relation.

For each channel, an S curve is made. As mentioned for the ABCStar chips, channels are grouped into half-chip groups with 128 channels each, corresponding to the 128 strips on each row of the sensor. Since this is a SS module, there are four rows of strips and two hybrids with 10 chips each on this module. In total, there are 40 half-chip groups with 128 channels each. The average effect for all 128 channels on a half-chip describes the performance of the half-chip. The occupancy versus threshold relations per half-chip at -30 °C are shown in Fig. 3.4a and the same relations at 30 °C are in Fig. 3.4b. Comparing the -30 and 30 °C instances, we can see that the equivalent noise charge coming from the sensor and electronics, implied with the width of the S curve, increases as the temperature goes up. As discussed in Chapter 1, some sources of noise are dependent on temperature and are expected to increase as the temperature is higher. Differentiation of the S-curves gives the Gaussian noise profile as shown in Fig. 1.11. The observation of lower electric noise at lower temperature can be seen in Fig. 3.4. It also agrees with the theoretical calculations for the front-end predictions as will be further demonstrated later.

As the S curve is proportional to a complementary error function as in Euq. 1.9, the relation



(a) Noise Occupancy (NO) with beam off at -30 °C. The threshold is measured in fC.



(b) Noise Occupancy (NO) with beam off at 30 °C. The threshold is measured in fC.

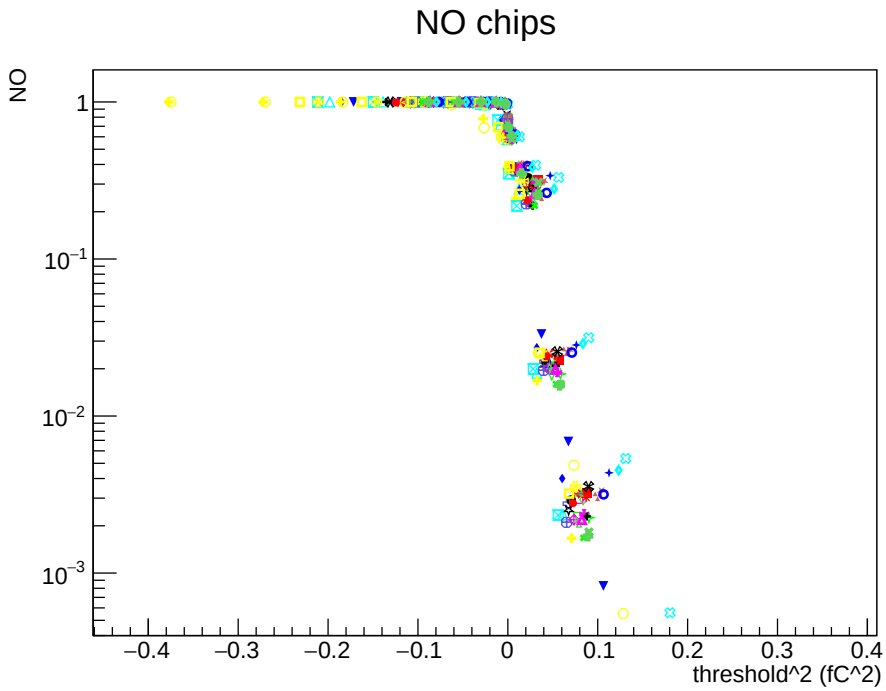
Figure 3.4: Pedestal noise occupancy vs threshold (fC), cold and warm. Each line represents a half-chip

between the occupancy and the threshold^2 is supposed to be linear in the falling part, which can be seen from Fig. 3.5. The occupancy-threshold^2 relation is linear for all half-chips at both cold and warm temperatures.

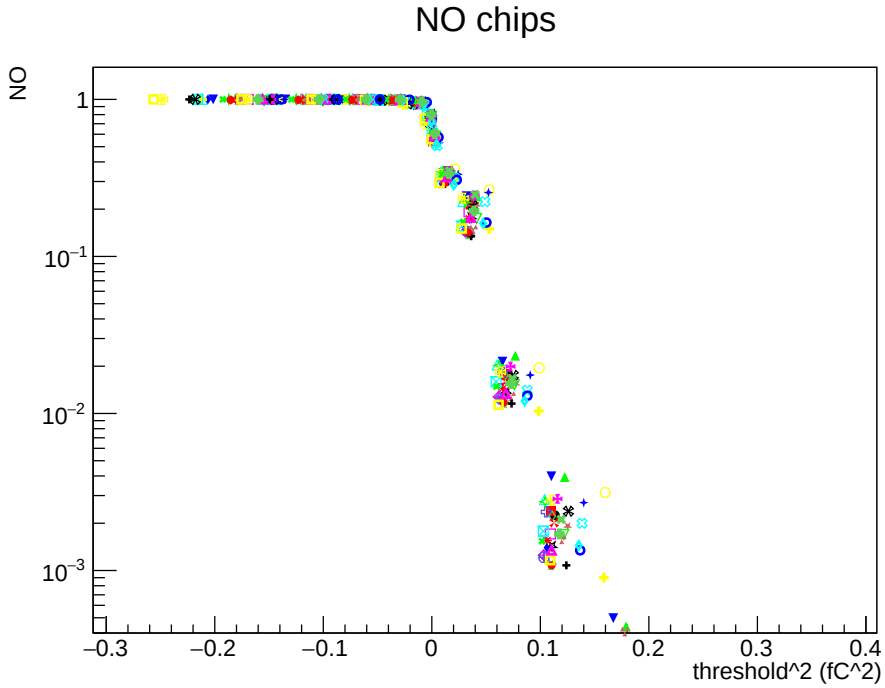
For each channel, their respective S curves are fitted with a complementary error function as described in Equ. 1.9 and their respective VT50 and sigma values are obtained. The sigma values from these S curves are $\sqrt{2}$ times of the width of the Gaussian distribution, which correspond to the electrical noise levels in these channels. The distributions of the sigmas from the Gaussian distribution for each channel at -30 °C and 30 °C are shown in Fig. 3.6, with the cold instance being the blue one and the warm one being the red one. The mean values for these histograms can be used as an indication of the noise level, which is 0.0957 fC at -30 °C and 0.1099 fC at 30 °C. These correspond to 597 e^- and 686 e^- respectively. For the both curves, there are larger tails so one way to get a better estimate of the actual input noise peak would be to fit the distributions with a Gaussian fit and get the Gaussian mean (the fit functions as shown in Fig. 3.7), which is 0.09098 fC and 568 e^- for cold and 0.1079 fC and 674 e^- for warm. The truncated mean is defined as the mean value of the charges falling within the Gaussian fit range (0.065 - 0.11 fC for the cold instance and 0.085 - 0.13 fC for the warm instance). It can be calculated as well, which is 0.09043 fC (564 e^-) at -30 °C and 0.1072 fC (669 e^-) at 30 °C.

Another data set used to determine the input noise is taken at 0.2 fC charge injection into the chip front-end. The output noise is read out then divided by the measured gain to obtain the input noise. Since 0.2 fC is the lowest charge injection possible, the resulting input noise should be comparable with the no charge injection instance. The results measured in e^- is shown in Fig. 3.8. The mean input noise is 0.0859 fC while cold and 0.1097 fC while warm, corresponding to 536 e^- and 685 e^- respectively. Similarly the peaks of the distributions can be fitted with a Gaussian function similar to Fig. 3.7, resulting in a Gaussian mean of 0.0859 fC (536 e^-) at -30 °C and 0.1097 fC (685 e^-). The truncated mean within the fit range are 0.0859 fC (536 e^-) and 0.1086 fC (678 e^-).

As there is a considerable amount of difference between the noise levels acquired with the two data sets, an average of all six measurements is taken as the "final" noise level. The six



(a) The relation between occupancy and threshold^2 at -30 °C.



(b) The relation between occupancy and threshold^2 at 30 °C.

Figure 3.5: The relation between occupancy and threshold^2 at cold and warm.

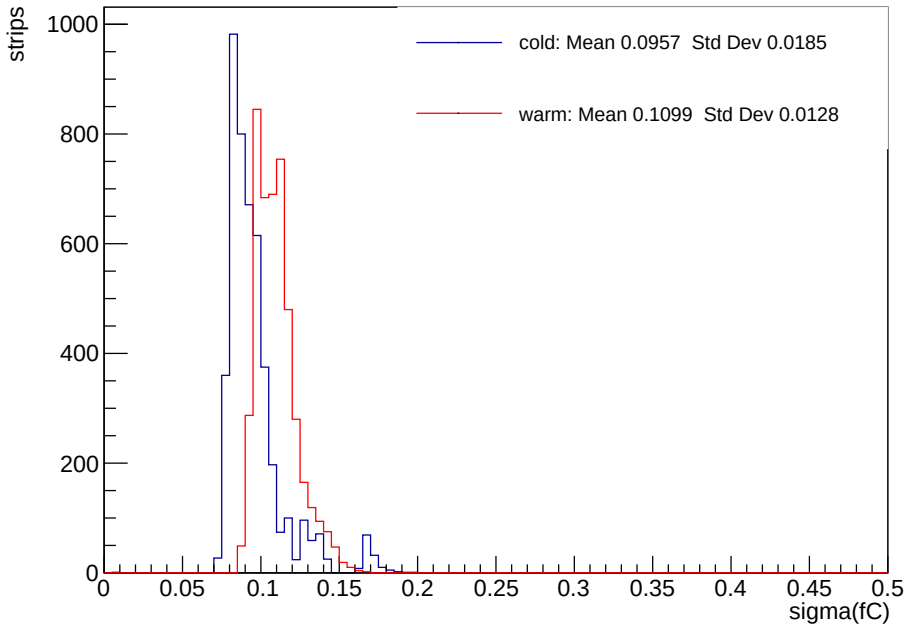
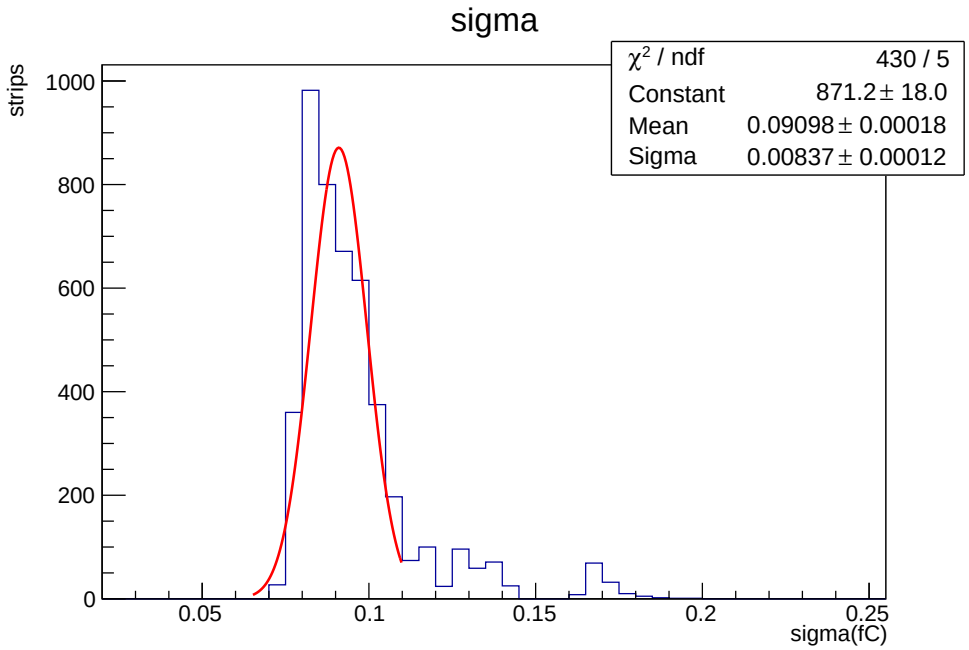


Figure 3.6: S curve sigma distributions with beam off at -30 °C (cold) as the blue line and 30 °C (warm) as the red line. The sigmas are from the S curve of each individual channels on this module. The sigmas correspond to the electrical noise level in the system.

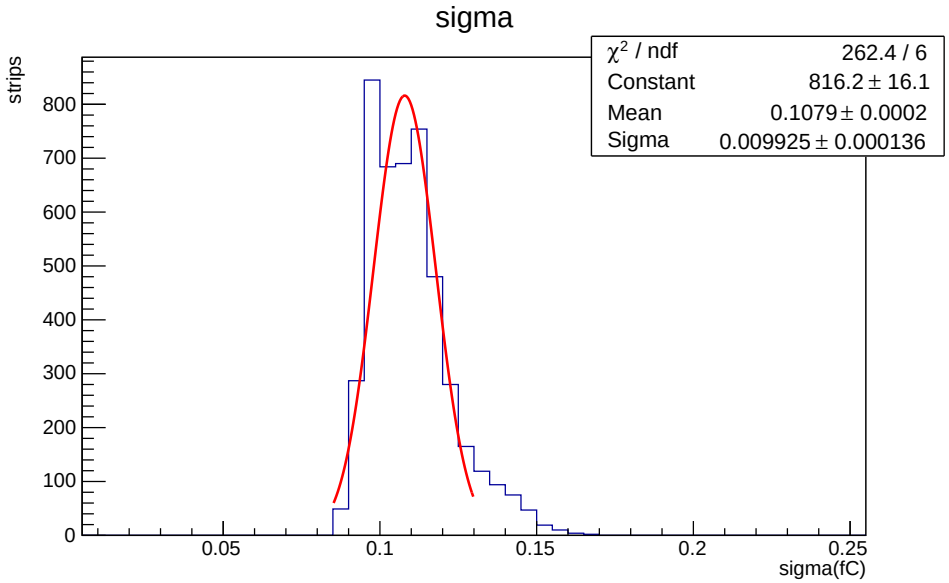
estimators are given in Table 3.1.

The systematic error is the difference between the measurements and the average outcome. The statistical error is much smaller than the systematic one, which is 1.6 e^- at -30 °C and 1.1 e^- at 30 °C. The average noise over all estimates for both data sets at -30 °C is 556 ± 25 e^-, while the average noise at $+30$ °C is 679 ± 7 e^-.

As discussed in Sec. 1.2 and expressed in Equ. 1.6, the noise level is expected to be higher in higher temperatures, which agrees with the average noise at 30 °C being higher than the -30 °C one by 22.4 % ± 5.7 %, which is the average of the six ratios obtained in these two ways. This is qualitatively larger than previous studies, where the noise level increases by about 13 % over -40 to 20 °C [43], [22]. The comparison is qualitative as the noise increase with temperature is not expected to be linear. The circuit model simulation [44] gives 17 % change in noise over -30 °C to 30 °C temperature change. The measurement is compatible with the simulation within errors.



(a) Gaussian fit of the distribution of fitted sigma values at -30 °C in Fig. 3.6



(b) Gaussian fit of the distribution of fitted sigma values at 30 °C in Fig. 3.6

Figure 3.7: Gaussian fit of pedestal noise occupancy vs threshold (fC) distributions, cold and warm.

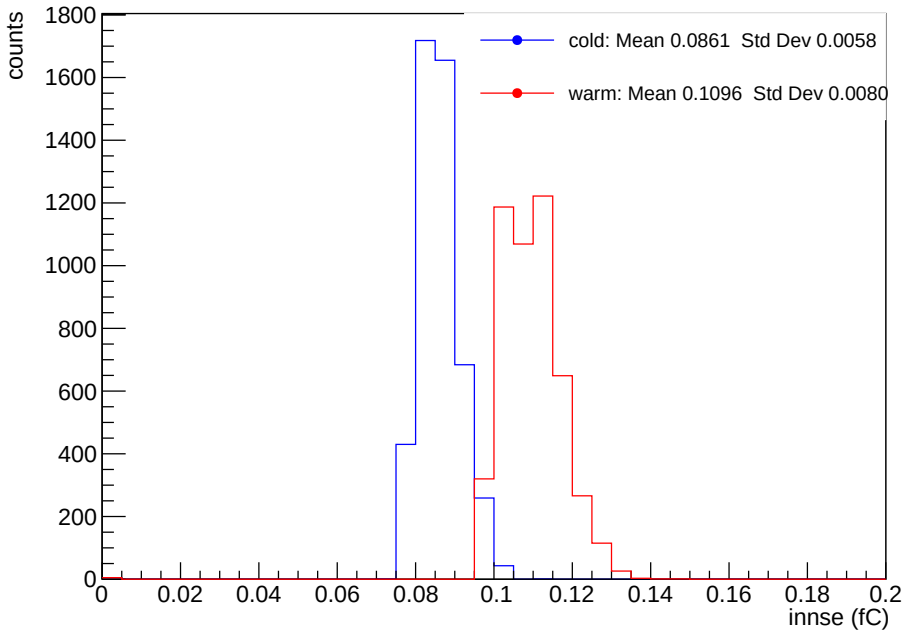


Figure 3.8: The input noise measurements obtained during the RC calibration procedure. The blue line stands for the cold distribution and the red line stands for the warm one.

	0 fC			0.2 fC		
	cold	warm	ratio	cold	warm	ratio
raw mean (ENC)	598	686	1.147	536	685	1.28
Gauss fit (ENC)	568	674	1.187	536	684.6	1.278
truncated mean (ENC)	564	669	1.186	535.8	678.1	1.266

Table 3.1: The estimators obtained by three different approaches applied on datasets corresponding to 0 fC and 0.2 fC of the injected charge (in ENC), respectively. The ratio is the warm noise over cold noise. The two data sets for the warm operation agree better with each other than the two data sets for the cold operation. This is due to the calibration issues with the code operation described in the text.

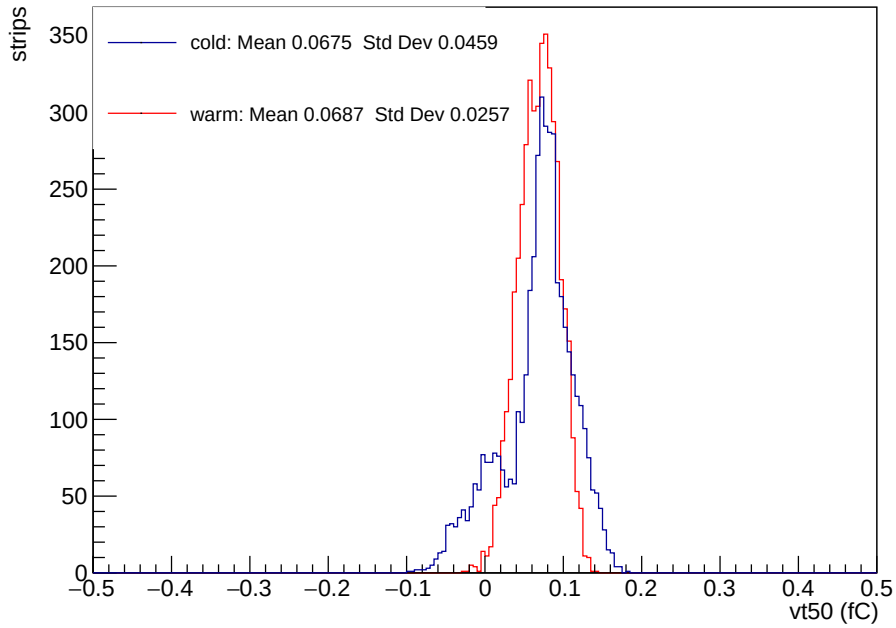


Figure 3.9: VT50 distributions with beam off at -30 °C (cold, blue) as the blue line and 30 °C (warm, red) as the red line. The VT50s are from the S curve of each individual channels on this module.

The distribution of VT50s obtained from the S curves for each channel is shown in Fig. 3.9. The blue line in Fig. 3.9 stands for the -30 °C instance and the red line stands for the 30 °C one. Even when there is no charge injection from the sensor and the leakage current effect is negligible for the un-irradiated module, there is an offset coming from the chip front-end of each channel. This leads to the Gaussian mean not being 0 fC. The VT50 for each channel serves as a respective "offset" from 0 fC. The VT50s should have similar distributions in both cold and warm environments. However, the distribution in Fig. 3.9 does not agree with this. Even if the mean values are comparable, the cold VT50 seems to have a wider distribution and larger tail.

Fig. 3.9 also shows that the VT50 distributions seem to be asymmetric and have tails on the lower side. There could be caused by the threshold differences between individual channels or the calibration process, in which threshold is converted from DAC settings to voltage then to charge. When compared with the same plots measured in DAC, it is obvious that the tail is not present in the DAC VT50 distributions. Fig. 3.10 is the VT50 measured in DAC at

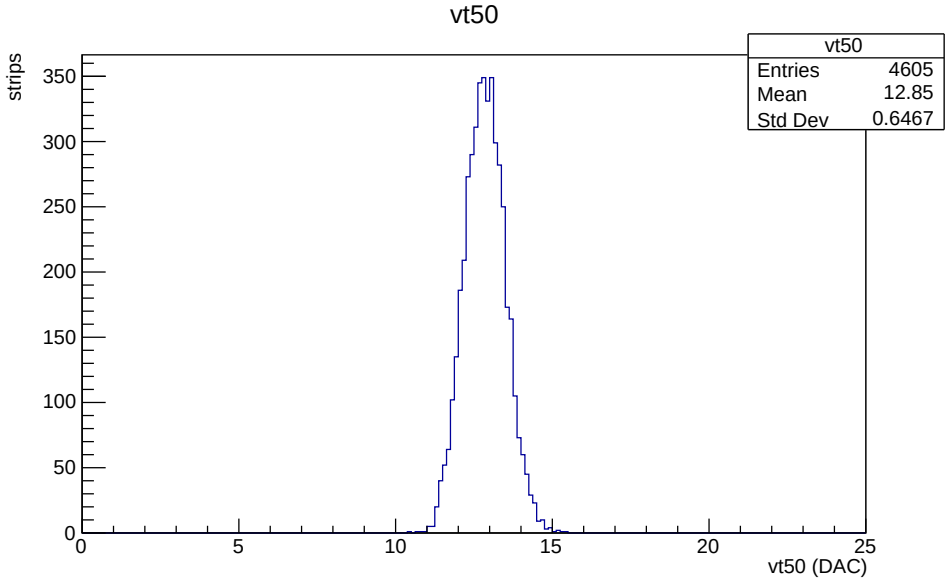


Figure 3.10: VT50 distribution at -30 °C measured in DAC.

-30 °C. This is the first indication that the calibration results for some chips are inaccurate.

Fig. 3.11 shows the relation between VT50 (measured in fC) and the channel number. Every 128 channels are grouped into one half-chip. Channel 0 to 1279 correspond to chip 0-9 stream 0 and channel 1280 to 2559 correspond to chip 0-9 stream 1. Streams correspond to different strip sections on the sensor. Similarly for chips on the second hybrid on the module, there are channel 2560 to 5119. In this way, the chips with inaccurate calibration can be identified in Fig. 3.11. Most of the channels have VT50 agreeing with each other, except for a few that have a very largely distributed VT50s. They are the chips that contribute to the tails in Fig. 3.9. There are two chips not turned on during the pedestal tests for unknown reasons during the test beam campaign. They can also be identified as the last two chips (chip 8 and 9) on the second hybrid in Fig. 3.11.

The mean values of the pedestal VT50 distributions correspond to the amplitude of background offsets at the two temperatures. They are the "baseline" of signals and are taken off from beam VT50 data to show the real signal charge collected.

If the chips with inaccurate calibration are used in the test beam, the charge measurements will be inaccurate as a result. Later sections will show this effect.

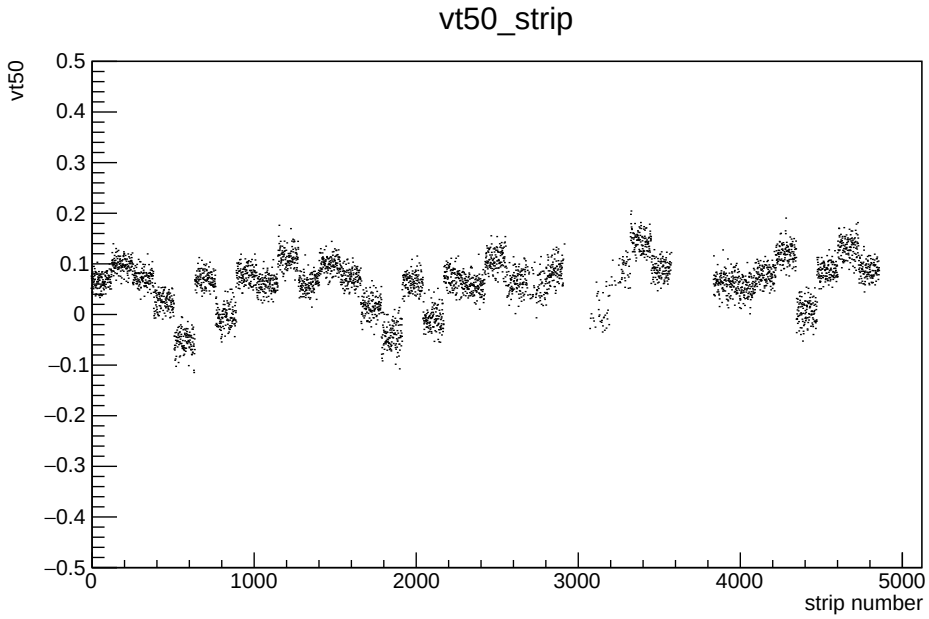


Figure 3.11: The relation between VT50 (fC) and channel number for pedestal data. Two chips are not turned on for this data taking. Most channels agree with each other and have a narrow VT50 distribution. However, VT50 distribution is obviously different for a few chips. The missing chips are not turned on during data taking.

3.3 Beam Data

The beam test for the cold versus warm studies is performed with an electron beam. Comparing the charge deposition in the sensors with theoretical predictions can ensure the module performance. The charge deposited on sensor strips should not be affected by the temperature so the signal induced by the charge should be unaffected as well. However, a lower noise level is expected when the temperature is low. Based on the position of the beam particle hitting the strip, the signal changes. If the particle passes the center of the sensor strip, it is more likely that the strip itself sees all the signal generated from the particle. But if the particle hits the edge of the strip, then the signal is likely to be shared with the adjacent strip or strips. Each strip will see a smaller signal.

To tell the position of the particle passing the module, the spatial resolution is of high importance. In the simplified situation when a particle gives a signal in one strip only, the spatial resolution for a strip with the width of X would be $\frac{X}{\sqrt{12}}$. In the case of the SS sensor

strips, the width is 75.5 μm, thus the ideal strip resolution is about 22 μm for a single hit event. The resolution can be better in case of two-hit events when signal sharing happens if the particle hits near the edge of a strip. With the signal sharing information, it is easier to localize where the hit happened. However, the particle track is calculated with the telescope system and the position of the particle passing through the module is predicted by the track in this study. Then the predicted track position is compared with the binary hit information from the strip to obtain the actual resolution. The effective resolution of the telescope is not negligible compared to the strip resolution of 22 μm. But if the resolution is good enough to ensure that the edge and center are at least one σ away from each other, there still can be some separation between the strip edge and the center.

When there is a larger signal on one strip, the probability that the signal on neighbouring strips to be over threshold as well is higher. When the threshold is lower, the same particle track is likely to trigger response from multiple strips as well. It is because when threshold is low enough, even the small signal that some neighbouring strips see can still pass the threshold. As mentioned in Sec. 2.1.1, "cluster" describes how many consecutive strips are "lit up" by a particle passing through. The cluster size is expected to decrease as threshold goes up. When the particle energy and the threshold is constant, if the particle passes near the edge of the strip, both the hit strip and the neighbouring strip are likely to see enough signal to be above the threshold. Then the cluster size will be slightly higher than the case when the particle passes the strip center. This can contribute to a better spatial resolution for two-hit events.

Timing is also an important factor. The signals on sensor strips come in the form of pulses as discussed in Chapter 1. In order to be picked up by the electronics at the pulse peak, timing delays are applied. The occupancy depends on where the delay falls on the pulse. If the timing window is not chosen correctly, the measurements are not representative of the actual signal size.

Two data sets are used in this study. The beam was focused on different parts of the module in these two sets. Data set 1 has the beam position on chip 4 of one hybrid while data set 2 beam position is on chip 5 of the other. They both consist of a threshold scan at -30 °C and

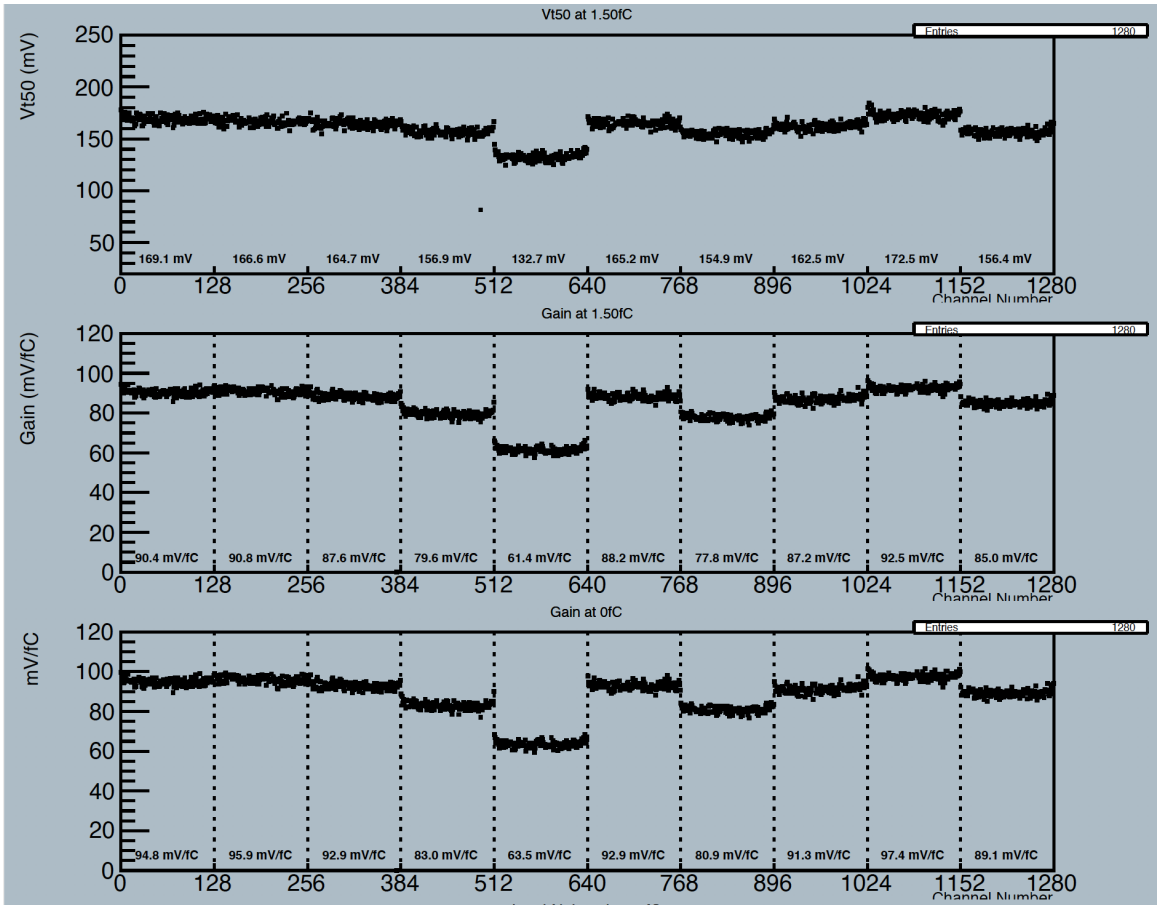


Figure 3.12: Calibration results for the module at -30 °C. VT50 (mV) at 1.5 fC, gain at 1.5 fC and 0 fC against channel number are shown as the top, middle and bottom plot. Top: VT50 vs channel number with charge injection of 1.5 fC; Middle: Gain vs channel number with charge injection of 1.5 fC; Bottom: Gain vs channel number with charge injection of 0 fC; Every 128 channels correspond to the same chip.

30 °C and the beam direction is perpendicular to the module.

3.3.1 Results From Data Set 1

In very early stage of the analysis, we realised that the calibration seems "off" for chip 4, which is where the beam is focused in this data set. This was first discussed in Sec. 3.2. As the cold calibration results in Fig. 3.12 shows, chip 4 (channel number 512-640) in the plot is obviously an anomaly in terms of gains and VT50s distributions compared to other chips. The warm calibration for chip 4 is also anomalous, but not as so severely as it is for the cold calibration.

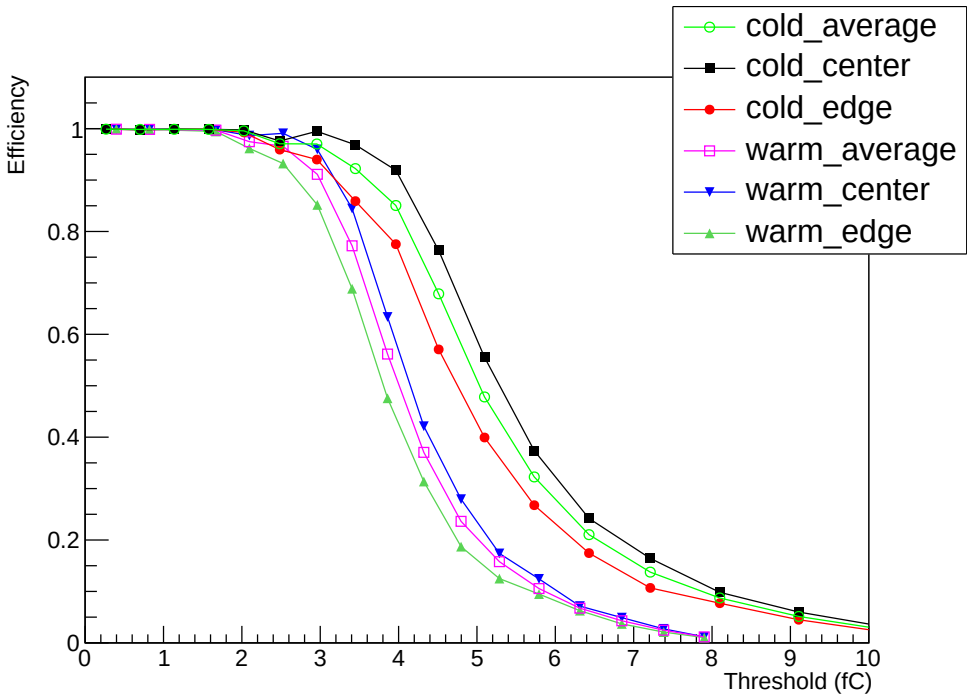


Figure 3.13: Cold vs warm comparisons with original chip 4 calibration.

When applying this calibration to the data, the outcome is largely distorted by the calibration inaccuracy, as can be seen in the X axis of Fig. 3.13. The VT50 obtained from cold and warm data should not be almost 2 fC apart. Combined with the calibration results in Fig. 3.12, it is indicated that the calibration for chip 4 is responsible for this situation.

In Fig. 3.13, the efficiency for each strip is defined as this:

1. A track predicted by the Telescope system passes through a strip A

2. Within ± 3 strips range from strip A, see if there is a strip fired as "hit" by the module

3. If there is a hit near the track, strip A is marked as efficient, otherwise, as inefficient.

This method is not perfect. For a dead strip, the efficiency of the strip can not go down to 0 as there is the possibility that the charge shared with some nearby strip will exceed its threshold and thus give the dead strip some efficiency. However, the most common case is the hit strip and the track strip is the same strip. A dead strip is defined as a strip that gives no response to an incoming particle through it. Dead strips will have obviously lower efficiency and can be easily identified. There is no indication that such a strip is present in this data set. But the

most obvious advantage of this definition is that if a strip is functioning, the efficiency can go to 1, which is more representative of the actual module or chip performance.

The "center" is defined as the 20 % region of the strip that is closest to the strip center. "Edge" is the 20 % furthest away from the center. When the strip center is defined as the 0 point, with the strip covering -0.5 to 0.5, within ± 0.1 would be the center and above 0.4 or below -0.4 would be the edge. "Average" describes the overall performance across the strip without separating the edge and the center. As a result, the "average" instance would have the highest statistics of all, about five times more than "edge" or "center". It is the most representative for the performance of the chip. For each strip within the beam region, an S curve is made and weighted by the number of events passing that strip. The weighted mean outcome is shown in Fig. 3.13, which represents the performance of the chip. Focusing on the average curves in the plot, the VT50 point, which corresponds to the signal, is about 4 fC at 30 °C and almost 5 fC at -30 °. It is not expected for sensors to have such a large difference in signal between warm and cold temperature. Combined with Fig. 3.11, it is safe to say that chip 4 calibration was inaccurate and can not be used in this study. The distribution differences between cold and warm visible in Fig. 3.13 are not physically real.

To bypass this problem, we first tried to reproduce calibration results at Rutherford Appleton Laboratory (RAL) where the module currently resides. However, the module was damaged by accident before the re-calibration setup could be cooled down to -30 °C, which is the original calibration temperature during the test beam. Thus, the attempt to re-calibrate in the same environment was blocked. But the calibration results at a higher temperature of -4.5 °C were obtained before the incident. Fig. 3.14 shows that when the calibration procedure is performed properly, chip 4 is not obviously different from other chips. Therefore, it could be sensible to assume chip 4 would have a similar calibration performance as the first three chips if nothing goes wrong. In this case, it would be acceptable to use the chip 1 calibration parameters to replace the chip 4 calibration parameters, which is the approach chosen eventually.

After replacing chip 4 calibration parameters with chip 1 calibration parameters, Fig. 3.13 was reproduced as Fig. 3.15. In Fig. 3.15, the VT50s for the cold and warm instances

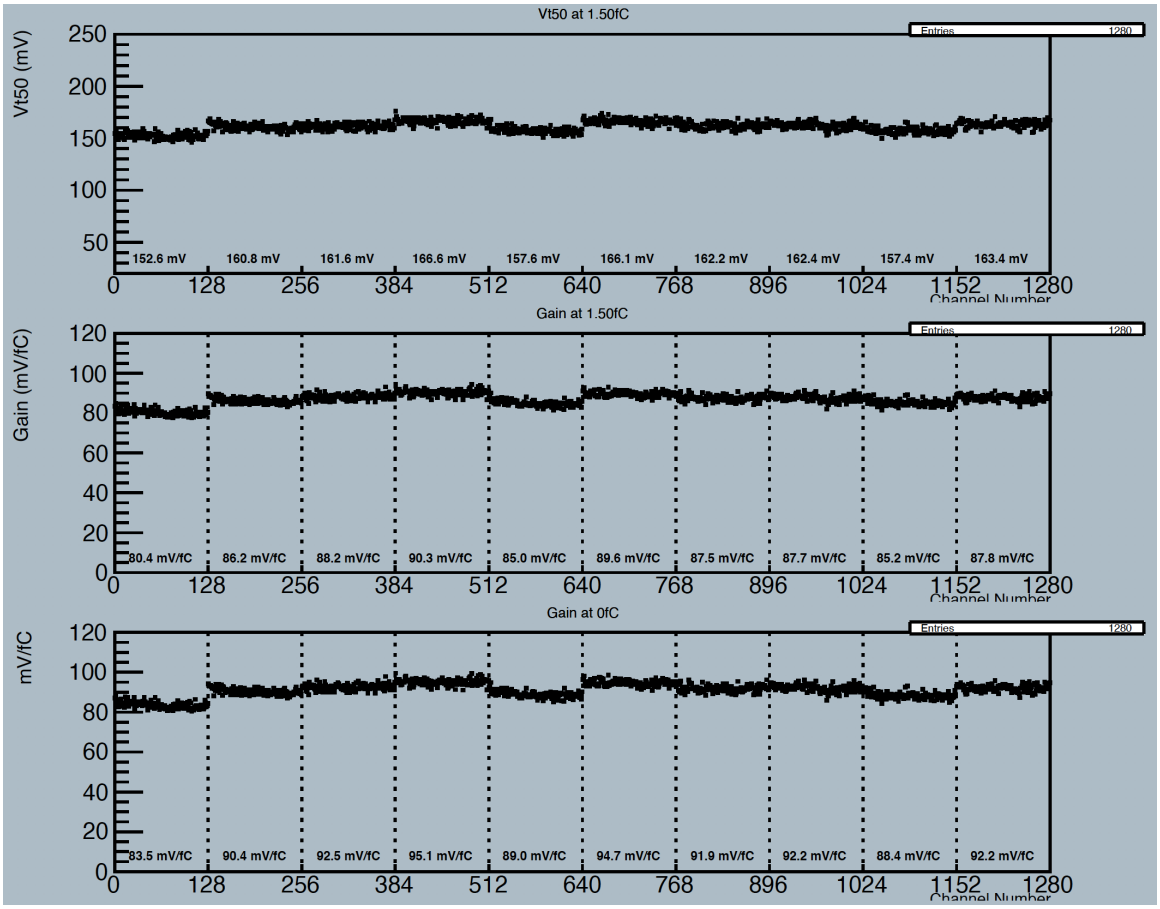


Figure 3.14: Calibration results for the module at -4.5 °C during a re-calibration process at RAL. VT50 (mV) at 1.5 fC, gain at 1.5 fC and 0 fC against channel number are shown. Top: VT50 (mV) vs channel number with charge injection of 1.5 fC; Middle: Gain vs channel number with charge injection of 1.5 fC; Bottom: Gain vs channel number with charge injection of 0 fC; Every 128 channels correspond to the same chip. In this calibration, chip 4 behaves very similarly as other chips.

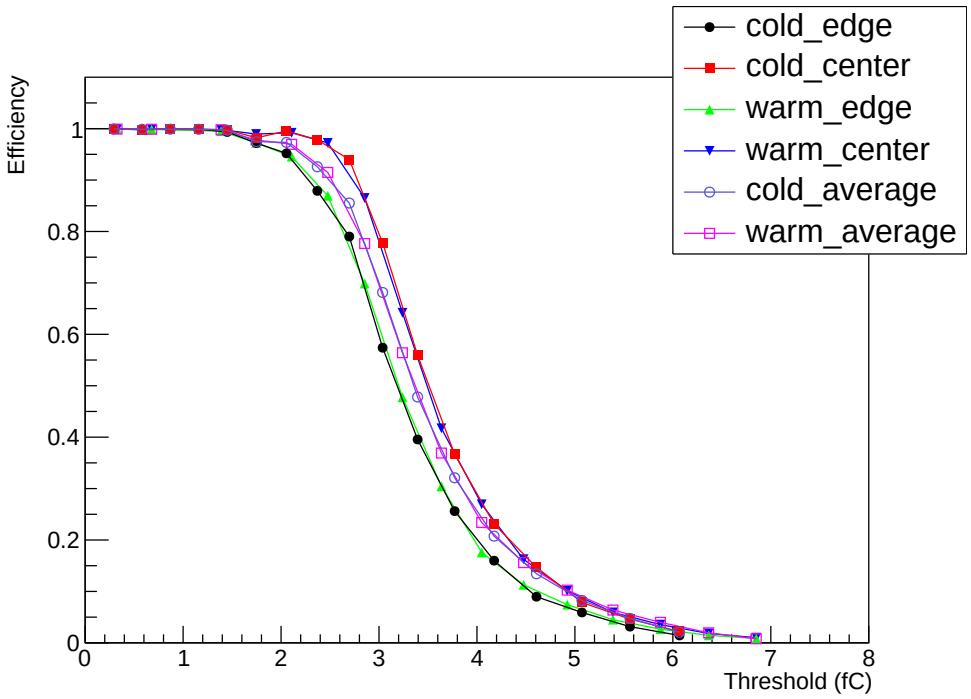


Figure 3.15: Cold vs warm comparisons with chip 1 calibration.

are much closer to each other. This agrees with the prediction that the temperature does not change the signal collected by sensors. The "edge" curve begins falling the earliest in threshold and at the same threshold it has the lowest efficiency. This is due to signal sharing between strips. The "center" one, on the contrary, falls the latest with threshold increase and has the highest efficiency at a given threshold because almost all signal is contained within the same strip. The "average" one falls in the middle.

From this point on, chip 4 calibration parameters are replaced with chip 1 ones for all charge calibration.

In the case of beam data, the S curves for each strip within the beam region is fitted with an empirical skewed complementary error function, as Equ. 3.1. [45] The signal shape is approximately Landau and the noise distribution is Gaussian. The differentiation of this S curve is the convolution of the Landau and the Gaussian.

$$f(x) = E_0 \cdot \mathrm{erfc}(\alpha \cdot (1 + 0.6 \cdot \frac{e^{-A\alpha} - e^{A\alpha}}{e^{-A\alpha} + e^{A\alpha}})), \quad \alpha = \frac{x - x_0}{\sqrt{2}\sigma} \tag{3.1}$$

in which,

E_0 means maximum efficiency, is 1 or very close to 1 in our case,

x_0 means median charge (50 % efficiency), the VT50 point,

σ means width of the distribution, correspond to noise in this case,

A is the skewed parameter.

Each channel has a VT50 value (x_0 in Equ. 3.1) from the fit. All the VT50s combined could show the charge deposition distribution. As mentioned before, the mean value of the VT50 distribution at pedestal should be subtracted as an offset. The VT50 distribution at -30 °C is shown as black in Fig. 3.16 and VT50 at 30 °C as red in Fig. 3.16. They both had their representative pedestal VT50 taken out. The plot shows that the VT50s in cold and warm instances are quite close. The cold VT50 is 3.3464 $\pm$ 0.0721 fC and the warm one is 3.3436 $\pm$ 0.1598 fC. The errors quoted are purely statistical and are uncorrelated. The error of the mean is 0.0065 fC for the cold distribution and 0.0138 fC for the warm distribution. The systematic errors are correlated between the cold and warm instances. The systematic errors are discussed in more detail in Sec. 3.4. The VT50s are quite close to one another, which is expected as the temperature has little effect on charge deposition in sensors.

From the Equ. 3.1 fit on each strip, they each has a different set of fit parameters. An "expected" S curve is made from Equ. 3.1 with these parameters. Then from 0 to 9 fC, the region is separated into 1800 steps. The differentiation of the expected S curve, which is the Landau-Gaussian convolution, can be calculated numerically through these steps. The differentiation is described with 1800 points of x_i and y', which definition is Equ. 3.2.

$$y' = \frac{y_i - y_{i+1}}{x_{i+1} - x_i} \tag{3.2}$$

The most probable values (MPVs) of the differentiation for each strips can be found as the maximum value of the 1800 y′s. Fig. 3.17 shows the distribution of the MPVs in cold and warm conditions. The black line in Fig. 3.17 is for the cold case and the red one in Fig. 3.17 is for the warm case. The MPVs are very close in both cases. The numerical approach was

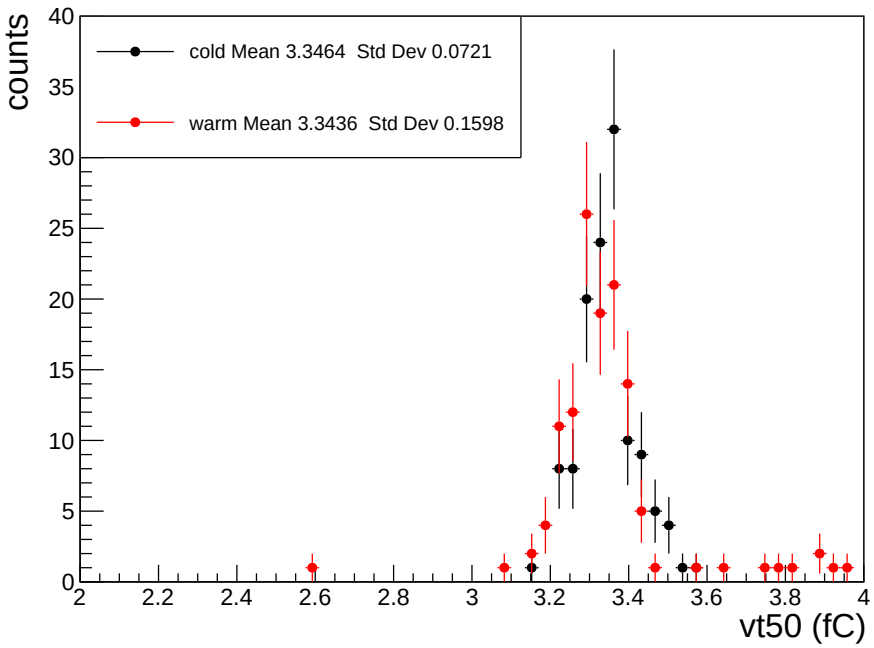


Figure 3.16: VT50 (fC) distributions with beam on at -30 °C (black) and 30 °C (red). The VT50s are from the S curve of each individual channels within the beam region.

chosen as a simpler way to achieve the required precision. The statistics come from the number of strips in the beam region, which are the same statistics in Fig. 3.16.

The MPV is the more accurate description of the signal in this case. The signal induced by charged particles in the sensor follows a Landau distribution. The signal is skewed by the Gaussian electrical noise. The outcome is not Gaussian or symmetric because of the Landau part. The MPVs can describe the Landau part better than the VT50, which is a more symmetric description. As can be seen in Equ. 3.1, it correspond to the MPV of the Landau distribution. The VT50 value is the median value, which would be slightly higher than the MPV. The MPV mean values at cold and warm are quite close, agreeing with the signal being consistent. The mean value for the cold distribution is 3.1930 fC with standard deviation of 0.0764 fC. The mean value for the warm distribution is 3.1819 fC with standard deviation of 0.1612 fC. The error of the mean is 0.0069 fC for the cold distribution and 0.0139 fC for the warm distribution. The measured mean MPV values are around 3.2 fC for this data set. The systematic errors will be discussed in the later sections.

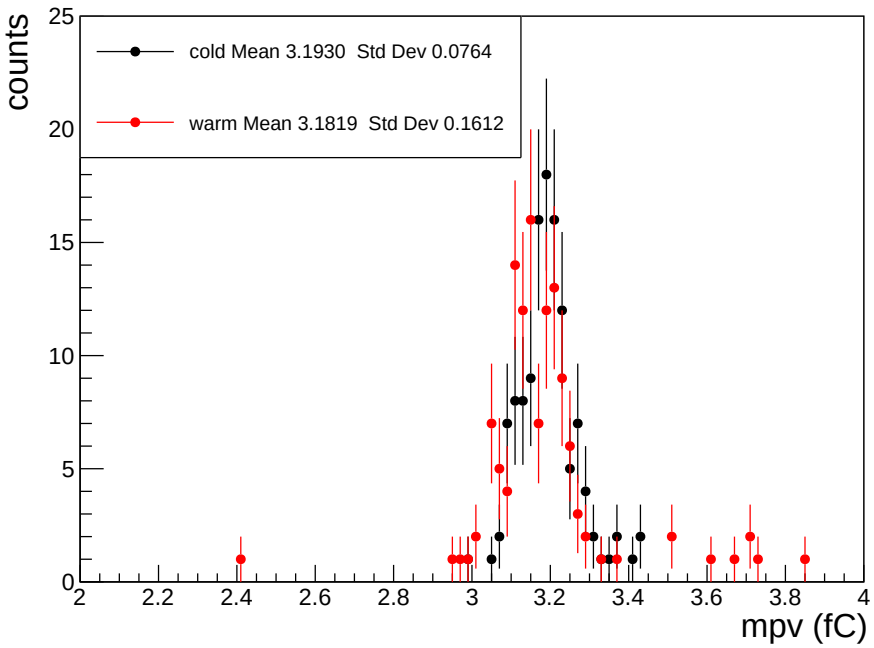


Figure 3.17: Most Probable Value (MPV) distributions, cold (black) and warm (red).

Cluster sizes at -30 and 30 °C are also studied. As shown in Fig. 3.18, cluster sizes are larger at low threshold and lower at high threshold. The black line in Fig. 3.18 is for the cold instance and the red line in Fig. 3.18 is for the warm instance. As discussed before, even though the beam energy is the same, when threshold is lower, it is more likely for signal induced on neighbouring strips to be higher than threshold. When the threshold is high, it is only likely for the strip with the hit to have signal over threshold. The uncertainty on the Y axis comes from the number of events with a certain cluster size. When the threshold is high, there are fewer events over threshold, resulting in a larger uncertainty. As mentioned before, the cluster size can be used to improve spatial resolution. Cluster sizes tend to be larger when the particle track passes the sensor edge instead of the center. An example of this effect is shown in Fig. 3.19 at the threshold of 40 in DAC, which is an intermediate threshold.

As mentioned in previous sections, timing is also an important factor in efficiency related studies. A TDC (time to digital converter) was used to measure the time delay between the rising edge of a BC clock and the particle trigger. 16 counts in delay correspond to 25 ns.

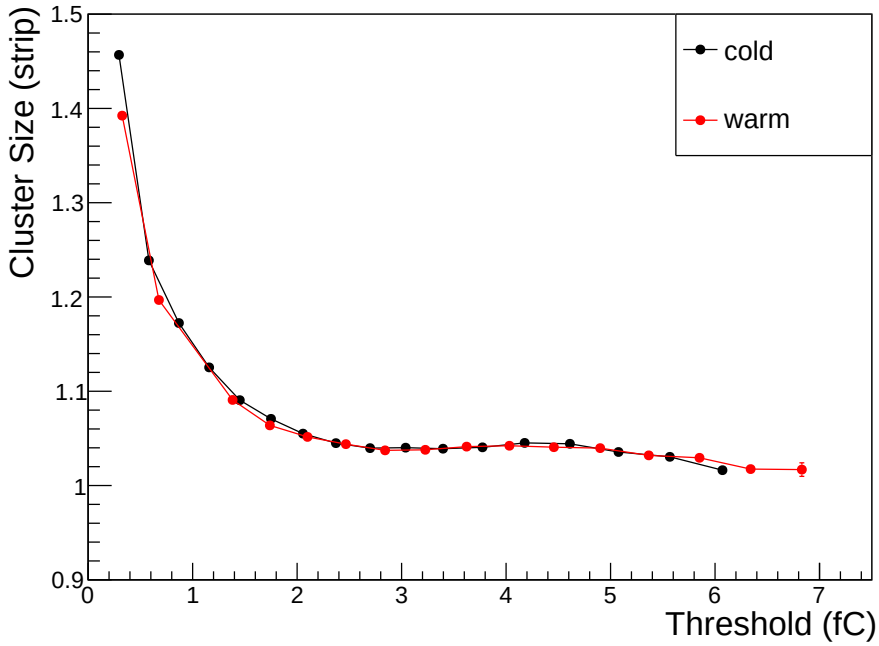


Figure 3.18: The cluster sizes at -30 °C as black and at 30 °C as red. The cluster size can not go below 1.

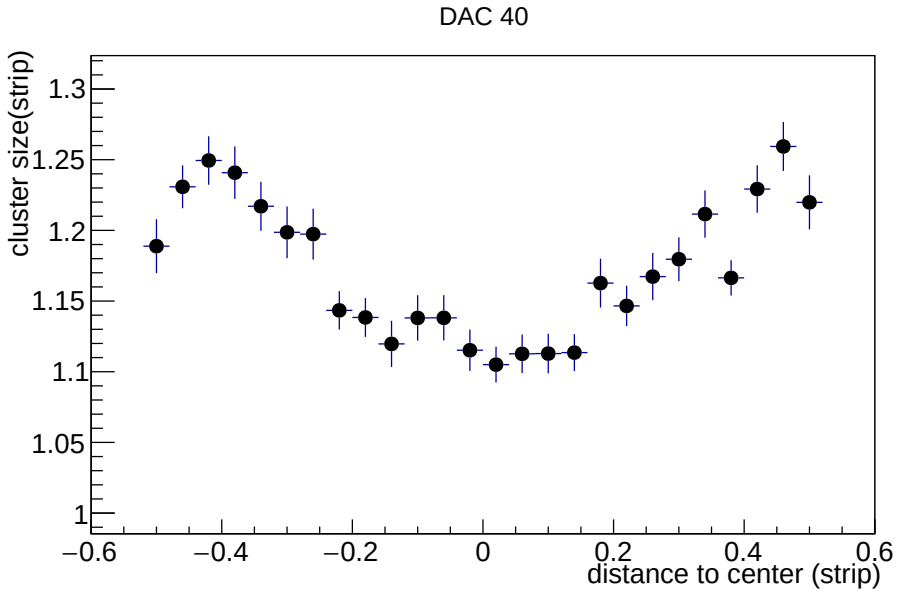


Figure 3.19: The relation between cluster size and the position where the particle passes through a strip. This test was performed at a threshold DAC setting of 40, which corresponds to a charge of 0.87 fC. The strip width is -0.5 to 0.5 with 0 point being the strip center.

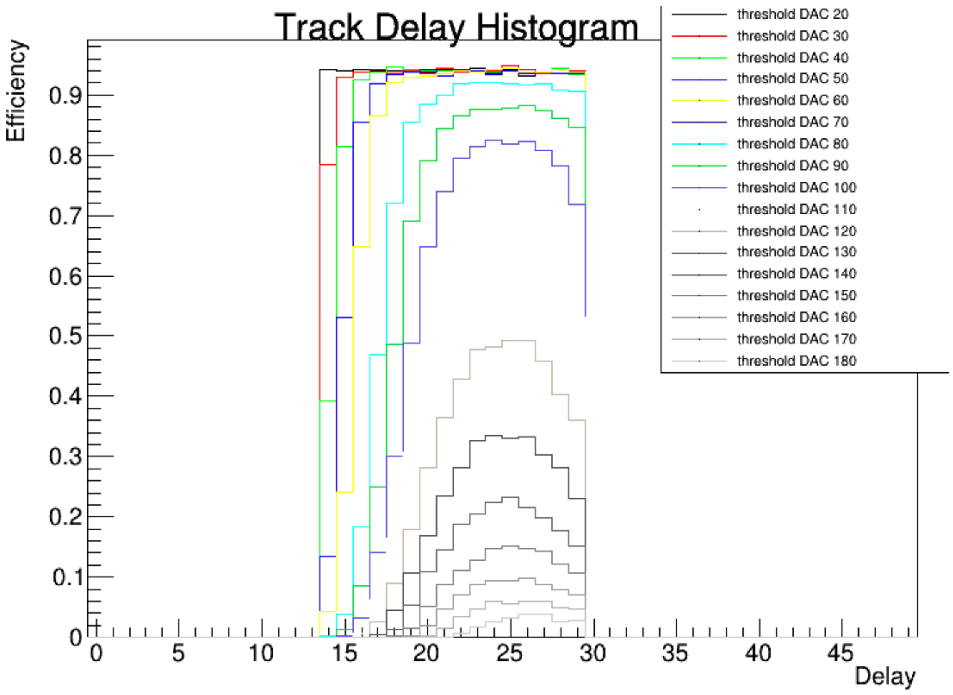


Figure 3.20: Relation between delay and efficiency at various thresholds. Thresholds are in DAC counts.

As shown in Fig. 3.20, even at the same threshold, the efficiency has a dependency on delay. The delay window for pulse selection here is chosen to be 21 to 28 in delay for this data set. The same delay window is applied for both warm and cold instances. For this test, only one bunch crossing (BC) of 25 ns is studied. For other tests, three BCs are covered.

At each delay point, the relation between efficiency and threshold (fC) can also be plotted as an S curve and a VT50 value can be obtained at each delay by fitting the curves. The relation between the delay setting and the VT50 at that delay is plotted as the pulse shape distribution and will be discussed in Sec. 3.5.

3.3.2 Results From Data Set 2

Apart from the previous data set, another pair of cold and warm data is available with beam on another chip, which does not have issues with the calibration. However, for the warm scan in this data set, there are a few runs that are recorded without information from the timing plane. Those data points are not recoverable for analysis. The threshold points that

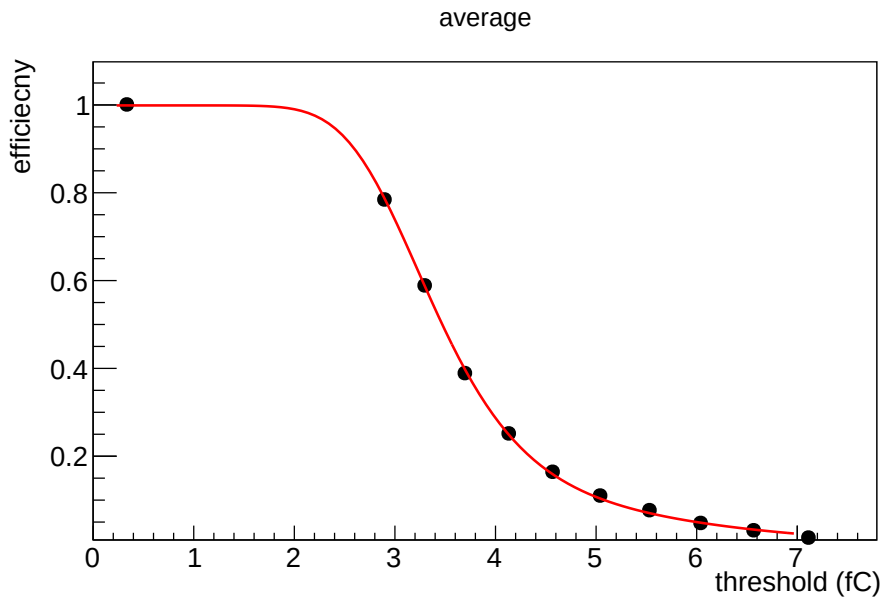


Figure 3.21: The S curve for the module with the warm scan of data set 2. The scan of this data is missing 5 points, but still possible to fit.

are influenced are 50 to 80 in DAC. The most obvious effect is that the warm S curve is missing 4 points, causing uncertainties when fitting the curves. But the general tendency of the curve is still possible to fit with Equ. 3.1, as shown in Fig. 3.21.

Another issue with this data set is the spatial resolution coming from alignment. As mentioned before, when the spatial resolution is too coarse, there is no separation between the edge and the center of a strip. The "residual" is defined as the difference between the predicted track from the telescope system and the hit position from the actual module. It is expected to center around 0 and in the ideal case to have a width of 22 μm. The actual residual distribution for a run in this data set is shown in Fig. 3.22, which has a RMS of about 40 μm. For data set 1, the RMS of the residual distribution is about 26 μm. This is caused by issues with aligning the telescope and the DUT. With the strip width being 75.5 μm, the edge and the center of the strip lie within one σ with each other according to Fig. 3.22. This means that it is not possible to tell apart the center and the edge of a strip. However, the importance of this data set is to have a charge deposition reconstruction with the correct chip calibration. As in data set 1 analysis, chip 1 calibration replaced the original chip 4 calibration. The results from data set 1 can be justified by comparing the outcomes

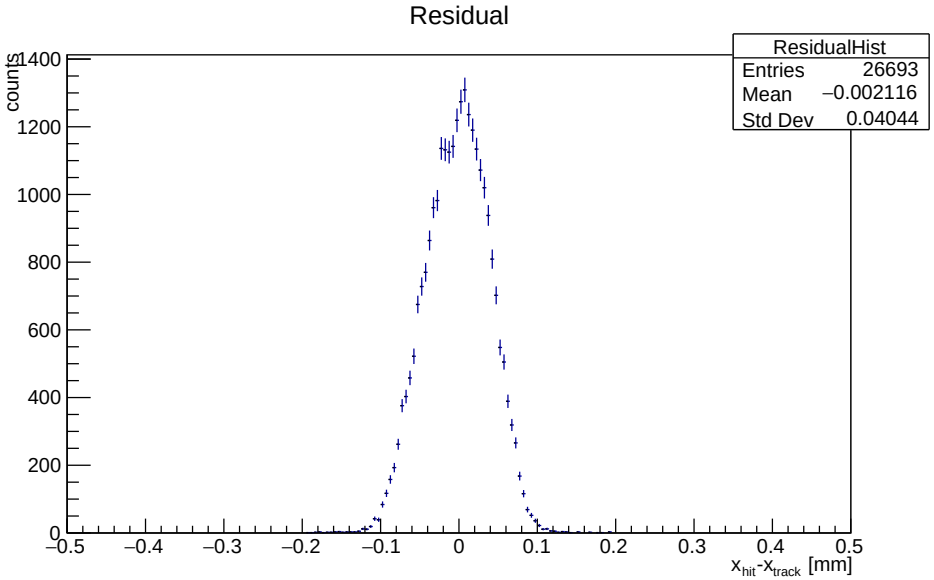


Figure 3.22: Example residual (x_{hit} - x_{track}) distribution. The resolution is about 40 μm.

from data set 1 and data set 2.

For this data, the same plots are made as for data set 1. Fig. 3.23 is the comparison between S curves from cold and warm instances. It agrees with Fig. 3.16. The signal magnitudes in the cold and warm instances are similar and the VT50s here are also similar with Fig. 3.16. This suggests that it is sensible to use chip 1 calibration parameters instead for data set 1.

For all strips in the beam region, their respective S curves are constructed and fitted. From each S curve, a VT50 value can be obtained. The distribution of the VT50 values are shown in Fig. 3.24 , with the black one for the cold instance and red one for the warm one. However, as mentioned before, the warm S curves are missing the falling edge, which will cause inaccuracies in the fit.

From the Equ. 3.1 fit on each strip, each of them has a different set of fit parameters. Similar to before, the differentiation is calculated with Equ. 3.2. The maximum value is the most probable value (MPV). The distributions of the MPV in the cold and warm environments are shown in Fig. 3.25. The mean values of the VT50 distributions are quite close to those in Fig. 3.17 for data set 1. The measured MPV while cold with statistical error is 3.177 $\pm$ 9.7 $\times 10^{-3}$ fC and the MPV with statistical error while warm is 3.23 $\pm$ 6.8 $\times 10^{-3}$ fC. The

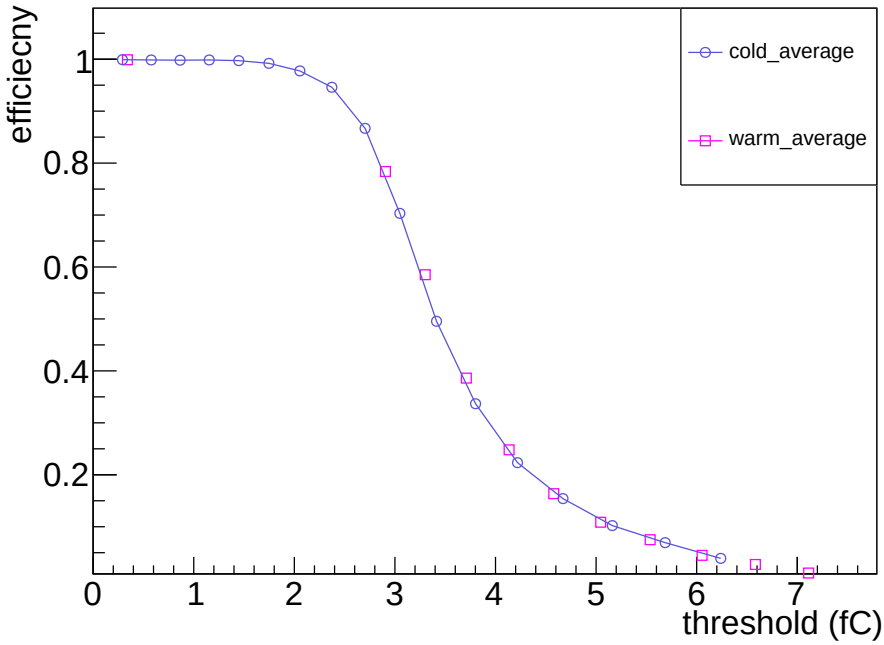


Figure 3.23: The efficiency-threshold relation comparison between cold (purple) and warm (pink) for data set 2.

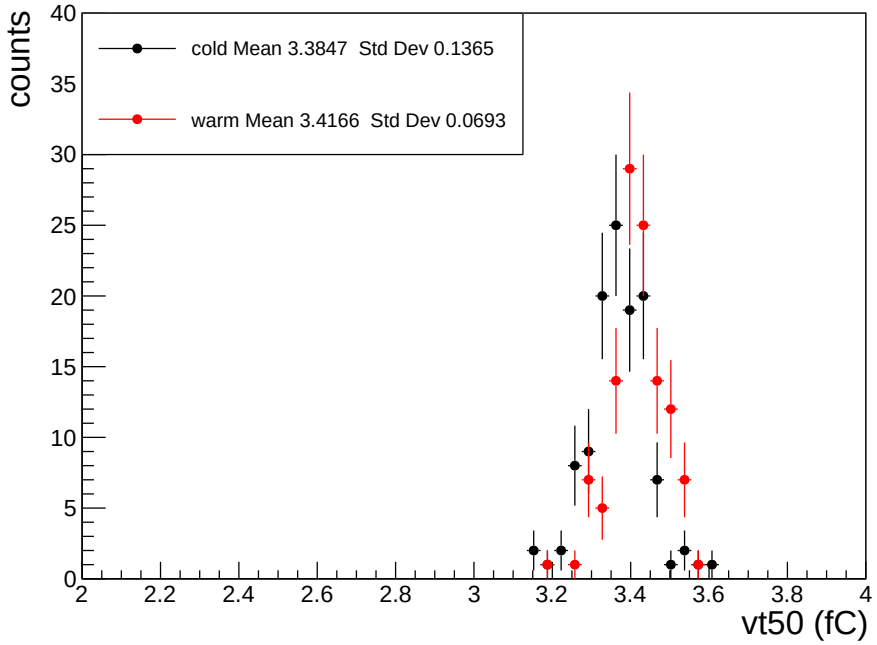


Figure 3.24: The VT50 (fC) distribution at -30 °C (black) and 30 °C (red) for data set 2.

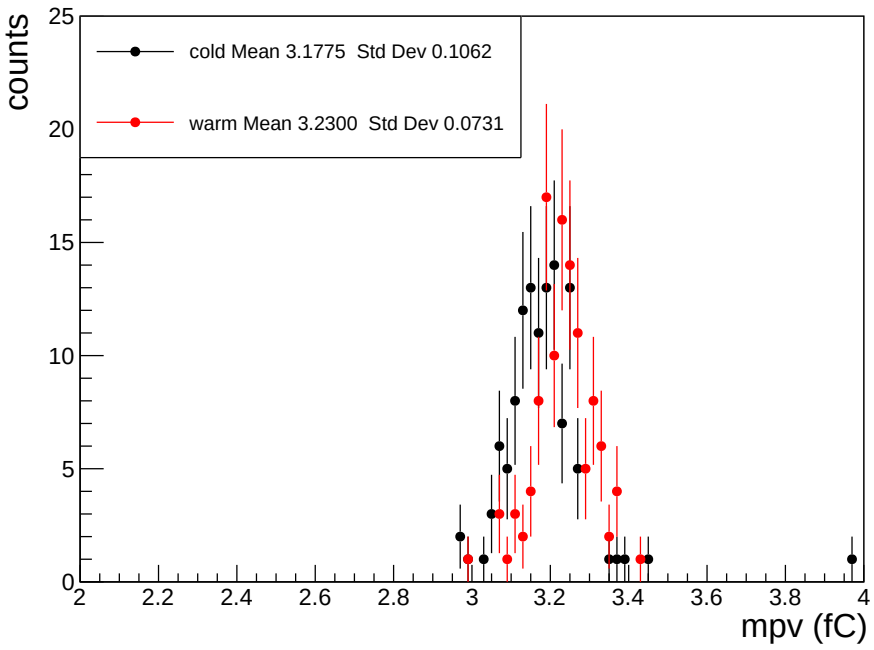


Figure 3.25: The MPV distribution at -30 °C (black) and 30 °C (red) for data set 2.

systematic errors will be considered in the later sections.

The cluster sizes in this data set is shown in Fig. 3.26. The performance agrees with the previous data set. The cluster sizes are larger when the threshold is low and smaller when threshold is high. The cold instance is in black and warm one is in red. The warm one is missing the falling edge due to the missing data points mentioned before. The statistical uncertainties are negligible.

3.4 Systematic Error Studies

Apart from the statistical errors that can be seen in the previous sections, there are systematic errors introduced by the analysis methods that are used. In this section, the effect of several factors are discussed.

First, the fit function described in Equ. 3.1 has 0.6 as an empirically fixed variable. But it does not have to be fixed, and setting 0.6 as a variable in the fitting process could influence the final outcome of VT50s and thus MPVs. Then comes the fact that the definition of the

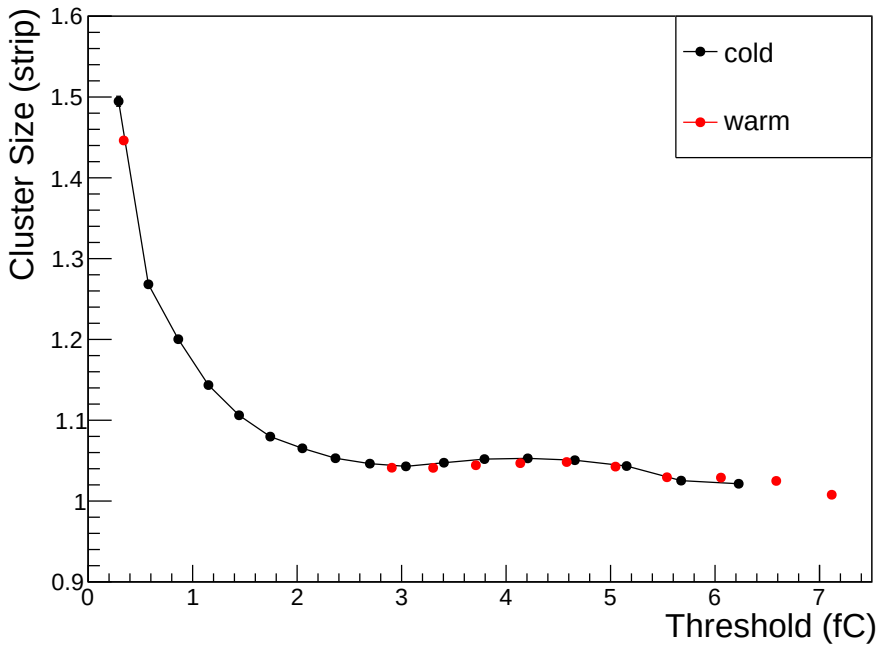


Figure 3.26: The cluster sizes at -30 °C (black) and 30 °C (red) for data set 2.

"center" and "edge" of a strip is chosen to be the 20 % closest to strip center or edge. The choice of the percentage will have an effect on the separation between center and edge. The σ in Equ. 3.1 is actually not an accurate description of the S curve width. As the differentiation of the S curve for beam data should be a Landau distribution and the σ in the fit function is more descriptive for a Gaussian error. To solve this issue, we define 1-σ confidence levels to use.

When the 0.6 is set as a free variable in Equ. 3.1, the function becomes Equ. 3.3. When S curves are fitted with Equ. 3.3, β has the starting value of 0.6 but is set to be a free parameter during the fit. The strips within the beam region each has an S curve and the S curves are fitted with Equ. 3.3 to obtain the new VT50s and new MPVs with β as a free parameter. Then the VT50 and MPV distributions are obtained from Equ. 3.1 and 3.3 are compared with each other, as shown in Fig. 3.27 and Fig. 3.28. As can be seen from the plots, the VT50s and MPVs are quite compatible with each other. The VT50s are very close while the MPVs are not as close. When the parameter β is not fixed, the MPV mean is 3.139 fC and the same mean is 3.191 when β is fixed at 0.6 at -30 °C. Even if they are less alike than

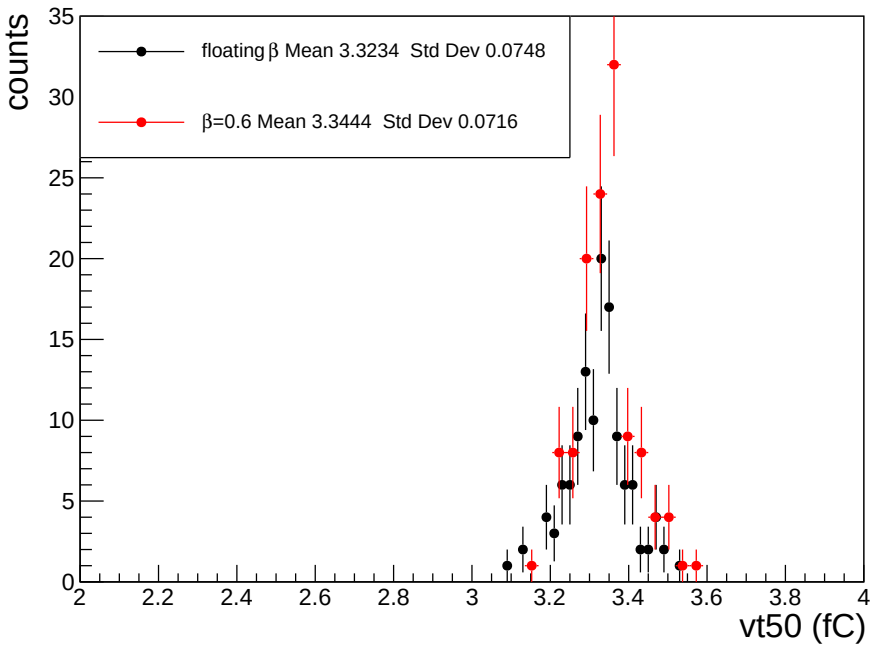


Figure 3.27: The VT50 distribution with β fixed at 0.6 (red) and as a float parameter (black) for cold data set 1 data.

the VT50s, the means are 2 % apart. The 30 °C equivalent plots are shown in Fig. 3.29 and 3.30. When β is fixed at 0.6, the MPV mean is 3.344 fC and the MPV mean is 3.306 fC when it is not. This agrees with the -30 °C instance. As a result, we come to the conclusion that it does not matter much if 0.6 is a fixed parameter or a free one during the fit. However, when β is not fixed, a distribution of βs can be obtained, as shown in Fig. 3.31. The peak of the β distribution is around 0.5. While the historical choice of 0.6 is not too far off, it is not the center of the peak either.

$$f(x) = E_0 \cdot erfc(\alpha \cdot (1 + \beta \cdot \frac{e^{-A\alpha} - e^{A\alpha}}{e^{-A\alpha} + e^{A\alpha}})), \quad \alpha = \frac{x - x_0}{\sqrt{2}\sigma}, \quad \beta = 0.6 \tag{3.3}$$

The definition of "center" and "edge" could also have an influence on the VT50s and MPVs. As is known, there is more charge sharing happening on the strip edges than the strip center, causing more signal loss deposited on a single strip. As VT50s and MPVs are indications of the signal magnitude, they are expected to be influenced by how "center" is defined. To study how much our choice of 20 % being considered the center would affect the resulting

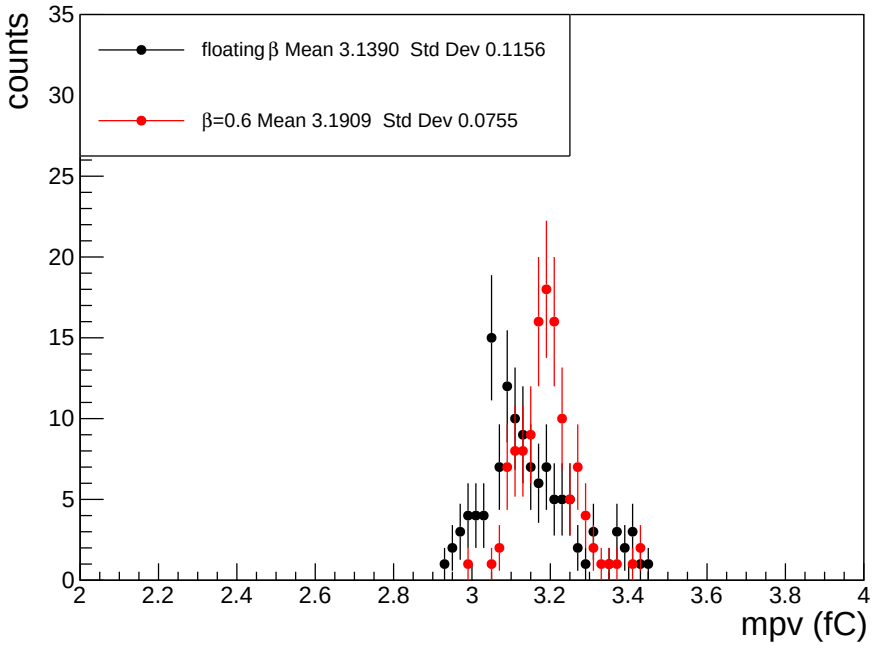


Figure 3.28: The MPV distribution with β fixed at 0.6 (red) and as a float parameter (black) for cold data set 1 data.

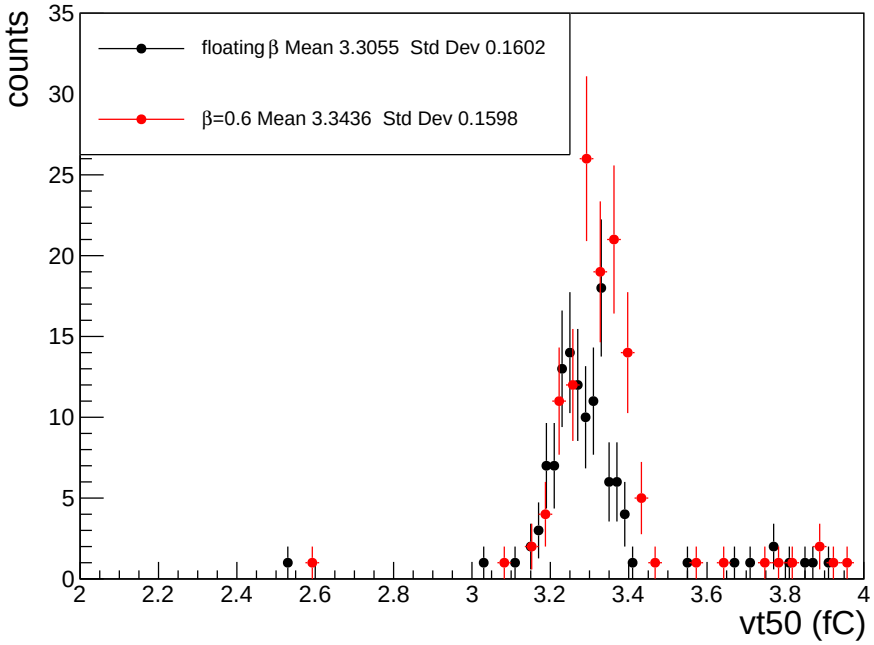


Figure 3.29: The VT50 distribution with β fixed at 0.6 (red) and as a floating parameter (black) for warm data set 1 data.

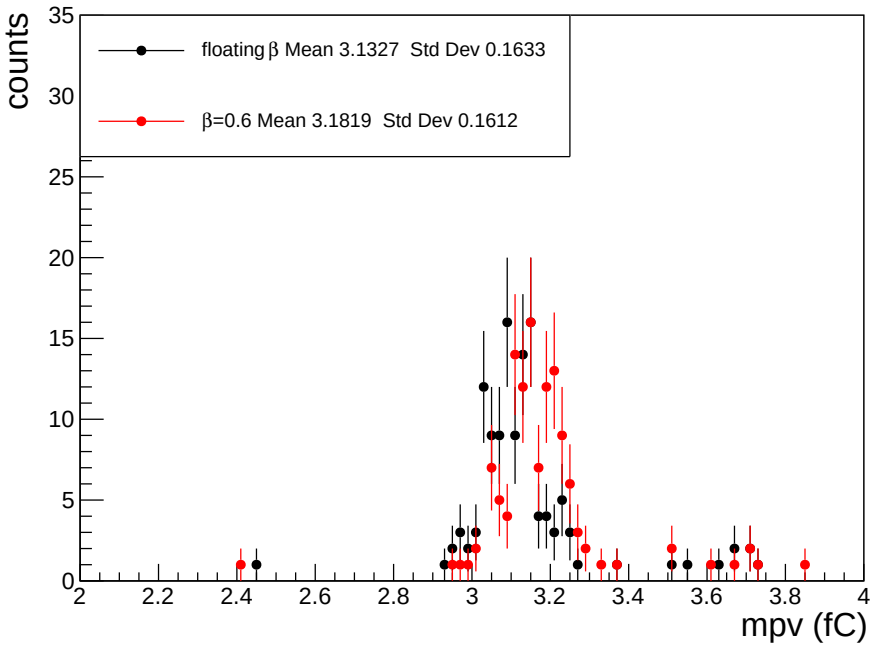


Figure 3.30: The MPV distribution with β fixed at 0.6 (red) and as a floating parameter (black) for warm data set 1 data.

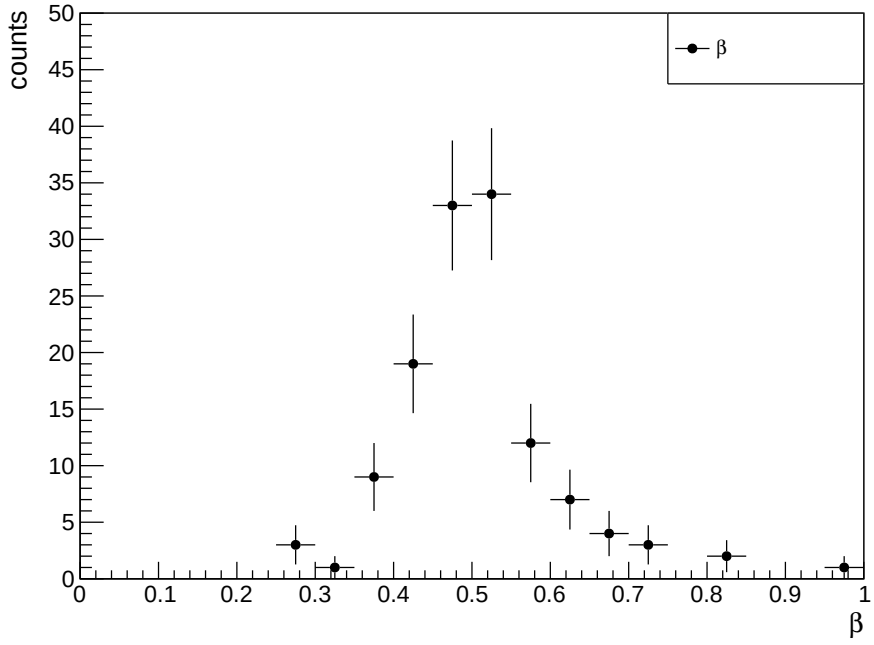


Figure 3.31: The distribution of β as a free parameter

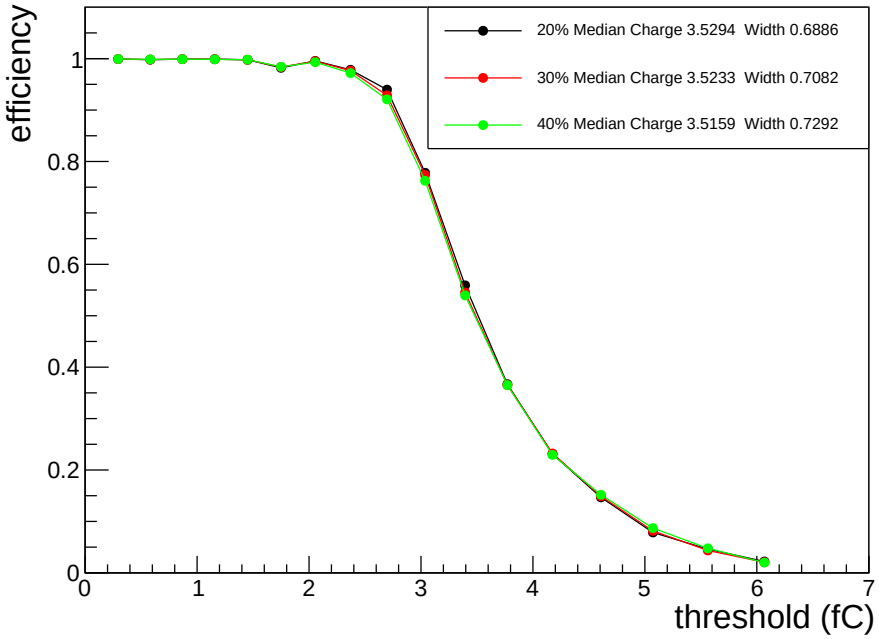


Figure 3.32: The threshold vs efficiency distribution when the particle track passes strip center when "center" is defined as within 20 %, 30 % and 40 % to the strip center with the cold data in data set 1.

signal magnitude, three percentages are chosen to be compared. They are 20 %, 30 % and 40 %.

As can be seen from Fig. 3.32 and Fig. 3.33, there is a slight change in the median charge obtained from the same fit (fit function as Equ. 3.1). But it is obvious that the change is not substantial enough to be disruptive to the signal magnitude results.

In Equ. 3.1, σ is introduced to describe the width of the S curve. But since the differentiation of the S curve is not a simple Gaussian function when it describes the threshold versus efficiency for a charged particle, it is not fully correct to just define width with a single value. The Landau distribution is not symmetric so it would be more sensible to use confidence interval to describe the width of the curve. We choose to use the 68 % confidence interval and define the width on high and low sides respectively as their 1-σ values.

In Fig. 3.34 (-30 °C) and Fig. 3.35 (30 °C), the distribution of σ from Equ. 3.1 fit and the 1-σ values on high and low sides are compared. As expected, σ from the fit is in the middle

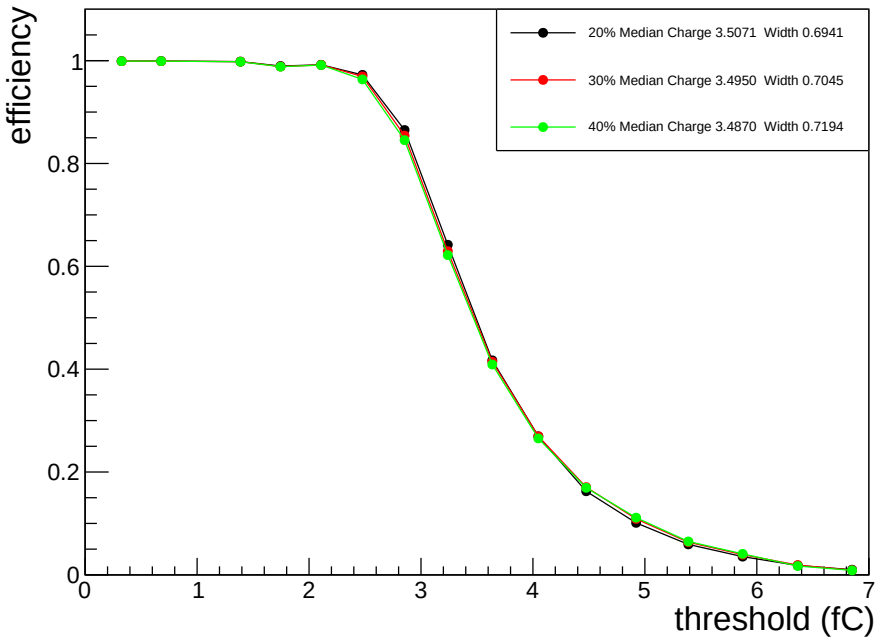


Figure 3.33: The threshold vs efficiency distribution when the particle track passes strip center when "center" is defined as within 20 %, 30 % and 40 % to the strip center with the warm data in data set 1.

of the 1-σ on the low and high side as the Landau distribution has a longer falling part than its rising part. The differences between the fitted σ and the 1-σ values are within 0.2 fC. The larger tail on the high side for the warm data in Fig. 3.16 gives rise to the wider distribution for high side of the 1-σ error (featured as green in Fig. 3.35).

Cross talk from the electronics part of the module also plays a part in the magnitude of the measured signal. Cross talk also introduces some signal sharing between neighbouring strips and the percentage of signal induced on an adjacent strip can be described as Equ. 3.4 as discussed in previous studies [45]. $C_{inter-strip}$ is the inter-strip capacitance and a major factor to the load capacitance. It contributes the most to the cross talk. $C_{backplane}$ is the capacitance of a strip with respect to the back plane. $C_{coupling}$ is the capacitance between a strip implant and the aluminum layer on top of it. Similarly the percentage of the signal collected and successfully transmitted to the readout channel is described as Equ. 3.5. Cross talk increases signal sharing between neighbouring strips, thus having a negative effect on the module performance. So a small inter-strip capacitance and a large coupling capacitance

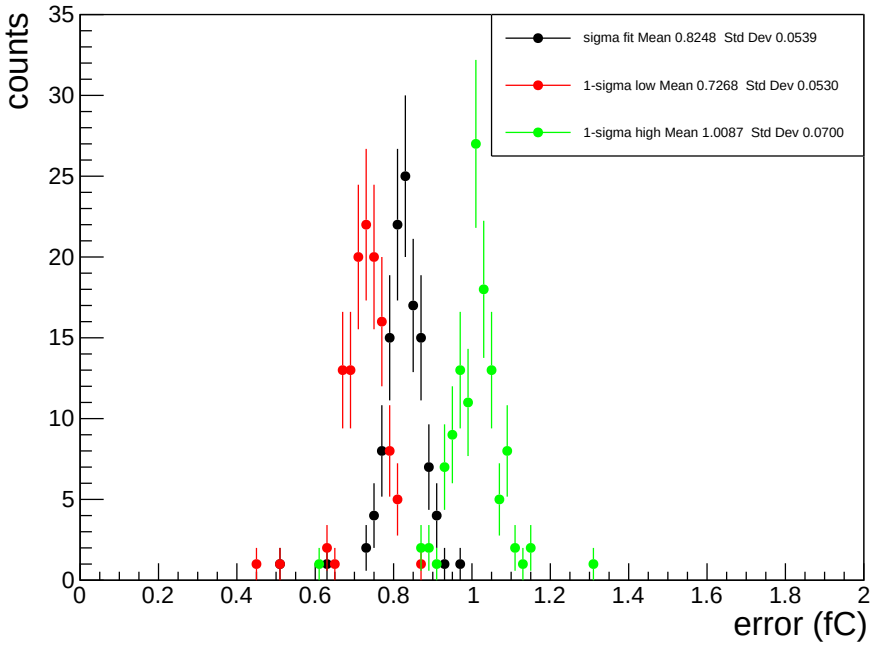


Figure 3.34: The fitted σ (black) compared with 1-σ values on both low (red) and high (green) side for the cold data in data set 1.

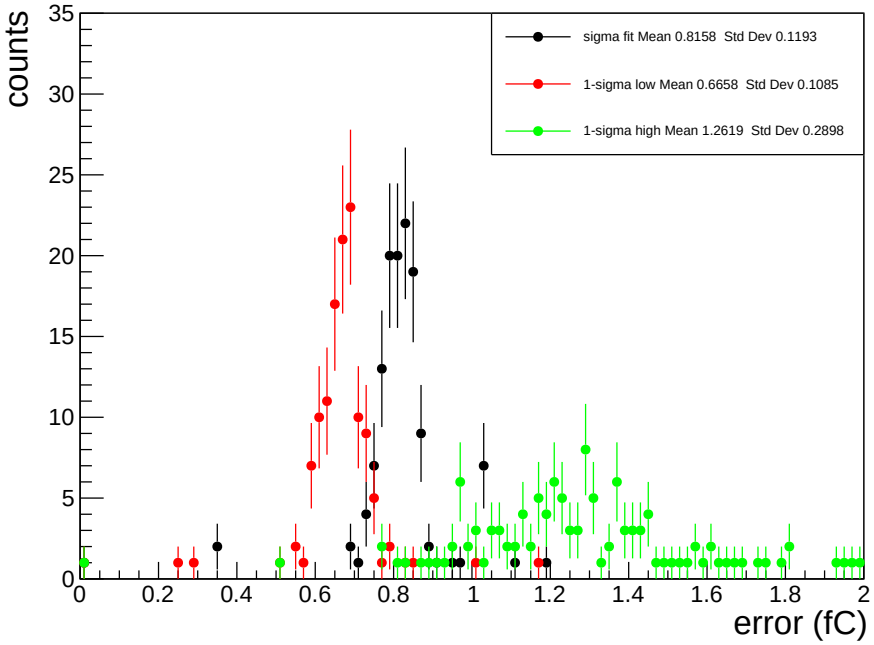


Figure 3.35: The fitted σ (black) compared with 1-σ values on both low (red) and high (green) side for the warm data in data set 1.

are good for the performance.

$$P_{crosstalk} = \frac{C_{inter-strip}}{C_{coupling} + C_{inter-strip} + C_{backplane}} \tag{3.4}$$

$$P_{transmission} = \frac{C_{coupling}}{C_{coupling} + C_{inter-strip} + C_{backplane}} \tag{3.5}$$

The capacitance values of the capacitors are as below from previous studies [45]:

$C_{coupling}$ = 24.28 ± 0.14 pF cm^{-1}

$C_{backplane}$ = 0.2877 ± 0.0008 pF cm^{-1}

$C_{inter-strip}$ = 0.747 ± 0.0004 pF cm^{-1}

So $P_{transmission}$ can be calculated as Eq. 3.6, with the error level of 2.27 $\times 10^{-4}$. The error is very small and does not have any substantial influence on the overall error level.

$$P_{transmission} = \frac{24.28pFcm^{-1}}{24.28pFcm^{-1} + 0.75pFcm^{-1} + 0.29pFcm^{-1}} = 0.959 \pm 2.27 \times 10^{-4} \tag{3.6}$$

For the possible systematic error sources discussed in this section, we noticed that they all have relatively small effects on the overall performance of the signal collection results. The statistical error is about 0.076 fC for the cold data set 1 MPV distribution. The uncertainties we inherit from the calibration is about 5 % according to previous studies. [22] It results in around 0.160 fC according to the same data set. These are the more substantial error sources. All the errors are summarized in Table 3.2. The sum of all uncertainties is around 0.17 fC for both the cold and the warm instances.

	fixed 0.6	Centering (20 % vs 40 %)	Capacitance	calibration	Statistical
cold	0.054	0.014	7.24 $\times 10^{-4}$	0.160	0.007
warm	0.038	0.02	7.24 $\times 10^{-4}$	0.159	0.014

Table 3.2: Charge Uncertainties (Based on data set 1) measured in fC

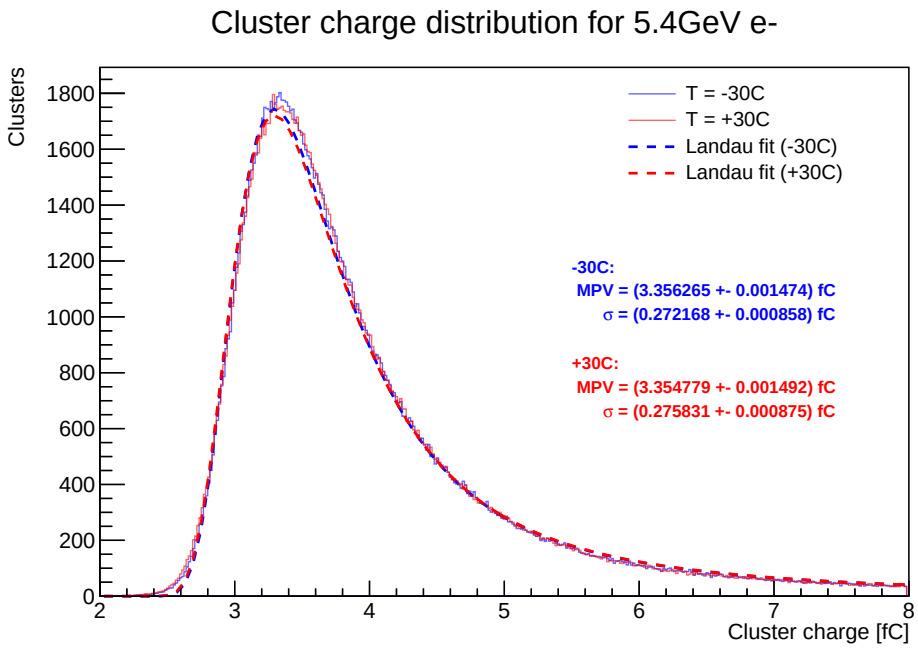


Figure 3.36: MC simulation of the module with 5.4 GeV electron. [48]

The next step is to compare the measurement with simulation and check if they agree with each other within errors. A Monte-Carlo simulation in the Allpix-Squared [46] framework, utilizing GEANT4 [47], is used to simulate the detector response to electrons with the energy of 5.4 GeV. The simulation has taken the cross talk factor into consideration, with the results shown in Fig. 3.36. [48] The simulated MPVs are 3.36 fC at -30 °C and 3.35 fC at $+30$ °C. This simulated signal is larger than the average signal seen from the MPVs obtained from the data. There are various aspects that could contribute to the signal loss in data taking.

The first one is the fact that MPVs are measured for all strips, regardless where the particle track possibly passes through. The MPVs correspond to the "average" distributions in the threshold versus efficiency plots. On the other hand, the simulation does not feature charge sharing so it corresponds to the "center" distributions. From Fig. 3.32, it is possible to get the estimation of the VT50 (corresponding to median charge) when particles pass through strip centers. As MPVs are not exactly the same as VT50s due to the Landau distribution of charged particles, a coarse estimate is introduced to know what MPV would be if particles pass through strip centers only. Comparing Fig. 3.16 and Fig. 3.17, along with Fig. 3.24

and Fig. 3.25, we can see that the ratio of $\frac{MPV}{VT50}$ is almost constant. The average of the $\frac{MPV}{VT50}$ ratio for all four instances is 94.75 %. With this ratio and the median charge study in Fig. 3.32, the measured MPVs are 3.37 fC at -30 °C and 3.34 fC at $+30$ °C, see Tab. 3.3.

	simulation (fC)	uncorrected charge (fC)	corrected charge (fC)	uncertainty (fC)
cold	3.36	3.19	3.37	0.17
warm	3.35	3.18	3.34	0.17

Table 3.3: Comparison of the total charge measured in the ITk Short Strip module tested by the 5.4 GeV electron beam - both uncorrected and corrected charge values are listed - with the output of the GEANT4 simulation.

After correcting for these factors, the measured signal from data is 3.37 fC for the cold instance and 3.34 fC for the warm instance while the simulation result is 3.36 fC for the cold instance and 3.35 fC for the warm instance. The uncertainty for the experiment measurement is estimated to be around 0.17 fC as shown in Table 3.2. This proves that the measurement agrees with the simulation within errors.

The signal-to-noise ratio (S/N ratio) can be obtained from the test beam measurements as well. According to the noise level that is obtained from the pedestal studies and the signal level from the beam studies, Table 3.4 shows the S/N ratios that is obtained from this test beam campaign. The detector requirements of at least 99 % efficiency and less than 0.1 % noise occupancy equate to a signal-to-noise ratio requirement of at least 10 throughout the lifetime of the detector.[4] According to previous studies, the noise is not hugely influenced by the radiation while the signal is expected to decrease from 17300 to 11500 electrons. [22] The average S/N ratio here for an un-irradiated module is about 30.

	Noise (fC)	MPV (fC)	S/N Ratio
cold	0.0891 ± 0.004	3.19 ± 0.17	33.33 ± 2.49
warm	0.1088 ± 0.0012	3.18 ± 0.17	28.94 ± 1.60

Table 3.4: Signal-to-noise ratios calculated for the ITk Short Strip module measured both at -30 °C and $+30$ °C. The estimate of noise and MPV both used the mean values of the distributions.

The requirement of the ATLAS experiment of ITk strip detectors is to have the detection efficiency above 99 % and the noise occupancy below 10^{-3} throughout their operation.

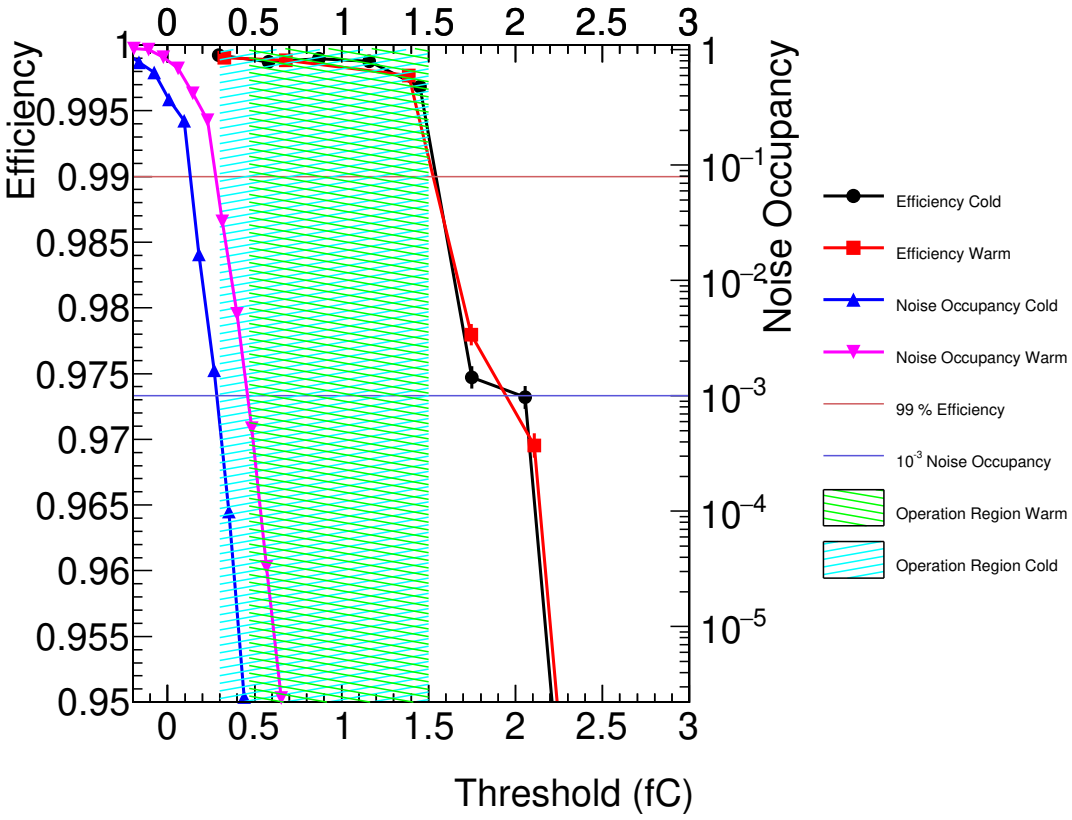


Figure 3.37: Operational region of an un-irradiated ITk Short Strip module with detection efficiency higher than 99 % and noise occupancy below 10^{-3}.

The plausible operational region for the ITk strip module defined by the noise occupancy obtained from the pedestal runs and detection efficiency from the tests with the beam is shown in Fig. 3.37. Even if the signal will degrade after radiation as discussed in Sec. 2.2, there is a wide operating window to meet the requirements. The results shown in Table 3.4 provide evidence that the safety margin of the SNR at the start of the HL-LHC will be larger than the factor of three.

3.5 Pulse Shape Studies

As is discussed in Sec. 3.3 and Sec. 1.2, timing plays an important factor in signal collection. The shaping time needs to be chosen so that the noise charge is controlled and the pile-up effect is minimized. Delays are a setting to adjust the selection window for the incoming signal pulse. 16 counts in delay correspond to 25 ns. As shown in Fig. 3.20, even at the

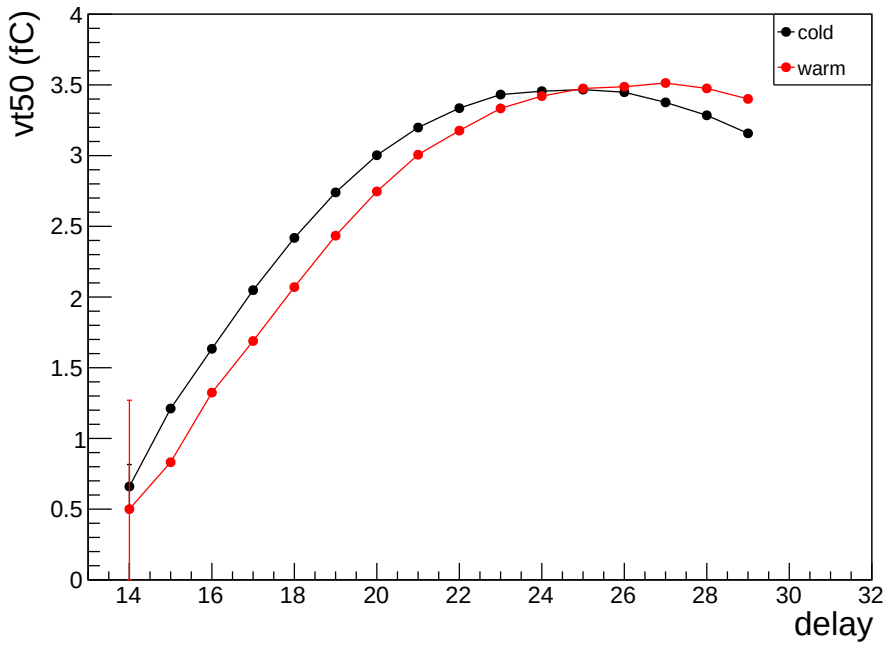


Figure 3.38: Relation between delay settings and VT50 at both cold (black) and warm (red) temperatures for data set 1. The uncertainty in the Y axis is the standard deviation.

same threshold, the efficiency has a dependency on delay. The delay window for pulse selection here is chosen to be 21 to 28 in delay in these studies. The same delay window is applied for both warm and cold instances.

At each delay point, the relationship between efficiency and threshold (fC) can also be plotted as an S curve and a VT50 value can be obtained at each delay by fitting the curves. The relations between delay and the VT50 at that delay in the cold and warm instances are shown in Fig. 3.38 for data set 1. The same relation for data set 2 is shown in Fig. 3.39. The two plots illustrate the relation between the VT50 (median charge) and timing, which suggests the shape of the signal pulse in the timing domain. Due to the missing points in the warm case for data set 2, at low delay settings where the efficiencies and statistics tend to be lower, the fit fails quite often. This leads to the disturbance in Fig. 3.39 before delay point 19. The statistical error bars on those points are quite large, indicating the points being inaccurate.

As can be seen from Fig. 3.38 and Fig. 3.39, the full pulse shape is not quite covered

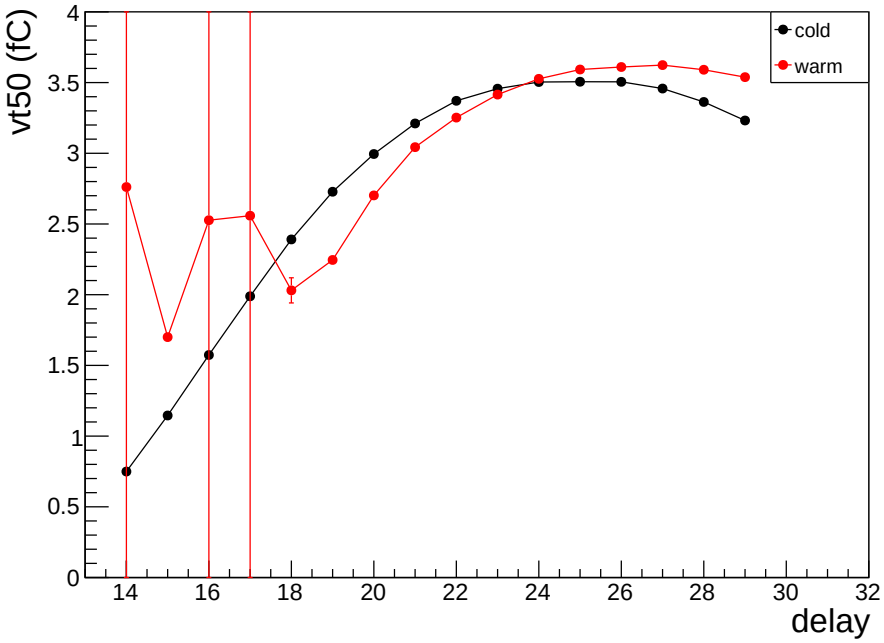


Figure 3.39: Relation between delay settings and VT50 at both cold (black) and warm (red) temperatures for data set 2. The uncertainty in the Y axis is the standard deviation. The scattering points from delay 14 to 18 in the warm plot presumably come from the fact that there are quite a few missing data points in the S curve.

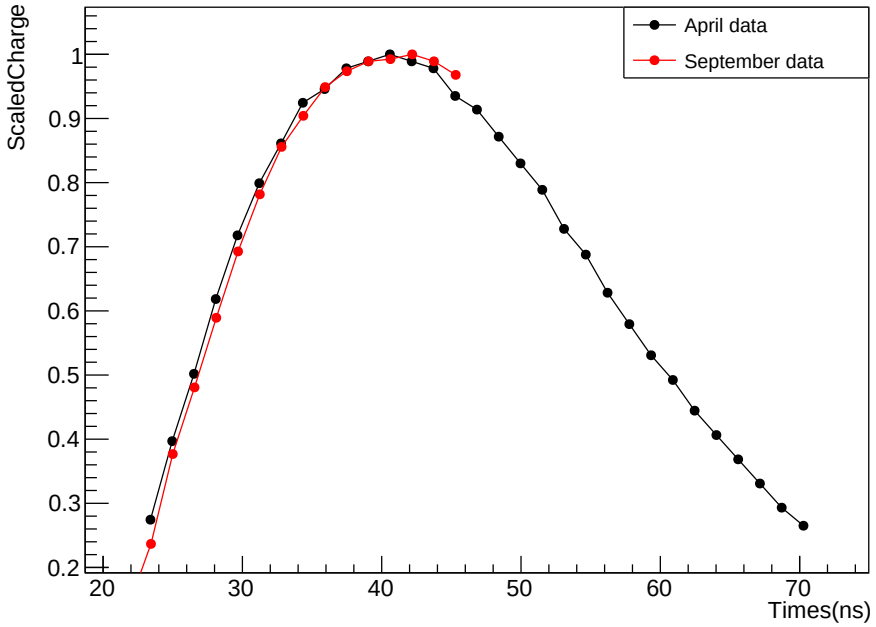


Figure 3.40: Comparing full three-BC data (black, labeled as "April data") with one-BC data (red, marked as "September data"). They agree very well.

within the delay settings range. This is because data was only taken corresponding to one BC, which is equivalent to 25 ns, in the Sept. 2019 test beam campaign. The full data should cover not only the BC with the trigger but also one BC before it and one after. Fortunately our colleagues looking at data from another test beam campaign (April 2019 campaign) provided the data with full coverage of three BCs. [49] That test beam campaign is performed only at the warm temperature. The full data now covers rising and falling edges and agrees with our warm pulse from data set 1 very well in shape as can be seen in Fig. 3.40.

Fig. 3.40 confirms that three-BC data, also named as April data as the test beam campaign took place in April 2019, agrees with the Sept. 2019 data sets quite well. So April data is used in this section to be compared with the simulation as it covers more of the pulse shape.

The pulse shape simulation is performed in two steps. First the performance of the pulse of a charged particle passing through the silicon, inducing a pulse. [50] Then this pulse is fed into the front-end amplifier and discriminator of the ABCStar chip, which is simulated with

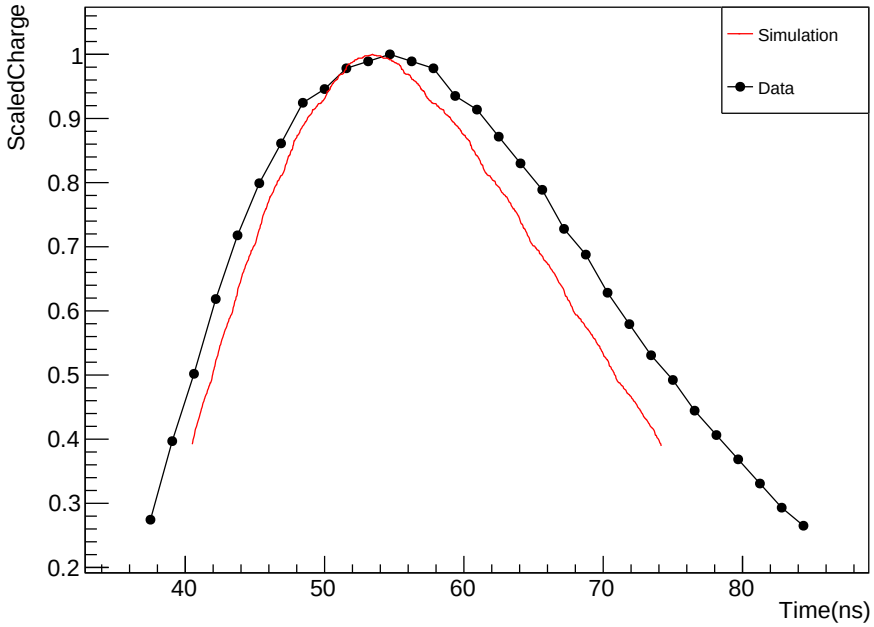


Figure 3.41: Comparing pulse shape from data (black) and simulation (red).

SPICE software [51]. The pulse voltage is measured in mV. Then the pulse is processed through a toy Monte Carlo algorithm to obtain the final time versus charge pulse shape needed. The toy Monte Carlo algorithm calculates the signal charge corresponding to time slices to give a time versus charge distribution. Then the output signal is scaled to be the actual signal deposition in data and compared to threshold in each time slice. The resulting efficiency versus threshold relation can then give a VT50 in each time slice. The VT50s are then scaled down to have a maximum at the value of 1 to be comparable with data. The relation between the scaled VT50 and time in ns is illustrated as "Simulation" in Fig. 3.41.

The data and the simulation comparison are shown in Fig. 3.41. As the simulation used a heavily simplified model, the agreement between the pulse shape from the simulation and the data is not too good. However, a more detailed model was applied to calculate the FWHM value of the pulse shape [22] and it gives 34 ns as the FWHM. The FWHM obtained from the data is 34.13 ns and the simplified simulation gives 28.96 ns.

To estimate the uncertainty on the FWHM from the data, both statistical and systematical aspects are considered. The largest uncertainty on the clock time measurement would be

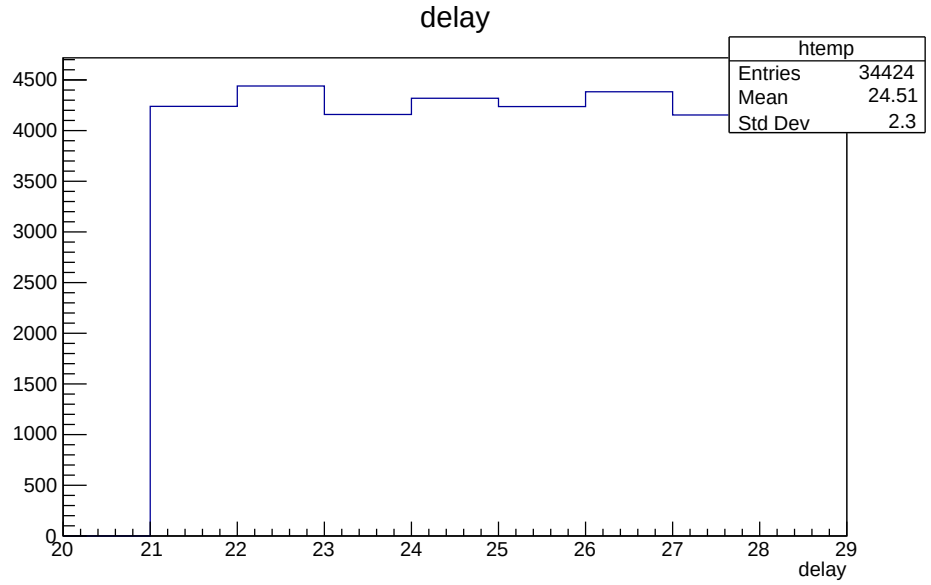


Figure 3.42: Number of events per delay count at one threshold in September campaign data. The number of events per delay is not unified.

clock-to-clock jitter, yielding at most 10 % of the cycle length, leading to about 150 ps. But the time duration of each delay bin could also vary. Assuming the event number per delay is consistent between April and September campaign, the uncertainty on one delay count duration can be estimated by Fig. 3.42. The number of events per delay is 4303 with uncertainty of 2.8 %. This suggests an uncertainty of 2.8 % on each delay count duration as the beam is expected to be even for each delay setting.

Assuming the April campaign data also has similar features and event number per delay, the uncertainty on the X axis of the pulse shape plot would be 2.8 % and $\frac{10\%}{\sqrt{4303}}$ added quadratically, which results in 2.80 %. The uncertainty on the Y axis is mostly propagated from efficiency statistical errors. A coarse calculation is done by identifying the four points closest to the FWHM line and propagating errors in the Y axis. In all, the statistical error on the FWHM is estimated to be 0.092 ns.

Considering the systematical uncertainty introduced by the uneven time bins, a toy simulation method was introduced to randomize the size of time bins and give a distribution of the resulting FWHMs. The FWHM distribution is shown in Fig. 3.43, with a width of 0.2 ns.

Finally there is the fact that the data points are not continuous. It is not certain that the peak

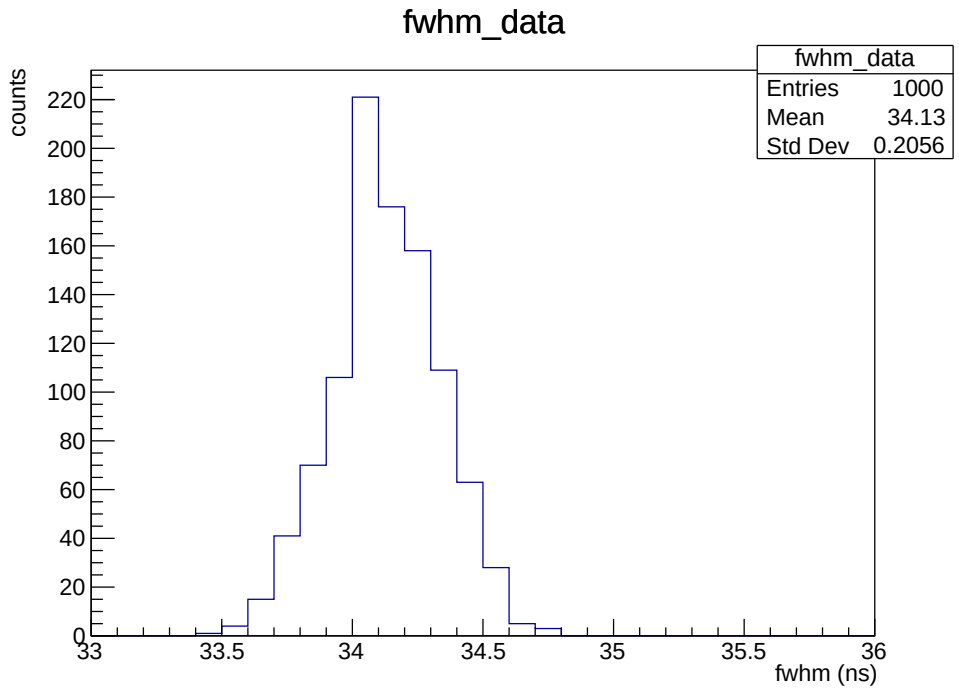


Figure 3.43: Distribution of FWHM when the delay bin size is randomised according to the uncertainties.

source	clock jitter	statistical	time bin randomisation	discontinuity
uncertainties (ns)	0.15	0.092	0.2	0.07

Table 3.5: Pulse shape FWHM uncertainties

of the curve actually falls at the position of the maximum point. A smooth fit of the peak to re-obtain the maximum value and its position is performed. The FWHM from the "new" maximum is 34.20 ns, resulting in a 0.07 ns difference.

The uncertainties are summarised in the Table 3.5.

In total the uncertainty of the FWHM can be very conservatively estimated to be 0.28 ns. The theoretical FWHM is 34 ns with circuit model according to previous studies [22]. As the pulse from the sensor is 98 % contained within a 5 ns bin, the pulse is short enough to be replaced by a delta pulse in circuit modelling on the scale of 34 ns. The data agrees with the theoretical calculations within uncertainties.

4 | Tape Tester Robot

The accuracy of the robot measurement of the fiducials needs to be the order of 50 um over the full area of the tape in order to check the dimensions are compatible with the specifications in Sec. 2.4.1. In order to probe pads with a width of 150 um for continuity and short circuit testing, the robot is required to have a local precision of 10um. This precision is achieved using measurements of local fiducials close to the bond pad fields.

4.1 Tape Test Robot Setup

The tape tester robot is composed of the control computer, the drive system, the power supplies, the DVM and the robot space. As shown in Fig. 4.1, the robot space includes two stages to do the measurement and a plate to place tapes. The two stages, named as Stage 1 (S1) and Stage 2 (S2) in later discussions, have camera systems for image taking and probe systems connected to a DVM for current and resistance measurements. The drive system is located inside a cabinet and the DVM and HV system is inside a crate in the lab. They are connected to the robot stages with cables. The drive system controls the movement of the stages. The DVM is used for resistance and leakage current measurements in the tape testing procedures. The HV system can deliver up to 1 kV in the HV leakage current measurements.

Fig. 4.2 is a photo of a stage, the stage includes two cameras and a probe connected to the DVM. One of the cameras is the main perpendicular camera and the other is the 45 ° camera. The main camera is for image taking as well as distance measurements during tests and calibration. The 45 ° camera is mainly for trouble shooting. The probe is connected to the DVM for connection measurements and HV leakage current measurements. The resistance measurement is achieved by the four-wire method [52] to minimise errors from the resistance of the wires in the test leads. There is also a ring of LED lights to illuminate the camera view area.

In order to hold the tapes down, especially the co-cured tapes, there is a heavy brass lid on

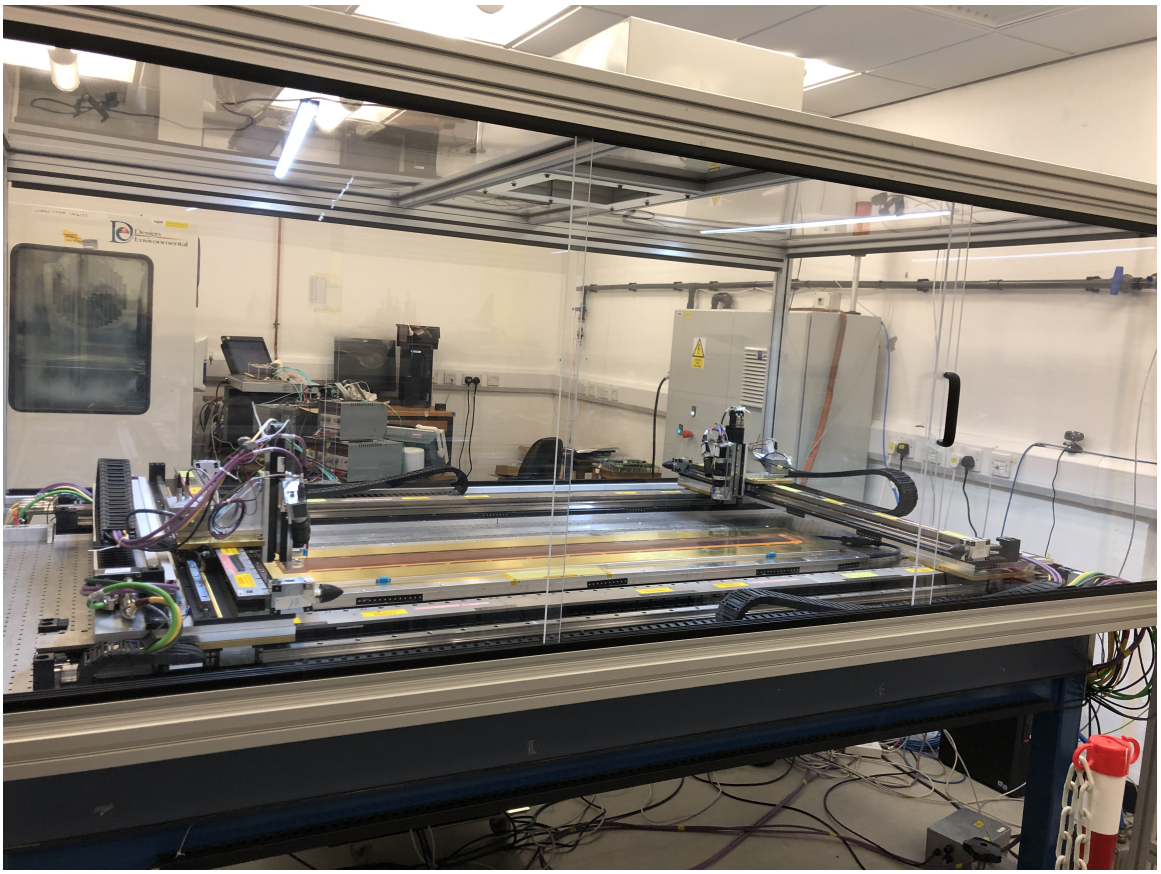


Figure 4.1: The robot layout in the lab. The drive system is connected to the stages from the cabinet in the right corner of the photo.

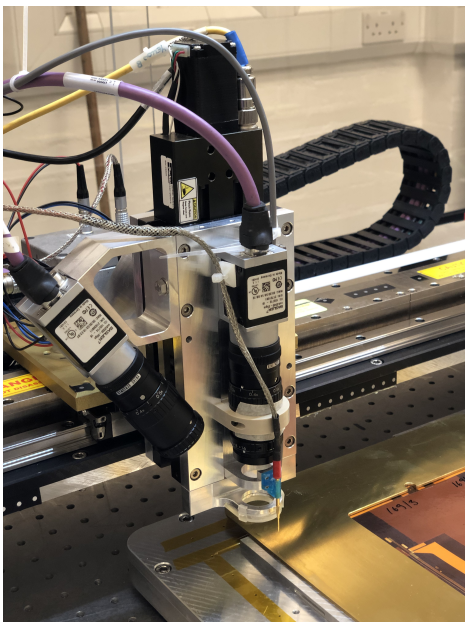


Figure 4.2: A stage. The perpendicular camera is the main camera used in tests and calibration, the 45° camera is for monitoring. The probe is connected to the DVM system for connection and HV tests.

the tape plate, as shown in Fig. 4.3. There is a vacuum pump connected to the tape plate and is used to make sure the tape position is secure during testing.

All the control software is developed and operated from the control computer located in the robot laboratory. A microscope is set up in the lab as well for visual inspection when unexpected issues arise.

To ensure the cleanliness of the testing area, the robot space is enclosed with sliding doors and an air pump is placed on the top to blow clean air through a High Efficiency Particulate Air (HEPA) filter to the testing area to remove dust. The operating personnel are required to wear clean room coats and hair nets. Regular cleaning is also planned in the lab.

4.2 Robot Calibration and Validation

4.2.1 Calibration Procedure

The tape tester robot is required to perform tests on pads of 150 μm in size and the maximum spatial resolution requirement is 50 μm. For the current status of the robot, the spatial

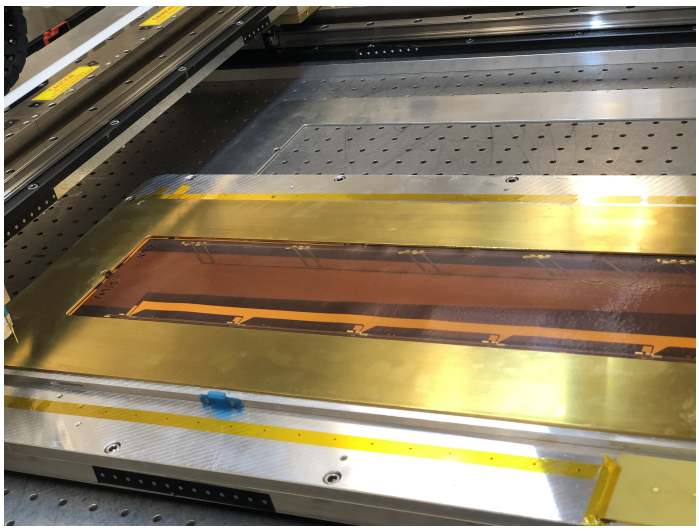


Figure 4.3: The brass lid used to hold down tapes

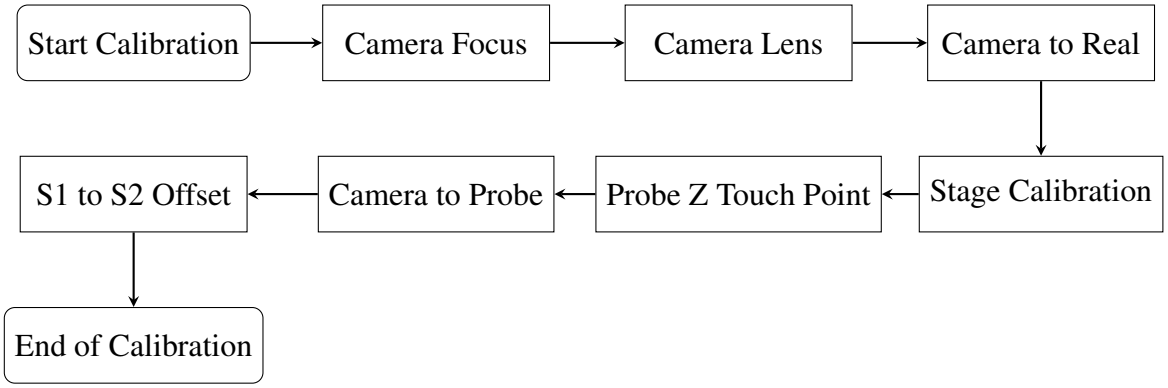


Figure 4.4: Robot calibration procedure

precision is limited to 10 μm, which is sufficient for the purpose of this robot. A strict and complete set of calibration procedure is required to keep the measurement accurate. Fig. 4.4 is the flow chart of the calibration process.

For calibrating the cameras, a calibration plate is needed, as shown in Fig. 4.5. There are three steps to complete the camera calibrations. In the first step, camera focus calibration, is to find the focus point of the cameras by moving the cameras along the Z axis. This process used to be achieved manually but was later automated. The camera for each stage is gradually lowered from nominal position by small steps, taking pictures of a calibration plate 4.5 in the process. Then the pictures of the plate taken are processed with a python script using the OpenCV package [53] to locate the position where the picture quality is the

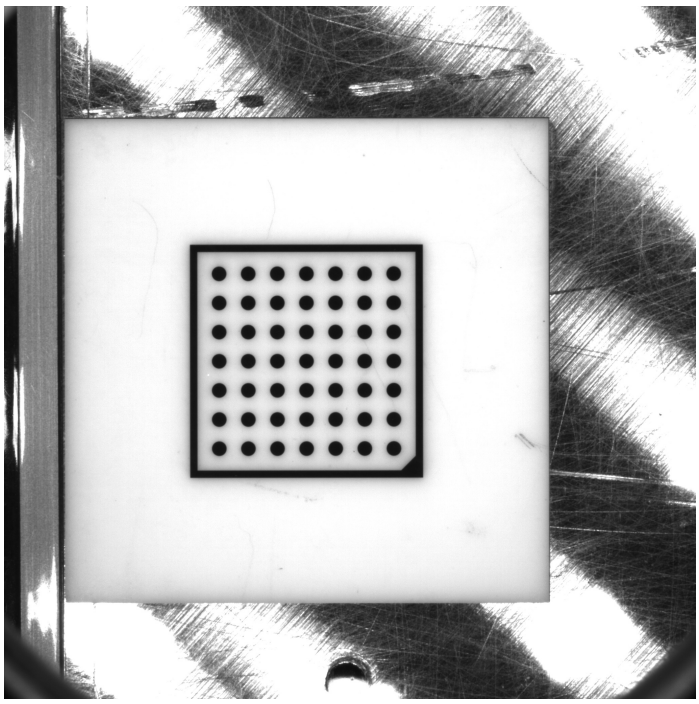


Figure 4.5: Camera calibration plate

best.

When the cameras are in focus, the next step is the camera lens calibration, which is to take a series of images of the calibration plate with both cameras so that the parameters of the cameras, such as the pixel size and optical distortion, are calibrated. Then the cameras are moved in various directions for known amounts of distance and take another series of images of the calibration plate. From these images, the axis angles and movement size in terms of the calibration plate can be calculated. This step is named as camera to real calibration. The height distance between the center of the camera and the measured surface needs to be the same as used in the camera calibrations in order to keep pixel sizes constant. After this, the cameras are known and calibrated, the next step is to find the area of measurement in the robot space.

A large plastic calibration film with evenly distributed circles is applied over the area of interest, as shown in Fig. 4.6. The circles are on a nominal grid and measured by a SmartScope [1]. The center of circles are 20 mm apart in both X and Y direction and the circle

[1] A SmartScope is a 3D multisensor dimensional measuring system that gives accurate dimensional measurements.

diameter is 5 mm. The directions are defined in Sec. 2.4.1. Both cameras scan across the surface and find each of the circles. The measurement made by the robot is then compared with the measurement done by the SmartScope of the same object. The stages' long-distance movement distortions and encoder positioning are thus calibrated in this process. This procedure is effectively calibrating the robot against the SmartScope. This step is called the stage calibration. In Fig. 4.7a and Fig. 4.7b, the positions of the points are the start points. The magnitude and directions of the differences are represented by the lines. The size of the lines is enlarged by a factor of 100 for visibility. Fig. 4.7a is for Stage 1 and Fig. 4.7b is for Stage 2. From the two plots, it can be seen that the lower Y region for Stage 2 and the higher Y region for Stage 1 have a better match between nominal and actual positions. Since the two stages' coordinates have an 180 degree rotation, the lower Y region for Stage 2 and the higher Y region for Stage 1 are the same area. This is also the same area used by the robot that has the highest requirement on calibration. The calibration procedure creates a look-up table which gives the offset between stage encoder location and "true" location at the centre of the circles. The robot software then uses this look up table to perform linear interpolation between the neighbouring circles to calculate the offsets to use in the X and Y directions.

The calibration of cameras and stages ends this step and then the probes on the stages, with which we probe pads on tapes and test connections, need to be calibrated.

Since the probes need to touch the surface of the tapes and have a firm but not too much pressure on the tape surface, the probe position in the Z direction also needs to be calibrated for both stages. The probe "Z touch point calibration" finds the position where the probe makes contact to the test surface. Another calibration plate (as shown in Fig. 4.8) is used for this purpose, when the probes make contact with the metal part of the plate, they will form connections, so that the probe Z height can be determined. The probes also need to be calibrated to the cameras, so that we know the exact distance between the center of the camera view and the probe. The same calibration plate is used in this process by using the cameras to find the circles in the middle of the cross and using the probes to locate the X and Y direction lines.

Apart from the cameras and probes, the relation between the coordinate systems of the

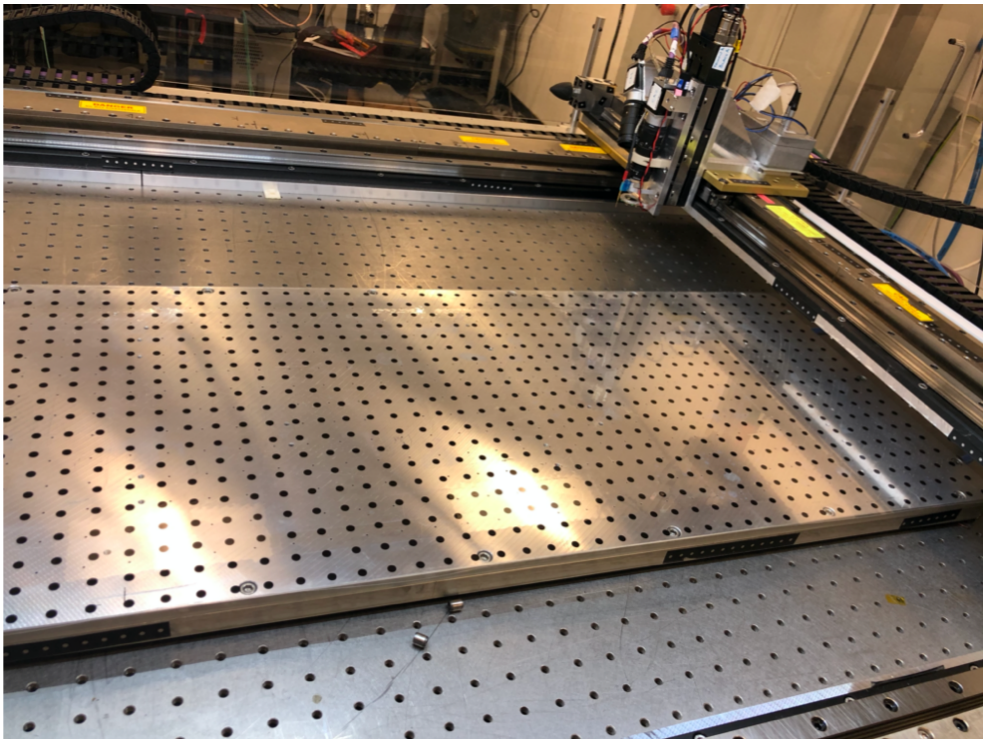


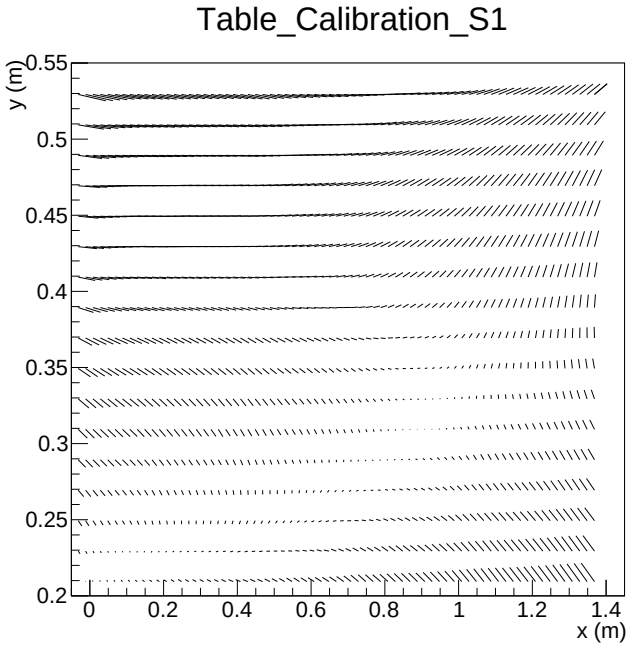
Figure 4.6: Plastic calibration film loaded in robot space

two stages also needs calibration. The coordinate system in the robot space is based on Stage 1 and a transformation relation is developed to obtain Stage 2 coordinates. This transformation relation calibration is achieved by measuring the same series of fiducial points with both stages. Fiducials are the reference points the system uses to locate items. Then a transformation equation is developed based on the measurements. This is the S1 to S2 Offset calibration. The calibration process is completed here.

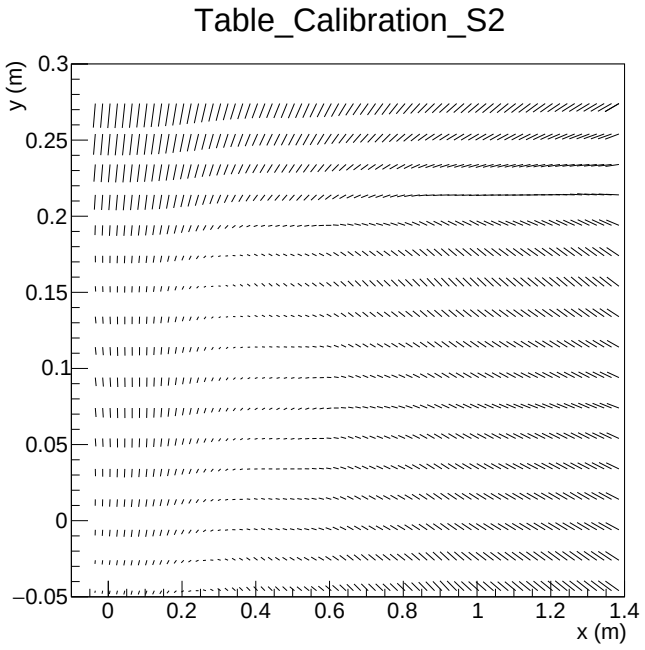
This is a general procedure for the robot calibration. To ensure the correctness of tests, the camera-probe calibration and probe Z touch point calibration needs to be repeated after changes of a probe pin or in the rare event of a collision. In production the probe pins should be replaced regularly to avoid the quality of contact deteriorating.

4.2.2 Calibration Validation

To ensure the accuracy of the calibration, the calibration validation process is introduced. This is performed by measuring the size and dimensions of the same object with the robot



(a) The positions (X,Y) of the points used in stage calibration and the difference between found positions and nominal positions measured by Stage 1.



(b) The positions (X,Y) of the points used in stage calibration and the difference between found positions and nominal positions. Measured by Stage 2.

Figure 4.7: The positions (X,Y) of the points used in stage calibration and the differences between found positions and nominal positions. The point positions are the SmartScope default positions. Differences scaled by 100 for visibility.

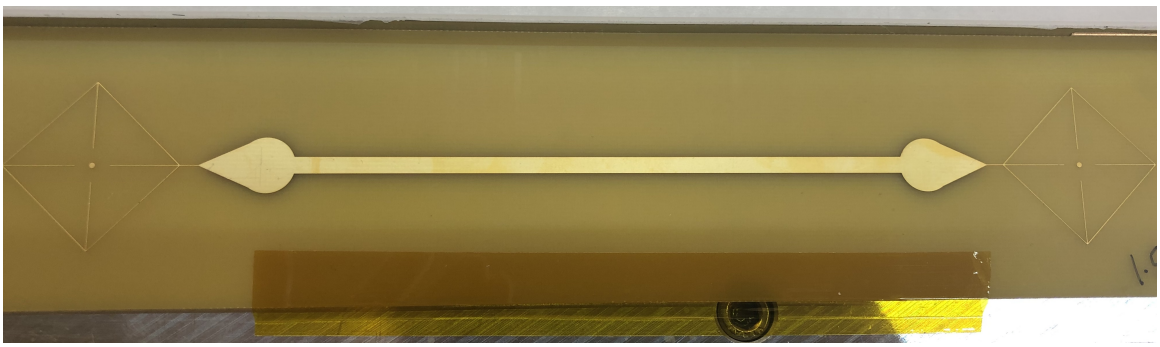


Figure 4.8: Calibration plate for Probe Z Touch Point calibration and Camera to Probe calibration.

and another known accurate system and comparing the results. The agreement between the two results indicates the accuracy of the robot calibration. The robot is required to identify if tapes have geometry differences from the CAD design by more than 1 mm/m. CAD, computer-aided design, is used here as the nominal position of tape features. As discussed in Sec. 2.4, the direction of the tape length is defined as the X axis and the perpendicular axis is the Y axis. In Y direction, the tapes need to be within 600 μm difference of the specifications. This specification is determined by preserving HV clearances at both sides of the module. On one side the sensor can get too close to data lines and on the other side, the HV pads can be too close to the edge of the tape. We expect the calibration error to be within 100 μm/m in X direction and within 200 μm/m over the size of the tape in Y direction to ensure the robot is able to identify tapes failing requirements. The 100 μm/m criteria is set to ensure the accuracy of the robot measurement.

As shown in Fig. 4.9, wire-bonds are used to connect pads on the bus tape (green pads) with corresponding pads on the module (purple pads). If the module pads and tape pads are not well aligned, the wire-bonds will have extreme angles and are very difficult to wire-bond. Since modules are always loaded at the nominal position, tapes are required to have a good accuracy to ensure the pads are well aligned.

There are two major validation campaigns since the finalisation of the calibration process. The first campaign happened in 2019 and the second happened in 2021 after a hardware system upgrade on the stages.

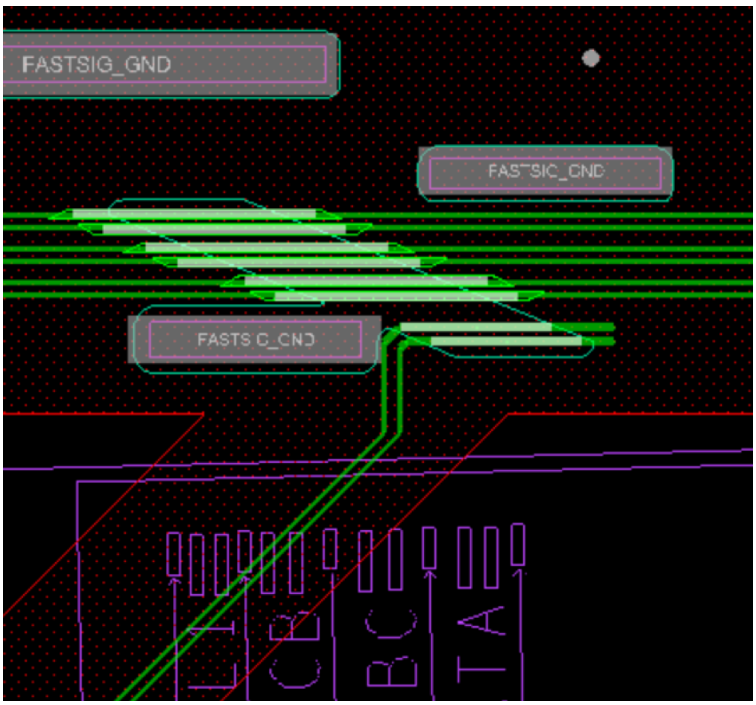


Figure 4.9: Wire-bonds are used to connect pads on the bus tape (green pads) with corresponding pads on the module (purple pads). If the angle or distance of a wire is too large, it is more difficult to make the wire-bond connection. The angle should be kept within 45 °.

4.2.2.1 2019 Calibration Validation Campaign

The first validation system introduced is the Vstar [54] system. It is a camera system that takes multiple pictures of a 3D object and reconstructs the dimensions of the measured object. The user adds a number of circles of a defined diameter on a sticky tape (see Fig. 4.10). The software identifies these circles and finds the circle centres. It then uses stereo reconstruction to determine the 3D co-ordinates of all the circles. The object measured with both VStar and the robot systems was a large carbon fibre sheet with calibration points distributed in five rows, as shown in Fig 4.10. All the calibration points are measured with both systems and the results are compared. Since the two stages in the robot system are heavily linked to each other by calibration, S1 was used to represent the robot measurements. In each row the distance between the first point and other points are measured with both systems and are compared. For each row a linear fit is applied to obtain the slope and offset, which indicates the agreement between the two measurements. An example curve and fit is shown in Fig. 4.11. The fit results are given in Table 4.1. Row 3 has a slightly different

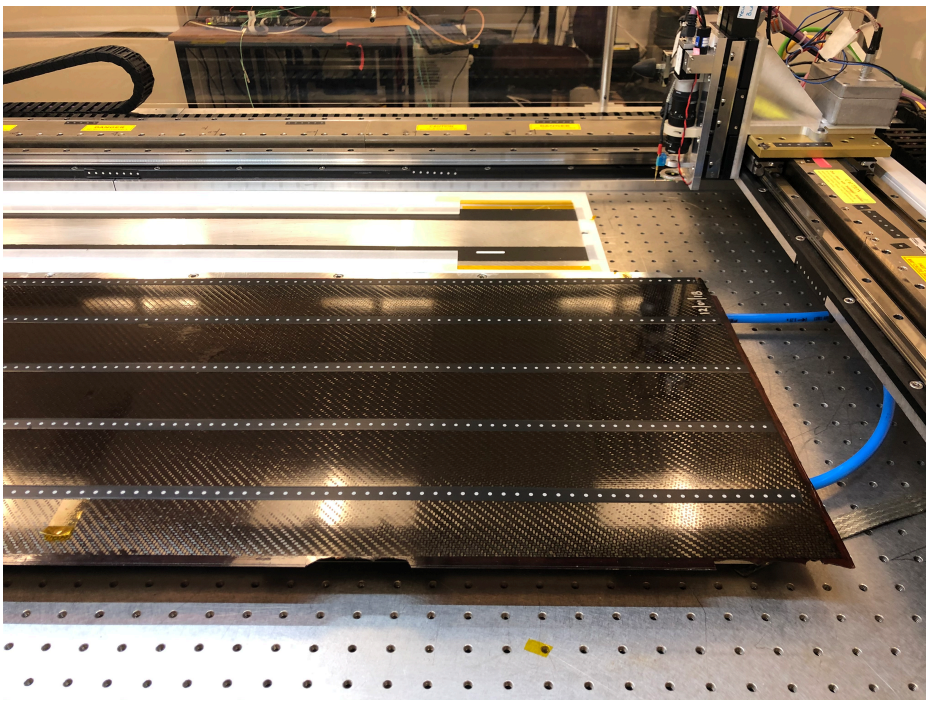


Figure 4.10: A large carbon fibre sheet with five rows of calibration points on it.

result from others as the robot missed a few points in this row, so that Row 3 is not included in further comparisons.

Row number	Offset (mm)	Slope	Slope Error
Row 0	4.149×10^{-5}	1.00018	1.6164×10^{-5}
Row1	-0.323841	1.00016	1.716×10^{-5}
Row2	-0.293391	1.00019	2.2313×10^{-5}
Row3	-0.753244	1.0003	0.0001139
Row 4	-0.2319	1.00019	2.03×10^{-5}

Table 4.1: Offsets and slopes of the linear fits of the Vstar versus robot correlation. Example fit shown in Fig. 4.11.

The slope data suggests that there is a 180 μm/m difference between the Vstar measurement and the robot measurement. To verify this observation and to get more insight in the cause of this difference, the SmartScope system [55] is introduced. Both the SmartScope and the robot performed measurements on CAD fiducials on a co-cured tape. CAD fiducials are larger fiducials that help locate the tape in the robot reference frame, which are discussed in Sec. 4.3.1. High and low Y side CAD fiducials are compared separately. "High" and "low" Y sides are determined with the tape X-Y dimensions as discussed earlier. Measured

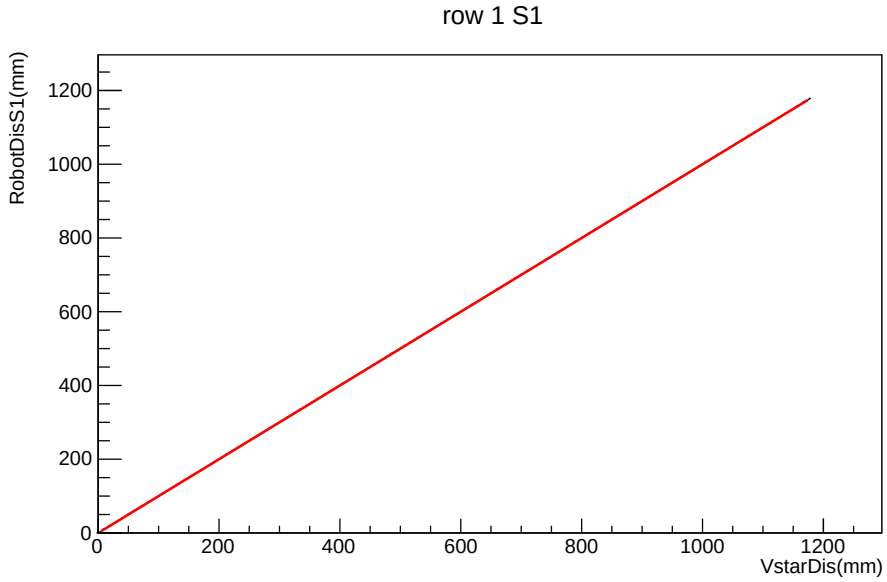


Figure 4.11: The correlation between two measurements for one of the five rows. The black line is made of data points and the red line is the linear fit. X axis features V-STARS measurements of the distance between the point measured and the first point and Y axis is the robot measurements. Unit in mm.

distance comparisons between SmartScope test results and robot test results are performed for both Y sides of the tape. The X axis is SmartScope measurements and the Y axis is the robot measurements. Then the curve is fitted with a linear fit in a similar manner as Fig. 4.11. Linear fit results, as in Table 4.2, show a similar difference of about 180 μm/m between the robot and the SmartScope measurements.

Y Side	Offset (mm)	Slope	Slope Errors
high	0.000931999	1.00019	3.31432×10^{-06}
low	-0.0125531	1.00017	1.51816×10^{-05}

Table 4.2: Offsets and slopes of the linear fits of the SmartScope versus robot measurement.

The offsets of the Vstar versus robot measurements for most rows (except for Row 0) are quite large, suggesting point-to-point matching issues. But the SmartScope versus robot measurement can ensure a good point-to-point match between the two systems. This disagreement suggests that the robot measurement is likely to be at fault. To understand the cause of such behaviour, we checked the distance difference between the robot and SmartScope measurements in a point-by-point manner. If there is an accumulating effect on

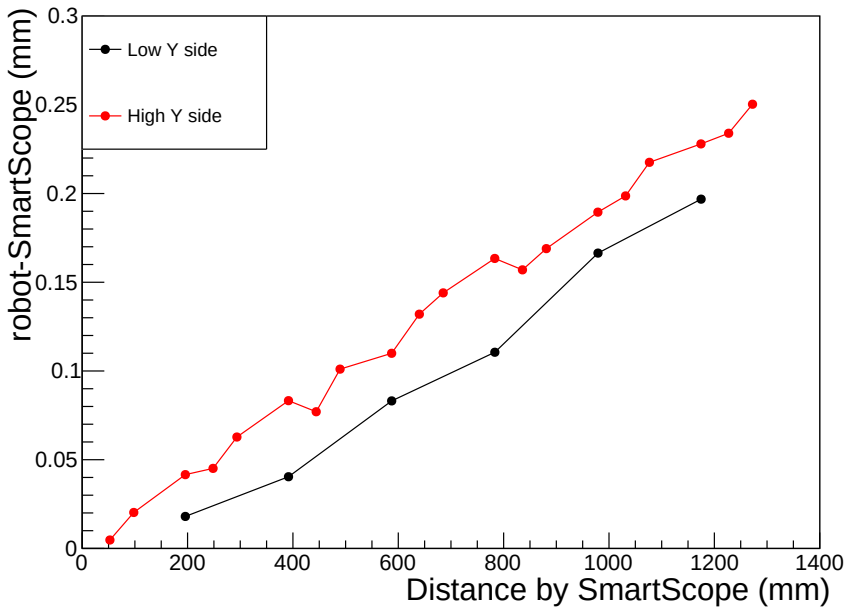
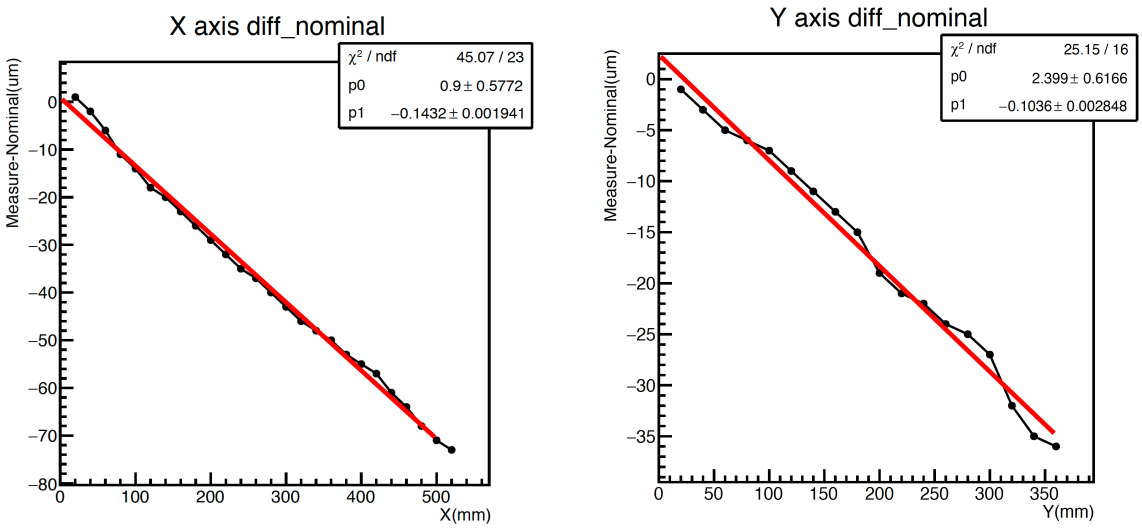


Figure 4.12: The difference between the robot and SmartScope measurements for CAD fiducials on both Y sides of a co-cured tape. X axis features SmartScope measurements and Y axis is the distance measured by the robot subtracting the distance measured by SmartScope. The low Y side is black and the high Y side is red

the differences, it would indicate the calibration being inaccurate. If there is a constant offset, the issue lies somewhere else. Fig. 4.12 shows that there exists an almost linear accumulating effect for the distance differences. It is safe to say the previous stage calibration was not accurate enough due to the possible distortion and stretch of the plastic film. It was believed to be accurately spaced and the calibration process was built upon this belief. However, there are scaling factors between the calibration film metric and the standard metric, which is presumably introduced when placing the plastic film.

To correct the error introduced by the calibration film, the calibration film was then measured with the SmartScope, which is the trusted system for such accurate measurements. The difference between the actual and nominal positions of each point on the film is studied, as examples in Fig. 4.13. The relation between this offset and the nominal positions are fitted linearly to obtain the average slope. This study is performed in both X and Y direction and two sets of slopes are generated, as shown in Fig. 4.14. There are different slopes for X and Y directions as shown in Fig. 4.14a and Fig. 4.14b. The average slope for the X direction is



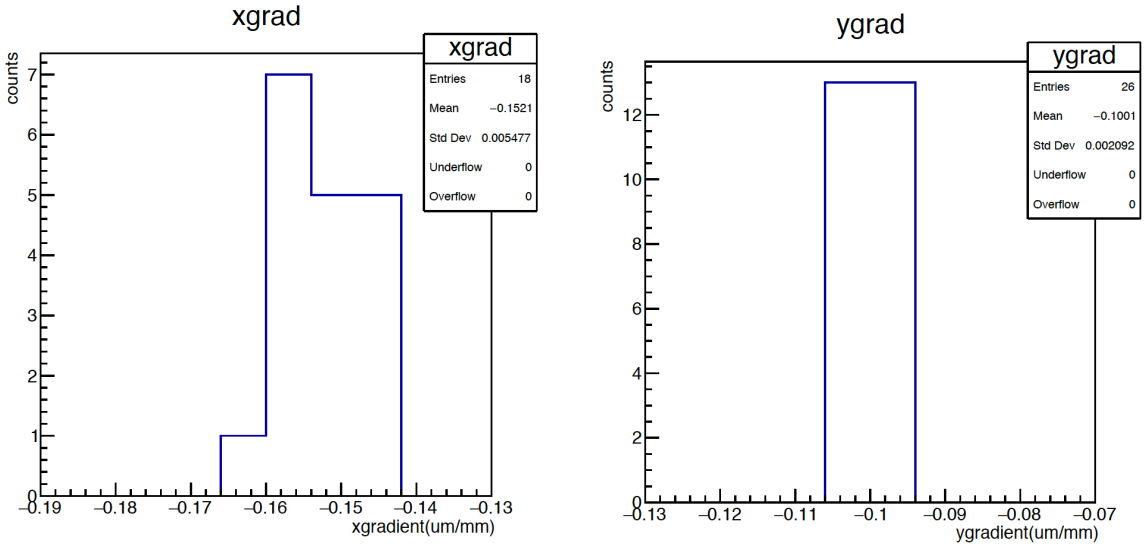
(a) The differences between measured and nominal positions of each point on calibration film in the X direction over the tested size of the film.

(b) The differences between measured and nominal positions of each point on calibration film in the Y direction over the tested size of the film.

Figure 4.13: The differences between measured and nominal positions of each point on calibration film in both directions over the tested size of the film versus measured positions obtained with SmartScope.

152.1 μm/m and for the Y it is 100.1 μm/m. The standard deviation of the slopes are 5.5 μm/m for the X gradients and 2.1μm/m for the Y gradients. This suggests that there are two scaling factors for the size of the film in X and Y directions. The actual distance is shorter than the nominal distance by 152.1 and 100.1 μm/m.

The calibration is corrected to take into consideration the scaling factors. The stage calibration process is repeated with the correct metric. Then the same co-cured tape is tested again to see how the robot is agreeing with the SmartScope after the corrections. Plots similar to Fig. 4.11 with SmartScope distance measurements on the X axis and robot measurements on the Y axis were produced and fitted with linear fit. The slopes between robot measurement and SmartScope measurement are 1.00007 for both Y sides of the measured tape, suggesting 70 μm/m difference. As shown in Fig. 4.15, the difference between two measurements still shows an accumulating effect but now within 70 μm/m. The calibration is still not perfect but it is good enough for the purpose of the robot as we need it to be within 100 μm/m. Fig. 4.16 extends the study to the Y direction. The distance between a point on low Y side and a corresponding point on high Y side is measured by both SmartScope and the robot and the



(a) Slopes in X direction distribution.

(b) Slopes in Y direction distribution.

Figure 4.14: The slopes obtained from linear fit to plots like Fig. 4.14a and Fig. 4.14b in both directions.

results are compared. It shows that they are mostly in agreement within 50 μm with one exception of 180 μm. The agreement is also within the 200 μm accuracy requirement in the Y direction. At this point the calibration of the robot is believed to be accurate enough for the purpose.

The calibration film used at this time was not fixed onto a rigid object. So even when this validation improved calibration performances, we did not know if the film stretch was the exactly same when it was measured by the robot and by the SmartScope. This issue was addressed in the following calibration campaign in 2021 when the film is fixed on a rigid object, thus limiting possible stretch changes.

4.2.2.2 2021 Calibration Validation Campaign

The robot underwent some hardware upgrades during the pandemic months. The calibration procedure was repeated and the calibration validation happened again.

The calibration film was again measured with the SmartScope system. To limit the stretch changes of the film, the calibration film was glued to a large aluminum plate in this calibration campaign, as shown in Fig. 4.17. Then the robot is calibrated to the measurement of the

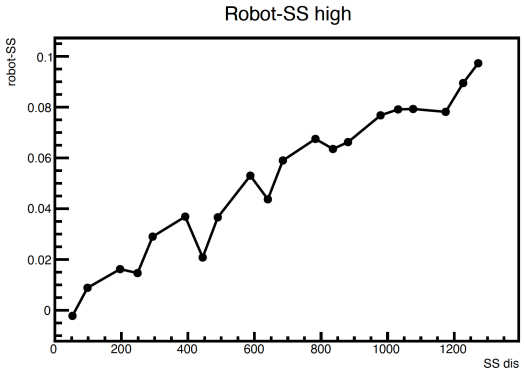


Figure 4.15: Distance differences measured by the robot and the SmartScope. The measured points are along the X direction of a co-cured tape. X axis shows measurements of distance between the first point and other points by SmartScope. Y axis is the differences between this distance measured by the robot and the SmartScope. Units in mm.

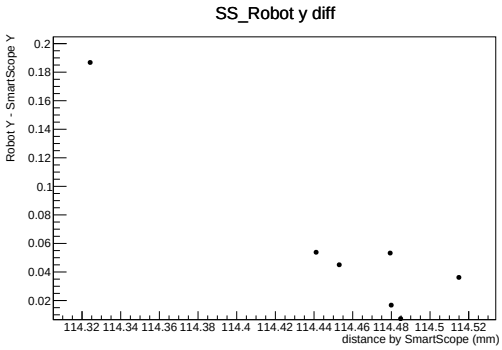


Figure 4.16: Distances between a CAD fiducial on low Y side and a corresponding CAD fiducial on high Y side are measured. X axis shows measurements by SmartScope. Y is the differences between this distance measured by robot and by SmartScope.

SmartScope.

To validate this calibration, three rows of circles were stuck to a plastic board, as shown in Fig. 4.18. The plastic board was then measured with both the robot and the Vstar system. The results are compared in a similar process as in the 2019 validation campaign (similar to Fig. 4.11).

Since the circles might not be very well aligned along the axes, measurement of distance between circles is a more reliable approach in comparing performances of systems. The relation between the robot distance measurements and the Vstar distance measurements is shown plotted as the X axis is the distance from the current measured circle to the first circle by Vstar system and Y axis is the same distance measured by the robot system. The offsets and slopes from the fit are shown in Table 4.3.

Fig. 4.19 shows a typical difference between robot and Vstar measured distances over the length of a bus tape. It can be seen that the robot and Vstar system agree very well. As shown in Fig. 4.19 and Table 4.3, the difference between robot and Vstar distance measurements is generally controlled within 100 μm/m, which is sufficient for the purpose of the robot.

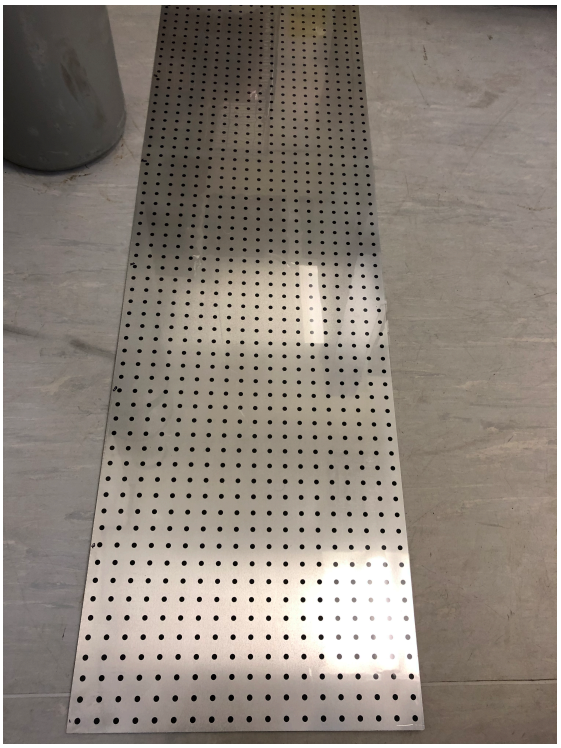


Figure 4.17: The calibration film is glued to a aluminium plate.

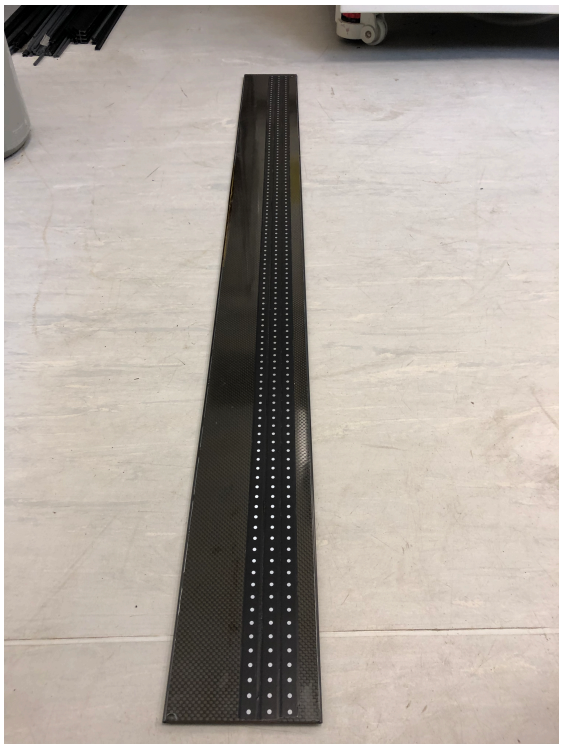


Figure 4.18: A plastic board with circles taped to it.

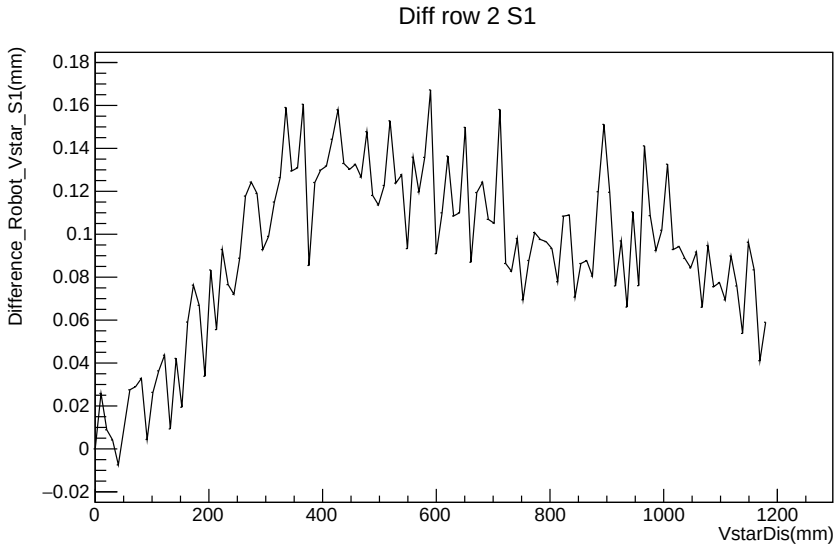


Figure 4.19: The distance difference between the robot and Vstar measurements over the length of a bus tape.

Stage	Row number	Offset (mm)	Slope	Slope Error
S1	Row 1	-0.0605	1.00013	1.08938×10^{-5}
S2	Row 1	-0.0736	1.00012	1.1016×10^{-5}
S1	Row 2	-0.0564	1.00006	9.3183×10^{-6}
S2	Row 2	-0.0634	1.00005	9.2682×10^{-6}
S1	Row 3	-0.0986	1.00005	9.8083×10^{-6}
S2	Row 3	-0.0925	1.0004	1.2593×10^{-5}

Table 4.3: Offsets and slopes for linear fits of Vstar and robot distance measurements in 2021 Validation campaign.

4.3 Tape Tester Robot Procedures

After a full set of calibration and verification, the robot is able to test bus tapes and give test results. The configuration and status of tapes are specified in the control panel. The control panel is shown as Fig. 4.20. There are four parameters used in the tests. Design types include the side and stave type, e.g. RHS LS for right-hand-side long strip tapes and which one of the several versions of the tape design was used. Then for the production stage, there are three stages for one tape, bare, co-cured and stave, corresponding to different tape situations, as discussed in Sec. 2.4.1. The manufacturer is the vendor that delivers the bare tapes. The serial number is used to track each individual tape.

The main panel mainly accounts for tape testing activities. The calibration procedures discussed before are included in the sub-panel accessible from the "Expert Mode" button.

The normal testing procedure starts from the "Apply" button, which read in the design information of the tape and the robot calibration data. Then the "Connect" button connect the operating system to other hardware systems, like the drives and the DVM. Geometrical measurements are achieved by "Measure Tape" and electrical testings are started with "Run Test".

Geometrical and electrical testing of tapes are the main purposes of the robot, which will be detailed in Sec. 4.3.1 and Sec. 4.3.2. In the case of unexpected issues, there are some auto-recovery procedures implemented as well.

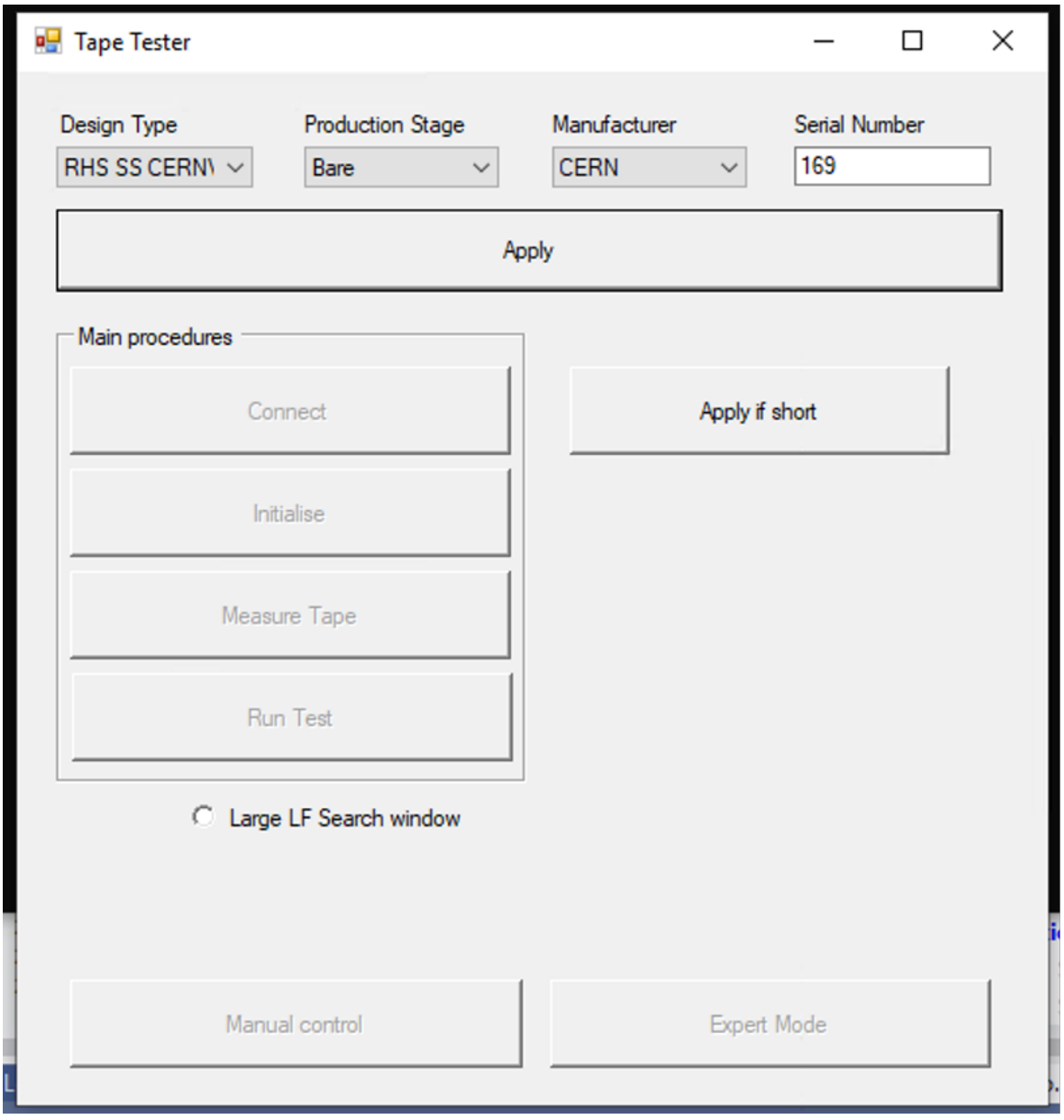


Figure 4.20: The robot control panel.

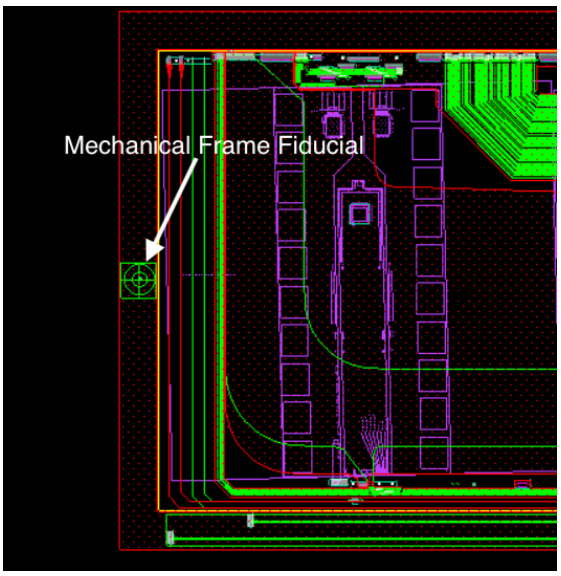


Figure 4.21: A mechanical frame fiducial on one end of the tape. Taken from the CAD file of a tape.

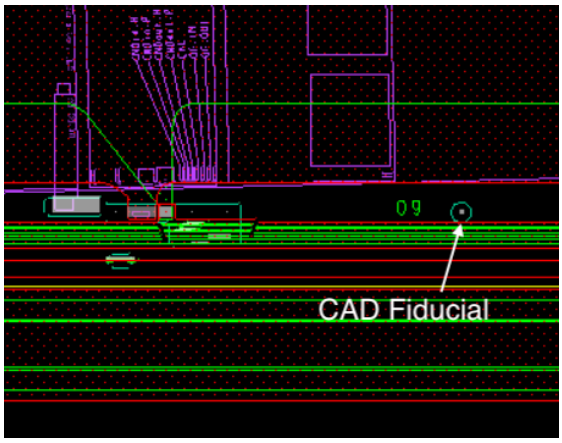


Figure 4.22: A CAD fiducial near a module.

4.3.1 Geometrical Measurements

To find tape wire-bonding pads with the robot system, fiducials are distributed along the tape on both Y sides of the tape. The two Y sides are named the low-Y and high-Y side as used in Sec. 4.2.2. The mechanical frame fiducials (MFFs) only exist at each X end of the tape, which is the reference point for the EoS card and module mounting as in Fig. 4.21. The line across the tape from one MFF to the other is the center line of the tape. The MFFs are used to make a hole and slot at each end of the tape. The hole is at the EoS end to ensure that the bond pads line up with the EoS. The stave assembly uses a dowel pin to locate this hole. This ensures that the bond pads in the EOS field are accurately located relative to the stave. The EOS card (see Chapter 2) is mounted relative to the mechanical features of the stave. The slot accommodates the fact that tapes are not exactly the nominal length. Dowel pins are used to locate the co-cured tape in the stave assembly jig. The lock points, which are used to attach the stave to the barrel, are added in the stave assembly jig. Modules are mounted with respect to the lock points. Therefore the center line between MFFs defines the reference frame for the stave. A technical drawing of a stave with modules, EoS PCB and lock points is shown in Fig. 4.25.

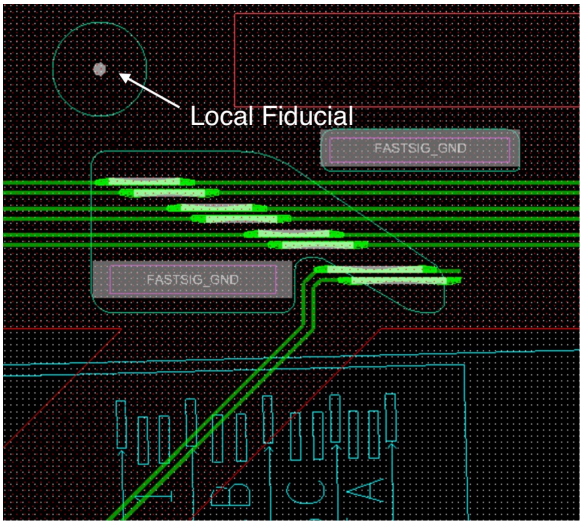


Figure 4.23: A local fiducial near a set of pads. After the robot finds the LF, it moves a known distance to find the pads.

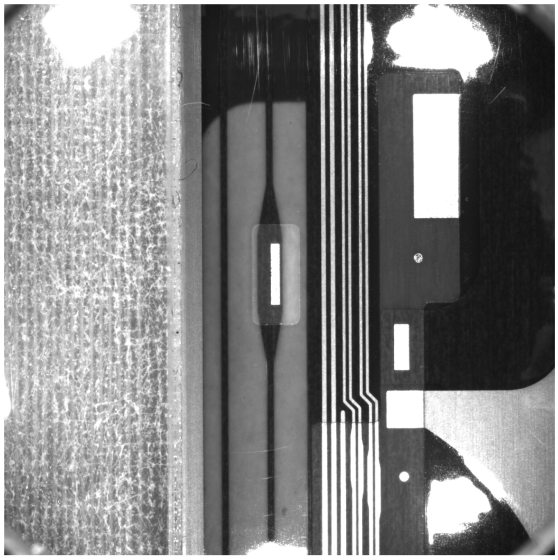


Figure 4.24: A typical bottom layer pad with poor alignment. The gold plated pad should lie in the middle of the HV line.

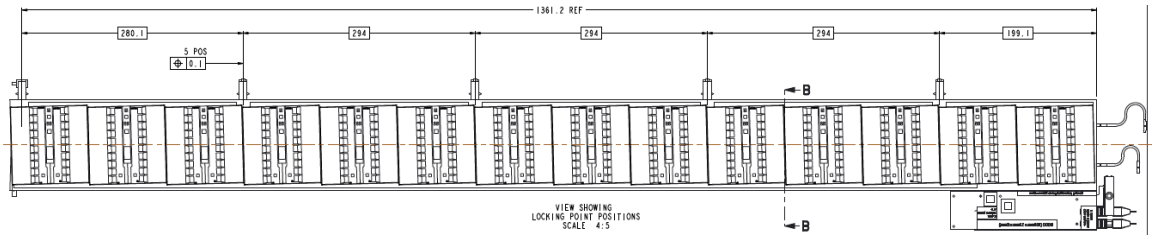


Figure 4.25: A stave with modules, EoS and lock points. Mechanical Frame Fiducials (MFFs) are removed on staves but they define the center line (dashed line) and define the reference system for loading the components. [56].

The CAD fiducials, which are larger fiducials that help locate the tape in the robot reference frame, can be seen from Fig. 4.22. This procedure allows for an offset and rotation. The local fiducials (LFs) are the smallest fiducials. They serve to locate sets of pads along the tape (refer to Fig. 4.23).

Due to uncertainties and limits in accuracy in manufacturing, the expected positions of pads are not necessarily their exact positions. LFs are then introduced to locate the pads, as shown in Fig. 4.23. After finding the LFs, the robot just needs to move a known amount of distance to find pads. To measure the alignment between the top and bottom layer of a tape for Altaflex tapes, pads with openings to the bottom layer need to be inspected as well. An example of such a pad is illustrated in Fig. 4.24 and it can be seen that the alignment is not ideal for this tape. This has to be checked with visual inspections before the robot testing as discussed in Sec. 2.4.1. Visual inspections should also include the plating quality and look for possible contamination.

When running the test, the robot finds the measured tape in the robot space by finding large CAD fiducials (shown in Fig. 4.22) with Stage 2 and locates pads that it needs to measure later in tests by finding local fiducials (LFs, shown in Fig. 4.23) with both stages. Even if the robot is exactly calibrated, each tape still has different distortions (will be detailed in Sec. 4.3.3) at the level of a few hundred microns. As the bond pads of the narrow tracks are only 150 μm wide, the robot needs a correction to the nominal pad locations to find them properly. This is achieved by measuring LFs. The robot camera takes a photo of the LF and the software finds the center of the fiducial circle. This is then used to generate an offset to the nominal pad locations. The LFs can be measured to very high precision, detailed in Sec. 4.3.3.

Then mechanical frame fiducial (MFF, shown in Fig. 4.21) finding process was implemented with requests from the EoS card mounting team. The MFF finding process is performed with both stages as well.

After these measurements, some brief analysis is carried out to check the sanity of the measurements and show the quality of the measured tape. The analysis and its indications will be detailed in Sec. 4.3.3.

If the fiducial findings are successful, the test carries on to electrical tests, which includes open/short circuits, resistance and HV leakage current tests.

4.3.2 Electrical Tests

If the tests in fiducial finding are successful, the robot starts to test for continuity for all pads along each network. An open circuit would indicate a broken track. An unusual high resistance reading could be a sign of contamination or poor quality plating. After the continuity tests, the robot checks for possible short circuits between neighbouring [2] lines. The HV power lines provide bias voltages for sensors. "HV leakage current" tests check for excessive current leakages between HV lines and their neighbours.

4.3.2.1 Resistance Measurements

The multi-drop lines (for distributing CCR signals) along the tape have pads for wire-bonding. Resistance is measured to check for open circuits or excess resistance caused by poor plating quality or contamination. The relation between resistance and length for the narrow lines is plotted, the slope of which is used as a proxy for the copper thickness and track width. Due to the differences in manufacturing techniques, for CERN tapes, it is particularly useful to check the copper thickness, which can vary if the electroplating is not well controlled. For Altaflex tapes it is more a check of the track width.

The robot is connected to a DVM as discussed before and by probing on pads, the resistances along the line between the pads are measured. The functionality of calculating expected resistance at each point is also implemented. With the characteristics of the material and width of the lines known, the gradient of the resistance increase can be calculated, and noted as k_R. The calculation allowed for the effect of etching narrowing the widths of the tracks. It assumed a trapezoidal cross section and that after etching the slopes of the sides were 45 degrees. The lengths along the tracks can be obtained from the tape design files. With the gradient and the lengths known, the expected resistance values can be calculated. To take into account the 10 $\%$ uncertainty of copper thickness in tapes, we define the maximum

[2] neighbouring for short circuit tests: the lines that are spatially closest to each other within the same layer.

resistance R_{max} value as:

$$R_{max} = k_R * 1.1 * length + A \tag{4.1}$$

, in which A is an empirical constant. R_{max} is calculated for each measured point and is compared with the actual measured resistance. A in Equ. 4.1 is determined by a study on the distribution of the difference between measured and nominal expected resistances calculated with k_R on 31 example tapes in 2019. An example of a data line is given in Fig. 4.26, where 2 Ω can contain all "good" measurements on this line. The ground lines and OF lines are relatively wide or short so they have a small resistance compared to others, as can be seen in the example given in Fig. 4.27. 2 Ω is sufficient to cover the resistance distribution for "good" measurements for lines with small resistance. So A is determined to be 2 Ω empirically.

With criteria in Equ. 4.1, it is possible for us to raise an error flag for excessive resistances and not to falsely flag acceptable measurements. If one point is flagged to have excessive resistance, then the re-measurement procedure is triggered.

The re-measurement is composed of five steps. The robot first raises one of the probes and presses 50 μm more onto the pad to check if there is a contact issue. Then it will step in four directions by 50 μm and probe down to see if the probe is not in the center of the measured pad. Eventually the smallest measurement of the five is accepted as the actual result. If the final result of the re-measurement still fails to pass the R_{max} criteria, then the first probe goes back to the original position. The same process is repeated with the second probe. If all attempts fail, the tester will be informed and asked to check this manually. Tapes that fails this test procedure are marked as "red" or failure. Tapes that required this procedure to achieve a good reading are flagged as "amber". The ones that pass tests without this recovery procedure are "green" or good tapes. The number of measurements flagged as amber on each tape can be used as a check on quality. The full test time ranges from 45 minutes to an hour for a "good" tape that requires few re-measurements. If manual checks are required because of genuine problems with the tape of the robot itself, the time needed will be longer.

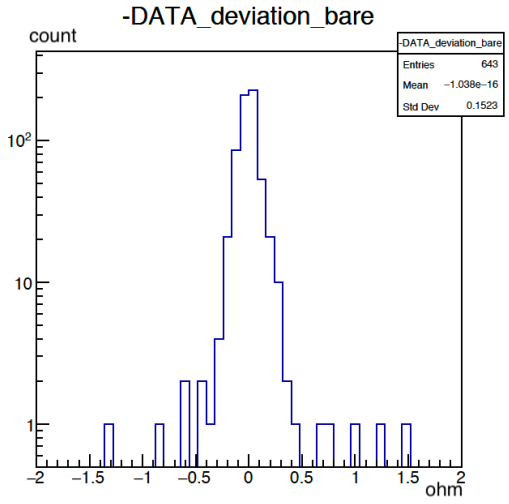


Figure 4.26: The difference between measured and nominal expected resistances calculated with k_R in a data line on 31 example bare tapes.

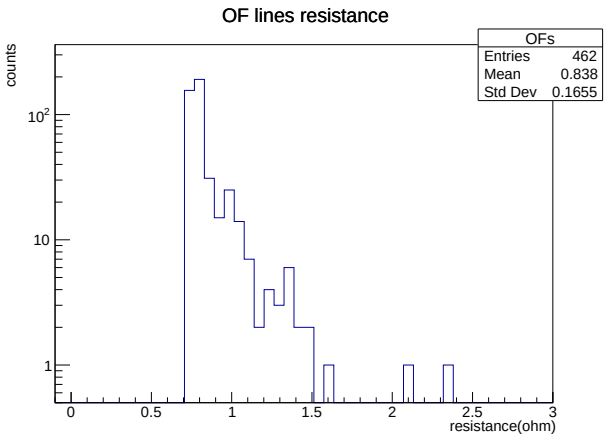


Figure 4.27: Resistances of OF lines on 31 example bare tapes. OF lines are short and have the same length, thus forming the peak in the distribution. Two of these measurements failed the 2 Ω cut.

This method is extended to all resistance measurements with tapes. With the 31 example tapes, the distribution of the difference between R_{max} and $R_{measure}$ is shown in Fig. 4.28. There is a peak around 2 Ω, corresponding to the 2 Ω headroom given in the R_{max} calculations. This validates the efficiency of the R_{max} method. There have been changes in tape deigns since but the resistance factors have been stable. So the 2 Ω choice is still satisfactory.

4.3.2.2 Short Circuit Tests

The DVM connected to the probes also looks for possible short circuits between neighbouring lines. Due to reasons that could range from dust in the robot space to DVM connection issues to probing inaccuracies, in the robot system, sometimes there are spurious short circuit measurements. "Spurious short" is a specific test error, where a short circuit measurement is recorded but it is actually not short circuit. For a given short measurement, there are two ways of knowing if this short is real. The first way is to do a manual retest with a hand-held meter, which takes more effort. The hand probing can introduce dents into the bond pads, which jeopardizes the wire bonding. The second way is to automatically identify the line with the short measurement and redo the electrical tests on the said line. Two different approaches were attempted to automate the procedure. One of them is to redo the nets

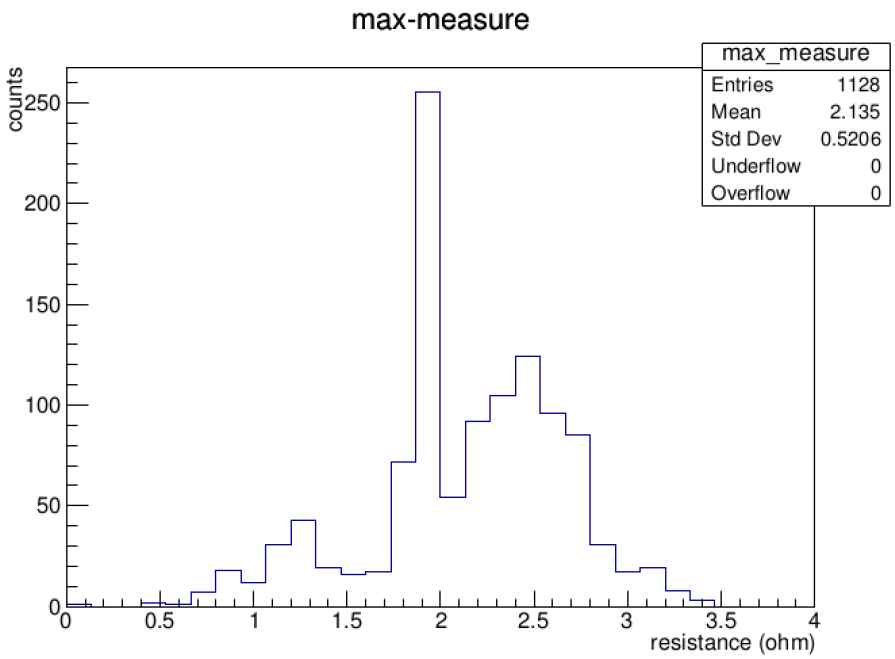


Figure 4.28: the difference between the calculated value of R_{max} (as in Equ. 4.1) and the measured resistance $R_{measure}$.

with short circuits before ending the test. However, this method can not get rid of spurious shorts. The spurious shorts are still reported as shorts, which does not help the situation. The other approach is to generate a shortened design file including only the lines that have short circuits and then restart the test with the shortened design. This method is tested to be able to get rid of the spurious shorts. So it is adopted.

To resolve the spurious short issue, the test procedure is slightly modified. If a tape is tested to have short circuits, a shortened tape design file only containing the lines with shorts is created by the end of the test. Then the operator starts a new test. But instead of the "Apply" button, the test starts with the "Apply if short" button (shown in Fig. 4.20). Then the test carries on as usual but in the end of the test, the new test results of the lines with shorts replace the original test results in test report files that will be discussed in later sections. It will ensure the short reports are real.

4.3.2.3 HV Leakage Current Measurements

The HV test measures the leakage current from HV pads to neighbouring pads. The leakage current is the current between two lines. A hard short circuit would be detected by the short circuit test but the HV test is sensitive to contamination resulting in small leakage currents. This is checked by High Voltage Insulation Resistance (HVIR) measurements. HV is applied to all HV pads and the leakage current is measured to neighbouring lines. The real leakage current should be very small (< 1 nA). A significantly higher value might indicate contamination between the pads from dirt, grease, carbon fibre dust etc. There is a danger that a large leakage current might grow with time. It is therefore important to verify that there is no significant leakage. From measurements with a commercial HVIR meter, it is known that the real leakage currents are below 1 nA. However, we need to automate these measurements using the robot and it is very difficult to make such precise current readings. Therefore a maximum leakage current was defined to be 20 nA, with reasons explained below. There is not enough room in the Y direction on the tape to always maintain the safe clearance between HV lines and low voltage lines. As discussed in Sec. 2.4.1, the HV lines have to provide HV up to 500 V. The specifications for 500 V states that the clearance should be greater than 0.8 mm (1.8 mm) under a cover layer (on the surface). Therefore in order to validate out designs, the HVIR is tested at 1 kV. The purpose is to detect anomalous leakage current. The source of the noise in the measurement is the robot drives. It is tested that when the drives are switched off the readings go down to about 1 nA. Since the drives have to be on during testing, some noise is to be expected. The procedure was later improved to minimise this noise. An RC filter was added to reduce the noise. In addition, some digital filtering was applied in the DVM by performing a running average of multiple measurements. The performance of HV measurements is expected to be improved.

With noise minimized, the leakage current at 1 kV for a good tape is measured to be within 1 nA as well. However, there is always noise present with our test setup to increase the measured leakage current. Also it takes time for the connection to stabilize as proved in Fig. 4.29. The leakage current of interest is the stabilized one. As can be seen from Fig. 4.29, the leakage current curve generally stabilizes after 10-15 s. Due to the limitation of the test,

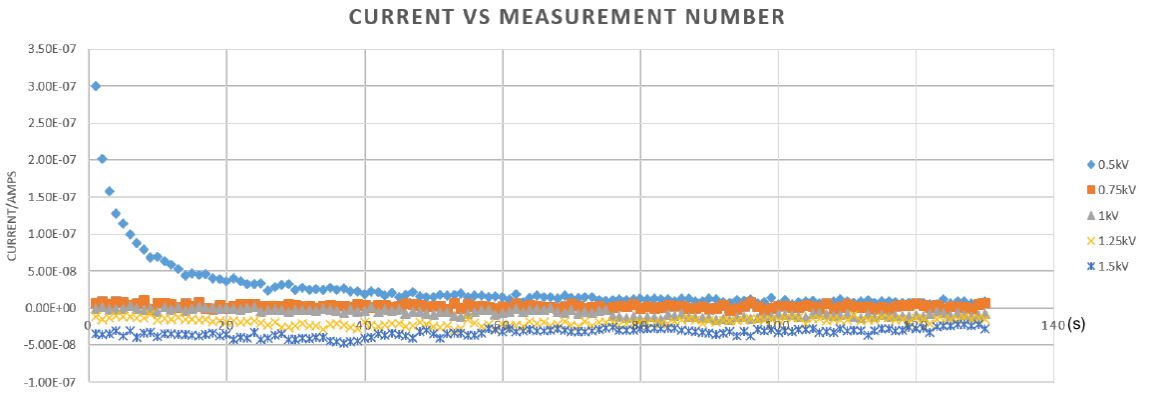


Figure 4.29: Leakage current in relation to time at different voltages.

we require the leakage current at 1 kV to be less than 20 nA to call it good. Even if there is no HV injection, there is still a small leakage current due to noise and capacitance discharge. As a first step for leakage current studies from previous studies, a scan of various voltages is performed and currents measured are shown in Fig. 4.29. Leakage currents at each point are the stabilized currents in the curves. A fit is applied on the voltage versus current relation. With the fitted slopes and offsets, leakage currents at each voltage are calculated.

To speed up the test, only two points, 0V and 1 kV, are taken for the real-time tape testing. The baseline noise current is measured at 0 V and then the current is measured at 1 kV. Since all lines on the tape are in a similar environment, it is safe to assume that the 0 V measurements are the same for all lines. This improvement is developed by our American colleagues at Yale and later adopted by the Oxford tape tester robot. Real leakage current at 1 kV would be the current at 1 kV with noise taken out. For each current measurement, the functionality finds the leakage current when the connection stabilizes within 2 nA by comparing the average of five measurements with the previous average of five. One reading is obtained per second. This method is applied to replace the old one of making numerous current measurements at each voltage point, which can both ensure that the connection is relatively stable as well as improving test efficiency. As shown in Fig. 4.29, the HV needs to be held at least 15-20 seconds to allow it to settle. This result is verified by the current test method, as each measurement at high voltage requires around four groups of five. This improvement was implemented in 2019 in Oxford. The leakage current measurement

process needs an even longer settling time when the DVM is set to "resistance" mode before and then changed to "current" mode. The process is improved by not changing the DVM back to "resistance" mode if the next measurement is also a HV leakage current measurement. When measuring very low leakage currents, there is sometimes negative leakage currents, which is not physical. The negative readings are later removed with an added low-pass RC filter and digital filtering in the DVM. These two improvements are also implemented by colleagues at Yale. These optimisations reduced the time taken for HVIR from several hours in 2018 to the average of 50 minutes in 2021. The performance of this test is studied in Sec. 4.3.3. It is proved that the test can still identify non-functioning tapes with this simplification.

Eventually after the full testing process, the full tape analysis is called and produces the tape test result that include all important performance information of the tested tape.

The robot is relatively stable and reliable and we have measured tapes of all stages, the performance is studied and results are presented in Sec. 4.3.4.

4.3.3 Tape Test Report

After the robot finishes the tape testing routine, a brief analysis is performed to show the quality of the tested tape. [57] The test report obtained is then saved to the ITk production database. With all tapes tested, statistical studies are carried out that indicate the quality of the batch of tapes that a manufacturer provides.

For each tape, a tape quality analysis report is generated at the end of the test. The top part of the report shows the name and status of the tested tape and tells the viewer if the tape has passed or failed the tests. Then it presents various test results of the tape, starting from the short circuit test plot. Short circuit plots, example of a "good" tape as in Fig. 4.30, show if there exist short circuits on the tape, featured by an abnormal small resistance. The HV tests are represented by a list of leakage currents between HV lines. Results over 20 nA are marked as failure. A typical tape that passes the HV test has a leakage current distribution like the one in Fig. 4.31.

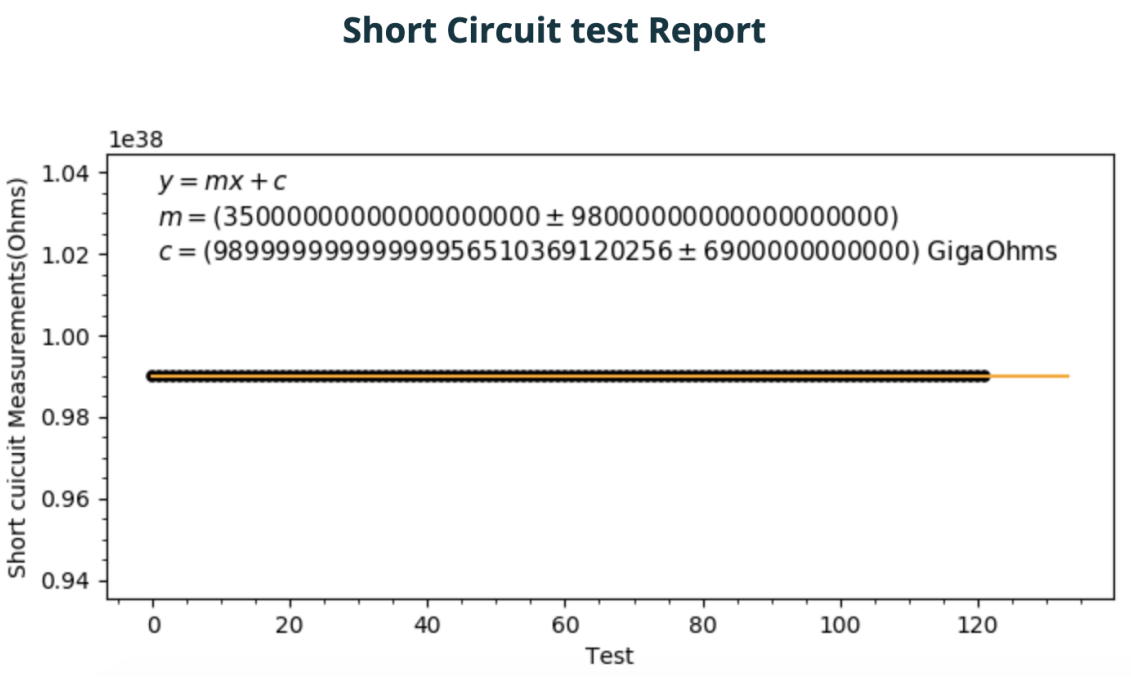


Figure 4.30: Short circuit test, featured by large resistance measurements. The X axis is the position of the short test pads along the length of the tape. These are the (unphysical) values returned by the DVM for open circuits.

General resistance measurements are presented as plots of resistance against length of the line. An example of a data line is shown in Fig. 4.32. The red line in Fig. 4.32 represents the maximum acceptable resistance described in Equ. 4.1. The black points are the resistance measurements along the data line. The yellow line is a linear fit on the data points. If any of the data points fall above the red line, indicating excessive resistance or open circuits, this line is marked as failed the test. Open circuits can be caused by micro-cracks in the line material. Excessive resistance would indicate bad surface plating of the pads or contact issues of the robot. Sometimes etching issues can also cause excessive resistance issues. These need to be manually investigated to be sure of the causes.

"Stretch" and "distortion" are another feature of interest on bus tapes, as discussed in Sec. 2.4.1. Due to the tape accuracy requirements, the difference between the longitudinal length of a tape and the designed length has to be within 1 mm/m. The change in longitudinal lengths per meter is defined as "stretch". Negative stretch values mean that the actual tape is shorter than the design and positive stretch values mean a longer tape. In the orthogonal

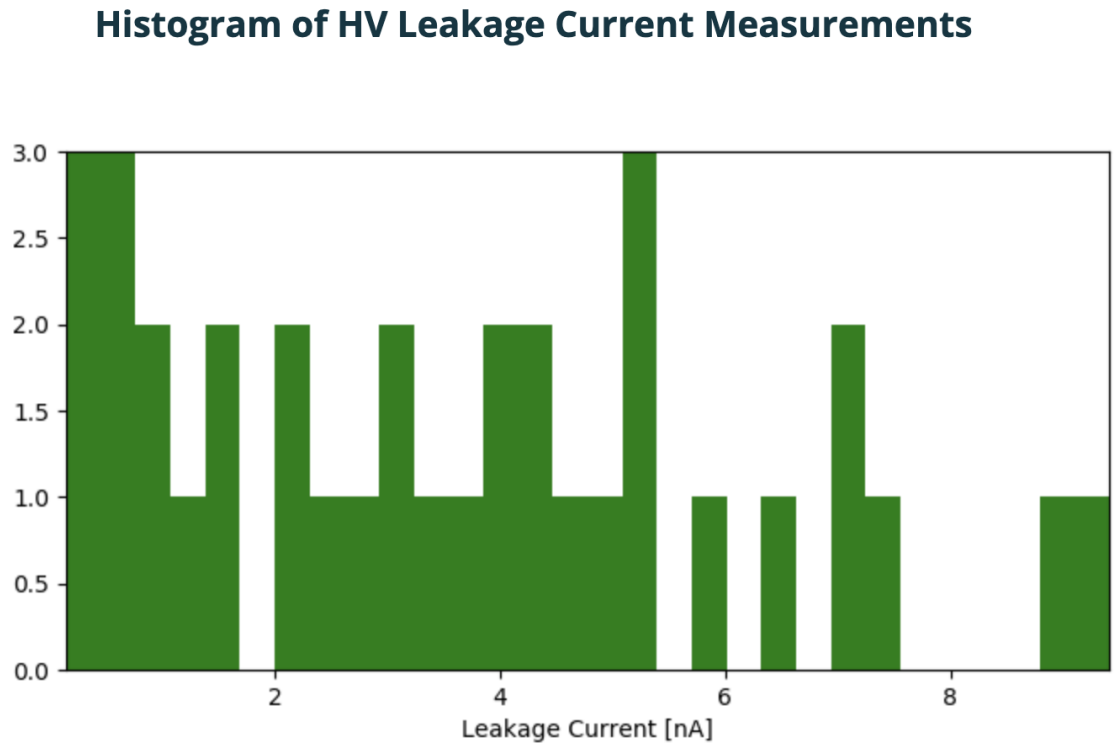


Figure 4.31: HV leakage current distribution of a "good" tape, with all leakage current below 20 nA.

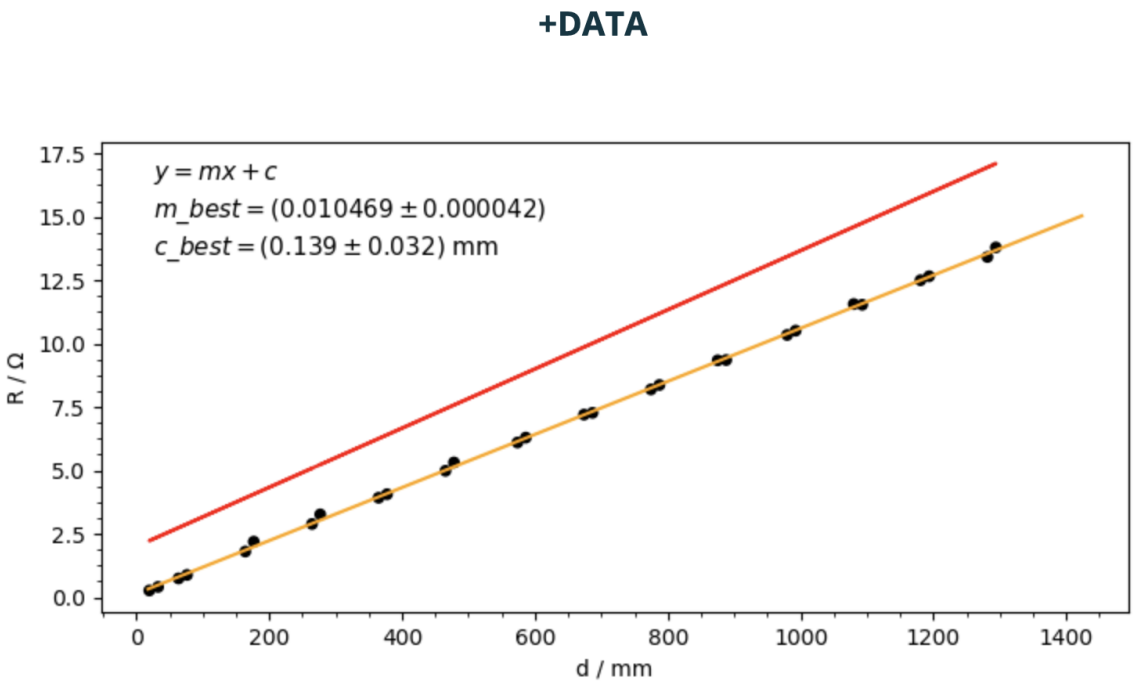
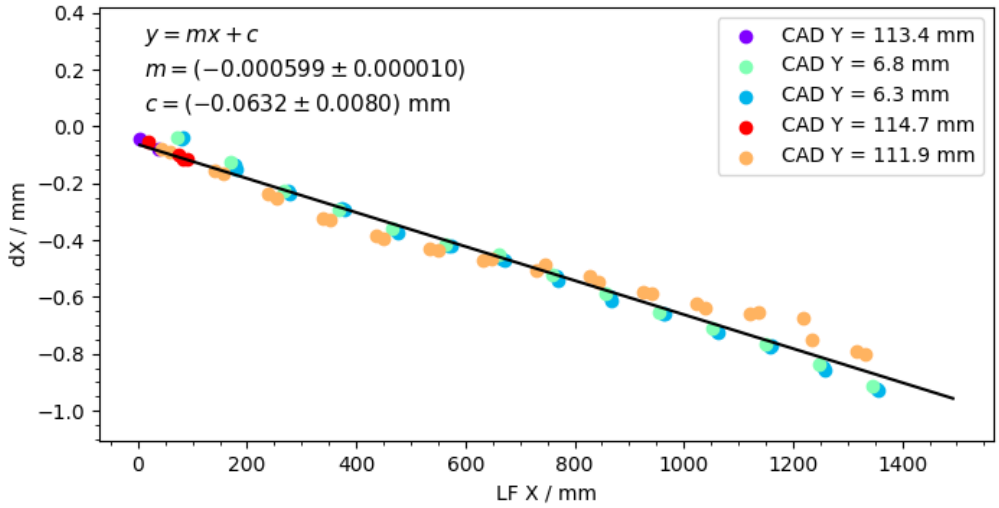


Figure 4.32: A typical data line with the length of the full tape. The red line is the maximum nominal value as calculated in 4.1. A linear fit is performed on the data points in this plot.

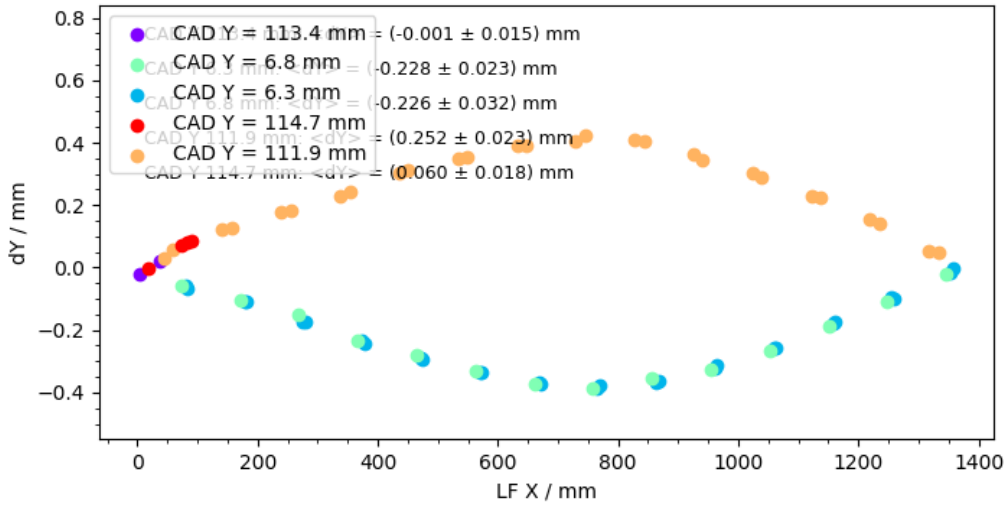
direction, the tape can have "distortion", which can be caused by the way the tape is held down on the table and manufacturing effects. If the tape is not laid in a straight line and have curved shapes (for instance a banana shape), the distortion is introduced when laying the tape on the robot chuck. If the tape itself is not manufactured to be straight enough, the distortion is a real feature of the tape. Since bare tapes are quite flexible, the stretch and distortion on a bare tape is more likely to be artifact of the tape placement. However, distortions after co-coure status can result in not enough clearance on the edges of the tape. When tapes are made into staves, tracks that are close to the tape edges, especially some HV lines, will have a larger risk to be accidentally cut, resulting in failures in stave making. In order to avoid failure, tape test results also include "stretch" and "distortion". Both CAD Fiducials and LFs can be used for this purpose. An example of stretch and distortion featured by LFs is shown in Fig. 4.33. The tape is shorter than its nominal length and has some distortion in the Y direction. The tape full width does not change.

According to the tape design, the LFs are expected to be in a certain position (x_{design}, y_{design}). The actual position where the robot finds them could be different, noted as $(x_{measure}, y_{measure})$. In Fig. 4.33a, dX = $x_{measure} - x_{design}$. The MFFs define the middle line of the tape and Y is the distance from the LF to the middle line. Similarly for each LF, there are two Ys of interest, y_{design} and $y_{measure}$. dY = $y_{measure} - y_{design}$ in Fig. 4.33b. Positive dY shows that this LF is further away from the middle point than designed to be and negative dY means that it is closer to the middle line. The MFF and LF layout is illustrated in Fig. 4.34. The two Y sides of the tape show different shapes. This suggests that the tape has a "banana shape". On one side the LFs are closer to the middle line while LFs on the other side are further away from it. This result is shown after the geometrical measurements to the operator as a sanity check. If the LF measurements are not reasonable, the test should be stopped and the issue needs to be investigated.

In order to minimise the distortion in the Y direction, a new co-cure jig was introduced as discussed in Sec. 2.4.1. This greatly reduces the distortion effect. Tapes with distortion larger than 600 μm are considered failures. There have been no failure due to distortion in the Y-direction since the introduction of these solutions.



(a) dX along the length of the tape. dX = $x_{measure} - x_{design}$



(b) dY along the length of the tape. dY = $y_{measure} - y_{design}$. The tape is further away from the middle line on one side and closer to it on the other side. The total width is consistent.

Figure 4.33: Stretch and distortion report example.

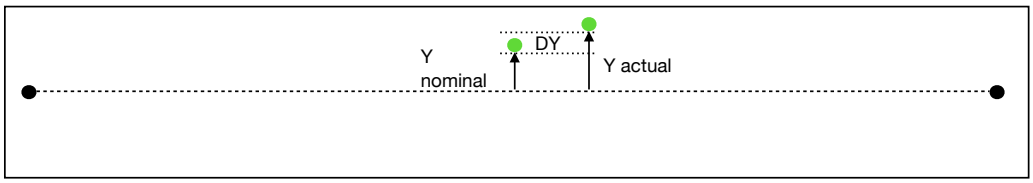


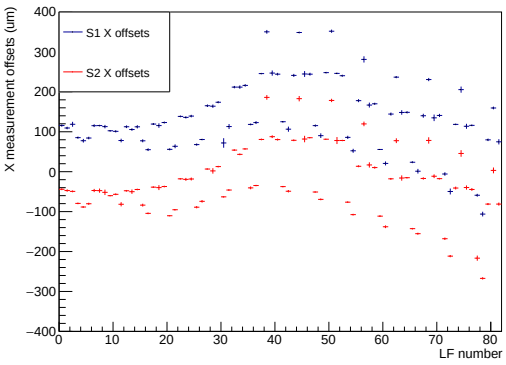
Figure 4.34: Illustration of two MFFs (black circles) and one LF (green). The distance from where the LF should be according to design to the line between MFFs is Y_{design} and the distance from where the LF is actually found to the line between MFFs is $Y_{measure}$.

4.3.4 Robot Reliability Studies

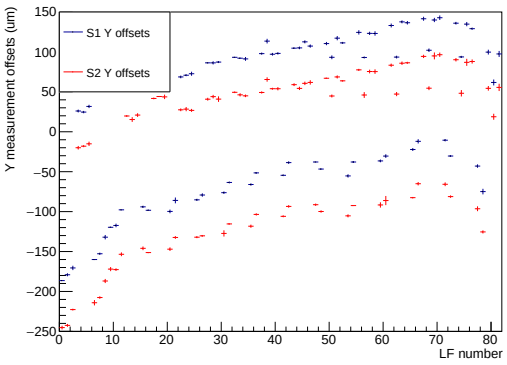
The tape tester robot is a key part of quality control of the bus tapes. The reliability of the robot is of vital importance to the production of useful strip barrel staves. To ensure the robot can deliver reliable test results, it needs to find all the pads and do the correct measurements. As discussed in Sec. 4.3.1, LFs are a crucial feature in tape measurement. Whether LFs are measured reliably and reproducibly is of great importance. Automatic recovery procedures like "stepping around and press harder" for excessive resistance measurements and "shortened design file" for potential short circuit measurements are introduced to ensure the failures that the robot reports are real. In this section, the reliability on LF finding is studied.

The Local Fiducials (LFs) measurement is performed with the robot cameras and tests are done with both cameras. For the same tape, six repetitive tests were carried out with both stages. The coordinates of each LF in each stage coordinate system are obtained. In this way we get the position of each LF in the coordinate system of each stage.

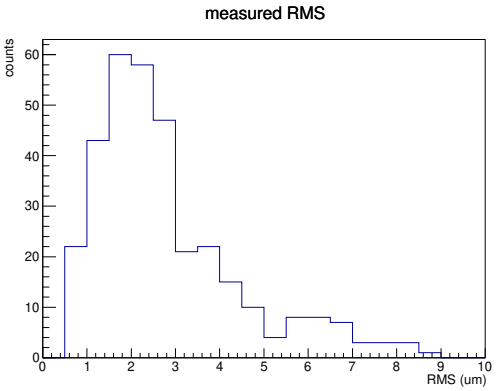
Fig. 4.35 gives the test result analysis. The errors shown are the standard deviations of the six measurements. These plots show that the measurements with two stages are in agreement with each other as the shapes of the curves in each plot are the same. Both X and Y distributions are smooth curves, for instance in Fig. 4.35a and Fig. 4.35b. It can also be seen that there exist eight points that do not fall on the smooth curve. They are the bottom layer LFs that can have a slight difference with top layer LFs in spatial distribution as this is



(a) Stage 1 and Stage 2 LF measurement of offsets from their nominal positions in the X axis. The vertical error bars are the RMS values for the six measurements of each LF.



(b) Stage 1 and Stage 2 LF measurement of offsets from their nominal positions in the Y axis. The vertical error bars are the RMS values for the six measurements of each LF.



(c) Distribution of RMS values for the six measurements of each local fiducial for the two stages and two axes.

Figure 4.35: Repetitive measurements of LFs on the same tape with both stages. The X axis of these plots is the LF number, 86 in total on this tape. The Y axis is the offset from the measured position to the nominal position of the LFs in the coordinate system of either stage with unit in μm. The offsets in the X axis is shown in (a) and the offsets in the Y axis is shown in (b). The distribution of all errors in (a) and (b) is shown in (c).

an Altaflex tape and there are LFs on the bottom layer. For an Altaflex tape, the alignment of the two layers are examined by how well they agree with each other. This alignment is studied with bottom pad measurements. The errors of these measurements are limited within 10 μm for each stage, both in X and Y directions, which satisfy our needs in terms of spatial measurement accuracy. The errors of all four situations have a distribution shown in Fig. 4.35c. The peak value is 2 μm, which confirms the accuracy of the measurements. The curves group into two families according to these plots. They show the LFs distributed on the two sides (low-Y and high-Y side) of the tape.

There are constant offsets between two stages for both X and Y coordinates (see Fig. 4.35a and Fig. 4.35b). This is expected as the two stages use two sets of coordinate systems that are calibrated to each other with offsets (introduced in Sec. 4.2). To support this point, one test is chosen to check the measurement differences in both axes between the two stages. The results are given in Fig. 4.36. As can be seen, the assumption of a constant offset is true of both X and Y axis, which proves the point.

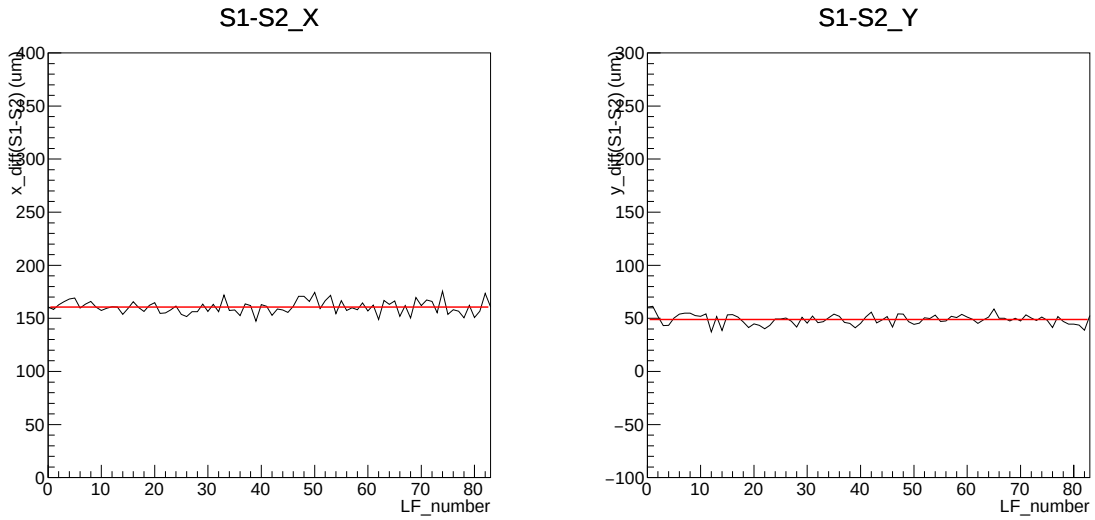
It can be seen that the robot fiducial findings are quite stable. Along with the auto-recovery methods, the robot performance is robust enough for production demands.

4.4 Pre-production Tapes Statistics Studies

Pre-production stage includes 5 % of the whole amount of tapes. This is to ensure the designs and procedures are validated before full production. The vendors that deliver the tapes are also chosen with contracts. Two companies are used, with one of them being the back-up. CERN is the main vendor for the bus tape production and Altaflex [3] is the back-up vendor.

Historically, the original bus tapes were produced by Altaflex. When Altaflex withdrew from the project, they outsource the tape production to an unknown Chinese company. It is called Altaflex Outsource since then. When this happened, tapes began to be made by the

[3] Altaflex is not the actual vendor. The project is outsourced to an unknown vendor in China while our contact is Altaflex (California). This vendor is named as Altaflex or Altaflex outsource for brevity.



(a) Differences between Stage 1 and Stage 2 measurements of X axis coordinates. The red line features the mean value. The error on the mean value is 0.66 μm.

(b) Differences between Stage 1 and Stage 2 measurements of Y axis coordinates. The red line features the mean value. The error on the mean value is 0.53 μm.

Figure 4.36: Differences between measurements of two stages in both axes on a same tape within one test. The X axis of these plots is the LF number, 86 in total on this tape. The Y axis is the difference (S1 - S2) of measured position of the LFs in the coordinate system of either stage. (a) is the difference (S1-S2) of X axis coordinates and (b) is the difference of Y axis coordinates.

CERN workshop as a backup.

Both manufacturers use double sided Cu/Polyimide/Cu substrate. As discussed in Sec. 2.4.1, Altaflex Outsource uses laser ablation to make openings and CERN uses a mechanical mill. CERN uses vias to connect the top and bottom copper layers.

The Taiflex cover layer material used by Altaflex was tested for radiation tolerance (500 kGy (Si)) in 2018 and it passed. Tests with Taiflex material were performed again in 2022 and repeated tests showed that it always failed the radiation tests. It is therefore concluded that Taiflex have changed their cover layer glue so that it is now no longer radiation tolerant. Similar radiation tests are performed for samples made using the Krempel cover layer used by CERN and it was very radiation tolerant. The US groups are investigating whether Altaflex Outsource can make tapes using the Krempel cover layer as a backup.

Since there is a possibility of failure in each stage of a tape, one tape is tested at each one of the stages. There are 115 tapes tested by the time of this analysis, 105 of them are bare tapes, 8 of them are co-cured and 2 are stave tapes. Altaflex delivered 73 of all tapes and CERN delivered 42. The tapes are tested at two separate sites with two individual tape tester robots. One site is at Oxford and the other is at Yale University in the US. 62 tapes are tested at Yale, 61 bare tapes and one co-cured. 53 tapes are tested at Oxford, with seven co-cured tapes and two staves.

The next sections discuss the qualities of all tapes and then tapes from each vendor. Several failure modes are also discussed.

4.4.1 Tape Statistics: Bare

There are 105 bare tapes tested in total by the time of this analysis. On a bare tape, there are a few features to study in the tape statistics, including the HV leakage current, the difference between measured resistance and maximum acceptable resistance (featured as the red line in Fig. 4.32), the difference between measured resistance and the fitted expected resistance (featured as the yellow line in Fig. 4.32), the average gradient of the yellow fitted line in Fig. 4.32 and the gradient difference between lines on the two Y sides of a tape.

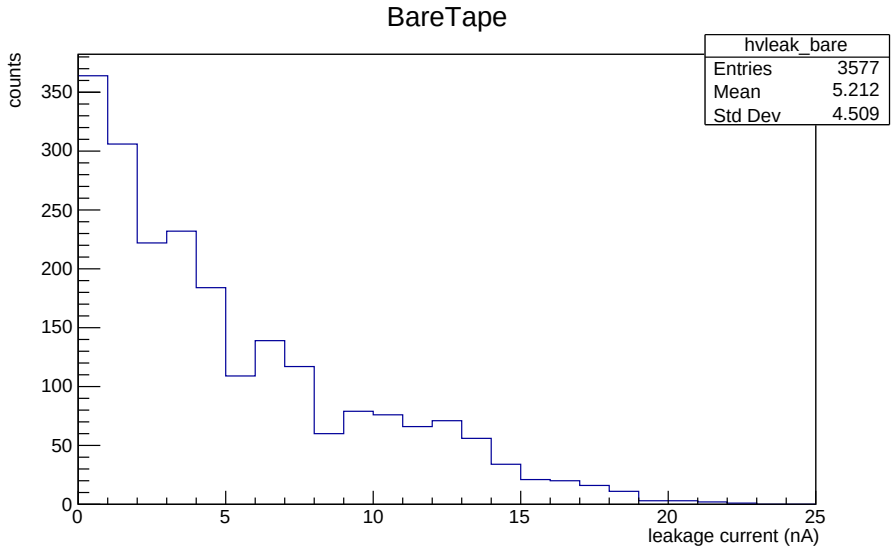


Figure 4.37: The distribution of HV leakage current measurements on 105 bare bus tapes

The distribution of HV leakage current, in Fig. 4.37, shows all the leakage current measurements on these tapes. Tapes with leakage current above 20 nA are marked as failures. There are a few tapes with leakage current above 20 nA. But this is an artifact from the Yale robot. The grounding for the HV measurements was not ideal when measuring a few tapes. This issue was fixed soon after. Four tapes were marked as false failures due to this reason.

Fig. 4.38 is the distribution of the differences between the measured resistance and the maximum acceptable resistance (the red line in Fig. 4.32). The measured resistances are safely below the maximum acceptable resistance for most tapes. There are underflow measurements, meaning there are excessive resistance measurements in some tapes. This failure is most commonly among CERN tapes as some of them have a plating issue. CERN tapes are made from base material with 5 μm Cu and electroplated up to a nominal thickness of 17.4 μm before etching. This is to allow plated through holes for the vias that connect the top and bottom Cu layers. The uniformity of the electroplating over the areas depends on how well the electrodes are distributed and how good the contacts are.

The excessive resistance measurements in CERN tapes show that there are uniformity issues of the Cu thickness after electroplating. This happened on one batch of CERN tapes. The situation has been greatly improved by more care with the distribution of electrodes used

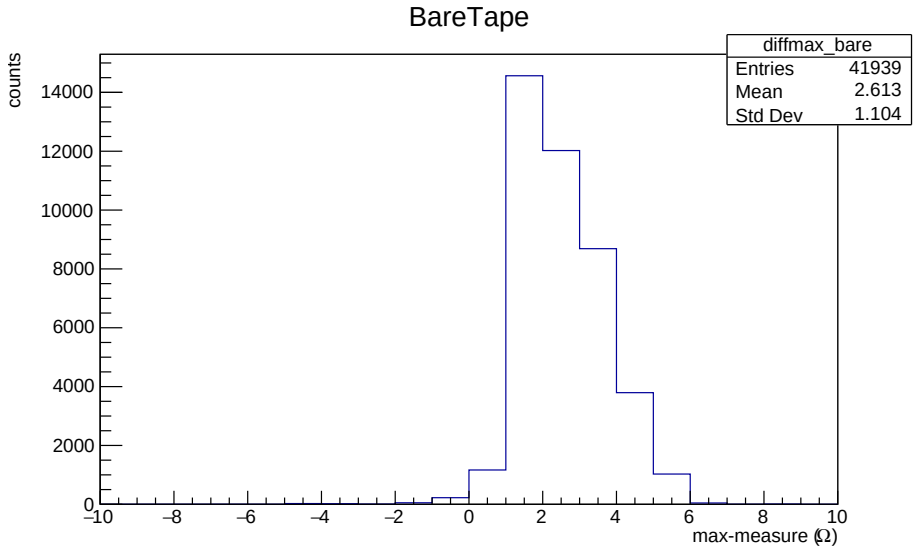


Figure 4.38: The distribution of the differences between the maximum and the measured resistance acceptable resistance (shown as the red line in Fig. 4.32).

in the electroplating process. The Cu thickness after electroplating and before etching is measured by CERN over the full area using very precise resistance measurements to determine the resistance per square and hence calculate the Cu thickness.

12 of the 36 bare CERN tapes failed because of this issue. The thickness of the line plating is not uniform in different regions of the tape, resulting in excessive resistance and inconsistency in gradients of lines on one side of the tape and lines on the other.

Another way to examine the quality of tapes is to study the gradients in the yellow line in Fig. 4.32. Since the width of the lines also influences the resistance gradient, a more sensible measure is gradient $\times$ width. The distribution is shown in Fig. 4.39. The distribution is narrow, indicating overall good consistency in resistance distributions. However, for some CERN tapes, the average gradient of lines on the low Y side (also called the bottom side) of the tape and the average gradient of lines on the high Y side (also called the top side) of the tape are not quite consistent. This can be seen in Fig. 4.40. While the Altaflex tapes, as shown in Fig. 4.40 are very consistent over the two sides, some CERN tapes show a clear difference between the two positions. This is also caused by the plating issues.

Similar with Fig. 4.38, the difference between the resistance measurement points (black

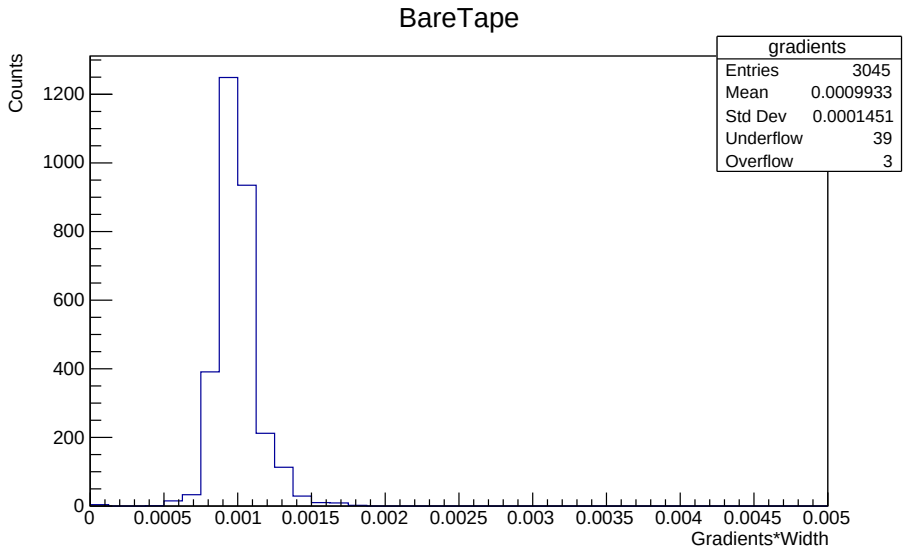


Figure 4.39: The distribution of the gradient from the fitted line in Fig. 4.32 $\times$ line width. The unit in the X-axis is Ω/mm.

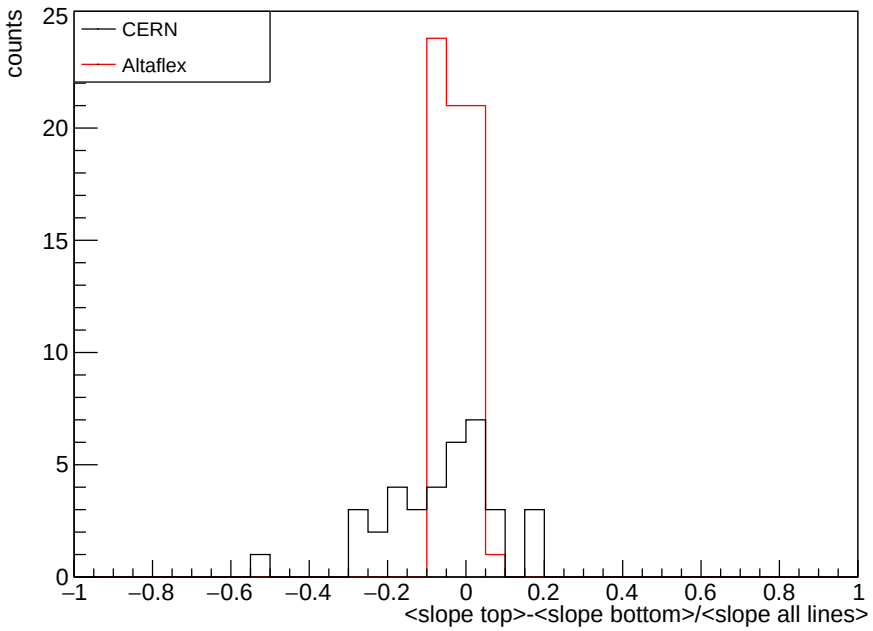


Figure 4.40: The fractional difference between the average gradient of lines on the bottom side of the tape and the average gradient of lines on the top side of the tape for CERN (black) and Altaflex (red) tapes.

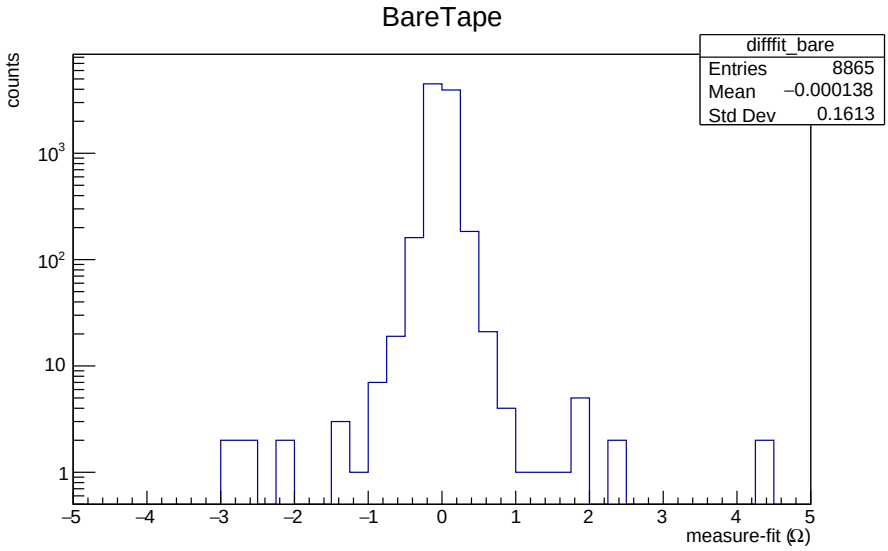


Figure 4.41: The distribution of the differences between the measured resistances and the expected resistances from the fit function (the yellow line in Fig. 4.32).

points in Fig. 4.32) and the expected resistances from the fit function (yellow line in Fig. 4.32) can show the consistency of the resistance distribution along the tape. The distribution is shown in Fig. 4.41. It is a relatively narrow distribution centering in 0, which shows that the resistance data is quite well represented by the linear fit. Most of the distribution is contained with $\pm$ 0.4 Ω.

Apart from the leakage current and resistance-related issues, there are also short circuit-related failures found in bare tapes. The real short circuits are mostly found among Altaflex Outsource tapes. Some lines are shorted by plating issues. Eight out of 73 Altaflex Outsource tapes suffer from this failure. Altaflex Outsource now understands this issue and the plating process is changed to eliminate this problem for future reference.

However, the Oxford robot sometimes reports spurious shorts. These are failures that can not be verified with manual tests with hand-held meters. Two tapes are recorded with false failures. The automatic recovery method introduced in Sec. 4.3.2.2 are introduced to resolve this issue.

There are also two bare tapes are marked as failures because of human error from the robot operator. In total, the bare tape performances are summarized in Table 4.4. 30 out of 105

bare tapes are marked as failures. 21 of them are real failures. The yield for CERN tapes is 67 % and the yield for Altaflex Outsource tapes are 87 %. Both vendors are notified of their respective issues and the same problems will be prevented in production. The overall yield for all pre-production tapes so far is 79 %, which is less than ideal. But since both vendors are working on solving the problems, the yield will be demonstrated to be significantly higher than this for the final batch of pre-production tapes. The robot design is now also more robust against spurious error results for future reference.

	Real Failure		False Failure			
Vendor	Excessive Resistance	Plating Spillage Short	Excessive HV leakage current	Spurious Shorts	Human Error	Total
CERN	12	0	0	2	0	14
Altaflex	1	8	4	1	2	16

Table 4.4: Failures in bare tapes. The total number of bare tapes is 105.

4.4.2 Tape Statistics: Co-cured Tapes and Staves

There are eight co-cured tapes and two stave tapes tested so far. The eight co-cured tapes are made from bare tapes that passed robot testing. Four of them are marked as failures. One of them shows signs of spurious open circuits that are not confirmed by manual tests. The other three are real failures.

The causes of real failures range from errors in the tape design to accidents in co-cure manufacturing. The tapes have openings on the bottom cover layer to the bottom Cu pads on a “ground” line to ensure the carbon fibre is shorted to “ground”. On the RHS LS Altaflex layout there was a mistake in the layout so there was an opening from the LV Return on the bottom cover layer. This resulted in a short circuit after co-cure. The design has been fixed for future production. Another failure was caused by the protection tape that was applied during the co-cure process. Some of the plating came off when the protection tape was peeled off. This is believed to be an one-off situation.

A pair of the four co-cured tapes that passed robot testings are made into a stave. Both of them survived the process. With the data available in the ITk database at the time of this

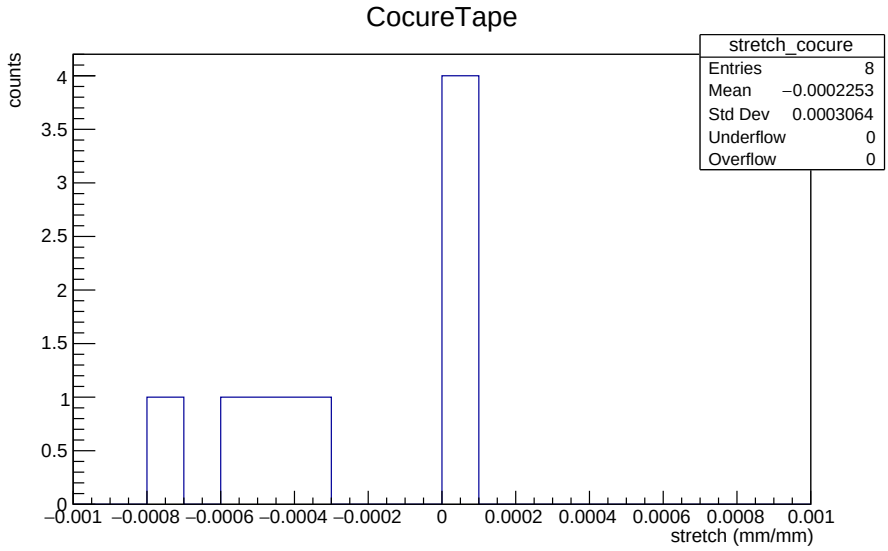


Figure 4.42: Distribution of "stretch" gradients from co-cured tapes. The requirement is that the stretch should be below $\pm$ 0.001 m/m.

analysis, there is one fully functional double-sided stave.

As discussed in previous sections, the geometrical features like distortion and stretch (Fig. 4.33) are only taken into consideration from co-cured stage onward. "Stretch" is the gradient of the linear fit in Fig. 4.33a. "Max dY" is chosen to be the parameter for distortion (as featured in Fig. 4.33b). It describes the largest absolute value of dY found along the tape as in Fig. 4.33b. The distribution of "stretch" is shown in Fig. 4.42. A "good" co-cured tape should have stretch within $\pm$ 0.001 m/m. The distribution of "max dY" for all the co-cured tapes are shown in Fig. 4.43. To ensure the quality of the stave making, the "max dY" should be within 0.6 mm. As shown in Fig. 4.42 and Fig. 4.43, the eight co-cured tapes so far all passed the geometrical requirements.

4.4.3 Summary

As shown in the discussion above, the robot is ready for production, with calibration validated and spurious failure recovery automation implemented.

As for the tape production, CERN is chosen as the baseline choice. CERN will be used for production if a good yield is achieved on 24 pre-production tapes. CERN are completing

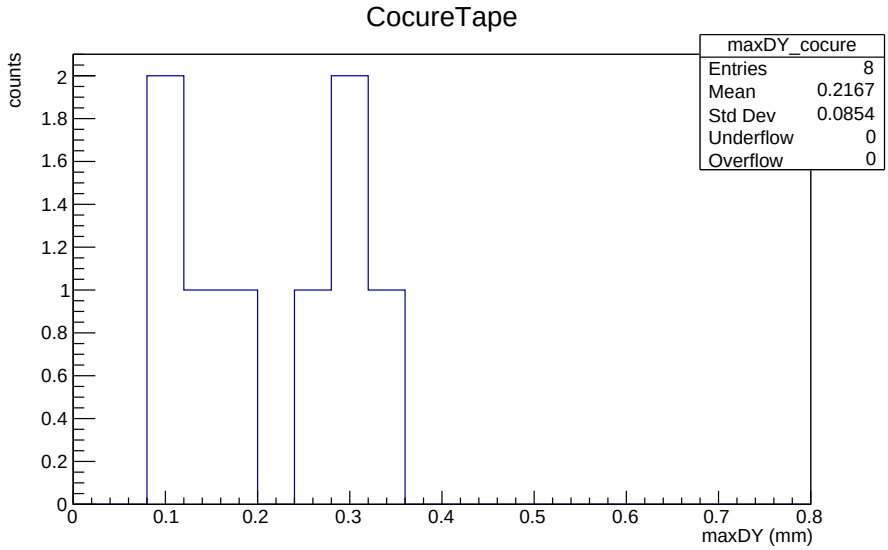


Figure 4.43: Distribution of "max dY" from co-cured tapes. The "max dY" should be below 0.6 mm.

the final 8 tapes out of a batch of 24 that will be used to assess the quality and yield. If the results on the batch of 24 pre-production tests of CERN tapes are good and good module performance is achieved with a stave made with CERN tapes, production could be started.

Work is underway with Altaflex Outsource to make new test samples for radiation testing using the same cover layer material as CERN. If these tests are successful, a sample of tapes with this material could be made by Altaflex Outsource to serve as a backup option.

5 | VTRx+ Reliability Test

As discussed in Chapter 2, the VTRx+ is a high-speed optical transceiver. It provides for optical links to and from the counting room from and to the EoS. The VTRx+ module is based on a radiation-hard laser diode driver (LDQ10) and transimpedance amplifier (GBTIA) ASICs, and commercial VCSEL and a *p-i-n* photo-diode (PD) component. The GBTIA ASIC also has a discriminator embedded.

The VTRx+ contains 4 VCSEL channels, either one or two of them are used for ITk strips. Two channels are used for SS staves per side and one channel for LS staves per side. This is to accommodate for the larger data rate for SS staves. The device is pig-tailed and the five fibres are terminated in an MT-12 connector [1]. The MT-12 will connect to a fibre ribbon terminated with an MTP [2]. These optical fibres and connectors connect the VTRx+ to off-detector electronics where optical transmitters and receivers serve as interface to FPGAs off-detector. The VTRx+ is compatible with lpGBTx on the EOS boards. The logical diagram is illustrated in Fig. 2.11 in Chapter 2. There is an optical coupling unit that turns the vertically-emitted light from the VCSEL 90° and focuses it into the optical fibre. [28] The space on detector for the VTRx+ modules is tight so the component is required to have a low-profile with a 20 mm $\times$ 10 mm $\times$ 2.5 mm limit, 2.5 mm being the height. The VTRx+ module is designed to operate over a wide temperature range (-35 to 65 °C).

As will be discussed in Sec. 5.1, VCSELs are very sensitive to humidity and a dielectric layer is added to avoid humidity ingress. Since the VTRx+ will serve the ATLAS detector for the whole lifetime when the ITk upgrade is installed, the reliability of the VTRx+ transceivers is of vital importance. This chapter covers the reliability test of the VTRx+ transceivers. The main area of concern are the VCSELs but other components can also fail for different reasons, e.g. the optical coupling might degrade with time.

[1] MT-12 connector: 12-way array connector with fibres on a 250 um pitch in a ferule
[2] a high performance optical fiber connector designed for high mechanical and optical specs

5.1 Introduction

VCSEL, vertical-cavity surface-emitting laser, is a semiconductor laser diode with laser beam emitting perpendicularly from the top surface. [58] The schematics of a typical VCSEL is illustrated in Fig. 5.1. [58] The inner cavity and active region contains Multiple Quantum Wells (MQW) [3]. The light emission is from excited states of the MQW. The inner cavity mirrors are distributed Bragg reflectors (DBRs). The layers are composed of an alternating sequence of high and low refractive index material layers. GaAs and GaAlAs are usually used. The DBRs below and above the MQWs act as mirrors with high reflectance. The active layer as a whole act as a laser. The active layers are surrounded by electrically conductive layer stacks, which form the laser mirrors to achieve optical feedback. Electrical current is injected from the Ohimic contacts, as illustrated on top of Fig. 5.1. In the demonstration, the current is confined to the center of the inner cavity. This is often achieved with aperture. VCSELs are usually designed to have emission wavelength of 850-980 nm. VCSELs without any aperture need very large currents to be above laser threshold and can therefore only be operated at very low temperatures or in pulsed mode. The laser threshold is reduced by funnelling the current into a smaller area and by confining the emission with a waveguide [4], which is the cause for adding aperture [58] [59].

As shown in Fig. 5.2, the aperture can be achieved via oxide or proton implants, which are the most commonly used. The aperture is not only necessary to achieve low laser thresholds, it can also help with modal stability and lowering jitter at higher data transmission rate (above 2 Gbps) [60].

There are two common ways of making the needed aperture, proton implant or oxide, as illustrated in Fig. 5.2. Earlier aperture was usually done with proton implants and this method was proven to have good reliability. But the oxide implants are smaller and therefore better for high speed VCSELs. It also introduces fewer optical losses in the cavity. So oxide aperture is now dominant in commercial VCSEL production despite that it does not often achieve the same reliability as proton implant. [59] Thermally stable oxide layers have been

[3] A quantum well is a potential well with only discrete energy values.
[4] a structure designed to confine and direct the propagation of electromagnetic waves into desired direction

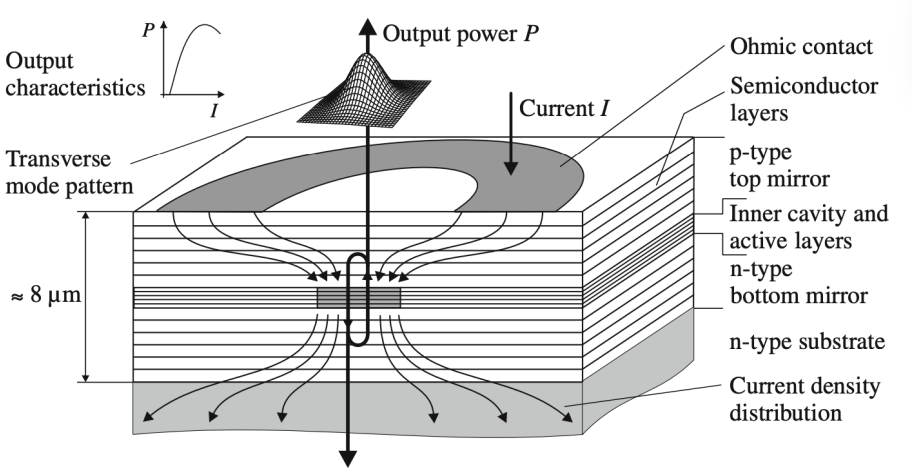


Figure 5.1: Cross section of a typical VCSEL. [58]

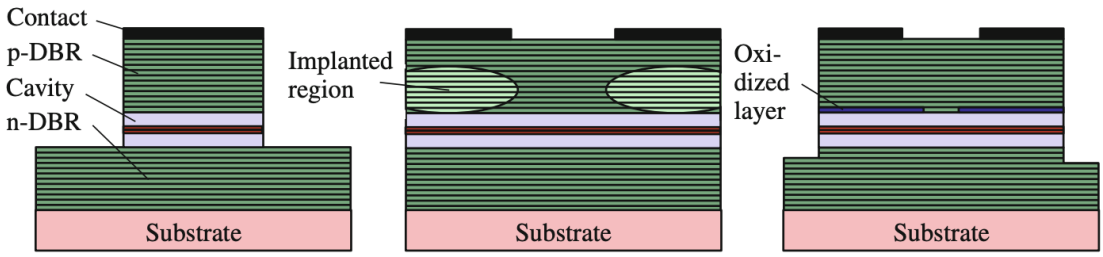


Figure 5.2: Main approaches to achieve current confinement in VCSELs. Air-post or mesa-etched (left), proton-implanted (center), and oxide-confined VCSEL (right). Proton implants and oxide-confined are the most commonly used. [58]

developed and applied in VCSELs. [61] And there is continuous effort in making oxide aperture with better reliability. The oxide layer is now considered to be generally stable and reliable according to industrial studies. [62] But the VSCELs using oxide aperture are known to have a premature failure mode in presence of water vapour due to corrosion failure. [63] They can also have the delamination issues between oxidized layer and the semiconductor layers. Cracks form on the edge of oxide aperture due to moisture. If there is damage in the oxide aperture, the moisture will get to the active region, reducing lifetime of the VCSEL.

The lifetime of VCSELs is very sensitive to temperature and humidity (as will be discussed in Equ. 5.1 and Equ. 5.2). To ensure the performance of the optical link until the end of life, a reliability test with controlled humidity and temperature is planned. In reliability theory, there are usually three modes of failures classified as infant mortality, random failure and end-of-life failure. Infant mortality can be excluded by "burn-in" tests and the rate for random failures is quite low. The reliability test focuses on the end-of-life failures. The main motivation for these studies is to validate the VTRx+ performances to ensure they can last for lifetime of the ITk.

The aging effect when the temperature is up to 150 °C was tested in industrial settings with VCSELs with proton implant aperture. [64] The lifetime of VCSELs scaling with temperature was found to fit with models featured by the Arrhenius equation

$$\frac{MTTF(T_1)}{MTTF(T_2)} = \frac{exp(E_A/(k_B T_1))}{exp(E_A/(k_B T_2))} \tag{5.1}$$

, where MTTF(T) stands for the Mean Time to Failure at the temperature of T and E_A is an activation energy. Activation energy is the minimal energy needed for the chemical or physical transformation to happen. Typical E_A for the oxide VCSEL used in earlier ATLAS SCT is about 0.53 eV according to previous ATLAS related studies. [65] To achieve the aging process desired, the temperature and humidity chosen for the test is 85 °C and 85 % relative humidity as the industrial common practice. [66] Relative Humidity (RH) is a ratio of the amount of atmospheric moisture present relative to the amount that would be present if the air were saturated. The 85 °C temperature gives a large acceleration factor compared

to the very low temperature at which the stave works in the HL-LHC.

In many cases, it is possible to place the VCSEL in a hermetic package to prevent humidity ingress. However, this is not compatible with the tight space constraints in ATLAS. Dielectric barrier layers, such as SiO_2, $Si_3N_4^-$ or SiO_xN_y, are thus introduced to cover the VCSEL and stop water vapor from coming in. [65] The ATLAS operates in a very dry environment but the VCSELs will be operated in normal laboratory humidity for a significant period of time. A dielectric layer is used for humidity resistance in VTRx+ VSCELs so that they can survive normal laboratory humidity for 10 years. [67] But the dielectric barrier can have pinholes or coverage defects. According to previous studies [65] and Eq. 5.1, the equation for median lifetime is

$$\textbf{Median time to failure} = f(I)f(T)f(RH) = Ce^{\frac{E_a}{k_B T}}e^{-A_{RH}RH} \tag{5.2}$$

,in which lifetime is a function of bias current, temperature and relative humidity (RH). The bias current was proven to be relatively unimportant based on previous studies. [65] So the current dependency is not taken into consideration to first order. There are three parameters of importance, the scaling factor C, the activation energy E_a and the humidity dependence A_{RH}. Given the dependency of VCSEL lifetime on temperature and humidity, stress tests on these two factors are important in VCSEL reliability studies.

There is usually a layer of epoxy over the oxide aperture. When the oxide aperture is already weakened by the water vapor corrosion, the epoxy layer can accelerate the cracking process as well. The coefficient of thermal expansion (CTE) of the epoxy can introduce mechanical stress on the oxide aperture. The coefficient of moisture expansion (CME) induces hygroscopic stress as the epoxy absorbs moisture at the same time. [65] In the VTRx+ VCSEL, there is not epoxy over oxide aperture, therefore this factor would not contribute to the VTRx+ failure in this study.

The dielectric barrier is designed to have good protection against humidity. But this protection can be reduced by thermal stresses and 85 % RH is added as a test against the humidity protection as well. In all, 85 °C/85% RH is considered a very harsh environment

for VCSELs and devices that are still alive after 1000 hours are believed to be able to function reliably for 10 years in HL-LHC.

The first test is the eye diagrams of the VTRx+ that are used in this study. An eye diagram is an oscilloscope display where a digital signal from a receiver is repetitively sampled and sent to the vertical input. [68] The data rate of the signal is then used to trigger the horizontal sweep. The eye diagram is usually a tool for the performance evaluation of the combined effects of channel noise [5], dispersion [6] and inter-symbol interference [7] of a pulse-transmission system. An open eye [8] pattern corresponds to minimal signal distortion. This suggests the BER in this system should be very low. If a clear open eye is not present, the VTRx+ can not be used in reliability test. All VTRx+ used showed clear eye diagrams, with an example eye diagram shown in Fig. 5.3.

With previous VTRx designs, several reliability tests were performed. The VCSEL current was set by a simple DC power supply and a series resistor. VCSELs are coupled to fibres and no driver electronics were used. The VCSELs are tested by measuring the DC power from the fibres during accelerated aging tests. The VCSEL spectrum before and after the accelerated aging was measured with an Optical Spectrum Analyser.

The reliability of the transceivers was studied with Bit Error Ratios (BER) and Optical Modulation Amplitude (OMA) scans. In telecommunications, the OMA is the difference between two optical power levels, like the high and low levels from a laser. The BER is the percentage of bits that have errors relative to the total number of bits received in a transmission. As discussed in Sec. 5.2, pseudo-random bits are sent to the VCSELs and what is sent back is compared with the bits sent. The attenuator is used to tune down the light intensity. For each attenuator setting, we measure the optical power, calculate the OMA using the extinction ratio and measure the BER. This is repeated at different attenuator settings until the BER falls below 10^{-9}. This is to show how high the power needs to be

[5] in telecommunications, the ratio of the noise in the channel at any point in a transmission system to an arbitrary reference level.

[6] dispersion means the light pulse spreading out in time as it propagates down the fibre.

[7] a form of distortion of a signal when one symbol interferes with other symbols. A symbol is a waveform or state that lasts for some time in a communication channel

[8] an open eye in eye diagram describes a good operating region where the high and low levels are clearly separable.

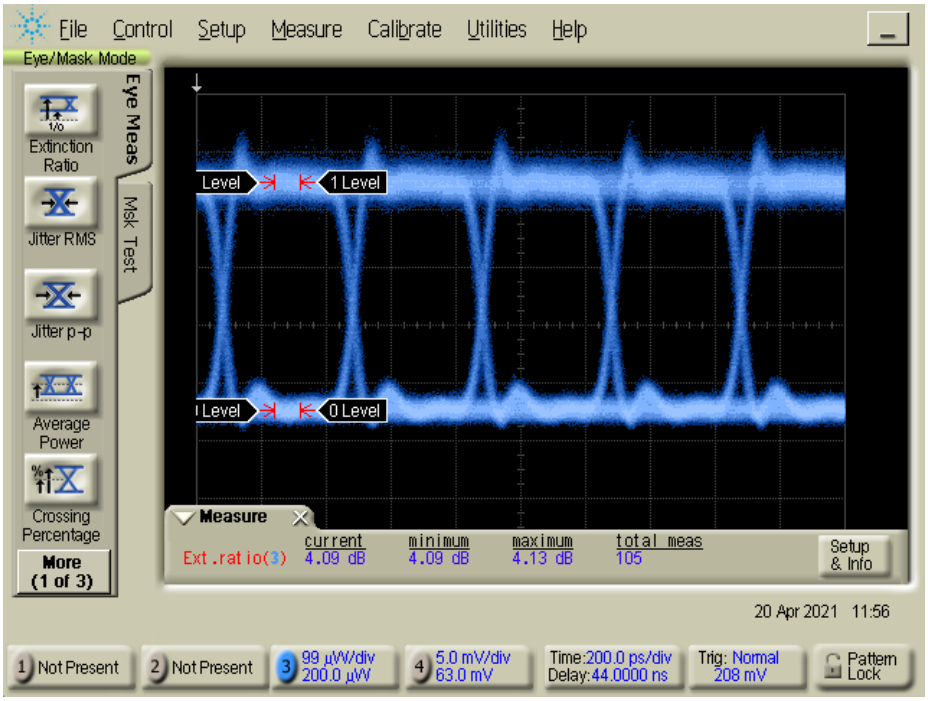


Figure 5.3: The eye diagram of an example VTRx+. A loop back system is adopted and the data rate is fixed to that of the Rx links to be 2.48 Gbps.

when the BER is as low as 10^{-9}. The OMA at a BER of 10^{-9} is adopted as a figure of merit for the optical link. While this definition is somewhat arbitrary, it is satisfactory for these studies in which changes in performance are the focus as opposed to absolute performance. These tests were performed with older VTRx designs in previous studies. With the latest production level VTRx+, these tests are repeated and results are recorded in this chapter.

In order to calculate the OMA values, the extinction ratios are taken from the eye diagram, as shown in Fig. 5.3. "Extinction Ratio" (r_e) is the ratio of two optical power levels of a digital signal generated by an optical source like a laser. The extinction ratio may be expressed as a fraction, in dB, or as a percentage. The extinction ratio can be defined as

$$r_e = \frac{P_1}{P_0} \tag{5.3}$$

, in which P_1 is the optical power level generated when the light source is on, and P_0 is the power level generated when the light source is off. The OMA is measured in dBm. dBm is a unit of level used to indicate that a power (voltage) level expressed in dB with reference to

one mW (mV). The power meter takes 10 % of the total signal to measure. So to get the real OMA, a factor of 10 needs to be accounted for. The relation between the real power and the power measured in the power meter is described in

$$\text{power}_{\text{real}} = 10 \times 10^{\frac{\text{power}_{\text{measured}}}{10}} \tag{5.4}$$

The power are also measured in dBm in this chapter. Even if larger r_e corresponds to a more open eye, the low current still needs to be above laser threshold in this case. So r_e is not expected to be very large in this study. The OMA is defined with the ratio between high and low of the power output. In this instance, the high and low power are defined as

$$\text{power}_{\text{low}} = \frac{2\text{power}_{\text{real}}}{1 + 10^{\frac{r_e}{10}}} \tag{5.5}$$

$$\text{power}_{\text{high}} = \text{power}_{\text{low}} \times 10^{\frac{r_e}{10}} \tag{5.6}$$

Thus the OMA in this instance can be defined as

$$OMA = 10 \times Log(\text{power}_{\text{high}} - \text{power}_{\text{low}}) \tag{5.7}$$

5.2 Bit Error Ratio Studies

To measure the quality of the complete transceiver (VTRx+) in extreme environments, a custom test system was adopted. The physical setup for the VTRx+ reliability test is composed of the VTRx+ transceivers located in a climate chamber, an optical switch, a power meter and an optical attenuator connected to the data taking PC, and the FPGA Mezzanine Card (FMC) and PCs connected to the system. There is also a reference VTRx+ mounted on the FMC, which sends and receives optical data to and from the VTRx+ in the climate chamber. Pseudo-random optical data is generated from the FPGA on the FMC and sent to the VTRx+ channels in the climate chamber and the one reference channel outside the climate chamber. The reference is not in extreme temperature and humidity environment

and serves as a baseline comparison. The data rate is 2.48 Gbps.

An electrical loop back from Rx to Tx is present for each VTRx+. The fibre output of the Tx is connected to the computer controlled optical attenuator and the power meter. The output of the attenuator is sent back to the FPGA which generated the pseudo-random data. Then the FPGA compares the returned data with the data it sent to obtain the Bit Error Ratio (BER). Scans of BER as a function of optical power are performed. The optical power is tuned with the attenuator and measured by the power meter. A computer controlled optical switch is used to cycle through the 11 VTRx+ in the climate chamber. There is the VTRx+0 used as reference outside the climate chamber. A schematic of the test system is shown in Fig. 5.4. This test process is directed by the black arrows. This test process is focused on the receiver (Rx, p-i-n diode) section of the VTRx+ transceivers. The experimental setup is shown in photos. Fig. 5.5 shows the PCB inside the climate chamber where the VTRx+ channels reside. Fig. 5.6 shows the FMC and the PCB where the reference VTRx+ is. Fig. 5.7 shows the overall setup which includes the computer, the optical switch and the FMC with the reference VTRx+ PCB on table.

In the other direction, as shown in Fig. 5.4 directed by the red arrows, the Tx side of the VTRx+ can be tested. The VCSEL on the FMC sends laser light to the optical switch. Then the signal gets to each of the VTRx+ in the climate chamber, from the Rx end to the Tx end. Then the signal goes through the attenuator along with the power meter and get back to the FMC board. The signal amplitude is proportional to the current measured in the system. The voltage over a 1-$k\Omega$ pull-up resistance is measured as the merit of measure for the signal amplitude.

The Received Signal Strength Indicator (RSSI) is the figure of merit for the signal intensity at the point of measurement. The RSSI output is a current sink that draws a current equivalent to the generated photo-current. It is achieved using current mirror "reflects" actual photo-current into a path with a pull-up resistor to the power supply voltage (2.5V in our application). Therefore the voltage drop (RSSI signal) can be used to estimate the photo-current. There are two RSSIs monitored in this study. One of the RSSI measurements uses the photocurrent on the reference VTRX+. This is monitoring the output power from

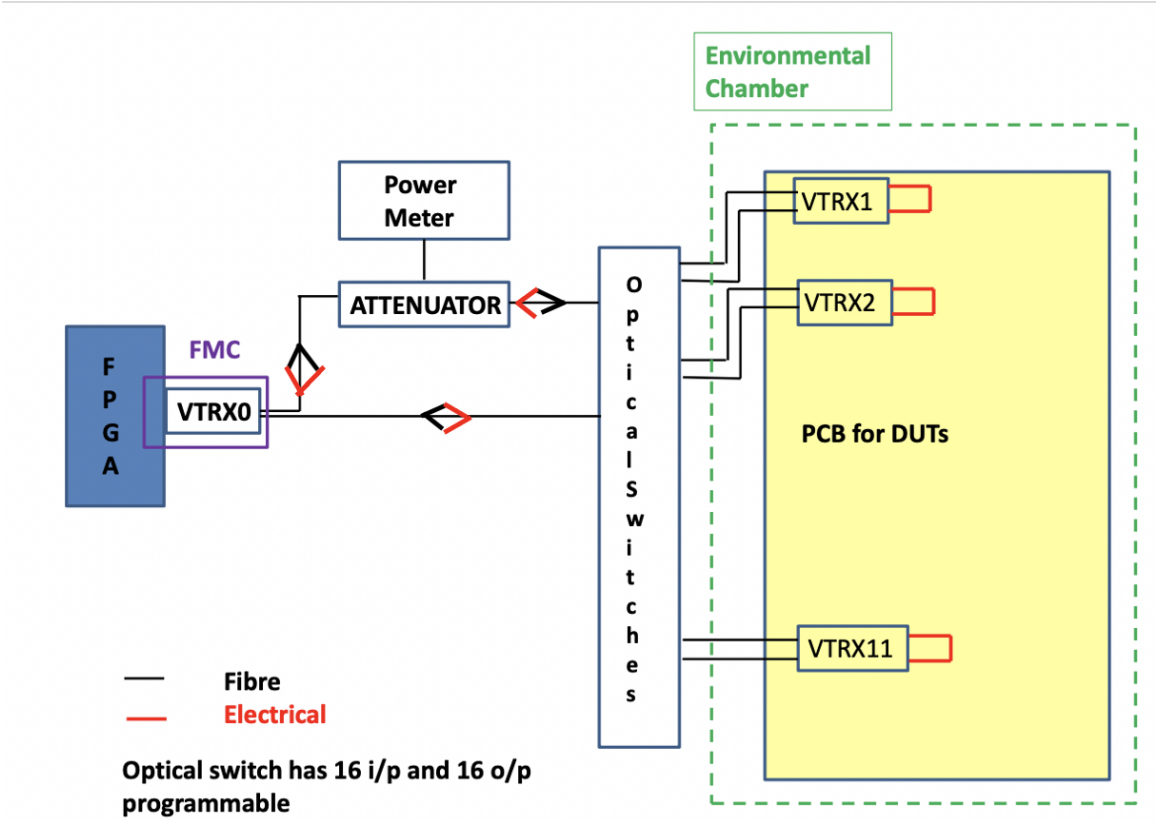


Figure 5.4: The schematic diagram of the test system for performing BER scans on 12 VTRx+. VTRx0 is the reference one on the FMC outside the climate chamber. The arrow direction indicates the data flow. Both the Rx and Tx channels of the DUT are tested, based on the direction of the data flow. The direction of the data flow is changed by reprogramming the optical switch. The black arrows show the direction when scanning the optical power of the reference VTRX+ and the red arrows show the direction when scanning the optical power of the DUT VTRX+.

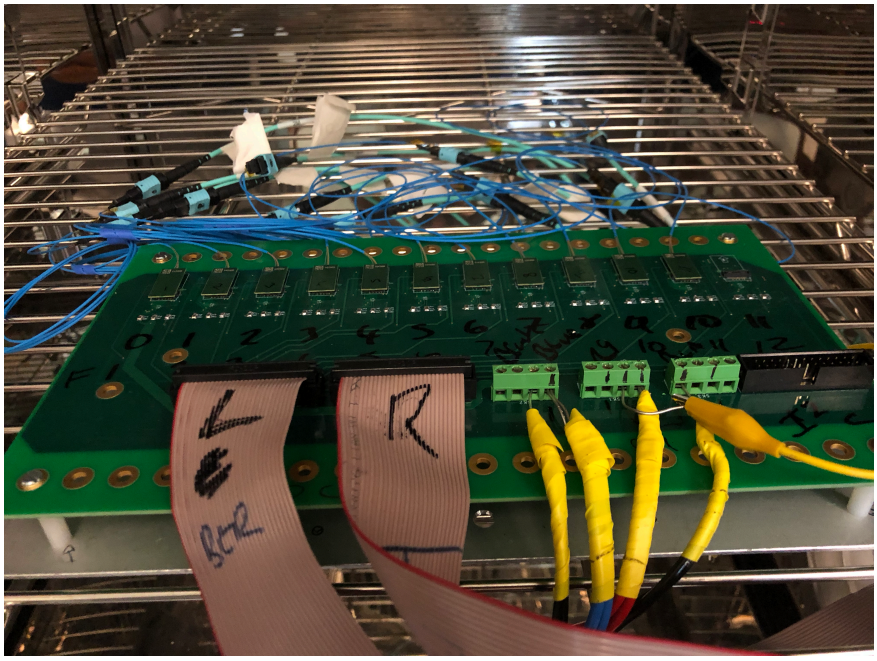


Figure 5.5: The PCB that holds 11 VTRx+ channels in the climate chamber.

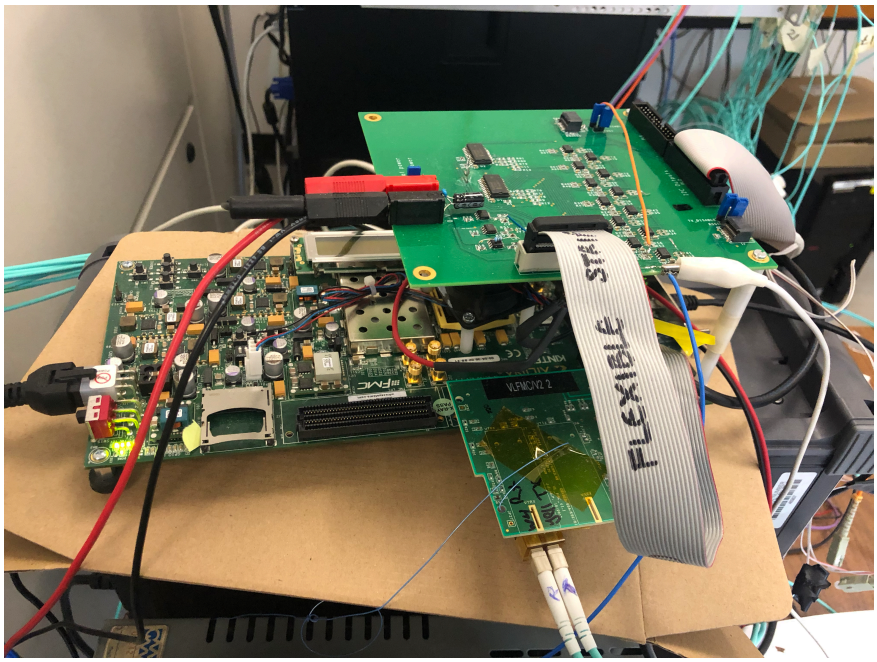


Figure 5.6: The FMC with the PCB where reference VTRx+ is mounted on top.

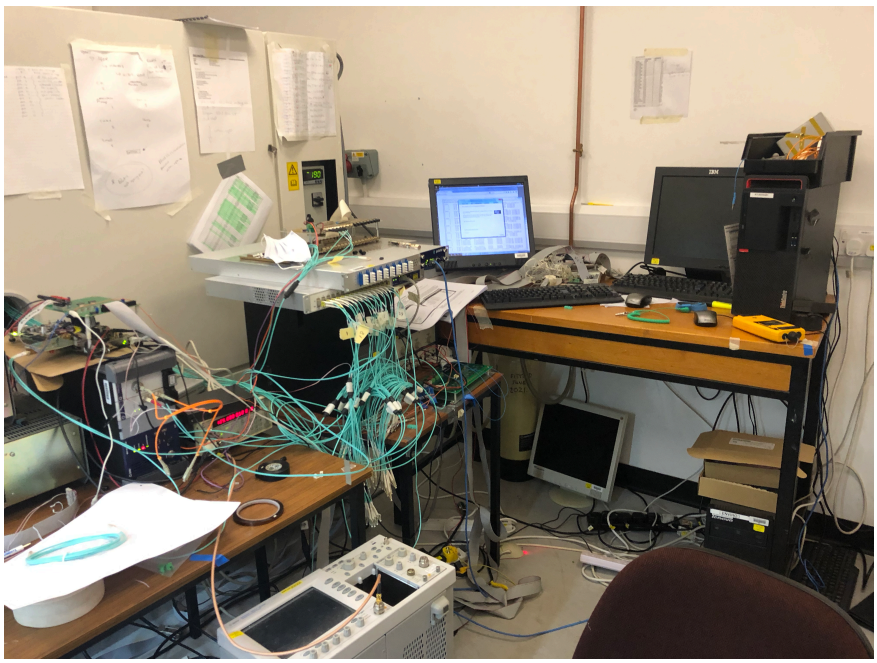


Figure 5.7: The overall setup with optical switch, control computer and power meter.

the VCSELs in the DUTs. The other RSSI measurements use the photocurrent on the DUTs. This is monitoring the output power from the reference VTRX+. The output signal from the VSCELs on DUTs is also measured with the power meter in this setup. But in the ATLAS operation, the VSCEL output can not be accessed via power meter, and can only be measured with RSSI measurements.

For luminosity-current scan (LI scans) studies to be discussed in Sec. 5.3, the VTRx+ bias and modulation currents can be changed via the I^2C links from the FPGA FMC. The dependency of the output power that is measured in the power meter on the bias current is important to understand the VTRx+ laser performance.

5.2.1 Room Temperature and Humidity Tests

Before turning on the climate chamber and starting the test in 85 °C / 85 % RH, the tests are first performed in room temperature and humidity. The data taken in this part starts when the climate chamber is not turned on and the temperature and humidity is the same as the room, which is about 23 °C and normal laboratory humidity. After around 200 hours, the climate chamber was turned on to be 85 °C and 85 % RH.

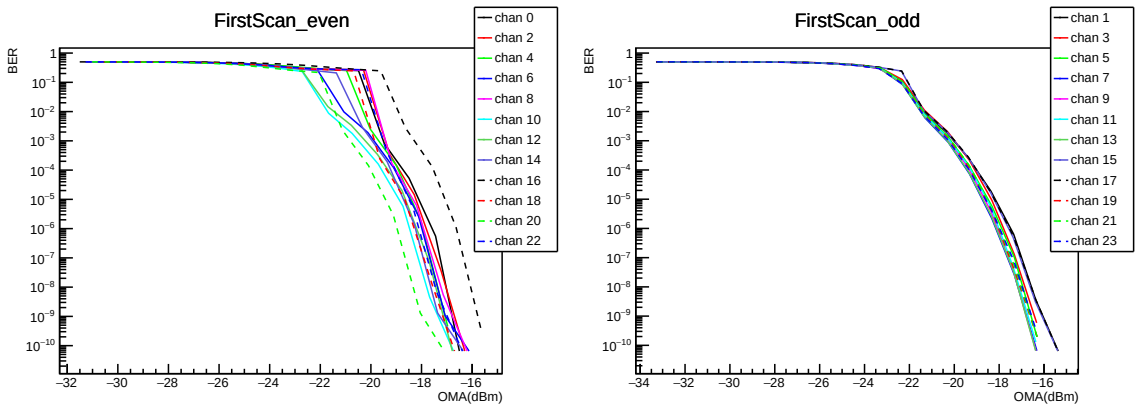


Figure 5.8: The BER-OMA relation for the first scan in room temperature and humidity. The left side of the plot include even channels of the system, corresponding to VCSEL on VTRx+. The right side of the plot includes odd channels, corresponding to the photo-diode VTRx+.

The results for the first BER scans performed at the beginning of the data taking is shown in Fig. 5.8. The BER scans are recorded about every 70 minutes with an hour interval in between scans. During each scan, the Optical Modulation Amplitude (OMA) point where the BER drops to 10^{-9} is chosen to be the figure of merit. For the instances where 10^{-9} is between two points, the OMA is obtained via interpolation as the interpolation is linear in Log (BER). The OMA at 10^{-9} is named "Minimal OMA" and 10^{-9} used as the BER metric in this study. The Minimal OMA is obtained from each BER curve performed and monitored over the duration of the test. The change in OMA would indicate the change in performance of the VTRx+ Rx end.

The minimal OMA is monitored for about a week, as shown in Fig. 5.9. Each point represents a BER scan and the neighbouring points are about 70 minutes apart. The climate chamber is turned on after about 200 hours. As shown on the left plot in Fig. 5.9, the minimal OMA of VSCELs on VTRx+ increases after the climate chamber is set to 85 °C and 85 $\%$ RH. If the change in OMA is over 2 dB over time in the same environment, which is a commonly used industrial standard, the VCSEL is classified as a failure. The minimal OMA from DUTs stay consistent during the 200 hours before the climate chamber is turned on according to Fig. 5.9. This shows that there were no failures in room environments. The right side plot in Fig. 5.9 shows the signal that PDs on VTRx+ receive, which stays the

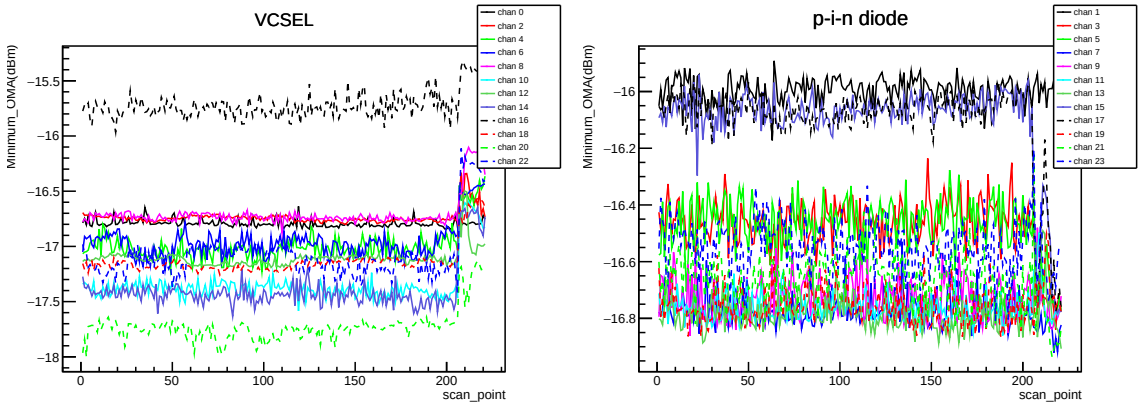


Figure 5.9: The OMA versus time. The climate chamber is turned on around 200 hours after the data taking beginning, where the minimal OMA on VCSELs increased as expected. The left side of the plot include even channels of the system, corresponding to VCSEL on VTRx+. The right side of the plot includes odd channels, corresponding to the photo-diode on the VTRx+.

same.

Another way to monitor the consistency of the VTRx+ performance is to monitor the optical power at a certain attenuation. The attenuation is tuned by the attenuator and the monitored optical power is the measured power as $power_{measured}$ in Eq. 5.4. The chosen attenuator setting in this study is 17. It is arbitrarily chosen to represent a medium attenuation. The optical power measured at this attenuation is monitored and shown in Fig. 5.10. The optical power from the VSCELs drops as the climate chamber is turned on after around 200 hours. The optical power is expected to decrease as temperature changes from normal operation temperature. As shown in the left side plot Fig. 5.10, the optical power at the attenuation of 17 is rather stable before the climate chamber is turned on. The right side plot corresponds to the power recieved by the PDs on DUTs, which will stay unchanged.

As discussed before, the RSSI signals of the light power from VCSELs on VTRx+ are monitored. The RSSIs are expected to be similar for all channels and largely stable over time. The photodiode is biased using a 1 kΩ series resistor. The RSSI signal monitors the voltage drop across this resistor, hence providing a measurement of the photocurrent. An example channel is shown in Fig. 5.11 and all VTRx+ channels perform in very similar patterns. The RSSI is read every 1-2 seconds, thus a lot more readings than the number of

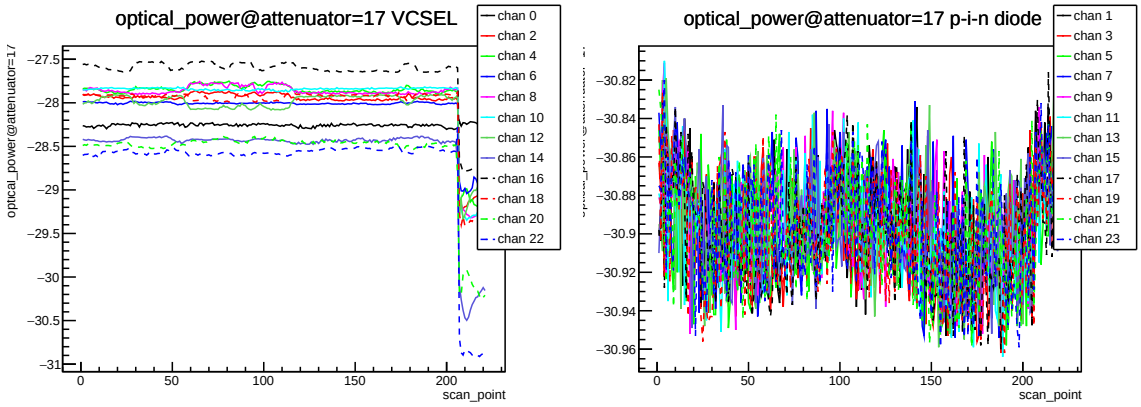


Figure 5.10: The measured optical power at the attenuation of 17 change with time. The optical power from the VSCELs drops as the climate chamber is turned on after 200 hours.

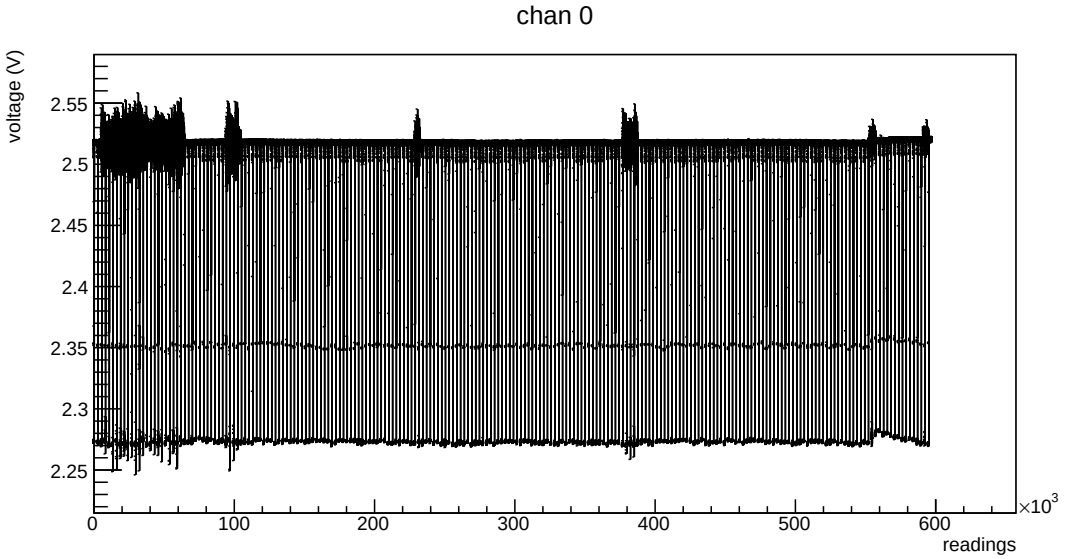


Figure 5.11: RSSI voltage readings for VTRx+ 0 as an example.

BER scans performed. When the system is not performing BER scans, the RSSI voltage is high at about 2.52 V. During the BER scans, the RSSI voltage drops to about 2.27 V. The difference between the high and low converted to current (with 1 kΩ pull-up resistance) is the RSSI.

As shown in Fig. 5.11, the highs and lows of the voltages are usually quite stable. There are a few instances of disturbance, presumably caused by current noise introduced by other electronic systems in the same laboratory.

For each BER scan, the zoomed in version of Fig. 5.11 is shown in Fig. 5.12. The low level

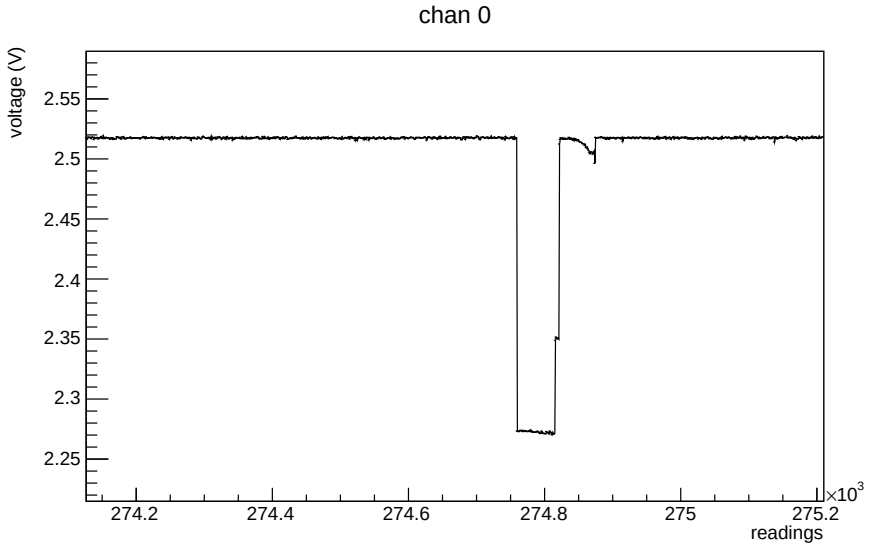


Figure 5.12: Zoomed in version of Fig. 5.11 to show an example BER scan. The low level happens before BER scans for this channel and BER scans are being performed for other channels. The high level happens during the intermediate waiting time between BER scans. The small dip after the large step corresponds to the BER scan for this channel, when the attenuation is being gradually reduced until the target BER is achieved.

voltages are taken during the BER scans and only last for a few minutes.

The current change between the high and the low for each channel is monitored over time, as shown in Fig. 5.13. The climate chamber is turned on after 200 hours of BER scan and the RSSI current change shows a large disturbance. All the VTRx+ channels perform in a similar manner. The current change is usually around 0.25 mA.

On the other side, the performances of Tx channels are monitored in room temperature and humidity as well. This RSSI monitors the light intensity after the signal going through the Tx end of the VTRx+ channels. The signal going into the VTRx+ is expected to be both consistent and the same for all VTRx+ channels, thus the expected outcome is similar for all channels.

The VTRx+ Tx signals come through a multiplexer into one channel. 12 VTRx+ Tx channels are monitored in this study. For each BER scan, a typical signal is shown in Fig. 5.14. The low levels correspond to the multiplexer being connected to a VTRx+ and the last VTRx+ is left connected during the interval between BER scans. BER scans for a given channel occur

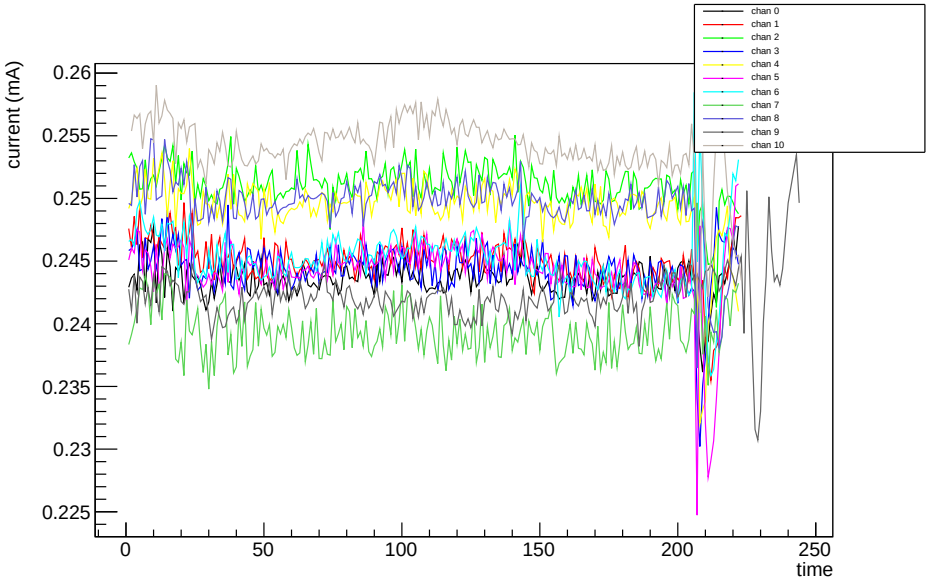


Figure 5.13: The RSSI current change for all VTRx+ channels. The typical current change is around 0.25 mA with 1 kΩ pull-up resistance.

once approximately every 70 minutes. The RSSI corresponds to the voltage drop between high and low voltage levels.

For each channel, the Tx RSSI low voltage is monitored over time as well. Each channel behaves in a similar manner but with a time delay between VTRx+ channels. VTRx+ Channel 0, 3, 6 and 9 are chosen as examples to show in Fig. 5.15. The count in the X axis stand for the number of BER scans and the time interval is around 70 minutes. There is a cycle pattern present that lasts around 24 hours. This is presumably caused by the daily temperature changes in the temperature controlled lab. The climate chamber is turned on after around 200 hours of BER scans, which causes the voltage monitored to increase.

The Tx signal is measured by the voltage difference between the high level (2.52 V) and the low level (as shown in Fig. 5.15). The Tx signal from all channels are shown in Fig. 5.16.

As shown from the results above, the VTRx+ performance is quite stable during about 200 hours in room temperature and humidity. The climate chamber turning on does have an influence on the system performance. The next step is to stress test VTRx+ reliability in an extreme environment.

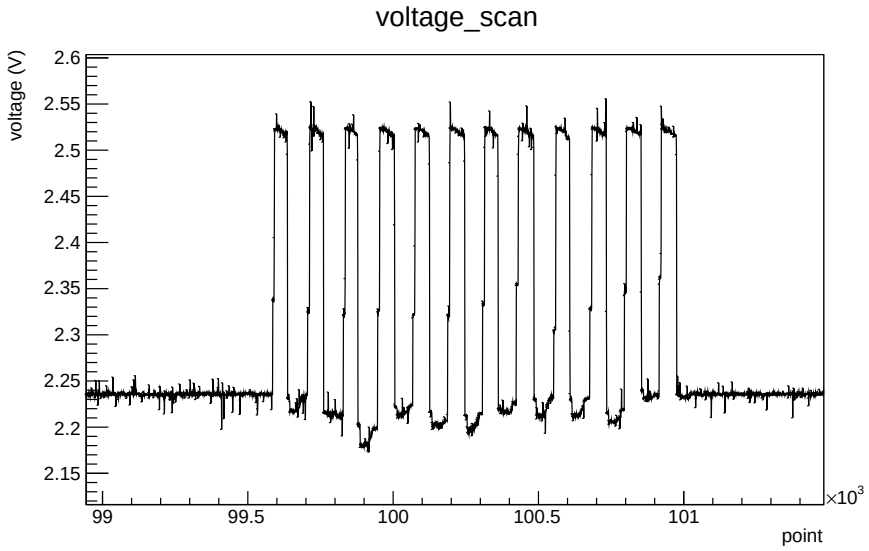
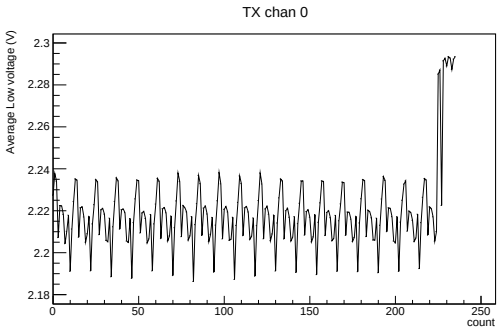
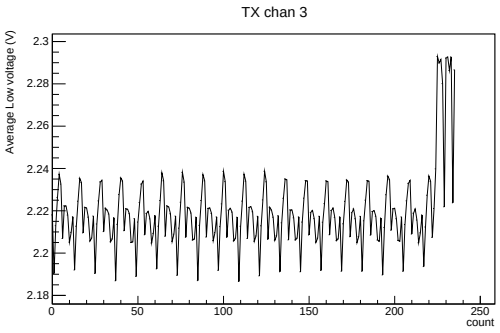


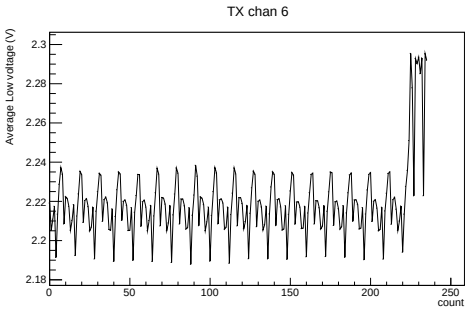
Figure 5.14: Typical signal for a BER scan from VTRx Tx. There are 12 VTRx+, corresponding to the 12 low levels. The last VTRx+ channel is usually left at low voltage during the intermediate time between BER scans.



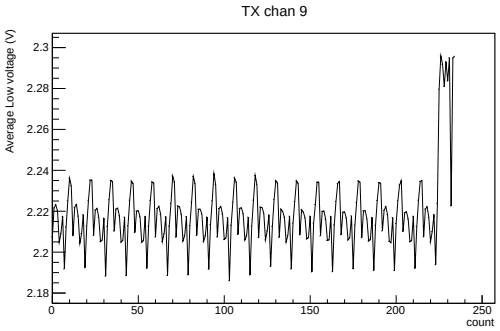
(a) The Tx RSSI low voltage for VTRx+ 0.



(b) The Tx RSSI low voltage for VTRx+ 3.

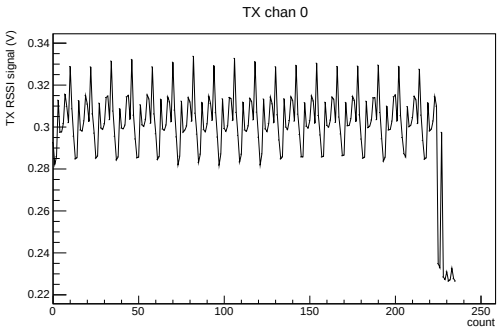


(c) The Tx RSSI low voltage for VTRx+ 6.

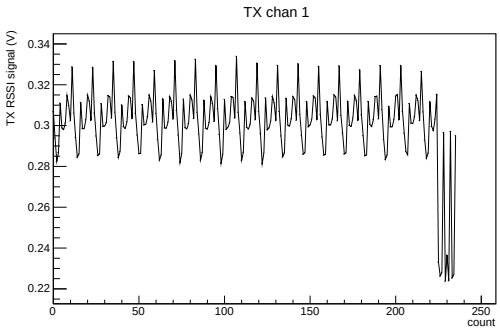


(d) The Tx RSSI low voltage for VTRx+ 9.

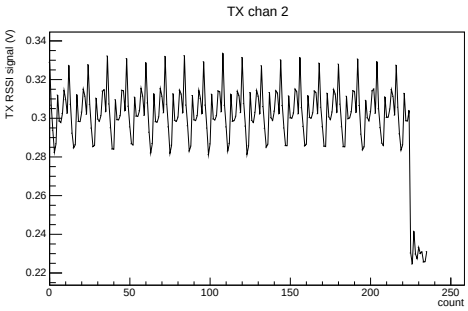
Figure 5.15: Tx RSSI low voltage examples. All VTRx+ follow the same pattern with a cycle of about 24 hours, with a count in X axis around 70 minutes. The climate chamber is turned on around the 200th BER scan.



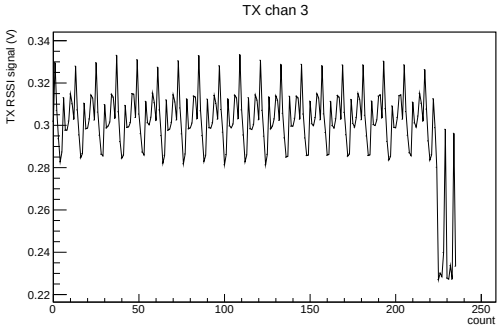
(a) The Tx RSSI signal voltage for VTRx+ 0.



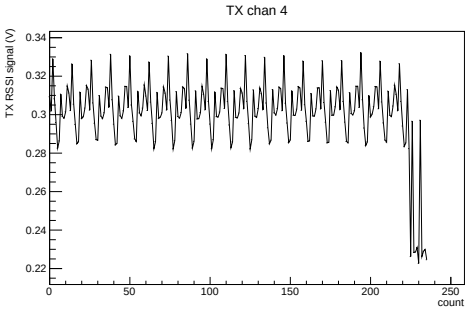
(b) The Tx RSSI signal voltage for VTRx+ 1.



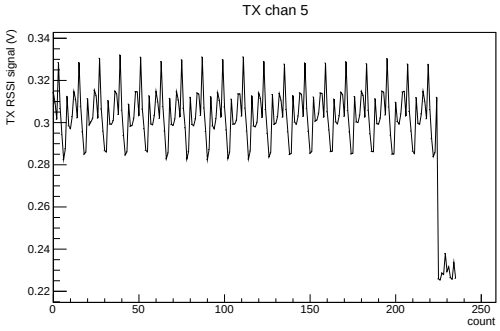
(c) The Tx RSSI signal voltage for VTRx+ 2.



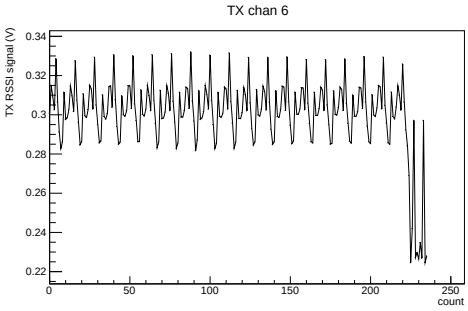
(d) The Tx RSSI signal voltage for VTRx+ 3.



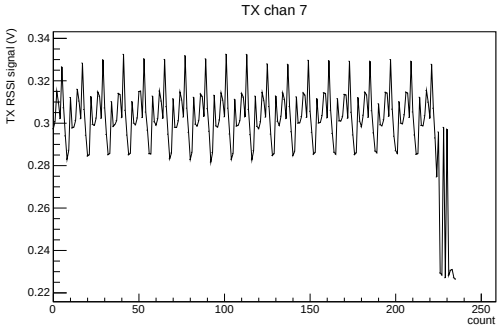
(e) The Tx RSSI signal voltage for VTRx+ 4.



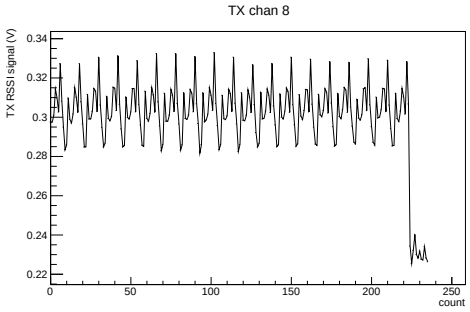
(f) The Tx RSSI signal voltage for VTRx+ 5.



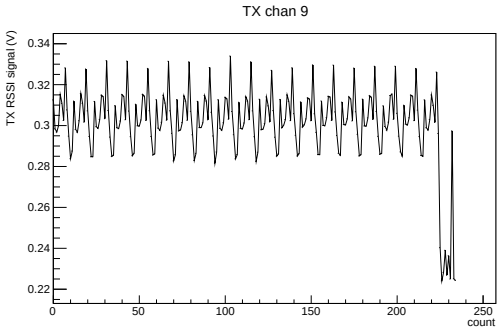
(g) The Tx RSSI signal voltage for VTRx+ 6.



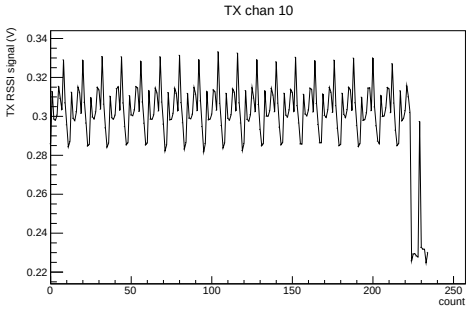
(h) The Tx RSSI signal voltage for VTRx+ 7.



(i) The Tx RSSI signal voltage for VTRx+ 8.



(j) The Tx RSSI signal voltage for VTRx+ 9.



(k) The Tx RSSI signal voltage for VTRx+ 10.

Figure 5.16: Tx RSSI signal voltage for all 11 VTRx+ Tx channels. All vtrx+ follow the same pattern with a cycle of about 24 hours, with a count in X axis around 70 minutes. The climate chamber is turned on after around the 200 hours of BER scans.

5.2.2 85 °C and 85 % Relative Humidity Tests

The same study as featured in Sec. 5.2.1 is repeated in the 85 °C and 85 % RH environment. The test lasted for around 700 hours, which is equivalent to around 550 data points. One channel (VTRx+ 11) died around 10 hours into the test due to connection issues. The I^2C link communication issue is caused by the noise from the tape tester robot (see Chapter 4). Both Tx and Rx connections were lost due to this issue. The other VTRx+ survived the duration of the test and the results of which are shown in this section.

The BER scans for the first and the last scan performed are shown in Fig. 5.17 and Fig. 5.18 respectively. As can be seen from the plots, the last VTRx+ (channel 23) started out fine in the first scan and was dead in the last. As the approach described in Sec. 5.2.1, the minimal OMA when the BER reaches 10^{-9} is recorded over the 550 data points. The minimal OMA is shown in Fig. 5.19. The time when last VTRx+ lost connection can be deduced from this plot. For other channels, it can be seen that they remained stable for the duration of the 700 hour test.

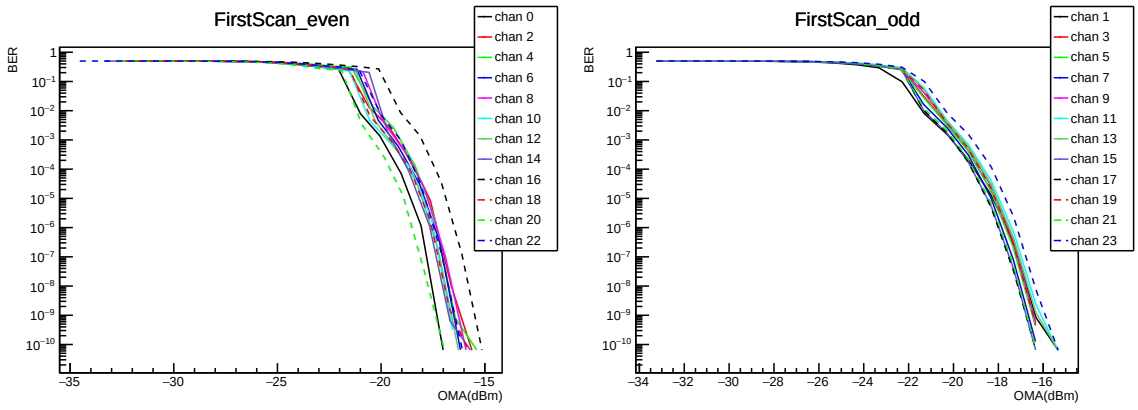


Figure 5.17: The BER-OMA relation for the first scan in 85 °C and 85 % RH. The left side of the plot include even channels of the system, corresponding to VCSEL on VTRX+. The right side of the plot includes odd channels, corresponding to the photo-diode on the VTRx+.

The measured optical power at the attenuation setting of 17 is shown in Fig. 5.20. The optical power remained stable for the channels that are alive for the duration of the test as well. There are periodic changes for the signal into the PDs on DUTs but the changes are quite small relatively. In general the performance of the 10 surviving VTRx+ in the climate

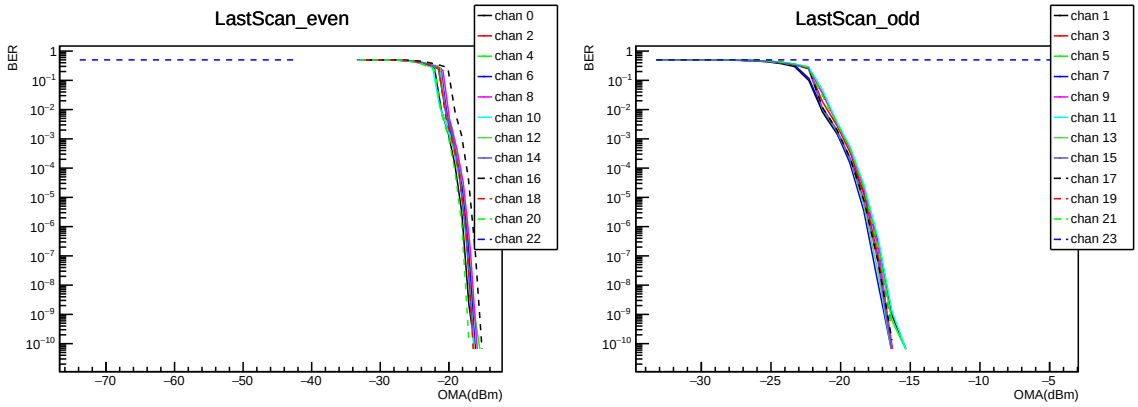


Figure 5.18: The BER-OMA relation for the last scan in 85 °C and 85 % RH. The left side of the plot include even channels of the system, corresponding to VCSEL on VTRx+. The right side of the plot includes odd channels, corresponding to the photo-diode on the VTRx+. Channel 23 and 22 correspond to the last VTRx+, and it lost connection to the PCB about 10 hours into the test.

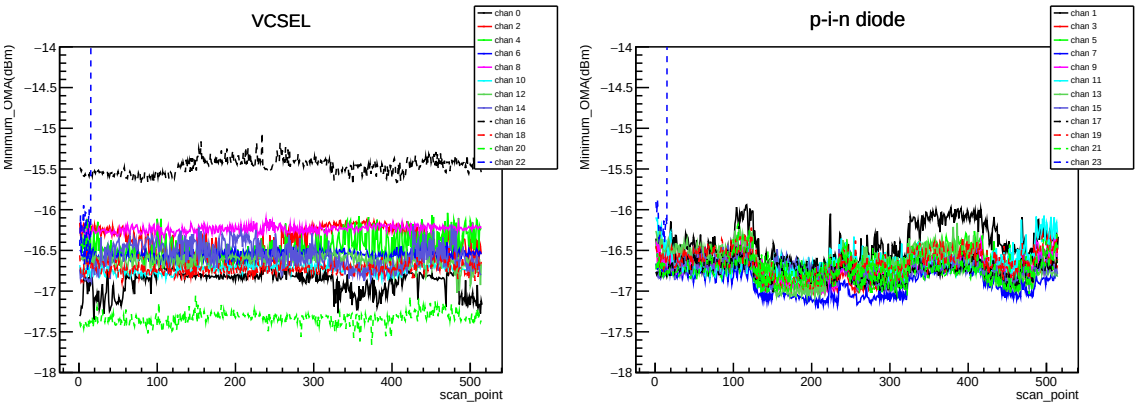


Figure 5.19: The minimal OMA versus time in 85 °C and 85 % RH. The left side of the plot include even channels of the system, corresponding to VCSEL on VTRx+. The right side of the plot includes odd channels, corresponding to the photo-diode on the VTRx+.

chamber is stable over the duration of the test.

The RSSI studies are also repeated for the 85 °C and 85 % RH tests to monitor the laser output and the Tx channels performance. Following the same process as introduced in Sec. 5.2.1, the RSSI current changes for all VTRx+ channels are obtained with 1 kΩ pull-up resistance. However, the connections to the RSSI measurements are not stable, as demonstrated with the Tx RSSI in Fig. 5.21. The RSSI data taking is supposed to happen whenever a BER scan is taken. But as can be seen from Fig. 5.21, there are fewer RSSI data

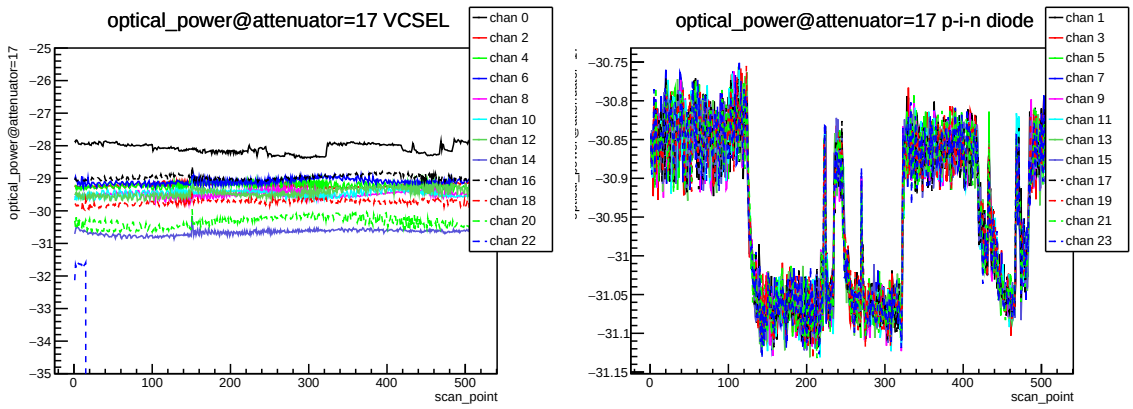


Figure 5.20: The measured optical power at the attenuation of 17 change with time in 85 °C and 85 % RH.

points taken. As a result, the RSSI results in 85 °C and 85 % RH studies are not used.

5.3 Luminosity-Current Scans

For all the studies discussed in Sec. 5.2, the bias currents and modulation currents for all lasers on the VTRx+ are fixed to be 5 mA, which is also the default settings. The bias current is the current that drives the laser into operation. It defines the current when the system is transmitting a logical 0. This is set to be slightly above laser threshold to optimise the turn-on speed. The modulation current is the current varies with time to modulate the output signal from the laser. It is the magnitude of the additional current that is sent when transmitting a logical 1.

The relation between laser power and the bias current is called the LI relation. When the modulation is set to 0, the bias current can be varied, forming a LI scan. Properties like the turn-on points and the linearity of the power-bias current relations are obtained from the LI scans. They serve as important figures of merit when describing how the laser performance changes over time. Changes are expected because of radiation damage after the VTRx+ is in operation at ATLAS.

The VTRx+ used for the BER scan studies are used for LI scan studies. 10 VTRx+ that survived the 85 °C and 85 % RH tests are used and the environment for performing the LI

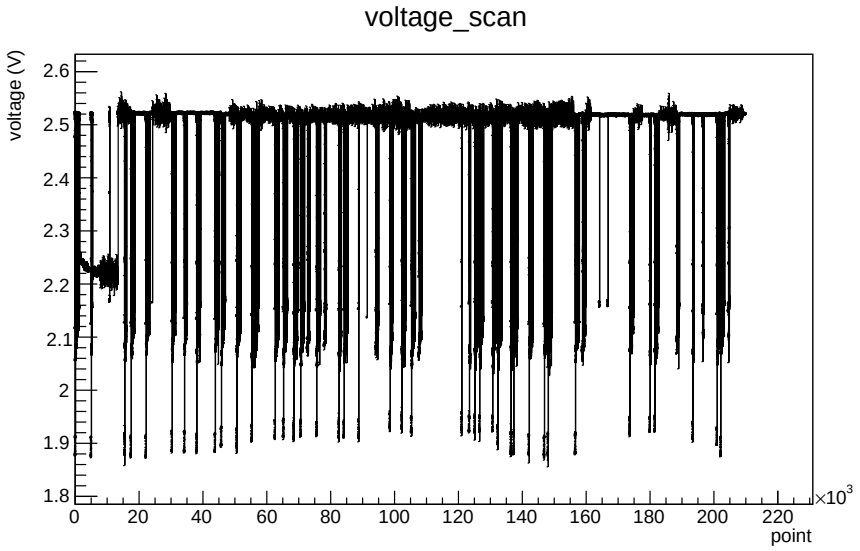


Figure 5.21: Tx data from 85 °C and 85 % RH. The number of data points taken are way fewer than the BER scan number.

scans in this section is maintained in 85 °C and 85 % RH. Connections via I^2C are stable for three VTRx+, the LI scans of which are shown in Fig. 5.22. The LI curve starts with a linear part and is highly non-linear at higher bias currents. This is a general feature for VCSELs, as the bias current increases, this causes self-heating of the VCSEL. The slope efficiency will decrease as the temperature increases. Restricted regions of the LI curve are used in order to have a reasonable linear fit.

In the linear part, the bias current needed for the laser to turn on is defined as the "turn-on point" and the linearity describes the relation between laser intensity and bias current. The linear fit is

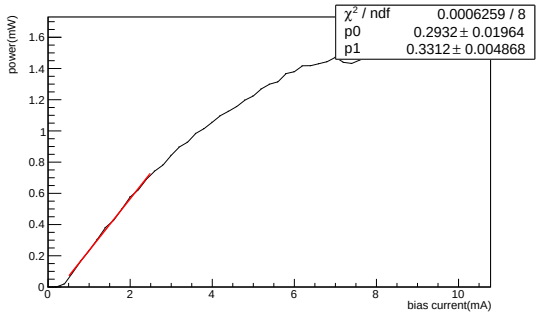
$$y = k(x - x_0) \tag{5.8}$$

, in which k is the linearity and x_0 is the turn-on point. The fit range is 0.5 to 2.5 mA for Channel 2 and Channel 6, and 0.5 to 2.0 mA for Channel 2. The fit parameters are summarised in Tab. 5.1.

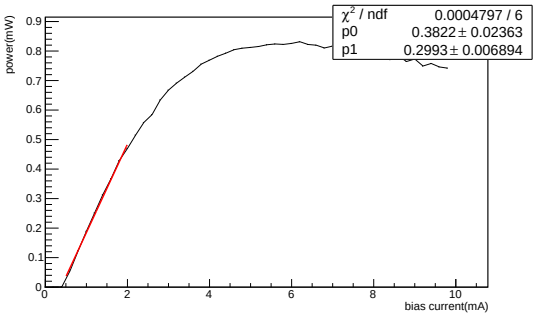
As can be seen from Tab. 5.1, the fit parameters are similar. The turn-on points are 0.3-0.4 mA for the lasers on VTRx+ tested. The average linearity is 0.2948 $\pm$ 0.0318 mW/mA and the average turn-on point is 0.3738 $\pm$ 0.0033 mA. The uncertainties are statistical.

	turn-on point (mA)	slope (mW/mA)
Channel 0	0.3312	0.2932
Channel 2	0.3822	0.2993
Channel 6	0.4076	0.2918
Average	0.3738	0.2948

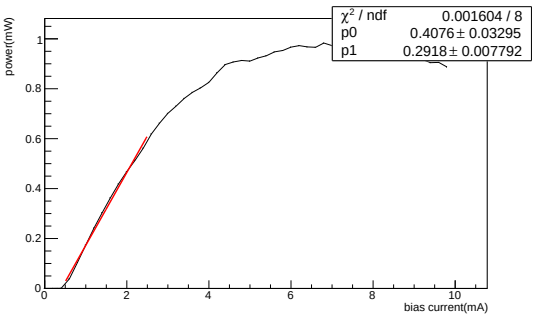
Table 5.1: The fit parameters obtained from Fig. 5.22.



(a) LI scan on Channel 0, which is the reference VTRx+ outside the climate chamber.



(b) LI scan on Channel 2.



(c) LI scan on Channel 6.

Figure 5.22: LI scans on three VTRx+, fitted by a linear function.

5.4 Summary and Outlook

The VTRx+ performance is tested in normal environment and extreme environments (85 % RH and 85 °C) for 700 hours. The aging effect for 1000 hours is expected to be on par with 10 years of aging in cooled environment of ATLAS operation. Due to experimental limitations, it was not practical to have 1000 hours, but 700 hours is enough to demonstrate the basic idea.

As discussed in Sec. 5.2.1, the VTRx+ performance is stable in room environment and there is a change in performance when the environment changes. Most VTRx+ survived the 700-hour test in 85 % RH and 85 °C, with one dead. The cause is that one VTRx+ lost connection inside the chamber 10 hours into the operation. The connection issue was caused by lost communication from I2C links for that channel. RSSI data taking was unstable during this test. A water leakage was observed during the 85 % RH/85 °C test so that the test was concluded at 700 hour.

The future plan is to move the setup to a new climate chamber and resume testing for 1000 hours. The PCB (shown in Fig. 5.5) board used for mounting the VTRx+ has been through multiple cycles and the connectors could be corroded or damaged in the process. Moisture could also get in the connector, reducing connection. These could lead to the result that only three VTRx+ had stable I^2C connection for the LI scan studies. A new PCB board is prepared and will be used when the setup is moved to the new climate chamber. The LI scan study is also repeated with the VTRx+ on a stave, as will be discussed in Sec. 6.4.

6 | Stave and System Testings

As discussed in Chapter 2, after all the components are tested individually, they are put together to make a stave. As discussed in Sec. 2.4.1, the modules are mounted on staves, which are carbon-fibre sandwiches. A stave is a minimal system to validate the performance of all sub-structures working together. Several staves are usually placed in a testing structure to be in close vicinity to test the overall performance of the system. The aim is to have an environment as close as possible to that of the final detector. [5] For the previous stave design (chip set ABC130), three staves were tested together at RAL. For the ABCStar chip set, the system test is planned to be composed of eight staves at CERN, which will take place in 2023. Tests at the level of one or several staves are important to validate the performance of the sub-system before the start of large scale production for all components.

For the content of this chapter, only one stave is used at a time but it proves the principle for testing in multiple stave systems. This thesis contains some of the results necessary for validating the detector performance on staves but many further tests will be performed using the 8 stave system test at CERN. The studies presented in this chapter are

- Cold stave noise study: The noise performance is first tested for a single stave in cold and warm environments to validate the system performance. Excessive noise was observed in the first cold stave test in Brookhaven National Laboratory (BNL). [69] Later tests at RAL tried to replicate and locate the problem. The results of the RAL study is detailed in Sec. 6.1.

- Magnetic trigger studies: As discussed in Sec. 2.3, the DC-DC converter on the power boards of each module can introduce a leakage field, which in turn manifest in a new noise source. This effect is observed in both cold and warm noise studies. It is studied with magnetic triggering on the leakage fields, as discussed in Sec. 6.2. The influence of two factors has on leakage field are studied, the two factors being:

  - influence of removing ACGND

  - influence of removing module capacitors

- Module performance on stave and standalone: The performance of a single module mounted on a stave or tested standalone is also compared, showing minimal changes in performance, as shown in Sec. 6.3.
- LI scan of VTRx+ on a stave: the methodology for the long term testing of the optical links is presented and evaluated on a stave at CERN, and these results are summarised in Sec. 6.4.

6.1 Cold Stave Noise Studies

To test the performance of a stave, three large scale demonstrators have been assembled: the 14-power-board stave test to demonstrate the principle of multi-drop communication between AMAC and lpGBT, a fully-loaded LS stave to demonstrate master-slave EoS communication, and noise performance in warm and cold temperature, and the 5-SS stave (a stave mounted with 5 SS modules on one side) test to demonstrate multi-drop command and clock between lpGBT and HCC/modules. The fully-loaded LS stave and the 5-SS stave tests are the focus of the noise performance studies.

The fully-loaded LS stave was assembled and tested at BNL in Feb. 2020. A stave cold box was built at BNL to facilitate thermal cycling and electrical tests at expected operating temperatures. The cooling system uses "NOVEC" engineered coolant. There is a 15 °C difference between chiller output and stave input. The full stave has been tested in room temperature and the noise performance is as expected.

The 5-SS stave was assembled and tested at RAL in May 2020. Due to limitations in the lab, the stave was not able to run in cold temperature in the beginning but was cooled down later. The stave is tested in room temperature in May and later was cooled down in Nov. 2020. The five modules on the stave have been individually tested cold before being mounted to the stave. The five modules are loaded onto the most heavily loaded multi-drop CCR segment (as discussed in Sec. 2.4.1) to verify the performance of muti-drop communication in this segment. The 5SS stave is shown in Fig. 6.1.

Excessive noise was observed on the fully-loaded LS stave in cold environment at BNL in

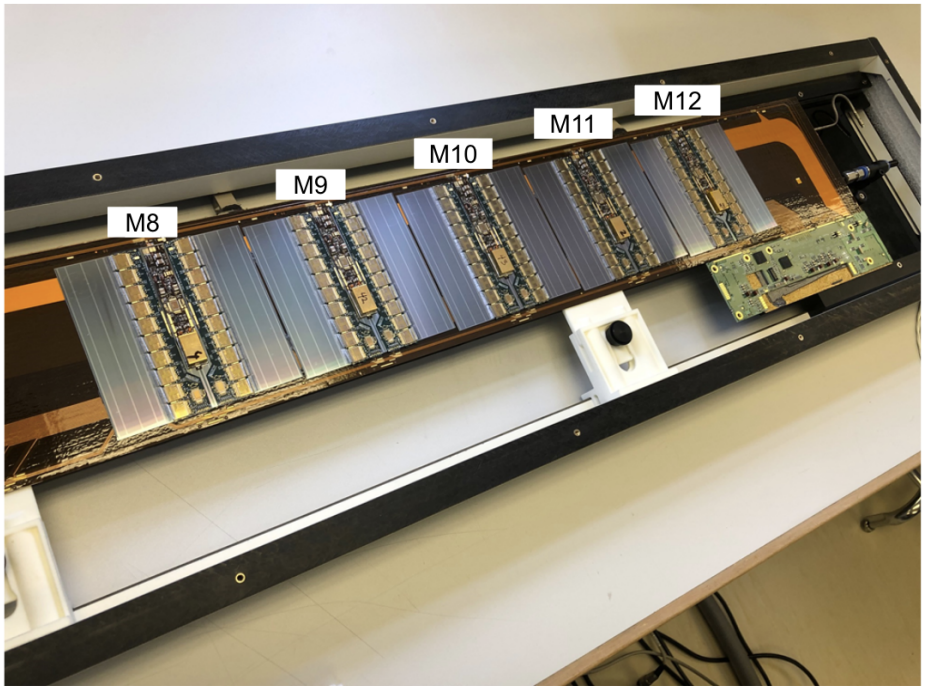


Figure 6.1: 5 SS stave at RAL. Five modules are loaded onto the multi-drop CCR segment near the EOS region.

previous studies. [69] As shown in Fig. 6.2, while the noise performance is still reasonable in room temperature (20 °C), there is a major increase in noise when the temperature is lowered to -40 or -50 °C.

This study was replicated at RAL with the 5SS stave. The cause for this issue was located. As shown in Fig. 6.3 [69], the power board on each module introduces a voltage step, dV, at every power board clock cycle. This voltage step introduces current flow into Signal Ground bonds (also referred to as ACGND bonds in this thesis), which connects the hybrid ground (also referred to as Signal Ground) to Fast Signal Ground. The chips to the right of the voltage step location are grounded via the ground pad in the middle. But the chips to the left of the voltage step have a mixture of grounds. They are grounded to the middle as well as to the signal ground. It can create unwanted ground loop currents if the two grounds are at different potentials. This will result in excess noise for the front-end amplifiers, which can be seen in Fig. 6.2. The ground loop issue affects mostly the left half of the module. Even if this effect is present for all modules on a stave, it is more obvious for the last few modules closest to the EoS region, as shown for hybrid 11 and 12 in Fig. 6.2. This is

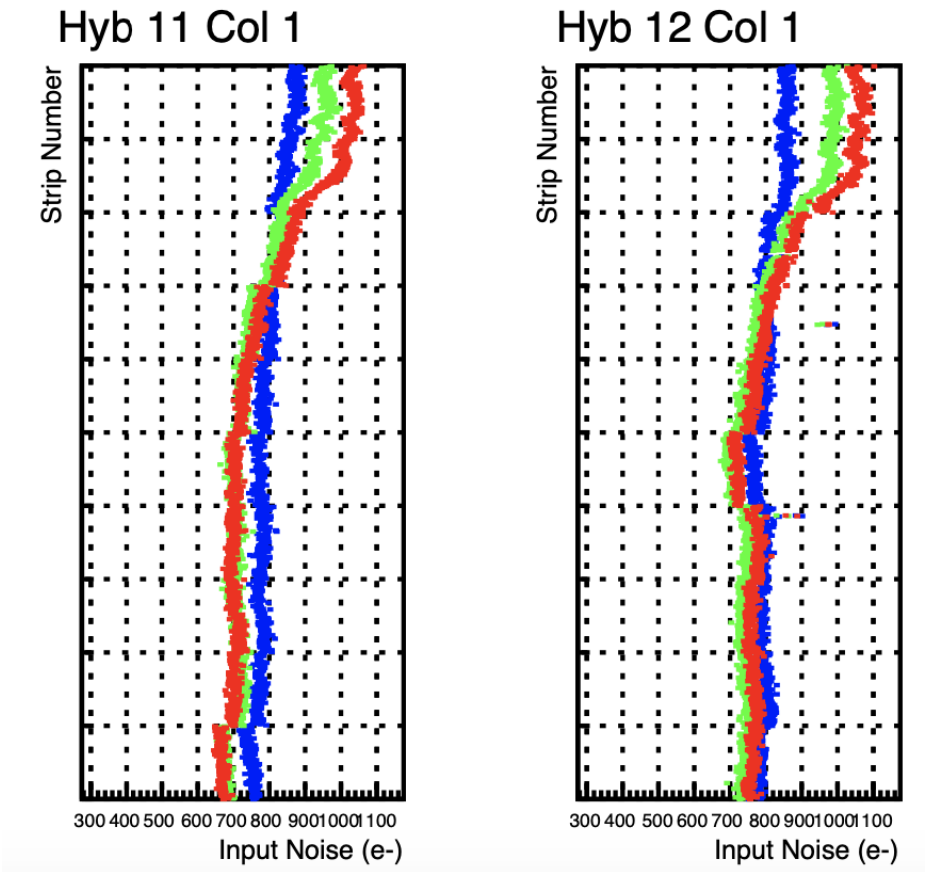


Figure 6.2: Input noise distribution with strip numbers on one sensor columns for Hybrid 11 and 12 on fully-loaded LS stave at BNL. The blue data points are for 20 °C, the green data points are for -40 °C and the red ones are for -50 °C. [69]

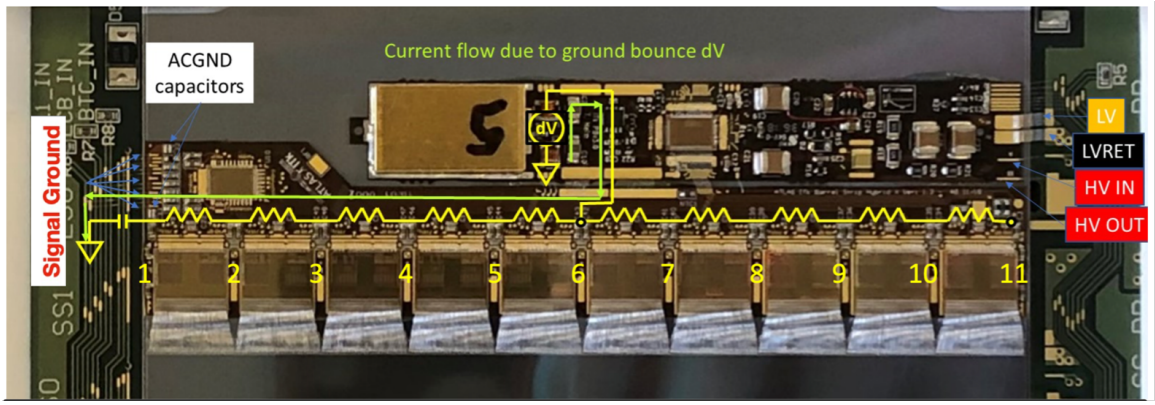


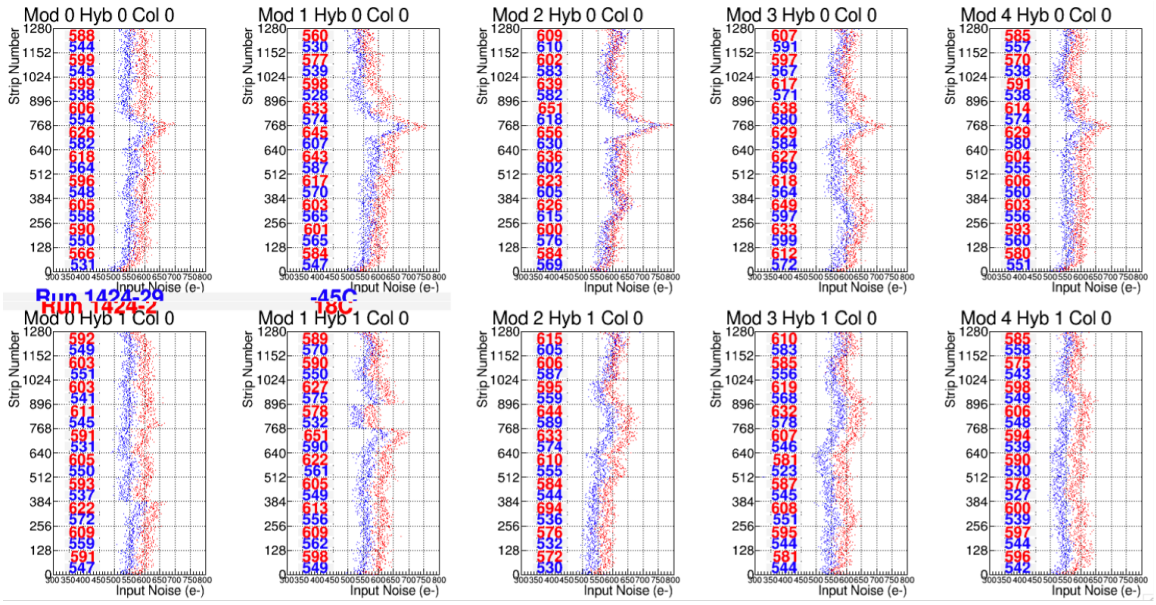
Figure 6.3: The power board introduces a voltage step, dV, at every power board clock cycle. This voltage step introduces current flow into Signal Ground bonds (ACGND bonds), which connects the hybrid ground (also called Signal Ground) to Fast Signal Ground. This causes extra noise seen in Fig. 6.2. [69]

presumably caused by the current mixing along the ground line on a stave. As more current flows through the module ground when the module is closer to the EoS region, the more noise introduced by current flow across ACGND bonds the module would see. The reason that this effect is not obvious when operating warm is that the noise caused by ACGND bonds is switching noise. It increases as the signal processing time becomes shorter when running cold.

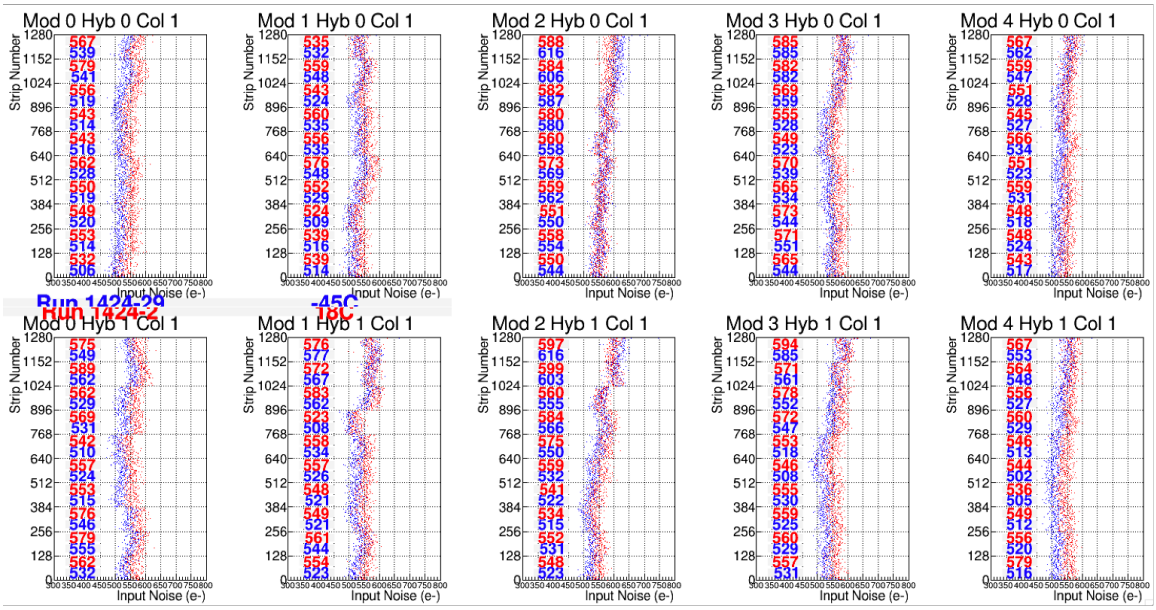
For the 5SS stave tests repeated at RAL, the cold (-45 °C) and warm (18 °C) input noise difference with ACGND bonds on are not as obvious as the BNL results. The results are shown in Fig. 6.4. Column 0 and 1 stand for the two strip columns that each chip are bonded to. Since the modules are SS modules, there are two hybrids on each module. There is some tendency that the cold input noise is higher in the region affected by the ground loop but not as obvious as the BNL results.

The gain and input noise were taken with and without ACGND at both cold (-40 °C) and warm (18 °C) for the 5SS stave. As shown in Fig. 6.5, removing the ACGND bonds does not interfere with the data transmission along the data lines as the eye diagram performance at full performance speed is still good. This justifies the legitimacy of removing ACGND bonds as it would not affect the data transmission.

In the warm instance, the ACGND bonds do not introduce to much effect on the input

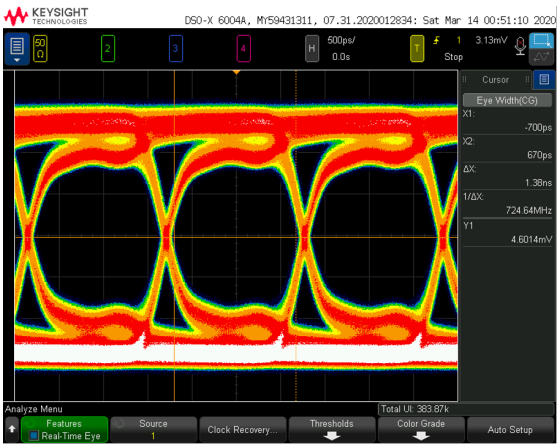


(a) The input noise of Column 0 in the 10 hybrids on the 5SS stave cold (-45 °C, blue) and warm (18 °C, red), with ACGND bonds.

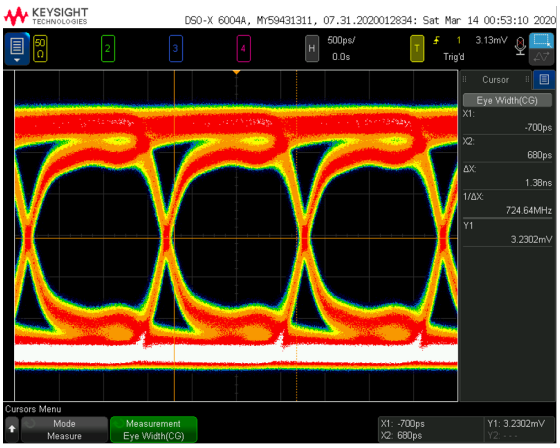


(b) The input noise of Column 1 in the 10 hybrids on the 5SS stave cold (-45 °C, blue) and warm (18 °C, red), with ACGND bonds.

Figure 6.4: Cold and warm input noise distributions of the 5SS stave with ACGND bonds on.



(a) Eye diagram of the data transmission line at 640 Mbps with ACGND bonds on.



(b) Eye diagram of the data transmission line at 640 Mbps without ACGND bonds.

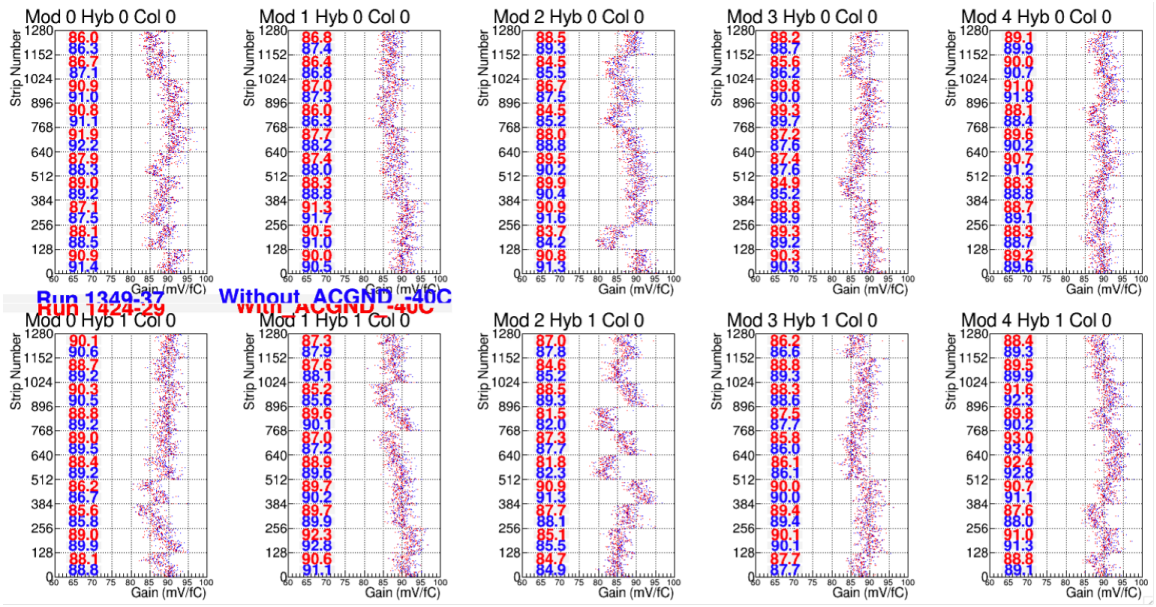
Figure 6.5: Eye diagrams with and without ACGND on data line at 640 Mbps. [70] The scope bandwidth is 1.0 GHz and the probe bandwidth is 1.5 GHz.

noise. While in the cold instance as shown in Fig. 6.6 and Fig. 6.7, removing the ACGND bonds does not have much influence on gain but it does have some influence on input noise. Fig. 6.6 shows that it is safe to remove the ACGND bonds without affecting gain performances. As shown in Fig. 6.7, the input noise tends to be lower in the region affected by the ground loop, especially for Hybrid 0 Column 0s, which are directly under the power board. Removing ACGND does not seem to have much influence on the input noise for other chips on the 5SS stave.

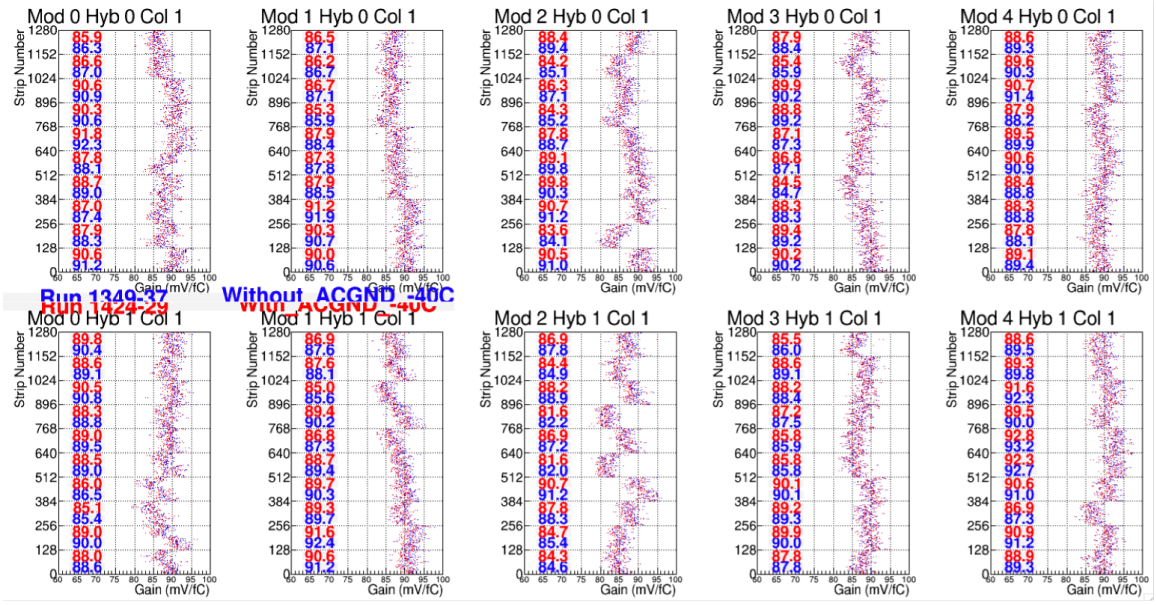
Despite the effect of removing the ACGND bonds on the 5SS stave being not obvious, this approach still shows improvement in regional input noise. This approach was later tested with the fully-loaded LS stave and it did improve the cold noise issue with the BNL stave. [69] Therefore to minimise noise, the wire bonds from the Fast Signal Ground to the hybrids will not be used.

6.2 Magnetic Triggering Studies

The magnetic triggering method is introduced by colleagues at RAL when investigating noise peaks observed in previous studies. [71] As mentioned in Sec. 2.3, a DC-DC converter on the power board is used to convert the 10-11 V coming from the EOS down to 1.5 V. A

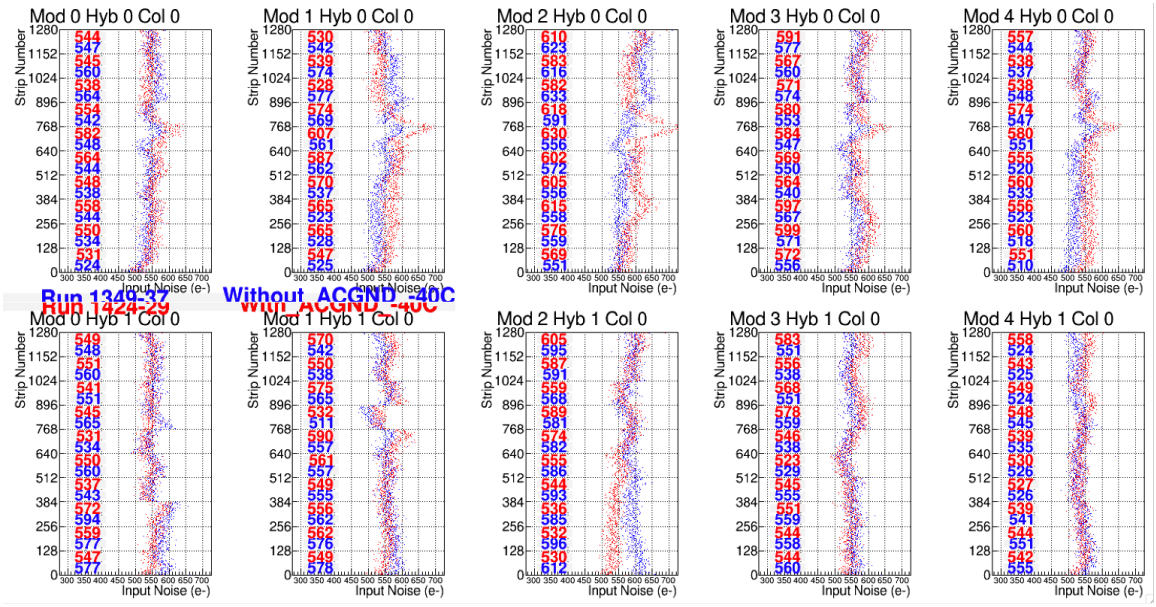


(a) The gain of Column 0 in the 10 hybrids on the 5SS stave cold (-45 °C), with (red) and without (blue) ACGND bonds.

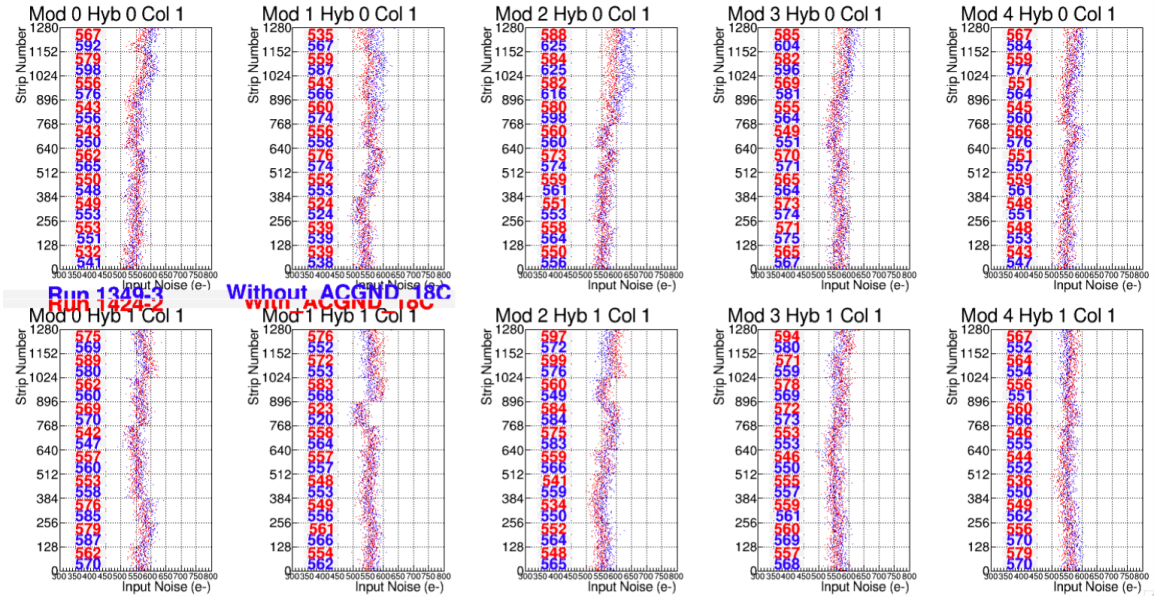


(b) The gain of Column 1 in the 10 hybrids on the 5SS stave cold (-45 °C), with (red) and without (blue) ACGND bonds.

Figure 6.6: Cold gain distributions of the 5SS stave with and without ACGND bonds on.



(a) The input noise of Column 0 in the 10 hybrids on the 5SS stave cold (-45 °C), with (red) and without (blue) ACGND bonds.



(b) The input noise of Column 1 in the 10 hybrids on the 5SS stave warm (-45 °C), with (red) and without (blue) ACGND bonds.

Figure 6.7: Cold input noise distributions of the 5SS stave with and without ACGND bonds on.

linear regulator is used to convert 1.5 V to 1.2 V that is required by AMACs, HCCStars and ABCStars. The DC-DC converter is made of a copper solenoid and the BPOL12V. It is glued directly on top of the silicon sensor, therefore the electromagnetic interference (EMI) noise from the circuit needs to be shielded from the sensor. The EMI noise is a disturbance generated by an external source, the DC-DC converter in this case, that affects an electrical circuit by electromagnetic induction, electrostatic coupling, or conduction. The current shielding consists of an aluminium shield box with continuous solder seams surrounding the components and a copper layer in the PCB underneath. Despite the shielding efforts, the channels connected to the strips directly under the DC-DC converter still show a considerable increase in noise.

The EMI noise is typically at 2 MHz and the module measurements happen asynchronously to the DC-DC frequency. So the overall effect is average over the full range of time bins considering the DC-DC frequency. To study the time dependency of the noise increase relative to the EMI noise frequency, the magnetic trigger [71] uses a magnetic field probe to detect the change in the stray magnetic field (see Fig. 6.8).

The magnetic triggering method works by triggering on the magnetic field emitted from magnetic trigger. The experimental setup is shown in Fig. 6.8. The magnetic field probe is fixed above the power board so that the probe coil roughly aligns with the DC-DC coil. The orientation of the coils are also aligned. The signal from the probe is sent through a radio frequency (RF) amplifier. The signal is then sent into an oscilloscope. The oscilloscope is configured to trigger on the magnetic trigger signal from the probe. The trigger is then sent to a pulse generator to generate a trigger. The trigger is then sent to the data acquisition (DAQ) FPGA to be used as trigger for the module data taking. General Purpose Interface Bus (GPIB) control of the pulse generator allows fine segmented delays to be applied. Or alternatively as mostly adopted in this section, the latency configuration of the ABCStar chips are scanned instead of the trigger delay. The latency granularity is the LHC bunch crossing time (25 ns) per count. By scanning latency, the length of internal data pipeline is adjusted, thus adjusting the trigger phase relative to the DC-DC switching. [71] The triggering method is explained in Fig. 6.9.

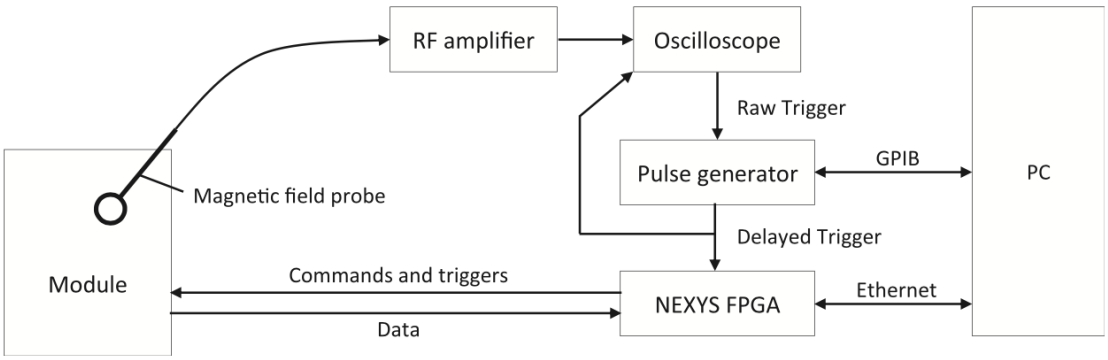


Figure 6.8: Schematic of the magnetic triggering test setup on a module. [71]

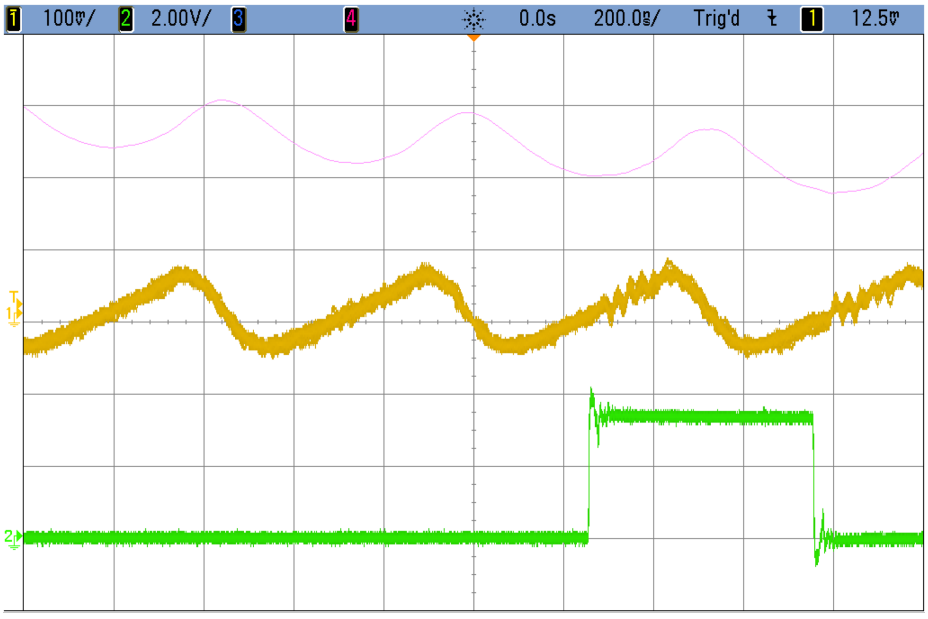
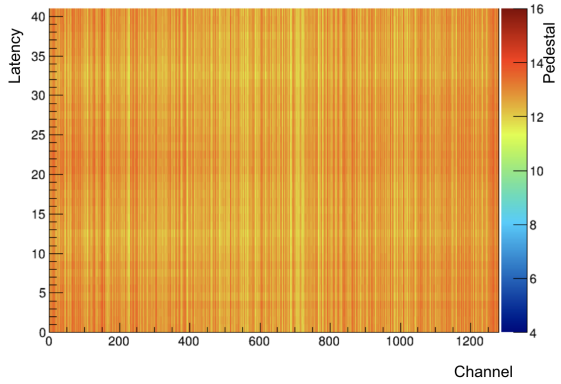


Figure 6.9: An oscilloscope image during a magnetic triggering test. Channel 1 (yellow) is the voltage signal from the probe which the scope triggers on. Channel 2 (green) is the trigger signal from the pulse generator which is sent to the DAQ system. The purple line is integrated magnetic probe signal. [71]

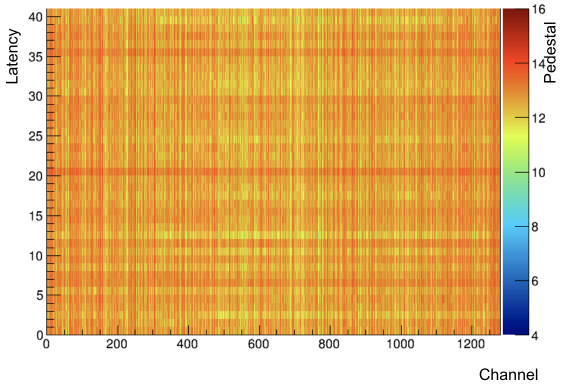
As discussed in Chapter 2 and Chapter 3, the chip response with no charge injection is called pedestal. For each of a number of set thresholds covering the expected pedestal region, the latency (named delay) is scanned relative to the external trigger from the pulse generator. At each threshold and latency, the occupancy is measured. The mean occupancy at each threshold is obtained with internal DAQ triggers, independent of the magnetic triggering. This is used as a baseline. The occupancy obtained during the delay scan is then normalised against the baseline. At each latency, an S-curve is formed with threshold and occupancy for each channel. With the S-curve, the pedestal VT50 and sigma for each channel at a certain latency is calculated and used as indicators for EMI noise. The increase in pedestal VT50 itself might not be considered as noise increase. But as the module data taking is normally independent of the DC-DC frequency, pedestal VT50 increase in only certain latency will manifest as noise in overall module performance.

Since the EMI noise comes from the DC-DC converter, the strips are separated to two types, the group directly under the DC-DC converter and the group away from the DC-DC converter and power board. According to previous studies [71], the EMI does not only affect the strips directly underneath but also causes noise increase on the strips away from it, but to a much lesser degree. As for the power boards in EoS region, they only have negligible influence on modules nearby. This is tested on the 5SS stave (see Fig. 6.1) with Module 12. The results on hybrid 0 are shown in Fig. 6.10. (Hybrid 1 results are omitted as they have very similar performances.) It can be seen that the time dependency of noise (which manifests as horizontal strips in the plots) is very marginal. It is to be expected due to two reasons. The first one is the physical separation between the sensors and the converter. The second reason is that the converters in the EoS region converts 11 V to 2.5 V or 2.5 V to 1.2 V. The voltage factor is lower that those on a module (11V to 1.5 V), which would in turn induce smaller switching signal. The most direct source of EMI noise comes from the power boards on the same module.

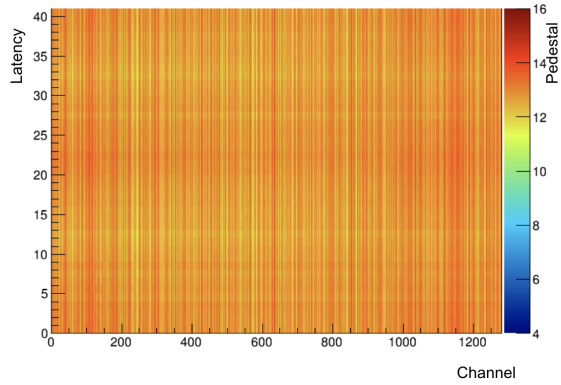
In this section, the influence of removing ACGND bonds and removing capacitors between the strip side rail and the module ground have on time dependent EMI noise are studied and results are presented in Sec. 6.2.1 and Sec. 6.2.2.



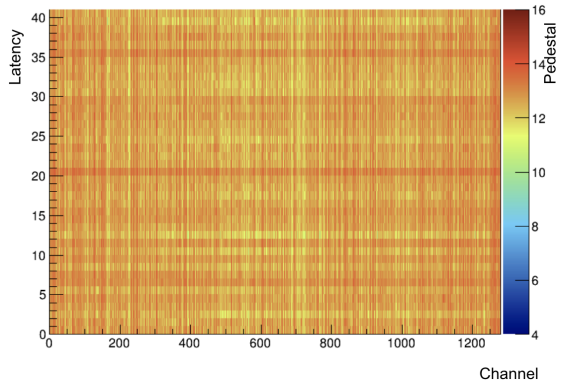
(a) The pedestal vt50 distribution of Module 12 hybrid 0 stream 0 when triggering on the 11 V to 2.5 V converter in the EOS region.



(b) The pedestal vt50 distribution of Module 12 hybrid 0 stream 0 when triggering on the 2.5 V to 1.2 V converter in the EOS region.



(c) The pedestal vt50 distribution of Module 12 hybrid 0 stream 1 when triggering on the 11 V to 2.5 V converter in the EOS region.



(d) The pedestal vt50 distribution of Module 12 hybrid 0 stream 1 when triggering on the 2.5 V to 1.2 V converter in the EOS region.

Figure 6.10: Pedestal vt50 distributions with regard to channel numbers and latency on M12 hybrid 0 when triggering on the two DC-DC converter coils in the EOS region.

6.2.1 Influence From ACGND Bonds

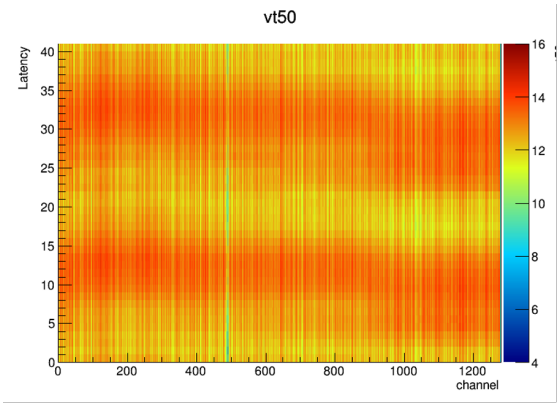
As discussed in Sec. 6.1, the ACGND bonds need to be removed due to increased stave noise in the cold temperature. This study is to show the influence of removing ACGND bonds have on EMI noise from the DC-DC converter. This test is performed on the 5-SS stave in room temperature with chiller setting at 17 °C. Magnetic triggering tests are performed on Module 12 and Module 11 to obtain the pedestal versus channel and latency plot similar to Fig. 6.10. As Module 11 and Module 12 give similar performances, the results from Module 12 are shown in Fig. 6.11 as an example.

The hybrid (where the power board and DC-DC converter are mounted) is glued to stream 0s. So stream 0 results are expected to show larger EMI noise influence. As shown in Fig. 6.11, removing ACGND bonds generally changes the pattern in vt50 vs latency and channel number. It also causes the noise increase to be more regional to certain latency, as in the horizontal strips becoming "flatter". This means that the noise performance across module is more uniform, which is a welcome change. This effect is presumably caused by the fact that there is only one intended ground across the module after removing ACGND bonds. This effect is more visible to stream 0 channels as expected. Despite the slight regional noise increase, removing ACGND bonds enhances the uniformity in performances across the module. This provides further evidence that ACGNDs should be not be used in future production process.

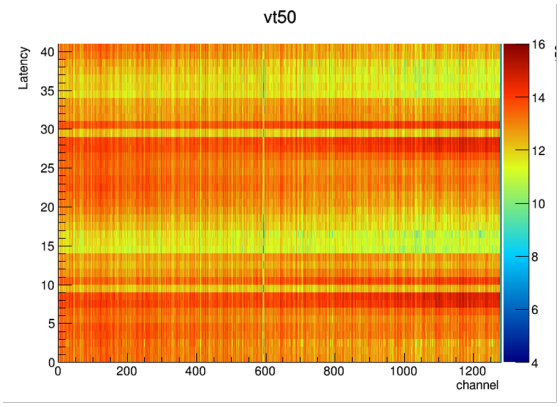
6.2.2 Influence From Capacitors

There are four capacitors between the strip side bias rail and the module ground. They are known to introduce noise in AMAC measurements of the sensor leakage currents on the same module. There is a proposal not to use these capacitors and the effect of this change on the module noise was studied in these tests. The results are shown in Fig. 6.12.

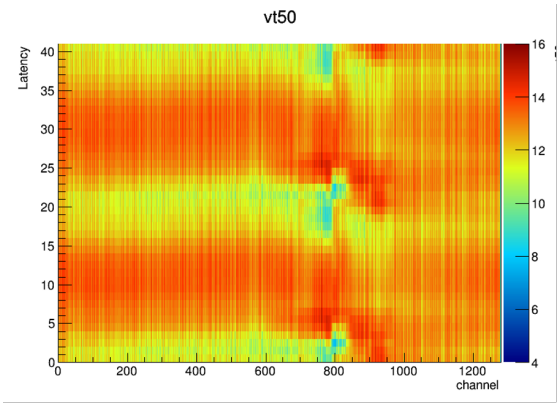
The test is performed on Module 8 on the 5-SS stave by removing the four capacitors on hybrid 0 and comparing the module performance before and after. The time dependent noise feature is shown in Fig. 6.12. Since stream 0 and stream 1 have similar performances



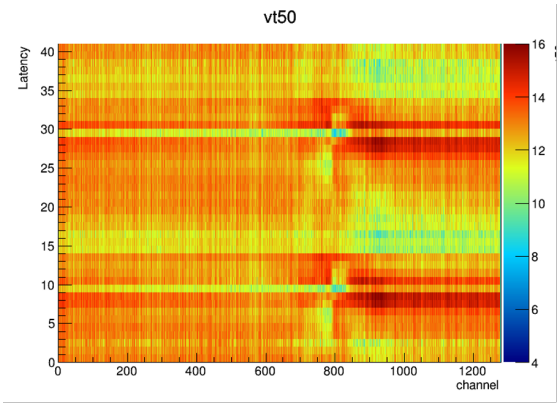
(a) Pedestal vt50 (z axis) distribution for Module 12 hybrid 0 stream 1 with ACGND bonds.



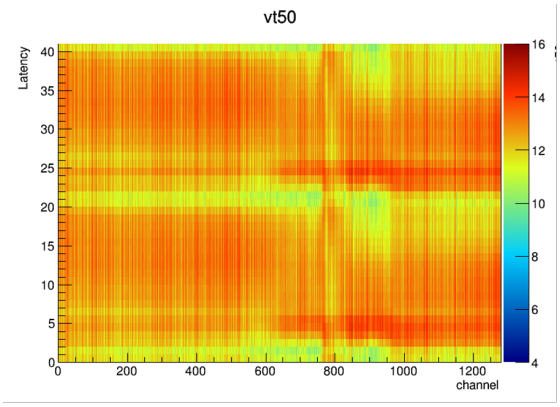
(b) Pedestal vt50 (z axis) distribution for Module 12 hybrid 0 stream 1 without ACGND bonds.



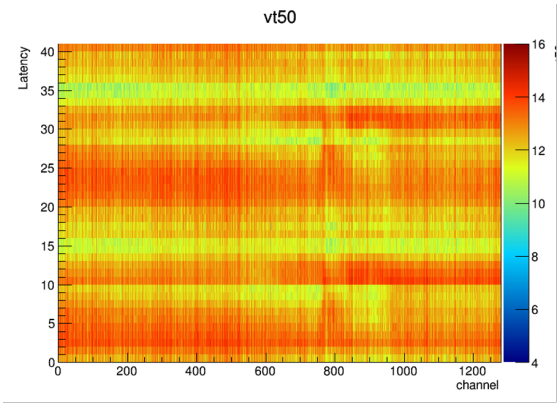
(c) Pedestal vt50 (z axis) distribution for Module 12 hybrid 0 stream 0 with ACGND bonds.



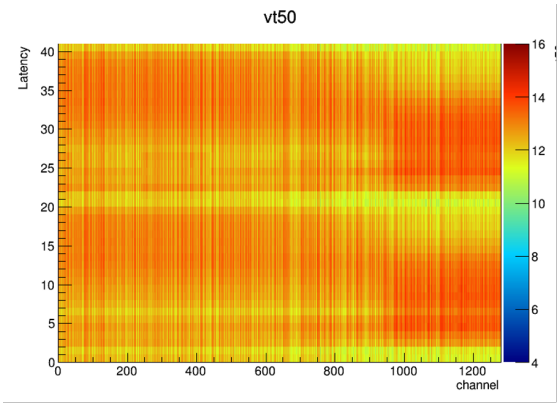
(d) Pedestal vt50 (z axis) distribution for Module 12 hybrid 0 stream 0 without ACGND bonds.



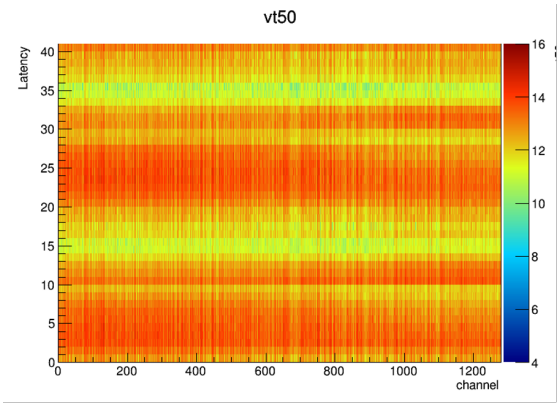
(e) Pedestal vt50 (z axis) distribution for Module 12 hybrid 1 stream 0 with ACGND bonds.



(f) Pedestal vt50 (z axis) distribution for Module 12 hybrid 1 stream 0 without ACGND bonds.

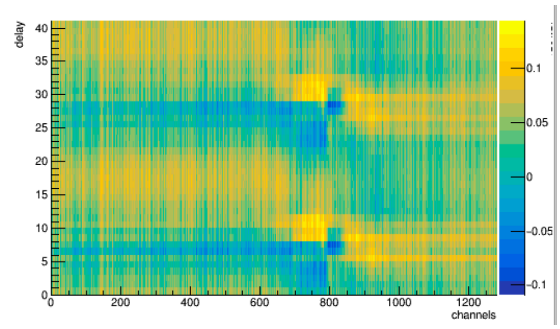


(g) Pedestal vt50 (z axis) distribution for Module 12 hybrid 1 stream 1 with ACGND bonds.

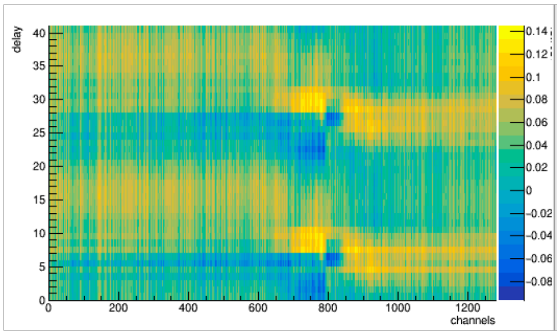


(h) Pedestal vt50 (z axis) distribution for Module 12 hybrid 1 stream 1 with ACGND bonds.

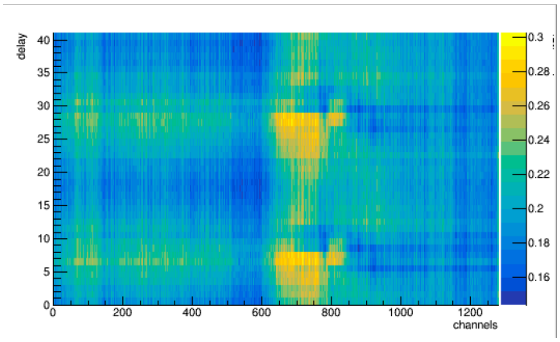
Figure 6.11: Pedestal vt50 (z axis) distributions with regard to channel numbers and latency for Module 12, with and without ACGND bonds.



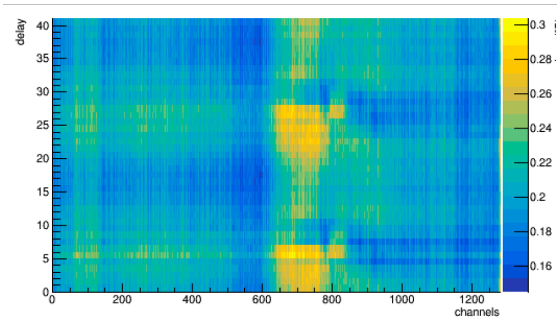
(a) The pedestal distribution of Module 8 hybrid 0 stream 0 before removing the capacitors.



(b) The pedestal distribution of Module 8 hybrid 0 stream 0 after removing the capacitors.



(c) The sigma distribution of Module 8 hybrid 0 stream 0 before removing the capacitors.



(d) The sigma distribution of Module 8 hybrid 0 stream 0 after removing the capacitors.

Figure 6.12: Pedestal vt50 and sigma distributions with regard to channel numbers and latency on M8 hybrid 0 stream 0 before and after removing the capacitors.

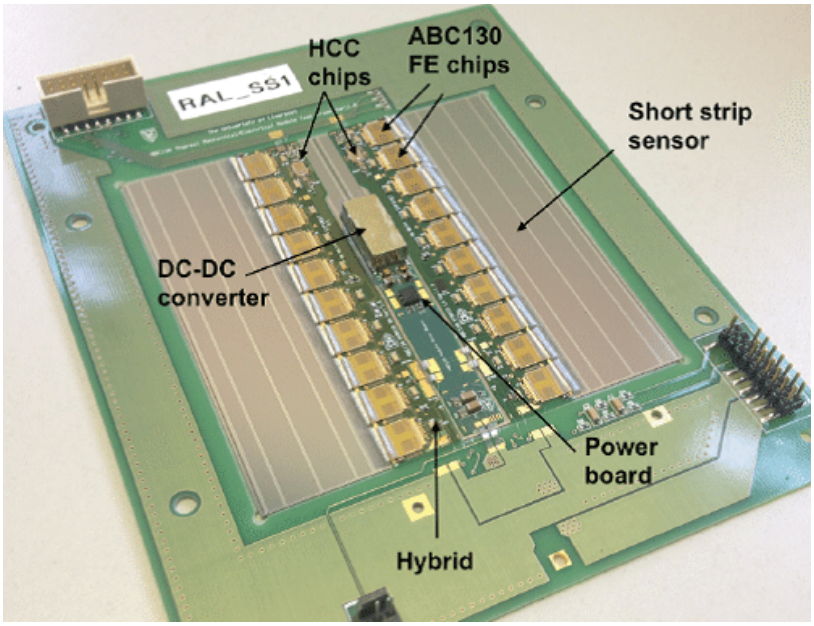


Figure 6.13: Short-strip barrel module with test structure (green frame). [13]

and time dependent noise is more visible for stream 0 channels, stream 0 pedestal relative to channel numbers and latencies is used as example. In Fig. 6.12, the pedestal VT50s before and after removing capacitors are shown in Fig. 6.12a and Fig. 6.12b. The sigmas before and after removing capacitors are shown in Fig. 6.12c and Fig. 6.12d. Comparing the performances before and after, there are no obvious performance changes in the time dependent noise. This test provides further evidence for not using these capacitors to reduce noise in AMAC measurements of the sensor leakage currents.

6.3 Modules on Stave

Stave 25 is another SS stave assembled at RAL in 2021. It was loaded with 7 modules to have a half-full side, then later loaded to have a fully-loaded side. When the stave is half-loaded (seven modules, positioned M0-M6), the performances of modules on-stave and standalone are compared to validate that module performance is not jeopardised on stave.

The modules are tested off-stave on a standalone module testing setup with a custom PCB, as shown in Fig. 6.13. The test setup can be put in cooling boxes as show in Fig. 3.3. The tests used in this study are done in room temperature, the same as the on-stave tests.

The gain comparisons on-stave and standalone for the 14 hybrids on Stave 25 are shown in Fig. 6.14. It can be seen that the performance is largely consistent on-stave and standalone for most hybrids. This is consistent with the expectation that modules still perform adequately after being mounted on the stave. This test was repeated after Stave 25 is fully populated with modules. The results remain similar with the 7-module instance, and are shown in Appendix A.2.

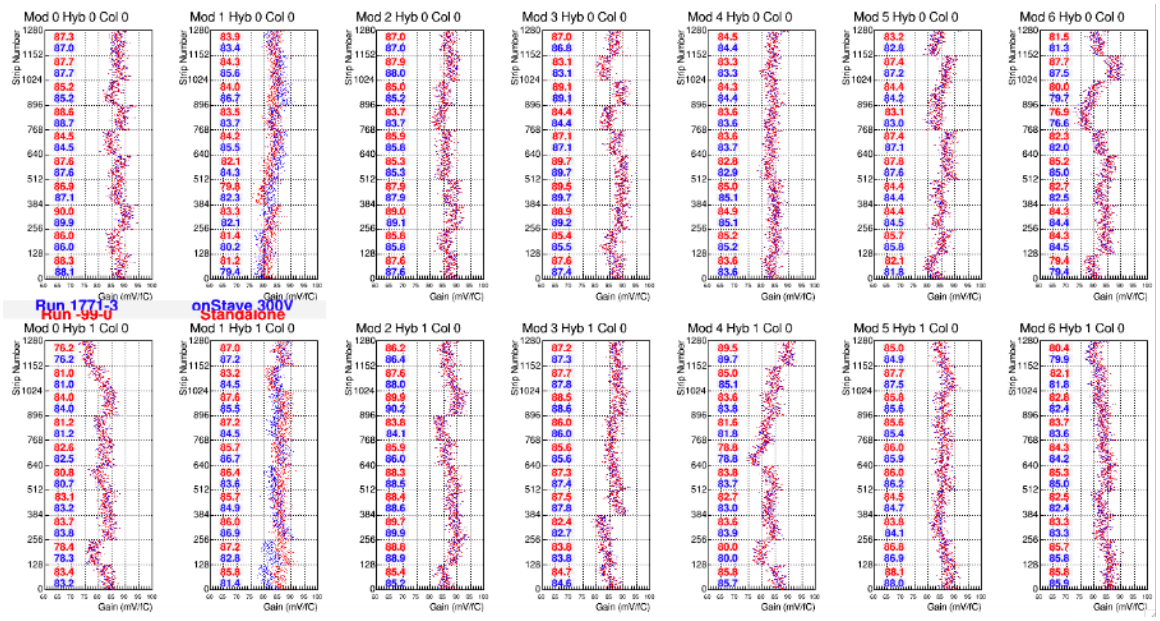
The input noise distributions of the 14 hybrids on-stave and standalone are shown in Fig. 6.15. It can be seen that there is some difference between the input noise on-stave and standalone. Especially for Column 0 sections that are under the power board, the difference on-stave and standalone is the most obvious.

6.4 System Test

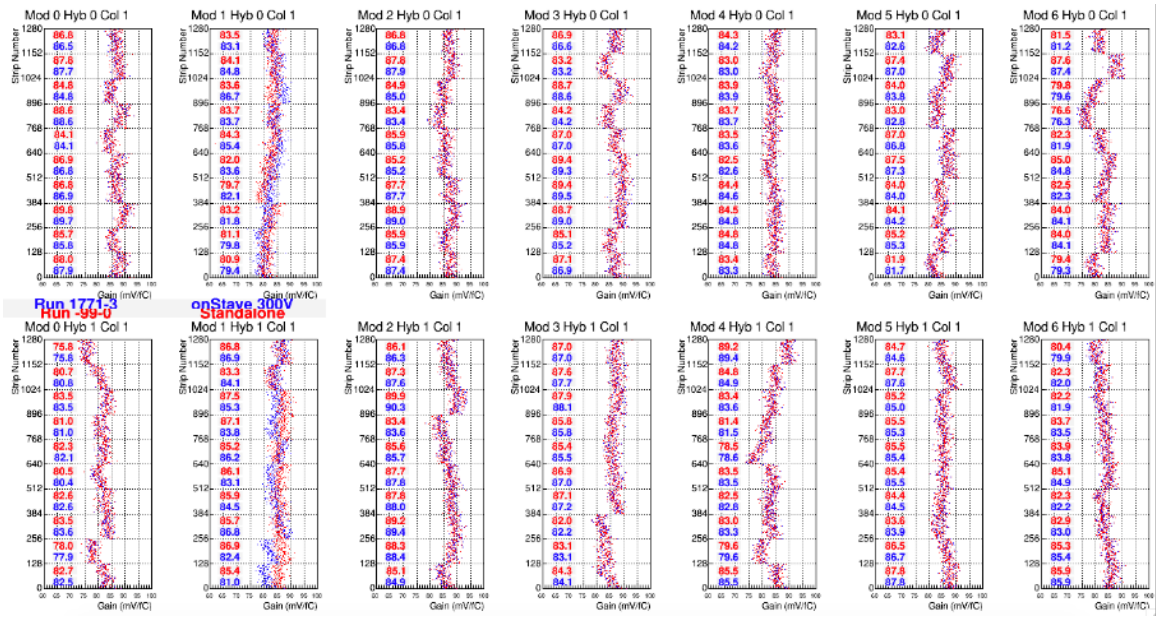
As discussed before, the stave system test is being setup at CERN. A double-sided LS stave is setup and tested to begin the system test. The VTRX+ and lpGBT performance tests on-stave were not set up before. In ATLAS operation, long-term degradation on VTRx+ from radiation damage is expected. This effect needs to be monitored. The system test is used to develop the tools to perform this long-term monitoring. In this section, first studies are made to prove feasibility of monitoring VTRX+ and lpGBT performances during operation.

For the VTRX+ on-stave monitoring, LI scans were performed for the VTRX+ on the CERN stave. The I^2C link was used to turn off the modulation current and change the bias current. The optical power was monitored by the miniPOD [1] at the receiver end of the optical link. The result of the LI scan is shown in Fig. 6.16. The curve is fitted with a linear function Equ. 5.8 in the range of 0.2 - 1.5 mA. The turn on point is calculated to be 0.241 $\pm$ 0.042 mA. The slope is 0.368 $\pm$ 0.015 mW/mA. The uncertainties are the statistical from the fit. As discussed in Sec. 5.3, the average linearity is 0.2948 $\pm$ 0.0318 mW/mA and the average turn-on point is 0.3738 $\pm$ 0.0033 mA. The uncertainties are also statistical. There is device

[1] The MiniPOD used here is a Twelve-Channel, Pluggable, Parallel-Fiber-Optics Receiver.

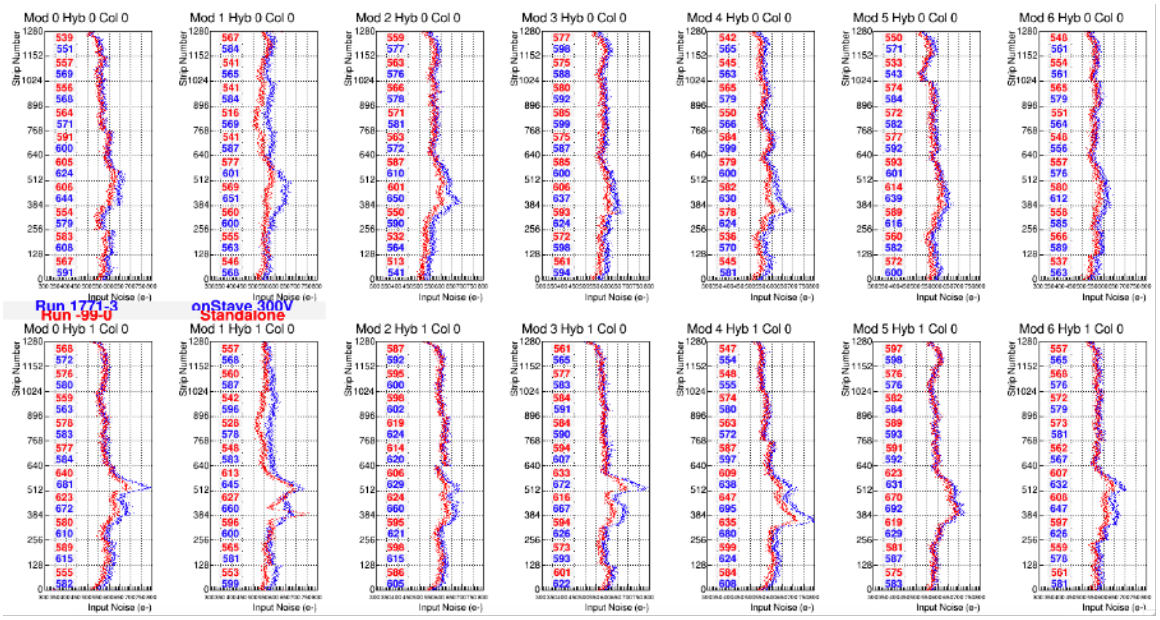


(a) The gain distributions of Column 0 in the 14 hybrids on Stave 25 on-stave (blue) and standalone (red).

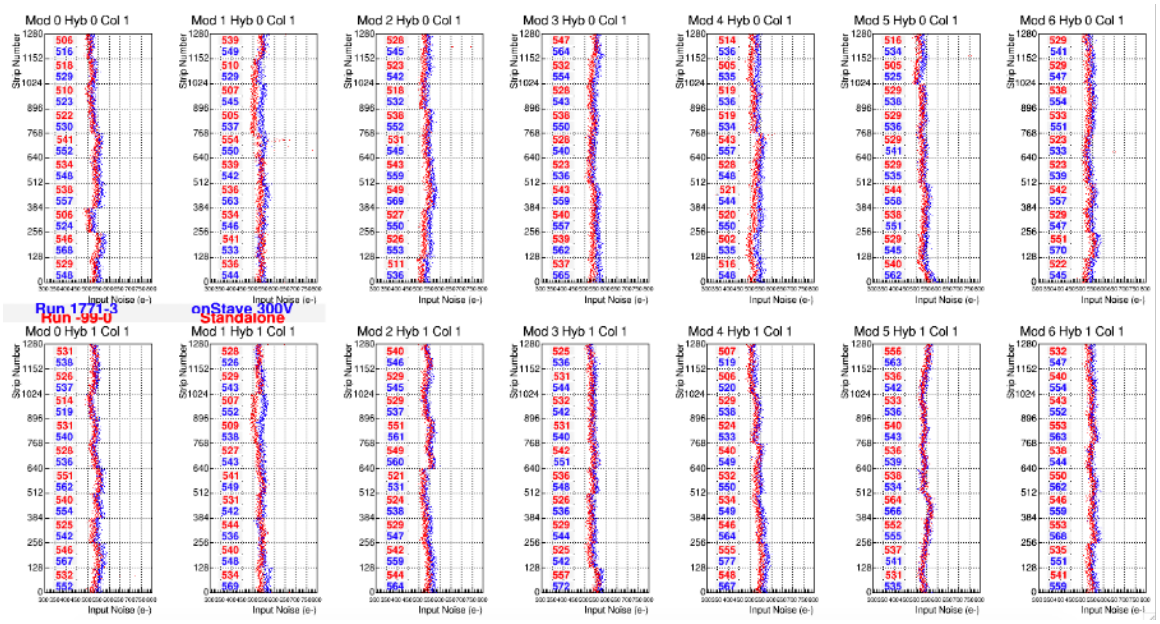


(b) The gain distributions of Column 1 in the 14 hybrids on Stave 25 on-stave (blue) and standalone (red).

Figure 6.14: The gain distributions of the 14 hybrids on Stave 25 on-stave and standalone.



(a) The input noise distributions of Column 1 in the 14 hybrids on Stave 25 on-stave (blue) and standalone (red).



(b) The input noise distributions of Column 1 in the 14 hybrids on Stave 25 on-stave (blue) and standalone (red).

Figure 6.15: The gain distributions of the 14 hybrids on Stave 25 on-stave and standalone.

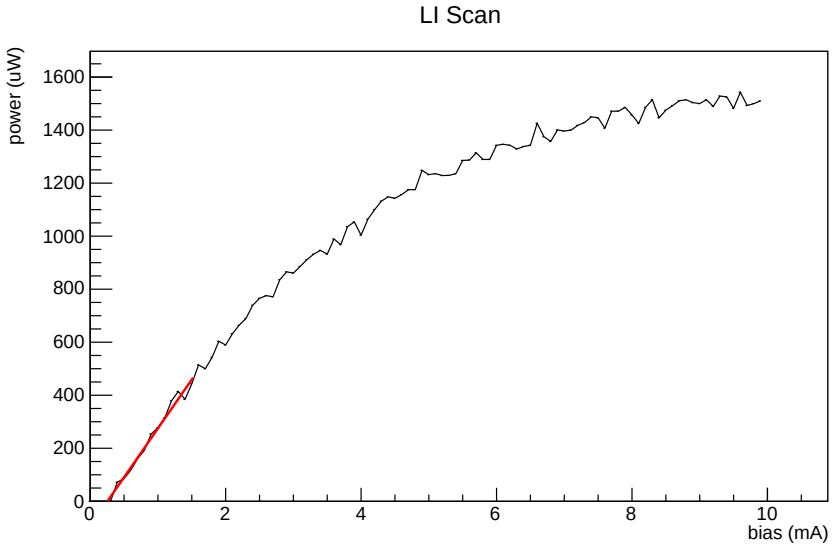


Figure 6.16: LI curve for the VTRX+ on the LS stave used in CERN system tests.

to device variation for slopes and turn-on points. So there is no reason to expect the identical threshold and slope efficiency for each VCSEL. But it can be seen that the on and off-stave measurements agree with each other.

As proven with this test, LI scans can be taken with on-stave VTRX+ amidst other tests. This will be integrated into online monitoring during ATLAS operation to observe any changes in the VTRX+ laser performances.

6.5 Sanity Checks

Without encoding, there is a long "quiet" time with a long string of 0s or 1s in the system, which is hard to automatise the clock recovery process. Clock recovery is the process of extracting timing information from a serial data stream. It allows the timing of the data in the stream to be determined without separate clock information. [72] To avoid this issue, 8b/10b encoding [73] is introduced. The performance of this encoding approach has been tested (as discussed in Appendix A.1) and there were no unexpected effects to the system.

The HV and LV input voltages are usually set to around 400 V (for full depletion) and 11 V in operation. Varying these input voltages can influence the performance of modules. This study is performed on a partially loaded stave and the results are shown in Appendix

A.3. While the HV input has an obvious influence on input noise, LV and HV inputs do not have obvious effects on the gain. When the LV input changes from 9 V to 11 V, there is no obvious change on input noise either.

6.6 Outlook

As discussed in this chapter, many different tests have been developed and performed to ensure the performance of a single ABCStar stave. Many problems are discovered in this stage and hardware designs are often required to make changes to improve performances. As of the current stage, RSSI readings of the VCSEL output signal are achieved. This RRSI is the same power signal and VCSEL RSSI studied in Chapter 5. But the system still needs to be calibrated. The RSSI readings have demonstrated the feasibility of long-term RSSI monitoring. As more staves are assembled and ready for testing at CERN, more system tests, including those on the optical links, are planned for the future.

7 | Conclusion

In this thesis, different parts of a ITk Strip Barrel stave are tested to ensure the overall performance of the stave system. This work is focused on testing performances of components on a stave and prepares for future system tests.

In Chapter 2, the pre-irradiation study results and the voltage-frequency operation window study results are presented. The idea of using pre-irradiation to reduce the increase in digital current was tested successfully. The temperature is shown to have a larger influence on voltage-frequency operation window than radiation.

Chapter 3 includes data analysis results on data taken in Sept. 2019. Calibration was studied to determine signal and noise amplitude. Issues with the calibration are found. The issue is bypassed by using calibration data from other chips. Pedestal data is taken when there is no beam on, and is used to study noise at cold and warm temperatures. The signal is taken with an electron beam at 5.4 GeV energy at cold and warm temperatures as well. There is no obvious cold/warm difference in signal but there is a noticeable difference for noise measurements. The noise is compared with previous studies and they agree within systematic errors. The signal data is then compared with simulation results after energy corrections. The corrections include charge sharing and the difference between MPV and VT50. After energy correction, the data agrees with the simulation results within uncertainties. The operational region is determined at cold and warm temperatures. The region, where the efficiency is sufficiently high and the noise rate is low, is wide.

The module pulse shape studies are also included in Chapter 3. The signal pulse in modules are designed to cover 2 bunch crossings to minimise both noise and pile-up with the 01X operation mode. The results are compared with theoretical calculations and approximate theoretical simulation. The results agree with the theoretical calculations quite well.

To achieve automatic electrical and dimensional performance tests on a 1.4 m long bus tape, a tape tester robot is developed and discussed in Chapter 4. Software and test procedures were developed. The calibration procedures developed were of critical importance. Calibration results were also validated. Test results were obtained and statistical analysis procedure was

set up using the data collected from pre-production tapes.

Chapter 5 discusses the VTRx+ reliability test results. Reliability tests are performed at room temperature for BER studies, VCSEL RSSI studies and VTRx+ TX studies. Using accelerated aging tests, BER tests were performed again. LI scans at 85 °C / 85 % RH are also performed. RSSI and LI studies validates the methodology for monitoring long-term VTRx+ performances on-stave.

Final validation of the ITk strip system use the operation of a multiple-stave system to look at all aspects of system performances. In Chapter 6, one-stave results of multiple performance validation tests are presented. The performance of a single stave system is as expected. The multiple-stave testing system is planned to be set up in 2023.

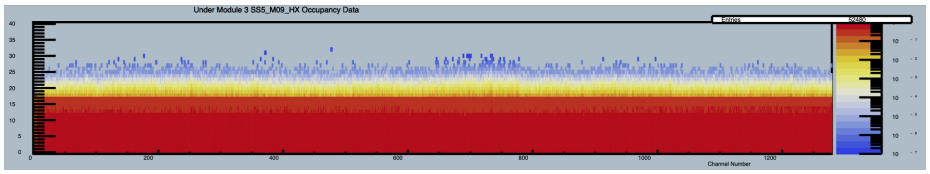
A | Other Stave Results

A.1 8b/10b Verification

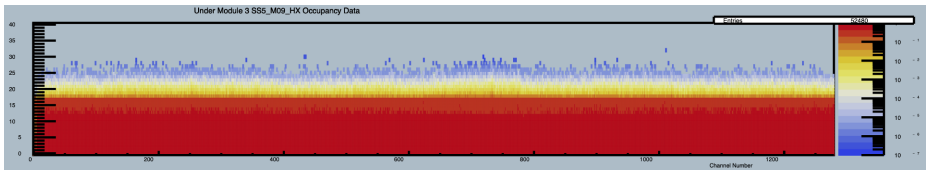
As mentioned in Chapter 2.5, the performance of 8b/10b encoding approach was tested and there were no unexpected effects to the system. The typical responses with and without encoding for a hybrid shown in Fig. A.1. As can be seen from Fig. A.1, there is no obvious difference in module performance after using the 8b/10b encoding. This verifies the legitimacy of this encoding approach in ITk strip.

A.2 Full Populated Stave 25 On-stave and Standalone Module Performance Comparison

As mentioned in Sec. 6.3, Stave 25 was later fully populated with modules. Comparisons of module performance on-stave and in standalone tests are made. The gain comparisons on and off stave for the all 28 hybrids on Stave 25 are shown in Fig. A.2. The input noise distributions of the 14 hybrids on and off stave are shown in Fig. A.3. As can be seen, the performance is largely the same as what is shown in Sec. 6.3 across the stave.

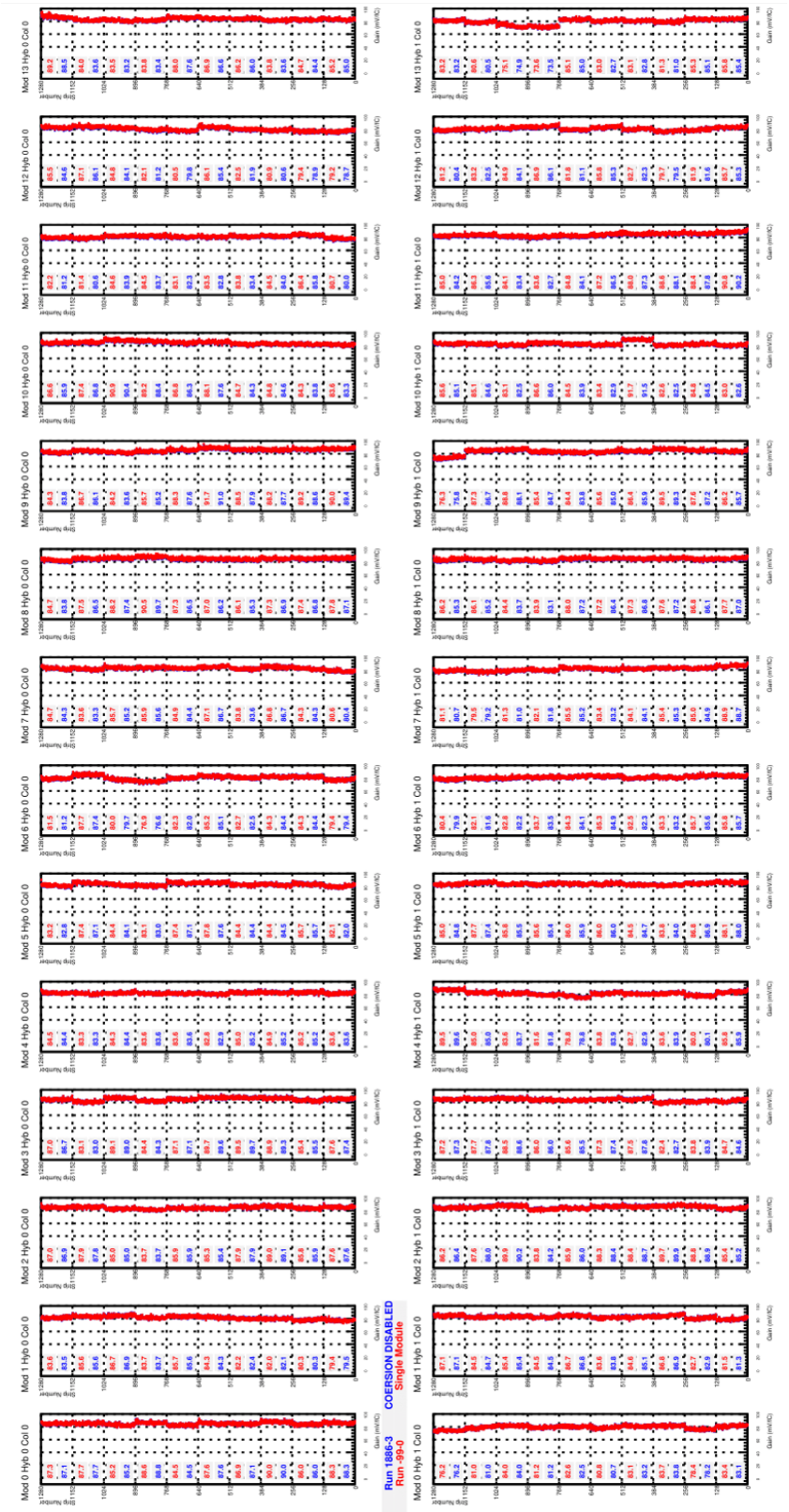


(a) A typical hybrid performance without encoding

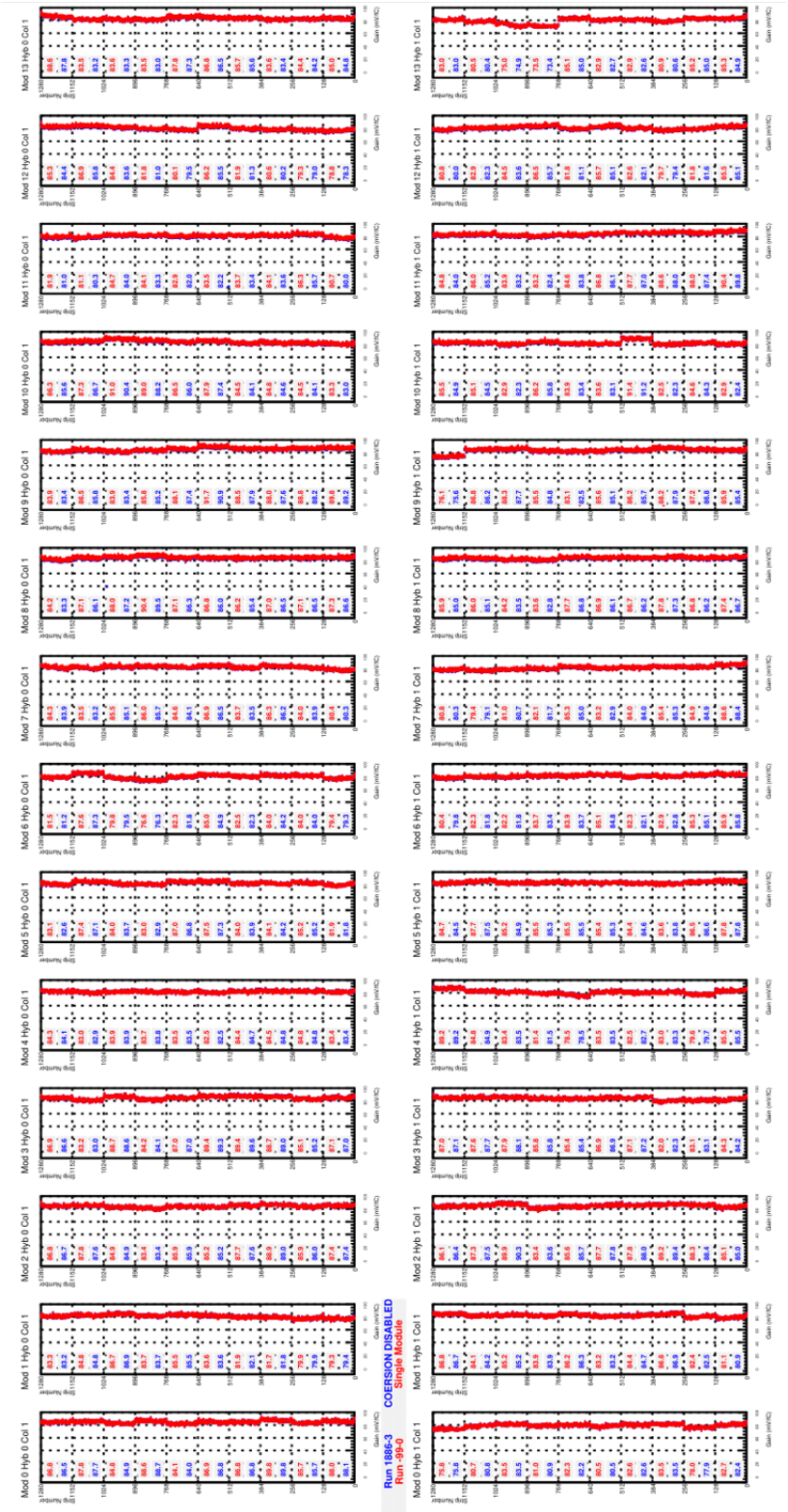


(b) A typical hybrid performance with 8b/10b encoding

Figure A.1: The performance of the same hybrid with and without 8b/10b encoding.

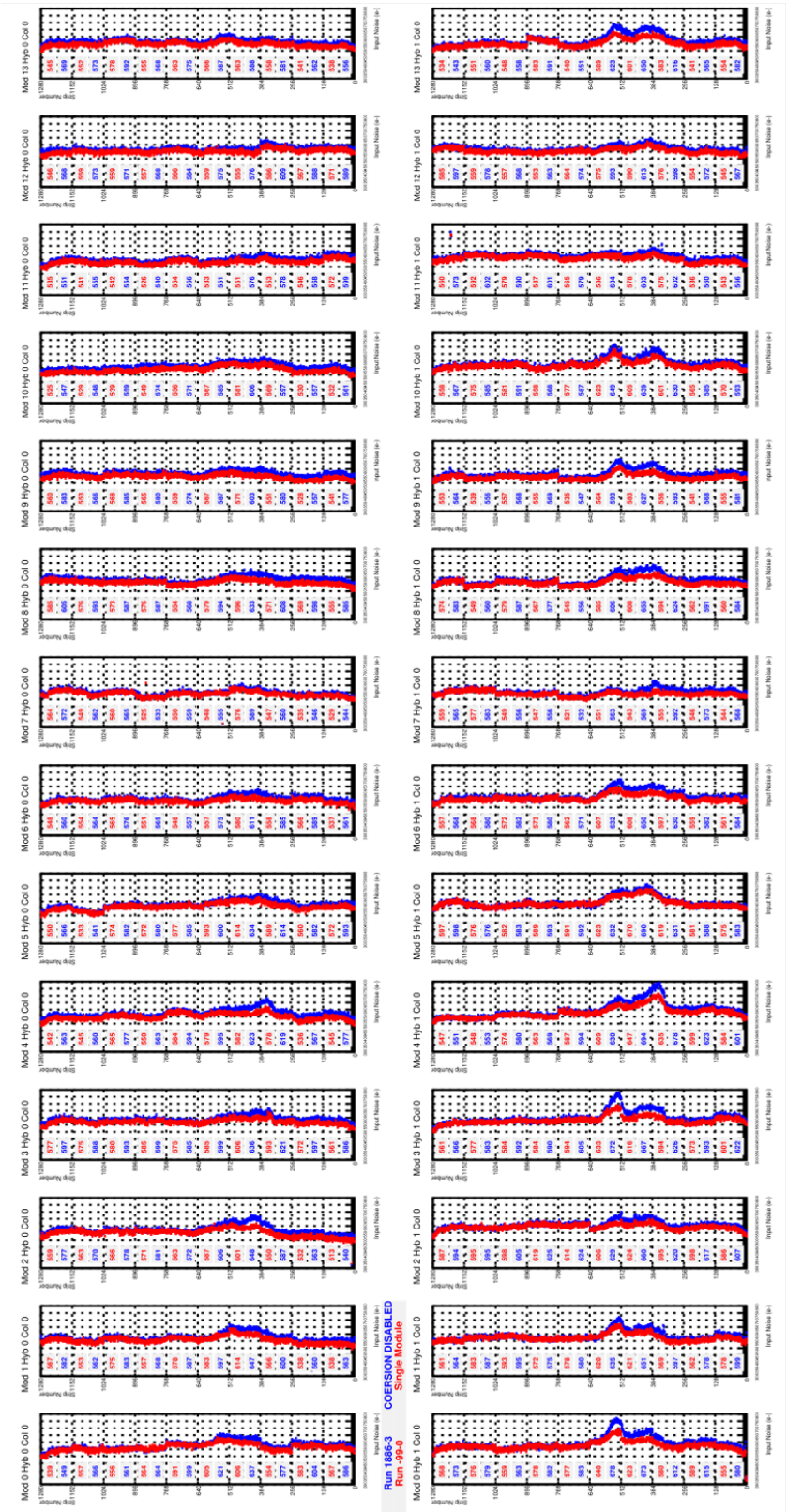


(a) The gain distributions of Column 0 in the 28 hybrids on Stave 25 on (blue) and off-stave (red).

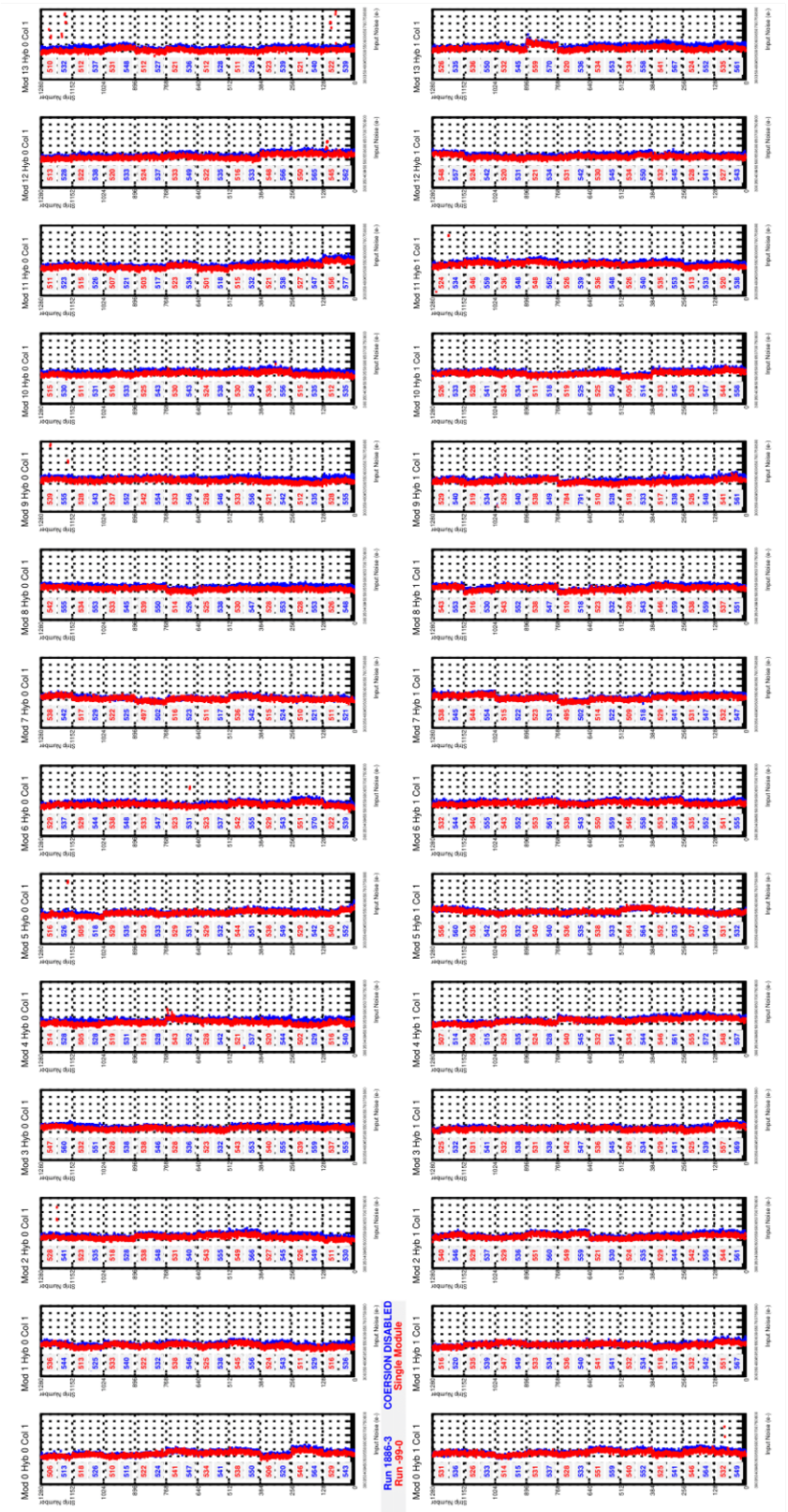


(b) The gain distributions of Column 1 in the 28 hybrids on Stave 25 on (blue) and off-stave (red).

Figure A.2: The gain distributions of the 28 hybrids on Stave 25 on and off-stave.



(a) The input noise distributions of Column 1 in the 28 hybrids on Stave 25 on (blue) and off-stave (red).



(b) The input noise distributions of Column 1 in the 28 hybrids on Stave 25 on (blue) and off-stave (red).

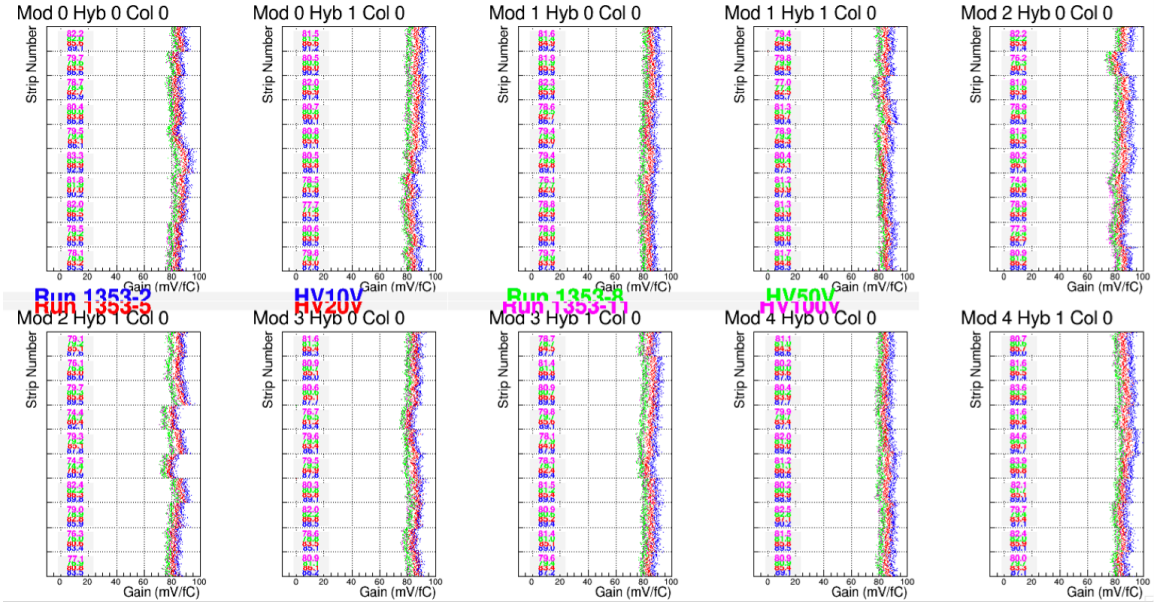
Figure A.3: The gain distributions of the 28 hybrids on Stave 25 on and off-stave.

A.3 5SS HV and LV Input Studies

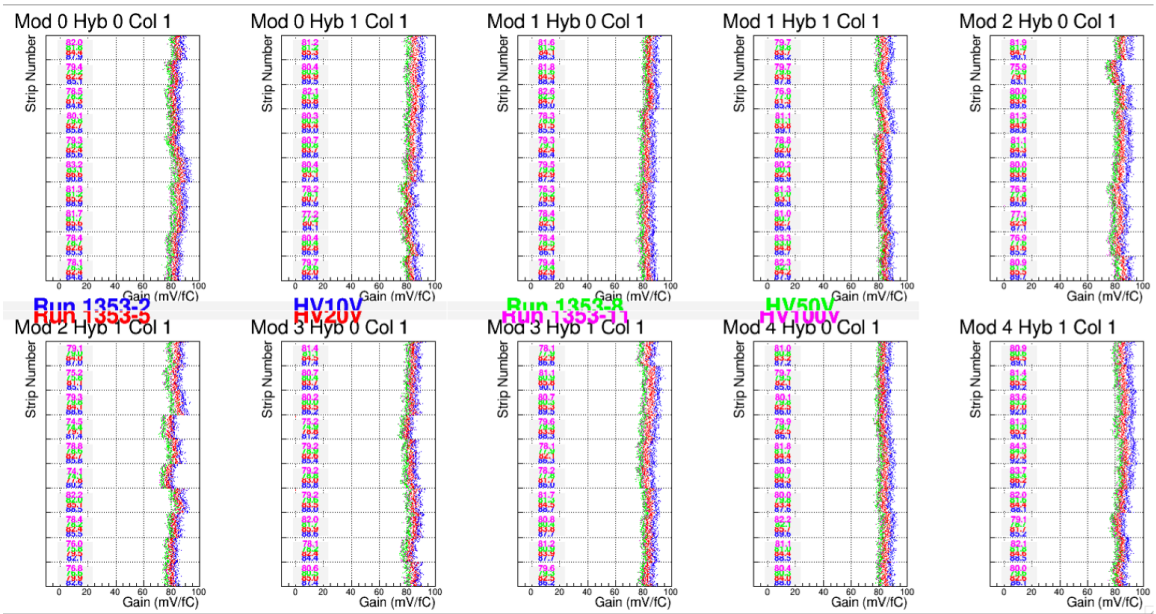
The sensor is fully biased at around 400 V HV input and the module LV input is around 11 V. Varying these voltage inputs can influence the module performances, as expected.

In this study, the HV bias voltage is varied for the 5SS stave (see Sec. 6.1). The response from the 5 modules on stave is shown. The gain comparisons for the 10 hybrids on 5SS stave when the HV is set to 10 V, 20 V, 50 V and 100 V are shown in Fig. A.4. The input noise comparisons for the 10 hybrids on 5SS stave when the HV is set to 10 V, 20 V, 50 V and 100 V are shown in Fig. A.5. The LV input is set to 11 V in these tests. While the gain does not show obvious differences between various HV settings, the input noise obviously decreases with the increase of HV bias voltage. As the bias voltage increases, the fully depleted region increases until fully depleted (around 400 V for un-irradiated sensors), resulting in the decrease of input noise.

Then the HV is fixed at 10 V for the LV variation studies. The LV is set to be 9 V, 10 V, and 11 V and the module responses are recorded for the 10 hybrids on the 5 SS stave. The gain comparisons with the three LV input voltage settings are shown in Fig. A.6 and the input noise comparisons are shown in Fig. A.7. It can be seen that the gain does not show obvious change with the change of LV inputs. The input noise also does not show obvious change when the LV input goes from 11 V to 9 V.

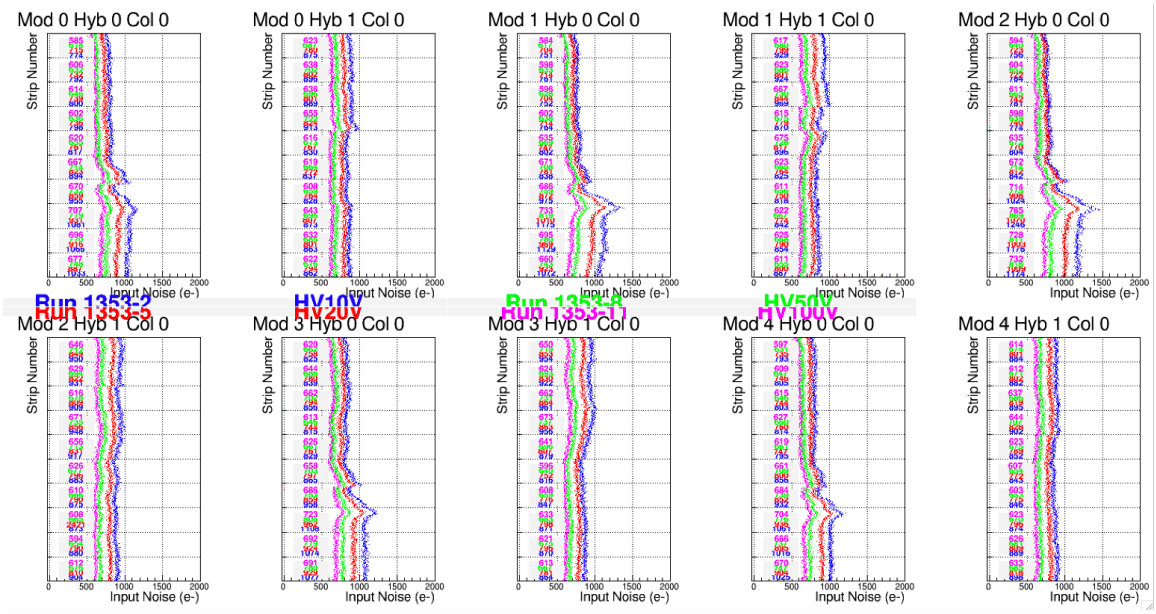


(a) The gain distributions of Column 0 in the 10 hybrids on 5SS when the HV is set to 10 V (blue), 20 V (red), 50 V (green) and 100 V (pink).

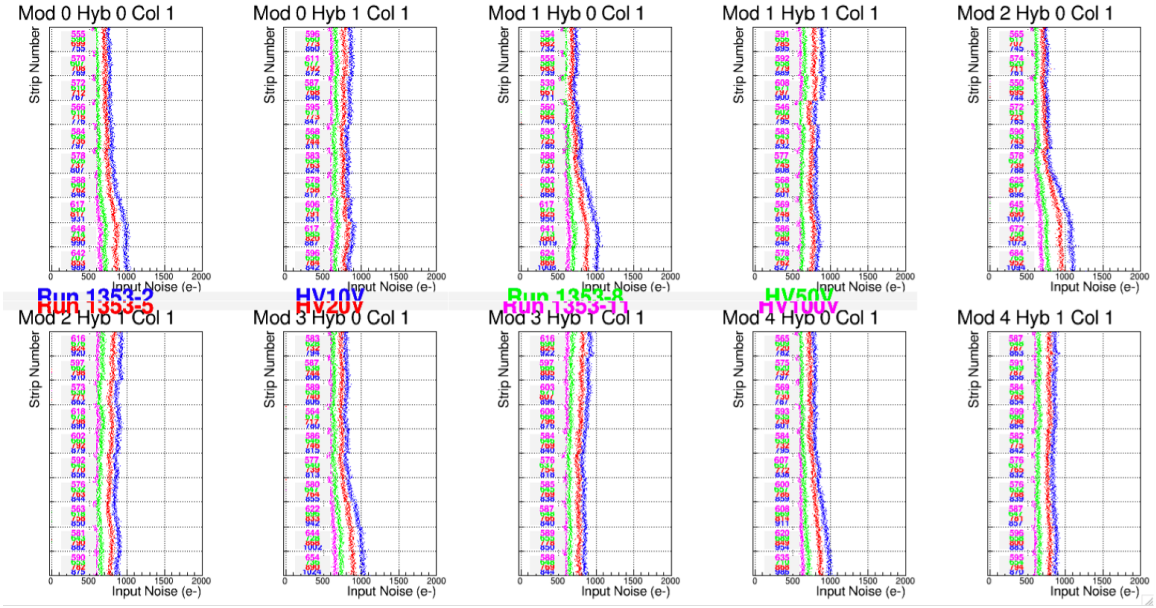


(b) The gain distributions of Column 1 in the 10 hybrids on 5SS when the HV is set to 10 V (blue), 20 V (red), 50 V (green) and 100 V (pink).

Figure A.4: The gain distributions in the 10 hybrids on 5SS when the HV is set to 10 V (blue), 20 V (red), 50 V (green) and 100 V (pink). The LV is set to 11 V for these tests.

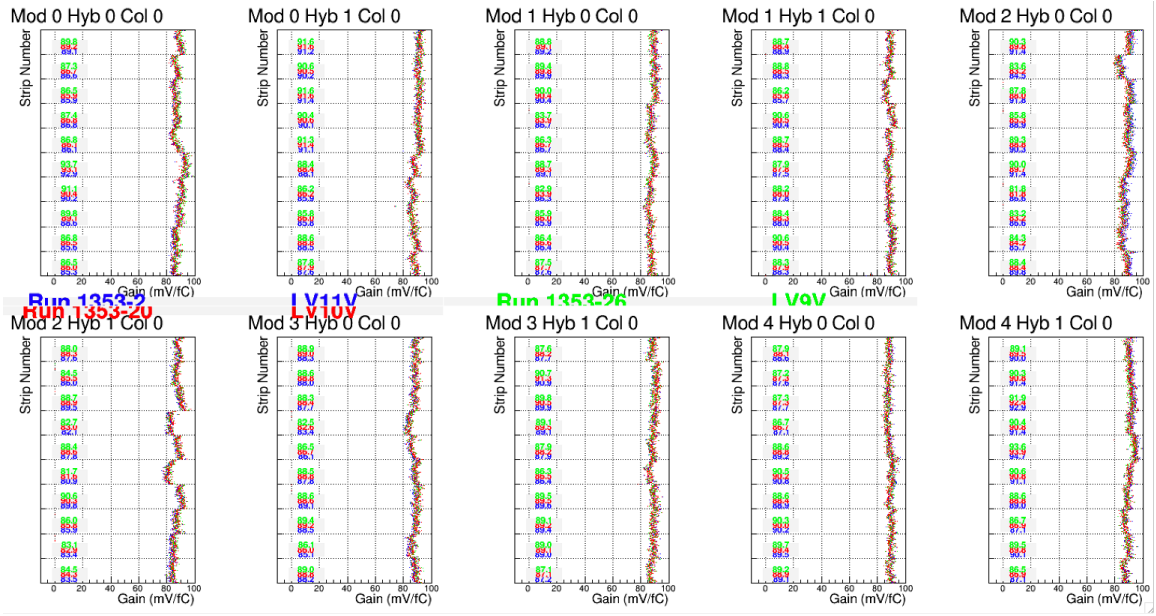


(a) The input noise distributions of Column 0 in the 10 hybrids on 5SS when the HV is set to 10 V (blue), 20 V (red), 50 V (green) and 100 V (pink).

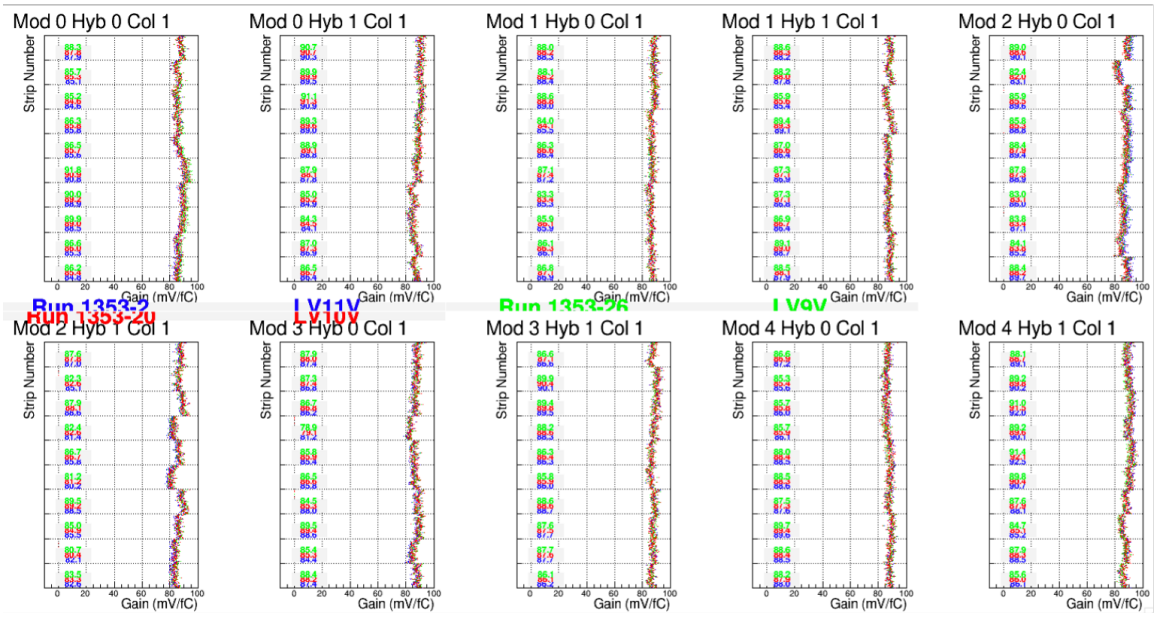


(b) The input noise distributions of Column 1 in the 10 hybrids on 5SS when the HV is set to 10 V (blue), 20 V (red), 50 V (green) and 100 V (pink).

Figure A.5: The input noise distributions in the 10 hybrids on 5SS when the HV is set to 10 V (blue), 20 V (red), 50 V (green) and 100 V (pink). The LV is set to 11 V for these tests.

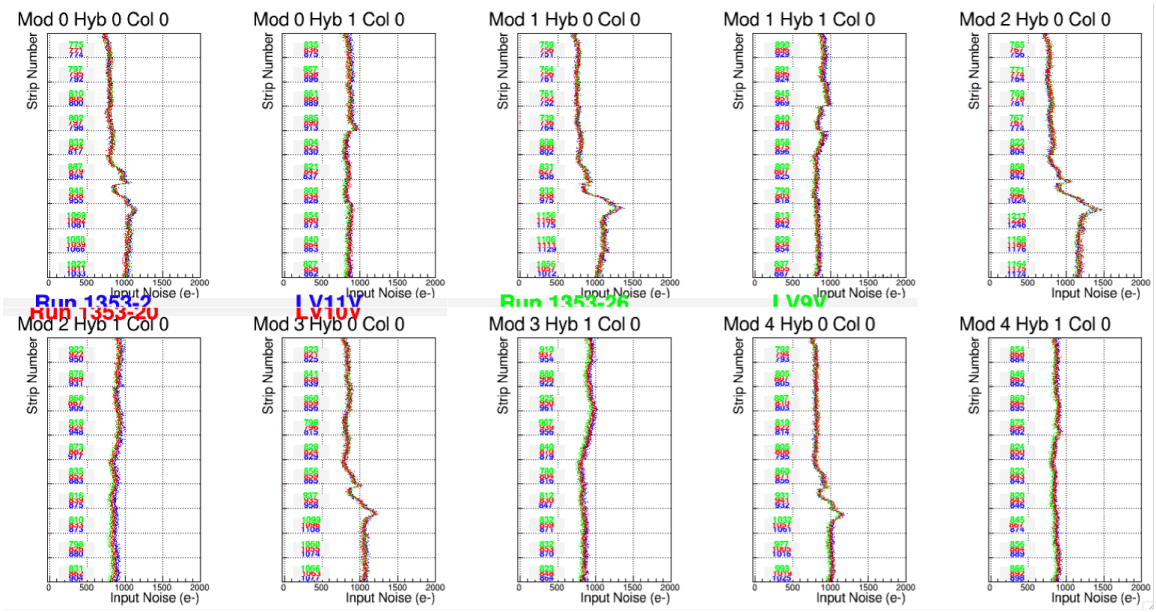


(a) The gain distributions of Column 0 in the 10 hybrids on 5SS when the LV is set to 11 V (blue), 10 V (red) and 9 V (green).

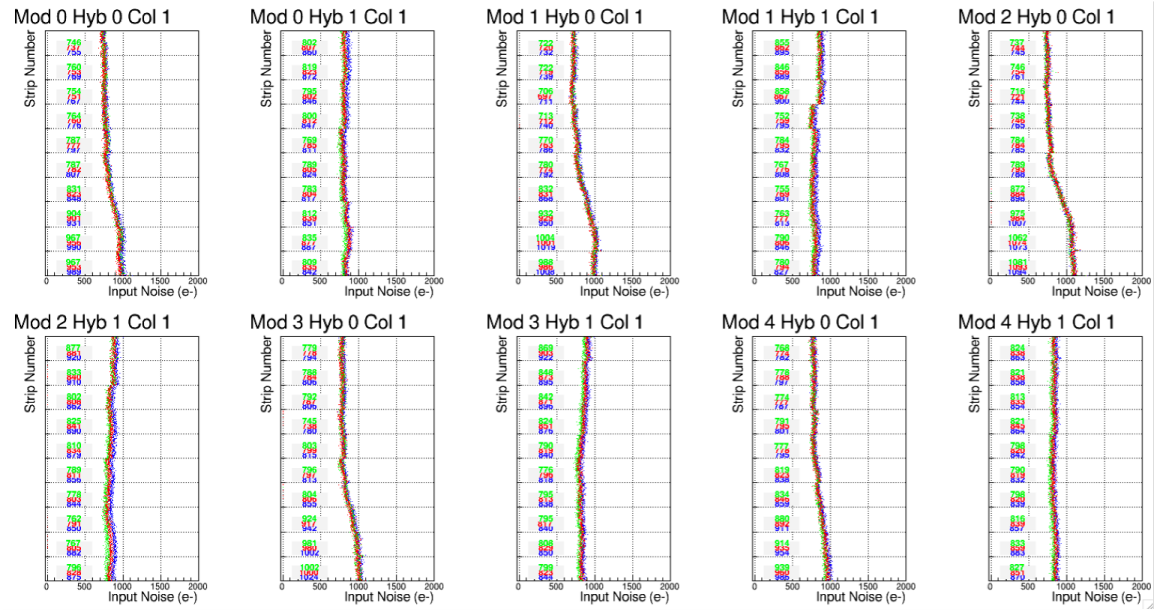


(b) The gain distributions of Column 1 in the 10 hybrids on 5SS when the LV is set to 11 V (blue), 10 V (red) and 9 V (green).

Figure A.6: The gain distributions in the 10 hybrids on 5SS when the LV is set to 11 V (blue), 10 V (red) and 9 V (green). The HV is set to be 10 V for these tests.



(a) The input noise distributions of Column 0 in the 10 hybrids on 5SS when the LV is set to 11 V (blue), 10 V (red) and 9 V (green).



(b) The input noise distributions of Column 1 in the 10 hybrids on 5SS when the LV is set to 11 V (blue), 10 V (red) and 9 V (green).

Figure A.7: The input noise distributions in the 10 hybrids on 5SS when the LV is set to 11 V (blue), 10 V (red) and 9 V (green). The HV is set to be 10 V for these tests.

Bibliography

[1] Tim Radford, Terry O'Connor, James Gillies, Vanessa Mexner, Camilla Jakobsson, and Arnaud Marsollier. Accelerating science and innovation: societal benefits of european research in particle physics. Technical report, 2013.

[2] Esma Anais Mobs. The cern accelerator complex. Technical report, 2016.

[3] Giorgio Apollinari, Lucio Rossi, and Oliver Brüning. High luminosity lhc project description. Technical report, 2014.

[4] ATLAS collaboration et al. Technical design report for the atlas inner tracker strip detector. Technical report, LHC/ATLAS Experiment, 2017.

[5] Peter William Phillips. *Design, development, characterisation and operation of ATLAS ITk strip staves*. PhD thesis, University of Oxford, 2020.

[6] Helmuth Spieler. *Semiconductor detector systems*, volume 12. Oxford university press, 2005.

[7] Mark Thomson. *Modern particle physics*. Cambridge University Press, 2013.

[8] Simon Ramo. Currents induced by electron motion. *Proceedings of the IRE*, 27(9):584–585, 1939.

[9] William Shockley. Currents to conductors induced by a moving point charge. *Journal of applied physics*, 9(10):635–636, 1938.

[10] Dennis V Perepelitsa. Johnson noise and shot noise. *Dept. of Physics, MIT*, 2006.

[11] Svante Arrhenius. Uber die dissociationswaarme und den einfluss der temperatur auf den dissociationsgrad der elektrolyte. *Zeitschrift fur physikalische Chemie*, 4(1):96–116, 1889.

[12] S Gonzalez-Sevilla, Y Unno, M Weber, A Clark, Y Ikegami, G Pelleriti, K Hara, D Ferrere, D La Marra, M Pohl, et al. Electrical results of double-sided silicon strip

modules for the atlas upgrade strip tracker. Technical report, ATL-COM-UPGRADE-2012-008, 2012.

[13] Weiguo Lu, F Anghinolfi, L Cheng, J De Witt, J Kaplon, P Keener, A Narayan, M Newcomer, and K Swientek. Development of the abcstar front-end chip for the atlas silicon strip upgrade. *Journal of Instrumentation*, 12(04):C04017, 2017.

[14] Zhijun Liang. Atlas strip detector upgrade for the hl-lhc. Technical report, ATL-COM-INDET-2015-058, 2015.

[15] Sven Wonsak, Atlas Collaboration, et al. The atlas itk strip detector system for the phase-ii lhc upgrade. Technical report, ATL-COM-ITK-2019-060, 2020.

[16] Federico Faccio, Antonio Cristiano, Georges Blanchot, Stefano Michelis, and Giacomo Ripamonti. Sissa: The bpol12v dcdc converter for hl-lhc trackers: towards production readiness. *PoS*, page 070, 2020.

[17] Helmuth Spieler. Introduction to radiation-resistant semiconductor devices and circuits. In *AIP Conference Proceedings*, volume 390, pages 23–49. American Institute of Physics, 1997.

[18] F Faccio. Radiation hardness issues in 130nm and 65nm cmos. In *ACES*, volume 16, 2016.

[19] Aristeidis Nikolaou, Matthias Bucher, Nikolaos Makris, Alexia Papadopoulou, Loukas Chevas, Giulio Borghello, Henri D Koch, and Federico Faccio. Modeling of high total ionizing dose (tid) effects for enclosed layout transistors in 65 nm bulk cmos. In *2018 International Semiconductor Conference (CAS)*, pages 133–136. IEEE, 2018.

[20] Y Unno, Y Abo, A Affolder, P Allport, I Bloch, A Blue, V Fadeyev, J Fernandez-Tejero, I Gregor, C Haber, et al. Atlas17ls–a large-format prototype silicon strip sensor for long-strip barrel section of atlas itk strip detector. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 989:164928, 2021.

[21] D Pitzl, N Cartiglia, B Hubbard, D Hutchinson, J Leslie, K O'Shaughnessy, W Rowe,

HF-W Sadrozinski, A Seiden, E Spencer, et al. Type inversion in silicon detectors. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 311(1-2):98–104, 1992.

[22] KJR Cormier, B Gallop, J Kaplon, Z Li, M Noy, PW Phillips, CA Sawyer, D Sperlich, and M Warren. Development of the front end amplifier circuit for the atlas itk silicon strip detector. *Journal of Instrumentation*, 16(07):P07061, 2021.

[23] Luise Poley, Craig Sawyer, Sagar Addepalli, AA Affolder, Bruno Allongue, Phil Allport, Eric Anderssen, Francis Anghinolfi, J-F Arguin, J-H Arling, et al. The abc130 barrel module prototyping programme for the atlas strip tracker. *Journal of instrumentation*, 15(09):P09004, 2020.

[24] Jens Ejury. Buck converter design. *Infineon Technologies North America (TFNA) Corn Desion Note*, 1:1, 2013.

[25] Jens Dopke, V Fadeyev, AA Grillo, B Lin, F Martinez-Mckinney, J Nielsen, P Phillips, C Sawyer, S Sullivan, J Volk, et al. Lessons learned in high frequency data transmission design: Atlas strips bus tape. *Journal of Instrumentation*, 12(01):C01019, 2017.

[26] Chaowaroj Wanotayaroj, Harald Ceslik, Helmut Colbow, Sergio Diez Cornell, Peter Goettlicher, Ingrid M Gregor, Anastasiya Melnik, Marcel Stanitzki, and Jonas Wolff. The end-of-substructure (eos) card for the striptracker upgrade of the atlas experiment. In *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC)*, pages 1–3. IEEE, 2018.

[27] Chaowaroj Wanotayaroj, Artur Boebela, Harald Ceslika, Helmut Colbowa, James Michael Keaveneyb, Mogens Damc, Sergio Dieza, Peter Goettlichera, Jan Oechslec, Marcel Stanitzkia, et al. First lpgbt-based prototype of the end-of-substructure (eos) card for the atlas strip tracker upgrade. In *Topical Workshop on Electronics for Particle Physics TWEPP2019*, volume 2, page 6, 2019.

[28] Jan Troska, Andrea Kraxner, Alexander Brandon-Bravo, Stephane Detraz, Carmelo Scarcella, Christophe Sigaud, Csaba Soos, Francois Vasey, and Lauri Olanterä. The vtrx+, an optical link module for data transmission at hl-lhc. *PoS*, page 048, 2017.

[29] Joash Nicholas Naidoo. Characterizing single event upsets within the lpgbt-based end-of-substructure card. Master's thesis, Faculty of Engineering and the Built Environment, 2021.

[30] J Troska, S Seif El Nasr-Storey, S Detraz, P Stejskal, C Sigaud, C Soos, and F Vasey. Single-event upset testing of the versatile transceiver. *Journal of Instrumentation*, 6(11):C11026, 2011.

[31] Mohsine Menouni, P Gui, and P Moreira. The gbtia, a 5 gbit/s radiation-hard optical receiver for the slhc upgrades. 2009.

[32] Z Zeng, T Zhang, G Wang, P Gui, S Kulis, and P Moreira. Ldq10: a compact ultra low-power radiation-hard 4$\times$ 10 gb/s driver array. *Journal of Instrumentation*, 12(02):P02020, 2017.

[33] Romina Diener, Jan Dreyling-Eschweiler, Heiko Ehrlichmann, Ingrid-Maria Gregor, Ulrich Kötz, Uwe Krämer, Norbert Meyners, Natalia Potylitsina-Kube, Anne Schütz, Paul Schütze, et al. The desy ii test beam facility. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 922:265–286, 2019.

[34] Igor Rubinskiy et al. An eudet/aida pixel beam telescope for detector development. *Physics Procedia*, 37:923–931, 2012.

[35] J Baudot, G Bertolone, A Brogna, G Claus, C Colledani, Y Degerli, R De Masi, A Dorokhov, G Doziere, W Dulinski, et al. First test results of mimosa-26, a fast cmos sensor with integrated zero suppression and digitized output. In *2009 IEEE Nuclear Science Symposium Conference Record (NSS/MIC)*, pages 1169–1173. IEEE, 2009.

[36] Hendrik Jansen, Simon Spannagel, Jorg Behr, Antonio Bulgheroni, Gilles Claus, Emlyn Corrin, David Cussans, Jan Dreyling-Eschweiler, Doris Eckstein, Thomas Eichhorn, et al. Performance of the eudet-type beam telescopes. *EPJ Techniques and Instrumentation*, 3:1–20, 2016.

[37] M Mager, ALICE collaboration, et al. Alpide, the monolithic active pixel sensor for

the alice its upgrade. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 824:434–438, 2016.

[38] A Miucci, L Gonella, T Hemperek, F Hugging, H Kruger, T Obermann, N Wermes, M Garcia-Sciveres, M Backhaus, M Capeans, et al. Radiation-hard active pixel sensors for hl-lhc detector upgrades based on hv-cmos technology. *Journal of Instrumentation*, 9(05):C05064, 2014.

[39] Sept. 2019 test beam test log book. private communication.

[40] Yi Liu, MS Amjad, P Baesso, David Cussans, J Dreyling-Eschweiler, R Ete, I Gregor, L Huth, A Irles, H Jansen, et al. Eudaq2—a flexible data acquisition software framework for common test beams. *Journal of Instrumentation*, 14(10):P10033, 2019.

[41] Tobias Bisanz, Hendrik Jansen, J-H Arling, Antonio Bulgheroni, Jan Dreyling-Eschweiler, Thomas Eichhorn, Ingrid-Maria Gregor, Phlillip Hamnett, Claus Kleinwort, Alexander Morton, et al. Eutelescope: A modular reconstruction framework for beam telescope data. *Journal of Instrumentation*, 15(09):P09020, 2020.

[42] Frank Gaede, Ties Behnke, Norman Graf, and Tony Johnson. Lcio-a persistency framework for linear collider simulation studies. *arXiv preprint physics/0306114*, 2003.

[43] CC Enz and EA Vittoz. Charge-based mos transistor modeling: the ekv model for low-power and rf ic design. 2006. *URL http://infoscience. epfl. ch/record/149582*.

[44] Private communication with jan kaplon. private communication.

[45] Edoardo Rossi. *Characterization of Silicon Modules and Sensors for the ATLAS Inner Tracker Strip Detector*. PhD thesis, Staats-und Universitatsbibliothek Hamburg Carl von Ossietzky, 2020.

[46] Simon Spannagel, Koen Wolters, Daniel Hynds, N Alipour Tehrani, Mathieu Benoit, Dominik Dannheim, Neal Gauvin, Andreas Nürnberg, Paul Schütze, and Mateus Vicente. Allpix2: A modular simulation framework for silicon detectors. *Nuclear*

Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 901:164–172, 2018.

[47] Sea Agostinelli, John Allison, K al Amako, John Apostolakis, H Araujo, Pedro Arce, Makoto Asai, D Axen, Swagato Banerjee, GJNI Barrand, et al. Geant4—a simulation toolkit. *Nuclear instruments and methods in physics research section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 506(3):250–303, 2003.

[48] Private communication with radek privara. private communication.

[49] Private communication with emma buchanan. private communication.

[50] Private communication with mphil student who deserves a name here. private communication.

[51] Andrei Vladimirescu. *The SPICE book*. Wiley New York, 1994.

[52] Jerry Janesch. Two-wire vs. four-wire resistance measurements: Which configuration makes sense for your application. *no. May*, pages 2–4, 2013.

[53] Joseph Howse. *OpenCV computer vision with python*. Packt Publishing Birmingham, 2013.

[54] John Brown. V-stars/sa cceptance t est r esults. In *Seattle: Boeing Large Scale Optical Metrology Seminar*, 1998.

[55] David Hoffa, Chad Laux, and Paul Kidwell. A comparison of ogp® smartscope® sensors. *Journal of Industrial Technology*, 26(1), 2010.

[56] ATLAS Collabration. Barrel stave drawings, 2020.

[57] Private communications with samuel henry. private communication.

[58] Rainer Michalzik. Vcsel fundamentals. In *VCSELs*, pages 19–75. Springer, 2013.

[59] Rainer Michalzik and Karl Joachim Ebeling. Operating principles of vcsels. In *Vertical-Cavity Surface-Emitting Laser Devices*, pages 53–98. Springer, 2003.

[60] Kent D Choquette, KM Geib, Robert Hull, HQ Hou, KL Lear, HC Chui, BE Hammons,

and JA Nevers. Wet oxidation of algaas vs. alas: A little gallium is good. In *Conference Proceedings LEOS'96 9th Annual Meeting IEEE Lasers and Electro-Optics Society*, volume 1, pages 390–391. IEEE, 1996.

[61] HQ Jia, H Chen, WC Wang, WX Wang, W Li, Q Huang, Junming Zhou, and QK Xue. Improved thermal stability of wet-oxidized alas. *Applied physics letters*, 80(6):974–976, 2002.

[62] Christopher J Helms, Ian Aeby, Wenlin Luo, Robert W Herrick, and Albert Yuen. Reliability of oxide vcsels at emcore. In *Vertical-Cavity Surface-Emitting Lasers VIII*, volume 5364, pages 183–189. SPIE, 2004.

[63] Robert W Herrick, Alexandru Dafinca, Philippe Farthouat, Alexander A Grillo, Stephen J McMahon, and Anthony R Weidberg. Corrosion-based failure of oxide-aperture vcsels. *IEEE Journal of Quantum Electronics*, 49(12):1045–1052, 2013.

[64] Robert A Hawthorne, James K Guenter, David N Granville, MK Hibbs-Brenner, and RA Morgan. Reliability study of 850 nm vcsels for data communications. In *Proceedings of International Reliability Physics Symposium*, pages 203–210. IEEE, 1996.

[65] Alexandru Dafinca, Anthony R Weidberg, Steven J McMahon, Alexander A Grillo, Philippe Farthouat, Michael Ziolkowski, and Robert W Herrick. Reliability and degradation of oxide vcsels due to reaction to atmospheric water vapor. In *Vertical-Cavity Surface-Emitting Lasers XVII*, volume 8639, pages 152–161. SPIE, 2013.

[66] D Stewart Peck. Comprehensive model for humidity testing correlation. In *24th International Reliability Physics Symposium*, pages 44–50. IEEE, 1986.

[67] AR Weidberg. Vcsel reliability in atlas and development of robust arrays. *Journal of Instrumentation*, 7(01):C01098, 2012.

[68] Gary Breed. Analyzing signals using the eye diagram. *High Frequency Electronics*, 4(11):50–53, 2005.

[69] Francesca Capocasa. Electrical characterisation of stave prototypes for the atlas itk strip detector upgrade. Technical report, ATL-COM-ITK-2021-039, 2021.

[70] Private communication with peter phillips. private communication.

[71] AJ Blue, B Gallop, T Heim, C Helling, K Krizka, B Li, C Labitan, E Mladina, L Poley, PW Phillips, et al. Magnetic triggering—time-resolved characterisation of silicon strip modules in the presence of switching dc-dc converters. *Journal of Instrumentation*, 16(06):P06012, 2021.

[72] Ming-ta Hsieh and Gerald E Sobelman. Architectures for multi-gigabit wire-linked clock and data recovery. *IEEE Circuits and systems magazine*, 8(4):45–57, 2008.

[73] Albert X. Widmer and Peter A. Franaszek. A dc-balanced, partitioned-block, 8b/10b transmission code. *IBM Journal of research and development*, 27(5):440–451, 1983.