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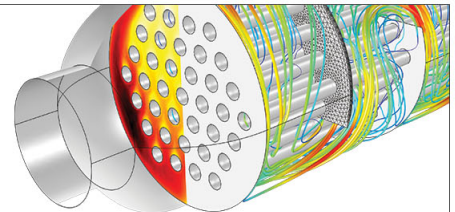
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Improving the performance of organic thin film transistors formed on a vacuum flash-evaporated acrylate insulator

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A systematic investigation has been undertaken, in which thin polymer buffer layers with different ester content have been spin-coated onto a flash-evaporated, cross-linked diacrylate gate-insulator to form bottom-gate, top-contact organic thin-film transistors. The highest device mobilities, $\sim 0.65 \text{ cm}^2/\text{Vs}$ and $\sim 1.00 \text{ cm}^2/\text{Vs}$ for pentacene and dinaphtho[2,3-b:2',3'-f]-thieno[3,2-b]thiophene (DNTT), respectively, were only observed for a combination of large-grain ($\sim 1\text{--}2 \mu\text{m}$) semiconductor morphology coupled with a non-polar dielectric surface. No correlation was found between semiconductor grain size and dielectric surface chemistry. The threshold voltage of pentacene devices shifted from -10 V to -25 V with decreasing surface ester content, but remained close to 0 V for DNTT. © 2013 AIP Publishing LLC.

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Polymer dielectric layers are desirable for flexible organic thin-film transistors (OTFTs) due to their favorable processability and inherent flexibility. Amorphous linear polymers, e.g., polystyrene (PS), may be used as a non-polar dielectric layer. However, such materials, deposited as polymers, either from solution or by thermal evaporation, may have high gate leakage due to, for example, pinhole defects. In order to make reliable transistors, it is necessary to constrain the dielectric polymer chains by cross-linking.¹ This involves using polymers with reactive sites such as acid anhydride,¹ cinnamate,^{2,3} silane,⁴ epoxy and acrylate⁵ groups that can cross-link during deposition or with a cross-linking agent *in-situ*. These chemical groups react under certain conditions, e.g., heat or radiation, to form covalent bonds between the polymer chains to yield a dielectric layer with better mechanical and electrical reliability. Radiation curing lends itself well to large area processing. For example, E-beam or plasma *in-situ* polymerization of a vacuum flash evaporated acrylate layer, which requires sub-second curing, yields tens of meters of polymer film per minute in a roll-to-roll process.^{6–8}

Use of these cross-linkable materials, however, inevitably leaves weakly polar chemical groups, such as ester groups, on the surface. Surface polar groups are believed to affect the growth of subsequently deposited organic semiconductors⁹ and are undesirable for achieving high carrier mobility in OTFTs.¹⁰ Accordingly, there is a tradeoff between the desirability of a non-polar surface and the processability as well as reliability of the bulk of the dielectric layer, which requires polar groups to form the cross-linking network.

In our development of an all-vacuum route for the roll-to-roll production of OTFTs, we have demonstrated that cross-linked, flash-evaporated tri(propylene glycol) diacrylate

(TPGDA) is an effective dielectric layer, giving rise to OTFTs with low gate leakage leading to on/off current ratios in excess of 10^5 , but owing to undesirable surface condition, yields relatively low mobility devices with unstable threshold voltage, V_T , in ambient air.⁷ In the following, therefore, we present the results of a systematic investigation (a) to understand the role of surface chemistry of the acrylic polymer on transistor performance and (b) to identify a suitable buffer material for cross-linked TPGDA that will enhance its surface properties, while maintaining its excellent bulk properties. In particular, we investigate the effect of surface ester group concentration on OTFT performance by examining a range of thin, spin-coated, surface buffer layers of polymers with different ratios of ester group to carbon atoms in their molecular structure.

OTFTs were made in a bottom-gate top-contact configuration (Fig. 1(a)) on a glass substrate. The cross-linked TPGDA dielectric layer, $\sim 450 \text{ nm}$ thick (as measured by Dektak thickness profiler), was deposited by flash evaporation onto glass slides with pre-patterned gold gate contacts and condensed as a liquid monomer before being cured by plasma.^{6,7,11} The TPGDA surface was then modified by the addition of $15\text{--}40 \text{ nm}$ thick (as measured by a Micro-XAM phase shift optical profiler) polymer buffer layers with different ester content (Fig. 1(b)). The following polymers: poly(1-vinylnaphthalene) (PVN), PS, poly(vinyl stearate) (PVS), poly(butyl methacrylate) (PBMA), and poly(methyl methacrylate) (PMMA) were spin-coated from toluene solutions at a concentration of 0.6 wt. \% . The treated dielectric layers were annealed at 70°C for 10 min to remove solvent from the spin-coated layer. Bare TPGDA reference layers were also annealed along with the buffer-treated dielectric layers. Thus, different dielectric surfaces with ester/carbon ratio ranging from 0 to $1:5$ were prepared. The polar (γ^{polar}) and dispersive ($\gamma^{\text{dispersive}}$) components of the surface energy of the buffer layers were calculated based on contact angle measurements using water and diiodomethane following

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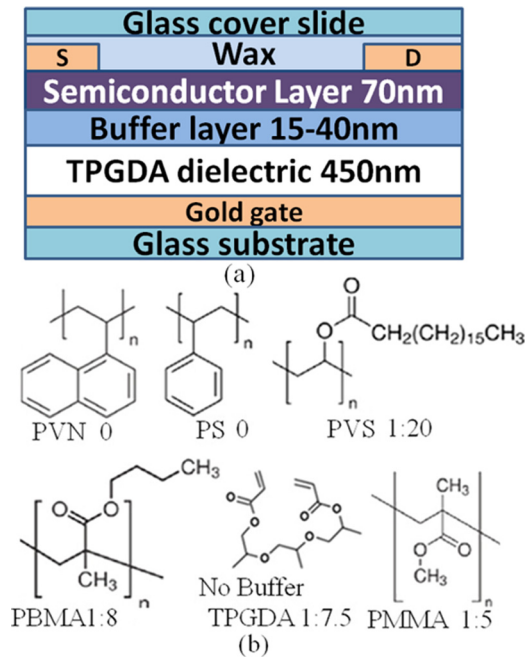


FIG. 1. (a) Schematic representation of the cross-section through our bottom-gate top-contact OTFTs indicating the approximate thickness of key layers; (b) molecular structure of the TPGDA monomer and each of the buffer layer materials, arranged in order of increasing ester group concentration in the chain relative to carbon content (given below each molecule).

Fowkes's method.¹² A pentacene or dinaphtho[2,3-b:2',3'-f]-thieno[3,2-b]thiophene (DNTT) film ~ 70 nm thick was thermally evaporated simultaneously at a rate of 0.2 \AA/s onto these dielectric surfaces with the substrates being held at room temperature. The crystals of the resulting semiconductor film were characterized by XRD. Gold source/drain contacts ($L = 200 \text{ }\mu\text{m}$, $W = 2400$ or $5000 \text{ }\mu\text{m}$) were thermally evaporated onto the semiconductor layer through a shadow mask. The TPGDA monomer, buffer polymers, and pentacene were all purchased from Sigma-Aldrich. The DNTT was synthesized based on the method of Takimiya.¹³ After fabrication, the pentacene devices were encapsulated using microscope cover slides sealed with paraffin wax. This encapsulation was effective in preventing the transistors from degrading during repeated measurements in air.⁷ The DNTT device proved to be stable and was not encapsulated. The surface topographies of the dielectric and semiconductor layers were characterized by AFM. The transistor

performance was characterized using two source measurement units (Keithley, model 2400) in air in the dark.

With no buffer layer, the root mean square, RMS, surface roughness of flash evaporated TPGDA films was about 0.4 nm over a $3 \text{ }\mu\text{m} \times 3 \text{ }\mu\text{m}$ sample area. This is close to that of thermally grown SiO_2 on Si, often used as a gate dielectric. Table I shows that with the spin-coated buffer layers the surface roughness was reduced slightly to $\sim 0.3 \text{ nm}$. The polar and dispersive components of the surface energy of each surface are given in the same table. As expected, the polymers without ester groups, i.e., PS, PVN, had highly non-polar surfaces. The low ester content PVS and PBMA also showed low polarity ($\gamma^{\text{polar}} \leq 1.2 \text{ mN/m}$), while bare TPGDA and PMMA surfaces had much higher values: 8.5 mN/m and 6.4 mN/m , respectively. The polar component of the surface energy of TPGDA is greater than in PMMA, probably as a result of exposure to the plasma during curing.¹⁴ The dispersive part of the surface energy and the total surface energy were generally not correlated with the ester group concentration, as evidenced by the data in Table I.

There have been plenty of reports on the relation between dielectric surface energy and pentacene morphology.^{14–18} Large pentacene grains have been reported on dielectric surfaces with the total surface energy ranging widely from 25 to 55 mN/m .^{14,17} In our experiment, the aliphatic ester-containing PMMA surface, with γ^{total} of 37 mN/m and γ^{polar} of 6.4 mN/m resulted in large pentacene grains (Fig. 2) and the highest XRD signal intensity (Table I). Large pentacene grains with diameter reaching $1 \text{ }\mu\text{m}$ were also observed on the non-polar ester free PS ($\gamma^{\text{total}} = 47.5$, $\gamma^{\text{polar}} = 0.0 \text{ mN/m}$) and the ultra-low surface energy non-polar: PVS ($\gamma^{\text{total}} = 23.1$, $\gamma^{\text{polar}} = 0.0 \text{ mN/m}$) buffer layers. The naphthalene-containing PVN, which might be expected to give large pentacene grains due to molecular similarity of the naphthalene units to the semiconductor, resulted in a grain size much smaller than that of PS, despite their comparable surface energy. The XRD signal peak intensity (Table I), which provides a rough measure of crystalline order in the pentacene films, is generally correlated with the pentacene grain size observed by AFM (Fig. 2).

We conclude, therefore, that pentacene crystalline morphology does not correlate with the presence/absence of either ester or aromatic groups on the dielectric surface. Furthermore, it does not correlate with the surface energy of the underlying substrate, as both weakly and strongly polar/dispersive surface energy gave large crystals in some cases.

TABLE I. Surface ester/carbon ratio, roughness, surface energy, and XRD peak intensity/position of pentacene on different buffer surfaces; also provided are hole mobility (μ) of transistors with different buffer layers.

Surface and ester/carbon ratio		RMS (nm) $3 \times 3 \text{ }\mu\text{m}$	Surface energy			XRD of pentacene		
			γ^{total} (mN/m)	$\gamma^{\text{dispersive}}$ (mN/m)	γ^{polar} (mN/m)	Intensity (counts per second)	Position 2θ (deg)	μ ($\text{cm}^2/\text{V s}$)
Bare TPGDA	1:7.5	0.44	43.1	34.7	8.5	5588	5.76	0.02 ± 0.01
PVN	0	0.23	43.1	42.0	1.1	3644 ^a	5.76 ^a	0.03 ± 0.01
PS	0	0.33	47.5	47.5	0.0	26 656	5.80	0.22 ± 0.09
PVS	1:20	0.33	23.1	23.1	0.0	73 154	5.76	0.20 ± 0.12
PBMA	1:8	0.20	42.1	40.9	1.2	4711	5.76	0.05 ± 0.01
PMMA	1:5	0.25	43.4	37.0	6.4	93 707	5.76	0.04 ± 0.01

^aPentacene on PVN was deposited in a separate batch for XRD but with deposition and measurement parameters being held the same.

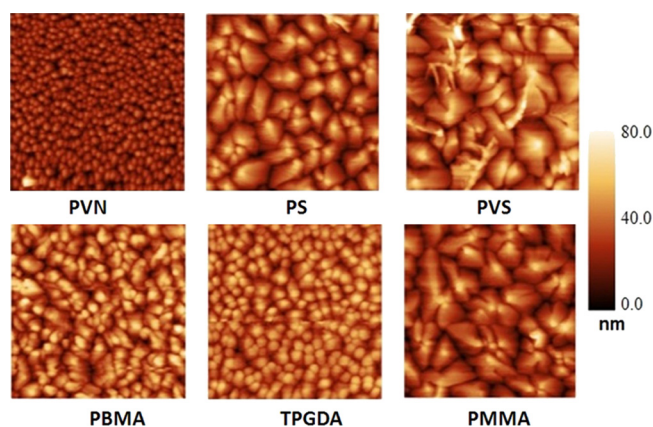


FIG. 2. AFM topography images ($3 \times 3 \mu\text{m}$) of pentacene grown on different dielectric surfaces.

The pentacene growth might be affected by other factors associated with the dielectric surface. Of course, the transistor performance is likely to be dominated by the pentacene order very close to the dielectric surface, which may be very different from the bulk and free-surface morphology, as suggested by the “layer + island” crystal growth mode for the first few layers of pentacene.^{16,17,19}

In Table I and Fig. 3(a), we present the charge carrier mobility of OTFTs with different dielectric surface buffers and bare TPGDA. The mobility is calculated from the saturation region of the transfer curves using the conventional square-law equation.^{7,20} The presented values are averages obtained from at least four, and up to 24, individual transistors. All pentacene layers were deposited simultaneously in the same run, thus excluding effects that may arise from batch-to-batch inconsistencies in the pentacene evaporation process (the pentacene film on PVN were deposited in a separate run for XRD with deposition parameters kept the same). Among the surfaces that gave large crystals, i.e., PS, PVS, PMMA, the highest mobilities were observed on the PS and the PVS surfaces, which have zero and one ester per 20 carbon atom, respectively, and displayed a near-zero polar surface energy. The PMMA surface, despite showing a large pentacene grain size, high XRD signal intensity, and similar signal peak position as that of PS and PVS, led to a mobility no better than that of PVN and PBMA on which the grain size was much smaller. The PBMA, bare TPGDA, and PVN with smaller grain size showed the expected much lower mobility. The low mobility associated with the high ester content PMMA buffer, despite the favorable morphology is in good agreement with the review by Veres *et al.*²¹ They summarized that a polar/high k dielectric surface restricts OTFTs mobility due to its polarity and, conversely, a non-polar surface gives high mobility. Two different models, i.e., a density of states (DOS)²² broadening model based on hopping transport of charge carriers and a Fröhlich polaronic coupling model,²³ have been built to explain the observation. However, the detailed mechanism is still not confirmed.

In a further experiment, we optimized the semiconductor deposition parameters and process and obtained large pentacene crystals of $2 \mu\text{m}$ on PS, PMMA (Fig. 4(c) insets), as well as on PVS. The mobility observed was $0.65 \text{ cm}^2/\text{V s}$

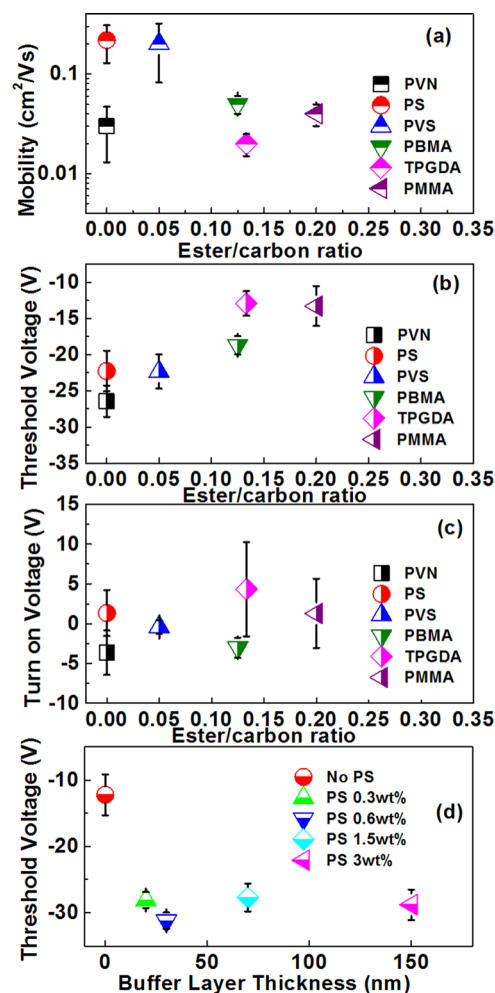


FIG. 3. (a) Hole mobility versus ester/carbon ratio of the buffer polymer. (b) The threshold voltage of transistors versus ester/carbon ratio of the buffer polymer. (c) Turn-on voltage of transistors versus ester/carbon ratio of the buffer polymer. (d) Threshold voltage of transistors with PS buffer layers of different thicknesses prepared from solutions with the concentrations indicated: 20 nm (0.3 wt. %), 30 nm (0.6 wt. %), 70 nm (1.5 wt. %), and 150 nm (3 wt. %).

on PS, $0.60 \text{ cm}^2/\text{V s}$ on PVS, and $0.15 \text{ cm}^2/\text{V s}$, $0.05 \text{ cm}^2/\text{V s}$ on bare TPGDA and PMMA surface, respectively (Figure 4(a)), again showing a strong correlation between insulator surface polarity and subsequent semiconductor mobility.

Owing to its better environmental stability,²⁴ we extended the buffer layer treatment to DNTT transistors²⁵ with all the parameters unchanged. The DNTT, similarly to the pentacene, showed quite large grains on the PS and bigger ones on PMMA (Fig. 4(d) inset) as well as PVS covered TPGDA. The PS and PVS surfaces show much higher mobility than that of the uncoated and PMMA covered surfaces, achieving an average value of $\sim 1.00 \text{ cm}^2/\text{V s}$ on PS and PVS with on/off ratio of about 10^6 – 10^7 .

We conclude that by restricting the concentration of polar ester groups to below about one ester group per 20 carbon in an amorphous polymer buffer layer on our TPGDA dielectric surface, the charge carrier mobility increased significantly for pentacene and DNTT films with large grain morphology.

While improving carrier mobility, the reduction in surface ester concentration caused a systematic change of

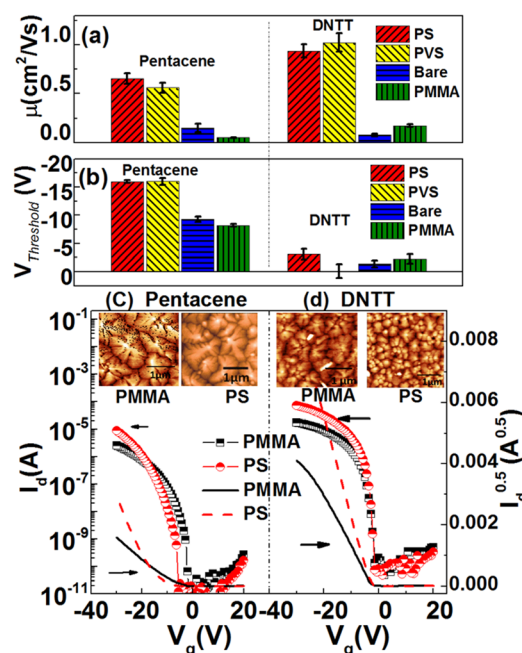


FIG. 4. (a) Hole mobility and (b) threshold voltage of transistors with pentacene and DNTT on different buffer surfaces; typical transfer curves of (c) pentacene and (d) DNTT transistors formed on PMMA-buffered and PS-buffered TPGDA. The insets are the typical AFM images of pentacene and DNTT on the PMMA/PS-buffered surface.

~15 V to more negative values in the threshold voltage, V_T , of the pentacene devices (Fig. 3(b)). A similar trend was observed in the group of devices with optimized pentacene deposition (Fig. 4(b)) although the extent of the shift was smaller. This is in contrast to the turn-on voltage, V_{to} , which was scattered around 0 V (Fig. 3(c)), suggesting a sensitivity to interface defects and/or contaminants.²⁶

Threshold voltage is a key transistor parameter so that shifts in its value due to dielectric surface modification have been studied intensively. In the case of self-assembled monolayers (SAMs), the dipole field across the SAM thickness is thought to be the cause of such shifts.²⁷ In our case, since the polymer buffers are amorphous, the average dipole moment across the film is likely to be zero and so cannot be the origin of the shift in V_T observed here. This is further confirmed by the lack of dependence of V_T on the buffer layer thickness (Fig. 3(d)).²⁸

According to Kobayashi,²⁹ the difference in electron affinity between dielectric and semiconductor can also induce a dipole across the insulator/semiconductor interface leading to differences in V_T from one dielectric material to the other. However, V_{to} should also follow the same trend—clearly this is not the case here for pentacene (Fig. 3(c)).

Further evidence that neither of these explanations apply is seen in the comparison between DNTT and pentacene. First, the different dielectric surfaces cause only a 2–3 V difference in the V_T of DNTT (Fig. 4(b)). Second, the V_{to} is close to zero in all cases (Fig. 4(d)), so the difference between threshold voltage and turn on voltage, $V_T - V_{to}$, for the DNTT is almost negligible, while that of pentacene devices is obvious. This suggests that interfacial and bulk trap states are much fewer in DNTT compared with pentacene. This is confirmed in simulations undertaken with Silvaco's UOTFT (Universal Organic Thin Film Transistor) model,

which suggest an almost ideal behavior for DNTT transistors utilizing PS buffering.²⁵ mobility was found to be insensitive to the applied gate voltage, V_G , resulting in the ideal square-law dependence on V_G of the device current, I_D , in saturation (Fig. 4(d)). In contrast, pentacene devices formed on the PS-buffered TPGDA display a high mobility only at high V_G —the strong dependence of mobility on V_G leading to the non-linear plot of $I_D^{0.5}$ vs. V_G in Fig. 4(c), a feature consistent with the presence of trap states in the semiconductor. The presence of trap states is highly likely to be the reason for the different transistors performance of Pentacene and DNTT³⁰ and perhaps is also responsible for the threshold voltage shift that we observed on the different combination of buffer layers with pentacene.

In conclusion, we have shown that vacuum flash-evaporated and cross-linked TPGDA is a viable approach to producing stable, high mobility transistors from both pentacene and DNTT, so long as the insulator surface is buffered with a layer with surface ester group content less than one per 20 carbon atoms. For pentacene devices, however, the higher mobility was accompanied by a detrimental shift of threshold voltage to more negative values. For DNTT devices, by contrast, buffering TPGDA with PS and PVS yielded a higher mobility accompanied by relatively low threshold voltage. Consequently, our on-going development of a vacuum-based roll-to-roll process is concentrating on DNTT devices and on alternative, vacuum-compatible methods of reducing the surface ester concentration of TPGDA.

Finally, although our primary goal was to establish the role of ester groups on transistor performance, the systematic modification of surface ester group concentration has shown that the overall dielectric surface energy is not the primary factor in determining grain size in subsequently evaporated films of pentacene and DNTT. Furthermore, we have shown that larger grain size does not necessarily lead to high mobility—it must be coupled with a low value for the polar component of the surface energy. These observations may go some way towards reconciling conflicting reports in the literature on such effects.

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