Functional Nanolayer Dielectrics for Improved Semiconductor Devices

by

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Abstract

Negatively charged dielectric films have significant potential to improve the performance of semiconductor devices by modifying its carrier densities. Such charges can be embedded by injecting electrons to dielectric defects, which can be intentionally engineered to control their density and location for specific applications. Understanding the interactions at the charged dielectrics and semiconductor interfaces is also essential for effective integration into devices.

The first part of this thesis focuses on the development of negatively charged dielectrics. The charging mechanism of defects at the SiO_x/AlO_x interface was investigated, highlighting the necessity of an electron source within a critical distance for defect-assisted charge injection. Based on this insight, negatively charged dielectrics were designed for field-effect doping of 2D semiconductors. Negative corona charge was identified as a suitable electron source, offering greater flexibility in charge location. Additionally, corona charging at elevated temperatures was found to generate deep acceptor states, enabling high charge stability at 450 °C. Strategies to fabricate negatively charged dielectrics with a charge density of ~10^{12} q cm^{-2} were developed.

The second part of this thesis explores the application of negatively charged dielectrics for passivating p-type silicon surfaces. The widespread adoption of silicon solar cells relies on both high energy conversion efficiency and cost-effective manufacturing. A $SiO_x/AlO_x/SiN_x$ passivation stack was designed using a chemically grown SiO_x layer at low temperature and an ultra-thin (~2.5 nm) AlO_x layer while maintaining a low S_{eff} of 6.3 cm/s. Detailed interface analysis revealed characteristic features of AlO_x-passivated Si interfaces and the critical role of valence band tail states in evaluating the overall passivation. Advanced atomic-scale characterisation using TEM and EELS correlated changes in electrical properties with elemental distribution and bonding configuration. Additionally, the effects of electric field in passivation were investigated, presenting a new strategy for further optimisation of device performance, yielding a further improved S_{eff} of 5.5 cm/s on p-type Si. A comprehensive model was proposed to account for the observed changes in interface properties, revealing an inherent correlation between chemical and field-effect passivation.

Finally, this thesis presents the application of negatively charged dielectrics for p-type doping of 2D MoS_2 – an ongoing challenge in incorporating 2D semiconductors in the next generation nanoelectronics. An all-dry fabrication process for 2D MoS_2-based field-effect transistors was developed, along with a controlled measurement environment to ensure reproducible electrical characterisation while fully preserving the dielectric charges. Correlating multiple characterisation techniques, this work provides converging evidence for p-type field-effect doping of 2D MoS_2, achieving a doping concentration of ~10^{12} q cm^{-2} without degrading channel mobility. A comprehensive model of the dielectric-MoS_2 interface was proposed, providing a foundation for further development of this doping strategy.

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List of Acronyms

ALD	Atomic layer deposition
2D TMDs	Two-dimensional transition metal dichalcogenides
AlO_x	Aluminium oxide, refers to the non-stoichiometric form of this dielectric film
CBM	Conduction band minimum
CPD	Contact potential difference
C-V	Capacitance-voltage
Cz	Czochralski
FEP	Field-effect passivation
FETs	Field-effect transistors
FZ	Float Zone
HfO_x	Hafnium oxide, refers to the non-stoichiometric form of this dielectric film
KP	Kelvin probe
MIS	Metal-insulator-semiconductor
MSE	Mean squared error
NAOS	Nitric acid oxidised Si
PECVD	Plasma-enhanced chemical vapor deposition
PERC	Passivated emitter and rear cells
PL	Photoluminescence
PV	Photovoltaic
SiN_x	Silicon nitride, refers to the non-stoichiometric form of this dielectric film
SiO_x	Silicon oxide, refers to the non-stoichiometric form of this dielectric film
SPV	Surface photovoltage
SRH	Shockley-Read-Hall
TOPCon	Tunnel oxide passivating contact
VBM	Valence band maximum

List of Symbols

V_{surf}	Applied surface bias (V)
τ_{bulk}	Bulk lifetime (s)
σ_q	Charge fluctuation (q cm^{-2})
ε_{diel}	Dielectric relative permittivity
I_{ds}	Drian-source current (A)
V_{ds}	Drian-source voltage (V)
Q_{eff}	Effective charge density (q cm^{-2})
S_{eff}	Effective surface recombination velocity (cm/s)
n_{el}	Electron density (cm^{-2})
$\sigma_{n/p}$	Electron or hole capture cross section (cm^2)
$S_{n/p}$	Electron or hole capture velocity (cm/s)
Δn	Excess carrier density (cm^{-3})
μ_{FE}	Field-effect mobility (cm^2 V^{-1} s^{-1})
V_{FB}	Flat-band voltage (V)
V_{gs}	Gate-source voltage (V)
V_{hys}	Hysteresis in transfer measurements (V)
Q_{it}	Interface charge density (q cm^{-2})
D_{it}	Interface state density (cm^{-2} eV^{-1})
E_t	Interface trap energy level (eV)
n_s	Surface electron concentration (q cm^{-2})
p_s	Surface hole concentration (q cm^{-2})
$\tau_{surface}$	Surface lifetime (s)
J_{0s}	Surface saturation current density (fA cm^{-2})
$U_{surface}$	Surface SRH recombination rate (s^{-1})
V_{th}	Threshold volage (V)

Preface

This thesis presents the research I conducted as a postgraduate student in the Department of Materials, University of Oxford, from January 2021 to April 2025. No part of this thesis has been submitted for a degree at Oxford or any other institution. Contributions from other authors are fully acknowledged within the text, with appropriate references provided. The main text contains 46,971 words (excluding references, appendixes, and front matter).

Throughout the course of this work, I have authored or contributed to the following publications:

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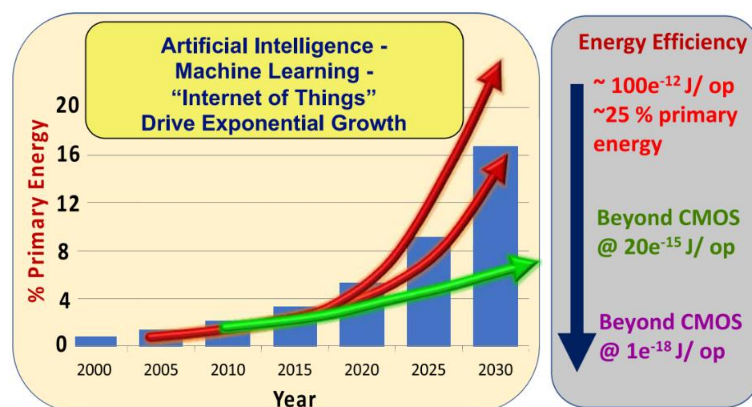
Chapter 1
Introduction

1.1 Semiconductor Devices and Energy Consumption

Semiconductors are materials with an electronic structure such that conduction electrons need to be activated through an energy bandgap. This moderate bandgap enables control of their electrical conductivity. For example, light can generate free carriers in semiconductors through the photovoltaic effect, converting photon energy into electric current. Applying external voltages can also introduce excess carriers in semiconductors, enabling the operation of devices such as transistors, which form the foundation of modern information technologies. Stemming from their versatile properties, semiconductor devices have driven a digital transformation of the world since the mid-20th century.

However, technology advancements have been accompanied by a sharp increase in energy demand. Energy consumption from large-scale computing and communication centres is growing rapidly with the emergence of Internet of Things (IoT), machine learning and artificial intelligence (AI). It has been predicted that the energy consumption for all microelectronics will grow to ~25% of primary energy by 2030, as shown in Figure 1.1.1 [1]. This growing energy demand has led to an increased reliance on fossil fuels, which exacerbates the depletion of non-renewable resources, the emission of greenhouse gases, and the associated environmental pollution. Addressing these challenges requires a shift towards a diverse combination of renewable energy and the development of energy-efficient technologies.



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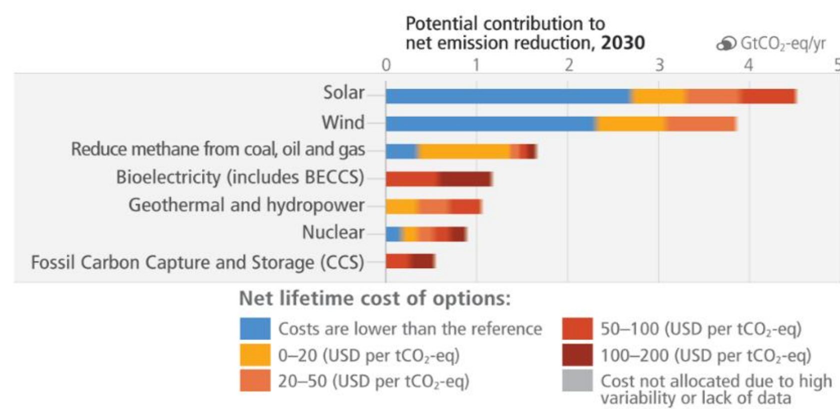
To minimise the environmental impact of the expanding digital landscape, renewable energy sources are being explored as alternatives. Among all the renewable energies, solar energy has been predicted to make the largest contribution in reducing global emissions, with the lowest cost, as shown in Figure 1.1.2 [3]. Silicon (Si) solar cells, in particular, are taking the lead in photovoltaics (PV) technology, with more than 97% of the total production in 2023 [4]. Additionally, efforts to lower the energy consumption in electronic devices, such as metal-oxide-semiconductor field-effect transistors (MOSFETs) – a fundamental building block of computing – have driven extensive research into novel materials, including 2D semiconductors or semiconducting carbon nanotubes (CNTs). These low-dimensional materials, either as a replacement or enhancement to silicon technology, enable more effective control over the transistor channel conductance and enable lower off-state current [2], [5], [6].



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Both solar cells and computing electronics rely on semiconductors as the active material to perform their core functions. However, supporting materials—such as dielectrics and metal contacts – play an equally crucial role in ensuring device operation. The efficiency and reliability of semiconductor devices require the optimisation of all components.

1.2 Functional Dielectrics

Dielectrics are materials with large bandgaps, making them poor conductors of electricity. In semiconductor devices, they serve multiple roles, including surface passivation, charge storage, optical coating, thermal management, and electric field control, in addition to functioning as insulating layers. Dielectrics that fulfil more than just preventing unwanted electrical conduction are referred to as functional dielectrics. Tailoring the properties of dielectrics and their interfaces to semiconductors is crucial, offering new opportunities to enable advanced functionalities that go beyond conventional applications.

In bulk semiconductor devices, the deposition of dielectric films can partially satisfy the surface defects caused by lattice termination, a process known as chemical passivation. These surface defects, when un-passivated, can act as carrier capture sites, and lead to loss of current and device instability. While bulk defects

can also degrade device performance, they are generally minimised in high quality materials, making defects at the semiconductor-dielectric interface the primary limiting factor for improving device efficiency [7]. One of the key parameters in evaluating the effectiveness of a chemical interface, and hence the dielectric passivation potential, is interface defect density (D_{it}). It describes the number of electronic states at a given energy level within the semiconductor bandgap. Defect states can also exist outside of the semiconductor bandgap, capturing carriers and becoming charged regardless of the changes in the Fermi level, which are referred to as fixed charges. Such fixed charges modify the density of either electrons or holes via the field-effect mechanism, thereby modifying the carrier capture process and enabling reductions in recombination. This process is referred to as field-effect passivation.

Chemical and field-effect passivation are the two most important strategies for surface passivation, which aims to mitigate the carrier capturing process near the semiconductor surface. Both the polarity and density of the fixed charges (Q_f), as well as the D_{it}, are strongly influenced by the type of semiconductor, the dielectric, and their deposition methods. In this section, these key parameters will be discussed in the context of silicon, which remains the most extensively studied bulk semiconductor system. The application of these dielectric layers in the context of surface passivation in silicon solar cells is further discussed in Section 1.3.

In contrast, 2D materials have van der Waals interfaces, which result in interactions with dielectrics that differ from those observed in bulk semiconductor-based systems. Therefore, Section 1.4 is dedicated to discussing the current understanding of these interactions.

I start by describing the four most used dielectrics in silicon solar cells and 2D material-based FETs: silicon oxide (SiO_x), silicon nitride (SiN_x), aluminium oxide (AlO_x), and hafnium oxide (HfO_x) [8], [9], [10], [11]. Each of these materials exhibits unique properties, such as forming high quality interface to silicon, offering tuneable optical properties, providing high density fixed charges, or having a high dielectric relative permittivity. These characteristics makes them indispensable for a variety of applications in semiconductor devices.

1.2.1 SiO_x

Silicon oxide (SiO_x) is the most employed dielectric in the semiconductor industry, primarily due to its low defect density interface to Si [11]. Silicon naturally forms a high-quality SiO_2 when oxidised, so the dielectric can be created directly from the substrate without adding foreign materials. There are various methods to grow SiO_x, which affect its bulk properties and its interface to silicon, making them suitable for different applications. The highest quality SiO_2 is grown thermally at 900-1200 °C, either dry (in dry oxygen) or wet (in water vapour), rendering a very low D_{it} to Si on the order of 10^{10} cm^{-2} eV^{-1} [12]. While wet thermal SiO_2 grows much faster than dry thermal SiO_2, a higher density of dangling bonds is introduced in the dielectric bulk, which reduces its breakdown strength [13]. Low-temperature grown SiO_x has also been studied extensively, as high-temperature processing is not ideal for industrial applications. Alternative growth techniques like atomic layer deposition (ALD) [14], plasma-enhanced chemical vapour deposition (PECVD) [15], wet-chemical oxidation

[16], [17], [18], [19], [20], and dry oxidation using O_3 [21], [22] have been explored. However, these methods typically result in a higher D_{it} of 10^{11} to 10^{13} cm^{-2} eV^{-1} [14], [19], [21]. Thus, despite of its high thermal budget, dry thermal oxide has been widely employed in complementary metal-oxide-semiconductor (CMOS) processing, but has now been gradually replaced by dielectrics with high relative permittivity (κ) due to scaling demand [23]. Meanwhile, in the PV industry, ultra-thin (<2 nm) low-temperature oxides are sometimes adopted to minimise the production cost [20].

The defects present at the Si/SiO_x interface have been well investigated. A schematic describing the types of defects, their recombination activities, and energy levels in relation to the conduction band minimum (CBM) and valence band maximum (VBM) is shown in Figure 1.2.1 [24]. Four types of dangling bonds with different back bond configurations are presented. Broad state distributions are formed due to statistic disorder in the bonds. Dangling bonds with three Si back bonds generate a symmetrical distribution of defect states in the bandgap, giving rise to both acceptor-like and donor-like states. Dangling bonds with one or two oxygen back bond forms donor-like states, which tend to donate an electron and become positively charged. Both types of defects create states inside of the bandgap and thus can capture electrons and contribute to performance degradation. Lastly, Si dangling bonds with three oxygen back bonds create an energy level above Si CBM, and thus stays positively charged, giving rise to a 5~20 × 10^{10} q cm^{-2} Q_f observed near the Si/SiO_x interface [25].

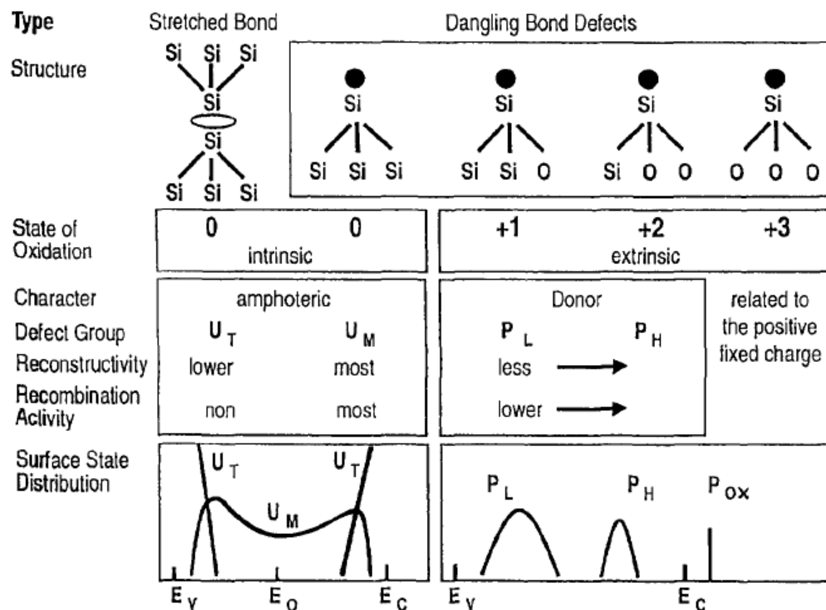


Figure 1.2.1 Defect model of the Si/SiO_2 interface, reproduced after [24].

1.2.2 SiN_x

Silicon nitride (SiN_x) films are typically deposited using PECVD with ammonia (NH_3) and silane (SiH_4) as precursors. Film properties including hydrogen concentration, positive Q_f, and refractive index depend heavily on the precursor ratios. In general, a lower NH_3/SiH_4 ratio results in a Si-rich film with higher refractive index, higher hydrogen content (Si-H and N-H bonds), and lower positive Q_f [26].

The most important defect present in SiN_x is the dangling bonds of Si back bonded to three N atoms (·Si≡N), also referred to as K centres. These defects exhibit amphoteric behaviour, meaning K-centres can stay in positive (K^+), negative (K^-) and neutral (K^0) charge state [27]. In most cases, K-centres are positively charged because their energy level is close to the CBM, giving rise to a positive Q_f on the level of 10^{12} q cm^{-2} [28], [29]. A schematic of the band diagram of SiN_x interfacing to Si is shown in Figure 1.2.2. While K-centres can be found throughout the bulk material, most of the positive charge is found close to the Si/SiN_x interface [27], [30]. The energy level of such K-centres has been reported to be right above the Si CBM [31], right below the CBM [32], or around the mid-gap [33]. The energy level of the defect states has also been reported to vary slightly depending on the stoichiometry ratio of the film [31]. External methods including corona charging and illumination have been demonstrated to manipulate the charge state of the defects and therefore change the overall Q_f [26], [29], [33].

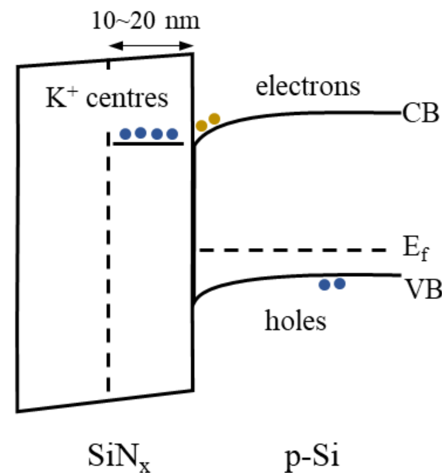


Figure 1.2.2 A schematic of the band diagram of SiN_x interfacing to p-Si, with K^+ centres lies up to 20 nm within the interface [27].

1.2.3 AlO_x

Aluminium oxide (AlO_x) is considered an excellent passivation layer since the introduction of ALD [34], [35]. This is primarily due to the high negative Q_f of 10^{12}~10^{13} q cm^{-2} found within 2~3 nm to the Si interface, which repulses electrons from Si surface and reduce its capture rate [18], [36]. At the same time, ALD-AlO_x was found to form a low defect density interface to Si with D_{it} on the level of 10^{11} cm^{-2} eV^{-1} [37]. PECVD-AlO_x, on the other hand, forms a lower quality interface due to plasma damage [38]. This superior interface quality makes ALD a preferred deposition technique despite of its long processing time. More recently, the emergence of spatial ALD sped up the deposition rate by 100 times by separating the precursors in space rather in time [39], making it easier and cheaper to scale up industrially.

Extensive studies have investigated the charging mechanism and its associated defects in AlO_x [18], [40], [41], [42], [43], [44]. It was found that the SiO_x interlayer formed between AlO_x and Si during the first few ALD cycles or post-deposition annealing plays an important role in determining the negative Q_f [42], [45],

[46], [47]. This is most likely related to the density of point defects present at the interface, which have been proposed to be Al vacancies and O interstitials by first principle calculations [48]. Experimentally, AlO_x layers with O-rich regions have been found to correlate with the negative charges [49]. Tetrahedral coordinated Al (AlO_4) has also been proposed to be the origin of the negative charge, and was found most abundant near the interface to Si [47], [50]. These defects are proposed to form acceptor-like states with energy levels right below the Si VBM, thus leading to a fixed negative Q_f [51].

Aside from the presence of chargeable point defects, a source of electrons within a tunnelling distance from the defects has also been shown to be essential for the negative Q_f formation [40], [44], [49], [51], [52], [53], [54], [55], [56]. A schematic of the band diagram of AlO_x interfacing to Si and the corresponding charging process is shown in Figure 1.2.3. In a Si/AlO_x system, the electron source has been proposed to be Si or dangling bonds near the interface [42], [57]. By intentionally increasing the thermal SiO_2 thickness between the AlO_x and Si from 0 to 10 nm, a decreasing negative charge density from 3 to 1 × 10^{12} q cm^{-2} was observed, indicating reduced tunnelling [57]. Meanwhile, 5 Å of HfO_x was found sufficient to eliminate the negative charge formation when deposited between AlO_x and Si [46].

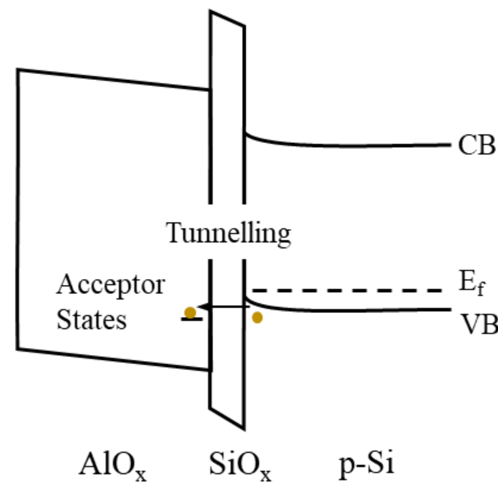


Figure 1.2.3 Band diagram illustrating charging of acceptor states near SiO_x/AlO_x interface from electrons near Si surface.

1.2.4 HfO_x

Hafnium oxide (HfO_x) is considered superior to SiO_x as a gate material in MOSFETs due to its high permittivity. Typical relative permittivity for HfO_x, along with SiO_x, AlO_x, and SiN_x are listed in Table 1.2.1 for reference. A higher dielectric constant increases $C_{ox}=\varepsilon_0\varepsilon_r/t$, so the same surface charge can be induced at lower voltage or keep the film thicker, thus strengthening electrostatic control while reducing current leakage. ALD is the most adopted deposition method for HfO_x for its high uniformity and controllability. A high defect density has been found in ALD-deposited-HfO_x, which lowers carrier mobility and leads to instability of the device [58]. However, these defects can act as fixed charge traps and are beneficial for field-effect passivation [59], [60].

Table 1.2.1 Typical relative permittivity for the four dielectric materials discussed in this thesis. Reproduced from [61].

Dielectric	Relative Permittivity (ε_r)
SiO_x	3.9
AlO_x	8.5-9
SiN_x	6.2
HfO_x	25

Oxygen interstitials and vacancies are identified as the most likely intrinsic defects in HfO_x bulk, while the energy level of such defects, especially at the interface to Si, is still under debate [58]. Energy levels of the intrinsic defects in bulk HfO_x have been calculated by K. Xiong et al. and shown in Figure 1.2.4 [58]. The fixed charge Q_f observed at Si/HfO_x is not universal in sign: Warwick's recent work systematically maps these dependencies—including precursor selection [62], co-reactant effects (O_2 plasma/O_3/H_2O), thickness/anneal windows [63], and demonstrates that stacking ALD-SiO_x/HfO_x enables tuneable field-effect passivation for silicon solar cells [64], [65]. As-deposited HfO_x on Si is reported to hold a positive Q_f on the level of 10^{12} q cm^{-2} [59], [66]. Annealing reduces the positive Q_f, which is related to the transformation from amorphous to polycrystal phase near the Si/HfO_x interface [67], [68]. Interdiffusion between HfO_x and Si is also likely to happen during annealing and form a SiO_2/Hf-O-Si interlayer, whose structure depends greatly on the amount of oxygen provided [69]. The existence of deep acceptor states has been reported empirically, which can be filled when annealed under N_2 ambient, leading to a less positive or negative Q_f, but neutralised when annealed in H_2 ambient, leading to a positive Q_f [59], [70]. HfO_x films subjected to different annealing conditions result in variation in interface structures with trapping states of different density and energy levels, which ultimately leads to the alteration of Q_f [59], [66], [67], [70].

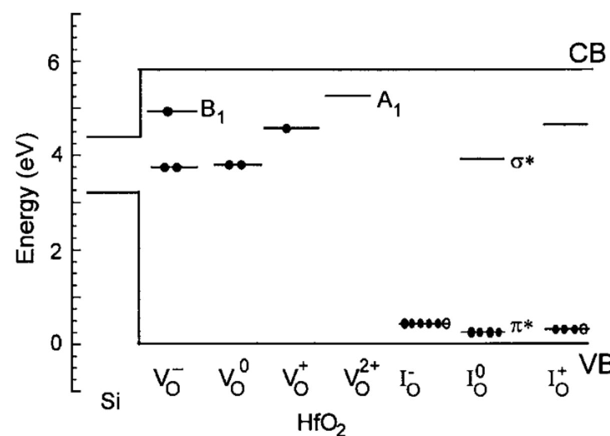


Figure 1.2.4 Summary of calculated energy levels of the relaxed O vacancy (V_O) and interstitial (I_O), in their various charge states in bulk HfO_x, reproduced after [58].

1.3 Surface Passivation in Silicon Solar Cells

This section focuses on the application of dielectric layers on the surface passivation of silicon solar cells. The operation of silicon solar cells relies on the collection of photogenerated carriers at metal contacts. To achieve

high-efficiency devices, it is crucial to minimise carrier capture at defect states, which can be realised with the deposition of dielectrics. To evaluate the effectiveness of different passivation layers, it is essential to understand the carrier capture mechanisms and their associated interface parameters. This section will focus on the Shockley-Read-Hall (SRH) surface recombination, while a description of bulk recombination is included in Appendix A. Considerations when incorporating different dielectric stacks into solar cell devices will also be discussed.

1.3.1 Surface Recombination

Large density of defects is present near the semiconductor/air interface due to the termination of crystalline structure, leading to strong surface recombination governed by SRH statistics. Such interface defects induce energy states throughout the bandgap, and its density D_{it} can be expressed as a function of energy. The surface SRH recombination rate is defined as:

$$U_{surface} = \int_{E_v}^{E_c} \frac{n_s p_s - n_i^2}{\frac{p_s + p_1}{D_{it}\sigma_n v_{th}} + \frac{n_s + n_1}{D_{it}\sigma_p v_{th}}} dE = \int_{E_v}^{E_c} \frac{n_s p_s - n_i^2}{\frac{p_s + p_1}{S_n} + \frac{n_s + n_1}{S_p}} \quad (1.3.1)$$

where n_s and p_s are the electron and hole concentrations at the surface. Here S_n and S_p are defined as the energy-dependent electron and hole capture velocities. The surface recombination velocity (SRV) is defined as the reciprocal of the surface lifetime ($\tau_{surface}$) that describes the total recombination activity at a charge-neutral surface. In reality, the presence of surface charge induces changes in carrier concentration, thus band-bending near the semiconductor surface that modifies recombination activity within the region. Effective SRV (S_{eff}) is thus introduced to account for the recombination in the band-bending region.

As S_{eff} cannot be measured directly, it is usually extracted from effective lifetime (τ_{eff}). The bulk lifetime (τ_{bulk}) is first calculated by adding the different mechanisms of bulk recombination from radiative, Auger, and SRH process of the bulk. Then S_{eff} can be calculated using the simplified approximation:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{W} \quad (1.3.2)$$

where W is the wafer thickness. It has been reported that S_{eff} is a term dependent upon the injection level [71]. A preferable approach to evaluate the effectiveness of surface passivation is by surface saturation current density (J_{0s}). Over a large range of conditions, J_{0s} is independent of the injection level. In this work, S_{eff} and J_{0s} are extracted following Kimmerle's formalism described in [72], which take account of the finite carrier diffusion coefficient leading to a reasonably injection-independent J_{0s} extraction.

1.3.2 State of Art in Surface Passivation of Silicon Solar Cells

The two main strategies of reducing surface recombination involve minimising the S_n and S_p, or the $n_s p_s$ terms in Equation (1.3.1), namely chemical and field-effect passivation. The commonly used dielectrics and their corresponding D_{it} and Q_f interfacing to Si has been discussed in Section 1.2. Effective passivation involves the

optimisation of both chemical and field-effect passivation. Here, the incorporation of such dielectric materials into cell structures will be discussed briefly.

When passivation layers are incorporated into devices, more factors including their optical properties, compatibility with metal contact, stability, and processing budget must be considered [73]. A summary of the passivation effectiveness of the dielectric layers on differently doped surfaces is shown in Table 1.3.1 [73]. In general, the most suitable passivation layers for a n-type (p-type) surface are positively (negatively) dielectrics. This is due to parasitic shunting, which refers to the loss of efficiency due to the formation of an unintended conductive pathway across the *n* and *p* carrier collecting sides. For example, while the positive charges in SiO_2 and SiN_x can induce effective field-effect passivation on both n and p-type surfaces, a high conductance pathway for electrons is formed on p-type surfaces, thus reducing the short-circuit current density [74]. For p-type surfaces, such an effect can be effectively removed with AlO_x. However, the industrial metallisation paste (Al) was found to degrade the passivation and require a SiN_x capping layer for protection. Finally, while SiO_2 has demonstrated excellent passivation on n-Si, it is not suitable for p^+ surfaces due to surface depletion of the boron emitter caused by the high solubility of boron in SiO_2 [75].

Table 1.3.1 Summary of the effectiveness of different passivation dielectric layers on different surfaces (based on τ_{eff}), reproduced after [73].

Dielectric layer	Doping type			
	p	n	p^+	n^+
SiO_x	✓	✓	×	✓✓
SiN_x	✓	✓✓	×	✓
Al_2O_3	✓✓	×	✓✓	×
TiO_2	✓✓	✓	✓	✓
HfO_2	✓	✓✓✓	✓	✓✓
SiO_2/SiN_x	✓✓	✓✓✓	✓	✓✓✓
$SiO_2/SiN_x/SiO_xN_y$	✓✓	✓✓	✓	×
Al_2O_3/SiN_x	✓✓✓	✓	✓✓✓	✓
$SiO_2/Al_2O_3/SiN_x$	✓	✓	✓✓✓	✓✓

× - ineffective, ✓ - less effective, ✓✓ - moderately effective, ✓✓✓ - highly effective.

1.4 2D MoS_2-based Field-Effect Transistors

This section will focus on the role of dielectrics in 2D MoS_2-based field-effect transistors (FETs). FETs are semiconductor devices that operate by controlling the flow of charge carriers within a channel through an externally applied electric field. In 1960, the invention of MOSFETs at Bell Labs marked the start of the modern semiconductor industry [76]. Over the past decades, silicon has been the most widely used material, largely due to its ability to form a high-quality SiO_2 layer, serving as a gate dielectric [11]. This allows effective control over the channel conductance, fast switching speeds, and low leakage current.

Extensive efforts have been invested in the miniaturisation of FETs, adhering to Moore's law [77], which predicts the exponential growth of the number of devices per chip over time. However, in recent years, bulk semiconductor-based FETs have encountered significant challenges as device channel length approaches 3-5

nm. At these dimensions, device operation is hindered by various physical phenomena, including quantum tunnelling, and thickness-fluctuation-induced scattering [5]. To address these challenges, 2D semiconductors have emerged as a promising candidate to replace or complement silicon in further downscaling device dimensions. Furthermore, enhanced control over channel conductance enables lower off-state current, thereby improving energy efficiency [2], [5], [6].

1.4.1 Basic Properties of 2D MoS_2

2D molybdenum disulfide (MoS_2) is a member of the transitional metal dichalcogenides (TMDs) family with a structure of Mo atoms sandwiched between two sulphur atoms, forming a three-atom thick monolayer. A schematic diagram of a 2D MoS_2 is shown in Figure 1.4.1 [78]. In bulk MoS_2, the layers are weakly bonded by van der Waals force, allowing monolayers to have dangling bonds-free surfaces. This enables 2D MoS_2 to be easily integrated with other van der Waals-structured materials while maintaining a relatively clean interface. More importantly, their atomically thin structures confine the carriers in a 2D channel, which can be precisely controlled by the gate voltage. 2D MoS_2 also has a direct bandgap of 1.8 eV and a comparable mobility (~ 400 $cm^2 V^{-1} s^{-1}$) to silicon [79]. These unique properties have made 2D MoS_2 an appealing candidate for various applications in electronics and optoelectronic devices. 2D MoS_2 is hence selected and studied in this thesis as a key material for future nanoelectronics.

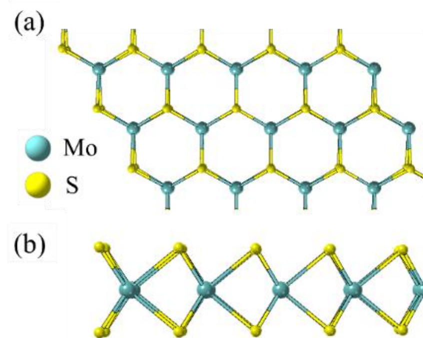


Figure 1.4.1 (a) Top view, and (b) front view of 2D MoS_2, reproduced from [78].

A strong photoluminescence (PL) is found in 2D MoS_2, primarily attributed to its direct bandgap [80]. The optical processes are dominated by excitons (electron-hole pairs), arising from the strong Coulomb interactions between the confined carriers [81]. Schematics of a fitted PL spectrum with marked peaks and their corresponding origin illustrated in the band diagram is shown in Figure 1.4.2. Exciton A and B with peaks around 1.84 and 1.98 eV are both present, due to the spin-orbit coupling induced valence band splitting. Excess electrons lead to the formation of A^- trions, giving rise to a red-shifted peak relative to A^0 in the spectrum [82]. A fourth peak, attributed to A_{xx} biexciton may emerge at a lower energy as a result of exciton-exciton interactions. By collecting and analysing the emitted photons, information including optical bandgap, layer thickness, doping density, defect states and material quality can be obtained [82], [83], [84].

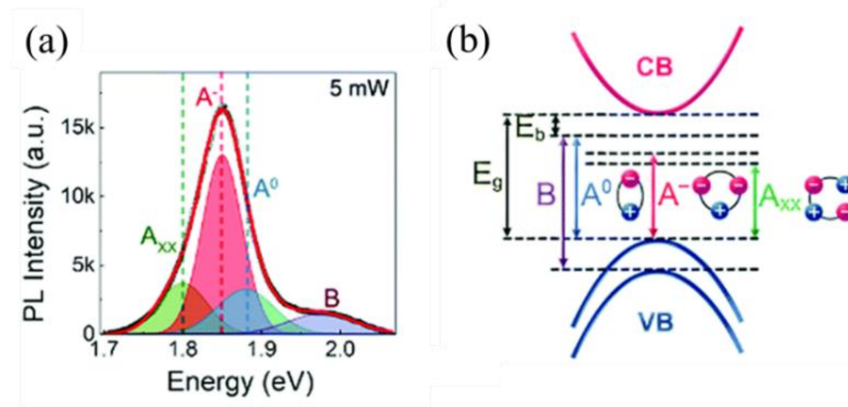


Figure 1.4.2 (a) A fitted PL spectrum marking the presence of A, B excitons, A^- trions, and A_{xx} biexcitons and (b) their corresponding energy transitions in the bandgap, reproduced after [85].

Vibrational properties provided by Raman spectroscopy are also important in the study of 2D MoS_2. The two typical vibration modes E_{2g} and A_{1g} arise from the in-plane opposite vibration of two S atoms and the out-of-plane vibration of S atoms, respectively [86]. An illustration of the vibration modes and their corresponding peaks in Raman spectrums is shown in Figure 1.4.3. Decreased van der Waals forces with fewer layers of MoS_2 lead to a red shift of A_{1g} and a blue shift of E_{2g}. The distance between the two peaks is found to vary significantly with increasing layer numbers until five, where the peak locations are the same as measured in bulk MoS_2, as shown in Figure 1.4.3 (b) [87]. In monolayer MoS_2, the peak difference is measured ranging from 17.5~21 cm^{-1} [88], [89]. Doping is also found to affect the peak positions. The A_{1g} vibration mode is particularly sensitive to long-range Coulomb interactions, which results in blue shifts of the peak with strong n-type doping. Meanwhile, E_{2g} mode is dominated by covalent bonding between Mo and S atoms, resulting in minimal peak shifts upon doping [90].

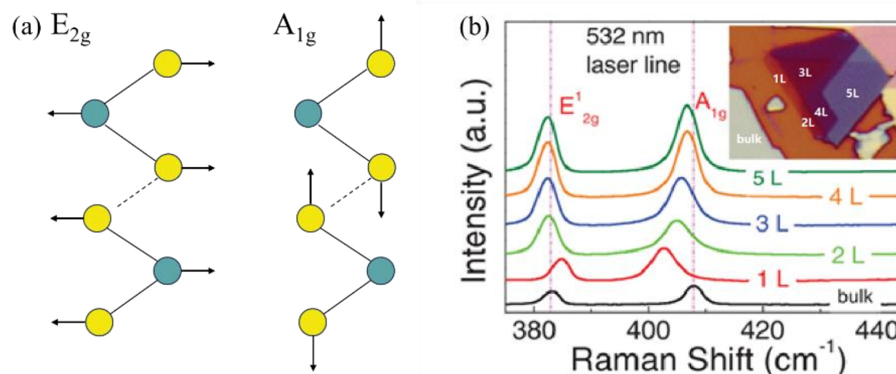


Figure 1.4.3 (a) Vibration modes of MoS_2. (b) Raman spectroscopy of MoS_2 with increasing layer numbers, and their identified E_{2g} and A_{1g} peaks, reproduced after [87].

1.4.2 Working Principle of 2D MoS_2-based FETs

The operation of FETs requires a source (S) and a drain (D) electrode, which are connected to the semiconductor to measure its conductance. An additional gate (G) electrode is required to form a metal-oxide-semiconductor (MOS) structure to control the conductance of the semiconductor via field-effect. Depending

on the relative position of these electrodes to the 2D MoS_2, different device structures have been designed and greatly affects device performance [91], [92]. Among them, back-gate top-contact (BGTC) configuration is the most widely adopted due to its ease in fabrication. A schematic of the BGTC structure is shown in Figure 1.4.4. All devices in this thesis are based on the BGTC configuration.

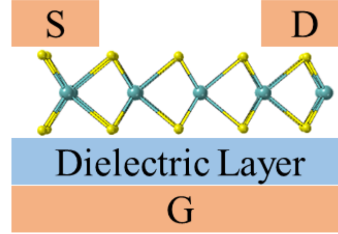


Figure 1.4.4 Schematic of a back-gate top-contact structured 2D MoS_2-based FET.

To understand the working principle of 2D MoS_2-based FETs, the scenario where a 2D MoS_2 channel is in contact with drain and source electrodes is first considered. Figure 1.4.5 (a) illustrates the band diagram of metal contacts and a 2D MoS_2 channel before contact. Here, we consider aluminium (Al) as the metal, which is used as contacts in this thesis. 2D MoS_2 is generally considered a n-type semiconductor in its pristine form [93], with a work function higher than Al (W_m<W_s). After contact, electrons in Al flow towards MoS_2 due to their work function difference, which rise the electron energy in MoS_2 near the contact region. This result in a downward band bending in MoS_2, as shown in Figure 1.4.5 (b).

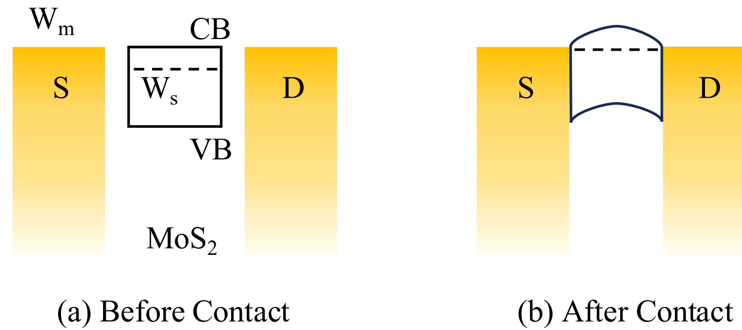


Figure 1.4.5 Band diagrams of source (S) and drain (D) electrodes (a) before and (b) after in contact with an 2D MoS_2 with W_m<W_s.

Next, the control of the current flow between S and D electrodes by gate voltage (V_{gs}) is discussed, demonstrated by the schematics in Figure 1.4.6. First, when a small positive drain-source voltage (V_{ds}>0) is applied, the potential difference drives electrons to be injected from the S to the 2D MoS_2 and collected by the D electrode, as shown in Figure 1.4.6 (a). This gives rise to a drain-source current (I_{ds}), whose value depends on the carrier density in the channel. When a negative V_{gs} is applied, excess holes are mirrored into the channel due to field-effect, leading to a decrease in the Fermi level in relative to the valence band, as shown in Figure 1.4.6 (b). Due to the reduced electron density, a smaller or neglectable I_{ds} is measured with the same V_{ds} applied (off-state). Hole conductance is possible, given a sufficiently high V_{ds} is applied to overcome the Schottky barrier (Φ_{SB}). More commonly, high work function metals such as platinum (Pt) and palladium (Pd) are used

to demonstrate p-type FETs based on 2D MoS_2 [94]. When a positive V_{gs} is applied, more electrons are injected into the channel, resulting in an increase in conductance and hence higher I_{ds} (on-state), as shown in Figure 1.4.6 (c). With strong negative V_{gs}, high density of holes can be generated in the channel.

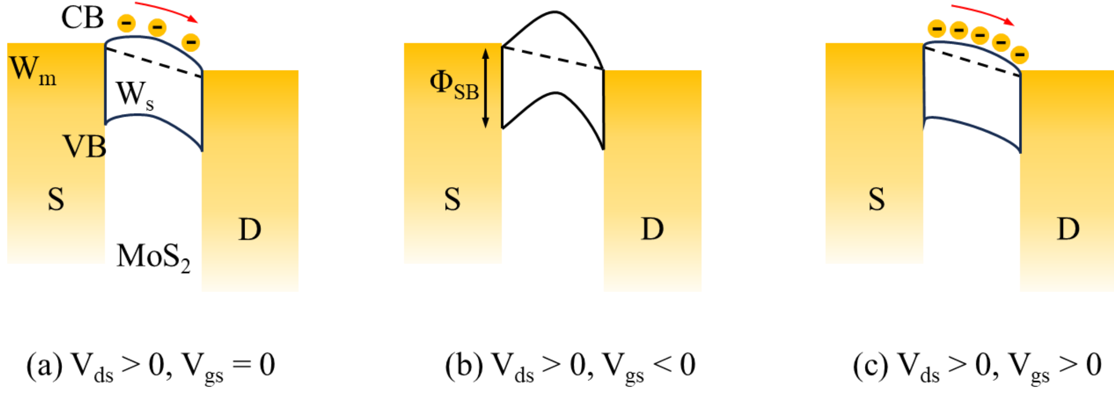


Figure 1.4.6 Band diagrams of the working principle of 2D MoS_2 FETs where $W_m<W_s$ with a small positive V_{ds} applied, and (a) $V_{gs} = 0$, (b) $V_{gs} < 0$, and (c) $V_{gs} > 0$. The arrow implies the direction of the electron flow. The difference between the MoS_2 CBM and the Fermi level is the Schottky barrier height Φ_{SB} for hole conduction.

1.4.3 Key Parameters in 2D MoS_2-based FETs

The performance of a 2D MoS_2-based FET can be evaluated through transfer and output characteristics. Transfer characteristics are obtained by analysing the changes in I_{ds} in response to different V_{ds}, as shown in Figure 1.4.7 (a). Meanwhile, the output characteristics are obtained by measuring the I_{ds}-V_{ds} relations at different V_{gs}, as shown in Figure 1.4.7 (b). When V_{gs} is smaller than the threshold voltage (V_{th}), the device is in off-state. When the device is turned on, and $V_{ds} < |V_{gs} - V_{th}|$, the FET operates in a linear region, where the behaviour of the channel is analogous to a resistor, as shown in Figure 1.4.7 (b). The current in the channel can be described by:

$$I_{ds} = \frac{W}{L}\mu C_i(V_{gs} - V_{th})V_{ds} \tag{1.4.1}$$

Where W is the channel width, L is the channel length, μ is the mobility, C_i is the dielectric capacitance per unit area. At larger V_{ds}, where $V_{ds} > |V_{gs} - V_{th}|$, the I_{ds} becomes independent of the V_{ds}, namely saturation region. This is due to the reduced number of electrons near the drain electrode, which is further described in [95]. In the saturation regin, I_{ds} in the channel can be described as:

$$I_{ds} = \frac{W}{2L}\mu C_i(V_{gs} - V_{th})^2 \tag{1.4.2}$$

In this thesis, all devices operate in the linear region.

From the transfer characteristics, key materials properties including doping density and mobility can be extracted. Assuming all the charge induced by the gate voltage is mirrored into the channel, the electron density (n_{el}) can be calculated from:

$$n_{el} = C_i \frac{V_{gs} - V_{th}}{q} \tag{1.4.3}$$

where q is the elementary charge. The doping density can be calculated at V_{gs} = 0. Different methods can be applied to extract the V_{th} of FETs, as reviewed in [96]. The most commonly adopted method is the extrapolation in the linear region method (ELR), where V_{th} is extracted by finding the axis intercept (I_{ds} = 0) of the linear extrapolation of the transfer curves, as demonstrated in Figure 1.4.7 (a).

Additionally, mobility can be extracted from the slope of the linear region of an on-state FET, as can be deduced from Equation (1.4.1):

$$\mu_{FE} = \frac{L}{W C_i V_{ds}} \frac{\partial I_{ds}}{\partial V_{gs}} \tag{1.4.4}$$

Here μ_{FE} refers specifically to field-effect mobility, which represents the carrier mobility in the channel of a FET. This is a device property which takes account of the materials quality, the quality of the semiconductor-dielectric interface, and the effectiveness of gate control.

In addition, the on/off ratio and subthreshold slope are also important parameters in evaluating the operation of FETs. In this thesis, I focus on studying the electrical properties of 2D MoS_2 using transfer measurements by extracting the V_{th} and μ_{FE}.

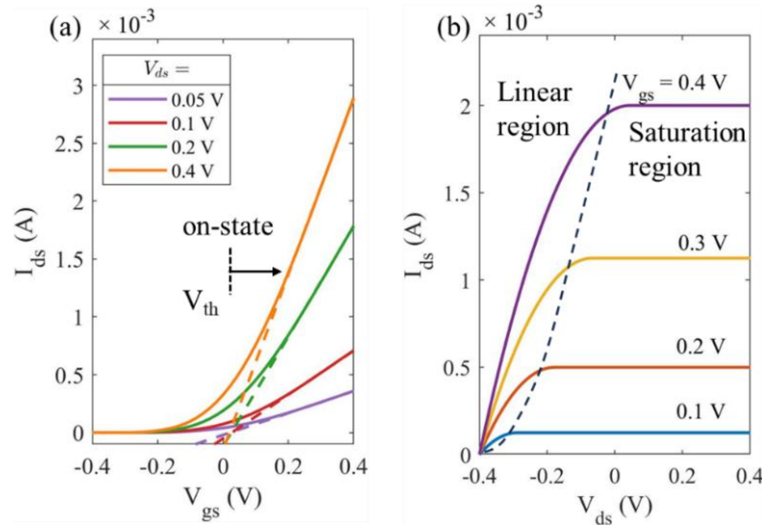


Figure 1.4.7 (a) Transfer characteristics of 2D TMD FETs at different gate drain-source voltages (V_{ds}). (b) Output characteristics of 2D TMD FETs at different back gate voltages (V_{gs}), reproduced after [97].

1.4.4 Interactions between 2D MoS_2 and Dielectrics

The atomically thin nature of 2D TMDs, such as 2D MoS_2, results in high sensitivity to the surrounding environment, particularly dielectric materials. These interactions can induce shifts in Fermi level across the entire 2D layer and significantly affect its properties. Such effects often contribute to device variations. However, when carefully controlled, they can be exploited to enable advanced device functions. Understanding

these effects is essential for studying and manipulating the material properties of 2D MoS_2. Key mechanisms including dielectric screening and charge transfer are next reviewed.

1.4.4.1 Dielectric Screening

Charge carriers in 2D materials have stronger Coulomb interactions compared to bulk systems due to their reduced spatial dimensions [98]. These stronger electron-hole interactions give rise to stable excitons even at room temperature, enabling advanced optoelectronic applications [99]. The tightly bounded excitons also lead to the renormalisation of the bandgap [98], [100]. When 2D materials are placed on a dielectric, the dielectric becomes polarised in response to the electric field generated by carriers in the 2D materials – a process referred to as dielectric screening. The strength of the screening effect depends on the dielectric relative permittivity of the environment. Such screening reduces the Coulombic interactions between charge carriers, leading to lower exciton binding energies and bandgap renormalisation [101]. The sensitivity of 2D materials to their surrounding dielectrics can thus be utilised for bandgap engineering, which shows potential for integration of multifunction photonic devices in the 2D plane [102].

It is important to note that this effect is primarily discussed in the context of optoelectronic devices and is not the focus of this thesis. However, its potential impact in analysing material properties, particularly when using photoluminescence spectroscopy (PL), must be considered.

1.4.4.2 Charge Transfer

Charge transfer from intentionally deposited molecules on the surface of 2D TMDs has been widely studied as a doping technique. Both n-type and p-doping have been demonstrated using strong electron donors or acceptors, enabling doping levels of 10^{12} q cm^{-2} [103], [104], [105], [106]. However, such doping effects are largely unstable under ambient conditions or involve highly reactive chemicals, making them less suitable for making high-performance FETs [103], [107], [108].

Charge transfer is also present between 2D TMDs and their surrounding dielectrics. Due to the van der Waals surface of 2D TMDs, their interfaces to dielectrics remain largely un-passivated, leading to a high density of interface defects. Such defects also arise from vacancies in the channel material [109], [110], [111], or hybridisation between 2D TMDs and dielectrics [112]. The defect states inside of the semiconductor bandgap can capture/release carriers depending on the Fermi level, leading to unintentional doping and large variations in device threshold voltages [108]. Charged defects also interact with the carriers in 2D TMDs and cause mobility degradation due to Coulomb scattering [112].

Aside from defects at the 2D channel-dielectric interface, border defects located a few nanometres from the 2D/dielectric interface should also be considered. An illustration of defects present in a 2D TMDs/dielectric system is shown in Figure 1.4.8. These border traps can be intrinsic oxygen vacancies, in the case of SiO_x and HfO_x [113], or extrinsically caused by trapped hydrogen atoms [114]. The charging/discharging behaviour of border defects varies with different oxides, deposition condition as well as post-deposition annealing process

[115], [116]. Unlike interface defects, border defects interact with 2D TMDs by a slower process of tunnelling, as evidenced by *1/f* noise studies [115], [117]. When sufficient energy is provided – either during processing or operation – charge carriers can overcome the energy barrier at the 2D TMD/dielectric interface, leading to unintentional doping and thus device instability. However, due to the longer distance between the charged state and channel carriers, the effect of remote Coulomb scattering may be reduced, leading to less or no mobility degradation [112].

Due to the reduced variability of border defects, they can be intentionally incorporated into dielectrics for advanced applications. Widiapradja et al. reported a charge injection memory transistor utilising the defects at the SiO_2/HfO_2 interface, which lie 5 nm from the 2D MoS_2/SiO_2 interface [118]. Electron capturing and releasing at the SiO_2/HfO_2 interface defects under external voltage can fulfil the function of writing and erasing required for memory devices.

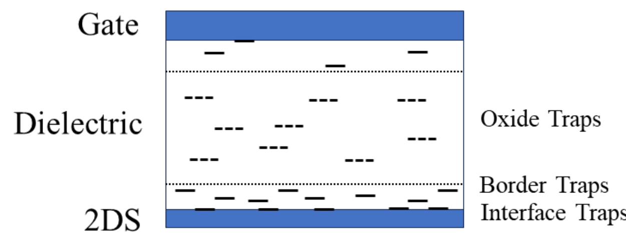


Figure 1.4.8 Schematic diagram of different trap states in 2D semiconductors (2DS) -dielectric system, including oxide traps, border traps, and interface traps, reproduced after [119].

Various methods have been used to extract the D_{it} at different 2D MoS_2/dielectric interfaces, as summarised in Table 1.4.1. Compared to the well-established Si/SiO_2 interface, D_{it} between dielectrics and MoS_2 are generally 1-3 magnitudes higher. The lowest D_{it} was found between MoS_2 and van der Waals insulators such as hexagonal boron nitride (hBN). However, it is important to account for differences in the extraction techniques. For example, subthreshold swing equation (SS equation) neglects the impact of Schottky barriers, potentially introducing uncertainty in the extracted D_{it} values. Capacitance-voltage (C-V) measurements at high frequencies (MHz) primarily capture fast interface defects [115], whereas *1/f* noise measurements are more sensitive to border traps near the interface [119], [120]. To reduce D_{it}, post-deposition treatments such as annealing are employed to improve interface quality [121]. Local oxidation of 2D TMDs, as in a HfS_2/HfO_2 system, can significantly improve the 2DS/dielectric interface quality by inducing structural reconstruction [115].

Table 1.4.1 D_{it} reported in selected literature with different dielectric/MoS_2 interface and extraction method partially adopted from Ref. [115]. 1L refers to one layer, and ML refers to multilayers (>5).

References	Interface	Channel MoS_2	D_{it} [$cm^{-2}eV^{-1}$]	Extraction Method
Boutchacha et al. [122]	Si/SiO_2	0.18μm Si	~10^9	*1/f*
Vu et al. [123]	MoS_2/hBN	Exfoliated 1L	5×10^9	*1/f*
Na et al. [124]	MoS_2/SiO_2	Exfoliated ML	7×10^{10}	*1/f*
Pan et al. [125]	MoS_2/cryst.-HfO_2	Exfoliated ML	5×10^{11}	electrical conductance equation
Xia et al. [111]	MoS_2/HfO_2	Exfoliated 1L	7×10^{11}	C-V
Liu et al. [126]	MoS_2/Al_2O_3	Exfoliated ML	2.4×10^{12}	SS equation
Liu et al. [127]	MoS_2/SiO_2	CVD 1L	1.6×10^{13}	SS equation
Lee et al. [128]	MoS_2/SiO_2	Transferred CVD ML	2.1×10^{13}	SS equation
Zhao et al. [110]	MoS_2/Al_2O_3	Exfoliated ML	1×10^{13}	C-V

Besides defects within the bandgap, deep states close to CBM or VBM of 2D TMDs can also lead to unintentional doping, but less affected by shifts in the Fermi level. The doping density and polarity depends strongly on the defect type and their energy levels, which is affected by the stoichiometry ratio of both the channel and the dielectric, as well as the processing [109], [110], [129], [130], [131]. For example, MoS_2 generally displays n-type conductivity due to the charging of intrinsic sulphur vacancies or carbon impurities [93]. However, both n-type and p-type conductivity has been reported on devices made on SiO_2 substrate, which is largely attributed to the difference in interface defects [131], [132]. First principle calculation revels that by adding a donor-like or acceptor-like defect state to an ideal SiO_2 substrate, the Fermi level of MoS_2 shifts towards n and p-type respectively [133].

Other commonly used gate dielectrics including AlO_x and HfO_x have also been adopted in making 2D TMD FETs. A high electron density of > 2×10^{13} q cm^{-2} was found in monolayer MoS_2 with a AlO_x capping layer [112]. Such high doping density is proposed to arise from a defect energy level above the CBM of MoS_2, which donates its electrons to the MoS_2 leading to n-doping. The dominant defect state at HfO_x/MoS_2 interface has been proposed to be oxygen vacancies, which forms a deep state level above the CBM of MoS_2 [130]. Such deep state is believed to alter the bandgap of MoS_2, leading to n-type doping. HfO_x has also been shown enhance channel mobility due to its stronger screening effect, which arises from its high-κ nature [134]. However, studies on the 2D TMDs/dielectric interface – particularly on the types of defects and their corresponding energy levels – are still under investigation. The challenge lies on the strong Coulomb interactions between channel carriers and various charged defects, which lead to large variability introduced by channel and dielectric stoichiometry, channel thickness and device structures [133].

Finally, it is important to note that the complete picture of 2D TMD-dielectric interactions also include doping by electrostatic dipole or hybridisation between the dielectric and 2D TMDs. A schematic of a non-ideal 2D TMDs/dielectric interface summarising the potential mechanisms is shown in Figure 1.4.9 [108]. To mitigate these complex and uncontrollable interactions, additional layers such as poly(methyl methacrylate) (PMMA), self-assembled monolayers or hBN can be inserted between 2D TMDs and dielectrics [108], [135]. However, these materials are not compatible with current CMOS processes.

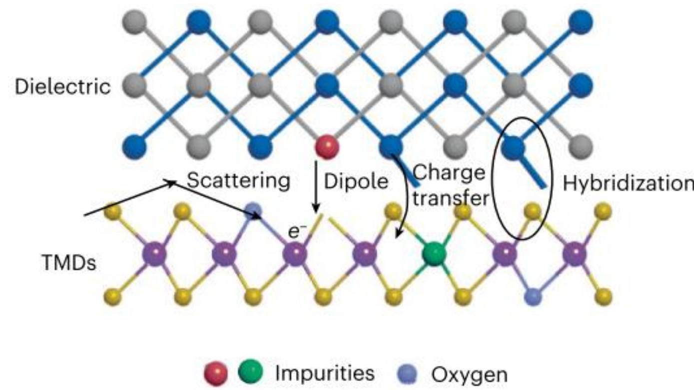


Figure 1.4.9 Schematic of a non-ideal 2D TMDs/amorphous dielectric interface. Possible interactions include: (a) carrier scattering leading to mobility degradation, (b) interface dipoles due to charge impurities in the dielectric, (c) charge transfer between the dielectric and 2D TMDs, and (d) hybridisation between dielectric dangling bonds and 2D TMDs. Reproduced after [108].

1.5 Summary of Band Alignment and Defect Levels in Relevance to Si and 2D MoS_2

In Section 1.3 and 1.4, the various interactions between semiconductors and dielectrics were reviewed. Interface and border defects significantly impact device performance, leading to degradations or, when intentionally designed, advanced functions. Here, a summary of the band diagram highlighting the key defects and their energy levels in relation to Si and 2D MoS_2 is provided. Figure 1.5.1 presents a summary of calculated thermodynamical defect charge state transition levels at the Si-SiO_2 interface [136], in amorphous AlO_x bulk [51], the energy levels of relaxed defects in different charged state in bulk HfO_2 [58], and experimentally observed defect states of K-centres at the Si-SiN_x interface from Ref.1 [31], Ref.2 [32], and Ref.3 [33]. This summary provides a guidance for designing suitable dielectric stacks for high-performance semiconductor devices based on Si or 2D MoS_2.

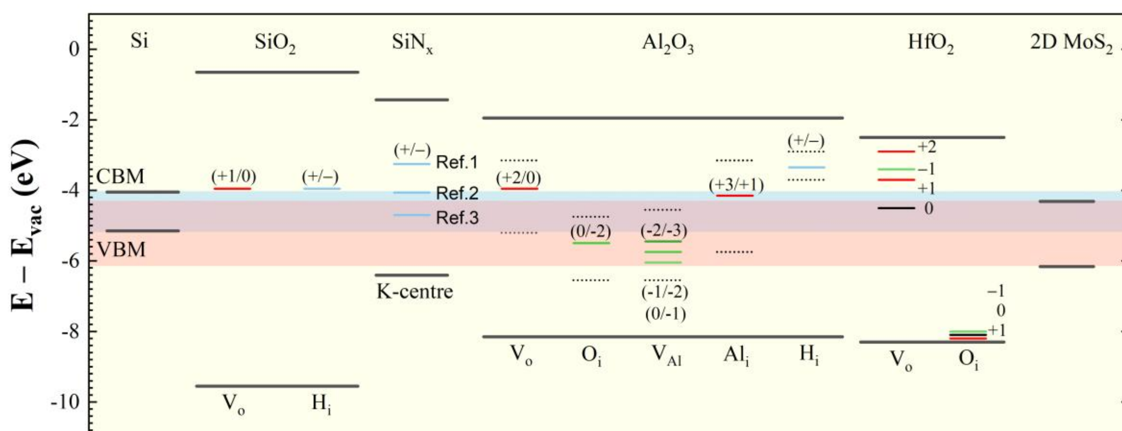


Figure 1.5.1 Summary of calculated thermodynamical charge transition levels of the most studied defects in different dielectrics and their relative position to the CBM and VBM of Si and 2D MoS_2. The blue and red shaded strip offers visual aid of the bandgap of Si and 2D MoS_2 respectively. The red lines represent donor-like defect levels, the green lines represent acceptor-like defect levels, and the blue lines represent amphoteric defects with a negative U. The numbers parentheses represent the transition of different charge states. For example, (+1/0) implies the defect stays positively charged when above the energy level, while stays charge neutral when below the energy level.

1.6 Thesis Objectives and Outline

The overall objective of this thesis is to develop functional dielectrics and study their interactions with semiconductors (Si and 2D MoS_2) to enable improved device performance. This thesis is split into three sections. The first section contains Chapter 1 and 2, which discuss literature on the most relevant dielectrics and their interactions with semiconductors, as well as the fabrication and characterisation techniques for such studies. The second section contains the main results, Chapter 3 to 7. The last section, Chapter 8, summarises the main findings and future work.

Dielectric stacks with negative fixed charges were identified as particularly interesting. Chapter 3 contains the development of such charged dielectrics. Chapter 4 and 5 focuses on their application to silicon surface passivation, including an in-depth understanding of the interface properties. The application of negatively charge dielectrics on 2D MoS_2 doping is then explored. Chapter 6 presents a novel all-dry FET fabrication process, which enables studies of field-effect doping of 2D MoS_2 using charged dielectrics in Chapter 7.

Chapter 2
Materials and Experimental Methods

2.1 Wafer Substrates

A summary of the silicon wafers used in this work is shown in Table 2.1.1. Mono-crystalline silicon wafers grown by the Czochralski (Cz) or Float Zone (FZ) method were used for different studies. Compared to FZ, wafers grown by the Cz method have lower production cost, but contain higher interstitial oxygen and a different impurity background [137]. For optimising the passivation quality on Si, high-quality FZ wafers were used to isolate the recombination activity of the Si surface without effects from the bulk. More cost-effective Cz wafers were used for other studies. Wafers from MEMC were 6-inch, while wafers from Fraunhofer ISE and University Wafer were 4-inch. Both single-side polished (SSP) and double-side polished (DSP) wafers were used. For Set 2 and 4, the thermal SiO_2 was removed by hydrofluoric acid (HF) prior to subsequent processing. For Sets 5 and 6, the thermal SiO_2 was used as gate dielectric in 2D MoS_2 FETs. The types of wafers used will be denoted as Sets 1 to 6, with a description of the subsequent processing provided in the relevant sections.

Table 2.1.1 Summary of the silicon wafers used in this thesis. * Measured values.

Label	Type	Resistivity (Ω·cm)	Thickness (µm)	Thermal SiO_2 (nm)	Surface	Source
Set 1	n-type Cz Si	30-60	675	No	SSP	MEMC
Set 2	n-type FZ Si	0.9-1.0*	200	100	DSP	Fraunhofer ISE
Set 3	p-type Cz Si	18-19*	500	No	SSP	University Wafer
Set 4	p-type FZ Si	0.9-1*	200	10	DSP	Fraunhofer ISE
Set 5	p-type Cz Si	10-20	500	300	SSP	University Wafer
Set 6	p-type Cz Si	1-10	500	300	SSP	University Wafer

2.2 Film Deposition

2.2.1 Atomic Layer Deposition (ALD)

In this thesis, nanolayer dielectrics including SiO_x, AlO_x, and HfO_x are grown by thermal ALD. Figure 2.2.1 illustrates the reaction mechanism using AlO_x as an example. Depositing one layer of AlO_x involves the injection of $Al(CH_3)_3$ (TMA) and H_2O as precursors. The compounds chemically absorb to the substrate surface until the area is fully covered. The injection of each precursor is separated by a purging step, during which excess precursor and reaction by-products are removed. The precursor absorption in each step is self-limiting, which leads to a layer-by-layer growth and high-quality films.

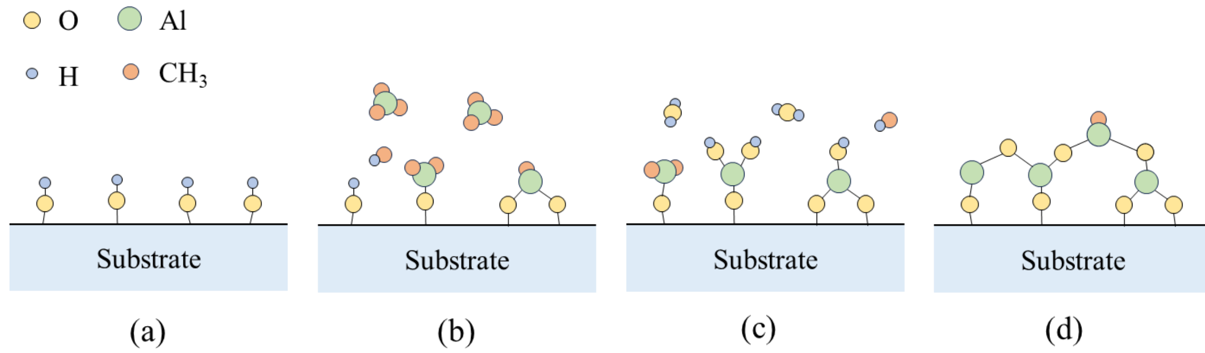


Figure 2.2.1 Reaction mechanism of thermal ALD using $Al(CH_3)_3$ and H_2O as precursors: (a) -OH terminated substrate surface, (b) chemical absorption of $Al(CH_3)_3$ forming a Al-terminated surface and CH_4 as by-products, (c) chemical absorption of H_2O, forming one layer of AlO_x, (d) the process is repeated to form AlO_x.

Two ALD systems were used in this work. A Vecco Savannah 200 is primarily used to deposit SiO_x, AlO_x, and HfO_x for studies related to 2D MoS_2, and an Anric thermal ALD is primarily used for the deposition of AlO_x for silicon surface passivation. The Savannah ALD is located at the David Wong Building (DWB) cleanroom, University of Oxford, and the Anric ALD is located at the Engineering and Technology Building (ETB), University of Oxford. Both systems were operated by the author. The precursors involved in the process and the related parameters are summarised in Table 2.2.1. In Savannah ALD, the precursor dose is controlled by the valve opening time. In Anric ALD, the valve opening time is fixed, while the precursor dose is controlled by the number of pulses. Exposure mode was used to deposit SiO_x in the Savannah ALD. The valve connecting the chamber to the vacuum pump is closed after the O_3 pulse to allow sufficient precursor absorption. An ozone generator with an O_2 flow of 0.5 SLM at 5 psi produces O_3 oxidant gas. Substrates for silicon surface passivation studies were RCA cleaned prior to ALD deposition. Further details of RCA cleaning are described in Appendix B. Test runs of 50 cycles of the corresponding film are deposited to fill the manifold with fresh precursors prior to depositions on the studied samples. For Anric ALD, a holder designed for double-side deposition is used, while for the Savannah system, samples are placed on the chamber plate directly for single-sided deposition.

Table 2.2.1 Deposition parameters for dielectric films deposited by ALD. BDEAS stands for bis(diethylamido)silane, TMA stands for trimethyl aluminium, and TDMAHf stands for tetrakis(dimethylamido)hafnium. No heating is required for TMA. Pulse time for Anric ALD is described as “3 × 0.6 s”, which refers to three pulses with valve opening time of 0.6 seconds for each pulse.

Parameters		Savannah			Anric
		SiO_x	AlO_x	HfO_x	AlO_x
Chamber Temperature (ºC)		150	150	150	150
Base Pressure (mTorr)			250		200
N_2 Flow (sccm)		20	20	20	
Precursor	Name	BDEAS	TMA	TDMAHf	TMA
	Precursor Temperature (ºC)	50	-	75	-
	Pulse Time (s)	0.10	0.015	0.15	3 × 0.6 s
	Purge Time (s)	5	8	20	11
Co-reactant	Precursor Name	O_3	H_2O	H_2O	H_2O
	Pulse Time (s)	0.075	0.015	0.015	2 × 0.6 s
	Exposure Time (s)	20	-	-	-
	Purge Time (s)	5	8	20	13

In studies involving 2D MoS_2, different dielectrics were deposited on the substrates using ALD. As reviewed in Chapter 1, Section 1.4.4, the dielectric/2D MoS_2 interface plays a crucial role in determining the overall device performance. For simplicity, substrates capped with SiO_x, AlO_x, and HfO_x are denoted as A, B, and C, respectively. For example, a Set 5 substrate with an additional 50 cycles of ALD-SiO_x on top is referred to as Set 5-A. Details of the processing are provided in the relevant sections.

2.2.2 Plasma Enhanced Chemical Vapour Deposition (PECVD)

PECVD is a widely adopted technique which enables the deposition of thin films at relatively low temperatures [138]. Plasma is applied to the gas precursors generally with a high-frequency electric field to provide the excess energy required for the reaction. In this work, an Oxford Instruments PlasmaLab 80+ system is used to deposit SiN_x using SiH_4 and NH_3 gases. The instrument is located at Begbroke Science Park, University of Oxford and operated by the author. Substrates for silicon surface passivation studies were RCA cleaned prior to ALD deposition. Further details of RCA cleaning are described in Appendix B. Samples are heated on the stage to 350 ºC and single-sided deposition was carried out at a pressure of 650 mTorr. The plasma power was 80 W, and silane gas mixture (95% N_2, 5% SiH_4) and ammonia gas (NH_3) of 400 and 40 sccm are admitted into the chamber. An additional N_2 of 580 sccm is used as carrier gas and flown throughout the process.

2.2.3 Metal Evaporation

Thermal evaporation was used to deposit metal contacts for electrical measurements in this work. High-purity (99.99%) Al is placed inside a tungsten boat as the source. Under high vacuum (~10^{-6} Torr), the boat is heated up by passing through a high current. The metal melts and evaporates onto the sample surface. The deposition rate is monitored using a quartz sensor, whose resonant frequency changes with the deposition of metal.

For C-V measurements, front contacts were deposited through a shadow mask with circular features of 1 mm diameter. Full area back contacts were formed after removing the back dielectric layers using a diamond scribe. A schematic diagram of the formed structure is shown in Figure 2.2.2. For FET devices, back contacts

were deposited prior to front contact formation to best preserve the transferred flakes. Front contacts were formed through shadow masks fabricated using TEM grids. Details of the mask fabrication process are included in Appendix B. A DTE-170 Desktop Thermal Evaporation coater from Vac Techniche Ltd is used with a source-to-sample distance of ~10 cm. The instrument is located at ETB, University of Oxford and operated by the author.

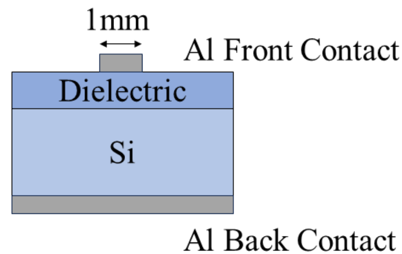


Figure 2.2.2 Schematic diagram of the formed MOS structure via thermal evaporation for C-V measurements.

2.3 Post-Deposition Processing

2.3.1 Annealing

Annealing at low (100-550 ºC) and high temperatures (800 ºC) was carried out. Hot plates were used for low temperature annealing in air. A clean silicon wafer was placed between the sample and the hot plate surface to minimise contamination. The temperature was monitored using a thermalcouple during annealing, and the measured temperatures were within 10 ºC of the set target. For temperatures above 400 ºC, a glass petri dish was used to cover the sample to reach the target temperature and improve temperature uniformity. For the high temperature annealing, a box furnace was used. Samples were loaded into the furnace at ~450 ºC, and an additional 25 minutes is required for the measured temperature to reach 800 ºC. After annealing, the box furnace is cooled down to 450 ºC before unloading the samples. The cooling process takes about 10 minutes.

2.3.2 Corona Discharge

Corona charge deposition is used to form temporary electric fields on sample surfaces. Corona charges are generated by applying a high voltage (>10 kV) through a sharp metal tip, which ionises the surrounding air. The sample is placed on a grounded metal plate. When a positive voltage is applied, positively charged ions such as $(H_2O)_nH^+$ is generated and deposit on the sample surface under the electric field. When a negative voltage is applied, negative ions such as CO_3^- is deposited [139].

For corona charge deposition at room temperature, the sample is placed directly underneath the metal tip on a grounded copper plate. The tip-to-plate distance is 20 cm. During charge deposition, voltage of ±30 kV is applied to the tip electrode. For corona charge deposition at elevated temperatures, an Al plate is used as the ground electrode. The Al plate is placed on a hot plate, and the tip-to-plate distance is 16 cm. During charge deposition, voltage of ±20 kV is applied to the tip electrode.

2.4 Characterisation Techniques

2.4.1 Ellipsometry

Ellipsometry is commonly used to determine the thickness and refractive index of nanolayer films. A schematic of the measurement is shown in Figure 2.4.1 [140]. A beam of linearly polarised light is incident on the sample, and the reflected light is collected by the detector. The change in the polarisation of the light is used to calculate film properties. The reflected light can be broken into two components, including p-polarisation R_p, which is parallel to the plane of incidence, and s-polarisation R_s, which is perpendicular to the plane of incidence. The R_p and R_s is then used to calculate the ellipsometric ratio:

$$\frac{R_p}{R_s} = \tan(\Psi)\, e^{i\Delta} \tag{2.4.1}$$

where Ψ is the relative amplitude, and Δ is the phase shift between R_p and R_s.

At each optical interface, the reflectance and transmittance of the light follows the Fresnel equation:

$$t_s = \frac{2n_1 \cdot \cos\theta_1}{n_1 \cdot \cos\theta_1 + n_2 \cdot \cos\theta_2}, t_p = \frac{2n_1 \cdot \cos\theta_1}{n_1 \cdot \cos\theta_2 + n_2 \cdot \cos\theta_1} \tag{2.4.2}$$

$$r_s = \frac{n_1 \cdot \cos\theta_1 - n_2 \cdot \cos\theta_2}{n_1 \cdot \cos\theta_1 + n_2 \cdot \cos\theta_2}, r_p = \frac{n_2 \cdot \cos\theta_1 - n_1 \cdot \cos\theta_2}{n_1 \cdot \cos\theta_2 + n_2 \cdot \cos\theta_1} \tag{2.4.3}$$

and the Snell's law:

$$n_1 \cdot \cos\theta_1 = n_2 \cdot \cos\theta_2 \tag{2.4.4}$$

where θ_1 and θ_2 are the incidence and refraction angles, and n_1 and n_2 are the refractive indices of the two materials. From Equation (2.4.1), (2.4.2), (2.4.3), and (2.4.4), R_p and R_s can be calculated [141]. In practice, film properties of each layer are put into a model and adjusted until the difference between the calculated and measured values of R_p and R_s is minimised.

In this work, a Film Sense FS-1 ellipsometer with a four-wavelength light source was used. The equipment is located at ETB, University of Oxford, operated by the author. For analysing the thickness of SiO_x, AlO_x, and HfO_x, a built-in model in the Film Sense software is used. This model uses the *N*, *C*, *S* definition of the ellipsometry parameters calculated from Ψ and Δ and minimise the difference between the calculated and measured data using the Marquardt-Levenberg algorithm [142]. The material optical properties of the materials are found in the literature [143]. A Cauchy model was used to analyse the thickness of SiN_x, which also allows the fitting of the refractive index [144].

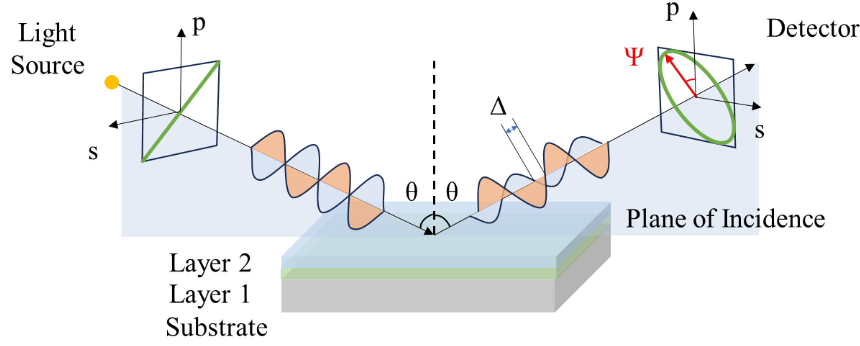


Figure 2.4.1 A schematic of an ellipsometry measurement. Reproduced from [140].

2.4.2 Photoconductance Decay

The effective lifetime (τ_{eff}) is defined as the average time that excess carriers persist before recombining. In this work, τ_{eff} is measured from photoconductance decay using a WCT-120 Sinton Lifetime Tester. The equipment is located at ETB, University of Oxford, operated by the author. Excess carriers are generated by shining light onto the samples, and its decay is monitored by the changes in the conductivity using an induction coil. The τ_{eff} can be calculated from:

$$\tau_{eff} = \frac{\Delta n(t)}{G(t) - \frac{d\Delta n(t)}{dt}} \tag{2.4.5}$$

where G is the generation rate, and Δn is the excess carrier density.

Depending on the length of the flash, the τ_{eff} can be measured in transient mode or Quasi Steady State (QSS) mode. For the transient mode, a short light pulse (100-200 μs) is shone upon the sample to generate excess carriers, and the changes in the excess carrier density are monitored after the light is turned off. This simplifies Equation (2.4.5) by assigning $G(t)$=0:

$$\tau_{eff} = \frac{-\Delta n(t)}{\frac{d\Delta n(t)}{dt}} \tag{2.4.6}$$

and τ_{eff} can be deduced from the changes in Δn over time. Transient mode has the advantage of not requiring a simultaneous measurement of the generation rate and is independent of the light optics. However, only samples with τ_{eff} longer than the light turn-off time (τ_{eff} >100 μs) are suitable for this mode.

QSS mode is used for samples with shorter τ_{eff}. A longer light pulse is used, and the generation and recombination are assumed to be in equilibrium at each moment in time. This simplifies Equation (2.4.5) by assigning $d\Delta n(t)/dt$=0:

$$\tau_{eff} = \frac{\Delta n(t)}{G(t)} \tag{2.4.7}$$

where $G(t)$ is determined by a separate measurement of the flash intensity using a light sensor. The optical constant of the samples needs to be known to convert the flash intensity to generation rate. Compared to the transient mode, the QSS mode is less prone to noise, and the measuring condition is closer to the working condition of solar cells under constant illumination [145], [146].

In this work, transient mode with an 1/64 s light pulse was used to measure all samples. The testing stage is at 25 ºC and the τ_{eff} values are quoted at $\Delta n=10^{15}$ cm^{-3}. The obtained Δn-dependent τ_{eff} can be fitted to analyse the different contributions of τ_{bulk} and $\tau_{surface}$, as discussed in Section 1.3. The MATLAB app used for the analysis is available in [147]. The surface recombination current density (J_{0s}) and effective surface recombination rate (S_{eff}) can be calculated following Kimmerle's formalism [11], [72].

2.4.3 Transparent Gate Electrode

To study the passivation quality of Si-dielectric interfaces, transparent electrodes were used to alter the surface carrier densities $n_{s/p}$. This leads to a change in the SRH surface recombination rate $U_{surface}$ according to Equation (1.3.1), and ultimately τ_{eff}. In this work, semi-transparent electrodes were used to apply voltages on both surfaces of the sample and allow simultaneous measurements of τ_{eff} on the Sinton Lifetime Tester [148]. All measured samples were symmetrically passivated. A schematic of the set-up is shown in Figure 2.4.2.

Undiluted poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS) was applied to both sides of the sample with a paint brush. Samples were then annealed at ~80 ºC for 2 minutes in air to remove excess water and improve film conductivity. One corner of the sample is scratched with a diamond pen to remove the dielectric layer. Indium gallium and silver dag was applied to the scratch region make a durable contact to the Si substrate. External voltages ($V_{applied}$) are applied between Si and both top and bottom surface of the sample using a Keysight B2901A unit. The surface voltages are monitored using two RS-14 multi-meters from RS Components. The surface bias (V_{surf}) refers to the average of the top and bottom measured voltages. The difference between the top and bottom measured voltages was kept under 15% of the $V_{applied}$ for $|V_{applied}|<15$ V.

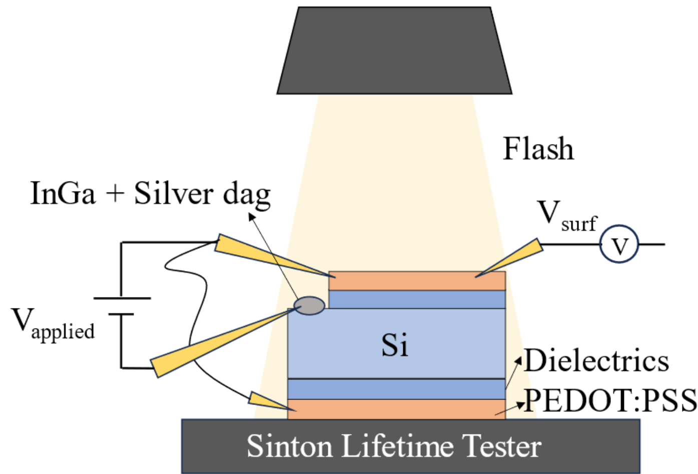


Figure 2.4.2 Schematics of the experiment set-up of measuring τ_{eff} with the application of different V_{surf} on both sample surfaces.

The obtained curves are fitted with a theoretical model using an extended Shockley-Read-Hall (SRH) formalism [149]. The key parameters include effective charge density (Q_{eff}), charge fluctuation (σ_q), interface states density (D_{it}) and carrier capture cross sections ($\sigma_{n/p}$). An arbitrary example of the parameters is shown in Figure 2.4.3. A single value of $D_{it,mg}$ and is $\sigma_{n/p,mg}$ is defined for D_{it} and $\sigma_{n/p}$ at mid-gap, respectively. Near the edges of the bandgap (ΔE<0.15 eV), a tail distribution identifies with a peak value of $D_{it,VB}$ ($D_{it,CB}$) at the valence band (conduction band) edge is defined. Such distribution is commonly referred to as band tails [150]. Different values of electron and hole capture cross sections are assigned to both band tails ($\sigma_{n/p,VB/CB}$). The interface defects are acceptor-like in the upper half of the band gap (E-E_t>0 eV) and are donor-like in the lower half of the bandgap (E-E_t<0 eV). This model is based on previous work in [149], [151], [152]. Carrier capture velocities at the band tails ($S_{n,VB}$ or $S_{p,CB}$) are calculated by averaging the values of $S_{n/p}$ at band tails. Carrier capture velocities at mid-gap (S_{n0} or S_{p0}) are calculated by $S_{n/p0} = D_{it,mg}\, \sigma_{n/p,mg}\, v_{th}$. The MATLAB app used for the analysis is available in [153].

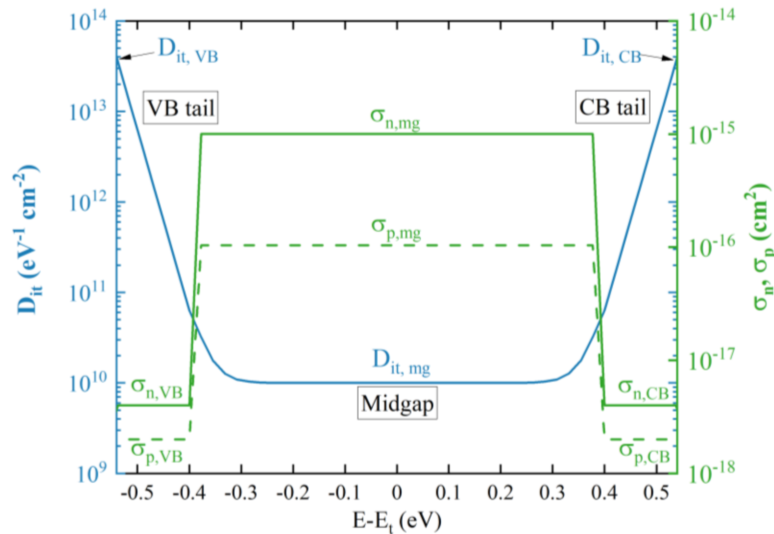


Figure 2.4.3 Interface parameters used to the model recombination activities in this work.

2.4.4 Capacitance-Voltage

Capacitance-voltage (C-V) measurements are used to study the Si-dielectric interface. A small AC signal is applied to the studied MOS structure to capture the capacitance, while a DC bias is swept through a range. The applied DC signal alters the surface carrier concentration and causes band-bending at the semiconductor surface and, thus, to the capacitance. The changes in band-bending and carrier distribution at different DC voltages in a passivation structure of AlO_x on p-Si is shown in Figure 2.4.4.

In accumulation, as shown in Figure 2.4.4 (a), the applied DC voltage increase the concentration of the majority carriers near the semiconductor interface. The MOS structure behaves like a parallel plate capacitor [154]:

$$C_{Acc} = C_{diel} = \frac{\varepsilon_0 \varepsilon_{diel} A}{t_{diel}} \tag{2.4.8}$$

where ε_0 is the vacuum permittivity, ε_{diel} is the relative permittivity of the dielectric, A is the capacitor area, and t_{diel} is the dielectric thickness. The capacitance at accumulation (C_{Acc}) equals to the dielectric capacitance (C_{diel}).

With the application of a positive DC signal, a space charge region (SCR) is formed near the semiconductor surface, which gives rise to a capacitance C_{SCR} in series with the C_{diel}:

$$\frac{1}{C_{Dep}} = \frac{1}{C_{diel}} + \frac{1}{C_{SCR}} = \frac{\varepsilon_0\, \varepsilon_{diel}\, A}{t_{diel}} + \frac{\varepsilon_0\, \varepsilon_{Si}\, A}{W_d} \tag{2.4.9}$$

$$W_d = \sqrt{\frac{4\, \varepsilon_0\, \varepsilon_{Si}\, \phi_F}{q\, N_d}} \tag{2.4.10}$$

where W_d is the width of the space charge region, ϕ_F is the Fermi energy of the semiconductor, and N_d is the dopant concentration.

The flat-band condition is defined when there is zero band-bending, meaning that there is no net charge in the SCR. The flat-band voltage (V_{FB}) is given by [155]:

$$V_{FB} = \frac{\Phi_m - \Phi_s}{q} - \frac{Q_{it} t_{diel}}{\varepsilon_{diel}} - \frac{Q_{eff}(t_{diel} - x_c)}{\varepsilon_{diel}} \tag{2.4.11}$$

where Φ_m-Φ_s is the work function difference between the metal and semiconductor, Q_{it} is the interface charge density, Q_{eff} is the effective charge density in the dielectric, which is located as a sheet of charges at location x_c in relative to the Si-dielectric interface.

At higher DC bias, minority carriers are mirrored into the SCR. This process is by diffusion of minority carriers from the bulk region or thermal generation of electron-hole pairs in the SCR [156]. Both of these processes happen over a period of time. As a result, the capacitance in inversion is frequency dependent. At low frequencies, carriers have sufficient time to response to the change of signal and form an inversion layer,

thus recovers the capacitance value. At high frequencies, the charges cannot respond fast enough to the signal, and the capacitance is kept at a low value.

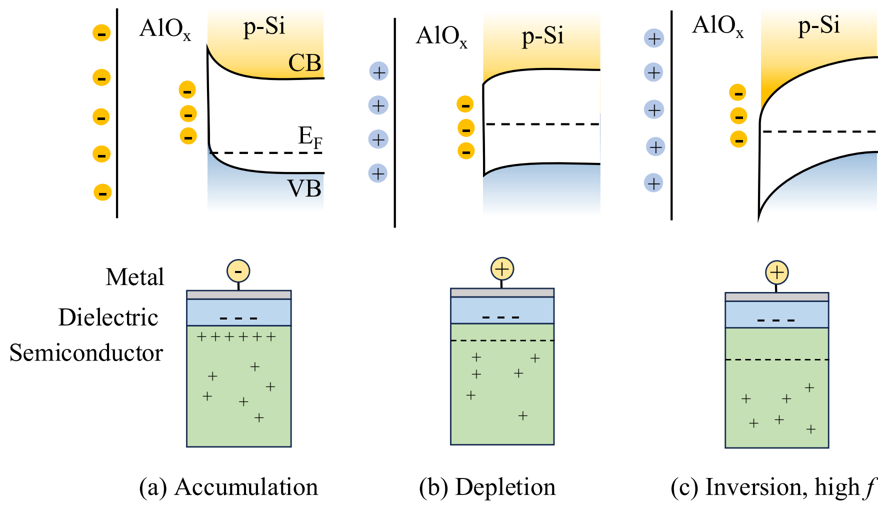


Figure 2.4.4 The changes in band-bending and carrier distribution in a passivation structure of AlO_x on p-Si under different DC bias: (a) accumulation, (b) flat band, and (c) inversion with high frequency (*f*) AC signal.

In an ideal MOS structure with no dielectric charges, the V_{FB} is close to 0 V. Shifts of the curve along the voltage axis indicate the magnitude and polarity of dielectric charges, which is also demonstrated by Equation (2.4.11). C-V plots with different Q_{eff} and D_{it} are shown in Figure 2.4.5. The curve left shifts with a decreased negative Q_{eff}. In practice, chargeable defects are also present at the semiconductor-dielectric interface. The charging and discharging of the defects are dependent on the applied DC bias, as shown in Figure 2.4.5 (a). This causes a left/right shift at each applied DC bias and, thus, a “smearing-out” feature in the curves.

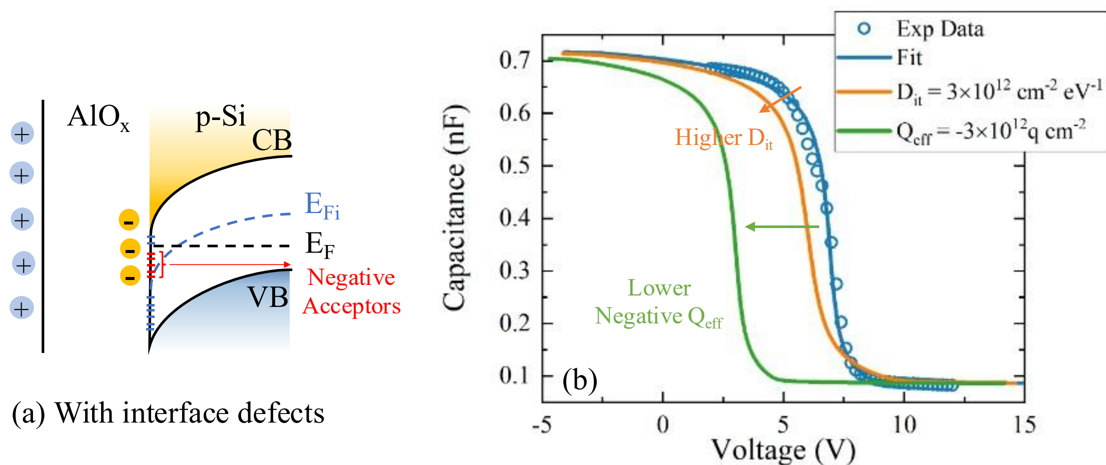


Figure 2.4.5 (a) Schematics of a MOS structure in inversion with charged interface defects, which causes a “smearing-out” feature in C-V curves. (b) Changes in C-V curves with different Q_{eff} and D_{it}.

In this work, the MOS structure is formed by depositing Al contacts on the dielectric surface, as described in Section 2.2.3. An Agilent E4980A precision LCR meter is used to obtain the C-V curves. The equipment is located at ETB, University of Oxford, operated by the author. The AC signal is set to 0.05 V, and the frequency

is set to 100 kHz to capture the high-frequency behaviour. At least 5 dots were measured on each sample, and each dot was only measured once. For detailed interface studies in Chapter 4 and 5, the obtained curves were fitted using Nicollian and Goetzenberg MOS theory [157]. Energy-dependent values of D_{it} and $\sigma_{n/p}$ were defined as described in Figure 2.4.3.

2.4.5 Kelvin Probe Measurements

Kelvin probe (KP) is a non-contact, non-destructive method to measure the work function difference between a conducting sample and the metal tip. Silicon samples were studied in this work. Schematics of the working principle are shown in Figure 2.4.6. When the metal tip and the sample are not in contact, the Fermi energies are not aligned due to their work function difference, as shown in Figure 2.4.6 (a). After contact, electrons flow from the sample to the metal tip, and a contact potential difference (CPD) equals to the work function difference (Φ_m-Φ_s) is created, as shown in Figure 2.4.6 (b). In KP, the metal tip oscillates up and down close to the sample surface, generating an AC current i_b. The CPD value can be determined by applying a backing potential V_b, at which i_b is nulled, as shown in Figure 2.4.6 (c). The applied V_b compensates the work function difference between the metal and the sample.

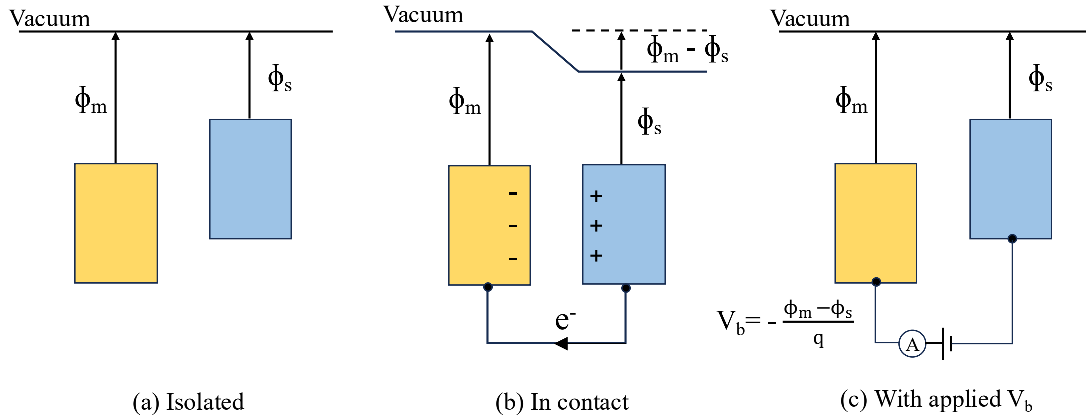


Figure 2.4.6 Energy diagrams of a metal and a Si sample, with different work functions, and $\Phi_m > \Phi_{Si}$ when (a) isolated, (b) electrically connected, and (c) electrically connected and with a backing potential applied to null the current flow.

In measuring a Si-dielectric system, the fixed charges in the dielectric causes band-bending near the Si surface. Additional potential shifts due to the dielectric charges must also be accounted for, and V_b is:

$$V_b = -CPD = -(\frac{\Phi_m - \Phi_s}{q} - \frac{Q_{eff}x_c}{\varepsilon_{diel}} - \phi_{scr}) \quad (2.4.12)$$

where Q_{eff} is the dielectric effective charge density located at x_c in relative to the Si-dielectric interface, ε_{diel} is the dielectric permittivity, and ϕ_{scr} is the semiconductor surface potential due to the space charge region [155]. Schematic diagrams of the potential changes due to dielectric charges is shown in Figure 2.4.7 (a). The determination of ϕ_{scr} requires a laborious iterative algorithm [152]. It has been demonstrated that a surface charge density larger than 10^{13} q cm^{-2} is required to produce a $|\phi_{scr}|$>0.25 V [155]. For the samples studied in this work, the potential change due to the space charge region is negligible.

Under illumination, electron-hole pairs are generated near the silicon surface, increasing the minority carrier density. This partially neutralises the charge imbalance near the interface, thereby reducing band-bending [158]. Changes in the band-bending under illumination is shown in Figure 2.4.7 (b). Surface photovoltage (SPV) is determined by the difference in CPD values under dark and illumination and can be written as $SPV=CPD_{illumination}-CPD_{dark}$. The SPV polarity contains information on the Si band-bending in equilibrium (in dark). For a Si sample passivated by negatively charged AlO_x, the band-bending upward, and decreases under illumination. This leads to a negative SPV value. Similarly, a positive SPV value indicate downward Si band-bending. In addition to the fixed dielectric charges, the magnitude of SPV is also dependent on the doping of Si, minority carrier lifetime, recombination activity, and illumination conditions [159], [160]. Only qualitative analysis is carried out in this work.

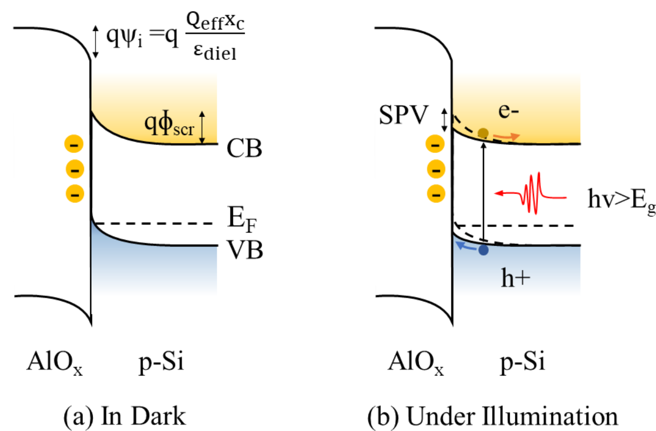


Figure 2.4.7 Schematic diagrams of an AlO_x-passivated p-type Si, demonstrating band-bending (a) in dark, and (b) under illumination, reproduced from [158].

A SKP5050 scanning Kelvin probe instrument from KP Technologies with 2 mm-diameter gold probe is used in this work. The equipment is located at ETB, University of Oxford, operated by the author. The instrument is kept in an enclosed box under dark conditions. An illumination of 10 mW cm^{-2} was used for light conditions in SPV measurements. To obtain spatial information, a motor was used to move the sample stage with a step size of 2 mm. At each location, the CPD value is averaged over 50 measurements.

2.4.6 Raman and Photoluminescence Spectroscopy

Raman and photoluminescence (PL) spectroscopy were used to characterise 2D MoS_2 in this work. The unique signatures of 2D MoS_2 in Raman and PL spectra are discussed in Chapter 1, Section 1.4.1. Both methods use monochromatic excitation sources. In Raman spectroscopy, the inelastically scattered light is analysed, providing information on the vibrational modes (phonons) of the material [161]. Such scattered light typically exhibits small energy shifts to the excitation wavelength and requires a high grove-density grating to achieve high spectral resolution [162]. Meanwhile, PL analyses the absorbed and subsequently re-emitted light, which corresponds to electronic transitions in the ~eV range [80]. A lower groove-density grating is generally used to disperse a broader range of the emitted light.

Raman and PL spectroscopy measurements were performed at room temperature, in air, using a Horiba LABRAM Aramis Raman Microscope with a 532 nm excitation laser. The equipment is located at Begbroke Science Park, available through Oxford Materials Characterisation Service (OMCS), operated by the author. A grating of 1800 grooves/mm was used to obtain Raman spectra, while a grating of 600 grooves/mm was used to obtain PL spectra. The spectrums are averaged over five measurements with 3 seconds of acquisition time each. The obtained Raman spectra were fitted to Lorentz distribution to extract the peak positions [163]. The obtained PL spectra were fitted to a pseudo-Voigt function [164]. The peak areas are calculated to estimate the electron density (n_{el}) in 2D MoS_2 according to mass action model based on the dynamic equilibrium between A^0, A^- and free electrons [81]:

$$n_{el} = \frac{I_{A^-}}{I_{A^0}} \times \frac{\gamma_{A^0}}{\gamma_{A^-}} \times \left[\left(\frac{4m_{A^0}m_e}{\pi\hbar^2 m_{A^-}}\right) k_B\, T\, exp(-\frac{E_b}{k_B T})\right] \tag{2.4.13}$$

where I_{A-} and I_{A0} are the area under peak A^- and A^0, γ_{A-} and γ_{A0} are the relative decay rates of A^- and A^0 excitons, and m_{A-} (1.15 m_0), m_{A0} (0.8 m_0) and m_e (0.35 m_0) are the effective masses of A^-, A^0 and electrons respectively, where m_0 is the mass of free electrons. In this work, γ_{A-}/γ_{A0} is ~0.15 [82], and the trion binding energy E_b is 20 meV [165].

2.4.7 Charge Transport Measurements in Field Effect Transistors

In this work, transport measurements were carried out under controlled atmospheric, light and temperature conditions within an enclosed box. A photo and a schematic of the measurement setup is shown in Figure 2.4.8. High purity argon gas is introduced into the box through a gas tube from the top to maintain an inert environment.

To ensure darkness during measurements, an acrylic board covered with Al foil is used as an opaque cover. The box is positioned beneath a stereo microscope, which is used to align the probes to the sample. The built-in halogen lamp can be used as a controlled light source. An opening in the Al foil, located directly above the sample stage, allows for probe alignment checks without disrupting the controlled gas environment. During measurements, this opening is covered with a black foam to maintain dark conditions.

A heating stage equipped with a proportional-integral-derivative (PID) controller was used to regulate the sample temperature. The PID parameters were set via a LabVIEW program, and a TSX1820P model from Thandar was used as the power source. Tungsten probes were used to electrically connect the source, drain and back-gate contacts of the device to voltage sources. The drain-source voltage is applied using a Keithley 2401, while the gate-source voltage is applied using a Keithley 487.

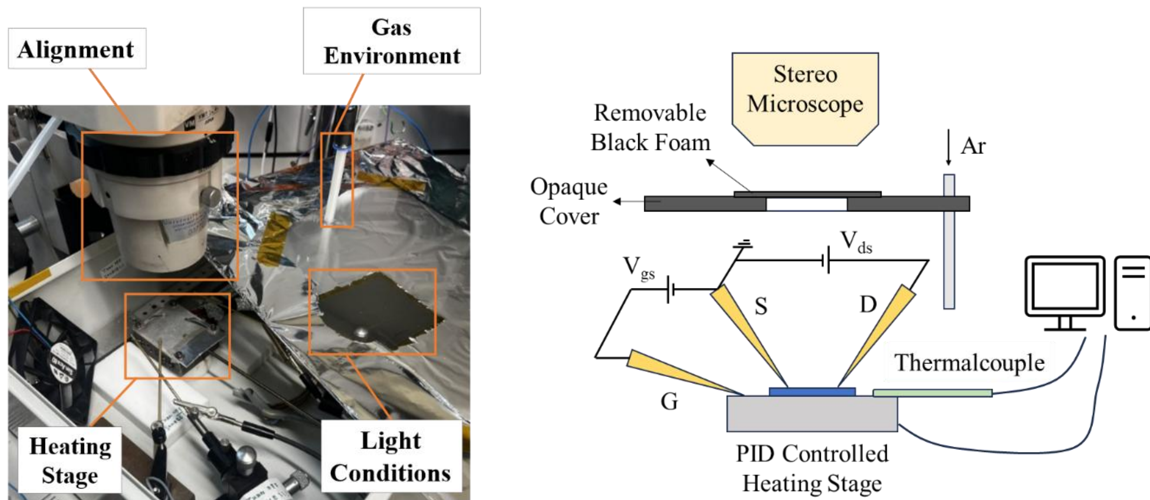


Figure 2.4.8 Measurement setup with controlled atmosphere, light conditions and temperatures for 2D MoS_2-based FETs.

The obtained transfer curves were analysed using MATLAB to extract key parameters including threshold voltage (V_{th}) and field-effect mobility (μ_{FE}). The critical step involves defining and fitting the linear region of the curves. The forward and backward curves were analysed separately.

The linear region is identified automatically by defining a window that moves along the x-axis of the obtained curve, fitting all the data points within the window to a linear function. The linear region is determined where the minimum R-squared value is achieved. V_{th} corresponds to the intersection point of the fitted line with the x-axis, while μ_{FE} is calculated from the slope of the fit ($\partial I_{ds}/\partial V_{gs}$), as given by Equation (1.4.4). To ensure optimal fitting, the window size is set to 20-30 V for the forward curve, and 15-20 V for the backward curve. A schematic of the fitting process is shown in Figure 2.4.9.

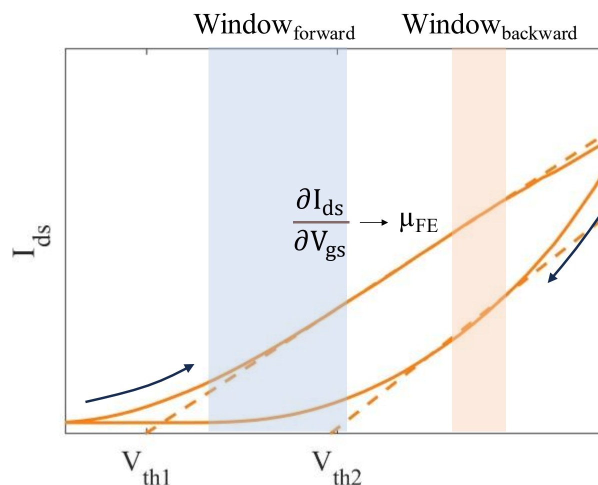


Figure 2.4.9 Schematics of the fitting process of transfer curves to extract V_{th} and μ_{FE}.

2.4.8 Scanning Transmission Electron Microscopy

In this work, scanning transmission electron microscopy (STEM) was used to obtain a high-resolution image of the interfaces between Si and the deposited dielectric layers. To protect the surface during lamella

preparation, ~100 nm of Al was thermally evaporated onto the sample. A STEM sample was then prepared using a Zeiss Nvision 40 FIB-SEM, lifted out onto a Cu grid, and thinned to ~50 nm using a 30 kV Ga^+ beam with current gradually decreased from 700 pA to 80 pA.

STEM images were then obtained using a Jeol ARM 200F operating at 80 kV with a Gatan image filter Quantum 965 ER. Elemental distribution and bonding configuration near the interface were analysed using electron energy loss spectroscopy (EELS). EELS measurements were conducted with a convergence semi-angle of 30 mrad and a collection semi-angle of 38 mrad and a probe size of ~1 Å. The zero-loss peak full width at half maximum (FWHM) was 0.8 eV. The sample was placed on a cryo sample holder to maintain a temperature of -180 °C throughout the measurement to minimise damage to the interfaces [50]. The EELS spectra were curve fitted using Digital Micrograph to map the atomic distribution.

Chapter 3
Negatively Charged Dielectrics

3.1 Introduction to Dielectric Charging

Charged dielectrics, also termed electrets, are materials with a quasi-permanent charge concentration on the surface or in the bulk and behave like an electrostatic equivalent of a magnet [166]. Traditional electrets were based on thick films of organic polymers or silica, and used in simple devices such as microphones and actuators [167], [168]. More recently, nanometre-thick electrets found application in air filtration [169], energy harvesting [170] and solar cell passivation [155].

The first practical electret was demonstrated by Mototaro Eguchi in 1919 by subjecting a wax/resin-treated material to ~130 ºC and voltage bias, producing an internal polarisation that persisted for years [171]. This process is referred to as the thermo-electrical method, which aligns the randomly oriented dipoles to an external electric field under an elevated temperature. After the electric field is removed, the polarisation gradually returns to a quasi-steady level and stays for a prolonged period.

Charged ions in dielectrics have also been reported to induce a quasi-permanent electric field. Initially, ions such as sodium (Na^+) and potassium (K^+) were found in SiO_2 and cause device instability in metal-oxide-semiconductor field-effect transistors (MOSFETs) [172], [173]. Studies suggest that under temperature-bias stress, these ions migrate towards the Si/SiO_2 interface, where they get trapped, resulting in a long-term storage [174]. This issue was later resolved by eliminating all contamination sources [175]. Recently, a field-assisted ion migration method was proposed, where ionic species such as K^+, Rb^+ and Cs^+ are intentionally deposited and driven into SiO_2 [175], [176]. A charge density higher than 5×10^{12} q cm^{-2} has been demonstrated, which was found to effectively enhance the field-effect passivation of Si surface [177]. So far, studies on charged dielectrics utilising mobile ions have predominately focused on positive polarity, with limited reports on negative polarity. This gap presents a potential area for future exploration, and in the following sections, alternative methods for developing negatively charged dielectrics is discussed.

Corona charging is another widely adopted method for charging dielectrics. As described in Chapter 2, Section 2.3.2, this technique involves applying a high voltage (~kV) to a needle electrode, ionising surrounding air molecules. These ions are readily absorbed near the dielectric surface, where they transfer their charges to the dielectric before re-entering the air. One of the main advantages of corona charging is its relatively simple experimental setup. Achieving uniform charge distribution and ensuring long-term stability is challenging [178], however effective solutions have been proposed. For example, charge uniformity can be enhanced by

adjusting the tip-to-sample distance [179] or employing multiple charging electrodes [180]. Meanwhile, increasing the temperature during corona charging [166] or applying post-discharge rapid thermal annealing (RTA) [181] facilitates charge penetration deeper into the dielectric bulk, improving the long-term stability of the electret. It has also been reported that charges tend to reside at interfaces, where the density of defects is particularly high [182]. A corona charged SiO_2 nanoarray has been reported to exhibit a much slower charge decay in the nanowire region than the planar region, with the former region has a higher defect density than the latter [174].

The development of negatively charged dielectrics is the primary focus of this chapter. These materials have promising applications in passivating p-type Si, where the negative charge repel electrons from the surface, thereby reducing surface recombination [183]. Additionally, they are useful for inducing p-type doping in 2D semiconductors, which is necessary for the formation of junctions that allows precise control of electrical properties in transistors. As discussed in Chapter 1, the formation of negative charge at the SiO_x/AlO_x interface requires both activation annealing, which creates deep acceptor states responsible for trapping charges [51], and proximity to the Si substrate, which serves as an electron source [57]. The charging mechanism of the SiO_x/AlO_x interface is first investigated. Negatively charged dielectrics as a means to induce doping in 2D semiconductors is then developed in this Chapter. Further incorporation of the negatively charged dielectrics into silicon passivation is presented in Chapter 4 and 5.

3.2 Charging of Defects at SiO_x/AlO_x Interface

3.2.1 Charge Embedding in Dielectrics near Si

This section aims to study the charging of defects at the SiO_x/AlO_x interface near a silicon substrate [40]. Dielectric stacks were deposited on Set 1 substrates using the Savannah ALD. The stacks comprise 20 cycles of SiO_x, either 0 or 10 cycles of AlO_x, and an additional 100 cycles of SiO_x to form a SiO_x/AlO_x interface. The deposition rates of SiO_x and AlO_x were determined by separately depositing 100-cycle films on Si substrates (Set 1) and measuring the film thicknesses using an ellipsometry, yielding growth rates of ~0.78 and 1.0 Å/cycle, respectively.

Annealing (in air at 450 °C) was performed to activate the negative charge, which has been proposed in the literature to arise from electron injection from the Si substrate [184]. The resulting changes in charge density were monitored using Kelvin Probe (KP). Changes in contact potential difference (CPD) with increasing annealing time for both sample structures are shown in Figure 3.2.1. For reference, the work function difference between the gold probe and the Si substrate was measured on a bare Set 1 substrate, as indicated by the dotted line.

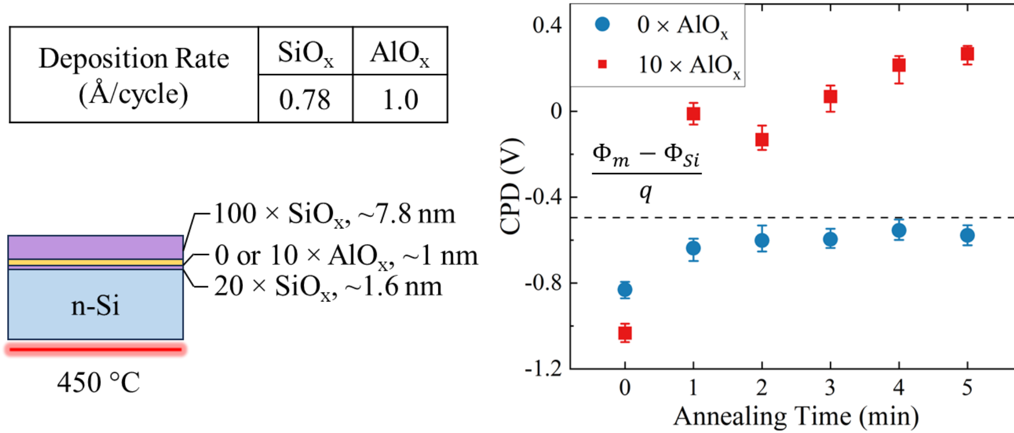


Figure 3.2.1 Contact potential difference (CPD) values of dielectric stacks with and without 10 cycles of AlO_x with different annealing time at 400 °C. The measured deposition rate for SiO_x and AlO_x and a schematic diagram of the sample structure are also included. The error bar represents 10-90% of the values obtained in a 6×6 mm map with 16 points.

The difference between the measured CPD values on samples with 0 or 10 cycles of AlO_x and those of bare silicon can be attributed to the presence of fixed charges in the dielectric layers. According to Equation (2.4.12), a higher CPD value indicates a net negative charge density, whereas a lower CPD value suggests a net positive charge density. Following the initial 1-minute annealing, an increase in CPD values from approximately -1 to 0 V was observed in the sample containing a thin AlO_x layer. After 5 minutes of annealing, the CPD value further increased to ~0.3 V, indicating the formation of negative charges. In contrast, the sample without a thin AlO_x layer exhibited CPD values lower than the probe-Si work function difference, both before and after annealing. This suggests the absence of negative charges and the presence of a small positive charge density, likely located near the Si/SiO_x interface in agreement with other reports in the literature [25].

The negative charge density induced by the thin AlO_x layer can be quantified by subtracting the contribution of the positive charges at the Si/SiO_x interface: $Q_{neg}\ x_c/\varepsilon_{SiO2}$= $CPD_{10\times AlOx,5min}$-$CPD_{0\times AlOx,5min}$, according to Equation (2.4.12). Assuming that the negative charges are positioned at the center of the AlO_x layer, x_c is estimated to be 2.1 nm, based on the measured deposition rate. The calculated negative charge density (Q_{neg}) is ~6.9 × 10^{12} q cm^{-2}, which is comparable to the reported value of ~ 6× 10^{12} q cm^{-2} for an ~1 nm AlO_x deposited on a chemically formed SiO_x layer [18].

These results demonstrate that the presence of an AlO_x and an activation annealing step (450 °C) are necessary for the formation of negative charges. A high negative charge density of ~6.9 × 10^{12} q cm^{-2} was achieved with only 10 cycles of AlO_x sandwiched between two SiO_x layers, highlighting the critical role of the SiO_x/AlO_x interface in negative charge formation. This high charge density, produced by merely ~1 nm of AlO_x, can provide effective field-effect passivation for the Si surface [177], and its underlying mechanisms is further discussed in Chapter 4 and 5.

3.2.2 Charge Embedding using Corona Discharge

This section further investigates the necessity of an external electron source in enabling charging of the SiO_x/AlO_x interface, as proposed in [42]. A 7 nm thermal SiO_2 layer between the Si substrate and the SiO_x/AlO_x interface has been reported to effectively suppress the negative charge density, from ~5×10^{12} q cm^{-2} to less than 0.5×10^{12} q cm^{-2}. To verify this observation, a $SiO_x/AlO_x/SiO_x$ structure was deposited on a Si substrate with a 300 nm thick thermal SiO_2 (Set 5) using a Savannah ALD reactor, with 20 cycles of SiO_x or AlO_x deposited for each layer. A schematic of the sample structure is shown in Figure 3.2.2 (a).

After ALD deposition, the sample was annealed at 450 °C for 5 minutes. The changes in the charge density before and after annealing were measured using KP and plotted in Figure 3.2.2 (b). It is noted that CPD values depend on both the density of charge and the distance between the charge and the Si surface, as described by Equation (2.4.12). As the negative charge is predicted to reside near the SiO_x/AlO_x interface, a negative charge density of ~10^{12} q cm^{-2} would give rise to a CPD value larger than 14 V, which is absent in my observation. Therefore, it is concluded that the SiO_x/AlO_x interface is not charged after annealing.

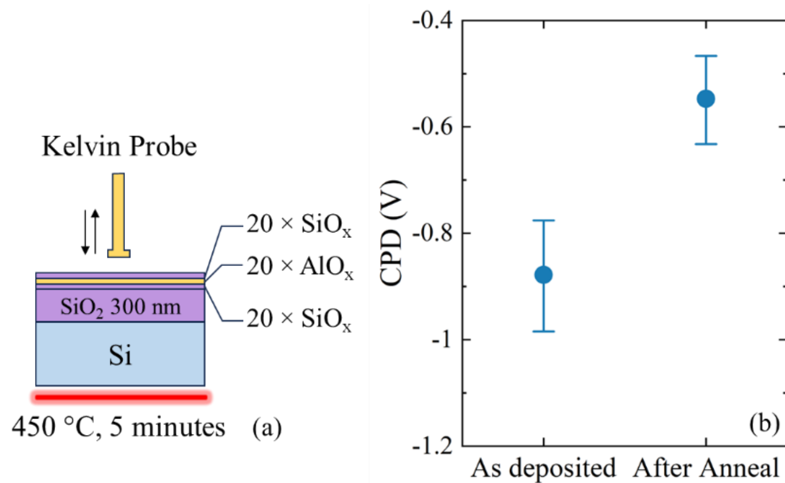


Figure 3.2.2 (a) Schematic of the sample structure. (b) CPD values before and after annealing at 450 °C for 5 minutes. The error bar represents 10-90% of the values obtained in a 6×6 mm map with 16 points.

To further verify the necessity of an electron source, a negative corona discharge was used to charge the SiO_x/AlO_x interface. Dielectric layers consisting of two 20-cycle SiO_x layers sandwiching either 0 or 20 cycles of AlO_x were deposited on Si substrates with a 300 nm SiO_2 (Set 5). The samples were annealed at 450 °C for 5 minutes to activate the formation of acceptor states at the SiO_x/AlO_x interface [184]. Negative corona charge was deposited for 30 seconds at room temperature, followed by annealing at 450 °C. The first annealing after charge deposition was conducted to provide sufficient energy for electrons to tunnel through the capping top SiO_x layer [185], while the subsequent annealing tests surface charge stability. The process consisting of one deposition of corona charge at room temperature followed by annealing is referred to as corona-anneal. The change in CPD values with annealing time is plotted in Figure 3.2.3. For comparison, the corona-anneal process was also performed on a bare substrate with a 300 nm SiO_2, and the results are included in the plot.

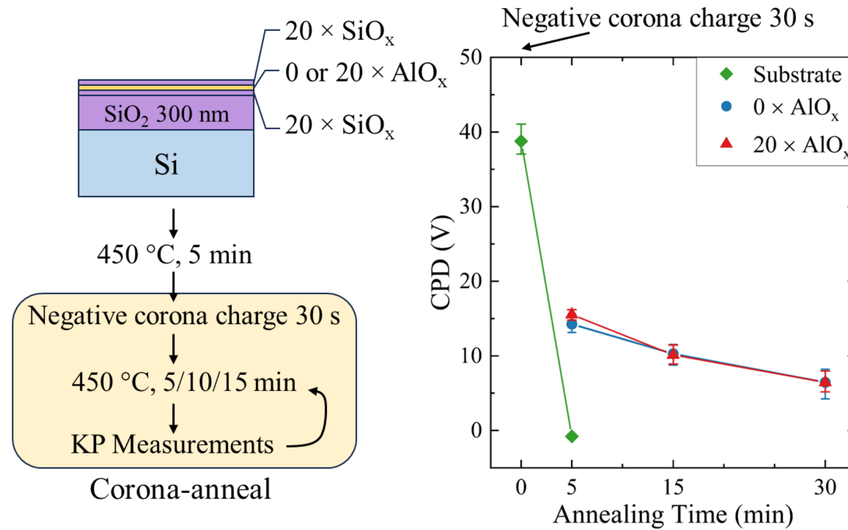


Figure 3.2.3 CPD values with increasing annealing time after depositing negative corona charge at room temperature. The error bar represents 10-90% of the values obtained in a 6×6 mm map with 16 points.

After the first 5-minute annealing, surface charge on the bare substrate was found to dissipate quickly under 450 °C, as indicated by the ~0 V CPD value measured. In contrast, samples with ALD-deposited layers, both with and without an AlO_x layer, exhibited CPD values well above 0 V, despite prolonged heating. This suggests the presence of chargeable acceptors states in the deposited ALD layers, beyond just the SiO_x/AlO_x interface. These defects are most likely to reside at the SiO_2/ALD-SiO_x interface or within the ALD-SiO_x layers. Previous reports have identified carbon impurities or oxygen vacancies to be present in ALD-SiO_x, which could be responsible for the high charge stability observed [186].

To better understand the charging behaviour of the SiO_x/AlO_x interface, as-deposited samples were annealed at 800 °C for 30 minutes. This high-temperature annealing has been reported to effectively remove defects at the Si/ALD-SiO_x interface, reducing the interface state density (D_{it}) by an order of magnitude [187]. Further details on the effectiveness of defect removal as a function of annealing time are provided in Appendix C. Positive or negative corona charge was deposited on the sample at room temperature, followed by annealing at 450 °C. The change in CPD values with increasing annealing time is shown in Figure 3.2.4.

For the sample without an AlO_x layer and deposited with negative corona charge, CPD values of ~0 V were observed after 5 seconds of annealing, suggesting the removal of chargeable defects from the SiO_2/ALD-SiO_x interface and/or in the ALD-SiO_x layers. On the other hand, samples with an AlO_x layer demonstrated high charge stability, as indicated by the ~10 V CPD values after 60 seconds of annealing at 450 °C.

For samples deposited with positive corona charge, CPD values decreased to ~0 V after 5 seconds of annealing, regardless of the presence of an AlO_x layer. This confirms the presence of acceptor states at the SiO_x/AlO_x interface, which can only be charged when an electron source is within a few nanometres from the interface. Negative corona charge has been identified as a suitable electron source as an alternative to Si.

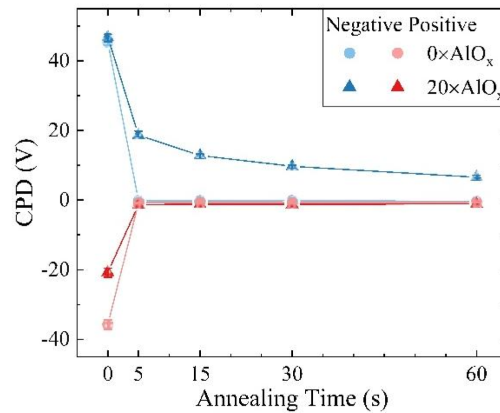


Figure 3.2.4 CPD values with increasing annealing time after deposition of positive or negative corona charge. All samples were annealed at 800 °C for 30 minutes prior to charge deposition. The error bar represents 10-90% of the values obtained in a 6×6 mm map with 16 points.

3.3 Design of Dielectric Capping Layer for Charge Retention

Field-effect doping of 2D semiconductors using charged dielectrics is a novel strategy proposed in this work. This strategy is similar to the working principle of field-effect transistors (FETs), where an external electric field alters the carrier density in the 2D semiconductor, and consequently its Fermi level. The electric field is generated by the charged defects embedded in the dielectric. The proposed dielectric stack consists of three components: an insulation layer, a charged layer, and a capping layer. A schematic illustrating the structure of the charged dielectric for field-effect doping of 2D semiconductors is shown in Figure 3.3.1.

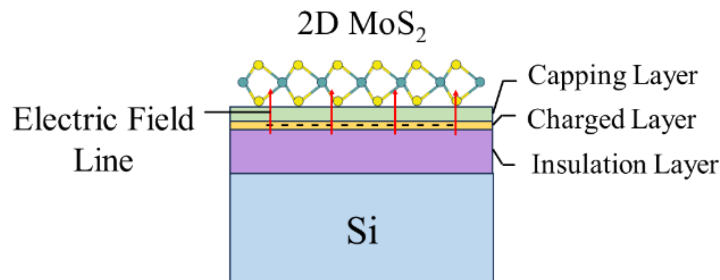


Figure 3.3.1 Schematic of a negatively charged dielectric stack on a Si substrate with 2D MoS_2 transferred onto the surface, demonstrating field-effect doping.

The three layers in the stack each serve distinct functions. The charged layer is designed to incorporate a high density of defects, which are then charged. This layer generates an electric field intended to modulate the carrier density of 2D semiconductor. The fabrication and charging processes of the charged layer are investigated in Section 3.4.

The insulation layer is the dielectric positioned between the charged layer and the Si substrate. A sufficiently thick layer is necessary to ensure that the Si substrate remains far from the charged layer, minimising its effects of shielding the electric field generated by the charged layer, as dictated by Gauss's Law. Additionally, in a functional 2D semiconductor-based FET, the Si substrate serves as the back gate, while the

insulation layer functions as the gate dielectric. Therefore, a high-quality dielectric is essential to minimise gate-source leakage. In this work, a 300 nm thick thermally grown SiO_2 is used as the insulation layer.

This section focuses on the design of the capping layer, which is positioned between the charged layer and the 2D semiconductor. Its primary function is to minimise charge degradation by preventing charge leakage due to air-absorbed H_2O molecules [188] and undesired charge transfer with the 2D semiconductor [112]. As a result, high-quality, thick films are preferred. However, to maximise the electric field near the 2D semiconductor, the capping layer must remain thin. The capping layer also needs to allow charge injection from an external source, creating conflicting design requirements. To address this challenge, a temperature-assisted charging strategy is adopted. The charge injection process occurs at an elevated temperature, providing sufficient energy for the external charges to overcome the barrier created by the capping layer. Once embedded, these charges remain stable at lower or room temperature. Finally, interactions between the capping layer and the 2D semiconductor, including dielectric screening and charge transfer [108], must also be considered to determine its compatibility with high-performance devices, which is discussed in Chapter 7.

In this section, the design of capping layer is investigated for charged layers based on defects at the SiO_x/AlO_x interface. ALD-deposited dielectrics, including SiO_x, AlO_x and HfO_x, are identified as potential capping layers due to their precise thickness control and highly insulating nature. The following experiment aims to determine the optimal thickness for SiO_x and HfO_x, which enables charge injection at elevated temperatures while preventing charge transfer between the charged layer and the 2D semiconductor at lower temperatures. A schematic demonstrating this requirement is shown in Figure 3.3.2 (a). To investigate the dielectric charge transfer dynamics, the device structure is flipped, and silicon is used as the active semiconductor, which can source electrons to charge SiO_x/AlO_x interface defects at high temperatures. A schematic demonstrating the experiment design is shown in Figure 3.3.2 (b), which avoids any issues arising with delicate 2D semiconductor transfer.

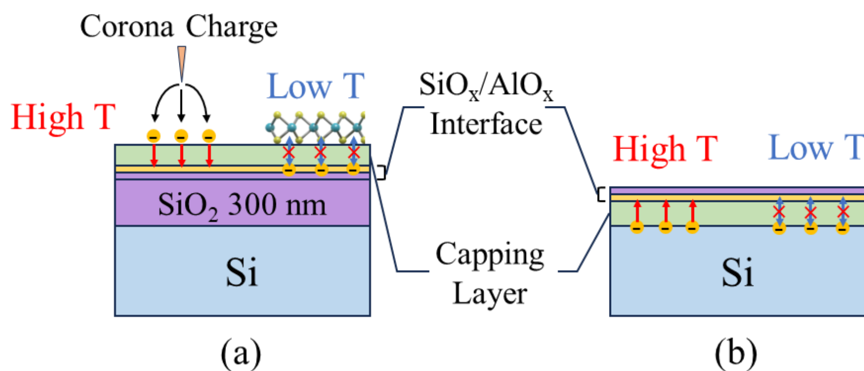


Figure 3.3.2 Schematics demonstrating (a) requirements for optimising the capping layer thickness, and (b) Si as a substitute for both negative corona charge and 2D MoS_2 for the optimisation process.

3.3.1 SiO_x

A 500-cycle ALD-SiO_x film was deposited on a 1×7 cm Si substrate (Set 1) using the Savannah ALD to simulate the capping layer. The sample was then annealed at 800 °C for 30 minutes to improve film quality, as described in Section 3.2.2. Next, the sample was vertically immersed in a 5% HF solution and slowly pulled out by 1 cm every 45 seconds, resulting in a SiO_x layer with a thickness gradient. The film thickness was measured using an ellipsometer every 5 mm along the etching direction and plotted in Figure 3.3.3 (a). A linear fit was applied to the measured SiO_x thickness data to correlate it with sample location. Following this, 20 cycles of AlO_x and SiO_x were deposited onto the sample using the Savannah ALD. To investigate the charging behaviour at the SiO_x/AlO_x interface, the sample was subsequently annealed from 150 to 450 °C for 10 minutes at each step. A KP scan was performed to monitor the change in charge density after each annealing with a 1×55 profile, with a step size of 1.02 mm, and 50 data points were collected at each location. CPD values were measured both in dark and under illumination. The obtained surface photovoltage ($SPV=CPD_{illumination}-CPD_{dark}$) profiles after annealing under different temperatures is shown in Figure 3.3.3 (b) as a function of the SiO_x thickness. Schematics of the etching process and the formed sample structure are also included.

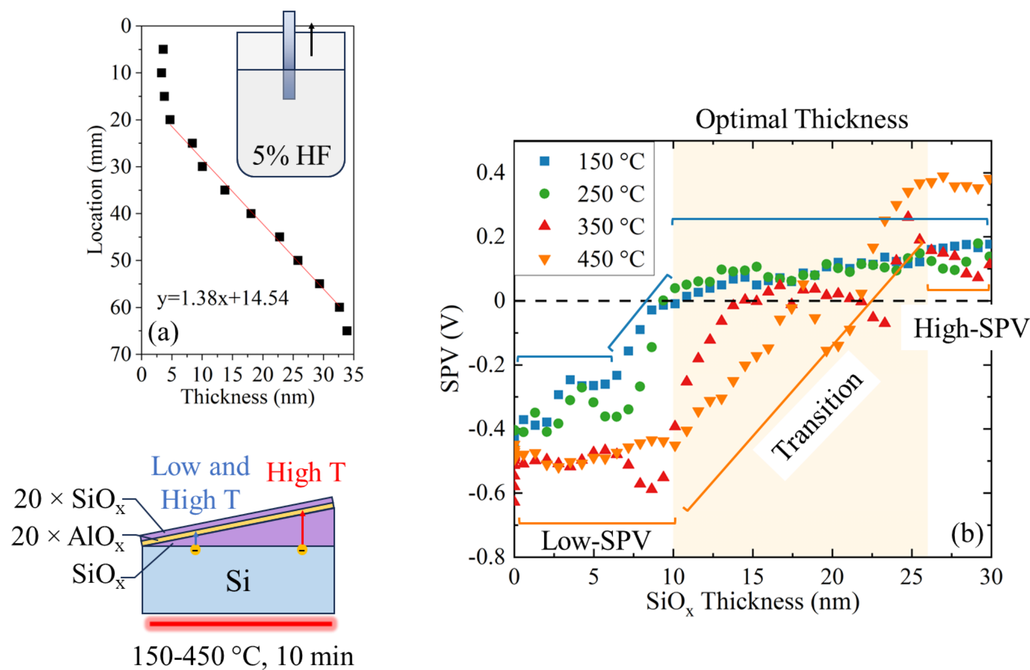


Figure 3.3.3 (a) measured SiO_x thickness along the etching direction, and (b) SPV profile measured as a function of SiO_x thickness after annealing at 150-450 °C for 10 minutes at each temperature. The blue and orange brackets mark the low-SPV, transition and high-SPV regions of the SPV profiles obtained after annealing at 150 and 450 °C, respectively. Each point represents the average of 50 measurements at a single location.

The changes in SPV values as a function of SiO_x thickness after annealing under different temperatures can be divided into three regions: (1) low-SPV, (2) transition, and (3) high-SPV. The corresponding regions for SPV profiles measured after annealing at 150 and 450 °C are marked by blue and orange brackets respectively in Figure 3.3.3. The observed changes in SPV with increasing SiO_x thickness are attributed to the reduction in electron injection from the Si substrate to the SiO_x/AlO_x interface.

In the low-SPV region, SPV values plateau at a negative value. More negative SPV values were obtained after annealing at higher temperatures. Within this region, energy provided by the annealing process is sufficient for electrons to tunnel through the SiO_x layer and be captured at the SiO_x/AlO_x interface. It is proposed that the negative charge density is primarily limited by the defect density at this interface. This hypothesis is supported by previous reports, where Al atoms are found to diffuse into the SiO_x layer during an activation annealing (350-450 °C), a process closely related to the formation of negative charge [50], [189]. At higher temperatures, increased thermal energy facilitates the intermixing of AlO_x and SiO_x layers, leading to an increased defect density, and subsequently higher negative charge density.

In the transition region, SPV reduces with increasing SiO_x thickness, indicating decreases in net negative charge densities. This reduction is attributed to the reduced electron injection efficiency, which refers to the likelihood of electrons successfully injecting from Si to the acceptor states at the SiO_x/AlO_x interface. As a result, the negative charge density is limited by the annealing temperature, leading to a delayed start of the transition region with higher annealing temperatures.

In the high-SPV region, SPV values plateau at a positive value. The net charge density becomes positive and remains relatively constant with further increases in SiO_x thickness. Positive charge is likely to reside near the Si/SiO_x interface [14], [19], [21], while the negative charge density near the SiO_x/AlO_x interface is minimal due to suppressed electron injection. The onset of the high-SPV region is also found to delay with increased annealing temperatures.

For capping layer design, the optimal SiO_x thickness falls in the overlapped portion of the high-SPV region in the SPV profile measured after a 150 °C anneal, and the low-SPV and transition regions in the SPV profile measured after a 450 °C anneal. The optimal thickness range, shaded in Figure 3.3.3, is found to be ~10-26 nm. The capping SiO_x layer with this optimal thickness allows negative charge injection at 450 °C while preventing charge transfer at temperatures lower than 150 °C.

3.3.2 HfO_x

To investigate the potential of HfO_x as a capping layer, a 500-cycle HfO_x film was similarly deposited on a 1×7 cm^2 Si substrate (Set 1) using the Savannah ALD. The same etching process described in the previous section was applied to create a thickness gradient for the HfO_x layer. Film thickness was measured using an ellipsometer and shown in Figure 3.3.4 (a). The thickness profile was linearly fitted to correlate the measured CPD values to layer thickness. Subsequently, 20 cycles of AlO_x and SiO_x were deposited using Savannah ALD to form a SiO_x/AlO_x interface. The sample was then annealed at multiple temperatures between 150 and 450 °C, with each annealing step lasting 10 minutes. After each annealing step, a SPV profile was obtained using the same settings as in the previous section. The resulting SPV profile as a function of HfO_x thickness is presented in Figure 3.3.4 (b). Additionally, the CPD profiles measured in the dark are shown in Figure 3.3.4 (c).

For SPV profiles obtained after annealing at different temperatures, similar trend was observed with increasing HfO_x thickness. The transition region and the high-SPV regions are consistently identified where

the HfO_x thickness is below or above ~5 nm, respectively. Meanwhile, the low-SPV region is absent in all SPV profiles. The corresponding regions are indicated by the black brackets in Figure 3.3.4 (a). This suggests a reduction in electron injection efficiency, and subsequently a reduced negative charge density at the SiO_x/AlO_x interface as the HfO_x thickness increases up to ~5 nm. Beyond this thickness, electron injection from Si to the SiO_x/AlO_x interface is effectively suppressed. This is further supported by the decrease in CPD_{dark} values and the plateaued feature with HfO_x thickness above ~5 nm, as shown in Figure 3.3.4 (b).

It was also observed that the absolute values of SPV and CPD_{dark} differ depending on the annealing temperature. Positive and negative SPV values were obtained after annealing at low temperatures (150 and 250 °C) and high temperatures (350 and 450 °C), indicating a net positive and negative charge density, respectively. In the high-SPV region, the dielectric charge is primarily attributed to charges at the Si/HfO_x interface. The change in charge polarity with increasing annealing temperature have been reported and is attributed to a phase transition from an amorphous to a polycrystalline state induced by annealing [67], [68]. It is likely that deep acceptor states are created after annealing above 350 °C due to the structural changes at the Si/HfO_x interface, shifting the net charge density from positive to negative [59], [69], [70].

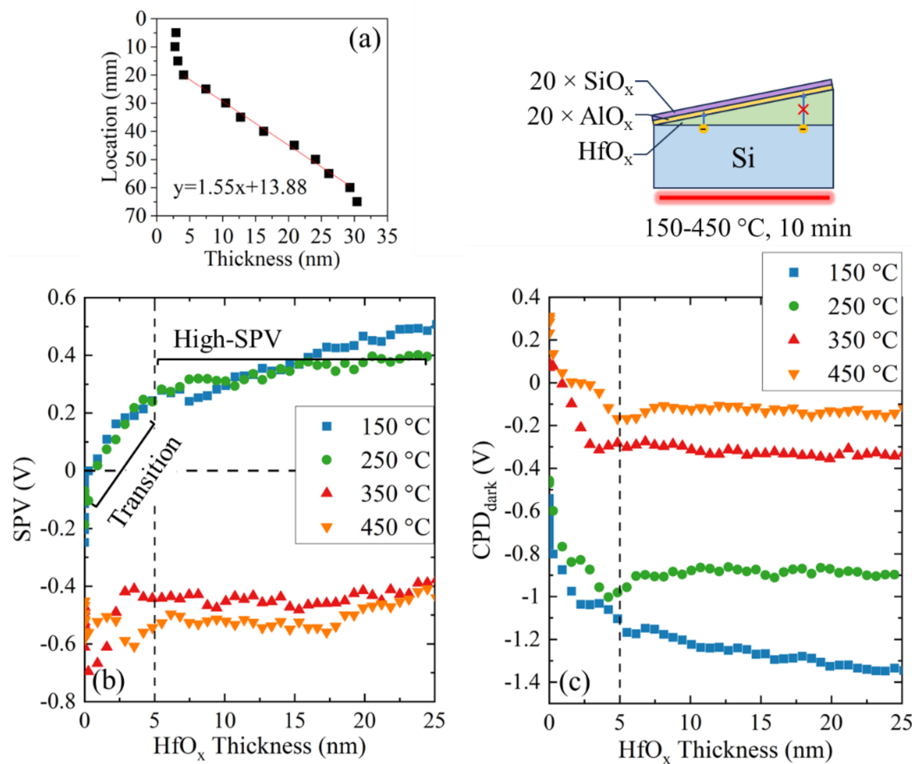


Figure 3.3.4 (a) SPV profiles and (b) CPD profiles measured in dark as a function of HfO_x thickness, measured after annealing at different temperatures. The black brackets mark the transition and high-SPV region for SPV profiles obtained after annealing at 150-450 °C. Each point represents the average of 50 measurements at a single location.

It is concluded that HfO_x is unsuitable as a capping layer when charges are injected after the layer deposition, as no significant difference was found in the electron injection efficiency across the temperature

range of 150-450 °C. However, its excellent insulation properties are ideal for protecting surface charge if the charges are injected before the capping layer deposition. This is further investigated in Section 3.4.2.

3.3.3 Discussion

Distinct differences in the charge injection behaviour were observed when using SiO_x or HfO_x as interlayers between Si and the SiO_x/AlO_x interface. For clarity, the dielectric thickness at which the SPV profiles change from the transition region to the high-SPV region is defined as the cut-off thickness, which marks the suppression of electron injection process. A higher cut-off thickness was observed for SiO_x compared to HfO_x. This is consistent with previous literature, where 15 cycles of HfO_x or 12 nm thermal SiO_2 were found to effectively reduce the negative charge density in AlO_x [40], [42]. Moreover, for SiO_x, the cut-off thickness exhibited temperature dependence, whereas a ~5 nm cut-off thickness was obtained for HfO_x across the tested temperature range. These findings suggest distinct charge injection mechanisms with interlayers of SiO_x and HfO_x.

The injection of electrons from the Si substrate to the defect states at the SiO_x/AlO_x interface requires an energetically accessible pathway. It is unlikely that this pathway is through the conduction band of the interlayer dielectric, given that the electron thermal energy at 450 °C (~64.5 meV) is much lower than the energy barrier created by the conduction band offset between Si and the dielectric.

Instead, a more plausible pathway is provided by localised trap states within the dielectric bandgap. Electrons can jump between these defect states through either thermal activation or tunnelling, effectively reducing the energy barrier [190]. It is proposed that the effective barrier height in SiO_x is comparable to the energy variation resulting from a 100 °C temperature change (~9 meV) [191], leading to a strong temperature dependence in the cut-off thickness observed between 150-450 °C. These trap states have been proposed to originate from oxygen vacancies incorporated during deposition [192]. A schematic representation of the defect-assisted injection process is shown in Figure 3.3.5. In contrast, a higher energy barrier could be present for the tunnelling process in HfO_x [193], resulting in a smaller cut-off thickness and minimal temperature dependence. Based on these observations, it is concluded that a defect-assisted tunnelling process is involved in the charging the SiO_x/AlO_x interface through a SiO_x interlayer but is absent through a HfO_x interlayer in the tested temperature range.

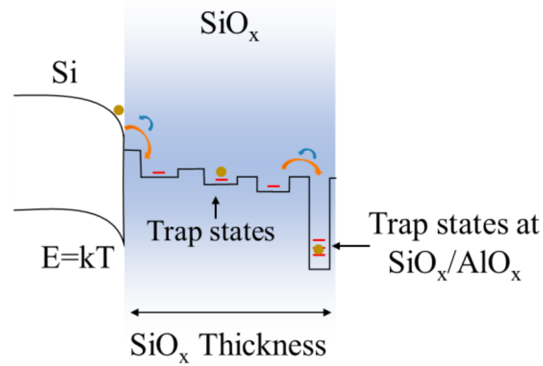


Figure 3.3.5 Schematic of the defect-assisted electron injection process for an interlayer of SiO_x at temperature T.

3.4 Charge Embedding

This section presents the charge embedding strategies for fabricating charged dielectrics. As discussed in the previous section, a thickness window for ALD-SiO_x as a capping layer has been identified, enabling the charging of defect states at the SiO_x/AlO_x interface at elevated temperatures. This allows the deposition of the full dielectric stack before the charging process, a method referred to as the post-cap charge embedding process. Alternatively, while a thickness window was not determined for ALD-HfO_x, it exhibits excellent insulating properties. This suggests an approach where charge is embedded prior to capping layer deposition, referred to as the pre-cap charge embedding process.

3.4.1 Post-Cap Charge Embedding

The post-cap charge embedding process focuses on charging defect states at the SiO_x/AlO_x interface, using ALD-SiO_x as the capping protecting layer. The dielectric stack, consisting of 0 or 20 cycles of AlO_x, followed by 360 cycles of SiO_x, was deposited using the Savannah ALD on quarter-sized Si samples with a 300 nm thermal SiO_2 layer (Set 6). The ALD-SiO_x layer was in parallel deposited on a bare Si substrate (Set 1) and is measured to be ~28 nm. To remove chargeable defects in the ALD-SiO_x layer, the samples were annealed at 800 °C for 30 minutes. Five corona-anneal cycles were performed, with each cycle involving a negative corona charge deposition of 30 seconds at room temperature, and an annealing at 450 °C for 60 seconds. Changes in the injected charge density was monitored using KP at the edges of the quarter-sized samples (~1-2 cm^2). The corresponding CPD values measured after each corona-anneal cycle are presented in Figure 3.4.1.

After each corona-anneal cycle, the dielectric stack with an AlO_x layer demonstrated a higher CPD value compared to the stack without AlO_x. This aligns with the previous observations, indicating the charging of defects at the SiO_x/AlO_x interface. The maximum surface charge density after five corona-anneal cycles is calculated to be ~4.3×10^{12} q cm^{-2}, according to Equation (2.4.12).

For the dielectric stack without an AlO_x layer, a linear increase in the CPD values was also observed with increasing corona-anneal cycles. This suggests the incomplete removal of chargeable defects, which could be attributed to a variation in the furnace temperature. When the number of corona-anneal cycles exceeded four,

the CPD values began to deviate from the linear trend. This result suggests the formation of additional defects in the dielectric due to the charging process itself. To balance maximising the injected charge density while minimising defect generation, four corona-anneal cycles were chosen as the standard charging process.

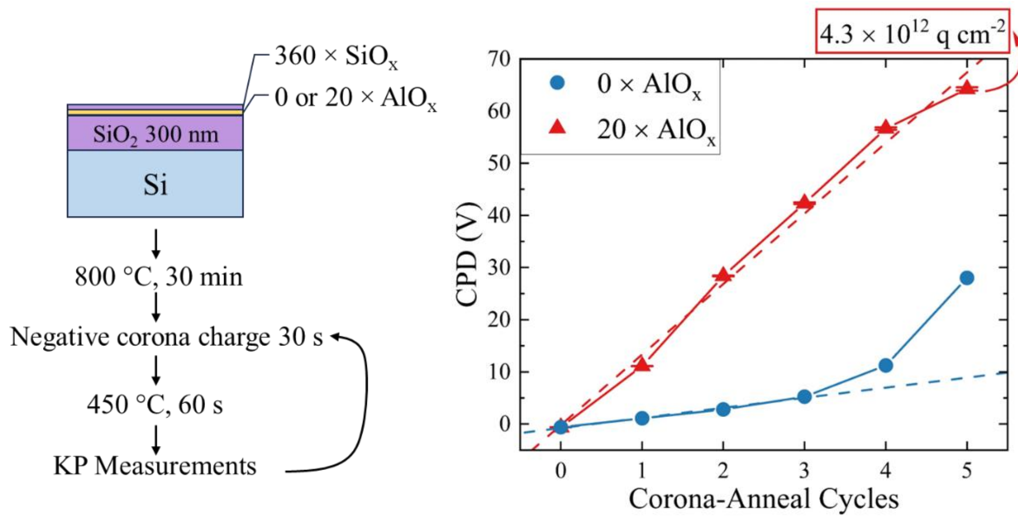


Figure 3.4.1 CPD values with increasing corona-anneal cycles. Each corona-anneal cycle consists of a deposition of negative corona charge for 30 seconds and room temperature, and an annealing at 450 °C for 60 seconds. The error bar represents 10-90% of the values obtained in a 6×6 mm map with 16 points.

The charging behaviour of the SiO_x/AlO_x interface with an AlO_x capping layer is investigated next. Prior to film deposition, the substrate (Set 6) was annealed at 800 °C for 30 minutes to remove chargeable defects in the thermal SiO_2 layer. Additional details are provided in Appendix C. A 100-cycle AlO_x layer was deposited on a quarter-sized sample using the Savannah ALD. The sample then underwent four corona-anneal cycles, each consisting of a 30-second deposition of negative corona charge followed by an annealing at 450 °C for 60 seconds. Changes in the CPD values with increasing corona-anneal cycles are presented in Figure 3.4.2.

It is demonstrated that charge injection remains possible with an ~10 nm AlO_x layer above the SiO_x/AlO_x interface. The charged defects are most likely located at the interface rather than the AlO_x bulk [47], [48], [50]. Based on this assumption, the injected negative charge density after four corona-anneal cycles is calculated to be ~1.7×10^{12} q cm^{-2}.

Furthermore, an increase in the injected charge density per cycle was observed after the first two corona-anneal cycles. This indicates the formation of defects in the AlO_x bulk, which subsequently facilitate the charging process. Alternatively, since the formation of defect states at the SiO_x/AlO_x interface also requires annealing around 450 °C [50], [189], the initial charging speed could be limited by a lack of chargeable defects at the interface.

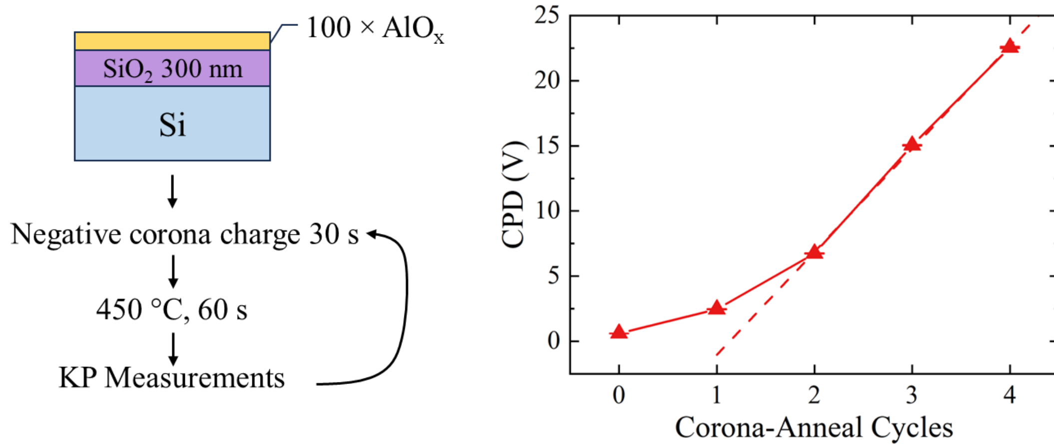


Figure 3.4.2 CPD values with increasing corona-anneal cycles on a substrate with 100 cycles of ALD-AlO_x on a 300 nm SiO_2 layer. Each corona-anneal cycle consists of a deposition of negative corona charge for 30 seconds and room temperature, and an annealing at 450 °C for 60 seconds. The error bar represents 10-90% of the values obtained in a 6×6 mm map with 16 points.

The injected charge density per corona-anneal cycle on different dielectric stacks, extracted from the linear region of the charging process, is summarised in Table 3.4.1 The dielectric stacks, consisting of ALD-deposited AlO_x/SiO_x, SiO_x, or AlO_x films on Si substrates with a 300 nm thermal SiO_2 layer, are referred to as stack I, II, and III, respectively. The charge injection rate follows I>III>II. It is proposed that the charge injection rate is limited by the density of chargeable defects. In stack I, the AlO_x is interfaced with both the thermal SiO_2 layer and the ALD-SiO_x layer, potentially introducing a higher defect density. Meanwhile, the AlO_x in stack III is only interfaced with the thermal SiO_2 layer, resulting in a smaller defect density. A higher charge injection rate is preferred to avoid excess sample handling and formation of defects during the charge injection process.

Table 3.4.1 Summary of negative charge injection rate (Q_{neg} per cycle) on different dielectric stacks. Stack structures are described by the number of ALD cycles deposited for the corresponding films. For example, 360×SiO_x represents 360 cycles of ALD-SiO_x deposited.

	I	II	III
Stack Structure	360×SiO_x / 20×AlO_x	360×SiO_x	100×AlO_x
	Thermal SiO_2 300 nm		
Q_{neg} per cycle (10^{11} q cm^{-2})	10	1.7	6.0

3.4.2 Pre-Cap Charge Embedding

A charging method involving the deposition of corona charge at elevated temperatures, also referred to as hot corona charging, is utilised for the pre-cap charge embedding strategy. Silicon substrates with a 300 nm thermal SiO_2 layer (Set 6) were diced into 1×1 cm^2 samples and subjected to negative corona charging at temperatures ranging from 150 to 450 °C. After an accumulated charging time of 120 seconds, the samples were annealed at 350 °C to investigate the charge stability. The change in surface charge density was monitored using KP and is plotted in Figure 3.4.3.

During the charging process, hot corona charging at higher temperatures resulted in lower CPD values, indicating a lower negative charge density. The injected charges likely reside near the SiO_2 film surface, where negatively charged ions transfer their electrons to trap states in the dielectric [166]. However, the high negative charge density achieved by hot corona charging at low temperatures (150 and 250 °C) degraded rapidly at 350 °C, reaching a lower charge density than the samples charged at higher temperatures.

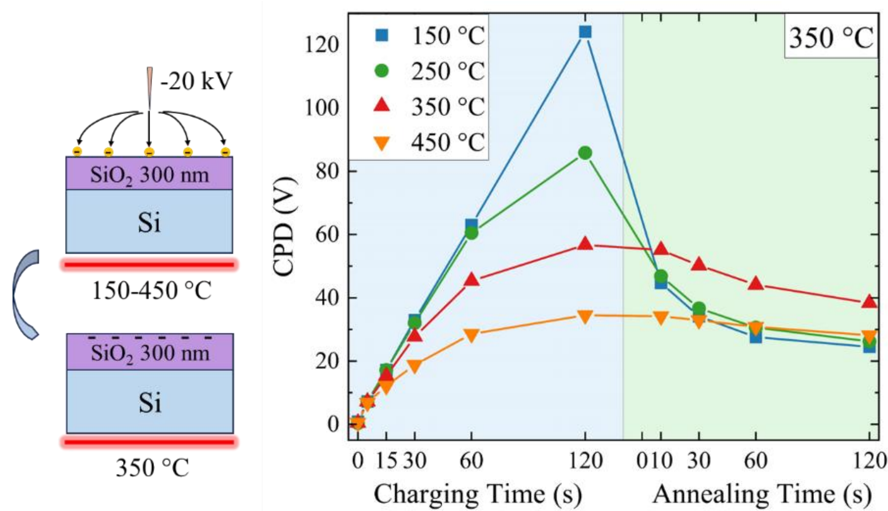


Figure 3.4.3 CPD values with increasing hot corona charging time and annealing time. The error bar represents 10-90% of the values obtained in a 6×6 mm map with 16 points but are not visible in this plot.

The high injected charge density and low stability observed on samples subjected to hot corona charging at low temperatures can be attributed to charge trapping and de-trapping of the dielectric defects. It is noted that the tested samples were deposited on Set 6 substrates without undergoing annealing at 800 °C. This suggests that chargeable defects were likely already present in the SiO_2 layer prior to the hot corona process, as demonstrated in Appendix C. Schematic diagrams of the proposed process are shown in Figure 3.4.4. At low temperatures, electrons from negative corona charge are captured by both shallow and deep defect states near the dielectric surface. The higher charge density is likely due to the abundance of available defects and the slower degradation of corona charge in air. Increased likelihood of charge de-trapping at elevated temperatures is supported by the decreased thermal stability of corona charge deposited at room temperature, as shown in Appendix C. During the annealing at 350 °C after charging, electrons trapped in shallow traps or traps near the dielectric surface are thermally activated to de-trap, leading to charge loss, as shown in Figure 3.4.4 (a), process (1). Meanwhile, during charging at high temperatures, electrons are driven into defect states deeper into the dielectric films, leading to an improved thermal stability, as shown in Figure 3.4.4 (a), process (2).

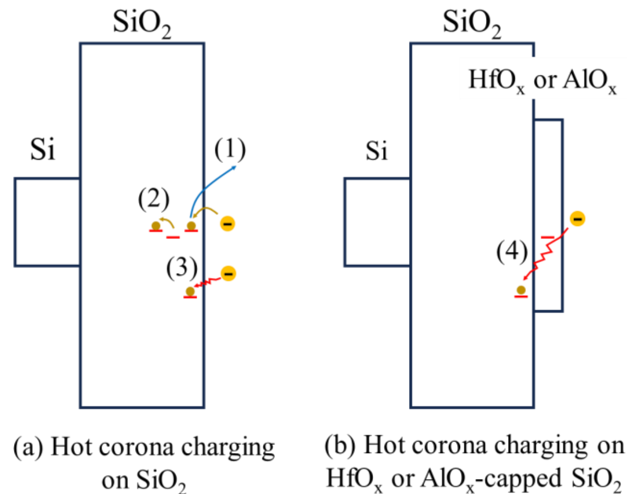


Figure 3.4.4 Schematic diagrams of (a) hot corona charging on SiO_2 and (b) hot corona charging on HfO_x or AlO_x-capped SiO_2. The numbers correspond to different processes proposed to occur during hot corona charging: (1) charge de-trapping, (2) charge injection deeper into the dielectric, (3) creation and charging of defects with deep energy levels, and (4) creation of defects in HfO_x or AlO_x, which enables charging of defects in SiO_2.

To investigate if additional defects were created in the hot corona process, a Set 6 substrate, annealed at 800 °C for 30 minutes, was deposited with 20 cycles of AlO_x and 50 cycles of HfO_x. A corona-anneal process was performed, with a negative corona charge deposition of 30 seconds, followed by annealing at 450 °C. The change in CPD values with increasing annealing time is shown in Figure 3.4.5 (a), represented by the light purple symbols. In line with the findings in Section 3.3, the CPD value decreased to ~0 V after only 5 seconds of annealing, indicating the lack of a charge injection pathway.

The sample was subsequently subjected to hot corona charging for 5 minutes at 450 °C. The surface charge was removed by immersing the sample in isopropyl alcohol (IPA) at room temperature. The same corona-anneal process was then repeated, with the corresponding changes in CPD value shown in Figure 3.4.5 (a), represented by the dark purple symbols. A high charge stability was demonstrated by the minimal change in CPD values after 60 seconds of annealing, which suggests the generation of defects by the hot corona process. For comparison, the same corona-anneal process was conducted on a Set 6 substrate with 20 cycles of AlO_x and SiO_x stack, as discussed in Section 3.2.2, represented by the red symbols in Figure 3.4.5 (a). The results indicate a higher charge stability in the hot corona-generated charged defects, comparing to charged defects at the SiO_x/AlO_x interface, suggesting defects with deeper energy levels were induced by the hot corona process, as shown in Figure 3.4.4 (a), process (3).

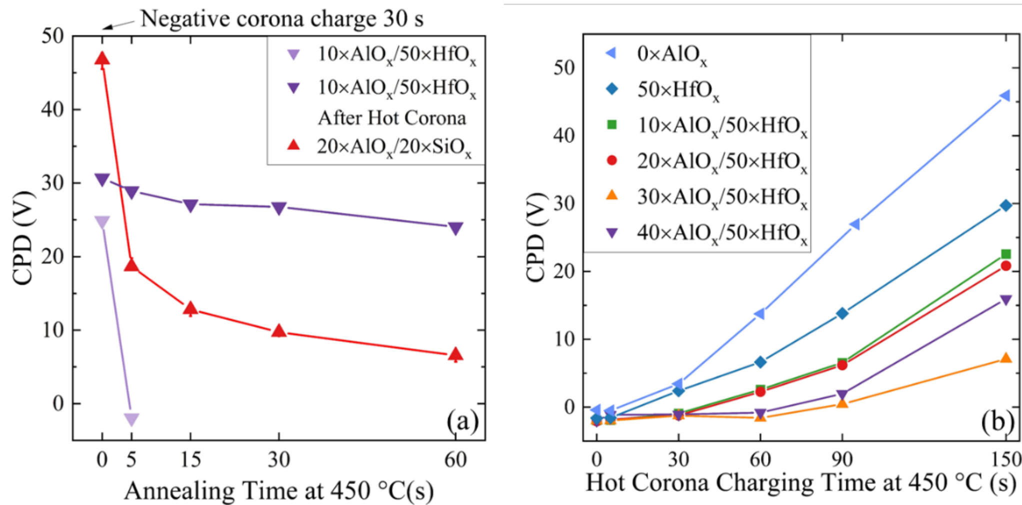
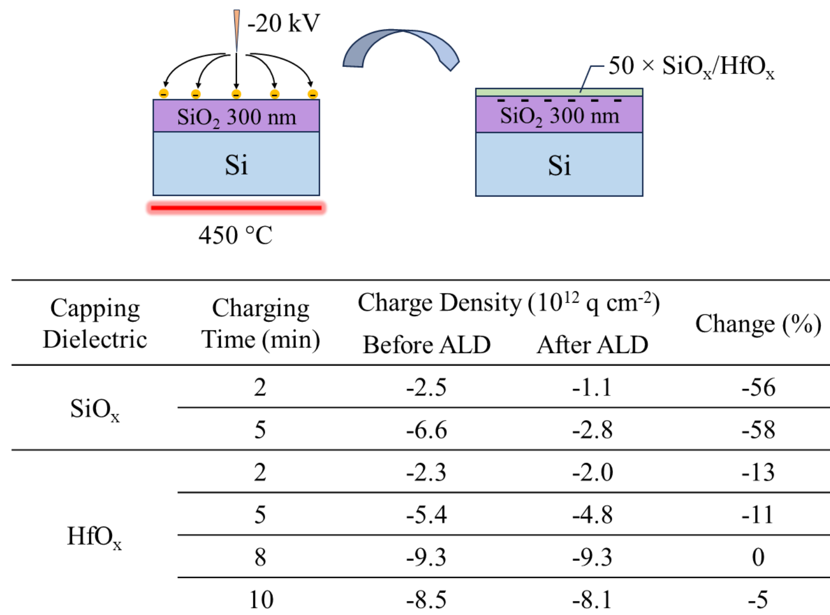


Figure 3.4.5 (a) CPD values with increasing annealing time at 450 °C after 30-seconds of negative corona charge deposition at room temperature. The different symbols represent different ALD layers deposited on 800 °C-annealed Set 6 substrates (b) CPD values with increasing hot corona charging time at 450 °C on substrates with different ALD layers on 800 °C-annealed Set 6 substrates. The error bars represent 10-90% of the 50 measurements obtained on a single location at the centre of the same sample with continued annealing or charging steps. The error bars are not visible in this plot due to the large differences of CPD values in successive steps.

To investigate the location of hot corona-generated defects on the thermal $SiO_2/AlO_x/HfO_x$ dielectric stack, Set 6 substrates were deposited with AlO_x or HfO_x films and subjected to hot corona charging at 450 °C. The substrates were annealed at 800 °C for 30 minutes prior to ALD deposition. The change in CPD values as a function of charging time is shown in Figure 3.4.5 (b). The results demonstrate that as the thickness of the AlO_x or HfO_x increases, a delay in the charging injection is observed compared to sample with a bare thermal SiO_2 layer. This suggests that the deep defect states are primarily located within the SiO_2 layer. When a AlO_x or HfO_x layer is present, a longer charging time is required to induce defect states in these films, which facilitate defect generation and charge injection into the underlying SiO_2 film, as shown in Figure 3.4.4 (b), process (4). This result also highlights the necessity of depositing the capping layer after the charging process to prevent defect generation in the capping layer dielectric. The generated defects in SiO_2 are proposed to be associated with Si dangling bonds, which are formed due to the bombardment of high energy charged ions [194], [195]. Hot corona charging of thermal SiO_2 at 450 °C is adopted as the standard process to maximise the generation of deep defect states.

Finally, to evaluate the effectiveness of ALD-HfO_x in preserving embedded charge, a Set 6 substrate (annealed at 800 °C for 30 minutes) was hot corona-charged for 2, 5, 8, 10 minutes at 450 °C. Following this, 50 cycles of SiO_x or HfO_x was deposited on the charged sample using the Savannah ALD. Surface charge densities before and after the ALD process were characterised using KP with the calculated values shown in Figure 3.4.6. A larger loss of negative charge was observed in SiO_x-capped samples compared to HfO_x-capped samples. This is likely due to the higher density of defects in the SiO_x layer relative to HfO_x, which facilitates charge degradation in a manner similar to the charge injection mechanism proposed in Section 3.3.3. The reduction in charge observed in both SiO_x and HfO_x-capped samples is likely related to the exposure to

precursor gases during the initial ALD cycles. Therefore, ALD-HfO_x is considered a more suitable capping layer for preventing charge loss. Overall, the hot corona-charged dielectric with HfO_x capping layer is identified as a promising charged dielectric system for the doping of 2D semiconductors.



Capping Dielectric	Charging Time (min)	Charge Density (10^{12} q cm^{-2}) Before ALD	After ALD	Change (%)
SiO_x	2	-2.5	-1.1	-56
	5	-6.6	-2.8	-58
HfO_x	2	-2.3	-2.0	-13
	5	-5.4	-4.8	-11
	8	-9.3	-9.3	0
	10	-8.5	-8.1	-5

Figure 3.4.6 Measured charge densities on hot corona-charged Set 6 substrate (annealed at 800 °C, 30 minutes) before and after depositing 50 cycles of SiO_x or HfO_x.

3.5 Summary

This chapter focuses on the design and fabrication of negatively charged dielectrics by introducing and charging defects. Charging of defects at the SiO_x/AlO_x interface was studied, identifying three key requirements for forming negative charge: the presence of an AlO_x layer (as few as 10 ALD cycles), activation annealing, and a nearby electron source. In addition to the widely reported Si substrate, negative corona charge has been identified as an alternative electron source, enabling defect charging at the SiO_x/AlO_x interface even 300 nm from Si. The insights gained on the charging mechanism of ultra-thin AlO_x layers lay the foundation for novel Si passivation strategies discussed in Chapter 4 and 5.

A field-effect doping strategy for 2D semiconductors using negatively charged dielectrics was proposed. The design for such dielectrics requires a capping layer, a charged layer, and an insulation layer. A 300 nm thermal SiO_2 layer serves as the insulation layer in this work. Two distinct dielectric charging strategies were presented based on different capping and charged layers.

The post-cap charge embedding strategy utilises defects at the SiO_x/AlO_x interface. A thickness window of ~10-26 nm has been identified for ALD-SiO_x, enabling negative charge injection at 450 °C while preventing charge degradation at temperature below 150 °C. After fabricating the full dielectric stack, four corona-anneal cycles were found to be the optimal charge injection condition, balancing high injected charge density with minimal defect generation. Each cycle consists of 30 seconds of negative corona charge deposition at room

temperature, followed by a 60-second annealing at 450 °C. The same corona-anneal process was applied to charge a ~10 nm AlO_x layer on 300 nm SiO_2, where charge injection was also observed but at a lower rate.

The pre-cap charge embedding strategy utilises defects generated by the hot corona process, which involves depositing corona charges at elevated temperatures. Defects with deep energy levels were found to form in the thermal SiO_2 layer, exhibiting greater stability than charged defects at the SiO_x/AlO_x interface at 450 °C. ALD-HfO_x was chosen as the capping layer for its excellent insulating properties. The charging process was performed before capping layer deposition to prevent defect generation in the film. The embedded charges were found to be preserved during the deposition of ALD-HfO_x, despite of the exposure to highly reactive precursor gases. Three charged dielectric stacks – capped with SiO_x, AlO_x, and HfO_x – have been developed in this chapter and showed potential to act as field-effect sources for 2D semiconductor doping, as later explored in Chapter 7.

Chapter 4
Passivation of p-Si Surfaces using $SiO_x/AlO_x/SiN_x$ Nanolayer Stacks

4.1 Introduction to Surface Passivation using Ultra-thin AlO_x

Achieving high-efficiency silicon solar cells is critical for the future of solar power, directly impacting the cost-effectiveness and scalability of photovoltaic technology in the push to meet global energy demands. Silicon surface passivation remains a critical factor in enhancing the efficiency of solar cells, particularly as the photovoltaic industry seeks to push the boundaries of conversion efficiency. Recent advancements in silicon technology showed that record-breaking efficiencies >26% are possible thanks to the optimised surface passivation to minimise carrier recombination, maximising open-circuit voltage and fill factor [196]. Dielectric materials such as silicon dioxide (SiO_2), silicon nitride (SiN_x), and aluminium oxide (AlO_x), have been widely studied to passivate silicon surfaces and minimise charge loss [11], [73].

Aluminium oxide has been particularly promising as it enabled the recent widespread adoption of the passivated emitter and rear cells (PERC), and it is crucial for the now mainstream tunnel oxide passivating contact (TOPCon) solar cells. AlO_x deposited by atomic layer deposition (ALD) can effectively passivate both n-type and p-type Si due to the presence of a negative fixed charge on the level of $1 - 10 \times 10^{12}$ q/cm^2 [197], [198], [199], [200]. Achieving optimal passivation requires films of 5-30 nm in thickness [201]. Effective surface recombination velocities (S_{eff}) as low as 1.6 and 4 cm/s have been obtained on n and p-type Si of 1 Ω·cm resistivity, passivated by ALD-AlO_x of 30 nm [202]. However, the deposition of such thick AlO_x layers poses challenges for industrial applications due to the substantial production costs required in lengthy ALD processes [203]. Furthermore, with the advent of TOPCon, excellent passivation of n-type Si has been deployed, and ever-higher efficiencies hinge on achieving superior p-type passivation via AlO_x [185], [201], [204]. Compared to thick AlO_x (5-30 nm) layers, surface passivation using ultra-thin AlO_x (<2 nm) is still ineffective, severely limiting cell efficiency [41]. While a S_{eff}<2 cm/s has been obtained with 4 nm of AlO_x on n-Si [18], the lowest reported S_{eff} is constrained to ~11 cm/s on p-emitters, passivated by a 3 nm AlO_x and an additional SiN_x capping layer for enhanced chemical passivation [198]. Understanding and developing methods to improve the passivation quality to achieve S_{eff}≤2 cm/s with ultra-thin AlO_x (<2 nm), is critical to enable >26% efficient TOPCon solar cells [205].

Surface recombination can be minimised by jointly exploiting chemical and field-effect passivation (FEP) [11]. Consistent with the observations in Chapter 3, ALD AlO_x with as few as 10 cycles thickness has been

reported to induce a negative charge density of ~5×10^{12} q cm^{-2} [40], providing sufficient field-effect passivation. Further increase in charge density showed minimal additional impact [177]. However, reduced AlO_x thickness can cause incomplete surface coverage and reduced hydrogen content [185], [206], leading to a high interface defect density and subsequently lower passivation quality. Therefore, optimising chemical passivation for ultra-thin AlO_x is crucial for high-efficiency solar cell applications.

Chemical passivation is achieved by reducing the amount of dangling bonds at silicon surface that act as carrier recombination sites [207]. In an AlO_x-passivated Si, an interfacial SiO_x layer grows between the AlO_x and Si and is crucial to the chemical passivation quality [18], [50], [208]. Intentionally growing a thin oxide prior to ALD deposition has been demonstrated to reduce surface recombination by effectively terminating the silicon crystalline structure with a SiO_x layer [56], [185], [207]. Table 4.1.1 presents a summary of the surface recombination parameters reported in the literature for schemes using an intentionally grown SiO_x combined with an AlO_x layer, where a general improvement in passivation was observed with a pre-grown SiO_x layer. A pre-grown SiO_x layer is also preferred in industrial applications, as it allows sample storage between cleaning and film deposition [20]. Among the low-temperature pre-deposition treatments reported, nitric acid oxidised Si (NAOS) offers an easy process control thanks to its self-limiting nature [209]. A higher passivation stability has also been reported after firing with a NAOS layer [20]. Despite the numerous studies employing NAOS prior to AlO_x deposition [16], [185], superior passivation (S_{eff}<2 cm/s) using NAOS and ultra-thin AlO_x (<2 nm) has not been demonstrated yet.

Besides the pre-grown SiO_x, another approach to enhance chemical passivation involves interface hydrogenation. Atomic hydrogen is introduced into the dielectric thin film, either in-situ from hydrogen-containing precursors or ex-situ during post-deposition treatments [210], [211], [212]. The most ubiquitous method is via hydrogenated silicon nitride deposited by plasma-enhanced chemical vapour deposition (PECVD), commonly used in a stack with thick AlO_x to passivate p-type silicon surfaces [197], [213], [214]. Besides serving as a hydrogen source, SiN_x films functions as an anti-reflection coating and a protective layer for AlO_x against metallisation paste [215]. Therefore, it is essential to study SiN_x films in combination with ultra-thin AlO_x – something rarely reported in the literature.

Considering both field-effect and chemical passivation, this chapter presents a $SiO_x/AlO_x/SiN_x$ passivation stack for p-type Si surfaces. The SiO_x layer is formed using nitric acid, combined with an ultra-thin AlO_x and a hydrogenated SiN_x layer. This low-temperature, fast process can reduce production costs. A detailed interface analysis is carried out to reveal the passivation mechanisms present.

Table 4.1.1 Summary of reported intentionally grown-SiO_x prior to ALD-AlO_x depositions. Pre-deposition treatment marked with * represents that the samples were cleaned using UV ozone, while others were cleaned with RCA followed by a HF dip prior to SiO_x growth or ALD depositions. HF-last stands for a process where no oxide was intentionally grown prior to AlO_x deposition. FGA stands for forming gas anneal. All AlO_x films are reported to be deposited by ALD, while SiN_x films are grown by PECVD.

Ref.	Si	Pre-deposition Treatment	SiO_x (nm)	AlO_x (nm)	SiN_x (nm)	Annealing	J_0 (fA/cm^2)	S_{eff} (cm/s)
Zin et al.[21]	n 2-5 Ω·cm 180 μm	UV Ozone*	4.3	10-15	No	450 °C, N_2, 30min	5	
		HF-last*					7	
Gao et al.[22]	n 2-5 Ω·cm 180 μm	UV Ozone*	1.3	10	No	450 °C, N_2, 30min	5	
		HF-last*					8	
Penaud et al.[20]	p 0.5-3 Ω·cm	H_2O_2/H_2SO_4		10	80	815 °C		9
		HNO_3/H_2O/surfactant						39
		RCA-1						4
		HNO_3						7
Kaur et al.[18]	n 3-4 Ω·cm 160 μm	HF-last	1.5	4	No	425 °C, 30 min		1
		RCA-2	1.75					2
Hiller et al.[185]	p 2.5 Ω·cm	FGA	1	7 cycles	No	RTA, 800-850 °C, 10-90s followed by FGA, 425 °C, 30 min	<75	
		HNO_3	1.6				<125	
		O_3 (in-situ of ALD)	0.6				<75	
		H_2O (in-situ of ALD)	0.6				<75	
		thermal SiO_2	1.6				<40	
Shedd et al.[216]	n 5 Ω·cm 200 μm	HF-last	1-2	15	80	425 °C or 450 °C, N_2, 30 min	19	
		Ozonised DI Water					16	

4.2 Nanolayer Passivation Optimisation on n-type Si

Isolating the precise surface recombination parameters without interference from the bulk requires high-quality n-type FZ-Si. For this reason, the $SiO_x/AlO_x/SiN_x$ nanolayer stack was first optimised on n-type Si, focusing on the thickness of the AlO_x layer. Symmetrically passivated samples were fabricated on quarter-sized Set 2 substrates. The samples were cleaned using the RCA process, followed by an immersion in heated nitric acid, as described in Appendix B, to form a SiO_x layer. AlO_x of 5 to 40 cycles were deposited on both sides of the samples using the Anric ALD, followed by a deposition of ~60 nm SiN_x films using PECVD. Details of the film deposition process is included in Chapter 2. The refractive index was measured to be 1.9 using an ellipsometer. After film deposition, the samples were annealed at 400 or 450 °C for 10 minutes in air. Negative corona charge was then deposited on both sides of the samples at room temperature to investigate the maximum effective lifetime (τ_{eff}) reachable with enhanced field-effect passivation. The τ_{eff} measured after annealing, and with additional negative surface charge, is shown in Figure 4.2.1.

An increase in τ_{eff} was observed with increasing AlO_x cycles, indicated by the blue bars in Figure 4.2.1, despite of the change in annealing temperatures (400 or 450 °C). With AlO_x cycles less than 30, increased τ_{eff} was observed with additional surface negative corona charge. This indicates that the intrinsic FEP provided by

the AlO_x layer alone was insufficient, and that external charge was required to enhance surface passivation. Such an increase becomes smaller with more AlO_x deposition until 30 cycles, beyond which little change in τ_{eff} was observed with additional negative surface charge deposition. The maximum τ_{eff} obtained with additional field-effect passivation was 1-2 ms with no clear relation to the number of AlO_x cycles. The improvements in τ_{eff} after annealing with increasing AlO_x cycles could, in principle be attributed to the enhancement of both chemical and FEP, as is discussed below. The optimum AlO_x thickness is determined to be 30 cycles.

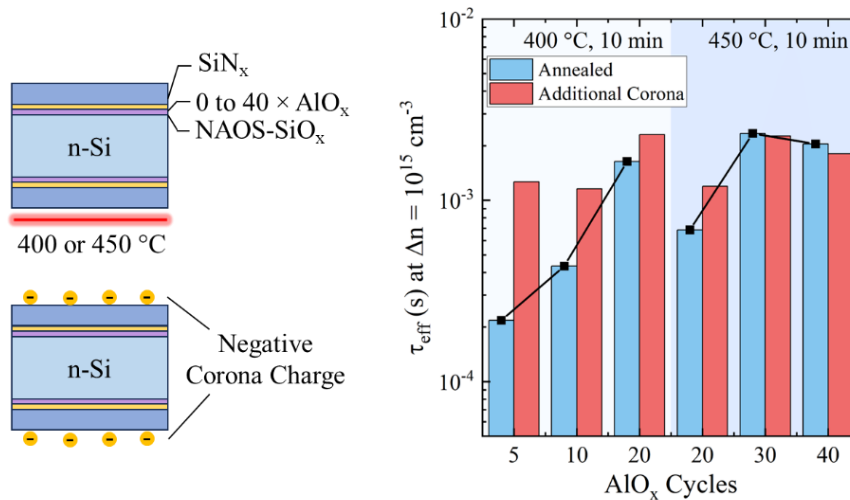


Figure 4.2.1 Effective lifetime (τ_{eff}) measured on $SiO_x/AlO_x/SiN_x$-passivated n-type Si with increasing AlO_x cycles. Different columns represent the τ_{eff} measured after annealing, and with additional negative surface charge.

To investigate the change in chemical passivation with increasing AlO_x cycles, positive corona charge was deposited on both sides of the samples to neutralise the internal fixed charge of AlO_x. The previously deposited negative corona charge was first removed by dipping samples in isopropyl alcohol (IPA) and drying with a N_2 gun. All samples were then re-annealed at 450 °C for 10 minutes to remove moisture and surface contamination. A slight decrease in τ_{eff} was observed compared to "Annealed" samples in Figure 4.2.1, likely due to sample handing [217]. Kelvin probe (KP) measurements were conducted to confirm the removal of surface charge before depositing positive corona charge in 5 or 10 seconds steps, on both sides of the samples. The changes in τ_{eff} were monitored as a function of positive surface charge density and plotted in Figure 4.2.2 (a). The calibration of the deposition rate of positive corona charge is included in Appendix D. With the deposition of positive surface charge, τ_{eff} decreases due to reductions in the FEP. The effective fixed charge density (Q_{eff}) of the films can be determined when the minimum τ_{eff} is reached, indicating the flat-band regime at which maximum recombination occur. The minimum τ_{eff} and Q_{eff} extracted at the flat-band condition with increasing AlO_x deposition is shown in Figure 4.2.2 (b), representing the quality of chemical and field-effect passivation, respectively.

An increased negative Q_{eff} was observed with more AlO_x cycles, as shown by the right shifts of the τ_{eff} minima. This dependence is nearly linear, as also reported by Richter et al. and Kaur et al [18], [198], suggesting that the limiting factor of negative Q_{eff} is the chargeable defect density at the SiO_x/AlO_x interface

[51]. A density of -5.3 × 10^{12} q/cm² was here produced by the deposition of 30 cycles of AlO_x, effectively passivating the n-Si surface. Although 40 cycles of AlO_x resulted in an increased negative Q_{eff}, no improvement in surface passivation was observed.

Figure 4.2.2 shows that the τ_{eff} minima increase with AlO_x film thickness, indicating a clear improvement in chemical passivation. While previous studies have attributed poor chemical passivation at low ALD cycles to incomplete surface reactions due to a deficiency of hydroxyl (-OH) groups, which can lead to a higher D_{it} [198], [218], this explanation does not apply here. In this work, the silicon surface was oxidised prior to ALD, resulting in near-complete hydroxylation [185]. Therefore, an alternative explanation must be considered.

One possible mechanism involves improved chemical passivation by hydrogenation. This is striking considering the presence of a hydrogenated SiN_x layer, which has a higher concentration of H (>10 at%) compared to ALD-AlO_x (3-4 at%) [219], [220]. The additional hydrogen introduced by an excess of 5-10 AlO_x cycles would be minimal by comparison. Therefore, it is proposed that the increased chemical passivation is a result of a specific hydrogen species. Here I suggest an increase in negatively hydrogen ions (H^-) was promoted by an increased film negative Q_{eff}. This hypothesis is supported by density functional theory (DFT) studies, where the preferred charge state of hydrogen depends of the alignment of its energy level to the Si bandgap [221]. Increased number of AlO_x cycles led to stronger FEP and upward band-bending, leading to a lower energy level of H with respect to the Fermi energy in the Si bulk, promoting H^- formation. Such H^- passivates the donor states at the Si/SiO_x interface, improving chemical passivation [222].

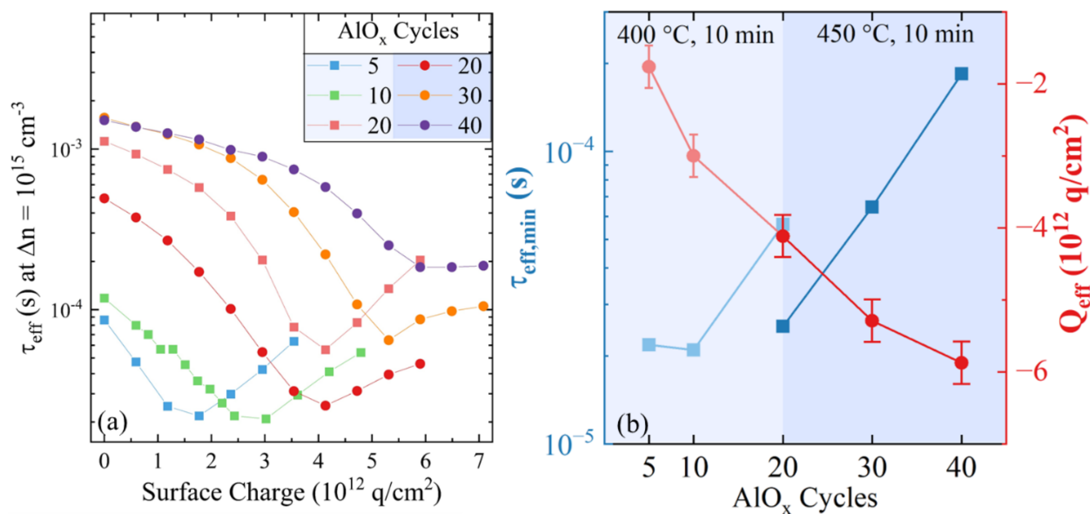


Figure 4.2.2 (a) τ_{eff} as a function of positive surface charge density $SiO_x/AlO_x/SiN_x$ passivated n-Si with increasing AlO_x cycles. (b) The extracted τ_{eff} minima ($\tau_{eff,min}$) and Q_{eff} with increasing AlO_x cycles. Error bars arise from the step size of corona charging (5.88 × 10^{11} q/cm² per 10 s) are included.

Finally, the effective surface recombination parameters are calculated. Figure 4.2.3 shows the injection level-dependent lifetimes for samples with 30 and 40 cycles of AlO_x deposited, including a theoretical calculation of surface recombination current density (J_{0s}) and effective surface recombination rate (S_{eff}) following Kimmerle's formalism [72]. The J_{0s} value was extracted with an effective intrinsic carrier concentration ($n_{i,eff}$) of 9.65 × 10^9/cm³ at 25 °C. The lowest S_{eff} of 3.3 cm/s and J_{0s} of 9.2 fA/cm² were

demonstrated with only 30 cycles of AlO_x, which is comparable to 10 nm AlO_x [22], as shown in Table 4.1.1. Only in one instance has S_{eff}<2 cm/s been reported via a 4 nm AlO_x on high resistivity Cz n-Si [18]. Here, only 30 cycles of AlO_x were deposited, which is equivalent to a layer <3 nm, yielding higher processing speed and compatibility with a SiN_x antireflection coating.

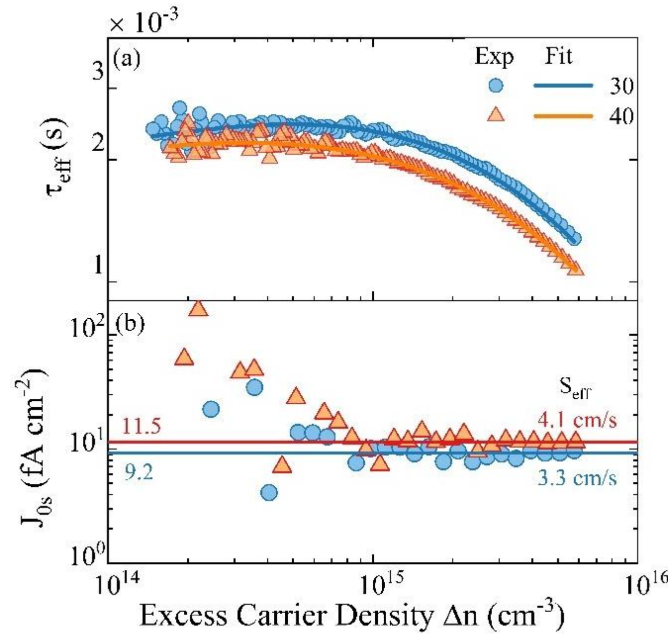


Figure 4.2.3 Extraction of recombination parameters. (a) Measured injection-dependent effective lifetime of $SiO_x/AlO_x/SiN_x$ passivated n-Si samples with 30 and 40 cycles of AlO_x. Solid lines indicate the best fit to extract (b) J_{0s} and S_{eff}.

4.3 Applying Nanolayer Passivation Stack to p-type Si

The passivation of p-Si using the optimised $SiO_x/AlO_x/SiN_x$ stack (Group A) is investigated next. Three additional passivation stacks with different combinations of the dielectric layers were studied in parallel to reveal the passivation mechanisms of the optimised stack. Only Groups A and B have an AlO_x layer of 30 ALD cycles, while only Groups A and C have a NAOS-SiO_x layer. The fabrication of each layer follows the same process described in Section 4.2. For Groups B and D, an additional dip in 5% HF was performed to remove native oxide prior to film deposition. The passivation stacks are symmetrically deposited on Cz p-Si with a resistivity of 5 Ω·cm (Set 3). A summary of the passivation stack structures is shown in Figure 4.3.1.

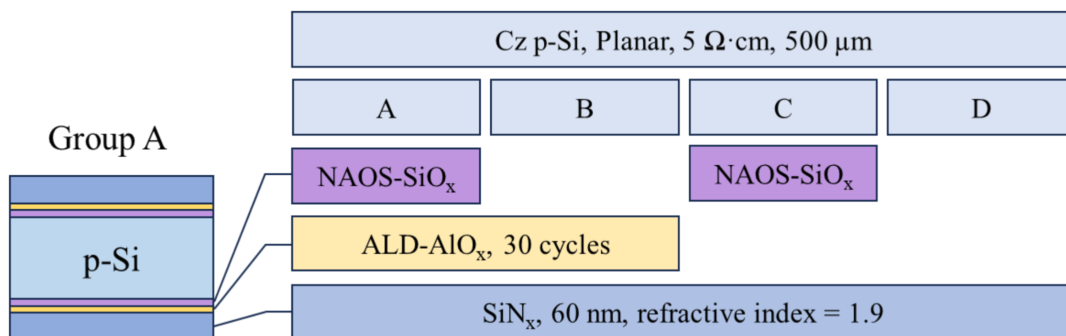


Figure 4.3.1 Summary of the passivation stacks studied.

After fabrication, Groups A-D samples were annealed at 450 °C for 10 minutes and the surface recombination parameters were evaluated by measuring the τ_{eff} at 25 °C. The measured excess carrier dependent effective lifetime and the theoretical calculation to extract S_{eff} and J_{0s} of each sample group is shown in Figure 4.3.2. The highest τ_{eff} and the lowest S_{eff} of 6.3 cm/s was achieved by the $SiO_x/AlO_x/SiN_x$ (Group A) stack, which is equivalent to a J_{0s} of 56.7 fA/cm^2. This is comparable to the reported S_{eff} of 7 cm/s achieved by a NAOS-SiO_x with an AlO_x layer of 10 nm [20]. This value is also higher than that observed on n-type Si in Section 4.2, which is attributed to the lower τ_{bulk} of the p-type wafers, limiting accurate S_{eff} extraction [223]. These results demonstrate effective passivation of p-Si is possible with an AlO_x thickness of only 30 cycles (<3 nm), significantly shortening the processing time.

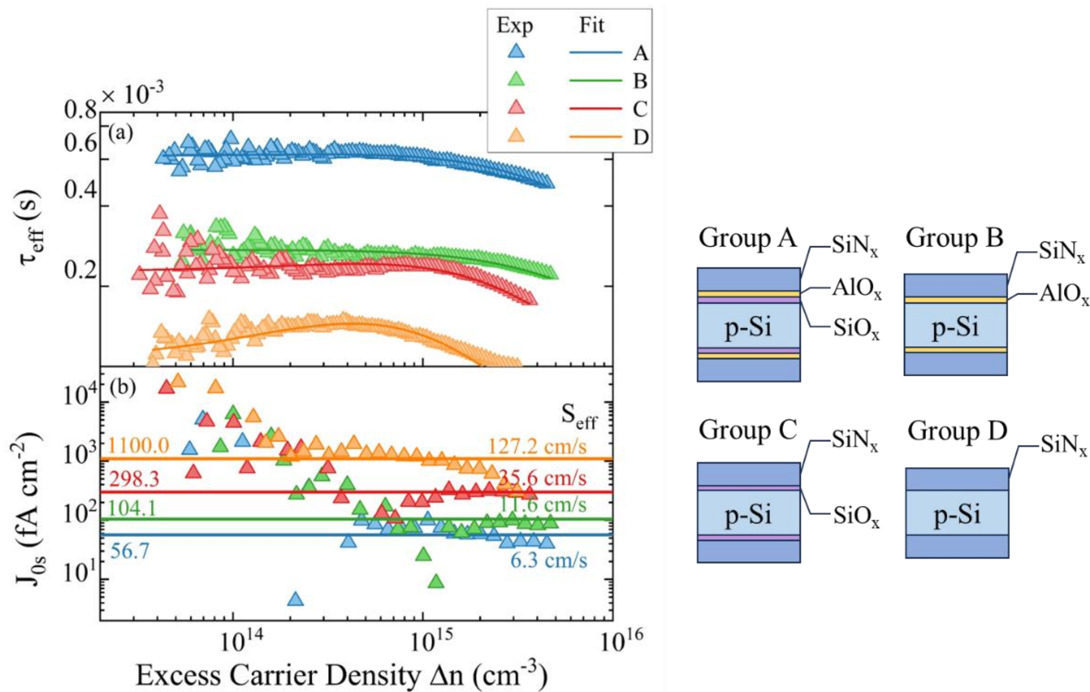


Figure 4.3.2 Extraction of recombination parameters. (a) Measured injection-dependent effective lifetime of $SiO_x/AlO_x/SiN_x$ passivated n-Si samples with 30 and 40 cycles of AlO_x. Solid lines indicate the best fit to extract (b) J_{0s} and S_{eff}.

4.4 Assessment of Si-Dielectric Interface Properties

In this section, detailed analysis of the Si/dielectric interfaces is presented to reveal the passivation mechanism of the optimised $SiO_x/AlO_x/SiN_x$ nanolayer stack. To obtain a detailed description of the Si/SiO_x interface, a surface bias was applied to a PEDOT:PSS as transparent electrode deposited on both surfaces of the samples, while monitoring the changes in τ_{eff} [148]. The measurements started with a surface potential (V_{surf}) of 0 V. A sweep with a positive voltage step was carried out until no significant change in τ_{eff} was observed. The V_{surf} was then set back to 0 V and the process was repeated with a negative voltage sweep. Using this method, a τ_{eff}-V_{surf} plot can be obtained, which contains detailed information on the Si/dielectric interface.

τ_{eff}-V_{surf} plots were obtained on Groups A-D samples both with and without an annealing at 450 °C for 10 minutes and plotted in Figure 4.4.1. Quantitative interface properties can be extracted by fitting the data to a

theoretical model described by an extended Shockley-Read-Hall (SRH) formalism [149], as described in Chapter 2, Section 2.4.3. The solid lines in Figure 4.4.1 represent the fitting where the minimum mean squared error (MSE) is obtained. The parameters used are included in Appendix E. It should be emphasized that, although only a single representative sample was characterised for each passivation scheme, the validity of the results is reinforced by complementary C–V and SPV measurements. Furthermore, the conclusions drawn in the subsequent sections are substantiated by analysis across multiple groups of samples, thereby ensuring their robustness and reproducibility.

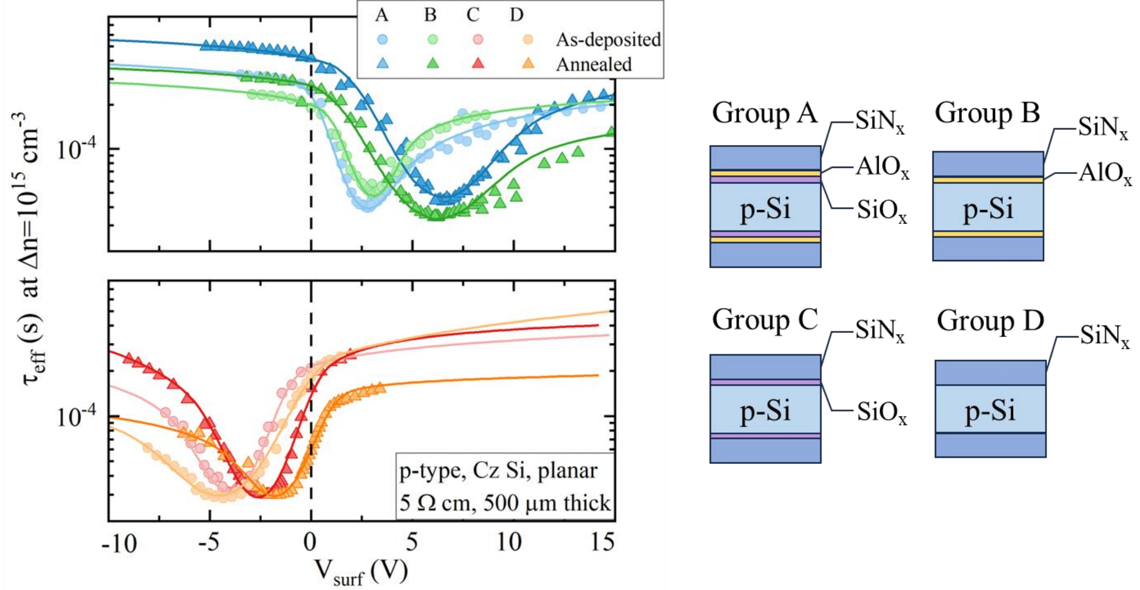


Figure 4.4.1 Effective lifetime as a function of surface voltage (τ_{eff}-V_{surf}) obtained for sample in Groups A-D, both before and after an activation annealing at 450 °C for 10 minutes, represented by the symbols. Lines represent the model fittings using energy dependent parameterisation.

4.4.1 Modelling and Understanding of τ_{eff}-V_{surf} Relations

Between samples with similar bulk properties, differences in τ_{eff} originate from defect-assisted surface recombination, governed by SRH statistics [71], [224]. As introduced in Chapter 1, the surface SRH recombination rate can be described as:

$$U_{surface} = \int_{E_v}^{E_c} \frac{n_s p_s - n_i^2}{\frac{p_s + p_1}{D_{it}\sigma_n v_{th}} + \frac{n_s + n_1}{D_{it}\sigma_p v_{th}}} dE \approx \int_{E_v}^{E_c} \frac{n_s p_s}{\frac{p_s}{S_n} + \frac{n_s}{S_p}} \tag{4.4.1}$$

which is restated here as it is critical to the following analysis. For the doping concentration in this work (moderate p-type doping), n_1, p_1, n_i are much smaller than n_s and p_s, and thus contribute negligibly as per the approximation in the above equation [71], [183]. It is therefore clear that $U_{surface}$ can be reduced by lowering $S_{n/p}$ or $n_s p_s$, namely chemical and field-effect passivation, respectively. The latter is achieved by reducing the density of one carrier type via fixed dielectric charge or externally applied electric fields, thus reducing the total $n_s p_s$ product.

By applying a surface electric field – via transparent electrodes or corona charge deposition – n_sp_s is varied, leading to a variation in $U_{surface}$, and consequently τ_{eff}. This dependency therefore provides a method to extract detailed interface properties from τ_{eff}-V_{surf} plots. An example of a τ_{eff}-V_{surf} plot obtained on an AlO_x-passivated p-Si is shown in Figure 4.4.2, with schematics of the interface states occupation depending on band-bending. By examining Equation (4.4.1), it is evident that $U_{surface}$ depends on the capture of the least available carrier near the Si surface. Under a net negative charge density, the band bend upwards, the minority carrier at the surface is electrons ($p_s \gg n_s$), resulting in a larger value of $(p_s+p_1)/S_n$ than $(n_s+n_1)/S_p$ in the denominator of Equation (4.4.1). As a result, $U_{surface}$ exhibits a stronger dependence on S_n than on S_p. Under strong upward band-bending, donor states at the valence band (VB) tail also participate in the recombination activity, as shown in Figure 4.4.2 (a). Due to the high defect density at band tails [149], the filling of band-tail states also affects field-effect passivation.

Similarly, at strong downward band-bending, as shown in Figure 4.4.2 (c), filling of the acceptor states at the conduction band (CB) tail strongly impact the overall $U_{surface}$. At minimal band-bending, $U_{surface}$ is primarily affected by recombination via states near the mid-gap. Therefore, by analysing and modelling the τ_{eff}-V_{surf} plots in detail, recombination at mid-gap and band tails can be distinguished. This methodology has only been recently proposed and only applied to limited cases [199], [225]. I adopt and improve the τ_{eff}-V_{surf} technique to elucidate the interface properties of $SiO_x/AlO_x/SiN_x$-passivated p-type Si surface, where a wet chemically grown SiO_x is present.

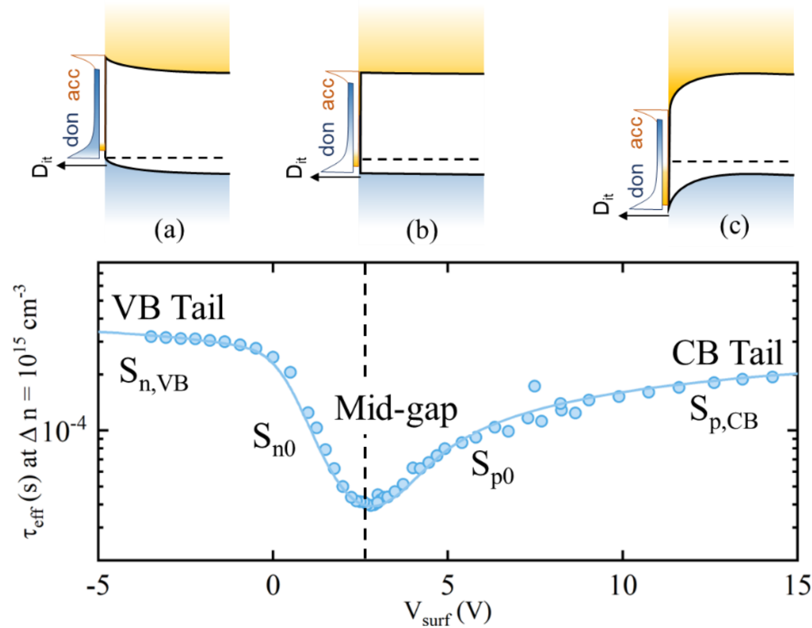


Figure 4.4.2 An exemplary τ_{eff}-V_{surf} plot of an AlO_x-passivated p-Si. (a) represents the condition under high negative surface charge, (b) represents zero net charge, and (c) represents the condition under high positive surface charge.

In the following analysis, S_{n0} and S_{p0} are used to quantify chemical passivation (as opposed to just D_{it}), as adopted in recent literatures [71], [207], [224], [226]. Carrier capture at band tails is represented by electron capture velocity at VB tail ($S_{n,VB}$) and hole capture velocity at CB tail ($S_{p,CB}$), respectively, while the impact of

electron capture at the CB tail ($S_{n,CB}$) and hole capture at the VB tail ($S_{p,VB}$) is negligible. Effective charge density (Q_{eff}) quantifies FEP, representing the total charge density in both shallow and deep traps.

To complement the extracted interface properties from τ_{eff}-V_{surf} plots, capacitance-voltage (C-V) measurements were carried out on sister samples for each of the passivation stack studied. However, it is noted that the C-V analysis formalism used, as described in Chapter 2, Section 2.4.4, does not take account of the charge fluctuations (σ_q) [151], [227], which also contribute to the "smearing-out" feature caused by an increase in D_{it}. Therefore, when fitting the obtained C-V curves, the D_{it} and $\sigma_{p/n}$ values across the bandgap are taken to be the same as extracted from the τ_{eff}-V_{surf} plots, while the Q_{eff} values are adjusted to find the best fit. The extracted S_{n0}, S_{p0}, and Q_{eff} from τ_{eff}-V_{surf} plots are shown in Figure 4.4.3. Q_{eff} extracted from C-V measurements are included in Figure 4.4.3 (c), represented by open symbols. The obtained C-V curves, the extracted Q_{eff} from each curve, and the parameters used for fittings are included in Appendix F.

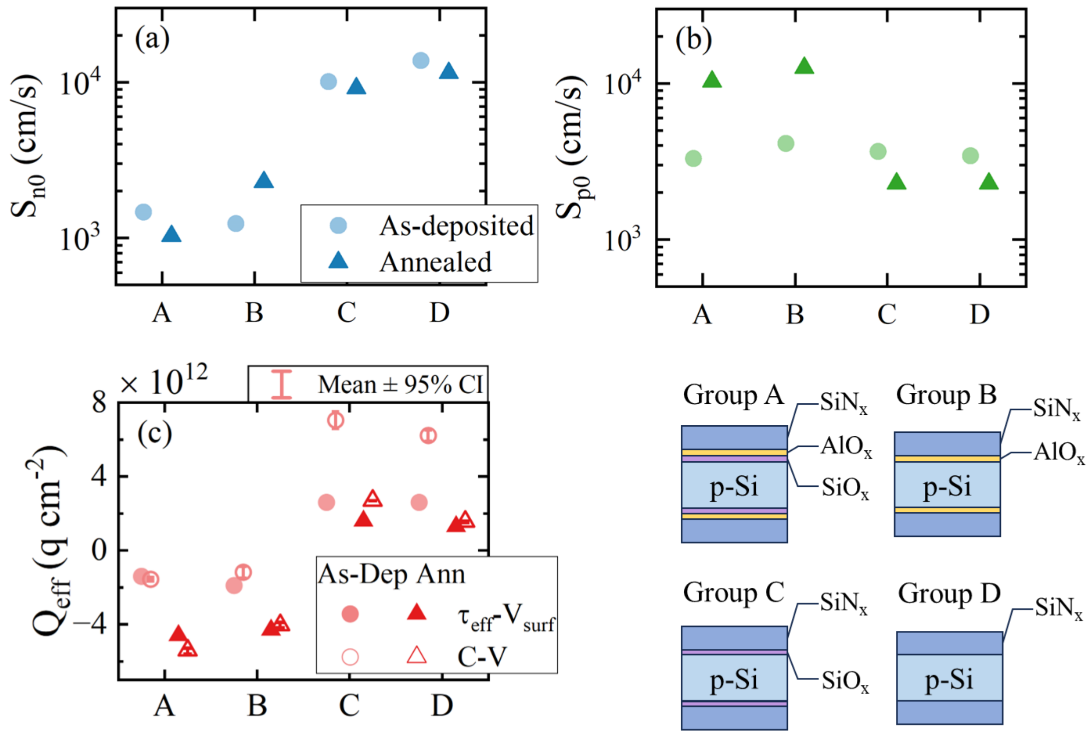


Figure 4.4.3 Extracted interface properties for Groups A, B, C, D as deposited (lighter circles) and after anneal (darker triangles) are shown in (a) S_{n0}; (b) S_{p0}; (c) Q_{eff} extracted from τ_{eff} - V_{surf} (solid symbols) and C-V (hollow symbols). The error bars represent the mean ± 95% CI obtained from 4-6 individual C-V measurements.

4.4.2 Discussion: Passivation upon Annealing

The effects of annealing for passivation stacks with an AlO_x layer (Groups A and B) are first discussed. An activation annealing at 450 °C has been widely reported to improve the passivation quality of AlO_x, partially attributed to the increased negative charge density [224]. Indeed, right shifts in τ_{eff}-V_{surf} plots of Groups A and B after annealing were observed in Figure 4.4.1, indicating an increased negative Q_{eff}. This is also supported by the extracted Q_{eff} values from both the τ_{eff}-V_{surf} and C-V measurements. A negative Q_{eff} of 4.2×10^{12} q/cm^2 was observed on Group A sample after annealing, which is comparable to the negative Q_{eff} of 5.3×10^{12} q/cm^2

obtained on n-type Si, as demonstrated in Section 4.2. Notably, both before and after annealing, the passivation was not limited by FEP, as indicated by the plateaued features at 0 V. Further increases in the negative Q_{eff} had minimal effects on τ_{eff}.

Changes in chemical passivation were also observed, as demonstrated by the shifts in τ_{eff} minima in Figure 4.4.2. An increased τ_{eff} minimum was observed for Group A, while a decreased τ_{eff} minimum was observed for Group B. Such changes are also reflected on the extracted S_{n0} values, as shown in Figure 4.4.3 (a), which play the dominant role in $U_{surface}$ in a p-Si with minimal band-bending. However, the changes in $S_{n/p0}$ were found to be insufficient to explain the improved τ_{eff} for both Groups A and B after annealing, particularly for Group B, where an increased $S_{n/p0}$ was observed after annealing.

It is therefore important to consider recombination via defects at the band tails. The determination of interface properties – interface state density (D_{it}) and carrier capture cross-sections ($\sigma_{p/n}$) – at the band tails is more complex than at the mid-gap. This is due to the higher D_{it} observed at the band tails due to the stretched Si-Si bonds [24], [228], and the strong impact of band-tail occupancy on FEP. Consider the case at the mid-gap. For a given S_{n0}, when σ_{n0} is lowered, $D_{it,mg}$ must be adjusted to a higher value. Due to the low values of $D_{it,mg}$ (~10^{11} cm^{-2}), this induces minimal change in FEP, allowing the final recombination rates $S_{n/p0}$ to remain nearly constant while still permitting the adjustment of $\sigma_{p/n,mg}$ and $D_{it,mg}$.

At the band tails, however, higher $D_{it,VB}$ and $D_{it,CB}$ (~10^{15} cm^{-2}) are present. At a given $S_{n,VB}$, when $\sigma_{n,VB}$ is lowered, the increase of $D_{it,VB}$ results in more charged donor states at the interface, consequently affecting FEP. Therefore, $D_{it,VB}$ needs to be further reduced to achieve the same $U_{surface}$, leading to a lower $S_{n,VB}$ value while maintaining the same fitting of experimental data. Conversely, at a high $\sigma_{n,VB}$, a slightly higher $D_{it,VB}$ (compared to the $S_{n,VB}$ divided by the original $D_{it,VB}$ value) is required, resulting in a higher $S_{n,VB}$ value.

To achieve a comprehensive representation of recombination at band tails, a fitting procedure is established via a confidence interval containing a collection of parameter values that can fit the experimental data to a minimum MSE. The workflow is as follows:

(1) $\sigma_{p,VB}$ and $\sigma_{n,CB}$ are fixed at 10^{-17} cm^{-2}, while $\sigma_{p,CB}$ is kept at 5×10^{-17} cm^{-2}.

(2) $\sigma_{n,VB}$ is set to 10^{-17} cm^{-2}, while $D_{it,VB}$ and $D_{it,CB}$ are varied to achieve a MSE within 10% of the minimum MSE.

(3) $\sigma_{n,VB}$ is then set to 8×10^{-17} cm^{-2}, while $D_{it,VB}$ and $D_{it,CB}$ are varied to achieve a MSE within 10% of the minimum MSE.

(4) Repeat (2) and (3) with $\sigma_{p,VB}$ and $\sigma_{n,CB}$ fixed at 10^{-18} cm^{-2}, while $\sigma_{p,CB}$ is kept at 5×10^{-17} cm^{-2}.

The confidence interval of $S_{n,VB}$ is determined by the values obtained in steps (2), (3) and (4). For determine the confidence interval for $S_{p,CB}$, $\sigma_{n,VB}$ is fixed at 5×10^{-17} cm^{-2} while $\sigma_{p,CB}$ is varied between 1 and 8×10^{-17} cm^{-2}, with both $\sigma_{p,VB}$ and $\sigma_{n,CB}$ fixed at 10^{-17} or 10^{-18} cm^{-2}. Simultaneously, $D_{it,VB}$ and $D_{it,CB}$ are adjusted

to maintain a MSE within 10% of the minimum MSE. The extracted $S_{n,VB}$ and $S_{p,CB}$ values for Groups A-D before and after annealing are plotted in Figure 4.4.4.

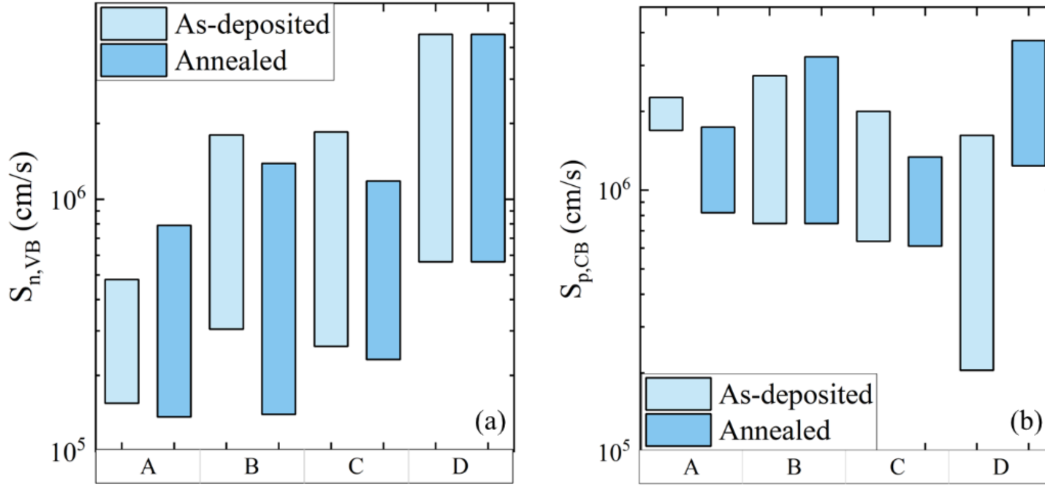


Figure 4.4.4 Extracted values of (a) $S_{n,VB}$ and (b) (a) $S_{p,CB}$ for Groups A, B, C, D before and after an annealing at 450 °C for 10 minutes.

For Groups A and B, where a high density of negative Q_{eff} is present, recombination is dominated by $S_{n,VB}$. Despite of the large ranges, a reduction of $S_{n,VB}$ was observed for Groups A and B after annealing, which is proposed to attribute to an improved chemical passivation after annealing. This impact of band-tail states is often underestimated when evaluating D_{it} using C-V measurements, where the focus is typically on the extraction of $D_{it,mg}$, while neglecting the contributions from band tails [37], [229], [230]. However, since most of the studied passivation layers exhibit strong FEP, recombination at band tails plays a crucial role and should not be overlooked [149]. Overall, it is concluded that the effective passivation of Groups A and B after annealing results from increased negative Q_{eff} and a decreased $S_{n,VB}$.

Next, the effects of annealing on passivation stacks without an AlO_x layer (Groups C and D) is considered. A deterioration of passivation was observed after annealing for both groups. This is mainly attributed to a reduction in positive Q_{eff}, as evidenced by the left shifts of the τ_{eff}-V_{surf} plots shown in Figure 4.4.1, and the extracted values in Figure 4.4.3 (c). The discrepancy between the Q_{eff} extracted from τ_{eff}-V_{surf} plots and C-V measurements is attributed to the charging of shallow states during C-V measurements, particularly in as-deposited samples where these states are more abundant [231], [232]. Such sa reduction in FEP has also been reported by Sharma et al. [27] and De Wolf et al. [26], and has been attributed to hydrogen passivation of K^+ centres or the de-passivation of K^- centres. Considering the observed decrease in both S_{n0} and S_{p0} following annealing, it is most likely that the passivation of K^+ centres by H^+ is the dominant mechanism responsible for the reduced positive Q_{eff} in the studied samples.

The additional NAOS-SiO_x layer was also found to improve passivation, evidenced by the lower S_{eff} and J_{0s} obtained on Groups A and C, compared to Groups B and D, as shown in Figure 4.3.2. Such improvement is also attributed to reduced recombination at band-tail states, as indicated by the lower $S_{n,VB}$ values observed

on Groups A and C, comparing to Group B and D, respectively, both before and after the activation annealing. Both the activation annealing and the purposely grown NAOS-SiO_x layer was found to improve $S_{n,VB}$, which is related to the reduction of extrinsic Si-O dangling bonds [24]. Meanwhile, a lower value of $S_{p,CB}$ was also observed on Group C compared to Group D after annealing, likely contributing to the improved surface recombination parameters.

4.4.3 Discussion: Signature of AlO_x-passivated Interface

Upon examination of the extracted $S_{n/p0}$ values in Figure 4.4.3 (a) and (b), a key trend emerges. A S_{n0}/S_{p0}<1 was obtained at AlO_x-passivated interface (Groups A and B), while S_{n0}/S_{p0}~10 was obtained at SiN_x-passivated interface (Groups C and D), both before and after annealing. S_{n0}/S_{p0} is reflected in the ratio of the slopes of the electron-dominated (left half) and the hole-dominated (right half) of the τ_{eff}-V_{surf} plots. In Figure 4.4.1 it is apparent that a right-tilting of the τ_{eff}-V_{surf} relationship near the minimum occurs for Groups A and B, while a left-tilting was observed for Groups C and D. The high S_{n0}/S_{p0} value for SiN_x-passivated interface has been well documented, attributing to a high σ_n/σ_p ratio of the defects at the Si/SiO_x or Si/SiN_x interface [31], [233]. Meanwhile, although right-tilting in the τ_{eff}-V_{surf} plots in AlO_x-passivated interfaces has also been observed previously [199], its underlying mechanism remains unclear.

The low S_{n0}/S_{p0} value observed at AlO_x-passivated interfaces is proposed to result from two separate processes, each leading a decrease in S_{n0} and an increase in S_{p0}. This hypothesis is supported by the observation that, before activation annealing, S_{p0} in Groups A and B was comparable to that in Groups C and D. An increase in S_{p0} was observed only in annealed samples, whereas a lower S_{n0} was present both before and after annealing, indicating two distinct processes with different activation energies. A lower energy is required for the reduction of S_{n0} and is proposed to be a hydrogen-related process. Hydrogen has been demonstrated to migrate quickly through SiO_2 with passivation being primarily rection-limited [206], [234]. Therefore, it is likely that the thermal budget during fabrication (350 °C for 30 minutes during PECVD) provided sufficient energy for H in AlO_x to migrate towards the Si-SiO_x interface and passivate the dangling bonds.

Considering the vast availability of H in SiN_x films, the added hydrogen content from 30 cycles of AlO_x is unlikely to be the sole reason for the 10x reduction of S_{n0} [206], [219]. An electrostatic effect where the charge states of H are changed under AlO_x is proposed, which has been introduced in Section 4.2, where an improved chemical passivation was observed with merely 10 cycles of AlO_x. Here, it is further demonstrated that such improvements could originate from the reduction of S_{n0} due to passivation of donor states by H^-. The increased H^- species could arise from the change in the electrostatic field in AlO_x, which was partially activated under thermal budget during PECVD, as shown by the negative Q_{eff} of Groups A and B, before activation annealing.

Lastly, the increase in S_{p0} after annealing is discussed. One explanation involves the change in interface structure. During activation annealing, Al atoms have been shown to diffuse towards the Si/SiO_2 interface [50], [189]. Such intermixing of AlO_x and SiO_x layer give rise to the negative fixed charges by creating new acceptor

states below the Si VB minimum [51]. Due to variations in the local bonding configurations, these defect states can span over a range of energies [24] and extend into the Si bandgap, contributing to an increase in S_{p0} after annealing. The presence of such in-gap acceptor states has also been suggested in previous reports [46], [199].

In conclusion, the distinctly low S_{n0}/S_{p0} ratio observed at AlO_x-passivated interfaces has been attributed to the formation of new acceptor states at the interface. These acceptor states are likely to have a span of energy levels. Defects with energy levels lower than the VB minimum of Si capture electrons and give rise to a fixed negative charge density, altering the charged state of hydrogen and lead to a reduction in S_{n0}. Meanwhile, acceptor states with energy levels within the Si bandgap contribute to recombination, increasing S_{p0}.

4.5 Atomic-scale Characterisation of the Si/Dielectric Interface

To study how the observed changes in passivation quality link to structural changes at the Si/dielectric interface, scanning transmission electron microscopy (STEM) and electron energy loss spectroscopy (EELS) was performed. A p-type FZ Si substrate with a resistivity of 1 Ω·cm (Set 4) was symmetrically passivated by the optimised $SiO_x/AlO_x/SiN_x$ nanolayer stack. An activation annealing at 450 °C for 10 minutes was performed. The sample was prepared as described in Chapter 2, Section 2.4.8. To study the electron loss near edge structure (ELNES), an energy loss ranges up to 570 eV was used to study the L-edges of Al and Si and K-edges of O and N. Reference spectra for Si and Si-N_x was obtained from the bulk region of the sample and then used to identify different bonding environments of Si.

The annular dark-field (ADF) transmission micrograph of the p-Si/$SiO_x/AlO_x/SiN_x$ structure is shown in Figure 4.5.1 (a). I note here that the experimental design, the microscopy requirements, and part of the sample preparation and data analysis were conducted by myself. The hands-on TEM operation was conducted by Prof Sergio Lozano, Dr Guanze He and Dr Anastasia Soeriyadi, to whom I am kindly thankful. Atomic-resolution imaging was not achieved because the accelerating voltage was limited to 80 kV to mitigate beam-induced damage. At higher voltages, higher-resolution images can be obtained, but this consistently led to the formation of pinholes near the interface. Preliminary trials with a cryogenic stage indicated that cooling is necessary to suppress damage and would permit operation at higher accelerating voltage; however, a systematic cryo-TEM was not feasible within the available microscope time.

Elemental maps and depth profiles were obtained from EELS analysis within the region highlighted by the red rectangle and shown in Figure 4.5.1 (b) and (c), respectively. The depth profile reveals a ~ 2.5 nm Al:SiO_xN_y layer with an average elemental ratio of Al:Si:O:N of 1:2.5:8.1:1.3. The high concentration of oxygen suggests the formation of interstitial oxygen defects, which are known to give rise to deep acceptor states [235]. Additionally, a ~0.8 nm SiO_x and ~1.2 nm SiO_xN_y layer were identified between Si and SiN_x. The formation of these interlayers is likely attributed to the thermal budget during deposition and activation annealing. Notably, while no pure AlO_x was detected, a significant negative charge density of 4-5 × 10^{12} q/cm^2 was observed, indicating that most of the defects responsible for the fixed charge reside near the interface to Si.

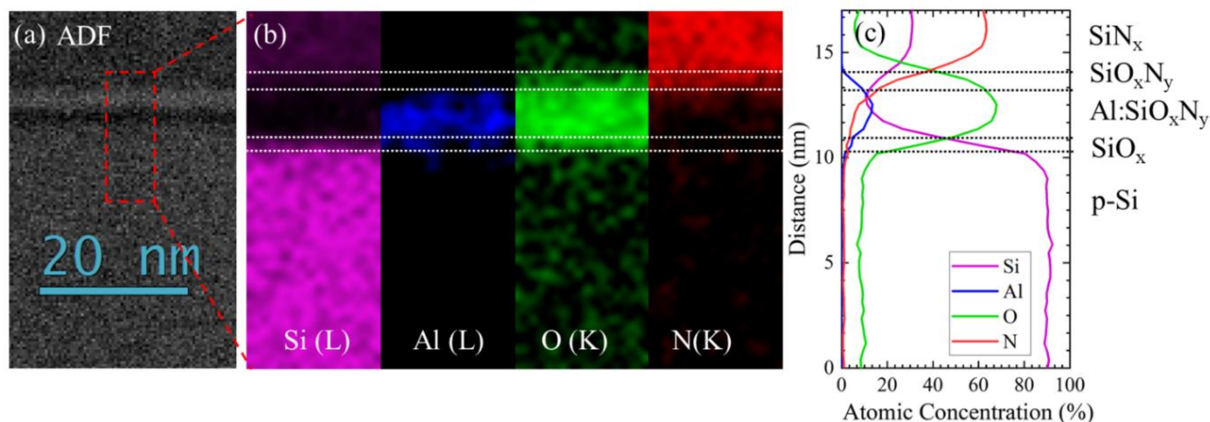


Figure 4.5.1 (a) ADF image of a p-Si passivated by the optimised $SiO_x/AlO_x/SiN_x$ after an activation anneal. EELS analysis was carried out in the red rectangle region to obtain (b) elemental maps and (c) depth profiles of Si, Al, O and N averaged over the marked area.

The ELNES from the highlighted area in Figure 4.5.1 (a) is shown in Figure 4.5.2 (a) and (b). Each spectra integrates all horizontal pixels in the highlighted area, with 4 Å between each horizontal line. Peaks between 76.2 eV and 79 eV correspond to the Al $L_{2,3}$ edge in amorphous AlO_x (a-AlO_x), reflecting different Al coordination. Literature reports lower energy losses (76.5~78.2 eV) for tetrahedral Al and higher (79.3~80 eV) for octahedral Al [50], [236], [237]. Tetrahedral Al, often found to be more predominant close to the interface to Si, has been reported to be related to the formation of negative charge [50]. However, only a mixture of tetrahedral and octahedral coordinated Al can be identified in Figure 4.5.2.

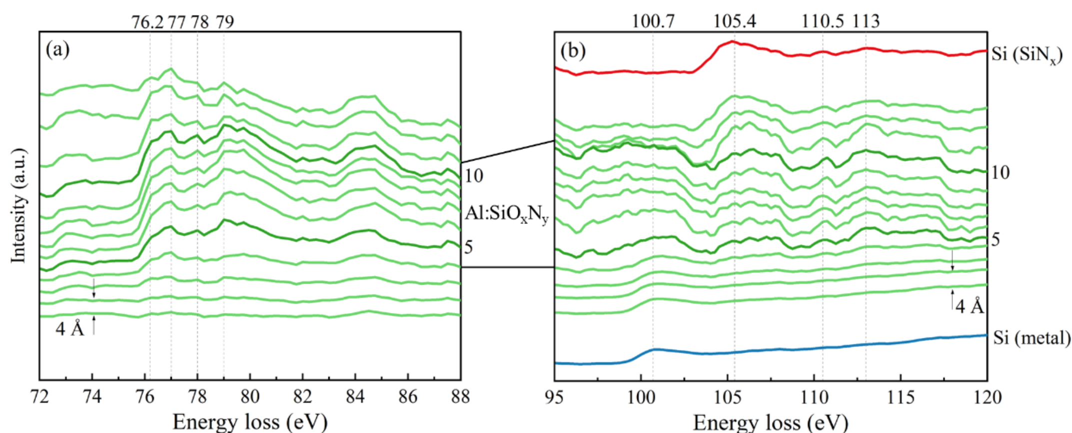


Figure 4.5.2 STEM-EELS spectra measurement showing (a) Al $L_{2,3}$-edge and (b) Si L-edge with the peaks identified. The distance between each green spectrum is 4 Å. The darker green colour marks the fifth and the tenth spectra counting from the first spectra on the bottom (Si side), also indicated by the numbers on the right. The blue and red spectra are reference spectra obtained in bulk region of Si and SiN_x ~ 4 and 2.7 nm from the interfaces.

Figure 4.5.2 (b) presents the measured spectra for the Si $L_{2,3}$-edge, including reference spectra of Si (metal) and Si (SiN_x) to illustrate the changes in fine structures throughout the film. A distinct peak at 100.7 eV was identified for Si (metal). Moving deeper into the dielectric film, a rightward shift in the peak and arises of additional peaks at 105.4, 110.5 and 113 eV were observed, indicating changes in the chemical environment of Si. The peak at 105.4 eV is likely related to Si-N bond as it coincides with the SiN_x reference spectra [238].

Peaks at 110.5 and 113 eV could be identified as Si-O bond as shown in [239]. The emergence of Si-O and Si-N bonds were detected at the same depth as the Al species, which suggests a mixed layer of Al:SiO_xN_y. The presence of this mixed layer, along with the excess oxygen identified in the elemental profile shown in Figure 4.5.1 (c), likely contributes to the fixed negative charge and increased S_{p0} after annealing discussed in Section 4.4.3.

4.6 Summary

This chapter presents the application of an ultra-thin AlO_x layer (~2.5 nm) for passivating p-type Si in high-performance solar cells. Beyond a high negative charge density, additional aspects such as interface state density (chemical passivation), optical properties, and processing cost were considered in the design of the nanolayer stack. The optimised $SiO_x/AlO_x/SiN_x$ structure, incorporating a low-temperature wet-chemically grown SiO_x layer, demonstrated effective passivation for both n and p-type Si, achieving low S_{eff} values of 3.3 and 6.3 cm/s, respectively. This is comparable to that achieved using thick >10 nm AlO_x layer while significantly reducing processing time.

A detailed analysis of the Si/dielectric interface was conducted to elucidate the passivation mechanisms of the optimised $SiO_x/AlO_x/SiN_x$ nanolayer stack. By examining variations in τ_{eff} with surface carrier densities (τ_{eff}-V_{surf} plots), recombination at mid-gap and band tail states was extracted. A set of parameters including $S_{n/p0}$ and Q_{eff} from τ_{eff}-V_{surf} and C-V measurements are selected to best represent the chemical and field-effect passivation across different nanolayer stacks.

The role of recombination at band tail states was highlighted, particularly at interfaces exhibiting strong band bending common in solar cells. The enhanced passivation observed at the AlO_x-passivated interface was attributed to a combination of increased negative Q_{eff} and reduced electron capture velocity at the valence band tail ($S_{n,VB}$). Improved chemical passivation, provided by the intentionally grown SiO_x layer, was also linked to a reduction of $S_{n,VB}$, associated with a lower density of extrinsic Si-O dangling bonds at the interface. Additionally, a low S_{n0}/S_{p0} ratio of less than 1 was observed at AlO_x-passivated interfaces, in contrast to the ~10 observed at SiN_x-passivated interfaces. Such signature low S_{n0}/S_{p0} ratio at AlO_x-passivated interfaces is proposed to originate from the intermixing of the interfacial SiO_x layer with the AlO_x layer, introducing new acceptor states near the interface. It is likely that such acceptor states have energy levels that span over a range. Acceptor states with deep energy levels contribute to the fixed negative charge density and an increased H^- density, leading to a reduction of S_{n0}. Meanwhile, acceptor states with energy levels within the Si bandgap assist recombination, increasing S_{p0}. These findings suggest an intrinsic link between chemical and field-effect passivation, which have so far considered independent mechanisms.

Finally, the elemental distribution and bonding configurations at the Si/dielectric interface were investigated using TEM and EELS on p-Si passivated by the optimised $SiO_x/AlO_x/SiN_x$ nanolayer stack. An Al:SiO_xN_y interfacial layer with high oxygen content and a mix of tetrahedral and octahedral coordinated Al was identified. This interfacial composition likely accounts for the observed changes in passivation after

annealing, further supporting the intrinsic link between chemical and field-effect passivation. The insights gained in this chapter on improving surface passivation provide a foundation for further optimisation of ultra-thin AlO_x layers for application in TOPCon solar cells, and the future improvement of solar cell devices.

Chapter 5
Field Induced Tailoring of $SiO_x/AlO_x/SiN_x$ Surface Passivation

5.1 Introduction to Field-Assisted Passivation

Recombination at the Si/dielectric interface can be minimised by jointly optimising chemical and field-effect passivation. While both mechanisms depend on the fabrication and temperature treatment processes of thin film dielectrics, recent reports show that an external electric field can drastically change the resulting passivation [225]. Field-effect passivation has been shown to improve with the application of external voltages, leading to an increase in negative charge density in AlO_x by more than 1×10^{13} q cm^{-2} upon the application of a positive voltage [240]. This suggests the potential for using an external electric field to tune or enhance FEP. However, these changes in the charge density are thought to stem from shallow trap states and are thus unstable [56]. An in-depth investigation is needed to understand the mechanisms and limits of external electric fields in controlling and enhancing dielectric fixed charges and, therefore, their potential to improve device performance. Such understanding complements current efforts in optimising the fabrication processes and dielectric stack design for advanced solar cell architectures [199], [241]. This is particularly important for ultra-thin AlO_x (<2 nm), where charge density remains limited despite optimisation of fabrication processes [41].

While the effects of electric field on FEP have been widely studied, its impact on chemical passivation remains largely unexplored. Hydrogenation is a well-established technique for improving chemical passivation both at the surface and in the bulk of semiconductors. High hydrogen concentrations in SiN_x (10-15 at%) [242] and AlO_x (3-4 at%) [220] near the interface have been experimentally observed through secondary ion mass spectrometry (SIMS) [243], [244], [245], atom probe tomography (APT) [244], [246], and elastic recoil detection analysis (ERDA).[247] Density functional theory (DFT) calculations suggest that hydrogen exists in different charge states (H^0, H^+, H^-), depending on the Fermi level alignment relative to the donor or acceptor level of hydrogen [48], [248]. Given its charged nature, external electric fields have been used to tune hydrogen migration and further optimise chemical passivation [225]. However, previous studies have focused on high-quality thermal oxide (>10 nm) combined with SiN_x; while low-temperature thin oxides have not been studied yet, although they are favoured for increased throughput and lower production costs [20]. Moreover, the hydrogen passivation mechanism in AlO_x/SiN_x stacks remains unclear, with some reports indicating that

hydrogen from AlO_x plays a dominant role in passivation in AlO_x/SiN_x stacks, despite the higher hydrogen concentration in SiN_x [206], [249], [250].

In this chapter, the potential of field-assisted annealing to enhance passivation of the $SiO_x/AlO_x/SiN_x$ nanolayer stack in Chapter 4 is evaluated. Corona discharge is used to establish a temporary electric field during annealing, and the resulting changes in interface properties are assessed by measuring effective minority lifetime as a function of surface voltage (τ_{eff}-V_{surf}), complemented by capacitance-voltage measurements. To fully understand the interface dynamics during annealing under electric fields, a SiO_x/SiN_x structure is also studied. A comprehensive model is proposed based on experimental findings.

5.2 Passivation Tailoring via Surface Electric Fields

The $SiO_x/AlO_x/SiN_x$ nanolayer stack, as optimised in Chapter 4, was symmetrically deposited on quarter-sized p-type Cz Si samples with a resistivity of 10-20 Ω·cm (Set 3). The SiO_x layer was formed wet chemically using nitric acid and 30 cycles of AlO_x were deposited using the Anric ALD. PECVD-SiN_x films of ~60 nm was deposited on both sides of the samples. Details of the film deposition process is described in Chapter 2, Section 2.2 and Appendix B. As-deposited samples were first annealed at 450 °C for 10 minutes to activate the intermixing of the SiO_x and AlO_x layers, giving rise to an improved passivation, as demonstrated in Chapter 4. Three different groups were used for surface passivation studies: (1) annealed, with no further processing; (2) annealed, followed by a positive corona-anneal (+ C-A); (3) annealed, followed by a negative corona-anneal (– C-A).

Each corona-anneal process comprises a positive/negative corona charge deposition of 90 seconds at room temperature on both sides of the sample, followed by an annealing at 450 °C for 30 seconds. The short annealing was found sufficient to remove the surface charge, as validated by the measurements of surface photovoltage (SPV). The SPV results are included in Appendix G. Effective lifetime was measured after the different annealing treatments.

A comparison of the injection level-dependent τ_{eff} for samples after an activation anneal, +C-A, or -C-A processes are shown in Figure 5.2.1, including a theoretical calculation of the surface recombination velocity (S_{eff}) and the surface recombination current density (J_{0s}), following Kimmerle's formalism [72]. The extracted J_{0s} at low injection levels are excluded from extraction due to the high noise-to-signal ratio in the measured τ_{eff} in this regime. Compared to the sample without additional corona-anneals, the sample with a +C-A demonstrated a reduction in S_{eff} from 6.9 cm/s to 5.5 cm/s, while the sample with a -C-A exhibited an increase to 39.4 cm/s. A J_{0s} below 45.3 fA/cm^2 was obtained on the sample with a +C-A, which was achieved by a low-temperature oxidised SiO_x and ~2.5 nm AlO_x.

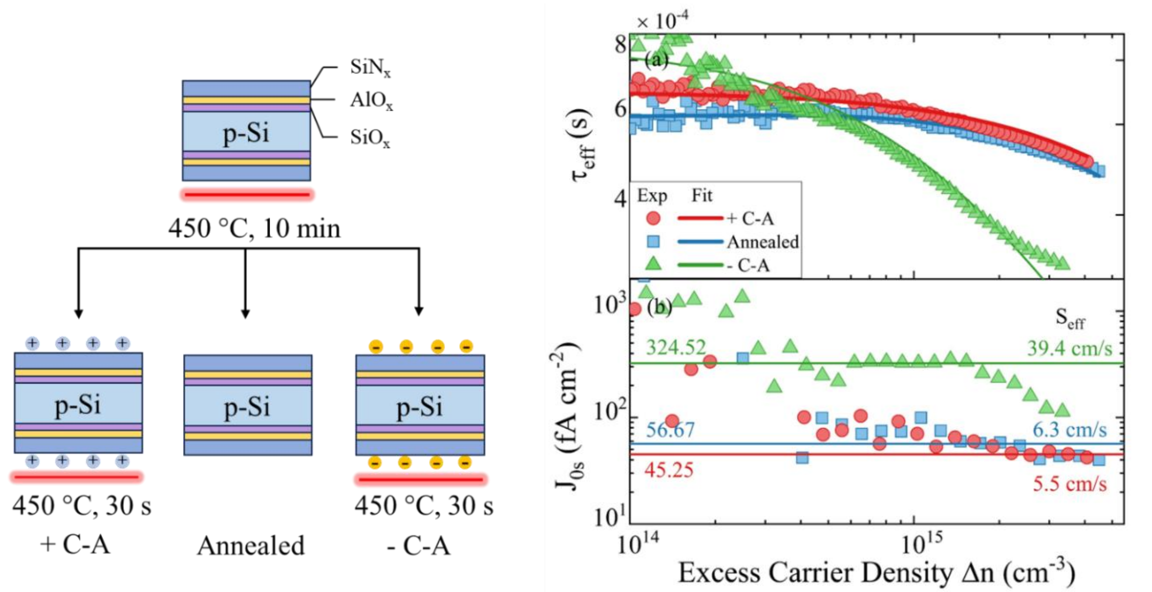


Figure 5.2.1 Extraction of recombination parameters. (a) Measured injection-dependent effective lifetime of $SiO_x/AlO_x/SiN_x$ passivated p-type Si after annealing, + C-A and – C-A. Solid lines indicate the best fit to extract (b) J_{0s} and S_{eff}.

To further investigate how changes in the interface properties influenced the observed variations in passivation quality, τ_{eff} was monitored as function of an external voltage applied by transparent electrodes (PEDOT:PSS) on both surfaces. To ensure consistency, the τ_{eff}-V_{surf} plots were obtained following two steps:

(1) V_{surf} was set to 0 V, and a positive sweep was performed.
(2) V_{surf} was set back to 0 V again, and a negative sweep was performed.

The resulting τ_{eff}-V_{surf} plots of samples with different annealing treatments are shown in Figure 5.2.2. Step (1) and (2) were repeated for multiple times, represented by the different shades of colour symbols. The solid lines represent the theoretical fitting using an extended Shockley-Read-Hall model considering all data points obtained [149], as described in Chapter 2, Section 2.4.3. The parameters used to best fit the experimental data are included in Appendix E.

Distinctly different τ_{eff}-V_{surf} plots were observed for samples passivated with $SiO_x/AlO_x/SiN_x$ nanolayer stacks subjected to different annealing treatments. The origin of the variations in passivation quality is first discussed qualitatively. X-axis shifts in the τ_{eff} minima indicate changes in the negative Q_{eff}. However, variations in field-effect passivation are unlikely to account for the changed passivation quality, as evidenced by the minimal increase in τ_{eff} with the application of a negative V_{surf} for all samples. Meanwhile, chemical passivation – commonly inferred from the minimum τ_{eff} – is also found to be insufficient to fully explain the observed changes in passivation quality. This is due to the significant increase in S_{eff} and J_0, despite the sample with a -C-A process exhibiting a higher minimum τ_{eff}. It is proposed that the primary factor driving the passivation changes on samples annealed under different electric field is an altered recombination in the tail states.

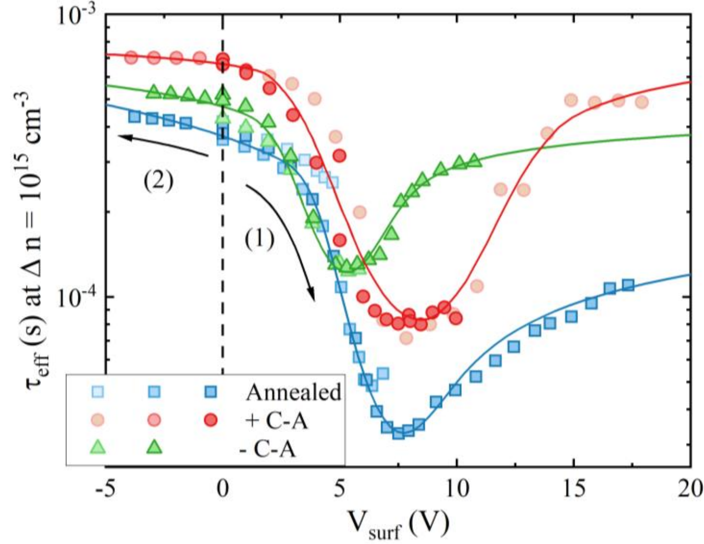


Figure 5.2.2 Effective lifetime as a function of surface voltage for $SiO_x/AlO_x/SiN_x$-passivated p-type Si via the PEDOT:PSS as transparent electrodes with different post-deposition treatment. Solid lines indicate model fittings using energy dependent parameterisation.

Following the previously developed fitting process (Chapter 4, Section 4.3.2), the confidence interval of electron capture velocity at the valence band tail ($S_{n,VB}$) and hole capture velocity at the conduction band tail ($S_{p,CB}$) are extracted and plotted in Figure 5.2.3. For the $SiO_x/AlO_x/SiN_x$ nanolayer studied in this work, the recombination rate is dominated by $S_{n,VB}$ due to a strong upward band-bending in the presence of a negative Q_{eff}. Despite the large confidence interval, the sample with -C-A showed a slight increase in $S_{n,VB}$, while the sample with +C-A exhibited a slight decrease, compared to the annealed sample. This corresponds to the $\tau_{eff,max}$-$\tau_{eff,min}$ values of the electron-dominated half (left half) of the τ_{eff}-V_{surf} plots, which was smaller for the sample with a -C-A, contributing to a worsen passivation despite of the high τ_{eff} minimum obtained. While $S_{p,CB}$ does not significantly contribute to recombination at high negative charge density, its decrease in both +C-A and -C-A samples is reflected in the larger $\tau_{eff,max}$-$\tau_{eff,min}$ values of the hole-dominated half (right half). The alignment between extracted $S_{p,VB}$ values and variations in the shape of the τ_{eff}-V_{surf} plots further supports the reliability of the extracted interface properties at band tails. It is concluded that the observed changes in surface recombination parameters on $SiO_x/AlO_x/SiN_x$-passivated samples are attributed to changes in $S_{n,VB}$. Such changes in carrier capture velocities in the band tails could arise from the passivation or de-passivation of Si-O dangling bonds [24].

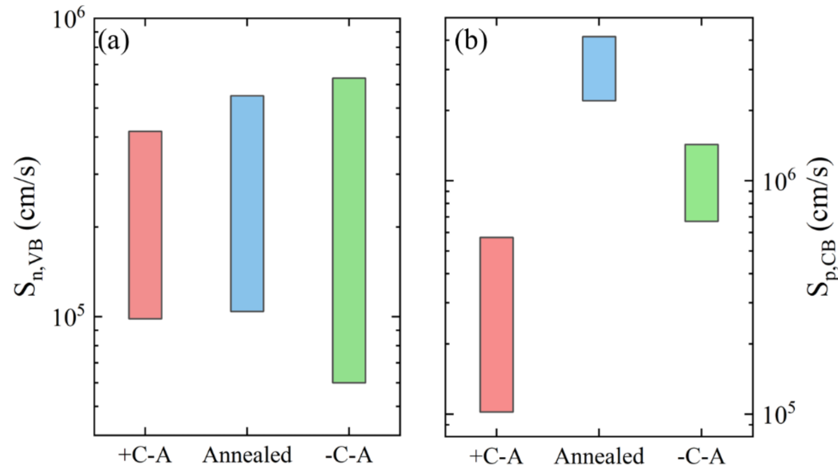


Figure 5.2.3 Extracted confidence interval of (a) $S_{n,VB}$ and (b) $S_{p,CB}$ on $SiO_x/AlO_x/SiN_x$-passivated samples with different annealing treatments.

5.3 Understanding Interface Properties

5.3.1 Field Induced Interface Modification in $SiO_x/AlO_x/SiN_x$ Nanolayers

Interface dynamics during annealing under electric fields are further investigated. Electron and hole capture velocities at mid-gap ($S_{n/p0}$) and effective charge density (Q_{eff}) were extracted from the τ_{eff}-V_{surf} plots and shown in Figure 5.3.1. To complement the extracted values, Q_{eff} was independently obtained from C-V measurements, and the extracted values are included in Figure 5.3.1. The measured C-V curves and numerical values are included in Appendix F.

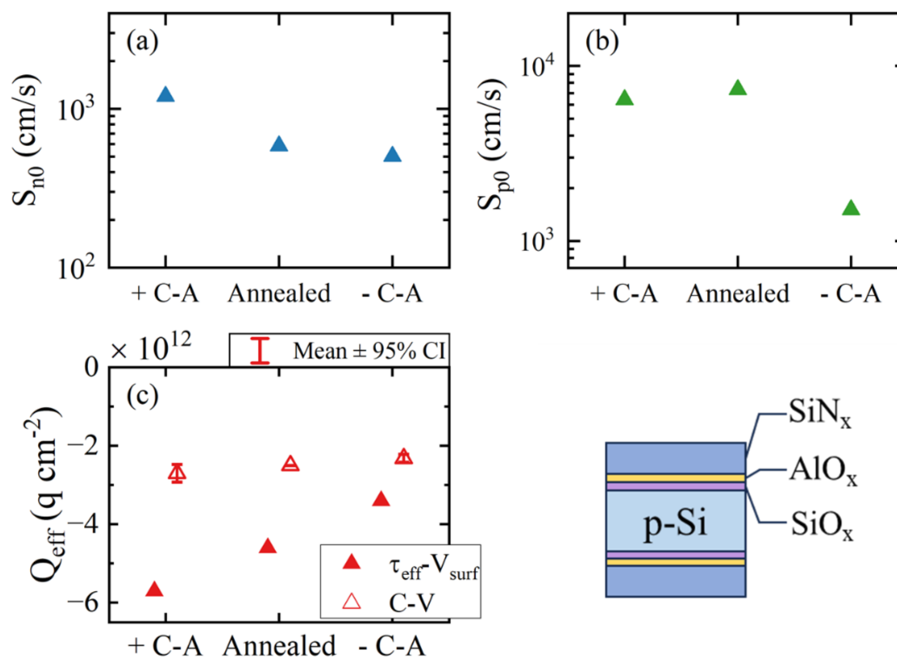


Figure 5.3.1 Extracted interface properties for $SiO_x/AlO_x/SiN_x$-passivated samples annealed under different electric fields are shown in (a) S_{n0}, (b) S_{p0}, and (c) Q_{eff}. The error bars represent the mean ± 95% CI of the four to six individual C-V measurements taken.

The effects of corona-anneals on the chemical passivation of $SiO_x/AlO_x/SiN_x$ nanolayer stack are first assessed. A decrease in both S_{n0} and S_{p0} was observed after -C-A, aligning with the observed increase in the minimum τ_{eff}. Meanwhile, after +C-A, S_{n0} increased while S_{p0} decreased, which is consistent with the less prominent increase in the τ_{eff} minima, as shown in Figure 5.2.2.

Considering the low thermal budget during the corona-anneal process (450 °C for 30 seconds), structural change at the interface is likely to be minimal [224]. A hydrogen-related mechanism is proposed, stemming from the response of charged hydrogen under the applied electric fields [225]. Schematics illustrating the proposed interface dynamics under corona-anneals are shown in Figure 5.3.2. As discussed in Chapter 4, a high density of negative Q_{eff} is present in the $SiO_x/AlO_x/SiN_x$ nanolayer after annealing, attributed to the negatively charged acceptor states in the Al:SiO_x layer, as shown in Figure 5.3.2 (a). Under a positive electric field, electrons with excess energy are injected from Si to the interface, breaking the bonds between donor states and H^- [251], [252]. Under the electric field, H^- migrates away from the interface, leading to an increased S_{n0}, while H^+ migrates towards the interface, leading to a decreased S_{p0}, as shown in Figure 5.3.2 (b). A similar process is likely to occur under a negative surface charge, where acceptor states are de-passivated due to hot hole injection. However, the abundance of H^+ in p-Si migrating towards the interface under the applied electric field produces a decrease in S_{p0}, as shown in Figure 5.3.2 (c).

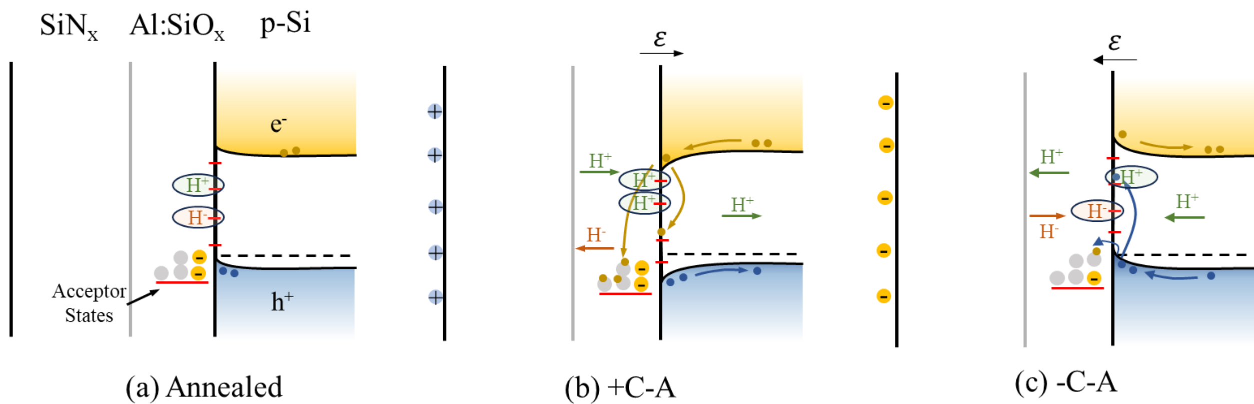


Figure 5.3.2 Schematics demonstrating the carrier injection and hydrogen migration process under surface electric fields corresponding to the sample (a) with an activation annealing, (b) during +C-A, and (c) during -C-A.

Changes in FEP were also observed after annealing under different electric fields, as evidenced by the right shifts in τ_{eff} minima in Figure 5.2.2. An increase of 1×10^{12} q cm^{-2} and a decrease of 1.3×10^{12} q cm^{-2} were revealed after +C-A and –C-A processes, respectively. This observation is further supported by C-V measurements, represented by the open symbols in Figure 5.3.1 (c). The smaller values of negative Q_{eff} extracted from C-V, compared to τ_{eff}-V_{surf} measurements, could be explained by film non-uniformities. Samples used to conduct C-V measurements could have a thinner AlO_x layer, which results in reductions in the negative Q_{eff} [18], [241].

The observed changes in the negative Q_{eff} are proposed to also arise from carrier injection from Si to the interface. An electric field is established at the Si/dielectric interface with the application with of a

positive/negative electric field, which lead to electron/hole injection to trap states near the interface, resulting in an increased/decreased negative Q_{eff}. These processes are demonstrated in Figure 5.3.2 (b) and (c), respectively. While similar observations have been reported previously [199], the stability of such trapped charges at elevated temperatures has not been demonstrated. In this work, an increased negative Q_{eff} was demonstrated after annealing at 450 °C under positive surface charge. This is particularly significant as it highlights an extrinsic strategy to enhance field-effect passivation in ultra-thin AlO_x, which remains a limiting factor for higher efficiency TOPCon devices [185], [201], [204]. Furthermore, it is pointed out that changes in both chemical and field-effect passivation are likely driven by carrier injection at the interface, indicating an intrinsic link between these two mechanisms, which are typically considered independently.

5.3.2 Field Induced Interface Modification in SiO_x/SiN_x Nanolayers

To further validate the proposed interface dynamics, changes in the interface properties of a SiO_x/SiN_x passivation nanolayer (without AlO_x) were studied after annealing under electric fields. Three samples were fabricated, where the SiO_x layers were formed via wet-chemical nitric acid growth. In obtaining the τ_{eff}-V_{surf} plots, significant hysteresis was observed. To ensure consistency, the τ_{eff}-V_{surf} plots were obtained in three steps:

(1) V_{surf} was set to 0 V, and a positive sweep was performed.
(2) V_{surf} was set back to 0 V again, and a negative sweep was performed.
(3) V_{surf} was kept at high negative voltage and a sweep from negative to positive V_{surf} was performed to investigate hysteresis.

The obtained τ_{eff}-V_{surf} plots from step (1) and (2) are shown in Figure 5.3.3 (a), while data collected in step (3) is shown in Figure 5.3.3 (b). The theoretical fittings of the experimental data are indicated by the solid lines. The extracted $S_{n/p0}$ and Q_{eff} are shown in Figure 5.3.3 (c)-(e). To complement the τ_{eff}-V_{surf} plots, Q_{eff} was independently obtained from C-V measurements, represented by the open symbols in Figure 5.3.3 (e). The measured C-V curves and numerical values are included in Appendix F.

Distinct τ_{eff}-V_{surf} plots were obtained in SiO_x/SiN_x-passivated samples after annealing under different electric fields. First, changes in chemical passivation at mid-gap are discussed. Compared to the interfaces passivated by $SiO_x/AlO_x/SiN_x$, higher S_{n0} and lower S_{p0} values were obtained. This aligns with the finding in Chapter 4, where a σ_n/σ_p ratio of less than 1 was observed at AlO_x-passivated interfaces, while a ratio of ~10 was observed at SiN_x-passivated interfaces, indicating distinct interface defects. Despite of the distinctively different interfaces, similar changes in S_{n0} and S_{p0} were observed. For S_{p0}, an increase was observed after +C-A, while a decrease was observed after -C-A. Decreased S_{n0} values were observed after both +C-A and -C-A. These results further support the previous hypothesis that changes in chemical passivation are primarily driven by a hydrogen-related process, which is abundant in both passivation stacks due to the hydrogenated SiN_x layer.

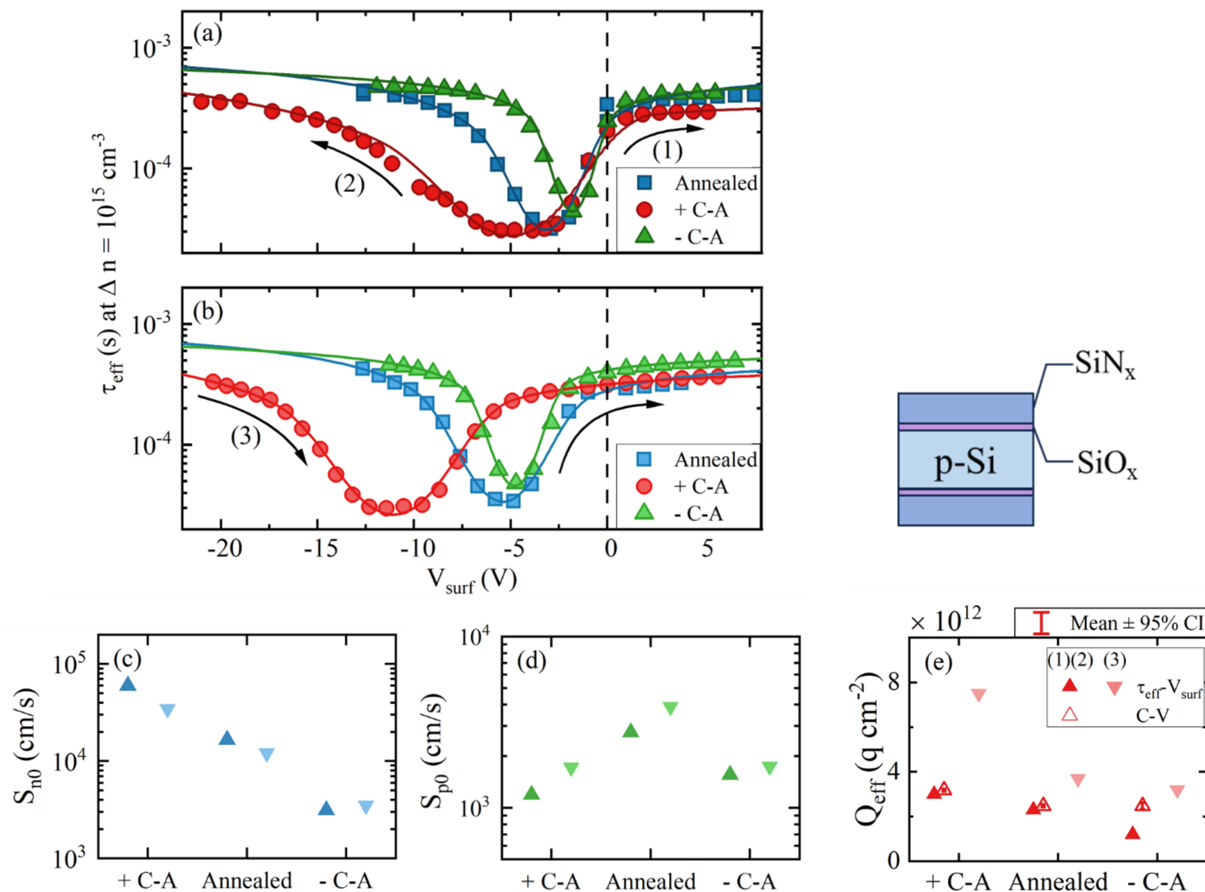


Figure 5.3.3 Effective lifetime as a function of surface voltage (τ_{eff}-V_{surf} plots) for SiO_x/SiN_x-passivated samples after annealing under different electric fields obtained from (a) step (1) and (2) and (b) step (3). Solid lines indicate model fittings using energy dependent parameterisation. The extracted interface properties are shown in (c) S_{n0}, (d) S_{p0} and (e) Q_{eff}. The darker symbols represent values extracted from (a), while the lighter symbols represent values extracted from (b). Extracted Q_{eff} from C-V measurements are included in (e), represented by the open symbols. The error bars represent the mean ± 95% CI of the four to six individual C-V measurements taken.

Changes in FEP were also observed, as evidenced by shifts in the τ_{eff} minima shown in Figure 5.3.3 (a). Extracted values from τ_{eff}-V_{surf} plots indicate an increase and decrease of 0.9×10^{12} q cm^{-2} after +C-A and -C-A, respectively, supported by C-V measurements. The change in Q_{eff} contrasts with that of $SiO_x/AlO_x/SiN_x$-passivated samples, suggesting an alternative charging mechanism. A possible explanation is the charging of Si≡N dangling bonds by corona charges. These defects, known as K-centres, exhibit three charged states of K^0, K^+, or K^-, and can be charged/discharged depending on the polarity of the corona charge [27], [225]. Under the annealing at 450 °C, the injected charges are likely to be driven deeper into material bulk, presenting a higher stability [32], [181]. This is supported by the minimal changes in the CPD values after the corona-anneal process. Further details of the measured CPD values are included in Appendix G. Charge injection to SiN_x is also likely present in the $SiO_x/AlO_x/SiN_x$ nanolayers, however less prominent than the charge injection to the deep acceptor defects in the Al:SiO_x layer. As a result, annealing under the same electric field led to opposite changes in Q_{eff} when comparing the $SiO_x/AlO_x/SiN_x$ and SiO_x/SiN_x stacks.

Hysteresis was also observed during measurements, as evidenced by the left shifts of curves in Figure 5.3.3 (b), compared to Figure 5.3.3 (a). Considering the measurement procedure, the observed increase in positive Q_{eff} was caused by the application of a large negative V_{surf}. An increase of 4.5, 2.6, and 2.0 × 10^{12} q cm^{-2} in positive Q_{eff} was found for + C-A, annealed, and – C-A samples, respectively. It is worth noting that the larger change in positive Q_{eff} after + C-A is likely to arise from the higher negative V_{surf} applied in step (2). Such changes in Q_{eff} have been extensively reported for SiN_x-passivated interfaces and attributed to the capturing/releasing of electrons from shallow traps [26], [27], [231]. This observation further supports the hypothesis that carrier injection at the Si/dielectric interface contributes to the observed changes in negative Q_{eff} at $SiO_x/AlO_x/SiN_x$-passivated interfaces. At both the SiO_x/SiN_x and the $SiO_x/AlO_x/SiN_x$-passivated interfaces, an inverse modification of Q_{eff} was observed with the application of surface electric fields – negative surface charge leads to an increase(decrease) in positive(negative) Q_{eff}.

Besides the changes in positive Q_{eff}, differences in charge fluctuation (σ_q) were also observed on samples with different annealing treatments, reflected in the curvature of the bottom region of the τ_{eff}-V_{surf} plots. Charge fluctuation is defined as the standard deviation in a Gaussian charge distribution centred on Q_{eff} [151]. A larger σ_q results in a larger curvature, broadened feature on τ_{eff} variations under weak field-effect passivation near the minimum, where τ_{eff} is highly sensitive to surface charge density changes. The extracted σ_q values are plotted in Figure 5.3.4 (a), indicating a higher σ_q after +C-A and a lower σ_q after -C-A. The coefficient of charge variation, defined as the ratio of charge fluctuation to mean charge density (σ_q/Q_{eff}), is used as a measure of charge dispersion. The calculated σ_q/Q_{eff} values are plotted in Figure 5.3.4 (b), where no significant difference between samples annealed under different electric fields was observed. These results suggest that changes in the curvature of the τ_{eff}-V_{surf} plots are also driven by variations in Q_{eff}. Lower σ_q/Q_{eff} values were extracted from τ_{eff}-V_{surf} plots obtained in step (3), suggesting a higher charge uniformity. This can be explained by the large increase in positive Q_{eff}, where more holes are injected to the trap states at the interface, saturating the interface. This reduces the variations in local charge density caused by the Coulomb repulsion of positive charges.

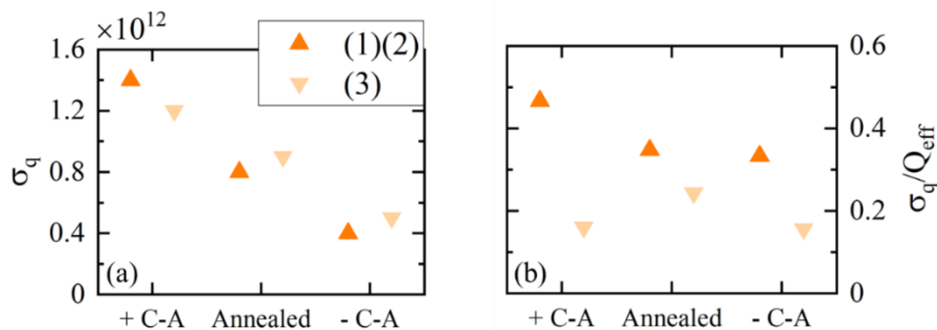


Figure 5.3.4 Extracted (a) charge fluctuation (σ_q) and (b) coefficient of charge variation (σ_q/Q_{eff}) extracted from τ_{eff}-V_{surf} plots.

5.4 Discussion

Taking account of observations at both $SiO_x/AlO_x/SiN_x$ and SiO_x/SiN_x-passivated interfaces, carrier injection and hydrogen migration under the applied electric field have been identified as the two key mechanisms which jointly affect the chemical ($S_{n/p0}$) and field-effect passivation (Q_{eff}) of Si-dielectric interfaces. The interface dynamics is further discussed, highlighting two seemingly contradictory observations in the changes of Q_{eff}.

Reversed changes in Q_{eff} were observed at the SiO_x/SiN_x interface following the application of a negative V_{surf} at room temperature and after -C-A, despite negative surface charge being present in both cases. To understand these contradictory findings, I refer to the two different charging processes and the location of the charged traps. Schematics illustrating these two processes are included in Figure 5.4.1. Under both treatments, the change in positive Q_{eff} is likely attributed to a shift in charge states of K-centres [28], [32]. Such defects are distributed throughout the SiN_x bulk and near the Si/dielectric interface [27], [28], [253]. Under a negative surface charge, holes are injected from Si to the interface and captured by K^0 and K^-, resulting in an increased positive Q_{eff}, as shown in Figure 5.4.1 (a). The location of the K^+ charged by hot holes is expected to be within 3 nm from the interface [254]. Meanwhile, K^-centres in SiN_x bulk capture electrons from the surface electrode (PEDOT:PSS or negative corona charges) and become negatively charged, resulting in a decreased positive Q_{eff}.

A higher density of charge is injected into the interface compared to the SiN_x bulk, resulting in a net increase in positive Q_{eff} after the application of a negative V_{surf}, as extensively reported in the literature [231], [232], [240]. Upon annealing, however, the surface electric field is removed and the trapped holes are released back to Si stimulated by the elevated temperature [255], while the K-centres in the SiN_x bulk remain negatively charged, resulting in a decrease in the positive Q_{eff} after –C-A, as shown in Figure 5.4.1 (b).

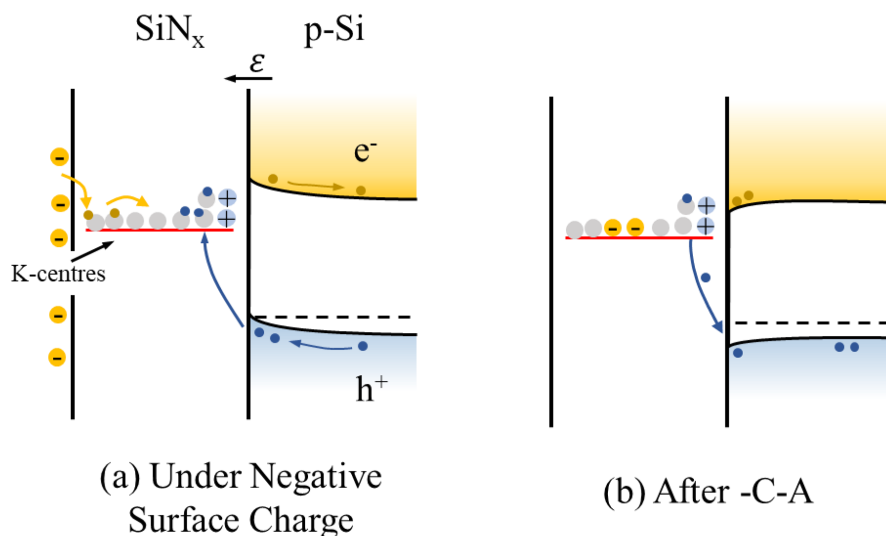


Figure 5.4.1 Schematics demonstrating charge injection near the SiN_x surface and at the Si/dielectric interface of (a) under negative surface charge, which corresponds to the application of a negative V_{surf} or corona charge at room temperature, (b) after annealing at 450 °C representing the interface change after -C-A.

Reversed changes in Q_{eff} were also observed at $SiO_x/AlO_x/SiN_x$ and SiO_x/SiN_x-passivated interfaces after the same corona-anneals, which is likely attributed to the difference in the defects at the Si/dielectric interfaces. Schematics demonstrating the charge injection processes under a positive surface charge are shown in Figure 5.4.2. As discussed previously, while positive charge is injected to the SiO_x/SiN_x-passivated interface under a negative surface charge, the injected charge is unstable under elevated temperatures, leading to a net decrease in positive Q_{eff} after -C-A. At the $SiO_x/AlO_x/SiN_x$-passivated interface, however, acceptor states are induced by the presence of Al atoms, as discussed in Chapter 4 and previously reported [57]. Such acceptor states have energy levels below the Si valence band minimum (VBM), therefore preserving the change in charge density near the interface after the removal of corona charges under elevated temperature (450 °C).

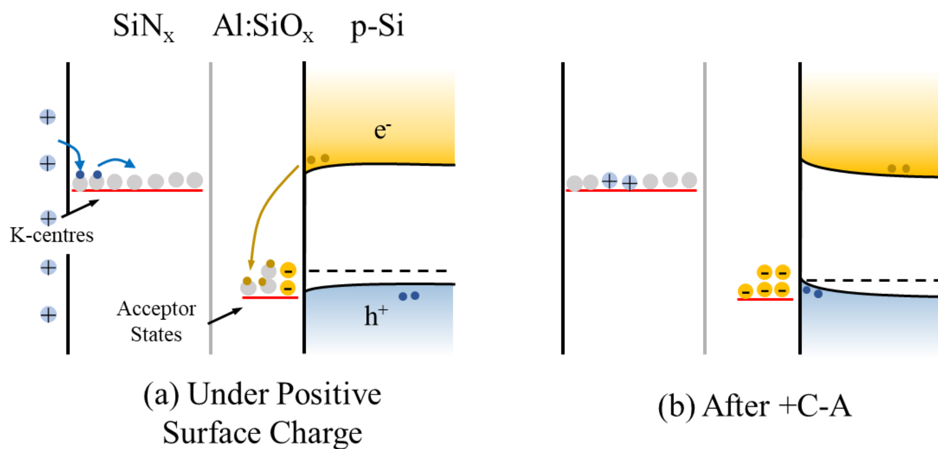


Figure 5.4.2 Schematics demonstrating charge injection near the SiN_x surface and at the Si/dielectric interface of (a) under positive surface charge, which corresponds to the application of a positive corona charge at room temperature, (b) after annealing at 450 °C representing the interface change after +C-A.

5.5 Summary

This Chapter presents a new strategy to modify and optimise the surface passivation quality through field-assisted annealing. A S_{eff} of 5.5 cm/s and a J_{0s} below 45.3 fA/cm^2 were demonstrated on p-Si passivated by a $SiO_x/AlO_x/SiN_x$ nanolayer stack after annealing under positive surface charge. This was achieved using low temperature, chemically grown SiO_x with a ~2.5 nm AlO_x layer. A detailed interface study was conducted by monitoring changes in τ_{eff} with varying applied surface voltages (V_{surf}), complemented by C-V measurements. Interface properties extracted from the fitting of the τ_{eff}-V_{surf} plots indicate that the changes in surface recombination properties are due to differences in electron capture velocity at the valence band tail ($S_{n,VB}$), highlighting the significant role of recombination at tail states in nanolayers with strong field-effect passivation.

Distinct changes in both chemical passivation at mid-gap (S_{n0} and S_{p0}) and field-effect passivation (Q_{eff}) were observed. A hypothesis involving carrier injection at the interface and hydrogen migration under the applied surface charge is proposed to explain these changes, indicating an intrinsic link between chemical and field-effect passivation. This hypothesis is further supported by changes observed at the SiO_x/SiN_x-passivated

interfaces after annealing under different electric fields and extensive indications in the literature [28], [32], [199], [225], [256].

Additional charging mechanisms were revealed, detailing the influence of the location and energy levels of the defect states involved in the charging process, which led to opposing changes in Q_{eff} observed under different conditions. It is pointed out that annealing under a positive surface charge can further promote negative charge density in ultra-thin AlO_x, with an increase of ~1×10^{12} q cm^{-2} observed after a single corona-anneal process. The promoted negative charge is stable through a 450 °C annealing.

The use of this strategy, which tunes interface properties by annealing under electric fields, offers the possibility of further adjustment of the nanolayer stacks for improved optical properties or reduced production cost, further improving device performance. The new understanding gained from this work is instrumental in developing alternative approaches to further enhance the surface passivation performance of different nanolayer, leading to solar cell efficiency improvements.

Chapter 6
Fabrication and Evaluation of 2D MoS_2 Field-Effect Transistors

6.1 Hysteresis in 2D MoS_2 Field-effect Transistors

Due to the atomically thin nature of 2D MoS_2, its properties are highly sensitive to both intrinsic factors (e.g. vacancies, interlayer interactions) [257], [258] and extrinsic factors (e.g. air adsorbates, residues, and dielectric traps) [259]. This pronounced sensitivity often results in unintentional doping, leading to significant hysteresis and device variations, posing challenges for practical applications [108]. In laboratory settings, such variations can obscure the intrinsic properties of MoS_2, making the minimisation of these unintentional doping essential. While unintentional doping is difficult to quantify and compare across devices, hysteresis serves as a useful indicator of its extent. It describes the difference in threshold voltage between forward and backward gate voltage sweep and is present due to the charge trapping/de-trapping process. Therefore, understanding the origins of hysteresis and minimising it is crucial to accurately extracting the intrinsic properties of 2D MoS_2 and for enabling high-performance, stable devices.

Figure 6.1.1 summarises the effects of various factors on the hysteresis of 2D MoS_2 FETs at different temperatures [260]. Water and oxygen in the air are recognised as the primary adsorbed species on the MoS_2 surface, primarily leading to n-type doping [261]. Air adsorbates also contribute most significantly to hysteresis commonly observed [123], [262], [263]. The resulting hysteresis is damped at elevated temperature due to increased desorption of these adsorbates, as shown in Figure 6.1.1 (a). The extent of doping depends on the humidity [263], as well as the quality of 2D MoS_2 which serves as reactive sites and contributes to device variations. The chemical mechanism by which water and oxygen molecules dope the MoS_2 channel surface has been described in previous studies [264], [265]. Weakly bound water molecules can dissociate or form dipoles on the MoS_2 surface, and these dipoles may donate electrons into the conduction band, effectively shifting the Fermi level upward and leading to n-type doping [266]. In addition, oxygen molecules adsorbed at sulphur vacancy sites or on the basal plane can also participate in charge transfer. Rather than extracting electrons, as observed in some oxides, oxygen in contact with MoS_2 tends to stabilise surface defects and facilitate electron donation from water or other species [264], [266]. The combined effect is an increased conductivity and left shifted V_{th}.

To minimise these effects, measurements are typically performed in a vacuum or inert gas. Alternatively, encapsulation layers such as h-BN, AlO_x, HfO_x, or polymers are commonly used to protect the channel from

environmental adsorbates [108], [123]. Another approach involves chemically passivating the channel, such as through exposure to H_2S gas, which has been shown to effectively eliminate hysteresis in air, although the chemical involved may introduce unwanted doping [262].

Additional factors also contribute to hysteresis, although their impact is comparatively minor. Ion impurities, such as Na^+, K^+, H^+, can be incorporated during dielectric growth. However, the mobility of larger ions like Na^+ and K^+ only occurs at elevated temperatures (340-450 K) under electric fields [267], [268], as shown in Figure 6.1.1 (b), rendering their contribution to hysteresis at room-temperature negligible. Charge trapping at the MoS_2-dielectric interface is also reported to cause unintentional doping and hysteresis, as outlined in Section 1.3.2.2 and shown in Figure 6.1.1 (c). This effect becomes more pronounced at elevated temperatures due to enhanced thermal-assisted trapping and de-trapping. Furthermore, the charging of oxide traps located near the Si substrate can screen out the gate voltage, thereby delaying the turn-on of the FET, as illustrated in Figure 6.1.1 (d). This effect manifests a sudden increase in current upon reversal of the gate voltage polarity. This specific effect has so far only been reported for SiO_2 at temperatures exceeding 400 K [269].

Finally, intrinsic factors such as traps in the 2D channel or interface defects between different van der Waals layers also contribute to hysteresis, as depicted in Figure 6.1.1 (e). This mechanism was proposed based on the observation of hysteresis in suspended devices, indicating that it arises from the filling and emptying of intrinsic traps [260].

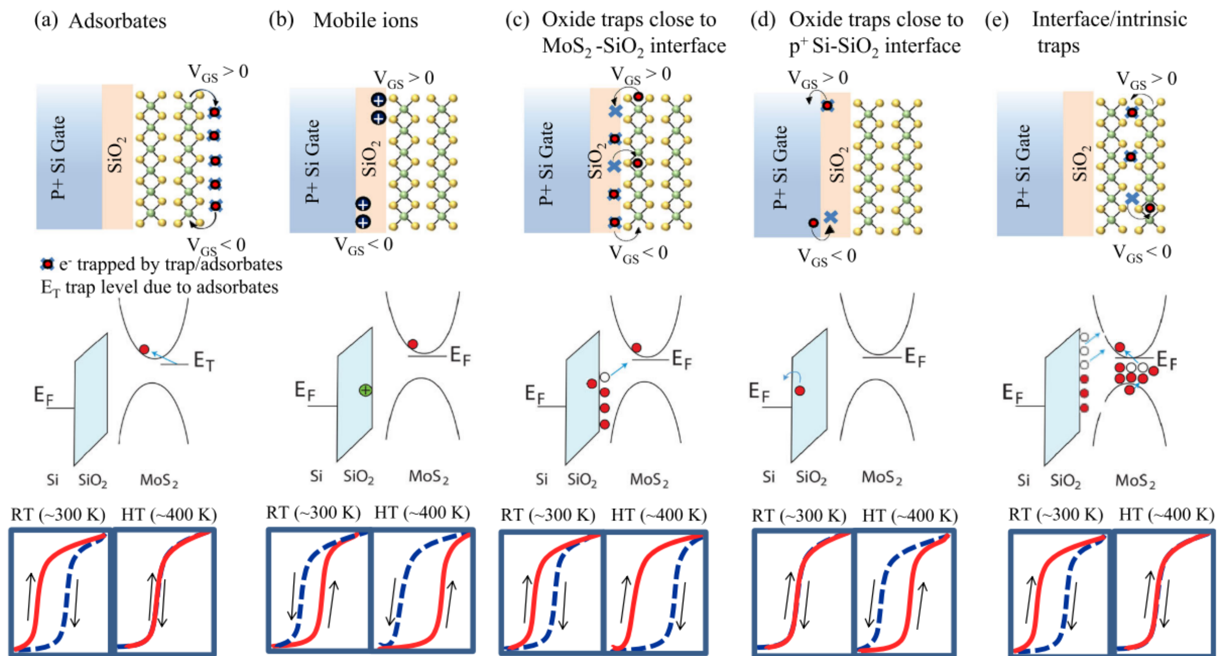


Figure 6.1.1 A summary of the different extrinsic (a) and intrinsic (b-e) factors inducing hysteresis in 2D MoS_2 FETs, their band diagrams, and schematics of the hysteresis curves under room temperature (RT) and high temperature (HT), reproduced after [260].

In summary, smaller hysteresis is indicative of a high-quality channel with minimal unintentional interactions with the surrounding environment. The objective of this Chapter is to establish a robust fabrication

and measurement protocol that mitigates the influence of such unintentional doping due to extrinsic factors. This protocol minimises device variability and hysteresis, providing a reliable foundation for investigating field-effect doping via charged dielectrics in Chapter 7. Furthermore, a comprehensive model is proposed to elucidate the observed phenomena.

6.2 All-dry Fabrication of 2D MoS_2 FETs

During the development of charged dielectrics, significant charge degradation was observed upon exposure to liquid solutions such as deionised (DI) water and common cleaning solvents. This degradation prevents the investigation of changes in the electrical properties of 2D MoS_2 using conventional photolithography-based FET fabrication processes. As a result, a novel all-dry fabrication method for 2D MoS_2 FETs is essential. The primary challenge lies in accurately aligning metal contacts to exfoliated MoS_2 flakes, which are typically only 10-20 μm in size.

6.2.1 Monolayer Identification

Mechanically exfoliated monolayers of MoS_2 are used as channel material in this work. The exfoliation and transfer process are described in Appendix B. Monolayers were identified based on their contrast to the substrate under an optical microscope and verified using Raman spectroscopy, as shown in Figure 6.2.1. The monolayers presented in this thesis have a wavenumber difference of 19-20 cm^{-1} between the E_{2g} and A_{1g} peaks, which is in line with the literature [86]. This frequency separation arises because the two vibrational modes shift systematically with increasing layer number: the in-plane E_{2g}^1 mode redshifts as additional layers reduce the restoring force for in-plane vibrations, while the out-of-plane A_{1g} mode blueshifts due to enhanced interlayer coupling that constrains out-of-plane motion [270]. The resulting increase in the peak separation therefore provides a reliable spectroscopic signature for identifying monolayer MoS_2.

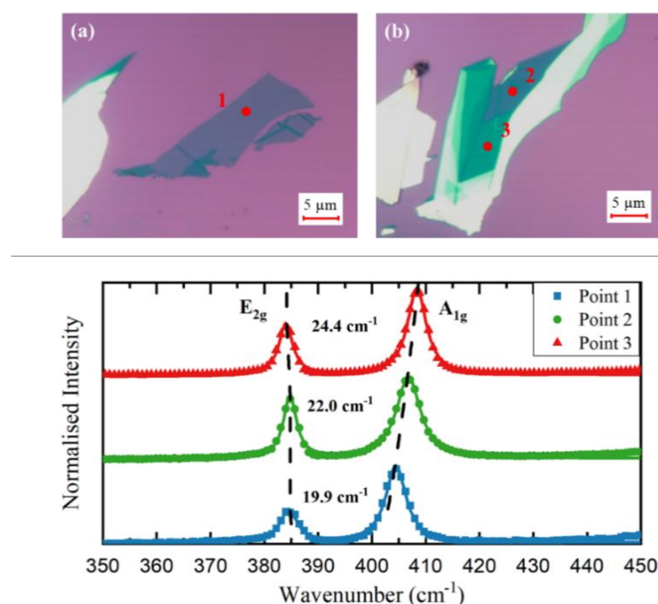


Figure 6.2.1 Exemplary optical microscope photos of exfoliated (a) monolayer and (b) multilayer flakes and their corresponding (c) Raman spectrums, which were obtained at the location indicated in (a) and (b) with red dots.

6.2.2 Mask Fabrication

Bottom-gate top-contact structured FETs were fabricated in this work, with a schematic of the device shown in Figure 6.2.2. To enable electrical measurements, full area aluminium (Al) back contact was used, while two front contacts were required to connect the selected monolayer MoS_2. Thus, a suitable mask is needed to protect the channel region during contact evaporation. Due to the micron-scale dimensions of exfoliated flakes, masks with features smaller than 10 µm are desirable. This is typically achieved using photoresist masks patterned by UV light or laser writers [271]. However, the use of solvents involved in such a process was found to degrade the dielectric embedded charge, as further discussed in Section 6.2.4. Therefore, to preserve the dielectric charge, a contactless all-dry patterning process is required. Additionally, to minimise the shadowing effects during evaporation, the mask must be flat. Finally, the mask design should be reproducible and easy to manipulate to be precisely aligned with the selected flake.

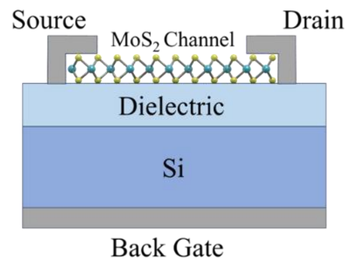


Figure 6.2.2 Schematic of a 2D MoS_2-based back-gate front-contact structured FET.

With the considerations above, TEM grids were identified as the optimal choice. The FETs presented in this thesis were fabricated using a copper TEM grid with 600 hexagon mesh with a bar size of 6 µm as the evaporation mask. A process flow of mask fabrication is shown in Figure 6.2.3 (a-c). TEM grids were first attached to M1.6 stainless-steel washers using wax. The flat side of the washer is covered with wax melted at 50 °C. After cooling, the washer is aligned on top of the TEM grid under a stereo microscope. The TEM grid-washer stack is then reheated on a hot plate, attaching the TEM grid to the washer. This low-temperature bonding process preserves the flatness of the TEM grid. The stainless-steel washer serves three critical functions:

(1) Structure reinforcement: it prevents deformation of TEM grid during handling.
(2) Ease of alignment: with a thickness of 300 µm, the washer allows for straightforward handling.
(3) Magnetic fixation: when placed on a magnet, the washer securely holds the TEM grid in the aligned position, enabling transfer to subsequent processing.

The channel and contact regions are then defined using a UV pico-second laser from Inngu Laser, as described in Appendix B. The mask is positioned with the side attaching TEM grid facing upward to ensure the lasered area bend away from the substrate during alignment, as shown in Figure 6.2.3 (c). To ensure structural robustness, minimal etching is preferred. It is also advantageous to leave space for additional contacts in the case of front-back shortage due to dielectric defects. After front contact evaporation, silver dag was

applied to form durable and sizable contacts suitable for probe landing. For these reasons, a design with bar-shaped contacts is optimal. An optical microscope image of the designed mask and a fabricated device is shown in Figure 6.2.3 (d), with an enlarged image of the channel region in Figure 6.2.3 (e).

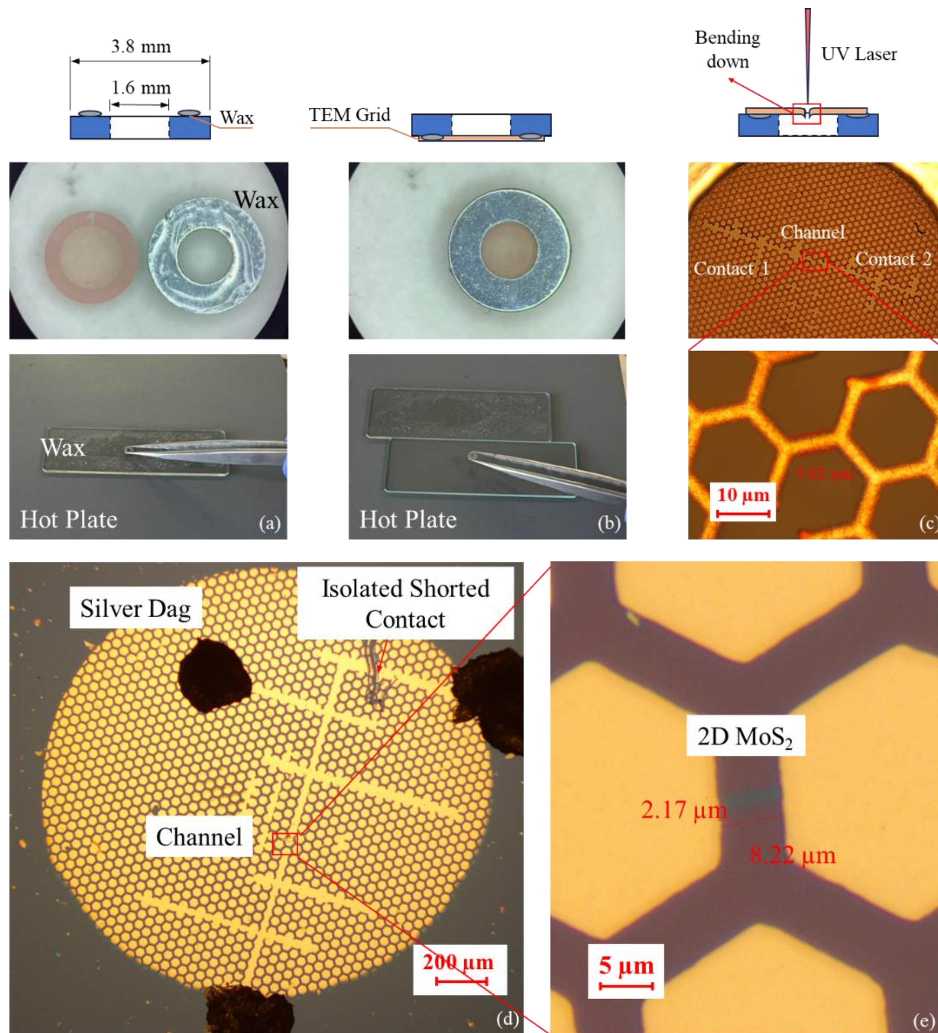


Figure 6.2.3 (a-c) Process flow to fabricate evaporation masks to fabricate 2D MoS_2 FETs using TEM grids and stainless-steel washers. (d) The optical microscope of a fabricated device with an isolated contact, which is shorted to the back gate. (e) An optical microscope image of the channel region.

6.2.3 Mask Alignment and Batch Processing

The fabricated mask is placed on a Si substrate and aligned to the exfoliated MoS_2 monolayer under an optical microscope. To ensure the mask remains securely in place after alignment, a flexible magnetised stripe with a uniform magnetic field was used to hold the masks. Cover glasses were placed between the magnet and sample to protect the magnets during evaporation. An image of a sample holder is shown in Figure 6.2.4.

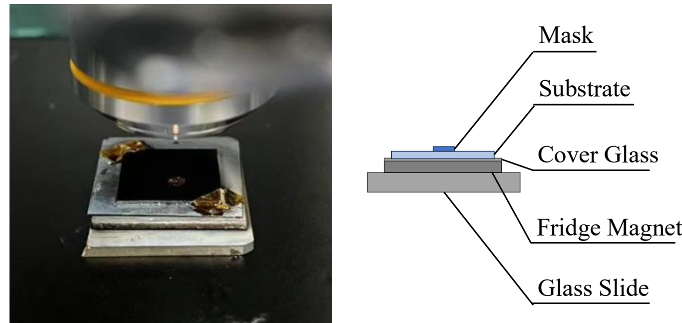


Figure 6.2.4 An image of a sample holder with a fridge magnet to secure the mask during transfer.

To achieve high-throughput device fabrication, an efficient and reproducible alignment method is crucial. A slot to hold and manipulate the washer during alignment was fabricated by etching a round window into a 200 µm thick mirror-polished Si substrate. The Si substrate is flat, robust, and thinner than the washer, which allows the washer to be securely held in place without contacting the substrate surface. A photo of the alignment set-up is shown in Figure 6.2.5 (a). Once the selected flake is identified under the optical microscope, the mask is roughly positioned on the substrate. The slot is then held above the sample while its height is adjusted by simultaneously adjusting the height of lab jack stands until the washer fits within the slot. Both the selected flake and the mask should be in focus. The mask is then aligned with the flake by moving the optical microscope stage. Once aligned, the optical microscope stage is lowered to detach the mask from the slot, leaving it held in place by the magnet.

An 8-slot holder is designed to facilitate the transfer of aligned samples to the subsequent thermal evaporation. A demonstration of the slot is shown in Figure 6.2.5 (a-b). All samples are first attached to the 8-slot holder prior to alignment. A pyramidal frustum-shaped holder is 3D printed, with the smaller side attached to the Si slot, while the larger side provides sufficient space for the optical lens, as shown in Figure 6.2.5 (c-d). The Si slot was cleaved to be ~1.5 cm × 2 cm, allowing for the alignment of each sample without disturbing the alignment of the neighbouring samples. This alignment procedure proves to be highly efficient, with an average of 6 working devices produced per batch. The failed devices are believed to result from shifts in the mask position during thermal evaporation. This issue arises when the wax glue is slightly heated and adheres to the silicon substrate, thereby causing mask displacement.

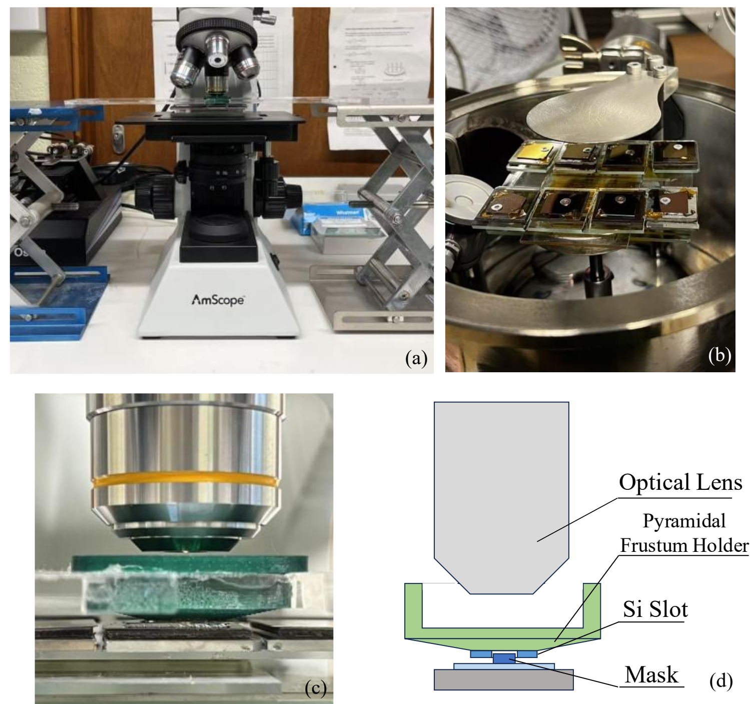


Figure 6.2.5 An image of (a) the alignment setup, (b) the 8-slot holder inside of the thermal evaporator, (c) a zoom-in image of the alignment setup and (d) a schematic of the Si slot securing the mask.

6.2.4 Assessing the Stability of Dielectric Charge

To study the charge stability after different treatments, a substrate with 300 nm of thermal SiO_2, charged at 450 °C for a total of 5 minutes using the hot corona method, and capped by 50 cycles of HfO_x (Set 4-C) was used. Charge densities were measured using KP before and after a 1-minute exposure to isopropyl alcohol (IPA) or O_3, which are commonly used in the photolithography process, and compared against the all-dry fabrication process, as shown in Figure 6.2.6. The variation in the initial CPD values arises from differences in the charging intervals. Charging strategies with intervals of 60 s, 30 s, and a continuous 5-minute duration were adopted for testing samples under IPA, O_3, and dry fabrication conditions respectively. A variation of less than 5% in CPD values was observed after device fabrication, while a ~50% loss was found after O_3, and a complete charge loss after exposing substrates to IPA and acetone. These results highlight the reliability of the substrates' charged state following the all-dry fabrication process. The underlying cause for the charge instability is further discussed in Chapter 7.

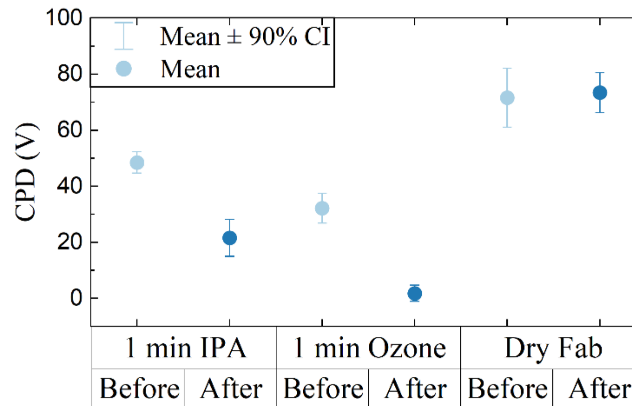


Figure 6.2.6 Contact potential differences (CPD) measured before and after treatment of 1-minute exposure to IPA, acetone, O_3, and all-dry fabrication. The error bars represent 90% confidence interval of data obtained on 3-5 samples.

6.3 Control and Optimisation of FET Measurements

Monolayer MoS_2 is highly sensitive to environmental factors, including air adsorbates, light exposure, and measurement history. This section explores the impact of various factors on the device performance and aims to establish an optimised protocol for accurately characterising the electrical properties of 2D MoS_2.

6.3.1 Effects of Atmosphere Environment

As reviewed in Section 6.1, adsorbates from ambient air have been recognised as a source of unintentional doping in 2D MoS_2. This doping effect is affected by environmental variations such as humidity, leading to device variability. To minimise unintentional doping caused by environmental factors, a measurement setup was designed to operate within an enclosed chamber filled with high-purity argon.

To evaluate the effectiveness of the argon environment in eliminating air-induced doping, an FET device was fabricated on a substrate consisting of 300 nm thermal SiO_2 capped with 50 cycles of ALD-SiO_x (Set 3-A). The hysteresis behaviour was characterised using a back-gate voltage (V_{gs}) sweep from – 80 V to 80 V with a step size of 2 V, and a drain-source voltage (V_{ds}) of 0.01 V. Measurements were conducted in darkness, with five transfer curves obtained with a 180-second interval before introducing the argon gas at a flow rate of 4-5 litre per minute (LPM). Immediately following this, an additional five measurements were performed under argon atmosphere.

For a clear demonstration of changes in the transfer characteristics, only the first and last curves obtained under air and argon conditions are presented in Figure 6.3.1 (a). The dotted lines in Figure 6.3.1 (a) indicate the linear extraction of V_{th}, while the arrows indicate the forward and backward sweep directions. To demonstrate the repeatability of the results, the extracted threshold voltages for forward and backward sweeps (V_{th1}, V_{th2}) and field-effect mobility (μ_{FE}) from the forward curves from all measurements taken are shown in Figure 6.3.1 (b). The extraction of threshold voltages is described in Chapter 2, Section 2.4.7. Due to the nature of the backward sweep, which is further discussed in Section 6.4, V_{th2} is much more dependent on environmental conditions compared to V_{th1}. Thus, the following discussions mainly focus on the properties

extracted from the forward transfer curves, while the backward curve is analysed to characterise the hysteresis ($V_{hys} = V_{th2} - V_{th1}$). The field-effect mobilities (μ_{FE}) were also extracted from the forward sweep.

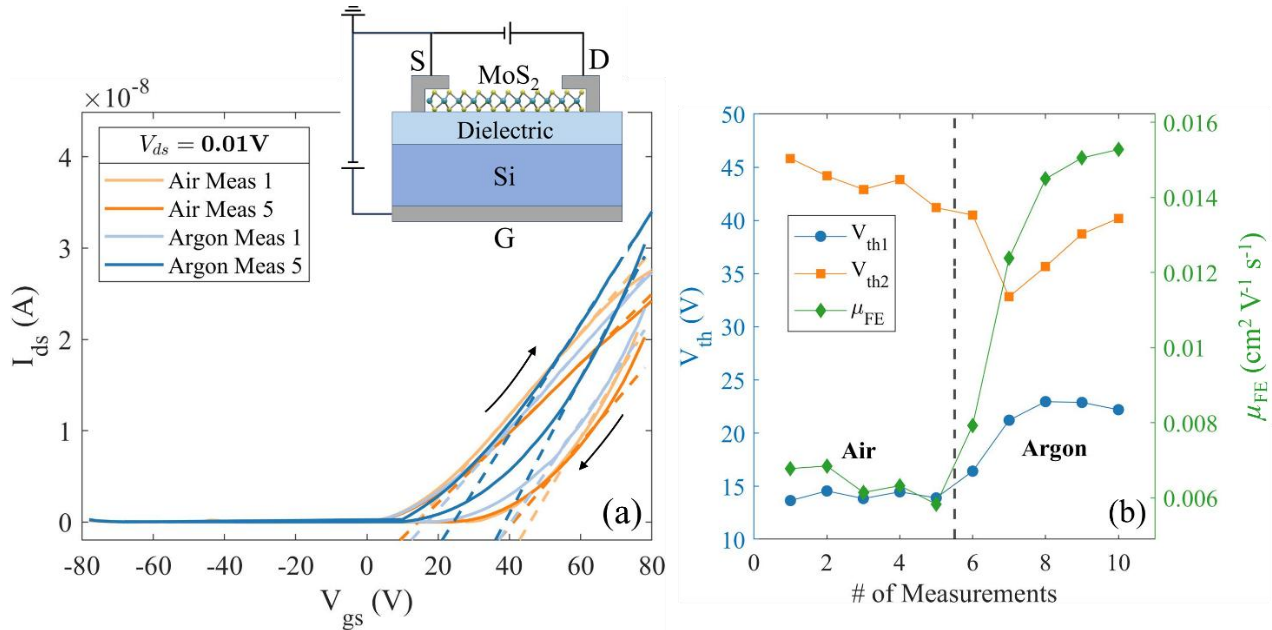


Figure 6.3.1 (a) Transfer characteristics measured in air and Argon and (b) the extracted V_{th} and μ_{FE}.

All curves in Figure 6.3.1 (a) exhibit a clockwise hysteresis. Repeated measurements in air revealed a slight decrease in μ_{FE}, as evidenced by the green diamond symbols in Figure 6.3.1 (b). Upon the introduction of argon, both V_{th1} and V_{th2} converge, thereby reducing the V_{hys}. Additionally, an increase in μ_{FE} was observed in measurements in argon, as shown in Figure 6.3.1 (b). The changes in both V_{th} and μ_{FE} were observed to plateau around the third measurement, suggesting the saturation of argon atmosphere. This takes approximately 15 minutes.

To confirm if the above changes in transfer characteristics is repeatable on multiple devices, nine devices fabricated on substrate Set 3-A were measured both in air and argon atmosphere. Five consecutive measurements with intervals of 180 seconds were taken on each device with the V_{th}, V_{hys} and μ_{FE} values extracted from the last measurement. To elucidate the influence of the measurement environment on device characteristics, the variations in V_{th1}, V_{hys} and μ_{FE} were determined by calculating the difference between values obtained in argon and air (argon – air) and plotted in Figure 6.3.2Figure 6.3.2. The error bars represent the 95% confidence interval. A predominately positive shift in ΔV_{th1} was observed, with the corresponding confidence interval slightly overlapping zero. This trend suggests an overall increase in V_{th1} when measurements are conducted in argon, indicative of a reduction in n-type doping. A consistent decrease was observed for V_{hys}, as indicated by the negative ΔV_{hys} values with the confidence interval lying below zero, demonstrating a decrease in hysteresis. Furthermore, $\Delta\mu_{FE}$ showed clear positive values, confirming an enhancement in the carrier mobility in an argon environment. Collectively, these results substantiate that measurements performed in an argon environment effectively suppress the influence of adsorbates present in air, thereby enabling a more accurate and reliable assessment of device performance.

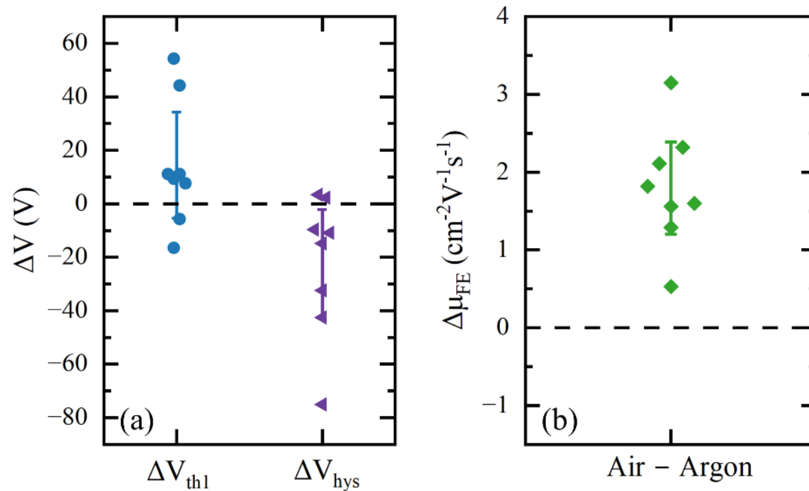


Figure 6.3.2 Changes in the extracted values of (a) V_{th1} and V_{hys} and (c) μ_{FE} from measurements carried out in air and argon (argon – air). The error bars represent the 95% confidence interval of the values obtained.

6.3.2 Effects of Measurement Range and Step Size

A substrate with 300 nm thick thermal SiO_2 capped with 360 cycles of ALD-SiO_x (Set 4-A) was used to fabricate a FET and investigate the effects of the measurement range. The substrate was annealed at 800 °C for 30 minutes prior to device fabrication. The device was set in darkness and argon environment 15 minutes before the start of measurements and remained in such condition throughout the measurements. The minimum and maximum values of V_{gs} were varied between – 80 to -120 V and + 80 to + 120 V, respectively. The measurements were carried out by first varying the minimum V_{gs}, followed by varying the maximum V_{gs}. The step size was 2 V for all measurements, and V_{ds} was kept at 0.01 V. At each condition, three measurements were taken at 180-seconds intervals. For a clear demonstration, the last transfer curves taken under each condition are shown in Figure 6.3.3 (a) and (b), while and the extract values of V_{th}, V_{hys} and μ_{FE} from all measurements are shown in Figure 6.3.3 (c) and (d). The dotted lines in Figure 6.3.3 (a-b) indicate the linear extraction of V_{th}.

As shown in Figure 6.3.3 (a) and (c), a statistically significant decrease in V_{th1} was observed when the minimum V_{gs} was reduced from –80 V to –120 V, indicating n-type doping. At the same time, a statistically significant increase in V_{hys} was recorded, while μ_{FE} showed minimal change. When higher maximum V_{gs} values were applied, as shown in Figure 6.3.3 (b) and (d), the forward curves largely overlap, indicating minimal changes in V_{th1} – as expected, since the forward measurement probe the same voltage range up to 80 V. It is noted, however, that care is required when extracting V_{th1} as an extended linear region can bias the algorithm described in Section 2.4.7 to a more accurate value, but the difference is not raised from changes in the intrinsic properties of the channel. To minimise this effect, The extracted V_{th1} in Figure 6.3.3 (d) are obtained by fixing the linear fit window to 0-80 V, while full curves are used to evaluate V_{hys} and μ_{FE}. Under these conditions, higher maximum V_{gs} yields a statistically significant increase in V_{hys}, with only minor changes in μ_{FE}. The larger V_{hys} is attributed to charge injection during the longer sweeps at higher V_{gs}, which raises V_{th2} and thus

widens the hysteresis. A sweep of –80 to +80 V was adopted for most devices to capture turn-on while minimising measurement-induced doping.

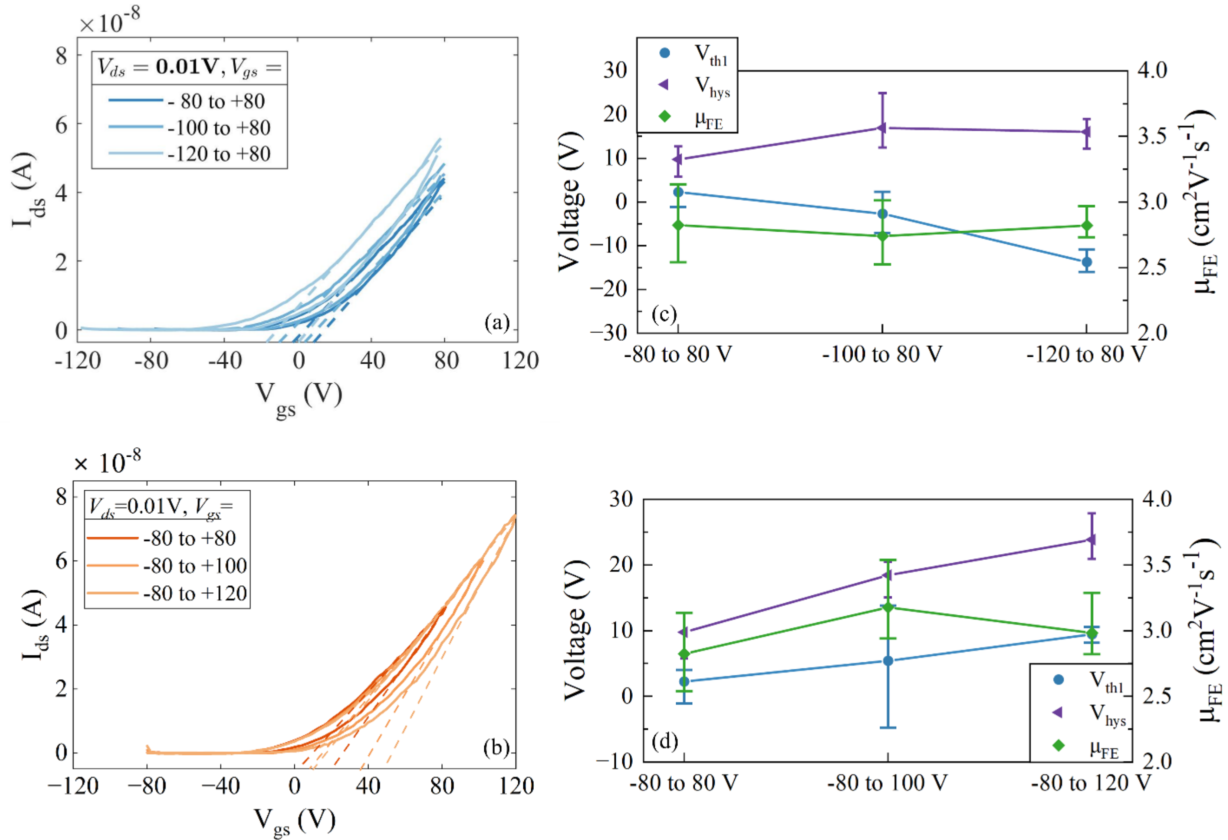


Figure 6.3.3 Transfer curves of the last measurements taken with (a) minimum V_{gs} ranging between – 80 and – 120 V, and (b) maximum V_{gs} ranging between + 80 to + 120 V. The extracted values of V_{th1}, V_{hys}, μ_{FE} of measurements taken with varying (c) minimum V_{gs} and (d) maximum V_{gs}. Three measurements were taken at each condition. The error bars represent the 10-90% of the values obtained in the three measurements.

The effects of the V_{gs} step size were then investigated using a device fabricated on a substrate with a 300 nm-thick thermal SiO_2, capped with 50 cycles of ALD-SiO_x (Set 3-A). The measurements were conducted in an argon atmosphere and in darkness, with a V_{gs} sweep between – 80 and + 80 V and the V_{ds} at 0.01 V. Step sizes of 1, 2 and 4 V were studied. The obtained transfer curves and the extracted values of V_{th1}, V_{hys} and μ_{FE} in Figure 6.3.4. Only the last curves measured in each condition are shown.

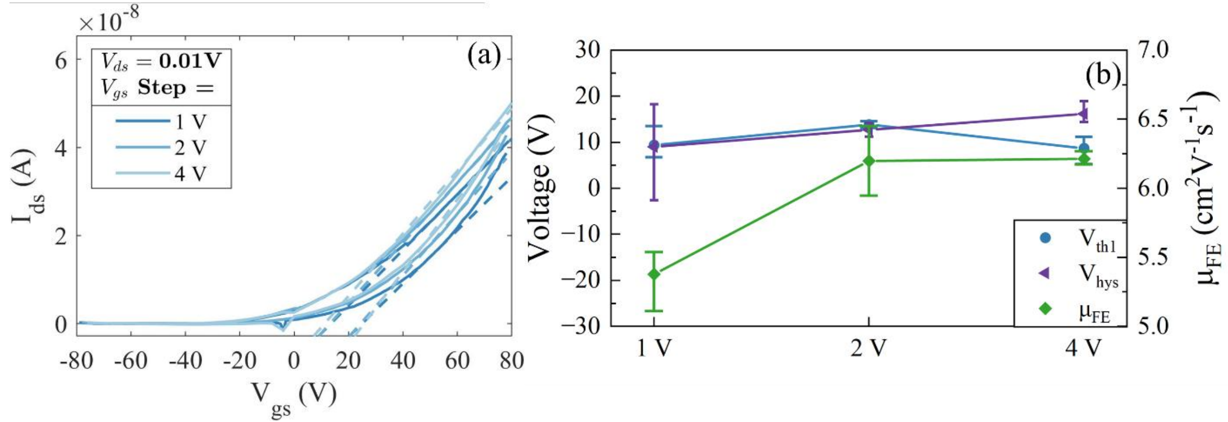


Figure 6.3.4 (a) Transfer curves of the last measurements taken with V_{gs} step sizes of 1, 2 and 4 V. (b) Extracted values of V_{th1}, V_{hys}, and μ_{FE} of all the measurements taken. The error bars represent the 10-90 % of the values extracted.

A variation of less than 10 V was observed in both V_{th1} and V_{hys}. Meanwhile, a statistically high channel mobility was observed by setting the step size to 2 or 4 V compared to 1 V. This increased mobility is likely due to the shorter measurement time associated with the larger step size, which generates less heat during the measurement and suppresses scattering. To balance the need for sufficient data points for reliable linear fitting with the need to minimize mobility degradation, a moderate step size of 2 V was selected.

6.3.3 Effects of Light

A substrate with a 300 nm thick thermal SiO_2, capped with 360 cycles of ALD-SiO_x (Set 4-A) was used to fabricate a FET and investigated the effects of light conditions. The substrate was annealed at 800 °C for 30 minutes prior to device fabrication, as shown necessary in Appendix C. The device was set in argon atmosphere 15 minutes prior to the first measurement. Three measurements with intervals of 180 seconds were taken in each condition, with the V_{gs} sweep between – 80 and + 80 V, a step size of 2 V, and the V_{ds} at 0.01 V. The device was illuminated with the highest power setting on the stereo microscope using a halogen lamp, designated the 'light' condition. A black foam was used to cover the setup in the 'dark' condition, as described in Chapter 2, Section 2.4.7. The last measured curves of each condition and the extracted V_{th1}, V_{hys}, and μ_{FE} of all the measurements taken are shown in Figure 6.3.5.

A statistically significant decrease in V_{th1} and an increase in V_{hys} were observed under illumination compared to measurements in the dark, indicating additional n-type doping induced by light. In contrast, no significant change was observed in channel mobility. These results suggest that performing measurements in a controlled dark environment is more appropriate for evaluating the intrinsic properties of 2D MoS_2.

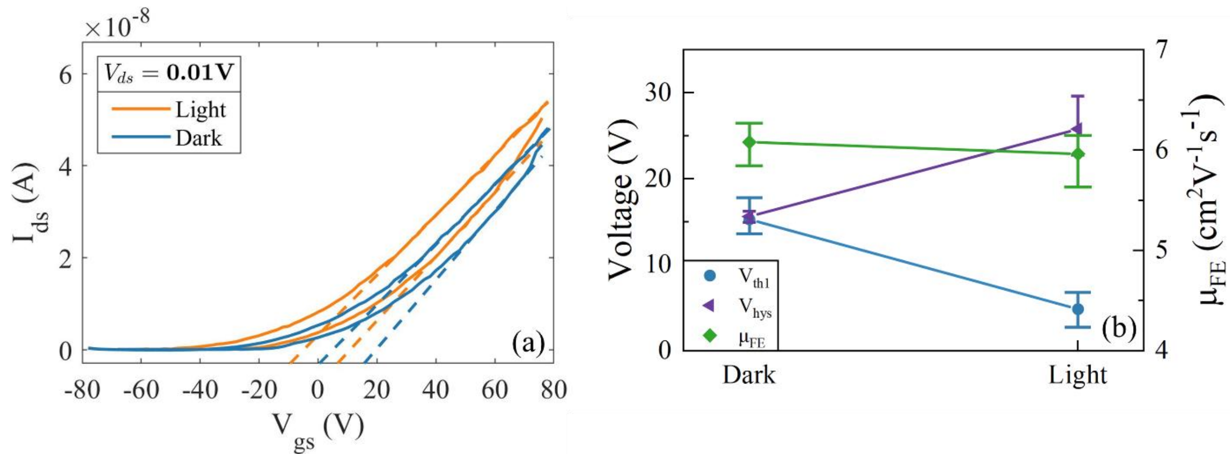


Figure 6.3.5 (a) Transfer curves of the last measurements taken under illumination and in dark. (b) Extracted values of V_{th1}, V_{hys}, and μ_{FE} of all the measurements taken. The error bars represent the 10-90% range of the values extracted.

6.3.4 Effects of Annealing

As demonstrated in Section 6.3.1, an argon atmosphere effectively mitigates the impact of air adsorbates. However, this approach does not address the unintentional doping caused by polydimethylsiloxane (PDMS) residues, strain, and air blisters formed during the dry transfer process [272]. Annealing at 200 °C in a vacuum has been reported as an effective method to mitigate these effects and further remove the air adsorbates. In this section, the impact of annealing 2D MoS_2 FETs in argon and vacuum at 100 and 200 °C was investigated to evaluate the necessity of incorporating such a process into the measurement protocol.

A substrate with 300 nm thick thermal SiO_2 capped with 360 cycles of ALD-SiO_x (Set 4-A) was used to fabricate a 2D MoS_2-based FET and investigated the effects of annealing in argon and vacuum. The substrate was annealed at 800 °C for 30 minutes prior to device fabrication, as shown necessary in Appendix C. The fabricated device was connected to a chip carrier using copper wires to prevent disconnection during heating, which could occur due to the thermal expansion of the measuring stage. A side view of a device on a chip carrier is shown in Figure 6.3.6. All measurements were taken in darkness, with the V_{gs} sweeping between – 80 and + 80 V at a step size of 2 V, and the V_{ds} at 0.01 V. Three to five measurements were taken at each condition, with an interval of 120 seconds between each measurement. Measurements were taken at room temperature (25-35 °C).

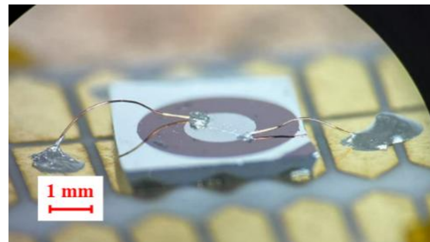


Figure 6.3.6 An image of a fabricated device bonded to a chip carrier.

Annealing in argon was conducted in the measurement setup described in Chapter 2, Section 2.4.7 on a temperature-controlled stage. The argon flow was set on to 4 LPM at the start of the first measurement. After

five measurements, the stage temperature was set to 100 °C, which took 10 minutes to ramp up. The set temperature was kept at 100 °C for 20 minutes before turning off the heater. The stage returned to room temperature after 1.5 hours. Subsequently, the same device was heated to 200 °C, with a ramp-up time of 16 minutes from room temperature and held at 200 °C for 20 minutes. The stage returned to room temperature after 2.5 hours. The last transfer curves measured in each condition, and their corresponding V_{th1}, V_{hys}, and μ_{FE} values are shown in Figure 6.3.7.

Following an annealing at 100 °C, a statistically significant decrease in V_{th1} was observed, with neglectable change in the V_{hys}. This change is likely attributed to the removal of PDMS residues or strain, and less likely to result from the removal of air adsorbates, as these are known to n-dope 2D MoS_2 [261]. Additionally, the observed increase in μ_{FE} from an average of ~8.2 to 11.7 cm^2 V^{-1} s^{-1} is likely due to the removal of a combination of PDMS residue, strain and air blisters, all of which contribute to carrier scattering [272]. On the other hand, μ_{FE} decreased to 6.8 cm^2 V^{-1} s^{-1} following annealing at 200 °C, indicating oxidisation of 2D MoS_2 to MoO_3 and causing p-doping [273]. This is also supported by the right shift in V_{th1} of ~20 V after the 200 °C-annealing. Therefore, it is demonstrated that while annealing in argon at 100 °C effectively removes unintentional doping, annealing at 200 °C is unsuitable, as it compromises the channel by inducing oxidation.

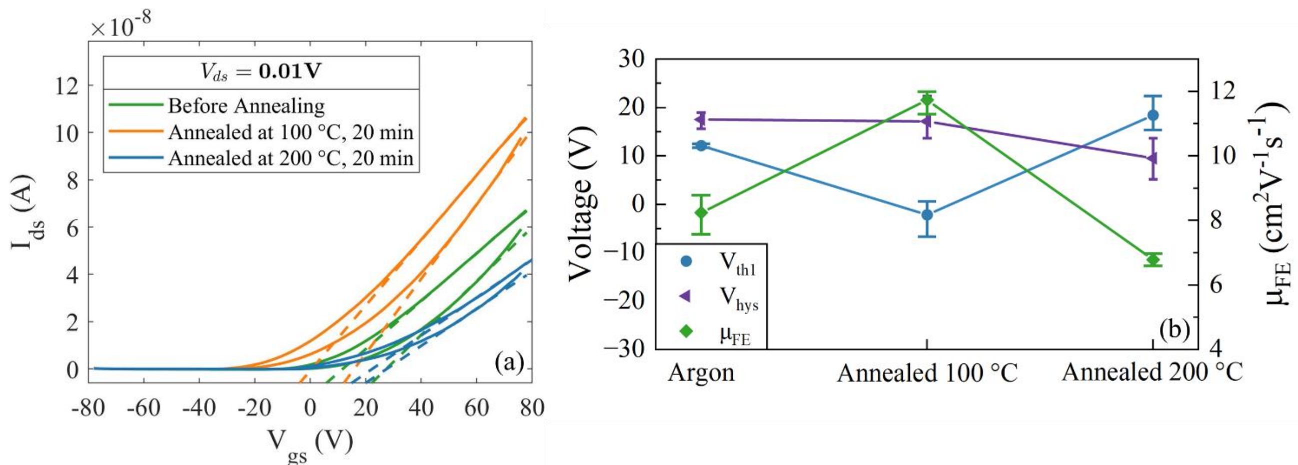


Figure 6.3.7 (a) Transfer curves of the last measurements taken before and after annealing in argon at 100 and 200 °C for 20 minutes. (b) Extracted values of V_{th1}, V_{hys}, and μ_{FE} of all the measurements taken. The error bars represent the 10-90% of the values extracted.

A setup modified from an Edwards E306A thermal evaporation system was used to test the effects of annealing under vacuum. The same sample used to evaluate argon annealing was subsequently used for this study. All measurements were conducted at a vacuum pressure of ~5 × 10^{-6} Torr. The stage temperature was set to 100 °C and took 20 minutes to ramp up. The set temperature was kept at 100 °C for 20 minutes before turning off the heater. The stage returned to room temperature after 1.5 hours. For the annealing at 200 °C, the stage took 25 minutes before first reaching the set-temperature. Due to the uncalibrated PID parameters, the stage temperature overshot to 280 °C, after which the heater was turned off. The time during which the device was kept above 200 °C was roughly 20 minutes. The stage returned to room temperature after 1.5 hours. The

last transfer curves measured in each condition, and the extracted V_{th1}, V_{th2}, and μ_{FE} from all measurements taken is shown in Figure 6.3.8. The transfer curve obtained after annealing in argon at 200 °C is included for comparison.

An average left shift of 10 V was found in V_{th1} in vacuum compared to argon. This indicates further elimination of the effects of air adsorbates in vacuum, although the improvement was modest. Similar to annealing in argon at 100 °C, left shifts in both V_{th1} and increases in μ_{FE} were observed after vacuum annealing under both 100 and 200 °C. No statistically significant change in V_{hys} was detected throughout these processes with all values below10 V, indicating minimal hysteresis. These results point to the effective removal of PDMS residues, strain and air blisters, which were not fully removed by prior annealing in argon. Compared with argon annealing, vacuum annealing proves more effective in suppressing unintentional doping introduced during the dry transfer process, primarily because it allows higher annealing temperatures and longer durations without risking oxidation of the 2D MoS_2 channel.

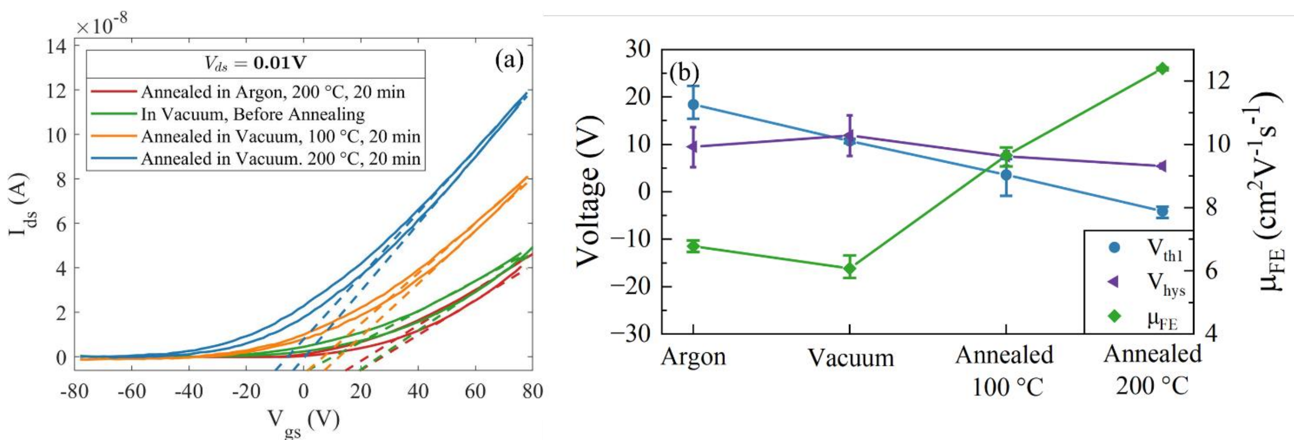


Figure 6.3.8 (a) Transfer curves of the last measurements taken before and after annealing in vacuum (~5 × 10^{-6} Torr) at 100 and 200 °C for 20 minutes. Curve measured after annealing in argon at 200 °C is included for comparison. (b) Extracted values of V_{th1}, V_{hys}, and μ_{FE} of all the measurements taken. The error bars represent the 10-90% of the values extracted.

However, due to practical considerations, annealing and measuring in a vacuum requires significant time, especially when dealing with a large number of devices. Argon annealing at 100 °C is thus further investigated for its effectiveness in reducing device variations. The annealing time was kept at 20 minutes.

Eight devices fabricated on substrate with a 300 nm SiO_2, capped with 50 cycles of ALD-SiO_x was measured in argon before and after annealing (Set 3-A). The extracted changes in V_{th1}, V_{hys} and μ_{FE} for each measured device are presented in Figure 6.3.9. Five consecutive measurements with intervals of 180 seconds were taken on each device with the extracted values from the last measurement plotted. All measurements were conducted in darkness, with the V_{gs} sweeping between – 80 to + 80 V, and a step size of 2 V. The V_{ds} was kept at 0.01 V.

No statistically significant change in V_{th1} was observed, as the 95% confidence interval crossed zero, indicating that some devices exhibited higher V_{th1} after annealing while others showed lower values. This

variation is likely a result of uncontrolled oxidation of the devices during argon annealing, which is also supported by the results in Figure 6.3.7. Hysteresis was consistently reduced across all devices, with the confidence interval lying entirely below zero, suggesting effective removal of adsorbates following argon annealing. In addition, a statistically significant increase in μ_{FE} was observed, as shown in Figure 6.3.9 (b). These results indicate that while annealing in argon at 100 °C can partially remove unintentional doping, it may also introduce oxidation due to non-ideal gas environment and variations in channel areas. Taking into account both these effects and the considerable time required to measure a large number of devices, measurements in an argon atmosphere were adopted as the standard protocol for this thesis.

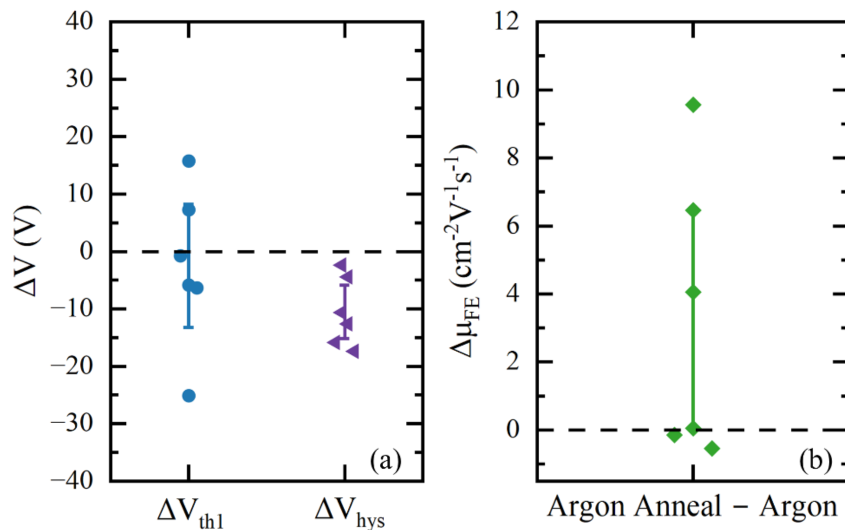


Figure 6.3.9 Changes in the extracted values of (a) V_{th1} and V_{hys} and (c) μ_{FE} from measurements carried out in argon and after argon annealing. The error bars represent the 95% confidence interval of the values obtained.

In summary, this section examined the effects of atmosphere, measurement sweep setup, light conditions, and annealing on the extracted electrical properties of 2D MoS_2-based FETs. Based on the findings and practical considerations, it was concluded that the optimal protocol for reliable, comparable results involve conducting measurements in a dark, argon environment with a V_{gs} sweep between – 80 to + 80 V and a step size of 2 V. At least three measurements at each condition should be taken with a 180-second interval. This protocol is followed throughout the remainder of this thesis, unless otherwise stated.

6.4 Discussion

Section 6.3 explored the effects of various extrinsic factors on the electrical properties of 2D MoS_2. Systematic changes in the V_{th}, V_{hys} and μ_{FE} were observed under varying environmental conditions. The origins of such changes are proposed to be a combination of air adsorbates and charge transfer from the dielectrics.

Figure 6.4.1 shows the band diagrams of the gate-dielectric-2D MoS_2 system during transfer curve measurements conducted in argon and air atmosphere. In an argon atmosphere, as V_{gs} increases, excess electrons are injected into the channel via field-effect, enhancing conductivity. This leads to a turn-on current

at point (a), as shown in Figure 6.4.1 (d). In contrast, when measurements are performed in air, adsorbates such as water and O_2 molecules can bind to the channel surface, introducing trap states. The acceptor nature of O_2 molecules have also been demonstrated in [274]. These acceptor states can capture the excess electrons injected by field-effect, resulting in a reduced conductivity at the same V_{gs} and a lower I_{ds} at point (b) compared to point (a). Additionally, the physically bonded adsorbates can act as scattering centres, further diminishing channel conductivity. It is hypothesised that the energy level of these acceptor states is lower in their charged state compared to their neutral state. Consequently, during the backward scan, more electrons are trapped at the same V_{gs} than during the forward scan, resulting in a clockwise hysteresis. This leads to a further reduction in I_{ds}, with point (c) showing a lower current compared to point (b). Measuring devices in an argon environment largely eliminates adsorbate-related trap states, resulting in higher I_{ds} and reduced hysteresis in the transfer characteristics.

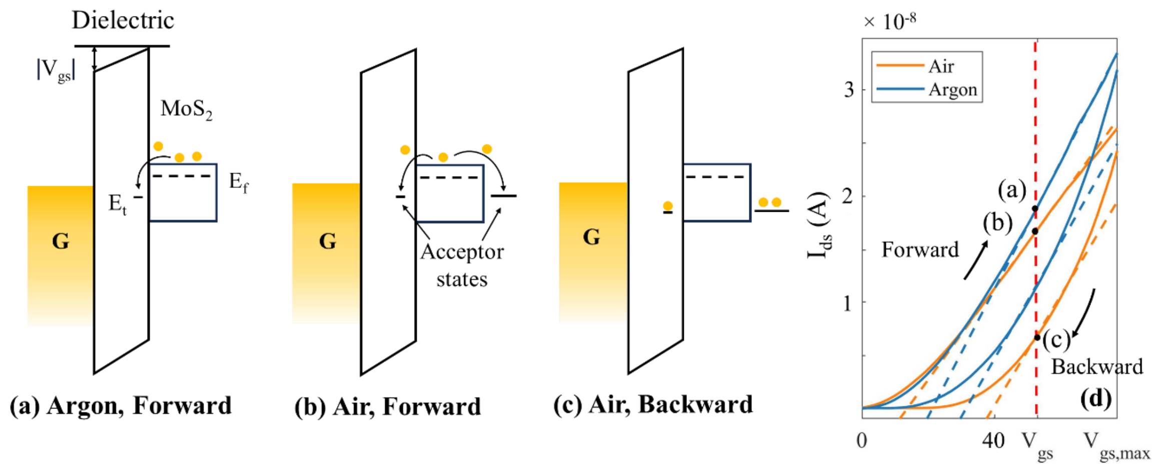


Figure 6.4.1 Band diagrams during (a) forward bias in argon, (b) forward bias in air, (c) backword bias in air, and (d) schematic illustration of the transfer curves. Numerical scales are partially omitted for clarity, as the full quantitative data presented in Figure 6.3.1.

It was observed that substantial hysteresis remains even when measurements were conducted in an argon atmosphere. This hysteresis is unlikely to originate from residual adsorbates in the environment, as a similar level of hysteresis was observed by measuring samples in vacuum (5×10^{-6} Torr), as shown in Section 6.3.4. It is proposed that, in addition to the acceptor states introduced by air adsorbates, trap states exist near the dielectric surface or at the channel-dielectric interface, as shown in Figure 6.4.1. The origin of these states could be related to PDMS residues, which can be removed through annealing, leading to higher I_{ds}, as demonstrated in Section 6.3.4. Additionally, these acceptor states may arise from dangling bonds at the dielectric surface or within the bulk material. These trap states capture electrons, and their Coulomb interactions with the positively charged ions in MoS_2, further contributing to the degradation of channel mobility [275]. The presence of these states could account for the hysteresis observed even after annealing.

Donor states are also likely to be present at the interface and alter the transfer characteristics. As demonstrated in Section 6.3.2, applying a larger negative V_{gs} led to a left shift in the V_{th}, indicating excess electrons within the channel. This shift occurred despite the additional measured points, which were found to

reduce channel mobility. The band diagrams of two measurements with different minimum V_{gs} values V_1 and V_2, where $V_1 < V_2 < 0$, is shown in Figure 6.4.2 (a-c), with exemplary transfer curves shown in Figure 6.4.2 (d). As illustrated in Figure 6.4.2 (a), when V_{gs} is at a high negative value, the strong electric field facilitates the injection of electrons from donor states located in the dielectric bulk and/or at the dielectric-channel interface. Meanwhile, for a measurement with a minimum V_{gs} of V_2 (Meas 2), fewer electrons are injected, resulting in lower I_{ds} at the same V_{gs} compared to a measurement with a minimum V_{gs} value of V_1 (Meas 1), as shown in Figure 6.4.2 (b) and (c). Overall, higher applied negative V_{gs} leads to higher I_{gs}, and thus a left shift in V_{th}.

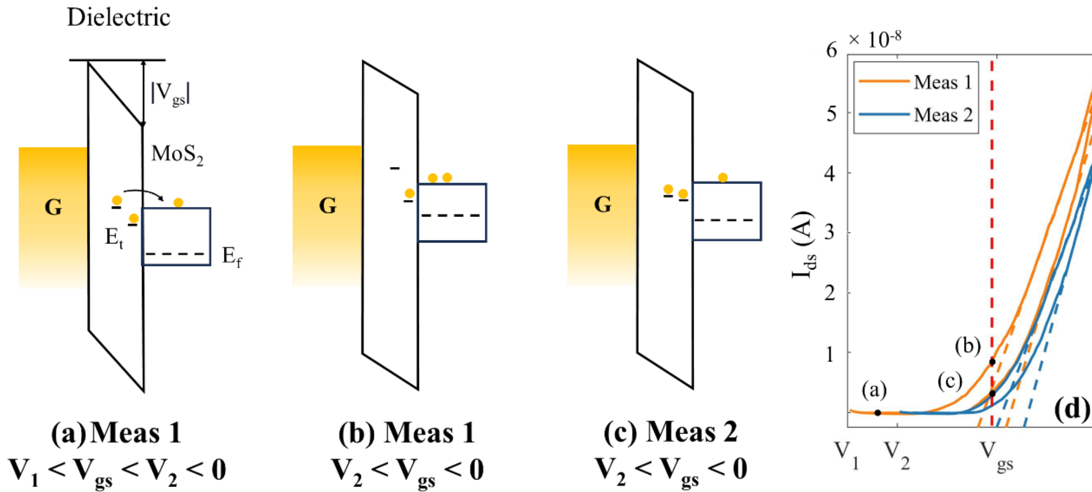


Figure 6.4.2 Band diagrams for (a) Meas 1 at $V_1<V_{gs}<V_2$, (b) Meas 1 at $V_2<V_{gs}$ and (c) Meas 2 at $V_2<V_{gs}$. Meas 1 has a more negative V_{gs} starting value of V_1 than Meas 2, which starts from V_2. Exemplary transfer curves are shown in (d), with the points corresponding to (a-c) marked. Numerical scales are partially omitted for clarity, as the full quantitative data presented in Figure 6.3.3.

Finally, the effects of illumination are discussed, which was found to shift both V_{th1} and V_{th2} towards more negative values, with an increase in V_{hys} and a decrease in μ_{FE}. Band diagrams under illumination and in dark and their corresponding I_{ds} in the transfer curve is shown in Figure 6.4.3. The changes in threshold voltages under illumination are analogous to that observed when a larger negative V_{gs} is applied, as discussed above. Indeed, in both cases, excess carriers are generated in the channel, which led to increased I_{ds} under the same V_{gs}, as shown in Figure 6.4.3 (c). Under illumination, the excess carrier is generated by the incident photons, which excites valence band electrons to the conduction band and contribute to channel conductance, as shown in Figure 6.4.3 (a). The decreased μ_{FE} can be explained by the increased scattering due to the elevated temperature under illumination.

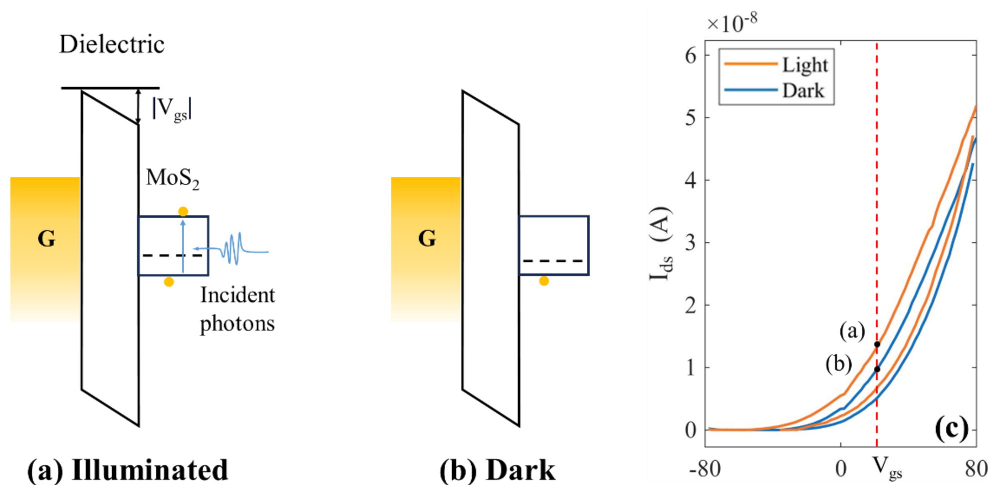


Figure 6.4.3 Band diagrams for MoS_2 FET (a) under illumination and (b) in darkness. Exemplary transfer curves are shown in (c), with the points corresponding to (a-b) marked. Numerical scales are partially omitted for clarity, as the full quantitative data presented in Figure 6.3.5.

The long-term stability of the MoS_2-based FETs was not systematically investigated in this work. Nevertheless, previous studies have reported that MoS_2 flakes undergo noticeable oxidation after approximately 110 days when stored under ambient conditions, whereas minimal degradation was observed when stored in vacuum [276]. In this work, all fabricated devices were stored in a dark vacuum box (~650 Torr) with repeated purging using dry N_2 and vacuum cycling to minimise the presence of water and oxygen. Under these storage conditions, the devices were expected to retain their performance for several months with negligible changes, which was sufficient to ensure the acquisition of comparable data.

6.5 Summary

This chapter presented an all-dry protocol for the fabrication of 2D MoS_2 FETs. The key steps involve the fabrication and alignment of evaporation masks with the exfoliated flakes to form front contacts. TEM grids attached to magnetic washers were used as masks to achieve clean, fast, and reliable fabrication of the devices. [276]Strategies to enable the fabrication of multiple devices in a single process were also demonstrated. The developed protocol has been shown to yield an average of 6 devices in a single process. More importantly, full preservation of the charge in the dielectric was demonstrated, providing a foundation for the study of field-effect doping in Chapter 7.

The effects of extrinsic factors, including air adsorbates, measurement settings and light conditions, on the electrical properties of 2D MoS_2 FETs have been systematically investigated. Measurements in argon environment were found necessary in reducing device variations and revealing the intrinsic properties of 2D MoS_2 channel. Meanwhile, appropriate settings for the measurement range, step size, and light conditions have been selected considering both their effects on the properties of 2D MoS_2 and practical reasons. Annealing in argon and vacuum have been found to further mitigate the effects of adsorbates. However, considering the time cost of annealing and its relatively limited effects, it was not included in the measurement protocol. A measurement protocol to minimise hysteresis and device variations have been established. Comprehensive

models to account for the observed hysteresis and its changes under different conditions were proposed, highlighting the effects of charge trapping and de-trapping of defect states.

Chapter 7
Field-Effect Doping of 2D MoS_2

7.1 State of the Art Doping of 2D MoS_2

Controllable and selective doping of semiconductors is crucial in enabling precise tuning of the channel conductance and optimising device performance. Substitutional doping using ion implantation, the default method for bulk semiconductors (eg. Si, Ge), is not applicable for 2D materials as the atomically thin structure will be destroyed when exposed to high-energy ions [277]. Therefore, various doping methods have been recently developed, including (1) "bottom-up" substitutional doping; (2) charge transfer doping; and (3) field-effect doping.

Substitutional doping involves the replacement of a lattice atom by an electron donor or acceptor. "Bottom-up" substitutional doping of 2D MoS_2 is usually carried out during the synthesis process, where foreign atoms are introduced to replace molybdenum (Mo) or sulphur (S). This method introduces permanent doping without destroying the 2D structure. Niobium (Nb) atoms introduced during the chemical vapour deposition (CVD) process have been reported to achieve p-type doping densities as high as ~10^{19} cm^{-3} [278]. Besides Mo substitution, the sulphur anion can also be replaced with electron acceptors such as nitrogen (N) using molybdenum chloride ($MoCl_5$) and thiourea as precursors [279], or with a N_2 plasma [280]. Meanwhile, n-type doping of 2D MoS_2 has been demonstrated with manganese (Mn) [281] and rhenium (Re) atoms [282]. However, a degradation in carrier mobility has been observed due to increased scattering from dopants. Furthermore, as dopants are incorporated during film synthesis, achieving controlled and area-selective doping is challenging [283]. These disadvantages make substitutional doping less suitable for high-performance transistors.

Charge transfer from chemically or physically surface-absorbed molecules on the 2D MoS_2 surface has also been demonstrated as an effective doping strategy. Strong electron donors such as polyethyleneimine (PEI) [103], [104] and benzyl viologen (BV) [107] have been reported to induce n-doping in 2D MoS_2, while $AuCl_3$ solution, molecular reductants and oxides, and organosulfur compounds, have been reported to induce p-doping [105], [106]. However, the stability of the chemical species and the doping effect remain a concern for this method along with the reduced mobility due to scattering from the surface adsorbates [103], [284].

Charge transfer doping from dielectric defects has emerged as a promising doping strategy. As discussed in Chapter 1, carriers in 2D MoS_2 can transfer to interface defect states in dielectrics and achieve doping without disturbing the 2D structure. Additionally, due to the long distance between the charged defect and

channel carriers, scattering due to Coulomb interactions is reduced, leading to minimal loss in mobility [112]. Area selective doping was demonstrated, with a spatial resolution of ~200 nm with a doping density of ~10^{12} cm^{-2} using an electron beam, enabling charge transfer between 2D MoS_2 and defects in the neighbouring hexagonal boron nitride (hBN) and SiO_2 [285], as shown in Figure 7.1.1 (a)-(b). However, encapsulation with hBN was found to be necessary to protect the 2D MoS_2 from the electron beam. Degradation in mobility was found under high-energy beam exposure used to induce high doping density of ~10^{13} cm^{-2}.

Field-effect doping is an underexplored strategy for tuning conductivity in 2D MoS_2. While the concept of field-effect doping is widely utilised in the operation of field-effect transistors (FETs), its application is limited by the need for a constant external voltage [286]. Other sources of electric field have been explored. Mallik et al. reported n-doping of 2D MoS_2 using sodium ions incorporated into SiO_2 during CVD growth [267], [287], as shown in Figure 7.1.1 (c)-(d). More recently, O'Sullivan et al. demonstrated a >60% of reduction in graphene sheet resistance using corona charge, where the charge carrier in graphene can be switched from electrons to holes depending on the polarity of the corona charge [288]. Additionally, air-stable n-doping of WSe_2 was achieved using SiN_x, where the electron sheet density increased with the NH_3/SiH_4 ratio, corresponding to a higher positive charge density in the SiN_x layer [289]. However, p-type field-effect doping on 2D TMDs using a dielectric system, which can be readily integrated into device structures, remains largely unexplored.

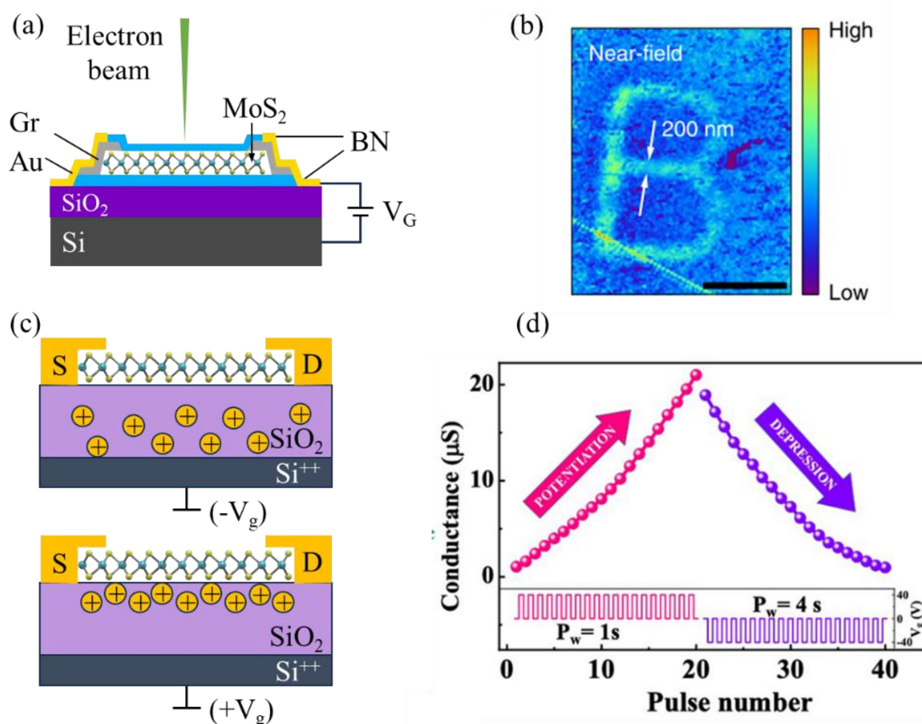


Figure 7.1.1 (a) charge transfer from interface defects, demonstrating (b) a doping resolution of 200 nm. (a)-(b) reproduced from [285]. (c) field-effect doping via mobile ions SiO_2, demonstrating (d) multilevel non-volatile memory. (c)-(d) reproduced from [267].

In this Chapter, field-effect doping of 2D MoS_2 using charged dielectric is presented. The channel mobility is proposed to be maintained due to the complete preservation of the 2D MoS_2 structure. The charges are embedded more than 5 nm beneath the dielectric surface, away from MoS_2, prior to device fabrication, which results in limited Coulomb interactions. In principle, high doping density and area selective doping of 2D MoS_2 can be achieved by engineering the charge density and distribution in the dielectric. This approach offers a promising doping strategy, which is critical in incorporating 2D MoS_2 in the next-generation electronic and optoelectronic devices.

7.2 Field-Effect Doping via a Virtual Top Gate

To verify the concept of field-effect doping using charged dielectrics, corona charge was deposited on a top-gate dielectric to modulate carrier densities in the 2D MoS_2 channel. Polymethyl methacrylate (PMMA) was used as the dielectric to retain the charge. The stability of corona charge on PMMA was first investigated. After depositing ~ 500 nm PMMA on a Si substrate (Set 1), negative corona charging was deposited for 30 seconds, and the degradation of the surface charge density was monitored using Kelvin probe (KP) at room temperature, in air. The change in contact potential difference (CPD) is shown in Figure 7.2.1. The sudden increase in CPD value is likely due to an unintended disturbance of the table, causing a change in the probe-to-sample distance. A CPD value of ~50 V, which is equivalent to a charge density of ~10^{12} q cm^{-2}, can be retained for more than 10 minutes. This enables the investigation of field-effect doping of 2D MoS_2 using charged PMMA as a virtual top gate.

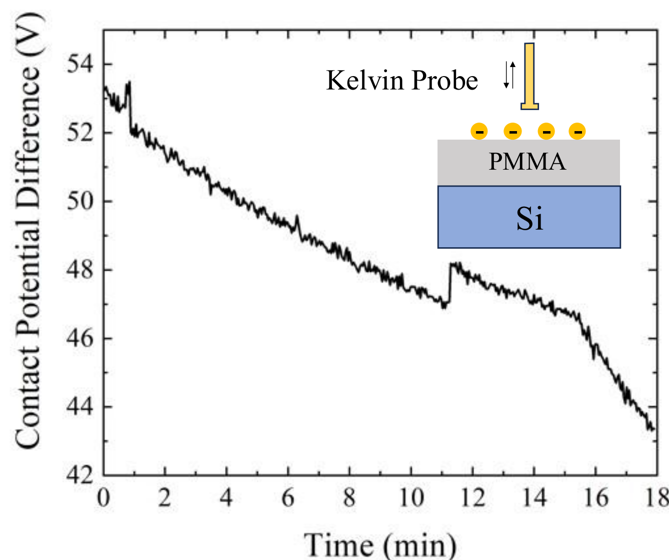


Figure 7.2.1 Degradation of the CPD values of negative corona charge on PMMA.

To modulate the carrier densities in 2D MoS_2, an FET device with a PMMA capping layer was fabricated. The device was first prepared on a substrate with a 300 nm-thick thermal SiO_2, capped with 50 cycles of ALD-HfO_x (Set 6-C). Silver dag were applied to form durable contacts and dried in air for 12 hours. PMMA was then spin coated and annealed as above. A schematic of the device with a top PMMA layer is shown in Figure

7.2.2. Negative or positive corona charge was deposited for 20 seconds at room temperature, and the surface charge density was estimated from KP measurements. The dielectric constant of PMMA is taken to be 3.9 [290].

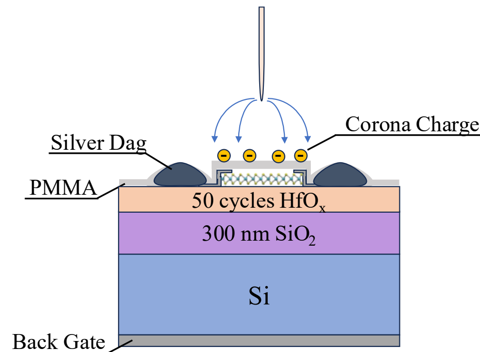


Figure 7.2.2 Schematics of a 2D MoS_2 device with PMMA as top gate dielectric. Silver dag is applied as durable contacts. Negative corona charge was deposited at room temperature on the PMMA.

After each deposition of corona charge, transistor transfer curves were obtained in air under dark conditions. The V_{gs} sweep range was –60 V to +60 V, with a step size of 2 V, and V_{ds} at 0.01 V. The effects of air adsorbates are expected to be minimal due to the protection provided by PMMA [291]. Two measurements were taken after each corona charge deposition. The time between the deposition of corona charge to the end of the second transfer measurement is 10±1 minutes. Only the last transfer curves obtained after each corona charge deposition is shown in Figure 7.2.3 (a-b) for clarity. The extracted V_{th1} and CPD values after each corona charge deposition are shown in Figure 7.2.3 (c).

Minimal hysteresis was observed in all transfer curves obtained, which indicates the protection of the channel from extrinsic adsorbates in air. With the deposition of negative/positive corona charge, the V_{th1} systematically increase/decrease, as shown in Figure 7.2.3. This suggests an injection of holes/electrons due to field-effect from the corona charge on PMMA. It is noted that the backward transfer curve measured after 60 seconds of positive corona anneal (dark orange in Figure 7.2.3) presents an abnormal curve shape, which could be the result of channel degradation after repeated measurements, or PMMA degradation due to charging. These results demonstrate the control of channel carrier density via the deposition of corona charge through a top gate dielectric.

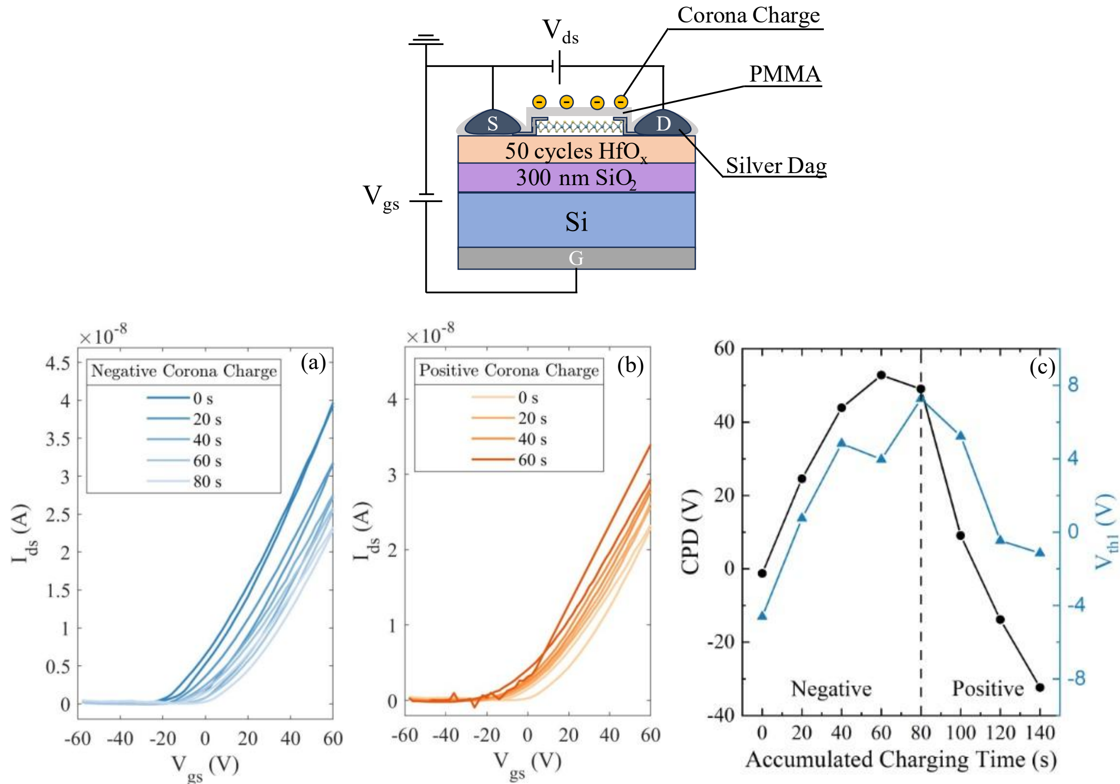


Figure 7.2.3 Transfer curves of the last measurements taken with the deposition of (a) negative corona charge, (b) positive corona charge, and (c) the extracted V_{th1} and the CPD values measured after each corona charge deposition.

To quantitively analyse the changes in carrier densities due to field-effect, corona charge density on the PMMA (Q_{corona}) and effective electron density in 2D MoS_2 (n_{el}) after each charge deposition are calculated from Equation (2.4.12) and Equation (1.4.3), respectively. The extracted values of Q_{corona} and n_{el} are plotted in Figure 7.2.4. The extracted slope characterising the charge density changing rate of Q_{corona} and n_{el} and the R-squared values for the fitting are shown in Table 7.2.1.

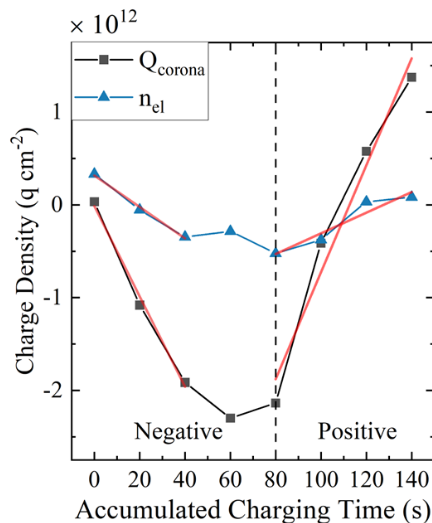


Figure 7.2.4 calculated channel electron density n_{el} and surface corona charge density Q_{corona} following each deposition of corona charge on PMMA. The red lines indicate the linear fit to extract the charge density changing rate for Q_{corona} and n_{el}.

Table 7.2.1 Extracted slopes and R-squared from the changes in Q_{corona} and n_{el} with corona charge deposition time.

Corona Charge	Negative		Positive	
Fitting	Q_{corona}	n_{el}	Q_{corona}	n_{el}
Slope (10^{10} q cm^{-2} s^{-1})	-4.9	-1.7	5.8	1.1
R-squared	0.99	0.99	0.97	0.92

In the initial 60 seconds of charging, the deposition of negative corona charge is linear, with an average rate of 4.9×10^{10} q cm^{-2}s^{-1}. A linear decrease in the n_{el} was also observed at an average rate of 1.7×10^{10} q cm^{-2}s^{-1}. The disparity between these values can be partially attributed to the instability of corona charge on PMMA. A decrease of $\sim 1.2 \times 10^{10}$ q cm^{-2}s^{-1} in the average deposition rate is estimated due to the 10-minute interval between corona charge deposition and transfer measurements. In addition to corona charge degradation, defects at the 2D MoS_2/PMMA interface likely contribute to the disparity between Q_{corona} and n_{el}. Changes in the 2D MoS_2 Fermi level due to field-effect doping can cause these interface states to become charged/uncharged. These defects do not contribute to channel conductivity and effectively screen out the electric field induced by the surface corona charge.

With corona charge deposition time longer than 60 seconds, a deviation from the initial linear trend was observed. It is likely that the PMMA film quality starts to degrade due to the high charge density, as evidenced by the smaller increases in the CPD values after each corona charge deposition.

With the deposition of positive corona charge, Q_{corona} exhibited an average deposition rate of 5.8×10^{10} q cm^{-2}s^{-1}, while n_{el} increased at a rate of 1.1×10^{10} q cm^{-2}s^{-1}. The previously proposed corona charge instability and interface states can similarly account for the discrepancy between these values. The larger disparity observed compared to the initial charging stage, along with the lower R-squared values, may be attributed to PMMA degradation resulting from prolonged charging.

In summary, this section demonstrates the control of 2D MoS_2 carrier density using corona charge on PMMA as a virtual top gate. The results provide proof of the concept proposed in this work: control of the carrier density of 2D MoS_2 using charged dielectrics. However, charged PMMA was found to be unstable, and thus has limited applications. The instability of corona charges on PMMA is mainly attributed to the lack of deep states [292]. A more reliable doping solution is explored next.

7.3 Interactions between 2D MoS_2 and Dielectrics

Charged dielectrics utilising embedded charged defects are a promising approach to achieve permanent and controllable doping in 2D MoS_2. In Chapter 3, charged dielectrics capped with SiO_x, AlO_x and HfO_x have been developed. The embedded charges are likely to reside more than 5 nm beneath the surface, minimising direct charge transfer between the charged defects and 2D MoS_2 [112], [118]. However, other interactions, such as dielectric screening [102] and charge transfer between the channel and defects near the dielectric surface or at the interface [108], [112], have been reported to influence hysteresis, doping density, and carrier mobility in

2D MoS_2. Therefore, it is crucial first to isolate the effects of different capping layer dielectrics in uncharged dielectric stacks.

To investigate how different capping layer dielectrics affect the properties of 2D MoS_2 FETs, substrates capped with SiO_x, AlO_x, and HfO_x were fabricated. Schematics for the substrates used for this study are shown in Figure 7.3.1. Set 6-A includes samples with 20 cycles of ALD AlO_x, followed by 360 cycles of and ALD SiO_x as the capping layer. The samples were annealed at 800 ºC for 30 minutes prior to device fabrication to improve the quality of both ALD-SiO_x and the substrate SiO_2, as explained in Appendix C. The substrates were then annealed at 450 ºC for 4 minutes in air to simulate the heating during a charging process. This enables a comparable surface defect condition with devices on charged dielectrics. For samples with an AlO_x capping layer, substrates were annealed at 800 ºC for 30 minutes prior to depositing 100 cycles of AlO_x (Set 6-B). The substrate was then annealed at 450 ºC for 4 minutes in air to simulate the heating treatment during a charging process. For samples with an HfO_x capping layer, substrates were annealed at 800 ºC for 30 minutes before depositing 50 cycles of HfO_x (Set 6-C).

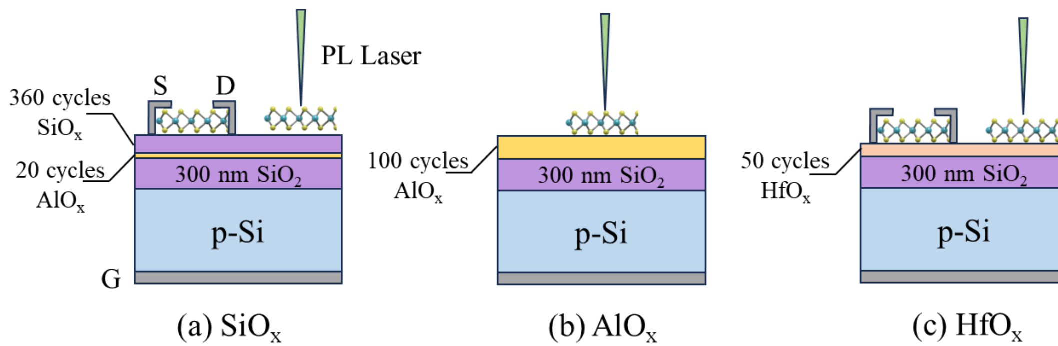


Figure 7.3.1 Diagrams of the substrates used with capping layers of (a) ALD-SiO_x, (b) ALD-AlO_x, and (c) ALD-HfO_x.

2D MoS_2 FETs were fabricated on SiO_x and HfO_x-capped substrates following the all-dry fabrication protocol described in Chapter 6. All devices were measured in an argon atmosphere under dark conditions. The V_{gs} sweep range was set to –80 to +80 V, with a step size of 2 V, and V_{ds} at 0.01 V. At least three measurements were taken on each device, with a 180-second interval between each measurement. The extracted V_{th1}, V_{hys} and μ_{FE} from the last measurements are shown in Figure 7.3.2. The last measurement is chosen as it avoids transient changes in the channel properties and is least affected by exposure to air and light during acquisition. At least four devices were measured in each group. The means ± SDs for each group and the Welch two-sample comparisons of the mean difference (Δ=HfO_x − SiO_x) reported as two-sided 95% confidence intervals (CI) are listed in Table 7.3.1.

For the V_{th1}, devices on SiO_x averaged 31.83 ± 7 V and devices on HfO_x averaged 16.41 ± 19.80 V. Despite of the lower mean of V_{th1} for devices on HfO_x, the 95% CI for Δ included 0, so a shift in V_{th1} was not resolved at the 5% level. A larger mean hysteresis was found on devices on HfO_x (9.70 ± 2.58) compared to SiO_x (5.92 ± 2.65), with the 95% CI marginally overlaps 0, making a difference not resolved at the 5% level, but consistent with a trend at the 10% level. This suggests a larger extent of unintentional doping, likely

originating from defects near HfO_x surface or at the 2D MoS_2/HfO_x interface. Field-effect mobilities are comparable between substrates (SiO_x 15.02 ± 6.59 $cm^2\ V^{-1}\ s^{-1}$, HfO_x 13.89±4.82 $cm^2\ V^{-1}\ s^{-1}$), with the corresponding CI also including 0. The obtained μ_{FE} is found comparable to the values obtained in the literature [293], [294], suggesting the use of good quality channels in this work. Taken together, within the present sample size and variance the data do not establish dielectric-dependent changes in V_{th1}, V_{hys}, or μ_{FE} and the observed trends should therefore be regarded as suggestive.

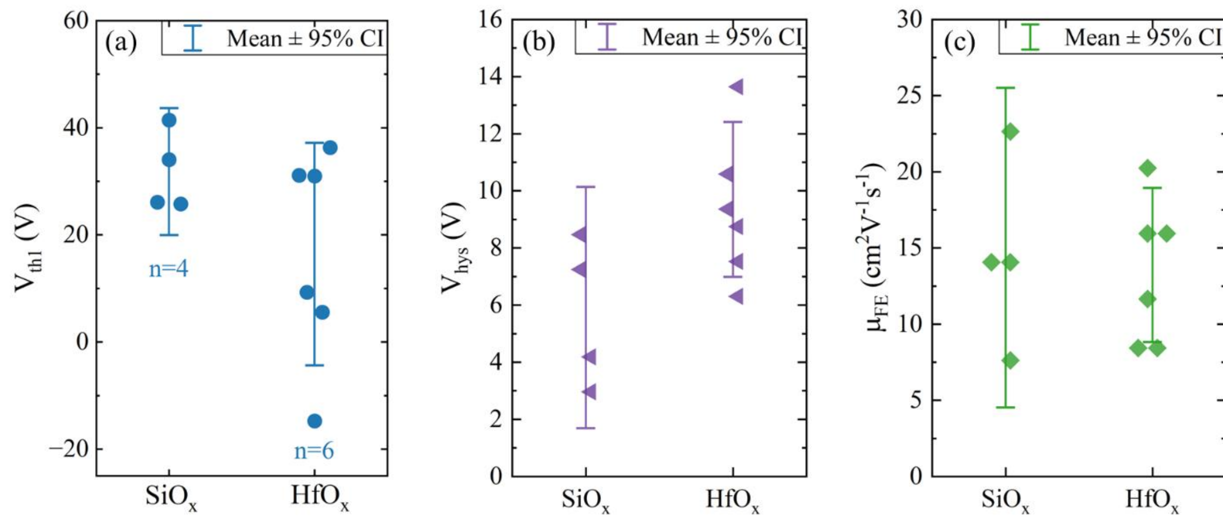


Figure 7.3.2 The extracted (a) V_{th1}, (b) V_{hys} and (c) μ_{FE} from 2D MoS_2 FETs fabricated on dielectrics with different substrates and capping layers. The error bars represent the mean ± 95% confidence interval (CI).

Table 7.3.1 Summary of mean ± SD and mean differences (Δ=HfO_x − SiO_x) with two-sided 95% Welch CIs for V_{th1}, V_{hys}, and μ_{FE}. A CI including 0 indicates the difference is not established at the 5% level.

Property	Sample Group	Mean ± SD	95% CI for Δ
V_{th1} (V)	SiO_x	31.83 ± 7.46	[-8.86, 39.69]
	HfO_x	16.41 ± 19.80	
V_{hys} (V)	SiO_x	5.92 ± 2.65	[-7.67, 0.10]
	HfO_x	9.70 ± 2.58	
μ_{FE} ($cm^2\ V^{-1}\ s^{-1}$)	SiO_x	15.02 ± 6.59	[-7.13, 9.39]
	HfO_x	13.89 ± 4.82	

Various factors, including gate control, contact resistance and interface states, have been suggested to affect the properties extracted from transfer curves [108], [295]. To further reveal the intrinsic properties of 2D MoS_2 interfacing to different dielectrics, photoluminescence spectroscopy (PL) was conducted, complementing the transfer measurements. Substrates capped with SiO_x, AlO_x, and HfO_x were prepared as described previously. 2D MoS_2 flakes were transferred onto the substrates and measured in air at room temperature to obtain their PL spectra. At least four monolayer flakes were measured on each substrate. This sampling was adequate because the flake-to-flake dispersion in the dry-exfoliated monolayers was small, with

further details on spatial variability provided in Appendix H. Optical microscope images of the flakes measured are provided in Appendix **Error! Reference source not found.**, demonstrating minimal PDMS residue. The individual PL spectra of the flakes obtained on each substrate are shown in Figure 7.3.3. The individual and the averaged spectra were fitted to a Lorentzian function [163], and peaks at 1.85, 1.89 and 2.03 eV (±0.01 eV) were attributed to be A^-, A^0 and B^0 excitons respectively. Lorentzian functions were adopted in this thesis as homogeneous broadening yields a Lorentz profile, whereas inhomogeneous and instrumental effects produce Gaussian broadening [296]. In this thesis, adding a Gaussian component (Voigt function) did reduce residuals, however the split between its Lorentzian and Gaussian parts is poorly defined and thus lead to variations in the extracted results. The choice of fitting function is further discussed in Appendix J. The averaged spectra together with the individual fitted peaks are also included in Figure 7.3.3 for visual comparison. Averaging is appropriate here as the fitted peak energies exhibit only small device-to-device dispersion (<0.01 eV), so the averaging does not distort the line shapes [297].

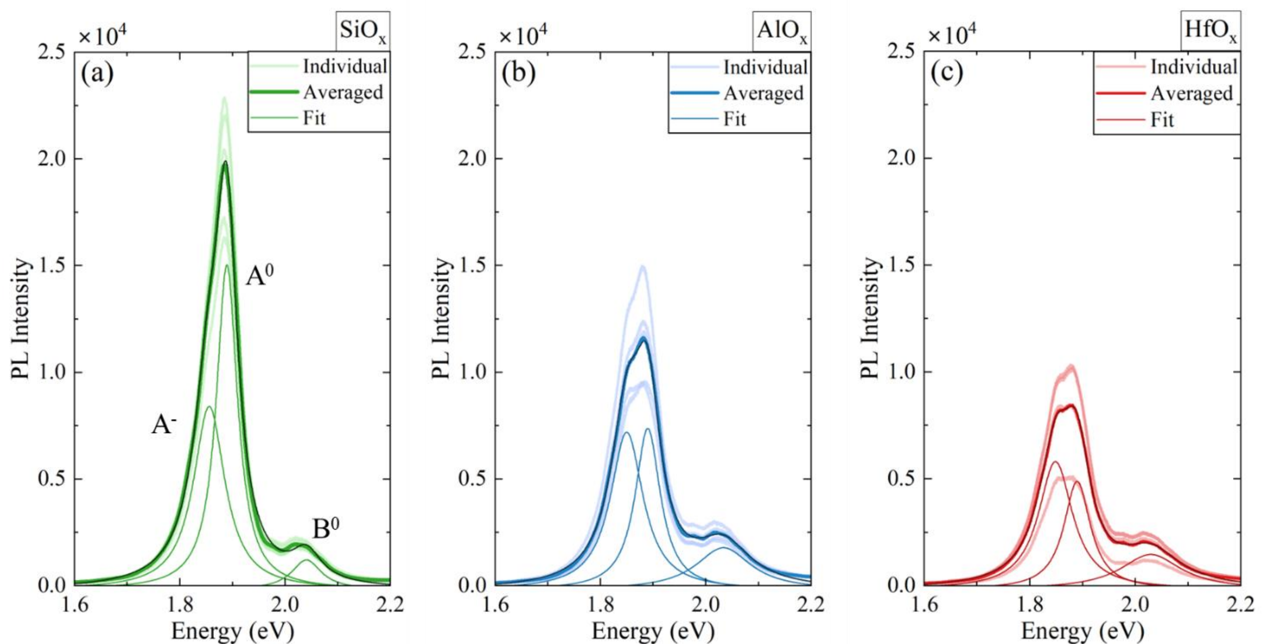


Figure 7.3.3 Photoluminescence spectra of flakes on substrates capped with (a) SiO_x, (b) AlO_x, and (c) HfO_x. The light-coloured curves represent the obtained data of individual flakes, while the dark-coloured curves represent the averaged spectra and their Lorentzian fit.

In general, flakes on AlO_x and HfO_x exhibited lower PL intensities and broader A peaks than those on SiO_x. This trend is consistent with an increased A^- trion fraction relative to the neutral A^0 exciton, indicative of higher electron densities [298]. To quantitively analyse doping across 2D MoS_2 on different dielectrics, the trion-to-exciton area ratio (I_A^-/I_A^0) was calculated per flake. The distributions for I_A^-/I_A^0 are shown in Figure 7.3.4. The means ± SDs for each group and the Welch two-sample comparisons of the mean difference (Δ_1=AlO_x − SiO_x, Δ_2=HfO_x − SiO_x, and Δ_3=HfO_x − AlO_x) reported as two-sided 95% confidence intervals (CI) are listed in Table 7.3.2.

Distinct I_{A^-}/I_A^0 values were obtained on the three dielectrics. Using Welch two-sample comparisons and the sign convention in Table 7.3.2, the 95% CIs for Δ_1 and Δ_2 are entirely below zero, demonstrating that both AlO_x and HfO_x have higher I_{A^-}/I_A^0 than flakes on SiO_x. The PL spectra support the transfer measurements, which indicate higher electron density in flakes on HfO_x than on SiO_x. In contrast, the CI for Δ_3 ([-0.67, 0.12]) includes zero, so the doping density difference between flakes on HfO_x and AlO_x is not resolved at the 5% level.

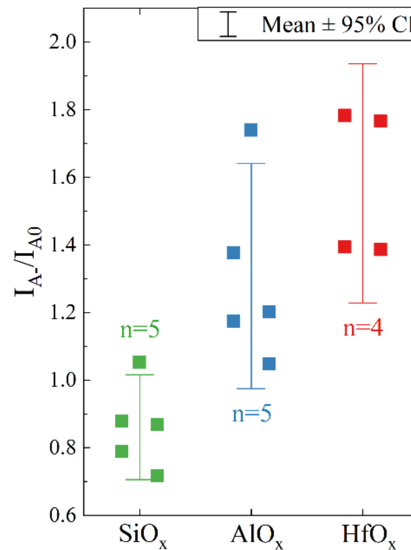


Figure 7.3.4 The extracted ratio of areas under peak A^- and A^0 (I_{A^-}/I_A^0) of flakes on substrates capped with SiO_x, AlO_x, and HfO_x. The error bars represent the mean ± 95% confidence interval (CI).

Table 7.3.2 Summary of mean ± SD and mean differences (Δ_1=AlO_x − SiO_x, Δ_2=HfO_x − SiO_x, Δ_3=HfO_x − AlO_x) with two-sided 95% Welch CIs for I_{A^-}/I_{A0}. A CI including 0 indicates the difference is not established at the 5% level.

Sample Group	Mean ± SD	95% CI for Δ_1	95% CI for Δ_2	95% CI for Δ_3
SiO_x	0.86 ± 0.13			
AlO_x	1.31 ± 0.27	[-0.75, -0.14]	[-1.00, -0.45]	[-0.67, 0.12]
HfO_x	1.58 ± 0.22			

7.3.1 Discussion

The effects of interfacial dielectrics on the properties of 2D MoS_2 were investigated using a combination of transfer measurements and PL. Differences were observed in both the average doping densities and their degree of variations in 2D MoS_2 flakes on SiO_x, AlO_x, and HfO_x-capped substrates. In all groups, the capping dielectric layer is thicker than 5 nm, and the changes in the channel properties are likely due to its interactions with the defects near the dielectric surface and at the 2D MoS_2/dielectric interface [109], [110], [111], [118].

In both transfer measurements and PL spectra, a higher electron density is observed in 2D MoS_2 on AlO_x and HfO_x compared to SiO_x. This aligns with previous reports, where an n-type channel is generally observed

in devices using AlO_x and HfO_x as gate dielectrics [112], [130], while both n-type and p-type conduction has been reported in devices using SiO_x [131], [132]. The origin of the doping has been proposed to be oxygen vacancies, whose energy level lies right above the conduction band minimum (CBM) [130]. Variations in oxygen vacancy density near the dielectric surface are proposed to contribute to the observed differences in doping densities of 2D MoS_2 on different dielectrics. The highest electron density was observed in 2D MoS_2 on HfO_x, which had no additional annealing prior to device fabrication. A slightly lower n-type doping density was observed in 2D MoS_2 on AlO_x, which was annealed at 450 ºC for 4 minutes in air. For both dielectrics, a high density of oxygen vacancies is likely to reside near the dielectric surface, which donates electrons to the neighbouring 2D MoS_2. Meanwhile, SiO_x-capped substrates were annealed at 800 ºC for 30 minutes in air before device fabrication. This annealing process is likely to remove the oxygen vacancies, leading to an absence of strong n-type doping in 2D MoS_2. Oxygen vacancies have also been proposed to form mid-gap states at the 2D MoS_2/dielectric interface, which increases hysteresis and variations in doping densities, as observed in 2D MoS_2 on HfO_x [299].

Next, the carrier density extracted from transfer measurements and PL spectra are analysed quantitatively. While an increased (decreased) electron (hole) density was observed in 2D MoS_2 on HfO_x compared to SiO_x in both transfer measurements and PL spectra, the polarity of the channel, as well as the extracted carrier density values are significantly different for the two techniques. Positive V_{th1} was observed for the majority of devices on both SiO_x and HfO_x, indicating p-type doping. Average channel hole density is calculated to be 2.32 and 1.21 × 10^{12} q cm^{-2} for devices on SiO_x and HfO_x, respectively, according to Equation (1.4.3). Meanwhile, the strong A^- peak identified in 2D MoS_2 on HfO_x indicates n-type doping. Average electron density is calculated to be 2.79 and 5.11 × 10^{13} q cm^{-2} for 2D MoS_2 on SiO_x and HfO_x, respectively, according to Equation (2.4.13). The origin of the p-type behaviour observed in transfer measurements and the large discrepancy between the extracted carrier density values are discussed as follows.

First, it is noted that transfer curves and PL spectra were obtained under different experimental conditions. Transfer curves were measured in an argon atmosphere and under dark conditions, whereas PL spectra were acquired in air under laser illumination. As discussed in Chapter 6, experimental conditions for PL measurements can lead to unintentional charge transfer between 2D MoS_2 and air adsorbates. While exposure to air promotes H_2O and O_2 absorption, causing p-doping [274], laser illumination induces oxygen desorption, partially reversing this doping effect [300]. If the discrepancy between the two measurements were solely attributed to experimental conditions, the higher p-doping density observed in transfer measurements would imply significant air adsorption in an argon atmosphere. This is inconsistent with the observations in Chapter 6. Therefore, additional factors must be considered.

It is proposed that the p-type behaviour observed in transfer measurements is related to poor metal/channel interfaces. The extraction of carrier density from transfer curves relies on the turn-on feature of the channel. In a device with n-type channel and a defect-free source/drain-channel interface, an I_{ds} is measurable at V_{gs} = 0 V. However, in reality, contact resistance is present due to a poor metal/channel interface,

which arises from channel structure degradation, interface states, or work function mismatches [301], [302], [303]. A contact resistance comparable to the channel resistance can significantly reduce the I_{ds} and delay the device turn-on. This issue has been widely reported in 2D materials-based FETs, where a good quality interface (< 1 kΩ μm) requires careful contact engineering [94], [304]. Considering that the metal evaporation process in this work was not optimised, the p-type behaviour is likely to originate from the 2D-metal contact properties. Metal contacts are not required in PL measurements, which allows the revelation of the n-type behaviour of 2D MoS_2.

Additionally, defects at the 2D MoS_2/dielectric interface can delay the device turn-on. Schematics of the 2D MoS_2 channel turn-on process with and without interface states are shown in Figure 7.3.5. At a defect-free interface, as shown in Figure 7.3.5 (a), the device turns on at $V_{gs} = V_{gs1}$. However, in reality, defects are present at the dielectric-MoS_2 interface, as shown in Figure 7.3.5 (b). At the same V_{gs1}, the applied V_{gs} induces the filling of defect energy states in both the channel and at the interface, resulting in a reduced channel carrier density, and subsequently lower I_{ds}. The device stays in the off state until a larger $V_{gs}=V_{gs2}$ is applied to induce a comparable density of carriers in the channel, as shown in Figure 7.3.5 (c). Furthermore, the turn-on delay is more pronounced in 2D MoS_2 on HfO_x than on SiO_x, owing to a higher interface state density, which results in an underestimation of the doping density difference when extracted from transfer curves.

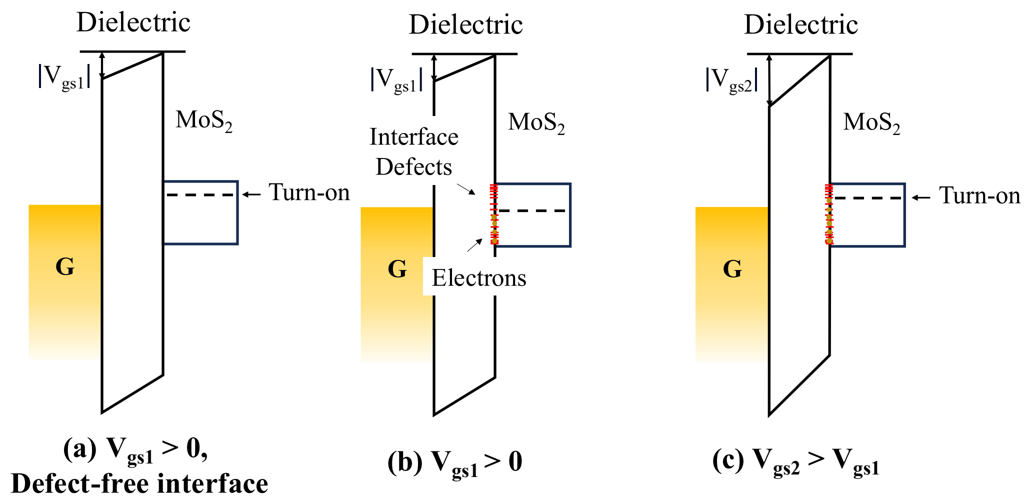


Figure 7.3.5 Schematics of (a) the turn-on point (V_{th1}) in an ideal FET device with a defect-free dielectric-MoS_2 interface, (b) where the same V_{th1} applied, but the device stays off due to filling of the interface states, and (c) delayed turn-on (V_{th2}) of FETs with interface states.

In summary, the observed differences in the doping density of 2D MoS_2 interfaced with different dielectrics are proposed to originate from oxygen vacancies near the dielectric surface, which donate electrons to the channel and induce n-doping. Such n-doping is less pronounced in 2D MoS_2 on SiO_x, likely due to the removal of oxygen vacancies during high temperature annealing (800 °C for 30 minutes). Furthermore, the 2D MoS_2/HfO_x interface is proposed to have a higher in-gap interface state density than the 2D MoS_2/SiO_x interface, as evidenced by the larger hysteresis observed. Both in-gap defect states and high contact resistance contribute to the delay in device turn-on, leading to the p-type behaviour observed in transfer measurements.

These in-gap defect states also cause the doping density difference between 2D MoS_2 on HfO_x and SiO_x to be underestimated in transfer measurements and overestimated in PL measurements. This results in significant discrepancies in the carrier densities extracted from the two characterisation techniques.

7.4 Field-Effect Doping using Charged Dielectrics

The previous section examined how 2D MoS_2 interfaced with different dielectrics affects channel doping density and hysteresis, along with potential misestimation of the doping densities extracted from transfer and PL measurements. Building on these insights, this section investigates the controlled modulation of doping density in 2D MoS_2 using charged dielectric stacks.

7.4.1 Charged Dielectric Capped with SiO_x

The uncharged dielectrics capped with SiO_x (Set 6-A) were fabricated as described as in Section 7.3. Prior to device fabrication, negative charges are injected into the dielectric by depositing negative corona charge for 30 seconds at room temperature, followed by annealing at 450 ºC for 1 minute (corona-anneal). This process was repeated four times, and the CPD values were measured to be 50~60 V on charged substrates. Assuming the charges are embedded at the SiO_x/AlO_x interface, the measured CPD values are equivalent to a charge density of –3.6 to –4.4 × 10^{12} q cm^{-2} according to Equation (2.4.12). 2D MoS_2 FETs were then fabricated on both uncharged and charged dielectrics following the all-dry protocol described in Chapter 6.

All devices were measured within 48 hours of the transfer of 2D MoS_2 to substrates. Measurements were performed in an argon atmosphere under dark conditions. To prevent possible degradation of the dielectric charges, the V_{gs} sweep range was set to 0 to +80 V, with a step size of 2 V. At least five measurements were taken on each device, with a 180-second gap between each measurement. Figure 7.4.1 shows the V_{th}, V_{hys} and μ_{FE} extracted from the last measurement taken on each device, which is the least affected by the exposure to air and light during measurement set-up. The means ± SDs for each group and the Welch two-sample comparisons of the mean difference (Δ=Charged − Uncharged) reported as two-sided 95% confidence intervals (CI) are listed in Table 7.4.1.

For V_{th1}, uncharged devices have an average value of 43.99 ± 4.78 V, while charged devices have an average value of 39.83 ± 7.43 V. The mean difference (Uncharged − Charged) was 4.16 V with a 95% CI that includes zero, thus a shift in V_{th1} was not resolved at the 5% level. Assuming both the embedded dielectric charges and the applied V_{gs} are fully mirrored into the 2D MoS_2 channel, an increase of 50~60 V in V_{th1} would be expected for devices on charged substrates, according to Equation (1.4.3) and Equation (2.4.12). The absence of this expected increase suggests: (1) a lack of excess holes mirroring into the 2D MoS_2 channel by the negatively charged dielectrics, (2) ineffective carrier density control by the applied V_{gs}, or a combination of both factors. In contrast, hysteresis increased on charged substrates, with the 95% CI for the mean difference entirely below zero. Consistent with enhanced charge trapping near the dielectric surface, the charged group

also shows larger SD in V_{th1}. Field-effect mobility was comparable between two groups with the 95% CI for the difference includes zero.

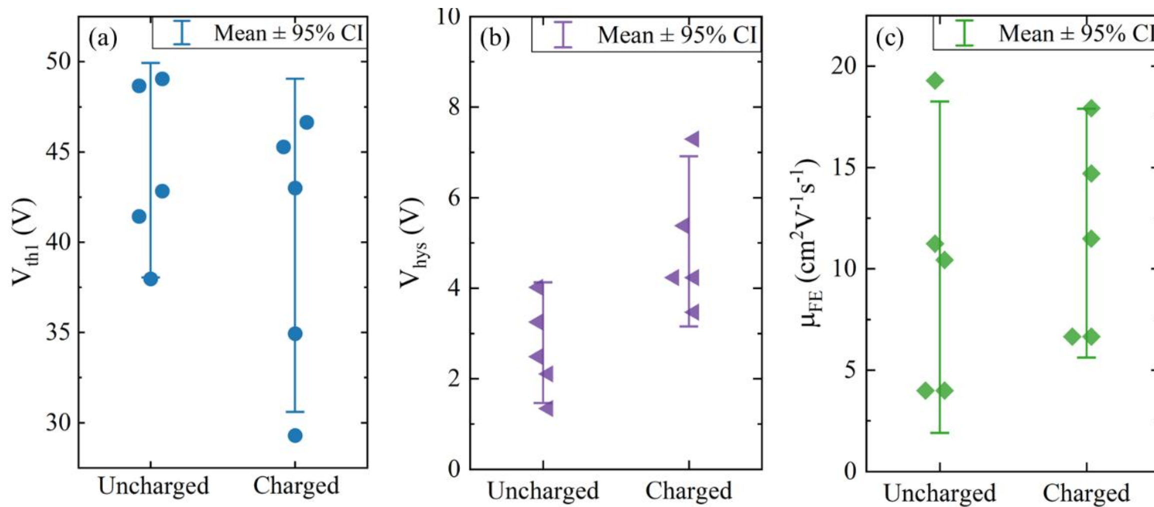


Figure 7.4.1 The extracted (a) V_{th1}, (b) V_{hys} and (c) μ_{FE} from 2D MoS_2 FETs fabricated on substrates capped with SiO_x, both uncharged and charged prior to device fabrication. Measurements were taken with V_{gs} sweeps from 0 to +80 V. The error bars represent the mean ± 95% confidence interval (CI).

Table 7.4.1 Summary of mean ± SD and mean differences (Δ=HfO_x − SiO_x) with two-sided 95% Welch CIs for V_{th1}, V_{hys}, and μ_{FE}. A CI including 0 indicates the difference is not established at the 5% level.

Property	Sample Group	Mean ± SD	95% CI for Δ
V_{th1} (V)	Uncharged	43.99 ± 4.78	[-11.51, 3.19]
	Charged	39.83 ± 7.43	
V_{hys} (V)	Uncharged	2.80 ± 1.07	[-0.32, 4.15]
	Charged	5.03 ± 1.51	
μ_{FE} ($cm^2\,V^{-1}\,s^{-1}$)	Uncharged	10.08 ± 6.58	[-6.80, 10.17]
	Charged	11.76 ± 4.94	

To further confirm the changes in the intrinsic properties of 2D MoS_2, PL spectra were obtained on flakes transferred onto SiO_x-capped dielectrics at room temperature, both uncharged and charged. The spectra were obtained within 24 hours of the flake transfer. At least 5 flakes were measured on each substrate. The individual and average spectra and the extracted I_A^-/I_A^0 ratios of each flake are shown in Figure 7.4.2. The means ± SDs for each group and the Welch two-sample comparisons of the mean difference (Δ=Charged − Uncharged) reported as two-sided 95% confidence intervals (CI) are listed in Table 7.4.2.

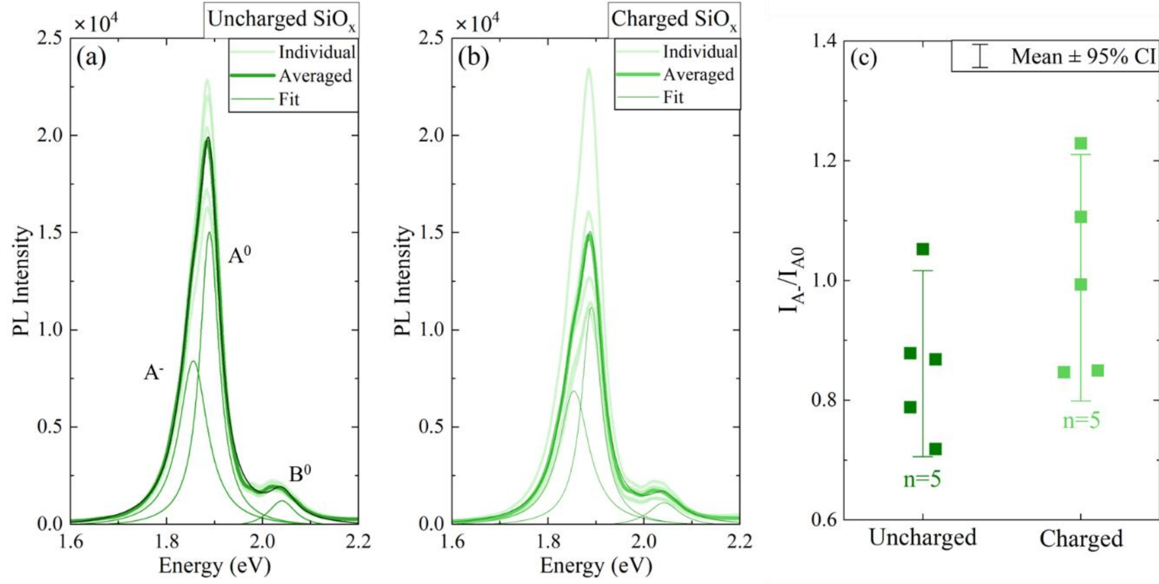


Figure 7.4.2 Individual and averaged PL spectra of five 2D MoS_2 flakes on (a) uncharged substrates and (b) charged substrates capped with SiO_x. (c) The extracted area ratio between peak A^- and A^0 (I_{A^-}/I_{A^0}) of the 2D MoS_2 flakes on uncharged and charged SiO_x-capped substrates. The error bars represent the mean ± 95% confidence interval (CI).

Table 7.4.2 Summary of mean ± SD and mean differences (Δ=Charged − Uncharged) with two-sided 95% Welch CIs for I_{A^-}/I_{A^0}. A CI including 0 indicates the difference is not established at the 5% level.

Sample Group	Mean ± SD	95% CI for Δ
Uncharged	0.86 ± 0.13	[-0.07, 0.36]
Charged	1.00 ± 0.17	

Similar peak features were observed on 2D MoS_2 flakes on uncharged and charged substrates, as shown in Figure 7.4.2 (a) and (b). Lower I_{A^-}/I_{A^0} values of 0.86 ± 0.13 are obtained from flakes on uncharged substrates compared to 1.00 ± 0.17 on charged substrates, with a 95% CI that includes zero, indicating a statistically insignificant trend at the 5% level. However, a tendency for n-type doping was found on 2D MoS_2 on charged substrates from both the transfer and PL measurements. The origin of such changes, as well as the absence of strong p-type doping expected from a negatively charged dielectric, is further discussed in Section 7.4.4.

7.4.2 Charged Dielectric Capped with AlO_x

Next, the doping effects of AlO_x-capped charged dielectrics on 2D MoS_2 were investigated. Uncharged dielectrics were fabricated as described in Section 7.3. The same corona-anneal process used for charging the SiO_x-capped dielectrics was repeated four times. CPD values were measured to be ~22 V, which corresponds to a charge density of -1.6×10^{12} q cm^{-2}, assuming all injected charges are located at the SiO_2/AlO_x interface. PL spectra were obtained from 2D MoS_2 flakes on both uncharged and charged substrates within 24 hours of the dry transfer process. The individual and average spectra and the extracted I_{A^-}/I_{A^0} ratios of each flake are shown in Figure 7.4.3. The means ± SDs for each group and the Welch two-sample comparisons of the mean

difference (Δ=Charged − Uncharged) reported as two-sided 95% confidence intervals (CI) are listed in Table 7.4.3.

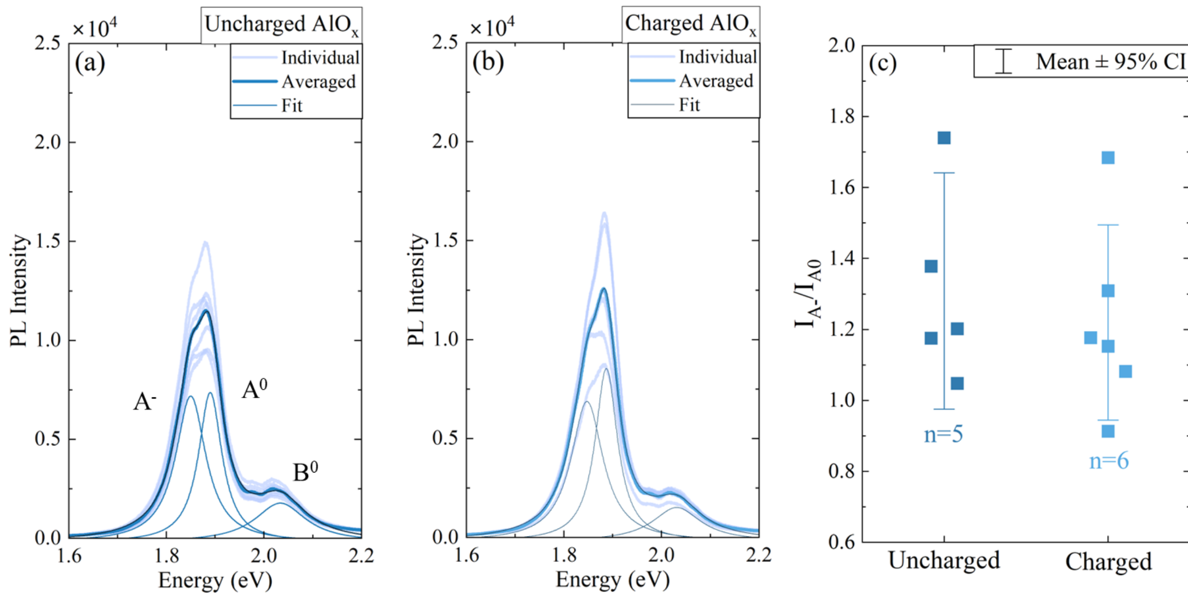


Figure 7.4.3 Individual and averaged spectra of 2D MoS_2 on(a) uncharged substrates and (b) charged substrates capped with AlO_x. (c) The extracted area ratio between peak A^- and A^0 (I_{A^-}/I_{A^0}) of the 2D MoS_2 flakes on uncharged and charged substrate. The error bars represent the mean ± 95% confidence interval (CI).

Table 7.4.3 Summary of mean ± SD and mean differences (Δ=Charged − Uncharged) with two-sided 95% Welch CIs for I_{A^-}/I_{A^0} obtained on flakes on uncharged and charged AlO_x-capped substrates. A CI including 0 indicates the difference is not established at the 5% level.

Sample Group	Mean ± SD	95% CI for Δ
Uncharged	1.31 ± 0.27	[-0.45, 0.27]
Charged	1.22 ± 0.26	

Only minimal changes were observed in the spectra shapes and in the I_{A^-}/I_{A^0} values, indicating similar doping densities across the 2D MoS_2 flakes on uncharged and charged substrates. The two-sided 95% CI for the pairwise mean differences includes zero, so no statistically significant differences are resolved at the 5% level. Neither AlO_x- nor SiO_x-capped (Section 7.4.1) charged substrates resulted in significant p-type doping of 2D MoS_2. This finding contradicts expectations, as the embedded negative charges in the dielectrics were anticipated to alter the carrier density in the adjacent channel. A more detailed discussion on the potential causes for the absence of field-effect doping is provided in Section 7.4.4.

7.4.3 Charged Dielectric Capped with HfO_x

To further investigate the requirements for realising field-effect doping of 2D MoS_2 using charged dielectrics, the doping effects of HfO_x-capped charged dielectrics were examined. It is noted that the capping layer, charging methods, and charged defects differ from those of the previously discussed SiO_x and AlO_x-capped charged dielectrics.

Uncharged substrates were fabricated as described in Section 7.3. For charged samples, Si substrates with 300 nm thermal SiO_2 were first annealed at 800 ºC for 30 minutes. Negative charges were then injected using the hot-corona process for 5 minutes at 450 ºC, as described in Chapter 3. Following the charging process, 50 cycles of ALD-HfO_x were deposited. CPD values were measured to be 70~90 V after the HfO_x deposition, equivalent to a charge density of –5.1 to –6.5 × 10^{12} q cm^{-2}, assuming the charges are located near the surface of the 300 nm SiO_2. FET devices were fabricated on uncharged and charged substrates following the all-dry fabrication protocol described in Chapter 6.

All devices were measured in an argon atmosphere under dark conditions, with the time between the dry transfer of 2D MoS_2 and transfer measurements under 48 hours. The sweep range was set to 0 to +80 V for devices on uncharged substrates, which was found insufficient to capture the full device turn-on on charged substrates. The majority of devices on charged substrates were measured with a V_{gs} sweep range of 0 to +120 V with two measured between 0 to +80 V. Extracted results from both measurement ranges were included for analysis as Section 6.3.2 has demonstrated that change in the maximum V_{gs} has minimal effects on V_{th1}. The measured transfer curves are also included in Appendix K, demonstrating the lower current of devices on charged substrates. These data indicates that the following observations are not an artifact of the linear-region fitting procedure, as discussed in Section 6.3.2. Furthermore, the five transfer curves obtained on each device are included in Appendix K, clearly demonstrating that the increased V_{th1} is not a result of reduced μ_{FE} due to repeated measurements. The V_{gs} step size was 2 V, and V_{ds} was 0.01 V. At least three measurements were taken on each device, with a 180-second interval between each measurement. The extracted V_{th}, V_{hys} and μ_{FE} from the last measurements of each device are shown in Figure 7.4.4, which are the least affected by the exposure to air and light during measurement set up. The means ± SDs for each group and the Welch two-sample comparisons of the mean difference (Δ=Charged − Uncharged) reported as two-sided 95% confidence intervals (CI) are listed in Table 7.4.4.

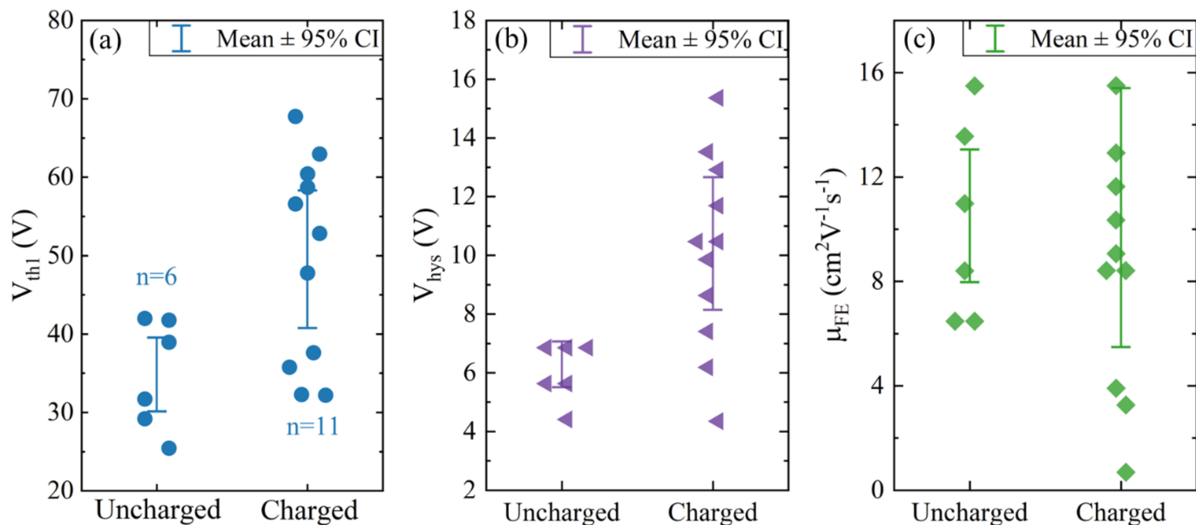


Figure 7.4.4 The extracted (a) V_{th1}, (b) V_{hys} and (c) μ_{FE} from 2D MoS_2 FETs fabricated on substrates capped with HfO_x, both uncharged and charged prior to device fabrication. The error bars represent the mean ± 95% confidence interval (CI).

Table 7.4.4 Summary of mean ± SD and mean differences (Δ=Charged − Uncharged) with two-sided 95% Welch CIs for V_{th1}, V_{hys}, and μ_{FE}. A CI including 0 indicates the difference is not established at the 5% level.

Property	Sample Group	Mean ± SD	95% CI for Δ
V_{th1} (V)	Uncharged	34.86 ± 7.02	[2.35, 27.04]
	Charged	49.55 ± 13.07	
V_{hys} (V)	Uncharged	6.29 ± 1.16	[1.05, 7.17]
	Charged	10.40 ± 3.37	
μ_{FE} ($cm^2\ V^{-1}\ s^{-1}$)	Uncharged	10.51 ± 3.78	[-7.00, 6.87]
	Charged	10.45 ± 7.39	

An increase in the V_{th1} from 34.86 ± 7.02 V (Uncharged) to 49.55 ± 13.07 (Charged) was observed, with a mean increase of 14.69 V and a Welch 95% CI entirely below zero, establishing a significant trend. As demonstrated in Section 6.3.2, increasing the maximum V_{gs} has minimal effect on the extracted V_{th1}, thus the increase in V_{th1} indicates the presence of excess holes in the 2D MoS_2 channel on charged substrates. Assuming that all applied V_{gs} is fully mirrored into the channel, this change in V_{th1} is equivalent to an excess hole density of 1.1×10^{12} q cm^{-2}. Hysteresis grows from 6.29 ± 1.16 V to 10.40 ± 3.37 V with an average increase of 5.24 V and a 95% CI of [1.05, 7.17] V, likely originating from the higher maximum V_{gs} applied, as shown in Figure 7.4.4 (b). Devices on both uncharged and charged substrates have a μ_{FE} of ~10 $cm^2\ V^{-1}\ s^{-1}$, as shown in Figure 7.4.4 (c), indicating high-quality channels. These results demonstrate p-type doping of 2D MoS_2 using negatively charged dielectrics, without the degradation of channel mobility – an issue commonly associated with charge transfer doping using chemically absorbed dopants [305].

PL spectra were acquired to further confirm the doping of 2D MoS_2 on HfO_x-capped charged dielectrics. 2D MoS_2 flakes were transferred onto both uncharged and charged substrates, and PL spectra were recorded at room temperature within 24 hours of transfer. The individual and averaged spectra and their extracted I_A^-/I_A^0 ratios for each flake are shown in Figure 7.4.5. The means ± SDs for each group and the Welch two-sample comparisons of the mean difference (Δ=Charged − Uncharged) reported as two-sided 95% confidence intervals (CI) are listed in Table 7.4.5.

Figure 7.4.5 (a) shows clear PL changes for flakes on negatively charged dielectrics with an A peak of higher intensity and sharper feature. Quantitatively, the I_A^-/I_A^0 value decreases from 1.58 ± 0.22 (uncharged) to 0.77 ± 0.15 (charged). The two-sided 95% CI for Δ is [-1.10, 0.52], entirely above zero, establishing a statistically robust reduction in I_A^-/I_A^0 on charged substrates. This implies lower electron density for flakes on negatively charged HfO_x-capped dielectrics. These results corroborate the transfer measurements, together indicating p-type doping of 2D MoS_2 induced by dielectric charges.

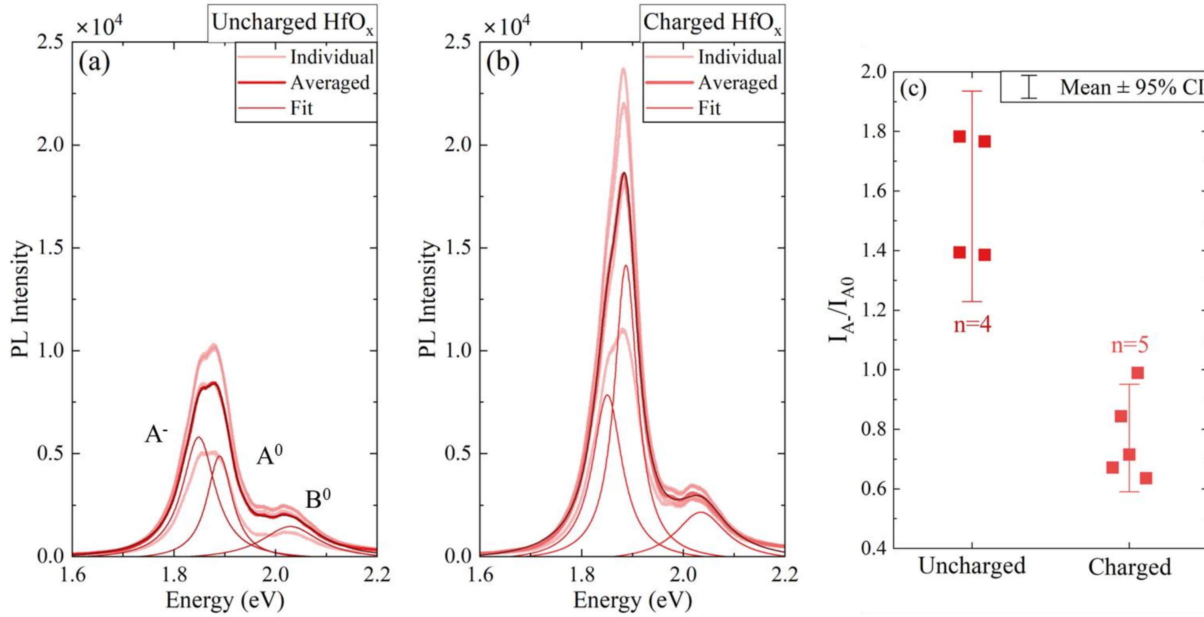


Figure 7.4.5 Individual and averaged spectra of 2D MoS_2 on(a) uncharged substrates and (b) charged substrates capped with HfO_x. (c) The extracted area ratio between peak A^- and A^0 (I_A^-/I_A^0) of the 2D MoS_2 flakes on uncharged and charged substrate. The error bars represent the mean ± 95% confidence interval (CI).

Table 7.4.5 Summary of mean ± SD and mean differences (Δ=Charged − Uncharged) with two-sided 95% Welch CIs for I_A^-/I_A^0 obtained on flakes on uncharged and charged HfO_x-capped substrates. A CI including 0 indicates the difference is not established at the 5% level.

Sample Group	Mean ± SD	95% CI for Δ
Uncharged	1.58 ± 0.22	[-1.10, -0.52]
Charged	0.77 ± 0.15	

7.4.4 Discussion

In this section, the doping effects of charged dielectrics capped with SiO_x, AlO_x, and HfO_x were investigated. P-type doping was demonstrated in 2D MoS_2 on negatively charged HfO_x-capped dielectrics but was absent on negatively charged SiO_x and AlO_x-capped dielectrics. A comprehensive discussion on the observed changes in 2D MoS_2 properties is provided here.

The origin of the differences in 2D MoS_2 on uncharged and charged SiO_x-capped dielectrics is first discussed. A minimal decrease in the average V_{th1} was found for devices on charged substrates, also accompanied by an increase in ΔV_{th1} and V_{hys}. Meanwhile, a slightly higher I_A^-/I_A^0 ratio was observed on charged SiO_x-dielectric. As discussed previously, increased interface state density can simultaneously increase variations in doping density, hysteresis in transfer measurements and I_A^-/I_A^0 ratio in PL spectra. Defects are likely created near the SiO_x surface during the charging process, as discussed in Chapter 3. These defects could contribute to the observed changes in both ΔV_{th1} and V_{hys} if their energy levels lie within the 2D MoS_2 bandgap.

However, due the minimal change in V_{th1}, it remains unclear whether these defects have also induced n-type doping in 2D MoS_2.

For HfO_x-capped charged dielectrics, no excess defects are expected near the HfO_x surface, as the charging process was performed prior to HfO_x deposition. The observed increase in the average V_{th1} and I_A^-/I_A^0 ratios for 2D MoS_2 on charged HfO_x-dielectric can be concluded to originate from field-effect doping. The excess hole density from such field-effect is calculated to be 1.1 and 26 × 10^{12} q cm^{-2} from transfer and PL measurements respectively, according to Equation (1.4.3) and (2.4.13). Discrepancies were observed in the doping densities extracted from both measurements when compared to the embedded negative charge density of 5.1 to 6.5 × 10^{12} q cm^{-2}, as estimated from the measured CPD values. This suggests a potential underestimation of doping density in transfer measurements and an overestimation from PL spectra similar to the observations in Section 7.3, where the difference in oxygen vacancies in the dielectric is proposed to play a role. However, as the surface defect densities of the charged or uncharged HfO_x-capped dielectrics are expected to be similar, additional factors must be considered to account for the discrepancy.

The overestimation of change in hole density form PL spectra is likely related to field-effect passivation. As discussed in the Section 7.3.1 and in the literature [129], [130], [306], a high density of in-gap defects is present at the HfO_x-2D MoS_2 interface, causing non-radiative recombination. When a high density of fixed charge is near the interface, the electron and hole ratio in the 2D MoS_2 changes, leading to a suppressed recombination activity, and thus higher A^0 exciton count. This leads to an overestimation of the decrease in electron density due to field-effect doping. It is also noted that other factors such as dielectric screening [307] and doping can change the interactions between excitons, trions and electrons (also referred to as many-body effects) [308], and leads to a correction in the E_b, and subsequently inaccuracy in the calculated electron density.

High contact resistance and interface states have been identified to affect the extracted carrier densities from transfer measurements, as discussed in Section 7.3.1. It is proposed that interface states also contribute to the incomplete coupling of the dielectric charge to the channel observed in transfer measurements. The embedded charge is mirrored into both energy levels in 2D MoS_2, and the in-gap defects at the interface, leading to a relation of:

$$Q_{dielectric} = -(Q_{channel} + Q_{interface}) \tag{7.4.1}$$

where $Q_{dielectric}$, $Q_{channel}$, and $Q_{interface}$ are the dielectric charge density, excess charge in the channel and at the interface states, respectively. This leads to a reduced mirrored charge density in the channel ($|Q_{channel}|<|Q_{dielectric}|$). A more effective field-effect doping is possible with an improved interface quality.

Previously, increased doping density (ΔV_{th1}) and hysteresis were considered jointly as indicators of a high interface state density. However, in devices on charged HfO_x-capped substrates, these two observations are proposed to have different origins. The higher maximum applied V_{gs} may contribute to the increased V_{hys}, as demonstrated in Chapter 6. Meanwhile, non-uniformity in the embedded charge density and potential charge

degradation could lead to larger variations between devices. Optimising both mechanisms can enable a more precise control of the doping of 2D MoS_2 using charged dielectrics.

Now, the conditions which enabled field-effect doping only in charged HfO_x-dielectrics are discussed. The three charged dielectric systems studied present three key differences: (1) capping dielectric layer, (2) sequence of charge injection and capping dielectric deposition, and (3) types of charged defects. It is proposed that the absence of p-type doping in 2D MoS_2 on charged SiO_x and AlO_x-capped substrates is due to dielectric charge degradation. Schematics of the proposed mechanism are shown in Figure 7.4.6.

As discussed in Chapter 3, despite the thick SiO_x (> 25 nm) layer, charges can be injected using a negative corona charge. This indicates the presence of bulk defects, which assist charge injection at high temperatures. These defects could be created by the negative corona charge, which are high energy CO_3^- ions [139], and form a pathway where electrons can hop through. Moreover, the Al-induced defects are likely to have energy levels inside of the 2D MoS_2 bandgap [51], making it energetically favourable for the electrons to dissociate with the Al-induced defects when neighbouring a semiconductor. Such degradation is forbidden without the 2D MoS_2 channel, which explains the observed high charge stability in air at elevated temperatures. The combination of a degradation pathway and the high energy levels of the charged defects facilitate charge degradation, as show in Figure 7.4.6 (a). On the other hand, as HfO_x is deposited after charge injection, no excess defects were generated. The defects responsible for the embedded charges were created during the hot-corona process, where high energy ions bombard the SiO_2 surface at 450 ºC. This could lead to creating defects with deeper energy levels than the Al-induced defects, as shown in Figure 7.4.6 (b). This hypothesis is also supported by the higher stability of the charges in air at elevated temperatures, as discussed in Chapter 3.

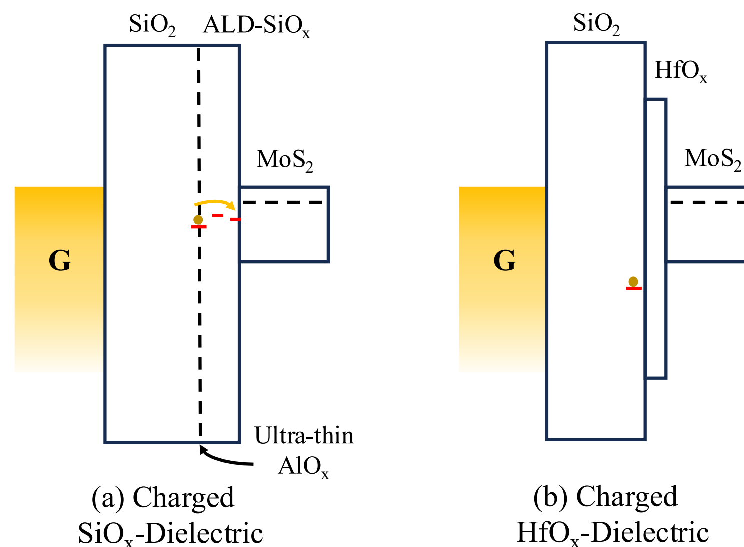


Figure 7.4.6 Schematics of the interaction between the charged defects and 2D MoS_2 in (a) charged SiO_x-dielectric and (b) charged HfO_x-dielectric.

7.5 Summary

This chapter explored field-effect doping of 2D MoS_2 using charged dielectrics. This concept was first validated via a top PMMA layer on a back-gated FET device. Modulation of the carrier density was demonstrated by depositing corona charge on the PMMA layer, creating a temporary electric field. A discrepancy was observed between the deposited corona charge density and the resultant change in carrier density in the 2D MoS_2 channel, likely attributing to defects at the PMMA/2D MoS_2 interface. However, the instability of charge on PMMA, along with degradation of film properties after repeated charging, rendered it unsuitable for practical applications.

Field-effect doping of 2D MoS_2 using ALD-deposited dielectrics with charged defects was then investigated as a more stable alternative. Interactions between 2D MoS_2 and dielectric materials, both charged and uncharged, were examined via transfer and PL measurements. Dielectrics with ALD-SiO_x, AlO_x, and HfO_x as capping layers were used. Statistical analysis focusing on carrier density, hysteresis, and mobility was carried out. On uncharged dielectrics, 2D MoS_2 on ALD-SiO_x exhibited higher electron density compared to those on ALD-AlO_x and HfO_x. The different annealing treatments applied to each dielectric, which are known to modulate oxygen vacancy concentrations, are proposed as the primary factor contributing to the observed variations in channel carrier density and hysteresis.

On charged dielectrics, the first p-type field-effect doping was demonstrated using hot corona-charged dielectrics with a HfO_x capping layer. No evident degradation in the channel mobility was observed – a commonly encountered issue in alternative doping strategies. Hole densities of 1.1 and 39×10^{12} q cm^{-2} were extracted from transfer and PL measurements, respectively, with a dielectric charge density of 5.1 to 6.5×10^{12} q cm^{-2}. Discrepancies among these values are attributed to non-optimised FET device fabrication and high defect densities at the 2D MoS_2/dielectric interface.

This chapter demonstrated a proof of concept for field-effect doping of 2D semiconductors using charged dielectrics and outlined the key design considerations for such dielectrics. Further investigation into the stability, tunability, spatial uniformity, and patterning of such doping strategy is essential to advance its application into high performance devices.

Chapter 8
Summary and Future Work

Semiconductor devices are fundamental to modern technology. The development of functional dielectrics and understanding their interfaces to the semiconductor are essential for enabling novel device applications and enhanced performance. While minimising dielectric defect density is typically pursued to improve device efficiency and stability, this work emphasises the engineering of interface defect states to enable novel functionalities. This work focuses on the role of negatively charged defects and explore their integration into two key applications: as passivation nanolayers for silicon solar cells, and as a doping strategy for 2D semiconductors such as 2D MoS_2. Advanced characterisation techniques including τ_{eff}-V_{surf}, capacitance-voltage, TEM, transfer measurements and photoluminescence were employed to reveal the interactions at the dielectric-semiconductor interface.

Novel charged dielectric nanolayers were developed with a focus on the controlled embedding, charging and protection of defect states. An ultra-thin AlO_x layer, as thin as 10 ALD cycles (~1 nm), demonstrated a high negative charge density of 6.9×10^{12} q cm^{-2} when sandwiched between two SiO_x layers, establishing a foundation for developing effective but low-cost passivation nanolayer stacks for silicon solar cells. Building on the understanding of the charging mechanisms, this work demonstrated for the first time that defects at the SiO_x/AlO_x interface can be effectively charged through negative corona charge deposition at room temperature followed by annealing at 450 °C – a process termed corona-anneal. This charging strategy yielded a stable negative charge density of 4.3×10^{12} q cm^{-2} at 450 °C, with the SiO_x/AlO_x interface placed 300 nm away from Si. An alternative approach, termed hot corona, involving corona charge deposition at elevated temperatures, was found to induce charged defects near the dielectric surface, exhibiting superior thermal stability at 450 °C compared to the charged defects at the SiO_x/AlO_x interface.

The effects of various capping dielectrics in preventing charge degradation were investigated. A defect-assisted charge injection mechanism was identified in ALD-SiO_x but was absent in ALD-HfO_x. Based on these insights, two distinct charging approaches were proposed, differing in the sequence of charge injection and capping layer deposition. Three stable charged dielectric systems were developed, which were tailored for the field-effect doping of 2D semiconductors.

Negatively charged dielectric is first applied to passivate silicon surfaces. An ultra-thin AlO_x layer was incorporated into nanolayer stacks for p-type silicon surfaces, with an emphasis on maintaining high passivation quality while reducing processing costs. A minimum S_{eff} of 3.3 and 6.3 cm/s was achieved on n-

type and p-type silicon, respectively, using a nitric acid oxidised silicon (NAOS) layer, in combination with an ~2.5 nm thick AlO_x layer and a SiN_x anti-reflection layer – forming a $SiO_x/AlO_x/SiN_x$ stack. Advanced characterisation of the interface revealed the critical role of carrier capture velocities at band tail states – an aspect often overlooked in the literature. Remarkably, the additional of just a 2.5 nm AlO_x layer resulted in a distinctly different chemical interfaces after annealing, suggesting the formation of new acceptor-like defect states which give rise to a negative charged interface. The creation of new defects was confirmed with interface analysis using TEM and EELS, which demonstrated the diffusion of Al atoms towards the silicon interface. These findings establish a strong correlation between the observed changes in chemical composition and bonding configuration to the changes in both chemical and field-effect passivation.

The passivation of the $SiO_x/AlO_x/SiN_x$ stack on p-type silicon was further enhanced by performing a short annealing under electric fields. A reduced S_{eff} to 5.5 cm/s on p-type Si was achieved by annealing under positive surface corona charge. Interface studies attributed this improvement to a reduction in electron capture velocities at the valence band tail ($S_{n,VB}$). Modifications in both chemical passivation at mid-gap and field-effect passivation were found and proposed to result from a combination of charge injection near the interface and hydrogen migration under the applied electric fields at elevated temperatures. This hypothesis is supported by additional studies on SiO_x/SiN_x-passivated interfaces, which further reveal the significance of the location and energy levels of defect states near the interface in determining the change in net charge density. Most notably, this novel post-deposition treatment has been shown to increase negative charge density within ultra-thin AlO_x layers (~2.5 nm). This is particularly significant as the trade-off between layer conductivity and field-effect passivation remains a critical challenge in mainstream TOPCon solar cell devices.

To enable field-effect doping of 2D MoS_2 using the previously developed charged dielectrics, a novel all-dry device fabrication protocol was developed. This process demonstrated full preservation of the embedded charge throughout the field-effect transistors (FETs) fabrication and demonstrated high reliability. A comprehensive measurement process was also established, defining controlled gas environment, measurement settings, and light exposure conditions. Comprehensive models were proposed to account for the observed hysteresis and their dependence on environmental factors.

Using the all-dry fabrication process, the doping of 2D MoS_2 using the previously developed charged dielectric systems was studied. Notably, this study demonstrated, for the first time, p-type doping of 2D MoS_2 via field-effect using the hot corona-charged, HfO_x-capped dielectrics. An excess hole density of 1.1×10^{12} q cm^{-2} was achieved with an embedded charge negative charge density of 5.1 to 6.5×10^{12} q cm^{-2}, extracted from transfer measurements. The discrepancy between embedded and induced charge density is attributed to a high density of interface defects. Requirements for achieving effective doping using charged dielectrics were proposed. The novel doping strategy demonstrated in this work has the potential to achieve controllable, stable, and patterned doping of 2D semiconductors, which has not yet been demonstrated in the literature.

8.1 Future Work

In this work, the $SiO_x/AlO_x/SiN_x$ nanolayer stack demonstrated strong potential for passivating p-type silicon surfaces. Corona-annealing has been found to further enhance the passivation quality, tuning both chemical and field-effect passivation. Additional studies are required to incorporate this nanolayer into TOPCon devices.

- While the passivation performance was evaluated on p-type Si surfaces, the $SiO_x/AlO_x/SiN_x$ stack is particularly relevant for boron-doped emitters at the front surface of TOPCon structures [309]. The passivation quality of the stack on a highly doped emitter surface with surface texturing requires additional investigation.
- This work demonstrated that negative charges in ultra-thin AlO_x layers can be further enhanced by annealing under a positive electric field. This is highly relevant for improving the performance of AlO_x as a passivating contact on the back surface of TOPCon devices. Currently, a trade-off exists between the conductivity of the layer to the passivation quality, depending on the layer thickness. The corona-anneal process has the potential to improve the field-effect passivation without increasing the AlO_x layer thickness [204].
- For industrial implementation, the long-term stability of interface charges must be assessed under elevated temperatures and UV exposure [176]. Additionally, to minimise additional thermal process, the possibility of combining the corona-anneal process to the firing step (800 °C for 1-2 seconds) should be investigated [310].

The dielectric/Si interface was analysed using τ_{eff}-V_{surf} plots, a straightforward yet powerful characterisation which provides detailed information of the semiconductor/dielectric interface. Further optimisation of the method could lead to a more detailed analysis of the interface properties.

- To improve accuracy, a more controlled experimental procedure is required. The automation of data acquisition allows precise control over key parameters such as V_{surf} step size, time between steps, and sweep range. This minimises the changes at the interface caused by the measurement process itself. For example, hysteresis was observed in the layers studied in this work, which could lead to inaccuracy in the extracted interface properties.
- Enhanced data accuracy would reduce the confidence intervals, especially for the carrier capture velocities at band-tails. With improved data accuracy, the effects of interface properties at band tails, including $D_{it,VB/CB}$, $\sigma_{n/p,CB/VB}$ can be studied in detail. This also require an adjusted fitting procedure, where the difference between the extracted range caused by difference in data accuracy between samples should be minimised.

This work demonstrated an all-dry fabrication protocol, focusing on the full preservation of the embedded dielectric charge. A p-type behaviour and large discrepancy in carrier density between the extracted carrier densities from transfer and PL measurements, which is proposed to attribute to the non-optimised device

fabrication. Several improvements can be made to minimise the effects of device fabrication in revealing the channel properties.

- Contact resistance can be characterised on multilayer 2D MoS_2 flakes. Optimisation of the metal deposition process should be carried out, particularly by minimising heating of the sample during metal evaporation [94]. This has the potential to decrease the contact resistance and its effects on the extracted carrier densities.
- For practical applications, the fabrication process must be compatible with standard lithography. This requires high stability of embedded charge against common solvents and photoresists. A high stability in air has been demonstrated, even at elevated temperatures. Further investigation is required to reveal the degradation mechanism during wet chemical processes. A denser capping layer or defect states with deeper energy levels has the potential of improving the stability of the charged defects.
- Alternative charging strategies, including ion embedding, should also be explored. For example, Na^+ or K^+ has been reported to induce positive charge [176], while Al^{3+} has been reported to induce negative charge [311]. Such ions have been shown to be stable through wet chemical processes [267], [287]. However, for Al^{3+} ions, the charging mechanism is likely similar to that observed at SiO_x/AlO_x interface, which still require an electron source. Further investigation into the stability of such charging methods is required.

This work observed different channel properties on different dielectrics, both charged and uncharged. Further investigation on the interactions between 2D semiconductors and dielectrics is required.

- It was proposed that the density of oxygen vacancies near dielectric surfaces affects the carrier density of the 2D MoS_2, as observed in ALD-SiO_x, AlO_x, and HfO_x with different annealing treatment. This hypothesis should be further confirmed by comparing the carrier densities of 2D MoS_2 on a single dielectric material (for example, ALD-SiO_x) with different annealing treatments.
- A larger hysteresis and carrier density variations was found among devices fabricated on ALD-HfO_x, which is not ideal for high performance FETs. The stability of hot corona-injected charges during ALD process of alternative dielectric layers, including SiO_x and AlO_x, should be studied for demonstrating field-effect doping with improved device performance.

Several critical aspects of the proposed doping strategy remain unaddressed in this work. Specifically, the controllability, versatility, and patterned doping has yet to be demonstrated, which are essential for enabling practical applications.

- P-type conductance has not been achieved, which is essential for complementary electronics. To achieve this, high work function metals such as Pt or Pd should be employed, combined with an improved metal/semiconductor interface [312].
- Precise control of the doping level is yet to be studied. Questions including limiting factors for the precision of the doping density, the upper limit of the doping density remain unanswered. The lateral

uniformity of the charge density should also be addressed. Further studies both to improve the controllability of the charge distribution in the dielectric as well as its interactions to 2D semiconductors should be carried out.

- Systematic investigation of the charge stability under room temperature should be carried out.
- Positively charged dielectrics using hot corona charging of SiO_2 is also possible, likely involving the creation new donor states [24]. This broadens the available doping range using one single charging strategy and opens the door to patterned doping.
- Novel patterned doping strategies should be developed. One pathway is to fabricate dielectrics with localised defects combined with a full area charging strategy. A localised charging strategy combined with a uniform dielectric is another promising pathway, as suggested by the point above. In both cases, a flat dielectric surface is ideal to preserve the atomically thin structure of 2D semiconductors to maintain a high mobility. Investigating the limiting factors for the resolution of such patterned doping would also be an interesting avenue for future work.
- Finally, the proposed doping strategy has the potential to be applied to a variety of 2D materials for diverse applications. For instance, 2D MoS_2 and WS_2 may be applied to make photodetectors, where control of the carrier density is also essential [313]. Doping is also required to reduce the sheet resistance of graphene as transparent conductors [288]. While the underlying principles remain the same, each material and application impose unique requirements.

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Appendix A: Additional Information on Bulk Recombination

In the semiconductor bulk, EHP can recombine by three different processes: radiative, Auger, and defect assisted (SRH). A summary of the three mechanisms is shown in Figure A 1.

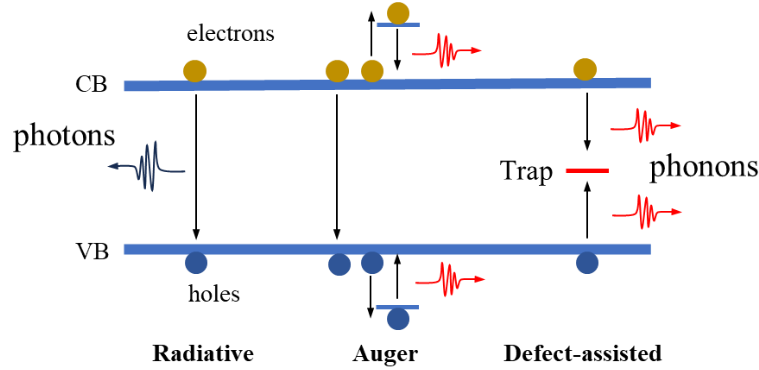


Figure A 1 Schematic of bulk recombination mechanisms: radiative, Auger, and defect-assisted recombination.

Radiative and Aguer recombination are intrinsic processes inherent to semiconductors. In indirect semiconductors such as Si, non-radiative recombination processes are dominant due to momentum conservation. The bulk recombination rate is the sum of the recombination rates of the three processes, and the bulk lifetime τ_{bulk} can be expressed as:

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}} \quad \text{(A 1)}$$

Radiative Recombination

In radiative recombination, electrons directly recombine with a hole in the valence band, emitting photons in the process. The radiative recombination rate is dependent on the carrier concentrations in the semiconductor. The net radiative recombination rate (U_{rad}) can be calculated as:

$$U_{rad} = B(np - n_i^2) \quad \text{(A 2)}$$

where B is the radiative recombination coefficient, which is a material-specific constant. In crystalline Si, the constant B has a value of 10^{-14} cm^3s^{-1} at 300 K [314].

Auger Recombination

In Auger recombination, the energy released from electron-hole recombination is transferred to a third carrier, exciting it to higher energy levels. This energy is ultimately lost by interactions with the lattice and emitted as phonons. This process can be labelled as *eeh* or *ehh* depending which type of carrier the energy is transferred to. The recombination rate is dependent on the concentration of the carriers involved:

$$R_{Aug} = R_{ehh} + R_{eeh} = C_n n^2 p + C_p n p^2 \quad \text{(A 3)}$$

where C_n and C_p are the Auger recombination coefficients for electrons and holes. The net Auger recombination rate can be expressed as:

$$U_{Aug} = (C_n n + C_p p)(np - n_i^2) \quad \text{(A 4)}$$

From Equation (A 4), it is evident that U_{Aug} is heavily dependent on the carrier concentrations. Additionally, the coefficient C_n and C_p are also found to vary drastically depending on the injection level (Δn) [315]. This arises from the strong Coulomb interactions between charge carriers at low injection levels, and the electron density increases in proximity to holes, enhancing Auger recombination [316]. To account for such effect, Coulombic interaction enhancement factors g_{eeh} and g_{ehh} are incorporated into Equation (A 4):

$$U_{Aug,LLI} = (g_{ehh} C_n n + g_{eeh} C_p p)(np - n_i^2) \quad \text{(A 5)}$$

where LLI represents for low injection conditions. In this work, Auger and radiative recombination are described by Niewelt's parameterisation [317].

Defect-assisted Recombination

Defect-assisted recombination, also referred to as Shockley-Read-Hall recombination (SRH recombination), is an extrinsic process which occurs due to the presence of impurity-induced states inside the bandgap and results in phonon release. Based on the nature of the defect, it can be either donor-like or acceptor-like. Donor-like states donate an electron and become positively charged and assist electron capture. Acceptor-like states accept an electron and becomes negatively charged and assist hole capture. A statistical model assuming a single defect at an energy level of E_T was proposed by Shockley, Read [318] and Hall [319], described as follows:

$$U_{SRH} = \frac{np - n_i^2}{\frac{p + p_1}{N_T \sigma_n v_{th}} + \frac{n + n_1}{N_T \sigma_p v_{th}}} \quad \text{(A 6)}$$

where N_T is the recombination centre concentration, $\sigma_{n/p}$ are electron/hole capture cross-sections, n_1 and p_1 are the SRH trap occupation factors, and v_{th} is the thermal velocity.

Appendix B: Additional Methods

Silicon Wafer Cleaning

To achieve superior surface passivation, silicon wafer cleaning is essential prior to the dielectric deposition to form a high-quality interface. Contamination could originate from the wafer cutting process, storage in the plastic box, inorganic compounds or metal species in solutions [320]. A cleaning procedure developed by Radio Corporation of America (RCA) in 1965 has been shown to effectively remove such contamination [321], and was adopted in this work.

The RCA cleaning process contains two main steps: standard cleaning 1 (RCA1) and standard cleaning 2 (RCA2). RCA1 is used to remove organic contaminants, while RCA2 is used to remove alkali and metallic residues. A thin chemical SiO_x is formed during each step and needs to be removed by HF.

RCA1 is a solution containing ammonia (NH_4OH, 40 wt%), hydrogen peroxide (H_2O_2, 30 wt%), and deionised water (DI water), in a volume ratio of 1:1:5. It is heated up to 80 ºC on a hot plate and the samples are immersed in the RCA1 solution for 10 minutes and then rinsed in DI water for 5 minutes. The thin oxide is removed by immersing the samples in 10 wt% HF for 1 minute. RCA2 solution contains hydrochloric acid (HCl, 36 wt%), H_2O_2, and DI water at a volume ratio of 1:1:6. Samples are then immersed in RCA2 solution at 80 ºC for 10 minutes and rinsed in DI water for 5 minutes. Another HF dip of 1 minute is used to remove the thin SiO_x formed during this process. An additional HF dip is carried out if samples have been stored in air prior to film deposition.

In some cases, a thin SiO_x is grown using nitric acid following the second HF dip after RCA2 cleaning. Samples are immersed in 68% HNO_3 solution at 80 ºC for 10 minutes and rinsed in DI water for 2 minutes to form a nitric acid oxidised silicon (NAOS-SiO_x) layer.

MoS_2 Exfoliation and Transfer

Thanks to the weak interlayer van der Waals forces, few or monolayer MoS_2 can be obtained by mechanical exfoliation, also referred to as the "Scotch-tape" method [322]. By folding and separating tapes with MoS_2 crystals, the layer thickness can be reduced. This method is straightforward and offers high-quality crystals, although the lateral size of monolayers is limited to 10-20 µm [111], [123].

In this work, high quality MoS_2 crystal was purchased from SixCarbon Technology. A photo of the flake is shown in Figure A 2 (a). The crystal is stored in a sealed bag in air. The exfoliation process flow is shown in Figure A 2 (b-c). Nitto blue tape was selected to first thin down the layer thickness due to its weak adhesion and minimal residue. A suitable amount of crystal was transferred to a piece of blue tape by folding, pressing, and unfolding the tape multiple times, until the material covers the whole tape. Polydimethylsiloxane (PDMS) stamps were then used to transfer the flakes from the blue tape to the substrate. The PMDS stamps were WF X4 from Gel-Pak with an elastomer layer thickness of 6.0 mil (152 µm). A schematic of the PDMS stamp used

is shown in Figure A 2 (d). The stamp was cut to ~ 1×1 cm^2, and the top polyethylene film was removed prior to the transfer process. The stamp was pressed onto the blue tape and separated, as shown in Figure A 2 (b). The PDMS stamp was then pressed onto the substrate surface and separated to transfer the flakes, as shown in Figure A 2 (c). This process was repeated until a sizable monolayer flake is identified on the substrate using an optical microscope. In this work, all substrates were heated at 120 ºC for 10 minutes prior to transfer to remove surface contamination and improve adhesion [323].

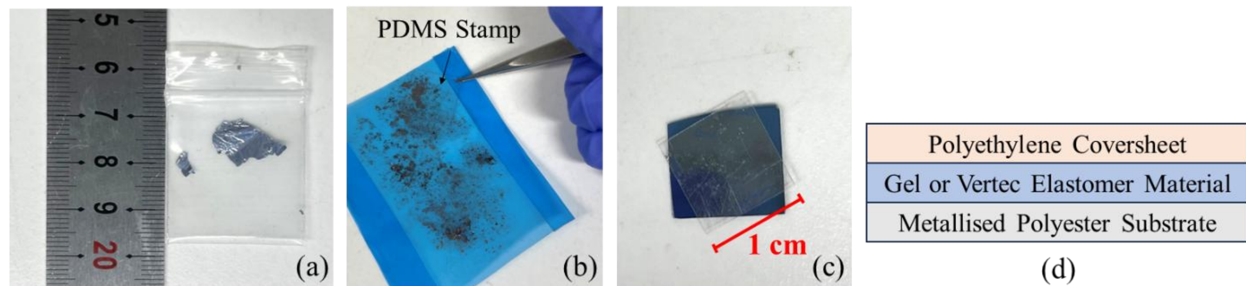


Figure A 2 Images of (a) MoS_2 crystal stored in a plastic bag in air, (b) transfer of MoS_2 flakes from the blue tape to a PDMS substrate, (c) transfer of MoS_2 flakes from the PDMS substrate to a Si substrate, and (d) layered structure of the PDMS stamp used.

Laser Cutting

In this work, a UV pico-second laser from Inngu Laser was used to pattern TEM grids as masks during metal evaporation. The design of the etching pattern and the fabricated TEM mask is shown in Figure A 3. The channel region indicated by the black lines was first defined by two 150 µm long lines with a 30 µm spacing. This pattern was displaced slightly in the central region of the TEM grid until one single metal bar was left between two larger openings, as shown in Figure A 3 (b). Bar-shaped contacts indicated by the green lines in Figure A 3 (a) were then defined on both sides of the channel region with longer lines of ~500 µm. For each etching process, the laser operated at a scanning speed of 2000 mm/s, a current of 7.25 A, a frequency of 1000 kHz, a Q pulse width of 0.1 µs, and a loop count of 15. This process was required only once to define the channel region but was repeated three to five times to define the contacts.

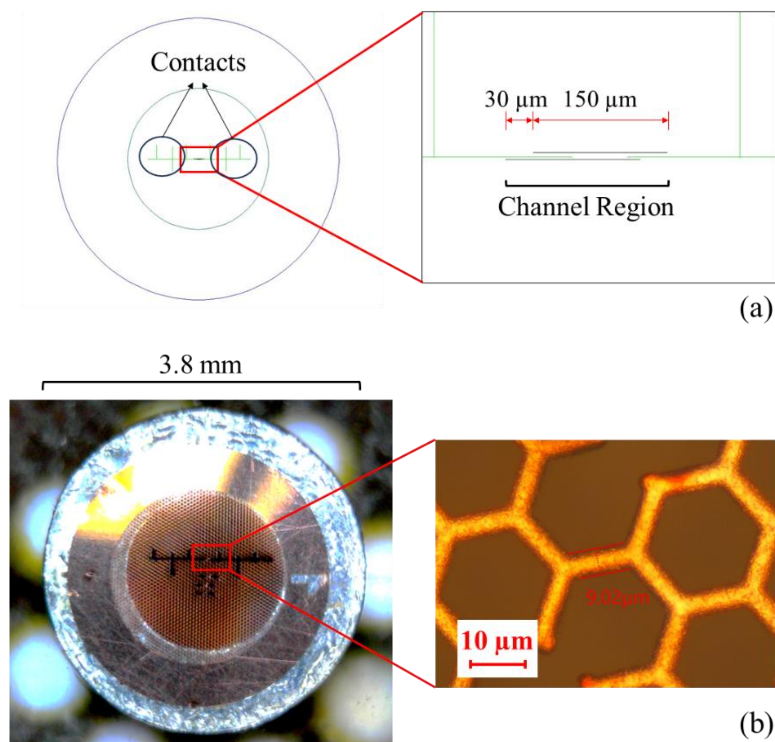


Figure A 3 (a) Schematics of the etching pattern used for TEM grids. The black lines leave only one metal bar after etching to define the channel. The black lines are displaced horizontally from the centre for a clear demonstration. (b) Image of etched TEM grid with the channel region.

Spin Coating

Spin coating was used to deposit polymethyl methacrylate (PMMA) on fabricated 2D MoS_2 FETs as a top-gate dielectric layer. A spin coater model WS-650MZ-23NPP from Laurell was used. A standard process with an adhesion step at 500 rpm for 5 seconds, a spin-off step at 4500 rpm for 50 seconds, and an additional step at 500 rpm for 5 seconds was used. Droplets of PMMA 490 A8 solution from Kayaku was dispensed during the adhesion step until the sample surface is fully covered with liquid. After spin coating, the sample was immediately annealed at 180 ºC for 90 seconds in air to remove residual solvent and improve film adhesion. The film thickness is estimated to be ~500 nm using the spin speed curve provided by the supplier.

Appendix C: Additional Information on Charged Dielectric Fabrication

Defect Removal with Increasing Annealing Time

The fabricated stack as shown in Figure A 4 was annealed at 800 °C for 5 or 30 minutes prior to corona-anneals. CPD values of ~0 V were observed on both samples without an AlO_x layer after 30 seconds of annealing, which suggests the removal of chargeable defects from the SiO_2/ALD-SiO_x interface and/or in the ALD-SiO_x layers. A small density of such defects is still present in the sample with a 5-minute annealing at 800 °C, as evidenced by ~5 V CPD value measured after 5 seconds of annealing following the charge deposition.

On the other hand, samples with an AlO_x layer demonstrated high charge stability, as indicated by the >10 V CPD values in both samples after 60 seconds of annealing at 450 °C. The sample annealed for 30 minutes at 800 °C was found to retain less charge than the one annealed for only 5 minutes. It is proposed that the 800 °C annealing also reduces defect density at the SiO_x/AlO_x interface. High-temperature annealing has been reported to favour AlO_6 octahedra over AlO_4 tetrahedra coordination [42], while the latter is associated with negative charge formation at the SiO_x/AlO_x interface [47], [50]. Thus, optimising the annealing temperature and duration is crucial for maximising the charge retention capability of the SiO_x/AlO_x interface while improving the quality of ALD-SiO_x.

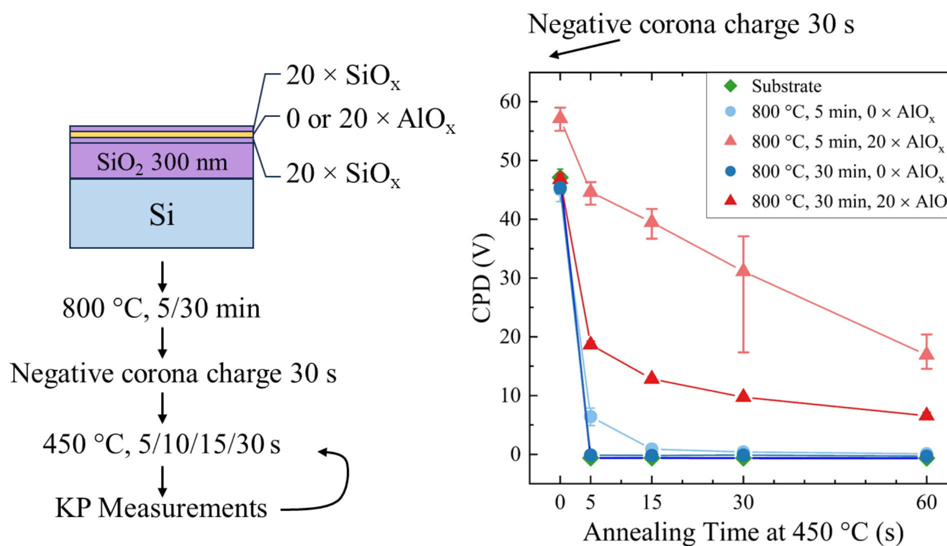


Figure A 4 Changes in CPD values with increasing annealing time at 450 °C after depositing negative corona charge at room temperature, with different annealing treatment prior to corona charge deposition. The error bar represents 10-90% of the values obtained in a 6×6 mm map with 16 points.

Defects in Substrate Oxide Layer

Variations in the quality of the thermal SiO_2 film on Set 5 and 6 substrates were found to interfere with the evaluation of the charging behaviour of purposely embedded defects. The as-received Set 5 substrate exhibited a minimal chargeable defect density, with the film quality degraded due to storage in air within the cleanroom.

The as-received Set 6 substrate displayed a high density of chargeable defects, which could be effectively removed by annealing at 800 °C for 30 minutes. This pre-deposition annealing was implemented to eliminate the effects of the substrate, enabling development of negatively charged dielectrics with controllable charge densities.

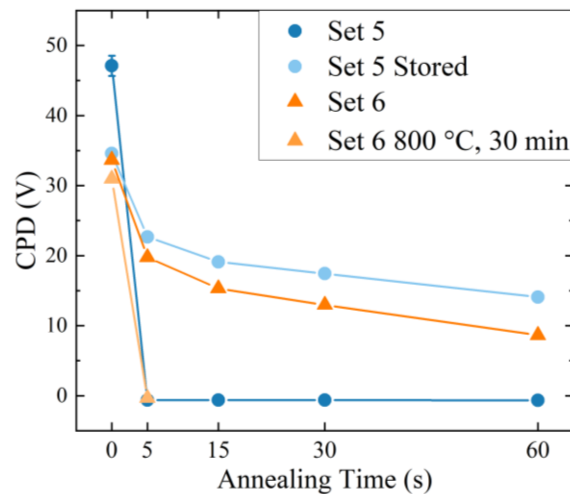


Figure A 5 Change in CPD values with increasing annealing time at 450 °C on substrate Set 5 and 6 after negative corona deposition of 30 seconds.

Negative Corona Charge Stability

On unannealed Set 6 substrates, negative corona charge was deposited for 90 seconds and annealed under different temperatures to investigate the stability of the charge. A faster charge degradation was found under annealing at higher temperatures. This supports the hypothesis that more charge de-trapping is present at higher temperatures, which accounts for the higher charge density obtained with hot corona charging at lower temperatures.

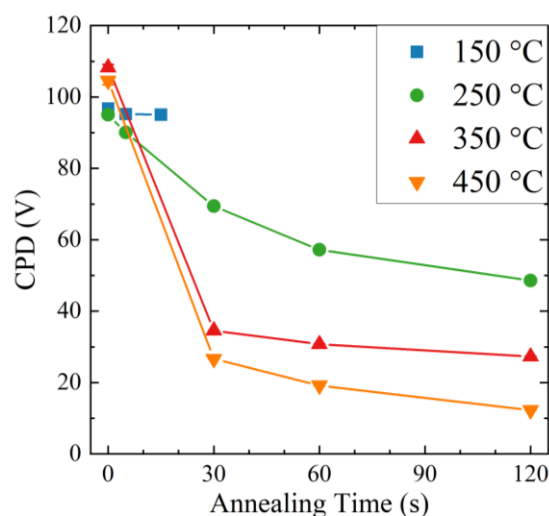


Figure A 6 Changes in CPD values with increasing annealing time under different temperatures between 150-450 °C. All samples were deposited with 90 seconds of negative corona charge at room temperature prior to annealing.

Appendix D: Corona Charge Deposition Rate Calibration

The deposition rate of corona charge at room temperature is calibrated by measuring the change in contact potential difference (CPD) with multiple deposition using KP. Changes in surface charge density are calculated from Equation (2.4.12). Different deposition rate for different charging intervals is required as the initial stage of the charging process is non-linear.

A FZ n-Si (Set 2), planar surface sample with a dielectric stack of $SiO_x/AlO_x/SiN_x$ was used to calibrate the positive corona charge deposition rate, as investigated in Chapter 4. Changes in CPD values with increasing charging time is shown in Figure A 7. A Cz p-Si (Set 3) with a passivation stack of $SiO_x/AlO_x/SiN_x$ after annealing was used to calibrate longer positive/negative corona charge depositions of 90s used for corona-anneals investigated in Chapter 5. A summary of the deposition rate of different charging times is shown in Table A 1.

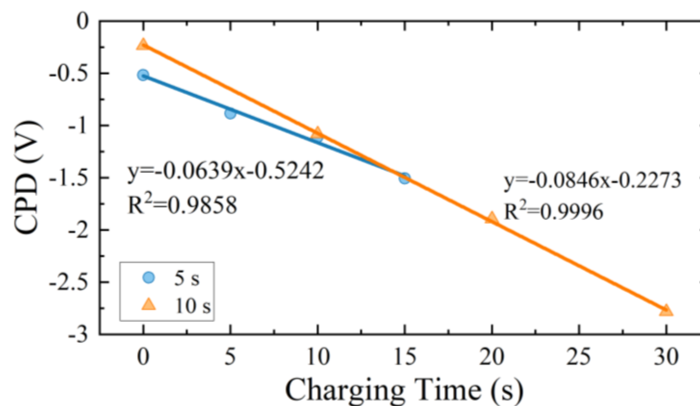


Figure A 7 CPD versus positive corona charge deposition time of 5 and 10 seconds.

Table A 1 Deposition rate under positive or negative corona charge deposition

	Charge Deposition Rate (q cm^{-2} s^{-1})		
Polarity	5 s	10 s	90 s
Positive	4.56×10^{10}	5.88×10^{10}	8.26×10^{10}
Negative	-	-	-7.91×10^{10}

Appendix E: Model Parameters to Fit τ_{eff}-V_{surf} Plots

Table A 2 Summary of modelling parameters used to fit the effective lifetime change with different surface potentials (τ_{eff}-V_{surf}) for samples in Group A, B, C, D in (1) As deposited; (2) After annealing at 450 °C for 10 minutes in air. ENT represents effective nitride thickness.

Dielectric Stack	A		B		C		D	
Treatment	As-dep	Annealed	As-dep	Annealed	As-dep	Annealed	As-dep	Annealed
τ_{bulk}	Niewelt's parametrisation							
ENT (nm)	58		56		57		55.5	
$\Delta\Phi_{ms}$ (V)	0.03							
Q_{eff} (10^{11} q cm^{-2})	-15	-42	-19	-38	29	17	29	13
σ_q (10^{11} q cm^{-2})	6	12	6	12	7	7	11	7
$D_{it,mg}$ (10^{11} cm/s)	8	45	9	10	8	10	10	10
S_{n0} (cm/s)	1465.57	1030.48	1236.58	2289.95	10075.80	9159.82	13739.73	11449.77
S_{p0} (cm/s)	3297.53	10304.80	4121.92	12594.75	3663.93	2289.95	3434.93	2289.95
$S_{n,VB}$ (10^5 cm/s)	1.6~4.8	1.4~7.9	3.1~18	1.4~12	2.6~19	2.3~12	5.6~45	5.6~45
$S_{p,CB}$ (10^5 cm/s)	17~23	8.2~17	7.5~27	7.5~32	6.4~20	6.1~13	2.1~16	12~37

Table A 3 Summary of modelling parameters used to fit the τ_{eff}-V_{surf} of SiO_x/SiN_x stacks annealed under different electric fields.

Dielectric Stack	SiO_x/SiN_x					
Treatment	Annealed		+ C-A		- C-A	
	forward	backward	forward	backward	forward	backward
τ_{bulk}	Niewelt's parametrisation					
ENT (nm)	58					
$\Delta\Phi_{ms}$ (V)	0.03					
Q_{eff} (10^{11} q cm^{-2})	23	37	30	75	12	32
σ_q (10^{11} q cm^{-2})	8	9	14	12	4	5
σ_q/Q_{eff}	0.35	0.24	0.46	0.16	0.33	0.16
$D_{it,mg}$ (10^{11} cm/s)	12	8.5	13	25	34	38
S_{n0} (cm/s)	16487.67	12068.06	59538.82	34349.32	3114.34	3480.73
S_{p0} (cm/s)	2747.95	3892.92	1190.78	1717.47	1557.17	1740.37

Table A 4 Summary of modelling parameters used to fit the τ_{eff}-V_{surf} of $SiO_x/AlO_x/SiN_x$ stacks annealed under different electric fields.

Dielectric Stack	$SiO_x/AlO_x/SiN_x$		
Treatment	Annealed	+ C-A	- C-A
τ_{bulk}	Niewelt's parametrisation		
ENT (nm)	58		
$\Delta\Phi_{ms}$ (V)	0.03		
Q_{eff} (10^{11} q cm^{-2})	-46	-57	-34
σ_q (10^{11} q cm^{-2})	8	14	8
σ_q/Q_{eff}	0.17	0.25	0.24
$D_{it,mg}$ (10^{11} cm/s)	16	35	11
S_{n0} (cm/s)	586.23	1202.23	503.79
S_{p0} (cm/s)	7327.85	6411.87	1511.37
$S_{n,VB}$ (10^5 cm/s)	1.0~5.5	0.60~6.3	0.98~4.2
$S_{p,CB}$ (10^5 cm/s)	22~42	6.7~14	1.0~5.7

Appendix F: Model Parameters to Fit C-V Plots

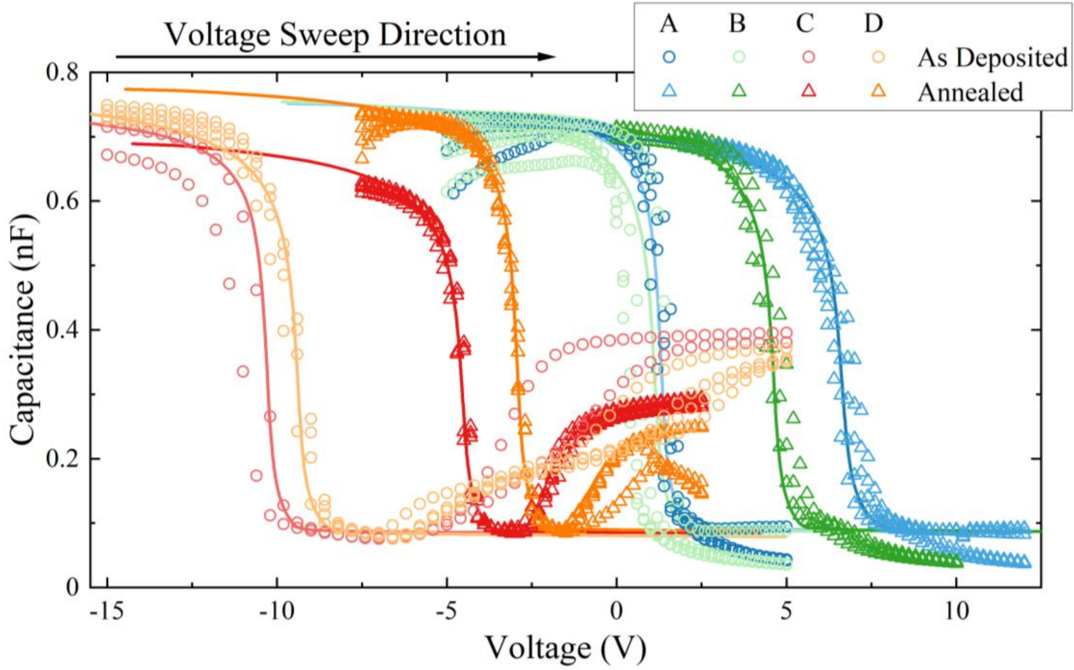


Figure A 8 Capacitance-Voltage (C-V) measured for Group A, B, C, D in (1) as deposited (lighter circles and lines); (2) after annealing at 450 °C for 10 minutes (darker triangles and lines). The symbols represent 2-6 measured curves on different Al dots. Each dot was only used once to make each measurement. The measurements were taken from low voltages with a positive voltage step towards high voltages. The lines are fitted curves using modelling parameters listed in Table A 6.

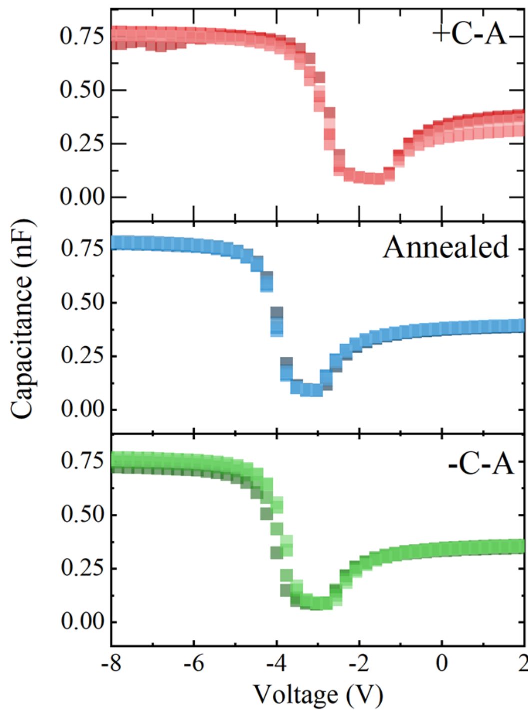
Table A 5 Extracted Q_{eff} from individual C-V measurements using the interface properties in Table A 6.

Q_{eff} (10^{12} q cm^{-2})	A		B		C		D	
	As Dep	Anneal	As Dep	Anneal	As Dep	Anneal	As Dep	Anneal
1	-1.5	-5.6	-1.7	-4.0	6.8	2.7	6.5	1.6
2	-1.5	-5.3	-1.0	-3.9	7.5	2.7	6.5	1.6
3	-1.5	-5.3	-1.0	-4.2	6.6	2.7	6.2	1.6
4	-1.6	-5.3	-1.0		7.3	2.7	6.2	1.5
5	-1.7	-5.5	-1.2			2.7	5.7	1.5
6							6.2	

Table A 6 Summary of modelling parameters used to fit the capacitance-voltage (C-V) curves for samples in Group A, B, C, D in (1) as deposited; (2) after annealing at 450 °C for 10 minutes.

Dielectric Stack	A		B		C		D	
Treatment	As-dep	Annealed	As-dep	Annealed	As-dep	Annealed	As-dep	Annealed
τ_{bulk}	Niewelt's parametrisation							
ENT (nm)	58		56		57		55.5	
Area (cm^2)	0.0068							
$\Delta\Phi_{ms}$ (V)	-0.80							

$D_{it,mg}$ (10^{10} cm/s)	8	45	9	10	8	10	10	10
$D_{it,VB}$, $D_{it,CB}$ (10^{15} cm/s)	1.5, 40	8, 8	5, 10	7, 9.5	3, 6.5	9, 14	8, 4	3, 20

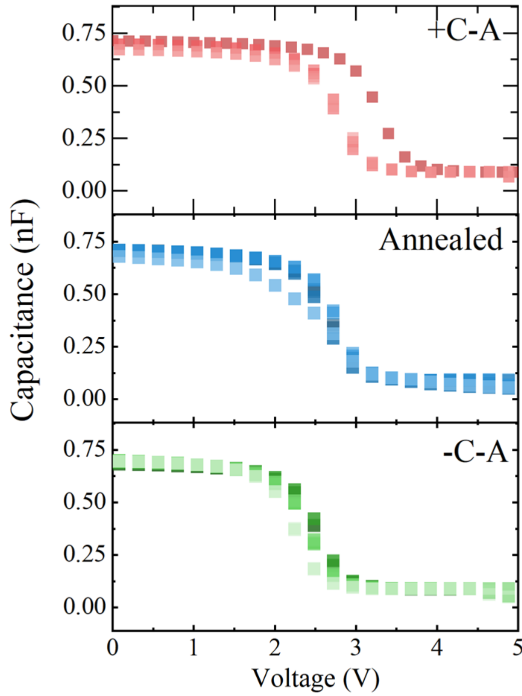


Q_{eff} (10^{12} q cm^{-2})	+C-A	Annealed	-C-A
1	3.2	2.4	2.6
2	3.1	2.5	2.5
3	3.2	2.5	2.4
4	3.2	2.5	2.4
5	3.2	2.5	

Figure A 9 Capacitance-Voltage (C-V) measured for $SiO_x/AlO_x/SiN_x$ stakcs after (1) annealed; (2) positive corona-anneal (+ C-A); (3) negative corona-anneal (- C-A). The symbols represent 4-6 measured curves on different Al dots. Each dot was only used once to make each measurement. The measurements were taken from 8 V with a negative voltage step to -4 V. The extracted Q_{eff} of each curve is also included.

Table A 7 Summary of modelling parameters used to fit the capacitance-voltage (C-V) curves for samples in SiO_x/SiN_x stacks in (1) annealed; (2) positive corona-anneal (+ C-A); (3) negative corona-anneal (- C-A).

Dielectric Stack		SiO_x/SiN_x	
Treatment	Annealed	+ C-A	- C-A
ENT (nm)		58	
Area (cm^2)		0.0068	
$\Delta\Phi_{ms}$ (V)		-0.80	
Q_{eff} (10^{11} q cm^{-2})	25	31	22
$D_{it,mg}$ (10^{11} cm/s)	12	13	34
$D_{it,VB}$, $D_{it,CB}$ (10^{15} cm/s)	2, 10	2.2, 9	3.5, 9



Q_{eff} (10^{12} q cm^{-2})	+C-A	Annealed	-C-A
1	-2.6	-2.5	-2.4
2	-2.6	-2.5	-2.4
3	-2.7	-2.5	-2.3
4	-2.9	-2.5	-2.3
5		-2.5	-2.2

Figure A 10 Capacitance-Voltage (C-V) measured for $SiO_x/AlO_x/SiN_x$ stakcs after (1) annealed; (2) positive corona-anneal (+ C-A); (3) negative corona-anneal (- C-A). The symbols represent 4-6 measured curves on different Al dots. Each dot was only used once to make each measurement. The measurements were taken from 8 V with a negative voltage step to -4 V. The extracted Q_{eff} from each curve is also included.

Table A 8 Summary of modelling parameters used to fit the capacitance-voltage (C-V) curves for $SiO_x/AlO_x/SiN_x$ stacks after (1) annealed; (2) positive corona-anneal (+ C-A); (3) negative corona-anneal (- C-A).

Dielectric Stack		$SiO_x/AlO_x/SiN_x$	
Treatment	Annealed	+ C-A	- C-A
ENT (nm)		60	
Area (cm^2)		0.0068	
$\Delta\Phi_{ms}$ (V)		-0.80	
Q_{eff} (10^{11} q cm^{-2})	-25	-27	-23
$D_{it,mg}$ (10^{11} cm/s)	16	38	11
$D_{it,VB}$, $D_{it,CB}$ (10^{15} cm/s)	2.5, 35	9, 2	2, 16

Appendix G: Surface Photovoltage Measurements

Surface photovoltage (SPV) was measured on p-Si passivated by $SiO_x/AlO_x/SiN_x$ and SiO_x/SiN_x passivation stacks with annealing under different electric fields. The measured contact potential difference (CPD) values indicate that surface corona charge has been removed during the 30-second annealing at 450 °C.

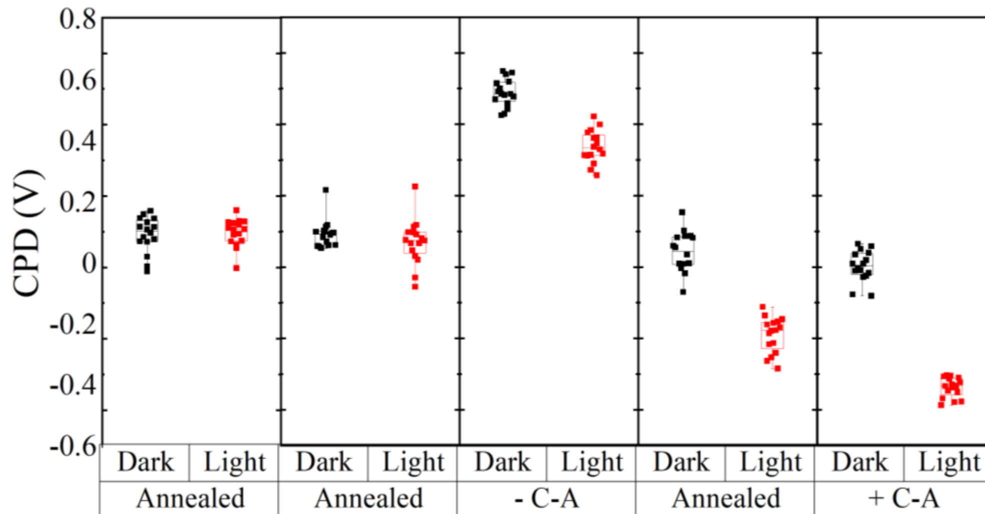


Figure A 11 Measured CPD values of $SiO_x/AlO_x/SiN_x$ stacks on annealed-only sample, before and after – C-A, and before and after + C-A.

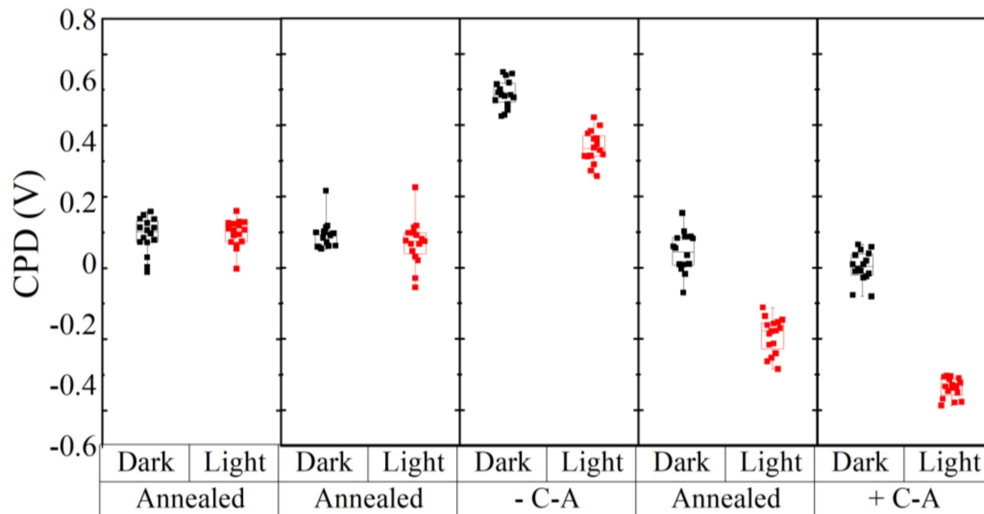


Figure A 12 Measured CPD values of SiO_x/SiN_x stacks on annealed-only sample, before and after – C-A, and before and after + C-A.

Appendix H: Spatial Variation of PL Spectra of 2D MoS_2

The PL spectra shown in Figure A 13 and parameters summarised in Table A 9 were acquired on additional substrates that are outside the scope of this thesis. During this session the spectrometer operated in a non-ideal state (response drift), so the curves appear atypical. Importantly, all spectra were collected sequentially from different areas of the same flake under identical settings. The close similarity of the traces demonstrates minimal area-to-area variation within a single flake. These data are provided solely to illustrate intra-flake uniformity rather than to support quantitative conclusions about substrate effects.

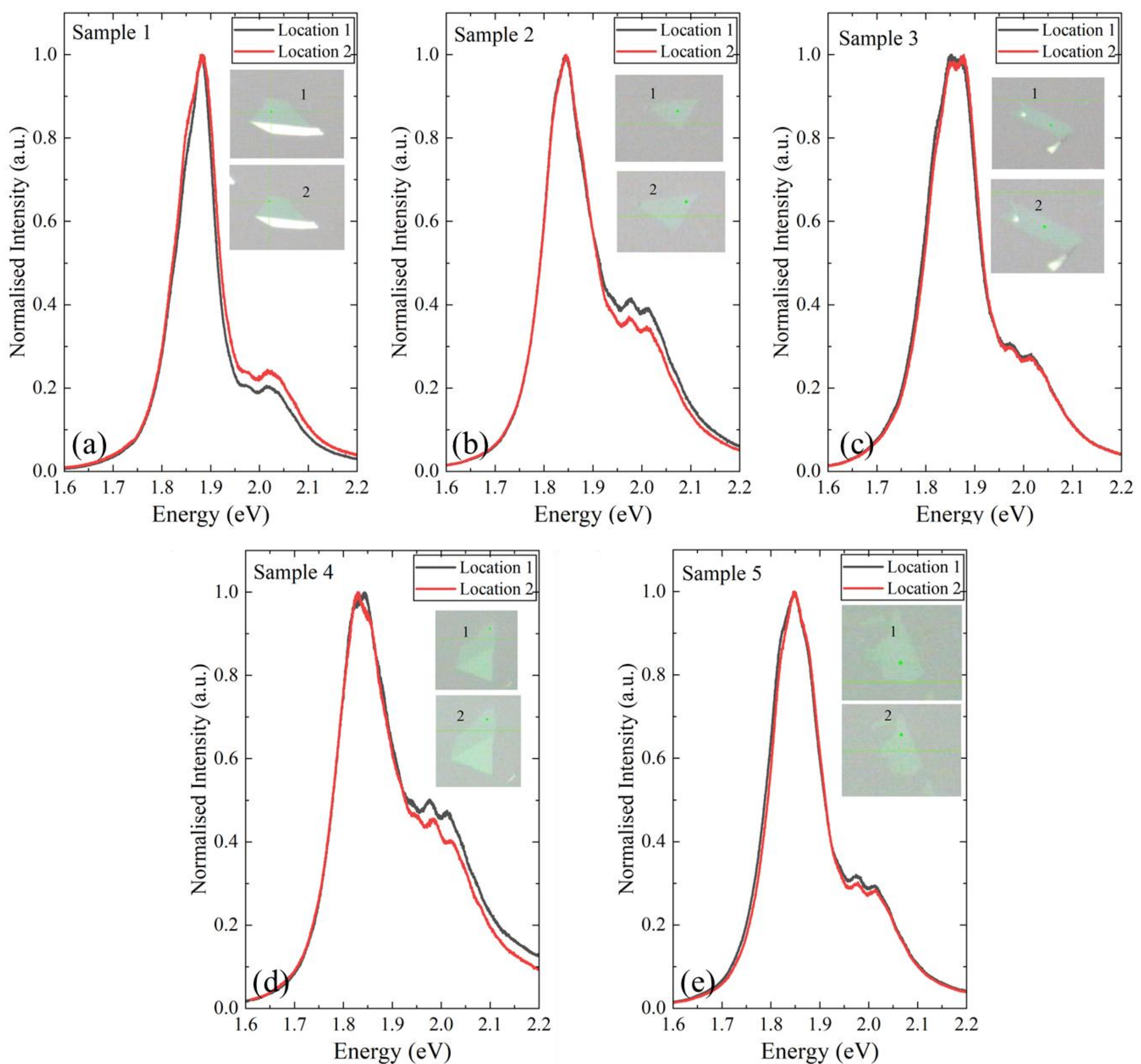


Figure A 13 PL spectra obtained on different locations on the same flake on various substrates. The insets are the optical microscope images of the measured monolayer flakes. The green dots represent the measured location.

Table A 9 Summary of extracted peak positions (x_{A-}, x_{A0}, x_B) and integrated areas (A_{A-}, A_{A0}, A_B) from PL spectra of different locations on MoS_2 flakes on various substrates fitted with a Lorentzian function.

Sample	Location	x_{A-}	x_{A0}	x_B	A_{A-}	A_{A0}	A_B	I_{A-}/I_{A0}	R^2
Sample 1	1	1.84301	1.88437	2.02694	0.05148	0.06916	0.03726	0.74	0.99672
	2	1.84743	1.88868	2.0301	0.06114	0.06794	0.04609	0.90	0.98625
Sample 2	1	1.82518	1.85986	2.00123	0.05968	0.08433	0.11812	0.71	0.99855
	2	1.82643	1.86314	2.00482	0.06712	0.08309	0.09385	0.81	0.99886
Sample 3	1	1.82543	1.87518	2.01353	0.07938	0.08268	0.06054	0.96	0.99384
	2	1.83196	1.8807	2.01582	0.09024	0.07002	0.05878	1.29	0.99419
Sample 4	1	1.81242	1.8543	1.99742	0.05682	0.09075	0.20247	0.63	0.99753
	2	1.81559	1.85728	1.99333	0.07229	0.07943	0.17854	0.91	0.99833
Sample 5	1	1.8248	1.86548	2.009	0.06952	0.09418	0.06662	0.74	0.99907
	2	1.8268	1.87037	2.01319	0.07478	0.0846	0.06033	0.88	0.99896

Appendix I: Optical Microscope Images of 2D MoS_2 Flakes Measured under PL

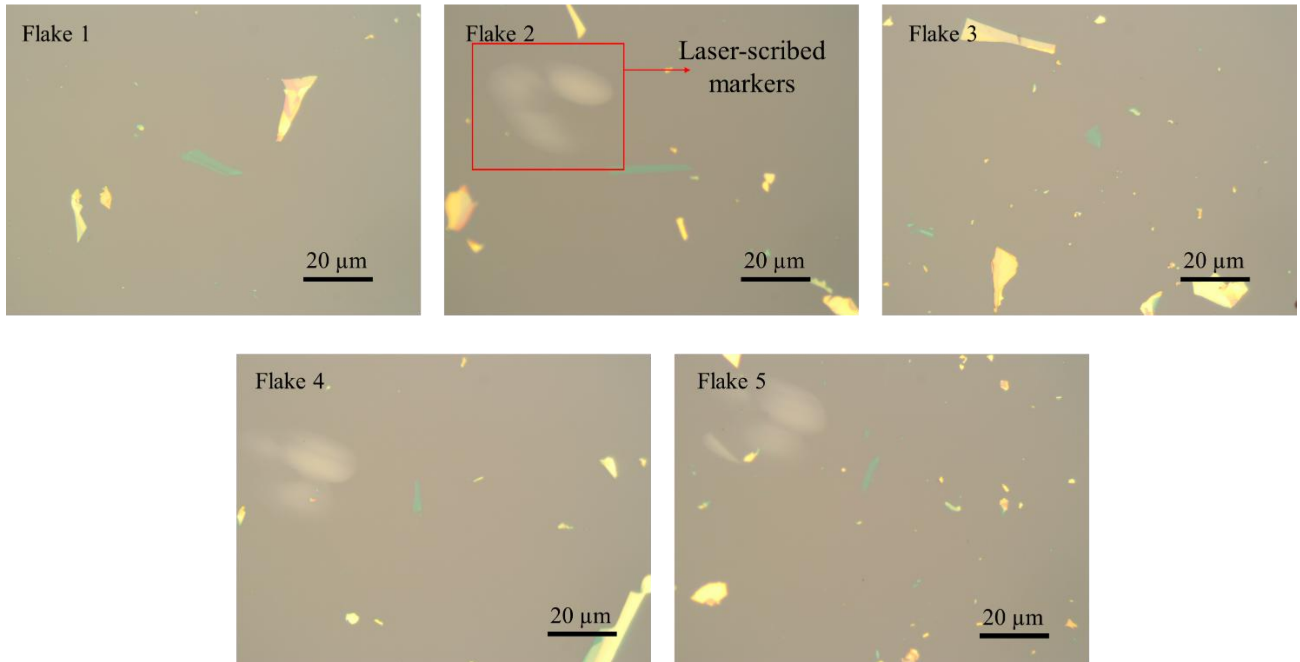


Figure A 14 Optical microscope images of flakes on uncharged SiO_x-capped substrates.

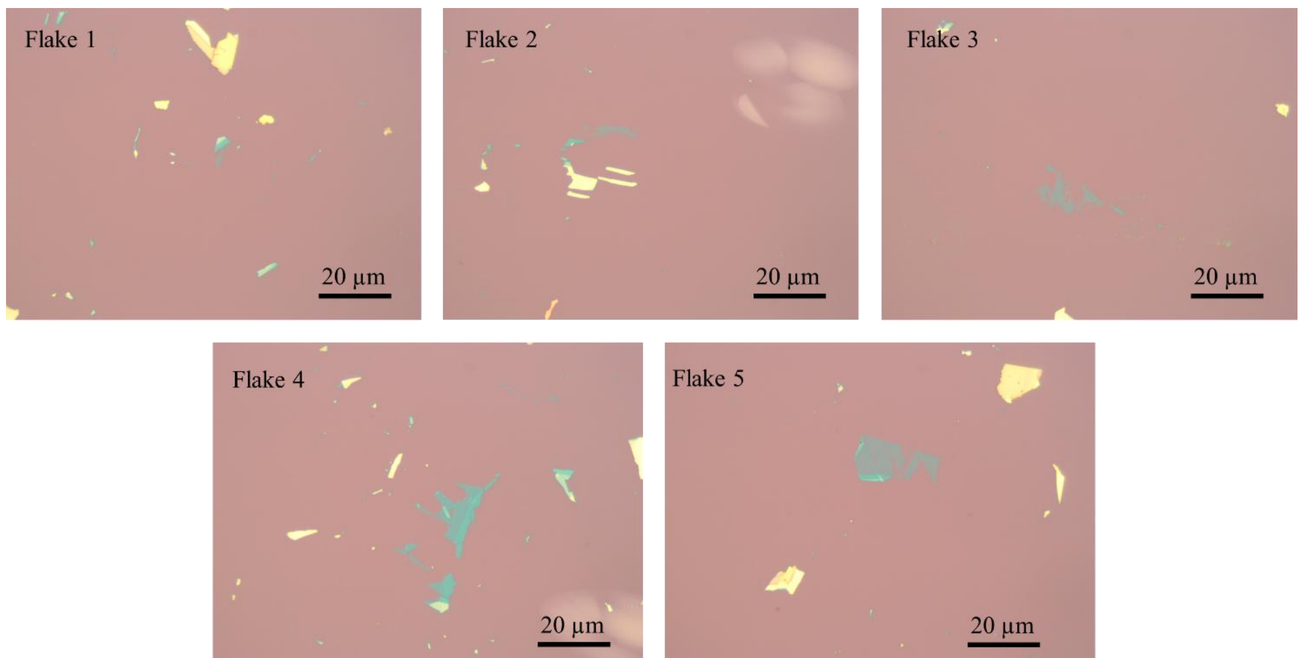


Figure A 15 Optical microscope images of flakes on uncharged AlO_x-capped substrates.

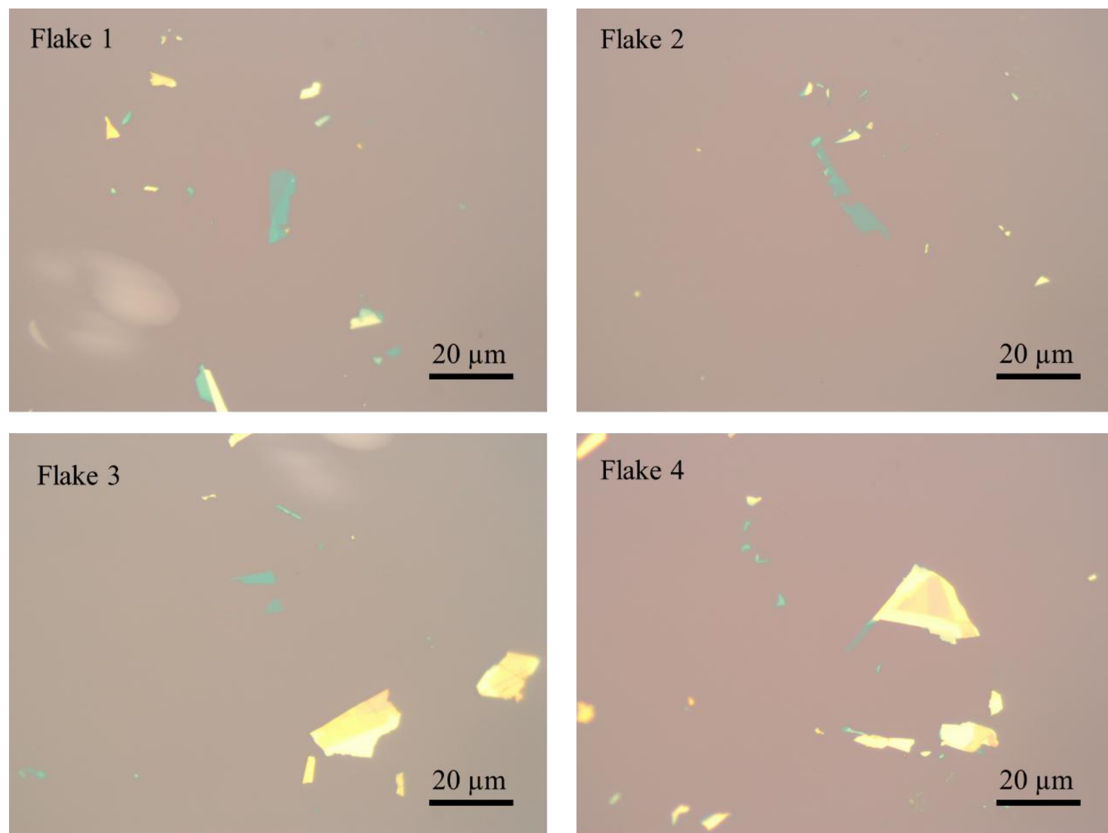


Figure A 16 Optical microscope images of flakes on uncharged HfO_x-capped substrates.

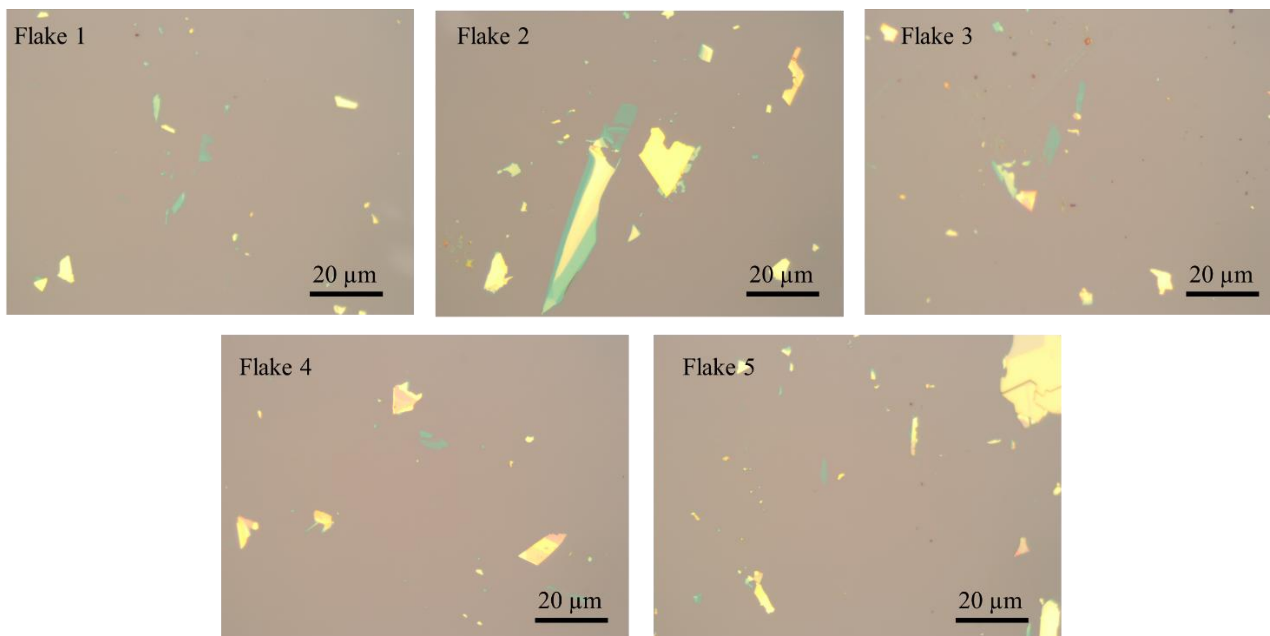


Figure A 17 Optical microscope images of flakes on charged SiO_x-capped substrates.

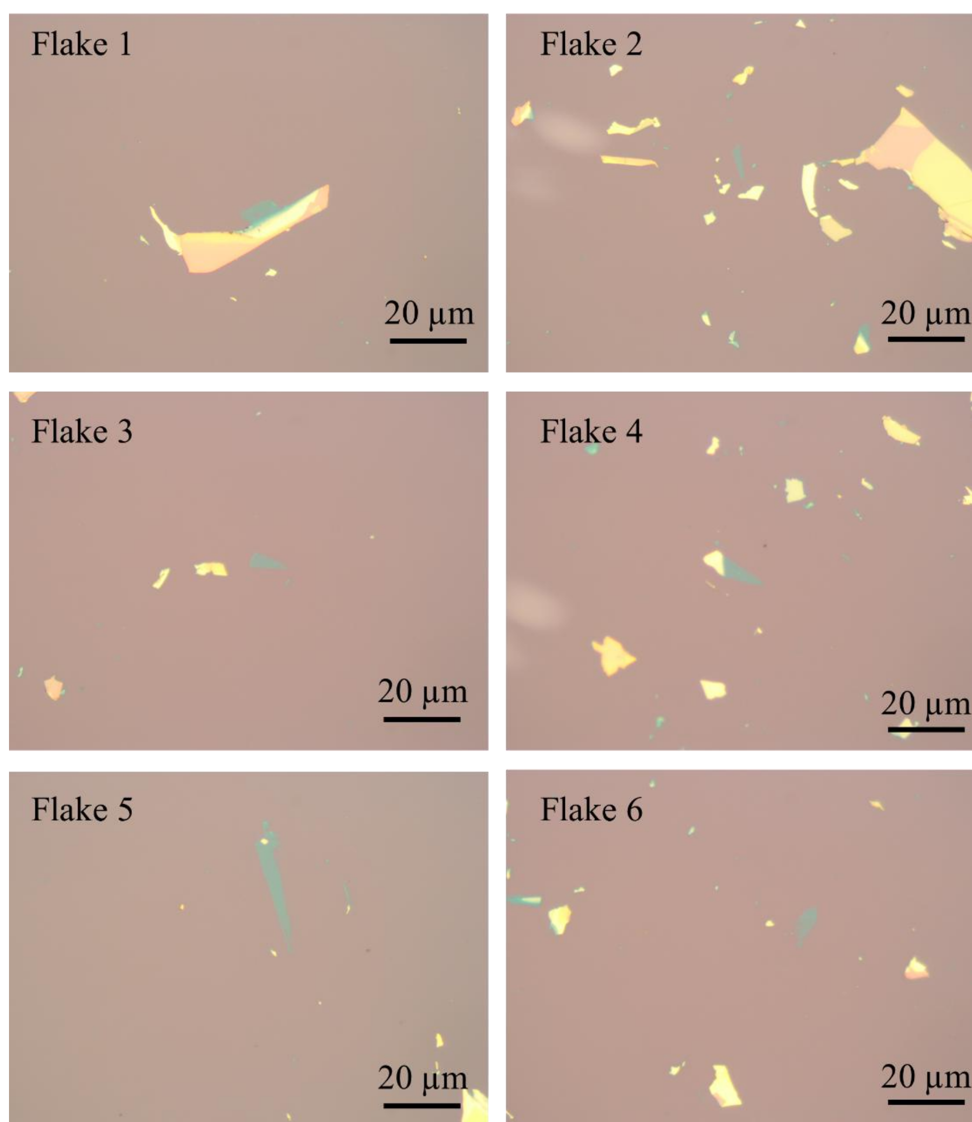


Figure A 18 Optical microscope images of flakes on charged AlO_x-capped substrates.

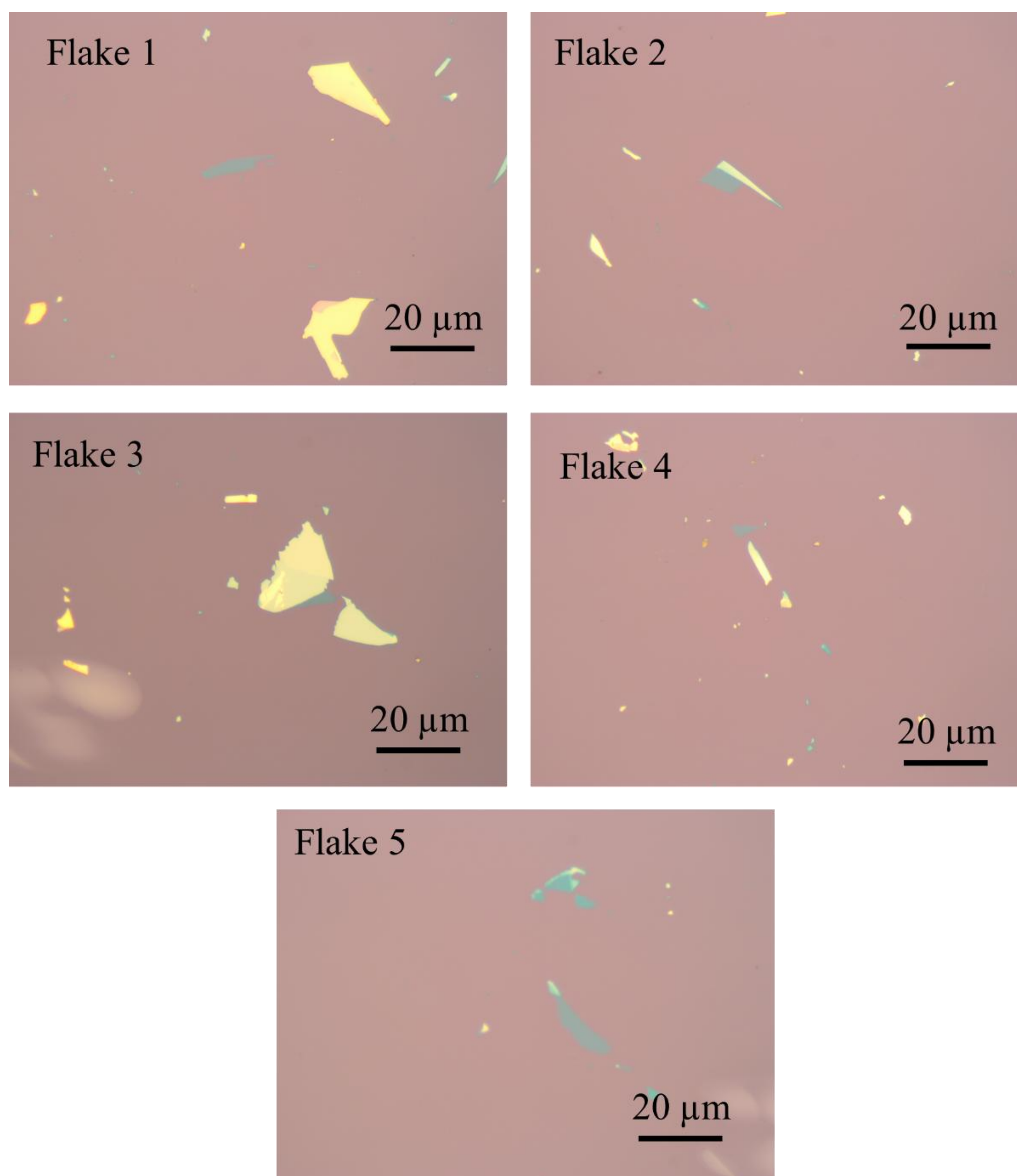


Figure A 19 Optical microscope images of flakes on charged HfO_x-capped substrates.

Appendix J: Choice of Fitting Functions for PL of 2D MoS_2

To justify the choice of a Lorentzian function, the PL spectra from flakes on uncharged HfO_x were refitted using both Lorentzian and Origin's PsdVoigt1 model. The fitted curves are shown in Figure A 20. Peak positions, integrated areas, and the R^2 are summarised in Table A 10. As expected for a model with an additional shape parameter, PsdVoigt1 yields a slightly higher R^2 than the Lorentzian, with visible differences confined mainly to the high-energy tail. Given (i) the negligible impact on the reported quantities and (ii) the instability of the Lorentz-Gaussian split without an instrument constraint, the Lorentzian function was adopted as the minimal sufficient model in the main text. Point (ii) is further demonstrated below.

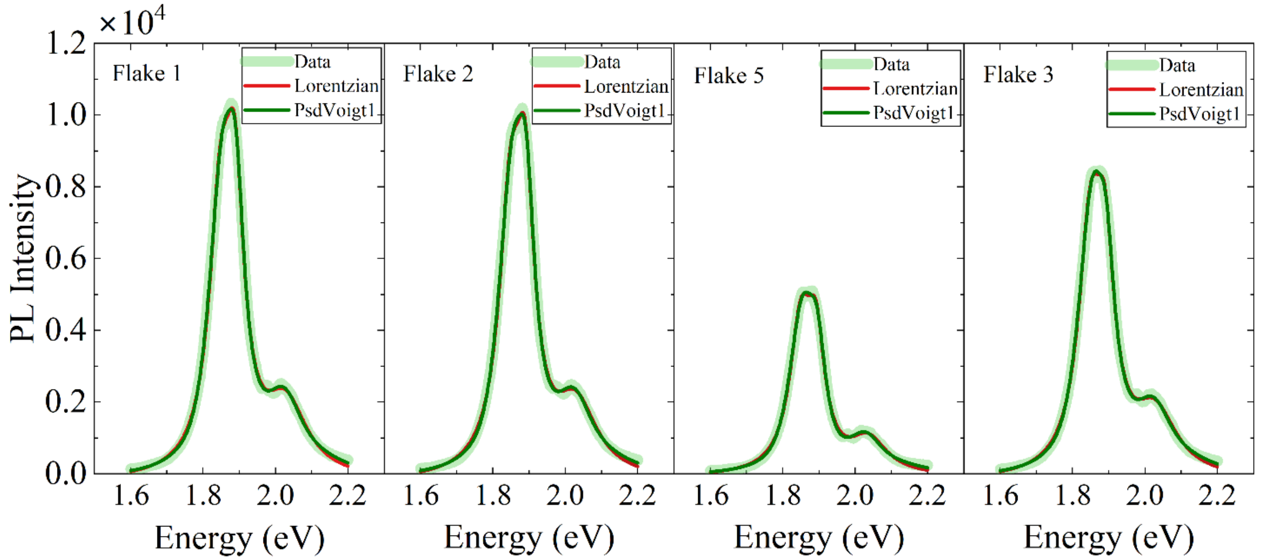


Figure A 20 PL spectra of MoS_2 flakes on uncharged HfO_x-capped substrates fitted with Lorentzian and pseudo-Voigt (PsdVoigt1) line shapes.

Table A 10 Summary of extracted peak positions (x_{A-}, x_{A0}, x_B) and integrated areas (A_{A-}, A_{A0}, A_B) from PL spectra of MoS_2 flakes on uncharged HfO_x, fitted with Lorentzian and PsdVoigt1 models.

Sample	Function	x_{A-}	x_{A0}	x_B	A_{A-}	A_{A0}	A_B	I_{A-}/I_{A0}	R^2
Flake 1	Lorentzian	1.84823	1.88821	2.02762	843.25663	608.5793	444.14051	1.39	0.9994
	PsdVoigt1	1.85211	1.89035	2.0241	901.03652	489.07434	501.9348	1.84	0.9997
Flake 2	Lorentzian	1.84833	1.88961	2.02875	848.73725	608.84888	433.86963	1.39	0.9992
	PsdVoigt1	1.85257	1.89207	2.02438	909.97515	471.92481	492.77882	1.93	0.9997
Flake 5	Lorentzian	1.84984	1.89237	2.03572	473.61442	268.18939	187.03843	1.77	0.9988
	PsdVoigt1	1.85245	1.89513	2.02882	500.55203	187.94338	239.33261	2.66	0.9996
Flake 3	Lorentzian	1.84874	1.89012	2.02681	810.48387	454.6726	400.58997	1.78	0.9993
	PsdVoigt1	1.85295	1.89296	2.0364	863.78824	347.7223	450.28974	2.48	0.9997

Although a Voigt profile can reduce residuals, its extra degree of freedom makes the fit unstable without an instrumental constraint. The Lorentzian and Gaussian contributions trade off, leading to strong parameter covariance and non-unique solutions. In practice, it was found that repeated fits often produce similarly high R^2 (>0.99) while yielding substantially different peak areas. This ambiguity inflates the uncertainty of derived quantities (I_{A-}/I_{A0}) and obscures conclusions. Two remedies are standard: measure and fix the instrumental Gaussian width via a calibration line or acquire low-temperature spectra to minimise inhomogeneous and instrumental broadening. Because neither was available for all datasets, the Lorentzian line shape was adopted as a stable model, which provides comparable and reproducible peak centres and areas across repeated fits. A side-by-side comparison and sensitivity analysis are provided in Figure A 21 and Table A 11.

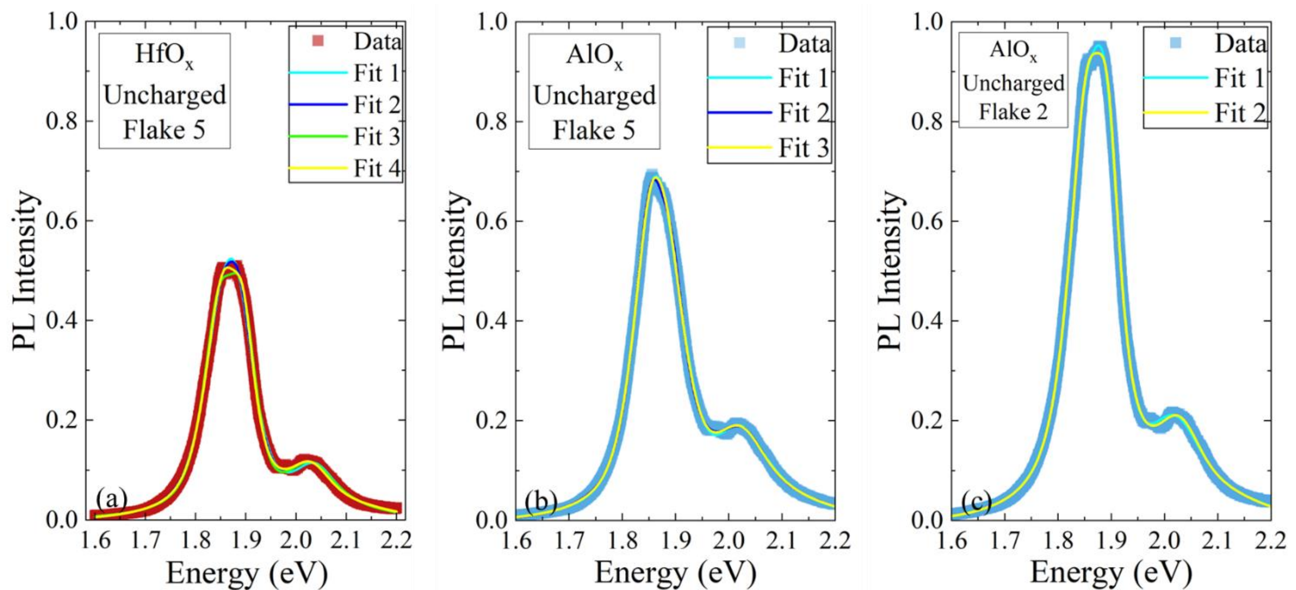


Figure A 21 PL spectra with repeated pseudo-Voigt (PsdVoigt1) fits obtained by varying the initial peak position guesses.

Table A 11 The extracted peak positions and areas from Voigt function fittings selecting different ones.

Sample	Fit	x_{A-}	x_{A0}	x_B	A_{A-}	A_{A0}	A_B	I_{A-}/I_{A0}	R^2
HfO_x Uncharged Flake 5	1	1.84686	1.88421	2.03711	358.62124	343.79529	207.71148	1.04	0.9979
	2	1.84686	1.88747	2.02966	405.36837	284.24002	242.58669	1.43	0.9989
	3	1.84465	1.89282	2.02966	419.14833	244.37873	219.2080	1.72	0.9985
	4	1.85245	1.89513	2.02882	550.55441	187.94172	239.33664	2.93	0.9996
AlO_x Uncharged Flake 5	1	1.85105	1.87886	2.02222	509.51496	346.15361	444.42423	1.47	0.9991
	2	1.8526	1.89421	2.02553	582.32083	332.93047	423.54895	1.75	0.9996
	3	1.85105	1.88747	2.02222	541.40828	340.16159	443.57045	1.59	0.9993
AlO_x Uncharged Flake 2	1	1.84622	1.88854	2.02176	774.6545	466.83874	482.13099	1.66	0.9995
	2	1.85252	1.89342	2.02767	905.02397	378.18836	431.89431	2.39	0.9997

Appendix K: Additional Transfer Curves

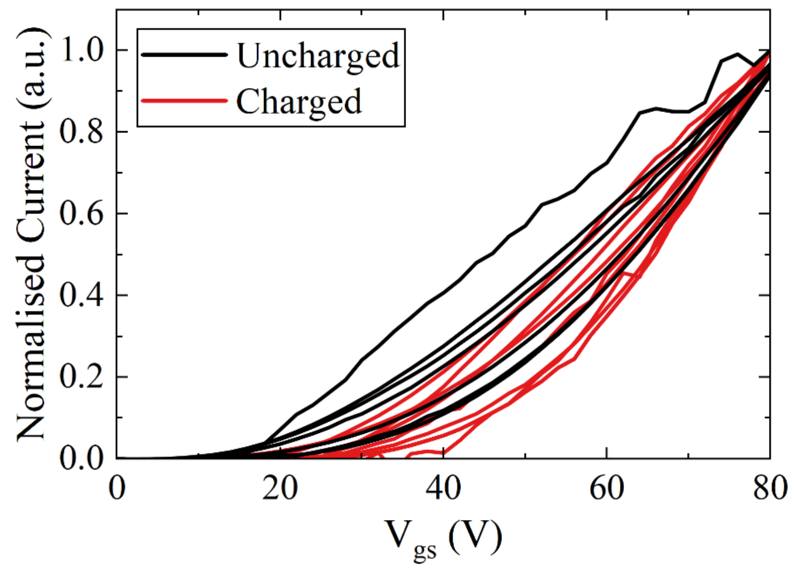
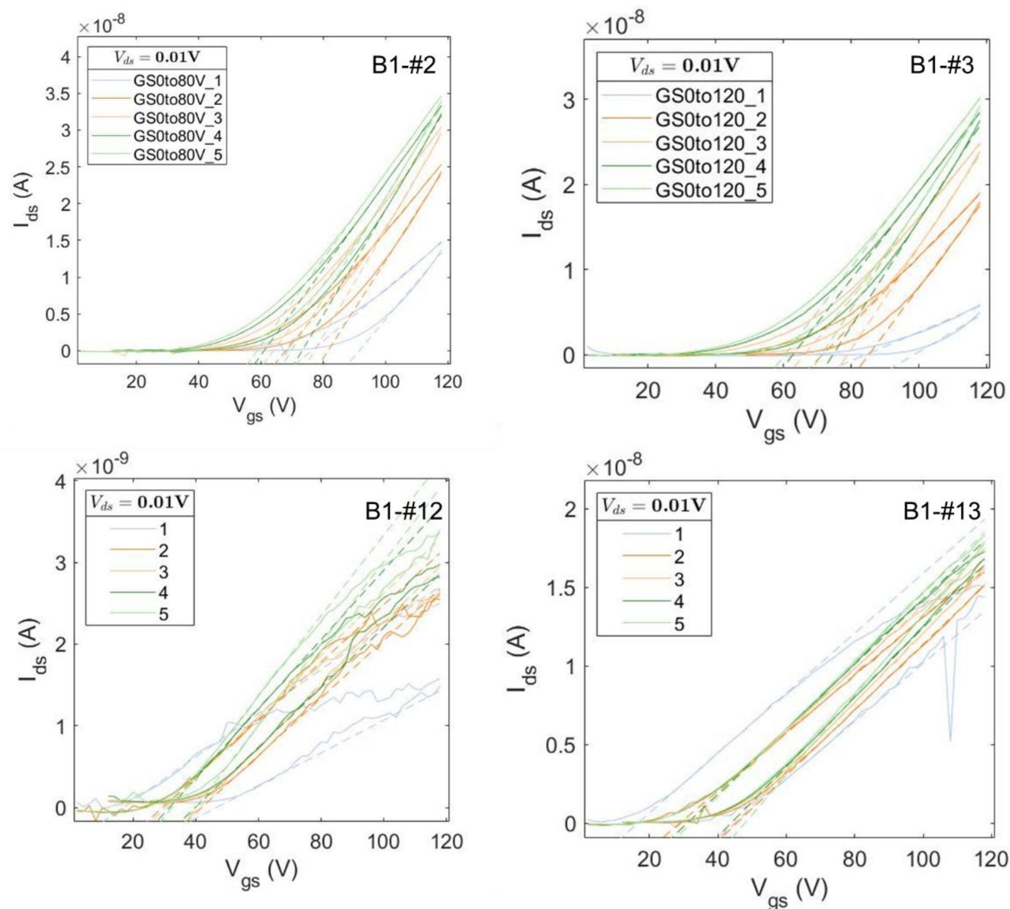


Figure A 22 Normalised forward transfer curves of 2D MoS_2 on uncharged and charged HfO_x-capped substrates. Only the last of the five measurements taken on each device are presented for clarity. This demonstrates the changes in V_{th1} is not an artifact of the change in the measurement range. Transfer curves on charged substrates are normalised to current at 80 V.



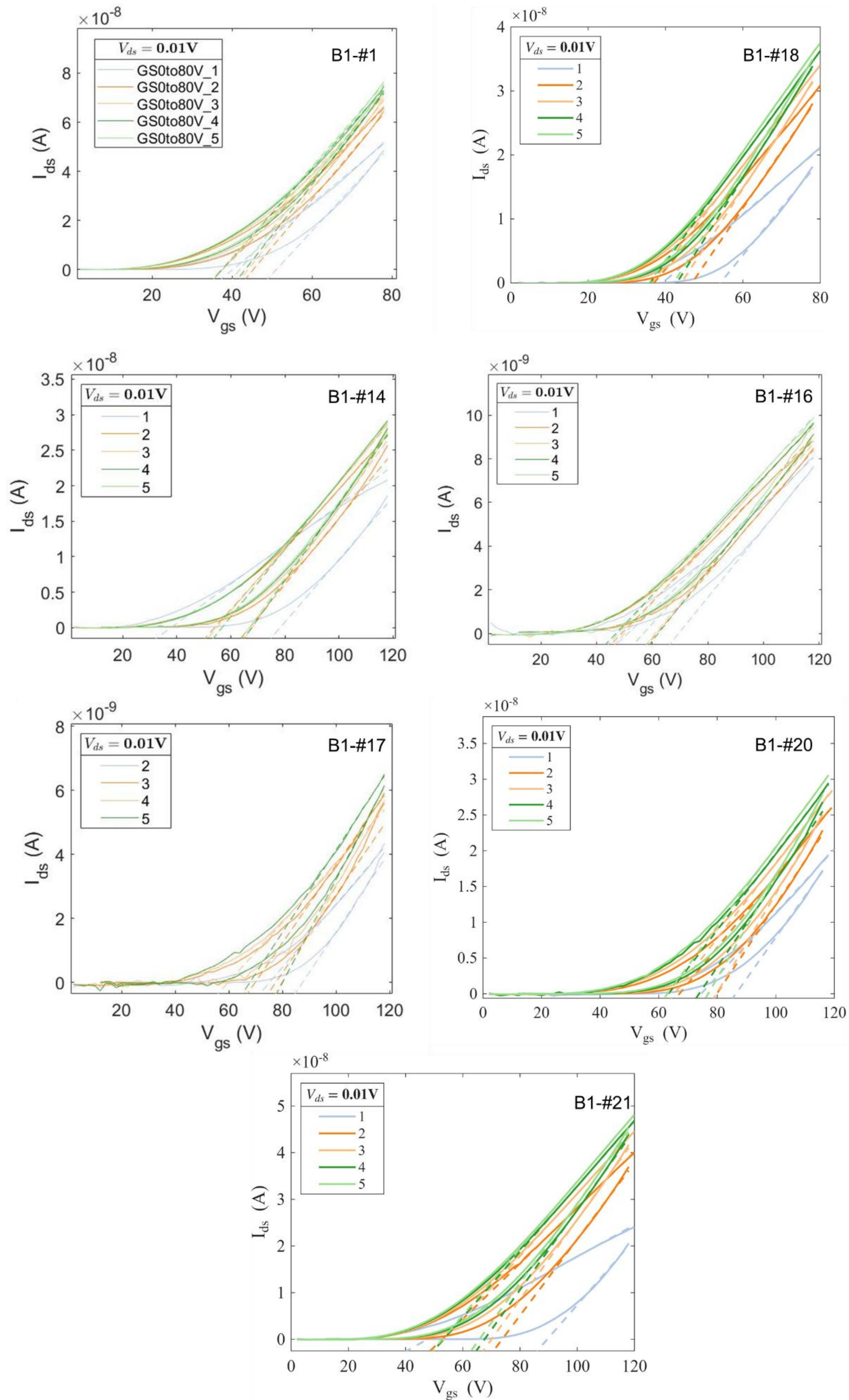


Figure A 23 Five transfer curves measured on each device on HfO_x-capped charged substrates, clearly demonstrating that the increased V_{th1} is not the result of reduced field-effect mobility due to repeated measurements.