Electronic and Optoelectronic Devices Based on 2-Dimensional Heterostructures



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Abstract

Two-dimensional materials, including graphene, h-BN, and monolayer transition metal dichalcogenides such as MoS_2 and WS_2, have attracted enormous attention due to their unique properties and potential application in electronics. A variety of heterostructures devices can be made based on 2D materials. In this thesis, we investigate the electronic and optoelectronic properties of heterostructures of 2D crystals grown by chemical vapor deposition.

In our study on graphene-MoS_2 heterojunction, we show that a rectification ratio over 10^4 can be achieved in Au-MoS_2-graphene device. The rectifying behavior can be tuned by external gating and photo-irradiation. The decrease of rectification ratio under irradiation can be explained by the quick drop of Au-MoS_2 Schottky barrier height, which is derived by fitting the output characteristics of Au-MoS_2-Au and Gr-MoS_2-Gr device as a metal-semiconductor-metal transistor.

The thickness of 2D materials is found to have a great impact on the properties of WS_2-graphene heterostructures. Heterojunction based on graphene and bilayer WS_2 have much higher conductivity and photoresponsivity compared to monolayer WS_2-graphene device. A greater than unity photogain is measured for both devices. The layer-dependent conductivity and photoresponsivity are due to different electron affinities and band gaps of monolayer and bilayer WS_2.

The fabrication methods of vertical heterostructures are also explored, including electron-beam lithography, wet transfer of pre-patterned materials, and graphene printing technique. Using graphene printing, a transfer resolution of 10 mm can be achieved, which is promising to be used in both lateral and vertical device making.

Acknowledgments

This is my final year at Oxford and my DPhil study is coming to an end. I still remember how hopeful and fearful I was when I first arrived here. I could barely speak English and knew almost nothing about 2D electronics. After four years, I am still learning English, but I definitely gained a lot in every respect. I would never reach this far without the help of my supervisor, my colleagues, and my family. So I would like to take this opportunity to say thank you to all of them.

First and foremost, I want to express my immense gratitude to my supervisor, Prof. Jamie Warner, who gave me the chance to study in Oxford and guided me when I lost the direction of my research. Over the years I have benefited so much from his extraordinary vision, knowledge, and patience. He also spent hours correcting my figures and even typoes. And He offered me the opportunity to present my research at UK Semiconductor Conference. My limited vocabulary cannot describe my unlimited thankfulness to him.

And second to my colleagues. Almost all my technical skills were learned from Dr. Ye Fan and Dr. Haijie Tan. They also laid the foundation for my research, which made my experiments not easier but less difficult. Coffee talks with them, from politics in Malasia to quantum computing, were so interesting even though I could not understand at all. My colleagues Yuewen Sheng, Xiaochen Wang, Yingqiu Zhou, Wenshuo Xu, Ren-Jie Chang, Tongxin Chen, Qianyang Zhang, and Linlin Hou provided lots of quality samples. Really appreciate their generosity and please forgive me if I did not yield the equivalent amount of results. My colleagues Dr. Jakyung Lee, Dr. Gyeong Hee Ryu, Dr. Viktoryia Shautsova, Dr. Thomas Samuels, Dr. Chuncheng Gong, Dr. Shanshan Wang, Dr. Qu Chen, Sha Li, Martin Tweedie, Sapna Sinha have all made my study at Oxford enjoyable. Many thanks to them.

Finally, I dedicate this thesis to my family. My beloved fiancée Pu Yan has been extremely supportive. She is the best listener, friend, and chef that I ever met. Her delicately cooked ramen is so delicious that makes all my pressure gone if only I do not have to do the dishes. I am forever in debt to my father Mingxu Huang and mother Xiuyun Wu, not because they provided financial support, but because they love me unconditionally. They supported every decision I made, and I will do everything to let them proud of me.

Publications

Presented here is a list of works submitted and published during the course of this DPhil project. Chapter 4 and chapter 5 are based on the first two papers. Other work listed here is beyond the scope of this thesis.

Huang, H.; Xu, W.; Chen, T.; Chang, R.; Sheng, Y.; Zhang, Q.; Hou, L.; Warner, J. H. High Performance 2D Schottky Diodes Utilizing Chemical Vapour Deposition Grown Graphene-MoS_2 Heterojunctions. *ACS Appl. Mater. Interfaces.* **2018**. 10(43), 37258-37266.

Huang, H.; Sheng, Y.; Zhou, Y.; Zhang, Q.; Hou, L.; Chen, T.; Chang, R.; Warner, J. H. 2D Layer Dependent Behavior in Lateral Au/WS_2/Graphene Photodiode Devices with Optical Modulation of Schottky Barriers. *ACS Appl. Nano Mater.***2018**. 1(12), 6874-6881.

Chen, T.; Sheng, Y.; Zhou, Y.; Chang, R.J.; Wang, X.; Huang, H.; Zhang, Q.; Hou, L.; Warner, J.H. High Photoresponsivity in Ultrathin 2D Lateral Graphene/WS_2/graphene Photodetectors Using Direct CVD Growth. *ACS Appl. Mater. Interfaces*. **2019**. 11(6), 6421-6430.

Zhou, Y.; Xu, W.; Sheng, Y.; Huang, H.; Zhang, Q.; Hou, L.; Shautsova, V.; Warner, J.H. Symmetry-Controlled Reversible Photovoltaic Current Flow in Ultrathin All 2D Vertically Stacked Graphene/MoS_2/WS_2/Graphene Devices. *ACS Appl. Mater. Interfaces*. **2019**. 2234-2242.

Lu, Y.; Chen, T.; Ryu, G.H.; Huang, H.; Sheng, Y.; Chang, R.J.; Warner, J.H. Self-Limiting Growth of High-Quality 2D Monolayer MoS_2 by Direct Sulfurization Using Precursor-Soluble Substrates for Advanced Field-Effect Transistors and Photodetectors. *ACS Appl. Nano Mater.* **2018**. 2(1), 369-378.

Wang, X.; Sheng, Y.; Chang, R.; Lee, J.; Zhou, Y.; Li, S.; Chen, T.; Huang, H.; Porter, B.; Bhaskaran, H.; Warner, J. H. Chemical Vapour Deposition Growth of Two-Dimensional Monolayer Gallium Sulfide Crystals using Hydrogen Reduction of Ga_2S_3. *ACS Omega* **2018**, 3(7), 7897-7903.

Chang, R.; Tan, H.; Wang, X.; Porter, B.; Chen, T, Sheng, Y. Zhou, Y. Huang, H. Bhaskaran, H. Warner, J. H. High-Performance All 2D-Layered Tin Disulfide: Graphene Photodetecting Transistors with Thickness-Controlled Interface Dynamics. *ACS Appl. Mater. Interfaces* **2018**, 10 (15), 13002-13010.

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Chapter 1 Introduction

1.1 Project Aims

This doctoral research aims to explore the fabrication and the electronic as well as optoelectronic properties of heterostructures based on two-dimensional (2D) materials. Lateral and vertical heterostructures made of CVD-grown graphene, MoS_2, WS_2, and BN are fabricated and characterized.

1.2 The Scope of This Thesis

This thesis covers my research results over the DPhil course of four years at the Department of Materials, University of Oxford. A literature review is given in chapter 2 which covers the basic physics of heterostructures, production of 2D materials, and relevant properties and applications of 2D materials and heterostructures. Methodology in chapter 3 demonstrates the techniques used in materials synthesis, device fabrication, and characterization and data processing.

Chapter 4 summarizes my research on three types of lateral heterostructures consisting of graphene, gold, and MoS_2. Rectifying behavior is found in Au/MoS_2/Gr heterostructures and the rectification can be tuned by static gating and laser irradiation. The mechanism is explained by modulated Au-MoS_2 and MoS_2-graphene Schottky barriers, which is directly evidenced by the output characteristics of Au-MoS_2-Au and Gr-MoS_2-Gr transistors.

Chapter 5 extends the study of heterostructure to WS_2. Both monolayer and bilayer WS_2 are studied in Au/WS_2/graphene heterostructure. Devices based on monolayer and bilayer

WS_2 display distinct conductivity and photoresponsivity. The difference is attributed to the different work functions and bandgaps between monolayer and bilayer WS_2.

Chapter 6 covers the investigation of vertical heterostructures based on 2D materials. A series of techniques were attempted to manufacture vertical heterostructures using 2D materials, including conventional e-beam lithography, transfer of pre-patterned materials, and graphene printing. The electronic properties of Gr/BN/Gr, Gr/Gr crossbars, and graphene transistors were studied.

The final chapter summarizes the results and discusses future research that may address the limitations of my research.

Chapter 2 Literature Review

2.1 Introduction

Two dimensional (2D) materials are crystals consisting of a single unit cell layer. Because carriers in 2D materials are confined in two dimensions, 2D materials display 2D transport properties and have a 2D density of states, as distinct from quantum dots (0D), nanotubes (1D), and bulk materials (3D). Although people used to believe that free-standing 2D materials are not stable at room temperature, graphene, a flake of carbon atoms, was extracted from graphite by Prof. Andre Geim and Prof. Konstantin Novoselov in 2004.[1]

The discovery of graphene makes 2D materials promising candidates for future electronic devices. The semiconductor and electronics industry has developed rapidly and the demands on novel devices, such as fast-charging batteries, wearable devices, and ultrafast computers, have emerged. 2D materials and their heterostructures might make these ideas possible. For example, graphene has ultrahigh mobility and it is predicted graphene transistors can be significantly faster than silicon transistors.[2] The mechanical flexibility of 2D materials also enables us to explore the manufacturing of foldable electronics.[3]

Heterostructures, such as p-n junction and Schottky junctions, are building blocks of modern electronics including logic gates, sensors, solar cells, etc. Thus heterostructures made of 2D materials are of great interest to study. The aim of this chapter is to review the recent progress of 2D materials and their heterostructures. To do this, the physics of heterostructures is summarized, including p-n junctions and metal-semiconductor junctions. The properties of the metal-semiconductor-metal transistor are discussed. Then the production methods and electronic

properties of 2D materials are covered. Based on all of the knowledge above, the applications of heterostructures based on 2D materials are reviewed.

2.2 Fundamentals of Heterostructures

A heterostructure or heterojunction is formed when two regions of different crystals are put together.[4] Heterostructures are essential for modern electronics due to their unique properties. One of the most intensively studied structure is the p-n junction.

2.2.1 p-n Junction

A p-n junction is formed when an n-type semiconductor (donor doped) and p-type (acceptor doped) semiconductor are put into contact.[5] The different doping levels will result in band bending and a depletion region at the interface, shown in **Figure 2.1**.

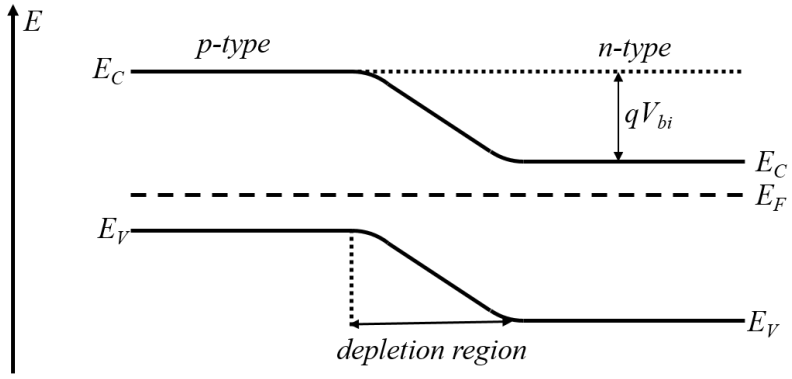


Figure 2.1. Energy band diagram of a p-n junction diode under zero bias. Reproduced with permission.[6]

The n-type (negative) semiconductor contains an excess of electrons and the p-type (positive) semiconductor contains an excess of holes. When connected together, an electrical field is formed at the interface as conduction electrons will diffuse down the concentration

gradient from the n-type to the p-type material, and similarly holes will diffuse in the opposite direction. This leaves a depletion zone at the interface.The resulting built-in or diffusion potential of a p-n junction can be obtained by the following expression:

$$V_{bi} = V_T \ln\left(\frac{N_d N_a}{n_i^2}\right), \quad (2\text{-}1)$$

where V_{bi} is the built-in potential in thermal equilibrium, n_i is the intrinsic carrier density, $V_T = k_B T/q$ is the thermal voltage, N_d is the donor-impurity density, and N_a is the acceptor-impurity density.[6] Due to the existence of the internal electrical field (potential difference), the junction only allows electrical current to pass through in one direction but not the other way. If the junction is made by putting two separate pieces of semiconductor together, the interface may be full of defects, which are likely to influence the property of the junction by scattering the carriers.

2.2.1.1 Forward Bias

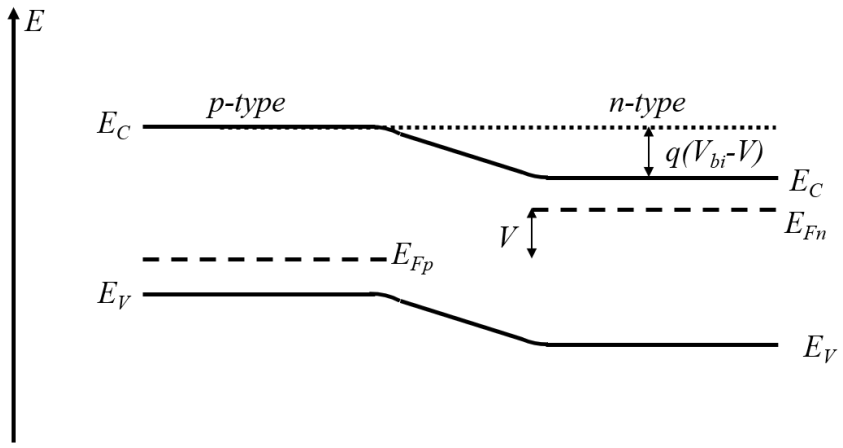


Figure 2.2. Energy band diagram of a p-n junction diode under forward bias. Reproduced with permission.[6]

Forward bias refers to the condition when the p-type region connected to the positive terminal of the battery and the n-type region is connected to the negative terminal. When a

forward-bias voltage V is applied to the junction, the potential barrier across the junction will decrease to ($V_{bi} - V$), as shown in **Figure 2.2**. The potential barrier for diffusion of the majority carriers is reduced, and the depletion layer width is decreased, resulting in a large increase in current flow across the junction.

2.2.1.2 Reverse Bias

Reverse bias refers to the condition that the p-type region is connected to the negative terminal of the battery and n-type region connected to the positive terminal. When a reverse-bias voltage V_R is applied, the potential barrier across the junction will increase to ($V_{bi} + V$), as shown in **Figure 2.3**. In this case, the potential barrier for the majority carriers and the depletion layer width will increase, resulting in a very small current flow through the junction, until sufficient voltage is applied to and the diode breaks down. The breakdown process can occur by different mechanisms, namely Zener or avalanche breakdown.[7,8] However, for both mechanisms, the breakdown is not destructive as long as the device is not damaged due to thermal heating. In many cases, a relatively low breakdown voltage is preferred. For example, it can be used to regulate the largest voltage in the circuit, because the diode may break down, and thus become conductive, when exceeding that breakdown voltage

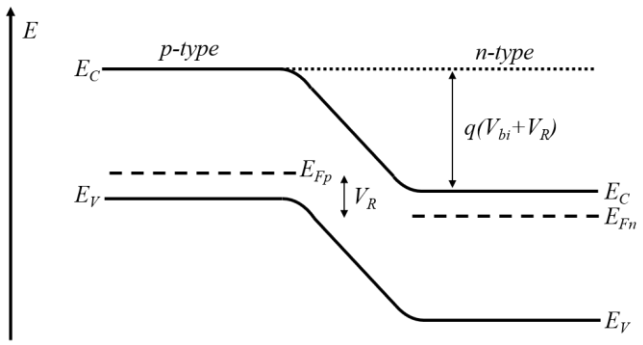


Figure 2.3. Energy band diagram of a p-n junction diode under reverse bias. Reproduced with permission.[6]

p-n junctions are fundamental components of modern electronic devices. Diodes,[9] solar cells,[10] LEDs,[11] and integrated circuits[12] can all be manufactured based on p-n junctions. Among all the p-n junctions, a special case is a Schottky junction, where metal and semiconductor are put together.[13]

2.2.2 Metal-Semiconductor Junction

When a metal (M) and a semiconductor(S) are put into contact, it forms a metal-semiconductor junction. The oldest practical semiconductor device used in early computers is made of a metal-semiconductor junction. The property of an M-S junction depends on the electron affinity and work function of the materials, resulting in either rectifying or non-rectifying behavior. The rectifying behavior is attributed to a Schottky barrier formed at the interface, making a device known as a Schottky diode. When an Ohmic contact is formed at the interface, the heterojunction displays a non-rectifying behavior.[13,14]

Metal-semiconductor heterostructures play an important role in semiconductor devices. An ohmic contact is favored for connecting electrodes with semiconductor channel and Schottky barrier is wanted for making functional devices such as rectifiers and logic diodes.[15]

2.2.2.1 Barrier height

As just discussed, a metal-semiconductor junction can be either rectifying or non-rectifying, which depends on the height of the Schottky barrier $\emptyset_B$.[13] When the Schottky barrier height is large enough, the semiconductor is depleted near the metal and behaves as a Schottky barrier. When the Schottky barrier is low enough, the semiconductor is not depleted and the junction

behaves as an Ohmic contact. The energy band diagram of a metal/n-type Schottky barrier diode under zero bias is shown in **Figure 2.4a**.

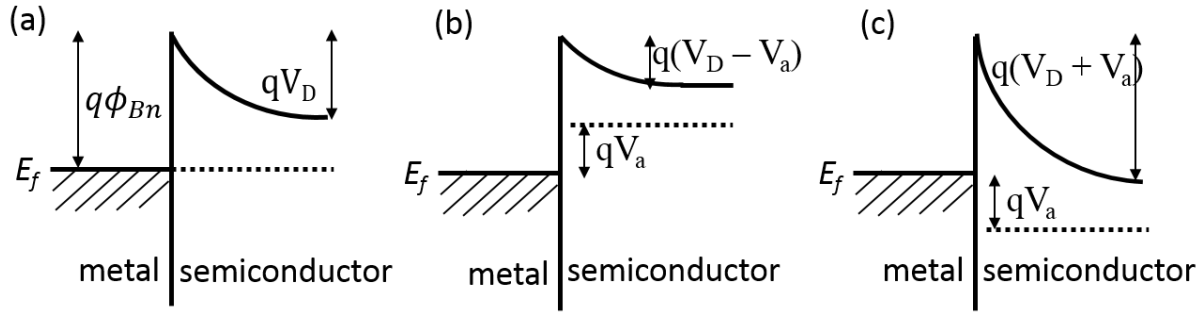


Figure 2.4. Energy band diagram of a metal/n-type Schottky barrier diode under (a) zero bias, (b) forward bias, and (c) reverse bias. Reproduced with permission.[6]

The Schottky barrier is the potential barrier for electrons moving from the metal side to the semiconductor side. The barrier height for a metal/n-type Schottky diode can be estimated using Schottky-Mott rule,[16]:

$$\emptyset_{Bn} = \Phi_{Metal} - \chi_{Semiconductor}, \tag{2-2}$$

where Φ_{Metal} is the work function of metal (and graphene), and $\chi_{Semiconductor}$ is the electron affinity of the semiconductor, as shown in **Figure 2.4a**. Because the Fermi levels of n-doped and p-doped semiconductors are different (measured from the conduction band edge and valence band respectively), the Schottky barrier heights are different for p-doped and n-doped semiconductor as well. The p-type Schottky barrier height $\emptyset_{Bp}$ and n-type Schottky barrier height ($\emptyset_{Bn}$, for the same metal) are related to each other through the following equations:

$$\emptyset_{Bp} = E_g - \emptyset_{Bn} = E_g - \Phi_{Metal} + \chi_{Semiconductor}, \tag{2-3}$$

where E_g is the semiconductor's bandgap, Φ_{Metal} is the work function of metal (and graphene), and $\chi_{Semiconductor}$ is the electron affinity of the semiconductor.

The contact potential or the diffusion potential V_D is the potential barrier for electrons moving from the semiconductor side to the metal side, as shown in **Figure 2.4a**. It can be expressed by:

$$V_D = \emptyset_{Bn} - V_n = \emptyset_{Bn} - (E_c - E_f) = \emptyset_{Bn} - (k_B T)\ln(\frac{N_c}{N_D}), \quad (2\text{-}4)$$

where $\emptyset_{Bn}$ is the barrier height, $V_n = E_c - E_f = (k_B T)\ln(\frac{N_c}{N_D})$is the Fermi (or chemical) potential of the n-type semiconductor, E_c is the conduction band, E_f is the fermi level, k_B is the Boltzmann constant, T is the absolute temperature, N_c is the effective density of states in the conduction band, and N_D is the concentration of donor atoms. The semiconducting materials including WS_2 and MoS_2 synthesized in my experiments are n-doped semiconductors.

2.2.2.2 Forward bias and reverse bias

A Schottky diode is under forward bias when the metal side is positively biased and the semiconductor side is negatively biased. The diode is under reverse bias when the metal side is negatively biased and the semiconductor side is positively biased. Under a forward bias voltage V_a, the Schottky barrier height remains relatively unaffected but the potential barrier on the semiconductor side of the diode is reduced to $V_D - V_a$, as shown in **Figure 2.4b**. And the net current flow from the semiconductor to the metal increases significantly. Under reverse bias, the potential barrier on the semiconductor side increases to $V_D + V_a$ as shown in **Figure 2.4c**. The

current flow from the semiconductor to the metal decreases dramatically and the diode becomes non-conductive. Thus, the I-V characteristics of a Schottky diode also show rectifying behavior.

2.2.2.3 Fermi level pinning

The validity of Schottky-Mott rule varies when using different semiconductors. It correctly predicts the existence of band bending in the semiconductor but the Schottky barrier height is not perfectly accurate when the surface state density is high. This effect is called Fermi level pinning.[17] As shown in **Figure 2.5**, the surface states are represented by the energy level $\emptyset_0$. This energy level can be considered as a separate level, and the surface states below the energy level must be filled in order to satisfy the charge-neutrality condition at the surface. The Fermi level at the surface will be pinned at $\emptyset_0$ if the surface states become significantly large and the Schottky barrier height for the metal-semiconductor contact and becomes independent of metal work function or doping level. Research shows that the Schottky barrier height for an n-type semiconductor with very high surface state density is estimated to be two-thirds of the bandgap energy:

$$\Phi_B \approx \frac{2}{3} E_g \tag{2-5}$$

where E_g is the size of the bandgap in the semiconductor.[6]

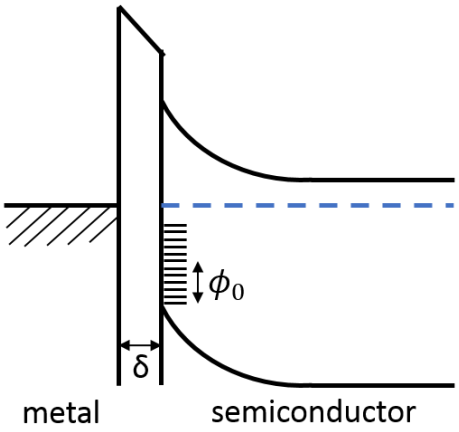


Figure 2.5. Energy band diagram for an ideal metal/n-type semiconductor, in contact with a small air gap δ and interfaces states. Reproduced with permission.[6]

2.2.3 Metal-Semiconductor-Metal Device

For a typical semiconductor transistor connected with metal electrodes, two Schottky barriers are formed at the interface of metal and semiconductor. Thus, a metal-semiconductor-metal device can be modelled simply as a back-to-back diode with a series resistor. If the two metal electrodes are the same, the two Schottky barriers have the same height and the diode is called symmetrical back-to-back diode, as shown in **Figure 2.6a**. If the two metal electrodes are different, then the diode is called asymmetrical back-to-back diode, as shown in **Figure 2.6b**.

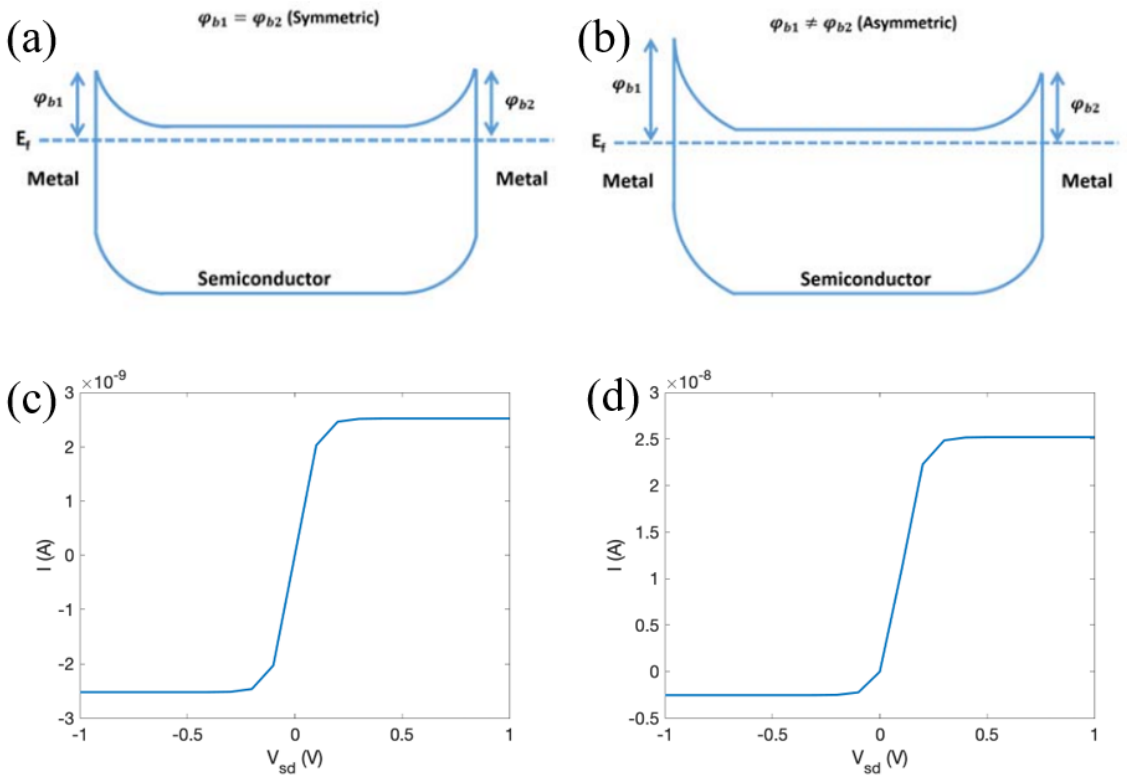


Figure 2.6. The band diagrams of metal-semiconductor-metal devices and simulated I-V curves of symmetrical/asymmetrical back-to-back diodes. (a) Band diagram of symmetrical back-to-back Schottky diodes. (b) Band diagram of asymmetrical back-to-back Schottky diodes. (c) Simulated I-V curve of symmetrical back-to-back diodes using CircuitLab. (d) Simulated I-V curve of asymmetrical back-to-back diodes using CircuitLab. Reproduced with permission.[18]

The simulation of I-V curves in **Figure 2.6c** and **Figure 2.6d** has been performed in CircuitLab. For the symmetrical back-to-back diode simulation, both diodes have a maximum reverse current of 2.52×10^{-9} A, an ideality factor of 1.752, and resistance of 0.568 Ω. For the asymmetrical back-to-back diode simulation, one diode has a maximum reverse current of 2.52×10^{-9} A, an ideality factor of 1.752, and resistance of 0.568 Ω, and the other diode has a maximum reverse current of 2.52×10^{-8} A, an ideality factor of 1.752, and resistance of 0.568 Ω. It can be seen that theoretically, the symmetrical back-to-back barrier curve shows non-linear and symmetrical I-V characteristics around the zero current mark. And the asymmetrical back-to-

back barrier curve shows non-linear and rectifying behaviour, with current saturating as V is increased. Examples of symmetrical and asymmetrical back-to-back diodes are shown in **Figure.2.7**.

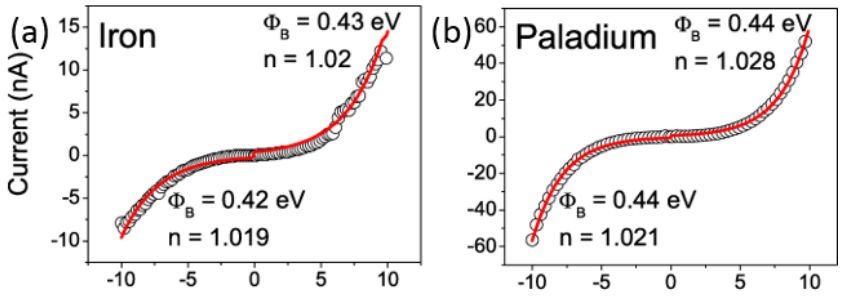


Figure 2.7. Measured I-V curves of SnO_2 transistor with (a) iron electrodes and (b) palladium electrodes. Red lines are fitted curves to extract ideality factor (n) and effective barrier height. Reproduced with permission.[19]

However, in practice, even when the two metal electrodes are the same, the I-V curve of the metal-semiconductor-metal device, such as Au-$MoTe_2$-Au transistor, can also be rectifying, as shown in **Figure 2.8**.[20]

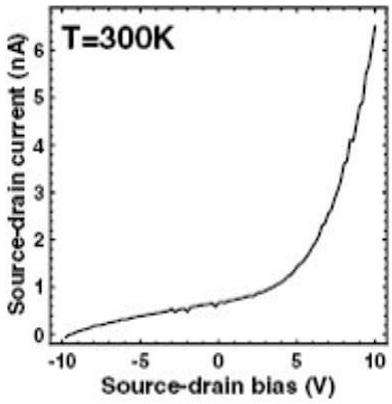


Figure 2.8. I-V curve of Au-$MoTe_2$-Au transistor. Few-layer $MoTe_2$ flake was obtained by exfoliation and the curve was measured at 300K. Reproduced with permission.[20]

This is because the semiconductor interface potential at one electrode is pinned by the bottom gate thus the energy barrier is essentially fixed. On the other side, the electrostatic potential of the biased interface decreases the barrier height with forward bias. In this case, though against intuition, the metal-semiconductor-metal device is more appropriatelyconsidered as a single diode connected with a series resistor. The estimated Schottky barrier height of $MoTe_2$-Au is about 30.3 meV for example.[20]

For an asymmetrical back-to-back diode, the non-linear and rectifying I-V curve of the device has been shown before in Figure 2.6b. Further research shows that an asymmetrical back-to-back diode can be well fitted as a single Schottky diode, especially when the series resistance is large, as shown in **Figure 2.9**.

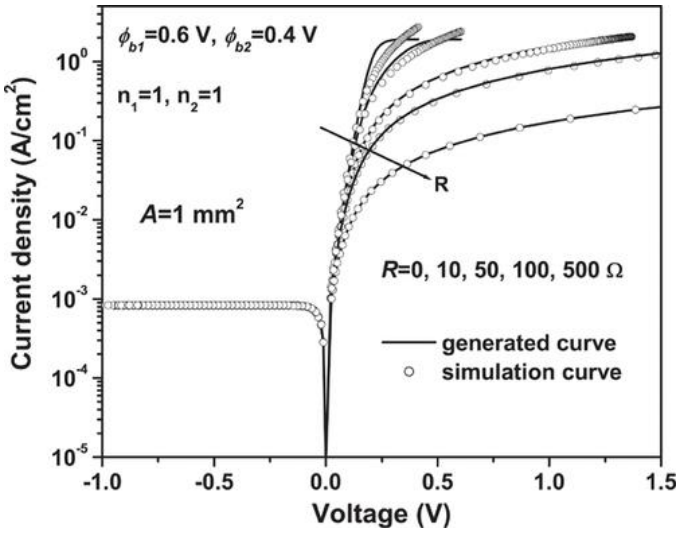


Figure 2.9. Dependence of I-V curves of back-to-back diode with Schottky barriers equal to 0.6V and 0.4V, on the series resistance. Black line: generated I-V curves of the back-to-back diode. White dote: simulated I-V curves based on a single Schottky diode. Reproduced with permission.[21]

When the series resistance is 500 Ω, the extracted parameters modelling the device as a single Schottky barrier (the device itself is an asymmetrical back-to-back diode) gives series resistance = 506 Ω and Schottky barrier height = 0.6 eV, with a rectification ratio over 10^4. That

is to say, the I-V curve of the asymmetrical back-to-back diode of different Schottky barrier heights maintains similar features of a single diode of the higher Schottky barrier height.[21]

2.3 Production Methods of 2D materials

There are several methods to obtain 2D crystals, such as exfoliation,[22] hydrothermal self-assembly,[23] chemical vapor deposition,[24] reduction of graphite oxide,[25] and nanotube slicing.[26] The list of production techniques is still rapidly expanding but currently, the most popular techniques are exfoliation and chemical vapor deposition (CVD). In this section, an overview of the techniques within these two categories is presented.

2.3.1 Exfoliation

Exfoliation is a top-down method to isolate 2D materials from bulk states. For example, graphene was discovered by isolating a single layer of graphene from graphite. The advantage of the exfoliation method is that the obtained materials usually have fewer defects and high electron mobility.[27,28]

2.3.1.1 Mechanical Exfoliation

To perform mechanical exfoliation, an adhesive tape, such as scotch-tape, is needed.[23] A piece of graphite is stuck onto the tape, as shown in **Figure 2.10a**. The tape is then folded and separated repeatedly until a single layer of graphite is obtained. Multilayer graphene is shown in **Figure 2.10b**. This exfoliation method can also be applied to other 2D materials such as MoS_2 and h-BN.[29,30] The tape can also be mounted onto a translator so that the separated 2D materials can be transferred onto a certain location. 2D heterostructures can also be stacked up using this

method. Though mechanical exfoliation is widely used to isolate materials and make proof-of-concept devices, the disadvantages are obvious: the yield rate is low and the exfoliation is labour intensive thus not suitable for large-scale production.

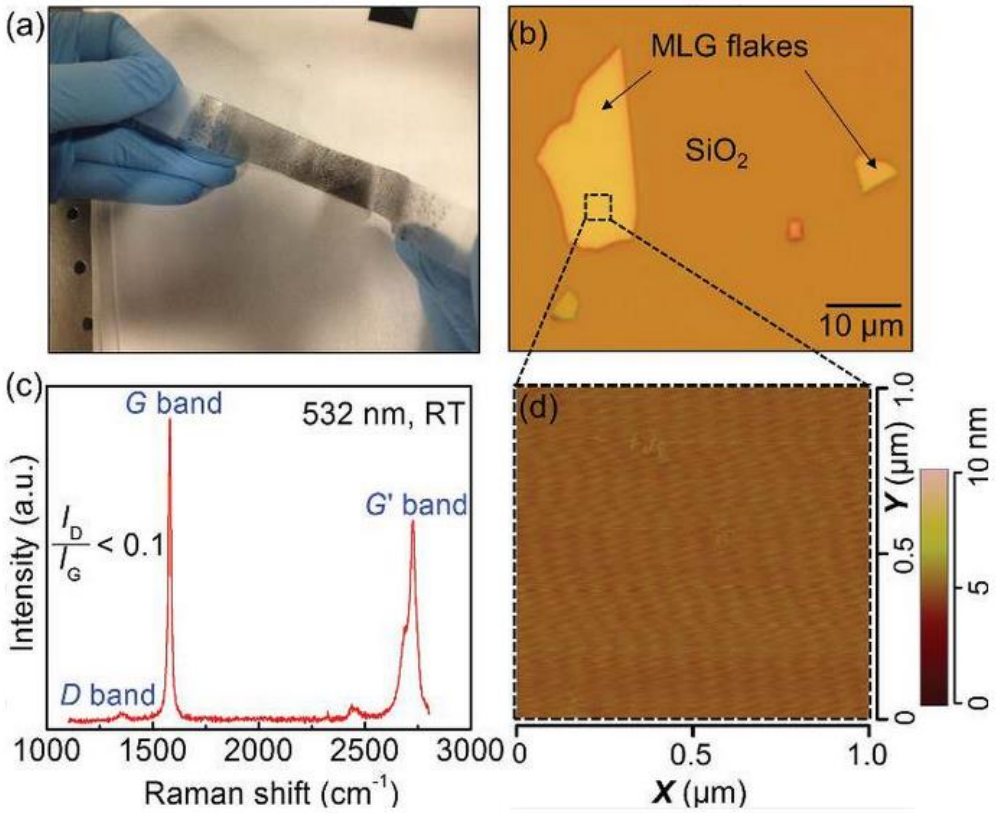


Figure 2.10. Mechanical exfoliation of graphene multilayer. (a) Exfoliated multilayer graphene with graphite on adhesive tape. (b) Optical image of multilayer graphene flakes. (c) Raman spectrum of the graphene. (d). AFM image of the framed region in (b). Reproduced with permission.[31]

2.3.1.2 Liquid Exfoliation

Another way to isolate single-layer crystal from bulk layered materials is sonicating bulk materials, which is promising to generate large quantities of exfoliated 2D materials. The solvents used for the exfoliation need to match the bulk materials to prevent solute aggregation. Taking graphene as an example, graphite powder was put into N-methylpyrrolidone (NMP) and

after sonication and centrifugation, the liquid containing graphene flakes is obtained. NMP and dimethylformamide (NDF) have been reported to produce graphene, BN, MoS_2, and WS_2.[32-34] **Figure 2.11** is an example of liquid exfoliation of various 2D materials using water.[35]

Compared to mechanical exfoliation, liquid exfoliation is easier to perform and more cost-efficient. The disadvantage is that the produced 2D materials are often not uniform. Flakes of different sizes and number of layers are often randomly dispersed on the substrates. And it can be time-consuming to find the suitable flakes.

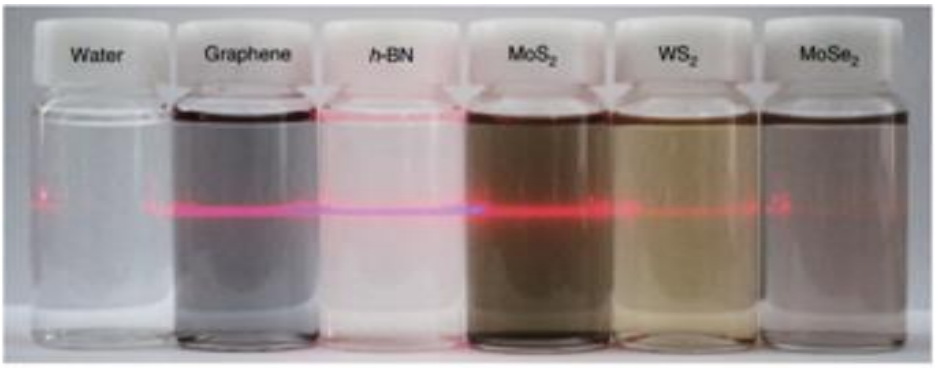


Figure 2.11. Images 5 types of solution of 2D materials dispersed in DI water for one month. Reproduced with permission.[35]

2.3.2 Chemical Vapor Deposition

Though the exfoliated 2D materials may be of good quality and free of chemical dopants, it is not suitable for large-scale production. Chemical vapor deposition, a bottom-up method, is promising to produce wafer-size 2D materials of high quality at a relatively cheap price. The main disadvantage is that the substrates used for growth have to be detached afterward,[36] which may require wet transfer and thus will introduce chemical dopants and cause cracks in the

materials. All the 2D materials, including graphene, MoS_2, WS_2, and BN used in this study were synthesized using the CVD method.

2.3.2.1 CVD Synthesis of Graphene

Graphene can be grown on Ni,[37] Cu,[38] Ru,[39] Ir,[40] Pt,[41] Co,[42] and other substrates using CVD method. The most commonly used substrates are Ni and Cu and they are briefly summarized below.

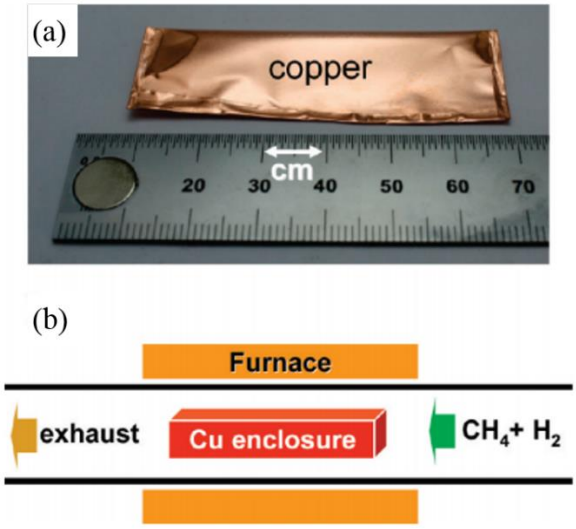


Figure 2.12 Chemical vapor deposition of graphene on Copper. (a) Copper foil enclosure prior to insertion in the furnace. (b) Schematic of the CVD system for graphene on copper. Reproduced with permission.[44]

Polycrystalline Ni films are first annealed to increase grain size at 900-1000°C in H_2/Argon atmosphere. Then CH_4/H_2 is introduced into the furnace. During this step, CH_4 decomposes and carbon atoms dissolve into the Ni film and form a solution. After that, the system is cooled down in argon gas to room temperature, during which the carbon atoms gradually diffuse out of Ni-C

solution and form into graphene film. Graphene synthesized on Ni is usually continuous film with both monolayer and multi-layer regions.[37, 43]

Using copper as the substrates one can achieve an improved quality of graphene. The schematic of the setup is shown in **Figure 2.12**. Copper foil is annealed in H_2/Argon at 1000 °C and then exposed to the CH_4/H_2 mixture. The system is then cooled down to room temperature. Graphene synthesized on Cu substrate is usually uniform as copper plays a role as a catalyst during the reaction. When a layer of graphene is synthesized on top of the copper, the further reaction is prohibited as copper and CH_4 are no longer in contact.[44] This self-limiting reaction results in better quality and uniformity. The temperature and synthesis time used in the reaction may vary slightly. The detailed process of graphene synthesis in my research is presented in Chapter 3 Research Methodology.

Graphene can also be synthesized on melted copper, as developed by my senior colleagues.[45] In this method, copper is mounted on top of a piece of tungsten. Due to the higher melting point of tungsten, it works as physical support. The substrate is then heated above the melting point of copper (1090°C). Crystal domains larger than 200 μm can be obtained by precisely controlling the amount of hydrogen used in the growth. The mechanism is revealed by stopping the growth before forming a complete film. It can be seen that domains of graphene are aligned in orientation, which yields graphene of larger domains and better quality.[45] The main drawback of this method is that the yield rate is limited, as a large piece of copper on uneven tungsten may spill when it melts.

2.3.2.2 CVD Synthesis of MoS_2 and WS_2

CVD methods are also utilized to grow large-scale transition metal dichalcogenide (TMD) crystals with precisely controlled thickness and domain sizes. Three types of method can be classified according to their growth mechanisms.[46]

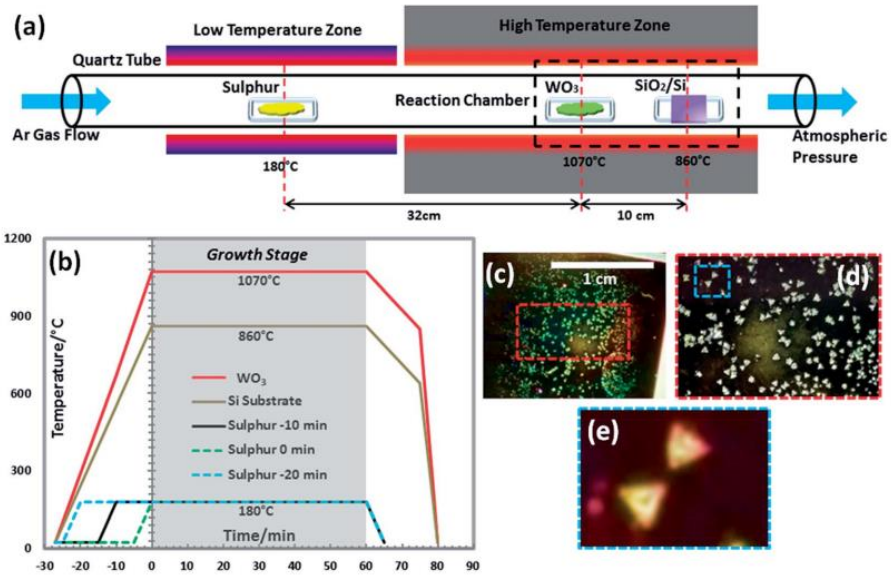


Figure 2.13 CVD synthesis of WS_2 domains on SiO_2/Si substrate. (a) Schematic figure of the experimental set-up. (b) Temperature profiles for the reaction. (c) Optical image of large triangular WS_2 crystals on SiO_2/Si substrate. (d) Optical image of the framed region in (c). (e) Optical image of the framed region in (d). Reproduced with permission.[51]

The first is the co-vaporization and decomposition of both metal oxides and chalcogen precursors, followed by a vapor phase reaction and deposition of TMD on a substrate. Properties of substrates, temperature, and atomic gas flux are reported to be key parameters influencing the characteristics of synthesized TMDs.[47,48] Large-scale MoS_2 layers were synthesized by Lee et al by CVD method using molybdenum trioxide (MoO_3) and sulfur powder at the temperatures around 650 °C.[49] The MoO_3 is first reduced into MoO_{3-x} by sulfur and then reacts with sulfur to form 2D layered MoS_2 film. The typical experimental setup and growth process is shown in

Figure 2.13a and **2.13b.** This method is relatively easy to operate but it often the case that synthesized flakes are randomly distributed, as shown in **Figure 2.13c – 2.13e**. Shape evolution of CVD grown MoS_2 domains from triangular to hexagonal is also found, depending on the spatial location of the silicon substrate.[50]

The second method is the direct sulfurization of metal films. A transition metal (Mo, W, Nb, etc) thin film is deposited on the substrate followed by thermal reaction with chalcogen (S, Se, Te) vapor at high temperatures (300-700 °C). Using this method, a wafer-scale MoS_2 film can be obtained and the layer number of MoS_2 can be controlled.[52] The thickness of grown MoS_2 is related to the thickness of deposited metal. In 2012, Zhan et al achieved the growth of MoS_2 using e-beam evaporation and CVD methods.[53] The measured mobility is in the range of 0.004-0.04 $cm^2V^{-1}s^{-1}$ as p-type conduction.

Metal-organic chemical vapor deposition is the third commonly used method. Different from the previous two methods, a metal-organic complex is used as a precursor in the reaction. Kang et al accomplished the synthesis of wafer-scale monolayer and multilayer MoS_2 and WS_2 on SiO_2 substrates using molybdenum hexacarbonyl ($Mo(CO)_6$), tungsten hexacarbonyl ($W(CO)_6$), ethylene disulfide ($(C_2H_5)_2S$) and H_2 gas-phase precursors.[54] Iy this way, wafer-scale uniform TMDs can be grown and the composition, as well as morphology, can be modified. The main limitation is that metal-organic gas, such as $W(CO)_6$ are very toxic and could be a hazard to operators if leaked from the chamber.

2.3.2.3 CVD Synthesis of h-BN

Hexagonal boron nitride (h-BN) can also be synthesized using the CVD method.[55] Cu and Ni can be used as substrates.[56] Song et al found that when Ammonia borane (NH_3-BH_3) was sublimed at around 120 °C and introduced to H_2/Ar gas flow, Boron nitride thin films with a

large optical band gap of 5.56 eV can be synthesized onto a substrate,[57] CVD growth of h-BN using other precursors, such as BF_3/NH_3 has also been reported.[58] Though the growth of few-layer h-BN on a large scale has been achieved, control of thickness and crystalline quality still needs further improvement.

2.4 Electronic Properties of 2D Materials

The ultrathin nature of 2D materials makes it is possible to design electronics of reduced channel thickness, which lead to improved gate control over the channel barrier and reduced short-channel effects.[59,60] Thus the application of 2D materials provides a promising solution for the compelling demand for electronics of better performance. In the following section, the electronic properties of graphene, TMDs, and BN are introduced.

2.4.1 Graphene

Graphene is a single layer of carbon atoms forming into a hexagonal lattice (honeycomb shape). It is semi-metallic (zero bandgap semiconductor) as there is a small overlap between its cone-shaped conduction and valence bands. Dirac points are the K points of the Brillouin zone where the conduction and valence bands connect, as shown in **Figure 2.14a**.[61] The valence and conduction bands connect at the Dirac point, where the density of states (DOS) is minimum and close to zero.

Unconventional superconductivity was also observed in bilayer graphene with an orientation angle of 1.1° of the two layers and may lead to more insight into the mechanism of high-critical-temperature superconductors.[62]

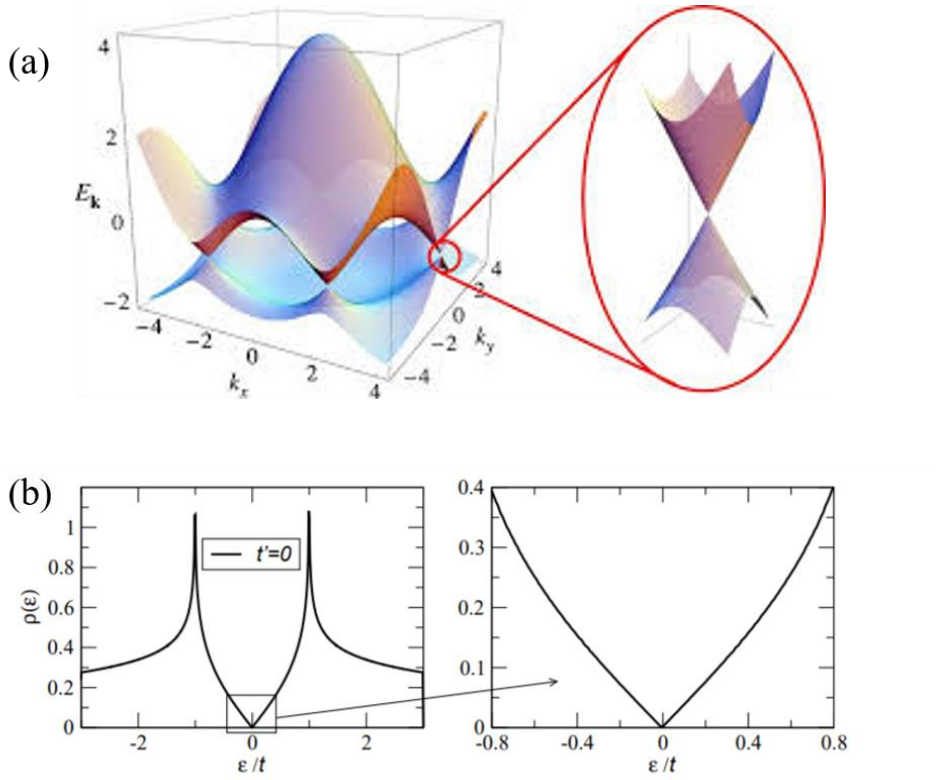


Figure 2.14 Band structure and density of states (DOS) of ideal graphene. (a) The band structure of graphene. (b) Calculated results of DOS of ideal graphene. Reproduced with permission.[61]

2.4.1.1 Bandgap engineering

The lack of a bandgap makes graphene very difficult to switch off, which results in a low on-off ratio and limits its application in logic devices. Much effort has been devoted to 'open' a bandgap of graphene. In general, there are several routes to do this.

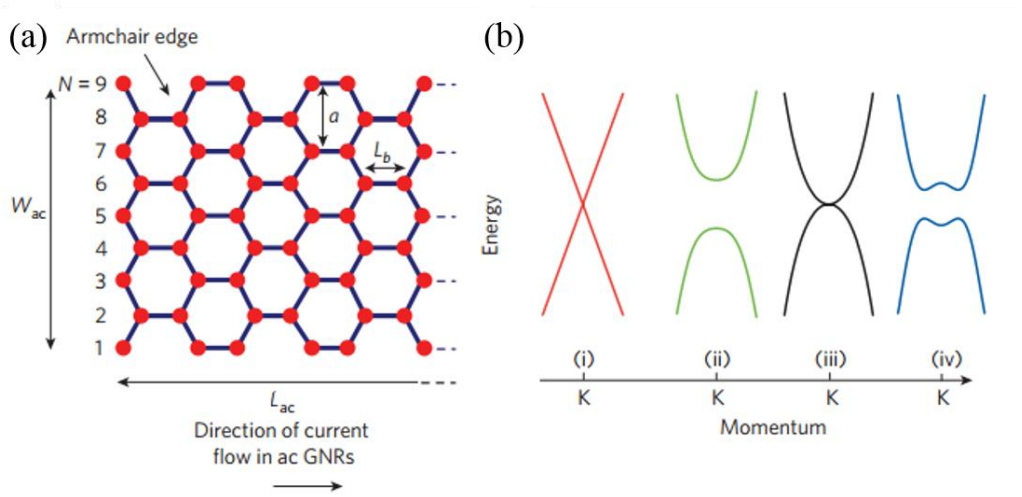


Figure 2.15 Properties of graphene and graphene nanoribbons. (a) Schematic of an armchair graphene nanoribbon. (b) Band structure around the K point of (i) large-area graphene, (ii) graphene nanoribbons, (iii) unbiased bilayer graphene, and (iv) bilayer graphene with the an applied perpendicular field. Reproduced with permission.[69]

The first one is to confine the dimension of graphene by making graphene into a very narrow ribbon, namely a graphene nanoribbon (GNR). The behavior of a graphene nanoribbon is different from a graphene film, due to the nanoscale size effect. The properties of graphene nanoribbons depend on the edge states of ribbons, which are armchair and zigzag shapes respectively.[63-65] It is predicted that zigzag GNRs are always metallic, supported by calculations based on tight-binding theory. By density functional theory (DFT), it is predicted that armchair nanoribbons, as shown in **Figure 2.15a**, are semiconducting.[66] When the width of GNR decreases, the bandgap becomes wider. Experiments on lithographically patterned graphene ribbons also verified the fact that the energy gap scales inversely with the ribbon width. When the width of the graphene ribbon gets close to 15 nm, a bandgap of around 0.1 meV was observed, as shown in **Figure 2.15b**.[67] The existence of bandgap in graphene nanoribbons

provides a technological alternative to silicon in the semiconductor industry. Graphene field-effect transistors with a width less than 10nm have been made and demonstrated an I_{on}/I_{off} ratio over 10^6 at room temperature.[68]

The second route to engineering a bandgap in graphene is to apply an external vertical electric field to bilayer graphene. The DFT calculation suggests that bilayer graphene is also metallic, shown in **Figure 2.15b**. The two parabolic-shape conduction and valence bands meet at K point when not biased. But a bandgap will be generated when a perpendicular electric field is applied.[70] Using this method, a graphene transistor with I_{on}/I_{off} ratio of 100 at room temperature has been reported.[71]

It was also reported that the opening of bandgaps at the Fermi level of graphene can be achieved by applying asymmetrical strain. Strain distribution parallel to C-C bonds and perpendicular to C-C bonds function differently but will generate a maximum width of 0.486eV when the parallel strain increases up to 12.2%.[72]

2.4.1.2 Carrier transport

The effective mass of charge carriers in graphene is quite small,[73] which results in a high carrier mobility. The electron mobility of graphene is reported that more than 1.5×10^4 $cm^2V^{-1}s^{-1}$ at room temperature.[74] Higher electron mobility, 2×10^5 $cm^2V^{-1}s^{-1}$, is reported for suspended single-layer graphene. This suggests that carrier mobility can be as high as that if it is free from charged impurities and ripples.[2] A promising way to approach is to use h-BN as a substrate or encapsulating layer for graphene. As h-BN is atomically flat and chemically inert, it will prevent chemical dopants from entering the graphene layer. The graphene mobility can be improved to

1×10^5 $cm^2V^{-1}s^{-1}$ at room temperature.[75] A statistics of mobilities of typical semiconductor materials is shown in **Figure 2.16**. It can be seen that graphene, in general, has higher electron mobility compared to silicon (around 500 $cm^2V^{-1}s^{-1}$). The mobilities of MoS_2 and WS_2 can be comparable to silicon but have larger variance.

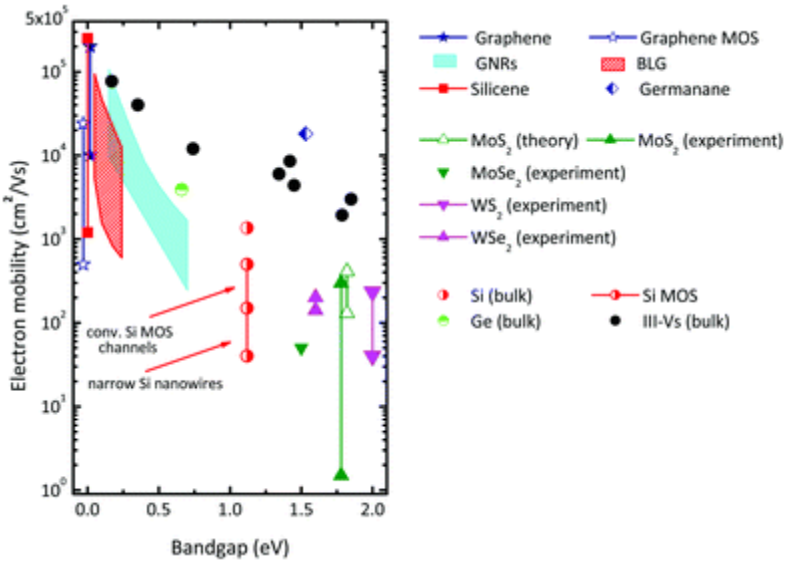


Figure 2.16 Statistics of room-temperature electron mobility and bandgap for various materials. Reproduced with permission.[76]

2.4.2 Transition Metal Dichalcogenides

Graphene is a fascinating material and it has been intensively studied. However, the lack of bandgap makes it is difficult to be applied in industry-level electronics. Meanwhile, transition metal dichalcogenides (TMDs, or TMDCs) provide an alternative due to their sizeable bandgaps. Transition metal dichalcogenides are semiconductors of MX_2 atomic form, in which M is a transition metal atom (group IV, V, VI, VII, IX, or X. Such as Mo, W, etc) and X is a chalcogen atom (S, Se, Te, etc).[77]

2.4.2.1 Crystal Lattice and Band structure

A single layer TMD consists of three layers of atoms: one layer of transition metal (M) sandwiched by two layers of chalcogen atoms. However, there are three types of lattices depending on the particular combination of transition and chalcogen elements. For TMDs formed by group VI transition metals (Mo or W), the most thermodynamically stable phase is a 2H phase, shown in **Figure 2.17**.

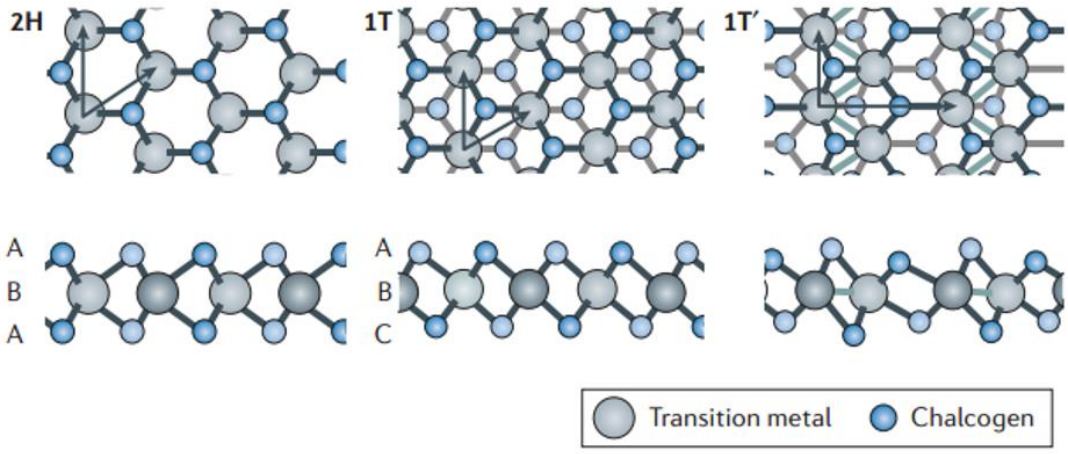


Figure 2.17 Atomic structure of single layers of transition metal dichalcogenides (TMDs) in their trigonal prismatic (2H), distorted octahedral (1T) and dimerized (1T') phases. Lattice vectors and stacking of atomic planes are indicated. Reproduced with permission.[77-79]

Here I focus on MoS_2 and WS_2 (group VI TMDs) as they are the two most studied TMDs materials due to their robustness and feasibility. The band structure of TMDs depends on the thickness of the materials. The bandgaps of bulk and monolayer MoS_2 are estimated to be 1.2 eV and 1.8eV respectively.[78,80] Mak et al studied the layer-dependent band structure of MoS_2.[81] A clear transition from indirect bandgap to direct bandgap can be observed. Electron-hole recombination process can happen without the participation of phonons for a direct bandgap semiconductor, which is favorable for photo-detecting and light-harvesting application.

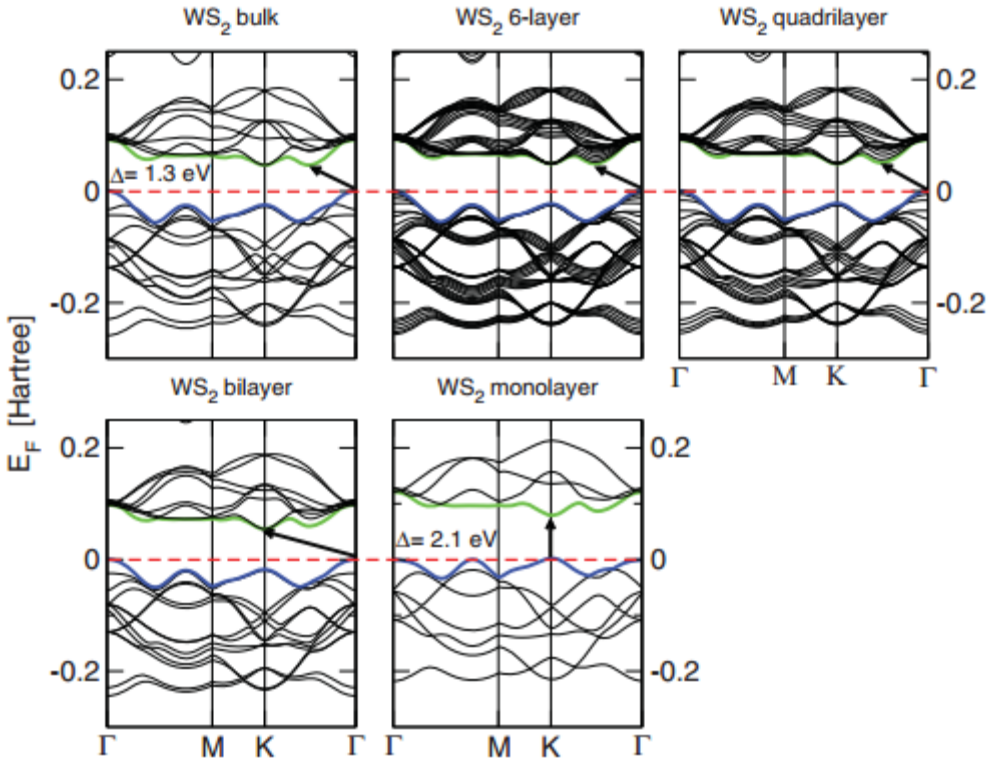


Figure 2.18 Band structures of bulk, multilayer and monolayer WS_2 calculated by DFT. The horizontal dashed line indicates the Fermi level and the arrow indicate the fundamental band gap for a given system. The top of the valence band (blue/dark gray) and bottom of the conduction band (green/light gray) are highlighted. Reproduced with permission.[82]

WS_2 share similar electronic properties as MoS_2. The band structures of WS_2 are also layer dependent, shown in **Figure 2.18**. When the thickness decreases, the bandgap becomes larger and it transits from indirect bandgap to direct bandgap.

2.4.3 Boron Nitride

There are several different structures of Boron Nitride, including amorphous form (a-BN), Hexagonal form (h-BN), Cubic form (c-bN) and Wurtzite (w-BN).[83] Among them, the h-BN is the most stable structure. As an analogy of graphene, h-BN also has a honeycomb structure,

formed by B and N atoms alternately with a bond length of 0.145 nm, as shown in **Figure 2.19b**. BN multilayers are also bonded by Van der Waals force, shown in **Figure 2.19a**, with an interlayer spacing of 0.333 nm.

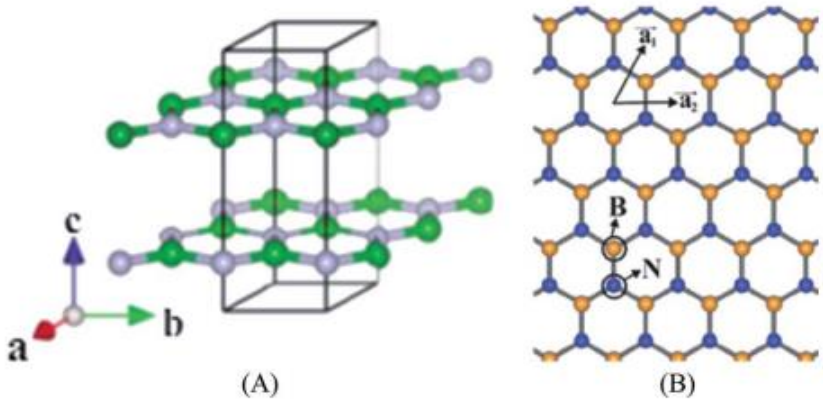


Figure 2.19. Crystal structure of h-Boron Nitride. (a) Schematic of a bilayer h-BN. Green: B atoms; grey: N atoms. (b) 2D structure of a single layer of h-BN. Yellow: B atoms and blue: N atoms. Reproduced with permission.[83]

It has been reported that h-BN is a direct-gap semiconductor with a large bandgap of 5.91 eV and can be seen as an insulator.[84] The interesting property of BN is the vertical conductivity of BN, allowing it to be used as tunneling barriers in electronics. A graphite-BN-graphite vertical device was made by Britnell et al, where BN films of different layer numbers were used.[85]

The measured electron tunneling current through the barrier proves that BN film can be a good tunnel barrier, even when it is only one layer thick, and the tunnel current depends exponentially on the layer number of h-BN, as shown in **Figure 2.20**. This property makes BN a potential candidate as a dielectric layer or substrate in tunnel devices and transistors.[86]

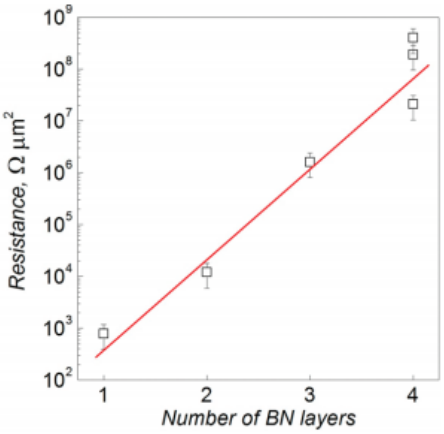


Figure 2.20. Exponential dependence of zero-bias resistance on the thickness of BN separating graphene and gold electrodes (1-4 layers of BN, 0.3-1.3nm). Reproduced with permission.[85]

Note that the graph uses an unconventional unit for impedance. This is because, first, for the tunneling device, the resistance is not linear to the thickness of BN, so it makes more sense to show the thickness-dependent resistance of BN layers, as shown in **Figure 2.20**. Second, for tunneling devices, it is better to compare the contact resistance because the electron tunneling happens at the interface. Because $R = \rho L/A$, where R is the resistance, ρ is the resistivity, L is the length (thickness of BN in this case), and A is the cross-sectional area, we can use $RA = \rho L$ for comparison. To compare the impedance of different devices, it is necessary to multiply the surface area with the measured resistance giving$\Omega\ \mu m^2$ as theunit of the contact impedance.

2.5 Device Applications of 2D Materials

2.5.1 Transistors

Transistors are fundamental devices in integrated circuits designed to accomplish the amplification or switching of electronic signals. Usually, these devices are based on a

semiconductor channel, such as Silicon and GaAs, and at least three terminals are connected to the external circuit. The terminals electrodes in a field-effect transistor (FET) are named as the drain, source, and gate electrodes. The gate between the source and drain is to control the semiconductor channel using field-effect so that the source-drain current can be switched on and off by external gating. By definition, on-current (I_{on}) is the transistor current when gate bias V_g (or V_{GS}) = V_{SD}, also equals to the process supply voltage V_{DD}. A transfer characteristics of a FET is shown in **Figure 2.21**. The off-current (I_{off}) is the current flow under the condition V_G = 0V. The on-off ratio I_{on}/I_{off} is a further parameter for FETs. For a FET to be used in digital logic, on-off ratios between 10^4 – 10^7 are required.[76]

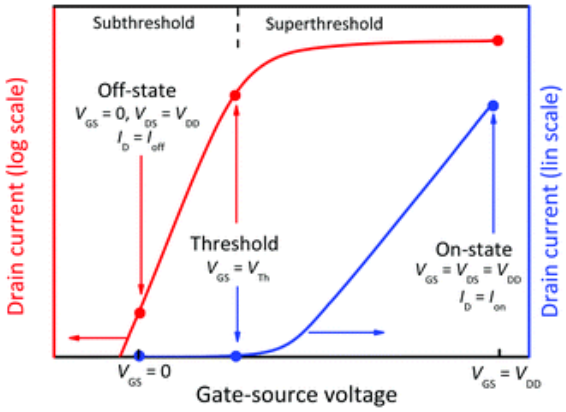


Figure 2.21. Transfer characteristics of a FET showing the drain current as a function of the gate-source voltage V_{GS} with the on and off operating points for logic devices. The scale of the left current axis is logarithmic and the right current axis is linear. Reproduced with permission.[76]

The mobility of a FET can be extracted from the transfer characteristics using the following expression:

$$\mu = \frac{dI_{ds}}{dV_g} \cdot \frac{L}{w} \cdot \frac{1}{V_{sd}} \cdot \frac{1}{C_{ox}}, \quad (2\text{-}6)$$

where L and w are the channel's length and width respectively, and C_{ox} is the oxide capacitance per unit area.[6] A summary of mobility and bandgap of conventional semiconductors and 2D materials is given in **Figure 2.16**. Many 2D transistors have been explored and here I focus on graphene and TMDs transistors as they are relatively thoroughly studied.

2.5.1.1 Graphene FETs

Though graphene is viewed as a possible option for post-silicon electronics, the absence of a substantial bandgap means that graphene field-effect transistors (FETs) cannot switch off effectively. Typically a graphene transistor has an I_{on}/I_{off} ratio of less than 10.

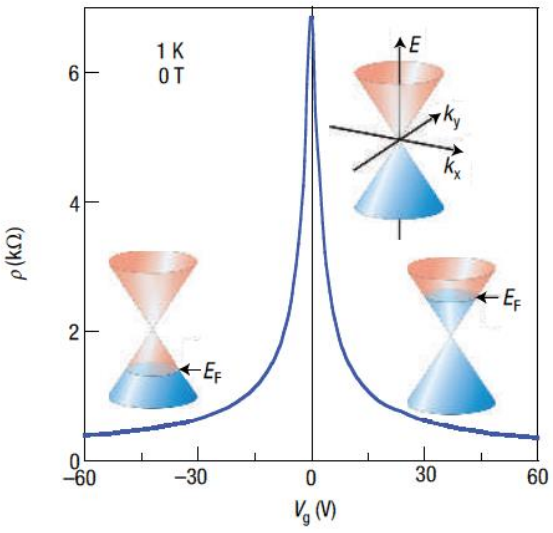


Figure 2.22. Ambipolar electric field effect in single-layer pristine graphene. Left: Fermi level lower than Dirac point; middle: Fermi level at Dirac point; right: Fermi level higher than Dirac point. Reproduced with permission.[22]

Graphene field-effect transistors display an ambipolar property in terms of resistivity as shown in **Figure 2.22**. Applying a positive gate voltage (V_g) could raise the Fermi level, and the conductivity is improved. The type of transport carriers is determined by the electric field

generated by external gating. When the graphene FET is positively biased, the carriers are electrons and if negatively biased, the carriers are holes. However, not all graphene is pristine and if graphene is doped, the Fermi level shifts from the Dirac point and maximum resistance occur when $V_g \neq 0V$. Doping occurs when impurities are introduced into intrinsic semiconductor. Doping is important in electronics as p-n junction are realized by doping two parts of semiconductor channel differently. In general, there are three ways to dope graphene transistors:[87]

1. Hetero-atom doping. This is simply to introduce some atoms, such as B or N as used in Silicon, into graphene transistors. B and N are of similar atomic sizes to C and can substitute in the C lattice. For example, n-doped graphene can be made using an electrothermal reaction with NH_3.[69,88,89] The nitrogen-doped graphene nanoribbon FET displays n-type nature and shows an I_{on}/I_{off} ratio over 10^5. Though the high I_{on}/I_{off} ratio is mainly because graphene nanoribbon has a relatively large bandgap, as shown in **Figure 2.15**, the ability to make n-doped graphene is important because graphene is usually p-doped by substrate and environment. The realization of n-type graphene enables researchers to fabricate complicated device structures such as p-n junctions.[88]

2. Chemical modification. As a 2D material only has a single layer of atoms, it is very sensitive to the surface conditions. Thus researchers can dope graphene FET using molecules absorption to control the electronic properties of graphene. For example, it was demonstrated that some nonaromatic or aromatic molecules, such as tetrafluorotetracyanoquinodimethane (F4-TCNQ), can tune the Fermi level of graphene because it can p-dope the graphene FET.[90]

3. Electrostatic field tuning. This is simply using the field effect of graphene to tune the Fermi level. The advantage of using a local or global gating is that the doping process is

controllable and reversible. Graphene p-n junction can be realized by putting a local gate on part of pre-doped graphene channel.[61]

Wafer-scale electronics have also been studied in the aim to realize practical graphene technologies. For example, a graphene integrated circuit was reported which functions as a broadband radio-frequency mixer at frequencies up to 10 gigahertz, by exploiting the high carrier mobility of graphene.[91]

Despite the extensive research on graphene FETs, the challenge of opening a sizeable and controllable bandgap still remains.

2.5.1.2 TMD FETs

As previously mentioned, monolayer TMDs such as MoS_2 and WS_2 are semiconductors with a direct bandgap. They are naturally favorable for making high I_{on}/I_{off} ratio field-effect transistors. The first single-layer MoS_2 transistor was reported in 2011 and the FET showed an I_{on}/I_{off} over 10^8 over a gate voltage range of -4V to 4V, shown in **Figure 2.23**.[92]

They used a layer of HfO_2 as a local gate to control the charge density and the thickness of the conductive MoS_2 channel is only 0.65 nm. A mobility of 200 $cm^2V^{-1}s^{-1}$ was realized, which is comparable to that in the thin silicon film.[76,93] Though most reported MoS_2 FET used exfoliated materials,[92,94,95] CVD-grown MoS_2 FETs have also been reported.[93] Just like graphene, integrated circuits based on MoS_2 transistors have also been studied.[96] A series of circuits containing 2-12 transistors all integrated on a single sheet of bilayer MoS_2 were fabricated and measured. The tested devices include an inverter, a NAND gate, a static random access memory, and an oscillator.

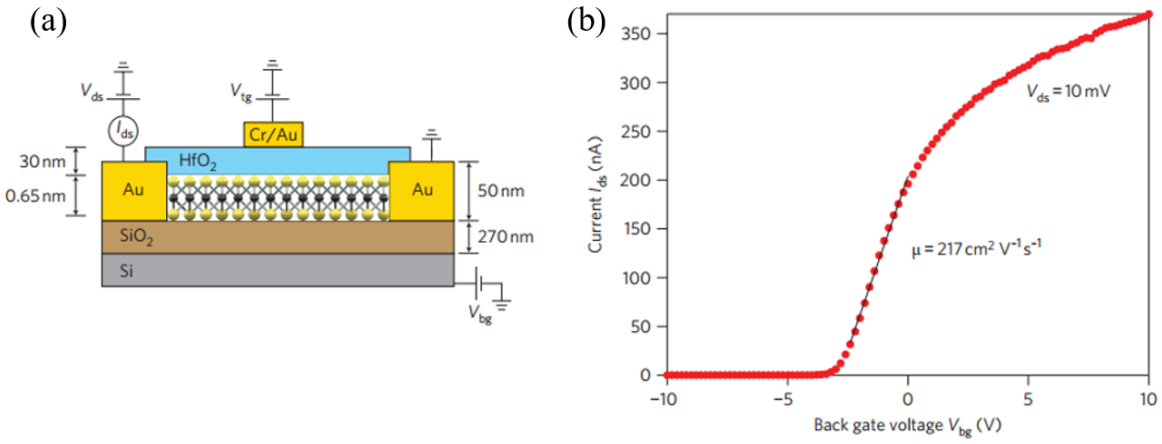


Figure 2.23 Property of MoS_2 monolayer transistors. (a) A cross-sectional view of the structure of a monolayer MoS_2 FET. (b) Transfer characteristics of the FET under a bias voltage V_{ds} = 10 mV at room temperature. Reproduced with permission.[92]

Similar to MoS_2, WS_2 transistors have also been studied and show good performance. An I_{on}/I_{off} ratio over 10^5 was realized in FET made from synthesized multilayer WS_2, at room temperature.[97] For single-layer WS_2 FET transistors, an on-off ratio about 10^5 has been achieved with a mobility as high as 140 $cm^2V^{-1}s^{-1}$ at low temperatures 83K (300 $cm^2V^{-1}s^{-1}$ for bilayer WS_2). Doping levels are found to be related to the chemical environment of the WS_2 channel, which can be improved by annealing in a vacuum chamber.[98] It was also found that monolayer and bilayer WS_2 transistors show different properties, such as conductivity and photoluminescence, due to their different band structures.[99]

The issue with TMDs is the contact resistance with metal electrodes. Schottky barriers form between the interface of semiconductor and metal. The Schottky barrier heights can be extracted from the output characteristics of the FETs, using a metal-semiconductor-metal model developed by my senior colleague Dr. Ye Fan.[100] Details of the model are given in Chapter 3 Methodology.

2.5.2 Photodetectors

Phtotodetecting devices based on graphene and other 2D materials have been studied intensively as their 2D nature is an advantage of making flexible devices. Before digging into the research on 2D photodetectors, the important figures of merit to characterize a photodetector including photocurrent, photoresponsivity (R), external photoconductive gain (G_{ext}), internal photoconductive gain (G_{int}), and specific detectivity (D^*) are briefly discussed here.

The photocurrent is the electric current through a photosensitive device, which equals the difference of the measured current under illumination and the dark current:

$$I_{photo} = I_{illuminated} - I_{dark}, \tag{2-7}$$

where $I_{illuminated}$ is the current under illumination and I_{dark} is the dark current.[101]

Photoresponsivity is a measure of the device's electrical response to incident light:

$$R = \frac{I_{\text{photo}}}{P_{\text{light}}}, \tag{2-8}$$

Where I_{photo} is the generated photocurrent and P_{light} the incident light power.[101]

External photoconductive gain (G_{ext}) is the number of photo-excited charge carriers that are collected at the electrodes for each unit of incident photons on the photoconductor. External photoconductive gain is related to photoresponsivity through the following formula:

$$R = G_{\text{ext}} \cdot e/h\upsilon, \tag{2-9}$$

where G_{ext} is the external photogain, e is the elementary charge unit, h is the Planck's constant and υ is the incident photon frequency.[101] As not all photons are absorbed by the material, the internal photoconductive gain (G_{int}) can be defined using

$$G_{\text{int}} = {G_{\text{ext}}}/{QE}, \tag{2-10}$$

where QE is the quantum efficiency and equals light absorbance for photoconductors.[101] The light absorbance rate of 2D materials for light of certain frequency can be obtained from the literature. For example, the light absorption rate and transmittance rate of MoS_2 under 532nm light (2.33 eV) are 10% and 90%.[102]

Specific detectivity (D^*) is also an important measure for photodetectors, taking into account the geometry, bandwidth and noise of the device. It is calculated as:

$$D^* = \frac{R \times (Af)^{1/2}}{i_{\text{n}}}, \tag{2-11}$$

where A is the effective area of the detector, f is the bandwidth, and i_{n} the noise current.[101] The bandwidth is the difference between the upper and lower frequencies in a continuous band of frequencies. The bandwidth of 2D TMDs is typically within 0.1Hz to 10kHz.[103] But for a simple estimation, the dark current is assumed to be dominated by short noise and is independent of frequency. Then D^* can be expressed as:

$$D^* = RA^{1/2}/(2eI_{\text{dark}})^{1/2}, \tag{2-12}$$

where R is the photoresponsivity of the device and I_{dark} is the dark current.[101]

	Active layer	Spectral range	Responsivity [AW^{-1}]	Response times [ms]	Detectivity [Jones]
	Mechanically exfoliated 1L	Visible	7.5×10^{-3}	50	–
	Mechanically exfoliated 1L	Visible	880	600	–
	Mechanically exfoliated ML	UV-visible-NIR	0.12	–	$\approx 10^{11}$
	CVD-grown 1L (in vacuum)	Visible	2.2×10^{3}	2.2×10^{5}	–
	CVD-grown 1L	Visible	1.1×10^{-3}	$>10^{3}$	–
	CVD-grown FL	Visible	0.57	7×10^{-2}	$\approx 10^{10}$
	Liquid exfoliated FL	UV-visible-NIR	3.6×10^{-5}	60	–
MoS_2	Magnetron sputtered 5L	Visible-NIR	1.8	–	5×10^{8}
	Solution-synthesized 2–4L	UV-visible	6.3×10^{-5}	20	4.2×10^{8}
	Self-limiting grown FL (after laser micromachining)	Visible	0.55	0.2	–
	Mechanically exfoliated ML (local bottom gated)	Visible	342.6	$>10^{3}$	–
	Mechanically exfoliated 1–2L (HfO_2 encapsulation)	Visible	10^{4}	10	7.7×10^{11}
	Mechanically exfoliated FL (enhanced by ferroelectrics)	Visible-NIR	2570	1.8	2.2×10^{12}
	Mechanically exfoliated 10L (MESFET structure)	Visible	5000	2	–
	APTES doped FL	Visible	5.75×10^{3}	–	4.47×10^{9}
	Mechanically exfoliated FL	Visible	97.1	15	–
$MoSe_2$	CVD-grown 1L	Visible	2.15×10^{-4}	25	–
	CVD-grown 1L	Visible	1.3×10^{-2}	60	–
	CVD-grown ML	Visible	93.7	400	–
	CVD-grown FL	Visible	9.2×10^{-5}	5.3	–
	Mechanically exfoliated ML (in NH_3 atmosphere)	Visible	884	$>10^{3}$	–
WS_2	CVD-grown 1L (in vacuum)	Visible	1.88×10^{-2}	$<10^{3}$	–
	PLD-grown ML (in vacuum)	UV-visible-NIR	0.70	9.9×10^{3}	2.7×10^{9}
	Magnetron Sputtered ML	UV-visible	53.3	–	1.22×10^{11}
	OTS-doped FL	Visible	1.45×10^{4}	–	5.3×10^{10}
	CVD-grown 1L	Visible-NIR	1.8×10^{5}	$>5 \times 10^{3}$	$>10^{14}$
WSe_2	Mechanically exfoliated 3L	Visible	7	1×10^{-2}	–
	CVD-grown 1L	Visible	1.1	$>10^{3}$	–
	PPh_3-doped FL on hBN	Visible	1.27×10^{6}	2.8	–
$MoTe_2$	Mechanically exfoliated FL	Visible	2560	–	–
HfS_2	Mechanically exfoliated FL	Visible	890	38	1.3×10^{10}

Table 2.1 Performance of photoconductors based on 2D TMDs. ML: Multilayer, CVD: Chemical vapor deposition, FL: Few-layer. Reproduced with permission.[104]

Performance of photodetectors based on common 2D materials, including MoS_2, $MoSe_2$, WS_2, WSe_2, $MoTe_2$, HfS_2, is shown in **Table 2.1**. The characterized properties include spectral range, responsivity, response times and detectivity. It is worth noting that even for the same materials, the performance could be significantly impacted by the production method, quality of the materials, substrate, device structure, and other parameters.

The on-off ratio (I_{on}/I_{off}) of photodetectors is similar to I_{on}/I_{off} of FETs, defined as the ratio of the current under illumination (on-current) of certain power versus the dark current (off-current).[101] The value of the on-off ratio can be obtained by the transient photocurrent characteristics of the device, such as **Figure 2.26e**

In general, there are two advantages of graphene-based photodetectors:[105] Graphene absorbs lights of a broad wavelength, from ultraviolet to terahertz frequencies.[106-109] Also, the response time is governed by the carrier mobility so the detecting process of graphene photodetector can be ultrafast. The graphene-based photodetector has a similar device structure as FETs and response at wavelengths of 0.514, 0.633, 1.5 and 2.4 um have been reported.[110] The main shortcoming is that the photoresponsivity of graphene-based photodetector is usually limited, owing to its low absorption coefficient.

Other 2D materials photodetectors have also been studied, including TMDs,[111] GaS,[112] black phosphorus,[113] and InSe.[114] The superiority of using these materials is higher absorption rate (due to the large density of states) and the possibility of local gating. A typical photodetector based on those materials is metal-semiconductor-metal types, as shown in **Figure 2.24**. Using MoS_2 for example, one can achieve a maximum external photoresponsivity of 880 AW^{-1} at a wavelength of 561 nm. The presence of a bandgap allows the photodetector to be turned off, resulting in low dark current.[115]

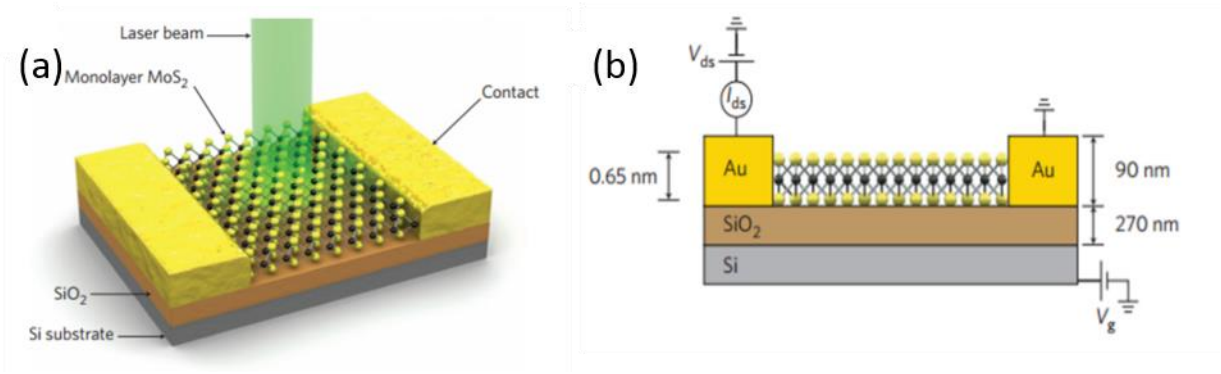


Figure 2.24. The structure of the metal-MoS_2-metal semiconductor photodetector. (a) Three-dimensional schematic view of a monolayer MoS_2 photodetector. (b) A cross-sectional view of the device. Reproduced with permission.[115]

2.5.3 Devices Based on 2D Heterostructures

By putting 2D materials together, it is possible to make more complicated devices with improved performance. A variety of devices have been studied including transistors, memory devices, optoelectronic devices, photovoltaics, capacitors, and sensors.[116] This section will briefly review some of these applications.

2.5.3.1 Transistors.

Different from the field-effect transistors mentioned above, Britnell et al. reported a field-effect tunneling transistor in 2012.[117] The transistor consists of an ultrathin layer of h-BN or MoS_2 layer, sandwiched by vertically stacked graphene layers, as shown in **Figure 2.25a**. The h-BN or MoS_2 layer acts as a tunneling barrier, and the effective height is tunable by external gating. Bipolar characteristics were obtained from the devices, as shown in **Figure 2.25c**, with an I_{on}/I_{off} ratio of about 50 and 1×10^4 for h-BN and MoS_2 respectively. Further improvements were

achieved by replacing the tunneling barrier with WS_2, after which a current modulation over 10^6 was achieved at room temperature.[118,119]

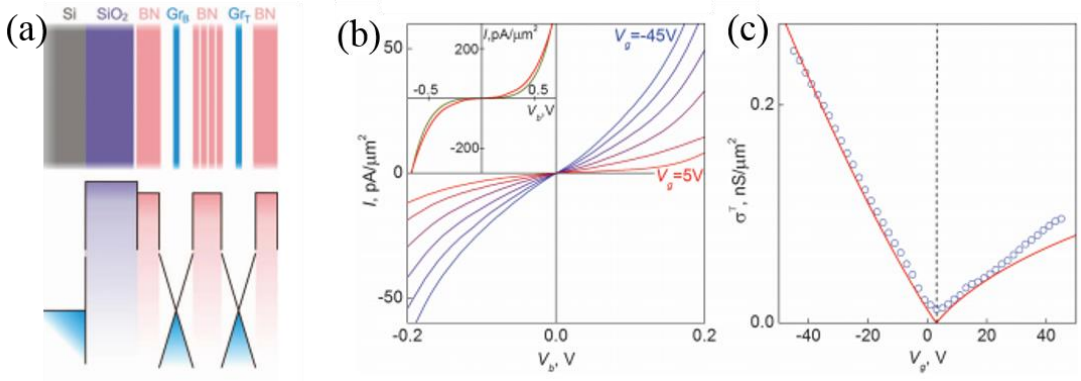


Figure 2.25. Structure and properties of graphene-BN tunneling transistors. (a) Schematic of the tunneling structure: cross-sectional view. (b) I_{ds}-V_{ds} curve of the devices under different gate voltages. (c) Transport curve of the devices. Reproduced with permission.[117]

2.5.3.2 Photodetectors.

2D heterostructures can also be used in photodetectors for enhanced performance. A study in our group showed that vertically stacked WS_2/MoS_2 semiconducting heterobilayers, shown in **Figure 2.26a**, **2.26b**, and **2.26c**, display a very high photoresponsivity up to 10^3 AW^{-1} under an illumination power density of 1.7×10^2 $mWcm^{-2}$, as shown in **Figure 2.26d**.[120] A large photoconductive gain of 3×10^4 can be achieved due to efficient charge transfer at the WS_2/MoS_2 heterointerface and long trapping time of photogenerated charges. The disadvantage of the photodetector is that the on-off ratio is within 10, as shown in **Figure 2.26e**.

Another type of photodetector is based on graphene-semiconductor heterojunction. A Schottky barrier forms at the graphene-semiconductor interface, thus the output characteristics of

the devices show rectifying behavior. The device operates under revise bias with a low dark current.[121]

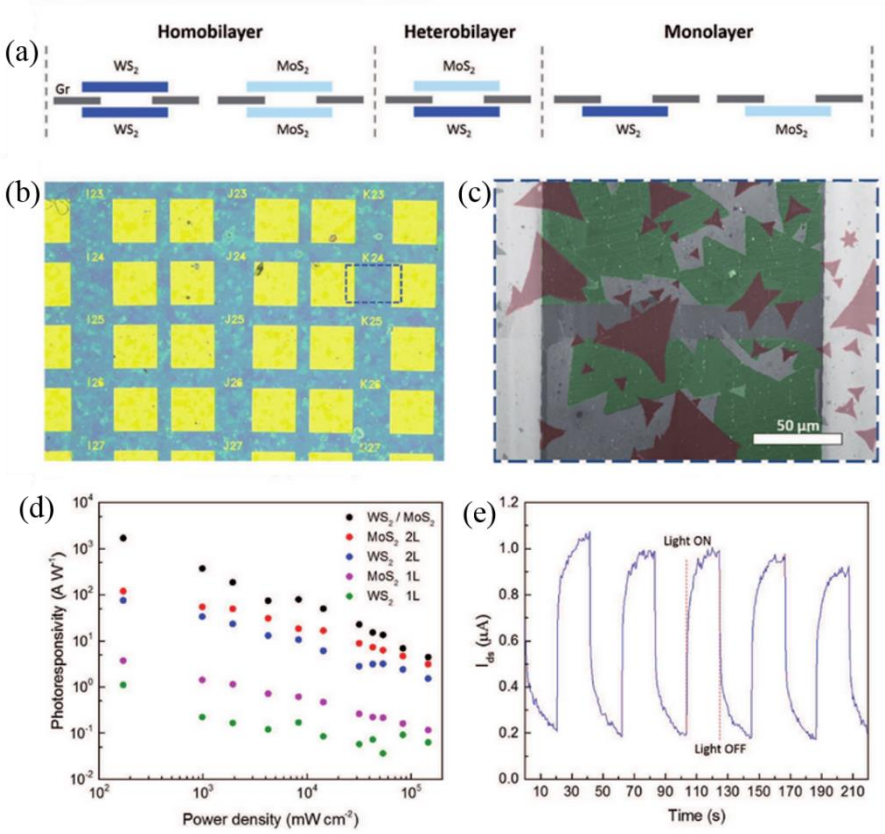


Figure 2.26. Structure and properties of the MoS_2/WS_2 heterobilayer photodetector. (a) Schematic of 5 types of structure. (b) Optical image of the heterobilayer device array. (c) False-color SEM image showing the framed region in (d) Red: MoS_2 and Green: WS_2 domains. (e). Photoresponsivity versus irradiation power. (f). Transient photocurrent characteristics of the device under V_{ds} = 1 V, V_g = −30 V under a power density of 1.7×10^2 mW cm^{-2}. Reproduced with permission.[120]

2.5.3.3 Light-emitting diodes

Light-emitting diodes (LEDs) can also be made using 2D heterostructures. Wither et al reported in 2015 that by stacking metallic graphene, insulating hexagonal boron nitride and various semiconducting monolayers vertically, as shown in **Figure 2.27a** and **2.27b**, an extrinsic

quantum efficiency of nearly 10% can be achieved and the frequency of the emission can be tuned over a broad range using different 2D semiconductors.[122] The heterojunction of the device is shown in **Figure 2.27c** and the electroluminescence of the junction is shown in **Figure 2.27d**. The increase of the quantum efficiency of the structures can be done by placing several layers of TMDs in series. So far, MoS_2, WS_2, and WSe_2 have been used in this type of LEDs and show great performance.[122,123]

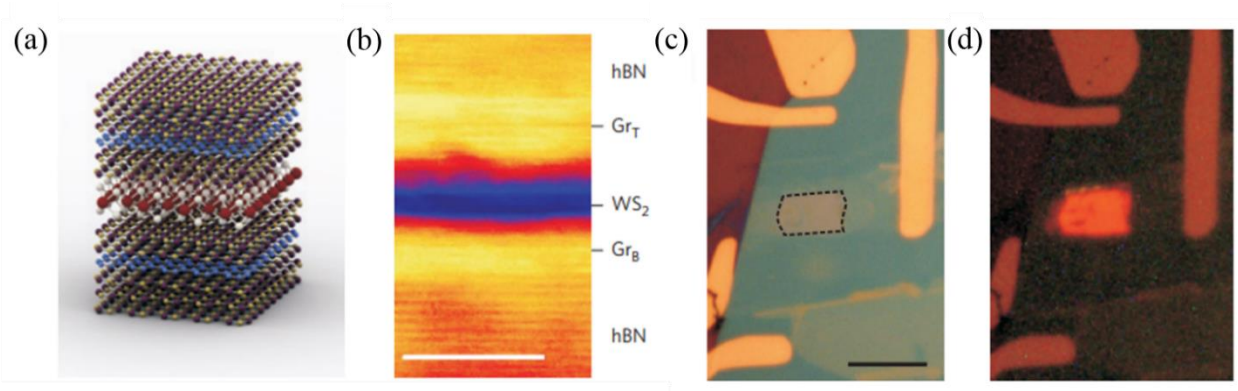


Figure 2.27. Light-emitting diodes based on 2D heterostructures. (a) Schematic of the hBN/Gr_B/2hBN/WS_2/2hBN/Gr_T/hBN. (b) Cross-sectional bright-field STEM image of the type of the heterostructure. (c) Optical image of an operational device. (d) Optical image of electroluminescence (EL) from the same device. Reproduced with permissions.[122]

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Chapter 3 Research Methodology

3.1 Introduction

The objective of this thesis is to explore the electronic and optoelectronic properties of 2D heterostructures. To realize this goal, many techniques have been used to obtain 2D materials and evaluate their properties. In this chapter, I will go through all the techniques used throughout the research. Topics covered are growth and transfer of materials, device fabrication, as well as characterization and data analysis.

3.2 Synthesis of Materials and Transfer Techniques

All the 2D materials studied in this research were synthesized using chemical vapor deposition. This technique allows researchers to obtain 2D materials of large scale and it is compatible with conventional semiconductor processing. The synthesized graphene can be as large as 9cm × 9cm. Small pieces of graphene can be cut off from the large one simply using a pair of scissors, as shown in **Figure 3.1b**. The synthesized WS_2 and MoS_2 are randomly distributed domains of various sizes. The synthesis details are given below.

3.2.1 CVD Growth of Graphene

Wafer-sized monolayer graphene was synthesized using the following recipe:[1]

1. A piece of copper (Cu) foil was cleaned using acetone and IPA, then put on a ceramic boat (support) and inserted into the furnace. The copper foil functions as both a catalyst and substrate for the deposition.

2. The growth was conducted with a flow of 500 standard cubic centimeters per minute (sccm) argon, 100 sccm argon (25% hydrogen), and 10 sccm argon (1% Methane) for 10 mins at 1060 °C. The detailed process is shown in **Figure 3.1d**.
3. The furnace was moved away to facilitate fast cooling for better graphene quality.

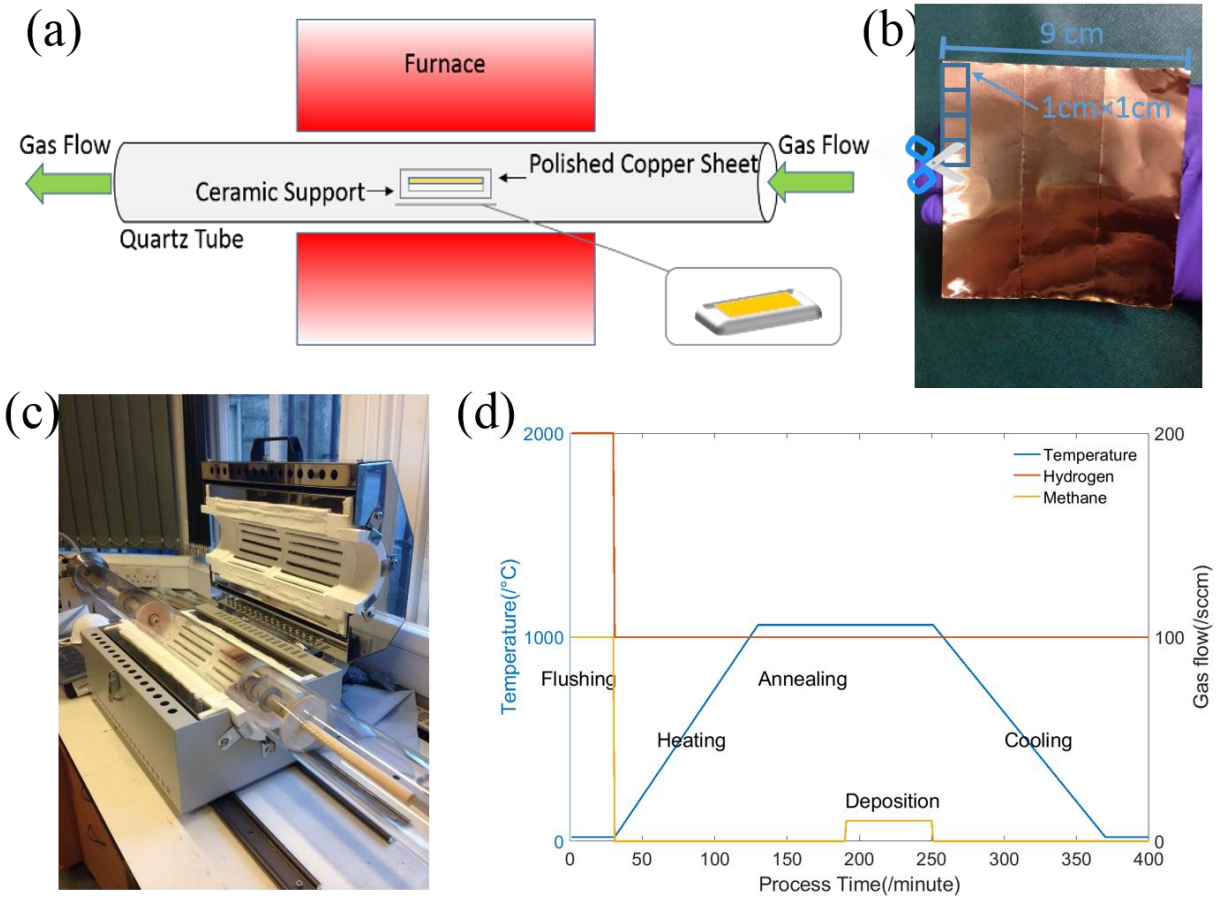


Figure 3.1. CVD synthesis of graphene. (a) Schematic figure of the setting for chemical vapor deposition of graphene. (b) A photo of a piece of cleaned copper foil, 9cm × 9cm. (c) A photo of the CVD furnace. (d) Detailed recipe of the synthesis process.

The annealing process is to enable the growth of copper domains. During high-temperature annealing, copper domain size increases and the domain size of graphene synthesized on copper domain will also increase, leading to better graphene quality. The growth of graphene takes place

on both sides of copper foil so that graphene at the back side needs to be removed by reactive ion etching or plasma etching before wet transfer. Polishing the copper foil before acetone cleaning is found to improve the uniformity of graphene film but will also leave white particles on the copper surface under SEM thus it is not recommended to do so.

It is found that the layer number of synthesized graphene is positively related to the amount of methane used and the deposition time. I optimized the recipe for monolayer graphene synthesis by gradually reducing the synthesis time and methane flow until discontinuous graphene was obtained. Then the methane flow and reaction time were slightly increased to obtain single-layer graphene. This was my first-year project and the results were presented in my first-year viva. The graphene I used in my devices were grown by my colleague Dr. Yuewen Sheng because after the recipe development, I focused on device fabrication and characterization. He also improved the uniformity of graphene by using a plate ceramic support instead of a boat support in step 1.

3.2.2 CVD Growth of WS_2 and MoS_2

WS_2 domains (mainly monolayer but also bilayer and multilayer regions) were grown on 300 nm SiO_2/Si substrates using a double-walled quartz tube using the following method:[2]

1. The two precursors, sulfur powder, and WO_3 were placed separately in a double-walled quartz tube. Sulfur (200 mg, Sigma-Aldrich) and WO_3 powder (100 mg, Sigma-Aldrich) were loaded in the external and internal tube, respectively.
2. S and WO_3 were then heated and vaporized by two independent furnace systems shown in **Figure3.2**, at 180 °C (right furnace) and 1150 °C (left furnace) respectively. WS_2 domains were then deposited onto SiO_2/Si substrate, at the end of the internal tube. The as-grown WS_2 samples were fast cooled once the reaction (3 minutes) is completed.

Monolayer MoS_2 domains were synthesized using similar methods to WS_2, as previously reported:[3]

1. Two precursors, molybdenum trioxide (MoO_3) and sulfur (S, >= 99.5%; Sigma-Aldrich) powders, were placed in a double-walled quartz tube at different positions.
2. Sulfur and MoO_3 were then heated and vaporized by two independent furnaces at 180 °C and 300 °C respectively. The reaction takes place on 300 nm SiO_2/Si substrates under atmospheric pressure for 30 minutes after which the furnaces were quickly cooled down.

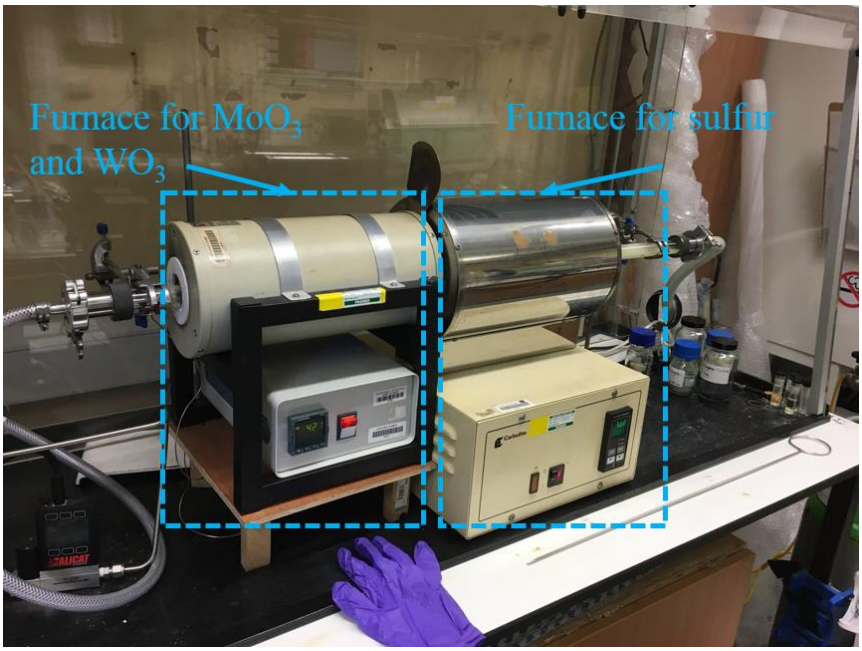


Figure 3.2. CVD settings for TMDs synthesis with two furnaces. MoO_3 (WO_3) and sulfur are put into two different tubes and heated at different furnaces.

The WS_2 and MoS_2 recipe was developed by my colleague Dr. Youming Rong and Dr. Shanshan Wang respectively. The WS_2 samples used in my research are provided by my colleagues Dr. Yuewen Sheng, Dr. Yingqiu Zhou, Miss Linlin Hou, and Miss Qianyang Zhang. It was found that monolayer WS_2 and MoS_2 are very sensitive to light and they may decompose

within a few weeks. Therefore the sample box was wrapped with tin foil and stored in dark conditions.

3.2.3 Water-based Wet Transfer

The morphology of the as-grown graphene film on copper foil was observed using a scanning electron microscope, but further characterization of the optical and electrical properties requires the transfer of the graphene film onto a silicon wafer:

1. The as-grown graphene film was spin-coated with a poly (methyl methacrylate) (PMMA) scaffold (8 wt% in anisole, 495k molecular weight) at 4500 rpm for 60s and baked at 180°C for 90s.
2. The graphene on the back side of the copper was removed using reactive ion etching to avoid difficulties, sabotaging the quality of transferred graphene film.
3. PMMA/graphene/copper sample was then put in ammonium persulfate solution (0.2 mol/L) for 3 hours to detach the copper substrate, shown in **Figure 3.3a** and **3.3b**. Then the floating PMMA/graphene film was carefully scooped up with a glass slide and transferred 3 times into deionized water to clean the film, shown in **Figure 3.3c** and **3.3d**.
4. The films were transferred onto SiO_2/Si chip and left in ambient environment overnight, shown in **Figure 3.3e**. Then the samples were baked at 180°C for 15 min. PMMA film was dissolved in hot acetone at 45°C for 3 hours, leaving graphene onto the chip.

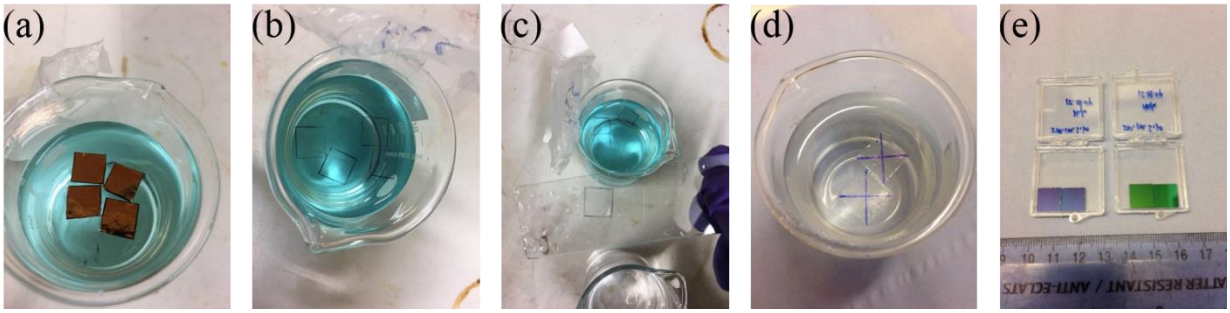


Figure 3.3. Wet transfer of graphene using ammonium persulfate. (a) PMMA/graphene/copper (back side cleaned) film on ammonium persulfate solution. (b) PMMA/graphene film with copper etched off. (c) Transfer the film into clean DI water using a glass slide. (d) PMMA/graphene film in DI water to clean the residue and other contamination. (e) Transfer the film onto the target substrate. Left: on SiO_2/Si, and right: on Si_3N_4/Si.

For MoS_2 and WS_2 samples it is possible to examine the electronic properties of as-grown films, but due to the high temperature during the synthesis, the underlying SiO_2 is likely to be damaged. Electrical measurements conducted on such substrates were found to have large gate current leakage. Therefore it is necessary to transfer MoS_2 and WS_2 domains onto new substrates using the following transfer method:

1. The TMD samples were spin-coated with a poly(methyl methacrylate) (PMMA) scaffold (8 wt% in anisole, 495k molecular weight) at 4500 rpm for 60s and baked at 180°C for 90s.
2. The top 4 edges of the film were carefully scratched off to expose the SiO_2 layer, which was covered by PMMA during spin-coating, shown in **Figure 3.4a** and **Figure3.4b**.
3. The PMMA/MoS_2/SiO_2/Si sample was put in KOH solution (1 mol/L) for 2 hours to dissolve SiO_2 and detach Si substrate, shown in **Figure 3.4c**.
4. The cleaning and transfer process is the same as for graphene transfer.

Using a Petri dish, instead of a beaker, for substrate etching is found to greatly improve the success rate. Because the etching of SiO_2 does not happen at the same pace, quite often the first detached Si part may sink and drag the whole film down to the bottom of the beaker. So using a Petri dish is preferable as Si substrate is supported by the bottom.

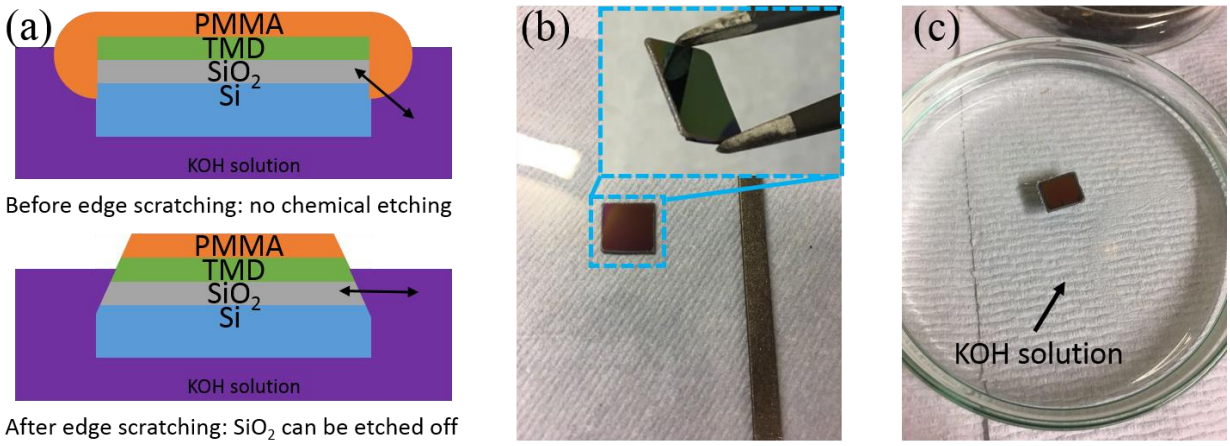


Figure 3.4. Wet transfer of TMDs using KOH. (a)Schematic figures of sample edge scratching and KOH etching. (b) PMMA/TMD/SiO_2/Si substrate with scratched edges. (c) The sample was etched using KOH solution in a petri dish.

3.2.4 IPA-based Wet Transfer

IPA transfer is also a solution-based transfer but it is an improvement on water transfer. This method is developed by my colleague Dr. Yuewen Sheng.[4] Two advantages of IPA transfer are:

1. 2D materials transferred using IPA display better quality.
2. For chips with pre-transferred TMDs, water transfer damages or even washes off the TMDs domains on the chip, making it very difficult to make vertical structures.

The detailed process of IPA transfer is:

1. The Copper or SiO_2 substrate were etched off following the same steps above.
2. PMMA/Graphene or PMMA/TMD film was lifted using a very thin glass/quartz slide, similar to **Figure 3.3c**.
3. The edge of the slide was put on the target substrate, as shown in **Figure 3.5**. IPA was dropped on the film so that the film slide slowly from glass/quartz to the target film
4. The film was carefully tilted and dragged to ideal position using a pair of tweezers.
5. The sample was left in an ambient environment overnight to dry out the water and IPA. The sample is then baked at 180°C for 15 mins, after which put into hot acetone at 45°C for 3 hours to remove PMMA film.

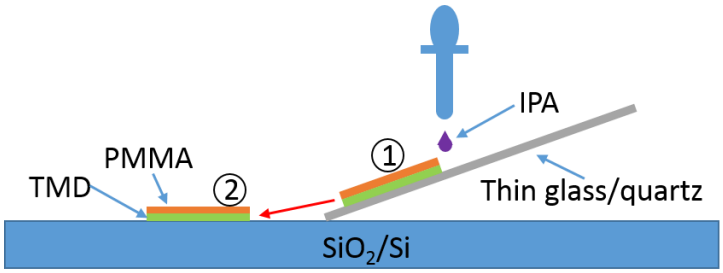


Figure 3.5. Schematic figure of IPA transfer of TMDs. The transfer is essential an IPA-supported sliding of PMMA/TMD film from a thin glass (position 1) to the target substrate (position 2).

3.3 Device Fabrication

Though it is possible to quickly test the electrical properties by putting two probes directly onto 2D materials, the disadvantages are obvious:

1. The results are inaccurate due to contact resistance between the probe and 2D materials.
2. The results are impossible to quantify as the tested 2D materials are not of regular shapes, lengths, and widths.

Therefore standard device fabrication techniques have been used to study the properties of 2D materials and their heterostructures, including pattern design, electron-beam lithography, metal evaporation, and plasma etching.

3.3.1 Device Pattern Design

The pattern design is to customize the shape of metal bond pads and 2D materials. Using AutoCAD 2015, the array of bond pads and graphene ribbons are drawn with different colors. Alignment marks with crossbar shapes, known as P marks and Q marks are also drawn to facilitate position alignment if necessary, as shown in **Figure 3.6a**. Typically there are 34 × 15 = 510 devices on a substrate of 1cm × 1cm. **Figure 3.6b** shows detailed of the features of the devices. Each devices have two bond pads of 150 μm ×150 μm. The specific designs of the devices are given in chapter 4 and chapter 5.

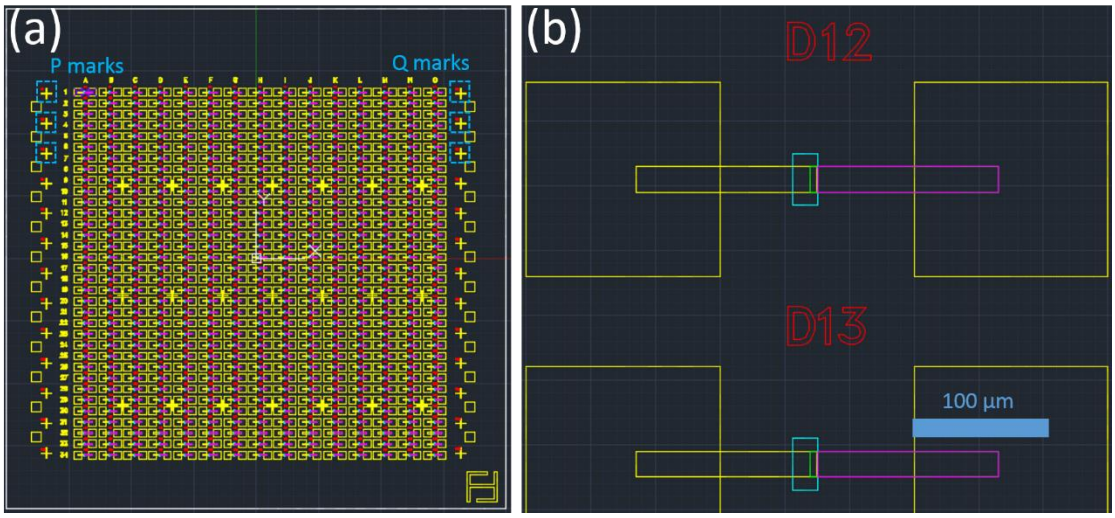


Figure 3.6. AutoCAD design of the device. (a) Device array and registration mark of the AutoCAD design. (b) The detailed feature of the device design. Red: device label; yellow: Cr/Au; purple: graphene. Light blue and green: gap making.

3.3.2 Electron-Beam Lithography

The idea of electron-beam technique (EBL) is to irradiate a focused beam of electrons onto a specific region covered with electron sensitive resist. The molecular structure of the resist exposed to electron beam will be changed so that its solubility in certain solutions will be changed as well.



Figure 3.7. Electron-beam lithography system used to pattern electron-beam resist. Resolution of about 200 nm can be achieved using PMMA as a positive resist and resolution of about 1 μm can be achieved using maN-2403 as a negative resist.

There are two types of photoresist: positive and negative resist. For a positive resist, the area irradiated by electron beam will be removed by the developer while for a negative resist, the area exposed to electron beam will be left on the substrate. To make metal bond pads, PMMA as positive resist has been used:

1. PMMA (A4 495k) resist was spin-coated onto SiO_2 (300nm)/Si chips, at 4500rpm for 60s.
2. The sample was baked on a hotplate at 180°C for 90 seconds.

3. PMMA (A8 950k) resist was spin-coated onto SiO_2 (300nm)/Si chips, at 4500rpm for 60s.
4. The sample was baked on a hotplate at 180°C for 90 seconds.
5. The sample was exposed at a dose of 600 $\mu C/cm^2$ using the imported AutoCAD design.
6. The sample was developed in MIBK/IPA (1:3) solution for 45 seconds, at room temperature.
7. The sample was rinsed in IPA for 30 seconds.

This bilayer PMMA method is to achieve a higher spatial accuracy of deposited bond pads.

To pattern graphene into the desired features, maN-2403 was used as a negative resist using the following recipe:

1. PMMA (A4 495k) resist was spin-coated onto graphene/substrate, at 4500rpm for 60s.
2. The sample was baked on a hotplate at 180°C for 90 seconds.
3. maN-2403 was spin-coated onto the chip for 30 seconds at 3000 rpm.
4. The sample was baked on a hotplate at 90°C for 60 seconds.
5. The sample was exposed at a dose of 120 $\mu C/cm^2$.
6. The sample was then developed in ma-D525 for 60 seconds, at room temperature.
7. The sample was rinsed in DI water for 30 seconds.

In principle, researchers can just use maN-2403 without the PMMA underneath, but it is found that maN-2403 may stick to the graphene. Using PMMA in between as a spacer helps remove the negative resist.

3.3.3 Metal Evaporation

Bond pads of Cr (10nm)/Au(80nm) were deposited using thermal evaporation. Cr is used to enhance the bonding between gold and SiO_2 substrate. The thickness of bond pads should be thin in principle so that 2D materials transferred onto it is not bent and broken. But if the P and Q mark are too thin, I found some problems during mark alignment as the signal might be too weak to detect.



Figure 3.8. Thermal evaporation system used to make bond pads. Three types of metal can be evaporated Cr, Al, and Au. Evaporation rate about 0.1-0.2 nm/s is used to secure the quality of the bond pads.

3.3.4 Plasma Etching

After developing the negative resist, the undesired part of graphene is covered by PMMA and the favored part is covered by PMMA/maN-2403. Oxygen plasma was employed to remove PMMA and graphene underneath, with the following conditions: pressure with introduced oxygen: 0.4 mbar, power: 60 W, time: 3 minutes. After etching, the sample is put into acetone at

45°C (water bath) for 3 hours, to remove the maN-2403 above graphene. If the processing is not done properly, maN-2403 ribbons will stick to the graphene.

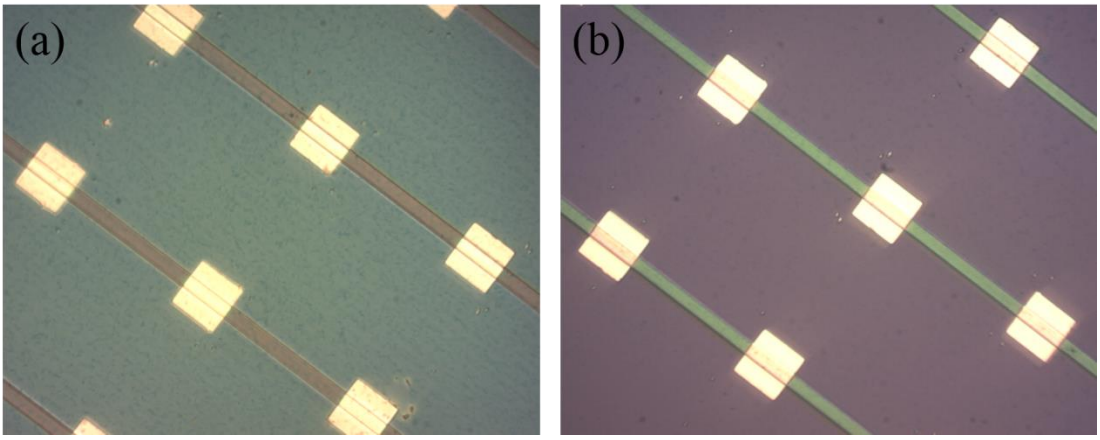


Figure 3.9. The process of plasma etching. (a) Graphene film on Cr/Au film, after developing the maN-2403 resist. Ribbon area is covered by PMMA/maN-2403 and the rest is covered by PMMA only. (b) The sample after plasma etching.

3.4 Characterization

To achieve a high yield rate, inspection is needed after each fabrication step. Commonly used characterization techniques include optical microscopy, scanning electron microscopy, Raman and photoluminescence spectroscopy, as well as electronic and optoelectronic measurements.

3.4.1 Optical Microscopy

A custom-built optical microscope is used to check the morphology of the as-grown materials and devices. For graphene, it is possible to see the uniformity after graphene transferred onto SiO_2, from the contrast with the substrate. But this method is usually used only to confirm the existence of graphene. For a detailed examination, scanning electron microscopy

is needed. The layer number of MoS_2 and WS_2 can also be estimated by comparing the colors of the domains under optical microscopes.

3.4.2 Scanning Electron Microscopy

The device morphology is analyzed using a scanning electron microscope (Hitachi-4300) under an accelerating voltage of 3.0 kV. The best spacial resolution is about 200nm. This characterization can be done either on the copper or SiO_2/Si substrate. The SEM is used to obtain an overall image of the device array and the detailed feature of the devices.

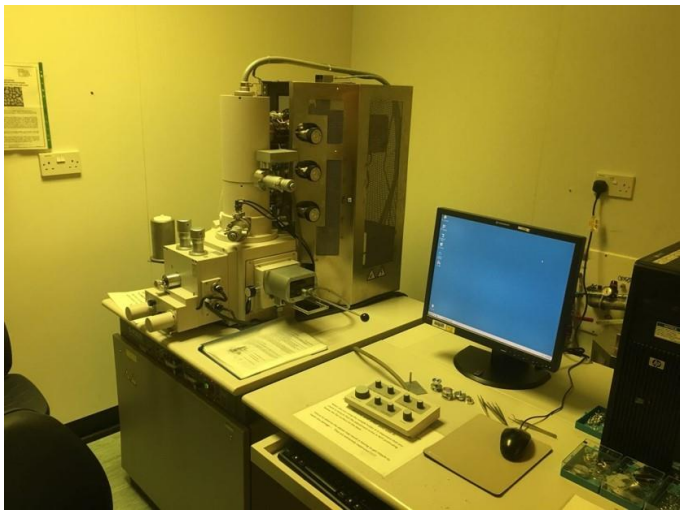


Figure 3.10. SEM facility used to characterize the morphology of the materials and devices.

3.4.3 Raman and Photoluminescence Spectroscopy

Raman spectroscopy was used to determine the layer number of graphene. G band and 2D band can be found in graphene Raman spectrum, as shown in **Figure 3.11**. When the layer number of graphene increases, the relative intensity between the G band (I_G) and the 2D (I_{2D}) band also changes. If $I_{2D}/I_G \geq 2$, then the graphene is monolayer. If $I_{2D}/I_G < 2$, then the graphene is more likely to be multilayer.[5]

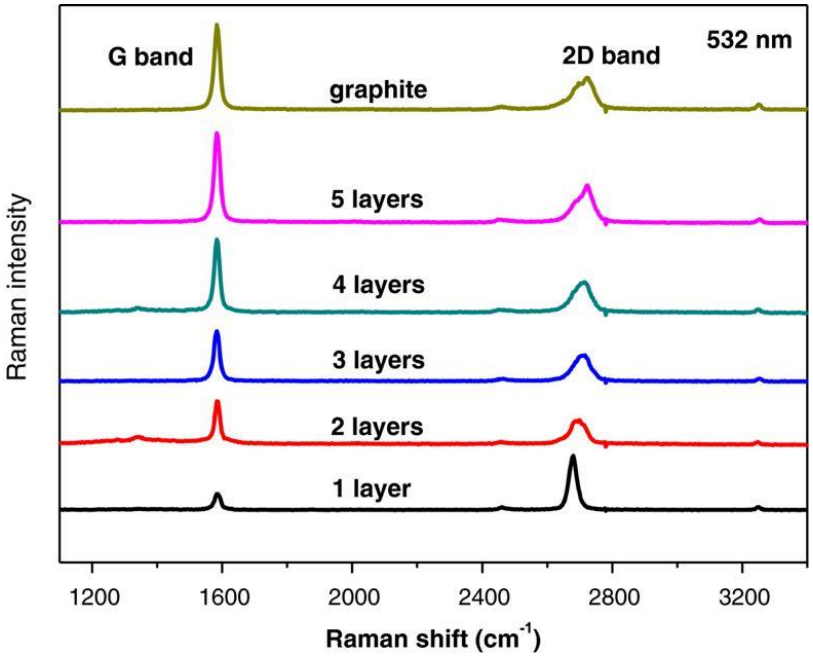


Figure 3.11. Raman spectra of graphene of different layer numbers at 532nm. Reproduced with permission.[5]

The thickness of MoS_2 and WS_2 can also be obtained by Raman spectroscopy. Take MoS_2 as an example, the Raman spectra of MoS_2 of different layer numbers are shown in **Figure 3.12a**. Two modes, E^1_{2g} (or E_{2g}) and A_{1g} can be found near 400 cm^{-1}. The E_{2g} mode is the in-plane vibration of molybdenum and sulfur atoms. The A_{1g} mode is associated with the out-of-plane vibration of sulfur atoms. With the increase of sample thickness, the E_{2g} vibration has a red shift while the A_{1g} vibration has a blue shift. Thus the thickness of MoS_2 samples can be determined correspondingly by the difference between the two peak positions, as shown in Figure **3.12b**.

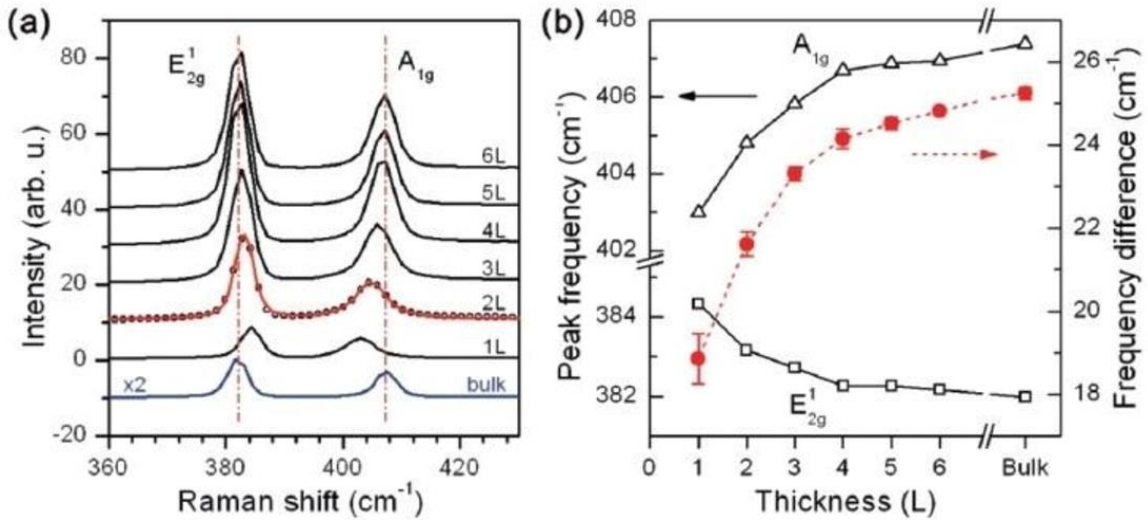


Figure 3.12. Determination of MoS_2 thickness by Raman spectroscopy. (a). Raman spectra of MoS_2 of different thicknesses. (b). Frequencies of A_{1g} and E^1_{2g} and their difference (red, right y-axis) versus layer thickness. Reproduced with permission.[6]

Photoluminescence can be used to examine the quality of 2D materials. **Figure 3.13** shows the photoluminescence of freestanding single-layer MoS_2 and MoS_2 on SiO_2/Si substrate. The photoluminescence is attributed to three peaks, A, A- and B and can be fitted into those peaks using Lorentzian fitting. The A peak and B peak are excitons of different energies while the A- peak is from trions. An exciton is a bound state of an electron and a hole attracted to each other. A trion is a localized excitation, consisting of two electrons and one hole. A peak is at about 1.89eV and A- peak is at about 1.82eV. The B peak is at a higher energy of about 2V. The fitting process is done by indicating the estimated peak position in the Origin 9 software, and the Lorentzian fitting function generates the accurate position and intensity of the three peaks. The fitting is generally good with adjusted $R^2 > 0.99$.

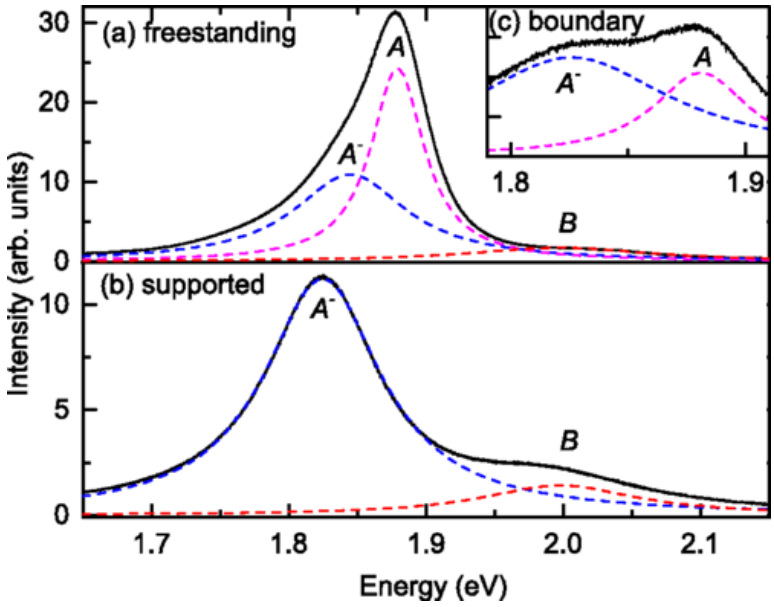


Figure 3.13. Photoluminescence of single-layer MoS_2. (a). Freestanding MoS_2. (b). MoS_2 on Si/SiO2 substrate. (c). From the boundary region between freestanding and supported regions. Dotted lines show fit functions of the A, A-, and B peaks. Reproduced with permission.[7]

For all my experiments, a Labram Aramis Raman Spectrometer was used to carry out Raman and PL spectroscopy for both graphene, MoS_2, and WS_2. My colleague Dr. Yuewen Sheng helped with the characterization of graphene and WS_2 and my colleague Tongxin Chen helped with the characterization of MoS_2.

3.4.4 Electronic and Optoelectronic Properties

To characterize the electronic properties of the devices, the highly conductive Si on the substrate was scratched using a file and then wired and to a socket as a back gate, as shown in **Figure 3.15b**. The silicon wafer is from University Wafer in the US (Item number: 1583, P<100>B doped with resistivity of 0.001-0.005ohm.cm). A Keithley 2400 source meter connected with two tungsten probes was used for measuring output characteristics. The gate was applied by another Keithley 2400 source meter. A 532 nm diode-pumped solid-state laser

(Thorlabs, DJ532-40) was integrated into a confocal microscope to generate a beam with a spot size of ~150 um^2 as a light source for optoelectronic properties. The setup of the probe stations is shown in **Figure 3.14a**.

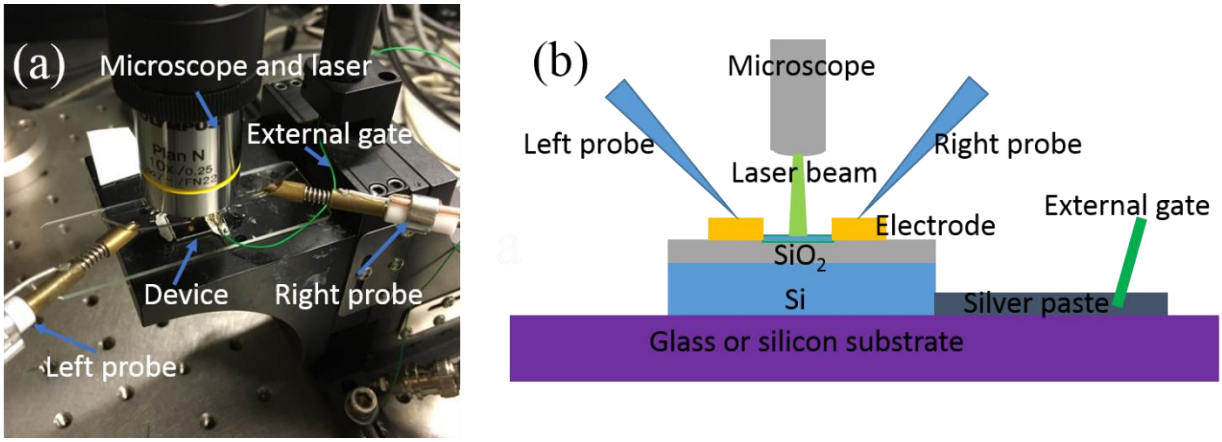


Figure 3.14 Facility settings for electronic and optoelectronic measurements. (a) Photo image of the probe station with my device. Left probe: connects to a source electrode; Right probe: connects to a drain electrode; Green wire: external gating wired with doped Silicon substrate. (b) Schematic figure of the structure. The key is to connect the external gate and conductive silicon with silver paste.

3.4.5 Data Analysis

Optical images and SEM images were processed using ImageJ software to rotate and crop the images into suitable sizes. Schematic figures of devices structure are made using Powerpoint. Atomic models of the devices are drawn by Discovery Studio 2016 and POV-Ray. Peak fitting of PL spectrum is done by Origin Pro9 using Lorentz fitting. Raman, PL spectra, and their intensity

mapping are plotted using Matlab 2015. Figures of electronic and optoelectronic properties are plotted using my own Matlab code for batch processing.



Figure 3.15 Data analysis tools. Image processing: ImageJ; Data fitting and plotting: Origin and Matlab; Configurations drawing: Powerpoint, Discovery Studios, and Pov-ray.

Schottky barrier fitting is done by Matlab scripts developed by my colleague Dr. Ye Fan, which is included in Appendix A. The barrier height of Au-MoS_2 and Gr-MoS_2 are calculated from I-V output curve of Au-MoS_2-Au and Gr-MoS_2-Gr separately. Each structure can be seen as a circuit with 2 back-to-back Schottky diodes paired with a resistor. Because both devices showed symmetrical I-V curves, it is more appropriate to use a back-to-back diodes model rather than a single diode model in this case as discussed in Chapter 2 Literature review. When the metal-semiconductor-metal device is biased, the current in the circuit can be expressed as:[8,9]

$$I = I_0 \cdot exp[-\left(1-\frac{1}{n}\right)e\beta V_1] \cdot [exp(\,e\beta V_1) - 1], \tag{3-1}$$

$$I = \frac{V_2}{R}\ , \tag{3-2}$$

$$I = -I_0 \cdot exp[\left(1-\frac{1}{n}\right)e\beta V_3] \cdot [exp(\,-\,e\beta V_3) - 1], \tag{3-3}$$

$$U = V_1 + V_2 + V_3, \tag{3-4}$$

where $\boldsymbol{U}$ is the source-drain bias, $\boldsymbol{I}$ is the source-drain current, $\boldsymbol{n}$ is the ideality factor, $\boldsymbol{e}$ is the elementary charge unit, and $\beta = \frac{1}{k_B T}$ is the Boltzmann factor, V_i $(i = 1,2,3)$ are the voltage drop across the left diode, middle resistor channel and right diode. $\boldsymbol{I_0}$ is a constant related to the Schottky barrier height which can be further expressed as:[10]

$$I_0 = S A_{2D}^* T^{3/2} \cdot \exp(-\beta e \Phi_{SB}^*), \tag{3-5}$$

where S is the contact width of Gr and TMD, A_{2D}^* is the 2-Dimensional equivalent of Richardson constant, T is the temperature, and Φ_{SB}^* is the effective Schottky barrier height. By solving equations above, it is possible to fit the I-V curves of the 2 types of MSM devices using fitting parameter I_0 and calculate the effective Schottky barrier heights.

3.5 Reference

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Chapter 4 Graphene-MoS_2 Schottky Diodes

4.1 Introduction

As mentioned in Chapter 2 Literature Review, two-dimensional materials show unique properties and many 2D materials have been studied.[1-10] By combining these 2D crystals, heterostructures can be created. Novel 2D devices, such as transistors, logic devices, light-emitting diodes, and photodetectors have been fabricated using 2D heterostructures.[11-18] Among these heterostructures, graphene-TMDs heterostructures are particularly interesting since many exciting phenomena have been observed.[19-32] For example, in graphene-MoS_2 hybrids, a responsivity of 5×10^8 A/W at room temperature was observed.[23] Gr-WS_2 heterostructures exhibit gate-tunable rectification with a maximum rectification ratio of 10^3, due to the existence of asymmetrical Schottky barriers.[19]

However, most 2D Gr-TMDs Heterostructures previously studied are based on mechanical exfoliated 2D materials thus the fabrication yield and scalability are severely restrained. Due to the small number of tested devices, it is challenging to obtain results that are statistically robust. Also, to fully understand the properties of the heterostructures, the responses of Au-TMDs and TMD-graphene interfaces to external modulations need to be thoroughly studied.

Here, Au-MoS_2-Gr heterojunctions made from all CVD-grown 2D materials were studied. A strong current rectification was observed in nearly all 44 devices tested, with a maximum rectification ratio over 2×10^4, which is 10 times higher than graphene-WS_2 device as reported.[19] Both external gating and laser illumination (532nm) can tune the rectifying behavior, which implies modified Schottky barriers of Au-MoS_2 and MoS_2-Gr interface. It was also observed that

laser irradiation could switch on the off-current thus greatly reduce the rectification ratio, while the rectification ratio under gating is relatively stable. To explain the different tunabilities between laser and gating, MoS_2 field-effect transistors with Au and Gr electrodes were fabricated separately. Au-MoS_2 and MoS_2-Gr Schottky barriers heights and their responses to external gate and laser were extracted from the output characteristics of the two FETs respectively. The height difference of Au-MoS_2 and MoS_2-Gr interface was found to be relatively constant under external gate voltage but quickly narrows down under laser irradiation.

4.2 Device Fabrication

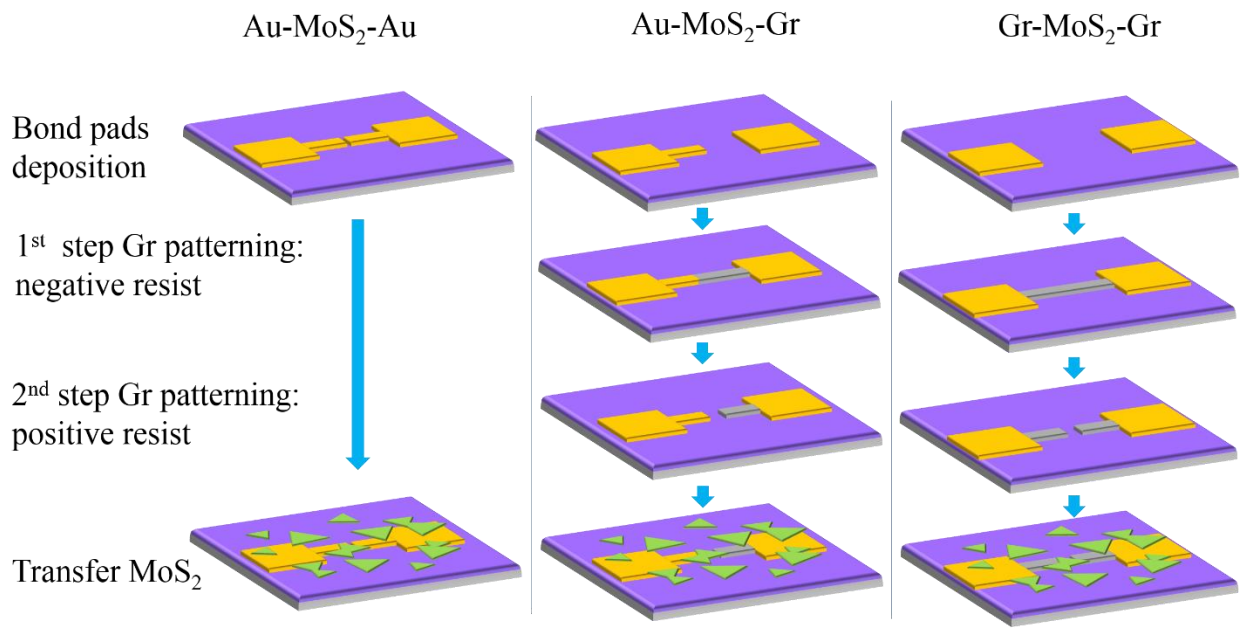


Figure 4.1. Fabrication process of devices of 3 types of structures. Fabrication process schematic of Au-MoS_2-Au, Au-MoS_2-Gr and Gr-MoS_2-Gr devices designed for this experiment. 2 steps of graphene patterning are used to achieve higher fabrication accuracy

The fabrication process of all three types of devices, Au-MoS_2-Au, Au-MoS_2-Gr, and Gr-MoS_2-Gr, is shown in **Figure 4.1**a. It takes up to 4 steps: 1. A clean chip (Si/SiO_2 300nm) was

spin-coated with PMMA and patterned using electron-beam lithography and Cr(10nm)/Au(80nm) was deposited onto the chip using thermal evaporation. 2. Graphene was transferred and roughly defined using negative resist and etched by oxygen plasma. 3. Graphene was finely defined using PMMA and etched by oxygen plasma. The etching of graphene took two steps as higher resolution and accuracy can be achieved by using PMMA. 4. MoS_2 domains were subsequently transferred onto the chip. For Au-MoS_2-Au structure, step 2 and 3 are not necessary as no graphene was used. Both MoS_2 domains and graphene films were synthesized using CVD method and transferred using the wet transfer method as previously demonstrated in chapter 3 methods section.[33-35]

The features of the three types of device were designed to be comparable with each other. On each 1cm×1cm silicon chip, 495 devices (33rows × 15columns) were made. Each device contains two bond pads of 150 μm×150 μm and source-drain electrode arm of either Cr/Au or graphene. The width of the source-drain electrode arms is 20 μm and the gap between the two arms is 1μm, which is designed to accommodate the conductivity of CVD-synthesized MoS_2 domains. To make sure both electrodes can fit in one photo under an optical microscope and to make it large enough to put a probe onto, the size of bond pads were deliberately chosen to be 150 μm×150 μm. The width of the source-drain electrode arm was designed to match the domain sizes and conductivities of both MoS_2 and WS_2. If the width is too small, the device might not be conductive and if too large, the gap will not be sufficiently covered. Previously, my colleague Dr. Haijie Tan has fabricated WS_2 transistors of 20 μm×5 μm and 20 μm× 0.2 μm. When the gap length is 5 μm, the device was nearly not conductive. And to make gap length of 0.2 μm, it is required to pattern the electrodes twice using electron-beam lithography for better resolution, resulting in a much higher failure risk and more effort input. I found that a gap length of 1 μm was a perfect balance for both

conductivity and fabrication (only one e-beam patterning is enough), so all my devices use 20 μm× 1 μm as standard gap size.

It is worth noting that MoS_2 domains were randomly distributed over the chip and the domain size of MoS_2 varies from 10 μm to 40 μm. Among all 495 devices, about 10% of them have sufficient MoS_2 coverage, giving about 50 functional devices for Au-MoS_2-Au. As the success rate of graphene patterning is around 80%, the number of testable devices is about 40 for both Au-MoS_2-Gr and Gr-MoS_2-Gr. For each structure, I fabricated one chip with 495 devices and all the results shown in this chapter were from those devices. All the MoS_2 samples were kindly provided by my colleague Dr. Wenshuo Xu.

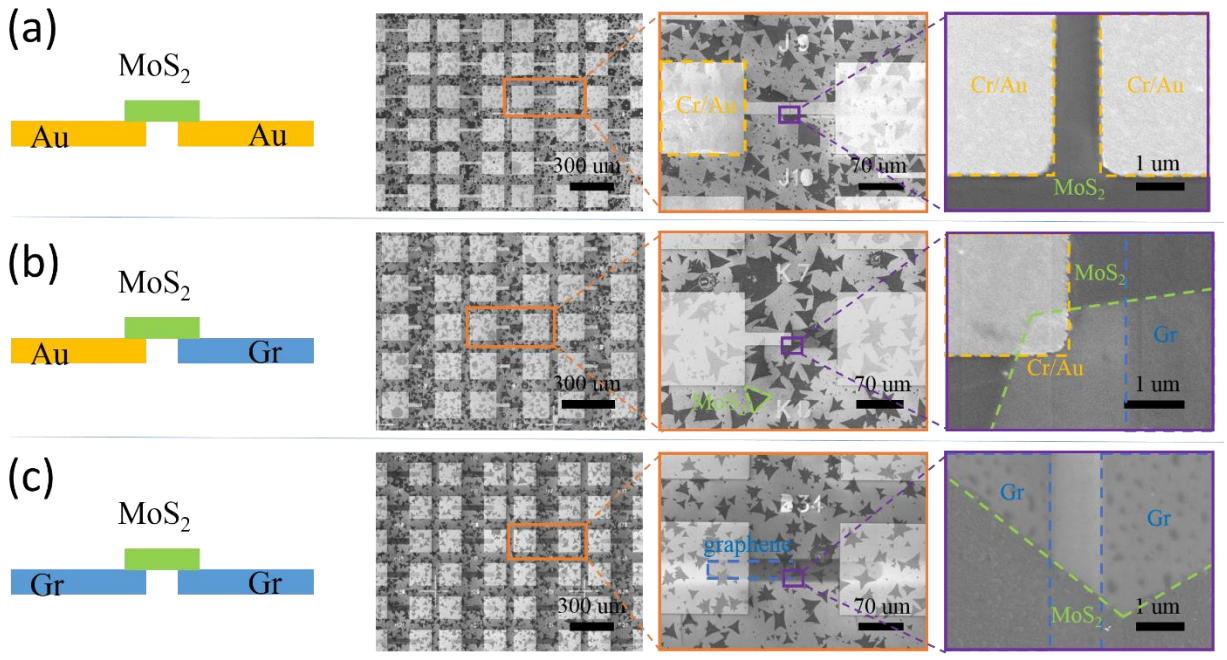


Figure 4.2. Configuration schematic and SEM images of fabricated structures. (a) Au-MoS_2-Au. (b) Au-MoS_2-Gr. (c) Gr-MoS_2-Gr. In SEM images, Cr/Au bond pads are indicated with the golden dashed line, MoS_2 domains with green dashed line and graphene with the blue dashed line.

Figure 4.2a, **4.2b**, and **4.2c** depict the cross-sectional schematic of Au-MoS_2-Au, Au-MoS_2-Gr, and Gr-MoS_2-Gr devices respectively. Alongside the device array, morphology and detailed feature of the heterostructure are shown. In the SEM images, gold, green and blue dashed lines are used to indicate Cr/Au, MoS_2 domains, and graphene film respectively. Given that in many cases MoS_2 domains do not fully cover Cr/Au or graphene electrodes, the active region of the devices is calculated using the overlapping area. Due to different contacts between MoS_2 channel and Au or Gr electrodes, the three devices display distinctive characteristics. For convenience, the properties of the symmetrical structure (Au-MoS_2-Gr), and asymmetrical structures (Au-MoS_2-Au and Gr-MoS_2-Gr) are discussed separately.

4.3 Results and Discussion

4.3.1 Materials Characterization

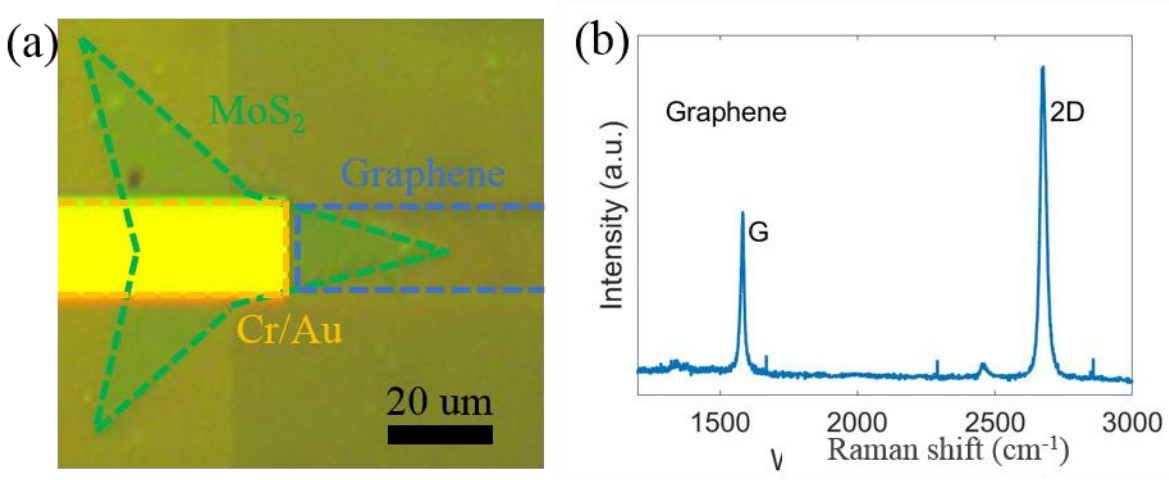


Figure 4.3. Raman characterization of CVD-grown graphene. (a) Optical image of an Au-MoS_2-Gr heterostructure showing Cr/Au in gold, MoS_2 in green and graphene in blue. (b) Raman spectra of graphene electrodes.

The 2D materials used in the heterostructure devices were characterized using Raman and photoluminescence (PL) spectroscopy. **Figure 4.3a** shows an optical image of the Au-MoS_2-Gr device including a spike-shaped MoS_2 domain. Optical images of Au-MoS_2-Au and Gr-MoS_2-Gr are shown in **Figure 4.4**.

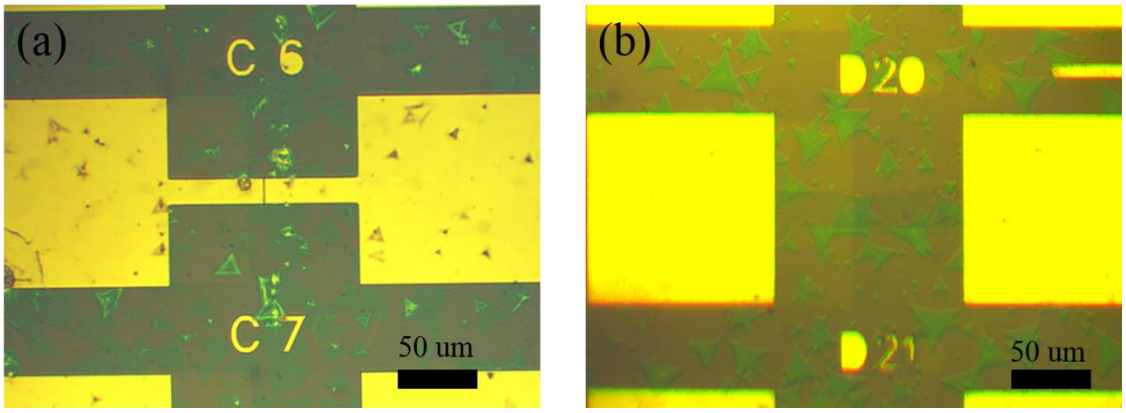


Figure 4.4. Optical images of two types of symmetrical heterostructures. (a) Au-MoS_2-Au and (b) Gr-MoS_2-Gr. The parameters of the devices are designed to be comparable.

Figure 4.3b shows the Raman spectra of the graphene electrode, under green laser with λ = 532 nm. The curve shows a 2D/G peak intensity ratio of about 2 (1.95 to be precise, after removing the background. The peak intensity is obtained by the maximum value of the peak, instead of integrated intensity), indicating that the graphene used in the device is in general monolayer, as discussed in Chapter 2 Literature Review.[36] Multilayer graphene region can also be found but does not influence the property of the devices.

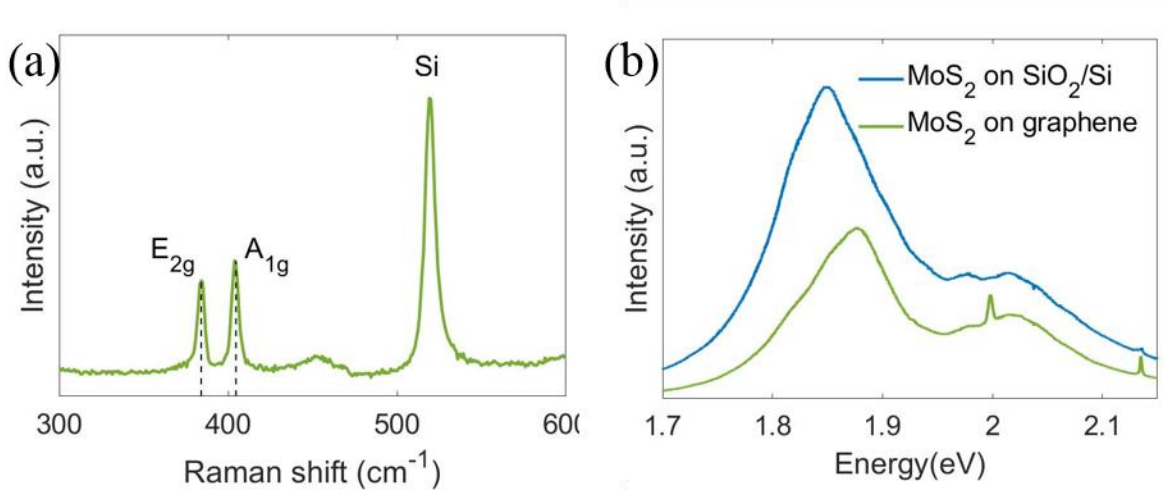


Figure 4.5. Raman and Pl characterization of CVD-grown MoS_2. (a) Raman spectra of the MoS_2 domain in the green framed region in **Figure 4.3a** under 532 nm laser. (b). PL spectra of MoS_2 domains: blue for MoS_2 on SiO_2/Si and green for MoS_2 on graphene. The two peaks near 580 nm and 620 nm corresponds to the G peak and 2D peak of graphene underneath.

Figure 4.5a shows the Raman spectra of MoS_2 domains used in the device. Two characteristic Raman vibration modes can be found in the spectra. The E_{2g} mode is the in-plane vibration of molybdenum and sulfur atoms. The A_{1g} mode is associated with the out-of-plane vibration of sulfur atoms. The thickness of MoS_2 domains has been extracted using the frequency difference between these two modes as discussed before. The spectra show that the two peaks located at 384.08 cm^{-1} and 404.64 cm^{-1}, giving a frequency difference Δk of 20.56 cm^{-1}. This result means that this CVD-grown MoS_2 is a monolayer as shown in **Figure 3. 12b**, Chapter 3 Research Methodology, which is also consistent with other reports.[34, 37]

The photoluminescence (PL) of monolayer MoS_2 on SiO_2 and graphene substrate, is shown in **Figure 4.5b**. All PL spectra in the figure were normalized against the Raman intensity. For the PL spectrum of MoS_2 transferred on graphene substrate, the PL peak intensity was significantly quenched compared to that on SiO_2 substrate. The quench corresponds to the interlayer coupling

and electronic interaction with the graphene substrate, as the photo-excited electrons and holes from MoS_2 domain easily transfer to graphene, resulting in a decreased recombination process of excitons and the quenching of PL signal. This indicates a good contact between graphene and MoS_2 interface, which is in good agreement with previous reports.[38,39] The two additional peaks near 580 nm and 620 nm corresponds to the G peak and 2D peak of graphene underneath.

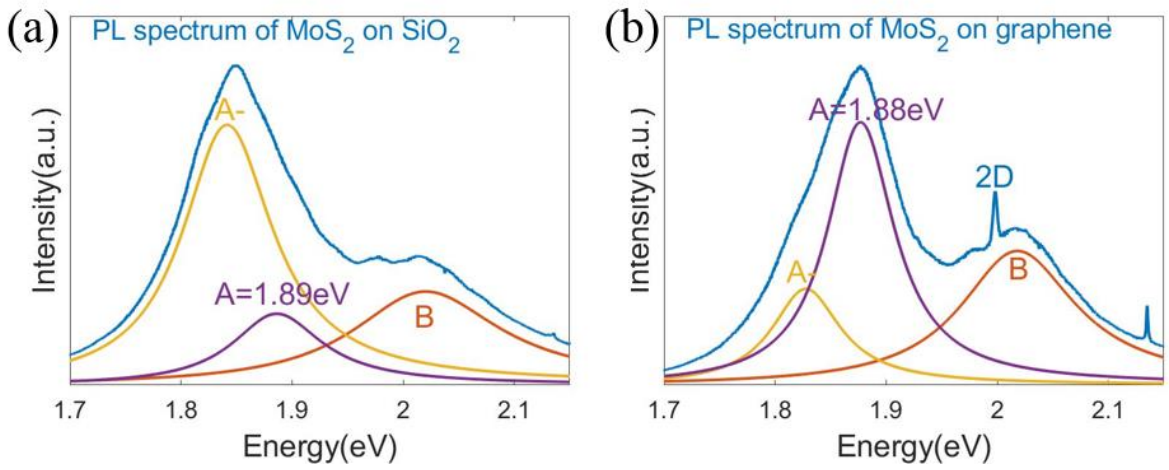


Figure 4.6. PL spectrum and peaks fitting of MoS_2. (a) PL spectrum and peaks fitting of MoS_2 on SiO_2/Si (b) PL spectrum and peaks fitting of MoS_2 on graphene.

Furthermore, peak fitting on PL spectra has been carried out based on Lorentz peak function to study the relative luminescence quantum efficiency. As is shown in **Figure 4.6a** and **4.6b**, the PL spectra of MoS_2 have three sub-peaks which correspond to A, A- and B peaks respectively as shown in **Figure 3.13**, Chapter 3 Research Methodology. Both fittings have an adjusted $R^2 > 0.99$. The A (at ~1.89eV) and B (at ~ 2.0eV) peaks are excitons associated with the direct transition from the conduction band to two spin-orbit split valence band at the K point. The peak A- (at ~1.82eV), which is located at slightly lower energy than A peak, corresponds to the recombination of negatively charged excitons of trions A-. The trion A- arises from a free electron bounded to a neutral exciton via Coulomb interaction because MoS_2 could be easily negatively doped by

contamination or contact with the substrate. As discussed in chapter 3, the fitting process is done by first inputting the estimated peak positions given above. Then the fitting function generates accurate peak positions and intensities. For both **Figure 4.6a** and **4.6b**, the adjusted R^2 is > 0.99, which means it is a relatively good fitting.

Upon comparing the integrated A and A- PL peaks of different spectra, it can be noticed that the PL intensity ratio of A to A- (A/A-) changed. The A/A- ratio presents the relative populations of neutral and charged A excitons. In the PL spectra of MoS_2 transferred on SiO_2, the PL peak is dominated by A- peak, revealing a high degree of charged impurities from the SiO_2 substrate which is in agreement with previous studies. [30,39] On the contrary, for MoS_2 transferred onto a graphene substrate, the A/A- ratio was reversed. This is due to the fact that conducting graphene acts as a p-doping agent for MoS_2. Moreover, a slight red shift of A peak could be observed alongside with the change of A/A- intensity ratio. Previous studies suggested that the uniaxial tensile strain in MoS_2 domains could result in the peak shift of A peaks. The redshift is associated with the difference in uniaxial tensile strain in the MoS_2 domain introduced by SiO_2 and graphene substrate respectively.

4.3.2 Electronic and Optoelectronic Properties of the Diode

To understand the properties of MoS_2-Gr heterostructure devices, I-V measurements were conducted under different gate voltages and illumination intensities. All electronic and optoelectronic measurements reported here were done at room temperature. The results of Au-MoS_2-Gr devices are shown in **Figure 4.7-4.9** and the results of Au-MoS_2-Au and Gr-MoS_2-Gr are shown in **Figure 4.10-4.12**.

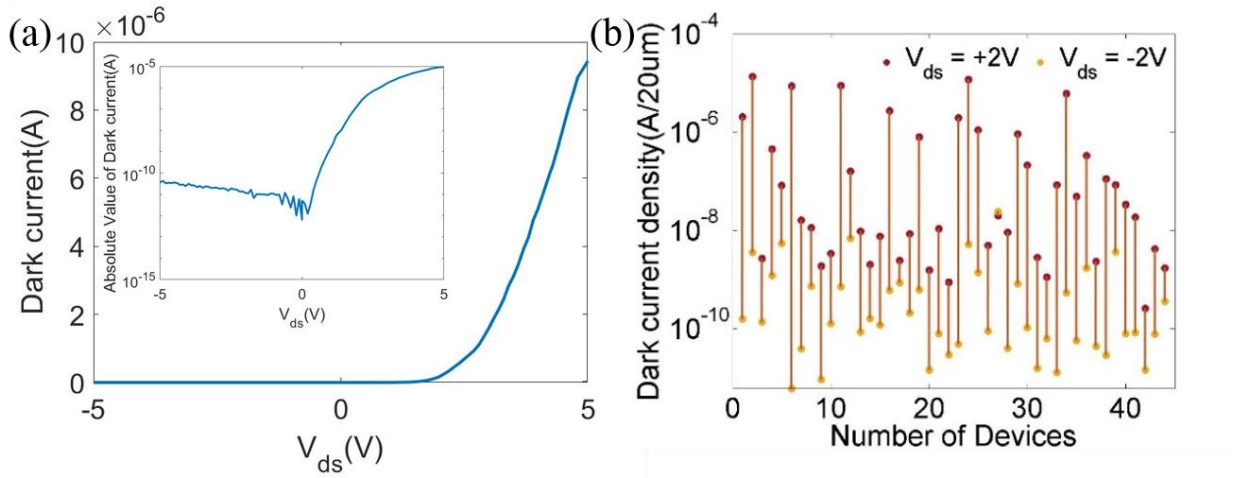


Figure 4.7. Characteristics of the MoS_2-Gr diode. (a) Typical output characteristics of the diode. Inset: the absolute value of the current in logarithm scale. (b) Statistics of rectification of 44 working devices. The sign of the current is ignored when a negative bias is applied, to better illustrate the on-off states.

For the Au-MoS_2-Gr heterostructure, 44 devices in total were measured and a typical output characteristic is shown in **Figure 4.7a**. Current rectification behavior can clearly be seen, allowing current to flow through only when the device is positively biased. Though the curve begins to saturate at around V_{ds} = 5V, which is consistent with the simulated I-V curve of the asymmetrical back-to-back diode shown in **Figure 2.6d**, it can be seen that the heterostructure functions as a diode connected with a resistor within V_{ds} = -5V to 5V. To explain this rectification behavior, Schottky barriers must have formed between Au-MoS_2 and Gr-MoS_2 interface. Schottky barriers inhibit the flow of electrons (holes), allowing only limited charge injection through tunneling and thermionic emissions. The theoretical height of Schottky barrier can be estimated using Schottky-Mott rule: $\Phi_{Schottky\ Barrier} = \Phi_{Metal} - \chi_{TMD}$ (2-2), in which Φ_{Metal} is the work function of metal (and graphene), χ_{TMD} is the electron affinity of semiconductor. Thus the height of Au-MoS_2 barrier is estimated to the the be $\Phi_{Au-MoS2} = \Phi_{Au} - \chi_{MoS2} = 5.1 - 4.0 = 1.1eV$.[40] The height of Gr-$MoS_2$ barrier is estimated to be $\Phi_{Gr-MoS2} = \Phi_{Gr} - \chi_{MoS2} = 4.6 - 4.0 = 0.6eV$. This

Schottky barrier height difference is the reason why rectification was observed in Au-MoS_2-Gr heterostructure: it is easier for electrons to migrate from graphene to MoS_2 as the barrier is lower, giving rise to the measured current when positively biased. When negatively biased, electrons need to flow through a higher Au-MoS_2 barrier, resulting a much smaller measured current. Although it is possible to roughly estimate the theoretical Schottky barrier heights under static conditions, the effective barrier height may change under certain conditions such as external gating and laser exposure.

It is worth noting that 4.6eV as a work function is for pristine graphene. My CVD grown graphene was p-doped, as the Dirac point was at around V_g = 30V instead of 0V. Thus 4.6eV is an underestimation of the CVD grown graphene. A more accurate estimation can be achieved by using the work function of p-doped graphene. It was found that the change of the work function was typically within 0.2 eV when the Dirac point was at V_g = 40V, using 300 nm SiO_2 dielectric layer.[43] So the more accurate estimation of Gr-MoS_2 Schottky height using Schottky-Mott rule is = 4.6 + 0.2 – 4.0 = 0.8 eV. This barrier height is still smaller than that of Au-MoS_2 which is 1.1eV.

The Au-MoS_2-Gr device contains two Schottky barriers: Au-MoS_2 and MoS_2-Gr, and each barrier can be simplified as a diode. The device can be simplified into a back-to-back diode, connected with a resistor in series. However, the I-V curve of the device showed typical single diode behavior. This result is consistent with **Figure 2.6b** and **Figure 2.9** in Chapter 2 Literature Review in which the property of asymmetrical back-to-back Schottky diode was demonstrated. The study has shown that back-to-back connected asymmetric Schottky diodes with series resistance show very similar performance as that of a single diode.[44] The I-V curve of the back-to-back diode maintains the barrier parameters of the higher-barrier diode. I measured the heights of

the Schottky barriers (Au-MoS_2 and MoS_2-Gr) using Au-MoS_2-Au and Gr-MoS_2-Gr respectively and proved the Au-MoS_2-Gr structure is an asymmetric back-to-back diode.

To better demonstrate the overall characteristics of the 44 devices, a statistic is shown in **Figure 4.7b**. The x-axis is simply device identification number and the y-axis is the dark current under different bias: V_{ds} = 2V and V_{ds} = -2V, namely on-current and off-current. The current (y-axis) is shown in logarithmic scale in order to make the data comparable, and the negative sign of current is omitted. The plotted current is calibrated by the area of the effective region. For example, if a MoS_2 domain only covers half of the channel (the active region is only 1μm × 0.5 × 20 μm), then the current is doubled. The overlapping width was measured using AutoCAD and the error was within 10%. The idea of the normalization is to show the estimated measured current if that device has full coverage of 20 μm by MoS_2 domains. This normalization allows us to compare the performance of the devices regardless of the MoS_2 domain size. And the normalization does not impact the on-off ratio because it changed on-current and off-current simultaneously. In brief, for each device, the two dotted points mean the absolute value of on-current and off-current when source-drain bias is +2V and -2V respectively, and the length of the line connecting two points stands for the rectification ratio, defined as on-current/off-current. It can be seen from the statistics that the overall off-current vary from 10^{-11} A to 10^{-9} A while the on-current has a larger variance, varying from 10^{-9} A to 10^{-5} A. The general rectification ratio about ~100 can be achieved and some devices perform pretty well, yielding a rectification ratio over 10^4. The best device had a rectification ratio of 1.4×10^6 but it was not representative as the off-current of it is 10^{-12} A which is lower than the limit of the measurement (10^{-11} A). Though the performance of the devices varies considerably, the rectification behavior is quite clear. The distribution of the dark currents and

forward voltages might result from the different doping levels of MoS_2 and graphene so that the Schottky barrier heights are different, according to Schottky-Mott rule discussed before.

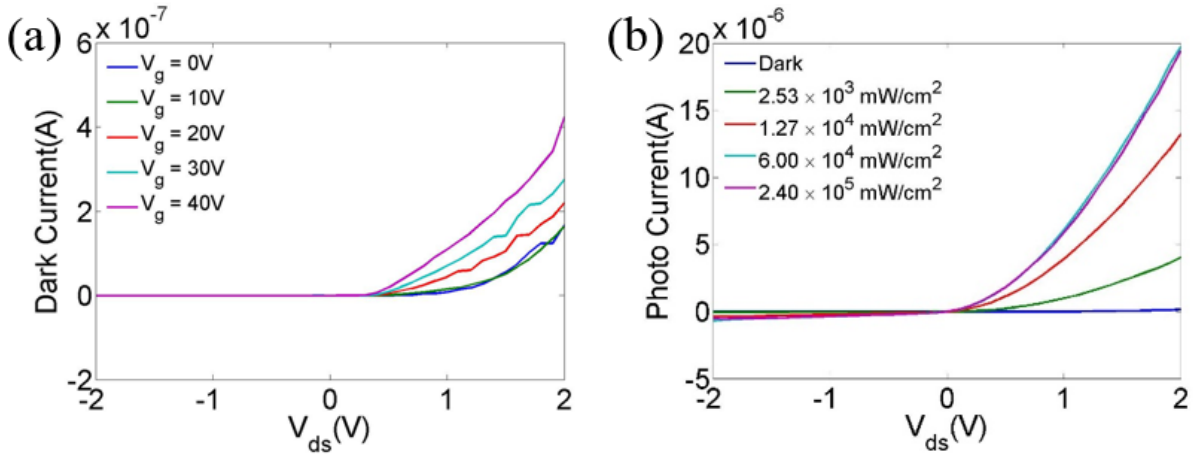


Figure 4.8. Characteristics of the MoS_2-Gr diode. (a) Gate-voltage dependence of rectifying behavior. (b) Laser-power dependence of rectifying behavior.

External gating and laser illumination are common techniques to modulate the properties of 2D materials. These have been found to have a substantial impact on the rectifying behavior of the device. **Figure 4.8a** shows the gate-dependence of rectification. Application of an external voltage increases both on-current and off-current. Under external gate voltage of V_g= 10V, 20V, 30V and 40V, the on-current increases by -3%, 32%, 64% and 153% compared to on-current without gating. The off-current increases by 28%, 40%, 92%, 67% in the meanwhile. The rectification ratio under various gate voltages remains around 10^4, shown in **Figure 4.8a**. **Figure 4.8b** shows the photocurrent of the device versus applied irradiation power intensity. A focused laser beam (532 nm) with various illumination power is used for optoelectronic measurements. The spot size of the beam is estimated to be ~150 μm^2. The photocurrent is defined as $I_{photo} = I_{illuminated} - I_{dark}$(2-7), which was extracted from I_{ds}-V_{ds} plots of the device under dark and illuminated conditions.

The laser power dependence of rectification of the heterostructure was also observed. Laser irradiation increased both on-current and off-current by several orders of magnitude, and the rectification ratio quickly decreased from 10^4 to about 40 at laser irradiation power of 2.53×10^3 mW/cm^2, as shown in **Figure 4.9b**. This decrease of rectification ratio is primarily because the off-current is significantly increased under laser irradiation, indicating a reduced Au-MoS_2 Schottky barrier height, as is discussed later in **Figure 4.14**. These results indicate that the modulation of the performance by external gating and laser irradiation are different mechanisms. To study how Schottky barriers are influenced by them, the properties of Au-MoS_2-Au and Gr-MoS_2-Gr devices are explored. Each of them can be seen as a Metal-Semiconductor-Metal (MSM) transistor, consisting of two back-to-back Schottky contacts.

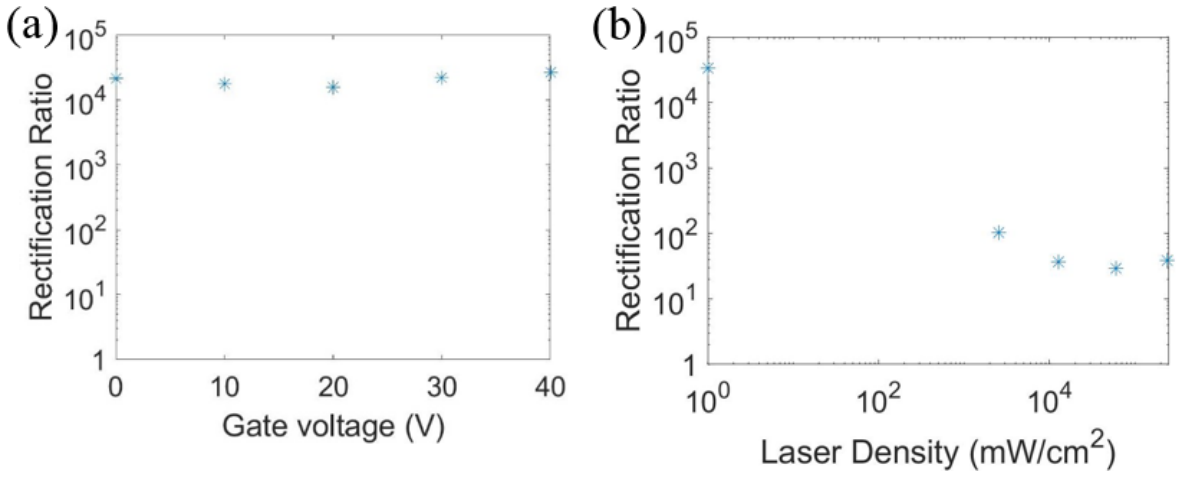


Figure 4.9. Rectification ratio of the MoS_2-Gr diode. (a) Rectification ratio, defined as $R = I_{ds}(V_{ds} = 2V)/ I_{ds}(V_{ds} = -2V)$, under various gate voltages. (b) Rectification ratio under various laser power.

4.3.3 Electronic and Optoelectronic Properties of the Transistors

The electronic and optoelectronic properties of Au-MoS_2-Au and Gr-MoS_2-Gr heterostructures are displayed in **Figure 4.10-4.12**. **Figure 4.10a** and **Figure 4.10b** show the dark current of Au-MoS_2-Au and Gr-MoS_2-Gr devices, under various gate voltages.

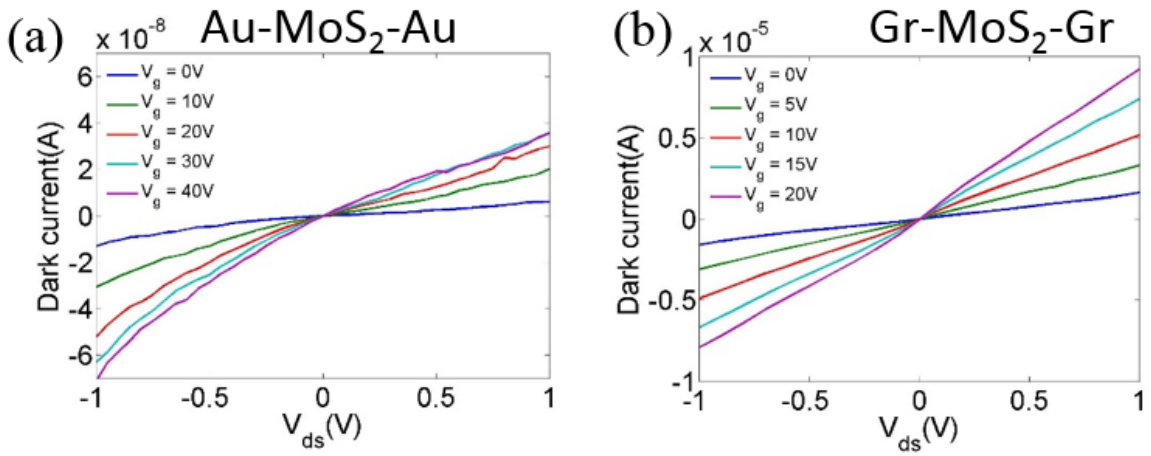


Figure 4.10. Electronic characteristics of the 2 symmetrical structures: Au-MoS_2-Au and Gr-MoS_2-Gr. (a) Gate-voltage dependence of the output characteristics of Au-MoS_2-Au structure. (b) Gate-voltage dependence of the output characteristics of the Gr-MoS_2-Gr structure.

The ranges are different to ensure the MoS_2 with graphene electrodes does not break down under high voltage. The two devices both exhibited a non-linear I-V curve, even under high gate voltage. This shows that both MoS_2-Gr and MoS_2-Au interfaces are non-ideal contacts, also known as the Schottky contact. The Schottky barriers contribute to the majority of the resistance and give rise to the non-linearity, resulting in a much better channel conductivity of MoS_2 with graphene electrodes due to the lower Schottky Barrier height. Note that the I-V curves of Gr-MoS_2-Gr device look less non-linear. This is because under high gating voltage, the Schottky barrier height has

decreased from 0.17eV to 0.11eV, and a linear I-V curve is reasonable, as shown in **Figure 4.14a**. Under low gating voltage, the measured current is too small compared to the y-axis, so the curvature was not very obvious.

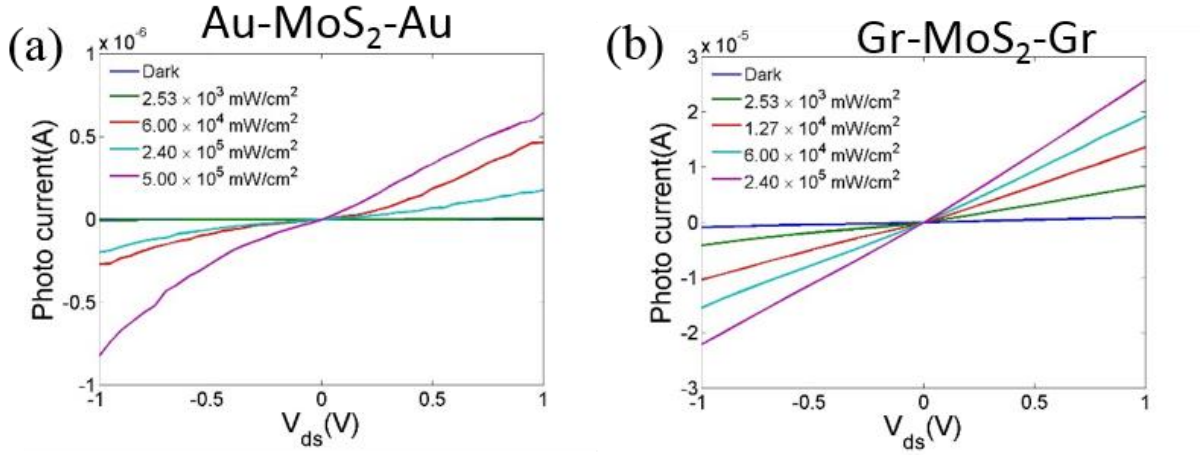


Figure 4.11. Optoelectronic characteristics of the 2 symmetrical structures: Au-MoS_2-Au and Gr-MoS_2-Gr. (a) Laser-power dependence of the output characteristics of Au-MoS_2-Au structure. (b) Laser-power dependence of the output characteristics of the Gr-MoS_2-Gr structure.

Figure 4.11a and **Figure 4.11b** show the photocurrent of Au-MoS_2-Au and Gr-MoS_2-Gr devices under various laser powers (λ=532 nm). The output characteristics of Au-MoS_2-Au are still non-linear upon illumination. However, the output characteristics of Gr-MoS_2-Gr became near-linear under illumination, suggesting a near ohmic contact between Gr electrodes and MoS_2 domains under irradiation conditions. To better describe the optoelectrical behavior of both types of devices, concepts of photoresponsivity (R), photoconductive gain (G), specific detectivity (D^*) were introduced in Chapter 2 Literature Review. **Figure 4.12b** shows the photoresponsivity of the two types of devices under an incident light power of 6.00×10^4 mW/cm^2, using equation (2-8). The photodetector with graphene electrodes shows higher photoresponsivity under ambient conditions, reaching 15AW^{-1} at a bias of +1V.

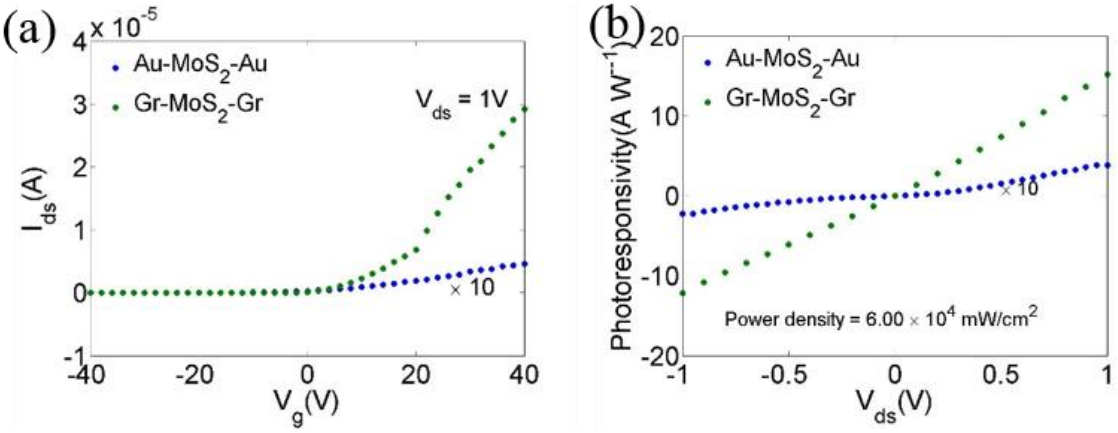


Figure 4.12. Field-effect and photoresponsivity of the 2 symmetrical structures: Au-MoS_2-Au and Gr-MoS_2-Gr. (a) I_{ds}-V_g plot of Au-MoS_2-Au and Gr-MoS_2-Gr heterostructure devices under drain-source bias = 1V, showing the n-type nature of CVD-synthesized MoS_2 crystal. (b) Photoresponsivity versus V_{ds} of the two types of devices, under illumination power density of 6.00×10^4 mW/cm^2.

The two devices as photodetectors can be characterized using photoconductive gain. As discussed in chapter 2, by assuming the light absorption rate and transmittance rate of MoS_2 under 532nm light (2.33 eV) are 10% and 90%,[41] it is possible to calculate the internal photoconductive gain for both types of devices using equation (2-10). The internal photoconductive gain (G_{int}) of MoS_2 with metal electrodes is 9 and MoS_2 with graphene electrodes is 353, at a bias of V_{ds} = 1V.

Using equation (2-11), the estimated detectivity of MoS_2 with Au electrodes is 8.8×10^{11} Jones (Jones = cm $Hz^{1/2}$ W^{-1}) and the detectivity of MoS_2 with graphene electrodes is 1.2×10^{10} Jones, which is lower than that of Au-MoS_2-Au, due to a much higher dark current.

Figure 4.12a shows the field effect of the two types of MSM transistors. Both of the plots shows the n-type nature of CVD-grown MoS_2 domains, with a threshold voltage (V_{th}) of ~ 10V. Although the threshold voltage is theoretically related to the Schottky barrier heights, the existence of trapped states will move the theoretical threshold voltage (V_{th}). The estimated mobility of both

types of devices can be extracted from **Figure 4.12a**, using $\mu = \frac{dI_{\mathrm{ds}}}{dV_{\mathrm{g}}} \cdot \frac{L}{w} \cdot \frac{1}{V_{\mathrm{sd}}} \cdot \frac{1}{C_{\mathrm{ox}}}$ (2-6), where L and w are the channel's length and width respectively, and C_{ox} is the oxide capacitance per unit area calculated by $C_{\mathrm{ox}} = \frac{\varepsilon_0 \varepsilon_r}{d} = 11.53\, nF/cm^2$, in which ε_0 = 8.854 × 10^{-12} F/m is the permittivity of free space, ε_r = 3.9 is the dielectric constant of SiO_2 and d = 300 nm is the thickness of the SiO_2 layer. The calculated mobility of MoS_2 with Au electrodes and Gr electrodes are 0.054 $cm^2\ V^{-1}\ s^{-1}$ and 4.21 $cm^2\ V^{-1}\ s^{-1}$ respectively.

The measured mobilities were much smaller compared to experimental record values of ~150 $cm^2V^{-1}s^{-1}$ as shown in **Figure 2.16**, chapter 2. This is a result of various reasons: first, the devices were measured at room temperature. The vibrating atoms create acoustic waves (phonons) in MoS_2, which can collide with carriers and scatter them. This lattice (phonon) scattering effect tends to reduce carrier mobility. Second, the MoS_2 domain used in my devices were CVD-grown instead of exfoliated, and the devices were measured in the ambient environment. There were more defects introduced to the MoS_2 domains during synthesis and measurement stages. The defects are typically ionized and deflect electrons or holes by the Coulombic forces. The more heavily the MoS_2 is doped, the higher chance that a carrier will collide with an ion in a given period, and the smaller the mobility. This effect is known as ionized impurity scattering.

The different values for MoS_2 mobilities for Au-MoS_2-Au and Gr-MoS_2-Gr devices are because of the two-contact measurement used in the experiments. Electron mobility is an intrinsic property of the CVD-grown MoS_2 channel and it can be obtained using formula (2-6). However, in a two-contact measurement, Schottky barriers cause a potential drop across the junction, so that the V_{sd} used in the calculation is much larger than the actual voltage difference

across the MoS_2 channel, resulting in a much smaller measured mobility, compared to the actual mobility. It can be seen that a high Schottky barrier (Au-MoS_2) greatly decreases the effective (measured) mobility of the device as the carrier injection over the barrier is less effective.[45,46] Thereforethe measured mobility of MoS_2 in Gr-MoS_2-Gr device is a closer estimation of the actual mobility of this CVD-grown MoS_2. To obtain the actual mobility, it is more accurate to use four terminal measurement, where a pair of leads is used to inject the measurement current while a second pair of leads is used to measure the potential drop across the channel. Although two-terminal measurements underestimate the actual mobility, it is still widely used for its simplicity and convenience. It was used in my experiments because there were only two probe stations available.

In **Figure 4.10-12** it can be seen that laser irradiation and external gating substantially impact the performance of MoS_2 by modulating the corresponding Schottky barrier heights between MoS_2 and metal (graphene). Though the barrier heights under static conditions were already estimated, it is difficult to estimate the change of barriers heights under external modulation. So a Schottky barrier fitting method was employed, which was developed by my colleague Dr. Ye Fan.[39] Using a symmetrical structure, for example, Au-MoS_2-Au and Gr-MoS_2-Gr, the MSM transistor can be simplified into a circuit with two back-to-back Schottky diodes and a resistor. After fitting the I-V curves under the different gates and laser intensity (**Figure 4.10, 4.11**) using a modified thermionic emission equation in Chapter 3 Research Methodology, the Schottky barrier heights under certain conditions were extracted. The results are shown in **Figure 4.14**.

4.3.4 Schottky Barrier Estimation

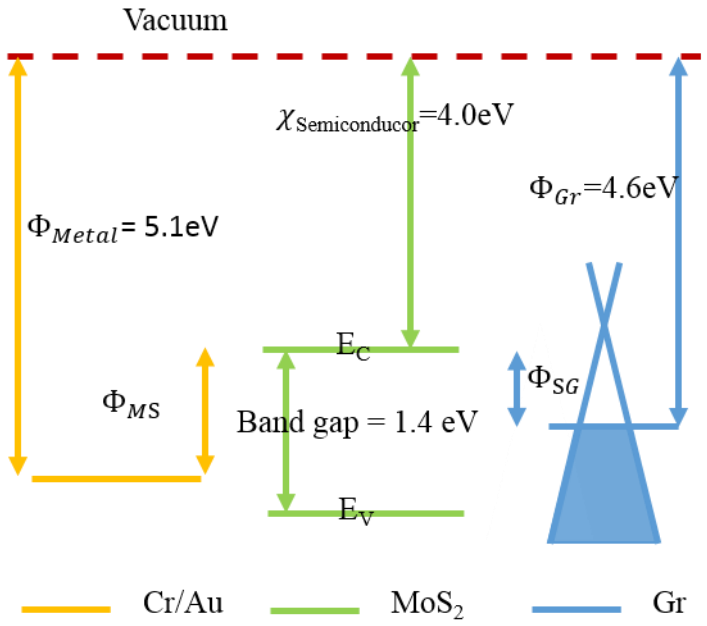


Figure 4.13. Band Schematic of a lateral Au-MoS_2-graphene heterostructure. Gold: Cr/Au electrode. Green: MoS_2 channel. Blue: graphene electrode.

The gate dependence of Schottky barrier heights is shown in **Figure 4.14a**. Both Au-MoS_2 and Gr-MoS_2 barrier heights decrease as back gate voltage increases. This is expected because it has been demonstrated in some prior results that gate voltage raises up the Fermi level in graphene.[30,39] This is due to the nature of 2D materials: The limited density of states of 2D materials makes them very sensitive to the gate voltage. The simultaneous change of Au-MoS_2 and MoS_2-Gr barrier heights could explain the relatively stable rectification ratio under gate voltage, as shown in **Figure 4.9a**.

The poor gate control of Au-MoS_2 junction might also result from the air between MoS_2 and SiO_2 substrate. The bond pads (thickness = 90nm) were evaporated first and MoS_2 film was transferred onto the bond pads. So naturally, there might be some air near the Au-MoS_2 junction.

The existence of the air gap will reduce the effectiveness of external gating. The effective capacitance near the junction is a complex capacitance of SiO_2 layer connected with an air gap in series: $C_{complex} = \frac{C_{air} + C_{oxide}}{C_{air} \times C_{oxide}}$, resulting in a smaller capacitance and thus poor gate control. This explanation can be verified by making devices where MoS_2 is under electrodes to eliminate the air gap. Details are given in Chapter 7 Future Work.

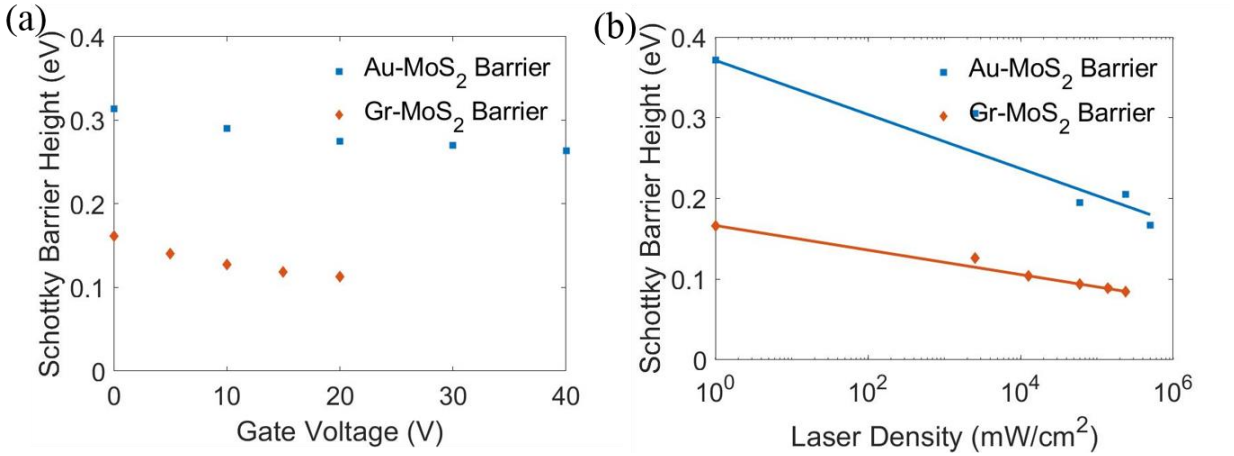


Figure 4.14. Mechanism of the tunable behavior explained by Schottky barrier change. (a) Calculated effective Schottky barrier height change of MoS_2-Au and MoS_2-Gr interface under various external gate voltages. (b) Calculated effective Schottky barrier height change of MoS_2-Au and MoS_2-Gr interface under various irradiation powers.

The laser density dependence of Schottky barrier heights is shown in **Figure 4.14b**. Laser illumination has different impact on Au-MoS_2 and MoS_2-Gr barriers. Laser irradiation quickly decreases the barrier height of Gr-MoS_2 to 0.2 eV, and the difference in heights with Au and Gr quickly narrowed down. This explains the quick drop of the rectification ratio of Au-MoS_2-Gr heterostructure under laser irradiation, as shown in **Figure 4.9b**. The modification of Au-MoS_2 barriers under laser irradiation can be explained by the photogating effect, which has been observed in a previous study.[30] After the application of the laser beam, the electron-hole pairs can

be generated. While electrons migrated and contributed to the photocurrent, holes only resided in MoS_2 domains, due to the existence of trap states between MoS_2 and Au electrodes. The accumulated holes act as active gating to MoS_2 so that the barrier heights of Au-MoS_2 decreased quickly.

For the graphene-MoS_2 barrier, the contact between these two 2D materials is good without a high density of trapped states. The decrease of barrier height results from the migration of photogenerated electrons. Those electrons traveled to graphene ribbons and reduced the work function of graphene (increased Fermi level), resulting in a decreased Schottky barrier height.

The predicted Schottky barrier heights using Schottky-Mott rule are larger than the measured ones. For Au-MoS_2 interface, the predicted one is likely to be an overestimation. The Schottky barrier height did not change much when gate voltage was applied, suggesting that there was Fermi level pinning effect so that the effective Schottky barrier height is lower than the predicted one, as demonstrated in Chapter 2 Literature Review. For MoS_2-Gr interface, it is also an overestimation because graphene was n-doped by MoS_2 domains so that the effective Schottky barrier is lower than the predicted one. [39]

As the Au-MoS_2-Gr device can be modulated by laser irradiation, the temporal response of the device under a laser beam was also measured and shown in **Figure 4.15**. Both positive bias V_{ds} = 1V and negative bias V_{ds} = -1V were applied, and the laser beam was turned on and off consecutively every 20 seconds. It can be seen that the response was relatively slow and the on-off ratio is smaller than 10, indicating that the possibility of using the device as a photodetector is limited.

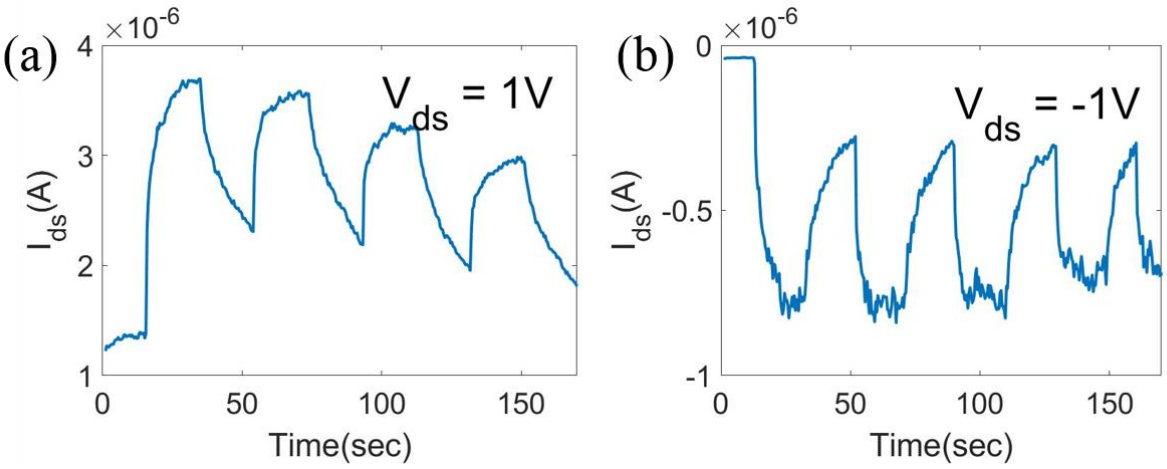


Figure 4.15. Temporal response of Au-MoS_2-Gr heterostructure. (a) Under a bias of V_{ds} = 1V and (b) Under a bias of V_{ds} = -1V. Both curves are measured using a green laser (532nm) of the power density of 6.00×10^4 mW/cm^2.

4.4 Conclusion

In summary, three types of heterostructure devices based on CVD-grown graphene and MoS_2 were fabricated. Their electronic and optoelectronic properties were measured. A significant rectification was observed in nearly all 44 Au-MoS_2-Gr devices, with the highest rectification ratio over 2×10^4. The rectifying behaviour can be tuned by application of a back-gate voltage or by laser irradiation, each will impact on the rectification ratio differently. Asymmetrical Schottky barriers of Au-MoS_2 and MoS_2-Gr interfaces are the reasons for the phenomenon. Schottky barriers of the two interfaces were estimated using output characteristics of Au-MoS_2-Au and Gr-MoS_2-Gr field-effect transistors. The difference between Au-MoS_2 and MoS_2-Gr barrier heights quickly narrows down under laser irradiation, which explains the quick drop of rectification ratio in the Au-MoS_2-Gr device. This study increases our understanding of 2D heterostructures and can be useful for future applications such as photosensors and gate-logics.

4.5 Contribution Statements

Dr. Ye Fan provided training in device fabrication and wrote the Matlab script for Shottky Barrier estimation. Dr. Haijie Tan provided training in AutoCAD design and electrical measurements. Dr. Wenshuo Xu provided CVD-grown MoS_2 for this study. Dr. Yuewen Sheng provided CVD-grown graphene for this experiment. Mr. Tongxin Chen did the spectroscopy (Raman and PL) characterization and provided constructive comments for the analysis.

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Chapter 5 Graphene-WS_2 Schottky Diodes

5.1 Introduction

The previous Chapter studied the electronic and optoelectronic properties of Au-MoS_2-Gr heterostructure device. Tunable rectifying behavior was demonstrated and the mechanism was explained. However, as discussed in Chapter 2 Literature Review, the thickness of 2D materials has a great impact on the properties of 2D materials. For example, MoS_2 transits from a direct gap semiconductor to an indirect semiconductor when layer number increases.[1] Due to the fact that it is very challenging to control the thickness of CVD-grown MoS_2 using the recipe previously introduced in Chapter 3 Methodology. WS_2 became a promising candidate to study the layer-dependent properties of 2D materials and their heterostructures as both monolayer and bilayer WS_2 can be obtained using the CVD method.[2,3]

As briefed in Chapter 2 Literature review, monolayer WS_2 is also a direct bandgap semiconductor, with a bandgap around 2.0 eV while bilayer WS_2 is an indirect gap semiconductor with a smaller bandgap around 1.3 eV.[4] By far, many electronic and optoelectronic devices based on WS_2 have been studied and show interesting properties, including transistors,[5-8] light-emitting devices,[9-11] solar cells,[12-14] photodetectors,[15,16] and chemical sensors.[17-20] Among all of the structures, heterostructures based on graphene and WS_2 show unique properties.[20-27] In few-layer MoS_2-Graphene heterostructures, nonlinear drain current with drain voltage sweep was observed.[28,29] Similar current rectification was also found in WS_2-graphene heterostructures, in which the rectification ratio can be modulated by external gate field as a result of modified Schottky barriers.[30,31] Photocurrent can also be generated as illumination facilitates electrons' thermionic tunneling through the Schottky barrier. Because the carrier separation in graphene-

TMDC heterostructures is very efficient, a high photoresponsivity (5×10^8 AW^{-1}) and quantum efficiency (32%) can be achieved,[32] making it promising for novel photodetectors.

However, previous work focuses mainly on materials obtained from mechanical exfoliation, which is not ideal for batching processing and thus mass production of devices and integrated circuits and image sensors. Also, in order to utilize these 2D heterostructures in modern electronics, it is important to study the layer-dependent properties of the heterojunctions based on 2D materials produced by a scalable method.

In this work, graphene-WS_2 heterostructure devices were fabricated using 2D materials synthesized by chemical vapor evaporation (CVD) method. Devices based on both monolayer WS_2 and bilayer WS_2 were studied. The output characteristics were measured and a clear current rectification was observed. External gate voltage and laser irradiation were employed to modulate the properties of the heterostructure. The tunability could be explained by the Fermi level moving of graphene and band bending of WS_2 respectively. The impact of WS_2 layer number was observed and discussed. An on-off ratio over 200 under illumination can be achieved for both monolayer and bilayer WS_2 devices, opening up the possibility of making photodetectors using graphene-WS_2 heterostructure from all CVD-grown materials.

5.2 Device Fabrication

Figure 5.1 shows the process of device fabrication, which is quite similar to the fabrication of Au-MoS_2-graphene device. Both WS_2 domains and graphene continuous films were grown using CVD method and transferred using methods summarized in chapter 3 methods section.[33]

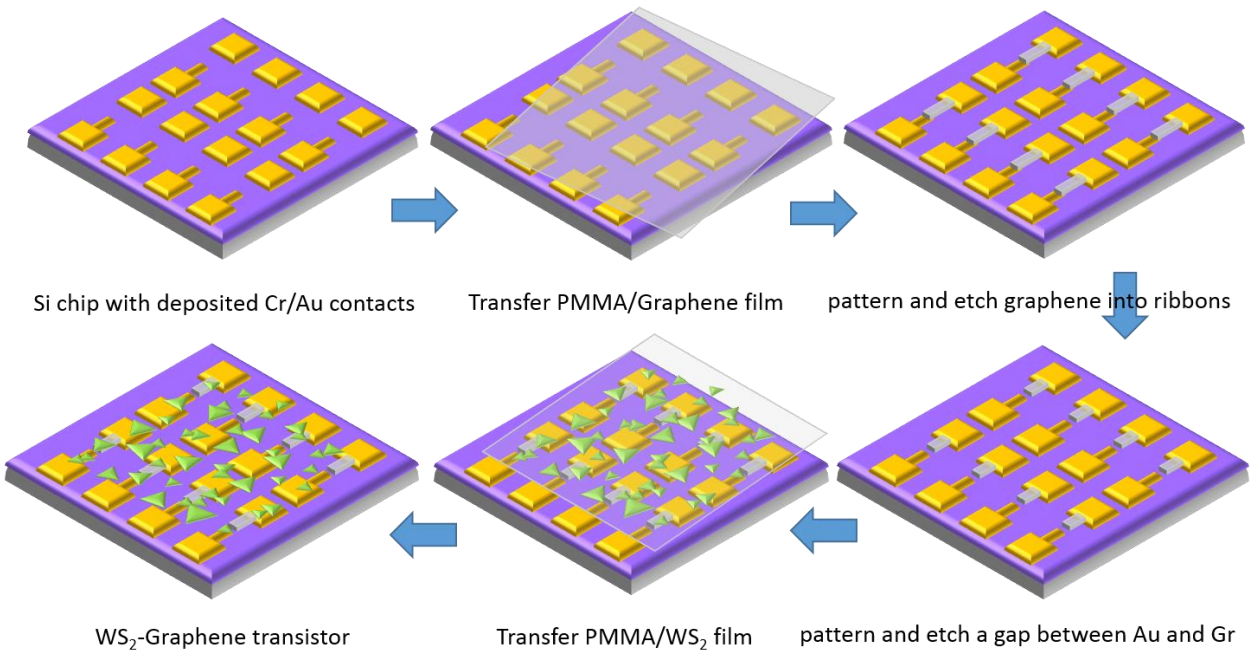


Figure 5.1. **Fabrication and characterization of the WS_2-graphene diode array.** (a) Schematic figure of the fabrication process, which involves 3 steps of e-beam patterning.

The device also has the same features as Au-MoS_2-graphene device with a gap length of 1μm and width of 20 μm. The gap width of 20 μm is designed to match the domain size of CVD-grown MoS_2 and WS_2. The domain size of WS_2 is about 30-60 μm so typically one single domain is sufficient to cover the whole gap. If the gap width is larger than 20 μm, then it cannot be covered by MoS_2 (~10 μm) as suggested in chapter 4. If the gap width is too small, then the device might not be conductive at all and the error of making narrow graphene ribbons is in general very large using maN-2403 as the electron-beam resist. The length of 1μm is determined by two factors: the conductivity of WS_2 and the fabrication difficulty. As discussed in chapter 3, for WS_2 of 20 μm width, it is only conductive when the length is < 5μm. But if the length is too short, like 200 nm, it takes 4 electron-beam (e-beam) lithography sessions to achieve the high fabrication resolution and accuracy, which decreases the success rate and productivity significantly. Using 1μm as length,

the device is still conductive yet only takes three e-beam sessions. The parameters of the graphene-WS_2 device are the same with the parameters of the graphene-MoS_2 device so that their performance is also comparable.

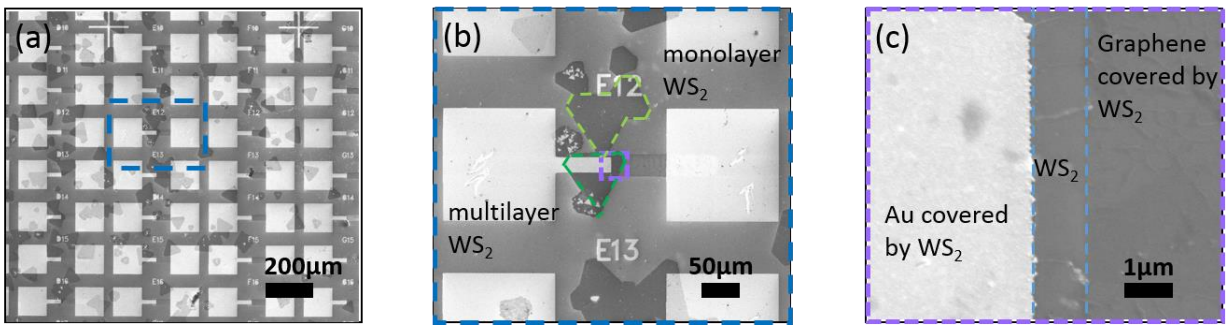


Figure 5.2. **SEM images of the WS_2-graphene diode array.** (a) SEM image of the fabricated diode array. (b) SEM image of a bilayer WS_2-Gr device in the framed region (blue dashed line) in **Figure 5.2a**. (c) SEM image of Au-WS_2-graphene heterostructure with a 1μm gap between Au and graphene in the framed region (purple dashed line) in **Figure 5.2b**.

Figure 5.2 shows the SEM images of as-fabricated devices. It can be seen that CVD-grown WS_2 are domains of random distribution over the chip. It is possible to find devices that both source (Cr/Au) and drain electrodes (Gr) are covered by WS_2 domains, forming a WS_2-Gr lateral heterostructure. Among the 510 devices on the chip, around half of them have graphene ribbons coverage as drain electrodes. With a success rate of 10% for WS_2 covering, around 20 functional devices were obtained. Because WS_2 domains of both monolayer (1L) and bilayer (2L) were synthesized, the process yields around 5 bilayer WS_2–graphene devices and around 15 monolayer WS_2-graphene devices. **Figure 5.2b** shows the SEM image of a device with monolayer WS_2. A closer look at the framed region with a purple line in **Figure 5.2c** shows the channel of 1 μm between metal and graphene. This gap size was optimized in consideration of conductivity of CVD-grown WS_2. As the width of Au and graphene electrodes is 20 μm, the area of the effective

region of the graphene-WS_2 heterostructure is 20 μm × 1 μm = 20 $μm^2$, which is used in optoelectronic properties characterization.

Figure 5.3a and **5.3b** show the schematic illustration of the 3D perspective and side views of the Au-WS_2-Gr-Au device layout.

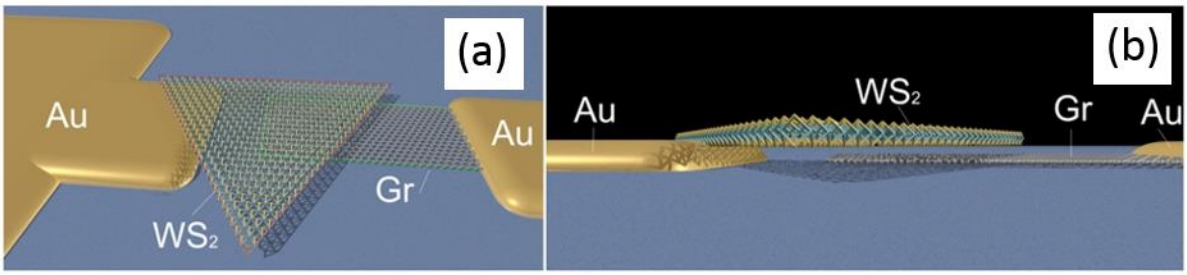


Figure 5.3. **Schematic figures of the device.** (a) Schematic illustration showing a 3D perspective view of the Au-WS_2-graphene-Au device with (b) side view. Figure was made by Prof. Jamie Warner.

5.3 Results and Discussion

5.3.1 Materials Characterization

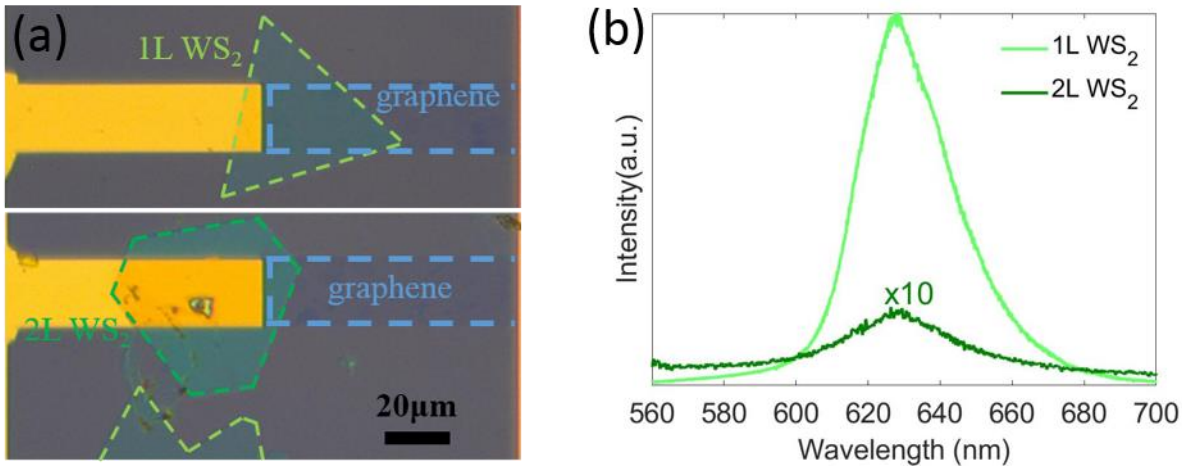


Figure 5.4. Optical images of the device and Raman spectrum of WS_2 domains. (a) Optical microscopy images of 1L WS_2-graphene and 2L WS_2-graphene devices. (b) PL intensity of monolayer WS_2 and bilayer WS_2. Bilayer WS_2 spectrum is multiplied by a factor of 10.

To identify the layer number of the WS_2 domains in the devices, a series of techniques were employed to do it, including the contrast difference of optical image in **Figure 5.4a**, photoluminescence (PL) measurements in **Figure 5.4b**, and Raman spectroscopy in **Figure 5.5b**. The graphene was characterized using Raman spectroscopy to evaluate layer thickness. **Figure 5.4a** shows an optical image of the heterostructure on SiO_2/Si substrate with metal (Cr/Au), monolayer WS_2, and graphene. The domains with the dark green dashed lines is a bilayer, while the ones with the light green dashed lines are monolayer WS_2. The results are consistent with **Figure 5.5a**, a typical optical image of as-grown WS_2 samples of different thicknesses, provided by my colleague Dr. Yuewen Sheng. Usually, the WS_2 domains synthesized have shapes of hexagonal or truncated triangle shapes as previously reported.[3] **Figure 5.4b** shows the PL spectra of both monolayer WS_2 and bilayer WS_2. The signal of bilayer WS_2 is amplified 10 times to show the peak. The peak intensity of monolayer is usually 100 times higher than that of bilayer WS_2 on the samples of both my colleagues and me. The difference can be explained by the change in the band structure. As layer number increases, WS_2 crystals transit from a direct band structure to an indirect band structure, as shown in **Figure 2.18,** Chapter 2 Literature review, thus the signal of the monolayer is much stronger than that of the bilayer. The results are consistent with the previous report.[34]

Figure 5.5 shows the different properties between monolayer and bilayer WS_2. Due to the difference in layer number, monolayer and bilayer WS_2 show different colors under an optical microscope. PL and Raman spectrum are also useful techniques to recognize the layer number of WS_2. For the Raman spectrum, the signal of bilayer WS_2 is higher than that of the monolayer WS_2. The peak positions are also different after peaking fitting. Using multiple Lorentzian distributions,

the curves can be fitted and peak positions were extracted. For monolayer WS_2 the peak positions are at 355.4 and 417.6 cm^{-1} for in-plane (E') and out-of-plane vibration mode (A_1'). For Bilayer WS_2 the corresponding peak positions are at 354.4 and 419.1 cm^{-1} for in-plane (E^1_{2g}) and out-of-plane vibration mode (A_{1g}).

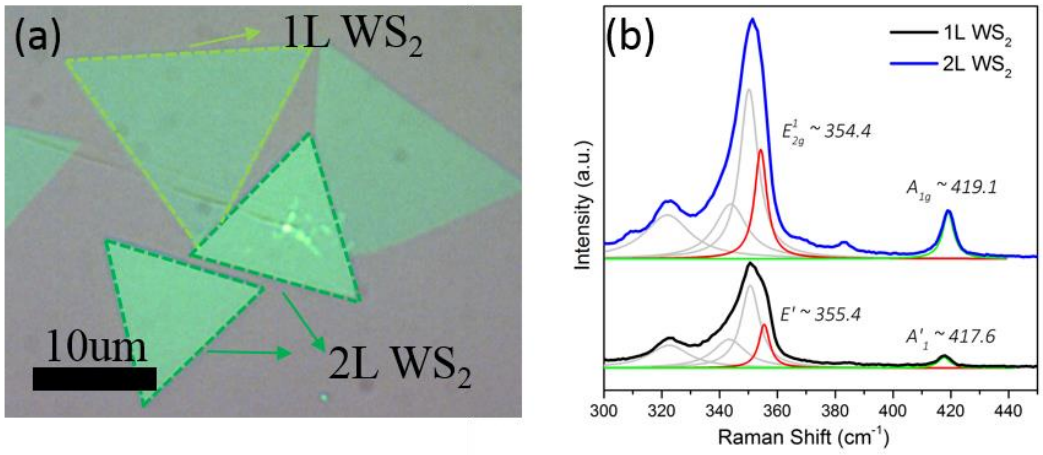


Figure 5.5. Characterization of monolayer and bilayer WS_2. (a) Optical image of monolayer and bilayer WS_2. (b) Raman spectrum and peak fitting of monolayer and bilayer WS_2.

Figure 5.6a shows the spatial map of integrated PL intensity (from 600 to 660 cm^{-1}) of the effective region of 1L WS_2– Gr device in **Figure 5.4a**. It is clear that the signal of WS_2 on gold and graphene electrodes is quenched. This is due to a suppressed recombination process of excitons, as photoexcited electrons in WS_2 can travel to gold or graphene electrodes. The quenching of the PL signal indicates that the Gr/WS_2 and Au/WS_2 contacts are of good quality. The phenomenon is also consistent with previous research on metal-semiconductor interfaces of 2D crystals.[35] This image echoes with the SEM image, which shows a gap of 1 μm between gold and graphene. The Raman spectra of graphene (**Figure 5.6b**) shows a 2D/G peak intensity ratio of around 2, indicating

the graphene used in the devices is mainly monolayer[36]. And a small D peak shows that graphene is of good quality with only a few defects.

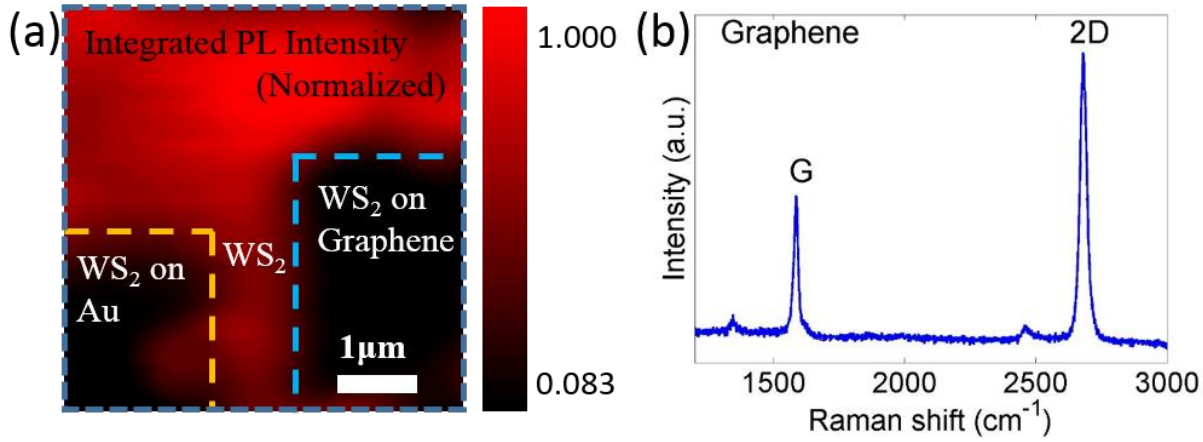


Figure 5.6. Characterization of the device. (a) 2D spatial map of the integrated PL intensity of the region of a 1L WS_2-graphene device. (b) Raman spectrum of graphene used in the heterostructure.

5.3.2 Electronic Properties of the Diodes

For electrical characterization of the fabricated devices, more than 10 devices were measured. Statistics of the dark current of both monolayer WS_2 (5 devices) and bilayer WS_2 (5 devices) is included in **Figure 5.7**. **Figure 5.7** shows statistics on the dark current of both monolayer and bilayer WS_2-Gr diode, under both positive and negative bias. For both types of diodes, the current rectification was observed. For monolayer WS_2-Gr diode, the dark current is around 10^{-11} -10^{-9} A when positively biased and 10^{-12} to 10^{-10} A when negatively biased, showing an on-off ratio of around 10. For bilayer WS_2-Gr diode, the dark current is around 10^{-8} to 10^{-5} A when positively biased and 10^{-11} to 10^{-8} A, showing an on-off ratio of around 10^3. It is worth noting that our measurement limits are around 10^{-11} so the difference of on-off ratio does not necessarily mean

bilayer WS_2-Gr is a better rectifier. Because the off current of monolayer WS_2-Gr diode has already reached the measurement limit.

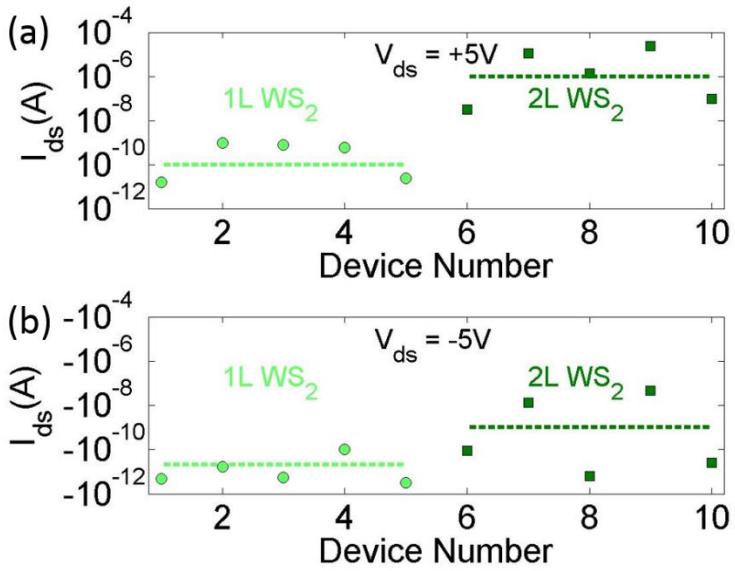


Figure 5.7. Properties statistics on WS_2-graphene heterostructure devices. (a). The dark current of both monolayer and bilayer WS_2 when positive bias V_{ds} = +5V is applied. (b). The dark current of both monolayer and bilayer WS_2 when negative bias V_{ds} = -5V is applied.

Current rectification is observed in the heterostructures based on both monolayer WS_2 and bilayer WS_2 devices, with current only able to pass through the heterostructure when positively biased. The dark current of bilayer WS_2 devices is in general about 2-3 orders larger than that of monolayer WS_2 devices when a positive bias was applied, and 1-2 orders larger when a negative bias was applied. The difference in conductivity of the two devices is discussed later.

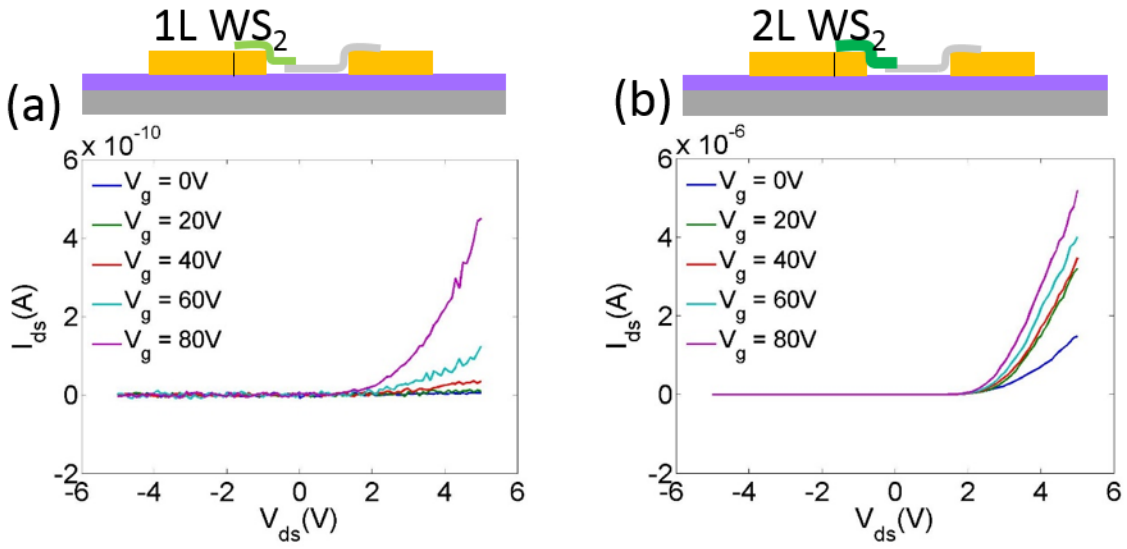


Figure 5.8. Electrical characterization of the WS_2-graphene heterojunction. (a) Gate dependence of the I_{ds}-V_{ds} characteristics of the junction based on monolayer WS_2. (b) Gate dependence of the I_{ds}-V_{ds} characteristics of the heterojunction based on bilayer WS_2.

Figure 5.8a and **Figure 5.8b** show typical electrical properties of monolayer WS_2 and bilayer WS_2 based heterostructures. It was found that the rectifying curves are tunable by an applied back-gate voltage. The dark current under positive bias (on-current) can be increased by an external gate voltage while it has little influence on the negatively biased current (off-current). Similar to MoS_2-graphene heterostructures in chapter 4, the rectification properties can be explained by the asymmetrical Schottky barrier heights formed at Au/WS_2 and WS_2/Graphene interface, shown in band diagram of the heterostructure shown in **Figure 5.9b**. In the figure, the grey dashed line represents the vacuum energy level; Φ_{Metal} and Φ_{Gr} are the work function of metal (Cr/Au) and graphene respectively; $\chi_{Semiconductor}$, E_C and E_V are the electron affnity, conduction band level and valence band level of WS_2. The light green colour represents monolayer WS_2 and the dark green colour represents bilayer WS_2. Φ_{MS} is the Schottky barrier height between metal (Cr/Au) and semiconductor (WS_2) and Φ_{SG} is the Schottky barrier height between graphene and WS_2 . The

work function of Au and graphene are estimated to be 5.1 V and 4.6 V.[37] The electron affinity of monolayer WS_2 (χ_{WS2}) is around 4.0 eV.[30] Asymmetrical Schottky diodes are formed from the difference in graphene and metal contacts to WS_2, as a result of the work function differences. Assuming that both Schottky diodes follow the Schottky-Mott rule[38]: $\Phi_{Schottky\ Barrier} = \Phi_{Metal} - \chi_{TMD}$ (equation 2-2), and graphene is considered as semimetal, the barrier heights of Au-WS_2 is: $\Phi_{MS} = 5.1 - 4.0eV = 1.1eV$ and Gr-WS_2: $\Phi_{SG} = 4.6 - 4.0eV = 0.6eV$. With the increase of layer number, the electron affinity of WS_2 increases and the size of the band gap decreases.[39] Again, it is worth mentioning that 4.6 eV as the work function of graphene is not very accurate for p-doped CVD-grown graphene, as have discussed in chapter 4. A better estimation is 4.8 eV for graphene with V_g = 30V (300 nm SiO_2). In this case, the Schottky barrier height of Gr-WS_2 is $\Phi_{SG} = 4.6 + 0.2 - 4.0eV = 0.8eV$.[37] The value is still smaller than that of Au-WS_2 barrier.

From the band diagram, it can be seen that the conductivity of this diode is subject to thermionic emission effects of carriers across the barriers. When a forward bias is applied, the electrons need to overcome the Gr-WS_2 barrier and thus the conductivity is governed by the height of the Gr-WS_2 barrier Φ_{SG}. But for the reverse bias, the conductivity is governed by an Au-WS_2 barrier Φ_{MS}, which is significantly higher than Φ_{SG} and relatively difficult for electrons to be injected. This results in a much larger current when positively biased than negatively biased as observed. The field effect of both devices is shown in **Figure 5.9a**. The I_{ds}-V_g plot shows that the n-type nature of CVD-grown WS_2 with a threshold voltage of V_{th} around 10 V.

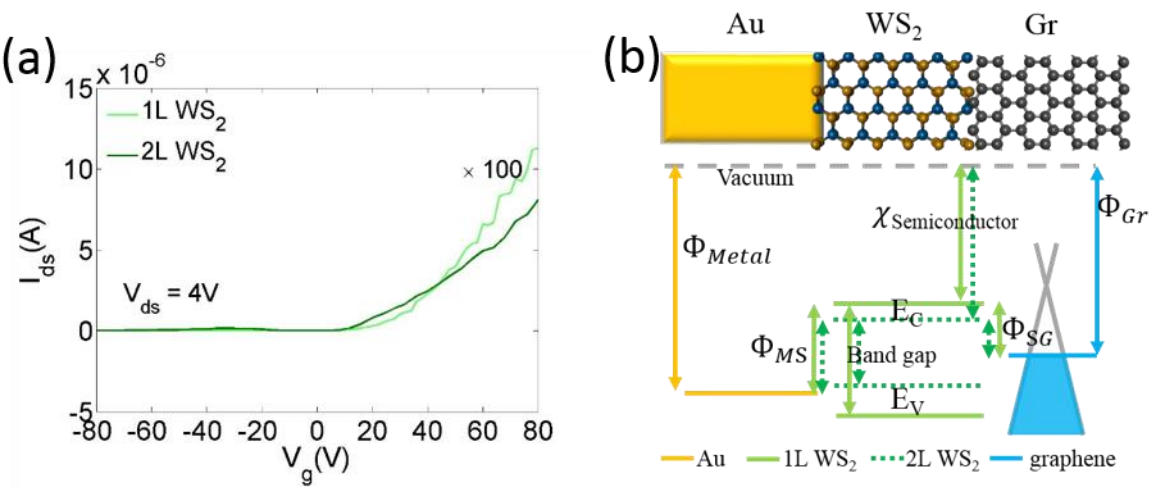


Figure 5.9. Electrical characterization of the WS_2-graphene heterojunction. (a) Field-effect measurements of the heterostructure based on monolayer (light green, enlarged 100 times) and bilayer WS_2 (dark green) at V_{ds} = 4V. (b) Atomic model of the heterostructure and schematic figure of the band structure of the device based on monolayer (light green) and bilayer WS_2 (dark green).

5.3.3 Optoelectronic Properties and the Mechanism

The optoelectronic properties of the heterostructure devices were demonstrated in **Figure 5.10-5.15**.

Figure 5.10a and **5.10b** show the photocurrent versus source-drain bias of monolayer and bilayer WS_2 heterostructure devices, under 532 nm laser excitation with variable power. For both types of devices, the I-V curve is modulated by laser illumination. For the monolayer WS_2 based device, both on-current and off-current is increased significantly by laser irradiation. For example, both on-current (at V_{ds} = 4V) and off-current (at V_{ds} = -4V) are 10^3 higher compared to dark current, under a laser power of 2.7×10^5 mW/cm^2.

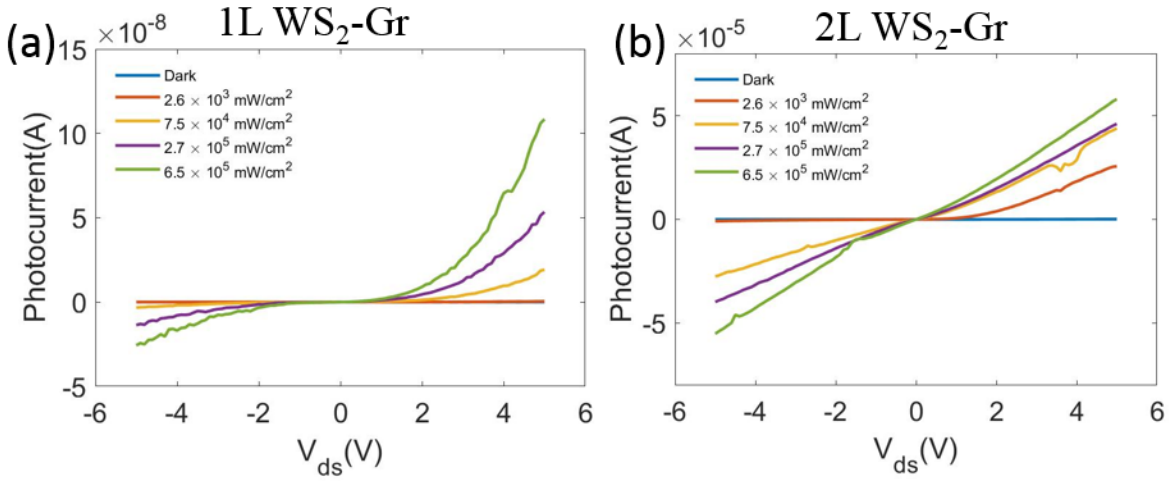


Figure 5.10. Optoelectronic properties of diodes based on both monolayer and bilayer WS_2. (a) The illuminated current of monolayer WS_2 based device. (b) The illuminated current of bilayer WS_2 based device.

A similar result was observed for bilayer WS_2 as well. However, a linear and symmetrical I_{ds}-V_{ds} curve was observed under high illumination power, which is different from monolayer WS_2 based diodes. Under a laser power of 2.7×10^5 mW/cm^2, the on-current (at $V_{ds} = 4$V) is 10^3 higher, but the off-current (at $V_{ds} = -4$V) is 10^6 higher, shown in **Figure 5.11**. This is attributed to different band structures of monolayer and bilayer WS_2, which is discussed later.

Figure 5.12a shows an optical microscope image of an illuminated device under an incident light density of 2.7×10^5 mW/cm^2. As the output property of the diode is highly dependent on laser illumination, the photodetector parameters of photoresponsivity (R), photoconductive gain (G) and specific detectivity (D*) were characterized. **Figure 5.12b** plots the photoresponsivity of both types of devices under an incident light density of 2.7×10^5 mW/cm^2 using equation (2-7) and (2-8).

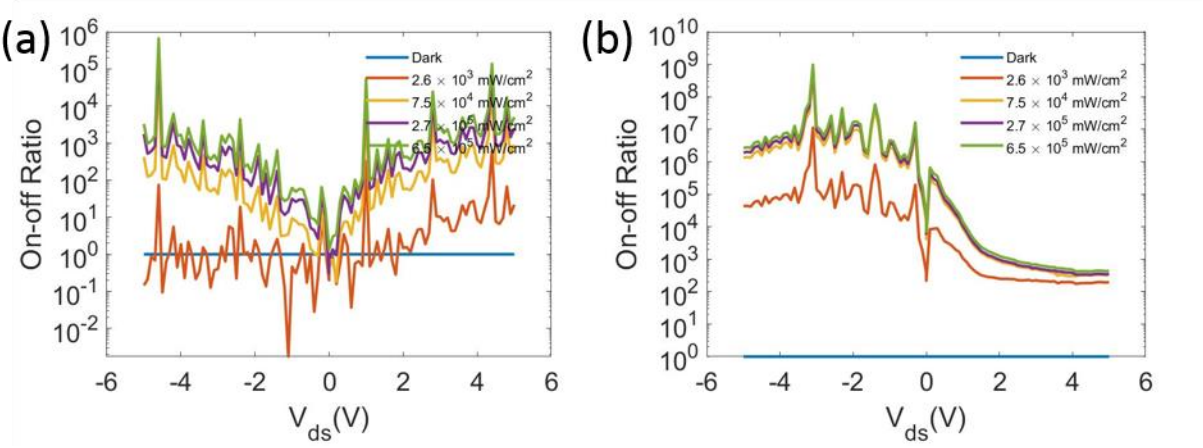


Figure 5.11. On-off ratio of current under illumination versus dark current. (a). Monolayer WS_2–Gr diode. (b). Bilayer WS_2–Gr diode.

The photoresponsivity of bilayer WS_2 based devices is 2 orders higher than that of the monolayer based device, and they also display different tendencies when the source-drain bias is increased. For the monolayer device, a maximum R of 1.0 mAW^{-1} is found when a positive bias (+5V) is applied, while for the bilayer device, a maximum R (absolute value) of 0.74 AW^{-1} is achieved when a negative bias is applied (-5V).

Photoconductive gain (*G*, or photogain) is another helpful metric to compare the performance of devices with different geometry and understand their operating mechanisms. An external photoconductive gain for the monolayer device as G_{ext} = 0.37 and the G_{ext} = 2.8 for bilayer device were obtained using equation (2-9). If further consider the absorbance (~8%) and transmittance (~92%)[40] of each layer of WS_2 under 532 nm (2.33eV) laser irradiation, the estimated internal photoconductive gain of monolayer WS_2-Gr and bilayer WS_2-Gr are 4.6 and 18, using equation (2-10). Using specific detectivity (D^*) obtained by equation (2-12), it is possible to compare the photodetectors' sensitivity. For V_{ds} = -5V, the detectivity of monolayer device is 7.2×10^9 Jones

(Jones = cm $Hz^{1/2}$ W^{-1}) and the specific detectivity of bilayer device is 2.7×10^{11} Jones, which are both comparable to other reports shown in **Table 2.1**, Chapter 2 Literature Review.

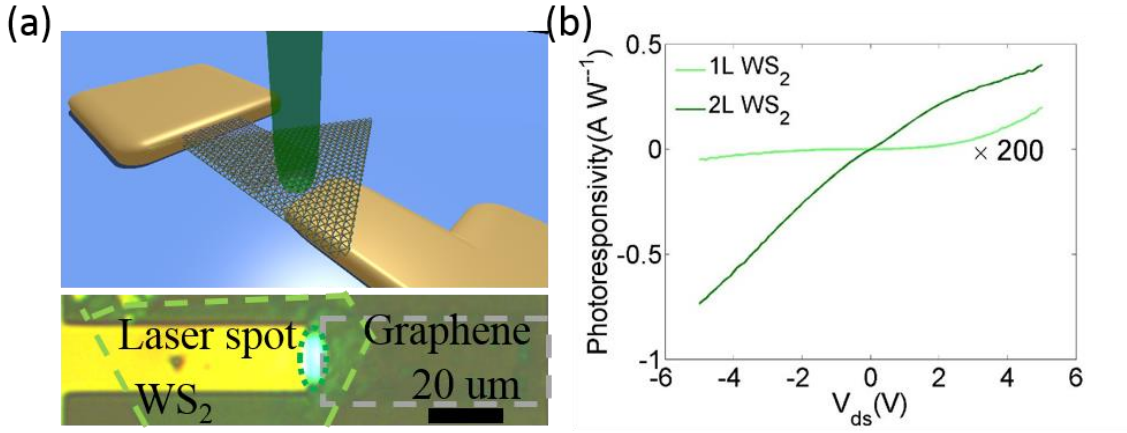


Figure 5.12. Optoelectronic properties of the devices. (a) Optical image of one of the devices under a laser power of 2.6×10^3 mW/cm^2. (b) Photoresponsivity of the two types of detectors under an incident light density of 2.7×10^5 mW/cm^2. The value for monolayer WS_2 is magnified by 200 times.

Figure 5.13a and **Figure 5.13b** show the band diagrams of the WS_2-Gr heterostructure diode under the applied gate and laser irradiation respectively, providing an explanation of the current modulation. As a result of the Dirac cone in the graphene band structure, graphene has a finite density of states (DOS), as shown in **Figure 2.14**, chapter 2. Thus the work function (and Fermi level) of graphene is susceptible to gate voltage modulation and laser irradiation effects, indicating a gate-tunable Schottky barrier. **Figure 5.13a** shows the band diagram of the device before and after applying a gate voltage. A positive gate will lower the work function and raise the Fermi level of graphene electrodes, and lead to a lowering of Φ_{SG} and thus an enlarged on-current. While the barrier height of Au-WS_2, Φ_{MS} is fixed, so the off-current of the diode is not greatly impacted by the gate voltage.

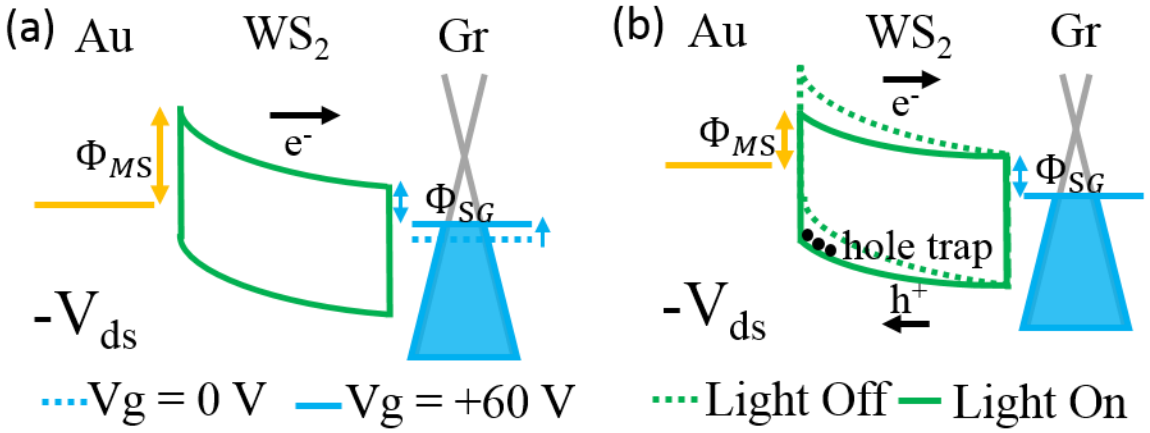


Figure 5.13. Band diagrams of the devices under different conditions. (a) Band schematic of the heterostructure before and after gate voltage applied. (b) Band schematic of heterostructure before and after laser illumination.

Figure 5.13b shows the band diagram of the devices under dark and illumination conditions. Similar to gate potential, laser illumination could also change the barrier height of Gr-WS_2. Under a negative applied bias -V_{ds}, electrons and holes drift in opposite directions. The electrons are collected at the drain electrode, contributing to the photocurrent. But due to the existence of trap states, holes could only accumulate near the metal-WS_2 interface and do not reach the source. These charges lower the Fermi level of the WS_2 and reduce Φ_{MS}. The re-injection of electrons, driven by thermal emission, is facilitated by the lowering of the Schottky barrier, leading to an increased off-current under negative bias. This also explains why a photoconductive gain over unity can be achieved, which is in good agreement with previous work on metal-TMDC-metal photodetectors.[41]

It is worth noting that the holes at WS_2 and Au interface are from two sources. Holes accumulate at the interface when n-doped WS_2 and Au put into contact, because electrons from WS_2 migrate to Au, leaving holes at the interface. And when laser is applied at the interface,

electrons-hole pairs are activated and electrons contribute to the current, while holes are trapped by local states, resulting in the photogating effect. The value of the photoconductive gain also confirms this photoconduction mechanism. For both monolayer and bilayer WS_2 based devices, the internal photoconductive gain is greater than 1, which means more than 1 electrons contribute to the measured current for 1 photon accepted by the device. This is because the photogating effect decreases the Schottky barrier height and increases the carrier concentration.

Figure 5.8 – **Figure 5.15** show different electrical properties of heterostructures based on monolayer WS_2 and bilayer WS_2. First, the dark current of bilayer WS_2 is about 2-3 orders of magnitude higher than in monolayer WS_2. There are several reasons that account for the difference: (i) the bandgap of bilayer WS_2 (around 1.4 eV) is much smaller compared with monolayer WS_2 (around 1.9 eV), as shown in **Figure 2.18** Chapter 2 Literature Review, resulting in a higher carrier concentration in the equilibrium state.[38,42] (ii) The bottom layer within bilayer WS_2 is encapsulated by its top layer and thus the mobility is increased. (iii) As layer number increases, the electron affinity of WS_2 also increases, resulting in a lower Schottky barrier.[39] A smaller Schottky barrier height for 2L-WS_2/Au compared to 1L-WS_2/Au results in higher thermionic emission currents for lower bias values.

The optoelectronic response in these diode devices is also different for monolayer and bilayers of WS_2 respectively. Upon high illumination power, the bilayer WS_2 diode exhibits an I_{ds}-V_{ds} curve that is linear and symmetric, while the monolayer WS_2 diode does not. This implies that Schottky barrier heights of bilayer-WS_2/Au and bilayer-WS_2/Gr are small under sufficient illumination but the barrier height of monolayer WS_2-Au is still considerable. Also, the photoresponsivity of the bilayer WS_2 diode is much higher than that of monolayer WS_2 diode. This is due to bilayer WS_2 having lower Schottky barrier heights and smaller bandgap, higher

absorbance, increased mobility owing to encapsulation effect, and suppressed recombination of electron-hole pairs due to interlayer charge transfer, relative to monolayer WS_2.

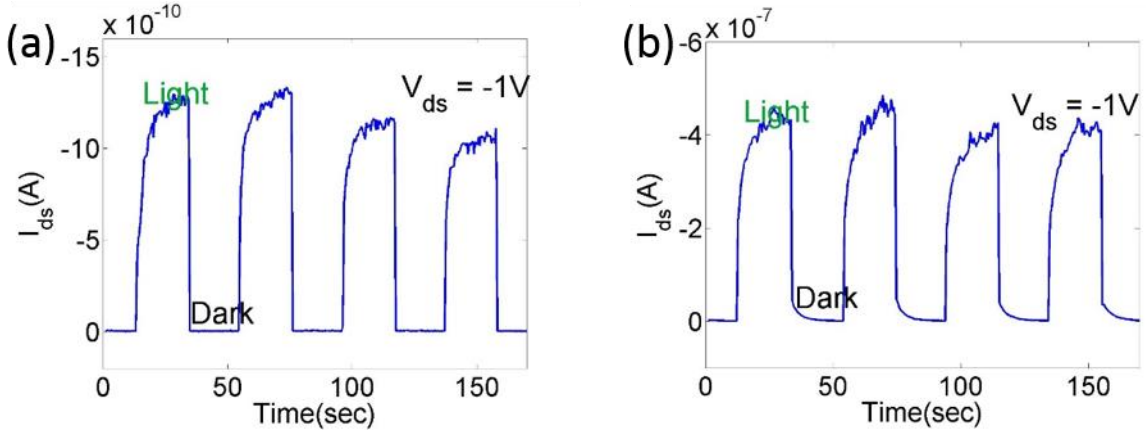


Figure 5.14. Temporal response of the photocurrent generation in the devices. (a) Temporal response of the photocurrent generation of monolayer WS_2 based device, under an incident light density of 2.7×10^5 mW/cm^2. (b) Temporal response of the photocurrent generation of bilayer WS_2 based device, under an incident light density of 2.7×10^5 mW/cm^2. For both types of devices, an on-off ratio over 200 could be achieved.

Since laser irradiation could switch on the off region of the heterostructure, the transient photocurrent characteristics of both monolayer and bilayer WS_2 devices were measured. **Figure 5.14a** shows the laser dependence of monolayer WS_2-graphene heterostructure. The laser was switched on and off repeatedly every 20 seconds, using a laser power of 2.7×10^5 mW/cm^2. **Figure 5.14b** shows the laser dependence of bilayer WS_2-graphene heterostructure. For both types of devices, an on-off ratio (defined as the off-current under illumination versus off-current in the dark) above 200 can be achieved, which is 4 times higher than graphene-WS_2-graphene photodetector.[16] For monolayer diode, the on-current and off-current are about -1.0×10^{-9} A and -5.0×10^{-12} A respectively whereas for bilayer diode, the on-current and off-current are about -4.0×10^{-7} A and -2.0×10^{-9} A respectively. Note that as negative bias was used, all the current measured are

negative as well. The relative large decay time also confirms the existence of trapped charges across the heterostructure channel. Taking on-off ratio, photoresponsivity, and photo gain into consideration, it is suggested that 2L WS_2-Gr diode performs better than 1L WS_2-Gr diode as a photodetector as the photocurrent is larger. The data were also presented in logarithmic scale in **Figure 5.15**.

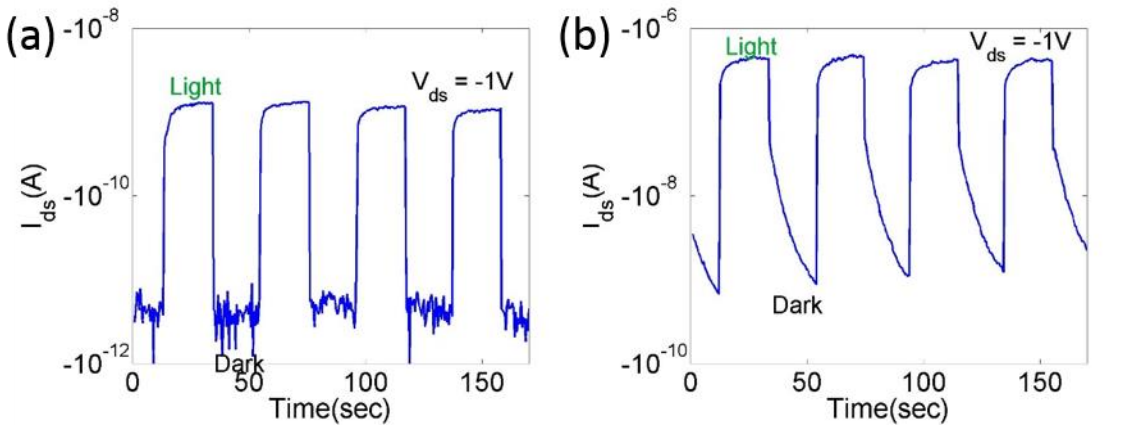


Figure 5.15. The temporal response of photocurrent generation of the devices in logarithmic scale. (a) Device based on monolayer WS_2. (b) Device based on bilayer WS_2. This figure plots the same data as **Figure 5.14.**

Figure 5.15 shows the temporal response of a current generation of the devices in logarithmic scale. The data plotted here are exactly the same with the dataset used in **Figure 5.14**. This figure is to show the on-off ratio of both types of devices is above 200. Though response time (time for the device to be switched on) and recovery time (time for the device to be switched off) of the detectors need to be measured by a more accurate method, the figures also provide some insight. By using the logarithmic scale, it can be seen that for both types of device, the response time for the device to switch on is very short as the current curve is very sharp. This means the long

switching-on process shown in **Figure 5.14** is mainly due to the display scale issue. But when the laser was switched off, it took more time for bilayer devices to recover, which usually indicates a high density of charge traps. Further research needs to be done to reveal the mechanism and details are given in Chapter 7 Future Work.

5.4 Conclusion

To summarize, CVD grown graphene and WS_2 domains were used to fabricate lateral graphene-WS_2 diodes with Au for asymmetric Schottky barrier contacts. Diodes based on both monolayer WS_2 and bilayer WS_2 display obvious rectifying behavior, while bilayer WS_2 devices have higher conductivity. This rectifying behavior can be tuned by the external gate voltage and laser irradiation. Application of an external gate voltage changes the Fermi level of graphene and thus raises the on-current of the diode.

As laser irradiation effectively switches on the off-current when negative source-drain bias is applied, the device can be potentially used as a good photodetector. A high on-off ratio under illumination for both monolayer and bilayer WS_2 based diodes can be achieved. These findings expand our understanding of the properties of lateral heterostructure based on 2D materials and pave ways for large-scale fabrication of high-performance rectifiers, gate electronics and photodetectors using CVD-grown materials.

5.5 Contribution Statements

Dr. Yuewen Sheng provided CVD-grown graphene for this experiment. He also did the spectroscopy (Raman and PL) characterization and provided constructive discussion for the results. Dr. Yingqiu Zhou, Miss Linlin Hou, Miss Qianyang Zhang provided CVD-grown WS_2 for this study. The WS_2 samples in the devices reported here were from Dr. Yingqiu Zhou alone for better consistency and comparability. Prof. Jamie Warner plotted Figure 5.3.

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Chapter 6 Fabrication of Vertical 2D Heterostructures

6.1 Introduction

In chapter 4 and chapter 5 the tunable rectifying behavior of Au-Graphene-TMD lateral devices was studied. Though lateral heterostructures have been intensively studied and show interesting results,[1-6] vertical heterostructure, or Van der Waals heterostructures, are less studied, despite their huge potential in electronic and optoelectronic devices.[7-15] One bottleneck of studying vertical 2D heterostructures is the lack of fabrication techniques

Conventionally, vertical structures can be made using a variety of techniques. For materials growth, using methods like magnetron sputtering,[16] thermal evaporation,[17] e-beam evaporation,[18] and molecular beam epitaxy,[19] one can control the thickness of the materials. For materials patterning, physical etching (plasma etching, reactive etching, etc) and chemical etching (different etchants for different materials) can be used to make complicated structures like Hall Bars. However, the fabrication of 2D vertical heterostructures is more challenging compared to conventional materials, because 2D materials only have a single layer of atoms, making most top-down fabrication methods very difficult to perform. Thus, developing successful fabrication methods for 2D vertical heterostructures is essential to investigate the property of 2D materials. In general, there are three routes to make vertical structures:

Mechanical stacking is the most frequently used method. A scotch tape exfoliation method is employed to isolate the material and then it is pressed gently onto the target substrate. To make a vertical structure of a few layers, one just performs the mechanical stacking repeatedly for each

layer. The main drawback of this method is that the heterostructures are not of standard shapes as each layer is typically exfoliated.

The second method is liquid transfer, similar to the wet transfer of CVD-grown 2D materials.[20,21] PMMA or other supporting layer is used to isolate CVD-grown materials from the original substrate and then the PMMA/2D materials film is transferred onto the target substrate. The main disadvantage of this method is that it is difficult to accurately determine the transfer location and orientation.

The third one is the direct synthesis of heterostructures. Several heterostructures made by direct synthesis have been reported, including graphene on BN,[22] MoS_2 on graphene,[23,24] and MoS_2/WSe_2/graphene[25,] etc. But the challenges of controlling the location, layer number and orientation of heterostructures still remain.

In this chapter, several methods to fabricate vertical heterostructures based on 2D materials have been investigated, including conventional e-beam lithography and patterning, wet transfer of pre-patterned structure, and graphene printing technique. Both the graphene and h-BN used in the experiments were synthesized using CVD method. A graphene-BN-graphene vertical structure was made using the conventional method. Graphene-graphene vertical crossbars were made by transferring a layer of pre-patterned graphene ribbons. A graphene printing technique was developed as a bottom-up method to make vertical 2D heterostructures, the optimal resolution was examined. Properties of graphene transistors made using graphene printing techniques were characterized.

6.2 Results and Discussion

6.2.1 Gr-BN-Gr Vertical Structure

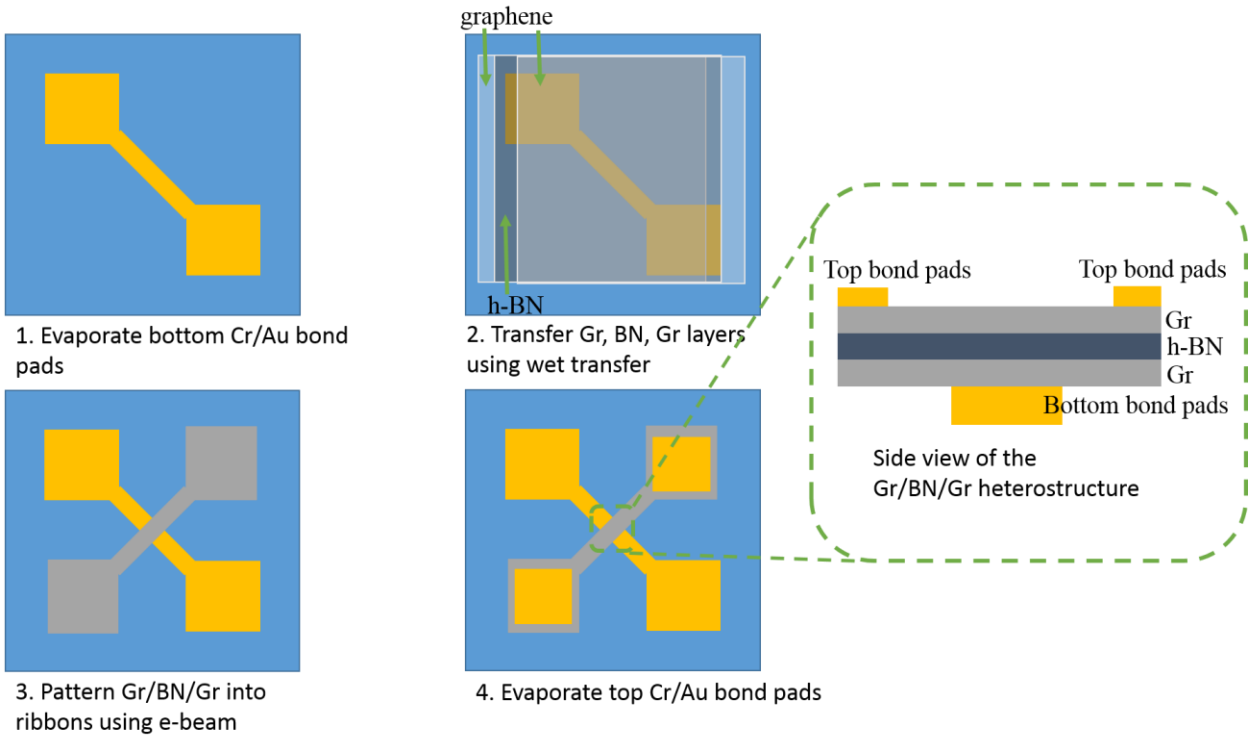


Figure 6.1. Fabrication of graphene/BN/graphene vertical heterostructure and cross-sectional structure of the device.

Tunneling transistors made of exfoliated graphene and BN have been reported.[26] However, to make devices of large quantities, CVD-grown materials are always favorable. A regular electron-beam patterning process was employed to make graphene/BN/graphene vertical structure using CVD-grown materials. The structure was designed to be a crossbar shape with four electrodes, two bottom electrodes, and two top electrodes. I designed the device structure and fabrication process myself and the fabrication process takes four steps:

1. Pattern bottom electrodes using e-beam and deposit Cr/Au bond pads (150um × 150 um).

2. Transfer graphene, BN, and graphene layer continuously using wet transfer method.
3. Pattern the 2D heterostructure into ribbons using e-beam and oxygen plasma.
4. Evaporate top bond pads (75um × 75um) onto the 2D heterostructure.

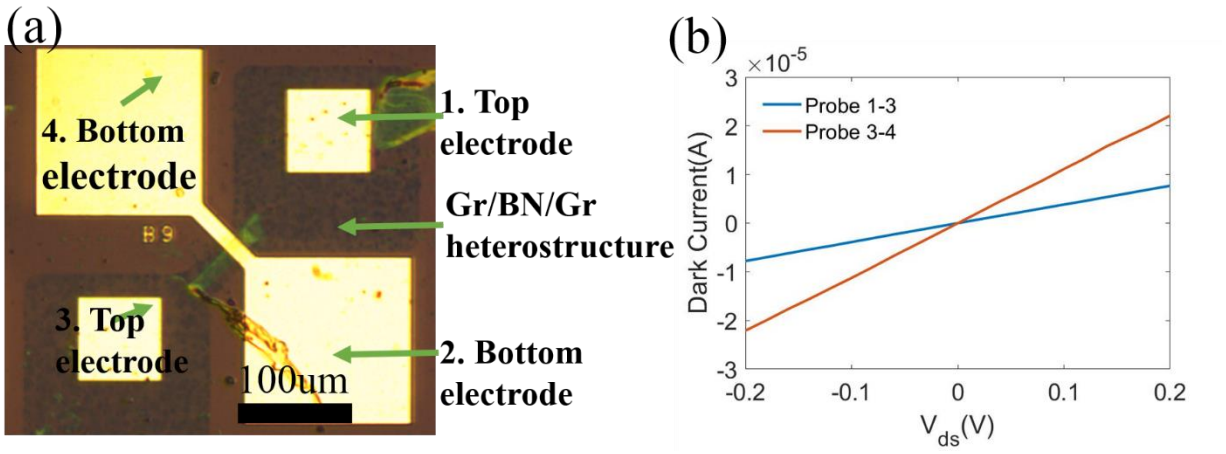


Figure 6.2.Optical image and performance of graphene/BN/graphene vertical heterostructure. (a) Optical image of the finished devices. There are two bottom electrodes (higher left and lower right) and two top electrodes (higher right and lower left). (b) Electronic properties of the heterostructure.

As there are four electrodes on one device, there are several measurements that can be performed: If the first probe was put at lower left (position 3), and the second probe was put at position 2 or 4, the resistance of the vertical heterostructure, as well as half of the graphene ribbon (by graphene ribbon length), can be obtained. If the second probe is put on position 1, then it measures the resistance of the whole graphene ribbon. The resistance of the tunneling barrier using the two measurements above can be derived using the following formulas:

$$R_{13} = R_{graphene\ ribbon} \tag{6-1}$$

$$R_{34} = R_{tunneling\ barrier} + \frac{1}{2}R_{graphene\ ribbon} \tag{6-2}$$

The results are shown in **Figure 6.2b**. It is obvious that the resistance of R_{34} and R_{13} are of the same magnitude, resulting in an insignificant tunneling resistance. Also, the I_{ds}-V_{ds} curve of the vertical structure does not show clear non-linearity, indicating the invalidity of the tunneling transistor. Several factors may contribute to such a result:

1. The transferred BN film is not continuous and may have cracks in it. The defects are inevitably introduced after wet transfer and the device is short-circuited.
2. The thickness (layer number) of h-BN is not enough to form a tunneling barrier, because only a single layer of BN was transferred. Carriers can easily tunnel through the barrier, and will not give rise to the resistance.
3. When putting the probes onto the top electrodes, it may puncture through the electrodes and reach the bottom graphene. This will make the vertical tunneling device short-circuited.

Following experiments could be done to examine the possibilities discussed above:

1. It is very challenging to examine how continuous a BN film is. Even if there is a crack in BN film, it might not be visible under SEM. However, two different tunneling devices can be made and characterized. In the first one, one layer of thick BN film is transferred and in the second one, a few layers of thin BN films are transferred. Assuming that cracks in each layer are independent, the tunneling resistance of the second device should be higher than the first one. This is because the possibility of cracks of different BN layers overlapping each other is small. If the two measured resistance values are comparable to each other. It suggests that the BN may have no crack at all or have too many cracks that both devices are short-circuited. If the BN has no cracks at all, the tunneling resistance should increase when thicker BN is used. And if BN has too many cracks, the tunneling

resistance will not change a lot when thicker BN was used because it is still short-circuited.

2. To examine the impact of BN thickness, devices of increasing BN thickness can be made. BN films of different thickness can be obtained using different synthesis times. After that, the tunneling resistance of the devices can be measured. If the resistance increases when thicker BN film was used, then it is safe to claim that BN thickness has a strong impact on the tunneling resistance. If all the devices show comparable resistance, then BN thickness is not the primary factor.
3. If the previous experiments cannot improve the device performance, it is likely that the device is short-circuited by the probes. It is better to redesign the device structure and make sure no conductive materials are under the top electrodes.

Though it is possible to improve the device performance, the fabrication method is fundamentally flawed as it only works for certain types of structures. For structures like graphene-WS_2-graphene crossbar, it is impossible to pattern the top graphene without damaging the bottom graphene using conventional ion etching technique. In brief, other methods need to be explored in order to find a more universal fabrication method.

6.2.2 Gr-Gr Vertical Structure

Transfer of pre-patterned 2D materials is another method to tackle the problem. The idea of this method is simply to pattern each layer into the desired shape and then stack them up using wet transfer. For example, the detailed process of making graphene/graphene vertical crossbar is shown in **Figure 6.3a**.

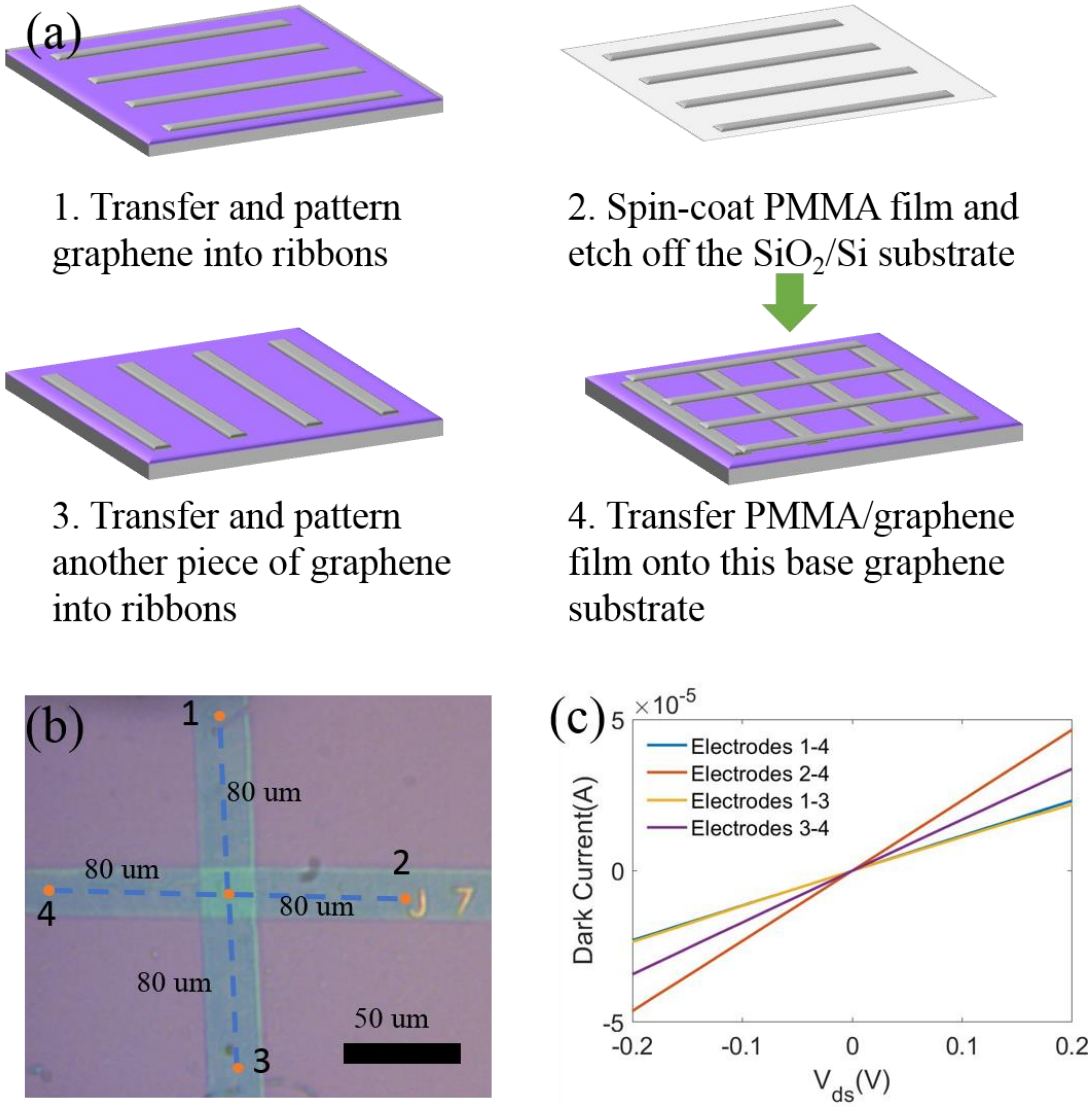


Figure 6.3 Wet transfer of pre-patterned graphene ribbons. (a) Schematic of the wet transfer process. (b) Optical image of one graphene/graphene crossbar. (c) Electronic properties of the graphene/graphene crossbar.

The detailed fabrication process is:

1. For the base chip, evaporate P, and Q marks (Cr/Au) using e-beam and thermal evaporation for future alignment, if deposition of electrodes is wanted.
2. Transfer a layer of graphene onto the base chip and pattern it into ribbons.

3. For the second chip, transfer another layer of graphene and pattern it into ribbons. Scratch off a corner of the chip to indicate the orientation of the ribbons.
4. Spin-coat a layer of PMMA supporting film and then etch off the SiO_2/Si substrate using KOH. The recipe is the same as the substrate etching for wet transfer of MoS_2/WS_2 on SiO_2/Si.
5. Transfer the pre-patterned film onto the graphene ribbons prepared in step 2. To make sure the two sets of ribbons are perpendicular with each other, the missing corner of the PMMA/graphene ribbons can be used to align with the bottom chip.
6. Evaporate gold bond pads onto the graphene ribbons. The bond pads can be aligned using the deposited P, and Q marks in step 1.

One of the fabricated crossbars is shown in **Figure 6.3b**. To characterize the property of the junction, I marked 4 positions, each of them is 80 μm from the center of the junction. When two probes were put onto the same ribbon, the resistance of the ribbon can be measured. When the two probes are put onto different ribbons, the resistance measured is from graphene ribbons as well as the junction. A typical result is shown in **Figure 6.3c**.

Statistics of the results of 15 crossbars is presented in **Figure 6.4**. It can be seen that the resistance of R_{14} and R_{34} are not significantly different from R_{24}, which is the top graphene ribbon. This means that the top layer graphene and bottom layer graphene are in good contact so the resistance of the interface is not significant.

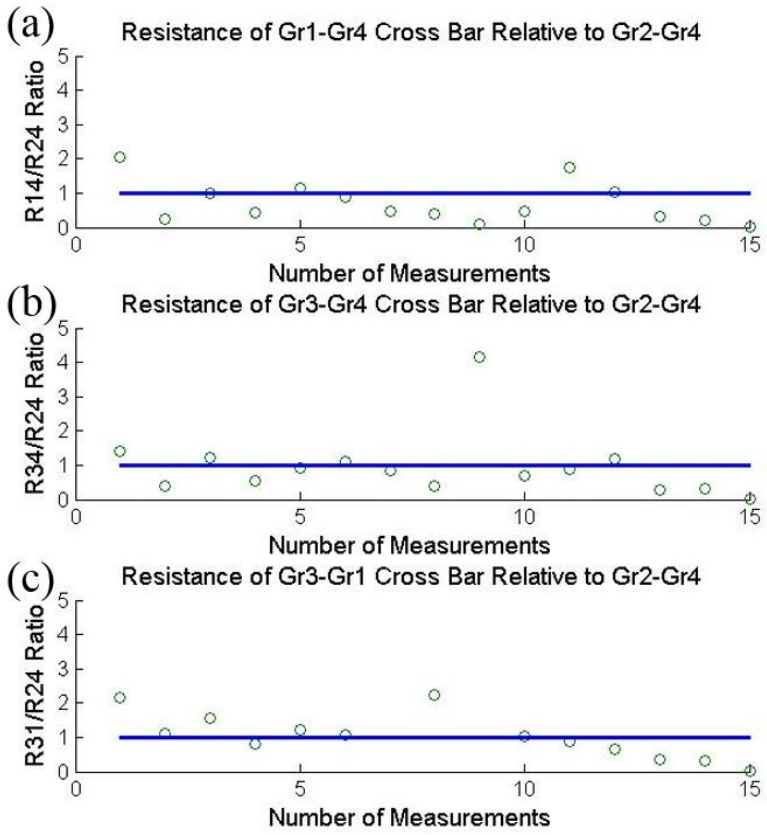


Figure 6.4 Statistics of electronic properties of 15 graphene/graphene crossbars. (a) Relative resistance of R_{14} versus R_{24}. (b) Relative resistance of R_{34} versus R_{24}. (c) Relative resistance of R_{13} versus R_{24}.

The advantages and disadvantages of this fabrication method are quite obvious: this method only requires some practice and is easy to perform. It also compatible with conventional fabrication method thus no additional facility is required. But it only has limited control of the alignment of 2D materials between layers. Two ribbons roughly perpendicular to each other can be achieved, with an error within 15 degrees. Also, chemical dopants will be introduced into the structure. With careful operation, some types of heterostructure could be made using this method, such as graphene-WS_2-MoS_2-graphene.[27] The paper was published by my colleague Dr. Yingqiu Zhou and I was also co-authored.

6.2.3 Graphene Printing Technique

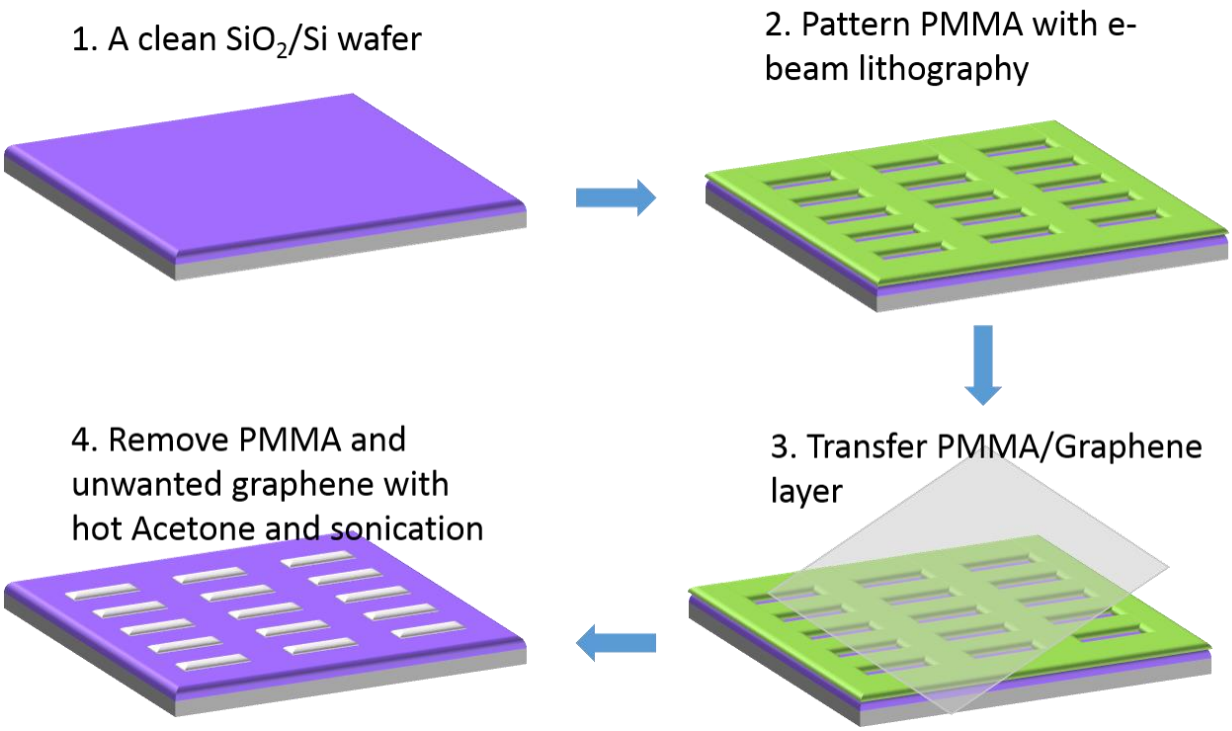


Figure 6.5 Schematic figures of graphene printing technique by steps. Blue: SiO2 layer. Green: Spincoated PMMA on top of the substrate. Transparent grey: PMMA/graphene film.

The process of graphene printing is shown in **Figure 6.5**. The idea originates from the deposition of metal electrodes, but instead of evaporating metal onto the window defined by e-beam resist, a layer of PMMA/graphene film was transferred on it. The first step was spin-coating PMMA and defines the resist into favored shapes. Then a layer of PMMA/film was transferred on top of the pre-defined chip. The removal of PMMA film and excess graphene is the key of this printing technique. The sample was baked at 80 °C for 2 hours to enhance the bonding between graphene and Si substrate. Then the sample was baked at 180 °C for 15 minutes, followed by 2 hours bathing in acetone at 45 °C.

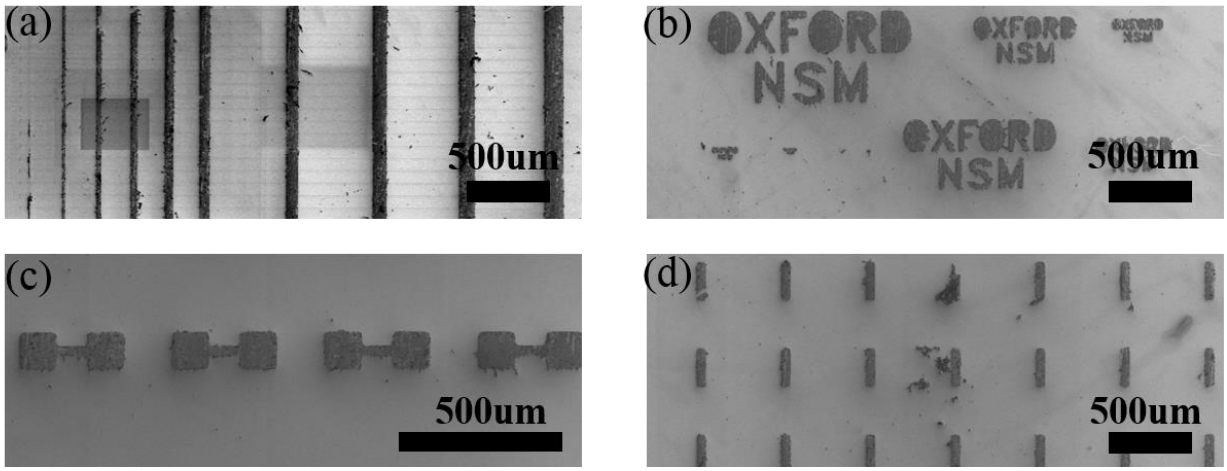


Figure 6.6 SEM images of printed graphene patterns on Si substrate. (a) Printed graphene ribbons of various widths. (b). Printed graphene alphabets of various sizes. (c) Printed graphene barbell. (d) Printed graphene short ribbons.

This printing technique allows me to print various shapes at different sizes. The finest resolution achieved is 10 μm, as shown in **Figure 6.6a**, where graphene ribbons of different widths have been designed and tested. The resolution of the technique is comparable to photolithography. Other shapes have also been tested by myself including square, round, barbell, short ribbon, and alphabets. The mechanism of this printing technique is easy to explain: PMMA/graphene film transferred onto the substrate is stretched out during drying and baking. The tension is ls large enough that graphene film breaks down along the edge of graphene domains, where the mechanical strength is the weakest.

Several tricks are found to improve the quality of graphene ribbons after transfer:

1. Use diluted e-beam resist and a faster spin rate during spin-coating so that the PMMA layer is thinner.
2. Gently sonicate the sample for 1s before remove PMMA will help clean the edge of graphene

ribbon. However, longer sonication totally removes the graphene ribbon from the substrate, so it is not recommended.

6.2.4 Graphene Transistors Fabricated by Graphene Printing

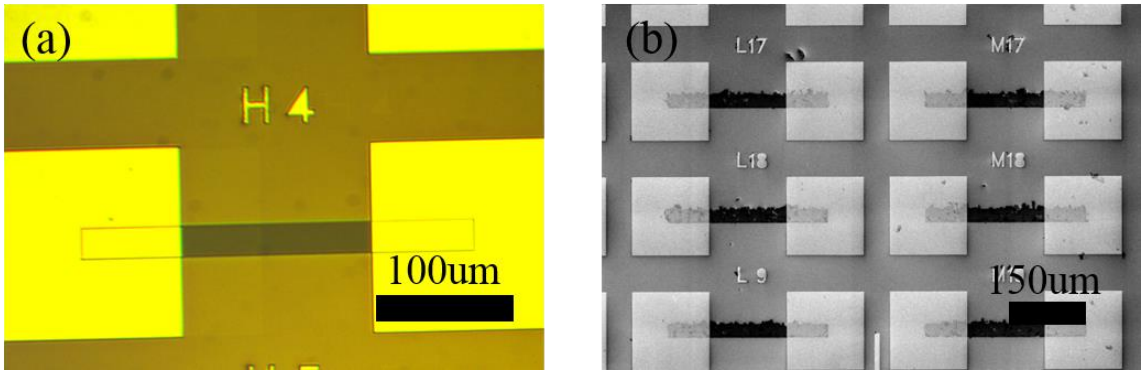


Figure 6.7 Images of graphene transistors made using graphene printing technique. (a) Pre-defined substrate covered by PMMA resist. Graphene will be left onto the exposed area. (b) SEM images of the device arrays.

To test the validity of this technique in device fabrication, this method was used in to make graphene lateral transistors, shown in **Figure 6.7**. The conventional way of making graphene transistor is to pattern a graphene ribbon with negative resist and etch off the unfavorable part using oxygen plasma. However, for this device, the fabrication process is slightly different. First, Cr/Au bond pads are evaporated. Then the shape of the graphene ribbon is defined by e-beam lithography, as shown in **Figure 6.7a**, after which a layer of graphene is transferred on top of it. After the removal of unfavored graphene. An SEM image of the device array is given in **Figure 6.7b**. The width of the graphene ribbon is designed to be 20μm. The device is ready to test.

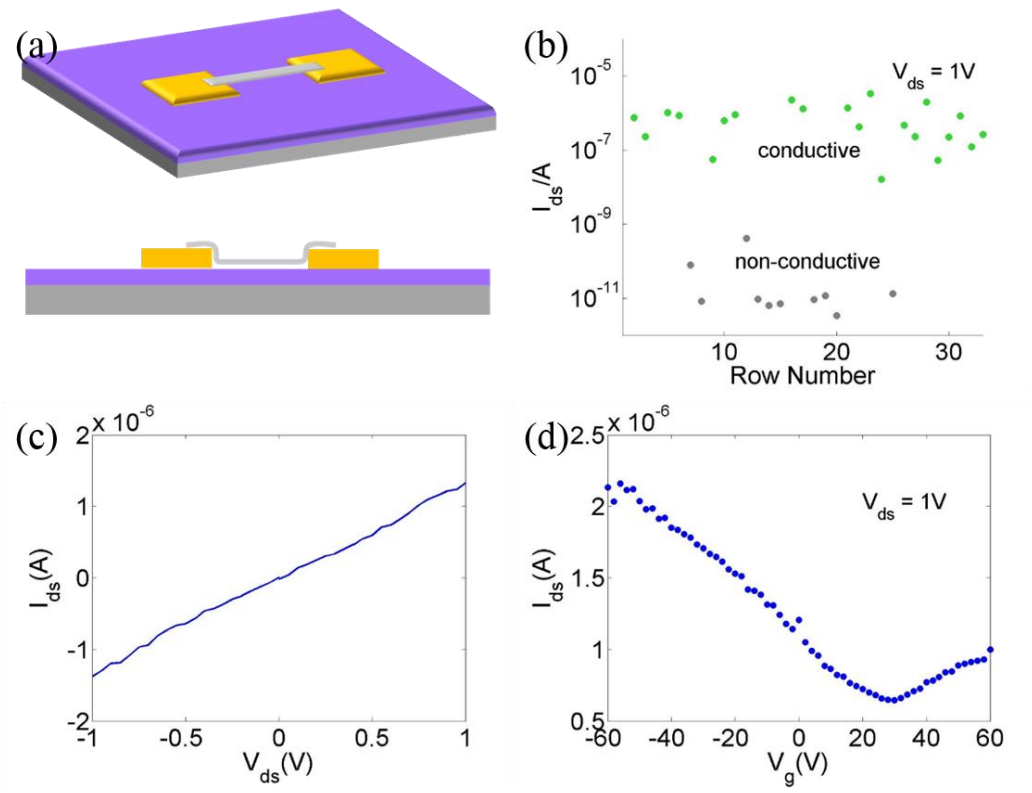


Figure 6.8 Properties of graphene transistors made using graphene printing technique. (a) Schematic figure of the transistor structure. (b) Statistics of 33 graphene transistors in a column. (c) A typical I_{ds}-V_{ds} curve of a graphene transistor. (d) Field-effect of graphene transistors showing the Dirac point of about 30V.

A schematic of the device structure is shown in **Figure 6.8a**. There are about 500 fabricated devices on one chip and to obtain an overall evaluation of the method, I tested a column of devices, including 33 devices. And the result is shown in **Figure 6.8b**. When a bias is applied, the drain-source current (y-axis) is measured and plotted according to the device number (x-axis). The y-axis is in logarithmic scale and a distinct divide between conductive states (current ranges from 10^{-8} to 10^{-6} A) and a non-conductive state (10^{-11} to 10^{-9} A) can be seen. Among all 33 devices, 19 of them were conductive, giving a yield rate of over 57%. This is comparable with the conventional fabrication method. A typical I_{ds}-V_{ds} curve is shown in **Figure 6.8c**. The device

displays good linearity, indicating good contact between graphene and bottom Au electrodes. The field effect of the device is shown in **Figure 6.8d**. The Dirac point of the device is around 30 V, which means it is p-doped, similar to conventional fabricated graphene transistors.[28] Dopants could be introduced from chemicals during copper etching and graphene printing or could be from the substrate and ambient environment.

The fabrication and characterization of the transistor array proved that this technique can be used in device fabrication and the printed graphene is of good quality. I have not tested if this printing technique can also be applied to other 2D materials, such as MoS_2, WS_2, and, BN due to practical issues: Because CVD synthesized MoS_2 and WS_2 are domains instead of continuous films and BN film are relatively difficult to characterize after printing. However, this technique is promising to apply to other continuous 2D films as the mechanical strength of graphene is stronger than other 2D materials. My colleagues Yang Lu has made some progress in making continuous WS_2 film. If time allows, I would like to make graphene-WS_2-graphene tunneling transistors and graphene-BN-WS_2-BN-graphene LEDs using this printing technique.

6.3 Conclusion

To make vertical heterostructures based on graphene and other 2D materials, a series of techniques were developed and verified. The graphene/BN/graphene vertical structure was made using a conventional fabrication method. No significant tunneling resistance was measured which might result from following reasons: a single layer of BN can be tunneled through easily; BN layer can be damaged after the wet transfer; the metal probe might puncture through the whole electrodes and short-circuit the structure. The direct transfer of pre-patterned graphene is a

useful method to make vertical heterostructure. Though lack of precise alignment, certain types of structures can be made and tested, such as graphene/graphene, graphene/WS_2/graphene. The resistance of the interface is insignificant, indicating good contact between the top and bottom graphene ribbons. However, for complex structures, alignment of different layers is usually required which may impair the yield rate. Also, chemical dopants and contamination can be brought onto the whole substrate after each transfer. Graphene printing is a bottom-up technique that could potentially tackle the alignment problem. A patterning resolution of about 10 um can be achieved, and various shapes and sizes of graphene can be printed onto the substrate. Graphene transistors were made using this method and show good yield rate, and conductivity. The limitation of the method is that it is not applicable to 2D materials that do not form large continuous films.

6.4 Contribution Statements

Dr. Aaron Chit Siong Lau and Dr. Haijie Tan participated in the project discussion. Dr. Martin Tweedie provided important insight on the printing process. Dr. Yuewen Sheng provided the graphene used in the devices. Dr. Xiaochen Wang provided CVD-grown BN.

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Chapter 7 Conclusions and Future Outlook

In this final chapter, the results of the research and their implications are briefly summarized. Future studies are proposed to address the unanswered questions in previous sections.

7.1 Thesis Summary

In chapter 4, the electronic and optoelectronic properties of three types of heterostructure based on CVD-grown MoS_2 and graphene were demonstrated. Rectification was found in nearly all 44 Au-MoS_2-graphene devices. The rectifying behavior is due to asymmetrical Schottky barriers of Au-MoS_2 and MoS_2-graphene, which can be tuned by both external gating and laser irradiation. By extracting the effective Schottky barriers the symmetrical devices, it was found that the Au-MoS_2 barrier height drops quickly under irradiation, which explains the decrease of rectification ratio. This work shows that graphene-MoS_2 heterostructures display a significant rectification and can be a potential structure for novel gate logics and rectifiers.

Further to chapter 4, the electronic and optoelectronic properties of Au-WS_2-graphene heterostructure were studied in chapter 5, with a focus on their layer-dependent performance. Both monolayer and bilayer WS_2-graphene heterostructures were manufactured and rectification was found in both types of devices. The rectifying behavior can also be modulated by the external gate voltage and laser irradiation. Especially the off-state (when negatively biased) can be switched on by laser exposure. For both types of devices, an on-off ratio of 200 can be achieved under a laser intensity of 2.7×10^5 mW/cm^2. The improved conductivity and

photoresponsivity of bilayer device compared to monolayer device results from the difference of electron affinities and bandgaps. The results show graphene-WS_2 heterostructure is a promising candidate for ultrathin photodetectors.

After thoroughly studying the lateral heterostructures based on graphene and TMD, the investigation to make vertical heterostructures were illustrated in chapter 6. A few techniques were proposed and tested, including conventional e-beam fabrication, wet-transfer of pre-patterned graphene, and graphene printing technique. Graphene-BN-graphene and graphene-graphene vertical structures were made and the insignificant tunneling resistance shows good contact between different 2D layers. Graphene lateral transistors were made using graphene printing technique, with a yield rate over 57%. This work provides researchers with another way to realize complex vertical heterostructures based on 2D materials.

In brief, the results of this thesis can be summarized into three parts: 1) investigation the tunable rectification in Au-MoS_2-graphene structure and its mechanism; 2) study of the layer dependence of the rectifying behavior in Au-WS_2-graphene heterostructure and its potential application as photodetectors; 3) exploration of the techniques to fabricate vertical 2D heterostructures and developed graphene printing for graphene-based devices.

7.2 Future Work

As discussed in previous chapters, there are several questions remain unanswered including the effectiveness of external gating, the slow recovery time of Au-WS_2-Gr photodetector, and the applicability of graphene printing technique. Several experiments can be done in future to address the issues.

The MoS_2 and WS_2 devices demonstrated in chapter 4 and chapter 5 are all essentially back-gate field-effect transistors where MoS_2 and WS_2 layers are transferred on top of metal electrodes. The air gap between 2D materials and substrate may potentially make the external gating ineffective, as the complex capacitance may decrease substantially. To rule out the influence of the air gap, the device structure can be optimized by evaporating metal electrodes after 2D materials are transferred. By measuring how external gating affect the device performance, the mechanism of the tunable rectifying behavior displayed in chapter 4 can be verified.

In chapter 5, it was mentioned that the recovery time of bilayer WS_2-graphene photodetector is larger than that of monolayer WS_2-graphene device. But the consistency and the mechanism of the results remain unclear. More devices need to be fabricated and characterized to prove the difference between monolayer and bilayer WS_2 is substantial. The long recovery time is usually related to defect induced trap states. To examine the mechanism, devices based on CVD-grown WS_2 and exfoliated WS_2 can be fabricated and compared. Exfoliated WS_2 are considered near pristine and free of defects so theoretically photodetectors based on exfoliated WS_2 should have a much faster recovery compared to CVD-grown WS_2. If the two show similar response and recovery time, then it can be concluded that the defects and trap states are from the fabrication process rather than 2D materials.

Chapter 6 studies the printing technique to make graphene-based devices. Yet it is still unknown whether the technique can be applied to other 2D materials such as MoS_2, WS_2, and h-BN. To make it a universal method for complicated 2D devices fabrication, continuous MoS_2, WS_2, and h-BN film need to be synthesized and transferred using the printing technique. Based

on that, vertical heterostructures such as Gr-WS_2-Gr and Gr-BN-WS_2-BN-Gr can be approached using the printing technique.

Appendix A Matlab Code for Schottky Barrier Fitting

```
% clear;
%close all;

Vgate=[0,10,20,30,40];        %input measured laser current
% laser_power=[2.53e3,1.27e4,6e4,1.4e5,2.4e5];
% input power meter number(uW)
% tier=size(laser_current,2);  %tier numbers of laser power

w=1e-6  %contact width of metal & semiconductor

Isd_fit=[];

% a={'dark'};
% file='dark.txt';
% d=importdata(file,' ',6);
Vsd=v0(11:32,1);
Isd1=i0(22:32,1);
Isd2=flipud(abs(Isd1));
Isd=vertcat(Isd2,Isd1);
Isd_fit=horzcat(Isd_fit,Isd);

% for i=2:tier+1
%     %a{i}=strcat(num2str(laser_current(i-1)),'.txt');
%     %file=a{i};
%     %d=importdata(file,' ',6);
%     Isd1=d.data(128:138,2);
%     Isd2=flipud(abs(Isd1));
%     Isd=vertcat(Isd2,Isd1);
%     Isd_fit=horzcat(Isd_fit,Isd);
% end
Isd1=i10(22:32,1);
Isd2=flipud(abs(Isd1));
Isd=vertcat(Isd2,Isd1);
Isd_fit=horzcat(Isd_fit,Isd);

Isd1=i20(22:32,1);
Isd2=flipud(abs(Isd1));
Isd=vertcat(Isd2,Isd1);
Isd_fit=horzcat(Isd_fit,Isd);
```

```
Isd1=i30(22:32,1);
Isd2=flipud(abs(Isd1));
Isd=vertcat(Isd2,Isd1);
Isd_fit=horzcat(Isd_fit,Isd);

Isd1=i40(22:32,1);
Isd2=flipud(abs(Isd1));
Isd=vertcat(Isd2,Isd1);
Isd_fit=horzcat(Isd_fit,Isd);

%A = 0.114; %2D equivalent of Richardson constant in yale
thesis
A=0.026

C1 = log(A*w*300^1.5); %(A*width*T^3/2)

%P(1) is epsilon_sb (eV), P(2) is 1/n, P(3) is R (ohms)
F = @(P,M) exp(C1-P(1)*38.5)*cosh((0.5-
0.5*P(2))*38.5*(M(:,1)-M(:,2)*P(3))).^(P(2)-
1).*sinh(0.5*38.5*(M(:,1)-
M(:,2)*P(3))./cosh(0.5*P(2)*38.5*(M(:,1)-
M(:,2)*P(3))).^P(2);
P_0 = [0.5, 0.98, 1000];
results = [];

for j = 1:5
    options = optimset('TolFun', 1E-20, 'TolX', 1E-20,
'MaxFunEvals', 4000, 'MaxIter', 2000);

    P1 = lsqcurvefit(F, P_0, [Vsd, Isd_fit(:,j)],
Isd_fit(:,j),  [0, 0.7, 0], [1.5, 1, 2000], options);
    results = [results;P1];
    figure();
    plot(Vsd, Isd_fit(:,j), Vsd, F(P1, [Vsd,Isd_fit(:,j)]))
end

x_axis=Vgate;
figure();
SB_results=horzcat(x_axis',results(:,1));
plot(x_axis,results(:,1),'o')

dlmwrite('SB_results.txt',SB_results);

save('data.mat')
```