High-Speed Pulse Generator for Electric Discharge Machining Using Gallium Nitride Transistors and Constant On-Time Control

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***Abstract*—This paper presents a high-speed pulse generator for electrical discharge machining (EDM), leveraging the high-speed switching capabilities of Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) to enhance pulse regulation. The proposed system employs a Transient-Enhanced Constant On-Time (TE-COT) control scheme to regulate the discharge current. Experimental validation at a discharge current of $10\,\mathrm{A}$ demonstrates a rise time of $645\,\mathrm{ns}$, a current ripple of $1.47\,\mathrm{A}$, and a high efficiency (92.6%) at a steady-state switching frequency of $2.5\,\mathrm{MHz}$. The adoption of GaN HEMTs enables an improved dynamic response without compromising current regulation. These results highlight the potential of GaN-based pulse generators for next-generation EDM systems.**

***Index Terms*—Power supply, electrical discharge machining (EDM), GaN transistors, constant on-time (COT) control, transient improvement**

I. Introduction

Electric discharge machining (EDM) is a non-contact manufacturing process that uses electric discharge energy to achieve precision material removal. This technology is particularly effective for electrically conductive materials, including those that are challenging to machine using conventional methods, such as titanium alloys and hardened steels. It also excels in creating complex and delicate geometries, as the reaction force generated is relatively insignificant [1].

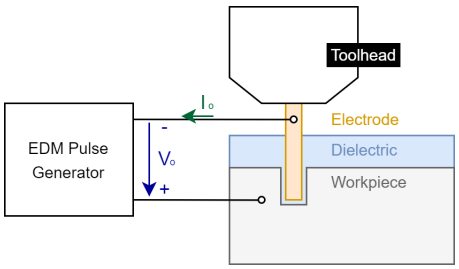

Fig. 1. Overview of an EDM system setup highlighting the role of EPG. The polarity of the EPG depends on the type of EDM process.

The electric discharge occurs in the gap between the electrode and the workpiece, which is typically filled with a dielectric fluid to facilitate controlled sparking and material removal [1]. The EDM Pulse Generator (EPG) is the core component of an EDM system (see Fig. 1), responsible for generating and controlling discharge pulses to ensure efficient and precise machining [2].

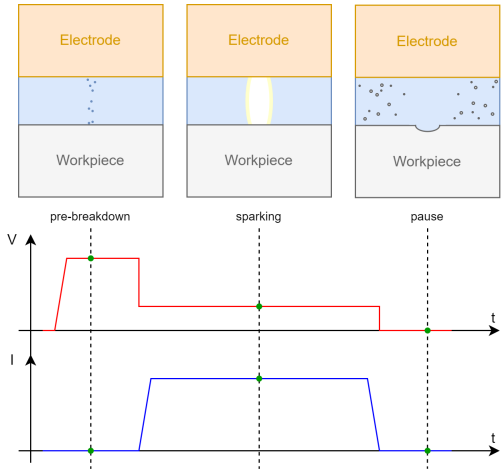

Fig. 2. Illustration of the EDM discharge process. The top section depicts electrode-workpiece interactions, while the bottom section presents corresponding voltage (V_o) and current (I_o) waveforms.

From a power electronics point of view, the delivery of an EDM discharge with a transistor-based EPG involves three stages (see Fig. 2).

- *Pre-breakdown*: A high voltage ($\sim 100\,\mathrm{V}$) is applied across the gap, which initially behaves as an open circuit before the breakdown occurs.
- *Sparking*: Once the gap breaks down, an ion channel forms, allowing the current to flow. The voltage across the gap drops rapidly and then stabilizes at a lower value ($\sim 20\,\mathrm{V}$).
- *Pause*: At the end of the pulse duration, the EPG halts the discharge by removing the applied voltage. The gap then undergoes an off-time period to flush away debris and de-ionize before the next discharge cycle.

These stages present distinct challenges for EPG design, as the load transitions abruptly from an open circuit to a high-conductivity plasma channel. The timing and properties of this transition are inherently stochastic, influenced by gap conditions and debris. This variability makes it difficult to regulate power delivery consistently, demanding precise control over discharge current and energy to ensure stable and efficient machining [3].

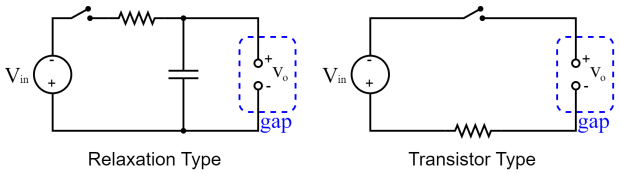

Fig. 3. Comparison of early EPG architectures: relaxation-type (left) and transistor-type (right).

Conventional EPG designs usually rely on simple energy delivery circuits (see Fig. 3). In the earliest relaxation-type systems, a capacitor is charged until the voltage across it causes gap breakdown, discharging the stored energy. This passive triggering has limited control over pulse timing and shape, as energy delivery depended entirely on component values and gap conditions. With advancements in transistor current capability, transistor-type systems delivered timed discharge pulses through active switching. However, current was often limited using series resistors, leading to significant power loss and low overall energy efficiency [1], [2].

More recently, modern EPGs have evolved into converter-based architectures that incorporate high-speed switching, energy buffering, and precise current regulation [4]–[7]. These architectures offer significantly improved control over discharge energy and pulse waveform, enabling better machining precision and adaptability to varying gap conditions. These systems often employ digital controllers such as microcontrollers or FPGAs to enable flexible, closed-loop pulse shaping—though at the cost of increased system complexity and overhead [6], [7].

In parallel, Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) have gained significant traction in power electronics because of their higher switching speed, lower conduction losses, and higher efficiency at high frequencies compared to silicon-based devices. These advantages have led to widespread adoption in applications demanding high power density and precise switching control, such as RF amplifiers, DC-DC converters, and electric drive systems [8], [9].

In the context of EPGs, they have been applied in a capacitor-driven topology [10], with discharge energy defined by the capacitor value and pre-charged voltage. While the above topology is optimized for ultra-low energy pulses, the present work supports sustained current regulation through extended pulse durations, making it suitable for medium-power EDM applications.

This study explores a closed-loop discharge regulation approach for EPG by leveraging the strengths of GaN HEMTs. A simple yet robust control scheme is implemented using discrete logic, enabling stable steady-state current regulation without complex digital platforms. The system is validated at a 10A discharge current and demonstrates transient response, steady-state regulation, and efficiency comparable to state-of-the-art solutions with minimal implementation complexity.

II. System Design

A. Problem Definition

The control variable for the electric pulse generator (EPG) is the discharge current. Due to the stochastic nature of gap discharge, open-loop control results in large current variations, compromising surface roughness and increasing tool wear.

This study proposes a closed-loop EPG design utilizing GaN power transistors, leveraging their high switching speed to achieve both efficiency and dynamic performance. For fair comparison with existing studies on the same application, the EPG is designed and evaluated at an output current of 10A with a rectangular pulse shape [2], [5], [7].

B. Power-Stage Architecture

The power stage consists of a buck-derived current source followed by some interfacing circuits to the load (see Fig. 4). The buck-derived current source is equivalent to a synchronous buck converter with its output capacitor removed.

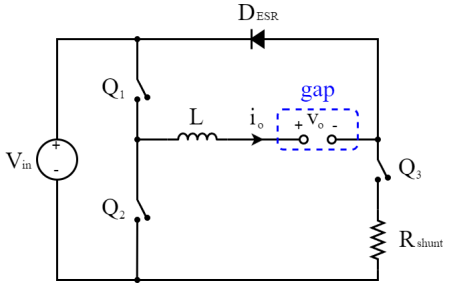

Fig. 4. Power stage of the EDM Pulse Generator (EPG), featuring a buck-derived current source and interfacing circuits.

The operating characteristics of proposed power stage are summarized below:

- *Pre-breakdown:* Q_1 and Q_3 close while Q_2 remains open, applying the full DC-link voltage across the machining gap.
- *Sparking*: Q_1 and Q_2 switch complementarily at high frequency, while Q_3 remains closed, regulating the output current for each pulse.
- *Pause*: Q_1 and Q_3 open while Q_2 closes to redirect current back into the DC link. After current ceases, Q_2 and Q_3 clamp the gap to ground, allowing for deionization before the next cycle.

By utilizing inductors for current limiting, this architecture achieves simple and efficient current regulation.

C. Implementation Challenges

The design and implementation of high-speed GaN HEMTs based EPG pose several practical challenges beyond the core control and powerstage architecture.

The high switching speed of GaN HEMTs makes circuit performance highly sensitive to PCB layout, especially due to parasitic inductance in the power loop. Inadequate layout can lead to voltage overshoot, ringing, and increased electromagnetic interference, degrading both efficiency and reliability [11]. To address these issues, the layout in this study was designed with attention to minimizing loop areas, placing decoupling capacitors close to switching nodes, and maintaining continuous low-impedance return paths.

In addition to layout optimization, the control strategy must support rapid transient response and maintain signal integrity in a noisy environment. While FPGAs offer precise timing control, they significantly increase design complexity and cost. In this work, a discrete logic implementation is adopted to achieve the necessary responsiveness and robustness, enabling effective use of the GaN HEMTs' switching capabilities without the overhead of a digital platform.

D. Control Strategy

The proposed system utilizes a Transient-Enhanced Constant On-Time (TE-COT) control scheme (see Fig. 5), adapted from the state-trajectory approach of Li et al. (2020) [12]. Constant On-Time (COT) control is a quasi-hysteretic modulation technique in which a fixed on-time pulse for the top transistor Q_1 is triggered each time the current falls below a set threshold.

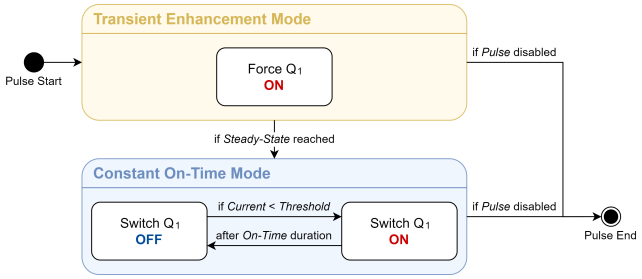

Fig. 5. State machine diagram of the TE-COT control scheme, with TE and COT modes shown in separate colored blocks.

While COT is a fast and simple control method, it struggles to handle large load steps. To address this, a Transient Enhancement (TE) mode is introduced [12]. The TE mode forces the Q_1 ON while the discharge current is below threshold. At the start of each pulse, the TE mode delivers a strong transient response to counteract the sudden load increase caused by the gap breakdown.

Once TE mode has driven the circuit near steady-state conditions, it deactivates. This allows COT mode to take over and regulate the discharge current around the reference for the remainder of the pulse.

E. Controller Implementation

The proposed control circuit implements the TE-COT scheme, as shown in Fig. 6. The circuit consists of two primary control blocks: Constant On-Time (COT) and Transient Enhancement (TE).

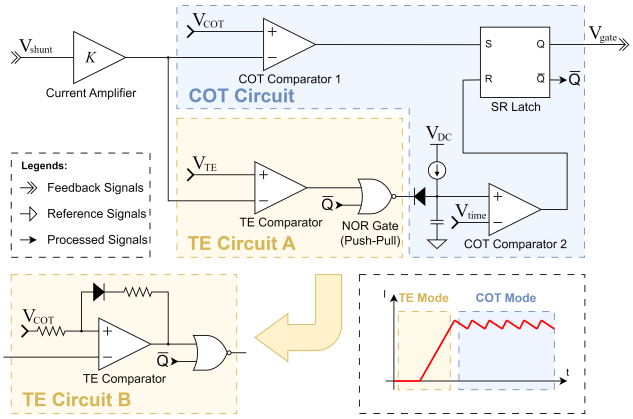

Fig. 6. Proposed implementation of TE-COT controller, with the TE and COT circuits distinguished by colored blocks.

The COT circuit (blue-highlighted) regulates steady-state operation. COT Comparator 1 compares the current shunt feedback voltage with a reference V_{COT} to determine when a new COT signal initiates. Its output sets the SR Latch, driving the gate signal high. This also begins to charge the timing capacitor, whose voltage is compared against the timing reference voltage V_{T} by COT Comparator 2. Once the capacitor voltage exceeds V_{T}, COT Comparator 2 resets the SR Latch, turning off the gate drive signal at the correct moment.

To complement COT regulation, the TE circuit (yellow-highlighted) enhances the system's response to large initial load steps. TE Circuit A is directly inspired by the implementation of Li et al. (2020) [12]. The TE Comparator compares the shunt feedback voltage with a reference voltage V_{TE}. When the discharge current is low, the comparator output forces the timing capacitor to discharge, preventing the SR Latch from resetting until the current rises above the V_{TE}.

This work proposes and implements an alternative strategy, TE Circuit B, which introduces a single-sided hysteresis network that lowers the TE Comparator's positive input after TE mode ends. This prevents TE mode from overriding COT control, improving robustness under noisy conditions. The design also reduces component count by sharing the same reference voltage V_{COT} with the COT circuit.

F. Performance Trade-offs

In the proposed EPG architecture, the inductor acts as the primary current limiting component. The choice of inductor directly affects both transient response and steady-state regulation.

Under the TE-COT control scheme, Q_1 is held ON until discharge current reaches reference. This gives the optimal rise-time for the TE stage:

$$\tau_{\text{rise}} = \frac{I_{\text{ref}}}{V_{\text{L}}} \times L \tag{1}$$

where V_{L} is the voltage across inductor during sparking, and I_{ref} is the discharge current reference.

On the other hand, for a given on-time t_{on} the current ripple in steady state (COT stage) is given by:

$$\Delta I = V_{\text{L}} t_{\text{on}} \times \frac{1}{L} \tag{2}$$

This reveals a fundamental tradeoff in EPG design – to improve transient response, a smaller inductor value is necessary to reduce rise time, according to (1); Conversely, to improve steady-state regulation, a larger inductor value is favored to reduce current ripple, according to (2). This trade-off is not unique to the TE-COT scheme. Keeping the half-bridge fully ON maximizes the current slew rate, which sets the lower-bound of rise time in transient. And, most switching strategy will inherently result in constant effective on-time in steady state.

The high-speed switching capabilities of GaN HEMTs provide a way to relax this trade-off. Because of their ability to switch very fast ($< 10\,\text{ns}$), the on-time can be kept shorter so that, according to (2), the current ripple can be reduced. Therefore, for EPGs built with GaN HEMTs, a smaller inductor value can be used to improve the transient response, without sacrificing the current regulation performance.

III. Experimental Validation

A. Component Selection

The prototype of EPG is designed for input voltage $80\,\text{V}$ and discharge current $10\,\text{A}$. The discharge gap voltage is assumed to be $20\,\text{V}$. This value is commonly reported in EDM applications, as described in [1], also aligns with the experimental data presented in [2].

A rise time of $500\,\text{ns}$ is targeted to highlight the fast transient capability of the proposed design. This corresponds to a required current slew rate of:

$$\frac{di}{dt} = \frac{I_{\text{ref}}}{\tau_{\text{rise}}} = 20\,\text{A}/\mu\text{s} \tag{3}$$

Given voltage across the inductor is $V_{\text{L}} = V_{\text{in}} - V_{\text{gap}} = 60V$, the selected $3.3\,\text{uH}$ power inductor roughly meets the requirement, yielding an actual slew rate of:

$$\frac{di}{dt} = \frac{V_{\text{L}}}{L} = 18.2\,\text{A}/\mu\text{s} \tag{4}$$

To keep the current ripple within 2A, an on-time of 100ns is selected, which gives rise to expected current ripple:

$$\Delta I = \frac{di}{dt} \times t_{\text{on}} = 1.82\,\text{A} \tag{5}$$

At steady state, the switching duty cycle d is given by:

$$d = \frac{V_{\text{gap}}}{V_{\text{in}}} = 25\% \tag{6}$$

Combining with selected on-time $t_{\text{on}} = 100\,\text{ns}$, designed EPG will switch at frequency of $2.5\,\text{MHz}$ in steady-state.

The switches in the power stage are EPC2307, and the half-bridge is driven by LMG1210. This study uses STTH30L06GY fast recovery diode for energy recovery from the inductor.

The load current is sensed with a $12\,\text{m}\Omega$ shunt resistor. The voltage drop across the current shunt is amplified by AD8099 high-speed operational amplifier in a non-inverting configuration with a gain of 20. This resulting feedback signal has a signal gain of $0.24\,\text{V}/\text{A}$. The on-board control logic is implemented with TLV-series high-speed comparators and LVC-family logic components from Texas Instruments.

B. Efficiency Calculation

The overall efficiency of the EPG system during sparking is estimated by quantifying major power losses and comparing their total to the load power:

$$P_{\text{gap}} = V_{\text{gap}} \cdot I_{\text{ref}} = 200\,\text{W}. \tag{7}$$

The primary losses originate from the GaN HEMTs. Q_1 and Q_2 alternate conduction in a half-bridge configuration, while Q_3 remains continuously on. With $R_{\text{DS(on)}} = 10.8\,\text{m}\Omega$, read from the EPC2307 datasheet at junction temperature $100\,^\circ\text{C}$, and $I_{\text{ref}} = 10\,\text{A}$, conduction loss is:

$$P_{\text{DC,transistor}} = 2 \cdot I_{\text{ref}}^2 \cdot R_{\text{DS(on)}} = 2.16\,\text{W}. \tag{8}$$

Switching losses are dominated by Q_1, which operates under hard-switching conditions. The overlap loss and capacitive loss per switching cycle are estimated as:

$$E_{\text{overlap}} = \tfrac{1}{2} V_{\text{in}} I_{\text{ref}} (t_{\text{r}} + t_{\text{f}}) = 3.86\,\mu\text{J} \tag{9}$$

$$E_{\text{cap}} = \tfrac{1}{2} C_{\text{oss}} V_{\text{in}}^2 = 1.12\,\mu\text{J} \tag{10}$$

where $V_{\text{in}} = 80\,\text{V}$, $C_{\text{oss}} = 350\,\text{pF}$, and $t_{\text{r}} + t_{\text{f}} = 9.65\,\text{ns}$, estimated from the EPC2307 and LMG1210 datasheets. At a switching frequency of $2.5\,\text{MHz}$, this yields:

$$P_{\text{SW,transistor}} = (E_{\text{overlap}} + E_{\text{cap}}) \cdot f_{\text{sw}} = 12.45\,\text{W}. \tag{11}$$

A shunt resistor of $2\,\text{m}\Omega$ used for current sensing introduces additional resistive loss:

$$P_{\text{shunt}} = I_{\text{ref}}^2 \cdot R_{\text{shunt}} = 1.2\,\text{W}. \tag{12}$$

Inductor losses include both DC and high-frequency AC components. With a DC resistance of $R_{\text{DC}} = 2.2\,\text{m}\Omega$, the conduction loss is:

$$P_{\text{DC,inductor}} = I_{\text{ref}}^2 \cdot R_{\text{DC}} = 220\,\text{mW}. \tag{13}$$

High-frequency copper loss is estimated via harmonic decomposition of the triangular ripple current at 2.5 MHz (25% duty cycle), using a frequency-dependent model for flat-wire inductors from [13]. Since model parameters were provided only for $N = 4$ and $N = 8$, interpolation was performed to estimate the correction factor at $N = 5.5$ turns used in the prototype. The resulting AC loss is:

$$P_{\mathrm{AC,inductor}} = 31\,\mathrm{mW}. \tag{14}$$

Other second-order losses such as gate drive, control, and capacitor ESR were not included.

Summing all losses accounted gives a total power dissipation of 16.1 W, corresponding to an overall efficiency of:

$$\eta = \frac{P_{\mathrm{gap}}}{P_{\mathrm{gap}} + P_{\mathrm{loss}}} = 92.6\%. \tag{15}$$

C. Bench Setup

The experimental validation of the proposed EPG was conducted using a custom bench setup, consisting of three main components:

- *Pulse Generator*: This is the primary circuit under evaluation, implementing the COT control scheme. The hardware integrates GaN-based EPG power stage and onboard closed-loop controller, as shown in Fig. 7.
- *Gap Emulator*: This module replicates the behavior of an EDM load using a diode-array-based emulator to provide a controlled breakdown voltage; a MOSFET is added to simulate gap breakdown, as shown in Fig. 8.
- *Signal Generator*: This module uses an Arduino to provide synchronized digital control signals to the bench setup. It does not participate in the current regulation.

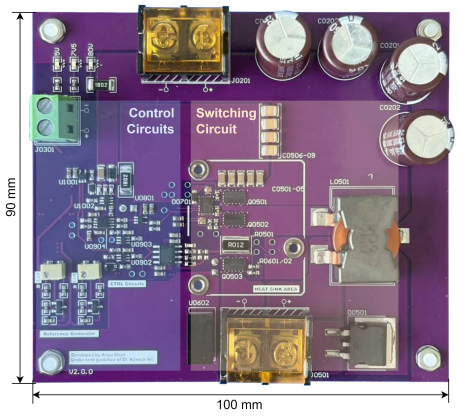

Fig. 7. Annotated image of the Pulse Generator board (100 mm × 90 mm), with control and switching sections highlighted. The background has been removed for clarity.

D. Experiment Results

The EPG has been tested under its full design condition using an 80 V input. Reference voltages have been tuned to achieve the target 10 A discharge current and 2.5 MHz switching frequency. The captured waveforms confirm proper TE-COT control behavior.

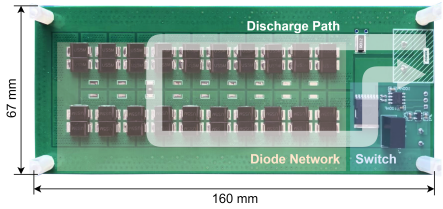

Fig. 8. Annotated image of the Gap Emulator (160 mm × 67 mm), highlighting the discharge path, diode network, and switching stage. Background removed for clarity.

Fig. 9 presents oscilloscope waveform demonstrating the operation of the TE-COT control scheme. The red trace shows the discharge current, derived from the amplified shunt signal, and the blue trace represents the gate-drive signal to the half-bridge. Three distinct phases of delivering electric pulse are visible on the captured waveform.

- *Pre-breakdown* is the first stage of generating an EDM pulse. The half-bridge is turned ON and the input voltage is applied across the discharge gap. No current flows until the gap breaks down.
- *TE Mode* is the stage after dielectric breakdown, with a sudden conduction path formation. The controller in TE mode forces half-bridge fully on, ensuring rapid current rise to the reference level.
- *COT Mode* is the stage after discharge current reaches its reference, and the TE mode deactivates. The controller transitions to COT regulation, where the half-bridge toggles periodically to sustain the discharge current at the reference value.

At the end of the predefined pulse duration, the control signal halts the discharge by redirecting the inductor current into the input rail, as described in the power-stage architecture (see Sec. II-B). Since this altered path bypasses the current shunt, the decay of the current is not captured in the waveform.

TABLE I
MEASURED PERFORMANCE PARAMETERS

Parameter	Value
Current Rise Time	645 ns
Mean Pulse Current	10.0 A
Current Ripple (pk-pk)	1.47 A
Switching Frequency	2.5 MHz

Table I summarizes the key parameters of the produced waveform. The results indicate good alignment with the predicted EPG performance.

With a 80 V DC supply for the experiment, the expected rise-time is

$$\tau_{\mathrm{rise}} = \frac{I_{\mathrm{ref}} L}{V_{\mathrm{L}}} = 550\,\mathrm{ns}. \tag{16}$$

Whereas we observe the measured current rise time is 645 ns. The slightly longer rise time and lower ripple than expected may be attributed to parasitic inductance in the connection to

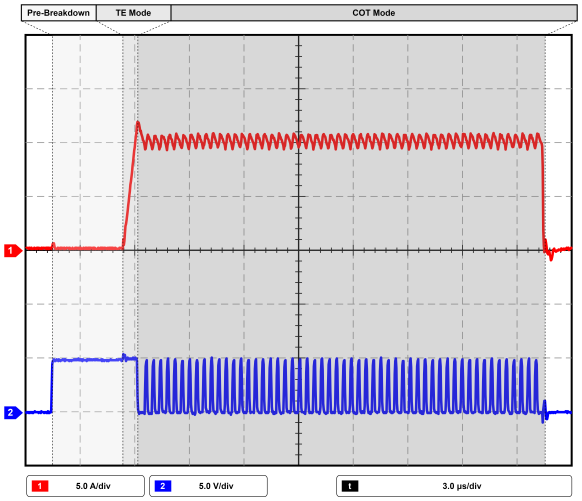

Fig. 9. Measured current waveform (red) and control signal (blue) for a single pulse, plotted from oscilloscope data using MATLAB.

the gap emulator and component tolerances, particularly of the inductor.

E. Discussion

A measured current rise time of 645 ns represents significant improvement over previously reported results and can enable EPGs to deliver energy-controlled pulses at a few μs duration. The rise time reported in literature on similar buck-derived pulse generators are compared in the table below.

TABLE II
COMPARISON OF EPG PERFORMANCE

	[7]	[8]	[9]	Design	Tested
Input Voltage (V)	100	100	80	80	60
Output Voltage (V)	25	25	25	20	20
Output Current (A)	10	2	10	10	10
Inductor (μH)	50[a]	15	10	3.3	3.3
Switching Freq.	150 kHz[a]	1 MHz	500 kHz	2.5 MHz	2.5 MHz
Rise Time	4 μs[b]	1.3 μs	2 μs	550 ns	645 ns
Current Ripple (A)	2[b]	0.6[b]	3[b]	1.8	1.5
Efficiency (%)	89.77[c]	85	—	92.6[d]	—

[a] Interleaved switching strategy is applied for this EPG.
[b] Values are visually estimated from figures in the original paper.
[c] Efficiency is calculated by Kane et al. [2].
[d] Theoretical calculation presented in Section III-B.

Following the reasoning presented in section II-F, improving dynamic response often accompanies a sacrifice in current regulations. This compromise is not seen in the proposed implementation because of the higher switching frequency. In addition, as shown in the efficiency calculation in section III-B, the switching loss is the dominating loss term at a discharge current of 10 A. Despite operating at a significantly higher switching frequency, the efficiency remains highly competitive, surpassing all EPG architecture investigated in Kane et al. (2020) [2]. This fact reinforces the advantage of GaN HEMTs in achieving high-speed pulse regulation without excessive switching losses.

The proposed solution also allows flexible control over both discharge current and pulse duration. The pulse length is managed by a microcontroller, making reconfiguration straightforward. In the prototype, the discharge current is set by the COT reference voltage generated on board. For enhanced integration with EDM machines, this can be replaced with a digital-analog converter, enabling direct discharge current control via the machine's computer.

IV. CONCLUSION

This study explored the application of GaN HEMTs in EDM pulse generators. To the best of the authors' knowledge, this is the first study to demonstrate a closed-loop current regulation using GaN HEMTs in EDM pulse generators. Paired with a dedicated TE-COT control scheme, the EPG demonstrated high efficiency, fast transient response, and good current regulations. These advances contribute to improved machining efficiency and more precise control over discharge energy, which are critical for achieving consistent EDM performance.

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