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# Alternative Dielectrics for Hole Selective Passivating Contacts and the Influence of Nanolayer Built-In Charge

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**Abstract.** Highly passivating, hole selective contacts are required for future high efficiency silicon solar cells. This work investigates selected dielectrics as potential SiO<sub>x</sub> replacements to act as hole selective contacts. AlO<sub>x</sub> and SiN<sub>x</sub> were identified as good candidates due to their low valence band offsets to silicon and proven surface passivation capabilities. Simulated J-V curves show AlO<sub>x</sub> and SiN<sub>x</sub> maintain acceptable contact resistivities at thicknesses below 1.4 and 1.7 nm, respectively. The SiO<sub>x</sub> hole contact was found to become extremely resistive even at thicknesses <1 nm, suggesting that either pinholes dominate conduction, or the band offset parameters differ from those in real TOPCon structures. The passivation of the dielectrics was also simulated, with SiO<sub>x</sub> outperforming both AlO<sub>x</sub> and SiN<sub>x</sub> primarily due to the excellent interface. Additionally, the effect of nanolayer built in charge was investigated. Charges below 10<sup>12</sup> q/cm<sup>2</sup> were found to have little effect, while negative charges above 10<sup>12</sup> q/cm<sup>2</sup> resulted in reductions in the contact resistivity and recombination current. The calculated selectivity for a 1.4 nm layer of AlO<sub>x</sub> was 12.9, while a value of 13.8 was calculated for SiN<sub>x</sub> at typical intrinsic charge levels.

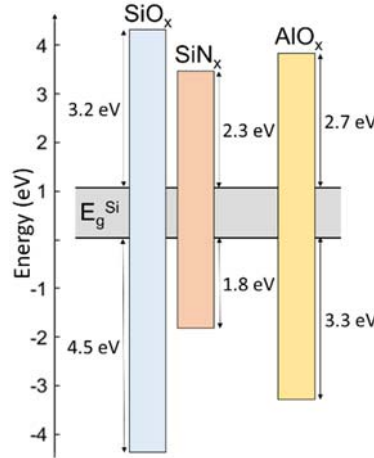
## INTRODUCTION

To continue to improve the efficiencies of silicon photovoltaic devices, recent work has focused on passivating contacts. TOPCon is one of such methods which has proved extremely successful and industrially viable for electron selective contacts. In the TOPCon device structure, a SiO<sub>x</sub> nanolayer provides low interface recombination, while permitting adequate current flow via tunneling and pinholes to a polycrystalline conducting layer which, in turn, is contacted by metal. Cells with this technology have reached efficiencies greater than 26% on both sides contacted cells [1], and IBC cells [2]. The highest efficiency results have been achieved using SiO<sub>x</sub> as an electron selective contact. However, a highly selective hole contact is also required for two reasons. The first is to allow easier integration into current PERC production lines which use p-type wafers. The second is that future, high efficiency, single junction cells will require passivating front and rear contacts - i.e. both on an n- and p-type silicon interface. Efforts to make hole selective contacts using SiO<sub>x</sub> have been less successful [3]–[6] than their electron counterparts.

Developing efficient passivating contacts requires a detailed understanding of the underlying conduction and passivating mechanisms. In the TOPCon structure the mechanism of current flow through the SiO<sub>x</sub> layer has been broadly studied and debated. The two proposed mechanisms reported in the literature are quantum tunnelling through the oxide, and direct conduction from the wafer to the poly Si via nano-sized pinholes [7]. It has been found that both processes can contribute to carrier transport through the dielectric, with the dominant mechanism depending on the oxide thickness and processing conditions. It has now generally been concluded that tunnelling is the dominant

mechanism when the oxide is less than 1.5 nm and the anneal is kept to temperatures  $\leq 850^\circ\text{C}$  [8]–[13]. Pinholes form during anneals at temperatures above  $850^\circ\text{C}$ , though the exact temperature at which they dominate conduction depends on the oxide growth technique and thickness. Such pinholes can form contacts with low resistivities which can improve conductivity but deteriorate the passivation. In general, the continuous oxide has been reported to produce superior passivation than that with the presence of pinholes [14]–[16]. The variability in the resulting contact as function of oxide processing sequences stresses the requirement for understanding the physical mechanisms, especially as we move towards the search for efficient hole selective contacts. The tunnelling mechanism, for example, could lead to a potential reason for poorer quality in  $\text{SiO}_x$  hole contacts compared to the equivalent electron contacts. This is due to the band alignment, as can be seen in Fig. 1. The valence band offset of 4.5 eV combined with a large effective mass for holes ( $m_h^*$ ) in  $\text{SiO}_x$  inhibits the tunnelling of holes. In comparison,  $\text{SiN}_x$  and  $\text{AlO}_x$  both have lower band offsets which could allow reduced contact resistivities. In addition, bulk  $\text{AlO}_x$  and  $\text{SiN}_x$  are known to provide excellent surface passivation of silicon. This has provided the motivation to study these dielectrics as an alternative to  $\text{SiO}_x$  in hole selective passivating contacts [17],[18].

Recently, the effect of the built-in charge has been considered in passivating contact structures [22]–[26]. It is proposed that charge accumulation could result in increased majority current, while reducing minority carriers at the interface. As it is well known that there is a high concentration of intrinsic charge in  $\text{SiN}_x$  and  $\text{AlO}_x$ , this could affect the contact properties. The negative intrinsic charge in  $\text{AlO}_x$  would provide a beneficial accumulation regime in a hole selective contact, while the typically positive charge in  $\text{SiN}_x$  may generate a depletion region at the Si/dielectric interface, which could be detrimental to the contact properties. In this work, we used Sentaurus TCAD to simulate hole selective passivating contacts with  $\text{SiO}_x$ ,  $\text{AlO}_x$  and  $\text{SiN}_x$  as the dielectric nanolayer. The contact resistivity as a function of dielectric thickness is obtained, then the nanolayer built-in charge is incorporated into the simulation. The influence of charge on the resistivity and the passivation of the contact is investigated. The simulated resistivity and the recombination current are combined to give an overall value for the contact selectivity [27], which allows the suitability of each dielectric as a hole selective contact to be assessed.



**FIGURE 1.** Typical literature values for band offsets between crystalline silicon and some dielectric layers with thickness below 2 nm [19]–[21].

## SIMULATION PARAMETERS

Sentaurus TCAD [28] is used to simulate the Current-Voltage (J-V) curve of a contact structure, to extract its resistivity, and the Kane and Swanson technique [29] is used to determine the saturation current. To analyse the current through the tunnelling contact structure, dark J-V simulations are carried out on the device structure is shown in Fig. 2a. The dielectric properties are taken from Table 1 and the simulation parameters used are shown in Table 2. Due to the widely different properties of  $<3$  nm films compared to bulk dielectric properties, the input parameters are obtained from studies of ultra-thin layers. The front diffusion is set using a Gaussian doping profile with a peak concentration of  $2 \times 10^{19} \text{ cm}^{-3}$  and a depth of  $0.4 \mu\text{m}$  based on the optimal diffusion found in previous work [30]. The current

mechanism simulated in this study is purely tunnelling, with no pinholes present. J-V curves between  $\pm 0.1$  V are simulated and the total resistivity,  $\rho_{tot}$ , is taken as the gradient of the J-V curve around 0 V. This method quantifies the influence of the contact resistivity on the J-V curve of the whole device and is in principle different from values obtained by TLM measurements. To isolate the contact resistivity,  $\rho_c$ , a reference resistivity,  $\rho_{ref}$ , was initially calculated. The reference resistivity accounts for the bulk spreading resistance and rear contact resistivity. It was determined using a structure without the tunnelling dielectric or front diffusion and setting the emitter contact resistivity to  $10^{-8} \Omega \text{ cm}^2$ . This gave a resistivity of  $21.7 \text{ m}\Omega \text{ cm}^2$  which was subtracted from the total resistivity to give the contact resistivity (Equation 1).

$$\rho_c = \rho_{tot} - \rho_{ref} \quad (1)$$

J-V curves are simulated with the dielectric thickness,  $t_d$ , varied between 0.1 – 2.5 nm or until the resistivity becomes excessively high.  $\text{SiN}_x$  and  $\text{AlO}_x$  both contain high levels of intrinsic charge which could affect the carrier flow through the junction. Therefore, the effect of charge in the contact resistivity of a passivating contact structure is investigated. For a set thickness, the nanolayer built-in charge is simulated by adding charge to the Si/dielectric interface. As the built-in charge depends on the processing conditions and can be manipulated through certain processing steps, positive and negative charge concentrations as high as  $10^{13} \text{ q/cm}^2$  are simulated.

Sentaurus TCAD simulations are also carried out on a lifetime structure as depicted in Fig. 2b. This allows us to investigate the passivation of tunnelling contact structures. Tables 1 and 2 show the key parameters used in the simulation and the details of the models used. A homogeneous optical injection is simulated to a depth of  $198 \mu\text{m}$ . This ensures there is no generation of carriers at the point when the recombination is probed, and therefore a simple current pattern is generated. The probing takes place at a depth of  $198.6 \mu\text{m}$ , before the dielectric layer. The concentration of  $1.4 \times 10^{19} \text{ cm}^{-2}$  corresponds to the average injection of a 1 sun global spectrum. The average density can be used as the diffusion length in the bulk is larger than the wafer thickness [31]. The key parameters in the simulation of  $J_0$  are the surface recombination velocities for electrons and holes,  $S_{n0}$  and  $S_{p0}$  respectively. For contacts, the values of  $S_{n,0}$  and  $S_{p,0}$  in ultra-thin layers must be considered. These were obtained from literature studies of each dielectric. Where possible, the values of  $S_{n0}$  were determined from experimental values of  $J_0$  from ultra-thin layers on p-type Si [32],[33]. Due to limited studies on ultra-thin  $\text{SiN}_x$  layers a study on n-type Si was used instead [22]. Given that  $S_{n0}$  will vary with the processing route, these values can only give an indication of the passivation quality for ultra-thin layers of each dielectric. The  $S_{n0}$  values used are shown in Table 1 and  $S_{p0}$  values are assumed to be  $0.1 S_{n0}$ .

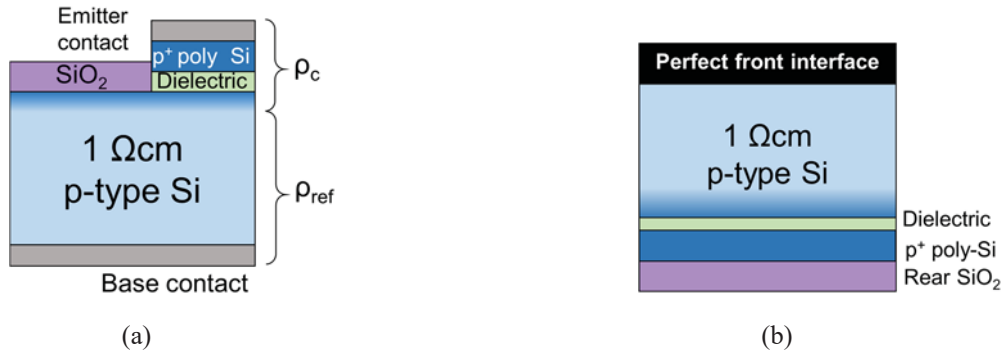


FIGURE 2. Structure used for simulation of a) Contact resistivity and b) Recombination Current

TABLE 1. Selected properties of ultra-thin dielectrics.

Dielectric	Conduction band offset (eV)	Valence band offset (eV)	Effective mass ( $m_e^*$ , $m_h^*$ )	Typical intrinsic charge ( $\text{q/cm}^2$ )	Surface recombination velocities, $S_{n0}$ , $S_{p0}$ (cm/s)
$\text{SiO}_x$	3.2[19]	4.5[19]	0.42, 0.58 [34],[35]	$+9 \times 10^{10}$ [22]	3000, 300
$\text{SiN}_x$	2.2 [20]	1.8 [20]	0.5 0.5 [36]	$+1.5 \times 10^{12}$ [22]	$10^4$ , $10^3$
$\text{AlO}_x$	2.7 [21]	3.3 [21]	0.4, 0.4 [37],[38]	$-4 \times 10^{12}$ [23]	$10^5$ , $10^4$

TABLE 2. Simulation Parameters

Parameter	Value
Wafer thickness	200 $\mu\text{m}$
Poly Si Layer Thickness	40 nm
Wafer resistivity	1 $\Omega\text{ cm}$ (p-type)
Poly Si doping	$1.3 \times 10^{20}\text{ cm}^{-3}$ [39]
Temperature	300 K
Recombination	SRH [40], Auger [41], Radiative [42]
Mobility	Philips unified mobility model [43]
Band gap Narrowing	Schenk low injection [44]
Tunnelling (J-V sim. only)	Non-local tunnelling model using Schenk and Hassens [45]
Optical injection ( $J_0$ sim. only)	Homogeneous optical injection of $1.4 \times 10^{19}\text{ cm}^{-2}$

## CONTACT RESISITIVITY

The contact resistivity extracted from the simulated J-V curve is shown in Fig. 3 as a function of dielectric thickness. There is zero interface charge simulated at present. An electron selective  $\text{SiO}_x$  layer is included as a reference. These results indicate that at larger thicknesses there is an exponential dependence on  $t_d$ , suggesting the contact is limited by the tunnelling current [8]. At lower thicknesses,  $\rho_c$  becomes independent of  $t_d$  due to  $\rho_c$  becoming limited by the series resistance in the poly Si. A  $\rho_c$  of up to  $100\text{ m}\Omega\text{ cm}^2$  is acceptable for a full area passivating contact [46]. For the electron selective  $\text{SiO}_x$ ,  $\text{AlO}_x$ , and  $\text{SiN}_x$  this gives thicknesses of 1.35 nm, 1.4 nm, and 1.7 nm, respectively. This shows that  $\text{AlO}_x$  as a hole contact can offer similar resistivities to  $\text{SiO}_x$  electron contacts, while lower resistivities may be achieved with  $\text{SiN}_x$ , or it could allow thicker tunnelling layers to be deposited, which would relax the process control requirements when implementing such layers. The hole selective  $\text{SiO}_x$  contact exceeds  $100\text{ m}\Omega\text{ cm}^2$  even at thicknesses  $<1\text{ nm}$ . This could suggest the presence of pinholes in real structures. However, there is experimental evidence that tunnelling is dominant in 1.3 nm p-type  $\text{SiO}_x$  structures, while maintaining a low  $\rho_c$  of  $30\text{ m}\Omega\text{ cm}^2$  [47]. Therefore, another possibility is that  $\text{SiO}_x$  in real, processed contacts has lower barrier heights to those measured in [19] and [20].

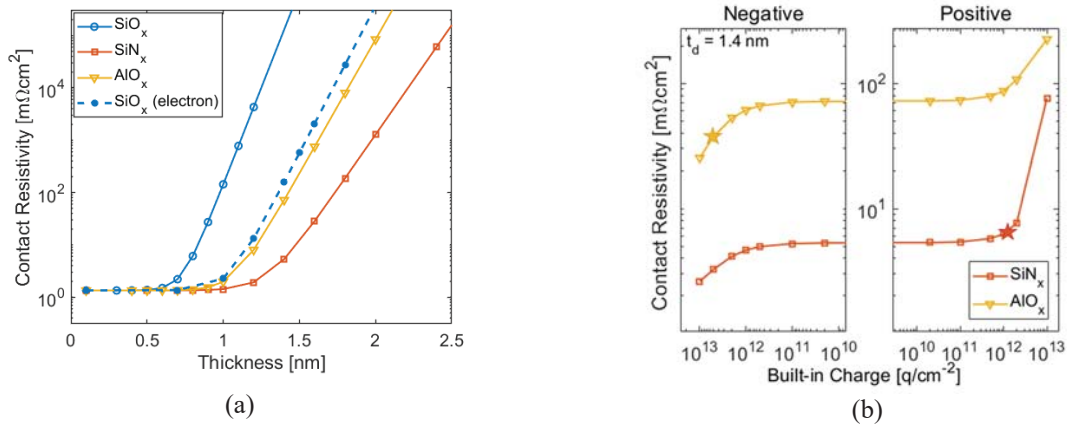


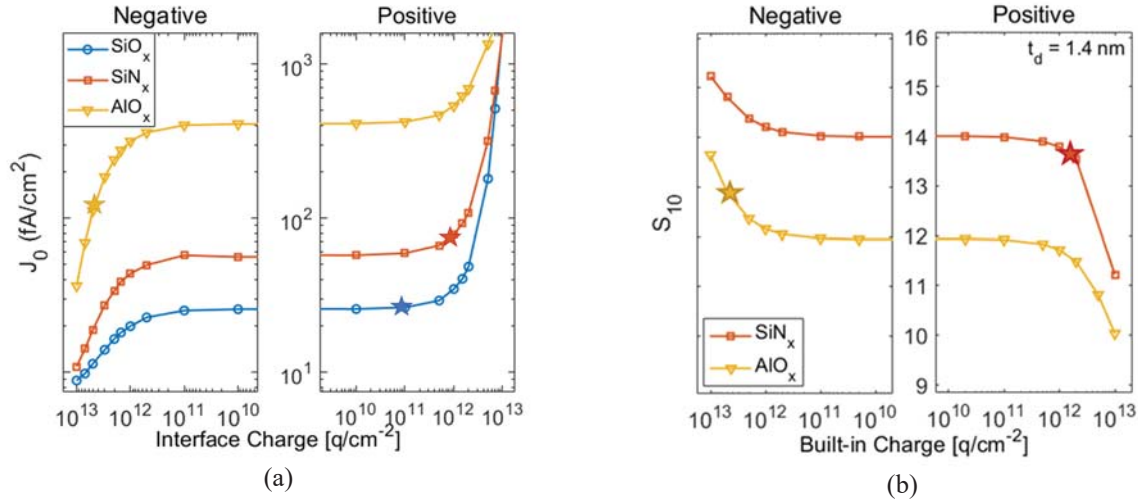
FIGURE 3. a) Simulated contact resistivity for  $\text{SiO}_x$ ,  $\text{SiN}_x$  and  $\text{AlO}_x$  as a function of thickness.  $\text{SiO}_x$  as an electron contact included for reference. b) Simulated contact resistivity for a 1.4 nm layer of  $\text{SiN}_x$  and  $\text{AlO}_x$  with varied built-in charge. Star symbols represent typical values of intrinsic  $Q_f$  present in each dielectric.

In a further simulation series, the tunneling thickness is kept constant at 1.4 nm and  $Q_f$  is varied up to  $10^{13}\text{ q}/\text{cm}^2$ . Fig. 3b shows the effect of this on  $\rho_c$  for the  $\text{SiN}_x$  and  $\text{AlO}_x$  layers with typical levels of intrinsic charge from Table 1 depicted with a star symbol. The  $\text{SiO}_x$  has been omitted due to the unrealistically high resistivity simulated. At charge concentrations below  $10^{12}\text{ q}/\text{cm}^2$  there is little effect, while higher concentrations result in an increase or decrease in

$\rho_c$  for negative and positive  $Q_f$  respectively. The values at neutral charge can be inferred from Fig. 3a where it is clear a smaller film thickness allows large tunnelling current, and thus would lower  $\rho_c$ . However, in all cases the addition of negative charge reduces  $\rho_c$  by a factor of 2 at  $10^{13} \text{ q/cm}^2$ . This illustrates that an  $\text{AlO}_x$  film with a negative intrinsic charge will result in a slight reduction in the resistivity, while an  $\text{SiN}_x$  film with a typical positive charge,  $\rho_c$ , is not adversely affected (contrary to prior predictions in the literature [48]). Fig. 3b shows that, while charge can influence the current transport in tunnelling contacts, the band structure of the dielectric remains of crucial importance to the contact resistivity.

## THE EFFECT OF CHARGE ON PASSIVATION AND SELECTIVITY

Figure 4a shows the  $J_0$  simulated for  $\text{SiO}_x$ ,  $\text{SiN}_x$ , and  $\text{AlO}_x$ , tunnelling layers as a function of  $Q_f$ . The chemical passivation for each material is characterised by the SRH interface recombination parameters  $S_{n0}$  and  $S_{p0}$ , which strongly influence  $J_0$ . As with contact resistivity, low charge concentrations have little effect. Positive  $Q_f$  causes severe degradation in the passivation quality due to an increase in the minority carrier concentration at the interface, while at high negative charge there is a clear reduction in  $J_0$ .  $\text{AlO}_x$  shows poor chemical passivation as seen by the high recombination current at neutral charge. However, the large, negative intrinsic charge induces field effect passivation which reduces  $J_0$  by a factor of 4. An improvement in the chemical passivation through optimised process routes including hydrogenation would lower  $J_0$  further.  $\text{SiN}_x$  shows reasonably low  $J_0$  values at neutral or small values of positive charge ( $< 1 \times 10^{12} \text{ q/cm}^2$ ). Optimising the  $\text{SiN}_x$  nanolayer could improve this further, including the potential to induce a negative fixed charge [49].  $\text{SiO}_x$  currently outperforms both  $\text{SiN}_x$  and  $\text{AlO}_x$  in terms of passivation, although it is larger than  $\text{SiO}_x$  measured on n-type structures which have reached values under  $3 \text{ fA/cm}^2$  [50]. Independent of the dielectric, the field effective passivation which results from interface charges of  $10^{13} \text{ q/cm}^2$  reduces the recombination current by almost an order of magnitude compared to chemical passivation alone. Selecting processes which provide high negative  $Q_f$  or tailoring the charge in the dielectric could improve the passivation of any dielectric nanolayer in a selective contact.



**FIGURE 4.** a) Simulated recombination current for  $\text{SiO}_x$ ,  $\text{SiN}_x$  and  $\text{AlO}_x$  nanolayers with varied built-in charge. b) Calculated selectivity for  $\text{SiN}_x$  and  $\text{AlO}_x$  with varied built-in charge. Star symbols represent typical values of intrinsic present in each dielectric.

Brendel et al. [27] defined a metric to give an overall selectivity of a contact by taking the ratios of resistances of minority and majority carriers. The selectivity can be defined by:

$$S_{10} = \log_{10} \frac{v_{th}}{\rho_c J_0} \quad (2)$$

Where,  $v_{th}$  is the thermal voltage. By combining the simulated values of  $\rho_c$  and  $J_0$ , the contact selectivity can be calculated over a range of  $Q_f$ . Figure 4b shows the calculated selectivity for  $\text{SiN}_x$  and  $\text{AlO}_x$ .  $\text{SiO}_x$  was again omitted



as the unrealistically high resistances result in an unrealistic selectivity. The value at neutral charge depends on the thickness and  $S_{n0}$  value for each dielectric. Therefore, the selectivity may be increased through improved chemical passivation or by depositing a thinner dielectric layer provided it maintains the same level of passivation. A significant increase in  $S_{10}$  can be achieved in all cases for a large, negative  $Q_f$ . As the selectivity parameter is logarithmic, the increase of over 1 in the selectivity at  $10^{13}$  q/cm<sup>2</sup> relates to over an order of magnitude improvement in the contact properties. The calculated values of selectivity from simulations show a high  $S_{10}$  value of 14 for a 1.4 nm SiN<sub>x</sub> with low charge. This is reduced to 13.8 at the typical intrinsic charge level of  $1.5 \times 10^{12}$  q/cm<sup>2</sup>, however, if the built-in charge is kept below  $1 \times 10^{12}$  q/cm<sup>2</sup> this effect is mitigated. The AlO<sub>x</sub> interlayer selectivity is below 13, despite the benefit from high negative charge. This is due to the larger contact resistivity at this thickness, and the high  $S_{n,0}$  value. Brendel calculated a maximum theoretical efficiency from a given selectivity [27]. This gives theoretical maximum efficiency of 26% for a full area contact with a 1.4 nm SiN<sub>x</sub> or AlO<sub>x</sub>. Both dielectrics have sufficiently low contact resistivity at this thickness, so the efficiency is limited by the passivation. Real SiO<sub>x</sub> contacts with a p Si/SiO<sub>x</sub>/p<sup>+</sup> polySi structure have selectivity values over 15 and theoretical maximum efficiencies over 29% [27], so further improvement is required for SiN<sub>x</sub> and AlO<sub>x</sub>, primarily in terms of the passivation of the nanolayer films.

## CONCLUSION

Through device simulations, potential options for tunnelling, passivating, hole selective contacts have been explored. SiN<sub>x</sub> and AlO<sub>x</sub> were investigated as an alternative to SiO<sub>x</sub> using simulated contact resistivity and recombination current. When simulating SiO<sub>x</sub> as the dielectric in hole contacts, high resistivities were calculated using the expected band offsets for a SiO<sub>x</sub> nanolayer. This is not seen experimentally and suggests that practical devices must have a lower effective barrier height, or the transport mechanism is dominated by pinholes. On the other hand, the low valence band offset of SiN<sub>x</sub> results in favourable transport properties for use as a hole selective contact. with layers up to 1.7 nm thick can maintain sufficiently low  $\rho_c$ . AlO<sub>x</sub> also has acceptable hole transport properties at thicknesses up to 1.4 nm.

The passivation of SiN<sub>x</sub> and AlO<sub>x</sub> cannot currently match the high chemical passivation of the SiO<sub>x</sub> layers. AlO<sub>x</sub> is limited by a poor chemical passivation. If this can be improved through adapted processing routes, then it can be combined with the large field effect passivation due to the high negative charge and result in a low recombination velocity. The recombination current of SiN<sub>x</sub> is closer to the SiO<sub>x</sub>, though the positive charge is detrimental for charges above  $10^{12}$  q/cm<sup>2</sup>. There is potential for further improvement to the passivation through optimising deposition processes for p-type Si and ensuring the positive charge is minimised. With improved passivation, combined with the low contact resistivity, extremely high selectivity for both SiN<sub>x</sub> and AlO<sub>x</sub> could be achieved, making both suitable candidates for hole selective contacts.

Overall, the analysis of the nanolayer built-in charge was shown to produce significant effects on the contact properties at concentrations above  $10^{12}$  q/cm<sup>2</sup>. Accumulation regimes reduce both the contact resistivity and the recombination current, resulting in increases in  $S_{10}$ . This could benefit dielectric layers with high levels of intrinsic charge, such as in AlO<sub>x</sub>, or, processes which manipulate the charge could be implemented to enhance the contact performance. While this work has focussed on hole contacts, high levels of accumulation charge could also be applicable to enhancing electron contacts.

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