Investigating Pin-Holes Issues in Josephson Junction Travelling Wave Parametric Amplifiers Requiring Large Area of Dielectric Layer

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***Abstract*—Microwave superconducting Josephson Travelling Wave Parametric Amplifiers (JTWPAs) exploit the non-linear inductance of a long superconducting metamaterial line formed by thousands of Josephson junctions to achieve broadband parametric gain with quantum limited added noise. Nevertheless, pin-holes in the dielectric (spacer) layer required for fabricating these superconducting transmission lines (STLs) represent a challenge for JTWPAs fabrication. In this paper, we explore two pin-holes mitigation techniques, which shown promising results with DC characterisation of a suite of test structures at cryogenic temperatures. When implemented for actual JTWPA designs with much longer length, they have shown to improve the fabrication yield albeit some pin-holes still seems to exist over the large wafer area. This indicates that further mitigation effort is required to completely eradicate the pin-holes issue for applications requiring large area of dielectric layer such as microwave JTWPAs.**

***Keywords*—travelling wave, parametric amplifier, quantum-limited, Josephson junctions, metamaterial, microwave.**

INTRODUCTION

Travelling Wave Parametric Amplifier (TWPA) can generate high amplification gain over a large bandwidth in the microwave regime with quantum-limited noise performance [1-3]. TWPAs use superconducting transmission lines (STL) with high non-linear inductance to promote the parametric processes required to transfer energy from a pump wave (ω_p) to a weak signal (ω_s). In this process, an idler tone (ω_i) is generated. The non-linear inductance can be sourced from high kinetic inductance superconducting films (termed K-TWPA) [1, 4, 5], or metamaterial films comprising many Josephson junctions (J-TWPA) [2, 3]. TWPAs find applications in many fields ranging from quantum computing [6], dark matter axion search [7, 8, 9] to astrophysics; replacing the semiconductor-based readout amplifiers for millimetre (mm) and sub-mm receiver to minimise heat dissipation and enhance sensitivity [10, 11].

JTWPAs are challenging to fabricate because they require a large number of junctions with low critical currents. Most recent JTWPAs have utilised shadow-evaporated aluminium junctions with high fabrication yield [2, 12]. However, the use of aluminium-based junctions restricts their operation to mK environments and frequencies below 90 GHz, which limits some potential applications for JTWPAs. Niobium/aluminium-aluminium oxide/niobium (Nb/Al-AlO_x/Nb) junctions offer an alternative solution to elevate the operational temperature and frequency into the mm/sub-mm range, as well as expediating JTWPA on-chip integration with astronomical receivers such as superconductor-insulator-superconductor (SIS) mixers.

Trilayer deposition techniques for fabricating Nb/Al-AlO_x/Nb junctions have been extensively explored and matured for the development of SIS mixers. Utilising them for JTWPAs, on the other hand, is a relatively new development. One of the challenges in fabricating niobium-based JTWPAs is related to the existence of pin-holes defects in the inherent dielectric layer, rather than just the need for many junctions. This dielectric layer, referred as the spacer, is required to define the trilayer-junctions and to form parallel plate capacitors (PPCs) needed in some JTWPA designs. These pin-holes can result in electrical connections between the bottom niobium layer of the trilayer and the top wiring layer, creating an unwanted short-circuits to ground effect, rendering the device unusable.

In this paper, we explore two mitigation techniques to reduce the number of pin-holes in the spacer layer. We measure the performance of these techniques by fabricating dedicated test devices that we characterised using DC signal analysis. Then, we implement one of these techniques in our JTWPA designs, that we fabricated and tested at cryogenic temperatures. The results from the preliminary tests are presented and discussed.

PIN-HOLES MITIGATION TECHNIQUES

The intended metamaterial transmission line designed for our JTWPAs is presented in Fig.1. This elementary unit cell representing a small section of length 'a' in the STL, is cascaded numerous times to create the entire device. Often, the unit cell includes one or several junctions and a parallel plate capacitor (PPC) to increase the shunt capacitance to the ground C_s, ensuring a characteristic impedance $Z_0 = 50\ \Omega$ of the line.

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Furthermore, resonators can be added to the transmission line [13] to correct for the phase mismatch caused by the cross and self-phase modulation of the tones propagating in the JTWPA, increasing the gain-bandwidth product.

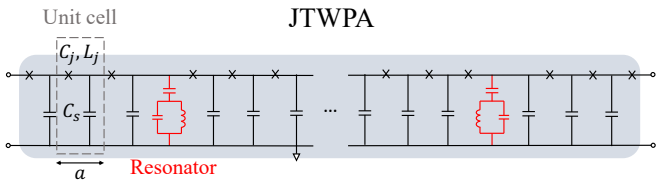

Fig. 1. Schematic circuit diagram of a JTWPA. The unit cell is composed of a single Josephson junction denoted with a cross, with capacitance C_j and inductance L_j, and the shunt capacitance C_s to the ground. The unit cell is cascaded to create the metamaterial nonlinear transmission line. Resonators are periodically added to the line for resonant phase matching (RPM), to enhance the gain and bandwidth.

For fabricating the tunnel junction required for the JTWPAs, we modify the trilayer fabrication process recipe originally developed for SIS mixers. As shown in Fig.2(a), the cross-section topology of our transmission line comprising the junctions is composed of a Nb/Al-AlO$_x$/Nb trilayer, a dielectric spacer layer surrounding the junction and a niobium wiring layer contacting the top electrode of the junction. For a detailed summary of the fabrication steps, we refer the reader to [14].

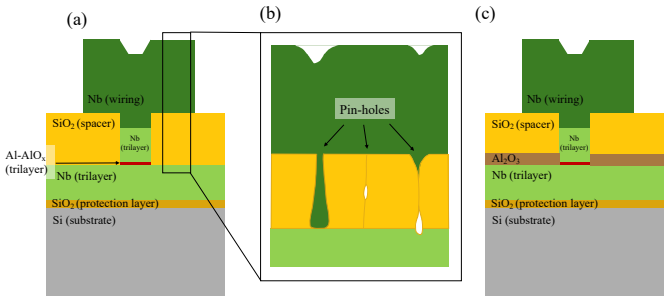

Fig. 2. Cross-section diagram of a trilayer niobium Josephson junction. (a) standard layer distribution. (b) Zoom-in the spacer layer, showing the formation of pin-holes. (c) Pin-hole mitigation strategy consisting of adding an extra layer of Al_2O_3 in the spacer layer. The diagrams are not to scale.

In principle, any dielectric material could be used for the spacer layer, although silicon dioxide (SiO_2) is our preferred choice due to its electromagnetic properties and the availability of existing equipment in our cleanroom facility to grow them on niobium. However, RF-sputtered SiO_2 layers suffer from the formation of pin-holes potentially leading to short-circuits between the trilayer bottom niobium and the wiring layer (Fig.2(b)). The issue is less critical for relatively small devices operating at mm/sub-mm frequency, but for a microwave JTWPA measuring several mm^2 in size, this could be a challenge. Numerous factors could contribute to the formation of these unwanted pin-holes, such as the substrate surface conditions, substrate's temperature during sputtering, a low RF power used and pressure fluctuations in the chamber. The density of these pin-holes decreases exponentially with the dielectric thickness [15], therefore, a thick dielectric layer is a viable mitigation strategy. Furthermore, the pin-holes density is also inherently related to the deposition technique and the material choice e.g., evaporated Al_2O_3 (aluminium oxide) have shown to have a lower pin-hole density, hence our alternative mitigation approach. We acknowledge that dielectric layer formed using plasma-enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD) technique could also help to resolve the pin-hole issue, but unfortunately, we do not have access to the required facilities to perform such deposition. Hence, we focus on exploring possible solutions to RF-sputtered SiO_2 for our JTWPA development here.

We have explored both pin-holes mitigation strategies described above: (a) increasing the RF-sputtered SiO_2 spacer layer from 200 to 400 nm, and (b) adding a protective layer of 20 nm evaporated Al_2O_3 underneath the 200 nm RF-sputtered SiO_2, as shown in Fig.2(c). We compare the performance of these two approaches by fabricating a suite of test devices composed of a niobium coplanar waveguide (CPW) embedded with 100, 500 and 1,000 PPCs coupled to the transmission line as shown in Fig.3. To ease the fabrication and reduce the complexity, the trilayer of these test devices was substituted with simply a bottom niobium layer, and no junctions are added to the line. Mitigation technique (a) and (b) are implemented in two different wafers, denoted Wafer 1 and Wafer 2 respectively. We use a 280-um thick high resistivity silicon wafers for the substrate.

These test devices were DC-screened at cryogenic temperatures using the 2-wires measurement shown in Fig.4. The DC screening setup allows us to measure the current-voltage (IV) curve through the trace of the devices and from the trace to the ground, by rewiring the experiment at room temperature. At temperatures below 9 K, the device's resistance is negligeable and we measured an average resistance ($R_{\text{throu}} = 31.1\ \Omega$) originated from the cooper wires used to connect the current source and voltmeter. When measuring the resistance from the trace of the device to the ground, we found an average value of $R_{\text{gnd}} = 19.4\ \Omega$ for short-circuited test devices and 2.22 kΩ for non-faulty devices. The two orders of magnitude difference in the resistance allows us to easily identify devices with pin-holes issues that result in electrical shorts to ground.

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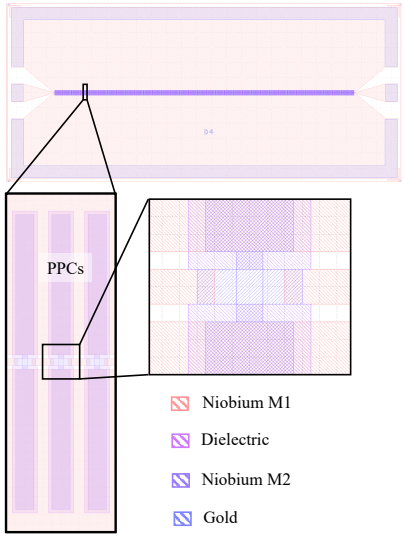

Fig. 3. Layout of the test devices used to study the performance of the two pin-holes mitigation techniques. The parallel plate capacitors are connected to the trace of the CPW.

To further confirm the validity of our measurements, we measure the RF transmission of two non-faulty devices with 1,000 and 100 PPCs, plotted in Fig.5(a) and (b) respectively. Note that the devices' characteristic impedance $Z_0 \neq 50\ \Omega$ (due to the absent of the tunnel junctions) results in a Fabry-Perot-like effect in the transmission profile, caused by the cavity modes. The periodicity of this transmission variation is inversely proportional to the length of the lines, hence the ten times more rapid periodicity for the 1,000 PPCs sample compared to the 100 PPCs sample.

A total of 16 test-structure devices were tested, 12 at cryogenic temperatures and 4 at room temperature, where the effect of the pin-holes can equally be observed through the DC screening process. The results from these measurements are summarised in Fig.5(c). Despite the limited number of fabricated test devices, the larger number of 'good' test devices in Wafer 2 indicates that increasing the dielectric thickness is the preferred pin-holes mitigation strategy. Although this may be applied for JTWPAs with purely bare junctions without PPCs, the solution may not be applied to cases that need PPCs. The capacitance of the PPCs decreases linearly with the thickness of the dielectric layer, therefore, to achieve the same shunt capacitance values, the PPCs will now need to have a much larger area than originally intended. The larger PPC area required not only increases the footprint of the JTWPA device, but will equally increase the chances of having a pin-hole, hence potentially limiting the yield. On the other hand, the addition of a 20 nm evaporated Al_2O_3 will barely modify the size of the required PPCs in our design, while showing promising improvements in the reduction of pin-holes. Therefore, we chose the pin-holes mitigation strategy (b) for our devices.

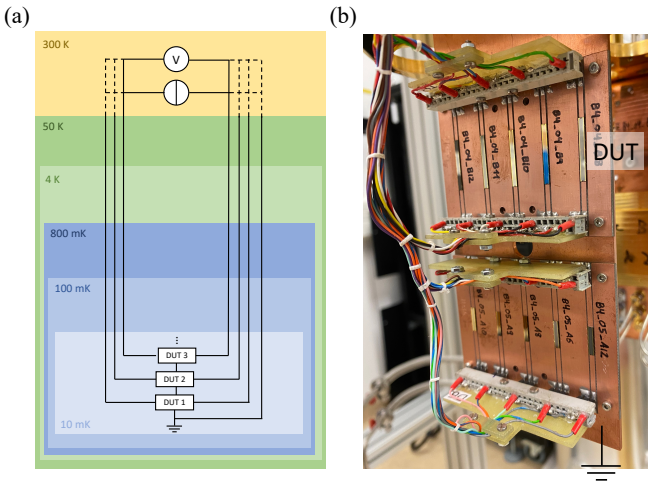

Fig. 4. DC-screening experimental setup. (a) Schematics of the experimental setup. The dotted lines indicate possible reconfiguration options to measure the different devices, as well as the connection from the device to the ground. (b) Picture of the DUT mounted on the DC-screening board inside the cryostat.

JTWPA DESIGN AND EXPERIMENTAL RESULTS

Using the chosen pin-hole mitigation technique presented in the previous section, we fabricated JTWPAs composed of 2,024 Nb/Al-AlO_x/Nb junctions and a targeted critical current density $J_c = 1.4$ and 0.9 kA/cm^2 (for two different designs), where the spacer layer is composed of the stack of 200 nm SiO_2 and 20 nm Al_2O_3. The spacer layer is equally used as the dielectric layer for a large number of PPCs deployed to match the impedance of our JTWPA to 50 Ω. Furthermore, 23 resonators (comprising a meandered inductive line and a PPC) are added to the transmission line for phase-matching purpose. More details on the design can be found in [16].

Fig.6 shows the IV curve measured for the two JTWPAs: Device A with $J_c = 1.4$ kA/cm^2, and Device B with $J_c = 0.9$ kA/cm^2. The measurements were taken using the DC-screening setup presented in Fig.4. The measured IV curves for Device A and B are plotted in the top and bottom panels respectively, with the left column measured through the trace while the right column from the trace to the ground.

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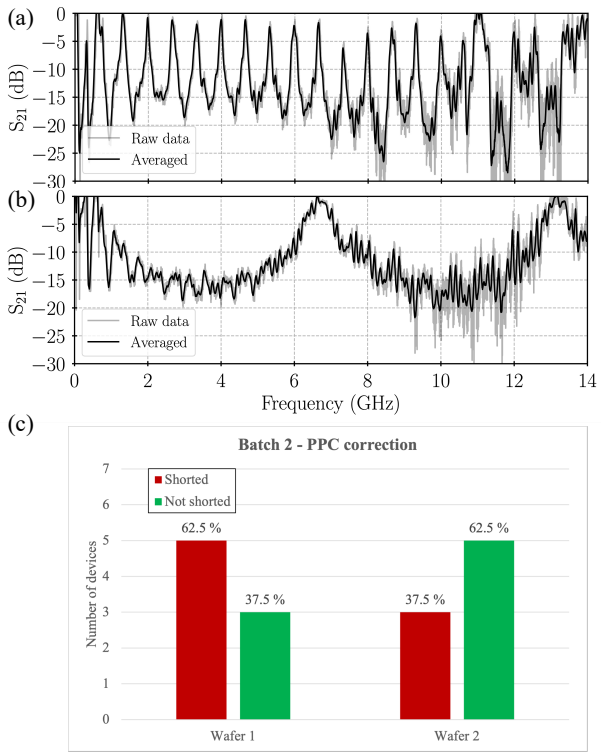

Fig. 5. RF transmission profile at T = 4 K calibrated with a passive feedthrough for (a) a test device with 1,000 PPCs and (b) a test device with 100 PPCs. The data is averaged with a 43.2 MHz window. (c) Number of short-circuited (red) and non-faulty (green) test devices after DC-screening. The spacer layer is formed of 20 nm evaporated Al_2O_3 and 200 nm RF-sputtered SiO_2 (Wafer 1), and 400 nm RF-sputtered SiO_2 (Wafer 2).

Assuming no short-circuits to the ground in our device, we would expect an IV characteristic similar to a bare single Josephson junction, but with a gap voltage 2,024 times higher than the V_{gap} of a single junction, since the junctions are connected in series. However, from Fig.6 (a) and (c), we observe that the transition to normal state happened at a value smaller than the expected $V_{gap} \approx 6.4$ V. We believe this is due to the presence of several short-circuits in the line as illustrated in Fig.7(a), where the current partly flows through the ground plane, bypassing a number of junctions. When measuring the IV curve to the ground (Fig.6(b) and (d)), we notice the same effect for a smaller value of V_{gap}. This is consistent with our theory, since in this case, the current only sees the junctions before the first short-circuit in the device, without returning to the trace, as shown in Fig.7(b).

Despite the existence of short-circuits in the line, the data in Fig.6 can be used to estimate the I_c of the junctions. From the V_{gap}, we estimate the number of junctions seen by the current to $N_{jj} = 74 \pm 7$, 218 ± 10 and 23 ± 2 for Fig.6(a), (c) and (d) respectively (we exclude Fig.6(b) due to the low quality of the V_{gap} transition). Measuring the normal resistance value and divideding by the number of junctions, we can make use of the Ambegaokar-Baratoff formula to estimate the average I_c of the junctions, resulting in $I_c = 7.25 \pm 0.68$ µA and $I_c = 2.85 \pm 0.23$ µA for device A and B respectively. These results are close, in terms of order of magnitude, to the targeted value of $I_c = 7$ and 4 µA for device A and B respectively.

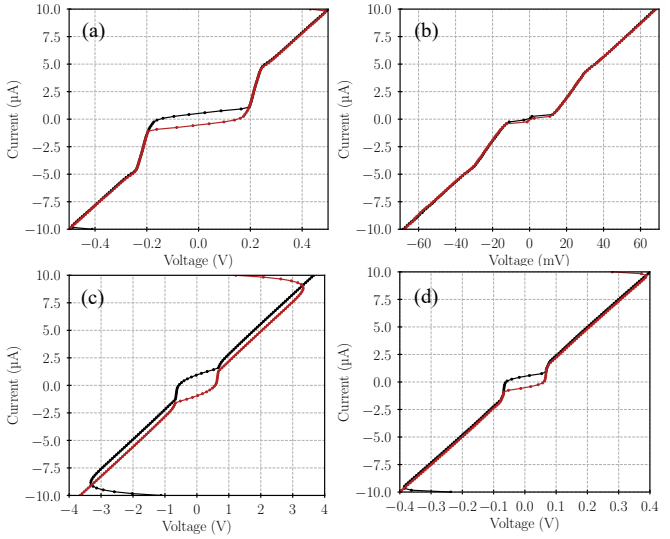

Fig. 6. Current-voltage (IV) curves of our JTWPAs measured at T = 10 mK for Device A (a) through the device and (b) from the device trace to the ground, and for Device B (c) through the device and (d) from the device trace to the ground. The non-linear behaviour from (b) and (d) indicates a possible short-circuit in the line. The current is swept from -10 to 10 µA (black) and from 10 to -10 µA (red).

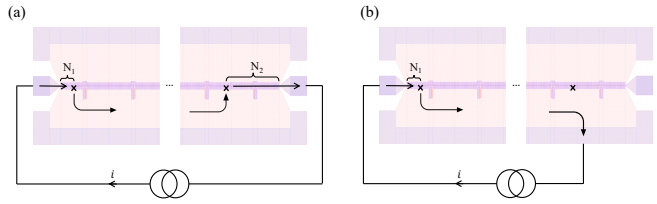

Fig. 7. Schematic representation of the current flowing in our device when several short-circuits to the ground are presented in the line, (a) when the current is applied through the device, and (b) from the device to the ground.

We found similar results for the most of the JTWPA devices measured using this DC-screening technique, suggesting pin-holes issues still persisted despite the yield improvement, most likely due to the much larger area of dielectric layer used in these devices. However, we did manage to measure a satisfactory transmission profile for some of the devices.

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The transmission measured for one of these devices is shown in Fig.8. We notice several high-Q resonant dips around 6 GHz, that we associated to the inclusion of the resonators originally designed for a resonance frequency at 7.4 GHz. The shift and spread in resonant frequency could indicate another fabrication issue, related to the fabrication tolerance of the photolithography technique used to define the resonators. Furthermore, the wider dip appears around 8.5 GHz is probably due to the loading effect of the resonators in the transmission line. Nevertheless, the device shows a satisfactory overall transmission, with a moderate expected frequency dependent loss originating from the dielectric layer in the PPCs.

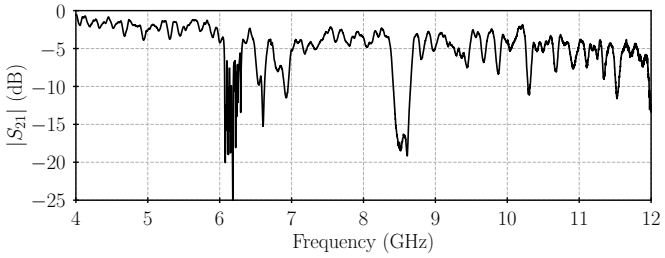

Fig. 8. RF transmission at T = 10 mK measured for the only satisfactory JTWPA, calibrated with a blank. We associate the resonance around 6 GHz to the resonators, and the dip around 8.5 GHz to the periodic loading effect of the resonators in the transmission line. We see a moderate loss with frequency as expected from the dielectric used for the PCCs.

CONCLUSION

Pin-holes formed in the dielectric used as the spacer layer in defining the trilayer-junction of a microwave JTWPA are a technical concern. They can result in a short-circuit to the electrical ground, rendering the device unusable. We explored two techniques to reduce the number of pin-holes in our RF-sputtered SiO_2 dielectric layer fabrication recipe: (a) increasing the SiO_2 layer, and (b) adding a protective layer of 20 nm of evaporated Al_2O_3 below the SiO_2 layer. Both techniques showed promising results on fabricated test structures. Nevertheless, when implemented in our JTWPA design with much larger spacer areas, it seems that the pinholes have not been completely eradicated, although we observe an improvement in fabrication yield. Therefore, we believe that further efforts are needed to eliminate them completely for devices requiring large area of RF-sputtered dielectric layer, such as our JTWPA design.

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