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Controlling surface carrier density via a PEDOT:PSS gate: An application to the study of silicon-dielectric interface recombination

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This communication reports a technique to control the surface carrier population of silicon during photo-conductance decay measurements, by using a semi-transparent PEDOT:PSS gate. The potential of this technique has been demonstrated by characterizing carrier-dependent surface recombination of 1 Ωcm n-type float zone silicon, passivated with dielectric stack layers of either SiO_2, SiO_2/SiN_x, a-Si/SiO_x, a-$Si/SiO_x/SiN_x$, AlO_x, or AlO_x/SiN_x. Carrier density at the Si-dielectric interface has been controlled from heavy inversion to heavy accumulation regimes despite leakage currents. This has provided insightful information into the recombination activity at the silicon surface.

Introduction

Surface recombination remains a major factor limiting the performance of silicon solar cells. Characterizing and understanding how surface recombination depends on carrier density is required to minimize such losses.[1–3] It can lead to the optimization of the passivating surface layers that control carrier population, and thus minimize interface recombination.[4–6] This is especially important in the recently developed passivating contact technology, where the surface carrier population determines the selectivity of the contact.[7,8] Through careful tuning, a surface layer can allow the transmission of one carrier type, while preventing the opposite

carrier to access recombination sites.[6,9,10] The ability of such a layer to control the surface carrier density is governed by the work function and the fixed charge concentration of such layers.[11] The precise control of the dielectric charge is therefore of great interest to the silicon photovoltaics field. This is particularly important since passivating selective contacts are regarded as extremely promising for future silicon-based single and tandem junction devices.[11]

The accurate characterization of dielectric fixed charge, and its influence on interface recombination, has long been a cumbersome task. It requires techniques that control carrier concentration in the space charge region, such as capacitance-voltage and corona discharge deposition. However, dielectric conduction largely hinders accurate capacitance-voltage measurements, and it influences charge stability when using corona discharge. To address this, a biased metal gate can be used on the dielectric to control and measure recombination rate as a function of surface carrier density. This method creates a metal-insulator-semiconductor structure, with the weakness of having an opaque electrode that impedes light injection of carriers and photo-conductance measurements, thus obstructing the characterization of, for example, minority carrier effective lifetime.

Attempts to overcome these issues have been previously proposed using: (i) Semi-transparent metal electrodes, requiring ultrathin controlled deposition of palladium[12] or aluminum.[13] (ii) Semi-transparent polysilicon gates in combination with *pn* diodes in complex 2-dimensional systems.[2] And (iii) an opaque gate at the rear of the specimen and light injection from the front in a photoluminescence[14–16], or microwave detected photoconductivity systems.[17,18] These methods rely on assumptions or models of the carrier flux inside the test structures, and are thus indirect. In this communication, I present a fast and simple sample preparation and measuring methodology that allows control of the surface carrier population using a

semitransparent gate. In turn this enables direct measurements of surface recombination as a function of the surface carrier population. This method can readily be used to extract the interface built-in potential that arises from fixed charge and work-function differences, thus providing insightful information into the carrier dynamics at the silicon-dielectric interface. Its potential has been demonstrated by characterizing carrier dependent surface recombination and built-in potential in six passivating dielectric layers on silicon. These have been selected since they are of great interest for today's silicon photovoltaics research and industry. These include SiO_2, SiO_2/SiN_x, a-Si/SiO_x, a-Si/SiO_x/SiN_x, AlO_x, and AlO_x/SiN_x.

Experimental Section

PEDOT:PSS contact bias in photo-conductance measurements: The new technique proposed in this communication is pictured in Figure 1.a. Two spring-loaded probes connect a source measurement unit (SMU) to a gate electrode at the front and rear of the specimen. The structure is placed on a photo-conductance decay system to measure effective lifetime while the gate is biased. Here an Agilent B2901A SMU, and a Sinton WCT 120 lifetime tester were used. The SMU is first set to a steady voltage bias, while both current and voltage are logged. A lifetime measurement is then obtained using the transient method, with 1/64 s flash time. The quasi-steady-state method was not used here since all samples showed sufficiently high lifetimes. The specimen comprised bulk silicon which is double sided coated with a dielectric layer (5-100 nm), on which a layer of Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS) is deposited and cured. Sigma Aldrich 3.0-4.0wt% in H_2O PEDOT:PSS solution was used. Samples were coated by painting the PEDOT:PSS solution on the specimen using a standard painting brush. The solution was immediately cured by placing the specimen on a hot plate at 70 ± 5 ^oC for 2 min, under an extracted hood. This process was repeated on each side. The influence of the deposition conditions were explored by using two variations to the PEDOT:PSS. In the first specimens were painted with two

layers, each layer cured independently after deposition. For the second, specimens were spin coated, instead of painted, with PEDOT:PSS at 1000 rpm for 60 s prior to curing.

The optical properties of the painted PEDOT:PSS were characterized using a Flame-NIR Spectrometer by Ocean Optics, and a Deuterium-Halogen Light Source. A quartz glass was painted and cured in the same manner as the silicon specimens, and used to characterize the average, minimum and maximum transmittance of the PEDOT:PSS layers deposited. The transmittance for such PEDOT:PSS layers is shown in Figure 1.b. Here, the typical filtered and unfiltered spectrum of the flash lamp used for lifetime photo conductance measurements has been included. Figure 1.b shows that the PEDOT:PSS layers produced here reduced the incident light on average by 50%. Despite this, it is easily possible to generate a substantial amount of photo-injected carriers, which makes this method rather attractive.

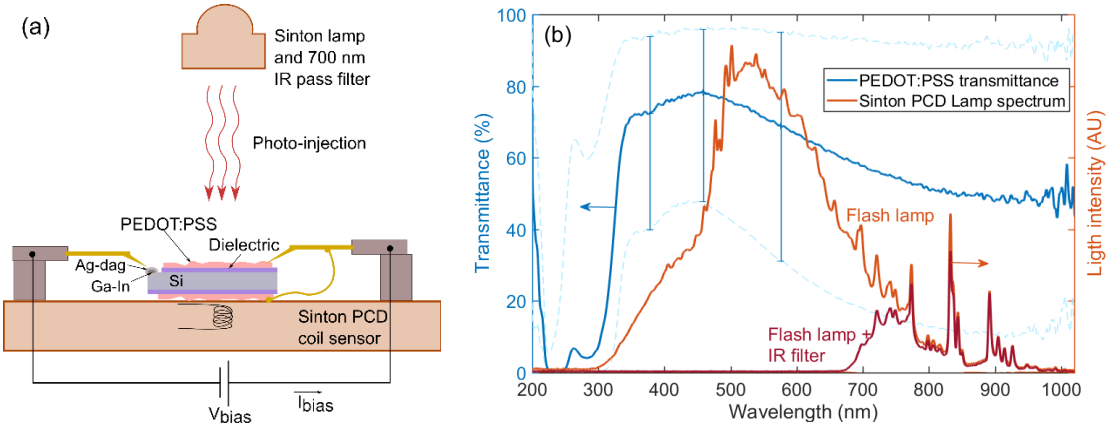

Figure 1. (a) Schematic of measurement set up including a semi-transparent PEDOT:PSS gated symmetrical specimen, (b) Optical transmittance of the PEDOT:PSS film used here.

Specimen details: The potential of this technique has been evaluated as follows. Double-side polished, <100>, 1 Ωcm, 200 μm thich, n-type float zone silicon wafers were used. These were coated on both sides with a dielectric layer stack following an RCA clean. The dielectrics studied here are:

Thermal silicon dioxide (SiO_2), grown at 850 ^oC or 1050 ^oC to produce 10 or 100 nm thick layers, in a dichloroethylene/oxygen atmosphere.[19] Plasma enhanced chemical vapor

deposited (PECVD) silicon nitride (SiN_x) using a Roth&Rau SiNA XS system, with silane and ammonia as precursors.[20,21] PECVD amorphous silicon (a-Si) using silane and hydrogen as precursors.[21,22] PECVD silicon oxide (SiO_x) using silane and nitrous oxide as precursors.[21,22] And lastly, plasma-assisted atomic layer deposited (PA-ALD) aluminum oxide using a Oxford Instruments OpAL reactor.[23] A 425 ºC, 25 min forming gas anneal was applied to a subset of SiO_2 and AlO_x passivated specimens.

These dielectric stacks were combined to form single, double and triple layers as summarized in Table 1. The PEDOT:PSS film was coated and cured, and its sheet resistance measured 30 times across the ~50 cm^2 area, on both sides, using the four-point probe method with gold spring loaded probes, spaced by 2.54 mm. The resulting sheet resistance of each PEDOT:PSS layer on top of a dielectric stack is summarized in Table 1.

Surface charge density characterization: Using Gauss' law for a parallel plate capacitor the charge present on the gate contact Q_{gate}, held at a V_{bias} potential, can be calculated as:

$$Q_{gate} = \frac{\varepsilon_0 K_{ins}}{t_{ins}} (V_{gate} - \frac{\Phi_{MS}}{q}) \quad (1)$$

Where $\varepsilon_0 \, K_{ins}/t_{ins}$ is the insulator stack capacitance.[24] This quantity is equivalent to the mirror charge present at the surface of the silicon either as surface states Q_{it} or space charge region Q_{scr}, plus any fixed charge in the dielectric stack Q_f:

$$Q_{Si} + Q_f = Q_{it} + Q_{scr} + Q_f = -Q_{gate} \quad (2)$$

Where Q_{Si} denotes the total charge density at the silicon surface. Q_{gate} was here calculated from the applied gate bias, subtracting a 0.53 V work function difference between the PEDOT:PSS and the 1 Ωcm Si. A nominal PEDOT:PSS work function of 4.85 eV was

used.[25] A Keysight E4980A LCR meter was used to conduct capacitance-voltage (CV) measurements at 10 kHz, and thus extract the dielectric stack capacitance. Metal-insulator-semiconductor (MIS) structures were fabricated with each of the dielectric stacks. The MIS structure was formed by depositing ~50 nm of pure aluminum in a thermal evaporator through a shadow mask, to form front contacts ~1 mm diameter. Back contacts were formed by removing the rear dielectric stack and spreading Gallium-Indium eutectic. The exact contact area (A) of the front Al contacts was measured using calibrated microscope images, and this value used for calculating the equivalent insulator capacitance:

$$\frac{\varepsilon_0 K_{ins}}{t_{ins}} = \frac{C_{ins}}{A} \qquad (3)$$

The insulator capacitance was determined in the accumulation regime using the McNutt-Sah method [26] with the extension in.[27] An expansion of these methods is found in [28].

Table 1. Summary of dielectric stacks and PEDOT:PSS gates used in this study

Dielectric stack	Synthesis	Nominal Thickness (nm)	Insulator stack capacitance (nF/cm^2)	PEDOT:PSS coating condition	Gate sheet resistance (Ω/sq)
SiO_2	Thermal growth	100	30.42 ±2.4	Painted, single layer	146 ± 46
SiO_2	Thermal growth	100	30.42 ±2.4	Painted, double layer	81 ± 45
SiO_2	Thermal growth	100	30.42 ±2.4	Spin coated, single layer	110 ± 13
SiO_2/SiN_x	Thermal growth/PECVD	10/60	63.875 ±5	Painted, single layer	173 ± 64
a-Si/SiO_x	PECVD	8/100	38.42 ±3.07	Painted, single layer	99 ± 50
a-$Si/SiO_x/SiN_x$	PECVD	8/13/60	71.8 ±5.87	Painted, single layer	186 ± 93
AlO_x	ALD	30	151.342 ±11.8	Painted, single layer	136 ± 40
AlO_x /SiN_x	PA-ALD/PECVD	10/60	71.53 ±3.8	Painted, single layer	164 ± 78

Carrier-dependent surface recombination in Si

The relation between semiconductor surface recombination and carrier population has long been suggested.[2,3,29] Multiple studies have characterized it experimentally by measuring

effective lifetime and dielectric charge in symmetrically passivated samples.[5,20,30–32] While effective lifetime in well-controlled specimens can directly render surface recombination,[33,34] the measurement and variation of dielectric charge is more involved. Such studies are often limited to either a single value of dielectric charge, or a secondary mechanism to vary the charge via for example corona discharge or changes to the deposition parameters. Measuring the charge concentration in corona charged dielectric is affected by leakage,[35] and changing the deposition parameters produces different Si-dielectric interfaces.[36,37] These aspects have made a characterization of carrier dependent surface recombination a complex task.

In this communication, the PEDOT:PSS gate has been used to control surface recombination at the dielectric-silicon interface by varying the surface carrier density. This has been carried out for a variety of dielectric passivation layers, all currently used in the production of high performance silicon solar cells, as summarized in Table 1. Figures 2.a and b illustrate the effective lifetime for such double-side passivated specimens, at 10^{15} cm^{-3} minority carrier injection, and as a function of gate charge. Here, it is evident that the concentration of charge carriers can be readily controlled by the bias applied to the PEDOT:PSS gate. This in turn regulates the carriers' access to recombination centers at the interface, and ultimately the effective lifetime of the specimen. By applying a wide range of gate bias voltage, this technique allows measuring the carrier dependent effective lifetime for conditions from strong accumulation, to strong inversion in the surface space charge region of silicon. These measurements are in good agreement with those done using other techniques, for example those reported by Schmidt *et al* in [5,38,39] , Glunz *et al* in [40], and most recently Haug *et al* [14–16], and the same author. [22,41]

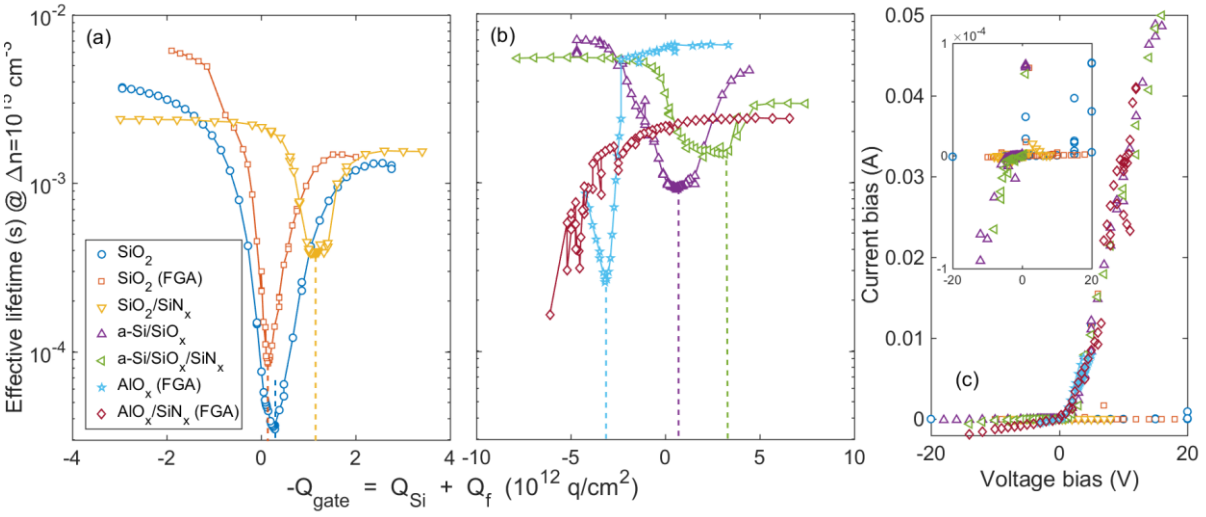

Figure 2. Effective lifetime as a function of gate bias on the surface of the dielectric for n-type 1Ωcm FZ Si passivated with (a) SiO_2 and SiO_2/SiN_x, (b) a-Si/SiO_x, a-$Si/SiO_x/SiN_x$, AlO_x and AlO_x/SiN_x layer stacks. Dotted lines indicate the gate charge for maximum recombination. (d) Leakage current as a function of gate bias for all dielectrics here studied.

The use of this technique also provides insights into the passivation quality and embedded fixed charged in these dielectric layers. Table 2 includes a summary of the maximum and minimum effective lifetimes observed. In Figure 2.a it is clear that hydrogenation from FGA or silicon nitride deposition largely improves the chemical passivation of a Si/SiO_2 interface, observed by a higher lifetime minimum. For a Si/a-Si interface, Figure 2.b, the chemical passivation is far better than $Si\text{-}SiO_2$, as widely reported in the literature using other techniques,[42–45] while for a Si/AlO_x interface the chemical interface is only superior to SiO_2 without PECVD SiN_x hydrogenation. This is clear from the 220 μs lifetime minimum for the Si/AlO_x interface. The deposition of a PECVD SiN_x on Si/SiO_2, Si/a-Si/SiO_x and Si/AlO_x seems to degrade their maximum attainable lifetime. For oxidized silicon, this can be partly explained by the fact that 10 nm SiO_2 is grown at 850 ^oC rather than 1050 ^oC. Recent reports have found that higher temperature oxidation annihilates in-grown defects in FZ silicon, providing a stable and higher quality benchmark for surface passivation studies.[46–48] For the a-Si and AlO_x structures, this can be explained by the plasma damage occurring during film deposition as has also been reported.[4,49,50] It is noted that the highest positive bias applied to the AlO_x stacks in Figure 2.b was less than for others in Figures 2. This was due to

degradation of the interface observed as a drop in the effective lifetime when applying higher positive biases, and for this reason heavy accumulation conditions were not measured in the AlO_x samples.

Another aspect evident in Figure 2 relates to the position of the lifetime minima with respect to gate charge. In a Si/SiO_2 interface, the capture cross section for electrons is higher than for holes,[2,12] and thus a small negative gate charge is required to maximize surface recombination, or minimize lifetime.[41] In other dielectric-silicon interfaces the capture cross sections can vary, yet the point of maximum recombination normally occurs at $Q_{Si} \sim \pm 2\text{x}10^{11}$ q/cm^2.[3,41,51,52] This means that the shift in the Q axis in the lifetime curves is due primarily to the dielectric fixed charge. For single SiO_2 layers dielectric charge minimally shifts the curve. This is in agreement with findings of small positive charge concentration in such oxides.[53] A summary of the estimated charge concentation in the dielectric stack here studied is included in the last column of Table 2. For a SiO_2/SiN_x double-layer, a higher negative gate charge is required since nitride films are known to have a higher built-in concentration of positive charge.[37] Similar conclusions can be drawn for Si/a-Si interfaces where the presence of a nitride film shifts the curve due to the additional positive charge. For AlO_x films, it is clear that a concentration of negative fixed charge is present in the film. Such charge is still present when a SiN_x film is deposited, yet the presence of the nitride also seems to modify the conduction mechanisms through the dielectric and at the silicon interface. This is evident in the scatter observed for positive bias in Figure 2.b, which originates from charge being injected or extracted from the dielectric, thus quickly modifying the recombination activity at the interface.

Table 2. Summary of effective lifetime and gate bias results in studied dielectric layers.

Dielectric stack	Maximum τ_{eff} (ms) in accumulation	Maximum τ_{eff} (ms) in inversion	Minimum τ_{eff} (ms)	Estimate Q_f (10^{12} q/cm^2)

SiO_2	3.71	1.31	0.0347	+0.3 ±0.2
SiO_2 (FGA)	6.12	1.48	0.0854	+0.143 ±0.2
SiO_2/SiN_x	2.41	1.52	0.387	+1.13 ±0.2
a-Si/SiO_x	6.97	4.61	0.90	+0.6 ±0.2
a-$Si/SiO_x/SiN_x$	5.51	2.94	1.47	+3.15 ±0.2
AlO_x (FGA)	-	6.56	0.22	-3.2 ±0.2
AlO_x /SiN_x (FGA)	-	2.41	-	~ -5 ±1

An assessment of the current leakage of these dielectric systems was conducted by recording the current voltage characteristics as the gate bias was varied. This is presented in Figure 2.c. Here it is evident that SiO_2 presents the lowest amount of charge leakage, as expected from its high resistivity. Structures with a-Si and AlO_x, on the other hand, show low resistance under positive bias as seen by the large increase in current in the right of Figure 2.c.An estimated film resistance in this regime is ~300 Ω. Despite this, it is clear that this methodology allows accurate variation of the surface potential in these films. This method is thus viable for layers with high leakage currents. In contrast to the recently developed PL method and other reported techniques to control surface carrier density, with this technique the surface recombination parameters can be extracted without careful calibration of the PL signal, 2D modelling of the carrier flux in the structure, or carefully tuned deposition of metal electrodes.

Conclusions

In this communication an easy and reliable technique to control the surface potential of dielectric-semiconductor systems is presented. Its main advantage is the use of a semi-transparent PEDOT:PSS gate that allows the use of photogeneration in the underlying semiconductor. This provides the possibility of conducting photo-conductance lifetime measurements as a function of specimen surface potential. It offers a new technique to study interface recombination as a function of surface carrier population, the built-in potential from charge or the work function of dielectric layers, and dielectric charge conduction mechanisms.

Supporting Information
All carrier dependent effective lifetime files are provided to aid future work on modelling carrier-dependent interface recombination in silicon. These can be downloaded from http://ora.ox.ac.uk.

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