

# Phase Modulation and Amplitude Modulation Interconversion for Magnonic Circuits

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Magnonic circuit elements generally operate using signals that are either amplitude or phase modulated. We propose a simple all-magnon circuit element capable of converting between these two types of encoding, and support our design with simulations. We highlight the potential of our technique to augment existing devices and propose an alternative schematic for an “equality” gate and exclusive NOR gate.

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## I. INTRODUCTION

Magnon-based computing is an emerging field of study, which aims to advance information processing beyond current CMOS technology [1–9]. The limits of Moore’s law are rapidly being approached [10], and a new computing paradigm is required to help stave off the impending computational crisis caused by the overheating of progressively smaller silicon-based transistors. Magnonics is one such technology. Magnon-based logic circuits utilize spin waves, whose quanta are called magnons, to perform complex computational processes using a fraction of the energy and space required by conventional circuitry and with potentially enormous clock speeds [1]. With its current trajectory, magnonics looks to augment this conventional circuitry with specialist designed-for-purpose microcircuits that can outperform standard devices. Several key elements of these circuits have so far been developed [1, 11–14], some of which are discussed below.

One aspect of these device elements whose significance is often neglected is the method by which data is encoded in the magnonic signal. For some devices, such as the majority gate [13], the digital data is encoded in the phase of the magnons, whereas for others, such as the all-magnon transistor [11], the amplitude is the relevant quantity. The ability to drive the input of one component with the output of another—regardless of the type of signal modulation used—is desirable, as this would provide the flexibility for future designers of larger, more complex magnonic circuits to utilize the full spectrum of components available to them. It is therefore necessary to create a device that can convert between phase-modulated (PM) and amplitude-modulated (AM) signals to enable the concatenation of magnonic circuit elements. Some conversion methods have already been proposed [15], however, these

require external electronics. In this paper, we propose an all-magnon-based method for PM to AM (P2A) and AM to PM (A2P) conversion.

Unlike in conventional computing, where data is stored in the scalar quantity of voltage, the fundamental unit of magnon-based logic is the complex number, representing the phase and amplitude of the spin wave. As we discuss the use of two different methods by which binary data can be encoded into these complex numbers, it is convenient to shift away from the nomenclature of purely 1s and 0s, and move to a system that provides the flexibility to discuss both modulation techniques simultaneously. The phase and amplitude of a magnon with respect to a reference source can be recorded in the form

$$\xi = \zeta(R, \theta, \phi) = Re^{i(\theta+\phi)},$$

where  $\theta$  encodes the phase-modulated binary state, which for one such implementation takes the values of 0 or  $\pi$ , and  $\phi$  is a controllable phase offset.  $R$  represents the relative magnitude of the signal. If  $\phi$  is set to 0, the phase-encoded binary states can be written as  $\zeta(R, \{0, \pi\}, 0) = \{-R, R\}$ . For amplitude modulation, the signal is either zero or nonzero, and can take any phase, and can be written as  $\zeta(\{0, R\}, \theta, \phi) = \{0, Re^{i(\theta+\phi)}\}$ . By combining phase and amplitude modulation and setting the amplitude to 1, a simple example of a three-level mixed-modulation system with  $\zeta(\{0, 1\}, \{0, \pi\}, 0) = \{-1, 0, 1\}$  is obtained, which is a useful starting point for the discussion below.

A method of converting between phase- and amplitude-modulated signals is proposed as follows: both types of converters work by interfering two magnon channels at a junction, with the incoming data signal entering from one of the input branches [Figs. 1(a) and 1(b)]. The other input comes from a pure tone continuous magnon source with a specific phase and amplitude.

For the P2A conversion where the signal input takes the values of  $\xi = \{-1, 1\}$ , the continuous-wave input is

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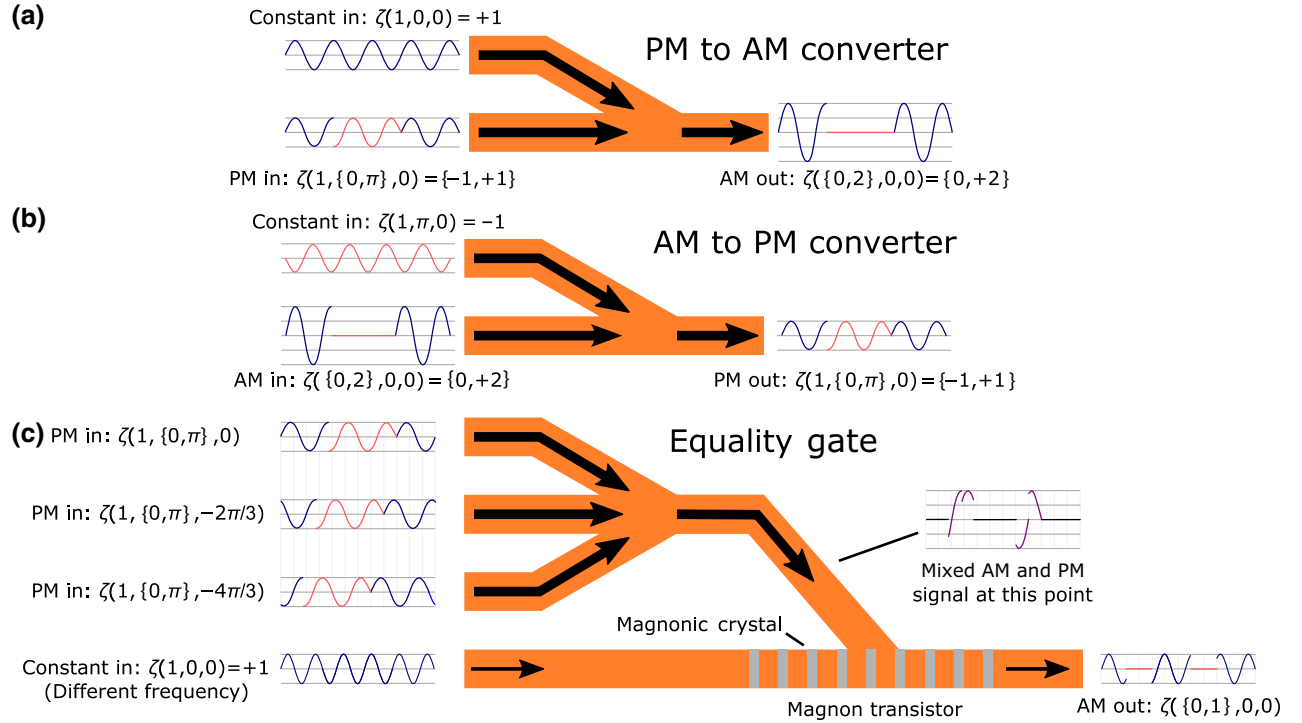


FIG. 1. (a) Schematic of the P2A converter with example waveforms. Binary 1s and 0s are indicated in red and blue. (b) The A2P converter, again with example waveforms. (c) Schematic of the equality gate, which takes a similar form to the majority gate [13], followed by the all-magnon transistor [11]. The three input channels are each separated by  $2\pi/3$ , and the output is 1 when all three inputs are in the same binary state.

set to  $\xi = +1$ . When the two pulse trains combine and interfere (constructively for +1 and destructively for -1), the output will be an amplitude-modulated signal with  $\xi = \{0, 2\}$ , which can be attenuated if necessary [Fig. 2(b)]. The reverse process (A2P) works by setting the continuous input to -1. In this case, an AM-signal input of  $\xi = \{0, 2\}$  results in a phase-modulated output of  $\xi = \{-1, 1\}$ , which can be amplified if required.

By controlling the phase and amplitude of the continuous pure-tone magnon source, additional functionality is available. For example, this method can be used to convert between different types of phase-modulated signals, such as the PM signals used in [15], which use a modulation of  $\theta = \{0, \pi/2\}$ . By adding a continuous signal with  $\zeta(\sqrt{2}/2, 0, 5\pi/4)$  to the  $\pi/2$  phase-modulated signal of  $\zeta(1, \{0, \pi/2\}, 0)$ , a new PM signal with  $\zeta(\sqrt{2}/2, \{0, \pi\}, -\pi/4)$  can be obtained, which we note has  $\Delta\theta = \pi$  [Fig. 2(c)]. This technique can also be used as an amplitude modulated NOT gate by simply adding a wave with  $\xi = -1$  to an AM signal with  $\xi = \{0, 1\}$ .

## II. SIMULATIONS

To demonstrate the functionality of the A2P and P2A converters, numerical simulations are performed using the MuMax3 software package [16]. Due to the similarity

between the geometry of A2P and P2A converters and the majority gate, the work of Klinger *et al.* [17] is referenced heavily during the creation of our model.

Yttrium-iron-garnet (YIG) films of thickness 100 nm are simulated with the following material parameters: saturation magnetization,  $M_s = 138.6 \text{ kAm}^{-1}$ ; exchange constant,  $A_{\text{ex}} = 3.5 \text{ pJm}^{-1}$ ; and Gilbert damping parameter,  $\alpha = 5 \times 10^{-4}$ . An external magnetic field is applied perpendicular to the plane of the film with a magnitude of 200 mT. The size of the cells used for the simulation are  $14.6 \times 9.8 \times 100 \text{ nm}^3$ .

The geometries used for the simulations can be seen in Fig. 3. Each waveguide is  $1\text{-}\mu\text{m}$  wide, and intersects the other waveguides at an angle of  $20^\circ$ . The two intersections in Fig. 3(d) are also staggered. These geometries are chosen as they have been shown to lead to a more efficient transfer of energy into the output channel [17].

Magnons of frequency 1.5 GHz are generated in each of the input arms of the device by applying an in-plane circular perturbation to the magnetic field localized to narrow (100 nm) strips across each input branch of the waveguide. By controlling the relative amplitudes and phases of these perturbations, it is possible to calibrate each device for optimal functionality. The simulations are run for 200 ns and the magnetization state of the system is recorded every 100 ps.

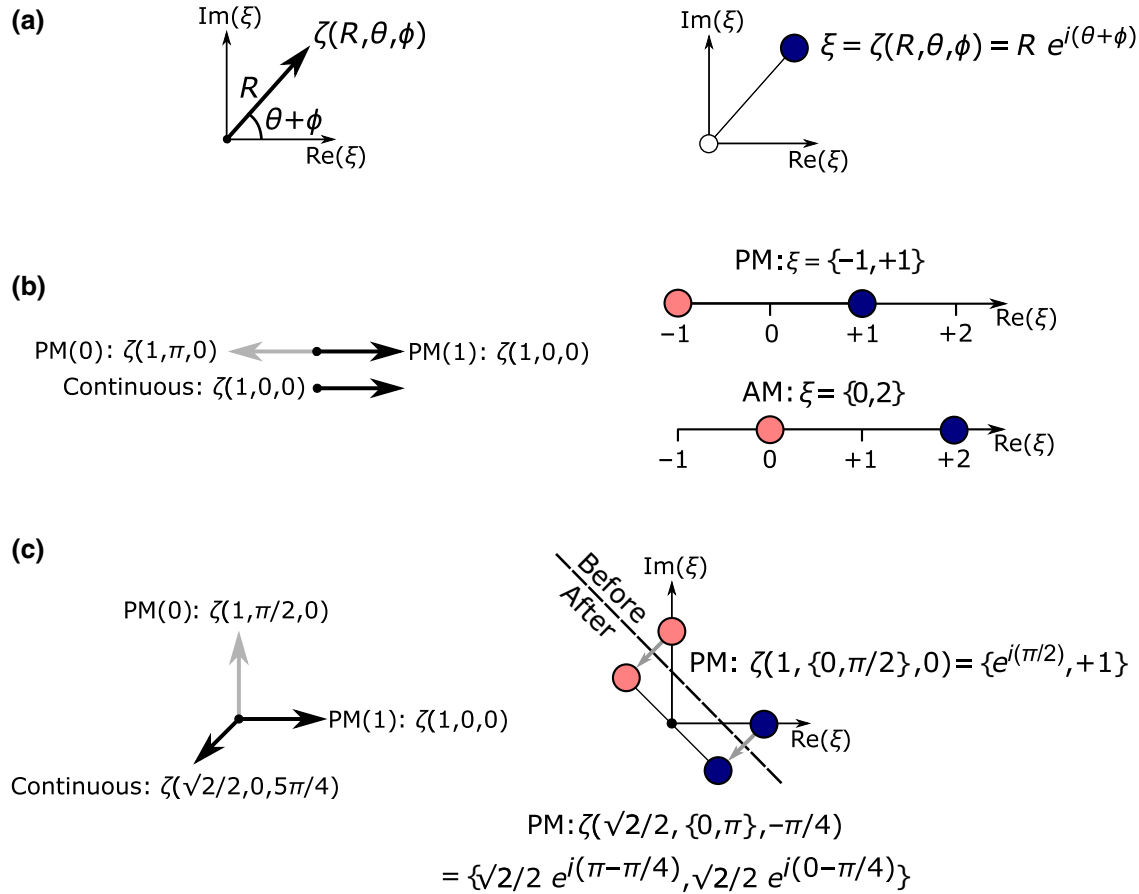


FIG. 2. (Left) Vectors in the Argand plane representing input states. (Right) The possible output values of  $\xi$  for the given inputs, plotted in a constellation plot on the Argand diagram. (a) Representation of a general  $\xi = \zeta(R, \theta, \phi) = R e^{i(\theta + \phi)}$ . (b) The P2A converter. The vectors labeled PM(1) and PM(0) represent the two phase-encoded logic states. Their corresponding  $\zeta$  values are also shown. The two possible PM inputs ( $\xi = \{-1, 1\}$ ) and the two possible AM outputs ( $\xi = \{0, 2\}$ ) are shown in the two constellation plots on the right. (c) Example of phase-to-phase modulation transformation in which a PM signal with  $\zeta(1, \{0, \pi/2\}, 0)$ , (which has a  $\Delta\theta = \pi/2$ ) is converted to a new PM signal with  $\zeta(\sqrt{2}/2, \{0, \pi\}, -\pi/4)$ , which has a  $\Delta\theta = \pi$ .

To incorporate the AM or PM signals into the simulation, one of the inputs is modulated at a frequency of 10 kHz by periodically reducing the amplitude of the perturbing magnetic field to 0 or by shifting its phase by  $\pi$ . Modulating at such a low frequency allows the system to settle into a steady state before transitioning to the alternative configuration. This provided the opportunity to clearly observe the behavior of the magnons as the system toggles between the two binary inputs.

Results of the simulations can be seen in Figs. 3(a)–3(c). Videos of the simulations can also be found in the Supplemental Material [18]. In the top two figures, the P2A conversion is demonstrated, whereas A2P is shown in Fig. 3(c). These images show each of the systems at the appropriate time after the binary state of the modulated input is switched, such that the point of switching coincides with the dotted black line. The significantly reduced amplitude of the signal after the black line in Fig. 3(a), and before the black line in Fig. 3(b) demonstrates the viability

of the P2A converter. In Fig. 3(c), the two consecutive red lobes either side of the black line indicates a  $\pi$  phase shift, as expected in the A2P converter. Together, these simulations provide a proof-of-concept of the A2P and P2A conversion devices.

### A. Other applications and potential devices

The  $\zeta$  notation introduced above can be used to describe the behavior of other magnonic devices, such as the interference-based PM-input majority gate:

$$\begin{aligned} & \zeta(1, \{0, \pi\}, 0) + \zeta(1, \{0, \pi\}, 0) + \zeta(1, \{0, \pi\}, 0) \\ &= \zeta(\{1, 3\}, \{0, \pi\}, 0) = \{-3, -1, 1, 3\}. \end{aligned}$$

This output is recognized as a mixed-modulation state, which means that using it to drive subsequent devices that expect either a pure AM or pure PM input may lead

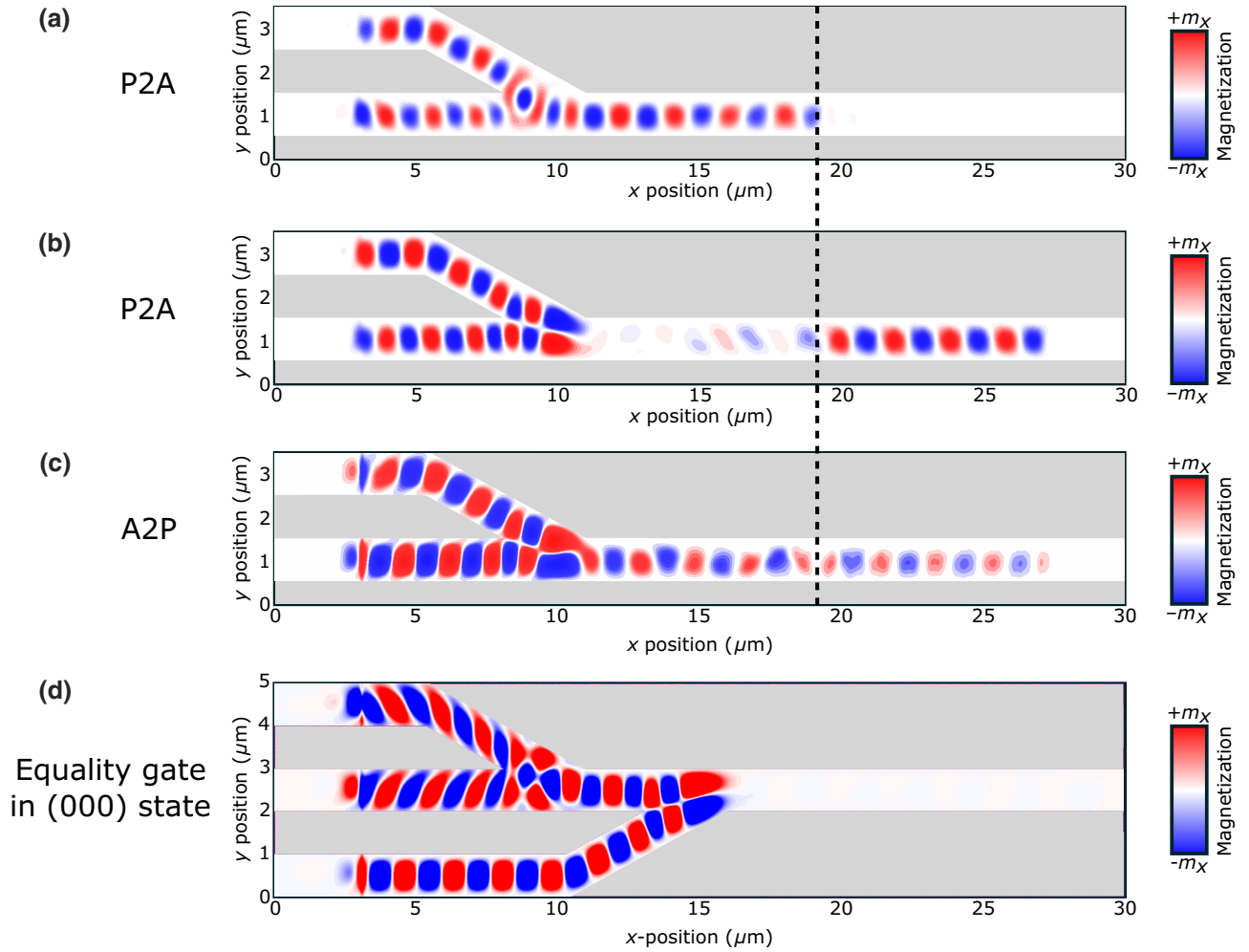


FIG. 3. (a)–(c) Simulations of the P2A modulation and A2P modulation converters. The magnitude of the  $x$  component of the magnetization is indicated by the color bar. The dotted black line indicates the point at which the binary input signal changes from one value to the other. In (a),(b), the AM output is evident in the significant change in amplitude between the two states. In (c), the two consecutive (red) lobes of positive  $m_x$  either side of the dotted line shows the  $\pi$  phase shift expected in a PM signal. (d) Simulation of the first half of the equality gate for the 000 input state. The three inputs have equal amplitude but are shifted by  $2\pi/3$  relative to each other. Due to the destructive interference between the three signals, the output amplitude is 0.

to unexpected behavior (e.g., a majority gate driven by the output of a majority gate will not function correctly without additional components that reduce the  $\xi = \pm 3$  states to  $\xi = \pm 1$ ). Although the generation of these mixed-modulation states appears to be problematic, they may in fact offer an opportunity for some unconventional logic operations.

The equality gate has the same appearance as the majority gate followed by an all-magnon transistor [Fig. 1(c)], and uses PM inputs with  $\theta = \{0, \pi\}$ . The key difference in this device is that the three input channels are each separated by a fixed phase of  $\Delta\phi = 2\pi/3$ . This phase shift can be created by altering the relative path lengths of each magnon channel before they reach the device. The eight possible output states from the majoritylike section can be

written in the  $\zeta$  notation as

$$\begin{aligned} & \zeta(1, \{0, \pi\}, 0) + \zeta\left(1, \{0, \pi\}, \frac{2\pi}{3}\right) + \zeta\left(1, \{0, \pi\}, \frac{4\pi}{3}\right) \\ &= \zeta\left(\{0, 2\}, \left\{0, \frac{\pi}{3}, \frac{2\pi}{3}, \pi, \frac{4\pi}{3}, \frac{5\pi}{3}\right\}, 0\right). \end{aligned}$$

They can also be displayed diagrammatically in a constellation plot on the Argand diagram [Fig. 4(a)]. If we define that logic 1 relates to  $\theta = 0$  and logic 0 with  $\theta = \pi$ , it is possible to use conventional logic notation to assist with the interpretation of Fig. 4.

In Fig. 4(a), the two states for which all three inputs take equal logic values (111, 000) lie on the origin ( $\xi = 0$ ), whereas the other six states lie on a circle with a constant

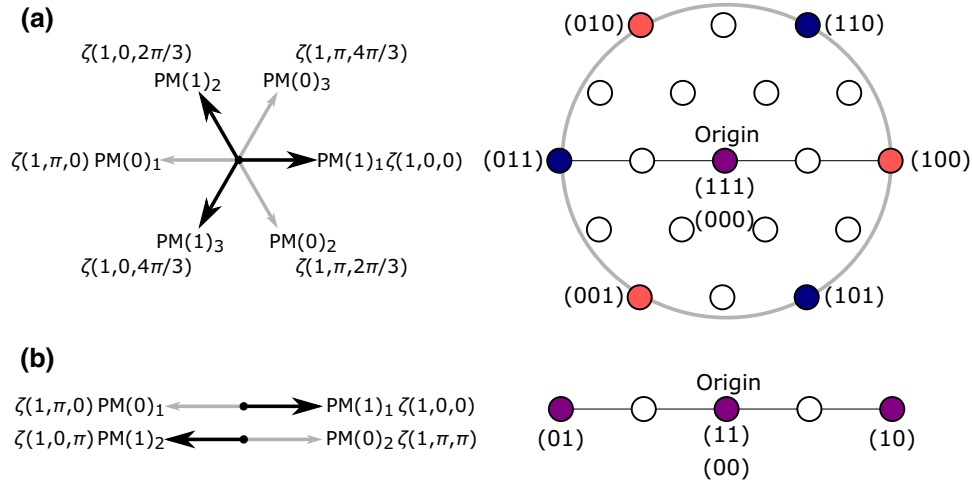


FIG. 4. (Left) Vectors in the Argand plane representing the input states and (right) the possible output states on a constellation plot on the Argand diagram relating to (a) the equality gate, prior to rectification in the magnon transistor and (b) an exclusive NOR (XNOR) gate (the two-channel analog of the equality gate) in which two  $\pi$ -separated PM signals interfere at a junction. The input vectors for each channel and each logic state are labeled [PM(binary logic value)<sub>ChannelNo.</sub>] along with their corresponding  $\zeta$ . The output states on the constellation plot are labeled by their binary logic values [e.g. (110) is obtained by adding PM(1)<sub>1</sub>, PM(1)<sub>2</sub>, and PM(0)<sub>3</sub>], and are colored to show which binary state is in the majority (blue for 1, red for 0). States with no majority, or ones that coincide with states of differing majorities are colored purple. The two “equality” states lie at the origin, whilst the other states lie on a circle of constant radius (amplitude).

radius of 2. By extracting the AM information from this mixed-modulation output state, this device is able to function as an equality gate. This operation is performed by the subsequent all-magnon transistor [11].

The magnon transistor uses a magnonic crystal to confine the gating magnons to a specific region of the waveguide. When the gating magnons are present, they increase the scattering rate of any other magnons passing through the crystal, preventing them from leaving. (These magnons must be of a different frequency to the gating magnons, otherwise they would not be able to pass through the magnonic crystal.) When the gating magnons are absent, the continuous magnons are able to flow unimpeded.

As the transistor only relies on the presence of the gating magnons within the magnonic crystal, the phase information of the input signal is irrelevant as the transistor works via scattering, not interference. As the 111 and 000 states have no amplitude and thus no magnons, the transistor will be open and produce an output value of  $\xi = +1$ . The other six states will close the transistor (by the same amount, as they all have the same amplitude of 2) and produce an output of  $\xi = 0$ . These values represent AM-encoded logic, which agrees with the truth table for the equality gate shown in Table I.

Figure 3(d) shows a simulation of the first half of an equality gate with an input state of 000. This means that each of the three inputs have the same amplitude, and are  $2\pi/3$  out of phase with each other. After the three channels have combined, it can be seen that the amplitude of the resultant magnons is 0—the three channels have

interfered destructively as predicted. If a nonequal input state is provided (e.g., 001, where the bottom channel has experienced a  $\pi$  phase shift), it is easy to see that the resultant interference at the second intersection would be entirely constructive. This would therefore lead to a significant magnon amplitude, sufficient to close any subsequent magnon transistor and provide the required logical output from the gate. Videos of the simulations using input states of 000 and 001 are provided in the Supplemental Material [18].

It is worthy of note that this equality gate is not the only logical operation that can be performed by converging

TABLE I. Truth table defining the “equality” operation, and how it can be used in conjunction with a majority, NOT, and XOR operations to produce the output of a full Adder circuit ( $A + B + C$ ).

Inputs			Three-input gates		Full Adder	
A	B	C	Equality (EQ)	Majority (MAJ)	Carry (MAJ)	Sum (EQ)XOR(MAJ)
0	0	0	1	1	0	0
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	1
1	0	1	0	0	1	0
1	1	0	0	0	1	0
1	1	1	1	0	1	1



multiple phase-separated magnon signals before passing to an all-magnon transistor. By changing the number of input channels, and their input phases and amplitudes, other functions are possible. Some of these are immediately useful, such as the XNOR gate, which can be created by using only two inputs channels separated by a phase of  $\pi$  radians [Fig. 4(b)]. We highlight the fact that by combining an equality gate with a majority, NOT, and XOR gate, it is possible to construct a full Adder circuit, the truth table for which is also shown in Table I.

### III. CONCLUSIONS

In conclusion, we present a simple method for converting between amplitude- and phase-modulated magnonic signals using wave interference at a waveguide junction and demonstrate its viability by way of simulations. We describe how this technique can be used to convert between different types of phase modulation, as well as provide the basis for other simple logic operations such as an amplitude-modulated NOT gate. We introduce a notation (the  $\zeta$  notation) to assist discussion of data that has been encoded into both the phase and amplitude of a magnonic signal. We suggest that magnonic circuit elements can be designed that utilize both AM and PM encoding simultaneously, and propose the schematic of two such devices: the equality gate and an XNOR gate. We believe these new circuit elements complement the many already existing magnonic components, and provide a missing piece of the puzzle that enables the sequentialization of magnonic devices.

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- [18] See Supplemental Material at <http://link.aps.org/supplemental/10.1103/PhysRevApplied.11.044065> for video files of the simulations of the A2P and P2A converters, and the equality gate with equal and nonequal inputs.