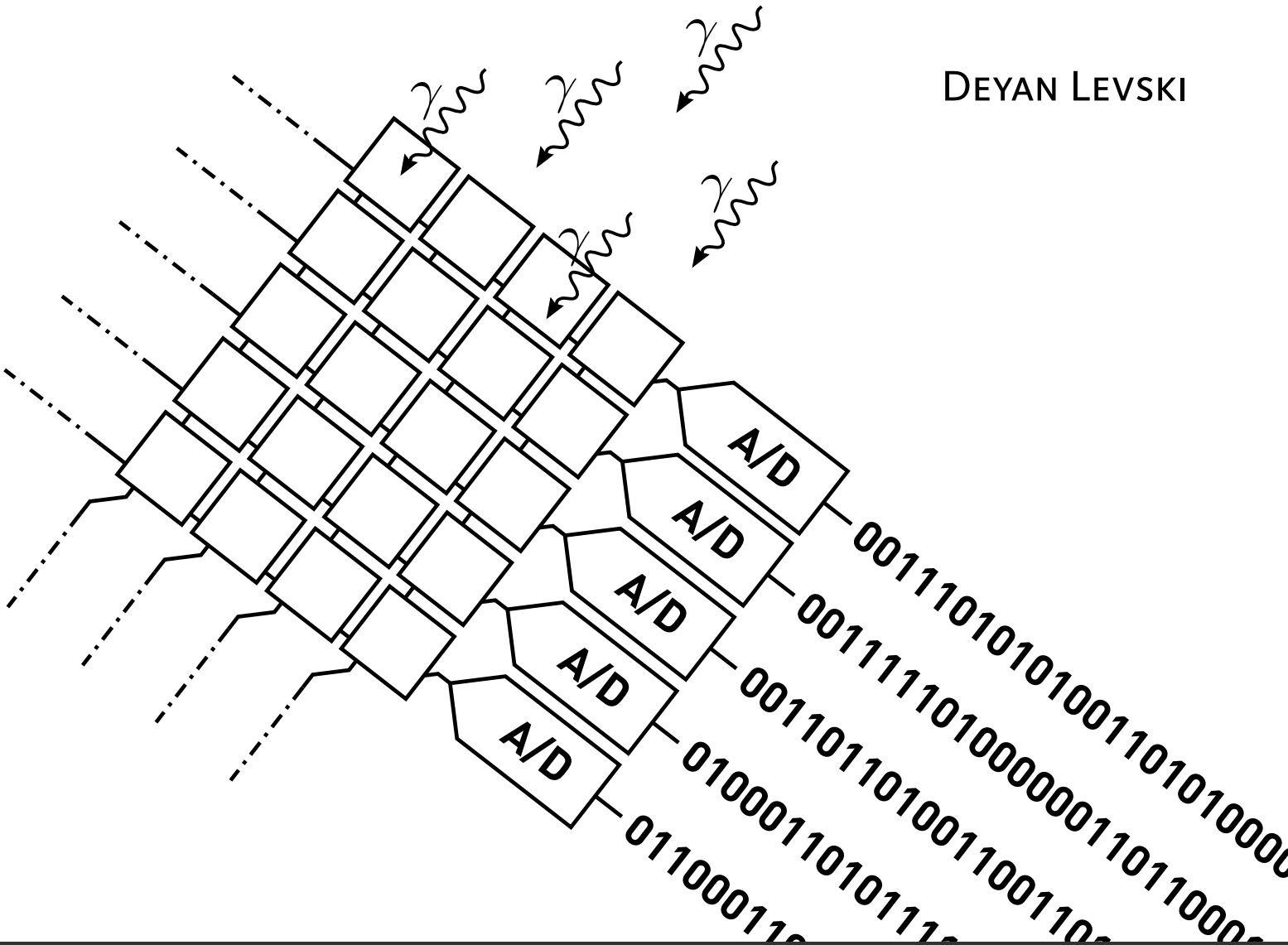
Investigations of

Time-Interpolated Single-Slope Analog-to-Digital Converters

for CMOS Image Sensors

Deyan Levski



D.Phil. Thesis

Microelectronic Circuits and Analogue Devices
Department of Engineering Science
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Investigations of Time-Interpolated Single-Slope Analog-to-Digital Converters for CMOS Image Sensors

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Somerville College

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A thesis submitted for the degree of

Doctor of Philosophy

Trinity 2018

Abstract

This thesis presents a study on solutions to high-speed analog-to-digital conversion in CMOS image sensors using time-interpolation methods. Data conversion is one of the few remaining speed bottlenecks in conventional 2D imagers. At the same time, as pixel dark current continues to improve, the resolution requirements on imaging data converters impose very high system-level design challenges. The focus of the presented investigations here is to shed light on methods in Time-to-Digital Converter interpolation of single-slope ADCs. By using high-factor time-interpolation, the resolution of single-slope converters can be increased without sacrificing conversion time or power.

This work emphasizes on solutions for improvement of multiphase clock interpolation schemes, following an all-digital design paradigm. Presented is a digital calibration scheme which allows a complete elimination of analog clock generation blocks, such as PLL or DLL in Flash TDC-interpolated single-slope converters. To match the multiphase clocks in time-interpolated single-slope ADCs, the latter are generated by a conventional open-loop delay line. In order to correct the process voltage and temperature drift of the delay line, a digital backend calibration has been developed. It is also executed online, in-column, and at the end of each sample conversion. The introduced concept has been tested in silicon, and has showed promising results for its introduction in practical mass-production scenarios.

Methods for reference voltage generation in single-slope ADCs have also been looked at. The origins of error and noise phenomenona, which occur during both the discrete and continuous-time conversion phases in a single-slope ADC have been mathematically formalized. A method for practical measurement of noise on the ramp reference voltage has also been presented.

Multiphase clock interpolation schemes are difficult for implementation when high interpolation factors are used, due to their quadratic clock phase growth with resolution. To allow high interpolation factors a time-domain binary search concept with error calibration has been introduced. Although the study being conceptual, it shows promising results for highly efficient implementations, if a solution to stable column-level unit delays can be found. The latter is listed as a matter of future investigations.

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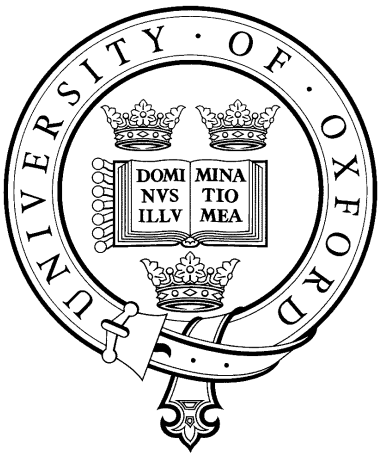

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Acknowledgements

I owe my acknowledgements to a number people, whose encounters have had both direct, and indirect impact on the shape of my world:

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Finally, I thank my family for their support and for always being there with me when I most needed it.

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Abbreviations and Acronyms

AC . . . . . Alternating current
ADC . . . . . Analog-to-digital converter
AFE . . . . . Analog front end
APS . . . . . Active pixel sensor
CDAC . . . . . Capacitive digital-to-analog converter
CDS . . . . . Correlated double sampling
CIS . . . . . CMOS image sensor
CTAT . . . . . Constant to absolute temperature
DCDS . . . . . Digital correlated double sampling
DC . . . . . Direct current
DDR . . . . . Double data rate
DLL . . . . . Delay locked loop
DNL . . . . . Differential nonlinearity
DN . . . . . Digital number
DR . . . . . Dynamic range
DSNU . . . . . Dark signal nonuniformity
FD . . . . . Floating diffusion
FET . . . . . Field effect transistor
FIFO . . . . . First-in first-out
FPGA . . . . . Field programmable gate array
FPN . . . . . Fixed pattern noise
FSI . . . . . Front-side illumination
FTDCSS . . . . Flash TDC-Interpolated Single-Slope
FTDC . . . . . Flash time-to-digital converter
GRR . . . . . Ground rejection ratio
INL . . . . . Integral nonlinearity
ISERDES . . . A serialization and deserialization hardware module found in Xilinx Spartan field programmable gate arrays
LAC . . . . . Look ahead controller

LSB . . . . . Least significant bit
LVDS . . . . . Low-voltage differential signalling
sLVDS . . . . . Sub-LVDS, LVDS with common-mode level lower than the standard of 1.25 V
MIM . . . . . Metal insulator metal
MLM . . . . . Multi layer mask
MPW . . . . . Multi-project wafer
MSB . . . . . Most significant bit
OTA . . . . . Operational transconductance amplifier
PGA . . . . . Programmable gain amplifier
PLL . . . . . Phase locked loop
PRNU . . . . . Photon response nonuniformity
PSD . . . . . Power spectral density
PSRR . . . . . Power supply ripple rejection
PTAT . . . . . Positive to absolute temperature
PTC . . . . . Photon transfer curve
PVT . . . . . Process voltage temperature
QE . . . . . Quantum efficiency
RDAC . . . . . Resistive digital-to-analog converter
RMS . . . . . Root mean square
SAR . . . . . Successive approximation register
SC . . . . . Switched-capacitor
SHR . . . . . Sample and hold reset
SHS . . . . . Sample and hold signal
SH . . . . . Sample and hold
SNR . . . . . Signal-to-noise ratio
SPICE . . . . . Simulation program with integrated circuit emphasis
SPI . . . . . Serial peripherral interface
SRAM . . . . . Static random access memory
SR . . . . . Set-reset
SS . . . . . Single-slope
SiPM . . . . . Silicon photomultiplier
TDBS . . . . . Time-domain binary search
TDC . . . . . Time-to-digital converter
UART . . . . . Universal asynchronous receive transmit
WSS . . . . . Wide sense stationary

1 Introduction

Contents

The history of CMOS imaging dates back to the 1990s, when a team from Jet Propulsion Laboratories in Pasadena, California, investigated ways for reducing the power consumption of CCDs to miniaturize cameras for interplanetary spacecrafts [1]. The target goal for the newly developed technology was to maintain the same high image quality as the one delivered by scientific CCDs in a much more efficient form factor. The group at JPL came up with the idea of integrating passive pixel arrays with an active charge-voltage converting amplifier, a technology which later became known as the Active Pixel Sensor (APS). It was soon realized by the investigators that without significant CMOS process advancements, the APS would not be able to reach scientific CCD image quality – at least not during that decade. However, CMOS was identified to be an excellent technology platform for camera miniaturization, due to its inherent ability for readout electronics integration on the same silicon die. Since this discovery, the group at JPL was also the first to attempt commercialization of this technology. Soon after, an avalanche of scientists and entrepreneurs would begin shaping the world of electronic imaging using the new discovery.

The expanding number of possible applications for the CMOS APS pushed the development of specialized process technologies and readout electronics. With the ever-increasing pixel array resolution and frame rates, it was soon realized that the bandwidth of the data converters was reaching an upper limit, which impeded improvements in APS spatial and temporal resolution. To overcome this limit, engineers invented the column-parallel data conversion and readout methods, which offer better speed-power-resolution performance. This allowed the array upscaling trend to continue its way up. The column-parallel readout architecture remained unchallenged until the late 2000s when new – even higher levels of conversion parallelism were

introduced with the adoption of three-dimensional chip stacking. Unfortunately 3D chip integration, until this day, has had a very slow market share growth due to a number of reasons related to fabrication process complexity. Until 3D-stacking becomes a standard and well-spread process, the only possibility for readout improvement remains in the column-parallel architectures. The imaging community has recently realized a secondary design strategy which offers an additional speed-power efficiency improvement – the group-parallel readout architectures. Together with the not fully explored world of column-parallel designs, and improvements in pixel dark noise which demand higher resolution from the imaging ADC, research in image sensor readout has remained an exciting area for future creativity.

1.1 Motivation and Aim

The primary motivation for investigating the problems of high-speed data conversion in CMOS image sensors is the ever-increasing need for high temporal resolution imagers. The initial problem set for investigation was the concept of CMOS Time-Delay-Integration (TDI) imaging. This thesis would have had a very different trajectory, if ultra-low-noise and high-speed image sensor readout existed, which is required by CMOS TDI.

The initial investigation ideas for this three-year project were set to cover the design of a multi-stage Time-Delay-Integration image sensor, implemented entirely in standard CMOS technology. TDI is a technique often used to improve the temporal resolution of cameras, without sacrificing light sensitivity or dynamic range. By increasing the integration time without changing the imager frame rate, TDI sensors have found their way to industrial applications on a CCD platform. In these applications, the scene objects are in motion, while also possessing very predictable velocities. This led to the adoption of multiple-line CCDs, which naturally use their charge-shifting architecture to perform multiple exposures on the same area of interest. This allows direct integration of the signal, while noise adds with the square root of its magnitude to the final signal – all due to its statistical stationarity. Hence, TDI offers a 3 dB increase in SNR for every doubling of the number of integration stages – one of its head advantages over conventional area-scan imaging [2].

Regrettably, TDI CCDs have a number of disadvantages related to their high power consumption, high manufacturing cost and limitations in camera system integrability. Most of these issues can be solved if TDI linecameras switch their platform to CMOS. Unfortunately, CMOS does not offer the sub-electron charge transfer efficiency of CCDs, which poses immense challenges with TDI CMOS design. Moreover, line-to-line charge transfer in CCDs is order of magnitudes quicker than conventional row readout in CMOS. Thus, these bottlenecks imposed by the CMOS platform require further investigations if it is to be adapted to suit the needs of TDI.

The primary challenge with CMOS TDI is the noisy operation in charge-voltage conversion which occurs every time a row is read. In addition to this, the data conversion operation adds up to the noise chain and slows down signal accumulation significantly (compared to the TDI CCD charge shifting time). While the problem of noise in charge-voltage conversion at the pixel level resides in the hands of semiconductor physicists, the speed-noise challenge could be solved through clever circuit and system-level optimizations of the Analog Front End (AFE) and ADC. This has also been the primary motivation for the investigations presented in this thesis.

High-speed image sensor data converters have been an ongoing area of research with an aim

to solve this imaging bottleneck. The exploration of the single-slope (ramp) ADC architecture was driven by its flexibility and inherent post-processing abilities for CMOS imaging, which no other ADC architecture can offer with such elegance. On the other hand, time-interpolation techniques have gained an increasing interest, due to the favourability of Time-to-Digital Converter (TDC) resolution increase with CMOS process scaling. The past decade has been extremely fruitful for the TDC community as it took the advantage of exploiting the last process nodes, before the end of Moore's law. A way to harness the most of the process node bandwidth is through the employment of an all-digital design shift paradigm.

Due to the above reasons, the core of this thesis aimed to combine both worlds by investigating the use of TDCs as direct interpolators in single-slope ADCs. The investigations culminated in the design and characterization of a high-speed column-parallel TDC-interpolated single-slope ADC, which uses all-digital design methods. While this work does not solve all issues with ADCs for CMOS TDI, it provides a step further to one of the solutions to state-of-the-art high-speed sub-1µs readout.

1.2 Thesis Organization

This thesis is organized in six chapters. In Chapter 2, the principles of time-domain interpolation applied to generic and column-parallel single-slope ADC architectures is reviewed. To provide the reader with a broader ground for comparison, some common column-parallel ADCs used in CMOS imaging applications have also been discussed.

Before introducing the main contribution of this thesis, Chapter 3 prepares the reader with a review of the typical methods for reference voltage generation in single-slope ADCs. The noise on the ramp and its impact on the final ADC output noise has been formalized in detail and a measurement technique for ramp noise estimation has been presented. The problem of comparator kickback noise in column-parallel single-slope ADCs has also been further addressed.

The core of this thesis is presented in Chapter 4. A single-slope ADC architecture using Flash TDC-interpolation has been presented. Following a digital migration design paradigm, the main contribution of this work presents a method for Flash TDC digital gain calibration, which relaxes analog design requirements of the clock delay line and its elements. To prove the concept, a 1024x column-parallel ADC has been implemented on a 0.11µm CMOS testchip. Measurement results show high potentials of the proposed architecture for employment in high-speed image sensors.

Chapter 5 presents an evolution of the architecture implemented in Chapter 4, by proposing a theoretical concept which replaces the Flash TDC interpolator with an open-loop time-domain binary search (TDBS) TDC. The latter is expected to provide more power and silicon area savings compared to the Flash TDC. However, there are a number of technical design-related challenges with TDBS TDCs implemented in column-parallel configurations, which have been discussed and planned as future work.

Finally, a summary of the findings produced by this research, along with the coming grounds for future investigations is provided in Chapter 6.

1.3 Contribution

To summarize, the main contribution of this work falls in the field of system-level readout design for CMOS image sensors.

A digital gain calibration concept and radix extraction technique in Flash TDC-interpolated single-slope ADCs has been developed. The concept of gain calibration was proven in silicon through the design of a 12-bit 1µs ramp time 1024 column-parallel ADC array. The column-parallel implementation led to the development of an online calibration technique which uses the existing ADC counters as processing elements with the help of a few timing techniques and low area global calibration blocks.

The noise in single-slope ADCs with emphasis on the sources of thermal and 1/f noise in the continuous-time (conversion) phase has been investigated in detail. The outcome of the investigations lead to the development of a measurement technique in companding PTC-inspired single-slope ADCs.

Follow-up investigations on potential replacement of Flash TDC interpolators with Time-Domain Binary Search TDCs were conducted. A radix correction technique of similar origins to the presented gain calibration concept could be successfully tailored to Time-Domain Binary Search interpolators. The drawbacks and challenges of the TDBS technique have been identified for further research.

The investigations in this thesis were conducted during the period between Oct. 2014 until Oct. 2017. The major findings were presented through the following publications:

I **Deyan Levski**, Martin Wäny and Bhaskar Choubey, "A 1 µs Ramp Time 12-bit Column-Parallel Flash TDC-Interpolated Single-Slope ADC with Digital Delay Element Calibration," in *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. PP, no. 99, pp., June 2018.

II **Deyan Levski**, Martin Wäny, Bhaskar Choubey, "Compensation of Signal-Dependent Electronic Readout Noise in Photodetector Characterization," *IEEE Photonics Technology Letters*, vol., no., pp., 2018, (under review).

III **Deyan Levski**, Martin Wäny and Bhaskar Choubey, "Ramp Noise Projection in CMOS Image Sensor Single-Slope ADCs," in *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 64, no. 6, pp. 1380-1389, June 2017.

IV **Deyan Levski**, Martin Wäny and Bhaskar Choubey, "A 12-bit Column-Parallel Flash TDC-Interpolated Ramp ADC with Online Digital Delay Element Correction," *International Image Sensors Workshop*, R42, Hiroshima, June 2017.

V **Deyan Levski**, Bhaskar Choubey, "On noise in time-delay integration CMOS image sensors," *Proc. SPIE 9891, Silicon Photonics and Photonic Integrated Circuits V*, 989122, 13 May 2016.

VI **Deyan Levski**, Bhaskar Choubey, "A Conceptual 12-bit Time-Domain Binary Search TDC-Interpolated Single-Slope ADC Architecture," *Oxford Circuits and Systems Conference*, 19 September 2017.

Listed papers in preparation:

I **Deyan Levski**, Martin Wäny and Bhaskar Choubey, “A Technique for Measuring Noise in Comparator Arrays”, prepared for submission in *IEEE Transactions on Circuits and Systems-II: Regular Papers*.

II **Deyan Levski**, Martin Wäny and Bhaskar Choubey, "An Active Kickback Noise Reduction Technique for Continuous-Time CMOS Comparators,"

III **Deyan Levski**, "Search Methods in A/D Converters: A Survey"

2

Time-Domain Interpolation in Column-Parallel Single-Slope ADCs

Contents

Single-slope (SS) ADCs have been the most popular ADC architecture in the CMOS imaging field due to their simplicity, convenience in process node stepping and linearity. However, conventional SS ADCs have a 2^N count speed limiting behaviour which has led to the exploration of various improved search architectures based on hybrid principles.

The first notable speed increase method was the use of Double-Data-Rate (DDR) counting which reduces the required count clock cycles by half. In [3], [4], [5] further speed enhancement has been obtained by a transition to Gray code representation in conjunction with DDR counting. This increases the effective quantization steps per clock cycle. As an alternative, dual-step (coarse-fine) SS converter systems have offered a significant leap in conversion rates [6]. However, such systems no longer retain the inherently low DNL of SS ADCs and impose significant challenges to obtain linearity at the interpolation point [6], [7], [8].

Another architectural approach for speed increase are the residual multi-step SS – Cyclic and

hybrid Successive Approximation Register (SAR) architectures. In [9] and [10], a 6-bit SAR-based MSB conversion is followed by a 6-bit SS-based LSB conversion of the residue to achieve a 12-bit final output word. Sharing analog circuits for the SAR and SS ADCs combines the benefits of both architectures by reducing the SAR area while improving the combined SS ADC speed. However, hybrid multi-step Cyclic/SAR – SS converters are more complex due to the additional circuitry involved in residue extraction and re-sampling, which comes at the cost of power and linearity. Multiple-ramp SS architectures have also been explored, offering significant speed improvements, but have a challenging ramp reference design due to stringent ramp-to-ramp and comparator matching requirements [7], [8].

In this chapter, the most usual methods for interpolation of Single-Slope (SS) ADCs are briefly reviewed. In order to introduce the concept a theoretical background on SS ADCs is provided in Section 2.1. To increase ADC speed, we need to understand problems in terms of nonlinearities which may occur, when we increase the clock rate.

To keep clarity we need to understand typical ways to increase data count, while keeping the counter clock the same. Section 2.2 provides a brief introduction to column-parallel SS ADCs and some of their variations used in imaging applications.

In order to build up on existing ADC designs and prepare the reader for the next chapter Section 2.3 provides the foundation of further presented concepts by introducing time-domain interpolation techniques.

2.1 Single-Slope Quantizers

Single-slope (SS) A/D quantizers convert continuous-time voltage signals with the use of a reference clock and ramp voltage. The ramp voltage is used to translate the sampled input voltage signal into a time interval which is then measured by a counter incremented by a reference clock. Fig. 2.1 shows a generalized overview of a single-slope voltage quantizer. At time t=0, the binary counter is reset and the reference voltage is initialized to V_H. As the ramp starts discharging, the continuous-time comparator toggles when the ramp level crosses the sampled input level which stops the counter. Hence, the comparator translates the voltage signal into time which gates the counting process – yielding a digital number (DN).

The quantization step in SS ADC systems is determined by the dynamic range of the counter as well as the ramp reference voltage span used for comparison. The code step in volts can be defined as

$$\Delta = \frac{V_H - V_L}{\frac{T_{s|V_H,V_L|}}{T_{ck}}} = \text{[V/LSB]} \tag{2.1}$$

where T_s is the search time within the ramp voltage span between $|V_H$ - $V_L|$ and T_{ck} is the count clock period.

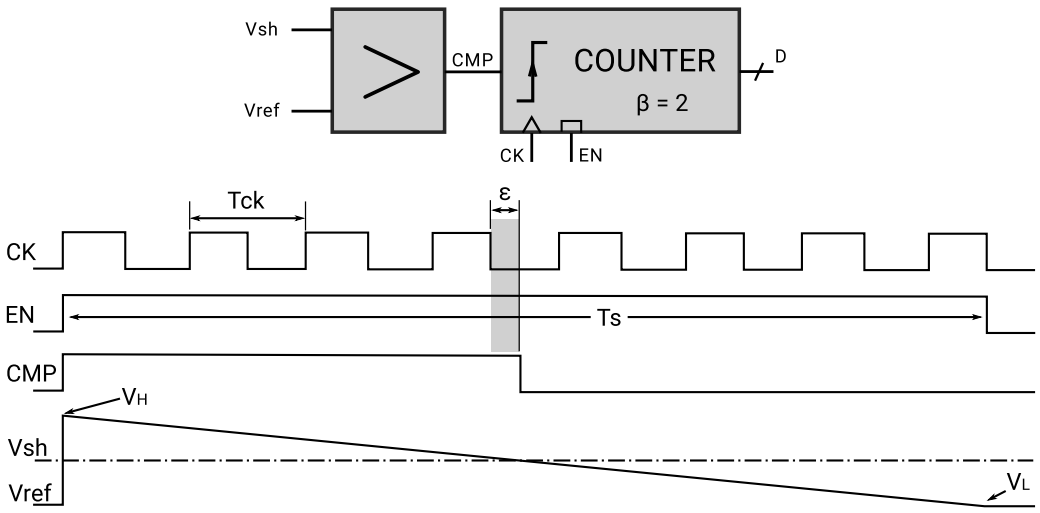


Figure 2.1: Generalized overview of a single-slope voltage quantizer

2.1.1 Ideal SS Quantizers

The search space of an SS ADC is $O(2^N)$, which is of the highest complexity depth amongst all known ADC architectures [11]. Single-slope ADCs form a uniform type of quantizer which rounds the signal and their quantizer function can be expressed as

$$Q(x) = \Delta \cdot \left\lfloor \frac{x}{\Delta} + \frac{1}{2} \right\rfloor = \Delta \cdot \text{floor}\left(\frac{x}{\Delta} + \frac{1}{2}\right) \tag{2.2}$$

where Δ is the quantization step size, which is reciprocal to the maximum search space. Any non-integer real value for x in a uniform round type quantizer would yield an integer-value output, hence the use of the floor function. Thus, the output quantization error for an SS ADC spans between 0 to 1 LSB and is visualized in Fig. 2.2.

The high search space complexity of counter-based SS quantizers by nature does not allow high conversion speeds. However, their property of a rounding quantizer allows an easier implementation of quantization error interpolative measurements, as the start of the next quantized step is strictly defined by the rising edges of the count clock.

2.1.2 Linearity

The simplicity of SS ADCs allows highly linear conversion operations. The full code coverage during the counting process in SS counters provides them with an inherent differential nonlinearity (DNL) of less than ±1 LSB. Differential nonlinearity errors in the range between 0 and 1 LSB are primarily induced by nonidealities in the reference clock, counter latching and voltage-to-time translation errors induced by the comparator.

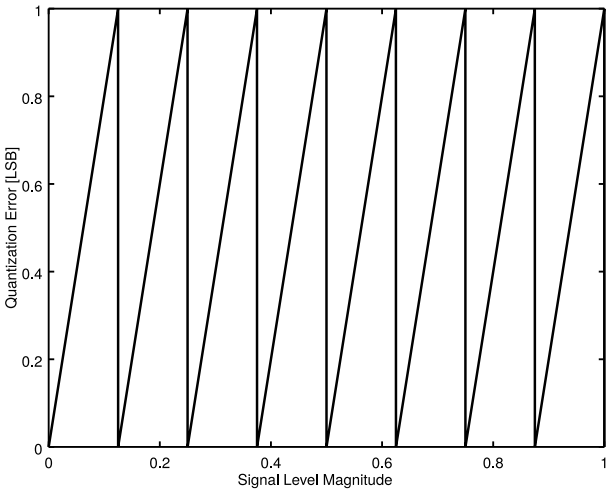


Figure 2.2: Quantization error in a uniform floor rounding type quantizer

Jitter and time-interval errors

High-resolution SS ADC systems, have long count clock periods which causes the accumulation of time-interval errors. Depending on local circuit-dependent parameters, long-term jitter may exhibit deterministic accumulation, which influences the gain of the ADC and translates to integral nonlinearity. Figure 2.3 shows the effect of deterministic time-interval errors on linearity. As jitter erros add up within each cycle, so does the linarity of the ADC drift in the direction of the jitter accummulation. Random Gaussian (nondeterministic) jitter of the count clock does not affect linearity but influences the output noise performance of the ADC.

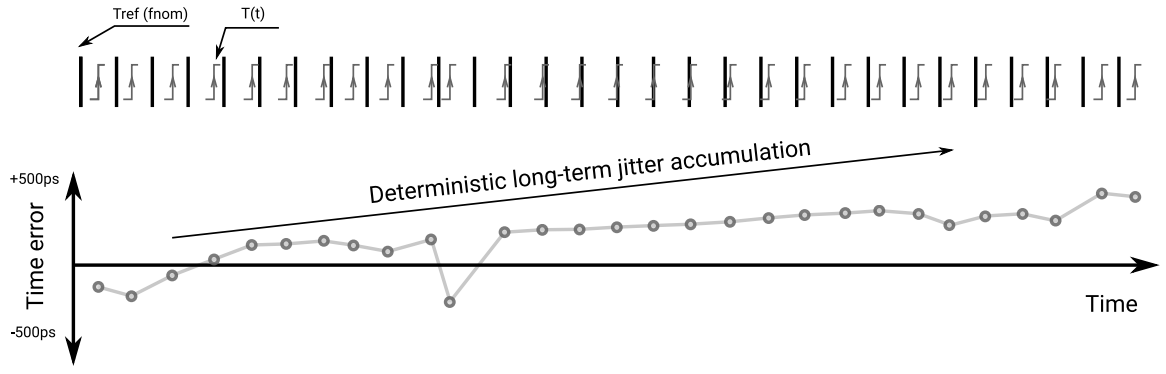


Figure 2.3: Accumulation of long-term jitter

We can define the long-term deterministic jitter impact on the linearity of SS ADCs by defining the time function of the clock signal as

$$T(t) = \frac{\Phi(t)}{2\pi f_{nom}} \tag{2.3}$$

where Φ is the phase and f_{nom} is the nominal clock frequency. Thus, for an ideal clock without

jitter the following relation holds

$$T(t) = t. \tag{2.4}$$

However, a real clock would have a momentary time error $\epsilon(t)$ which can be defined as

$$\epsilon(t) = T(t) - T_{ref}(t) \tag{2.5}$$

where $T_{ref}(t)$ is the ideal reference clock. Therefore, the time $E_{t_0}(t)$ and maximum time-interval $E_{max_{t_0}}(t)$ error are

$$E_{t_0}(t) = \epsilon(t_0 + \tau) - \epsilon(t_0), \tag{2.6}$$
$$E_{max_{t_0}} = \max_{t_0 \le t \le t_0+\tau}[E(t)] - \min_{t_0 \le t \le t_0+\tau}[E(t)]. \tag{2.7}$$

The translation of time-interval errors has a linear relationship with integral nonlinearity (INL). To maintain INL within <1 LSB, the maximum accumulated error E_{max} should be

$$E_{max} = \text{sec/DN} = \frac{T_s}{k \times 2^N} \begin{cases} k = 1, & \text{SDR} \\ k = 2, & \text{DDR} \end{cases} \tag{2.8}$$

where SDR and DDR define whether the counter increments on a single edge or both rising and falling edges respectively. Deterministic time-interval errors are less probable to have a high magnitude for low-resolution SS ADCs due to their short time counting period. However, in high-speed and resolution converters >12-bit, where the used count clock period approaches the magnitude of cycle-to-cycle jitter, accumulated time-interval errors become considerable [12].

Counter metastability

Metastability errors in the counter latch elements lead to bit-errors and eventually differential nonlinearity of the single-slope ADC. Such errors are heavily pronounced when the least significant bit latch metastability is asymmetric. If the comparator stop event occurs when the input state of the counter latch elements reside at their threshold level, a temporary metastable counter state may occur. It stays until the gain of the latch combined with noise induced on the power supply force the latch to settle towards a valid logic level.

If the probability of a latch to settle towards a high or a low output logic level when set at the center of its metastable state is equal, then the latch is said to have a symmetric metastability. Shown on Fig. 2.4a and 2.5a is a symmetric latch metastability response. This is the ideal case which does not introduce additional differential nonlinearity errors, but rather translates to output noise. The x-axis in Fig. 2.5 represents a normalized overlap of the clock and comparator

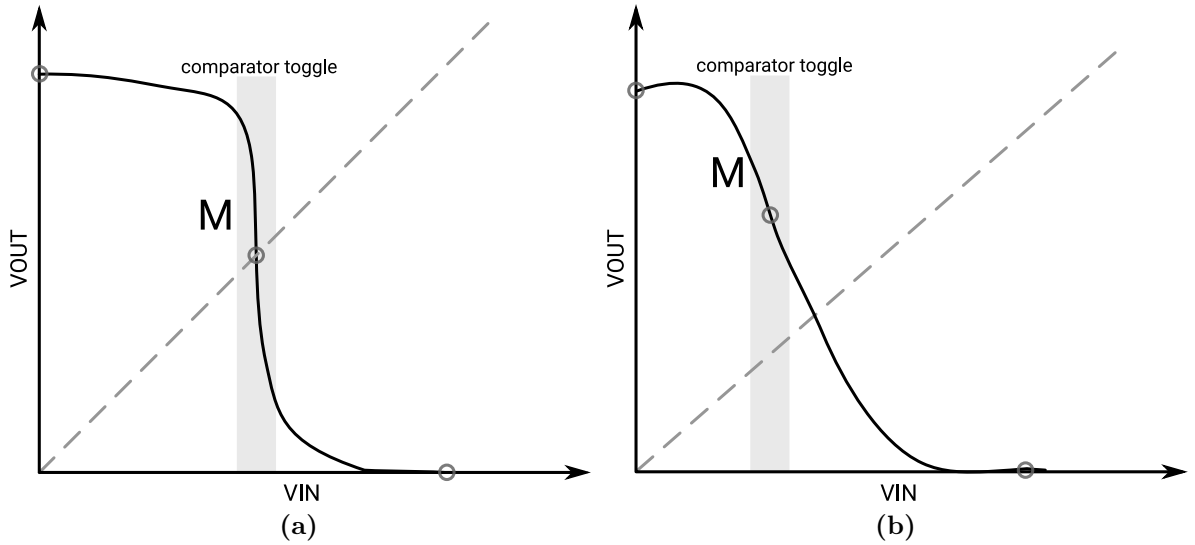


Figure 2.4: Transfer function of typical CMOS inverter-based latches and their metastability points: a) symmetric latch; b) asymmetric latch

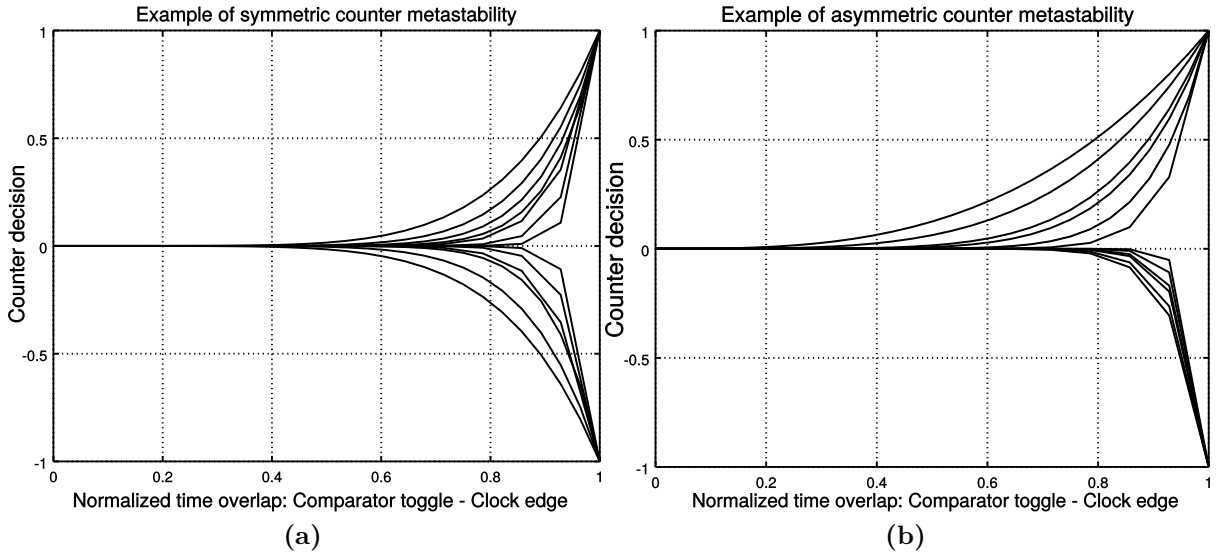


Figure 2.5: Metastability on overlap of comparator gating signal with the count clock: a) symmetric; b) asymmetric

stop signal, while the y-axis shows the counter decision probability of the latch. Figure 2.5b shows the decision probability of a latch exhibiting asymmetric metastability.

It may be noted that asymmetric metastability effectively offsets the count clock from the consecutive ripple-carry incrementation, which leads to DNL errors in a DDR-counter based SS ADC. Asymmetric metastability can be seen as an equivalent to a clock duty cycle error. Methods for hardening metastability errors include; sizing of the P/N FET latch devices for gain-

bandwidth product optimization, keeping short latch feedback paths, minimizing latch transmission gate capacitances, or reduction of Miller capacitances in the inverter latches and other [13], [14].

Clock duty cycle

Single-slope ADC counters which are clock rising edge triggered do not suffer from linearity degradation with drift of the count clock duty cycle. Both rising and falling edge triggered systems (also known as DDR), however, suffer from linearity degradation with the deviation of the main count clock duty cycle from 50 %. Deviations translate to mismatch between the code step width of even and odd-numbered codes. The absolute maximum tolerable duty cycle to maintain DNL of 0.5 LSB can be defined as

$$\epsilon_{\%} = \left(\frac{T_{1/2} \pm T_{1/4}}{T_{clk}} \times 100 \right) - 50 = 25 \;\; [\pm\%] \tag{2.9}$$

where $T_{1/2}$ and $T_{1/4}$ is 1/2 and 1/4 the count clock period T_{clk}, which for a DDR counter yield a <±25 % duty cycle error to maintain a differential nonlinearity of <0.5 LSB. In practical scenarios, the tolerance should be tightened to accommodate other sources of error.

Voltage-time translation errors

The comparator element in a single-slope ADC, together with the generation of the ramp reference effectively forms a voltage-to-time translating block. Systematic voltage-time translation errors result in integral nonlinearity and gain errors, while random time-errors and jitter projects as output noise at the output converted word. The largest source of voltage-time translation errors is caused by nonlinearities in ramp voltage generation. Chapter 3 discusses a few approaches taken to generate a linear ramp reference voltage. Nonlinear comparator response in the form of propagation delay dispersion which is a function of the input signal level is another source of INL errors in SS ADCs.

2.2 Column-Parallel Single-Slope ADCs

In this section we discuss popular approaches and use them as comparison purpose. The Single-Slope ADC is by far the most popular architecture used in column-parallel imaging applications. While there are a number of reasons for this, the most obvious is the simplicity favouring low-area and ease in process scaling. Single-slope ADCs do not rely on high linearity or matching in capacitors (nor they contain any, with exception of the S/H stage). They rely on a linear ramp reference voltage to digitize the input sample. The last is often simpler to implement in a column-parallel form factor compared to Capacitve and Multiplying DAC stages (in the case of a SAR/Cyclic ADC), due to high associated crosstalk and matching requirements between the column capacitors.

Single-Slope ADC Highlights
1. Low area
• consists of a continuous-time comparator and a digital counter
2. Circuit simplicity
• no need for capacitor matching or linearity as compared to Cyclic or SAR as it has no capacitors (excluding S/H stage)
• DNL is guaranteed to be $<$ 1 LSB in a conventional SS ADC provided that there are no bit-errors and metastability in the counter
• uses one continuous-time comparator <-> compared to x2 latched comparators and an OTA in the case of the Cyclic architecture
3. Digital processing
• column-level binary counters allow for inherent processing operations such as DCDS
• simple to intertwine with an ALU to perform additional processing such as CMS, TDI accumulation, DCG combine and other
5. Noise
• noise from the ramp reference voltage directly translates to output noise
• all other ADC architectures perform some form of noise division from the references, example - CDAC in SAR ADCs
• kickback noise on the shared ramp reference voltage is difficult with continuous-time comparators
• single-slope continuous-time comparison (conversion) phase is difficult to model in column-parallel form factors
4. Ease of design
• if conversion time or resolution is not an issue it is easier to design compared to other architectures

Table 2.1: Common aspects of single-slope ADCs

The SS ADC uses a single continuous-time comparator compared to other architectures such as the Cyclic or Delta-Sigma which rely on the execution of multiple parallel comparison and amplification (multiplication) operations. Consequently, the DNL of a conventional SS ADC is guaranteed to be less than 1 LSB provided that there are no occurring bit errors or metastability in the counter – thus possessing an inherently low DNL. A high-level overview is shown in Table 2.1 which provides the most common aspects of SS ADCs, emphasizing on their use in imaging applications.

2.2.1 Common Architectures Reported in Literature

Column-parallel single-slope ADCs have been under development primarily in industrial environments which is evident by the low number of detailed official publications on the ramp architecture compared to individual (single-unit) ADCs such as the SAR, Pipelined, Sigma-Delta, Dual-slope, Flash and others. This section provides an overview of a few common existing column-parallel single-slope ADC schemes, reported as books, papers or patents.

Counter vs latch

Two main approaches can be considered with column-parallel single-slope architectures. A principle diagram of both is shown in Fig. 2.6. In the case of Fig. 2.6a, a global counter can

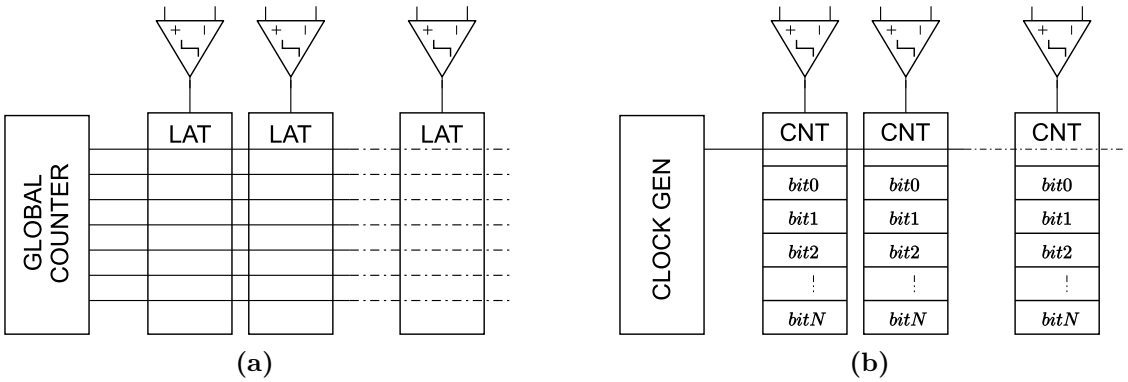


Figure 2.6: Global a) and local in-column counter based scheme b)

be used, which distributes the binary clock values to individual latches located in the columns, while the method in Fig. 2.6b uses local counters per column and a distributed single clock is routed to the array.

The latch method offers lower area, power and higher speeds of operation. This is due to the low diffusion load of the distributed latch elements, which also do not consume any direct path current during count or store mode. However, the local latch methodology does not provide the benefits for in-column signal processing operations which can be easily achieved using local counters. Column counter methods such as in Fig. 2.6b can be easily transformed into simple column-level ALUs used for computations such as digital correlated double sampling (DCDS) or correlated multiple sampling (CMS). However, this comes at the cost of large area and direct path current consumption from all counters during count operation. High non-uniformity of current activity on the power supply causes noise injection and propagation to the sensor readout and pixel. This compromises noise performance and requires careful design – usually achieved through constant current draw counter designs [15], [16], [17].

Coarse-fine multiple ramp scheme

Chip designs based on a multiple-ramp ADC scheme have been previously reported in [7], [8], [18], [19]. These designs distribute multiple ramp voltage references to all columns, instead

of the classic single comparison. An initial fast coarse ramp is applied, which increments a low-resolution binary counter and is also used to determine the position of the sampled voltage to be converted within the reference rails, Fig. 2.7 provides an overview of the concept. After the coarse ramp step, switches inside the column circuitry determine the reference line to be used for the second fine ramp counting phase. After the fine step, the values of both coarse and fine counters are combined together to form the final ADC value.

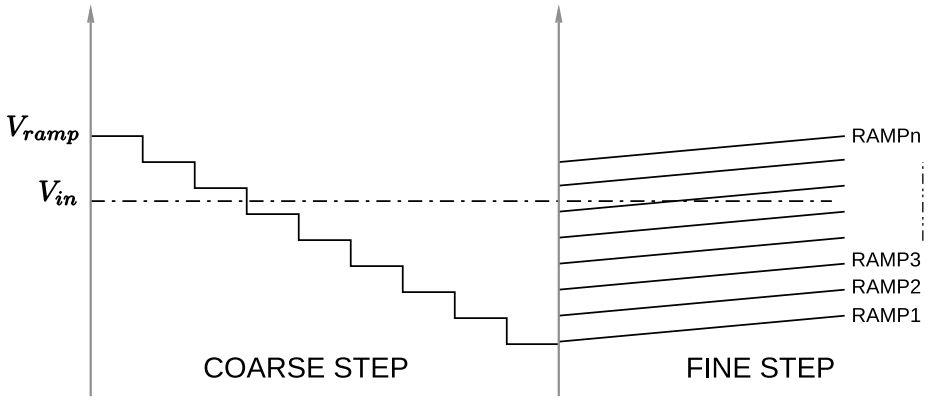


Figure 2.7: Principle timing diagram of a coarse-fine multiple-ramp architecture

The number of used ramps m is equal to a power of two e.g. $m = 2^p$ [7]. In this case, the total conversion time can be reduced to

$$T_{conv} = \frac{2^p - 1}{f_{clk}} + \frac{2^q - 1}{f_{clk}} \tag{2.10}$$

where $p + q = n$, the quickest conversion would be when $p = q$. However, in such a case for a 10-bit conversion, the number of needed ramps would be 32 which is impractical, due to area, power and matching difficulties. A prototype using 8 ramp references has been reported, which achieves a reduction in A/D conversion time of 3x times compared to a traditional DDR single-slope ADC, whilst requiring only $\approx$ 16 % more power in the reported implementation [7].

Look-ahead ramp

Due to the variable conversion time of the Ramp ADC architecture often conversion time is lost due to unnecessary counting associated with unpredictability of the input signal. A design which aims to cope with the nature of this issue has been reported – a look-ahead ramp ADC scheme where the reference lines perform jumps. This forces all columns to toggle in advance [20]. A voltage feedback (analog prediction voltage) is used to sense the highest toggled column and therefore correct the ramp's trajectory end. The concept is sketched in Fig. 2.8

The look-ahead controller (LAC) steers the ramp reference voltage. After an n number of clock cycles, the LAC toggles the ramp generator which adds a predefined offset to the ramp reference voltage, the LAC also controls the global counter which jumps an n number of counts. The predictor circuitry in the column consists of simple AND logic which drives a global prediction feedback. If all comparators have toggled after the short issued ramp ahead, then the conversion

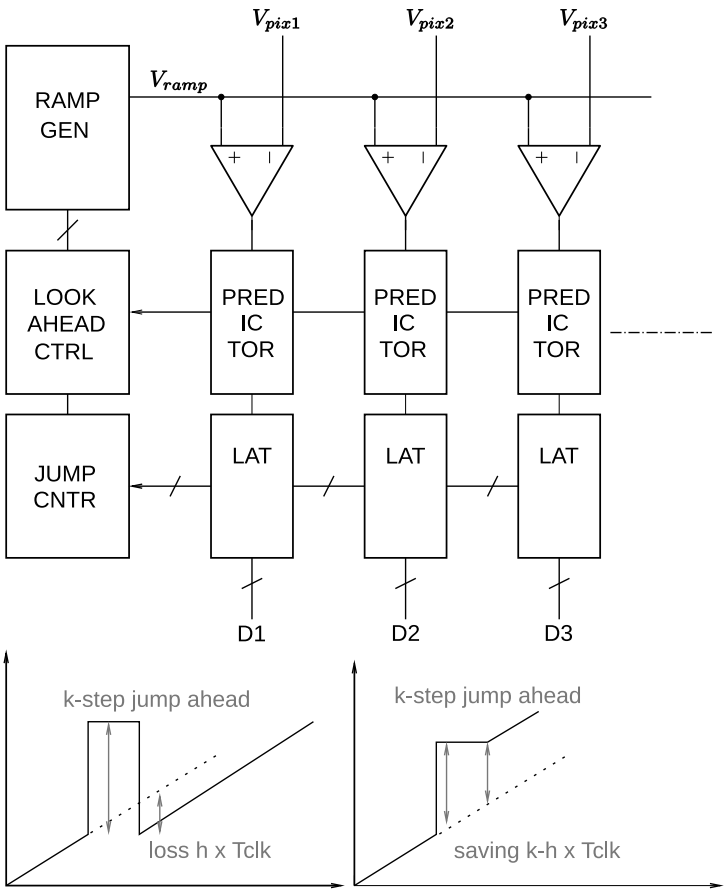


Figure 2.8: Principle schematic diagram of the Single-Slope Look-Ahead Ramp ADC as proposed by [20]

is stopped and finished. However, if only one of the columns appears to toggle directly after the jump, then the LAC returns to the initial jump position minus an h number of steps.

The architecture has signal and spatial information dependent conversion time, which is one of the major system-level drawbacks. On a circuit level, the look-ahead ramp controller adds additional complication to the ramp generator, counter and column-level comparator. When the ramp reference needs to jump back, the already toggled comparators, need to be reset and start with initial conditions the same as the rest of the comparators in the columns or within a maximum of $\pm$ 0.5 LSB error accuracy. This drawback may introduce signal-dependent row fixed-pattern noise FPN which is difficult to correct.

Dual-counter based ramp ADC with one-shot DCDS

A number of dual-counter based Ramp ADCs capable of performing digital correlated double sampling have been reported [15], [16], [17]. The proposed architecture targets to speed-up the column-level ADC by using only one ramp cycle to measure previously sampled column reset and signal levels. It also equalizes current consumption from the counters through alternation of the counting through two counters. Figure 2.9 shows a basic functional timing

diagram of the architecture.

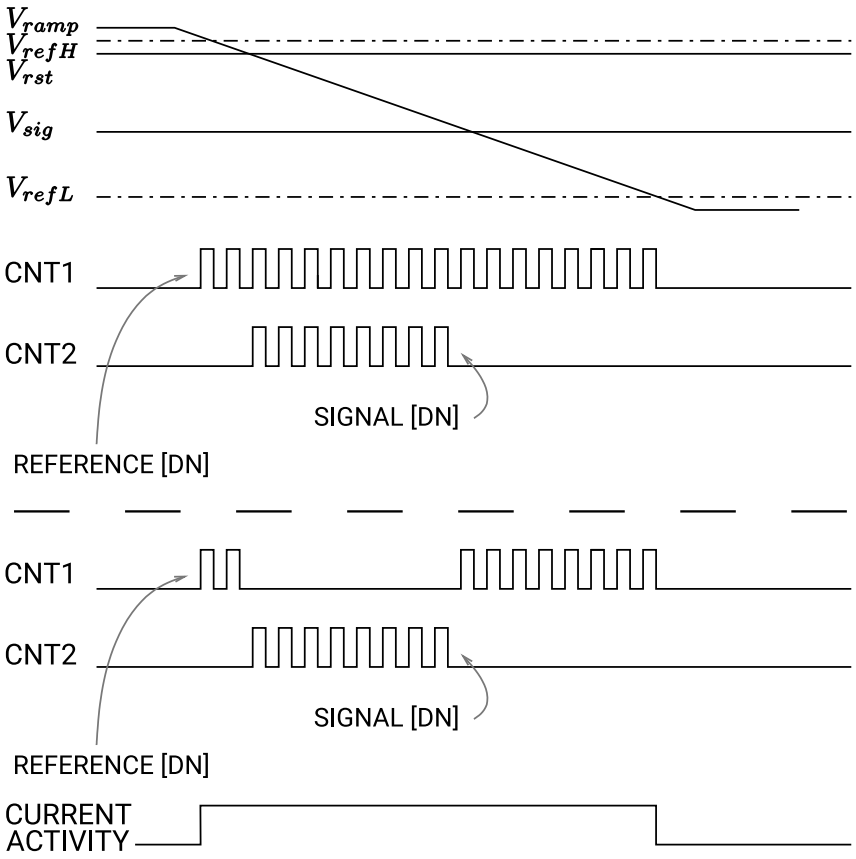


Figure 2.9: Basic functional timing diagram of the proposed by [17] architecture

Two counters count the clock cycles between the reference levels V_{refH} and V_{refL}, as well as the reset V_{rst} and signal V_{sig} levels. The final converted value is then calculated as the ratio of the two counters, or

$$\text{ADC [DN]} = \frac{\text{Signal [DN]}}{\text{Reference [DN]}}. \tag{2.11}$$

Equalizing the current consumption from the counters throughout the whole ADC conversion phase is important in column-parallel configurations, where a very different power consumption activity power can be exhibited. Nonuniform current consumption results in high power supply ripple, which propagates to sensitive analog design blocks. The counter alteration method shown in the bottom of Fig. 2.9 has been proposed as a solution to current equalization in all columns. In the former case, the final converted value is calculated as

$$\text{ADC [DN]} = \frac{\text{Signal [DN]}}{\text{Reference + Signal [DN]}}. \tag{2.12}$$

The final results include implicit digital subtraction of the reset and signal levels (Digital CDS). This is achieved through division of the DCDS result *Signal* with the *Reference*, while the final

result is normalized between the reference voltage ranges V_{refH} and V_{refL}. Having control over the ramp range provides a number of advantages, such as removing the need of having a programmable gain amplifier (PGA) at the front of the ADC if the noise performance requirement of the ADC is low. In addition, integral non-linearity is further reduced, as usually the ramp reference and drivers exhibit a slightly non-linear behaviour within the ramp extremes due to reach of current source saturation margins and channel length modulation.

Multiphase operation period reduced clocks

There have been various attempts at reducing the required number of count clocks to achieve a given resolution through the arrangement of multiphase clocks. Classic Johnson coded interpolation has been reported by [21], [22] while a combination of binary and unary coded counting has been presented by [23], other hybrid interpolation methods have also been proposed [24]. Chapter 4 provides a detailed description of operation period reduced methods.

Photon transfer curve based methods

The main concept behind Photon Transfer Curve (PTC) based ADCs (also known as companding) is to take advantage of the photon shot noise [25]. The required quantization step for an image needs to be fine only at low-light conditions or signal levels respectively. At high light conditions, noise in the readout system is limited (masked) by photon shot noise. As the signal already contains high amount of noise at high light levels, the ADC transfer function can be modified such that a coarser quantization step is used at high signal values, while a fine step at low (dark) signal levels.

The single-slope ADC architecture offers an easy method for generating non-linear quantization step behaviour. A recurring skip of counts at high signal levels can automatically provide higher quantization steps at high signal levels. A primitive thresholding circuit can provide control over the recurring count skipping. The latter can be embedded in the counter, forcing it to count faster by skipping LSB bitcells beyond a certain digital threshold value. In order to smoothen-out the coarse binary steps, some methods add pseudo-random digital noise to the final output ADC word. The PTC based ramp generation is further discussed in Chapter 3.

Other methods

The listed above methods represent some common approaches which modify the classic single-slope architecture. However, the list by far does not provide even a bird's eye overview of the hybrid single-slope ADC field. Hundreds of different combined hybrid approaches exist. This makes this summary a rather ambitious task, which does not fall within the scope of this chapter and had thus been left out.

2.3 The Time-Domain Interpolation Technique

To overcome the count search complexity of the single-slope quantizer, and to reduce the total number of count cycles required for achieving a specific resolution, one can employ methods of time interpolation. This section presents the concepts of time interpolation used in later chapters and provides the reader with a high-level overview of the processes involved.

2.3.1 Refining Quantization Errors

Section 2.1 provided a brief overview of the single-slope quantizer and Fig. 2.2 showed the single-slope quantization error in response to the input signal for a uniform floor rounding type of quantizer. It may be noted that the quantization error is related to the finite time resolution of the counter, which was visualized as ϵ in Fig. 2.1. The method of time-interpolation is based on a consecutive measurement and resolving of the quantization error ϵ. There are two distinct time-interpolation methods of this family which can be identified: direct and time-stretching.

Direct interpolation

As its name suggests, direct interpolation is based on a direct measurement of the quantization error ϵ using a Time-to-Digital Converter (TDC). Fig. 2.10 shows an overview of the concept.

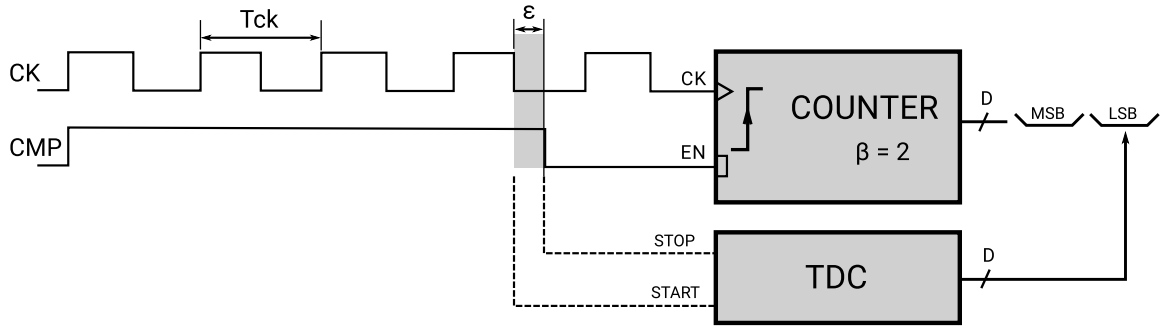


Figure 2.10: Concept of direct quantization error interpolation

A digitizing low Dynamic Range (DR) TDC is started at the beginning of the comparator toggle event, and is stopped by the next encountered count clock edge. The output word of the digitizing TDC forms a fine-count LSB word which can be concatenated with the output word of the single-slope counter. However, a requirement for direct lower-bit word concatenation with this method is that the full DR of the error measurement TDC matches the maximum quantization error range, or:

$$DR_{TDC} = \epsilon_{max} = T \begin{cases} T = T_{clk}, & \text{SDR} \\ T = T_{clk}/2, & \text{DDR} \end{cases} \tag{2.13}$$

where, SDR and DDR denote the counting type – rising, or both rising and falling edge. Failure to match the dynamic range of the TDC leads to a radix mismatch between the upper MSB

word with the lower LSB word provided by the interpolating TDC. The problem of direct word concatenation and radix matching forms the main area of investigations in this thesis.

Time-stretching method

When the count clock period of the counter is small and approaches the gate propagation delay of the used CMOS process, the measurement of ϵ becomes challenging with conventional low ($\approx$ 10 ps) resolution TDCs. To ease small quantization error measurements, an approach which aims to amplify ϵ in time can also be adopted [26].

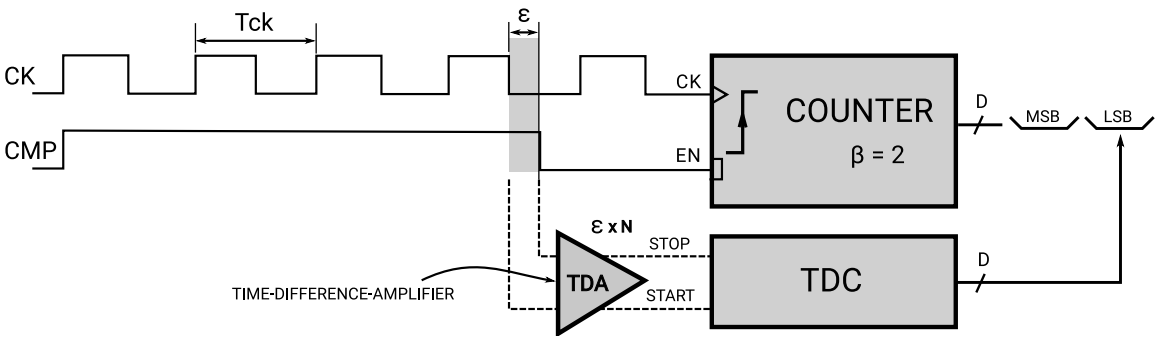


Figure 2.11: Concept of time-stretching interpolation

Figure 2.11 shows a diagram of a time-stretching method. The comparator toggle event and the clock edges to be measured are fed to a time-difference amplification circuit which extends the measured error ϵ to $N \times \epsilon$. A conventional wide dynamic range TDC can then be used to interpolate the error, whose full DR must equal $N \times \epsilon$ to obtain radix matching.

A significant drawback of the time-stretching method stems from linearity degradation caused by the time-difference amplifier [24], [26]. Therefore, this method is only practical when a sub-ps or fine (relative) time resolution TDC can not be employed due to area or power constraints. Alternatively, this method could be used when the count clock period approaches the gate propagation limit of the CMOS process.

Time-stretching remains a valid system-level proposition and method for exploration in future generation CMOS designs possessing fine time resolution [24]. However, at the current stage the design of time-difference amplifiers is challenging due to their exhibited severe nonlinearities which originate from device nonidealities.

2.3.2 Practical Time Interpolators

Although two basic methods for time-interpolation of single-slope ADCs can be identified, there is an abundance of practical schemes for achieving time-interpolation. Here we explore two of the most common implementations of time-interpolators applied to column-parallel architectures.

Gray code interpolation

Gray codes, also known as reflected binary codes are a number representation system in which two successive values differ by only one bit. Historically Gray codes were designed to prevent glitches produced by simultaneous operation of electromechanical relays. Gray together with thermometer codes are commonly used in high-resolution DAC designs to prevent glitches between extreme successive values e.g. "01111" to "10000" [27].

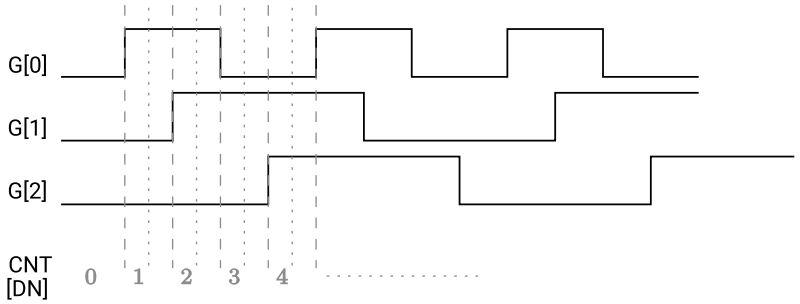


Figure 2.12: Principle of Gray code interpolation

In the case with single-slope ADCs a time-domain interpolation can be performed by extending the count clock of the converter with two (or more) additional period-divided and phase-shifted count clocks. This is also known as Gray code counting [3], [4], [5]. Figure 2.12 shows the basic principle in Gray code bit-extension. The LSB of the Gray code (G[0]) is used to increment a traditional ripple-carry counter. The state of the signals G[0], G[1] and G[2] are stored in a traditional latch on comparator toggle event. The stored Gray code in the latches is converted to a normal binary number and added to the total sum of the conversion. A major advantage of Gray codes is that as shown in Fig. 2.12 the Gray codes can have a twice as large clock period, which relaxes clock distribution and design effort significantly. However, the Gray code scheme is still limited by the maximum frequency of operation of the Gray LSB code (G[0]). It also produces an output gray code which needs a consecutive conversion in binary which is not always convenient in column-parallel implementations [3].

Johnson code interpolation

To increase the counting speed of Gray and traditional binary counting methods, a Johnson code based interpolation scheme could be used. Johnson codes share the same code family with Gray codes as two Johnson adjacent states differ by only one bit. By adding one additional delayed count clock, the resolution of the converter is extended with two additional quantization steps in the case of a rising edge only counting scheme. Similarly, adding two or three additional clocks provides three and respectively four quantization steps. Figure 2.13 shows the basic principle of Johnson code interpolation, also known as Flash TDC interpolation.

For a DDR counting scheme we can note that adding ten delayed clocks (as shown on Figure 2.13) gives us ten additional quantization steps. For the general rising-edge only counting scheme the gained quantization steps within a single bit is doubled. The Johnson code count scheme increases resolution without clock speed increase. However, the latter increases the requirements on the time-domain resolution of the comparator and counter modules. Moreover, to ensure that there are no differential non-linearity (DNL) errors, the individual delays

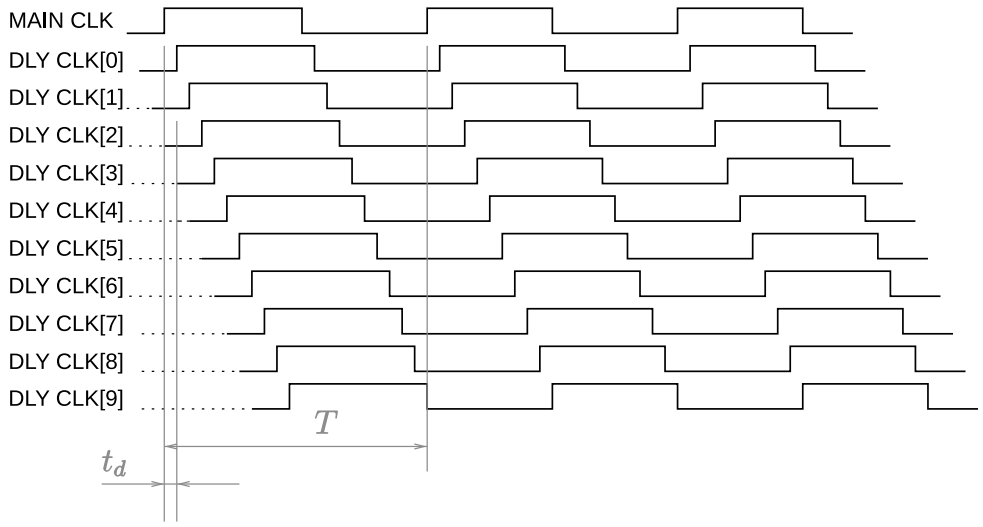


Figure 2.13: Principle of Johnson code interpolation, also referred to as Flash TDC interpolation

must maintain good matching. The theoretical resolution gain of a Johnson scheme based ADC can be expressed as

$$N_{add} = 2 \times n_{johnson} \tag{2.14}$$

where $n_{johnson}$ is the number of delayed clock lines. To maintain DNL $<$ 0.5 LSB the total sum of the delays must lie within:

$$\Sigma_{t_{delays}} \leq \frac{T}{2} \pm 0.5 t_{delay}. \tag{2.15}$$

At very high clock and phase interpolation rates, the requirement on the delay time of a single cell becomes comparable with the intrinsic inverter delay of the CMOS process. In such cases Johnson codes become difficult to implement due to the hard matching requirements at all process voltage and temperature variations. To overcome this problem a correction method has been implemented which is discussed in Chapter 4.

2.3.3 Problem of Time Synchronization

From the previous section it becomes evident that the use of time interpolation requires precise matching of the TDC radix with the single-slope counter. In most practical applications, radix matching is achieved through dynamic phase alignment of the multiple count clocks through the use of PLL or DLL methods [28]. A well-designed locked-loop structure can easily achieve jitter performance of less than 100 ps. However, even small phase misalignment errors of a few tens of picoseconds translate in DNL errors when encountered in a high interpolation ratio design. The consequence of this is illustrated in Fig. 2.14.

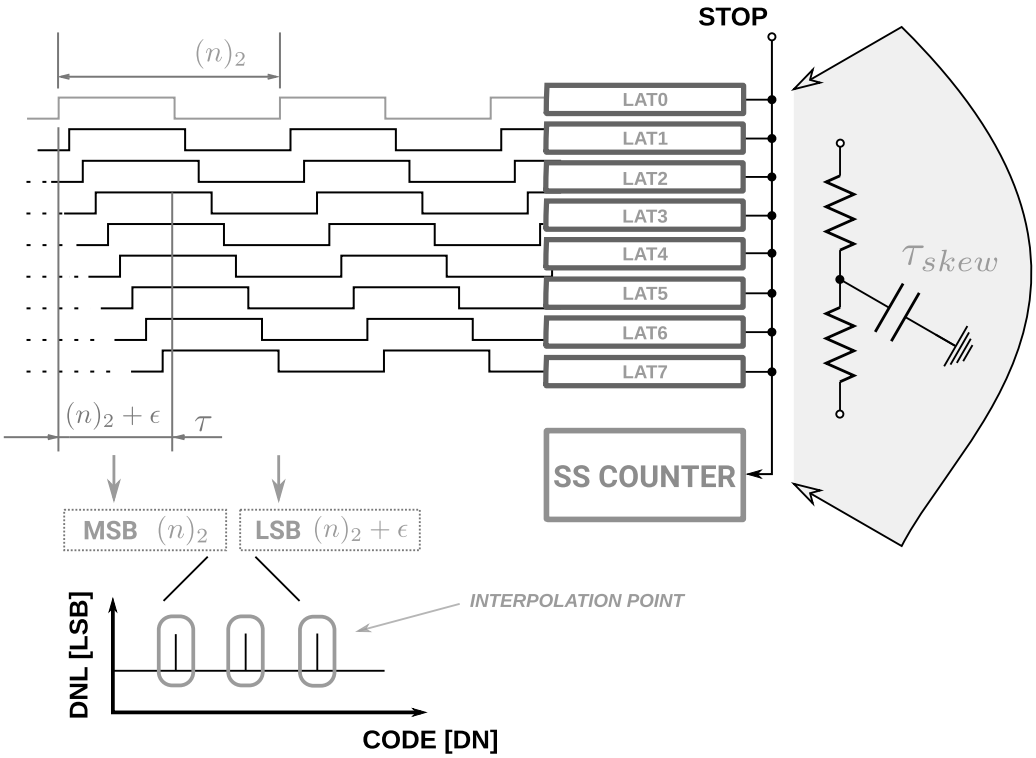


Figure 2.14: Issues with stop time latch synchronization and phase alignment

The main count clock period defines the radix-2 of the binary counter which is indicated as $(n)_2$. The example case shows a set of interpolation clocks whose total delay varies with DLL jitter. Thus, the radix compression of the LSB word translating to DNL errors. With high interpolation ratios, the spatial position of the capturing latches (LAT0-LAT7) introduces stop time mismatch due to physical clock skew τ_{skew}. When the phase-to-phase delay approaches the order of tens of picoseconds the impact of clock skew becomes prevalent. Thus, direct time-interpolation methods of this family would always suffer from DNL errors at the interpolation point codes. However, their magnitude can be suppressed with circuit optimization methods and low-skew oriented design.

2.4 Discussion

This chapter provided a brief overview of the single-slope architecture tailored for use in CMOS image sensors. Conversion time speedup methods using time domain interpolation were presented. While there are other principal methods used to increase speed, time interpolation was chosen for further exploration due to the simplicity of its open-loop single step method. Compared to other methods from the coarse-fine and multiple ramp family methods, time interpolation requires less analog voltage-domain circuitry, but rather more digital discrimination blocks, which benefits process scalability and power. Most voltage-domain interpolation methods, notably the multiple ramp and look-ahead ramp, have very high matching requirements on their reference voltages. A large set of distributed voltage ramps requires high modelling

effort, which is best verifiable through silicon proof.

The design of high-speed time-interpolated single-slope ADCs currently faces two major design challenges. The speed and linearity of the provided ramp reference voltage becomes crucial when high-resolution quantization is required. To address these issues Chapter 3 provides a detailed analysis on ramp references used in column-parallel ADCs.

It was identified in Section 2.3 that the time interpolation techniques require low-skew clock generation and small phase misalignment errors. These challenges are primarily led by clock generation limitations of delay locked loops. Thus, the design of open-loop multiphase clocks have been addressed in Chapter 4. The introduction of a digital gain calibration technique relaxes delay line drift requirements and simplifies the design of the multiphase clock generators.

3

Ramp Voltage References in Column-Parallel Single-Slope ADCs

Contents

The ramp reference voltages of column-parallel Single-Slope (SS) ADCs have a dominant influence on the overall system linearity and gain. The noise in SS ADC architectures apparent on the ramp reference line is directly translated to time-domain noise through the comparator, and appears as output noise in the ADC. High loads and comparator kickback noise on the

shared ramp reference line, influence ADC offset and induce crosstalk between columns. This chapter addresses several ramp voltage generation challenges in column-parallel systems, and provides a theoretical framework on the effects occurring during the voltage-to-time translation phases in SS ADCs.

Section 3.1 presents the most common ramp voltage generator topologies used in column-parallel SS ADCs. Section 3.2 gives a theoretical background on the steady-state noise sources for a generalized case of an SS ADC. Section 3.3 shows how ramp noise translates to output ADC noise during the continuous-time integration phase. An experimental validation and method for measuring noise on the ramp using indirect methods is shown in Section 3.5. Finally, Section 3.6 comments on dynamic noise and errors induced by comparator kickback.

3.1 Ramp Voltage Generator Topologies

The generation of a linear ramp has been typically approached by a few solutions, starting with low-resolution resistive string DACs as in [29], [30]. The output of the DAC is usually low-pass filtered through high-order continuous-time filters, which interpolates the DAC voltage steps to provide a smooth linear ramp response. To achieve high ramp linearity needed in fine-resolution converters of more than 10-bits, the resistive string DAC steps must be increased in a binary-weighted trend, and a very high roll-off DAC interpolation filter must be used.

However, all fine-step DAC and continuous-time filter approaches come at the cost of high power consumption, making them impractical for high-resolution applications. Wide-step DAC solutions shift the design complexity and silicon area from the Resistive DAC (RDAC) to the filter. However, even with this approach, the increase in RDAC element matching requirements for high-resolution are still unavoidable. For this reason, RDAC approaches have been widely substituted by Capacitive DAC (CDAC) structures due to the easier fabrication of well-matched MOS capacitors, which leads to power efficiency and easier design of higher number of quantization steps [31], [32], [33]. To reduce the number of capacitor elements, other topologies using fine C-2C DAC generators have been proposed. The C-2C approach reduces the requirement for number of DAC elements to $3 \times N$. Here, N is the desired resolution of the DAC, which can then be followed by lower order low-pass interpolation filters to smooth the ramp staircase function [33].

Alternatively, due to the aforementioned matching difficulties, the most common solution in the case of larger than 10-bit resolution SS converters is the use of active or passive continuous-time integrator-based ramp generators [34], [35], [36], [37]. In [36] a continuous-time sampled gmC integrator has been used to store a ramp reset (V_r) and end (V_e) voltage on a capacitor. The difference between the two voltages is integrated on a feedback capacitor of a discrete-time integrator. The linearly slewed voltage reference by the integrator is then buffered through a linear driver and distributed to the column comparators. Provided that the integration capacitance and resistances (if used) of the continuous-time integrator are linear, then the sole component introducing nonlinearity and distortion to the system is the integrator OTA.

The following subsections present an introduction to the most common ramp generator topologies for column-parallel SS ADCs, and emphasize on their strengths and weaknesses.

3.1.1 Resistive Flash and C/C-2C DAC-based Topologies

Resistive string Flash DAC and C-2C DAC based topologies can be used to create step voltages for interpolation if the resolution requirement of the ADC is less than 10-bits. This is due to the resistive string matching in typical CMOS processes and reference voltage ranges of about 1 V. Figure 3.1 shows typical resistive flash DAC ramp generator designs [29], [30], [38], [39]. A reference current is fed through a resistive string generating individual voltage steps which are multiplexed to an interpolating filter. The multiplexer is controlled through a thermometer (one-hot code) binary counter which is incremented throughout the counting phase of the SS ADC. The interpolated reference is buffered though a linear amplifier and distributed along the columns.

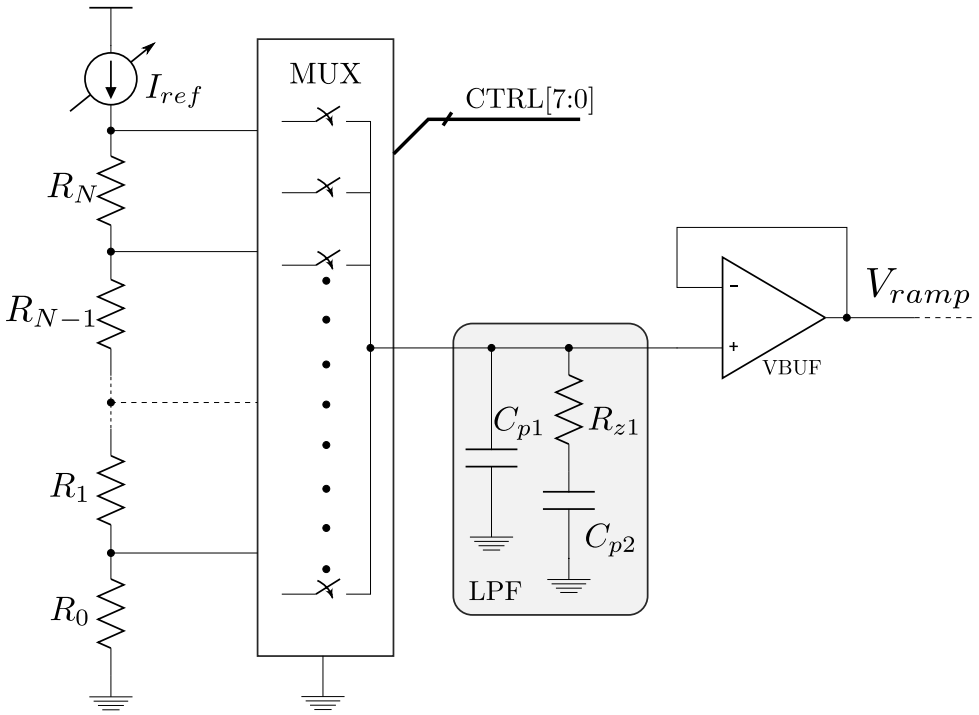


Figure 3.1: Principal ramp generator based on a resistive string Flash DAC

The individual voltage steps can be designed to be smaller than an ADC quantization step as in [39]. Alternatively, the steps can be kept higher with the use of a high-order interpolation reconstruction filter [38]. A variable reference current allows for changes in the step size. An advantage of resistive string architectures is their inherent monotonicity. However, the immunity to power and ground supply ripple in the resistive string is mediocre. This is a consequence of the direct coupling of ground or power supply noise to the system depending on the used resistive structure. Should, current references be used at both ground and supply ends, the DAC system requires a common-mode feedback which further complicates the design.

An alternative approach to DAC-based ramp generation is the use of capacitive DAC structures. In [31] a binary weighted capacitive DAC has been used, while in [32], [33] a C-2C DAC structure is employed. Figure 3.2a shows a principle schematic diagram of a C-2C DAC used as a ramp generator which fed through a voltage buffer to the columns.

The DAC array uses binary-weighted capacitive charge division. The bottom plates of the C

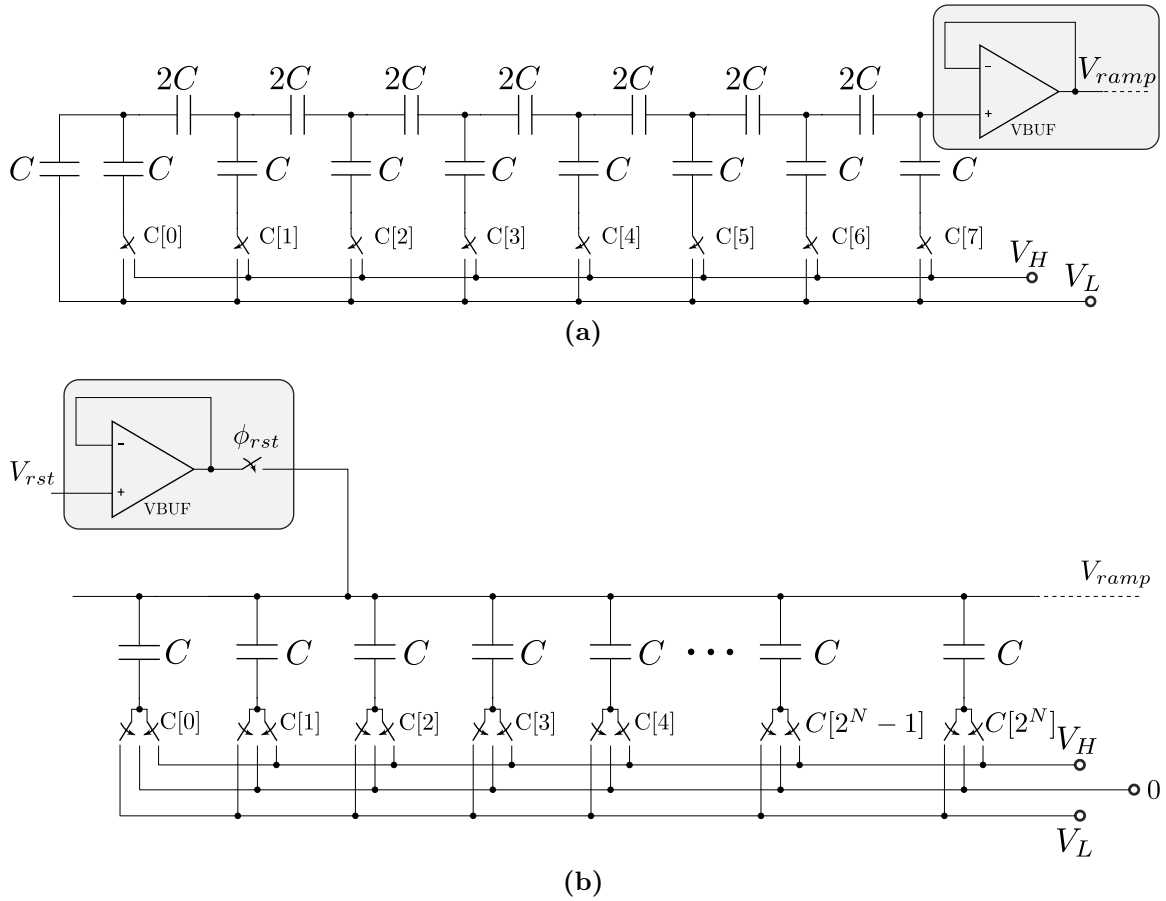


Figure 3.2: Principal ramp generator based on capacitive DACs: a) C-2C DAC buffered, b) CDAC direct coupling architectures.

capacitor nodes are switched between a high and a low reference voltage which causes charge accumulation or depletion. This topology requires high-bandwidth high-accuracy reference voltage drivers in order to maintain linearity. While it is possible to implement a 12-bit resolution capacitive array, a CDAC approach is not commonly found in larger than 10-bit resolution ADC systems due to capacitor matching and settling complexities.

A solution using a Flash-type array [31] of equally sized capacitors is shown in Fig. 3.2b. Due to the large total array capacitance $C_{tot} = 2^N C$ the output of the DAC in Fig. 3.2b can be directly connected to the ramp reference voltage line. The damping between the total comparator drain-gate capacitance and the CDAC is large enough, so that kickback from the comparator does not impact accuracy. The switches of the DAC are closed sequentially in a thermometer-coded sequence, thereby adding an equal amount of charge which lifts the reference voltage line.

Both resistive and capacitive approaches have proved to be sufficient in the case of lower than 10-bit resolution designs at approximately 1 V ramp span. However, high resolution (>10-bit) designs of the R/C DAC topologies become impractical due to stringent component matching requirements.

3.1.2 Switched-Capacitor Integrators

The Switched-Capacitor (SC) integrator has been one of the most versatile electronic blocks since the early 1970s [40]. Figure 3.3 shows a principle diagram of an SC integrator used as a ramp generator. The sampling capacitor C_s of the integrator samples the differential value of two voltages V_1 and V_2 which determine the integrating step. During the second phase, the differential value on C_s is accumulated on the feedback capacitor C_f. The process occurs every clock cycle which gradually causes the voltage at the output node to increase.

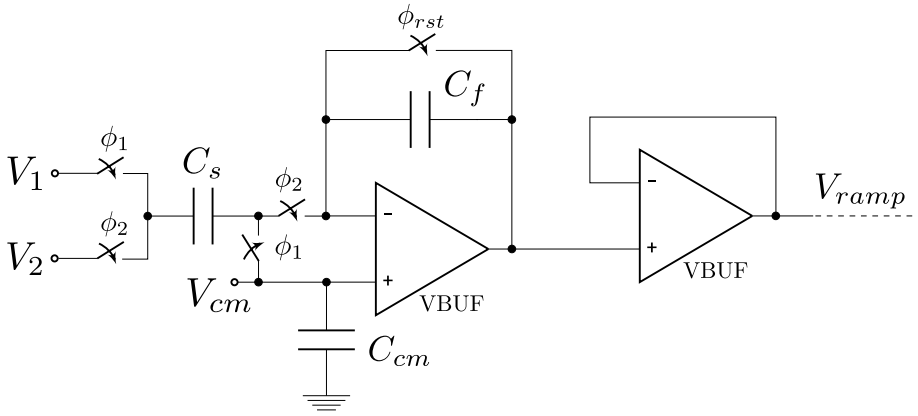


Figure 3.3: A principle diagram of a switched-capacitor integrator

Several designs employing SC integrator based references for imaging have been reported in literature [36], [41], [42], [43]. Common in all structures is the accurate control over the integration step due to the discrete operation. The generation of varying ramp slopes is therefore much easier compared to continuous-time integrator approaches. The noise from the sampled charge which is to be integrated is dampened by the ratio between the sampling and feedback capacitors [40]. This ratio can be easily increased to 100 times, thereby making the kTC noise from sampling virtually zero. However, the major noise source contribution in this approach comes from the SC feedback phase and the OTA. Therefore, SC-integrators do not necessarily have a noise advantage over conventional continuous-time integrators. In addition, any high-speed switching activity during integration adds to the conditions of injecting power supply and substrate noise, which requires additional filtering.

3.1.3 Continuous-Time Integrators

Ramp generators based on continuous-time integrators are another common approach for reference generation in column-parallel ADCs [34], [35], [37], [44], [45]. Depending on the generation method they can be divided into two types. These are global buffered active integrators [37], [44], [45] or local per-column integrators [34], [35].

Figure 3.4 shows a diagram of both structures used in column-parallel ADCs. A global buffered constant-current OTA-based integrator is shown in Fig. 3.4a. During the initialization phase, the OTA feedback capacitor C_f is discharged which resets the integrator. In the consecutive integration phase, C_f is connected in the feedback, while the virtual ground node at the inverting input of the OTA is constantly pulled by a current-mode DAC. The OTA compensates for the deprived charge by correcting its output level which is connected to C_f. This leads to a natural

continuous linear increase of the ramp voltage. This is unlike all previous discrete-time systems which yield a staircase response which requires filtering.

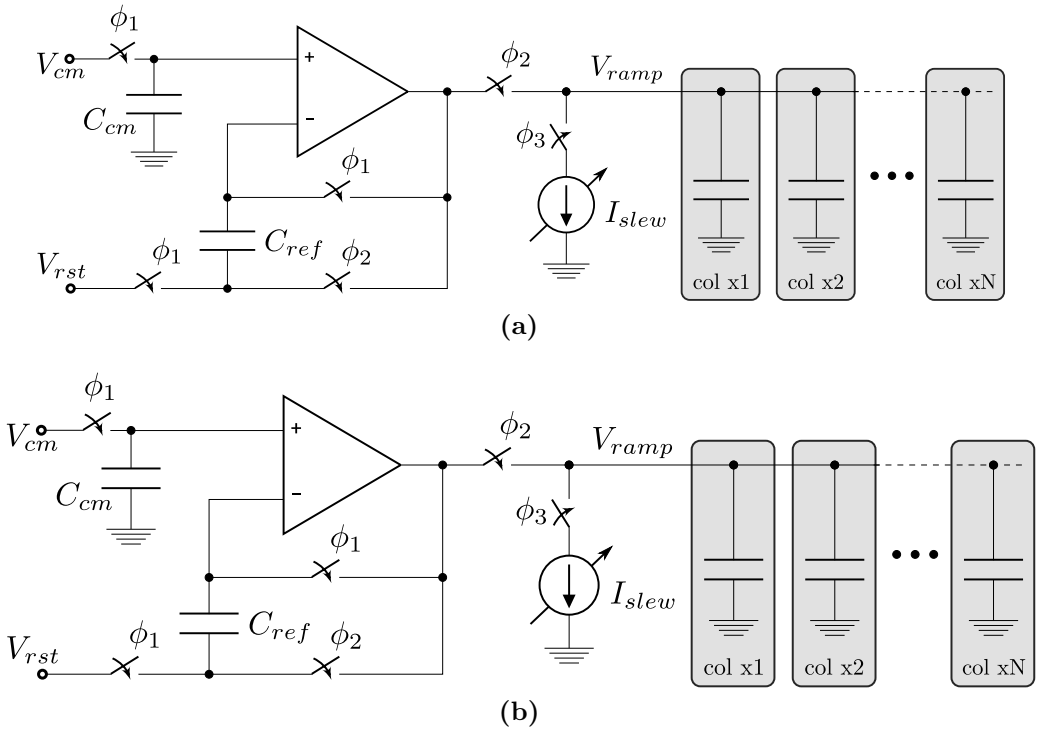


Figure 3.4: Principal continuous-time ramp generators: a) global buffered constant-current integrator; b) local per-column integrator.

Current noise from the current source and OTA is integrated on the feedback capacitor. This noise is normally dampened by the use of a large integration capacitor, as long ramp times combined with low integration capacitances may lead to a significant drift of the ramp trajectory. Continuous-time integrator approaches, presented as such, highly influence the INL of the ADC. This is due to the frequency drift and jitter of the reference clock which is independent of the integrating current. Integration currents may also be affected by temperature and voltage variations. To reduce ramp slope errors, continuous-time integrator approaches require dynamic current calibration. Typically, a frequency-to-current converter can be employed which tracks the count clock frequency and adjusts the integration current relative to the count speed [45], [46].

An architecture using local per-column integration capacitors is shown in Fig. 3.4b. During the initialization phases ϕ_1/ϕ_2, the offset and targeted ramp reset voltage level are sampled on the plates of capacitor C_{ref}. During ϕ_2, C_{ref} is connected in the feedback loop and precharges the ramp line. During ϕ_3 the OTA buffer is disconnected and a constant current source is connected to the ramp line, which linearly discharges the local integration capacitors in each column. This ramp generation method is more sensitive to comparator kickback noise, as the column integration capacitors have a size comparable to the C_{gd} parasitics of the comparator differential pair. Thus, the approach requires high suppression of any residual kickback from the comparator, which leads to complications in its design [35]. However, local integration capacitor schemes benefit from increased ground/power supply rejection ratios due to the local ramp ground coupling. Such methods also feature lower thermal integrated noise on the ramp due to the high capacitive load which limits the bandwidth for noise in-fold. In high column

number implementations the distributed ramp capacitor becomes large enough to suppress most thermal noise from the integration current source. A disadvantage of this scheme is that the combined distributed capacitance is large which limits the settling time during ramp reset operations. The last also adds up and can become comparable to the total conversion time in very high-speed systems.

3.1.4 Compressing Ramp Generators

Except for one-step linear ramp, imaging ADCs may also employ companding functions. This requires linear ramp generation with alternating slopes.

A naturally occurring physical light phenomenon lets travelling photon particles to vary spatially and temporally, which causes their different time of arrival at the photo detector. The variation of these events is known as photon shot noise which has a Poisson distribution [47]. Its statistical variance increases with the increase of the optical flux and follows a square root law. Thus, stronger light intensity translates to a larger electrical signal with stronger variations. This phenomenon can be exploited in ADC design as fine quantization steps are no longer needed in a photon shot noise dominated signal.

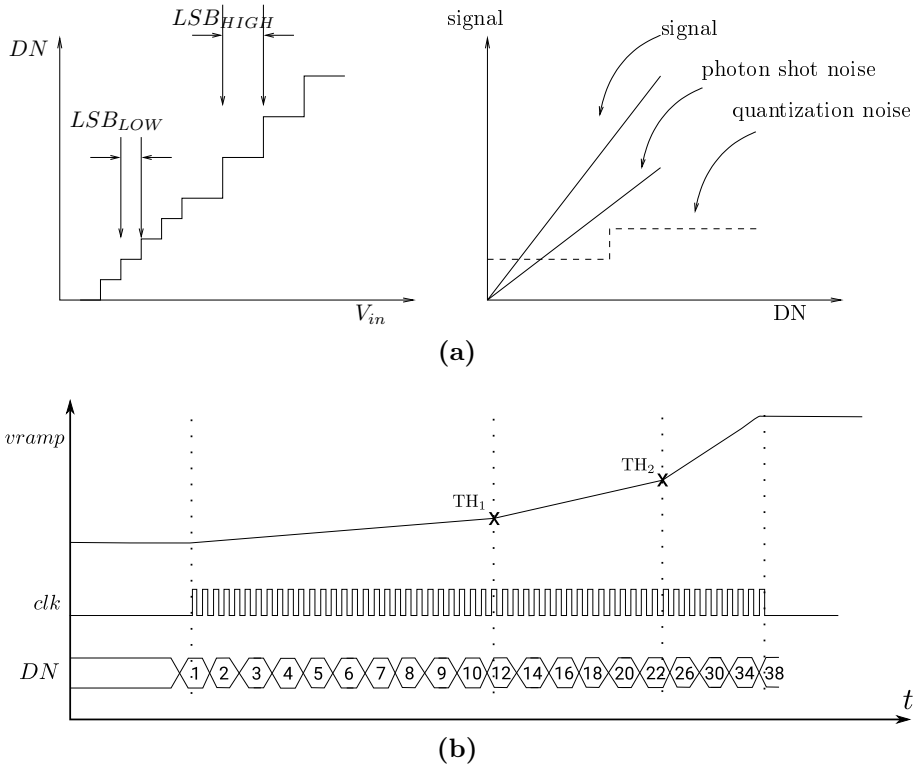


Figure 3.5: Photon shot noise inspired architecture: a) basic principle; b) ramp compression and consecutive expansion through fast counting

This ramp ADC architecture has an inherent advantage towards the design of a varying quantization step implementation. The ramp reference voltage can be easily altered during the conversion process, modifying the quantization noise. Consequently, the converter can be designed to increment N-times faster, after the ramp has reached the next-level slope change.

This architecture is known as companding or Photon Transfer Curve (PTC) inspired, and has been widely used within high-speed imaging ADC implementations.

Figure 3.5 shows a diagram illustrating the principle of photon shot noise and transfer curve inspired ramp ADC designs. After reaching a certain signal level threshold, the ramp voltage slope is doubled, while the counter is set to count twice as fast. Doubling the ramp slope causes signal compression, while the 2× faster counting expands the signal – a process causing a 1-bit increase of quantization noise at the gain of a 2× faster conversion rate. Various architectures using a few threshold slope changes which provides higher speed gains have been presented [48], [49], [50]. The ramp generation in companding ADCs can be implemented using all previously mentioned architectures by doubling the current (in the case of integrator-based structures) or directly doubling the DAC word scanning (in the case of DAC-based generators). It is worth noting that the threshold switching levels of the ramp must occur when the signal level noise (and photon shot noise) is marginally higher than the expected quantization noise increase, which has also been illustrated with dashed line in Fig. 3.5a. Figure 3.5b provides an overview of the PTC process in a ramp ADC as a function of time. After reaching initially set count (ramp) threshold levels TH_1 and TH_2 the slope of the ramp is increased, while the counter is operated at a 2× fast mode, thus implementing the expanding operation.

Compressing ramp generators are usually beneficial in high-speed imaging applications, where counting time increase is undesirable. Compression (and consecutive expansion) comes at the cost of increased design complexity of both the ramp generator and ADC counter. In additon, a form of digital additive dither is needed to mask the high quantization noise magnitude.

3.2 Noise During Steady-State Phases

The previous section discussed the principal methods for generation of ramp reference voltages in single-slope (SS) ADCs. Having qualitatively discussed noise, this section will quantitatively analyze the dominant noise sources in SS ADCs and their effect on signal conversion.

Previous approaches of noise analysis in image sensor SS ADCs have formally assumed a noise-free reference voltage [51], [52], [53]. Such assumptions have primarily been considered due to the difficulties in modelling noise in the continuous-time domain. Frequency domain steady-state models provide the designer with an easy understanding for noise estimation. However, such simple assumptions lead to inaccurate total noise magnitude assessment and often to significantly optimistic noise estimations.

When compared to other ADC architectures, ramp ADCs differ with their semi-steady —semi-continuous-time states of operation. The conventional frequency-domain noise estimation can typically be successfully applied only to fully-sampled ADC systems. This assumes that their sampled steady-states are linear time-invariant, and that no noise is induced during the transition periods between the switching of states [11]. In ramp converters, however, one needs to consider the noise during the continuous-time (ramping) operation, for which a non-stationary noise analysis proves useful.

Such studies have been applied to a number of other systems. In [54] a non-stationary noise analysis has been studied and applied to an isolated case of a transconductance amplifier. This has been further extended to a periodic filtering frequency domain model, analyzing the steady-state noise induced by the series of discrete-time samples during the conversion zooming steps

in a pipelined ADC. The authors have shown that the periodically sampled values have the same statistics and form a wide-sense cyclostationary discrete-time series. In [55] an analysis of white noise integration during the transition period of a CMOS inverter cell in a ring oscillator has been studied, which is also of similar origin to the integrated on the ramp ADC reference noise. Cheon et al. [51] have conducted a study on the impact of various noise simulation methods for single-slope ADCs employing correlated double sampling. This has resulted in a comprehensive high-level analysis of the underlying noise during the steady conversion phases. In this section we elaborate on the noise sources induced during the WSS static sampling phases. Parts of the follow up section form a revised version of the published [II] paper which is copyright of IEEE.

3.2.1 Background on SS ADC Phases for Noise Analysis

To simplify noise analysis, a divide and conquer approach between the steady-state and continuous-time phases is essential. For this purpose Fig. 3.6 a) shows a principle schematic of a conventional column-parallel ramp ADC architecture used in CMOS image sensors. A simple 4-Transistor pixel is shown as an input source, as well as a reference voltage generator, formed by directly discharging a capacitor through a current source. The analog-to-digital conversion occurs in two phases: ϕ_1 — *signal sampling and ramp reset*, and ϕ_2 — *conversion phase*. Their timing diagram is also presented on Fig. 3.6 b). During phase ϕ_1, the output of the in-pixel source follower transistor $\mathrm{M_{sf}}$ is sampled on capacitor C_s. At the same time, the starting point of the ramp reference voltage V_{ref} is sampled on capacitor C_r, which is driven by the voltage buffer VBUF. The counter CNT is also reset. During phase ϕ_2, the counter is enabled and a reference count clock CLK is applied. The charge stored on capacitor C_r is slewed by the reference current I_{ref}, leading to a linear voltage discharge of C_r. At this instance, when the discharging voltage on C_r ($vramp$) crosses the voltage sampled on C_s (vsh), the comparator toggles, thereby stopping the counter and digitizing the voltage sampled on C_s.

Typically, in CMOS image sensors, a second consecutive digitization operation is performed, followed by a subtraction between two consecutive conversions, denoted as Sample and Hold Reset and Sample and Hold Signal (SHR/SHS) [56], [57]. The difference operation cancels the comparator offset V_{os} and noise, programmable gain amplifier (if used), as well as pixel reset kTC noise at the sense node.

The latter operation is often referred to as digital correlated double sampling (DCDS), which has a high-pass filtering effect on the noise and does not alter its roots of origin [58]. The following subsections focus on the origins of the noise induced by the various sampling and slew operations during a single raw conversion, and do not consider the system-level noise cancellation effects of the DCDS transfer function. These have been extensively studied in [56], [57], [58].

3.2.2 Steady-State Noise in Single-Slope ADCs

The conventional frequency domain noise estimation, assuming wide sense stationarity (WSS) of signals is a commonly used technique in the analysis of sampled systems [11]. In purely sampled ADC systems, including the pipelined, cyclic, delta-sigma and SAR architectures, where the reference voltages eventually reach a steady state, the WSS frequency-domain methodology provides an adequate noise estimation. However, SS converters form a hybrid between sampled

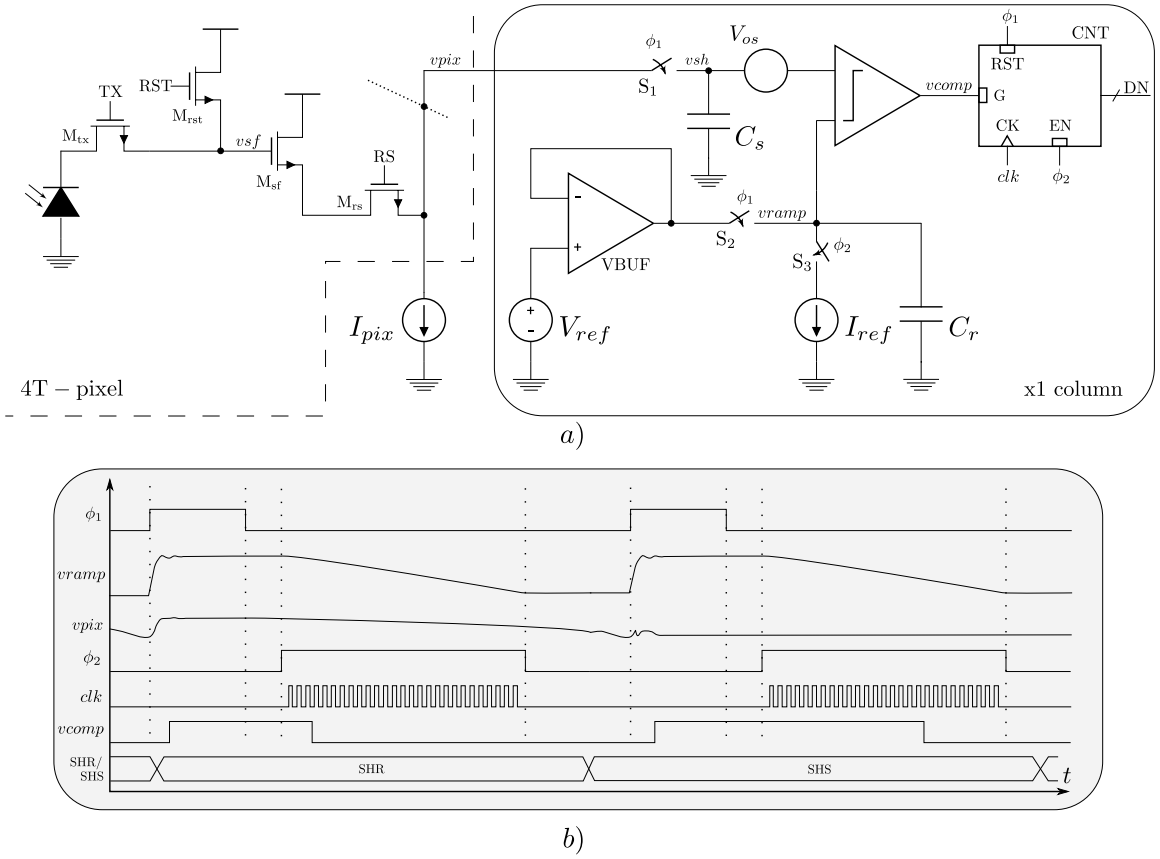


Figure 3.6: Principle schematic diagram a) and timing b) of a conventional column-parallel ramp ADC, ([II], reprinted by permission of IEEE)

and continuous-time systems, which makes them difficult for analysis solely in the frequency domain.

In [51], noise estimation in single-slope converters was presented basing on WSS assumptions during the steady sampling phases. It has resulted in a comparison between frequency and time-domain noise simulation models for comparator- and pixel- induced noise. However, the noise voltage on the ramp reference is difficult to evaluate by applying the frequency noise simulation technique. This is due to the time-domain voltage noise integration on the ramp capacitor. As reference voltage non-idealities in ramp ADCs directly translate into the digitized output, an accurate ADC noise model must also include the accumulated noise during the continuous-time ramping phase. Moreover, phase noise induced by the counting clock jitter is also directly digitized at the output. Lastly, the time-domain jitter injected by the voltage-time conversion from the comparator must also be addressed with attention, due to the second order effects, related to the slope of the ramp and its crossing with the level of the sampled input voltage.

To revise the noise power analysis during the steady phases, let us revisit Fig. 3.6. During the *signal sampling and ramp reset phase*; switches S_1 and S_2 are closed and switch S_3 is open. Assuming uncorrelated additive white noise, the total combined power spectral density (PSD)

of the noise during these stationary phases, can be estimated as

$$S_{sig/rst}(f) = S_{pix}(f)|H_{pix}(f)|^2 + S_{vref}(f)|H_{vref}(f)|^2 \tag{3.1}$$

where $H_{pix}(f)$ and $H_{vref}(f)$ are the transfer functions of the pixel and reference voltage buffer respectively. $S_{pix}(f)$ and $S_{vref}(f)$ are the double-sided noise PSDs of the vsf and $vref$ voltage nodes.

For simplicity the thermal kTC noise from the sampling switches is neglected, as they are an order of magnitude lower than the other contributors and can be typically minimized by choosing suitable capacitor sizes [59]. The comparator is assumed to have no noise contribution during ϕ_1 as it is connected in open-loop. The total noise power during ϕ_1 can therefore be estimated as

$$\langle v^2_{n:\phi_1} \rangle = 2 \int_{1/T_{rst}}^{\infty} S_{sig/rst}(f) df \tag{3.2}$$

where the T_{rst} boundary is the reset time. The lower boundary of the integral in (3.2) should be limited to the duration of the reset phase ϕ_1. Otherwise, at 0 Hz, the 1/f noise approaches infinity which results in a false noise estimation.

3.3 Noise During Continuous-Time Ramp Phase

During the continuous-time conversion phase, the core ADC principal noise sources are the comparator, ramp voltage noise, as well as clock jitter. We can assume that the clock jitter is independent of the ramp voltage, as the clock and ramp generators are two entirely isolated ADC sub-systems. Furthermore, if the comparator is operated in saturation and with sufficient margins, we can also assume that its noise contribution is fixed flat within its operating input range. Hence, during the entire duration of the continuous-time ADC phase. Although, an effect known as comparator propagation-delay dispersion [60] is present in every voltage comparator, it is not directly linked with its output noise, and thus the propagation-delay dispersion accumulates as integral non-linearity in single-slope ADCs.

3.3.1 Theoretical Framework

The ramp reference voltage is typically generated by the integration of constant current into a capacitor, which is produced by a real (non-ideal) current source. Hence, it is not noise-free. It can be represented as a process linked to a window of integrated noise induced by the non-idealities of the current source. Let us consider the scheme on Fig. 3.7, which shows a simplified model of a continuous-time current integration based ramp reference generator in an image sensor ADC [53], [61].

A typical design approach would be to keep a local integration capacitor in each column-parallel ADC, whose top plates share a global initialization (reset) voltage buffer and a sinking current

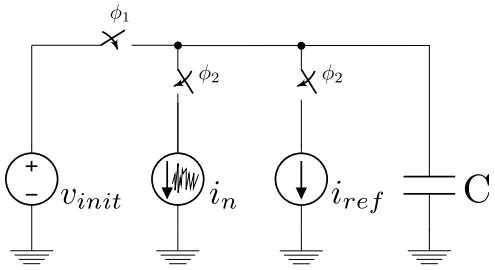


Figure 3.7: Equivalent schematic diagram of typical ramp reference voltage implementations as presented in [61].

source. During ϕ_1, the capacitor C is charged to v_{init} while during ϕ_2, C is discharged by a mean reference current i_{ref} with current noise i_n due to thermal, shot, and 1/f noise of a realistic MOSFET current sink. The resultant reference voltage v_{ref} at a specific time instance t_d is hence obtained by the definite integral of both currents

$$v_{ref} = v_{init} - \frac{1}{C}\left[\int_0^{t_d} i_{ref}dt + \int_0^{t_d} i_n dt\right]. \tag{3.3}$$

It is worth noting that the second term of (3.3) contains an integral of a random current noise i_n with uniform distribution. This noise is formally represented by a continuous-time Wiener process [62], explored by the well studied equation

$$W_n(t_n) = \frac{1}{\sqrt{n}} \sum_{1 \le k \le [nt_n]} \xi_k. \tag{3.4}$$

This is a random step function, whose increments $W_n(t_n)$ are independent, as the random uniform variables ξ_k are independent. With white noise as an input, $W_n(t_n)$ is no logner white, although its distribution remains Gaussian. As $n \to \infty$, W_n approaches a Wiener process [62].

The first term in (3.3) contains an integral of fixed current i_{ref}, which combined with the noise component i_n in the second term in (3.3) forms a Wiener process with drift, which is generalized as

$$X_t = \mu t + \epsilon W_t \tag{3.5}$$

where μ is the drift and ϵ represents an infinitesimal variance σ^2. It is well-known that the standard deviation of X_t is dependent with the square root of time [62]

$$\sigma \propto \epsilon\sqrt{t}. \tag{3.6}$$

To provide a better representation of this process, Fig. 3.8 a) shows a numerical simulation of a Wiener process with drift versus iteration time unit N, using normalized unit variance $\epsilon = 1$ and a drift coefficient μ = 0.1. It can be seen that as the iteration N (equivalent to time) increases, the original ramp trajectory drifts following a standard deviation, which is visually provided on Fig. 3.8 b). As such, b) represents a numerical proof that σ of X_t does increase with the square root of time, as formalized by Equation 3.6.

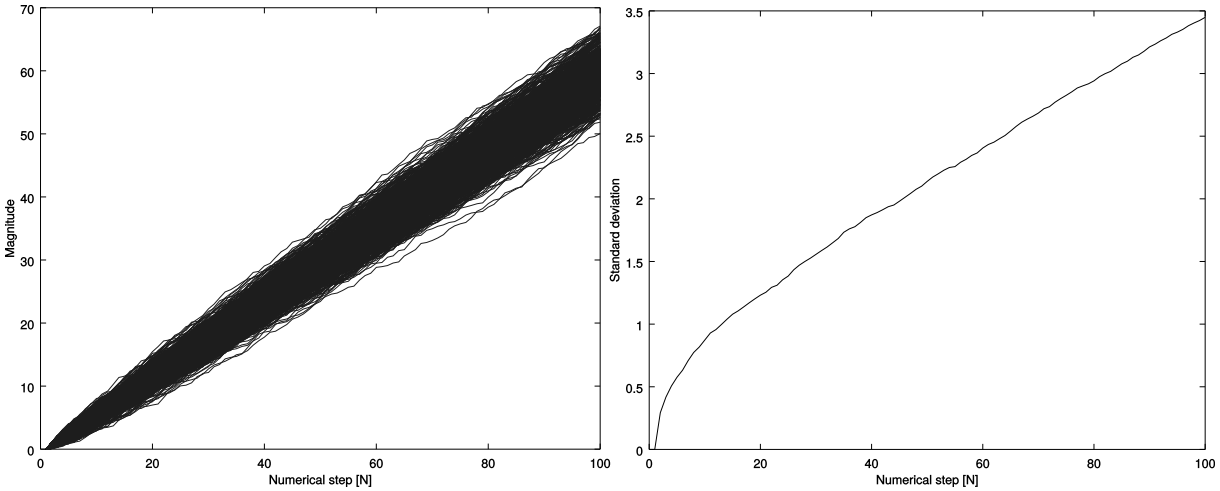


Figure 3.8: A numerical simulation of the random walk phenomenon using a drift coefficient μ = 0.1 and $\epsilon = 1$ for 1000 iterations of $N = 100$ steps : a) iteration progression, b) calculated standard deviation σ for each step N, ([II], reprinted by permission of IEEE)

To combine the WSS and non-WSS noise models used for evaluation of the noise processes in ϕ_1 and ϕ_2, a designer would ideally know the PSD of this continuous-time process in the frequency domain and its expected RMS value and power for a specifically defined time. Using a technique similar to [55], one way to solve this problem is to convert the integral in (3.3) into a convolution with a rectangular unit window w_{td} with a size of t_d and perform a second integration

$$v_{ref}(t) = v_{init}(t) - \frac{1}{C}\int_0^{\infty} \Big(i_n(x) + i_{ref}(x)\Big) \times w_{t_d}(t-x)dx. \tag{3.7}$$

This provides us with insight on the RMS value of the ramp noise. In order to obtain the noise PSD, we can treat the sink current source noise $S_{i_n}(f)$ as passing through an LTI system [55]. This has a transfer function equivalent to the Laplace transform $W_{td}(s)$ of a rectangular window. Thus, we can express the PSD as

$$S_{v_n}(f) = \frac{1}{C}|W_{td}(f)|^2 \times S_{i_n}(f). \tag{3.8}$$

The noise power for the rectangular window $|W_{td(f)}|$ of current noise $S_{i_n}(f)$ can be obtained

by applying the Wiener-Khinchine theorem [62]

$$\langle v_n^2 \rangle = \int_0^\infty S_{v_n}(f)df = \frac{1}{C}\int_0^\infty S_{i_n}(f)|W_{td}(f)|^2 df. \tag{3.9}$$

The frequency response of the rectangular window is well-known, which is a convolution of the window length with a sinc, as a function of the frequency

$$|W_{td}(f)| = t_d \times \mathrm{sinc}(ft_d) \Leftrightarrow t_d\left[\frac{\sin(\pi f t_d)}{\pi f t_d}\right]. \tag{3.10}$$

For the current source noise PSD model, if we consider the presence of both 1/f and thermal noise, the solution to the noise power becomes overly complex. Thus, we approximate the input noise power to be thermal, coming from the channel resistance of the current source, or

$$S_{i_n}(f) = 4kTg_o n(f) \tag{3.11}$$

where g_o is the output conductance of the drain-source channel and $n(f)$ is 1, except for ultra-high frequencies due to quantum effects [63]. When working with this MOSFET thermal noise model, the drain-source channel conductance gradient can no longer be assumed to be uniform when $V_{ds} > 0$. Moreover, g_o at V_{ds} = 0 is obtained by means of extrapolation from measurements under saturation conditions, as I_{ds} = 0 when V_{ds} = 0 [64]. Hence, to obtain a better representation of the channel resistance gradient, g_o can be approximated as

$$g_o = \frac{\mu^2 W^2}{L^2 I_{ds}} \int_0^{V_{ds}} \Big(C_{ox}(V_{gs} - V_t)V_0(V_{ds})\Big) dV_{ds} \tag{3.12}$$

where V_0 is the channel potential profile, and μ and C_{ox} are the channel carrier mobility and gate oxide capacitance per unit area respectively. Fig. 3.9 provides a graphical representation obtained by means of an AC noise SPICE simulation, of the shrinking channel resistance gradient, impacting the channel thermal noise as V_{ds} is slewed during the current integration process.

Substituting (3.10) and (3.11) in (3.9) and solving yields

$$\langle v_n^2 \rangle = \frac{2kTg_o t_d}{C}. \tag{3.13}$$

Appendix A shows a detailed calculation for the integrated noise power per hertz of bandwidth.

3.3.2 Numerical Validation

It can be clearly seen that the integrated noise power increases with time, as expected and shown by the ramp spread in Fig. 3.8. As the noise current spectral density S_{i_n} in a MOSFET source is not usually under good control by the designer, there are two practical control mechanisms for reduction of the spread. Increasing the integration capacitor size C, or a reduction of the ramp time t_d. Hence, to better understand the spread phenomenon, Table 3.1 provides a simulated and calculated noise power spread over two discrete time points and five integration capacitor cases, with corresponding current source bias conditions. These results were extracted by means of a thermal noise only transient noise SPICE simulation, using typical $0.11\,\mu\mathrm{m}$ CMOS image sensor process models, with their flicker noise parameters deliberately asserted to zero. The simulation testbench consists of an ideal switch charging an ideal capacitor to 3.3 V with a classic current mirror in parallel. To ensure that the noise contribution of the current mirror comes only from the copying current device, a 1 F ideal capacitor was placed on the gate-source of the biasing diode. This limits the bandwidth and virtually cancels the noise contribution from the diode MOSFET including any poly or bulk resistance thermal noise modelled in the device. The detailed device sizes and bias are also provided in Table 3.1. The operating temperature for all cases was kept at 70 °C and the calculations were made using a noise bandwidth of

C, [pF]	W/L	i_d, [µA]	i_n^2, [A^2/Hz]	$i_d/\square$	t_d	1 µs	10 µs	Δ
10	1.5 µ/2 µ	2.25	$306.4e^{-27}$	3.00 µA	$\sigma_{v_{n_{sim}}}$, [µV]	39.5	113.4	2.87
					$\sigma_{v_{n_{calc}}}$, [µV]	27.6	87.5	3.16
					$\sqrt{v_{n_{calc}}^2}$, [pV]	766	7660	10
20	3 µ/2 µ	4.50	$612.7e^{-27}$	3.00 µA	$\sigma_{v_{n_{sim}}}$, [µV]	27.7	80.2	2.89
					$\sigma_{v_{n_{calc}}}$, [µV]	19.5	61.9	3.16
					$\sqrt{v_{n_{calc}}^2}$, [pV]	382	3830	10
40	6 µ/2 µ	9.01	$1225e^{-27}$	3.01 µA	$\sigma_{v_{n_{sim}}}$, [µV]	19.8	56.7	2.87
					$\sigma_{v_{n_{calc}}}$, [µV]	13.8	43.8	3.16
					$\sqrt{v_{n_{calc}}^2}$, [pV]	191	1910	10
80	12 µ/2 µ	19.02	$2451e^{-27}$	3.16 µA	$\sigma_{v_{n_{sim}}}$, [µV]	13.9	40.1	2.88
					$\sigma_{v_{n_{calc}}}$, [µV]	9.7	30.9	3.16
					$\sqrt{v_{n_{calc}}^2}$, [pV]	95.7	957.4	10
160	24 µ/2 µ	38.11	$4902e^{-27}$	3.18 µA	$\sigma_{v_{n_{sim}}}$, [µV]	9.9	28.3	2.86
					$\sigma_{v_{n_{calc}}}$, [µV]	6.9	21.9	3.16
					$\sqrt{v_{n_{calc}}^2}$, [pV]	47.8	478.1	10

Table 3.1: Simulated and Calculated Noise Power and Spread for a set of Capacitances and Ramp Times

1 GHz and a noise scale factor of 1. Standard deviations of both the simulation $\sigma_{vn_{sim}}$ and hand calculation $\sigma_{vn_{calc}}$ model are provided and show a σ increase of approximately 2.86 and 3.16 = ($\sqrt{10}$), respectively.

It can be observed that the rate of σ increase in the SPICE simulation is lower than the theoretically expected: 2.86 < 3.16. This is primarily due to the modulation of g_o (respectively $i_{n_{ds}}$), with V_{ds} as the ramp slews down, modelled by Eqn. 3.12 and indicated on Fig. 3.9.

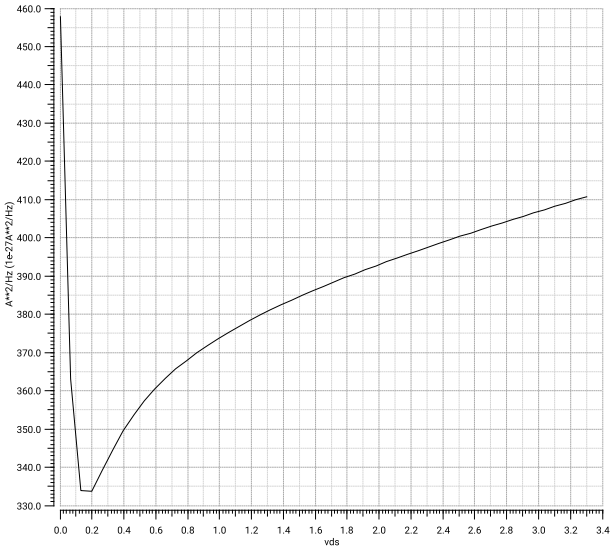


Figure 3.9: Channel current noise at 1 MHz vs applied Vds of a 2 µm/2 µm NFET biased at 3 µA obtained by means of an AC noise sweep, ([II], reprinted by permission of IEEE)

We can summarize that, after a certain capacitance threshold, Wiener noise from the integration source can be dampened below a distinguishable least significant bit for the typically achievable resolution of 12-14 bits for a ramp ADC with a 1.3 V ramp swing [65]. Similar to our approach in Section 3.2.2, we can summarize the total noise power during ϕ_2 as

$$\langle v_{n:\phi_2}^2 \rangle = \frac{2kTg_o t_d}{C} B + 2 \int_{1/T_d}^{\infty} S_{comp}(f) df \tag{3.14}$$

where the first term represents the ramp noise for a given bandwidth B, and the second term is the comparator noise contribution.

It is worth noting that in practice, apart from the aforementioned noise phenomenon, column-parallel ADCs which share their reference voltage line exhibit a secondary deterministic noise effect on the ramp. It is caused by the kickback noise injected on the ramp during comparator toggling. This alters the charge on the distributed ramp capacitor, and therefore the reference voltage seen by other neighbouring column ADCs. Kickback noise on the ramp has a profound effect on the performance of such ADC systems, however, its consequence can be reduced by careful system-level comparator design for kickback minimization [66].

3.4 Voltage Noise Translation to Time-Domain Noise

A secondary effect is observed during the voltage-to-time translation by the comparator. Let us consider a voltage ramp signal which has a ramping time window of Δt and spans between voltages V_1 - V_0 = ΔV, as shown on Fig. 3.10a. The ramp V and the sampled signal V_{sh} are compared with uncertainty error V_{nc}^2 which is the comparator input-referred noise power. To simplify the illustration on Fig. 3.10a, the latter is added on top of V_{sh}.

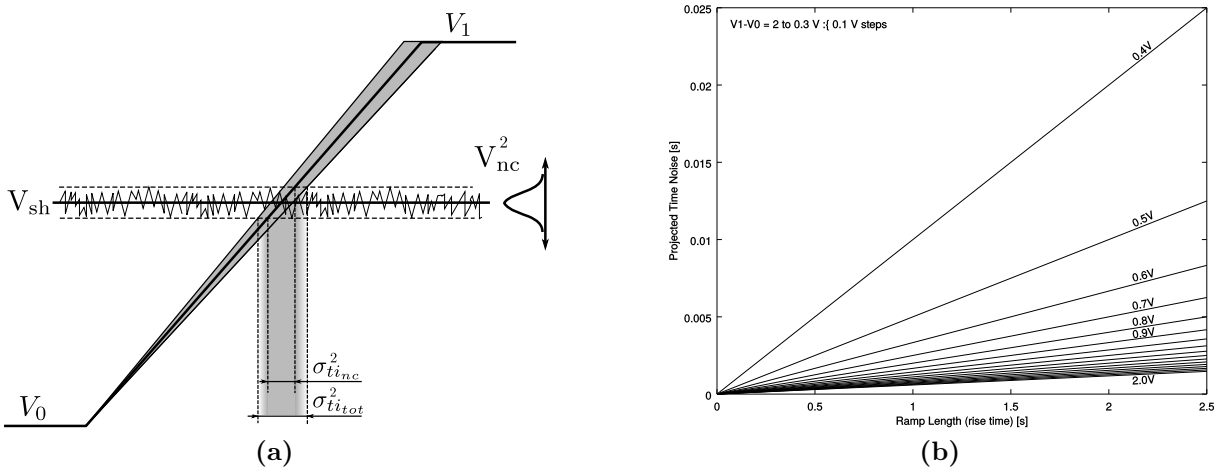


Figure 3.10: Ramp illustrations: a) ramp angle of crossing and voltage-time noise projection for different slopes; b) family plots of projected time-domain noise σ_{ti} for an input-referred noise of 5mV and ΔV from 2 to 0.3 V in 0.1V steps, ([II], reprinted by permission of IEEE)

It can be observed that the ramp angle of crossing with V_{sh} changes with the ramp time window Δt as well as its voltage span ΔV. The slope of the ramp effectively determines the comparator input-referred RMS noise projection to time uncertainty error σ_{ti}^2. The latter can be expressed as

$$\sigma_{ti}^2 = \frac{V_{nc}^2}{\Delta V/\Delta t} + \frac{V_{rw}^2}{\Delta V/\Delta t} \tag{3.15}$$

where V_{rw} is the calculated Wiener noise power. Equation 3.15 assumes that the Wiener noise increases minimally between the lower and the upper bounds of the comparator input-referred voltage noise. To provide a qualitative representation of the described second order effect, Fig. 3.10b shows family plots of ramp span from 2 to 0.3 V in steps of 0.1 V as a function of the ramp time. The projected time-domain noise power σ_{ti}^2 is calculated for a fixed input-referred comparator noise voltage of 5 mV.

From the above it is evident that as the ramp slope becomes steeper, voltage-to-time noise undergoes a transformation with a lesser gain. This suggests that the use of faster ramp times can improve time noise. However, after a certain point, when the ramp slope reaches very high values, the benefit of using a fast ramp vanishes. This leaves the noise performance equivalency to that of the comparator, Wiener noise on the ramp and clock jitter. As expressed in Eqn. 3.6, the standard deviation of Wiener noise is proportional to $\sqrt{t}$, this reduces its significance with very short ramp times. As clock jitter is not typically scalable with frequency, and the

comparator noise is fixed, the fundamental limits to ramping faster are solely dependent on clock σ^2_{jclk} and comparator jitter σ^2_{ti}. The noise σ^2_{ti} and σ^2_{jclk} add-up and their total combined probabilities form the final output Digital Number (DN) noise of the ADC counter.

In practice, however, a faster ramp requires higher bandwidth comparator, which increases its input-referred noise due to wider in-band thermal noise integration. This leads to a contrary effect of degradation. When the total combined clock jitter σ^2_{jclk} and comparator jitter σ^2_{ti} reach a value comparable to $T_{clk}/2$ in the case of a double data rate (DDR) counter, the ADC would no longer retain distinguishable least significant bit at Nyquist rate, which formally sets its fundamental speed limit.

3.5 Experimental Measurement of Ramp Noise

Wiener and comparator time-domain noise projection from the ramp angle of crossing can be identified accurately only by comparing a broad range of ramp integration times due to purely practical noise measurement reasons. Therefore, measurements of signal-dependent output noise should be conducted in various ramp slope scenarios along with a high data oversampling rate. This section provides one measurement and calculation solution in the case of a photon transfer curve quantization based ADC, which allows the use of contrasting ramp slope scenarios. Such strategy eases the comparison and measurement of the integrated thermal noise on the ramp.

3.5.1 Measurement Setup

It is difficult to measure random walk directly on the on-chip ramp due to the bandwidth limitations imposed by bonding wires and PCB track parasitics. In addition, usually some form of buffering is needed for feeding the ramp off-chip undisturbingly which is an additional source of noise. From Section 3.3 and 3.4 it may be recalled that the effect of the noise on the ramp leads to a signal-dependent output noise characteristic in ramp ADCs. By sweeping the input signal and highly oversampling the measurement data, following our model, we should be able to theoretically detect an increase in the ADC output noise with a square root trend. However, this trend may be dampened significantly by numerous other on-chip noise contributors. Changes in the ramp voltage span modulate the time for noise accumulation, and hence, lead to a signal-dependent noise trend. Moreover, a fold in the ramp integration time should yield a much lower signal-dependent noise magnitude.

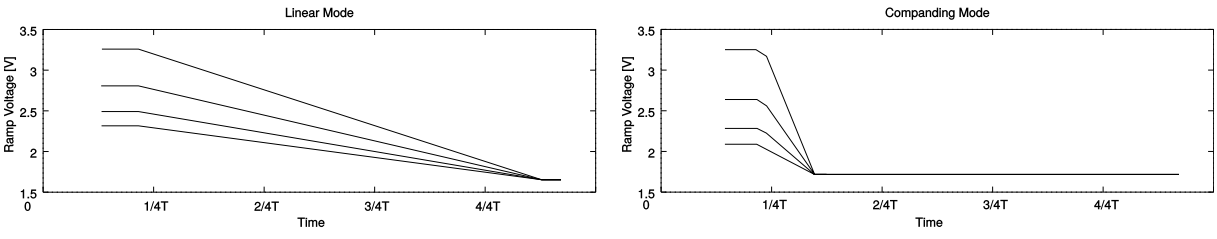


Figure 3.11: Modelled set of ramps in linear and companding ADC mode

In order to perform an experimental validation, the DR-4k-3.5-LCC sensor [67] was chosen, which is a line-scan CMOS image sensor array with 4096 column-parallel ADCs. It owes the flexibility to be configured in slow and high-speed modes, ranging from 10 to 250 kSps. Fig. 3.12 presents an overview of our ADC and measurement setup. This chip provided the possibility to use a wide range of ramp slopes by employing an additional feature of a companding conversion mode. Using an ADC with broad conversion time tuning capabilities allows the impact of the integrated current noise to be put to evidence. The ramp generation is implemented as a distributed capacitance C_r added to the differential pair of each column comparator. The capacitor distributed in 4096 parts (one capacitor per column), is driven and discharged by a wide-swing programmable current mirror.

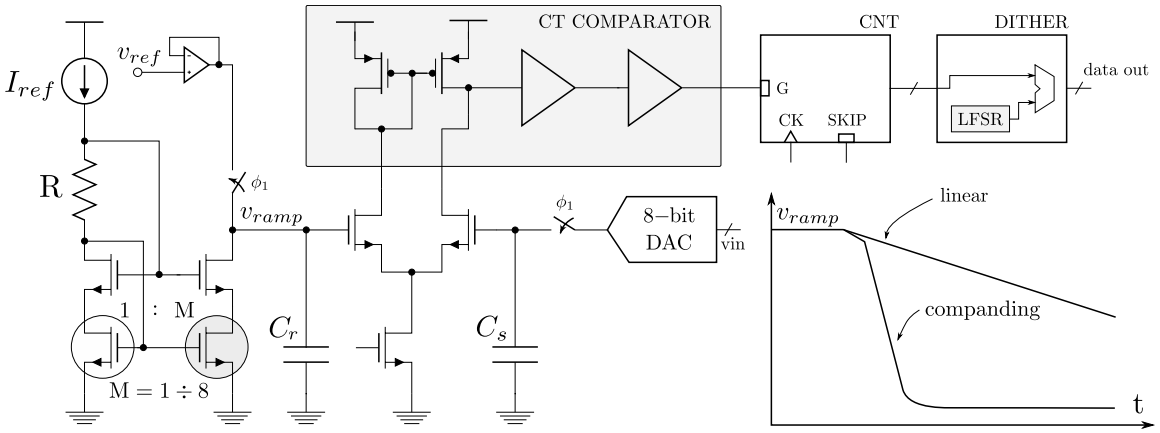


Figure 3.12: Overview of the ADC measurement setup, ([II], reprinted by permission of IEEE)

A DAC present on the chip for another function was used as a test source, which provided a controllable input voltage to the column ADCs. The last is also photon shot noise free, compared to the typical mode of ADC operation which uses the pixel as an input voltage source. The column ADC counters are binary and asynchronous with the ability to carry out an expanding counting function. When this function is enabled, the counters can skip counts and increment only on even clock cycles after reaching a pre-programmed binary threshold. At the same time, the current through the ramp current source is doubled after reaching the set threshold for binary count skipping, which compresses the signal. Thus, the signal is first compressed by the altered ramp slope, and at the same time expanded by the expanding counting function, leading to a resultant linear output of the ADC.

We refer to this ADC mode of operation as *companding* — originating from the signal compression and consecutive expansion. To decrease conversion time, our test chip contains three threshold levels for binary skipping, therefore the current through the ramp doubles after reaching each threshold. This yields a ramp which is 8 times as fast as compared to conventional mode. A principal overview of the ramp in linear and companding mode, plotted versus time for different ADC gain settings is shown on Fig. 3.11. Ramp companding is a commonly used scheme for ADC conversion time reduction in CMOS image sensors, where at high signal levels (resp. light intensity), the photon shot noise drastically dominates thermal circuit and quantization readout noise [68].

With the use of companding mode quantization noise is traded for readout time, because a fine quantization step is no longer needed in a photon shot noise dominated signal. Count skipping however, introduces ADC linearity errors. In order to hide the increased DNL steps, we digitally

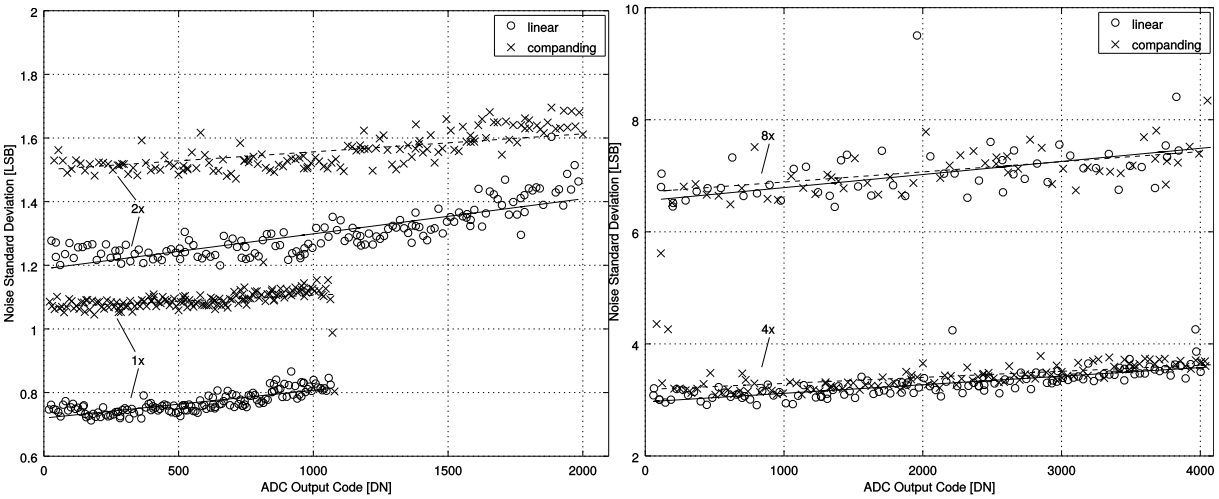


Figure 3.13: Measured noise standard deviation in LSB vs ADC code based on 2M samples per code step : a) 1x and 2x gain; b) 4x and 8x gain, ([II], reprinted by permission of IEEE)

add a uniform PSD dither of 1/2 LSB to the output of each counter, which is generated on-chip with a multi-stage linear feedback shift register. This addition does not affect the overall Wiener noise growth, as the digital dither is of high uniformity and can be treated as a fully independent and stationary noise source, which is not linked with and integrated by the analog circuits.

3.5.2 Interpretation of Measurements

Compared to linear, the companding ADC mode uses a ramp with much steeper slope. Hence, this yields a shorter Wiener noise process with a relatively larger mean drift component. This means that under equal conditions, the rate of increase in the ADCs random noise standard deviation should be lower in companding than in linear mode. Moreover, a change in the ramp time, or ADC gain respectively, should modulate the noise standard deviation slope and increase with higher signal levels, due to the larger ramp and its accumulated Wiener noise.

To perform the measurements for a large set of input voltages, an on-chip 8-bit current-steering DAC was used as direct signal input to the comparator. Four ADC gain settings were used in both linear and companding mode, which gives us a set of eight different modes (ramp slopes respectively) for comparison. The ADC analog gain is implemented by means of altering the ramp slew rate and its start and stop levels, while keeping the same counter accumulation capacity and count frequency. Each set of measurements includes a full-sweep of the 8-bit DAC, while acquiring 2 million conversion samples per each input DAC step. Fig. 3.14 shows the acquired mean value of the ADCs versus the measurement input voltage step for all eight ADC modes. It could be seen that the linear and companding modes yield an almost identical static DC response. The voltage range of the DAC was fixed to 1.55 — 1.2V which matches the lower 1/4 end of the ADC input range at 1x gain, as seen on Fig. 3.14. Plots of the measured standard deviation of the ADC output noise versus the mean converted code for the set of the

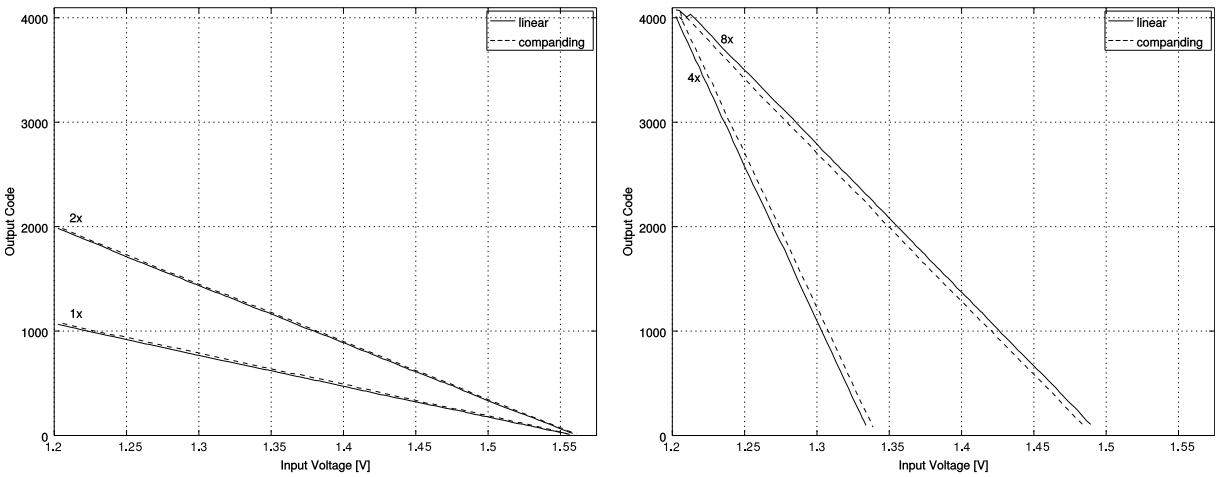


Figure 3.14: Input-output characteristic of the characterized ADCs for 1x, 2x, 4x and 8x gain in linear and companding mode, ([II], reprinted by permission of IEEE)

8-bit test DAC steps are shown on Fig. 3.13 where a) shows measured values at 1x and 2x gain, while b) gives the 4x and 8x respectively. The rate of noise spread is indicated by 1st order linear approximation lines. The ADC gain of 8x has an 8-times more flat ramp compared to 1x gain. It is observed that all measurements show a rate of σ increase, which is due to the current noise induced Wiener process on the ramp. The change in companding mode compared to linear is approximately 1/2 smaller in all gain modes, measured under equal conditions. The latter is caused by the much shorter ramp time in companding mode, and thus, a lesser presence of Wiener noise as the code increases. The effect of the stationary noise contribution of the uniform PSD digital dither can be seen under 1x and 2x gain on Fig. 3.13 a), as a mean increase of the noise standard deviation with approximately 1/2 LSB for companding mode. Under 4x and 8x gain the circuit noise is greatly amplified which causes the dither to hide under the thermal noise floor, and its contribution is no longer observed in the plots.

A precise conclusion of a square root trend directly matching the theoretical model is not always possible and highly depends on the system scenario. This is due to numerous other on-chip noise contributors having a partial masking effect on the ramp noise. Such evidence is lowest at 1x gain, where the growth approaches a factor of 2 which is closest to the theoretical expectations. At 4x and 8x gain, the masking of the integrated ramp noise is highly exhibited which is the reason why the noise growth trend with signal level appears to have been dampened. A further explanation for the noise growth reduction in 4x and 8x gain is that the size of the sink current source is also reduced, which reduces its thermal noise contribution.

3.6 Comparator Kickback Noise Effects

The previous section discussed noise due to thermal fluctuations sampled by the ADC and accumulated during the counting phase. However, column-parallel configurations exhibit a secondary deterministic effect on the ramp reference which is caused by comparator charge kickback. This section aims to provide an insight on the problem of kickback noise.

The shared nature of the reference voltage line in column-parallel configurations creates conditions for propagation of any disturbances to consecutive column comparator stages. This disturbance effect is known as comparator kickback noise and has a profound influence on column-parallel systems. Figure 3.15 shows a schematic diagram showing column-parallel continuous-time comparators sharing a ramp voltage reference line. Kickback noise originates primarily form the differential pair drain-gate parasitic capacitance C_{pk} which is coupled to the ramp voltage node. The charge disturbance induced on the reference line is linked to the size of C_{pk} (differential pair FET respectively), the bandwidth of the differential pair (tail bias current and speed of switching), the parasitic resistance R_p, and the damping parasitic capacitance C_p of the distributed voltage line.

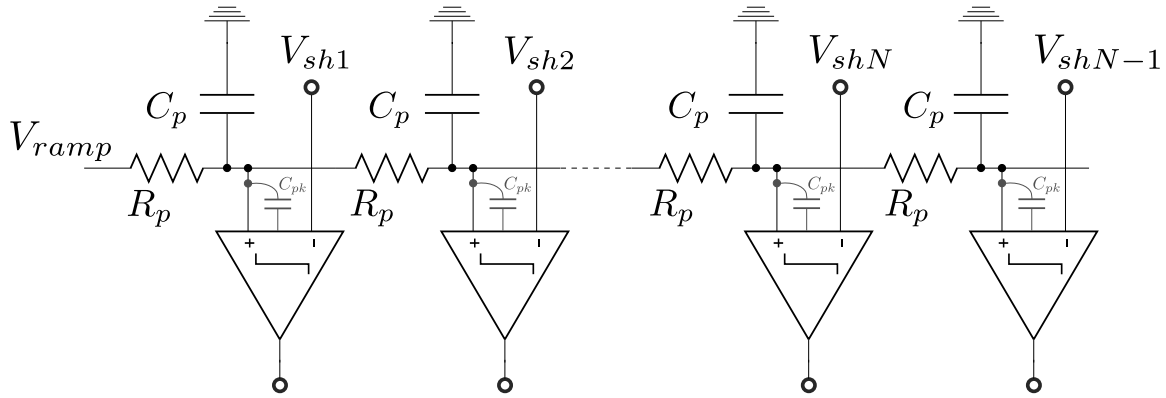


Figure 3.15: Column comparator kickback noise on shared ramp reference line

While if the reference line resistance can be decreased by wider sizing of the horizontal routing metal, such approach to achieving kickback immunity is not desirable due to the increased damping parasitics C_p which leads to additional energy needed for charge-discharge of the ramp node. A typical approach for reduction of the kickback noise effect is its elimination from the origin. Various continuous-time comparator kickback noise reduction approaches exist, however the most prominent ones include the cross-coupled neutralization and equivalent techniques [69], [70]. Another method for reducing kickback is to eliminate fluctuations on the parasitic kick capacitance and keeping the load on the ramp constant. In [35] the use of a variable tail bias current is controlled by an error amplifier referenced by a static high drain line voltage. When the comparator toggles and its drain line swings high, the error amplifier increases the tail bias current such that the drain voltage of the ramp node pair remains constant. This eliminates any charge and disturbance injected on the shared ramp node. This technique however, requires more energy for keeping a secondary high-bandwidth error amplifier loop within the comparator and its use is application specific.

3.6.1 Effect of Input Offset and Kickback Estimation

Another parameter influencing the effect of kickback noise in SS ADCs is column comparator input-referred offset. The worst case kickback conditions in array ADCs are when all comparators toggle at the same time instance which occurs when all individual sampled voltages have an equal magnitude. In a real-life system however, every comparator exhibits an amount of input offset, which reduces the conditions for simultaneous comparator toggling, leading to

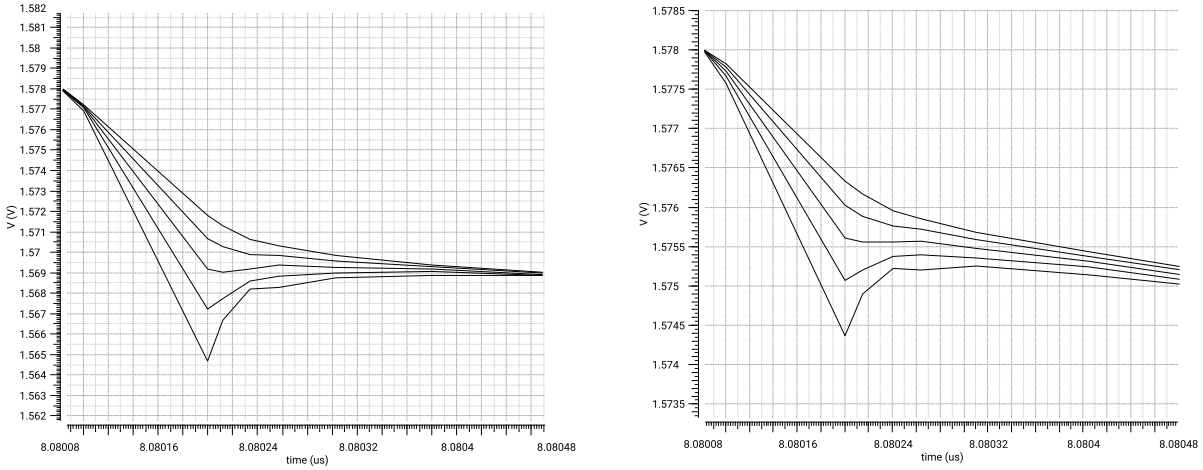
lower kickback crosstalk. Figure 3.16 displays an ideal simulation of high-bandwidth column comparators connected to- and sharing a global ramp. Sub-figure 3.16a shows the dip of the ramp reference line during comparator evaluation with a coupling factor of $1/10$ of C_{pk} with C_p. Sub-figure 3.16b displays the effect of added comparator offset under equal conditions. By applying a 10 mV artificial random uniform offset, the kick time between the five comparators is offset by 10 ns using the same ramp slope derivative. This leads to a less vigorous disturbance of the reference line and smaller absolute voltage difference between the internal nodes before and after comparison. In the general case, the voltage kick on the ramp could be modelled as

$$V_{kick} = \frac{NC_p}{C_{ramp}} \times \Delta V_{dp} \times k \tag{3.16}$$

to a first order approximation, k forms a transient damping coefficient:

$$k = 1 - \frac{1}{\frac{\frac{\delta V_{ramp}}{\delta t}}{\sigma_{os}}} \tag{3.17}$$

where N represents the number of column comparators, C_{ramp} is the total ramp capacitance and ΔV_{dp} is the differential pair drain node swing during toggling. The transient damping coefficient k is dependent on the ramp slope and the comparator offset variance σ_{os}. Under uniform comparison voltage conditions, higher comparator offset dampens the strength of the momentary transient kick on the ramp, assuming that the column offset has a random uniform distribution. Column offset is usually Gaussian which is why this model can be treated as a first order approximation.



(a) **(b)**

Figure 3.16: Simultaneous comparator kickback noise effect on shared ramp reference lines with and without comparator input-referred offset: a) no offset; b) 10 mV offset

Figure 3.17 shows linearity evaluation plots of a real reference system driving 1024 column-parallel ADCs with a load of 100 fF each and realistic comparators. The top plot shows the

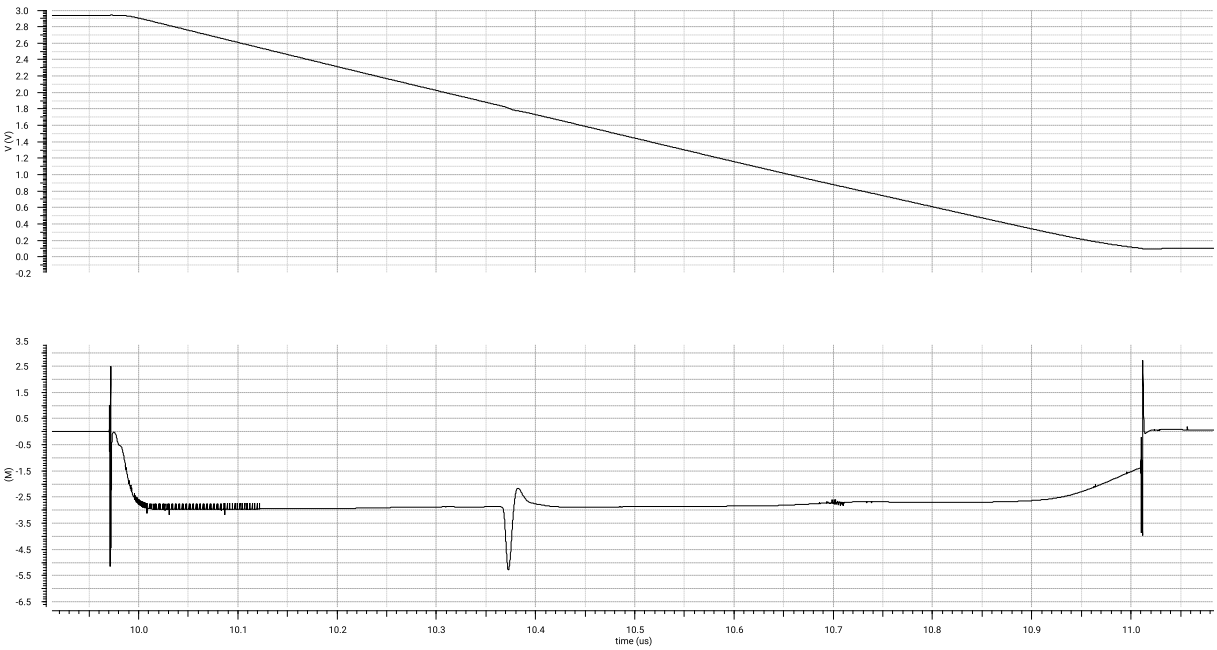


Figure 3.17: Ramp linearity evaluation of a real reference system. Top plot shows the reference voltage line; bottom displays the first derivative of the ramp. Kick on the ramp can be seen around time=10.4 µs

gradually slewed reference voltage line, while the bottom displays the first derivative of the ramp voltage. This calculation technique allows for detection of small disturbances, which are otherwise hard to distinguish in the conventional time-domain voltage waveforms. In this example case, the kick on the ramp can be observed to be within 350 µV which occurs at around time=10.4 µs. Ramp slew nonlinearity due to current sources exiting saturation and channel length modulation can also be identified with such techniques, which is seen as a static offset between the start and stop of the ramp in Fig. 3.17.

3.6.2 Wave Effects and Crosstalk on the Ramp Line

Wave effects occurring on the ramp line are illustrated in Fig. 3.18 which shows kickback propagation at intermediate points on the ramp line. R_p denotes the parasitic line resistance, C_r is the local per-comparator damping capacitor and C_{pk} models the coupling parasitic differential pair capacitor driven by a step input. If we assume that all comparators have no input offset and are all driven by the same DC input, the following wave propagation occurs: at time t_0 the comparator at node A toggles, which causes a wave propagation to node B and C after time $2 \times \tau_{RC}$ which is the propagation skew through two columns. The propagated disturbance to node B triggers the comparator at node B, and after comparator evaluation time τ_{cmp} a new kick wave occurs at node B. The latter propagates to nodes A and B for $1 \times \tau_{RC}$ and the newly propagated wave triggers the comparator at node C, which injects kickback charge after time τ_{cmp} propagating back to nodes B and A.

The kick waves are dampened as they propagate along the columns, however, even low-amplitude

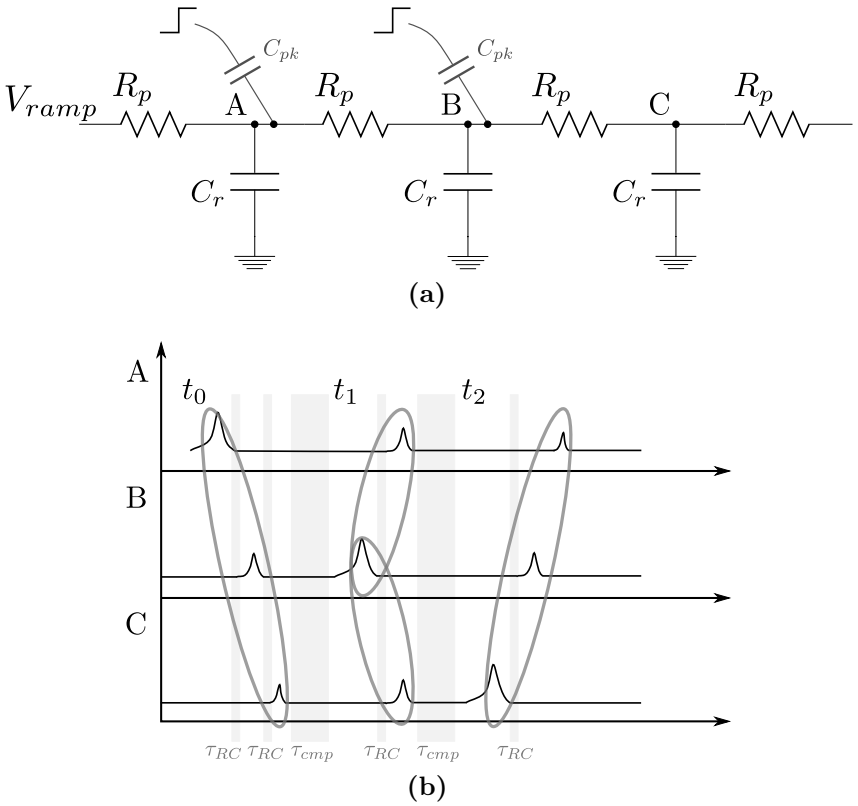


Figure 3.18: Wave propagation: a) equivalent ramp line model; b) wave propagation at intermediate points A, B and C

glitches can trigger consecutive columns. Thus, in the case of uniform input voltage and minimum offset, a single kick at the first column initiates a wave trigger chain reaction which propagates throughout all columns. Kick wave effects on the ramp are complex dynamic relationships which are difficult to model or simulate due to the extreme coupling complexity between all shared columns in an image sensor. A usual solution to the kick wave problem is root cause elimination by designing low-kickback comparators. Alternatively, an increase of the ramp load can also dampen kickback passively and forms another possible solution to the problem.

3.7 Discussion

This chapter provided an overview of the ramp generation process in SS ADCs. An analysis of the noise accumulation during the continuous-time phase was presented. While it is possible to dampen thermal noise from the ramp to an insignificant level, it is important that the ramp derivative (time) is also taken into account when calculating the predicted output ADC noise.

A set of second-order effects impacting the references were also introduced. To achieve high ADC linearity, all continuous-time ramp generator topologies require a voltage control feedback mechanism linked to the count clock frequency. Such feedback compensates any long-term clock jitter impact on the INL of the ADC by an equivalent negative correction in the voltage

ramp derivative. Further, all column-parallel systems exhibit kickback noise injection on the ramp reference, which is induced by the comparator. A few common mitigation methods were presented along with insight on the impact of comparator offset on kickback noise.

Basing on the conducted work there remains a possibility for future investigations on comparator crosstalk. It may be beneficial that coupling through kickback is modelled mathematically in-depth — perhaps by comparing column-parallel comparators in relation to another natural coupling system — a mass-spring coupled structure. That way various kickback damping mechanisms from 2nd and higher orders could be explored as potential mitigation methods.

In the next chapter we explore the design of a TDC-interpolated single-slope ADC topology. Along the architecture details, the presented topology uses continuous-time integrator ramp generation method. Concrete implementations for ramp generation, including a kickback noise suppression scheme using a dynamic comparator bias approach are presented and follow-up on the challenges in accurate ramp voltage generation.

4

Design of a Column-Parallel Flash TDC-Interpolated Single-Slope ADC

Contents

Single-slope ADCs are limited in speed due to the associated high number of count periods with

increase of bit-resolution. One way to exploit the simplicity of the single-slope (SS) architecture, while maintaining high-speed operation is through clock interpolation. An architecture which shares similarities with the Grey-coded SS scheme is Flash TDC interpolation earlier introduced in Chapter 2. Originally proposed by R. Nutt [71], this method uses a coarse SS counter and time-domain measurement of the quantization error between comparator toggle and the next clock edge using a Time-to-Digital Converter. More recently, such schemes applied to column-parallel implementations which use a delay-locked-loop (DLL) to provide accurate multiphase clocks and form a Flash TDC (FTDC) have been actively explored [21], [22], [28], [72], [73].

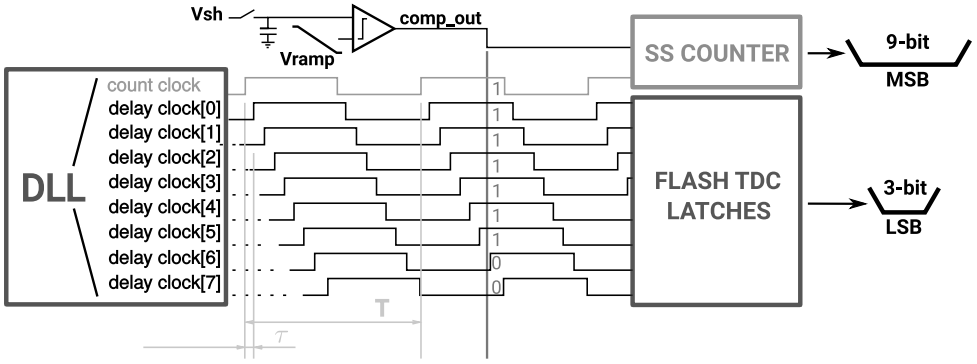


Figure 4.1: Concept of DLL-based Flash TDC-interpolation in single-slope column-parallel ADCs.

This chapter reports an innovative implementation of a Flash TDC interpolated SS ADC applied to a column-parallel CMOS image sensor. A small fraction of the material in this chapter has been reported earlier in [I] and [III] which is Copyright of IEEE. Consents from all authors have been taken for the reproduction of some images and text.

4.1 Introduction

As one may recall from Chapter 2, Figure 4.1 shows a conceptual diagram of Flash TDC interpolation in SS counters using a DLL in a column-parallel configuration. During a comparator toggle event, the SS counter and Flash TDC latches are stopped, which digitize the delayed phase states. The information in the latches is then converted from thermometer to binary code, and both are directly concatenated to the MSB (SS counter) word which forms the final ADC output word. The DLL ensures that the alignment of the Flash TDC operation period reduction clocks is locked with the main count clock edge. In order to maintain monotonicity, the total sum of all delays in the DLL line in a Double Data Rate (DDR) single-slope counter should be within the tolerance of

$$T = \sum_{i=0}^{2^N} \tau_{dly_i} = \frac{T_{clk}}{2} \pm \left[1/2 \times \frac{T_{clk}/2}{2^N} \right], \text{s} \tag{4.1}$$

where T_{clk} is the count clock period, τ_{dly_i} is a single delay unit and N is the interpolation resolution in bits.

However, employing a global DLL increases the system complexity, and imposes difficulties in high column number implementations due to RC clock degradation in long clock lines. This introduces metastability errors and requires clock phase re-buffering which adds additional phase-to-phase mismatch. The latter is especially true when the phase difference of one TDC quantization step approaches the gate propagation limit of the used CMOS process. Although various phase averaging and interpolation re-buffering schemes can be used to improve the long-line distribution of the DLL clocks, these typically come at the cost of increased complexity and power [74], [75].

To reduce sensitivity to clock line degradation and metastability errors this chapter investigates the idea of using an open-loop, local per-128 column delay lines with added TDC code redundancy. This also avoids the necessity of a DLL by employing a digital TDC gain correction method. It compensates the open-loop delay element drift with Process Voltage and Temperature (PVT) variations, which can also be regarded as an equivalent to digital gain feedback loop.

Section 4.2 presents the concept of Flash TDC-Interpolated Single-Slope (FTDCSS) systems with radix correction. Details on radix estimation, digital gain correction and architecture-inherited errors are also described respectively. Section 4.3 provides design details of an ADC test-array implementation of 1024 columns, while Section 4.4 presents characterization results of the implemented testchips. Section 4.5 provides a discussion on the implemented testchip and the implications and use expandability of the proposed digital gain correction method.

4.2 Architecture and Radix Calibration

Figure 4.2 shows a high-level overview of the proposed ADC architecture, while the concept of the FTDCSS ADC is presented in Fig. 4.3.

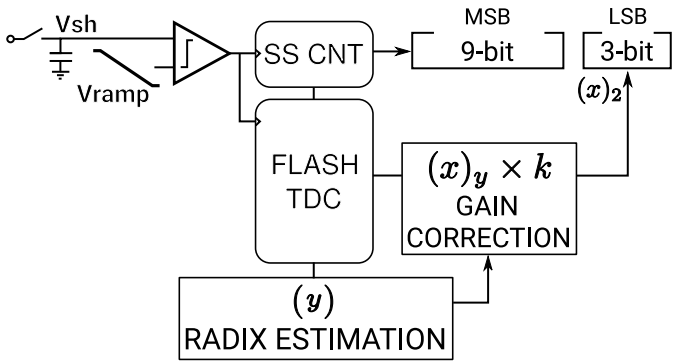


Figure 4.2: System-level concept of the interpolation method with gain calibration

A count clock incrementing an SS ADC counter is fed through a chain of delay elements. This provides an N number of multiphase clock taps, phase shifted by time τ. During an A/D comparator toggle event, the state of the main and multiphase clocks are latched. Each additional clock phase adds one quantization step whose value, after thermometer to binary code conversion, is directly concatenated as a lower 3-bit LSB word to the 9-bit MSB word of the main binary SS counter. One principal requirement for the successful direct word concatenation in TDC-interpolated SS ADCs is that, the SS counter and interpolating TDC yield a radix-2

output word. Thus, for the general case of an FTDC interpolating a DDR SS counter, the total sum of the delay phases must equal 1/2 the clock period T.

In order to maintain DNL of less than 0.5 LSB, the delayed clocks must be designed such that the deviation of the sum of all delays is less than ± ½ τ_{dly}. The same is also applicable to the delay-to-delay matching. The design of fixed analog delay elements, which maintain stable delay time within PVT corners is challenging, if not impossible, without the use of some form of referenced feedback. For example, schemes in [21], [22], [28], [72], [73] use DLL clock generators with a stable clock reference to maintain phase accuracy.

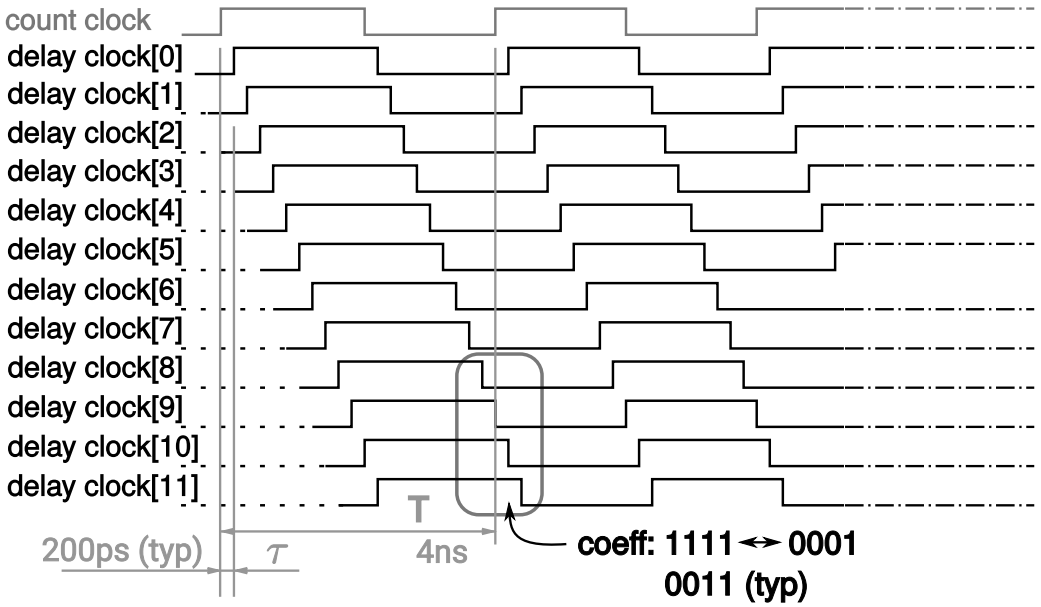


Figure 4.3: Principle of Flash TDC-Interpolated SS ADCs

This work uses a digital feedback and solves the delay element and clock period matching problem by employing TDC code redundancy with a follow-up TDC code retraction back to radix-2. This is achieved using an online in-column calibration operation. The interpolating TDC is formed by eight primary clock phases delay_clock[0:7] and four additional clocks delay_clock[8:11] which introduce the redundancy and lower the TDC radix – it is designed to vary from 1.4 to 1.8. The delays are designed such that under all PVT corners, the last 4 clock phases yield an overlap with the main count clock edge within the limits of "1111" - "0001", as shown in Fig. 4.3. The typical targeted overlap value is "0011" (radix 1.6), this maximizes the margin for delay drift with PVT corners in both slow and fast directions.

4.2.1 Radix Estimation and Digital Gain Correction

A measurement of the overlapping phases with the rising edge of the main count clock provides a correction coefficient which acts as a feedback which determines the intrinsic FTDC gain. This allows the correction of its radix back to 2 using a scaling multiplication operation.

Following the overlap, we can derive four scaling coefficients which follow the function

$$c = f(s) \begin{cases} {}^{8}/_{9} = 0.89, & s = \text{"1111"} \\ {}^{8}/_{10} = 0.80, & s = \text{"0111"} \\ {}^{8}/_{11} = 0.72, & s = \text{"0011"} \\ {}^{8}/_{12} = 0.67, & s = \text{"0001"} \end{cases} \tag{4.2}$$

where c is the multiplication coefficient and s is the stored correction coefficient value. The multiplication coefficients are derived by the normalization of all 12 possible quantization levels in the range between the rise and fall edges of the main clock, with the four redundant quantization levels. Fig. 4.4 shows binary maps of all possible allowed quantization combinations for the four allowed correction coefficient scenarios. Each column represents a single discrete state in time, while rows CK and $J0 - J10$ visualize the possible latch states of the clock phases retaining information. Phases spanning beyond the next edge of the count clock (>1/2 T_{clk}) are discarded as they do not provide any signal information states. For example, phase $J10$ in case of coefficient "0011", phase $J9, J10$ for "0111". These are instead used to determine the radix and form a calibration coefficient.

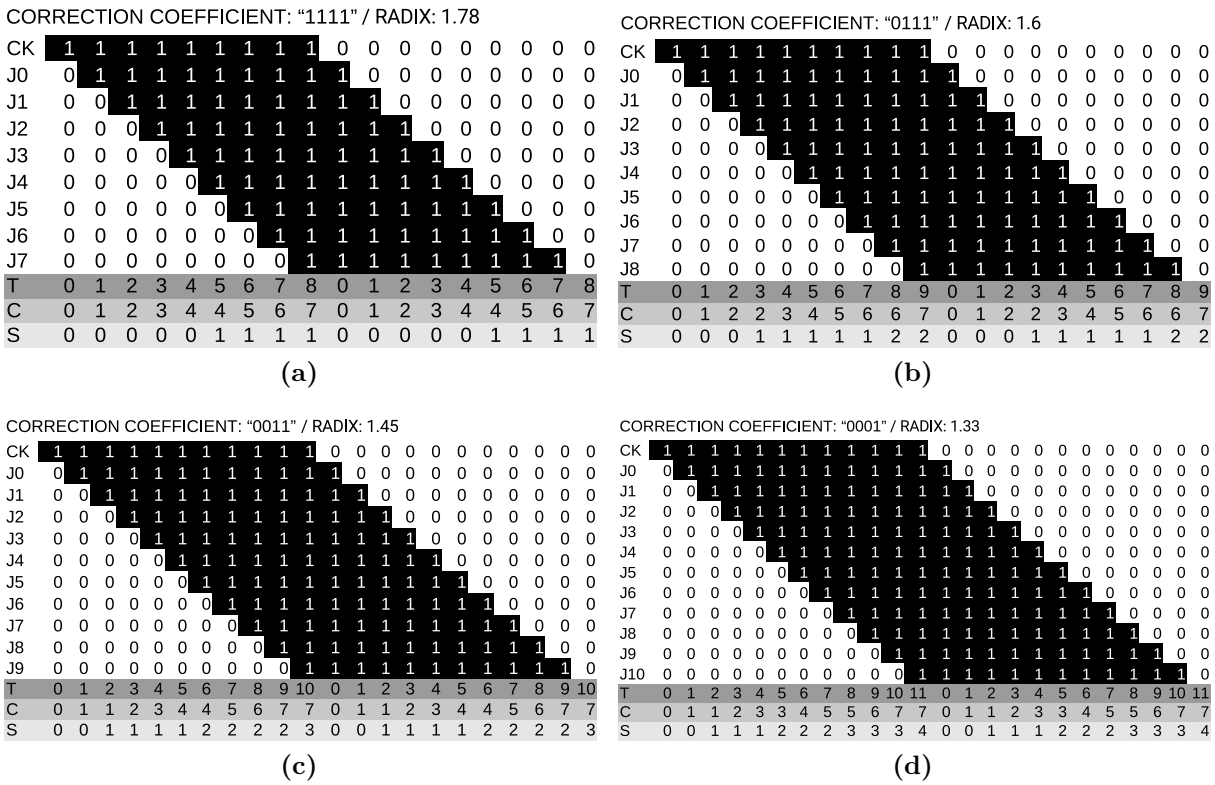


Figure 4.4: Binary maps of the four allowed quantization combinations

The row denoted with T shows the sum Digital Number (DN) of the raw (uncorrected) TDC signal, C presents the ideal value after correction obtained by applying the coefficients in Equation 4.2, and S shows the difference between T and C. As floating-point multiplication operations are hardware and time-costly arithmetic operations these are generally unsuitable for

column-parallel implementations. Thus, a primitive signal-dependent fixed-point subtraction is implemented which is a balanced compromise between accuracy and area. Moreover, the acquisition of the correction coefficient is also fixed-point which nevertheless leads to a fixed-point result. From the binary maps in Fig. 4.4, it can be observed that S (the signal-dependent subtraction) increases with the increase of T (the TDC DN count). Hence, it effectively provides the subtraction count needed for correcting each signal value, which makes it equivalent to a fixed-point multiplication.

4.2.2 Architecture-Inherited Nonlinearity

A fixed-point digital multiplication introduces numerical noise due to residue truncation which variably alters the ADC code step width – thus, translating into differential nonlinearity (DNL).

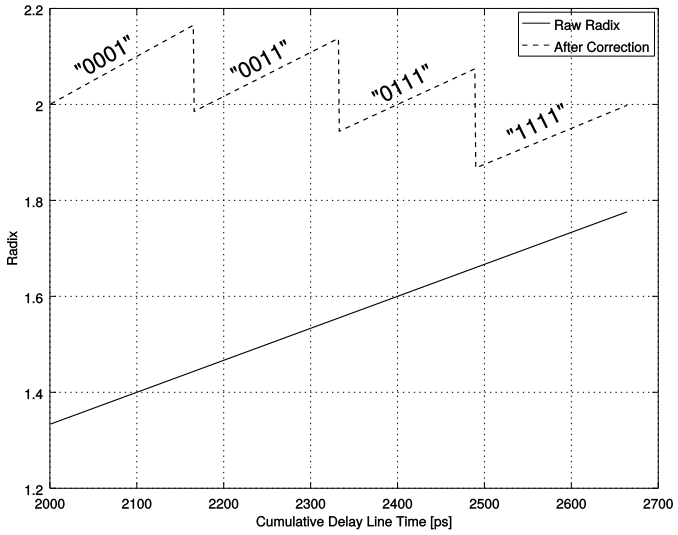


Figure 4.5: TDC radix comparison, before and after TDC gain correction

A graphical overview of the exhibited numerical noise effect is shown in Fig. 4.5. This presents the estimated radix before and after gain correction versus the total delay line time, which is affected by PVT corners. The shown case of a 4 ns period count clock requires a nominal total delay line time of ~2.3 ns to achieve an overlap coefficient of "0011" equivalent to ±0.333 ns (2 ns/12 × 2) for spanning within the range "1111 - 0001". If we consider a normalized reference voltage of 1 and following the map cases in Fig. 4.4, we can note that one LSB out of the maximum 11 information retaining quantization steps is equal to 0.091, which needs to be compressed back to 8 steps having an LSB of 0.125. Following this approach, the maximum architecture-inherited linearity errors ϵ_{DNL} due to residue truncation (indicated in Fig. 4.5) are estimated to occur at coefficient "0001" and "1111" or

$$\epsilon_{\text{DNL}} = \pm \left| \frac{(1/8 - 1/11)}{1/8} \right| = \pm 0.272 \text{ LSB}. \tag{4.3}$$

Architecture-inherited DNL errors are generally acceptable, as long as the former, combined with delay mismatch yield a total absolute DNL of less than 1/2 LSB throughout the entire ADC range. The integral nonlinearity (INL) of the ADC is not affected by the correction

scheme, because it is dominated by the nonlinearity of the ramp voltage reference generator and the column comparator.

4.2.3 Clock Duty Cycle Impact

As the proposed scheme is double-data-rate operated, errors in the duty cycle of the main count clock of the SS counter modulate the radix of the rising and falling edge interpolation. This translates into DNL jump at the interpolation point or every even/odd LSB bit of the MSB SS counter. The maximum tolerable duty cycle variation [%] maintaining a DNL of less than 0.5 LSB is defined as

$$\epsilon_{duty} = \Big(\frac{T_{half} \pm \tau/2}{T_{clk}} \times 100\Big) - 50 = \pm 3.125\ [\%] \tag{4.4}$$

where τ is one unit delay time and the calculated worst case duty cycle deviation is for a count clock of $T_{clk} = 250$ MHz. This requirement is also applicable to the phase-to-phase clock duty cycle matching.

4.3 Design of a Column-Parallel ADC Testchip

To test the proposed architecture, a 1024 column × 128 row linescan test sensor was designed. Fig. 4.6 shows a physical block overview of one out of eight 128-column ADC cluster groups. To accommodate the clock delay line and correction circuitry in each group, the implementation uses stepping in the column pitch. Such configuration allows for group-central real estate for clock driver placement, which minimizes the multiphase clock degradation gradient along the columns and improves metastability errors in the TDC.

4.3.1 System-Level Design of the FTDCSS ADC

Each ADC group contains individual TDC control blocks: clock delay line, a global correction coefficient memory and an error correction block. Fig. 4.7 shows a principle schematic diagram of the FTDCSS ADC core. Each column contains 11 TDC latches which are differentially driven by the clock delay line and are differentially latched by the comparator. All TDC latches share a vertical bitline through individual switches, which is used for latch data readout after the end of the ADC ramping phase. Through the *bitline*, the value of the TDC register is scanned and converted sequentially from thermometer to binary code by incrementing a 3-bit LSB counter. The TDC gain correction occurs during the TDC latch scanning process by correction coefficient driven control of the opening of the SW0-SW10 switches, sequenced by the error correction module.

As the TDC interpolates a DDR MSB SS counter, depending on the SS counter LSB value, the counted states in the TDC latch should be high (ones) if the MSB counter's LSB value has stopped high, or low (zeros) if the MSB counter LSB has a low state. The rationale behind state inversion can be understood by observing the first row CK (the LSB state of the MSB

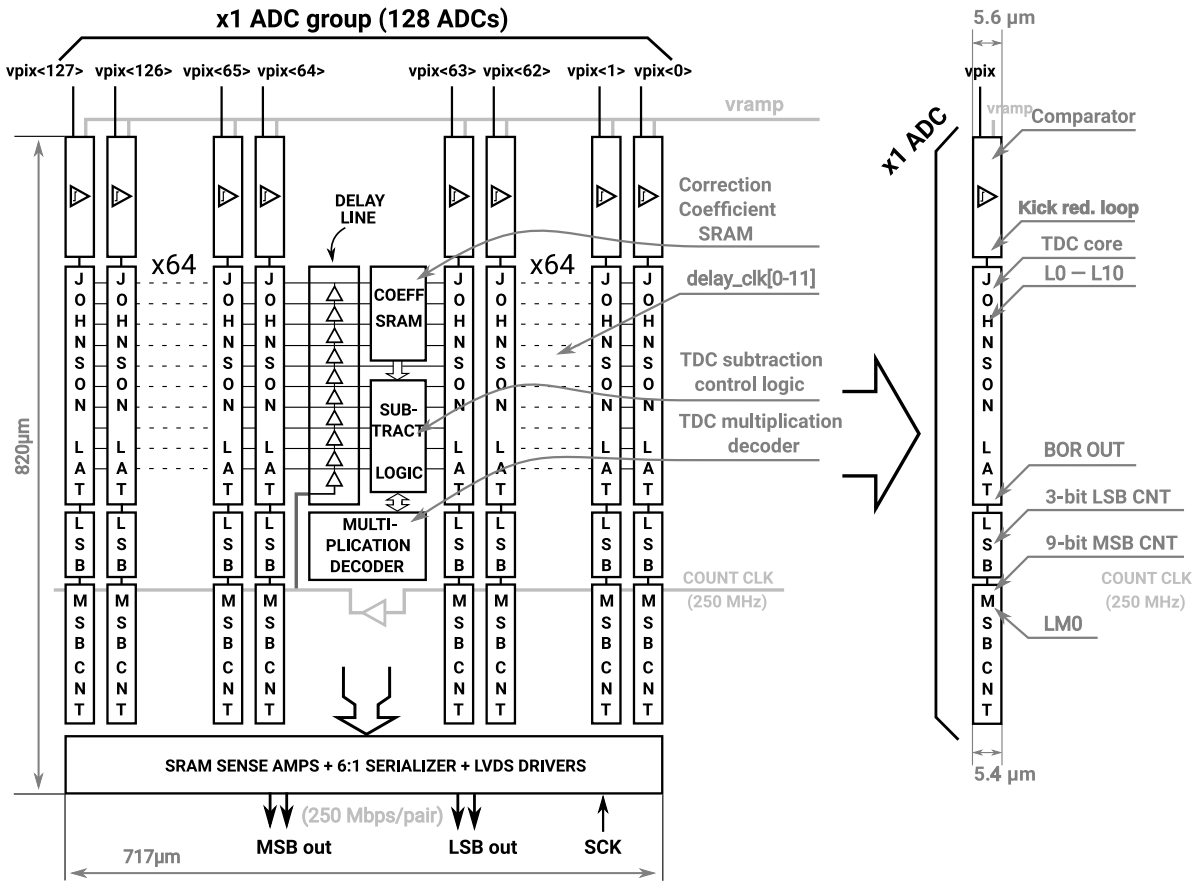


Figure 4.6: Floorplan of a single (128-column) FTDCSS ADC group, ([I], reprinted by permission of IEEE)

counter) in the binary maps in Fig. 4.4. When CK is low (zero), the TDC latch states $J0$-$J10$ are inverted. To achieve the inversion, the *bitline* signal, after being sensed, passes through an XOR gate which is controlled by the LSB of the MSB counter.

A Digital Correlated Double Sampling (DCDS) mode is implemented using the counter inversion method and is applied to both the MSB and the LSB counters. Performing DCDS on the entire interpolated 12-bit word requires a borrow-out operation to ensure that a single count decrements from the MSB counter. This is only valid when the subtracted TDC words from SHR and SHS sampling result in an underflow. The latter is executed by the BOROUT block (Fig. 4.7), which ensures a borrow-out propagation link between the LSB and MSB counters. Each column contains dual swappable sample and hold capacitors which allows for a fully pipelined mode of operation.

Figure 4.8 displays the timing procedure of a complete DCDS conversion, while Appendix C shows more detailed external sequencer data. After the counter and reset voltages are set to their initial conditions with *count_rst*, the MSB counter gate is enabled globally following *count_en*. During the count period, the digital sequencer introduces 255 count clock cycles while the ramp reference is slewed. At the instance when the input sample and ramp cross, the comparator toggles freezing the MSB counter and the TDC latch content. When *count_en* is

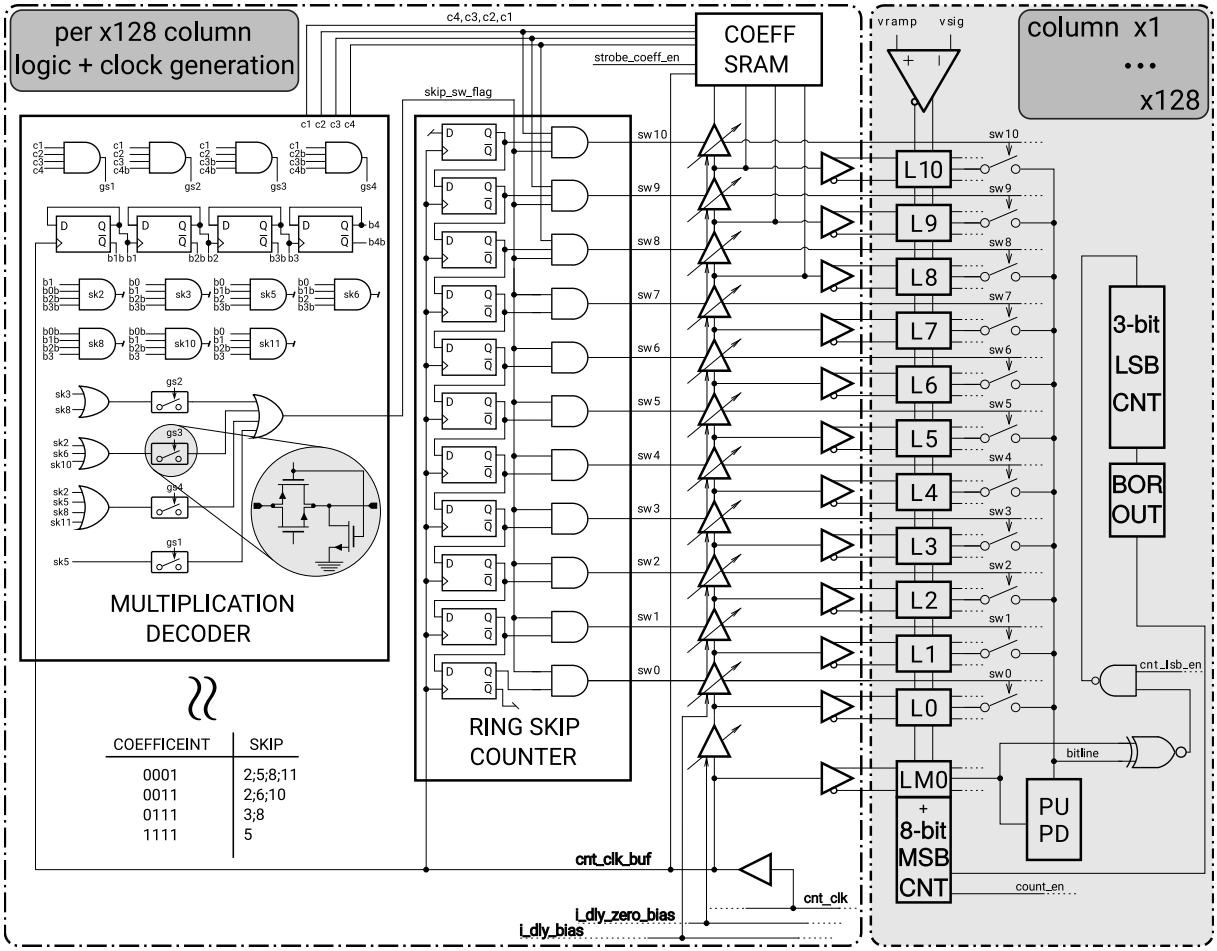


Figure 4.7: FTDCSS core principle block diagram

disabled, the conversion operation is finished and the last correction coefficient acquired during the conversion phase is stored into the coefficient storage memory *coeff[3:0]* by the *strobe_coeff_en* signal. After the MSB count phase, the LSB counter is enabled with *count_lsb_en*. During that period the sequencer issues twelve count clocks on *count_clk* which drive the ring skip counter. The latter addresses each TDC latch consecutively, while skipping those latches flagged by the *sw_disable* signal. The flag signal is issued by the multiplication decoder and controlled by the stored correction coefficient and algorithm in Fig. 4.4. To perform DCDS, the values of both counters are inverted followed by a second A/D conversion operation of SHS. Finally, the counter state is transferred to a shadow SRAM for readout via per-group 2 × 6:1 serialization blocks and LVDS Tx.

4.3.2 Analog Front End

The Analog Front End (AFE) of the ADC has been designed for ease of testability, and does not necessarily provide the best signal conditioning to readout the pixel and utilize its maximum voltage swing. Instead, the pixel design was altered to match the input range of the ADC.

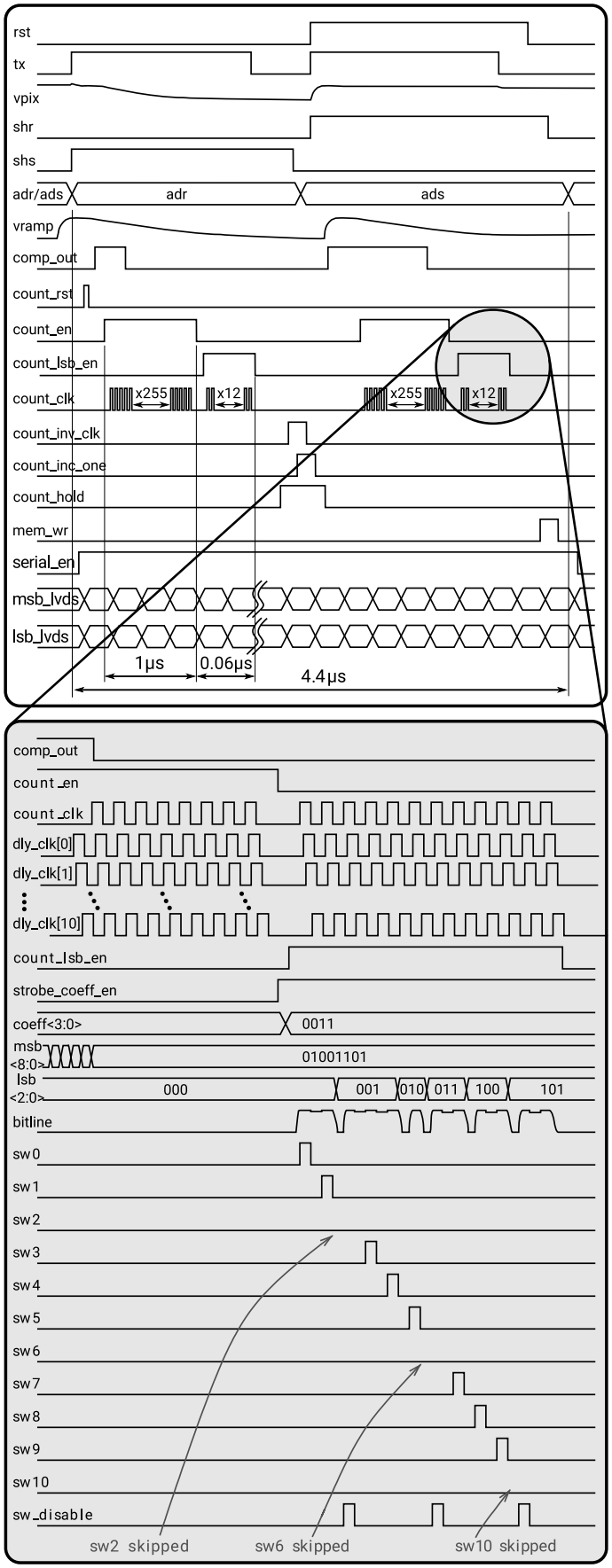


Figure 4.8: Principle ADC timing diagram with top plot showing global signals while the bottom plot showing in-group signals

The readout gain modes of 1×, 2× and 4× are implemented through ramp slope modulation. This approach does not offer the same noise performance but higher, at larger than 1× gain, as compared to a system which uses a Programmable Gain Amplifier (PGA). A PGA ensures the signal swing at the input of the ADC to be always maximized – thus reducing the impact of ADC-induced noise at the final output digital word.

Signal Input and Sample and Hold

Figure 4.9 shows the analog voltage input configuration and a principle diagram of the sample and hold block. All column ADCs use an analog multiplexer which selects between two globally shared individual test voltages V_{SHR}, V_{SHS}, and the internal pixel column-level bitlines.

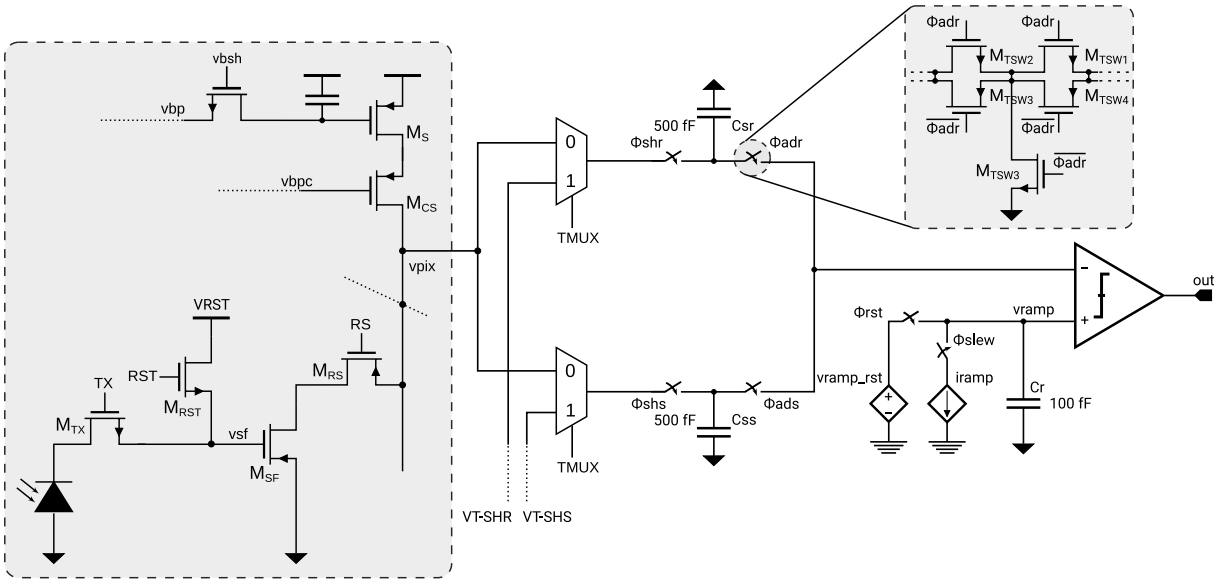


Figure 4.9: ADC Front-end and Sample and Hold

Designing a PGA to allow the accommodation a large pixel voltage swing and matching with the input range of the comparator unnecessarily increases the complexity of the test system. Instead, in this implementation the pixel (as shown under the highlighted area in Fig. 4.9) is adapted such that its output range overlaps the input range of the N-FET input differential pair of the comparator. The pixel employs a P-FET source follower and row-select transistor, which are indicated as M_{sf} and M_{rs} in Fig. 4.9. In order to be able to perform true correlated double sampling with this pixel configuration, the reset level ($VRST$ - charged via transistor M_{rst}) has to be independent of the pixel source follower supply voltage. There are two possible methods for achieving true CDS with this pixel; one is to reduce the pixel reset voltage level to maintain the source follower $V_{gs} > V_{th}$ and $V_{ds} > V_{dsat}$, or either the supply voltage of the biasing current source can be raised beyond 3.3V to increase V_{gs} and V_{ds} to maintain saturation. If the source follower is not operated in saturation, even if the charge has been successfully transferred from the diode to the floating diffusion (FD), the readout of the reset level is not possible. Both approaches compromise the total dynamic range of the pixel, however despite the drawbacks, a decision was taken to omit the design of a PGA, as the pixel dynamic range will not limit the possibility for rigorous testing of the ADC.

In order to fully utilize the speed gains of the ADC, a fully pipelined sample and hold stage has been implemented. The latter makes use of dual Metal-Insulator-Metal (MIM) capacitors each having a capacitance of 500 fF to dampen kTC noise an order of magnitude lower than the quantization noise of the ADC in 12-bit mode. The switches Φ_{ADR} and Φ_{ADS} are used to select the signal or reset conversion sampled voltage source, and Φ_{SHR} and Φ_{SHS} are the input sampling switches. To minimize the impact of charge injection and clock feedthrough, the latter were chosen to have a size approaching the process minimum allowed, but still large enough to accommodate dual source-drain contacts for reliability. To minimize charge injection the P/N FET devices of the sampling transmission gates were chosen to have an equal gate capacitance which to a first order follows

$$W_p L_p C_{ox_p} = W_n L_n C_{ox_n} \tag{4.5}$$

where C_{ox_p} and C_{ox_n} is the gate oxide capacitance in F/m^2. Additionally, minimizing charge injection requires that the input and output switch node impedance is of an equal magnitude. The switches share the top plates of the capacitor. In order to reduce clock feedthrough the transmission gate switches use the T-switch based topology shown in Fig. 4.9. It clamps switched-off floating nodes and neutralizes any charge injection or clock feedthrough from adjacent nodes through least resistance path drainage.

Comparator and Ramp

The column comparator uses the single-ended continuous-time architecture shown in Fig. 4.11a, whose structure was inspired by [76]. Each column contains a local ramp load MIM capacitor C_R which is used for passive reference voltage generation through current integration. To improve linearity, C_R significantly dominates the nonlinear gate capacitance C_{gd} of the differential pair device M1. The choice of sizing of the linearization MIM capacitor is directly linked with the dynamic range of the ADC, its resolution, and the lumped nonlinear capacitance of the differential pair device.

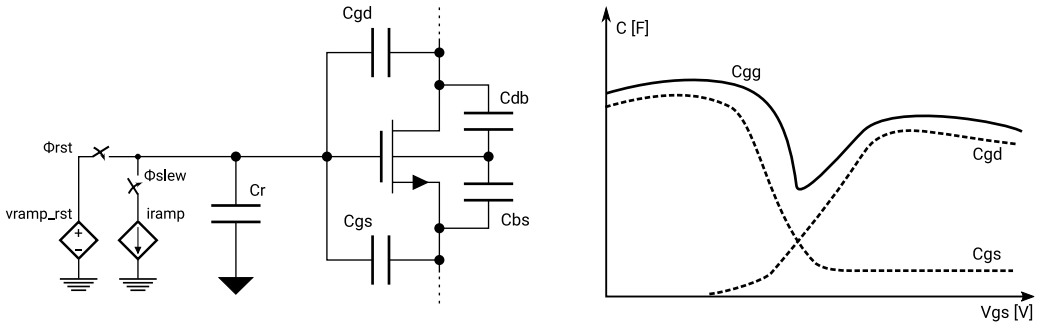


Figure 4.10: Ramp linearization MIM capacitor

Figure 4.10 shows a simplified illustration of the linearization effect. In order to dampen any nonlinearity below 1 LSB on the constant-slew-generated ramp, the minimum MIM capacitor

size can be estimated by

$$C_R = \frac{\max\left(C_{GG}(V_G)\right) - \min\left(C_{GG}(V_G)\right)}{\epsilon_{NL}} \times \left(V_{REF_H} - V_{REF_L}\right) \tag{4.6}$$

where ϵ_{NL} is the minimum desirable nonlinearity and max/min C_{GG} is the absolute nonlinear capacitance of the differential pair device throughout the ramp voltage span $V_{REF_H} \div V_{REF_L}$.

All sampling capacitors and reference currents use an individual quiet ground with no quiescent current flow to improve noise isolation. During reset operation, the distributed 1024-capacitor ramp reference line is pre-charged to a reset level at the upper saturation input level of the comparator (2.95 V). The basic reset drive and ramp intergator topology is shown in Fig. 4.11b. At the same time the signal is sampled on C_{sr}/C_{ss} and connected to the non-inverting differential pair input through an SHR or SHS selection switch. With the start of the counting process, the reference line is gradually discharged through a wide-swing self-biased constant current source, which creates the linearly decreasing reference voltage. Comparator kickback noise has a profound effect on passive schemes due to the insignificant damping factor of the local ramp MIM capacitor C_R with C_{gd} of the differential pair device.

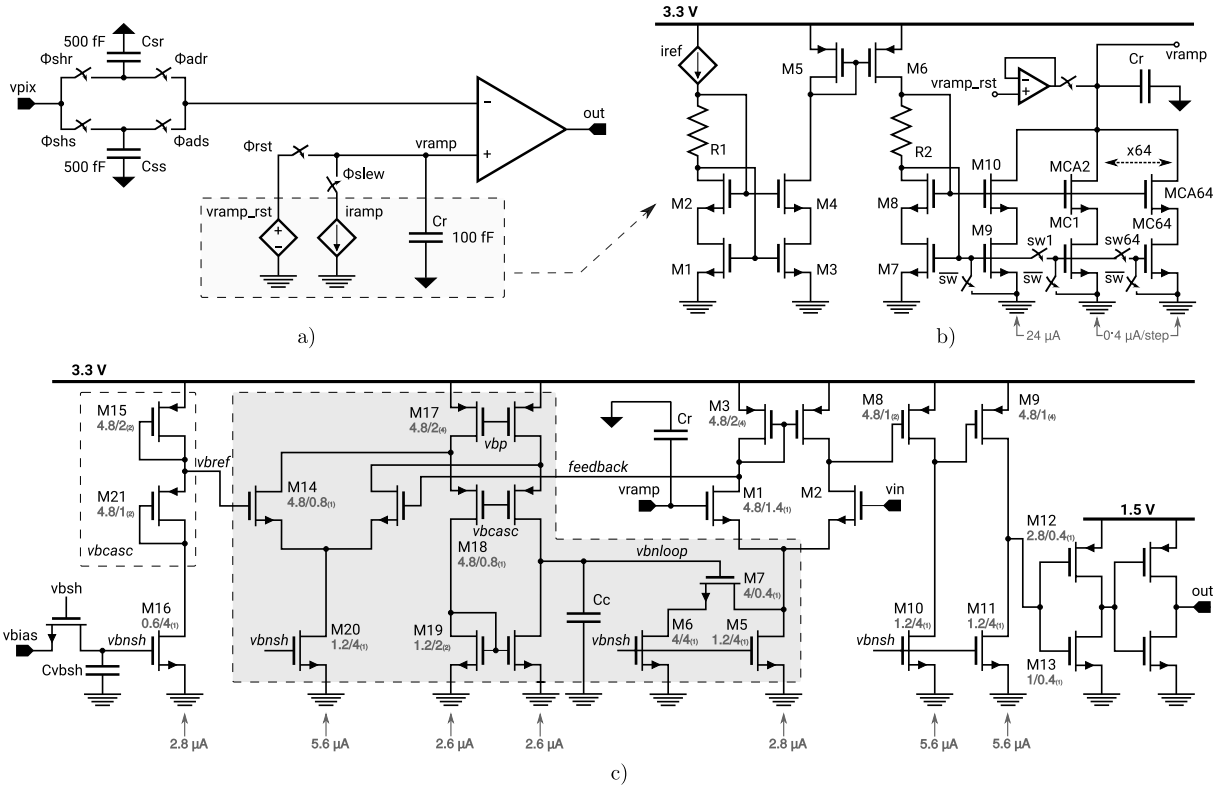


Figure 4.11: Column comparator: a) top-level schematic; b) ramp generator topology; c) comparator core

To mitigate kickback noise, the dynamic bias compensation scheme highlighted in Fig. 4.11c has been used. The comparator is formed by the bandwidth-limited differential pair $M1-2$ followed by two cascaded PFET common source gain stages $M8-11$. During a comparator

toggle event, the drain of the ramp device $M1$ exhibits a strong rising voltage swing, which is the cause of kickback noise due to coupling to the reference line through C_{gd}. One way to reduce the drain voltage swing is to increase the tail bias current of the differential pair during toggling. A replica bias circuit of the differential half-pair is formed by $M15 - M21$ and is used as a reference voltage to the folded-cascode error amplifier formed by $M14 - M20$ (highlighted area). The feedback from the drain of $M1$ controls the tail bias of the differential pair through the error amplifier. The tail current control is achieved through a gradual increase of the m-factor of the $M5 - 6$ tail current sources via $M7$ which operates in linear mode and varies its resistance. An exhibited lag compensation induced by $M7$ and C_c stabilizes the loop. The feedback loop is non-dominant pole compensated and has two major poles associated, one related to the parasitics on the comparator tail current source and differential pair

$$|p_1| = \frac{1}{\frac{1}{g_{ds_7}} s C_p} \tag{4.7}$$

and one related to the parasitic load of the folded cascode error amplifier:

$$|p_2| = \frac{1}{R_o C_L} = \frac{1}{\left(g_{ds_{14}} + g_{ds_{17}} + \frac{g_{ds_{18}} + g_{ds_{19}}}{g_{ds_{18}} g_{ds_{19}}}\right)\left(sC_{ndp} + sC_{gd_{14}} + sC_c\right)}. \tag{4.8}$$

To a first-order approximation the DC-gain of the comparator is determined by the product of the three individual cascaded stages or

$$A_0 = \underbrace{\frac{g_{m_1}}{g_{ds_1} + g_{ds_3}}}_{\text{STAGE 1}} \times \underbrace{\left(-\frac{g_{m_8}}{g_{ds_8} + g_{ds_{10}}}\right)}_{\text{STAGE 2}} \times \underbrace{\left(-\frac{g_{m_9}}{g_{ds_9} + g_{ds_{11}}}\right)}_{\text{STAGE 3}}. \tag{4.9}$$

As in every cascaded system the noise figure and gain of the preceding stages should be optimized to minimize noise amplification in consecutive stages. The noise contributors in the comparator architecture on Fig. 4.11c are shown below

$$\sigma_{V_{out}} = \Bigg(\Bigg(\Bigg(\Bigg(\overbrace{\left(g_{m_1}^2\sigma_{n_1}^2 + g_{m_2}^2\sigma_{n_2}^2 + g_{m_3}^2\sigma_{n_3}^2 + g_{m_4}^2\sigma_{n_4}^2\right)\frac{1}{g_{ds_2} + g_{ds_4}}}^{\text{NF STAGE1}} + \\ + \underbrace{\sigma_{n_5}^2\Big)g_{m_5}^2 + g_{m_6}^2\sigma_{n_6}^2\Big)\frac{1}{g_{ds_5} + g_{ds_6}}}_{\text{NF STAGE 2}} + \underbrace{\sigma_{n_7}^2\Big)g_{m_7}^2 + g_{m_8}\sigma_{n_8}^2\Bigg)\frac{1}{g_{ds_7} + g_{ds_8}}}_{\text{NF STAGE 3}}. \tag{4.10}$$

It may be observed that the highest (relative to the other stages) noise is contributed by the first differential pair stage. It is therefore essential that the differential pair input devices are biased in weak inversion and the differential-to-single-ended conversion mirror loads are biased in strong inversion. Ensuring such current densities will maximize the gain of the first stage. The noise injected from the error amplifier (highlighted area) through the tail bias control should be

minimal due to the high common-mode rejection ratio of the differential pair. Power and ground supply ripple rejection (P/G/SRR) has been minimized by the addition of local per-branch bias sampling capacitors, which act as local supply rail regulation feedback. The use of a sampled bias also helps in minimizing power noise crosstalk as the biases between individual columns are disconnected during the comparison operation. This allows for bias kickback isolation between individual columns. A further detailed derivation of the output poles, DC gain and noise is provided in Appendix B.

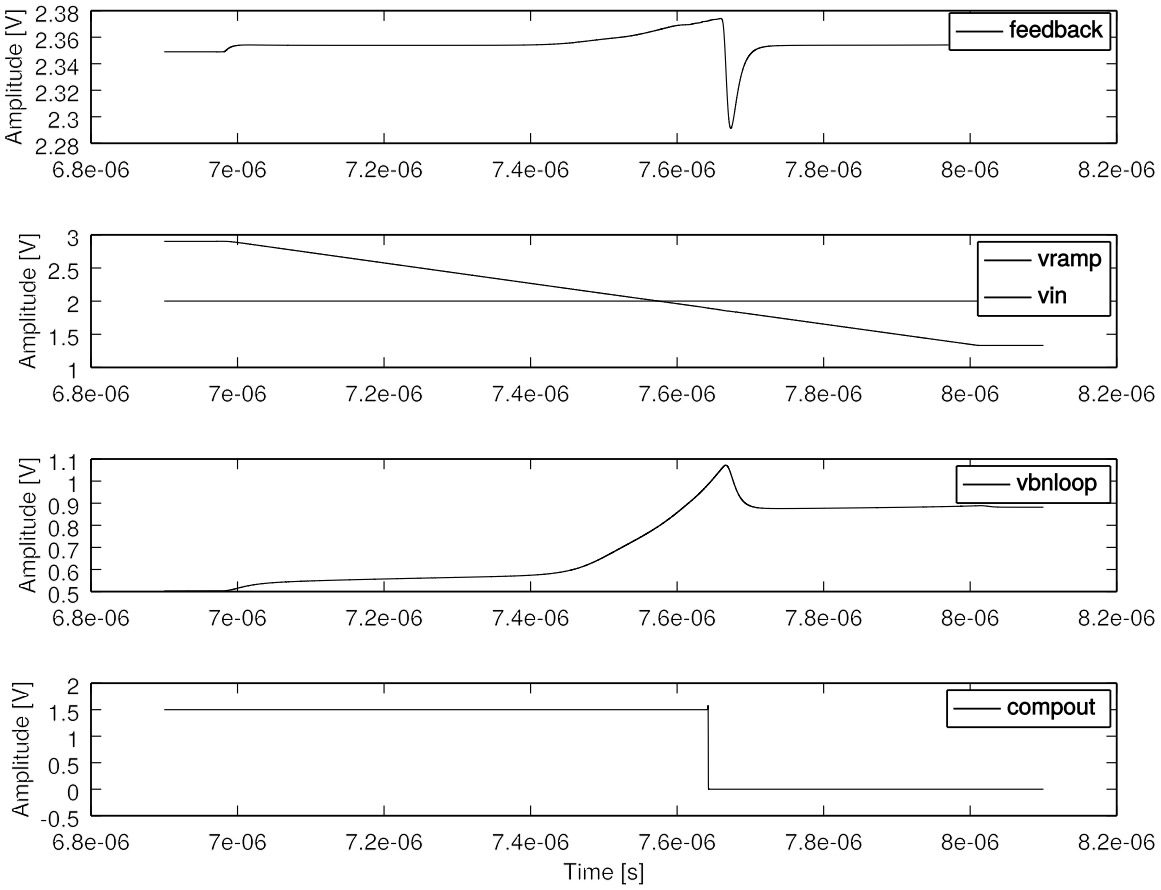


Figure 4.12: Internal comparator nodes showing input pair drain (feedback) stability leading to a constant ramp load

Figure 4.12 shows a simulation of the internal comparator nodes during the ramp phase, which use the same notation names as in Fig. 4.11c. After the ramp crosses the input signal, the output of the error amplifier senses a change on the drain of $M1$ and increases the m-factor of the tail current source, which ensures a flat voltage on $M1$ with minimum disturbance. On comparator toggling, the feedback loop settles within 50 ns while keeping voltage peaks on the drain of $M1$ to within 20-50 mV. This ensures a minimal ramp kick, while not compromising the noise performance of the comparator due to its common-mode rejection ratio. The gain of the error correction feedback loop is not critical as the drain node can tolerate differences with the error amplifier reference up to within 5-10 mV, which is equivalent to gains in the order of ×100-500. The gain of the differential pair (first stage) has been maximized by the use of long pair devices and measured at 42.8 dB typical. The total comparator gain is >130 dB, and has a PSRR of >30 dB and GRR of >34 dB which is improved by the dynamic local bias sampling

technique. The typical comparator power consumption is 60 µW with a propagation delay of 80 ns equivalent to an ADC dynamic range of ≈328 DN at 1 µs ramp time mode (250 MHz). The output comparator noise variance contribution at 1 µs ramp slope between 2.8 –1.5 V was measured to be at 350 ps, which is equivalent to ≈1 LSB at 12-bit mode.

4.3.3 TDC Interpolator

Each column TDC contains eleven identical clock latching elements $L0-10$ (annotated in Fig. 4.7) which sense the reference delay clocks. The LSB cell of the MSB counter uses the $LM0$ latch, whereas the rest of its count cells are rising-edge triggered T-flip-flops, thus forming an asynchronous counter. It is incremented by the output of the latch $LM0$, which forms the DDR count behaviour. However, $LM0$ differs from the TDC latches $L0-10$, as it has to provide a valid output logic level which increments the MSB counter.

TDC latches

Figure 4.13 provides transistor-level schematics of the TDC latch elements $L0-10$ and $LM0$. To eliminate dynamic current consumption during conversion, the TDC latch register $L0-10$ uses the latch structures in Fig. 4.13a which have their power cut during count mode. When g is high, the power to the latch is cut, while it is still driven by the complementary reference clocks *delay_clk*. During a comparator toggle event, the driving switches formed by $M3-4$ are opened while at the same time instance the latch is powered via $M1-2$, thus keeping its state and retaining a valid logic level. The transmission gate in Fig. 4.13a is used for latch readout after the end of the conversion phase through a shared bitline.

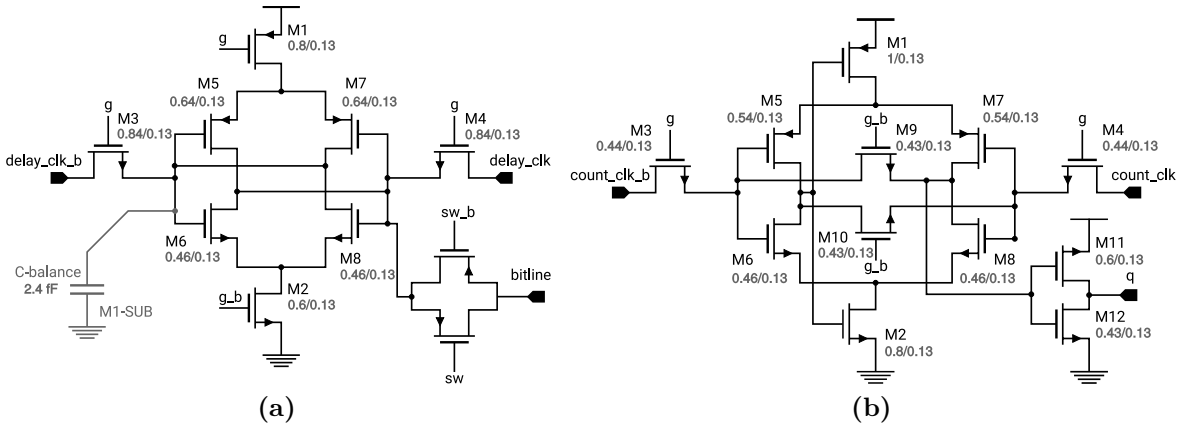


Figure 4.13: TDC latch elements: a) element L0 to L10; b) element LM0

Ensuring low interpolation errors requires that the stop response time of all TDC latches and the MSB counter to be identical. To achieve a matched latch response time while providing a valid logic level, $LM0$ uses the self-biased latch architecture shown in Fig. 4.13b. Transistors $M1-2$ sense the output of the driven latch inverter $M5-6$, and provide power to enable the output of a valid logic level. The inverter formed by $M11-12$ reduces load sensitivity by buffering the clock to the T-flip-flop MSB counter.

Operating the main clock at 250 MHz for a 12-bit linear conversion with the FTDCSS scheme requires a typical delay clock phase difference of 200 ps. To achieve accurate interpolation resolution, the time response matching between $L0-10$ and $LM0$ should be within ≈50 ps (with an added 2/3 time safety margin). Although $L0-10$ and $LM0$ share a similar architecture, their time response differs, typically with a longer propagation delay for $LM0$ due to its higher output load from the self-biasing and output inverter gate capacitances. To equalize the time response of $L0-10$ with $LM0$, a metal-substrate capacitance C_b was added to $L0-10$, thus balancing the diffusion capacitance of the bitline select transmission gate. Further, a compensating offset has been introduced between delay cell 0 and 1-10 through a

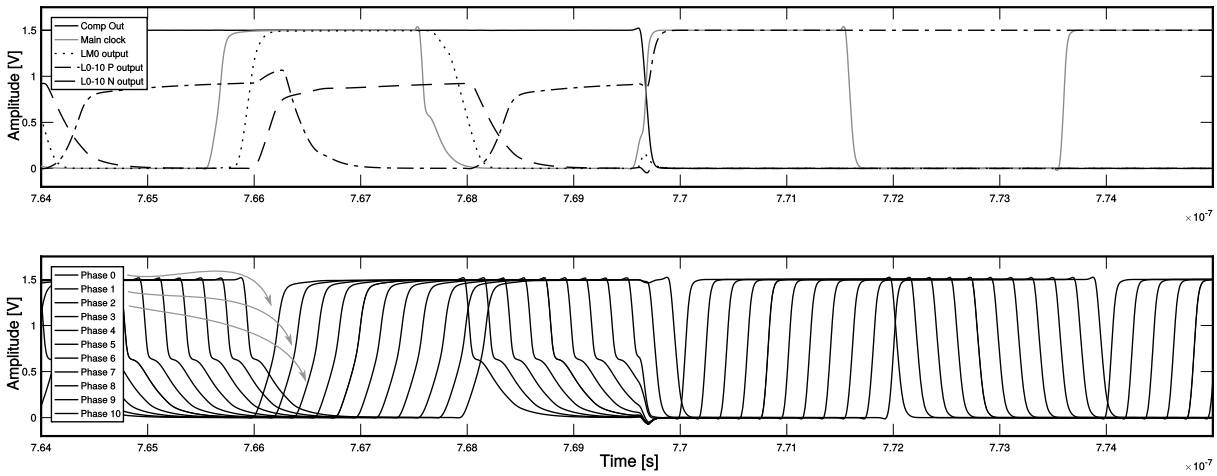


Figure 4.14: Column distributed clock phase loading before and after comparator toggle

static imbalance of the currents *i_dly_bias* and *i_dly_zero_bias*. The differential clock drive helps improve time resolution of the TDC latches and also reduces sensitivity to asymmetric loading and jitter. Figure 4.14 shows a parasitic extracted simulation of the clock phases. The top sub-plot shows the limited output node swing of $L0-10$ during count mode and the full-swing latched state after comparator toggle. The output response time of $LM0$, retaining a valid logic level before the comparator has toggled is also displayed.

The bottom sub-plot in Fig. 4.14 shows the slew of the distributed clock phases before and after comparator toggling (at Time=7.7 µs) of all 128 latch elements. One may observe a minor difference in the worst case loading conditions, e.g. see the phase delay difference before T=7.7 µs and after. In addition, the exhibited fall edge distortion at loaded conditions is caused by the nonlinear diffusion capacitance of the latches, however the latter fall below the threshold detection level of the TDC cells. To reduce the power supply variation sensitivity of the latches and delay generation, each latch cell contains a local decoupling capacitance of 35 fF. Any mismatch in the threshold of the latch devices translates into DNL errors. Thus, although being bandwidth limiting, the latch device structures are sized larger than the process minimum to reduce variation-induced linearity errors. The derivative of the rise and fall times of the clock phases is linked to metastability, DNL and noise. Thus, the reasoning behind the choice of a small ADC group size of 128 columns was driven by clock rise/fall edge oprimization.

TDC latch readout

After comparator toggling and the end of the count period, the content in the TDC latches is serially read and converted from thermometer to binary code. Figure 4.15 provides a principle diagram of the implemented column-level readout. Due to the narrow pitch a serial readout via a single vertically routed bitline has been implemented. All TDC latches per column connect to a shared bitline through latch addressing switched SW0-SW10.

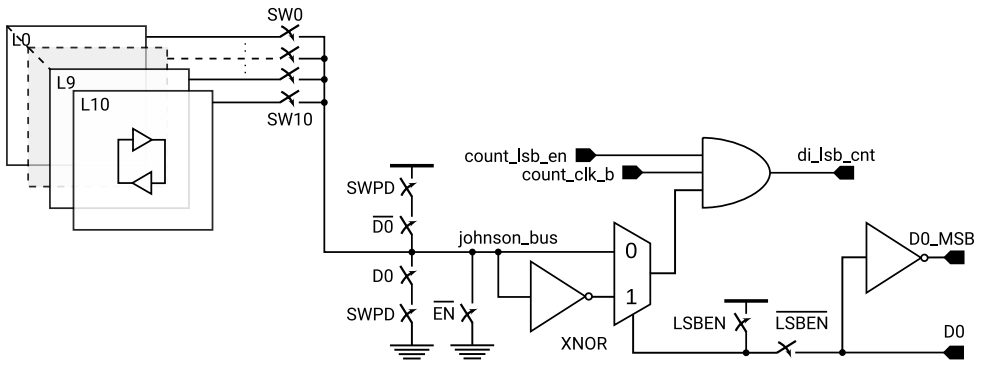


Figure 4.15: TDC latch serial readout

During the latch dumping process, the switches SWPD are switched during the first half-period phase of the count clock (Fig. 4.8). This pre-charges the shared bitline $johnson\_bus$ to a high or low logic level depending on the LSB value of the stopped MSB-counter. The latter is due to the thermometer code inversion in DDR Flash TDC-interpolation as discussed in Section 4.2. During the second half-period phase of the count clock, the $johnson\_bus$ is let floating while consecutive addressing pulse (SW0-SW10) is applied to the latches as shown in Fig. 4.8. Depending on the stored data in each latch the charge on the shared bitline is either maintained or lost. The latter is sensed by an XNOR element and is fed forward for incrementation by the LSB counter.

4.3.4 Column Counters

The column counters are implemented at a 5.4 µm pitch compared to the comparator and pixel pitch which is 5.6 µm. Such strategy has been used as it provides free in-column silicon space per ADC group which is used for circuit blocks related to the TDC.

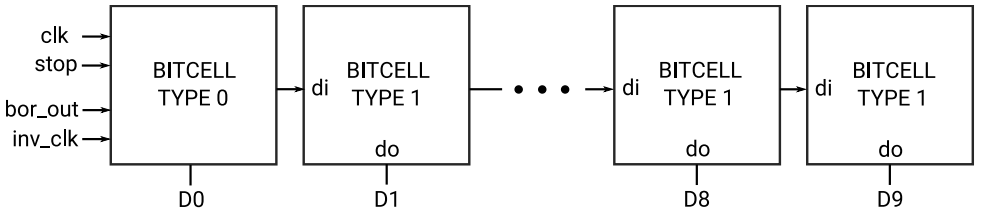


Figure 4.16: An overview of the asynchronous ripple-carry column counter

Figure 4.16 shows a block-level diagram of a single ripple-carry column counter. The counter works in a double-data-rate (DDR) count mode which requires the use of a different bitcell

structure for its first LSB bit (bitcell type 0). The rest of the counter bitcells (type 1) have an identical structure. The counter uses a two's complement word arithmetic, thus it can perform word inversion and addition with one, which is used when performing digital correlated double sampling.

MSB and LSB counters

The MSB and LSB counters are formed by identical asynchronous ripple-carry bitcells with built-in inversion capability, except the LSB bitcell of the MSB counter. Figure 4.17 shows a schematic diagram of a single bitcell.

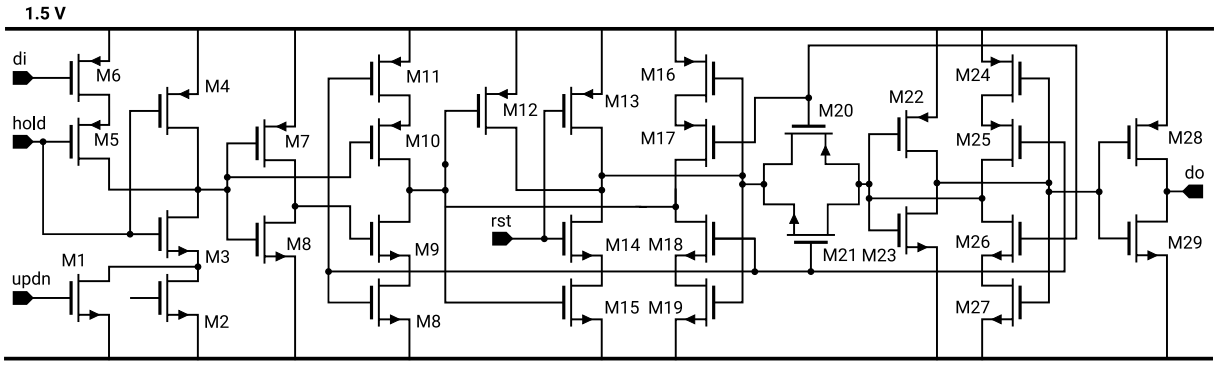


Figure 4.17: A principle schematic diagram of counter bitcell type 1

Bitcell (type 1) forms an equivalent of a JK flip-flop with added additional inversion logic. The *hold* and *updn* signals are used for bit value inversion of the cell. Additionally, the AND gate formed by M14, M15, M12 and M13 is used for an asynchronous bitcell reset, which is achieved by controlling the gated inverters in the counter loop. Each bitcell contains 8T SRAM cells (not shown in Fig. 4.17) used for storing a shadow image of the counter's value. The shadow data transfer is controlled globally for the whole chip using global row select signals, which are sequenced in short time bursts of 2 ns. Although the SRAM cells use an 8T power-gated structure, toggling the cells globally introduces current glitches due to the large amount of parasitic capacitance associated with the gates of the SRAM power switches. Hence, the consecutive SRAM write row sequencing is to minimize high current power supply glitches.

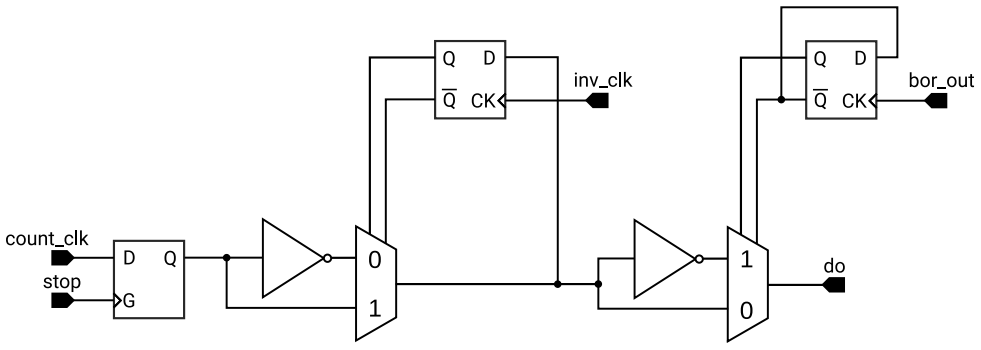


Figure 4.18: A principle schematic diagram of counter bitcell type 0

Figure 4.18 shows a principle diagram of the LSB cell of the MSB counter. It uses a gated latch structure and two consecutive inversion stages. The first inversion stage is controlled by the global inv_clk pulse which adds +1 increment to the counter after the two's complement inversion, which ensures a correct subtraction operation. The bor_out signal is provided per-column from the LSB counter borrow-out detector. This implements a propagation link between the LSB and MSB counters (discussed in the next subsection) which ensures the correctness of the subtraction operation.

LSB to MSB counter propagation link

Due to the Digital Correlated Double Sampling (DCDS) subtraction operation, it is important that both the MSB and LSB counters not only concatenate their individual 9- and 3-bit words, but the latter should also behave as a single 12-bit word during the subtraction operation. To

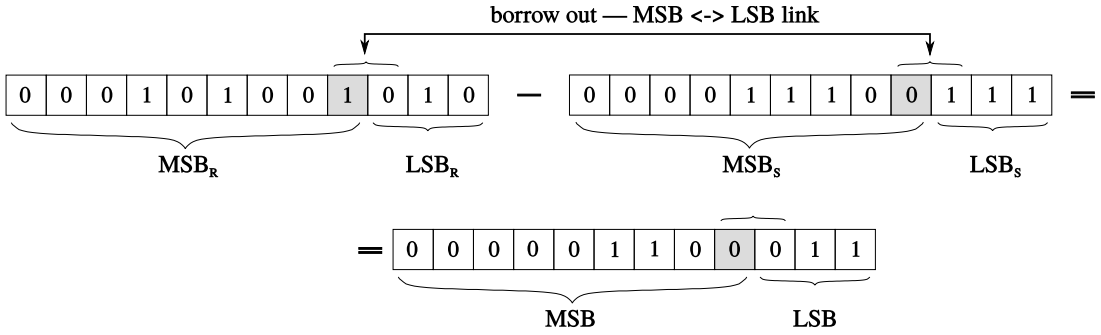


Figure 4.19: Borrow out operation and propagation link between the LSB and MSB counter

achieve this a borrow-out operation block is introduced in-between the counters, which has the task to decrement the MSB counter word in the case of an underflow of the LSB counter during the subtraction operation. Arithmetic details on the DCDS operation are shown below

$$\mathrm{DCDS} = (\mathrm{MSB_R}||\mathrm{LSB_R}) - (\mathrm{MSB_S}||\mathrm{LSB_S}). \tag{4.11}$$

A borrow-out operation shown as a binary word representation example is shown in Fig. 4.19. The LSB in the signal conversion is larger than the reset signal, thus the LSB of the MSB counter (shown in gray) is toggled in accordance with the subtraction conditions. In hardware this is implemented by an underflow detection block located in the LSB counter, which monitors all of its 3-bits and issues a flag using a one-shot RS-latch which toggles the LSB latch of the MSB counter, thereby adding an extra count.

4.3.5 Error Correction Module

The four radix estimation overlapping clock phases delay_clk[8:11] are sensed by a 4-bit latch block (indicated as COEFFSRAM in Fig. 4.7) positioned close to the delay line to reduce its sensitivity to errors induced by RC clock line loading. The content of the sensing latches is transferred to a shadow memory to keep its state during the conversion phase. The multiplication decoder module contains a binary counter which is reset during MSB conversion and is

incremented by 12 count clock cycles during the TDC latch scanning process. The correction coefficient value and the output of the binary counter pass through combinatorial logic issuing the *skip_sw_flag* signal which disables the TDC latch addressing of specific counts defined by the correction maps shown in Fig. 4.4.

Table 4.1 provides a summary of the skipped TDC latches depending on the captured correction coefficient.

C4,C3,C2,C1	Skip Switch	Global Skip
0001	sw2; sw5; sw8; sw11;	–
0011	sw2; sw6; sw10;	sw10;
0111	sw3; sw8;	sw10; sw9;
1111	sw5;	sw10; sw9; sw8;

Table 4.1: Error Correction Module Addressing

The scanning of the TDC latches is performed by a ring skip counter with a global disable input (driven by *skip_sw_flag*) as shown in Fig. 4.7. Clock phases overlapping with the main clock yield useful TDC radix information, but do not retain any valid signal information – hence, their global exclusion: sw10, sw9 and sw8 are gated by the correction coefficients c3, c2 and c1, which is equivalent to a static signal-independent subtraction.

4.3.6 Clock Generation and In-column Distribution

Each ADC group generates its internal TDC reference clock phases using a single-ended delay line shown in Fig. 4.20. The count clock is tapped from the main clock line and is fed to a buffering element which conditions the clock to drive the tunable delay elements.

Delay line

The tunable clock delay line contains 12 differential delay elements, as shown on the diagram in Fig. 4.20. Adding some degree of static tunability to the delay line allows for rigorous testing of the calibration scheme, although such tunability may not be necessary in a mass-production scenario. The tuning range of each cell falls between 166 – 600 ps and is controlled in 64 steps which allows changes in the ramp time from 1 µs (F_{clk} = 250 MHz) to 2 µs (F_{clk} = 125 MHz).

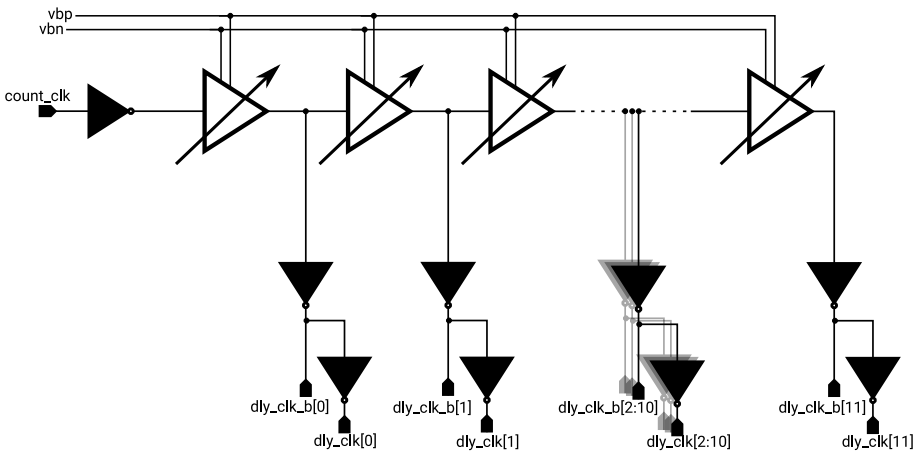


Figure 4.20: Delay line

Figure 4.21a shows a schematic of a current-starved unit delay element. Although a fully differential current-starved structure is superior to power supply noise immunity and has low jitter, the use of a single-ended delay structure with consecutive differential conversion was chosen due to area constraints in the mid-ADC-group gap area. As mentioned in Section 4.2.3 the TDC clock duty cycle has a high impact on differential nonlinearity. Thus, the current single-ended circuits have been designed such that the positive and negative slew currents are well-matched to minimize clock duty cycle degradation (beyond the accuracy requirements) of the produced delayed clock. It is important to note that due to the series connectivity of the delay line, each consecutive delay cell adds up to the total duty cycle degradation. Therefore, duty cycle should be measured for the last in the chain delay element, while the difference between the first (DC_{DLY_1}) and last ($DC_{DLY_{12}}$) clock phase should be below the accuracy limit, or

$$|(DC_{DLY_1} - DC_{DLY_{12}})| < \epsilon_{duty}. \tag{4.12}$$

Figure 4.22b provides an idealistic plot of the duty cycle degradation in each delay line tap for six delay bias settings. The mismatch response between the P and N-FET current-starve devices impacting duty cycle can be seen from the tap spread in the most extreme delay tuning range.

In the use case for the TDC clock generator, nonlinearities in the tuning range can be tolerated due to the static delay line operation. The tuning range of the current-starved delay elements as a function of their global bias control current is shown in Fig. 4.22a.

The biasing of the delay lines in each group is individual and controlled using current-mode steering. Routing of very long (on-chip) bias lines requires a current-mode control approach to minimize the potential capacitively coupled noise on the bias line which can degrade the jitter performance of the delay elements. The simple current-mode biasing methodology is also shown in Fig. 4.20. The total delay line drift with PVT corners is within 3× the nominal unit delay of 200 ps, which spans within the recoverable dynamic gain range by the TDC gain correction circuitry, Fig. 4.22c shows the delay element drift and duty cycle degradation versus process corners.

In the case of wider column pitch where a larger gap space can be accommodated in the mid-ADC group area, the use of fully differential delay elements provides more robust noise

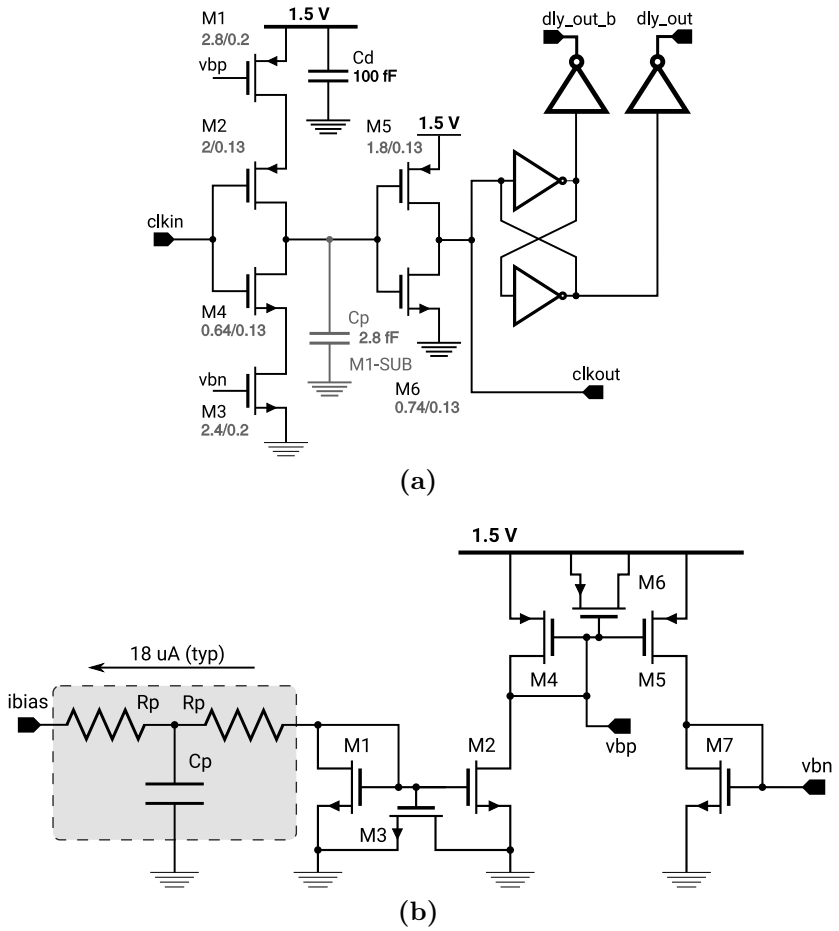


Figure 4.21: Delay line components: a) delay element; b) current-mode group bias

immunity, delay drift and duty cycle, which has been discussed in [77] and [78]. Alternatively, CMOS Thyristor-based delay elements as also reported in [79] and [80] can offer better immunity to PVT corner delay drift compared to the currently proposed single-ended solution. This is due to the symmetric charge-discharge currents in the CMOS thyristor-based structure. The currents can be well-matched due to their generation by the same type of FET device (in the example case N-type).

4.3.7 Chip Data Readout and Clocking

Figure 4.23 shows a clock distribution diagram of the TDC reference phases which are buffered differentially and routed per ADC group. This improves edge steepness and minimizes metastability errors. The count clock is received on-chip through an AC-coupled LVDS receiver (shown in Fig. 4.24a) which eliminates signal common-mode DC level sensitivity of the receiver and the potential drift of the eye opening. This ensures that the duty cycle of the received clock is kept at 50 % with minimal error which is critical for the correct operation of the ADC.

As the testchip consists of 1024 columns, no intermittent clock re-buffering was needed, although high-column implementations may require re-buffers. In order to improve the dis-

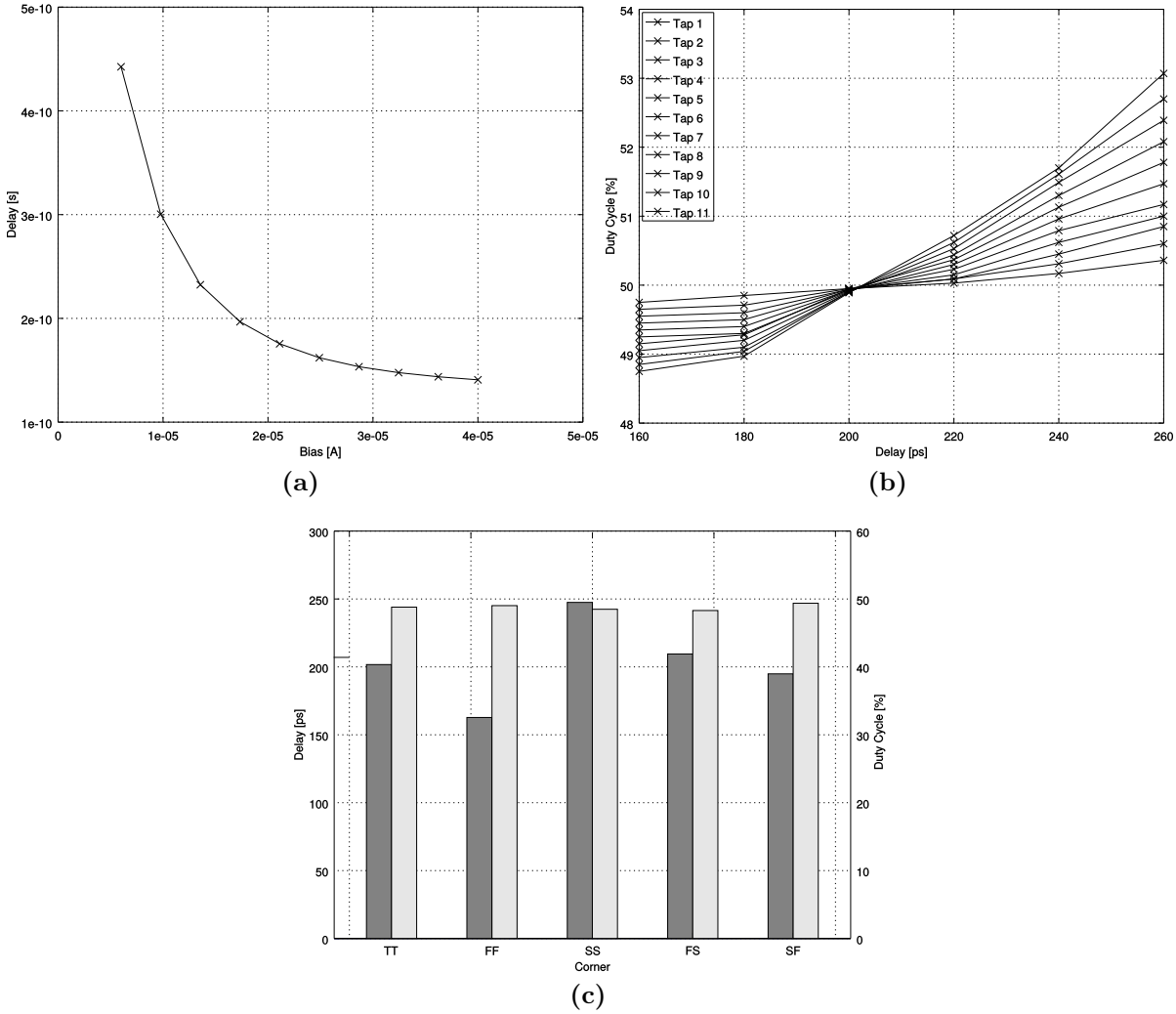


Figure 4.22: Delay versus: a) bias; b) duty cycle for individual line taps; c) corners and duty cycle

tributed clock, guard clocks adjacent to the main clock have been routed using minimum distance to improve the coupling capacitance C_g as shown in Fig. 4.23. The guard clocks are driven globally using individual CMOS buffers, the latter reduces the effective capacitance seen by the main clock and improves clock rise and fall times by 20 %.

An individual clock source has been used for the memory serialization and readout. Each ADC contains two 6:1 DDR serialization modules, which form individual 6-bit MSB and LSB words. After SRAM readout and serialization, the data is fed to sub-LVDS transmitters whose architecture is shown in Fig. 4.24b. To overcome issues with keeping the LVDS drive transistors in saturation with power supply of 1.5 V, and to maintain the standard sub-LVDS common-mode voltage, the architecture uses data-dependent dynamically switched current sources formed by M9 and M10. Depending on the data d and db respectively, the current source PFET transistors as well as the output switches M7 and M8 are controlled such that the current path charges the external termination (receiver) resistor in the corresponding direction. The driver uses

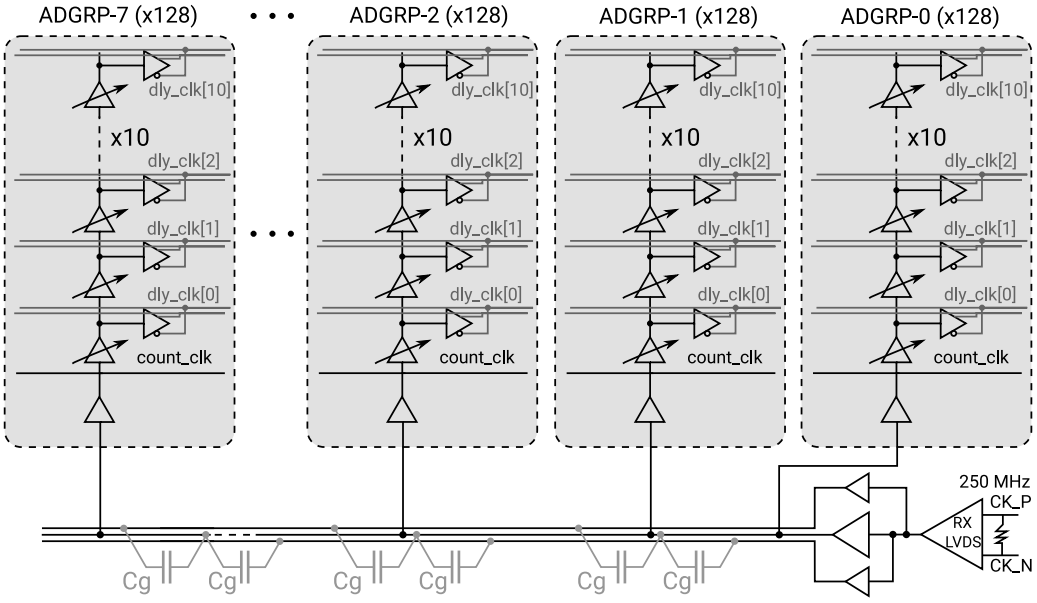


Figure 4.23: TDC reference clock distribution tree, ([I], reprinted by permission of IEEE)

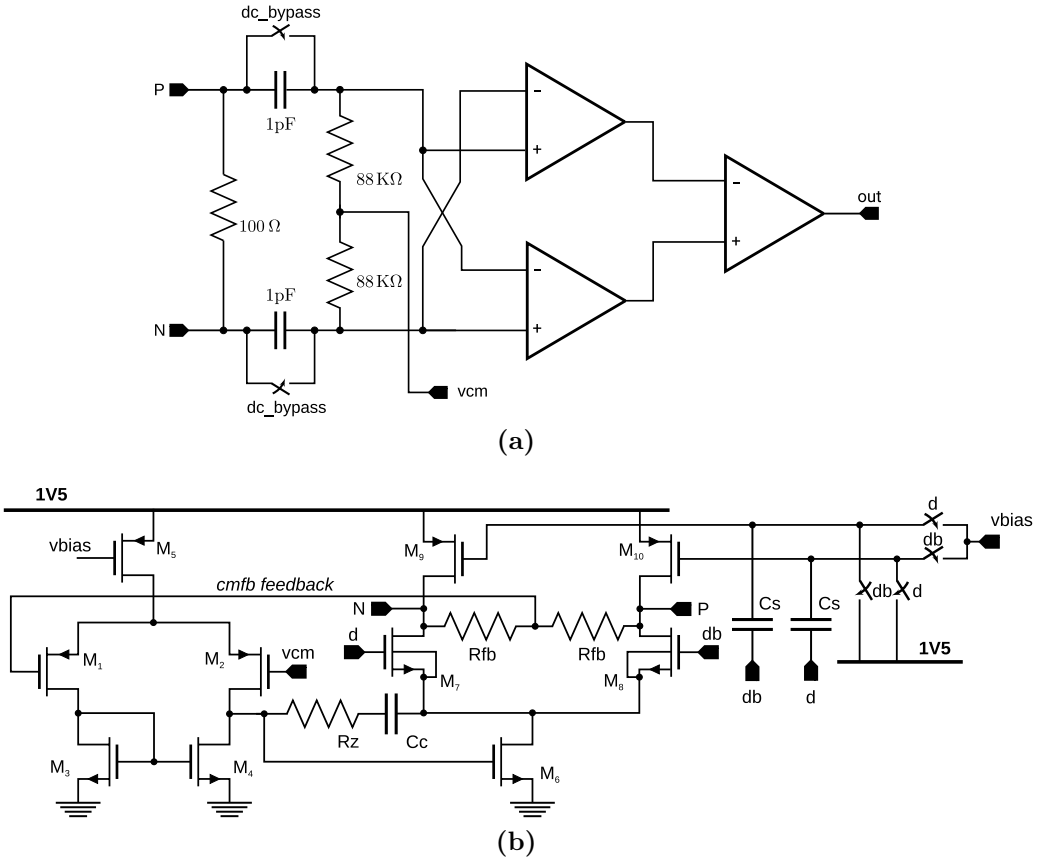


Figure 4.24: Principal LVDS architectures: a) receiver; b) transmitter

voltage-domain common-mode feedback which is maintained by a PFET differential pair error amplifier. The feedback loop is non-dominant (output) pole compensated by the miller capacitor Cc and zero resistor Rz.

The use of the presented LVDS Receiver and Transmitter structures in Fig. 4.24 provides a good enough clock delivery and data readout solution for the purpose of the ADC testchip. While there could be more energy efficient solutions, the presented architectures offered simplicity and robustness. All other sequencer signals required for the operation of the ADC were generated off-chip and are provided using individual external bonding pads in full-swing 1.5 V CMOS logic.

4.3.8 Power Supply and Signal Distribution

A typical optical Front-Side Illumination (FSI) CMOS process offers a limited number of metal routing layers due to the exhibited optical degradation with every additional layer and its associated insulation. The current implementation uses three metal and one poly connection layers. In order to provide the columns with a rigid power grid the column power distribution scheme shown in Fig. 4.25a was used. Each column contains a vertical power routing channel, which is alternated between analog (AVDD), digital (DVDD) power and ground supply. The power ring shown in Fig 4.25b is split in active high current (dirty) and quiet low pixel-drawn quiescent current (clean) domains. All ADC modules are enclosed in deep N-well structures to isolate all active high-charge-release devices from the substrate. The substrate is primarily connected to the pixel anode and the bottom plate of the ADC sampling MIM capacitors.

The data output is realized at the bottom of each ADC group, with the pinout structure as shown in Fig. 4.25. Each LVDS data pair is separated by analog and digital column supply. A separate LVDS transmitter power ring has been routed at the bottom ring, providing symmetrical power from the left and right side of the power pinout. The bonding pads have a custom integrated ESD protection diodes and a power supply sequence initiation clamps ensuring that no latch-up occurs if any combination of power domains is applied to the device.

The global ADC signalling has relatively low settling time constraints compared to the count clock and is routed horizontally in top metal layer. The signalling line widths have been kept close to minimum width, while bias and sampling switch control lines have been shielded wherever necessary.

4.3.9 Pixel Array Grid

The choice of pixel structure was driven by the input voltage range requirement of the ADC and was detailed in Section 4.3.2. The physical array configuration was driven by the limited availability of silicon real estate with the MLM tapeout run. Thus, a 128-row linescan array was chosen as a compromise whose structure is shown in Fig. 4.26.

The pixel array provides strong vertical quiet ground AGND_NC required to achieve sufficient settling time of the sampling operation. The array provides vertical power needed for the PFET column current sources. The pixel structure has been stacked such that the latter alternate the photodiode with the readout transistors in multiples of the pixel pitch 5.6µm. This ensures ease of line synchronization and maximizes the linescan fill-factor. If the shutter is assumed

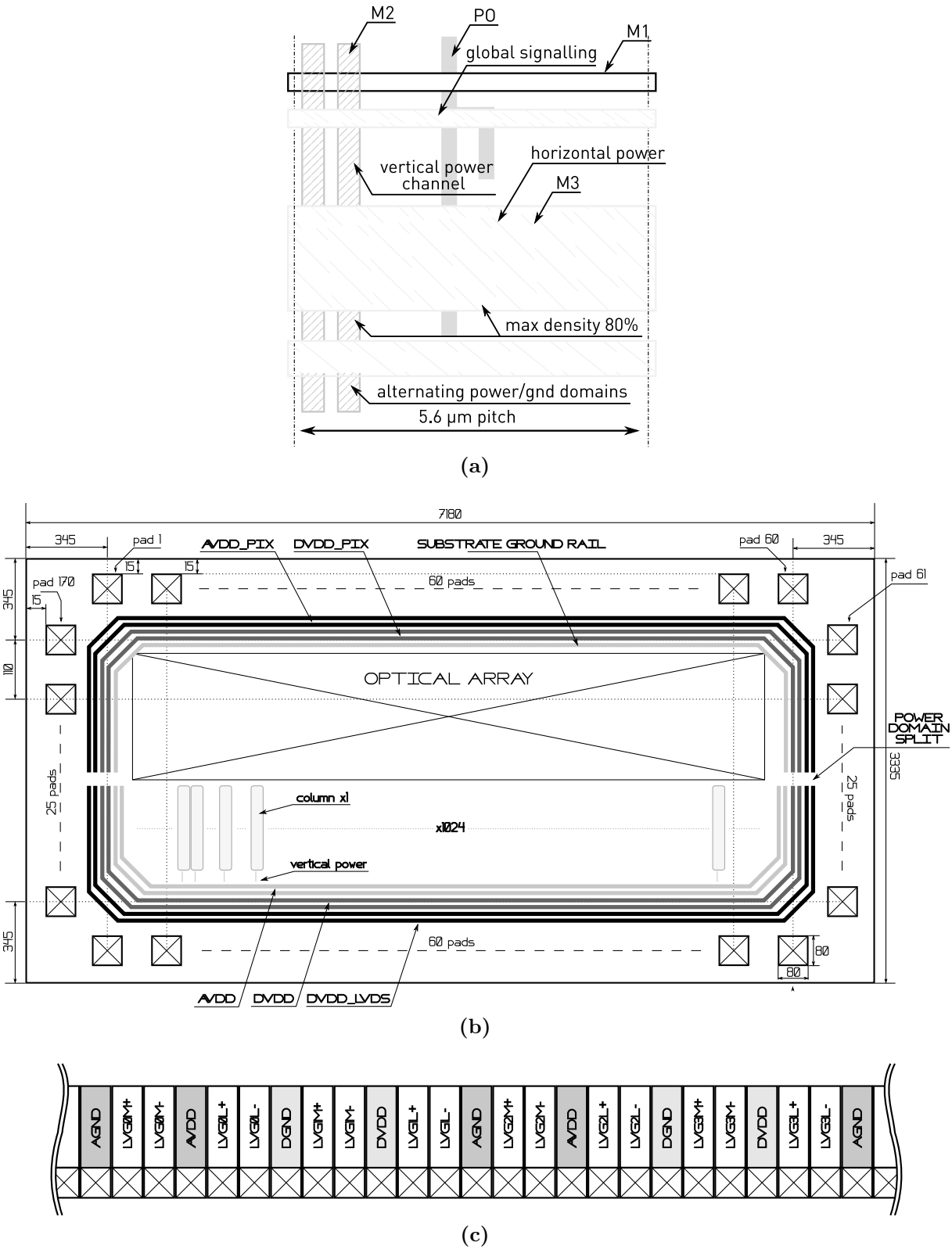


Figure 4.25: Power supply distribution: a) metal arrangement in a single x1 column; b) power ring and column grid distribution; c) chip LVDS data output

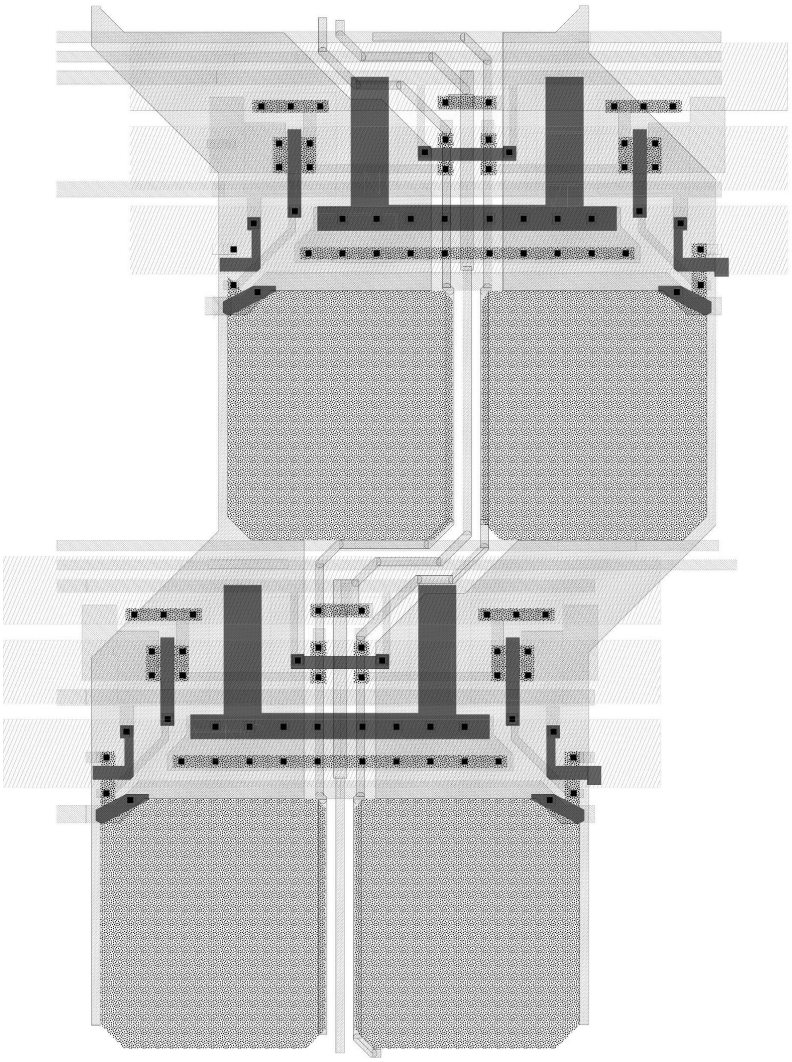


Figure 4.26: Overview of the used linescan pixel, shown is a x4 cluster

to have 100 % accuracy, the equivalent fill-factor and modulation transfer function (limited by pixel aperture) is maximized to >98 %. Microlenses have also been used for further reduction of optical crosstalk, and increase of QE.

4.3.10 Chip Top Level

The total die size of the testchip is 7.75 mm × 4 mm while ~30 % of this area is occupied by the pad frame, power rings and an experimental Silicon photomultiplier (SiPM) module which is seen on the top-left side of the layout masks shown in Fig. 4.27.

All reference blocks are placed on the side of the ADC array (seen on the right hand side), along with the array row control. The bottom side of the ADCs contains the serial data LVDS taps and power supply pads. Figure 4.28 shows a block-diagram of the top level.

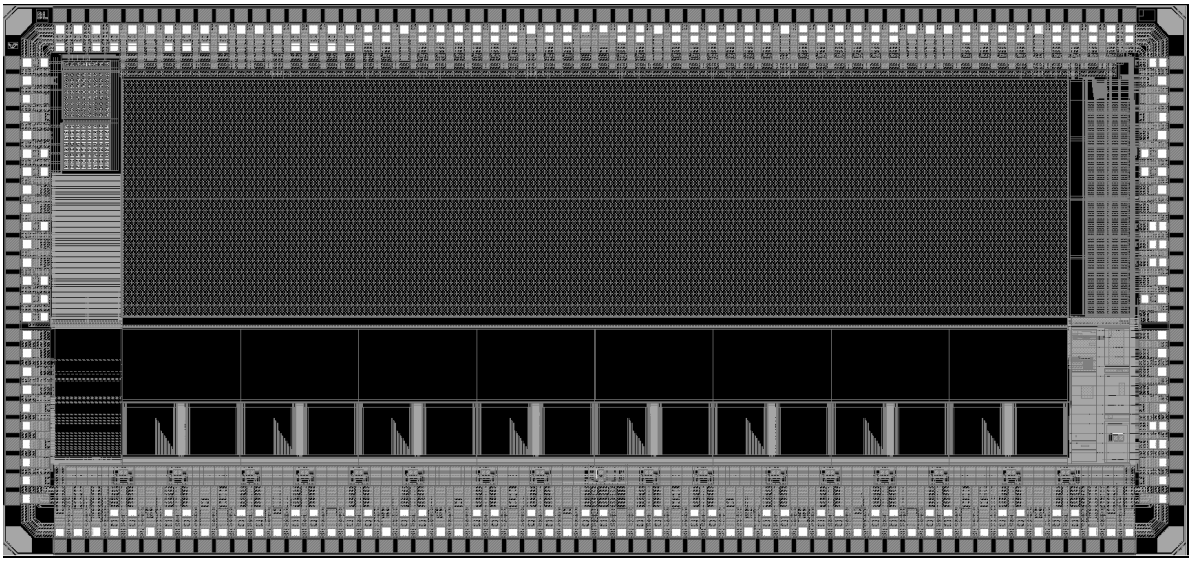


Figure 4.27: Chip top-level overview (die size 7.75 mm x 4 mm)

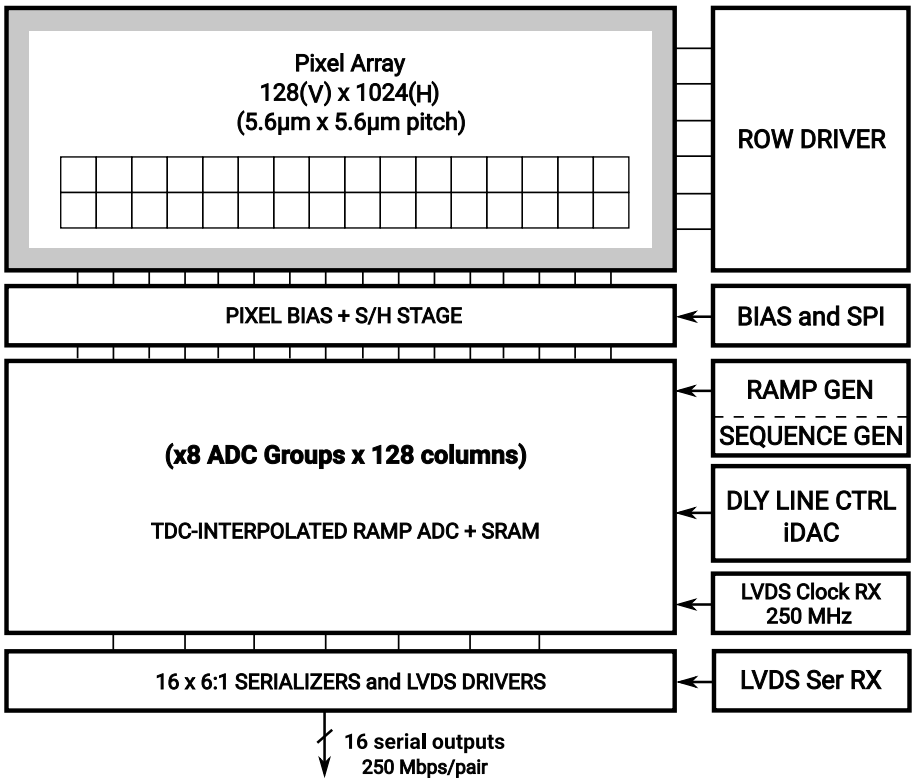


Figure 4.28: Sensor block diagram with ADC group configuration

4.3.11 Sensor Readout System

A simplified functional block diagram of the digital readout system implemented on an FPGA is shown in Fig. 4.29.

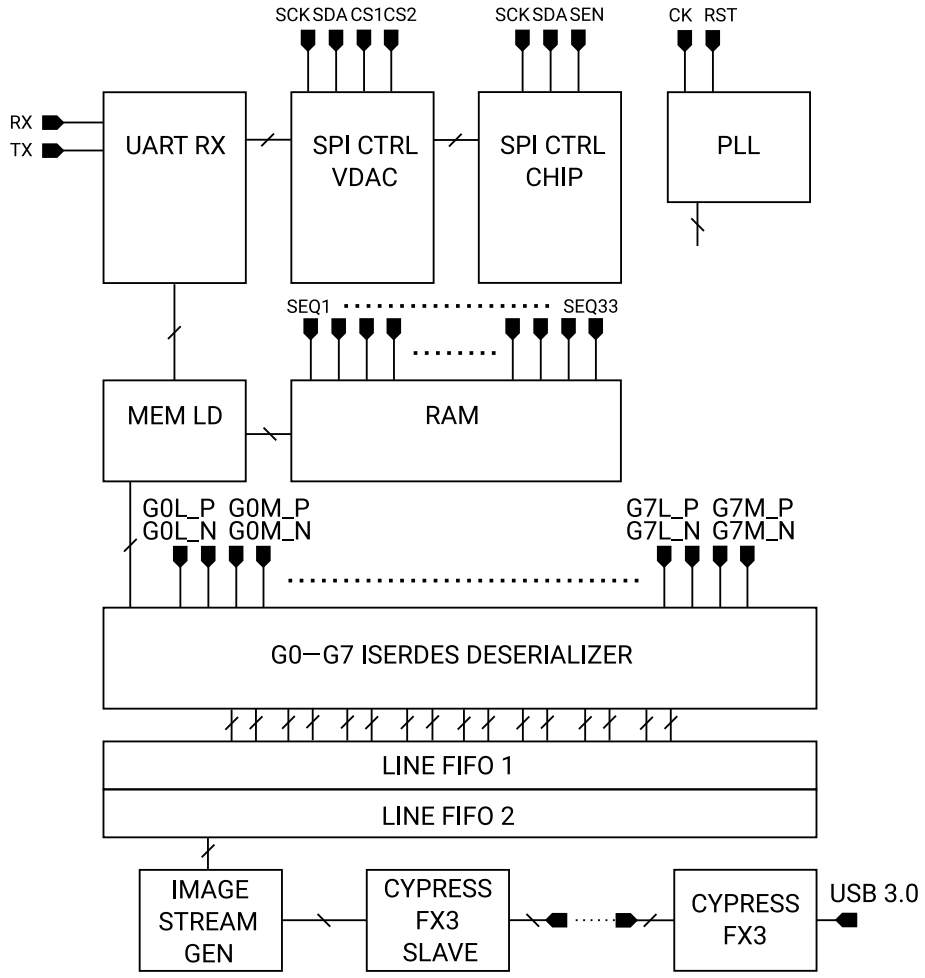


Figure 4.29: High-level functional block diagram of FPGA design

The input data stream (G0L/M - G7L/M) is fed via 16 LVDS pairs to hardware deserialization modules (ISERDES) on a Xilinx Spartan 6 LX150 FPGA. The deserializer uses internal clock re-synchronization PLLs with dynamic eye opening alignment for each ISERDES module. It also uses a hardware bitslip module monitoring and bit-aligning the deserialized word in accordance with the training pattern provided by the chip when not in data transmission mode. The deserialized parallel data is then fed to a dual line FIFO buffer memory. The FIFO lines are swapped after conversion of every row, which allows for a fully pipelined readout (when FIFO1 is read, FIFO2 is being written). The FIFO data is pre-processed by the IMAGE STREAM module, which combines the full frame data, which is being fed to a slave module controlling an external Cypress FX3 USB 3.0 controller chip. The latter contains a high-speed microcontroller, USB 3.0 PHY and a parallel 32-bit general purpose I/O bus. The bus is driven by the FPGA and the FX3 slave controller.

The chip clocks are generated by PLLs and are driven using LVDS PHY, while the sequencer signals are generated by the sequential scanning of a blockram memory module. The content of the RAM is generated using a custom pseudoassembly-to-binary conversion tool. The RAM is preloaded from a PC through UART, hence the presence of a bit-banged UART receiver in

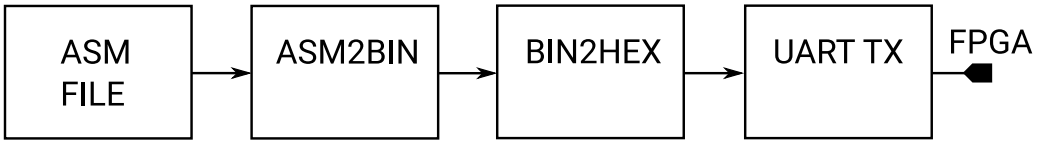


Figure 4.30: Assembly sequencer to block RAM download flow

the FPGA shown in Fig. 4.30. UART is also used for transferring of the SPI chip register settings. Figure 4.31 shows an overview of the developed tools for SPI register control. A few SPI voltage DAC modules are also present, which control the input reference test voltages for reset and signal A/D conversion.

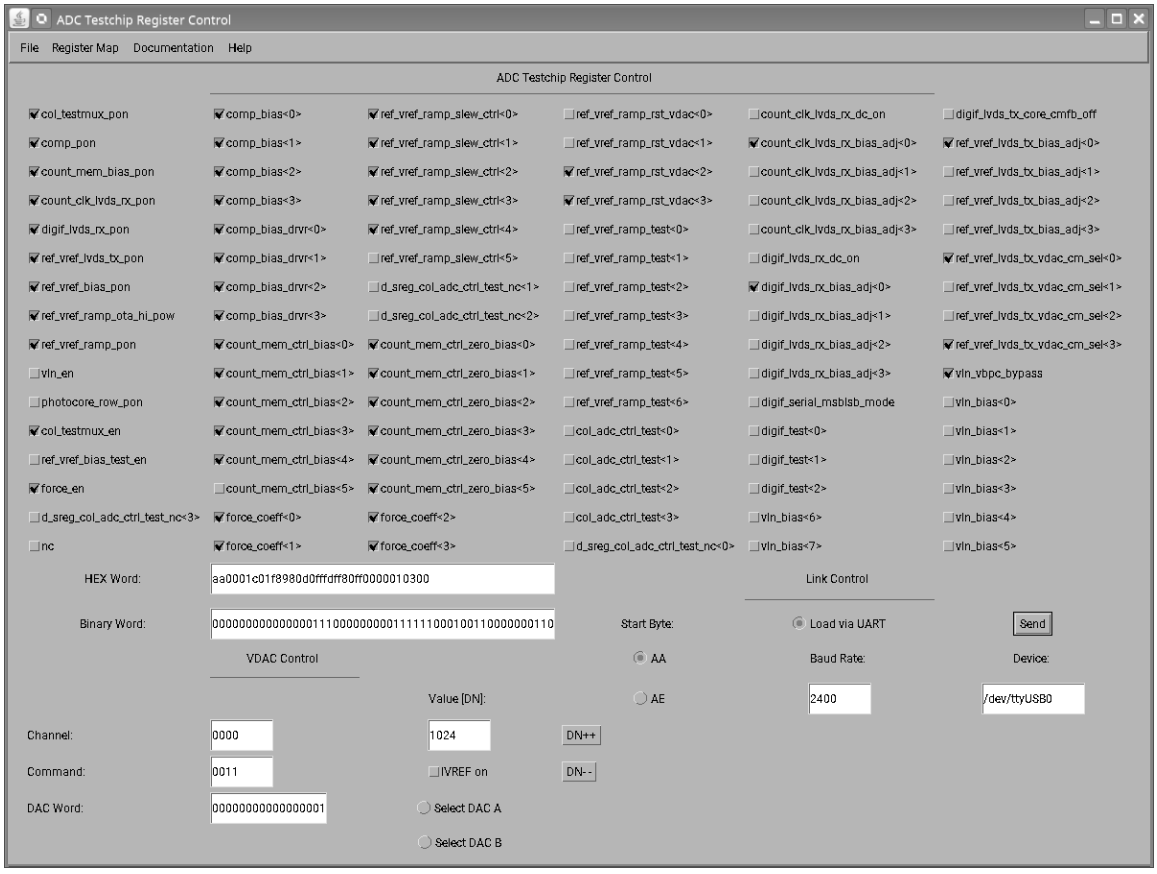
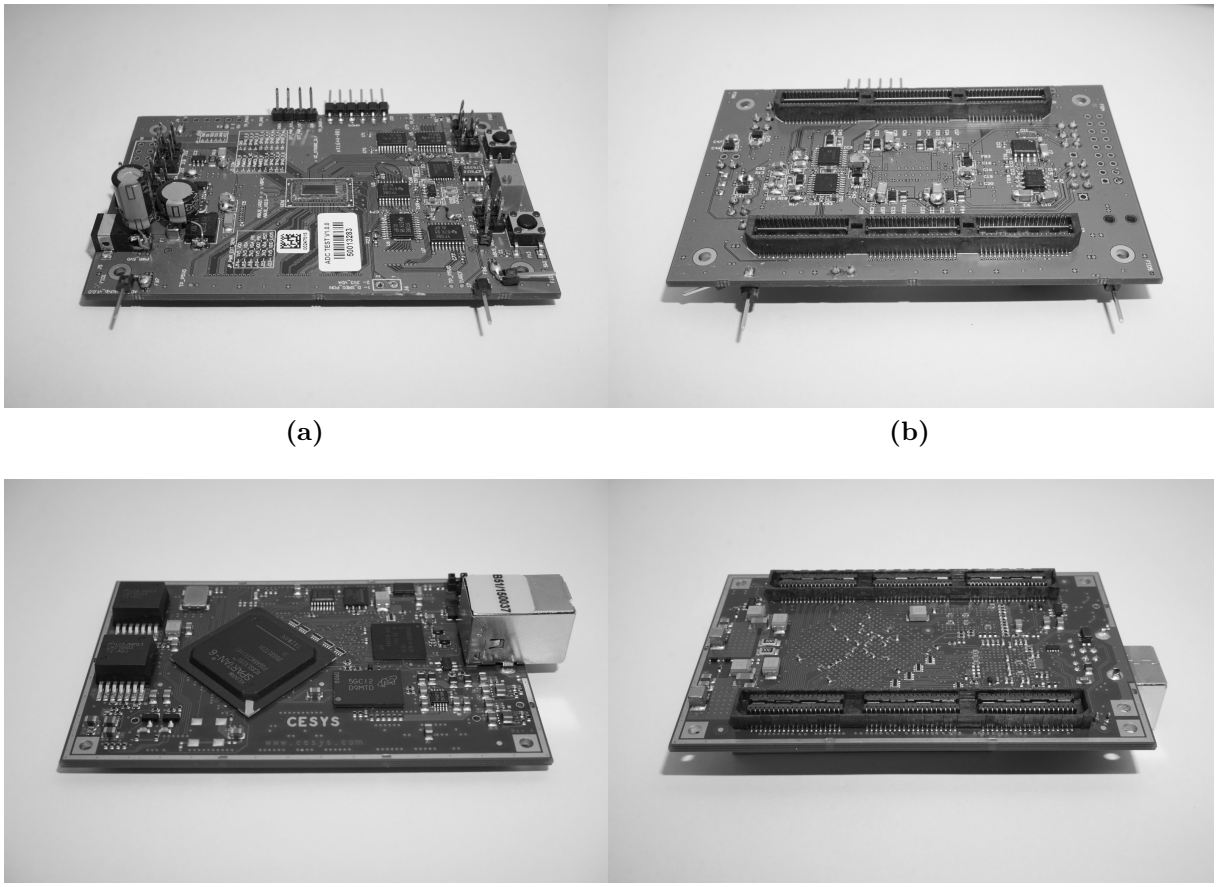


Figure 4.31: Outlook of the SPI chip register settings loader tool

The readout system uses a generic FPGA board and is shown in Fig. 4.32. The chip board contains power supply LDOs, bus level shift transceivers, global bias trimming, VDACs, and an ADC measuring the power consumption of the chip through a shunt resistor.



(a) **(b)**

(c) **(d)**

Figure 4.32: Photographs: a) test board top side; b) test board bottom side; c) FPGA board top side; d) FPGA board bottom side

4.4 ADC Characterization

A 1024 column x 128 line testchip was manufactured in 0.11/0.13 µm 1P3M aluminium CIS process (IL11SJ) by Dongbu Semiconductor. Figure 4.33 shows a die microphotograph of the implemented testchip, and provides a top-level block overview of the device. Each ADC group possesses dual 6:1 serialization channels and 250 Mbps Sub-LVDS drivers.

Table 4.2 presents summarized ADC characterization data measured at 1 µs ramp time mode. The count clock runs at 250 MHz, which imposes a typical Flash TDC delay unit time of 200 ps, being $\approx 6\times$ the intrinsic gate propagation delay in the used process.

4.4.1 Linearity and Calibration

Figure 4.34 shows the DNL and INL of the mid-array column (512) with calibration turned on and off, although the linearity performance is well-matched within all columns. It should be noted that the plotted code includes offset to start from code 0, while the total tested ADC code

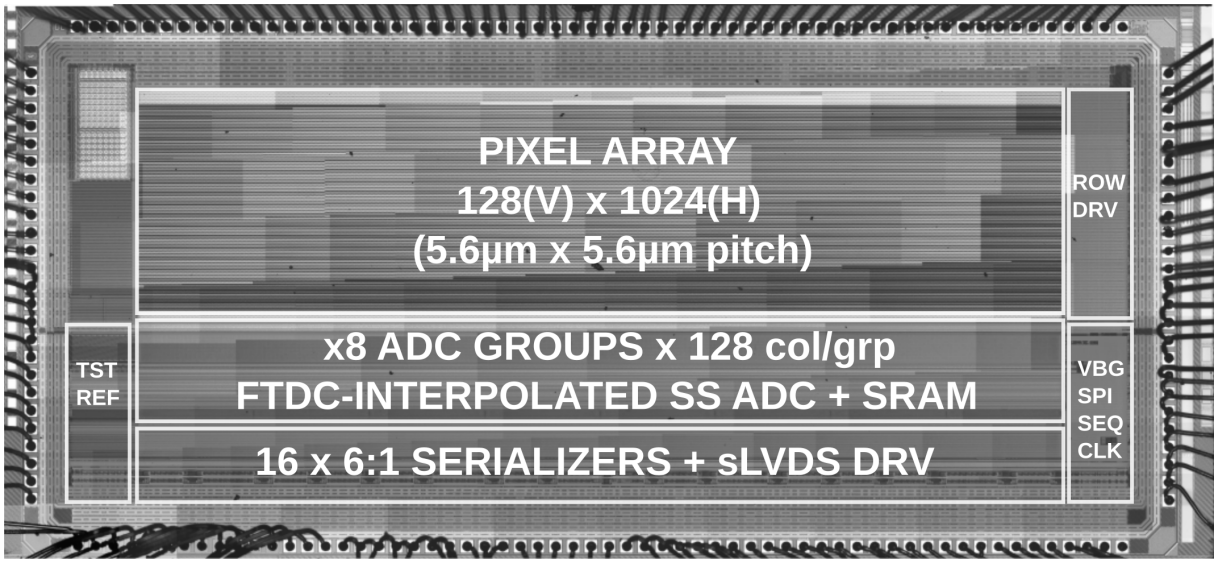


Figure 4.33: Chip microphotograph (die size 7.75 mm x 4 mm)

range is 3500. This is due to an error in sequencer timing and the fact that about 120 ns of the 1 microsecond conversion time are allocated (and lost) in comparator propagation delay. Figure 4.35a provides code density histograms of a single column and ADC group, 4.35b shows the matching of the DNL response of one ADC group, while 4.35c and 4.35d present a step plot of the discrete-time domain ADC response before and after radix expansion.

The observed DNL glitches in Fig. 4.34 after calibration occur only at the interpolation point between the MSB and LSB counter and can be noticed at every 16th code. These are due to an unfortunate but correctable design-influenced propagation delay difference in the TDC latch elements (L0– L10) and the DDR latch zero (LM0) of the MSB counter. The LM0 – L0-10 latches were measured to have a propagation delay time difference of ≈140 ps which is the main source of the observed DNL glitching. Partial degradation of the count clock duty cycle by the LVDS clock receiver also contributes to the observed non-linearity peak at the interpolation point codes. Such DNL errors can be easily eliminated with the use of an accurate on-chip PLL and precise latch optimization. A large portion of the random DNL floor below 0.5 LSB is caused by the numerical noise introduced through the fixed point multiplication and the truncation of numerical residue, which is architecture-inherited and matches well with our predicted model. The absolute difference between the theoretical non-linearity versus the measurement result, excluding the DNL glitch errors is 0.3 LSB which is due to latch V_{th} variations.

The seen INL has been hypothesized to be induced by a non-linearity in the ramp, originating from the ramp generator integration source. The implemented continuous-time distributed integrator does not employ current calibration, which is essential if INL is to be kept close to ideal [45], [46]. Additionally, the expected nonlinear drain diffusion capacitance of the comparator differential pair might have been underestimated. Therefore, the linearization role of the column integration MIM capacitor appears to have an insufficient capacity. Nevertheless, even with such pessimistic measurement scenario the INL levels are of low enough magnitude such that the latter have low impact on image quality for visual applications.

Design Parameter	Value
Process	0.13 µm 1P3M FSI CIS
Array Size	1024 (H) × 128 (V) RGBW
Pixel Pitch / Height	5.6 µm / 820 µm
Resolution	12-bit
Row Time (incl. DCDS)	4.4 µs
Ramp Time	1 µs
Counting Scheme	Flash TDC-Interpolated
ADC Count Clock Frequency	250 MHz
INL	+5.8/-8.2 LSB
DNL	+1.1/-0.4 LSB
Input Range (µV/LSB)	1.5 – 2.9 V (341 µV/LSB)
Noise Stdev. at 1x gain (LSB)	477 µV (1.48 LSB)
Data Output	16 LVDS ports at 250 Mbps
Power/Column (incl. refernces)	177 µW
Temperature Range	-20 – 70 °C
Power Supply	1.5 V (dig), 3.3 V (ana)

Table 4.2: Summary of measured ADC performance

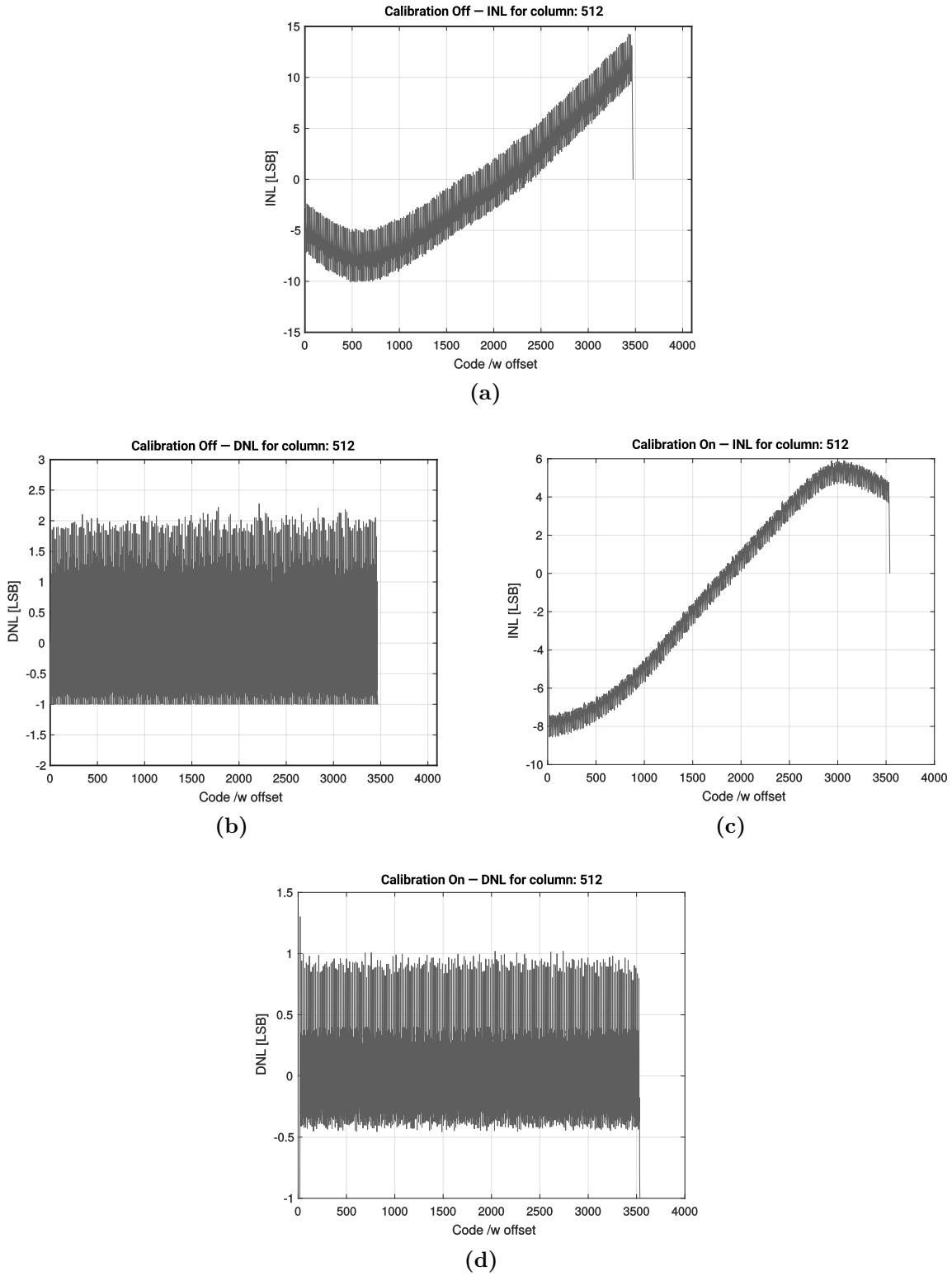


Figure 4.34: Measured DNL and INL: a) INL calibration off, c) INL calibration on; b) DNL calibration off, d) DNL calibration on, ([I], reprinted by permission of IEEE)

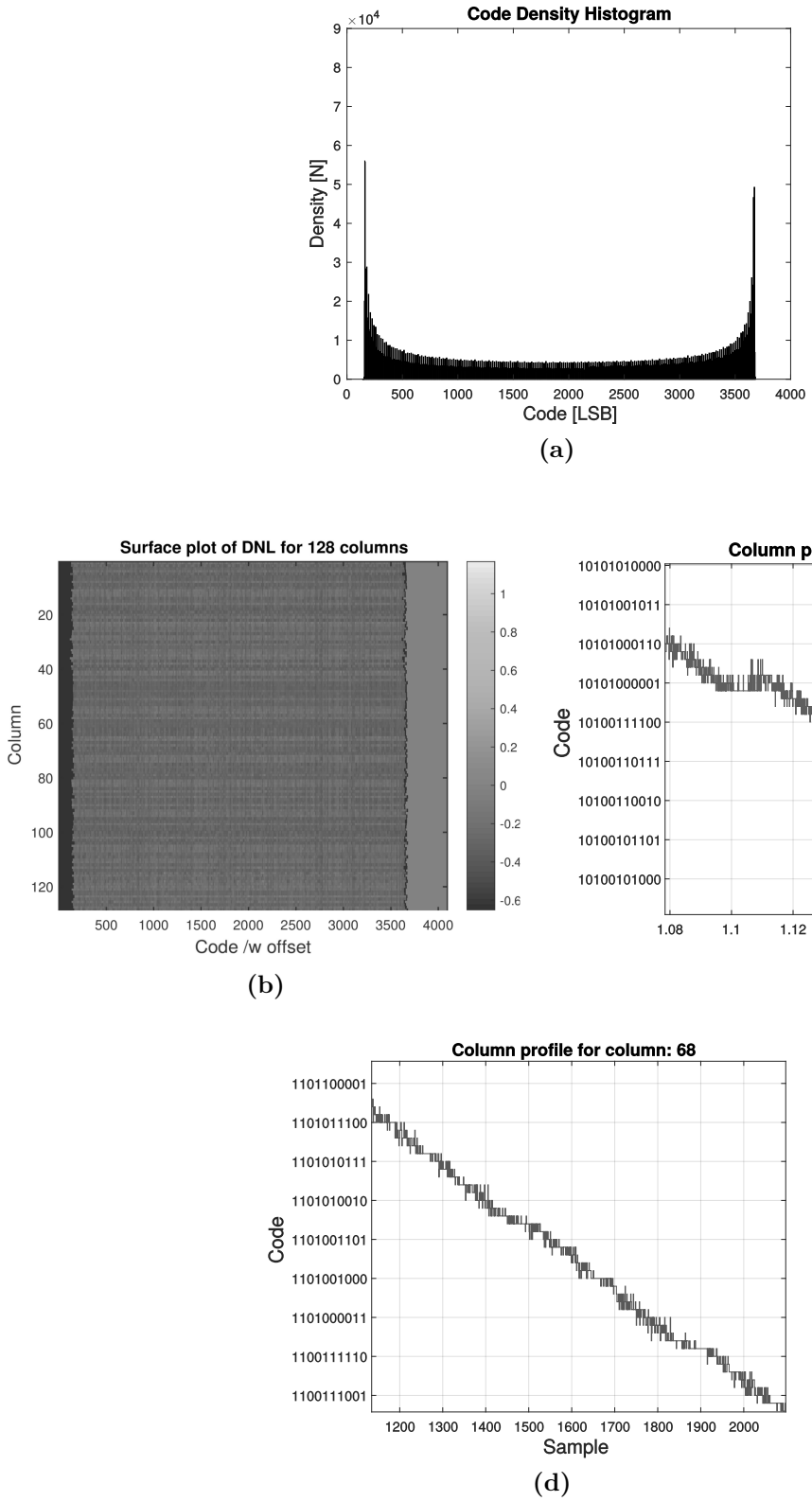


Figure 4.35: Measured code density and DNL: a) code histogram of one column; b) DNL of one ADC group of 128 columns; Measured discrete-time ramp response: c) calibration off; d) calibration on, ([I], reprinted by permission of IEEE)

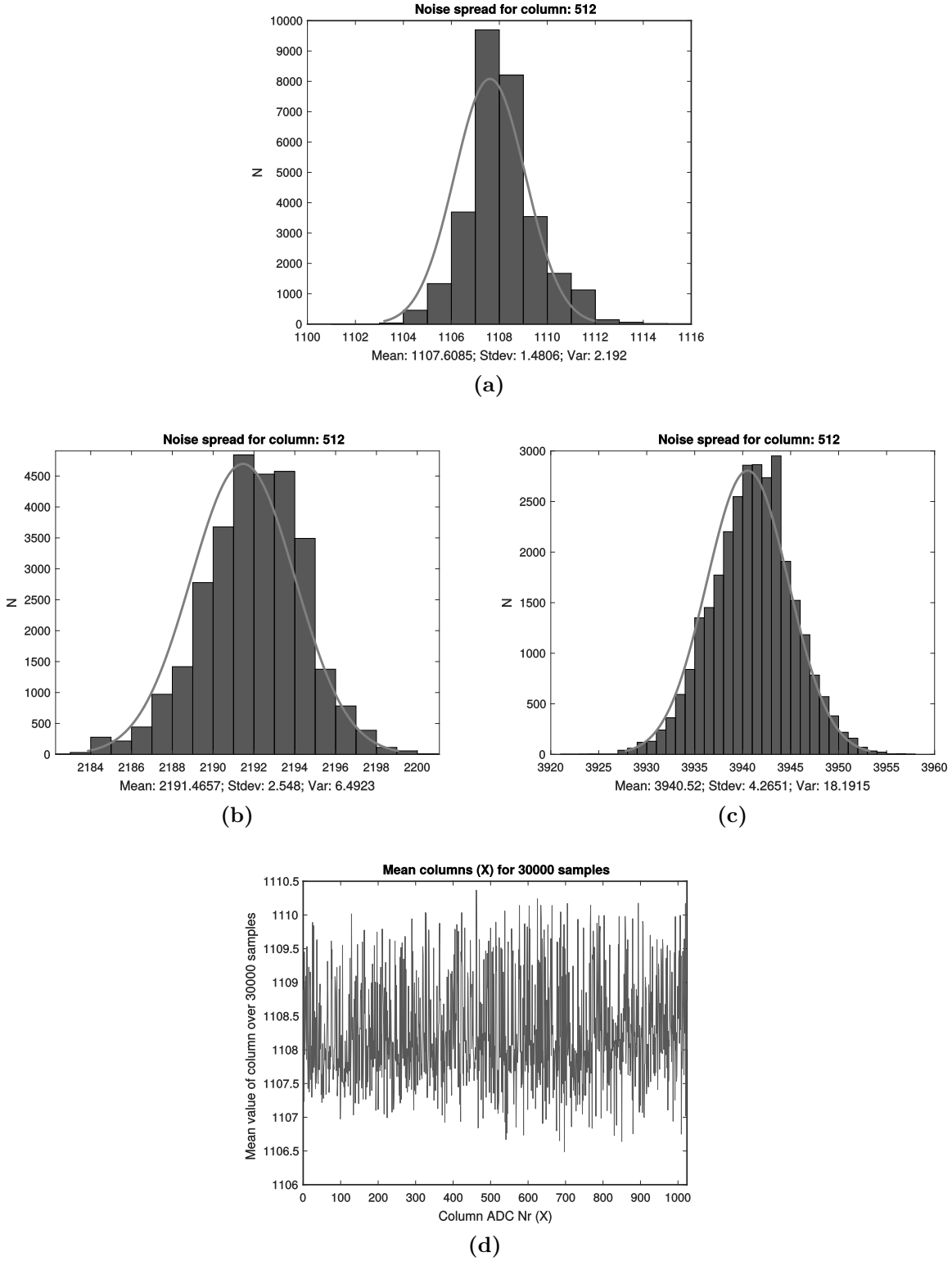


Figure 4.36: Measured output noise: a – c) for a full DCDS conversion at 1×, 2× and 4× gain; d) Mean value of columns (X) in DCDS mode over 30 K samples, ([I], reprinted by permission of IEEE)

4.4.2 Noise and Column Matching

All on-chip circuit blocks are isolated from the substrate through a deep N-well with separate quiet signal sampling ground planes which reduce noise coupling. The measured column noise characteristics using an ideal DAC voltage shared between all columns is shown in Fig. 4.40. Subfigures a-c present the total output ADC noise of a full DCDS conversion at 1×, 2× and 4× gain, which was achieved through ramp slope modulation. The input range of the ADC at 1× gain spans between 1.5 – 2.9 V (1.4 V abs) with an LSB of 341 µV. This leads to an input-referred noise with a standard deviation of 477 µV. Figure 4.36d shows the mean output of all columns averaged over 30 K samples, provided with a shared input test DC voltage level of ≃1000 DN to all 1024 columns. The contribution of comparator noise was measured by statistical cross-correlation of the output noise of adjacent columns and was estimated to be ≃300 µV referred to the input. Column fixed pattern noise normalized over full scale (4096) as a function of the converted output signal is provided in Fig. 4.40a. It is identified to be ≃ 0.15% when run at DCDS time difference of 2 µs.

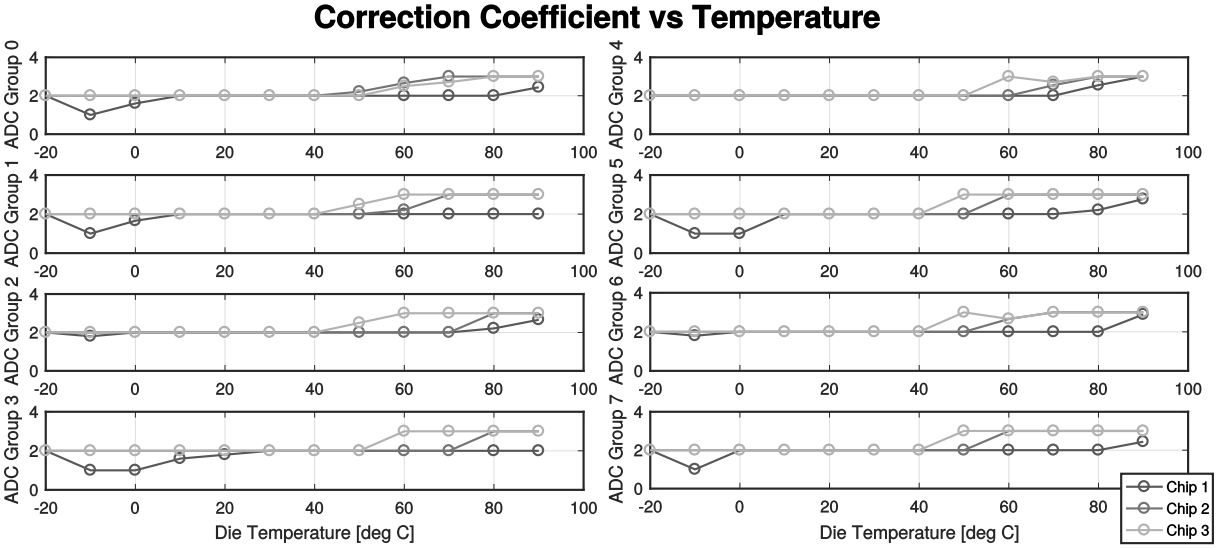


Figure 4.37: Captured correction coefficient versus temperature for each ADC group (GRP0 – 7), measured on 3 individual chip die samples, ([I], reprinted by permission of IEEE)

Figure 4.37 shows the captured correction coefficient versus temperature corners for each ADC group (GRP0 – 7) and provides data for three individual chip die samples. The calibration coefficient capture is within the designed recoverable process and temperature range and for the measured samples spans between “0001” (1) and “0111” (3). Voltage variations on the digital supply within 10 % prove to modulate the captured coefficient insignificantly. The group-to-group correction coefficient matching is seen to span between ±1 digital code and does not induce a noticeable group-to-group ADC offset. Tests under uniform (DAC-provided) and random (pixel-provided) input voltage confirm that latch load-induced calibration coefficient drift is within less than $1/2\tau$, owing to the strong digital power supply network and local decoupling.

4.4.3 Comparator Noise Correlation Analysis

In order to evaluate the noise performance of the column comparator an adjacent noise cross-correlation analysis technique can be applied. Figure 4.38 shows a principle noise path diagram which is used as a reference further in text.

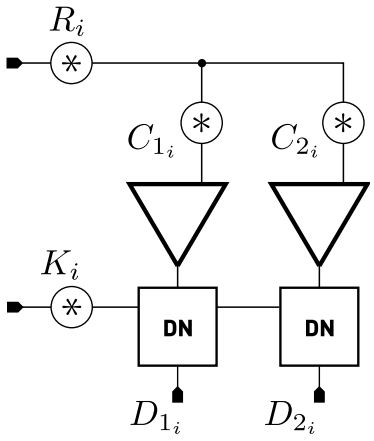


Figure 4.38: Noise path assumption diagram

R_i represents the noise sample contributed by the shared ramp reference, which is common for both columns. The same applies to K_i which represents the noise induced by random clock jitter and counter fluctuations. The noise samples from two adjacent columns C_{1_i} and C_{2_i} represent the thermal noise induced by the comparator. Therefore, for this analysis it has been assumed that the correlation ρ for R_i and K_i for both column data D_{1_i} and D_{2_i} equals 1, and that the thermal noise from C_{1_i} and C_{2_i} between adjacent comparators has a correlation coefficient of $\rho = 0$, or

$$\overbrace{R_i}^{\rho=1} + \overbrace{C_{1_i}}^{\rho=0} + \overbrace{K_i}^{\rho=1} = D_{1_I} \tag{4.13}$$

$$\underbrace{R_i} + \underbrace{C_{2_i}} + \underbrace{K_i} = D_{2_I}. \tag{4.14}$$

By knowing the output samples for a converted static DC signal of adjacent columns we can compute the comparator noise statistically using subtraction of the random variables (statistically equivalent also to addition). To calculate the noise standard deviation of the comparator we must first compute the total mean μ of the adjacent column samples

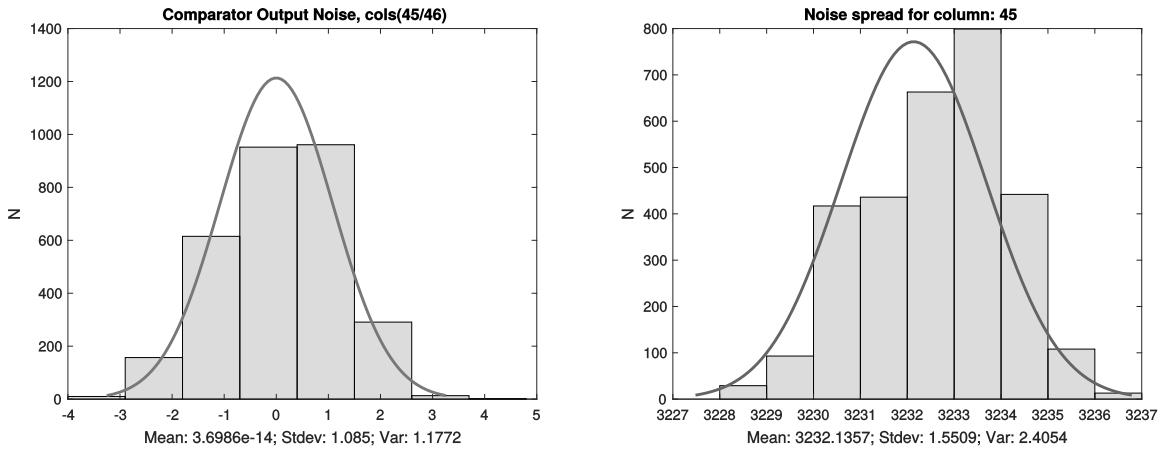
$$\mu = \frac{\dfrac{\sum_{i=1}^{N} D_{1_i}}{N} + \dfrac{\sum_{i=1}^{N} D_{2_i}}{N}}{2} \tag{4.15}$$

where D_{1_i} and D_{2_i} are the data samples at the output of the ADC. Assuming full correlation $\rho_R = \rho_K = 1$ and zero correlation for $\rho_{C_1} = \rho_{C_2} = 0$ we can write the compara-

tor standard deviation as

$$\sigma_{comp} = \frac{\sqrt{\sum_{i=1}^{N} \Big((D_{1_i} - D_{2_i}) - \mu \Big)^2}}{\frac{N-1}{2}}. \tag{4.16}$$

One may note that it has also been assumed that the thermal noise contribution of both comparators is identical, thus based on the summation rules of probabilities the noise magnitude should be halved in order to obtain the thermal noise contribution of a single comparator, hence the used denominator.



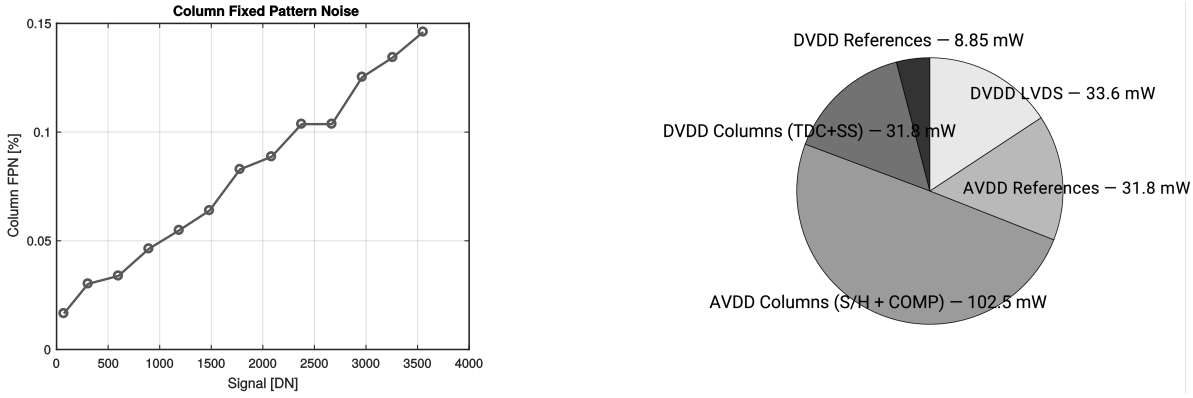
(a) **(b)**

Figure 4.39: Comparator noise contribution: a) comparator only (from comparator correlation analysis); b) total column output noise

Figure 4.39 shows output data computed using the method in Eqn. 4.16, Subfigure a) shows the calculated comparator noise being of 1/3 lower magnitude as compared to the total output column noise which is shown in Subfigure b). The difference is assumed to be contributed by clock jitter, sampling thermal noise and random walk noise on the ramp reference line.

4.4.4 Power Consumption

The chip operates at 1.5 and 3.3 V, and contains multiple isolated power and ground nodes. The measured power consumption was ≈0.2 W when run at 4.4 µs row time, excluding the power dissipated in the pixel array and LVDS drivers. The ADC power consumption per column, including references, was measured to be ≈177 µW. Figure 4.40b provides a visual representation of power division.



(a) (b)

Figure 4.40: a) Measured column fixed pattern noise as a function of the converted output signal level; b) Measured division of power consumption, ([I], reprinted by permission of IEEE)

4.5 Discussion

The presented work explored the proposed theoretical concept with a practical implementation of the hybrid scheme for Flash TDC-interpolation of SS ADCs. The implementation provides a proof of the presented concept for online radix calibration. The testchip of 1024 columns provides a realistic RC line drop test model which can be directly applied to large-scale implementations. The use of fully-independent ADC group segmentation allows ease of system scalability towards high column implementations which fits well in multi-thousand high-resolution column linescan sensors.

Excluding a slight linearity glitch caused by an unfortunate design error, the radix calibration scheme of the testchip matches well with the theoretical model. The observed linearity glitch provides a good representation of the Achilles heel of this architecture – namely that the matching and duty cycle of the count clock, as well as the propagation delay of all latches should be tightened to within the estimated limits. This especially holds critical for the difference between the TDC and LSB SS counter latch. It was verified that the open-loop delay line and correction coefficient stability can be kept within the designed correction coefficient recoverable range with delays close to the minimum process gate delay. The presence of column FPN due to the varying 5.6 – 5.4 µm column pitch has not been observed. The results show that the DCDS is able to completely eliminate the effect of comparator routing fanout-induced propagation delay difference on the ADC output.

The system has achieved a power consumption of 177 µW/column, 477 µV input-referred noise at ramp time of 1 µs and row conversion speed of 4.4 µs, which competes with recently reported column-parallel designs [81], [82], [83]. Despite the presence of a glitch in differential nonlinearity, the testchip proves the feedback-free clock phase generation and the proposed concept of delay-line calibration.

It can be concluded that the proposed digital gain calibration of interpolating TDCs in SS ADCs is fully feasible and can be applied not only to Flash TDCs but also other TDC designs. An emerging TDC system concept forms a good candidate for a combination with the presented

radix correction technique, tailored to column-parallel configurations. The next chapter focuses precisely on these other combination concepts, as well as system-level studies of the correction concept, applied to a different type of interpolating TDC.

5

Studies on Time-Domain Binary Search TDCs in Interpolated Single-Slope ADCs

Contents

The previous chapter explored the use of Flash TDC interpolator based systems. Unfortunately, expansions of the interpolation ratio with Flash TDCs is difficult due to the quadratic increase of the number of required clock phases with each additional bit of resolution. This is a major limitation of the Flash architecture, which impedes such systems from taking full advantage of the process gate speeds in the CMOS node. Here, albeit theoretically and on a high-level, we explore the potentials of a relatively new to the TDC world architecture, which takes advantage of the binary search algorithm.

The methods of binary-search have been known since ancient times and are widespread among various technical and scientific fields. Successive Approximation Register (SAR) A/D converter systems make use of this algorithm, and have been an area of research since the emergence of the silicon industry.

The binary search is a technique which compares the input sample with the mid-level of the

ADC reference dynamic range. If the input sample is lower, the upper half of the reference range is eliminated and the sample is compared to the half of the lower end of the refined range. These operations are performed successively until the search range falls within the desired resolution.

The time complexity $\mathcal{O}(n)$ of the binary search algorithm is by far the lowest within all known search methods applied to data converters, which has led to the excellent power-resolution metrics of voltage-domain SAR ADCs [84]. More recently, with the rise of popularity in Time-to-Digital Converters (TDC), a new area of binary search algorithm implementations in the time domain has been invented [85], [86].

This chapter is organized in three parts. Section 5.1 provides a high-level overview of the Time-Domain Binary Search (TDBS) technique by listing some of its features and design challenges. The use of TDBS in TDC-interpolated Single-Slope ADCs is discussed in Section 5.2, which also emphasizes on the use of a digital radix calibration method sharing similarities with the one presented in Chapter 4. Finally, some remaining challenges with the integration of TDBS TDCs in practical column-parallel systems are discussed in Section 5.3.

5.1 Principles of Time-Domain Binary Search

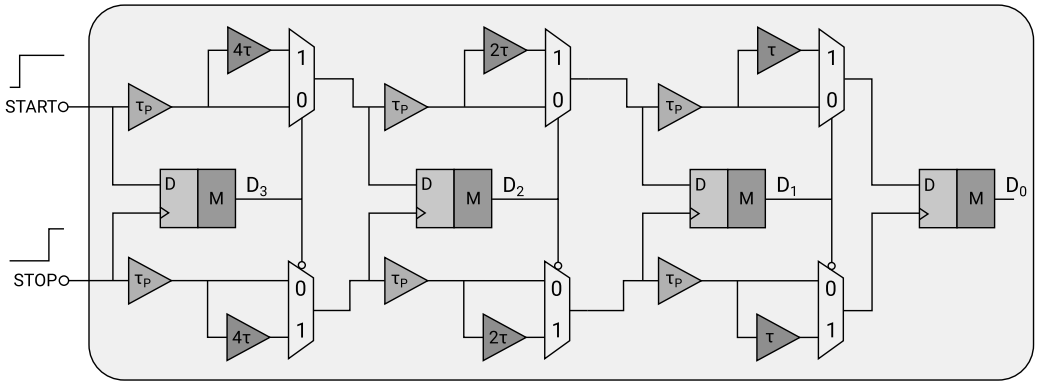
The time-domain binary search technique (TDBS) in the form of a closed-loop cyclic implementation has been explored long ago, and its properties as a standalone TDC are well-known [86]. The presented study in this chapter is based on the recent open-loop TDBS technique based on signal path divergence through a set of binary weighted delay elements [85].

The main concept of the time-domain binary search (TDBS) technique is presented in Fig. 5.1. Illustrations a) and b) show a block and timing diagram of the open-loop (feedbackless) TDBS TDC architecture. The time-difference between the START and STOP clock edges is measured in one step without any time-residue recycling. Compared to conventional SAR ADCs, which use consecutive reference voltage settling and recycling by the capacitive DAC [87], the TDBS scheme offers inherent conversion speed, which is equal to the binary-weighted dynamic range of the TDC.

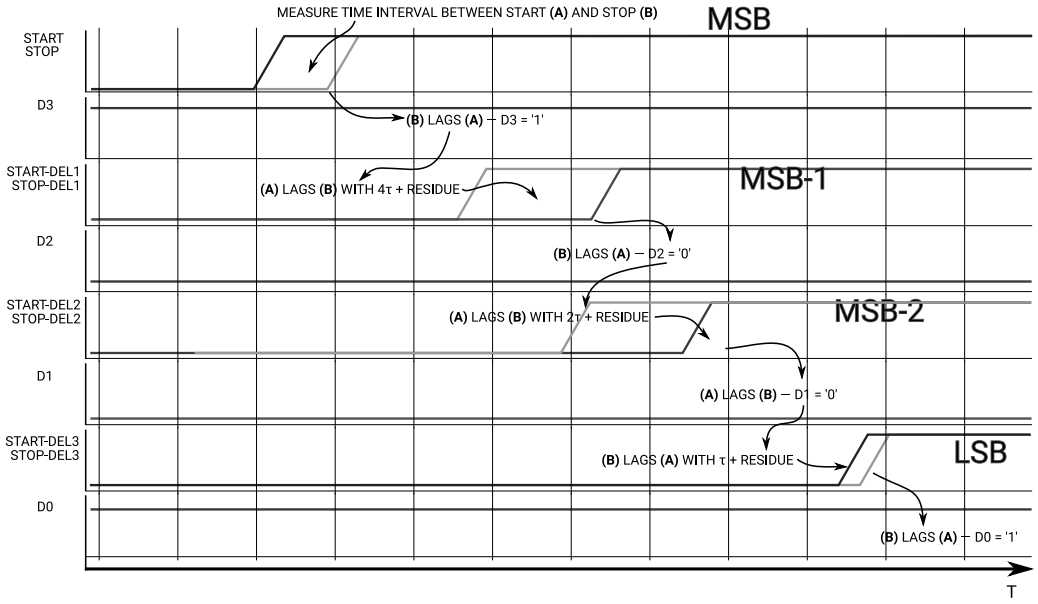
5.1.1 Operation

The first stage arbiter D3 in Fig. 5.1a measures the initial occurrence of the START (A) and STOP (B) signals. If (B) lags (A), the arbiter flags a high state, which is the MSB of the time-resolved signal. The output of the MSB arbiter controls the first stage multiplexers, which switch the signal path between a direct connection and passage through a reference delay element 4τ. The intentional pre-delay τ_p compensates the intrinsic propagation delay of the arbiters, and ensures that the signal path would be switched in prior to the arrival of the time-signal to be measured.

Signal subtraction is formed through the use of complementary multiplexers. This implies that only one of the (A) or (B) signals is fed through a delay path. Hence, the multiplexed through the delay signal is lagging behind the non-multiplexed. Fig. 5.1b shows the consecutive in time input-output of each TDBS stage. After signal time-subtraction of (B) referenced to (A), the arbiter of the second stage resolves whether (A) or (B) arrives first, which determines the



(a)



(b)

Figure 5.1: Time-Domain Binary Search: a) block diagram; b) timing

value of the MSB-1 bit. The signal is the fed to a binary-weighted $1/2 \times 4\tau = 2\tau$ delay stage and the arbitration operation continues in all consecutive stages until the resolution of the LSB. The remaining time-difference at the output of the LSB stage is the time residue of the binary search. Its amplification with a time difference amplifier (TDA) and consecutive time-domain measurement is technically possible. However, practical applications achieving higher resolution using this approach have been avoided due to difficulties of maintaining linear response of CMOS TDA blocks. Nevertheless, this remains a possible option for fine time resolution CMOS processes and shares a number of similarities with the single-slope time-interpolation technique presented in Chapter 2.

5.1.2 Delay Element Multiplexing

One may notice a redundancy in the use of dual delay elements in the concept presented in Fig. 5.1. Further circuit simplifications which reduce the number of required delay elements is possible. Fig. 5.2 shows a simplified schematic diagram of a TDBS delay multiplexing scheme, which removes the redundancy in the use of delay elements. Its principle of operation is described as follows.

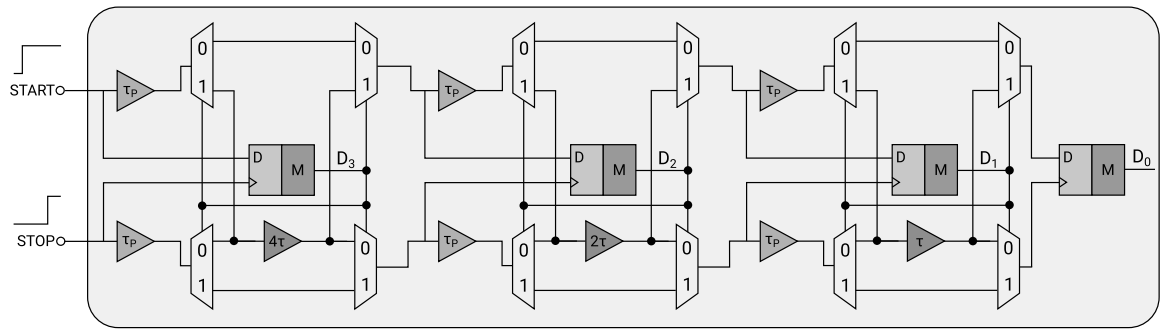


Figure 5.2: Delay element muxing scheme

The signals (A) and (B) are delayed one at a time, therefore the use of a single delay element per stage is possible. Each stage contains an additional front-end demultiplexer which diverts either signal (A) or (B) through a delay element. The non-delayed signal is fed through a direct path to the back-end multiplexer whose output enters the consecutive stage. A reduction of the delay element count allows for an improved mismatch resistance, area, and power, which makes column-parallel-based implementations of the TDBS scheme easier for practical implementation.

5.1.3 Errors and Nonidealities

Having explored the architectural principles of operation and possible improvements, some errors associated with the topology must be considered.

Differential nonlinearity errors associated with TDBS-interpolation originate from three sources: delay element mismatch; gain errors in the binary search TDC and cycle-to-cycle errors introduced by clock nonidealities. With the first degrading the interpolated word, while the second and third introduces DNL errors at the interpolation point.

Delay element matching and gain errors

To maintain a differential nonlinearity of less than 0.5 LSB, all TDBS module delay elements should be matched within $1/2\tau$ or better. It is worth noting that delay variation due to local device uncertainties increases with the increase of the absolute delay element time, which to a first order approximation follows a square root law. Thus, delay elements being part of the most significant bits are prone to higher mismatch. The explanation for this is the longer drift trajectory of the starved current integration devices and the impact of threshold variations on

voltage nodes with lower derivatives (being the case of a long delay time). This is evident in the Monte Carlo simulation results of a current-starved CMOS inverter shown in Fig. 5.3.

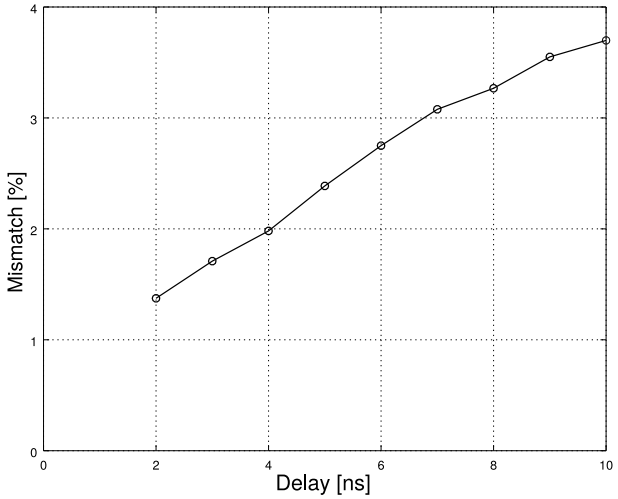


Figure 5.3: Current-starved delay element mismatch versus delay time — data obtained by means of monte-carlo analysis

Group delay instability with PVT corners can be easily corrected through a global gain correction. However, the matching in a column-parallel implementation is critical for correct operation. It should be noted that from Fig. 5.3, it is also evident that mismatch is significantly improved with delay times approaching the intrinsic gate delay of the used CMOS process. Thus, although being unintuitive, running the TDBS at higher speeds helps in handling mismatch errors.

Metastability errors

Metastability in delay capture flip-flops in the TDBS leads to arbitration errors. Once an arbitration error has occurred (unless the signal pulse difference has occurred closer than $\tau/2$), this leads to code gaps which can not be corrected. It is therefore of high importance that the pulse edges are always maintained sharp with as fast a rise time as the process allows, or at a maximum of $1/2 - 1/4\tau$.

5.2 Interpolation with the Time-Domain Binary Search

The use of the TDBS as a time interpolator in a single-slope ADC is sketched in Fig. 5.4.

The TDBS TDC (displayed as SAR TDC in Fig. 5.4) detects the time distance between the comparator toggle pulse and the next count clock edge. The architecture in Fig. 5.1a provides a differential TDC conversion which is referred relative to the STOP pulse and provides a positive "0XXX" or a negative "1XXX" binary value. Unfortunately, this mode of operation impedes the use of the TDBS as a direct interpolator. The TDC and ADC words can be concatenated if the TDC word is offset which can be done either digitally by adding $1/2 \times 2^N$, or through the addition of a long enough $> \tau_{MSB}$ delay element, which provides an artificial offset of the TDC.

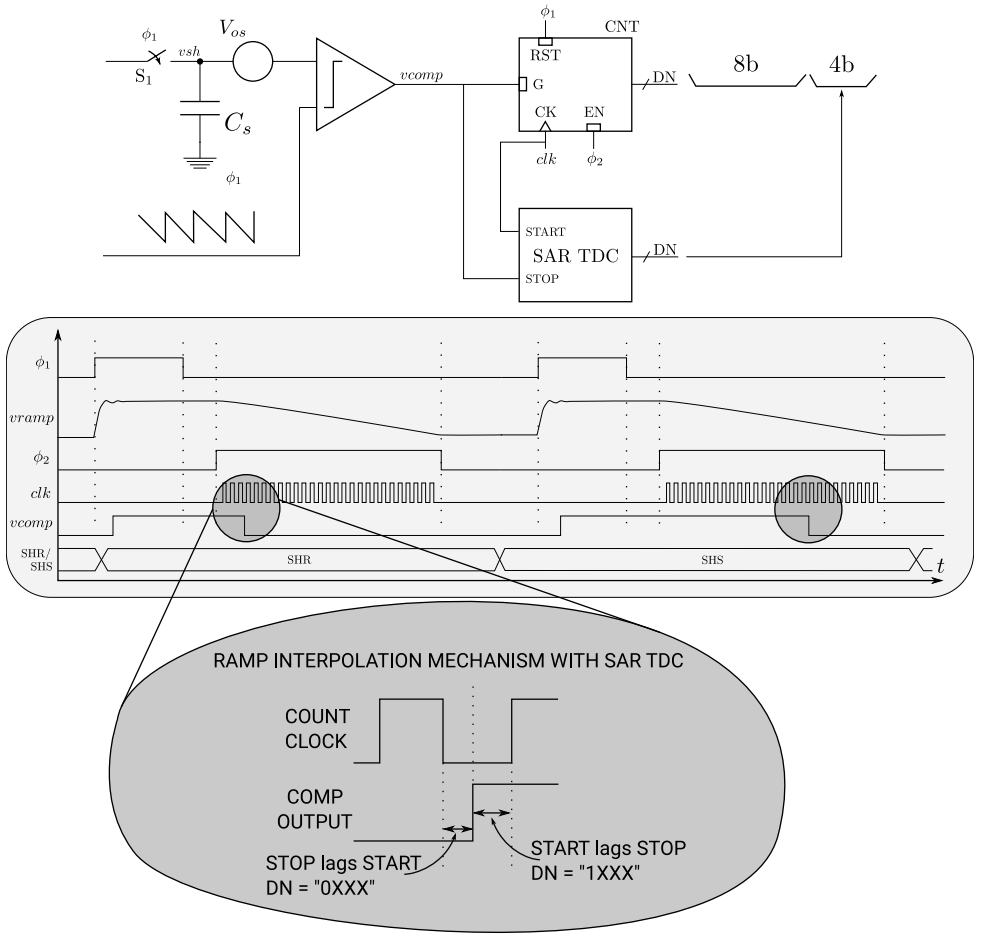


Figure 5.4: Principle of TDBS intrpolation of a Single-Slope ADC

The latter, compared to the digital solution extends the dynamic range of the TDC without the need for the addition of an extra stage, which is the case with the digital method. Figure 5.5 shows the concept underneath both approaches.

To perform a successful interpolation of the word produced by the single-slope ADC, the total dynamic range of the TDBS must equal 1/2 the clock period used to increment the counter. The use of open-loop current-starved delay elements is challenging for maintaining drift stability with voltage and temperature corners. Therefore, the use of a similar to the presented self-calibration method in Chapter 4 could be applied in the case of a TDBS TDC as well.

5.2.1 TDBS Gain Calibration

To undertake calibration of the TDC to eliminate gain errors originating from delay element drift one must be able to measure its full dynamic range. One way to achieve this is by comparing the measured TDC word to a time reference signal. As the clock period of the single-slope ADC is usually generated by a PLL and its period is well-known, it forms the base of the output word of the single-slope counter. Therefore, the count clock can be used to measure the

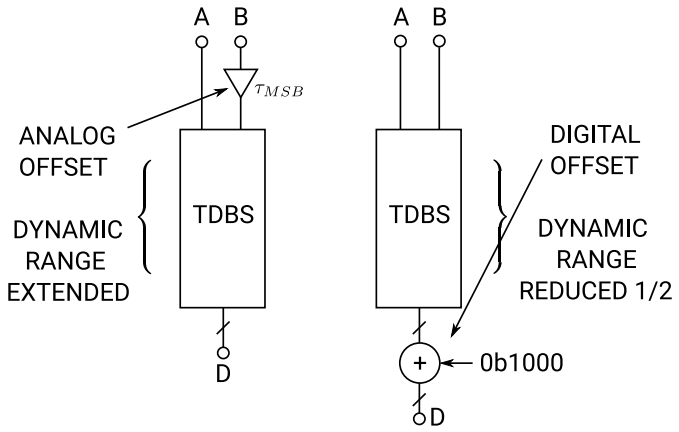


Figure 5.5: Intentional offset to use the most out of the TDC dynamic range. Left: analog; Right: digital methods

TDC dynamic range which can be corrected in a consecutive operation. Figure 5.6 shows an overview of the dynamic range measurement principle.

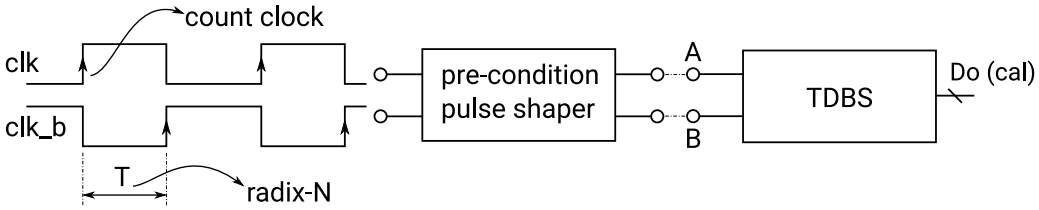


Figure 5.6: Principle of TDC gain (radix) measurement, referred to the count clock (main radix of SS counter)

The differential single-slope count clock can be used as a TDC reference stimulus. The pulse-shaper block shown in Fig. 5.6 is used to pre-condition the clock signal to feed-out one-shot rising edge pulses to the TDC. This is thereby leading to a converted TDC binary number which is equivalent to a full single-slope (interpolated word) LSB. The equivalence is due to the use of the same clock period to increment the single-slope counter. Once the measured value is known, a correction coefficient can be derived by means of a simple division operation

$$K = \frac{D_{fs}}{D_{o_{cal}}} \tag{5.1}$$

where D_{fs} is the ideal full-scale signal ('0b1111' in the case of a 4-bit TDBS) and D_{ocal} is the measured output word. It may be noted that this coefficient can only be valid if the TDC is intentionally designed to have a lower gain in all PVT scenarios, so that the calibration measurement output does not lead to saturation and overflow.

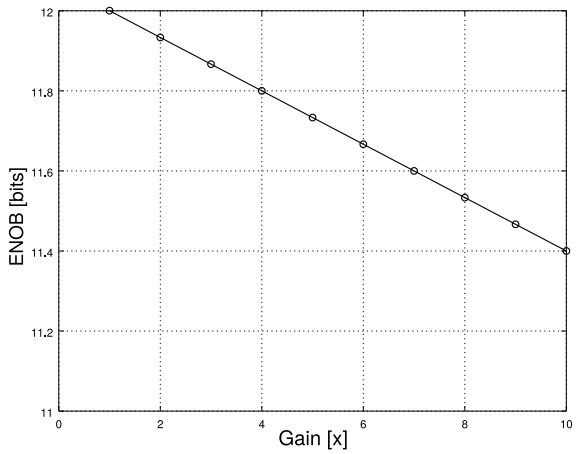


Figure 5.7: ADC Effective Number of Bits (ENOB) versus TDC gain

$D_{o_{cal}}$	D_{fs}	G	K
1111	1111	0.93	1
1110	1111	0.86	1.07
1101	1111	0.80	1.15
1100	1111	0.73	1.25
1011	1111	0.66	1.36
1010	1111	0.60	1.5
1001	1111	0.53	1.66
1000	1111	0.46	1.88
0111	1111	0.40	2.14
0110	1111	0.33	2.50

Table 5.1: Gain calculation scenarios and desirable operating range

Table 5.1 summarizes the gain calculation scenarios. The desirable operating range lies at TDC gains closer to x1 (shown in gray), as otherwise a loss of Effective Number of Bits (ENOB) is exhibited (shown in Fig. 5.2.1) and a higher numerical noise floor is introduced due to the correcting multiplication operations.

5.2.2 Preconditioning Block

The single-slope count clock and comparator can not be directly fed to the TDBS module. This would otherwise generate an excessive amount of switching and power (energy) consumption, which is undesirable and potentially disastrous in a column-parallel implementation. Therefore, a preconditioning circuit block isolating the clock and comparator output with the TDBS module and thus limiting unnecessary switching is proposed and shown in Fig. 5.8.

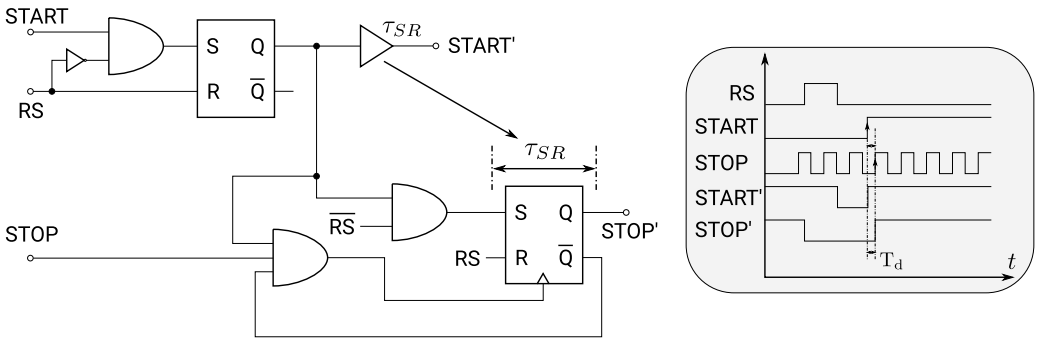


Figure 5.8: Principal pre-conditioning block

The first stage of the preconditioning circuit latches the start signal transition to high state using an SR latch. Its output is used in the follow-up SR flip-flop to enable the stop operation. When a stop pulse is encountered it is latched by the secondary SR latch and hence the stop propagates

to the TDBS module. The slave SR latch remains set until an external (global) reset pulse RS is applied which initializes the preconditioning module for a new conversion cycle. The delay element τ_{SR} in the start signal chain compensates the added delay offset to the stop signal by the AND logic gates and the clocked SR latch. If the offset compensation delay has a mismatch and the delay path is unbalanced, such a mismatch is further cancelled by the gain correction circuitry and it only has an impact of the total TDC dynamic range measurement.

5.2.3 Proposed Column-Parallel ADC System Design

In order to facilitate the TDBS in a per-column parallel configuration it is necessary that each column converter stores an individual calibration coefficient. In order to ease readout and post-processing, the integration of a simple multiplication and subtraction-capable ALU must also be present. Figure 5.9 shows a proposed block diagram for the TDBS module, containing three individual bits of memory per stage. Each bit block stores the Reset (SHR3-0), Signal (SHS3-0) as well as correction coefficient data (K3-0).

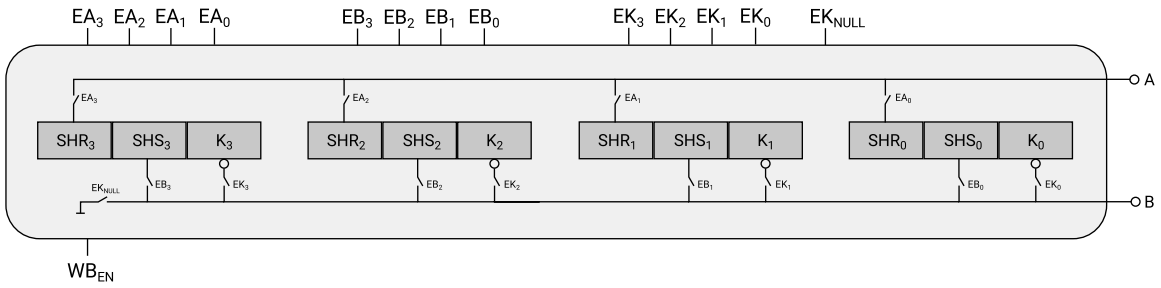


Figure 5.9: TDBS register memory cells

To save power and silicon area, the storage cells dedicated for the Reset (SHR3-0) conversion are also re-used as an output post-DCDS result register. Such configuration allows for an online DCDS conversion and parallel correction, which is invisible to the end user and the consecutive image processing pipeline. To achieve these system requirements a re-configurable bit-serial multiplier and subtracter is proposed in Fig. 5.10. It consists of a re-configurable adder/subtracter block, a latency flip-flop and an 8-bit partial product register. Once the multiplication operation is performed, the fixed-point result is rewritten back to the SHR3-0 memory array through the WB_{EN} pulse and the A/B serial data lines. It is important to note that the DCDS subtraction operation should be performed on the whole ADC word (including the word from the single-slope counter) for which a propagation link between the TDBS multiplier and the binary counter should be implemented.

Figure 5.11 shows an overview of the digital back-end of a complete ADC column which includes the TDBS TDC, multiplier and single-slope counter. The blocks should be prepared such that there is minimal vertical routing, which is the driving force for the use of a bit-serial multiplier, trading speed with area and simplified vertical routing. All global control signals are distributed horizontally. The delay elements present in the TDBS must be accompanied by strong decoupling due to the lack of delay trimming feedback which impacts data output jitter and power supply ripple translation to timing errors. The problem with open-loop delay elements forms a major implementation challenge with the proposed open-loop architecture. Some of the associated issues are further discussed in the next section.

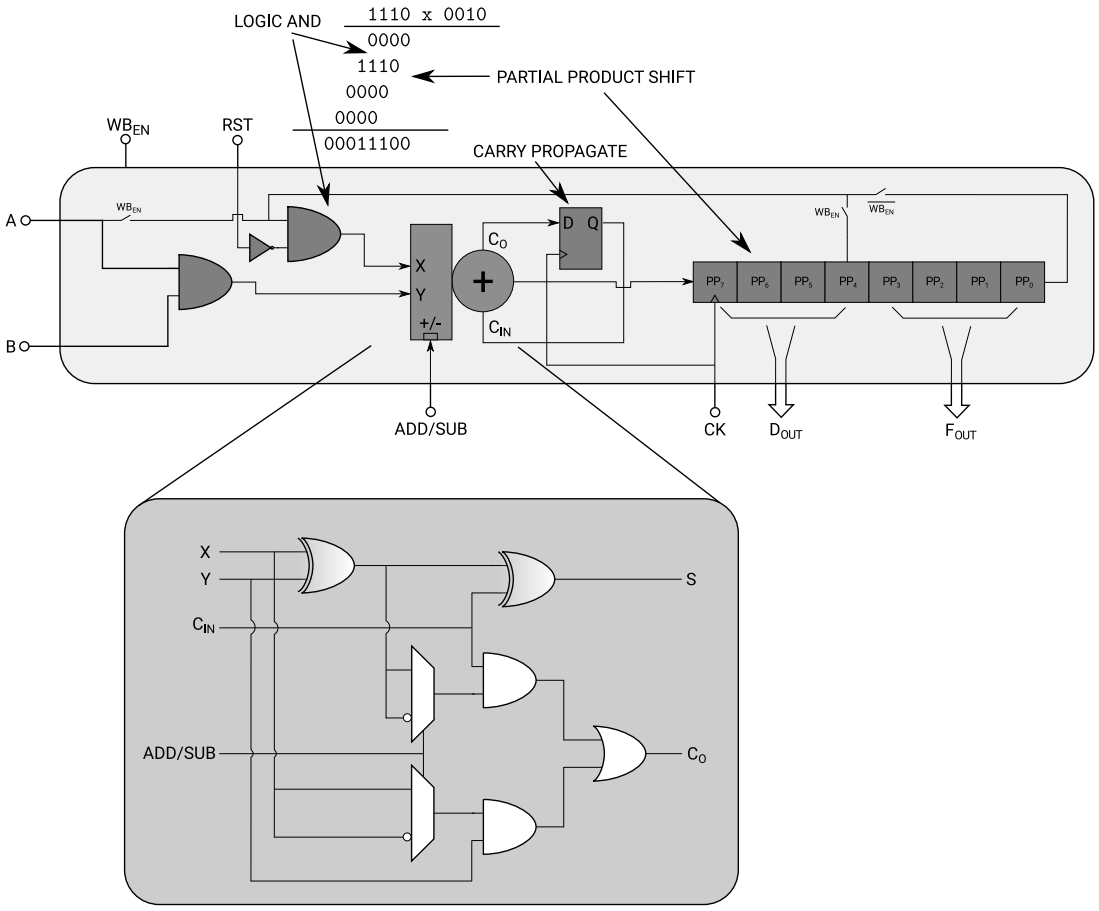


Figure 5.10: Proposed bit-serial multiplier

5.3 Prospective Conversion Rates and Unsolved Issues for Column-Parallel Implementation

As the goals of the presented conceptual architecture are to increase conversion rate while maintaining the same resolution, it is important to list the estimated rate of speed increase by TDBS interpolators. Table 5.2 provides theoretical conversion time estimates for TDBS-interpolated SS ADCs for a few possible configurations.

N	MSB	LSB	Rate	Delay Elements	Clock Speed	τ	T_{conv}
1	8	4	SDR	3	4 ns	250 ps	1 µs
2	9	3	SDR	2	4 ns	500 ps	2 µs
3	8	4	DDR	3	4 ns	250 ps	0.5 µs
4	9	3	DDR	2	4 ns	500 ps	1 µs
5	8	4	DDR	3	8 ns	1000 ps	1 µs

Table 5.2: Theoretical conversion time estimated for various TDBS-SS configurations

The presented configurations take into account the maximum bandwidth offered by conven-

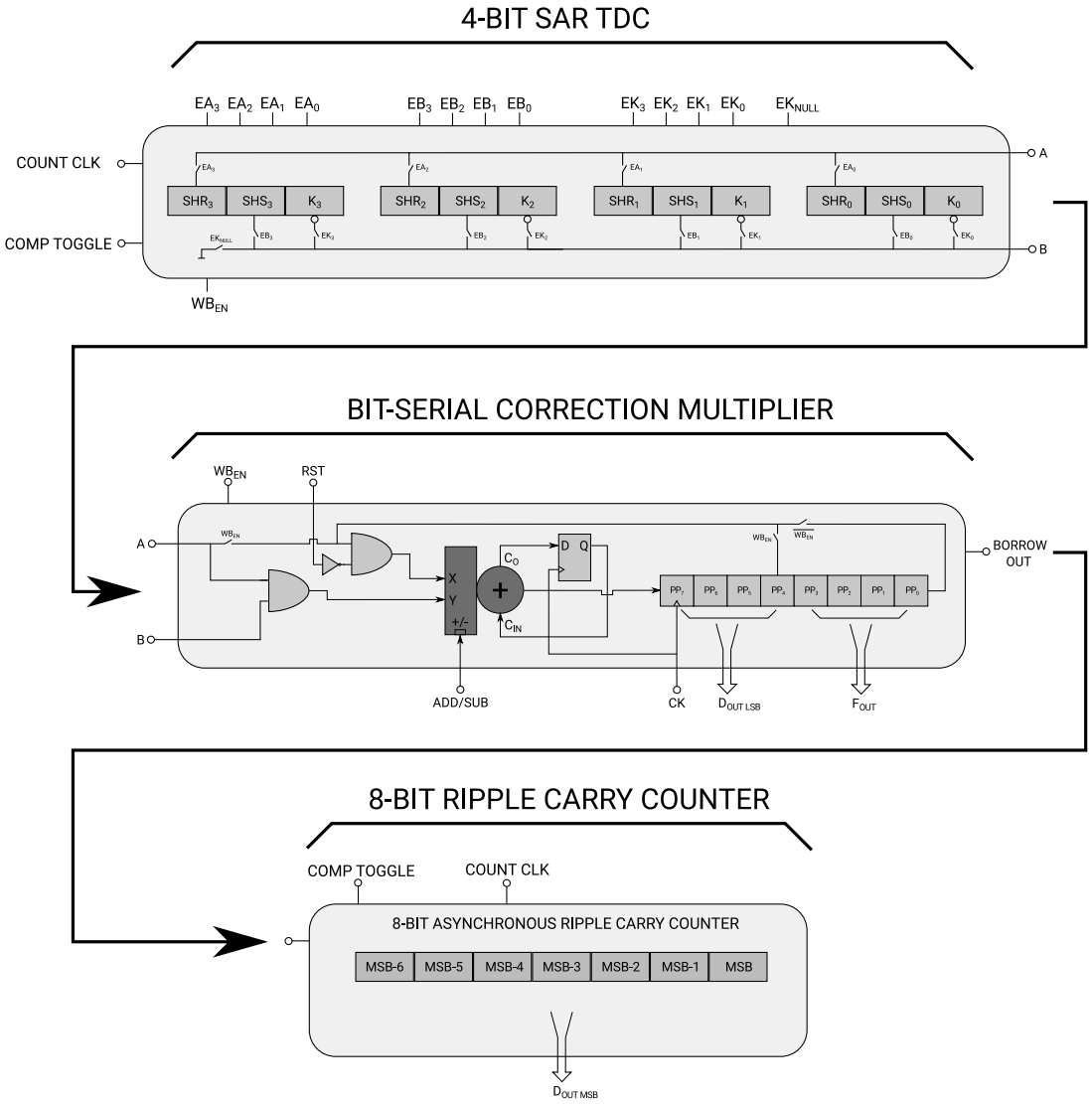


Figure 5.11: Digital back-end of a single ADC column

tional current-day CMOS image sensor process nodes such as 90 nm. A configuration employing a 4-bit interpolating TDC requires three delay elements, which in combination with a 250 MHz count clock make up a requirement of a 4 ns TDC dynamic range. With the use of a double data rate single-slope counter, a standard conversion cycle would be in the order of 500 ns, which is approximately 2× faster than the currently reported cutting edge 12-bit column-parallel image sensor ADCs [81], [82], [83].

Achieving the estimated conversion rates with the proposed architecture, however, can only be realized if a solution to the major issue linked with the in-column reference delay elements is found. Proving the functionality of the proposed TDBS interpolator can not be achieved by means of sole simulations. This is due to the computational and modelling complexity involved with ADC array implementations. The use of open-loop reference delay elements inside the column poses questions related to their stability and jitter, as well as the matching of individual delay stages with a special emphasis the most significant bit-cells. The MSB bitcells have the

longest reference delays which amplifies the impact of device mismatch. However, all of these questions remain unexplored and form grounds for future investigations.

6 Conclusions and Perspectives

This chapter summarizes the outcome of the presented chapters and points to grounds for potential future investigations. This thesis explored methodologies for time-interpolation of single-slope ADCs with a target to improve conversion speed in CMOS image sensors while maintaining the same ADC resolution and power consumption.

This chapter gives a summary of the conducted investigations. Section 6.1 lists a chronological condensed summary, while Section 6.2 provides details on the main outcome of this thesis. Section 6.3 lists a natural continuation of the conducted investigations by defining some possible topics for future exploration.

6.1 Condensed Summary

Chapter 1 settled the motivation and goals of the conducted investigations by focusing on the core problem which this thesis is attempting to solve.

The reader was provided with a brief introduction to column-parallel single-slope ADC architectures in Chapter 2. The critical performance degradation errors have been summarized while previous work on interpolation methods and similar speed-resolution improvement schemes were also presented. The concepts of the use of TDCs as interpolators were introduced.

Chapter 3 prepared the reader to the further presented design by discussing reference voltage generation techniques. A detailed noise analysis during both fundamental conversion phases in single-slope converters was presented, including a numerical simulation and experimental proof.

Chapter 4 proposed a digital gain calibration method applied to Flash TDC-interpolated SS ADCs. A proof of concept through the design of a 1024-column 12-bit hybrid ADC structure was presented, which showed promising results in favour of the proposed architecture. Detailed design implementation, useful characterization techniques and data was also listed and discussed.

Finally, a natural continuation of the introduced radix correction method applied to a more efficient TDC architecture using a Time-Domain Binary Search approach was presented in Chapter 5. Albeit conceptual, the TDBS technique forms solid grounds for future investigations and a continuation of this research.

6.2 Conclusions

The core of this work investigated a time-interpolation technique following a design paradigm favouring digital techniques. It allows for a complete elimination of analog DLL- and PLL-based clock generation blocks in column-parallel TDC-interpolated ADC architectures. This was achieved through the introduction of a TDC radix correction technique, which uses the single-slope ADC reference clock for radix calibration. The digital feedback mechanism relaxes the requirements on the clock generation block and therefore eliminates the necessity of analog clock feedback loops. As a result a new high-speed column-parallel data converter was designed and fabricated which competes and advances state-of-the-art imaging ADCs in terms of speed-resolution and power.

6.2.1 Main outcome

The proposed correction technique was proven in silicon through the implementation of a 1024 channel column-parallel ADC array. Measurement results have shown the validity of the technique, while the preliminary implementation results provide solid grounds favouring the feasibility of the technique and its employment in a mass-production scenario. The presented ADC group segmentation, combined with the correction technique allows for local clock generation, which improves the sharpness of the TDC clock edges. Those combined techniques improve the time resolution of the TDC. It was thus shown and proven that an ADC segmentation approach is highly desirable in Flash TDC-interpolated implementations. It is worth noting that the concept of group segmentation is also applicable in group-parallel ADC implementations, where a single ADC channel serves a few column pixel lines.

6.2.2 Reference generation analysis

Followed by the characterization efforts in evaluating the performance of the testchips, the noise contribution during the ramping phases in a secondary mass-production device has been identified and formalized mathematically. Contrary to intuition, a quicker conversion phase yields lower ADC output noise. It was identified that the effect is caused by thermal noise integration on the reference voltage which strictly follows a random walk uncertainty with a growing deviation with time. This effect occurs in all single-slope ADCs which use continuous-time integrator based reference generation. Except for integration of noise on the ramp, its translation was identified to be linearly linked to the derivative of the ramp and its angle of crossing with the input sample level.

6.2.3 Introducing a more efficient hybrid interpolator

Some exploratory work and a natural continuation of this research was the expansion of the presented radix calibration technique to more efficient TDC architectures. The Flash TDC architecture does not possess high intrinsic energy efficiency per converted bit of resolution due to its 2^N complexity. Therefore, to further refine the radix correction scheme, and to take advantage of potentially more efficient implementations, some studies on a recent open-loop Time-Domain Binary Search (TDBS) TDC architecture were conducted. The TDBS architecture has an inherent advantage on size and delay element count. Its simplicity in distribution of clock lines compared to Flash TDCs is also favorable. Unfortunately, with this advantage comes an associated (and contradictory) drawback. This is the number of delay elements required for potential column-parallel TDBS implementations. The number of delays are a multiple of the number of columns. The added additional complications with respect to delay element matching between columns as well as their binary weighted accuracy with process, voltage and temperature variations were identified and prepared for further investigations.

6.3 Future Work

There are plenty of improvement opportunities in the field of high-speed IC design for imaging. Basing on the conducted work as part of this thesis, a few natural experimentation paths could be pursued. This section summarizes and identifies some of the most relevant areas for exploration.

6.3.1 Improvements in time-domain interpolators and column-parallel architectures

A very exciting continuation of the core topic of this thesis is the further development of the examined in Chapter 5 architecture. The main design challenge of the proposed TDBS scheme is the finding of highly accurate delay elements. Naturally, the search for a rock-solid CMOS delay element could be continued. Once the right approach in building a process, voltage and temperature insensitive delay element is found, a high column number implementation would ultimately prove how realistic the TDBS concept is in practice. If successful, this would lead to a development strategy which significantly advances the implementation presented in the current thesis as well as the designs currently known to the imaging community.

Going off-track with regular analog VLSI engineering (which is the case if the delay element improvement approach is sought), another exciting research opportunity lies at the possibilities for correction of binary weight mismatch between the reference delay elements. This could be achieved through offline digital back-end calibration techniques. A potential candidate for exploration which uses binary weight correction are the Beta expansion techniques [88], [89], [90]. In theory, these methods could be successfully applied to the pipelined and cyclic architectures [90]. However, Beta expansions calibrations have never been implemented in many real world designs due their high back-end computation complexity. They also require large memories for coefficient storage. A column-parallel implementation case would add even more complexity and memory overhead in a potential implementation. However, there have been recent advances in Beta and flaky quantizers pursued by the mathematical combinatorics

community [91], [92], [93]. Thus, a revisit of Beta expansions and research towards practical back-end calibration schemes could show high potentials in improving the performance of column-parallel ADCs.

6.3.2 Appications of time-domain interpolators in 3D-stacked integrated circuits

Recent advances in semiconductor technology have allowed us to manufacture microchips with three-dimensional level of integration, also widely known as 3D stacking. This packaging approach has shown to be very beneficial for all high-integration level VLSI devices, and more specifically CMOS image sensors. 3D integration allows complete isolation between the pixel array substrate from the readout IC device. Essentially, a modern 3D stacked imager comprises two, or more silicon devices. This allows substantial improvements in sensor noise performance and temporal bandwidth, but imposes various challenges linked not only with the packaging of the device itself, but also the organization of the readout IC chip. Modern readout IC chips which form part of a stacked CMOS image sensor have to employ creative group-parallel, or even pixel-parallel ADC implementations. On top of everything, the obvious improvements in image quality and pixel performance of isolated imaging arrays imposes even higher requirements on ADC resolution, to yield most out of the pixel signal. Fortunately, the single-slope ADC favours CMOS node scaling and together with the time interpolation technique it is an exceptional candidate for 3D stacked ROIC implementations.

A potentially important task for future explorations within this direction would be the reconfiguration of the explored techniques in this thesis. The column-parallel architecture could be re-arranged in ADC clusters suitable for 3D stacking. This includes a complete redesign of the comparator structure, ramp generation as well as the clock distribution network. The final goal of such an architecture translation would be the achievement of the first pixel or cluster-level implementation of a FTDC interpolated single-slope ADC for a 3D stacked image sensor.

6.3.3 Research in wave propagation of kickback noise on ramp references in high-resolution image senors

The conventional approach for comparator kickback noise mitigation is its elimination from the origin. One approach for kickback reduction was presented in Chapter 3 and 4 and used active analog techniques. A drawback in the conventional active reduction approach is that it uses additional power. In the case of the technique presented in Chapter 4 the scheme also influences the linearity of the comparator which is undesirable.

Another approach for kickback noise mitigation is the decoupling of the columns by creating a high-resistance reference line which isolates high-bandwidth glitching between the columns. This approach does not yet fully limit the bandwidth and allows for a gradual decrease of the reference line. However, the modelling of high-column-number coupled systems is complex. The choice of coupling resistance to maintain the required derivative of the ramp, while isolating kickback is currently approached with empirical methods, if considered for implementation at all. A potentially exciting continuation of the work presented in Chapter 3 is the establishment of a physical model of the column comparators as a coupled electrical system. The transient

behaviour of these systems should be further modelled to include the wave model of the kick-back noise to find out the wave interference of neighbouring columns. The back-propagation self-triggering due to wave interference should also be explored.

The outcome of such a study could be of great benefit to the understanding of kickback noise coupling and propagation. A column-parallel system designed using the proposed decoupling approach could greatly improve the power consumption and linearity of column comparators.

6.3.4 Fundamental search algorithm exploration

Current state-of-the-art data converter designs have not by far reached even the mid-point of the physical efficiency limits of Nyquist rate data converters [94]. In the meanwhile, research in theoretical computer science has advanced dramatically, offering a deep understanding of fundamental search algorithms and their efficiency.

Analog-to-digital converters could be looked as effectively forming a type of voltage search algorithm. They possess surprising similarities with some search algorithms explored within the field of theoretical computer science. Investigations of theoretical search algorithms applied to voltage domain search could provide a different angle towards ADC design, albeit the abstract sounding of the proposed study. Mapping and categorization of all existing voltage search techniques could show hidden possibilities in data converter configurations in the form of unexplored hybrid ADC architectures. The derivation of fundamental efficiency figures (from the perspective of information theory) for these algorithms could provide an insight and even spur new ideas not only for hybrid, but fundamentally new ADC architectures.

Appendices

A

Integrated Thermal Noise Power During the Ramping Process

The following appendix provides a step-by-step solution of the ramp noise power model. Substituting the frequency response of the rectangular window in (3.10) and the thermal noise PSD (3.11) in (3.9) leads to the following definite integral problem

$$\langle v_n^2 \rangle = \frac{1}{C} \int_0^\infty 4kTg_o t_d^2 \left(\frac{\sin(\pi f t_d)}{\pi f t_d} \right)^2 df$$

computing the indefinite integral, taking the constants out and refining

$$= 4kTg_o t_d^2 \int \frac{\sin^2(\pi f t_d)}{\pi^2 f^2 t_d^2} df = 4kTg_o t_d^2 \frac{1}{\pi^2 t_d^2} \int \frac{\sin^2(\pi f t_d)}{f^2} df$$

applying integral substitution $\int f(g(x))g(x)dx = \int f(u)du$, $u = g(x)$; $u = \pi t f$, $du = t\pi df$

$$= 4kTg_o t_d^2 \frac{1}{\pi t_d} \int \frac{\sin^2(u)}{u^2} du$$

integrating by parts $\int uv' = uv - \int u'v$; $u = \sin^2(u)$, $u' = 2\sin(u)\cos(u)$, $v' = 1/u^2$, $v = -1/u$

$$= 4kTg_o t_d^2 \frac{1}{\pi t_d} \left(-\frac{\sin^2(u)}{u} - \left(-2\frac{1}{2} \int \frac{\sin(2u)}{u} du \right) \right)$$

final integral substitution $v = 2u$, $dv = 2du$ and simplifying

$$= 4kTg_o t_d^2 \frac{1}{\pi t_d}\left(- \frac{\sin^2(\pi f t_d)}{\pi f t_d} - \left(- \mathrm{Si}(2\pi f)\right)\right)$$

computing the boundaries $f \rightarrow 0$

$$\lim_{f\to 0}\left(4kTg_o t_d^2 \frac{1}{\pi t_d}\left(- \frac{\sin^2(\pi f t_d)}{\pi f t_d} - \left(- \mathrm{Si}(2\pi f)\right)\right)\right) = 0$$

and for $f \rightarrow \infty$

$$\lim_{f\to \infty}\left(4kTg_o t_d^2 \frac{1}{\pi t_d}\left(- \frac{\sin^2(\pi f t_d)}{\pi f t_d} - \left(- \mathrm{Si}(2\pi f)\right)\right)\right) = 2kTg_o t_d$$

subtracting the boundaries and adding the $1/C$ constant, the noise power per hertz of bandwidth is:

$$\langle v_n^2 \rangle = \frac{1}{C}\Big(2kTg_o t_d - 0\Big) = \frac{2kTg_o t_d}{C}.$$

B

Complete Derivations for Comparator DC Gain and Noise

A detailed calculation of the DC Gain, poles and bandwidth of the comparator in Fig. 4.11 is provided below.

B.1 Feedback Loop for Kickback Reduction

To analyze the properties of the stability loop and derive its poles, for convenience we first draw its first-order equivalent small-signal model as shown in Fig. B.1. One may note that the highlighted area in Fig. 4.11 contains a feedback controlling the tail bias source of the comparator to eliminate the varying load on the ramp. Thus, all devices associated with the comparator stages can be omitted from this analysis.

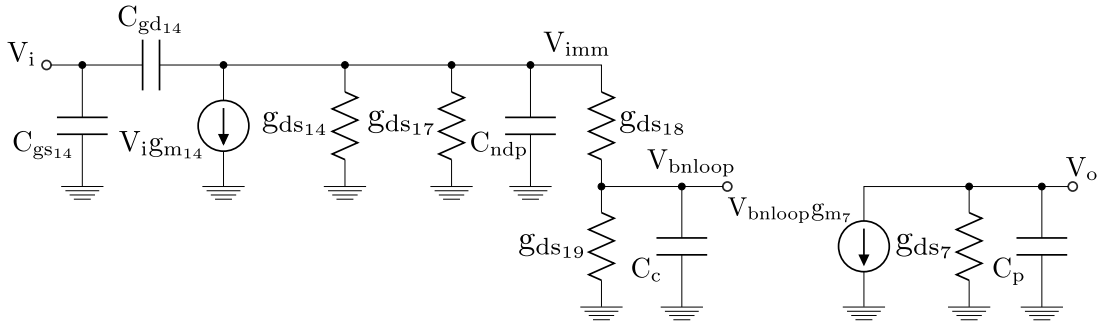


Figure B.1: Equivalent small-signal model of the kickback compensation loop

We can divide the feedback loop to three sections

$$TF_{LOOP} = TF1 \times TF2 \times TF3$$

therefore, for the input section

$$TF1 = \frac{V_{imm}}{V_i} = -\frac{g_{m_{14}} + sC_{gs_{14}} + sC_{gd_{14}}}{g_{ds_{14}} + g_{ds_{17}} + \frac{g_{ds_{18}}+g_{ds_{19}}}{g_{ds_{18}}g_{ds_{19}}} + sC_{ndp} + sC_{gd_{14}}}$$

for the folded cascode output branch

$$TF2 = \frac{V_{bnloop}}{V_{imm}} = \frac{g_{ds_{18}} + g_{ds_{19}}}{g_{ds_{18}}g_{ds_{19}}} sC_c$$

and the tail source m-factor bridging transistor M7

$$TF3 = \frac{V_o}{V_{bnloop}} = -\frac{g_{m_7}}{g_{ds_7} + sC_p}.$$

Finally for the dominant pole in the feedback loop we obtain

$$|p_1| = \frac{1}{\frac{1}{g_{ds_7}} sC_p}$$

and the second pole

$$|p_2| = \frac{1}{R_o C_L} = \frac{1}{\left(g_{ds_{14}} + g_{ds_{17}} + \frac{g_{ds_{18}}+g_{ds_{19}}}{g_{ds_{18}}g_{ds_{19}}}\right)\left(sC_{ndp} + sC_{gd_{14}}\right)}.$$

The stability of the feedback loop has been further discussed in Section 4.3.2.

B.2 DC Gain and Noise

The DC gain of the comparator is the product of the individual gains of its three cascaded stages

$$A_0 = \underbrace{\frac{g_{m_1}}{g_{ds_1} + g_{ds_3}}}_{\text{STAGE 1}} \times \underbrace{\left(-\frac{g_{m_8}}{g_{ds_8} + g_{ds_{10}}}\right)}_{\text{STAGE 2}} \times \underbrace{\left(-\frac{g_{m_9}}{g_{ds_9} + g_{ds_{11}}}\right)}_{\text{STAGE 3}}.$$

The contribution of a cumulative (both thermal and 1/f) noise from each active device is taken into account for the noise analysis. Figure B.2 presents the noise analysis equivalent for a small circuit branch.

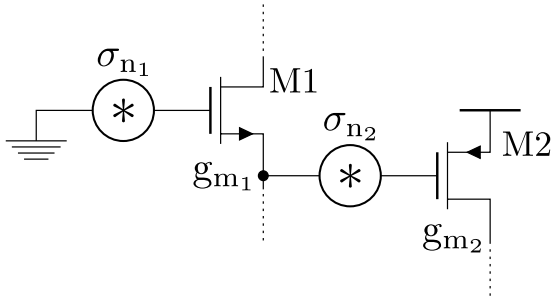


Figure B.2: Principal noise analysis applied to a circuit branch

In this sample case the output noise current at the drain of M1 is

$$i^2_{oM1_n} = g^2_{m_1}\sigma^2_{n_1}.$$

Similarly to obtain the output noise voltage at the drain node of M1 we multiply the output noise current with the node impedance

$$v^2_{oM1_n} = i^2_{oM1_n}\frac{1}{g_{ds_1}}.$$

The output noise voltage power of M1 is summed with the input-referred noise voltage σ_{n_2} to produce a final output noise current of

$$i^2_{oM2_n} = \left(g^2_{m_1}\sigma^2_{n_1}\frac{1}{g_{ds_1}} + \sigma^2_{n_1}\right)g^2_{m_2}$$

and output voltage noise power respectively

$$v^2_{oM2_n} = \left(\left(g^2_{m_1}\sigma^2_{n_1}\frac{1}{g_{ds_1}} + \sigma^2_{n_1}\right)g^2_{m_2}\right)\frac{1}{g_{ds_{M2}}}.$$

Following the same principle, for the comparator in Fig. 4.11 we can derive the output voltage noise for the differential pair (stage 1)

$$i^2_{o_n} = g^2_{m_1}\sigma^2_{n_1} + g^2_{m_2}\sigma^2_{n_2} + g^2_{m_3}\sigma^2_{n_3} + g^2_{m_4}\sigma^2_{n_4}$$

$$\sigma^2_{v_o} = i^2_{o_n}\frac{1}{g_{ds_2} + g_{ds_4}}.$$

Respectively the output noise voltage for the second and third stage will be

$$i^2_{o_{n_2}} = g^2_{m_5}(\sigma^2_{V_o} + \sigma^2_{V_{n_5}}) + g^2_{m_6}\sigma^2_{n_6}$$

$$\sigma^2_{V_{o_2}} = i^2_{o_{n_2}} \frac{1}{g_{ds_5} + g_{ds_6}}$$

and for the third stage

$$i^2_{o_{n_3}} = g^2_{m_7}(\sigma^2_{V_{o_2}} + \sigma^2_{V_{n_7}}) + g^2_{m_8}\sigma^2_{n_8}$$

$$\sigma^2_{V_{o_3}} = i^2_{o_{n_3}} \frac{1}{g_{ds_7} + g_{ds_8}}.$$

Combining the three stage equations we obtain for the output noise:

$$\sigma_{V_{out}} = \Bigg(\Bigg(\Bigg(\Bigg(\overbrace{\Big(g^2_{m_1}\sigma^2_{n_1} + g^2_{m_2}\sigma^2_{n_2} + g^2_{m_3}\sigma^2_{n_3} + g^2_{m_4}\sigma^2_{n_4}\Big)\frac{1}{g_{ds_2} + g_{ds_4}}}^{\text{NF STAGE1}} + \underbrace{+\sigma^2_{n_5}\Big)g^2_{m_5} + g^2_{m_6}\sigma^2_{n_6}\Big)\frac{1}{g_{ds_5} + g_{ds_6}}}_{\text{NF STAGE 2}} + \underbrace{\sigma^2_{n_7}\Big)g^2_{m_7} + g_{m_8}\sigma^2_{n_8}\Big)\frac{1}{g_{ds_7} + g_{ds_8}}}_{\text{NF STAGE 3}}.$$

It could be noted that the noise from the first stage is multiplied by the gain of consecutive stages, therefore one should design the first stage for lowest noise and highest gain, so as to maximize the signal swing early in the signal chain. Section 4.3.2 provides an in-depth discussion on the issue.

C

Principal ADC Timing Diagram

A more detailed timing diagram of the ADC is shown in Fig. 4.11. Note: absolute time units shown are different from the fully optimized sequencer.

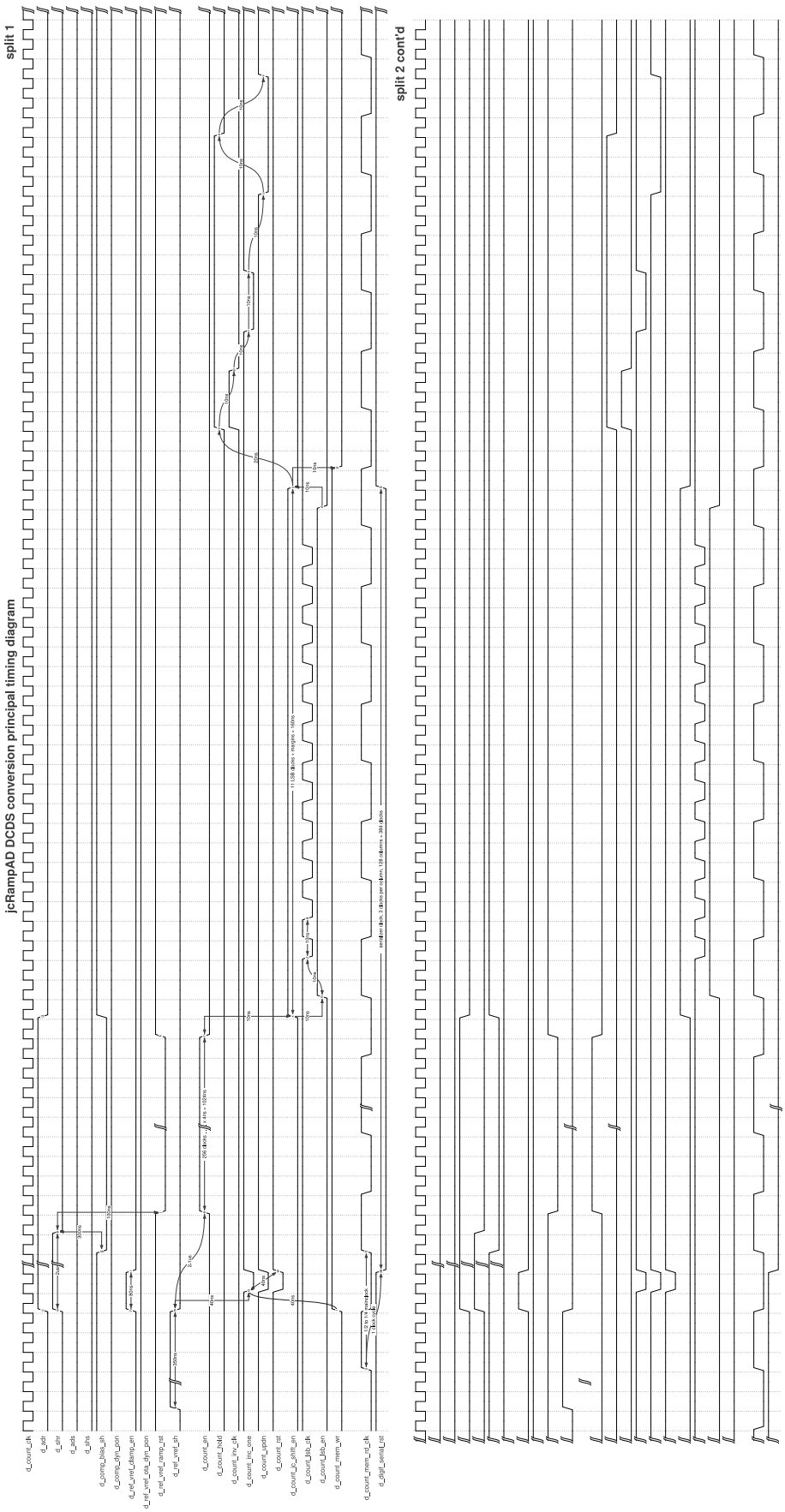


Figure C.1: Principal timing diagram

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