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Optimizing Interface Dielectric Loss in Superconducting Coplanar Waveguide Resonators for Improved Quantum Circuit Coherence

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Abstract

Superconducting quantum computing systems, including coplanar waveguide (CPW) resonators and qubits, are highly susceptible to energy dissipation from two-level systems (TLS) within bulk and interfacial dielectrics. CPW resonators serve as an ideal platform for characterizing these material losses at the single-photon excitation level. Building on recent experimental evidence that interface engineering can mitigate TLS losses, this study employs simulations to evaluate resonator quality factors across various interface modifications. Our results demonstrate that reducing losses at the substrate–air (SA) interface can increase the internal quality factor Q_i by up to three orders of magnitude. While etching the SA interface also enhances Q_i, material loss remains the dominant dissipation mechanism. Furthermore, we find that other lossy interfaces have a significantly smaller impact on the quality factor compared to the SA interface. These simulation results align with established experimental findings, providing a robust framework for refining resonator design. This work offers precise guidelines for TLS mitigation, essential for enhancing coherence times and developing more reliable superconducting quantum processors.

Keywords: simulation of superconducting quantum chip; two-level system (TLS) losses; CPW resonators

Received: 29 November 2025
Revised: 23 January 2026
Accepted: 4 February 2026
Published: 18 February 2026

1. Introduction

Quantum computing and information processing represent a transformative approach to computational challenges beyond classical limits [1]. While various technologies, such as trapped ions, photonics, and topological qubits [2–4], have shown potential, superconducting quantum circuits have emerged as particularly promising due to their scalability and integration with established microfabrication techniques [5]. Superconducting circuits offer key advantages, including fast gate times and compatibility with microwave resonators, making them essential for complex computational tasks and quantum error correction in processing architectures [6,7]. However, superconducting qubits face significant challenges to maintain coherence, primarily due to interactions with their environment that destabilize

quantum states. Decoherence in superconducting qubits results from factors like nonequilibrium quasiparticles, magnetic flux noise, phonon interactions, and two-level systems (TLS), each impacting qubit stability [8–10]. Among these, TLSs present the most substantial challenge [11–13], typically originating from oxide and defects at metal–substrates interface [9,14]. TLS defects couple with the electromagnetic fields in qubits, leading to energy loss that directly impacts coherence times [11]. Notably, TLS-related losses correlate with oxide presence at air interfaces [15,16], so reducing oxide thickness can improve quality factors in resonators, resulting in suppressed TLS-related decoherence.

TLS detection typically involves spectroscopic analysis and time-domain measurements, which assess the impact of material quality on performance [17,18]. Coplanar waveguide (CPW) resonators are a central component in many superconducting qubit architectures, and also provide a flexible stand-alone vehicle for characterizing microwave frequency material losses in the single quantum excitation regime [9,18,19]. Enhancing the quality factor of these resonators through geometric modifications or surface treatments leads to better qubit coherence [17,20,21]. Several approaches have been explored to minimize TLS losses, enhance substrate preparation [22,23] to reduce TLS at the substrate–metal (SM) interface, and eliminate chemical residues [24]. Engineers have also redesigned qubits and resonators to minimize the influence of electromagnetic (EM) fields on surrounding material interfaces, all in the pursuit of reducing TLS-related losses [25,26]. These efforts have led to notable improvements, with coherence times exceeding 50 μs [27] and planar CPW resonators achieving an unprecedented internal quality factor (Q_i) over 9 million, even at single-photon energy levels [28]. Tantalum (Ta) has recently demonstrated coherence times of 0.5 ms [29]; however, losses due to TLS remain a persistent challenge in superconducting circuits. Prior research has investigated minimizing interface losses through the implementation of shadow evaporation and hydrofluoric acid (HF)-based etching. These techniques effectively remove metal- and silicon-oxides at the metal–air (MA) and substrate–air (SA) interfaces [23,30]. Nevertheless, these methods can inadvertently induce oxide regrowth, which reintroduces decoherence and negatively impacts long-term device stability [15]. Furthermore, the application of non-oxidizing metallic capping layers, such as gold (Au) [31,32], titanium nitride (TiN) [33], magnesium (Mg) [34], and ruthenium (Ru) [35], to superconducting MA interfaces has proven effective in reducing TLS density in superconducting resonators. Surface treatment using ion beam treatment [36,37] has been reported to reduce or control oxide growth. Additionally, substrate etching has been reported to improve coherence by cleaning and modifying the geometry of the resonators [23,27]. However, while these methods typically address the MA interface, they may still be susceptible to oxidation and other surface-related issues at the SA interface. Concurrently, self-assembled monolayers (SAMs) have emerged as a promising approach for suppressing oxide growth at both MA and SA interfaces [38,39]. This suppression has been shown to enhance the Q_i of CPW resonators. SAMs, therefore, offer a versatile and adaptable solution applicable to a range of materials [40,41], ensuring long-term protection and improved performance across diverse quantum circuit designs. These results demonstrate the availability of numerous strategies for mitigating TLS losses through interface modification with additional materials. In the initial two decades of superconducting circuit development, various techniques were explored to reduce TLS losses. However, minimal interface treatment with any additional material was often preferred due to the prevailing assumption that such materials, potentially due to lattice mismatch, would inevitably increase TLS density. Recent experimental findings have challenged this assumption, demonstrating that interfaces can be effectively modified with various materials to reduce TLS losses. The introduction of additional layers at different interfaces in quantum circuits presents a new avenue for experimentalists. However, experimentally

testing a wide variety of materials in numerous configurations poses a significant challenge, requiring dilution refrigerators, specialized measurement expertise, and substantial time investment. With these new possibilities, simulations have become increasingly important. Relatively rapid simulation results can provide experimentalists with valuable insights for designing targeted experiments with specific parameters.

CPW resonators are essential for qubit state readout and manipulation, and they serve as a platform for studying TLS losses under various interface treatments [18,19]. In this study, we utilized simulations of CPW resonators to investigate the impact of lossy materials at three distinct interfaces, MA, SA, and SM, on the resonator's Q_i. Notably, all Q_i simulation results presented correspond to the same 8-CPW resonator design previously employed by our experimental collaborators and ourselves [15,39,42]. Using Ansys HFSS, we simulated the 8-CPW resonator chip to analyze the effects of TLS-related losses on Q_i. By varying the loss, thickness, and location of lossy materials (dielectrics/oxides) in the simulations, we aimed to determine how these parameters influence Q_i. We find from simulations that certain lossy interfaces have a dominant effect on Q_i at specific locations compared to others, and these simulation results align with recent experimental findings.

Furthermore, we implemented a deep substrate etching simulation technique, which demonstrably improved Q_i by minimizing dielectric losses at critical interfaces, indicating a significant reduction in TLS-related losses. Our simulations revealed that minimizing losses at the SA interface yielded the greatest improvement in Q_i, while the MS interface showed minimal impact within the investigated range of lossy material parameters. Given the time-consuming nature of experimental Q_i measurements, these simulation results can guide experimentalists in selecting and testing new, less lossy materials of specific thickness at specific interfaces. SAMs represent a promising approach for reducing lossy oxides at the SA and MA interfaces [38,39], and accurate loss information for specific SAMs obtained through simulations can unlock new avenues for experimentalists to mitigate TLS losses. Although the simulation of the quality factor of CPW resonators has been previously reported [38,43–45] and supported by experimental data, this comprehensive simulation study of lossy materials at different interfaces including deep etching can be a valuable resource for experimentalists, facilitating more detailed loss simulations in the future, especially with the recent advancements in additional material deposition at various CPW resonator chip interfaces.

2. Design and Simulation

We modeled actual 8-qubit chip geometry into a simulation model, focusing on the 8-resonator section coupled via a bus structure (Figure 1a–c). For the simulation, we used a silicon substrate and superconducting aluminum (Al), as shown in Figure 1e. Figure 1a shows an optical image of the actual chip, and Figure 1b provides a schematic representation. This particular design was chosen strategically for our simulations and for investigating two-level system (TLS) losses at the resonator interfaces. This design has been experimentally validated [15,39,42], ensuring its reliability and consistency in real-world applications. For simulation of the CPW resonators, we removed other chip components from the chip, as shown in Figure 1c. The resonators, numbered 1 through 8, each have a different resonant frequency within the range of 6 to 7 GHz. The chip is designed on a 10 mm $\times$ 10 mm square silicon (100) substrate, consisting of eight quarter-wave ($\lambda/4$) resonators. These frequencies are below the energy threshold required to break Cooper pairs responsible for superconductivity and lower than K_B, the thermal energy, ensuring that no thermal excitations disturb the system. This setup allows for a precise investigation of material losses.

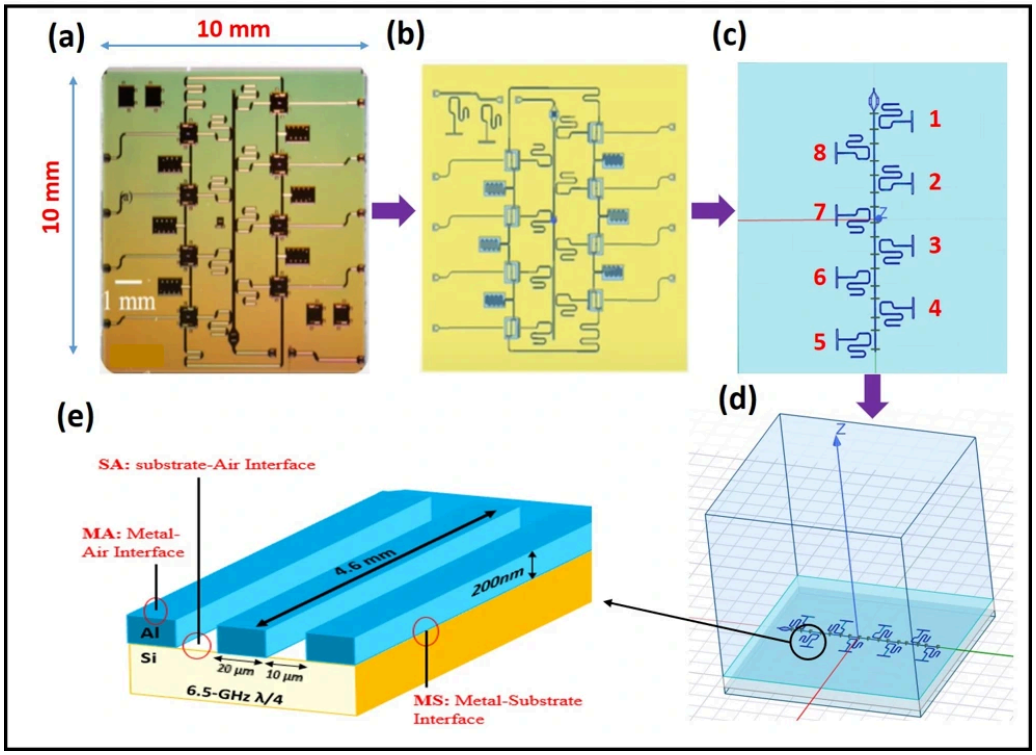

Figure 1. (**a**–**c**) Conversion of the actual 8-qubit chip geometry into a simulation model, focusing on the 8-resonator section coupled via a bus structure. (**d**) Model geometry, including the presence of a sample box used to simulate environmental effects during the analysis. (**e**) Schematic representation of a quarter-wavelength (λ/4) CPW resonator, showing its key parameters and the interfaces where TLS loss occurs. One end is open, and the other is shorted.

The resonators are fabricated on a 674 μm thick low-temperature silicon substrate, chosen for its mechanical rigidity and high relative permittivity of 11.57. This selection ensures minimal energy loss and efficient confinement of electromagnetic fields; high-resistivity silicon substrates exhibit an extremely low loss tangent at millikelvin (mK) temperatures and GHz frequencies. To excite the resonators, they are coupled to a single waveguide port, a device designed to guide electromagnetic waves in a specific direction. A rectangular transmission waveguide is utilized to confine and direct the microwave signals with precision, ensuring minimal energy leakage and efficient transfer of electromagnetic energy into the resonators, thereby enhancing their overall performance.

After constructing the resonator model in Ansys-HFSS, the chip was placed in a vacuum box measuring 10 mm × 10 mm × 10 mm on top, and a 10 mm × 10 mm × 0.4 mm vacuum region was included below the substrate, as illustrated in Figure 1e, which was used solely to define electromagnetic boundary conditions and prevent artificial field confinement at the simulation boundaries. All simulations are performed using the HFSS eigenmode solver, which is appropriate for extracting resonance frequencies and quality factors without external excitation. The eigenmode analysis is carried out over a frequency range of 5–9 GHz, with adaptive refinement enabled (maximum number of adaptive passes = 30, maximum delta frequency per pass = 1%, convergence based on the real part of the eigenfrequency).

Figure 1d illustrates the side view of the resonators on the chip, showing one end grounded (shorted) and the other end open. We kept the edges of the CPW resonators vertical in our simulation to simplify the process. Although achieving perfectly vertical edge resonators is difficult, deliberate over- and under-etching can have a considerable effect on the Q_i of the CPW resonators [19]. This resonator operates at 6.5 GHz, with a

characteristic impedance of 50 Ω and a length of 4.6 mm. The center conductor is 20 µm wide with 10 µm insulating gaps. A 200 nm thick superconducting layer, modeled as a perfect conductor with layered impedance boundary conditions, represents the actual superconductor. The resonator interfaces, including those between the superconducting layer and the silicon substrate or air, are key sources of TLS losses, which significantly impact the resonator's quality factor and overall performance. Addressing these TLS losses is a primary focus in enhancing the coherence time of qubits and a major objective of this study as well.

Finite-element simulators like Ansys HFSS cannot solve continuous problems directly; therefore, we must discretize our problem through appropriate meshing while preserving the accuracy of our calculations. In this framework, each mesh element is approximated by a field distribution that either is constant or follows a low-order polynomial dependence on position [46]. Following the computation of an initial solution, the mesh is iteratively refined; the solver identifies regions where the mesh is too coarse and generates a finer discretization. This adaptive process was repeated until reaching the optimized configuration shown in Figure 2a. Mesh density is a critical aspect of the simulation, as it facilitates the solver's ability to navigate smoothly over the model geometry without encountering singularities. While establishing boundary conditions is essential for incorporating physical principles into the model, creating an appropriate mesh is an engineering design step that discretizes the spatial dimensions of the problem space.

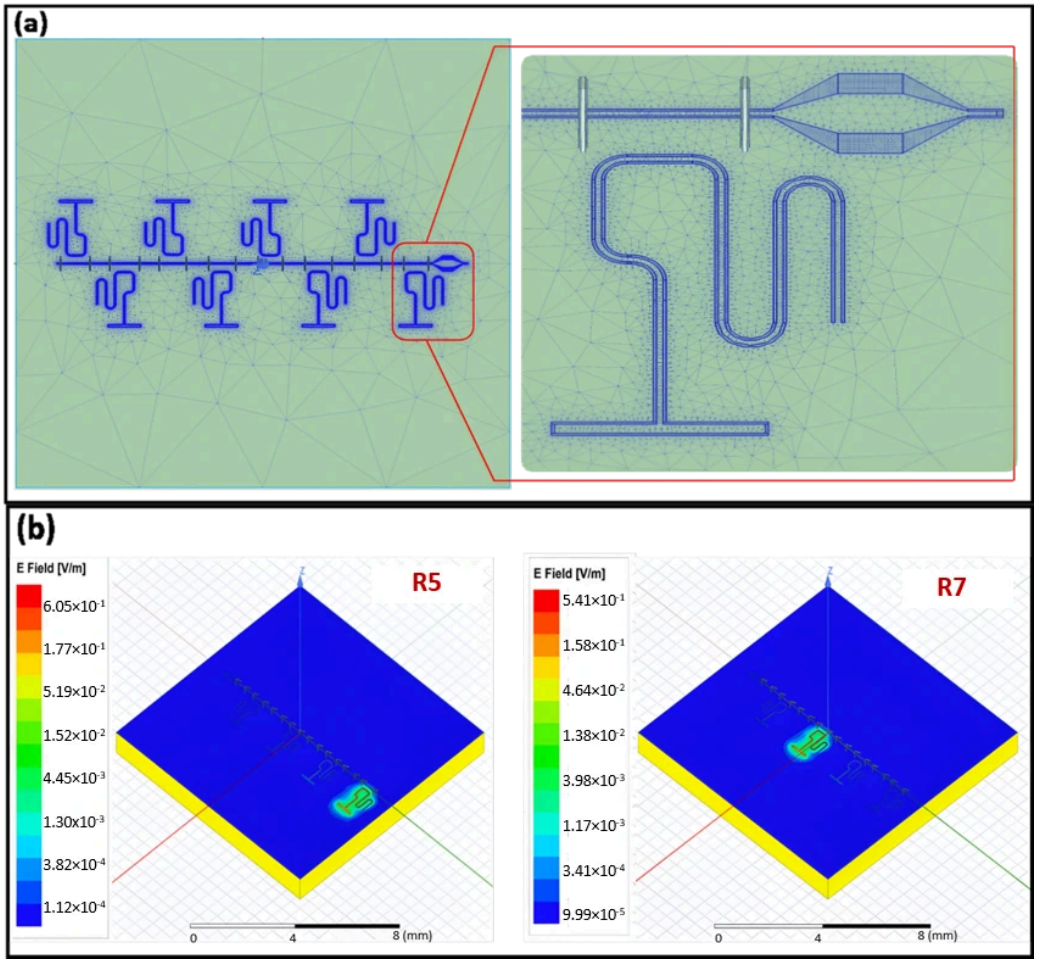

Figure 2. Typical finite-element mesh that is seeded at the start of a simulation and electric field distribution. (**a**) Mesh distribution of the model. (**b**) Electric field distribution of eigenmodes of the fifth and seventh resonator.

In our simulation, we strategically varied the mesh density based on the significance of different areas. For less critical regions, we utilized a coarser mesh to reduce computational load. However, in areas where the electric field (E-field) exhibits significant changes such as around bends or edges, where the E-field reaches its maximum, we increase the mesh density. The resonator region is discretized with a characteristic element size of 0.01 mm to accurately resolve the conductor width and gap. The coupling bus and resonator end regions—critical for defining resonance properties and boundary conditions—are meshed with characteristic element sizes of 0.02 mm and 0.04 mm, respectively. By avoiding coarse discretization in these regions, we ensure precise control over the device's simulated electromagnetic behavior. To optimize computational efficiency without compromising accuracy, a graded mesh strategy is employed: only regions distal to the resonator and bus, where fields are negligible, are meshed coarsely. This approach ensures numerical rigor across all physically significant domains, ensuring that the simulation accurately captures the effects of the changing field direction. Finally, the mesh parameters were verified through a convergence study, yielding stable resonance frequencies and quality factors upon further refinement.

Ansys HFSS solves Maxwell's equations at each mesh element, which describe how electromagnetic fields propagate and interact with materials. These equations are typically represented in their differential form, but the software reformulates them into a finite-element form suitable for numerical analysis. Specifically, HFSS converts Maxwell's equations into an eigenvalue problem, where the electric and magnetic fields can be expressed in terms of their eigenfunctions and eigenvalues. Figure 2a illustrates the mesh specifically used for calculating the eigenmodes of the fields. The eigenvalue problem arises when we seek the natural resonant frequencies of the system; the software identifies these frequencies by solving for the eigenvalues associated with the field distribution within the defined mesh. Each mesh element is treated as a small volume where the equations are approximated, and the solver iteratively refines the solutions based on the boundary conditions and material properties.

Through this process, HFSS determines the allowed resonant modes and their corresponding field distributions, providing critical insights into how the resonator will behave under specific operational conditions. Figure 2b presents the resulting field distributions at the fifth and seventh resonant frequencies, highlighting the effectiveness of our meshing strategy in capturing the complex electromagnetic behavior of the system.

The quality factor is a key indicator of a CPW resonator's performance, reflecting the number of oscillations required for the system's energy to dissipate. The internal quality factor, Q_i, measures the rate of energy loss due to parasitic environmental influences [47]. A higher Q factor indicates that the resonator can store energy for a longer period before it dissipates, which is essential for maintaining the integrity of quantum states. By reducing losses, the resonator can better preserve the quantum information encoded in the qubit. This stability directly contributes to longer coherence times, allowing qubits to perform more complex operations and maintain quantum information for extended periods [9].

In our design, we fixed the value of the coupling or external quality factor, or Q_{ex}, which represents the strength or weakness of a resonator's capacitively connected state to the transmission line. Q_t is defined as the rate at which energy held in the resonator escapes into a bigger component. From the two quantities mentioned, the internal Q_i factor can be found as

$$\frac{1}{Q_t} = \frac{1}{Q_{ex}} + \frac{1}{Q_i} \tag{1}$$

Generally, in superconducting resonators, TLS losses can be molded by incorporating an interface participation ratio p_i into the model [38]. The resonator dielectric loss is then a linear combination of the loss tangent, or dissipation factor ($\tan \delta_i$) [48], associated with

energy absorbing TLS in each region i, weighted by the fraction of the total electric field energy stored according to the following [49,50]:

$$\frac{1}{Q_i} = \sum_{\mathrm{i}} p_i \tan\delta_i \tag{2}$$

The dielectric participation ratio of region iii is defined as

$$p_i = \frac{\int_{V_i}^{a} \mathfrak{E}_i |\boldsymbol{E}|^2 dV}{\int_{V}^{a} \mathfrak{E} |\boldsymbol{E}|^2 dV} \tag{3}$$

Here, a is a dimensionless scaling parameter that represents the effective contribution of the lossy interfacial layer, incorporating both its thickness and electric-field participation in the resonator. $\mathfrak{E}_i$ is the permittivity of the region, and $\boldsymbol{E}$ is the electric field solved self-consistently in the inhomogeneous structure by HFSS. For ultra-thin oxide layers of thickness d_i resonator dimensions, modeled as boundary conditions, the thin-film approximation is used:

$$p_i \approx \frac{\int_{S_i}^{a} d_i \mathfrak{E}_i |\boldsymbol{E}|^2 dV}{\int_{V}^{a} \mathfrak{E} |\boldsymbol{E}|^2 dV} \tag{4}$$

where S_i is the interface surface. One of the fundamental properties of a particular dielectric material is dielectric loss, which is appropriately measured by the loss tangent [51]. The dielectric permittivity of a material can be written as

$$\mathfrak{E}_d = \mathfrak{E}'_d(\omega) - i\mathfrak{E}''_d(w) \tag{5}$$

where $\mathfrak{E}'_d(\omega)$ is the real part (relative permittivity), which represents the energy stored in the dielectric, and $\mathfrak{E}''_d(w)$ is the imaginary part (dielectric loss factor), which represents the energy dissipated as heat within the dielectric material. The electromagnetic field's frequency is denoted by ω and given by

$$\omega = \frac{1}{\sqrt{LC}} \tag{6}$$

A non-zero imaginary component indicates the presence of dielectric loss [47]. Thus, the loss tangent ($\tan\delta$) that quantifies the intrinsic dissipation of electromagnetic energy within a dielectric material can be determined to be

$$\tan\delta = \frac{\mathfrak{E}''_d(w)}{\mathfrak{E}'_d(\omega)} \tag{7}$$

In this work, we systematically varied these two loss parameters on different device interfaces to quantify their influence on Q_i and identify the interface most critical for improving Q_i. Gaining insight into these interface losses will facilitate enhanced control, leading to superior performance and extended coherence times in superconducting qubits.

Contaminations are modeled in simulations by adding thin layers of oxides with certain thickness and loss tangents using layered impedance boundary conditions shown in Figure 3. In this model, the layer was assigned lossy material properties of Al_2O_3/SiO_2 at various interfaces. The relative permittivity was set to $\epsilon = 9.8$, consistent with the dielectric constant of metal oxides. The relative permeability was set to 1, and the conductivity was set to zero. The model included a sweep of the loss tangent and loss thickness values. The analysis of contamination thickness demonstrates a distinct correlation with the quality factor. This correlation is intuitive: as the thickness of the contamination increases, there is

more lossy material available for the electric field to interact with, leading to a decrease in the quality factor [43].

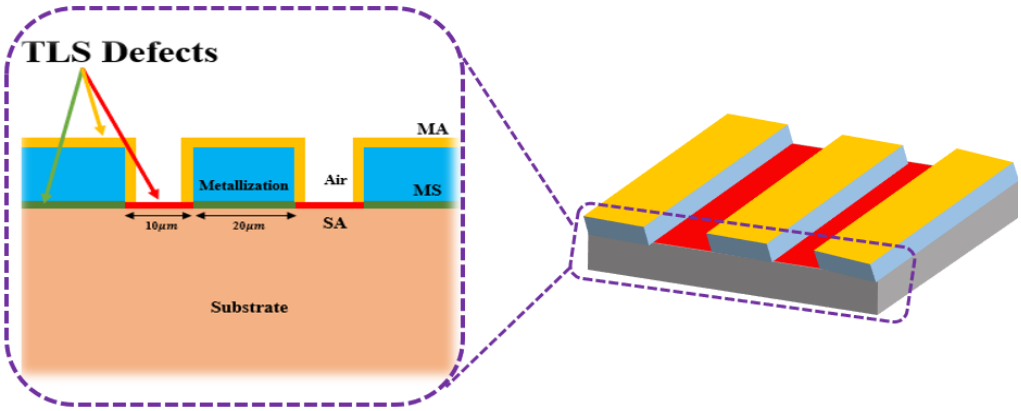

Figure 3. Typical cross-sectional sketch of CPW resonator with various interfaces highlighted. These highlighted interfaces are major hosts of TLS losses.

Initially, the external quality factor for the 8-resonator chip was calculated by setting the design to have no loss and running the simulation. In this scenario, the extracted Q_t is equal to the Q_{ex}; when there is no loss, the internal quality factor approaches infinity. This indicates that the resonator can store energy indefinitely without any dissipation. Figure 4 displays the Q_{ex} as a function of frequency for the eight resonators. The calculated frequencies for the eight resonators fall within a range similar to the design range.

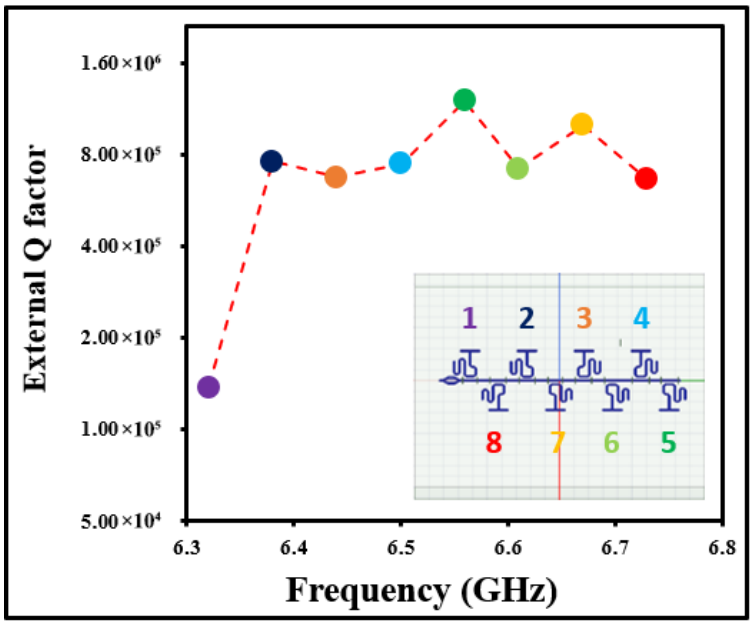

Figure 4. External quality factor of the 8-resonator chip vs. frequency. Colors represent specific resonators, as marked in the figures.

3. Results and Discussion

3.1. Substrate–Air Contamination Study

In our analysis, first, we calculated the Q_i with all three lossy interfaces, SM, MA, and SA, with $\tan\delta = 10^{-3}$ and loss thickness of 3 nm, and Q_i results are summarized in Figure 5. We then systematically removed the loss from each interface, one at a time, to assess its effect on the quality factor. The results demonstrated that eliminating contamination from the SA interface led to the most significant improvement in the Q_i, highlighting the critical

role this interface plays in minimizing losses [15,48,50,52]. These results align with our recent experimental observation [15], where we reported that the SA interface is more lossy than the MA interface. Specifically, removing oxides from the SA interface accounts for more than 50% of the reduction in TLS loss, compared to removing oxides from the MA interface, which only reduces loss by approximately 10% [15].

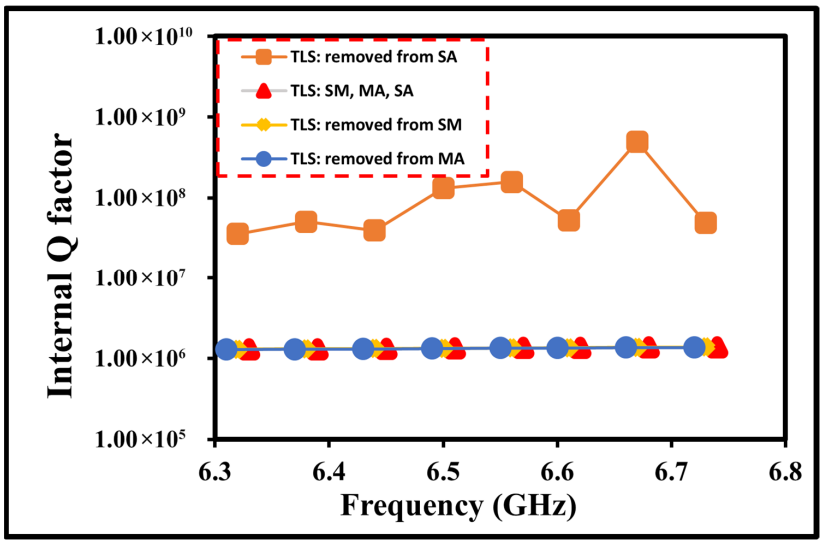

Figure 5. Internal quality factor of 8-resonator chip by removing TLS losses from each interface one at a time.

The contribution of contamination to the effective dielectric loss differs across interfaces, even when the loss tangent, loss thickness, and dielectric constant are identical. This variation arises from the unique boundary conditions the electric field encounters at each interface, resulting in distinct participation ratios and, consequently, varying effects on dielectric loss:

$$\frac{p_{MA}W}{d_{MA}} = \int_{S_{MA}}^{a} \left(\frac{\varepsilon_{air}^2}{\varepsilon_{MA}} |E_{A\perp}|^2 + \varepsilon_{MA} \left| E_{A||} \right|^2 \right) dS \tag{8}$$

$$\frac{p_{MS}W}{d_{MS}} = \int_{S_{MS}}^{a} \left(\frac{\varepsilon_{S}^2}{\varepsilon_{MS}} |E_{S\perp}|^2 + \varepsilon_{MS} \left| E_{S||} \right|^2 \right) dS \tag{9}$$

$$\frac{p_{SA}W}{d_{SA}} = \int_{S_{SA}}^{a} \left(\frac{\varepsilon_{air}^2}{\varepsilon_{SA}} |E_{A\perp}|^2 + \varepsilon_{SA} \left| E_{A||} \right|^2 \right) dS \tag{10}$$

where W is the total time-averaged energy. Since the superconductor is modeled as a perfect conductor, this enforces the boundary condition $E_{A||} = 0$. Since the oxide layer is conformal to the metal, its tangential component relative to the metal surface is also strongly suppressed. The same argument applies for the MS interface where the tangential electric field at the metal boundary is negligible due to the perfect-conductor condition. On the other hand, at the SA interface, there is no perfect conductor. The tangential field is not suppressed; in fact, CPW fields are concentrated at the substrate edges, with a significant tangential component along the surface. Therefore, both terms must be kept in Equation (10) [43].

In the next phase of the study, we maintained a constant loss layer thickness of 3 nm at the SA interface while progressively varying the loss tangent (TLS loss) from 10^{-4} to 10^{-1}, one order at a time, without introducing any losses at the other interfaces. The results summarized in Figure 6 show a remarkable transformation in the Q_i of the 8-resonator chip, with an impressive three-order-of-magnitude increase. Q_i is of the order of 10^7 for

tan$\delta = 10^{-4}$ and is approximately 10^4 for tan$\delta = 10^{-1}$. Furthermore, at a loss tangent of 10^{-3} at both the SA and MS interfaces, the Q_i was approximately 2×10^6 (blue dots in Figure 5). When this same loss tangent was present only at the SA interface, the Q_i increased to approximately 8×10^6 (green dots in Figure 6). This increase occurs because Figure 5 accounts for two lossy layers, whereas Figure 6 includes only one lossy layer. However, the order of magnitude remains the same in both cases. Therefore, TLS losses at SA interfaces are highly sensitive to the tanδ of the lossy layer; the same thickness can result in an order-of-magnitude difference in Q_i. This increase is supported by the strong electric field confinement between conducting pads close to the substrate–air interface.

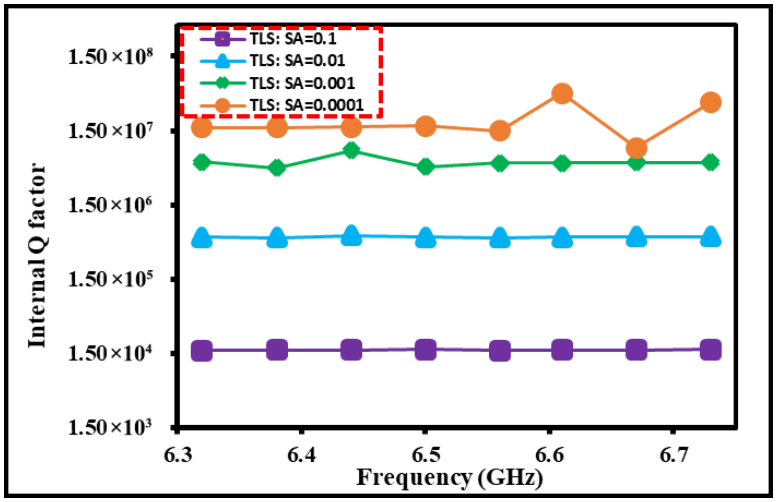

Figure 6. Internal quality factor for different loss tangents (TLS losses), 10^{-1} to 10^{-4} at the SA interface for 8-resonator chip.

To further investigate how critical the small change in tanδ at the SA interface is to the Q_i, Figure 7a,b illustrate the behavior of Q_i with a fixed loss thickness of 3 nm and incremental increases in the tanδ from 0.001 to 1.0 at the SA interface. On the other hand, the lossy layers at the MS and MA interface were fixed with tan$\delta = 10^{-3}$ and a loss thickness of 3 nm. This study provides a comprehensive view of both the internal and total quality factor improvements as a function of resonator frequency over this range for the 8-resonator chip.

The total Q_t follows a similar trajectory, though with slightly less pronounced changes due to external factors contributing to the overall losses. Figure 7c,d highlight the change in both the Q_t and Q_i with loss tangent for the first resonator specifically, serving as a representative example. The exponential response of Q_i in these curves indicates that changes in larger loss tangent values have a diminished effect on Q_i, whereas small variations at lower loss tangent values can significantly alter Q_i. While decades of research have identified low-loss-tangent materials, even minor variations can drastically affect Q_i. Therefore, meticulous control of low-loss materials is essential to maintain high resonator quality factors.

Building on these insights, we fixed the tanδ of 0.001 for both the SM and MA interfaces. We then experimented with the loss tangent at the SA interface across a lower range, from 10^{-3} to 10^{-6}. The data summarized in Figure 8 reveal that, even with fixed losses at the other interfaces, fine-tuning the TLS loss at the SA interface can dramatically boost the Q_i, highlighting the critical role of the SA interface in enhancing performance. While the significance of the SA interface on the quality factor has been experimentally reported [15,39], our results provide a more in-depth analysis and can assist researchers in designing more precise experiments with a targeted focus on the SA interface.

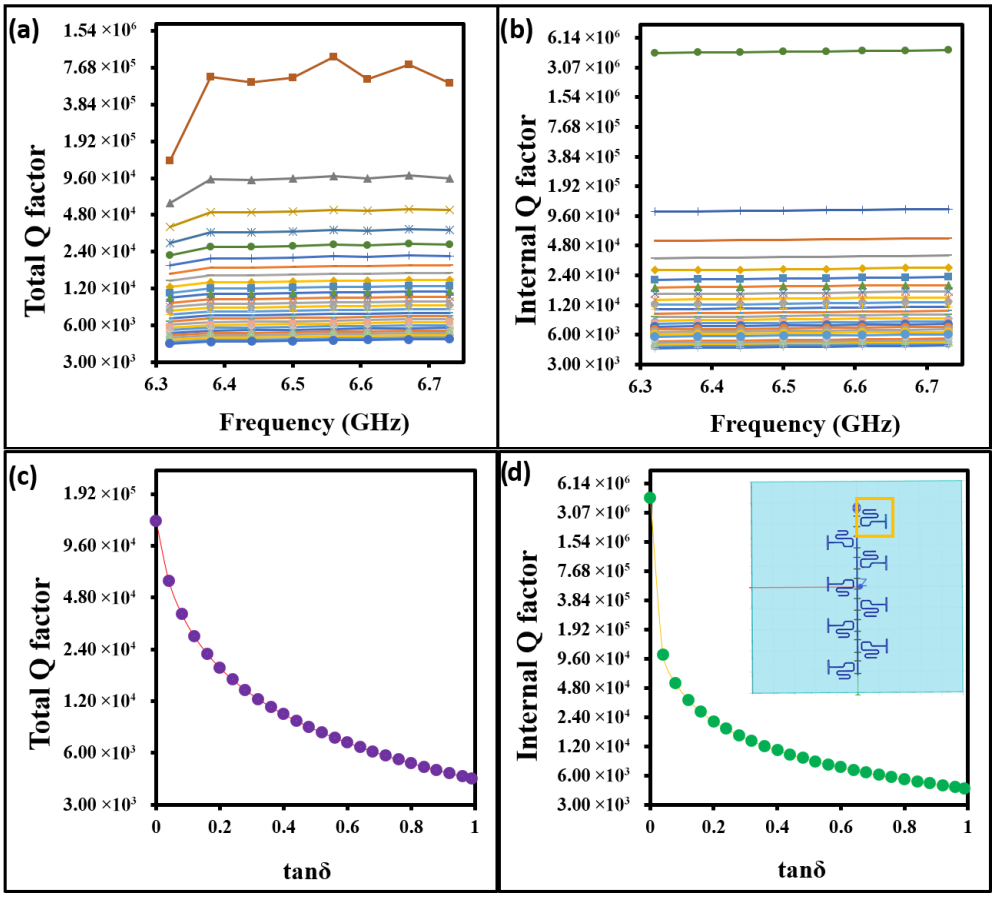

Figure 7. (**a**) Total quality factor vs. frequency for 8-resonator chip. (**b**) Internal quality factor vs. frequency for 8-resonator chip. In panels (**a**,**b**), colors from bottom to top represent regular, incremental decreases in the loss tangent. (**c**) Total quality factor improvement with reduced loss tangent (1 to 10^{-3}) for the first resonator. (**d**) Internal quality factor improvement with reduced loss tangent (1 to 10^{-3}) for the first resonator on the chip. MA, MS: tan$\delta = 10^{-3}$, thickness = 3 nm (fixed).

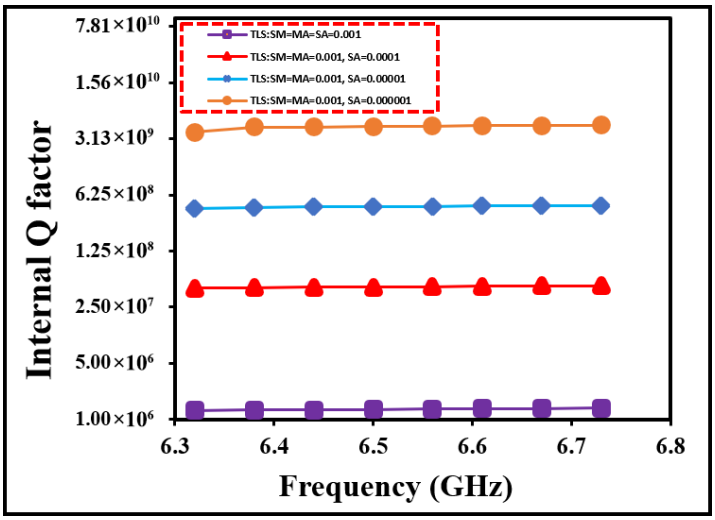

Figure 8. Improvement of internal factor when the loss at SM and MA interfaces is fixed at 0.001 while swept at SA.

Next, we will focus on understanding how the thickness of the dielectric loss layer at the SA interface impacts the resonator performance. The motivation behind varying the loss layer thickness stems from our previous experimental findings [15], which demonstrated that controlling the thickness of oxides at the SA interface plays a significant role in

determining the resonator's internal and total quality factors. For this simulation step, we fixed the MS and MA interfaces at a loss tangent of 10^{-3} and a thickness of 3 nm. We then kept the loss tangent constant at 10^{-3} for SA interface as well while progressively increasing the loss layer thickness at the SA interface from 0.5 nm to 20 nm. This approach allowed us to analyze how changes in thickness affect energy dissipation within the resonators. This step is crucial because as the dielectric layer becomes thicker, likely due to oxide growth, it may absorb more energy from the resonator's electromagnetic field, leading to higher losses and reduced quality factors. Figure 9 summarizes the results of this phase. Figure 9a,b show the effects of varying loss thickness on both the Q_i and Q_t as a function of frequency for the 8-resonator chip. Figure 9c,d shows the variation in Q_t and Q_i with loss thickness, specifically for the fifth resonator.

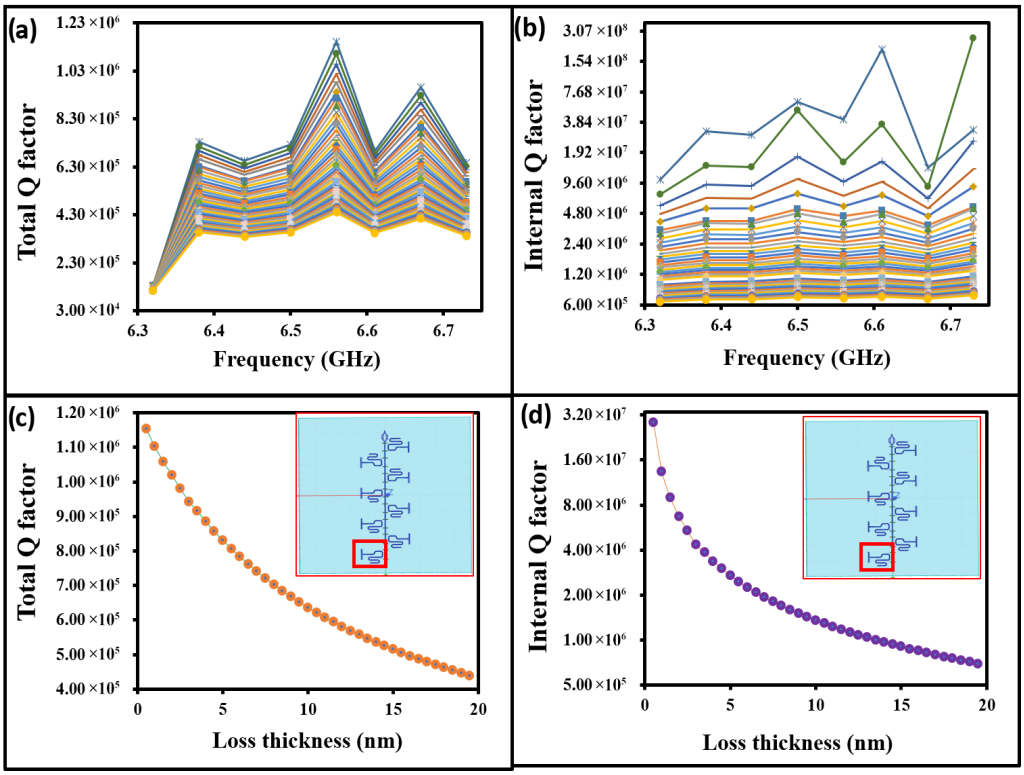

Figure 9. (**a**) Total quality factor vs. frequency with varying loss thickness (0.5 nm to 20 nm) at SA interface for 8-resonator chip. (**b**) Internal quality factor vs. frequency with varying loss thickness (0.5 nm to 20 nm) for 8-resonator chip. In panels (**a**,**b**), colors from bottom to top represent regular, incremental decreases in the loss tangent. (**c**) Total quality factor vs. loss thickness for fifth resonator. (**d**) Internal quality factor vs. loss thickness for fifth resonator. MA, MS: $tan\delta = 10^{-3}$, thickness = 3 nm (fixed).

The analysis of lossy layer thickness demonstrates a distinct correlation with the Q_i. This correlation is intuitive: as the thickness of the contamination increases, there is more lossy material available for the electric field to interact with, leading to a decrease in Q_i [48]. Crucially,Q_i exhibits an exponential dependence on thickness, meaning small variations below 5 nm can significantly alter Q_i. Experimentalists aim to minimize oxide thickness, but even minor variations in thin lossy layer thickness, such as oxide growth, can substantially reduce resonator Q_i. These results align with reported experimental findings where small oxide variations around Josephson junctions significantly impact qubit coherence time [53]. When the lossy layer thickness exceeds 6–7 nm, variations in loss become less prominent, demonstrating that the initial growth of the lossy layer is crucial. This initial oxide growth is fast and difficult to control, but its influence diminishes after a

certain thickness. Therefore, any process that minimizes this rapid initial growth, such as SAM application, could significantly reduce loss at the SA interface.

In practical CPW resonators, the SA interface usually develops stacked oxides with different oxidation states (Si^{+2}, Si^{+3}, Si^{+4}), or a high-loss native oxide capped by a lower-loss layer. Furthermore, organic SAMs have recently been employed at air interfaces to reduce TLS losses in quantum circuits [38,39]. SAMs typically bind to either surface oxides or metal atoms at these interfaces, creating a double layer. Consequently, simulations that account for this double-layer structure are highly valuable for such cases. The double-layer simulations in Figure 10 are intended to represent these experimentally relevant cases rather than arbitrary combinations.

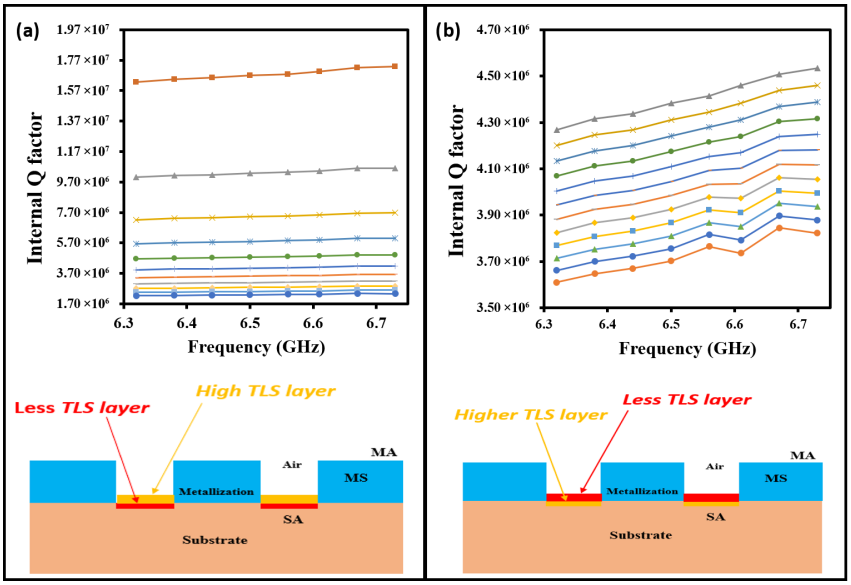

Figure 10. The internal quality factor behavior for two different configurations of lossy layers that model varying oxidation states of the substrate. (**a**) The inner layer is fixed at a thickness of 3 nm, while the upper, more lossy (higher $\tan\delta$) layer has its thickness swept between 0.5 nm and 6 nm. (**b**) The loss tangents of the two layers are reversed, making the upper layer less lossy. The thickness of the upper layer is swept over the same range (0.5 nm–6 nm). In panels (**a**,**b**), colors from bottom to top represent regular, incremental decreases in the loss tangent.

In Figure 10a, we modeled the first scenario where the outer oxide layer had a higher loss tangent of 10^{-3} and the inner layer had a loss tangent of 10^{-4}. Further, we swept the thickness of the outer, more lossy layer, while keeping the inner layer's thickness constant at 3 nm. In this case, as the thickness of the outer oxide layer increased from 1 nm to 3 nm, the Q_i showed significant reductions of one order of magnitude, from 10^7 to 10^6. This occurs because the outer, more lossy layer absorbed a greater portion of the exponentially decaying electric field energy, resulting in increased energy dissipation and a more significant impact on Q_i. These results are consistent with Figure 9, which demonstrates that when the lossy layer thickness is less than 6 nm, the loss depends exponentially on the thickness of the lossy material. In Figure 10b, we considered the opposite scenario, where the outer layer was less lossy with $\tan\delta = 10^{-4}$, while the inner layer had a higher loss tangent of 10^{-3}. Again, we varied the thickness of the outer layer while maintaining the inner layer at 3 nm. Here, the simulation results demonstrate that changes in the Q_i were much less pronounced. The lower loss tangent of the outer layer resulted in less energy absorption, and as a result, Q_i remained relatively stable, even as the thickness of the outer layer increased, staying within the range of 10^6. This narrower variation in Q_i occurs because when the less lossy layer is on the outside, it absorbs little energy and partially shields the underlying high-loss oxide.

This effect is consistent with oxidation states where stoichiometric SiO_2 (Si^{+4}) overlies more defective suboxides and reduces their effective participation. These results can be highly valuable for simulating the recently reported use of capping layers to reduce TLS losses at air interfaces [31–34].

These results illustrate that when the outer oxide layer has a higher loss tangent, it leads to larger reductions in Q_i, especially as its thickness increases. On the other hand, when the outer layer is less lossy (Figure 10b), the Q_i remains more stable, indicating that the outer layer plays a crucial role in determining overall resonator losses. These double-lossy layer simulation results support recent findings [23,30–32,38], which demonstrate that a less lossy capping layer, effectively suppressing the growth of more lossy oxides, leads to sustained improvement in quantum circuit coherence.

3.2. Substrate–Metal (SM) Contamination Study

Shifting focus to the SM interface study, we first fixed the loss layer thickness at 3 nm and varied the loss tangent between 0.001 and 1, while ensuring no losses at other interfaces. Interestingly, the quality factor remained nearly unchanged throughout this sweep, shown in Figure 11a. These results are similar to a recent study which reported that the contribution of air interfaces to TLS loss is much greater than that of the MS interface when the MS interface is oxide-free [15]. Therefore, based on these findings, we did not explore the MS interface in detail.

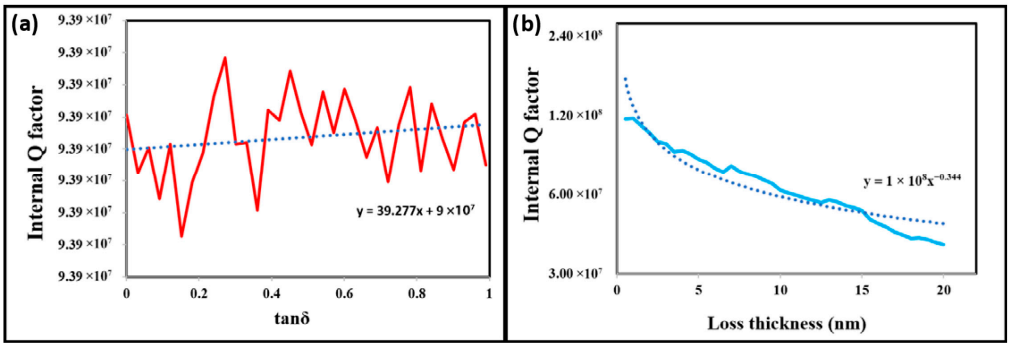

Figure 11. Simulation of lossy MS interface. (**a**) Effect of varying loss tangent at SM interface with no loss at other interfaces on the internal quality factor at fixed loss thickness (3 nm) for the first resonator. (**b**) Decrease in internal quality factor with increasing loss thickness at 0.001 loss tangent at SM interface for the same resonator. The dotted lines in (**a**) and (**b**) represent the best-fit lines and curves, respectively.

However, when we held the loss tangent constant and instead varied the loss thickness up to 20 nm, we observed a noticeable shift in the internal quality factor, indicating that thickness plays a more critical role in this scenario than the loss tangent alone (Figure 11b). The likely reason for this behavior is that at the SM interface, the electric field's interaction is less sensitive to changes in the loss tangent when the loss layer thickness is minimal, such as at 3 nm. Since the electric field strength decreases near the metal surface due to boundary conditions, small variations in the loss tangent have minimal impact on the overall dielectric loss. However, when the loss thickness increases, the interaction between the electric field and the loss layer becomes more significant, leading to a noticeable change in the internal quality factor. This suggests that at this interface, the extent of the loss layer (thickness) plays a more dominant role in influencing the quality factor than the material's loss properties (loss tangent) at thin layers. These simulation results support recent experimental findings that demonstrate a significant decrease in Q_i due to a thick amorphous MS layer [54].

3.3. Substrate–Metal and Substrate–Air Contamination Study

In our previous observations, we analyzed the impact of dielectric losses at the SA and SM interfaces individually. In the earlier study of the MS interface, we found that sweeping the loss tangent did not lead to significant improvements in the Q_i. This indicated that the SM interface had a relatively lower impact on the resonator's Q_i compared to the SA interface.

In this phase, however, we introduced varying loss thickness at both the SA and SM interfaces, ranging from 0.5 nm to 20 nm. Figure 12 illustrates these findings: panels (a) and (b) show the Q_t and Q_i for the 8-resonator system with the loss tangent swept at both the SA and SM interfaces from 10^{-1} to 10^{-3}, while panels (c) and (d) depict the variation in the lossy layer thickness between 0.5 nm and 20 nm. The observed improvement in the Q_i was less pronounced than expected. This can be attributed to the increased loss thickness affecting both interfaces, which allows the SM interface to contribute more significantly to overall losses. For the SA interface, increasing oxide thickness enhances the overlap of the electric field with the lossy layer, resulting in stronger energy absorption and a reduction in Q_i. At the SM interface, the electric field participation is weaker for very thin oxides, but as the thickness grows, more field penetrates into this region and additional dissipation occurs, likewise leading to lower Q_i. As the thickness of the lossy layer increases, the effective interaction volume of the electric field with the lossy material also grows. For the SA interface, this can lead to greater energy absorption, positively impacting Q_i up to a certain point. However, for the SM interface, the increased thickness may enhance energy absorption and dissipation, leading to higher losses. Consequently, this diminishes the overall effectiveness of the resonator, especially as energy is dissipated at both interfaces.

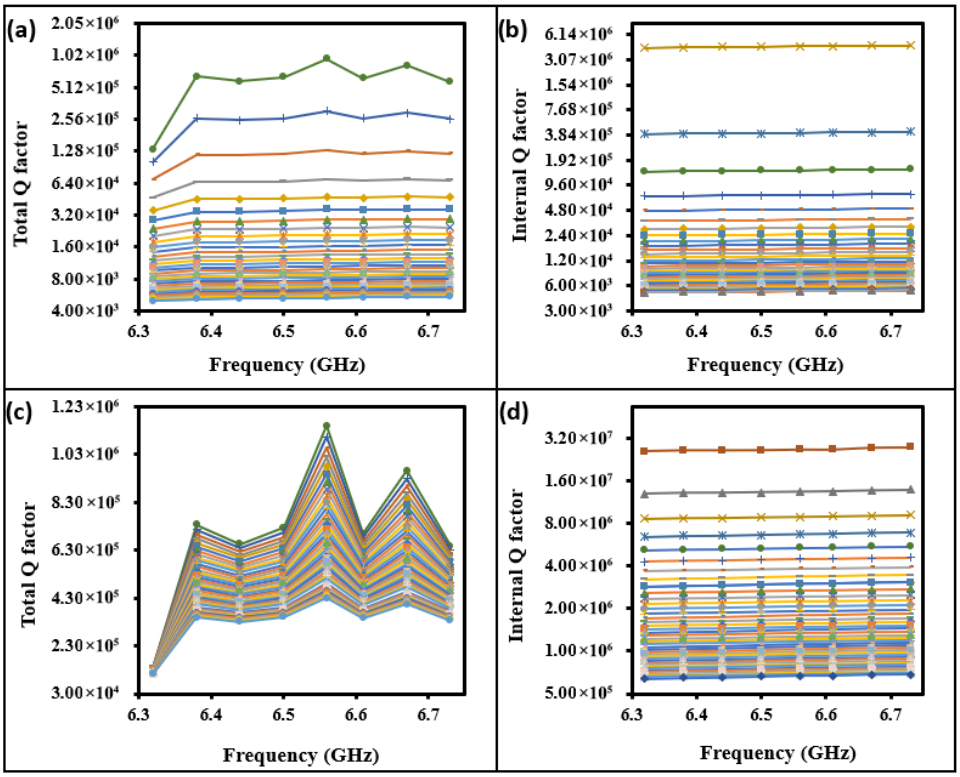

Figure 12. (**a**) Total quality factor vs. frequency for varying dielectric loss tangent at SA and SM interfaces. (**b**) Internal quality factor vs. frequency for varying loss tangent $(10^{-1} - 10^{-3})$ at SA and SM interfaces. (**c**) Total quality factor vs. frequency for varying loss thickness at SA and SM interfaces. (**d**) Internal quality factor vs. frequency for varying loss thickness at SA and SM interfaces. In panels (**a**–**d**), colors from bottom to top represent regular, incremental decreases in the loss tangent.

3.4. Trench Depth (Etching) Study

One promising strategy for enhancing the quality factor of CPW resonators and thus extending the coherence time of qubits lies in the strategic use of trench depths through substrate etching at the SA interface [23,27,30,48,55]. This method has been explored extensively in research, showcasing its ability to minimize interface participation losses, which are critical to device performance [27,55]. In addition to trench depth, our simulation also varied the loss tangent of the trench walls. Such variations are typically not achievable with capping layers [23,30–32,38]. However, recent SAM-based modifications of air interfaces [38,39] allow for the control and variation of the loss tangent of trenched air interfaces.

However, the exact relationship between trench depth and the resulting improvements in device functionality remains somewhat elusive. To unravel this complexity, we turn to our finite element model, but now we include the two reference resonators in Figure 1c integrated with a transmission line chip. This advanced modeling tool is pivotal in examining the effects of varying trench depths, allowing us to quantify how deeper etching might contribute to loss reduction in superconducting CPW resonators. Figure 13 shows the cross-section of a resonator with etching depth being added.

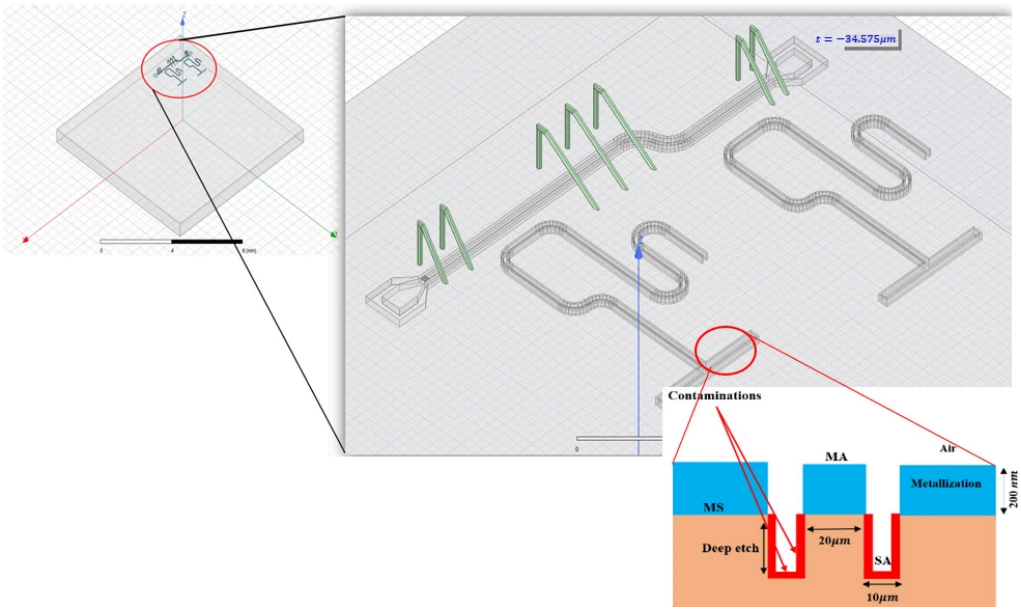

Figure 13. Tow resonator chip with cross-section of the resonator showing the deep etching.

By leveraging this model, we aim to illuminate the subtle yet significant benefits that deep trenching can offer. The predictive capabilities of our simulations will enable us to draw valuable insights into the interplay between trench depth and resonator performance. Initial findings are expected to reinforce the reliability of interface participation ratio-based models in forecasting device losses, paving the way for innovative strategies to further diminish losses in superconducting devices. In essence, this approach not only deepens our understanding of the mechanics at play but also charts a course for future advancements in the design and fabrication of high-performance quantum circuits. Due to the change in CPW resonator geometry, we began by varying the etch depth from 1 to 10 μm, calculating the external quality factor for the two resonators at each step, as shown in Figure 14. Additionally, we monitored the frequency shift, shown in Figure 15, which occurred as the etch depth increased.

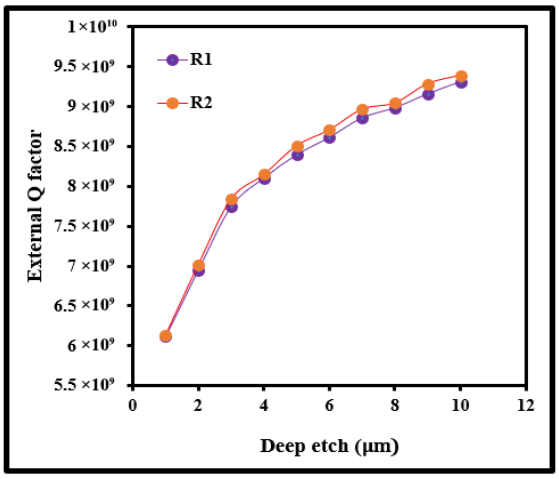

Figure 14. External Q factors for both resonators increasing with deep etching.

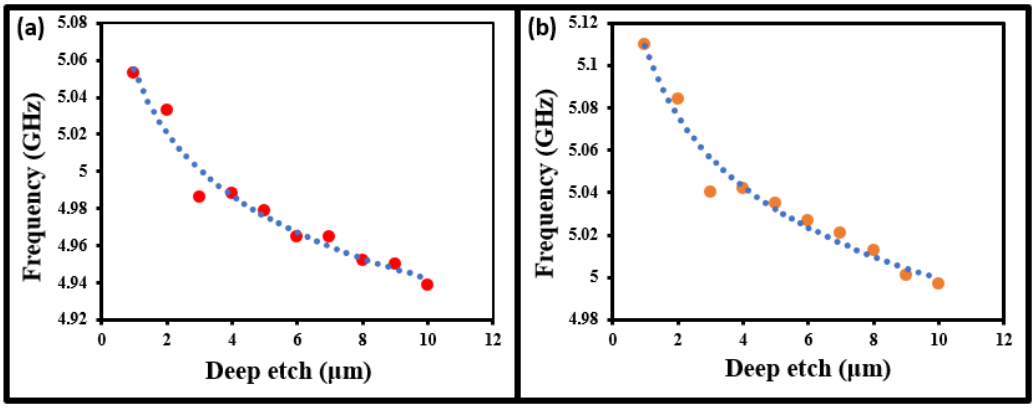

Figure 15. Frequency shift after (1–10 µm) deep etching for the (**a**) first resonator and (**b**) second resonator.

Alongside varying etch depth, we performed quality factor measurements at three loss tangent values: 0.1, 0.01, and 0.001. Figure 16 illustrates the improvement of the internal Q factor with deep etching for (a) the first resonator and (b) the second resonator, highlighting the effects of deep etching and different loss tangents. The loss thickness employed in this study was 5 nm. Notably, as the loss tangent decreased, Q_i improved by an order of magnitude with each successive reduction in the loss tangent. The improvement in the Q_i with deep etching arises because the electric field decays rapidly away from the superconductor's plane. Since dielectric loss is proportional to $|E|^2$, the increase in Q_i corresponds to the inverse of this decay, as described by Equations (2) and (3). Furthermore, the behavior of improvement Q_i up to 4 nm of etching is different from 4–10 nm because as the trench gets deeper, electric field penetration and interaction effects decrease.

Figure 16 cannot be directly compared with Figures 5 and 6 because the thickness of the lossy layer is 5 nm in Figure 16, whereas it is 3 nm in Figures 5 and 6. For a similar lossy layer thickness, the trenches showed an improvement in Q_i (figure not shown). However, we are reporting on a higher thickness, and the Q_i remains of the same order of magnitude. We reported these values because sometimes etching can result in thickness variation due to contamination if the process is not carried out carefully. These results demonstrate that such an adverse effect will not significantly degrade the Q_i.

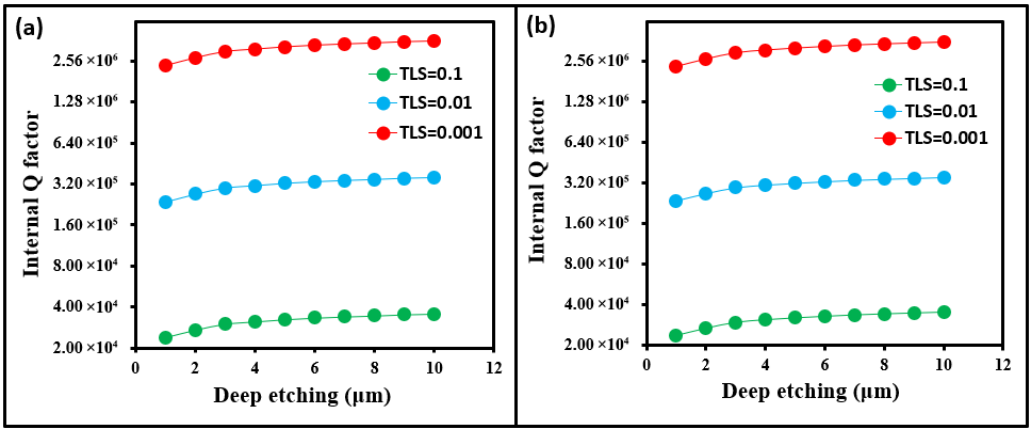

Figure 16. Improvement of internal quality factor with deep etching for different loss tangents in (**a**) first resonator and (**b**) second resonator (loss thickness: 5 nm).

To determine the etching depth at which Q_i is no longer affected, we extended our investigation by increasing the etching depth up to 100 µm, while maintaining a lossy layer thickness of 5 nm. The results for the two resonators are summarized in Figure 17. These results are similar to Figure 6, for the deep etching loss tangent of the air–interface has a similar dominant effect. However, it was observed that after reaching an etch depth of 20 µm, the Q_i showed little to no further improvement. Beyond a certain depth, the E-field's interaction with the lossy substrate diminishes, and the resonator may no longer experience significant dielectric losses. This is due to boundary conditions preventing the E-field from penetrating deeply into the trench. At shallower depths, the field is influenced by the substrate. However, as depth increases, the field remains confined within the resonator and its immediate surroundings, leading to minimal changes in Q_i once a sufficient etch depth is reached. Furthermore, the intrinsic material properties of the resonator and substrate play a dominant role. While trench depth increases Q_i, the loss tangent of the trench air interfaces has a more significant impact. Modifying these trench air interfaces is challenging, if not impossible, with conventional methods, but they can be readily altered using SAMs. Therefore, SAM-modified trenches offer a substantially greater improvement in Q_i compared to trenches alone.

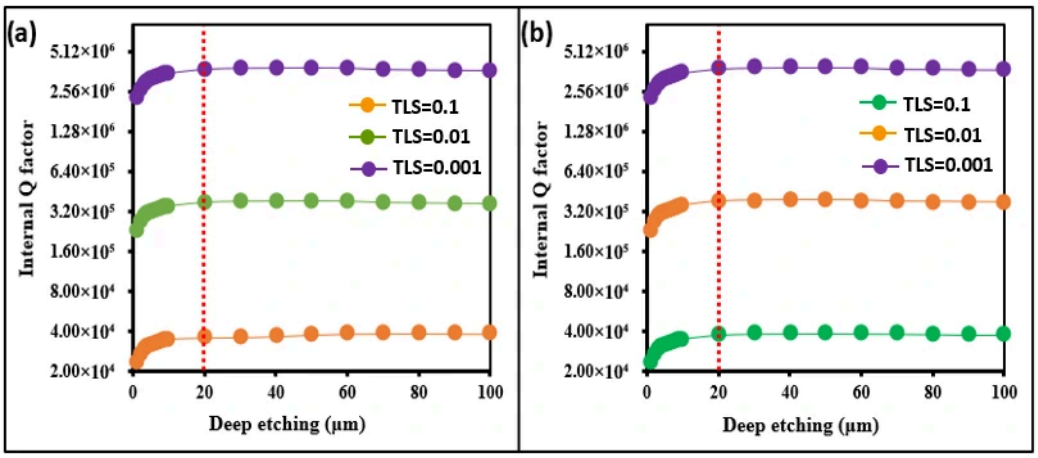

Figure 17. Deep etching up to 100 µm for (**a**) first and (**b**) second resonator with different loss tangents (loss thickness: 5 nm) showing no improvement after 20 µm.

To analyze which part of the trenched-region SA interface contributed the most to the resonator's loss, we conducted a series of targeted simulations. Initially, a loss tangent of 0.001 and a loss thickness of 5 nm were applied uniformly to both the vertical and horizontal parts of the trenched SA interface. We then compared three scenarios: (1) losses applied to both the vertical and horizontal interfaces, (2) losses removed from the vertical interface while keeping them on the horizontal one, and (3) losses removed from the horizontal interface while keeping them on the vertical one. Figure 18 shows the results of Q_i versus deep etching for the (a) first and (b) second resonator, highlighting the significant impact of removing losses from the vertical, horizontal, and both SA interfaces on the Q_i with deep etching.

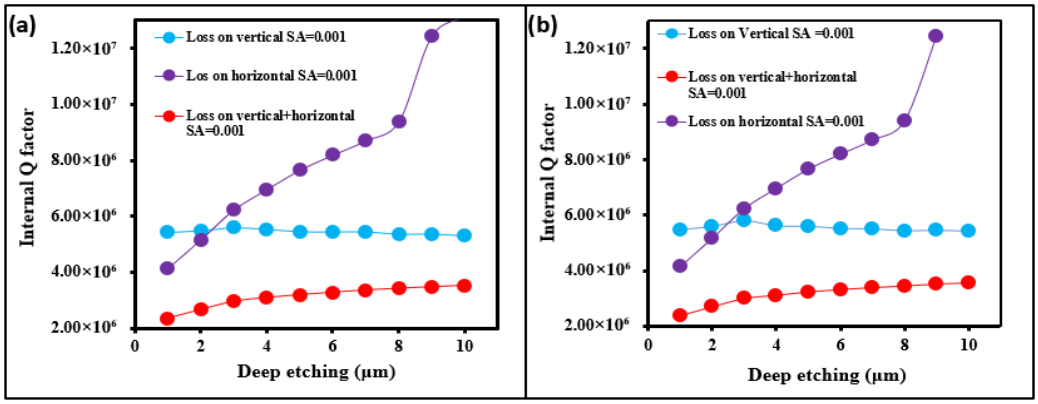

Figure 18. Q_i for (**a**) the first and (**b**) the second resonator with etching depth, comparing different loss configuration: loss on both SA interfaces, loss removed from vertical interface, and loss removed from horizontal interface (loss tangent = 0.001, loss thickness = 5 nm).

The results revealed a substantial improvement in the Q_i as the trench depth increased, particularly when the dielectric loss was exclusively removed from the vertical interface while being maintained on the horizontal surface. Under this condition, the Q_i improved by an order of magnitude as the etching depth extended up to 10 μm. This significant enhancement indicates that the vertical interface plays a more critical role in contributing to the overall losses. This disparity is attributed to the energy participation ratio, which quantifies the extent of electric field interaction with a specific material interface. The participation ratio is likely higher at the vertical interface because this region is in closer proximity to the concentrated electric field of the coplanar waveguide (CPW) resonator. Consequently, the vertical component of the superconductor–air (SA) interface participates more extensively in absorbing energy from the resonator, thereby amplifying losses. By minimizing the dielectric loss in this dominant vertical region, the resonator achieves a substantial improvement in the Q factor.

Conversely, when the loss was removed from the horizontal interface but retained on the vertical interface, the Q factor still improved compared to the reference scenario where both interfaces were lossy, but the enhancement was notably less pronounced. This comparison strongly suggests that while both interfaces influence the resonator's performance, the vertical interface constitutes the dominant source of dielectric loss, and thus mitigation efforts focused on this specific interface yield the most significant improvement in the Q factor [56].

The simulation results presented in this study clearly demonstrate that the SA interface has the greatest impact on Q_i compared to the MA and MS interfaces. These simulation results strongly support both recent and established experimental findings regarding reduction in resonator losses [15,38,39]. Efforts have focused on reducing TLS density at both MA and SA interfaces by fabricating cleaner interfaces [24–26] in addition to post-

fabrication surface treatment like nitrogen plasma and ion beam treatment [36,37]. Recently, TLS defect density has been reduced through sustained suppression of oxide growth using capping layers, leading to improved resonator Q_i [23,30–32,38]. However, these capping layers are not suitable for sustained suppression of oxide growth at SA interfaces, which exhibit the highest TLS defect density. SAMs offer a viable option for sustained oxide suppression [57], potentially reducing TLS defects at both MA and SA interfaces [38,39]. Our simulation results corroborate the observed relative improvement in Q_i when SAMs were applied to SA and MA interfaces.

Simulations of CPW resonator Q_i have predominantly been used to validate experimental data. In this paper, we present comprehensive simulations that not only replicate most reported experimental results but also extend beyond them. Furthermore, our simulations investigate the impact of loss tangent and lossy material thickness on Q_i over a broader range than previously explored experimentally. These simulation results can be used for targeted experiments, such as those involving artificial dielectrics [58] and new materials that could lead to enhanced CPW resonators Q_i. Additionally, these simulation-derived findings may facilitate the exploration of novel materials, designs, and capping layer options for improving Q_i and, ultimately, the coherence of quantum circuits.

4. Conclusions

This study provides significant insights into mitigating TLS-induced losses in superconducting CPW resonators. Through finite-element simulations, we investigated the impact on Q_i of introducing low-loss materials at various interfaces and selectively etching specific regions of the CPW resonator geometry. Our results demonstrate that targeted interface modifications with low-loss material can significantly enhance the Q_i, aligning with experimental trends reported in the literature. By systematically simulating dielectric loss layers, we identified the SA interface as a primary source of loss. Our findings show that reducing the layer thickness and optimizing the loss tangent at this interface significantly improve Q_i, thereby extending the coherence times essential for robust quantum processors. Notably, while we simulated SA interface etching up to 100µm, improvements in Q_i were saturated beyond $\sim$ 10µm. Furthermore, while increased trench depth generally enhances Q_i, losses at the trenched SA interface still remain the dominant limiting factor. These results identify the critical interface thicknesses and loss tangent ranges necessary to reduce TLS density. This provides a predictive framework for designing high-coherence quantum hardware, effectively streamlining the development process by reducing reliance on lengthy and resource-intensive fabrication and testing cycles.

Author Contributions: Conceptualization, S.G.R. and M.A.; Methodology, O.A.S., S.G.R., M.A., A.A.O. and M.F.; Software, O.A.S., M.A., A.A.O. and M.F.; Validation, A.A.O.; Formal analysis, O.A.S., S.G.R., M.A., A.A.O. and M.F.; Investigation, O.A.S. and S.G.R.; Data curation, O.A.S.; Writing—original draft, S.G.R.; Writing—review & editing, O.A.S., S.G.R., M.A., A.A.O. and M.F.; Visualization, S.G.R. and M.A.; Supervision, S.G.R. and M.F.; Project administration, S.G.R. and M.F.; Funding acquisition, S.G.R. and M.F. All authors have read and agreed to the published version of the manuscript.

Funding: The APC was funded by the Deanship of Scientific Research, King Fahd University of Petroleum and Minerals.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

Acknowledgments: Support from the KFUPM Department of Physics is gratefully acknowledged. This study was supported by the Deanship of Scientific Research, King Fahd University of Petroleum and Minerals (Grant No. INSS2408).

Conflicts of Interest: The authors declare no conflict of interest.

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